N32G032 x6/x8 Datasheet

N32G032 series based on Arm® Cortex®-M0, runup to 48MHz, up to 64KB embedded flash, 16KB SRAM, integrated analog interface, 1x12bit 1Msps ADC, 1xOPAMP, 3xcomparator, integrated multi-channel U(S)ART, I2C, SPI, CAN and other digital communication interfaces, built-in hardware acceleration engine for cryptographic algorithm.

Key features

- **Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - Run up to 48MHz
- **Encrypted memory**
  - Up to 64KByte embedded Flash memory, supports encrypted storage, multi-user partition management and data protection, supports hardware ECC verification, data 100,000 cycling and 10 years of data retention
  - SRAM of 16KB, supporting hardware parity
- **Low-power management**
  - Stop mode: RTC Run, maximum 16KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode: support 3 IO wakeup
- **Clock**
  - HSE: 4MHz~20MHz external high-speed crystal
  - LSE: 32.768KHz external low-speed crystal
  - HSI: Internal high-speed RC OSC 8MHz
  - LSI: Internal low-speed RC OSC 30KHz
  - Built-in high-speed PLL
  - MCO: Support 2-way clock output, configurable SYSCLK, HSI, HSE, LSI, LSE, and PLL clock output that can be divided.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Support watchdog reset
- **Communication interface**
  - 6xU(S)ART, with a maximum rate of 3 Mbps, of which 2 USART interfaces (support 1xISO7816, 1xIrDA, LIN), 4x UART interfaces, 2 of which support low power (LPUART, the highest communication rate in this mode is 9600bps) , Stop mode can be awakened
  - 3xSPI, up to 12 MHz, one of which supports multiplexing with I2S
  - 2xI2C, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode. Supports dual-level communication: normal level (signal level matches chip VDD) and low level (chip VDD 3.3V or 5V, signal level 1.8V) two levels can be selected.
  - 1x CAN 2.0A/B bus interface.
- **Analog interface**
  - 1x12bit 1Msps ADC, up to 16 external single-ended input channels

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- 1xOPAMP, internal programmable gain amplifier up to 32 times
- 3xCOMP, built-in 64-level adjustable comparison reference

- **Up to 56 GPIOs**
- **1xDMA, 8-channel, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **2xBeeper, support complementary output, 16mA output drive capacity**
- **Timer counter**
  - 2x16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, each timer support 4 independent channels. 3 of which support 6 pairs complementary PWM outputs
  - 2x16-bit general purpose timer counters, each timer has 4 independent channels, supports input capture/output compare/PWM output
  - 1x16-bit basic timer counters
  - 1x16-bit low power timer counter
  - 1x24-bit SysTick
  - 1x7-bit Window Watchdog (WWDG)
  - 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Hardware Divider(HDIV)and Square Root(SQRT)**
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Support AES, SM4 algorithms
  - Flash storage encryption
  - Flash storage encryption, Multi-user partition Management Unit (MMU)
  - TRNG true random number generator
  - CRC16/32 calculation
  - Support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 1.8V~5.5V
  - Operating Temperature Range: -40℃~105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - QFN32(5mm x 5mm)

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- LQFP32(7mm x 7mm)
- LQFP48(7mm x 7mm)
- LQFP64(10mm x 10mm)
- WLCSP25(2.128mm x 2.065mm)

- **Order model**

Series	Part Number
N32G032x6 N32G032x8	N32G032F6U7, N32G032F6S7, N32G032F8S7 N32G032P6W7, N32G032P8W7 N32G032K6L7, N32G032K8L7, N32G032K6Q7 N32G032C8L7 N32G032R8L7

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1 Product introduction

N32G032 family of microcontrollers features an ARM Cortex®-M0 core. Maximum operating main frequency 48MHz, integrated up to 64KB of in-chip encrypted storage Flash, supports multi-user partition permission management, maximum 16KB of embedded SRAM. It has an internal high speed AHB bus, two low speed peripherals clock bus APB and bus matrix. It supports up to 56 reusable I/ Os and provides a rich array of high performance analog interfaces, including 1x 12-bit 1Msps ADC, up to 16 external input channels, 1 independent operational amplifier, and 3 high-speed comparator. At the same time, it provides a variety of digital communication interfaces, including 6x U(S)ART, 2x I2C, 3x SPI, 1xI2S, 1x CAN 2.0B communication interface, built-in password algorithm hardware acceleration engine.

N32G032 series products can work stably in the temperature range of -40℃ to +105℃, supply voltage from 1.8V to 5.5V, provide a variety of power modes for users to choose, meet the requirements of low-power applications. This series of products are available in 20~64 pin package, according to the different package form, the device in the peripheral configuration is different.

N32G032 series microcontrollers are suitable for various application scenarios such as mobile devices, home appliance applications, motor control, balance vehicles, power management systems, etc

Figure 1-1 shows the bus block diagram of this series of products.

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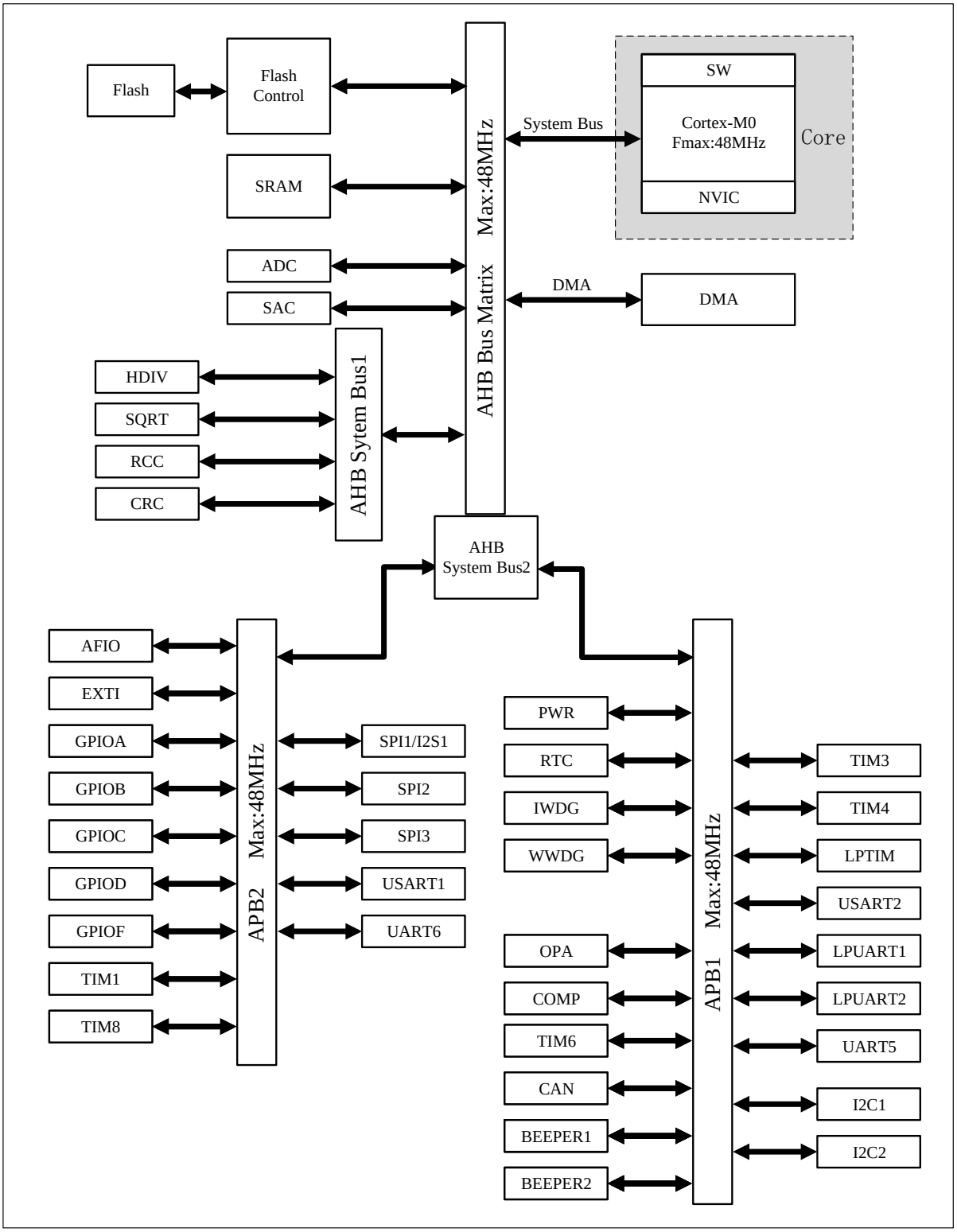
Figure 1-1 N32G032 Block Diagram



1.1 List of devices

Table 1-1 N32G032 Series devices features and peripheral list

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Part Number		N32G032 F6U7	N32G032 F6/8S7	N32G032 P6/8W7	N32G032 K6Q7	N32G032 K6/8L7	N32G032 C8L7	N32G032 R8L7
Flash capacity (KB)		32	32/64	32/64	32	32/64	64	64
SRAM capacity (KB)		8	8/16	8/16	8	8/16	16	16
CPU frequency		ARM Cortex-M0 @48MHz						
working environment		1.8~5.5V/-40~105℃						
Timer	General	2						
	Advanced	2						
	Basic	1						
	LPTIM	1						
	RTC	1						
communication interface	SPI	1			2		3	3
	I2S	1						
	I2C	2						
	USART	2						
	UART	1		2				
	LPUART	2						
	CAN	1						
GPIO		16		21	28	26	40	56
DMA Number of Channels		1 8Channel						
12bit ADC Number of channels		1 7Channel	1 9Channel	1 10Channel	1 10Channel	1 10Channel	1 10Channel	1 16Channel
OPA/COMP		1/2	1/3	1/2	1/3	1/3	1/3	1/3
Beeper		2	1	2				
Algorithm support		AES、SM4、CRC16/CRC32、TRNG						
security protection		Read and write protection (RDP/WRP), storage encryption, partition protection						
Package		UFQFPN20	TSSOP20	WLCSP25	QFN32	LQFP32	LQFP48	LQFP64

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2 Functional description

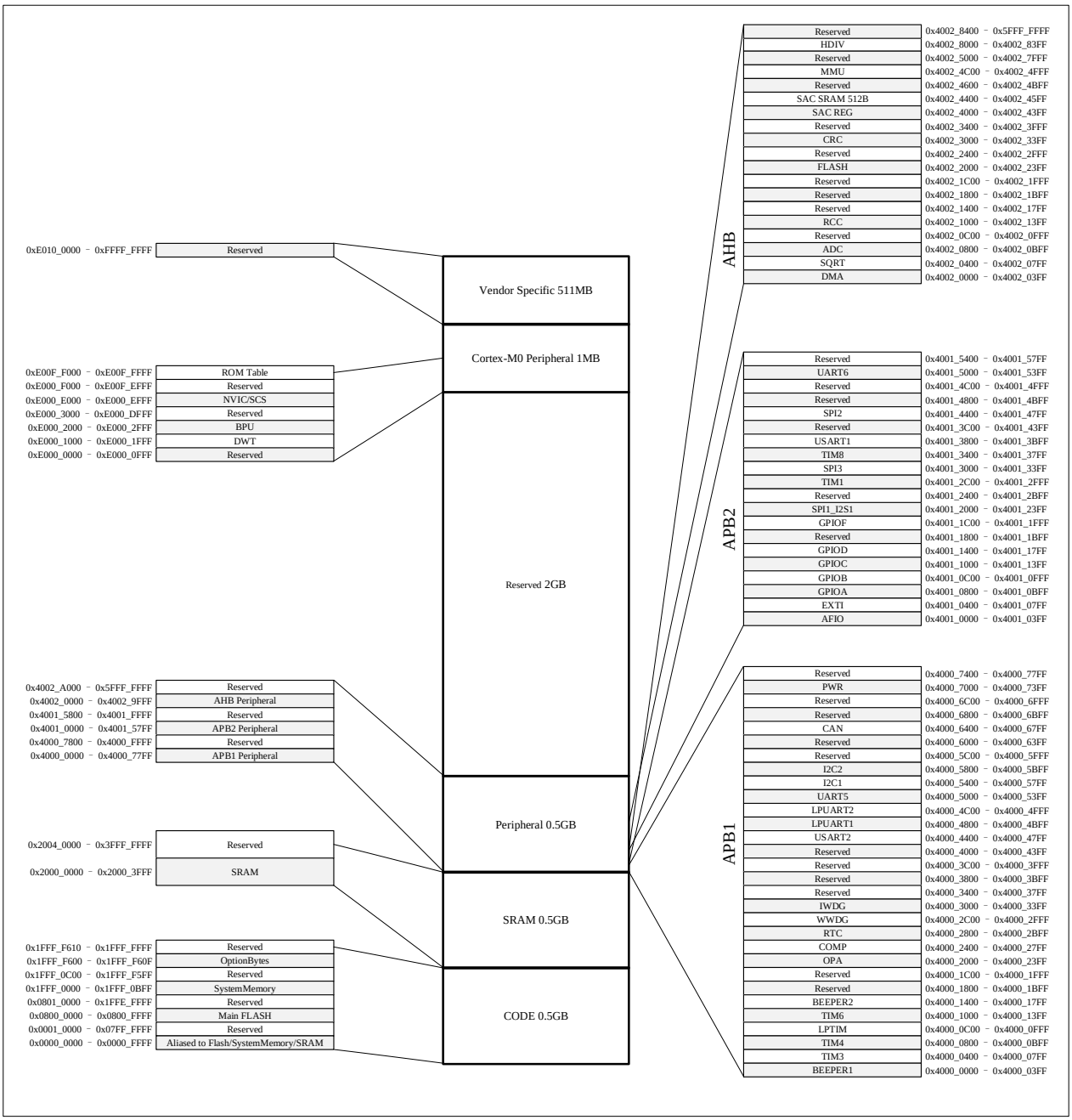
2.1 Processor core

N32G032 series integrates the latest generation of embedded ARM Cortex®-M0 processor

2.2 Storage

N32G032 series devices include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory address map



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2.2.1 Embedded FLASH memory

Integrated from 32K to 64K bytes embedded encryption FLASH (FLASH), used to store programs and data, page size of 512byte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operation).

Support user partition management, can be divided into a maximum of three user partitions, different users cannot access each other's data (only executable code).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 16K bytes. In STOP mode, SRAM can hold data.

2.2.3 Nested vectored interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is tightly connected to the interface of the kernel, which can realize low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 32 maskable interrupt channels (not including 16 Cortex®-M0 interrupt lines)
- 4 programmable priority levels (using 2-bit interrupt priority levels)
- Low-latency exception and interrupt handling
- Power management control
- Realization of system control register

The module provides flexible interrupt management functions with minimal interrupt delay

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 24 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its triggering event (rising edge or falling edge or bilateral edge) and can be individually shielded. There is a suspended register that maintains the state of all interrupt requests. The corresponding bit of the suspend register can be cleared by writing '1'.

2.4 Clock system

The device provides a variety of clocks for users to choose from, including internal high speed RC oscillator HSI (8MHz), internal low speed clock LSI (30KHz), external high speed clock HSE (4MHz~20MHz), external low speed clock LSE (32.768khz), PLL.

The system clock (SYSCLK) can choose the following clock sources:

- HSI
- HSE
- PLL
- LSI
- LSE

Secondary clock source:

- 30KHz low-speed internal RC, which can be used as the clock source of IWDG, RTC, LPTIM and LPUART. Used to automatically wake up the system from STOP mode.
- 32.768 KHz low-speed external crystal can also be used as the clock source of RTC, LPTIM and LPUART.

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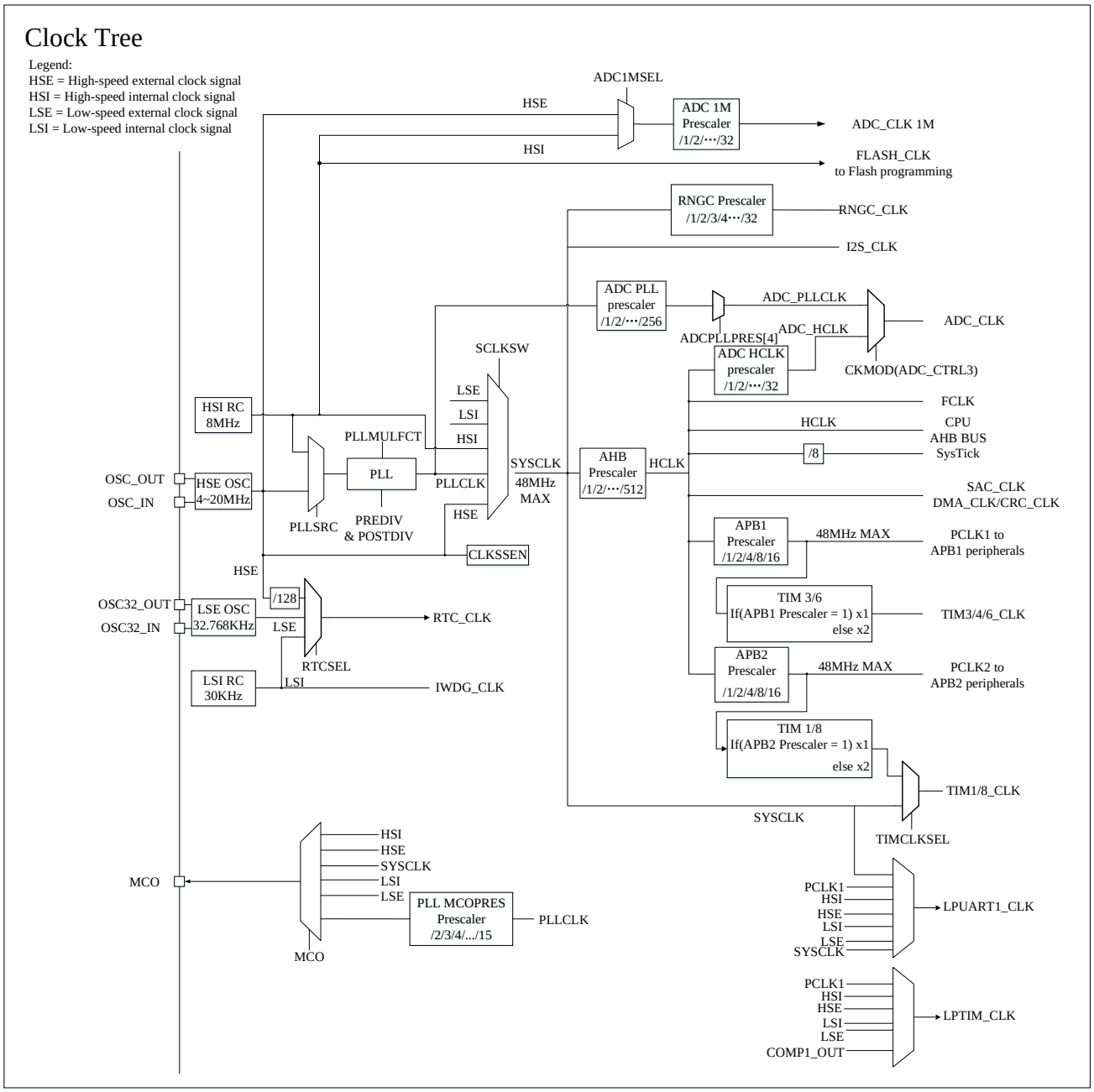
- When not in use, any clock source can be independently shut down to reduce system power consumption.

During reset, the internal HSI clock is set as the default CPU clock, and then the user can choose the external HSE clock with failure monitoring function. When HSE failure is detected, it will be isolated, the system will automatically switch to HSI, and if interrupts are enabled, the software can receive the corresponding interrupt. Also, security interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

Multiple prescaler are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. AHB has a maximum frequency of 48MHz, APB2 has a maximum frequency of 48MHz and APB1 has a maximum frequency of 48MHz.

Figure 2-2 Clock Tree



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2.5 Boot mode

At BOOT time, the BOOT mode after reset can be selected with the BOOT0 pin and option byte BOOT configuration (USER2).

- Boot from program FLASH Memory
- Boot from System Memory
- Boot from internal SRAM

The Bootloader is stored in the system memory.

2.6 Power supply scheme

- VDD area: The voltage input range is 1.8V~5.5V, which mainly provides power input for Main Regulator, IO and clock reset system.
- VDDA area: The input voltage range is 1.8V~5.5V, which supplies power for most analog peripherals. For more information, please refer to the electrical characteristics section of the relevant data sheet.
- VDDD area: The voltage regulator supplies power for the CPU, AHB, APB, SRAM, FLASH and most digital peripheral interfaces.
- PWR is the power control module of the entire device, its main function is to control N32G032 to enter different power modes and can be awakened by other events or interrupts. N32G032 supports RUN, LPRUN, SLEEP, STOP and PD modes.

2.7 Programmable voltage detector

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 1.8V. When V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device remains in the reset state. The device has a programmable voltage detector (PVD), which monitors the V_{DD}/V_{DDA} power supply and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, it will generate an interrupt. The PVD function is turned on by software.

Table 4-6 is the value reference of $V_{POR/PDR}$ and V_{pvd}.

2.8 Low power mode

N32G032 is in RUN mode after system reset or power-on reset. When the CPU does not need to run, you can choose to enter a low power mode to save power.

N32G032 has the following four low power modes:

- LPRUN mode (the system is in 32.768KHz low-frequency and low power RUN mode)
- SLEEP mode (the core is stopped, all peripherals including Cortex®-M0 core peripherals (such as NVIC, SysTick) are still running)
- STOP mode (most of the clocks are turned off, the voltage regulator is still running in low power mode)
- PD mode (V_{DDD} power down mode, V_{DD} retention, 3 WAKEUP IO and NRST can wake up)
- In addition, the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses

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- Optional configuration of PWR_CTRL4.STBFLH in RUN mode allows FLASH to enter deep standby mode. When exiting, the system needs to wait about 10us before re-accessing FLASH

2.9 DMA

The device integrates a flexible general-purpose DMA controller that supports 8 DMA channels to manage data transfers from memory to memory, peripherals to memory, and memory to peripherals.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, USART, general-purpose, basic and advanced control timers, I2S, ADC.

2.10 Real time clock (RTC)

Real Time Clock (RTC) has a set of BCD timers/counters that independently count continuously. Under the corresponding software configuration, the function of calendar can be provided. The RTC also provides two programmable alarm clock interrupts.

Two 32-bit registers contain decimal format (BCD) for subsecond, second, minute, hour (in 12 or 24 hour format), day of the week, day (date), month, and year.

Two 32-bit programmable alarms registers contain seconds, minutes, hours, date, day of week.

Two 32-bit programmable alarms registers contain sub-seconds.

The RTC provides automatic wake up in low power mode.

When a timestamp event or tamper detection event is enabled on GPIO, the current calendar is saved in a register.

2.11 Timer and watch dog

Up to 2 advanced control timers, 2 general-purpose timers and 1 basic timer, 1 low power timer, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low power timer:

Table 2-1 Timer function comparison

Timer	Counter resolution	Counter type	Prescaler	Generate DMA request	Capture/ Compare channel	Complementary output
TIM1 TIM8	16-bit	Up Down Up/Down	Any integer between 1~65536	support	4	support
TIM3 TIM4	16-bit	Up Down Up/Down	Any integer between 1~65536	support	4	Unsupported
LPTIM	16-bit	Up	1/2/4/8/16/32/64/128	Unsupported	0	Unsupported
TIM6	16-bit	Up	Any integer between 1~65536	support	0	Unsupported

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2.11.1 Basic timer -TIM6

The basic timer contains a 16-bit counter.

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- The events that generate the interrupt/DMA are as follows:
  - Update event

2.11.2 General-purpose timer (TIM3/TIM4)

There is a built-in general-purpose timer (TIM3/TIM4) that can run synchronously. Both timers are completely independent, each with a 16-bit auto-loading increment/decrement counter, a 16-bit prescaler, and 4 independent channels. The general-purpose timers (TIM3/TIM4) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Up to 4 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- Timer can be controlled by external signal
- Timers are linked internally for timer synchronization or chaining
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.11.3 Low Power Timer (LPTIM)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for PD mode. LPTIM can run without internal clock source, it can be used as a "Pulse Counter". Also, the LPTIM can wake up the system from low-power modes, to realize "Timeout functions" with extreme low power consumption.

LPTIM introduces a flexible clocking scheme that provides the required functionality and performance while minimizing power consumption.

Main features of the low power timer:

- 16-bit up-counter
- 3-bit clock prescaler, 8 dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources
  - Internal: HSI, HSE, LSI, LSE, APB1 and COMP1_OUT clock

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  - External: External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for pulse counter applications)

- 16-bit auto-reload register
- 16-bit compare register
- Continuous/One-shot counting mode
- Programmable software and hardware input trigger
- Programmable digital filter for filtering glitch
- Configurable output: Pulse, PWM
- Configurable I/O polarity
- Encoder mode

2.11.4 Advanced-control timers (TIM1 and TIM8)

Two independent advanced timers (TIM1/TIM8), each consisting of a 16-bit auto-load counter driven by a programmable prescaler. A variety of functions are supported, including measuring the pulse width of an input signal (input capture), or generating an output waveform (output compare, PWM, complementary PWM output with embedded dead time, etc.). Using a timer prescaler and an RCC clock-controlled prescaler, pulse widths and waveform periods ranging from a few microseconds to a few milliseconds can be realized. Each timer is completely independent and does not share any resources with each other.

The main functions of the advanced timer:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Supports up to 48Mhz as the timer input clock;
- Up to 4 separate channels:
  - Input capture;
  - Output comparison;
  - PWM generation (edge or middle alignment mode);
  - Single pulse mode output;
- PWM triggered ADC sampling:
- The trigger time point is software-configurable throughout the PWM cycle.
- Dead-time programmable complementary output;
- Use an external signal to control the timer or the synchronization circuit when multiple timers are connected;
- Allows the repeat counter of the timer register to be updated after a specified number of counter cycles;
- Break Input signal. The output signal of the timer can be set to the reset state or a known state;
- An interrupt /DMA occurs when the following events occur:
- Update: Counter overflow up/overflow down, counter initialization (triggered by software or internal/external);
- Trigger events (counters start, stop, initialize, or count internally/externally triggered);
- Input capture;
- Output comparison;
- Break signal input;

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- Support for incremental (orthogonal) encoders and Hall sensor circuits for positioning;
- Triggers the input as an external clock or periodic current management

In debug mode, the counter can be frozen while the PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Many of the functions are the same as standard TIM timers, and the internal structure is the same, so advanced control timers can operate in conjunction with TIM timers through the timer link function to provide synchronization or event link functions.

2.11.5 Systick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard decrement counter.

- It has the following characteristics:
  - 24-bit decrement counter
  - Automatic reloading function
  - A maskable system interrupt is generated when the counter is 0
  - Programmable clock source

2.11.6 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit decrepit counter and a 3-bit predivider. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the decline counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit decrement counter value (in the control register) is flushed before the decrement counter reaches the window register value, then an MCU reset will also occur. This indicates that the decrement counter needs to be refreshed in a finite time window.

- Main features:
  - WWDG is driven by the clock generated after the APB1 clock is divided.
  - Programmable free-running decrement counter;
  - Conditional reset:
    - When the decrement counter is less than 0x40, a reset occurs (if the watchdog is started);
    - A reset occurs when the decrement counter is reloaded outside the window (if the watchdog is started);
  - If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWI) occurs when the decrement counter equals 0x40, which can be used to reload the counter to avoid WWDG reset.

2.12 I2C bus interface (I2C)

The device integrates up to two independent I2C bus interfaces, which provide multi-host function and control all

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I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus (SMBus), and Power Management Bus (PMBus).

The functions of the I2C interface are described as follows:

- This module can be used as master device or slave device;
- I2C master device function:
  - Generate a clock;
  - Generate start and stop signals;
- Function of I2C slave device
  - Programmable address detection;
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
  - Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and broadcast calls;
- Support different communication speeds;
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz);
  - Fast + (up to 1MHz);
- Status flags:
  - Transmitter/receiver mode flag;
  - Byte transmit complete flag;
  - I2C bus busy flag;
- Error flags:
  - Arbitration is missing in Master Mode.
  - Acknowledge (ACK) error after address/data transfer;
  - Error start or stop condition detected
  - Overrun or underrun when disable extend clock function;
- One interrupt vectors:
  - Event interrupt and error interrupt share one interrupt vector
- Optional extend clock function
- DMA of single-byte buffers;
- Generation or verification of configurable PEC(Packet error detection)
  - In transmit mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25 ms clock low
  - 10 ms accumulates low clock extension time of master device

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- 25 ms accumulates low clock extension time of slave device
- PEC generation/verification of hardware with ACK control
- Support address resolution protocol (ARP)

◆ Compatible with the PMBus

◆ I2C interface supports dual signal level communication, normal level (signal level matches chip VDD) and low level (chip VDD 3.3V or 5V, signal level 1.8V) two levels can be selected.

2.13 Universal synchronous/asynchronous transceiver (USART)

N32G032 series products integrate up to 6 serial transceiver interfaces, including 2 universal synchronous/ asynchronous transceivers (USART1 and USART2) and 4 universal asynchronous transceivers (LPUART/LPUART2/UART5/UART6).

The USART1 and USART2 interfaces have hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and synchronous/asynchronous communication mode, supports for IrDA, SIR, ENDEC transmission codec, multi-processor communication mode, single-wire half-duplex communication mode, and LIN master/slave function, all of which can use DMA operations.

The LPUART interfaces have hardware CTS and RTS signal management, asynchronous communication mode, all of which can use DMA operations. LPUART can wakeup system from stop mode.

■ Main features of USART are as follows:

◆ Full duplex, asynchronous communication;

◆ NRZ standard format;

◆ Fractional baud rate generator system, baud rate programmable, used for sending and receiving up to 3Mbits/s

◆ Programmable data word length (8 or 9 bits)

◆ Configurable stop bit, supporting 1 or 2 stop bits;

◆ LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters

◆ Output sending clock for synchronous transmission;

◆ IrDA SIR encoder decoder, supports 3/16 bit duration in normal mode;

◆ Smart card simulation function;

- The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3.
- 0.5 and 1.5 stop bits for smart cards;

◆ Single-wire half duplex communication;

◆ Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer;

◆ Independent transmitter and receiver enable bits;

◆ Test flag

- Receive buffer is full
- Send buffer empty
- End of transmission flag

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- Parity control
  - Send parity bit
  - Verify the received data
- Four error detection flags;
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Ten interrupt sources with flags
  - CTS change
  - LIN disconnect detection
  - Send data register is empty
  - Send complete
  - Received data register is full
  - Bus was detected to be idle
  - Overrun error
  - Frame error
  - Noise error
  - Parity error
- Multi-processor communication, if the address does not match, then enter the silent mode;
- Wake up from silent mode (via idle bus detection or address flag detection)
- Two ways to wake up the receiver: address bit (MSB, bit 9), Bus idle
- Mode configuration:

USART modes	USART1	USART2	LPUART	LPUART	UART5	UART6
Asynchronous mode	support	support	support	support	support	support
Hardware flow control	support	support	support	support	nonsupport	nonsupport
Multi-cache Communication (DMA)	support	support	support	support	support	support
Multiprocessor communication	support	support	nonsupport	nonsupport	support	support
Synchronous	support	support	nonsupport	nonsupport	nonsupport	nonsupport
Smart card	support	support	nonsupport	nonsupport	nonsupport	nonsupport
Half duplex (single wire mode)	support	support	nonsupport	nonsupport	support	support
IrDA	support	support	nonsupport	nonsupport	support	support
LIN	support	support	nonsupport	nonsupport	support	support

2.14 Serial peripheral interface (SPI)

The device integrates 3 SPI interfaces.

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SPI allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCLK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-wire simplex synchronous transmission using a bidirectional data wire, and reliable communication using CRC checks.

- The main functions of SPI interfaces are as follows:
  - 3-wire full-duplex synchronous transmission;
  - two-wire simplex synchronous transmission with or without a third bidirectional data wire;
  - 8 or 16 bit transmission frame format selection;
  - Master or slave operations;
  - Support multi-master mode;
  - Fast communication between master mode and slave mode;
  - NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes;
  - Programmable clock polarity and phase;
  - Programmable data order, MSB before or LSB before;
  - Dedicated send and receive flags that trigger interrupts;
  - SPI bus busy flag;
  - Hardware CRC for reliable communication;
    - In send mode, the CRC value can be sent as the last byte;
    - In full-duplex mode, CRC is automatically performed on the last byte received.
  - Master mode failures, overloads, and CRC error flags that trigger interrupts
  - Single-byte send and receive buffer with DMA capability: generates send and receive requests
  - Maximum interface speed: 12Mbps

2.15 Serial audio interface (I2S)

I^2S is a 3-pin synchronous serial interface communication protocol. I^2S interfaces (multiplexed with SPI) and can operate in master or slave mode. I^2S can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8KHz to 96KHz. It supports four audio standards, including Philips I^2S, MSB and LSB alignment, and PCM.

It can work in master and slave mode in half duplex communication. When it acts as a master device, it provides clock signals to external slave devices through an interface.

- The main functions of I^2S interface are as follows;
  - Half-duplex communication (send or receive only);
  - Master or slave operations;
  - 8-bit linear programmable predivider for accurate audio sampling frequencies (8 KHZ to 96KHz);
  - The data format can be 16, 24, or 32 bits;
  - Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame);
  - Programmable clock polarity (steady state);
  - The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode;

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- 16-bit data registers are used for sending and receiving, with one register at each end of the channel;
- Supported I²S protocols:
  - I²S Philips standard;
  - MSB alignment standard (left aligned);
  - LSB alignment standard (right aligned);
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame);
- The data direction is always MSB first;
- Both send and receive have DMA capability;
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.16 Controller area network (CAN)

The device integrates a CAN bus interface compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.
Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Send:
  - Three sending mailboxes
  - The priority of sent packets can be configured by software
  - Records the timestamp of the time when the SOF was sent
- Receive:
  - Level 3 depth of 2 receiving FIFO
  - Variable filter group
  - There are 14 filter groups
  - Identifier list
  - The FIFO overflow processing mode is configurable
  - Record the time stamp of the receipt of the SOF
- Time-triggered communication mode:
  - Disable automatic retransmission mode
  - 16-bit free run timer
  - Timestamp can be sent in the last 2 bytes of data
- Management:
  - Interrupt masking
  - The mailbox occupies a separate address space to improve software efficiency

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2.17 General purpose input/output (GPIO)

This design supports 56 GPIO, divided into 5 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOF), GPIOA/GPIOB/GPIOC each have 16 pins, GPIOD has 1 pins and GPIOF has 7 pins. Each GPIO pin can be configured by software as output (push-pull or open drain), input (with or without pull-up or pull-down) or alternate peripheral function ports (output/input), most GPIO pins are shared with digital or analog reuse peripherals, some IO pins are also reused with clock pins. Except for ports with analog input function, all GPIO pins have the ability to pass through a large current.
GPIO ports have the following characteristics:

- Each GPIO port can be individually configured into multiple modes by software
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Open drain output and pull-up/pull-down can be configured
  - Push-pull output and pull-up/pull-down can be configured
  - Push-pull alternate function and pull-up/pull-down can be configured
  - Open-drain alternate function and pull-up/pull-down can be configured
- Individual bit set or bit clear function
- All IO supports external interrupt function
- All IO supports low power mode wake-up, rising or falling edge configurable
  - 16 EXTIs can be used to wake up from SLEEP or STOP mode, and all I/Os can be reused as EXTIs
  - PA0/PC13/PA2 three wake-up IO can be used for PD mode wake-up, the maximum I/O filter time is 1us
- Support software remapping I/O alternate function
- Support GPIO lock mechanism, reset the lock state to clear
- Each I/O port bit can be programmed arbitrarily, but I/O port registers must be accessed as 32-bit words (16-bit half-word or 8-bit byte access is not allowed).

2.18 Analog/digital converter (ADC)

The device supports a 12-bit 1Msps sequential comparison ADC with a sampling rate of single-ended inputs, it has up to 19 channels to measure 16 external and 3 internal signal sources.The A/D conversion of each channel can be performed in single, continuous, scan, or discontinuous mode. The ADC results can be stored left- or right-aligned in 16-bit data registers. Input clock of ADC can not exceed 18MHz.

The main features of ADC are described as follows:

- Supports 1 ADC, single-ended input, measuring 16 external and 3 internal signal sources
- Support 12-bit resolution, the highest sampling rate is 1MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 48MHz
  - PLL can be configured as a sampling clock source, up to 18MHZ, support 1,2,3,4,6,8,10,12,16,32, 64,128,256 frequency division

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- The AHB_CLK can be configured as the sampling clock source, up to 18MHz, and supports frequency 1,2,3,4,6,8,10,12,16,32
- The timing clock is used for internal timing functions and the frequency must be configured to 1MHz

- Supports timer trigger ADC sampling
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options
- discontinuous mode
- ADC power supply requirements: 2.4V to 5.5V
- ADC input range: 0≤ VIN ≤ VDDA
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion.

2.19 Operational amplifier (OPAMP)

Intergrated an independent operational amplifier with multiple working modes such as external amplification, internal follower and programmable amplifier (PGA).

The main functions are as follows:

- Support rail-to-rail input
- OPA linear output range 0.4V~V_{DDA}-0.4V
- Can be configured as independent OPAMP and programmable gain OPAMP
- Non-inverted and inverted input multiple selection
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)
  - PGA mode, programmable gain is set to 2X, 4X, 8X, 16X, 32X
  - Follower mode
- The internally connected ADC channel is used to measure the output signal of the OPAMP

2.20 Analog comparator (COMP)

The device integrates up to 3 comparators, support low power mode. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

The main functions of comparator are as follows:

- 3 independent COMP1/COMP2/COMP3, COMP1 supports low power mode(can work at LPRUN, SLEEP, STOP mode)
- Internal 64-level programmable reference input compare voltage source VREF1/VREF2.

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- Support filter clock, filter reset
- Output polarity can be configured to high or low
- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to either I/O or timer input for capturing events, OCREF_CLR events, breaking events, triggering event.
- Input channel can select I/O port/VREF1/VREF2
- Can be configured with read-only or read-write, and needs to be reset to unlock when locked
- Support blanking, blanking source can be configured
- COMP1/COMP2 can form a window comparator
- COMP can wake up the system from low power mode by generating an interrupt, and COMP1 has the ability to wake up the system from STOP. COMP1 output generate interrupt by connect to EXTI.
- Configurable filter window size
- Configurable filter threshold size
- Configurable sampling frequency for filtering

2.21 Temperature sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in the range of 1.8V <V_{DDA} <5.5V. The temperature sensor is internally connected to the ADC_IN16 to convert the output of the sensor to a digital value.

2.22 BEEPER

Beeper1/Beeper2 module supports complementary outputs and can generate periodic signals to drive external passive buzzers. Used to generate a beep or the alarm to sound.

2.23 HDIV/SQRT

The divider (HDIV) and square root (SQRT) are mainly used in some scenarios with high requirements for computing energy efficiency, and are used to partially supplement the deficiencies of the microcontroller in computing. The divider and square root calculator can perform division or square root calculation of unsigned 32-bit integers.

The main features of HDIV and SQRT are as follows:

- Only support word operation
- 8 clock cycles to complete an unsigned integer division operation
- 32-bit dividend, 32-bit divisor, output 32-bit quotient and 32-bit remainder
- Divisor is zero warning flag, division operation end flag
- 32-bit unsigned radicand integer, 16-bit square root output
- Complete an unsigned integer square operation in 8 clock cycles
- You can judge whether the calculation is complete by setting the interrupt enable or query the relevant register bits

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2.24 Cyclic redundancy check calculation unit (CRC)

Integrated CRC32 and CRC16 functions, the cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting flash memory errors, CRC cells can be used to calculate signatures of software in real time and compare them with signatures generated when linking and generating the software.

The CRC has the following features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + X^0$
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.25 Algorithmic hardware acceleration engine (SAC)

Embedded algorithm hardware acceleration engine, support a variety of international algorithms and national cryptosymmetric cryptography algorithm and hash cryptography algorithm acceleration, compared with pure software algorithm can greatly improve the encryption and decryption speed.
The hardware supports the following algorithms:

- Supports AES symmetric algorithm
  - Supports 128bit, 192bit, and 256bit keys
  - Supports CBC, ECB, and CTR modes
- Supports TRNG true random number generator
- Supports SM4 algorithm

2.26 Unique device serial number (UID)

N32G032 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of flash memory.The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G032 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory.

UCID is 128-bit, which complies with the definition of Nations chip serial number. It contains the information related to chip production and version.

2.27 Serial wire SWD debug port (SWD)

Embedded Arm® SWD Interface.

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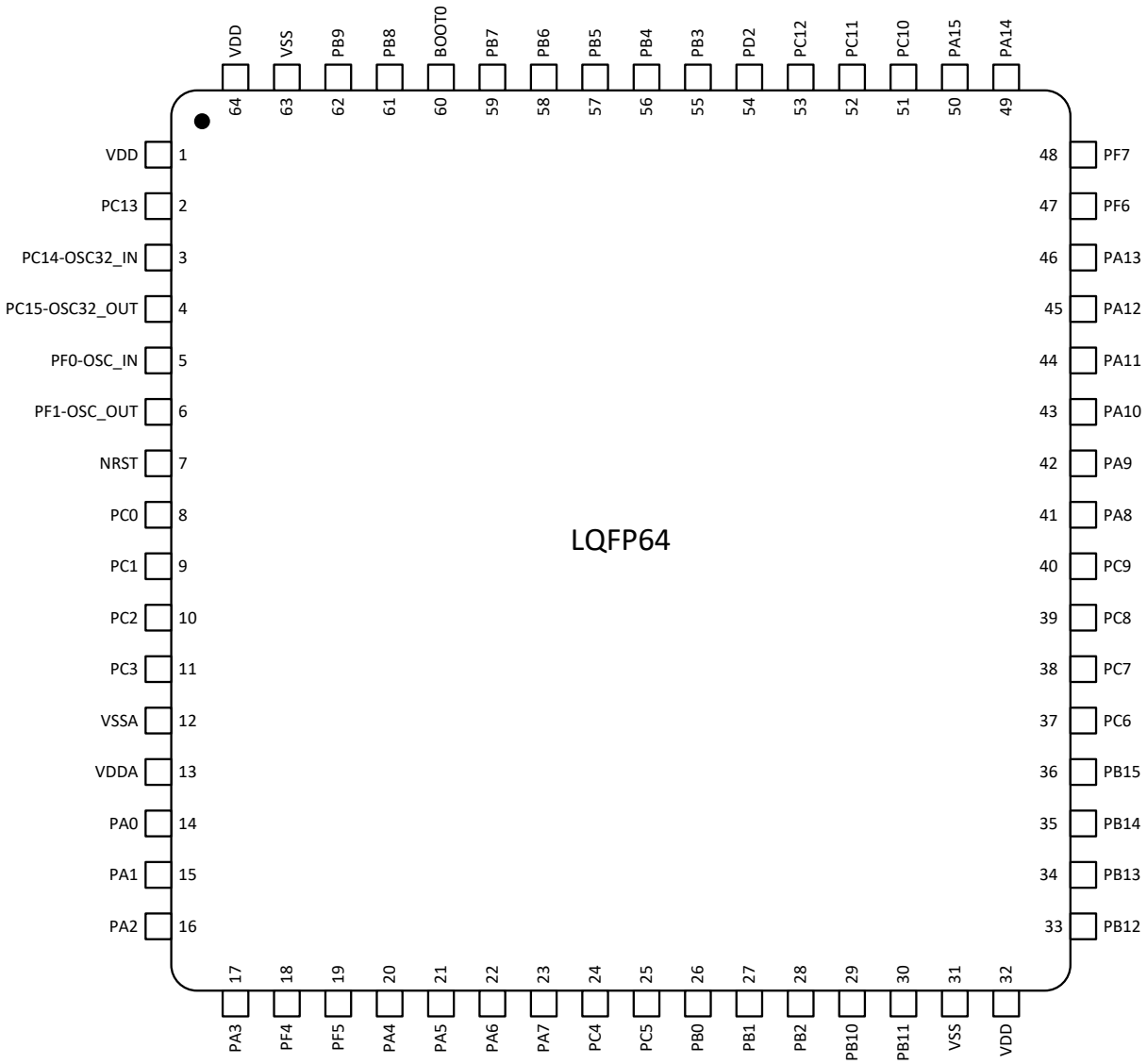
3 Pin descriptions

3.1 Pinouts

3.1.1 LQFP64

Figure 3-1 N32G032 Series LQFP64 pinouts



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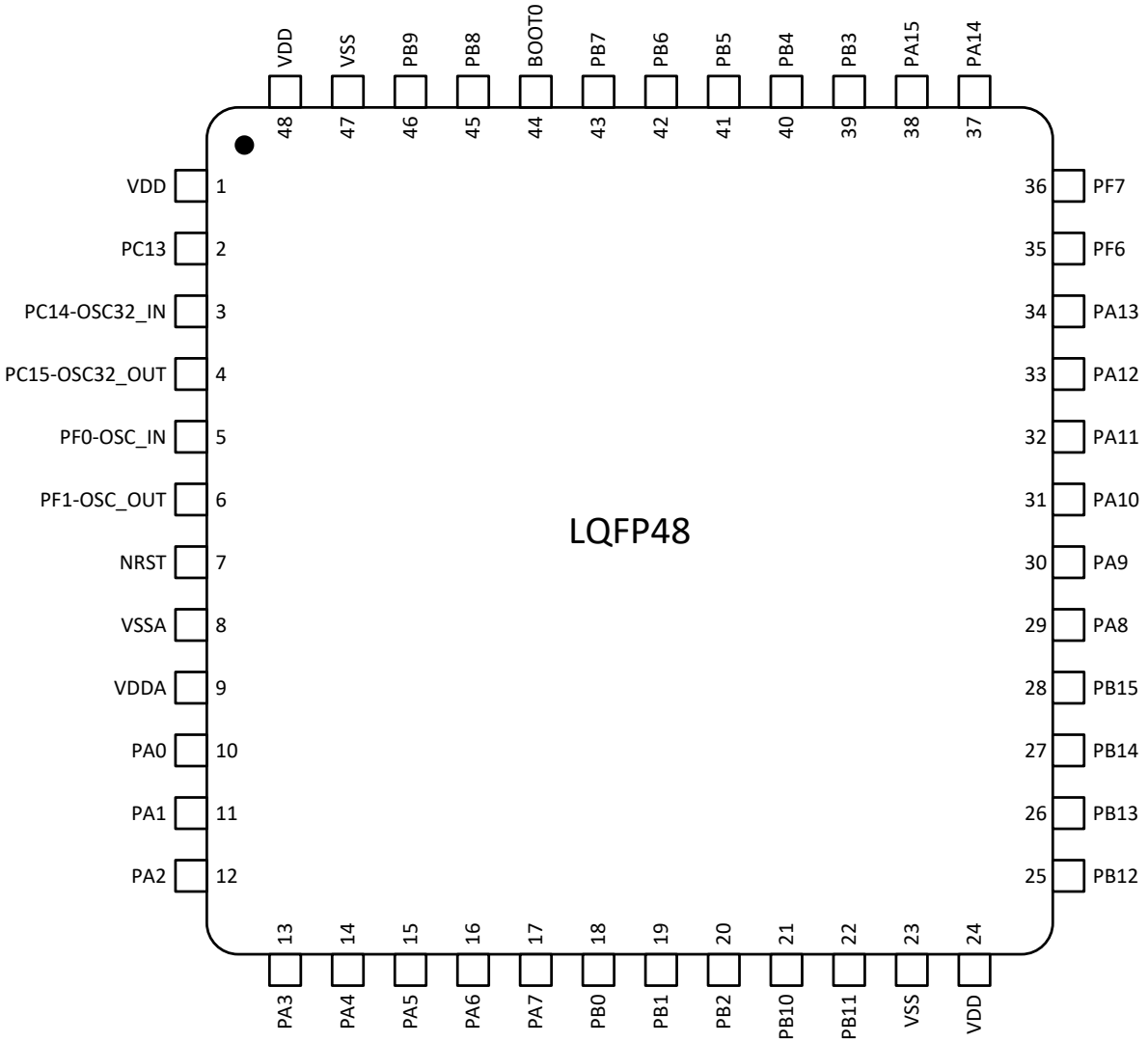
3.1.2 LQFP48

Figure 3-2 N32G032 Series LQFP48 pinouts



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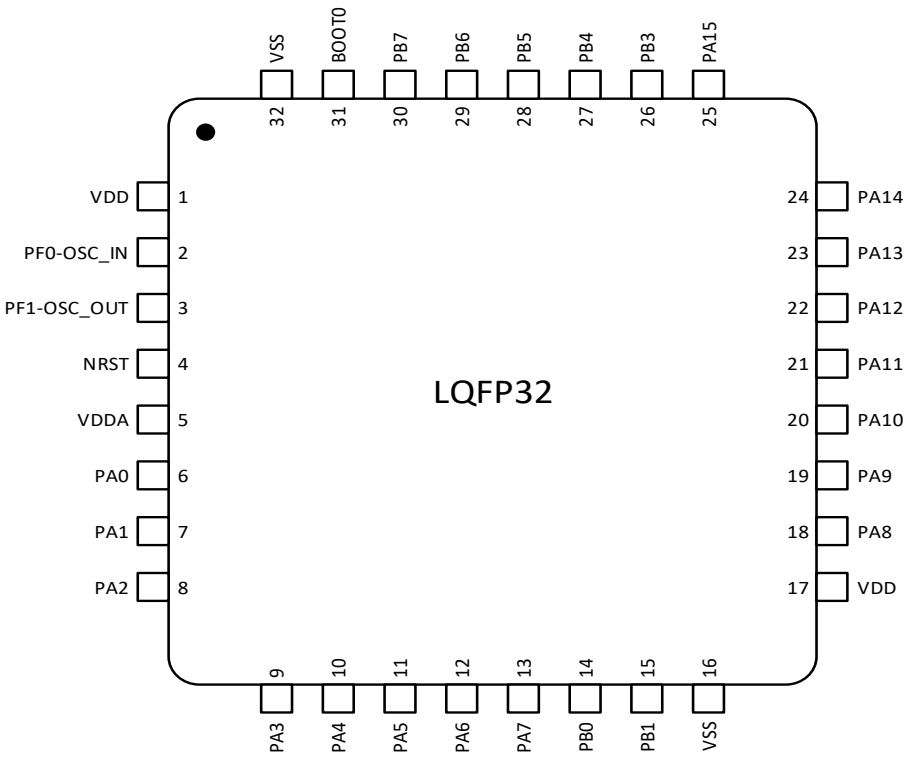
3.1.3 LQFP32

Figure 3-3 N32G032 Series LQFP32 pinouts



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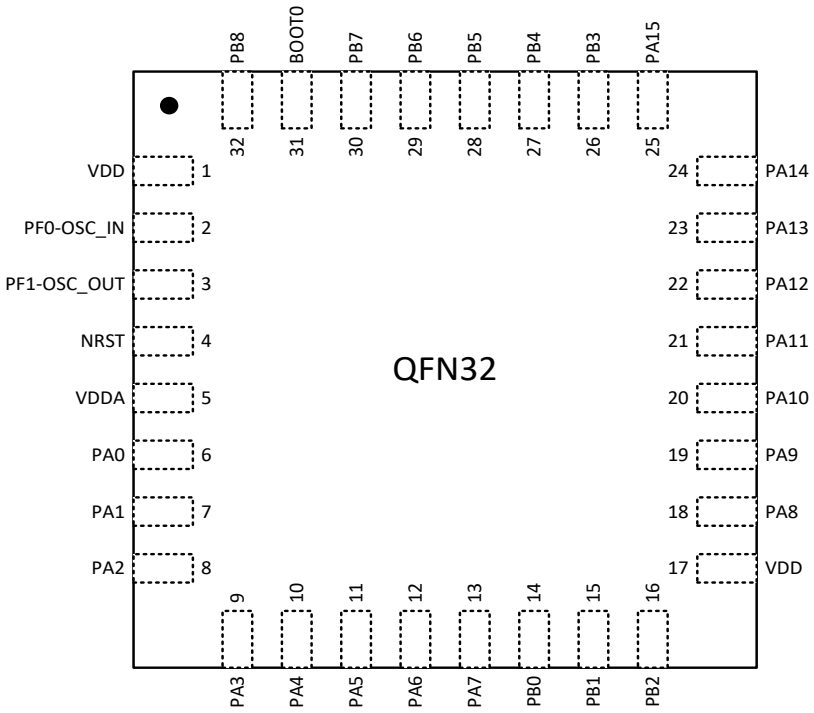
3.1.4 QFN32

Figure 3-4 N32G032 Series QFN32 pinouts



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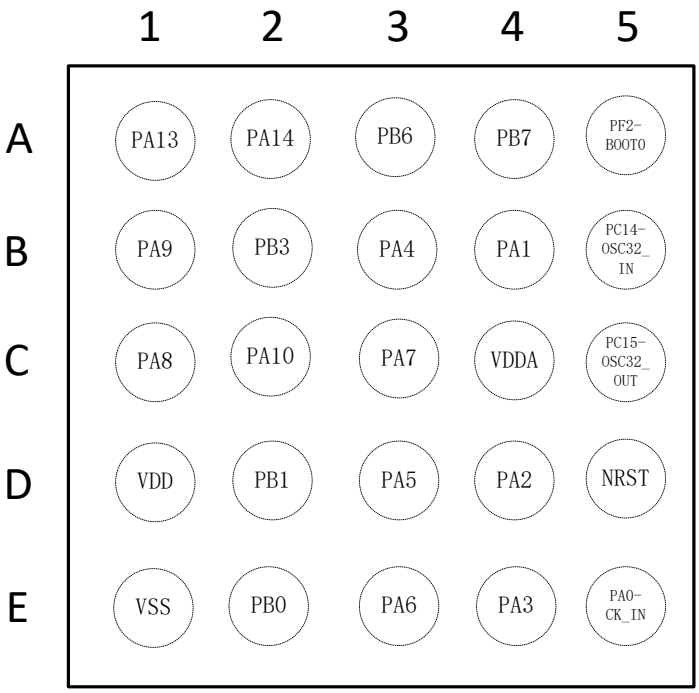
3.1.5 WLCSP25

Figure 3-5 N32G032 Series WLCSP25 pinouts



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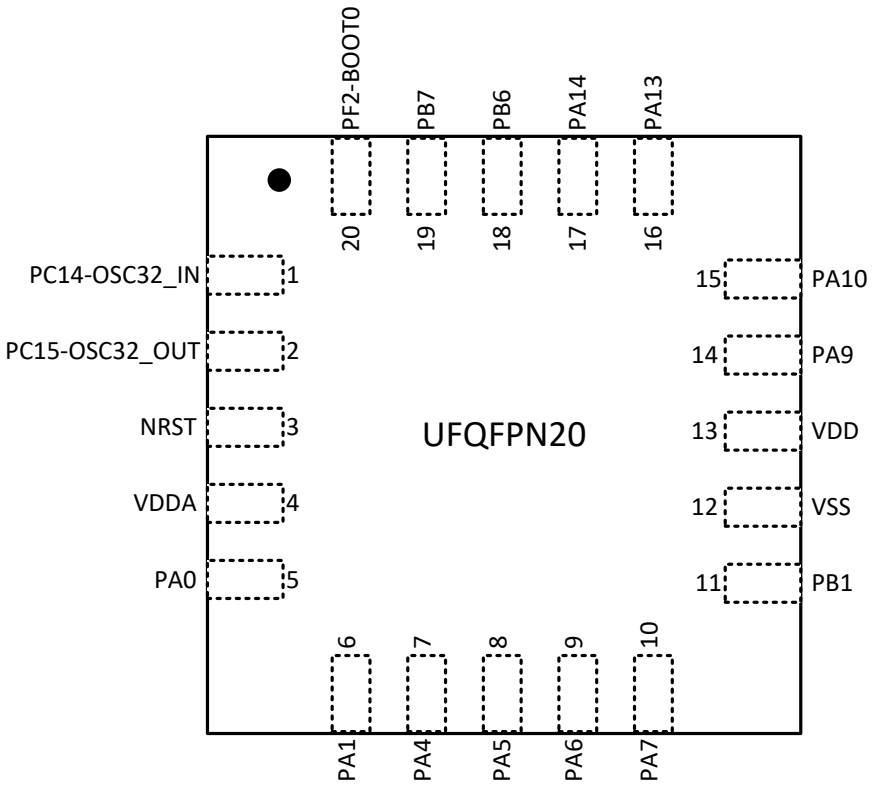
3.1.6 UFQFPN20

Figure 3-6 N32G032 Series UFQFPN20 pinouts



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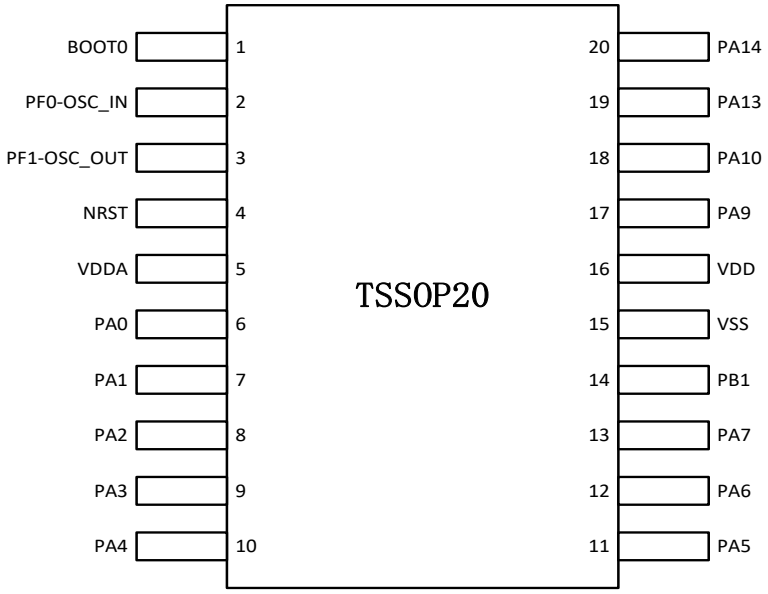
3.1.7 TSSOP20

Figure 3-7 N32G032 Series TSSOP20 pinouts



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3.2 Pin definitions

For details of alternate functions for IO, please refer to the "Alternate function" section within the "GPIO and AFIO" chapter of the User Manual.

Table 3-1 Pin definitions

Package							Pin name (function after reset)	Type(1)	I/O structure	Alternate functions	Additional functions
LQFP64	LQFP48	LQFP32	QFN32	WLCSP25	UFQFPN20	TSSOP20					
1	1	1	1	-	-	-	VDD	S	-	Complementary power supply	
2	2	-	-	-	-	-	PC13	I/O	TC	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP1
3	3	-	-	B5	1	-	PC14-OSC32_IN (PC14)	I/O	TC	-	OSC32_IN
4	4	-	-	C5	2	-	PC15-OSC32_OUT (PC15)	I/O	TC	-	OSC32_OUT
5	5	2	2	-	-	2	PF0-OSC_IN (PF0)	I/O	TC	I2C1_SDA, CAN_TX, COMP3_OUT,	OSC_IN, OPAMP_VINP, COMP3_INM
6	6	3	3	-	-	3	PF1-OSC_OUT (PF1)	I/O	TC	I2C1_SCL, USART1_CK, USART2_CK, CAN_RX	OSC_OUT, OPAMP_VINM, COMP3_INP
7	7	4	4	D5	3	4	NRST	I	RST	Device reset input / internal reset output (active low)	
8	-	-	-	-	-	-	PC0	I/O	TC	EVENTOUT, UART6_TX, LPTIM_IN1	ADC_IN10
9	-	-	-	-	-	-	PC1	I/O	TC	EVENTOUT, UART6_RX, LPTIM_OUT BEEPER1_OUT	ADC_IN11
10	-	-	-	-	-	-	PC2	I/O	TC	SPI2_MISO, EVENTOUT, LPTIM_IN2 BEEPER1_N_OUT	ADC_IN12
11	-	-	-	-	-	-	PC3	I/O	TC	SPI2_MOSI, EVENTOUT, LPTIM_ETR	ADC_IN13
12	8	-	-	-	-	-	VSSA	S	-	Analog ground	
13	9	5	5	C4	4	5	VDDA	S	-	Analog power supply	

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14	10	6	6	E5	5	6	PA0	I/O	TC	USART1_CTS USART2_CTS LPUART2_TX, SPI1_SCK, I2S_CK USART2_RX, LPTIM_IN1, TIM8_CH1, TIM8_ETR, LPUART1_RX, COMP1_OUT,	ADC_IN0, RTC_TAMP2, WKUP0, COMP1_INM, OPAMP_VINP OSC_IN(BYPASS)
15	11	7	7	B4	6	7	PA1	I/O	TC	USART1_RTS USART2_RTS EVENTOUT, LPUART2_RX, SPI1_NSS, I2S_WS LPTIM_IN2, TIM8_CH2, I2C1_SMBA, TIM3_ETR, LPUART1_TX	ADC_IN1, COMP1_INP, COMP2_INP, OPAMP_VINP
16	12	8	8	D4	-	8	PA2	I/O	TC	USART1_TX, USART2_TX, TIM8_CH3, SPI1_MOSI, I2S_SD TIM1_BKIN TIM3_CH1, LPUART1_TX, COMP2_OUT,	ADC_IN2, WKUP2, COMP2_INM, OPAMP_VINM
17	13	9	9	E4	-	9	PA3	I/O	TC	USART1_RX, USART2_RX, TIM8_CH4, TIM1_CH2, SPI1_MISO, TIM3_CH2 LPUART1_RX	ADC_IN3, COMP2_INM COMP1_INP
18	-	-	-	-	-	-	PF4	I/O	TC	EVENTOUT	-
19	-	-	-	-	-	-	PF5	I/O	TC	EVENTOUT	-

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20	14	10	10	B3	7	10	PA4	I/O	TC	SPI1_NSS, I2S_WS, USART1_CK, USART2_CK, TIM4_CH1, UART6_TX, TIM1_CH1, SPI1_MISO, CAN_TX，LPTIM_IN1, LPTIM_ETR, I2C1_SCL, TIM8_ETR, LPUART1_TX, COMP2_OUT	ADC_IN4, COMP1_INM, COMP2_INM OPAMP_VINP
21	15	11	11	D3	8	11	PA5	I/O	TC	SPI1_SCK, I2S_CK, UART6_RX, TIM8_ETR, TIM1_CH2N, TIM1_CH3 SPI1_MOSI, I2S_SD, CAN_RX，LPTIM_IN2, TIM8_CH1	ADC_IN5, COMP1_INM, COMP2_INM OPAMP_VINM
22	16	12	12	E3	9	12	PA6	I/O	TC	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM8_CH1, EVENTOUT, LPUART1_CTS, LPUART1_TX, I2C2_SCL BEEPER1_OUT LPTIM_ETR, COMP1_OUT	ADC_IN6, COMP1_INP OPAMP_VOUT
23	17	13	13	C3	10	13	PA7	I/O	TC	SPI1_MOSI, I2S_SD, TIM3_CH2, TIM4_CH2, TIM1_CH1N, TIM8_CH2, EVENTOUT, LPUART1_RX, I2C2_SDA LPTIM_OUT, USART2_CTS, TIM3_ETR, COMP2_OUT, BEEPER1_N_OUT	ADC_IN7, OPAMP_VINP COMP1_INP

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24	-	-	-	-	-	-	PC4	I/O	TC	EVENTOUT, LPUART1_TX, CAN_TX	ADC_IN14
25	-	-	-	-	-	-	PC5	I/O	TC	LPUART1_RX, CAN_RX	ADC_IN15, OPAMP_VINM
26	18	14	14	E2	-	-	PB0	I/O	TC	TIM3_CH3, TIM1_CH2N, EVENTOUT, UART5_TX, SPI3_SCK，SPI1_MISO, TIM8_CH2, USART2_RTS	ADC_IN8, OPAMP_VINP
27	19	15	15	D2	11	14	PB1	I/O	TC	TIM3_CH4, TIM4_CH3, TIM1_CH3N, LPUART1_RTS, UART5_RX，USART2_CK, SPI1_MOSI, I2S_SD LPTIM_IN1, TIM8_CH4，COMP3_OUT	ADC_IN9
28	20	-	16	-	-	-	PB2	I/O	TC	I2C1_SMBA, I2C2_SMBA, TIM4_CH4, LPTIM_OUT	OPAMP_VINM
29	21	-	-	-	-	-	PB10	I/O	TC	SPI2_SCK, I2C1_SCL, I2C2_SCL, LPUART1_TX, TIM4_ETR, SPI1_MOSI, I2S_SD	OPAMP_VINP
30	22	-	-	-	-	-	PB11	I/O	TC	I2C1_SDA, I2C2_SDA, EVENTOUT, LPUART1_RX, TIM8_CH3, CAN_RX	
31	23	16	-	E1	12	-	VSS	S	-	Ground	
32	24	17	17	D1	13	-	VDD	S	-	Digital power supply	
33	25	-	-	-	-	-	PB12	I/O	TC	SPI1_NSS, I2S_WS, SPI2_NSS, TIM1_BKIN, EVENTOUT, CAN_TX, TIM8_CH1	

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34	26	-	-	-	-	-	PB13	I/O	TC	SPI1_SCK, I2S_CK, SPI2_SCK, I2C2_SCL TIM1_CH1N, LPUART1_CTS, TIM8_CH2	-
35	27	-	-	-	-	-	PB14	I/O	TC	SPI1_MISO, SPI2_MISO, I2C2_SDA, TIM1_CH2N, TIM8_CH3, LPUART1_RTS	OPAMP_VINP
36	28	-	-	-	-	-	PB15	I/O	TC	SPI1_MOSI, I2S_SD, SPI2_MOSI, TIM1_CH3N, TIM8_CH3N, TIM8_CH4, TIM4_CH2	RTC_REFIN,
37	-	-	-	-	-	-	PC6	I/O	TC	TIM3_CH1	COMP3_INM
38	-	-	-	-	-	-	PC7	I/O	TC	TIM3_CH2	COMP3_INP
39	-	-	-	-	-	-	PC8	I/O	TC	TIM3_CH3 COMP3_OUT	
40	-	-	-	-	-	-	PC9	I/O	TC	TIM3_CH4 SPI3_MOSI	
41	29	18	18	C1	-	-	PA8	I/O	TC	USART1_CK, USART2_CK, TIM1_CH1, EVENTOUT, MCO, SPI3_NSS, TIM8_CH2N， LPTIM_IN1, TIM8_CH1	COMP2_INM
42	30	19	19	B1	14	17	PA9	I/O	TC	USART1_TX, TIM1_CH2, TIM8_BKIN, I2C1_SCL, I2C2_SCL, SPI3_SCK, TIM8_CH1N， MCO, LPTIM_OUT, USART2_TX, TIM3_CH2, COMP1_OUT	COMP2_INP

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43	31	20	20	C2	15	18	PA10	I/O	TC	USART1_RX, TIM1_CH3, TIM8_BKIN, I2C1_SDA, I2C2_SDA, SPI3_ MISO，TIM3_CH1, COMP2_OUT，USART2_RX, TIM8_CH3，RTC_REFIN,	OPAMP_VINP
44	32	21	21	-	-	-	PA11	I/O	TC	USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL , SPI3_ MOSI, UART6_TX，COMP1_OUT	COMP3_INP
45	33	22	22	-	-	-	PA12	I/O	TC	USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA, SPI3_MISO, UART6_RX，COMP2_OUT	COMP1_INP COMP3_INM
46	34	23	23	A1	16	19	PA13 (SWDIO)	I/O	TC	USART1_TX, SWDIO USART1_RX, USART2_RX, LPTIM_ETR, I2C1_SDA, SPI1_SCK, I2S_CK LPUART1_RX，COMP1_OUT	-
47	35	-	-	-	-	-	PF6	I/O	TC	I2C1_SCL , I2C2_SCL, SPI3_SCK	COMP1_INM COMP3_INP
48	36	-	-	-	-	-	PF7	I/O	TC	I2C1_SDA , I2C2_SDA , SPI3_NSS	COMP1_INP COMP3_INM
49	37	24	24	A2	17	20	PA14 (SWCLK)	I/O	TC	USART1_TX , USART2_TX, SWCLK，LPTIM_OUT, I2C1_SMBA, SPI1_MISO, LPUART1_TX, COMP2_OUT	-

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50	38	25	25	-	-	-	PA15	I/O	TC	SPI1_NSS, I2S_WS, USART1_RX, USART2_RX, LPUART2_RTS, EVENTOUT SPI3_MOSI, COMP1_OUT,	OPAMP_VINP
51	-	-	-	-	-	-	PC10	I/O	TC	LPUART1_TX, LPUART2_TX SPI3_MISO	
52	-	-	-	-	-	-	PC11	I/O	TC	LPUART1_RX, LPUART2_RX	
53	-	-	-	-	-	-	PC12	I/O	TC	UART5_TX	
54	-	-	-	-	-	-	PD2	I/O	TC	TIM3_ETR, LPUART1_RTS, UART5_RX	
55	39	26	26	B2	-	-	PB3	I/O	TC	SPI1_SCK, I2S_CK, EVENTOUT, UART5_TX, LPUART1_TX，TIM8_CH2,	OPAMP_VINM COMP2_INM
56	40	27	27	-	-	-	PB4	I/O	TC	SPI1_MISO, TIM3_CH1, EVENTOUT, TIM8_BKIN UART5_RX, LPUART1_RX, LPTIM_OUT	OPAMP_VINP COMP2_INP
57	41	28	28	-	-	-	PB5	I/O	TC	SPI1_MOSI, I2S_SD, I2C1_SMBA, TIM8_BKIN, TIM3_CH2, LPUART2_TX, LPTIM_IN1, TIM8_CH3N	OPAMP_VINP COMP2_INP
58	42	29	29	A3	18	-	PB6	I/O	TC	I2C1_SCL, USART1_TX, USART2_TX, LPUART1_TX, TIM8_CH1N, TIM8_CH3, LPTIM_ETR BEEPER2_OUT	COMP2_INP

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59	43	30	30	A4	19	-	PB7	I/O	TC	I2C1_SDA, USART1_RX, USART2_RX, LPUART1_RX，TIM8_CH2N, LPUART2_CTS, LPUART2_RX, LPTIM_IN2，TIM8_CH4, PVD_IN BEEPER2_N_OUT	COMP2_INP
60	44	31	31	A5	20	1	PF2-BOOT0	I	B	Boot memory selection	
61	45	-	32	-	-	-	PB8	I/O	TC	I2C1_SCL, TIM8_CH1	
62	46	-	-	-	-	-	PB9	I/O	TC	I2C1_SDA, USART1_TX , SPI2_NSS, TIM8_CH2, EVENTOUT	
63	47	32	-	-	-	15	VSS	S	-	Ground	
64	48	-	-	-	-	16	VDD	S	-	Digital power supply	

1. *I = input, O = output, S = power, HiZ = High resistance, B = BOOT0 pin*
2. *TC: Standard 5V I/O, RST: bidirectional reset pin with built-in weak pull-up resistor*
3. *Some functions are only supported in some models of chips.*
4. *During and immediately after the reset, the multiplexing function is not enabled, and the I/O port is configured as an analog input mode (PMODEx[1:0]=2'b11). But there are a few exception signals:*
   - *NRST has no GPIO function by default*
   - *NRST pull-up input*
   - *After reset, the default state of the pins related to the debugging system is the SWD function, and the SWD pin is configured to input pull-up or pull-down mode:*
     - *PA14: SWCLK is configured as input pull-down mode*
     - *PA13: SWDIO is configured as input pull-up mode*
   - *PA0/PF0:*
     - *PA0/PF0 is configured as floating input mode by default*
     - *PA0/PF0 is multiplexed to OSC_IN*
   - *PF2/BOOT0:*
     - *PF2/BOOT0 is configured as pull-down input mode by default*

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4 Electrical characteristics

4.1 Parameter conditions

All voltages are based on VSS unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures T_A=25 ℃.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production line; On the basis of comprehensive evaluation, the minimum and maximum values are obtained by samples tested.

4.1.2 Typical numerical values

Unless otherwise specified, typical data is based on T_A=25 ℃ and V_{DD}=3.3V (1.8V ≤ VDD ≤ 5.5V voltage range). These data are only used for design guidance and not tested.
Typical ADC accuracy values are obtained by sampling a standard batch, tested at all temperature ranges.

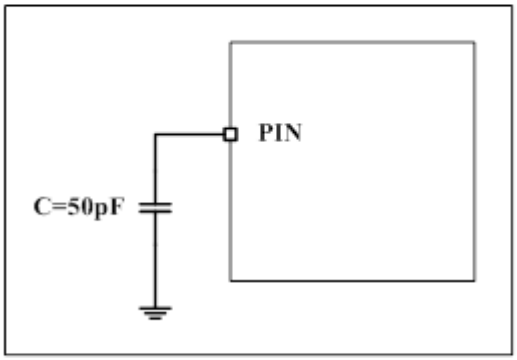
4.1.3 Typical curves

Unless otherwise specified, typical curves are for design guidance only and have not been tested.

4.1.4 Loading capacitor

The load conditions when measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 pin loading conditions



4.1.5 Pin input voltage

The measurement method of the input voltage on the pin is shown in Figure 4-2.

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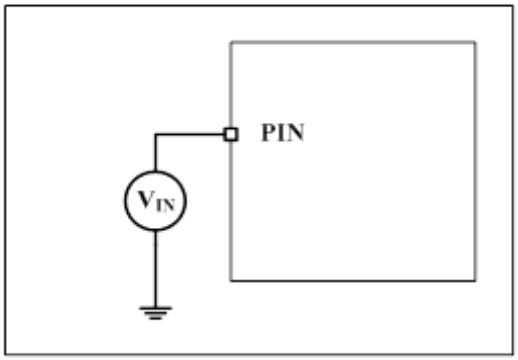
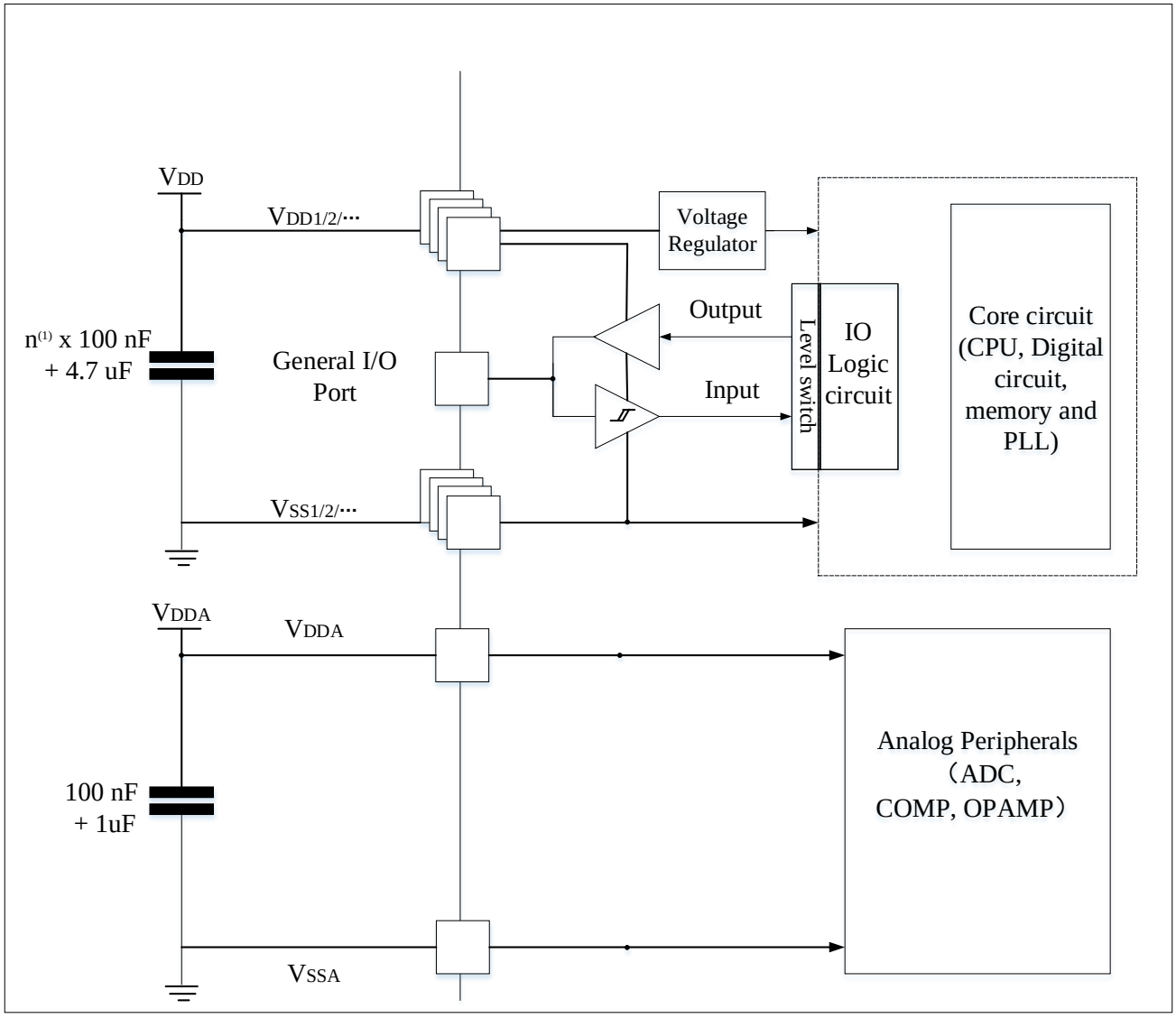
Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

Figure 4-3 Power supply scheme



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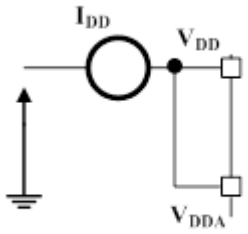
1. n is the count of VDD.

Note: Please refer to the hardware design guide for the capacitor connection method.

4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement



4.2 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage(including V_{DDA} and V_{DD})(1)	-0.3	5.5	V
V_{IN}	Input voltage on any I/O and control pins	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}$- $V_{SS}\rvert$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (human body model)	See section 4.3.11		

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an external power supply within the allowable range.

Table 4-2 Current characteristics

Symbol	Parameter	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines(1)	200	mA
I_{VSS}	Total current out of V_{SS} ground lines(1)	200	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/O and control pins	-16	
$I_{INJ(PIN)}$ (2)	Injected current of NRST pin	0/-5	
	Injected current of OSC_IN pin of HSE and OSC_IN pin of LSE	+/-5	
	Injected current of other pins	+/-5	

1. All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power supply within the allowable range.
2. Negative injected current can interfere with the analog performance of the device. See section 4.3.17.

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Table 4-3 Temperature characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-40 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	-	0	48	MHz
f_{PCLK1}	APB1 clock frequency	-	0	48	
f_{PCLK2}	APB2 clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	1.8	5.5	V
V_{DDA}	Analog operating voltage	Must be the same voltage as V_{DD}(1)	1.8	5.5	V
T_A	Temperature range	Maximum power consumption	-40	105	℃
T_J	Junction temperature range		-40	125	℃

1. Use the same power supply to supply V_{DD} and V_{DDA}. During power-up and normal operation, a maximum difference of 300mV between V_{DD} and V_{DDA} is allowed.

4.3.2 Operating conditions at power-up and power-down

The parameters given in the following table are based on testing under the ambient temperature listed in Table 4-4.

Table 4-5 Operating conditions at power-up and power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rising time rate	From 0 to V_{DD}	100	650	μs/V
	V_{DD} falling time rate	From V_{DD} to 0	100	∞	μs/V

4.3.3 Reset and power control module features

The parameter test conditions in the following table are based on Table 4-4.

Table 4-6 Reset and power control module features

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{PVD}	Rising	PLS[3:0]=0	1.78	1.88	1.98	V
	Falling	PLS[3:0]=0	1.68	1.78	1.88	
	Rising	PLS[3:0]=1	1.98	2.08	2.18	
	Falling	PLS[3:0]=1	1.88	1.98	2.08	
	Rising	PLS[3:0]=2	2.18	2.28	2.38	
	Falling	PLS[3:0]=2	2.08	2.18	2.28	

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	Rising	PLS[3:0]=3	2.38	2.48	2.58	
	Falling	PLS[3:0]=3	2.28	2.38	2.48	
	Rising	PLS[3:0]=4	2.58	2.68	2.78	
	Falling	PLS[3:0]=4	2.48	2.58	2.68	
	Rising	PLS[3:0]=5	2.78	2.88	2.98	
	Falling	PLS[3:0]=5	2.68	2.78	2.88	
	Rising	PLS[3:0]=6	2.96	3.08	3.2	
	Falling	PLS[3:0]=6	2.86	2.98	3.1	
	Rising	PLS[3:0]=7	3.16	3.28	3.4	
	Falling	PLS[3:0]=7	3.06	3.18	3.3	
	Rising	PLS[3:0]=8	3.36	3.48	3.6	
	Falling	PLS[3:0]=8	3.26	3.38	3.5	
	Rising	PLS[3:0]=9	3.56	3.68	3.8	
	Falling	PLS[3:0]=9	3.46	3.58	3.7	
	Rising	PLS[3:0]=10	3.76	3.88	4	
	Falling	PLS[3:0]=10	3.66	3.78	3.9	
	Rising	PLS[3:0]=11	3.92	4.08	4.24	
	Falling	PLS[3:0]=11	3.82	3.98	4.14	
	Rising	PLS[3:0]=12	4.12	4.28	4.44	
	Falling	PLS[3:0]=12	4.02	4.18	4.34	
	Rising	PLS[3:0]=13	4.32	4.48	4.64	
	Falling	PLS[3:0]=13	4.22	4.38	4.54	
	Rising	PLS[3:0]=14	4.52	4.68	4.84	
	Falling	PLS[3:0]=14	4.42	4.58	4.74	
	Rising	PLS[3:0]=15	4.72	4.88	5.04	
	Falling	PLS[3:0]=15	4.62	4.78	4.94	
$V_{PVDhyst}$(1)	PVD hysteresis	-	80	100	125	mV
$V_{POR/PDR}$	VDD power on/power down reset threshold	-	-	1.53	-	V
$T_{RSTTEMPO}$(1)	Reset temporization	-	-	100		us

1. Guaranteed by design, not tested in production.

4.3.4 Internal reference voltage

The parameter test conditions in the following table are based on Table 4-4.

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Table 4-7 Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃< T_A< +105℃	1.16	1.21	1.26	V
$T_{S\_vrefint}$(1)	When reading the internal reference voltage, the sampling time of the ADC	PLS[2:0]=001 (Rising edge)	-	10	-	μs

1. The shortest sampling time is obtained through multiple loops in the application.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.5 Power supply current characteristics

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, I/O pin flip rate, program location in memory, and code executed.

The measurement method of current consumption is illustrated in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

Maximum current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level——V_{DD} or V_{SS} (no load).
- All peripherals are in the off state, unless otherwise specified.
- The access time of flash memory is adjusted to the frequency of f_{HCLK} (0~18MHz is 0 waiting period, 18~36MHz is 1 waiting period, and more than 36MHz is 2 waiting periods).
- The command prefetch function is enabled (Note: this parameter must be set before setting the clock and bus frequency division).
- When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-8 Typical current consumption in RUN mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in RUN mode	External clock(2), Enable all peripherals	48MHz	11.5	mA
			24MHz	6.5	
			8MHz	3.4	
		External clock (2), Disable all peripherals	48MHz	5.8	
			24MHz	3.7	
			8MHz	2.4	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-9 Typical current consumption in RUN mode when running code from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current	External clock (2),	48MHz	12.15	mA

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	in RUN mode	Enable all peripherals	24MHz	6.85	
			8MHz	2.9	
		External clock (2), Disable all peripherals	48MHz	6.3	
			24MHz	3.8	
			8MHz	1.85	

1. Guaranteed by design and comprehensive evaluation, Tested in production with maximal V_{DD} and maximal f_{HCLK}.
2. External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.

Table 4-10 Typical current consumption in SLEEP mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) T_A = 105℃	Unit
I_{DD}	Supply current in SLEEP mode	External clock (2), Enable all peripherals	48MHz	9.35	mA
			24MHz	5.32	
			8MHz	2.4	
		External clock (2), Disable all peripherals	48MHz	3.55	
			24MHz	2.45	
			8MHz	1.45	

1. Guaranteed by comprehensive evaluation, V_{DDMAX} and $f_{HCLKMAX}$ enabled peripherals are tested in production.
2. External clock, when f_{HCLK} is 24M or 48M, PLL needs to be enabled.
3. When ADC is enabled, there is a current of 1.1mA (guaranteed by design).

Table 4-11 Typical consumption in PD mode and STOP mode

Symbol	**Parameter**	**Conditions**	**Typ (1)** V_{DD}=3.3V	**Max** V_{DD}=3.3V	**Unit**
Low power mode	Current in SLEEP mode	The core is stopped, all peripherals including Cortex®-M0 core peripherals, such as NVIC, system tick clock (SysTick) is still running)	0.868	5	mA
	Current in STOP mode	Turn off RTC, SRAM data retention, all I/O status retention, register retention	2.18	23	uA
	Current in PD mode	V_{DD} power-down mode, 3 WAKEUP IO and NRST can wake up the chip	0.4	1	uA

1. The typical value/maximum value is tested under T_A=25℃.

Typical current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are in the off state, unless otherwise specified.
- The access time of flash memory is adjusted to the frequency of f_{HCLK} (0~18MHz is 0 waiting period, 18~36MHz is 1 waiting period, and more than 36MHz is 2 waiting periods).

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- The command prefetch function is enabled (Note: this parameter must be set before setting the clock and bus frequency division).
- When the peripheral is turned on: $f_{PCLK1}= f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/3$.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-12 Typical current consumption in RUN mode when running code from FLASH

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in RUN mode	External high-speed clock (HSE), use AHB prescaler to reduce the frequency	48MHz	11.2	6.08	mA
			24MHz	6.2	3.75	
			8MHz	3.1	2.11	
		Internal high-speed RC oscillator (2) (HSI), using AHB prescaler to reduce the frequency	48MHz	10.6	5.36	mA
			24MHz	5.63	3.1	
			8MHz	2.53	1.7	

1. The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.
2. The internal high-speed clock is 8MHz, and PLL is enabled when f_{HCLK} > 8MHz.

Table 4-13 Typical current consumption in SLEEP mode when running code from FLASH or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Current in SLEEP mode	External high-speed clock (HSE), use AHB prescaler to reduce the frequency	48MHz	9.15	3.72	mA
			24MHz	5.15	2.41	
			8MHz	2.2	1.27	
		Internal high-speed RC oscillator (2) (HSI), using AHB prescaler to reduce the frequency	48MHz	8.6	3.07	mA
			24MHz	4.6	0.76	
			8MHz	1.65	0.70	

1. The typical value is obtained by testing at T_A=25℃ V_{DD}=3.3V.
2. The internal high-speed clock is 8MHz, and PLL is enabled when f_{HCLK} > 8MHz.

4.3.6 External clock source characteristics

High-speed external clock generated by external oscillator

The characteristic parameters in the following table are measured using a high-speed external clock source.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-14 High-speed external clock characteristics (Bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External high-speed clock frequency (1)	T_A=25℃	4	8	20	MHz
V_{HSEH}	OSC_IN input pin high level voltage (1)		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage (1)		V_{SS}	-	0.3V_{DD}	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(HSE)}$ $t_{l(HSE)}$	OSC_IN high or low time (1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time (1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive reactance (1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN input leakage current (1)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Low-speed external clock generated by external oscillator source

The characteristic parameters in the following table are measured using a low-speed external clock source.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-15 Low-speed external clock characteristics (Bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External low-speed clock frequency	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage (1)		0.7VDD	-	VDD	V
V_{LSEL}	OSC32_IN input pin low-level voltage (1)		VSS	-	0.3VDD	
$t_{h(LSE)}$ $t_{l(LSE)}$	OSC32_IN high or low time (1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time (1)		-	-	10	
$DuCy_{(LSE)}$	Duty cycle (1)		30	-	70	%
I_L	OSC32_IN input leakage current (1)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

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Figure 4-5 AC timing diagram of external high-speed clock source

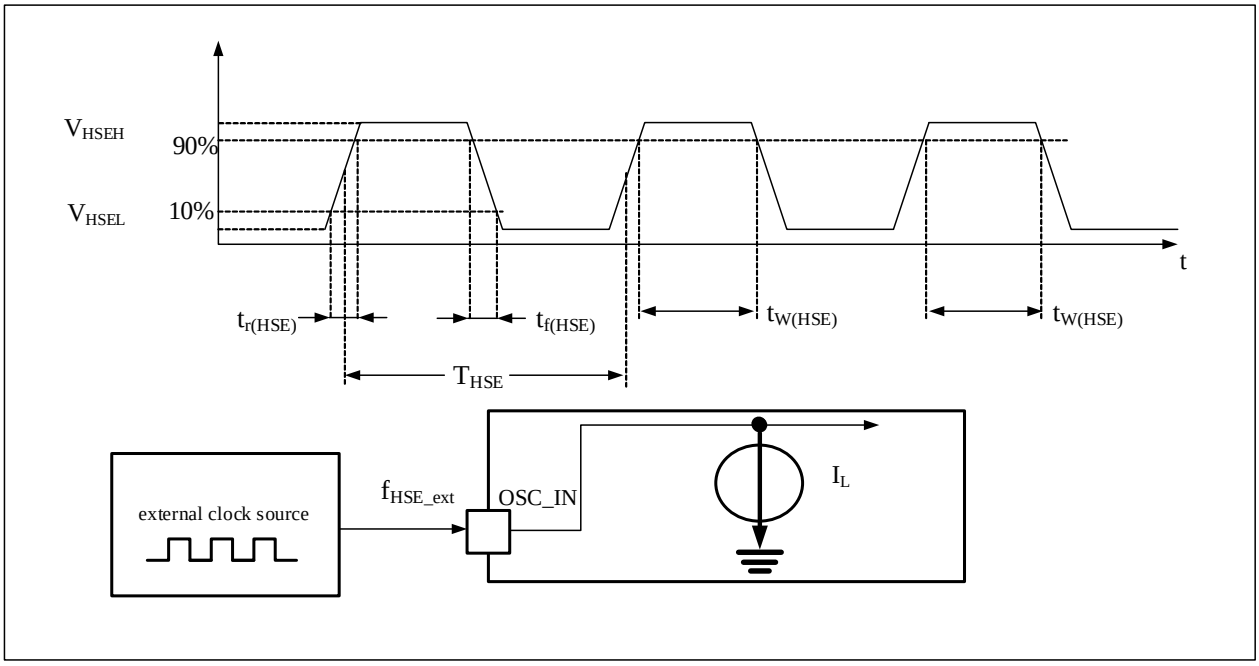
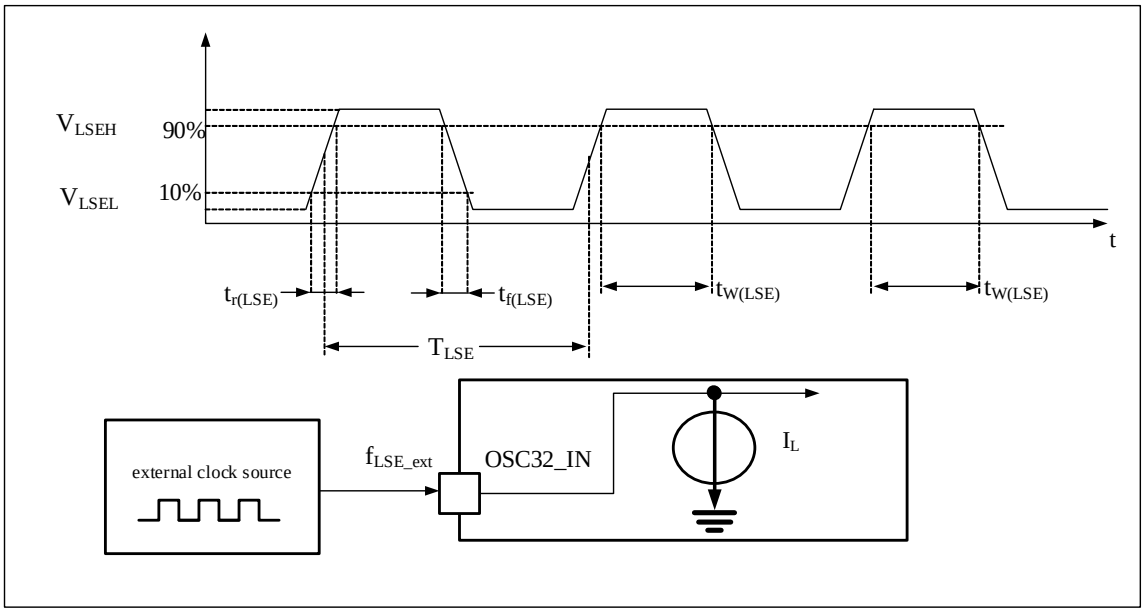


Figure 4-6 AC timing diagram of external low-speed clock source



High-speed external clock generated by a crystal/ceramic resonator

The high-speed external clock (HSE) can be generated using a 4-20MHz crystal/ceramic resonator oscillator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we usually call passive crystal oscillator).

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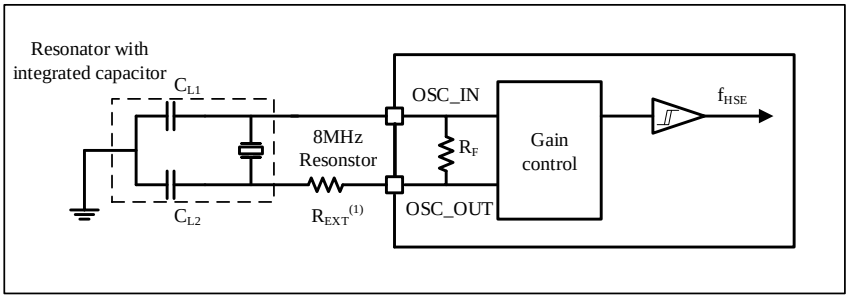
Table 4-16 HSE 4~20MHz Oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	20	MHz
$t_{SU(HSE)}$(3)	Startup Time	V_{DD} is stabilized, f_{out} = 20MHz	-	3	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design and comprehensive evaluation, not tested in production.
3. $t_{SU(HSE)}$ is the start-up time, which is the time from the software enabling HSE to start measurement until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

Figure 4-7 Typical application using 8MHz crystal



1. R_{EXT} value is determined by the characteristics of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The Low-speed external clock (LSE) can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we usually call passive crystal oscillator).

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}.

The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + Cstray$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

Table 4-17 LSE Oscillator characteristics (f_{LSE}=32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LSE)}$(2)	Startup Time	V_{DD} is stabilized	-	3.5	-	s

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. $t_{SU(LSE)}$ is the start-up time, which is the time from the software enabling LSE to start measurement until a stable 32.768KHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

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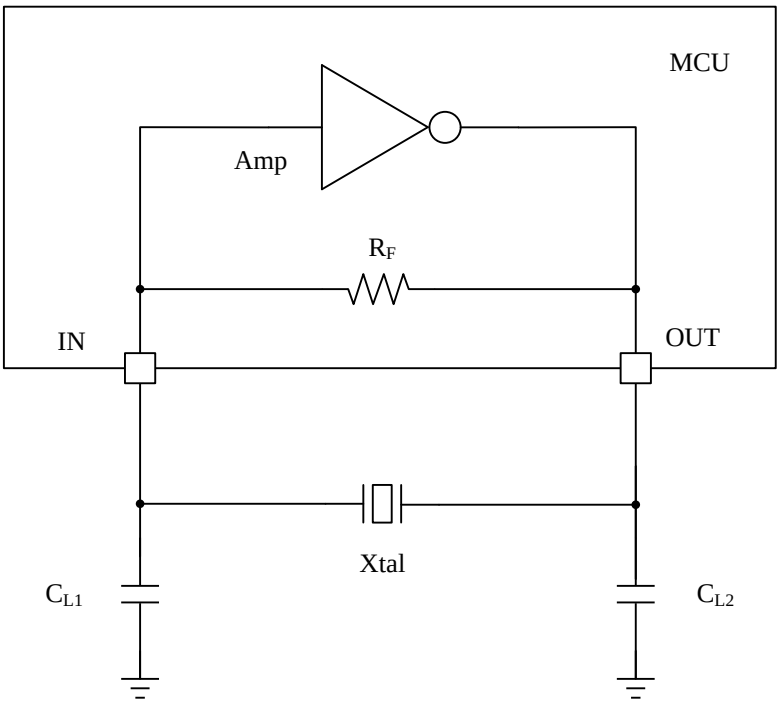
Figure 4-8 Typical application using 32.768kH crystal



4.3.7 Internal clock source characteristics

The parameter test conditions in the following table are based on Table 4-4.

High-speed internal (HSI) RC oscillator

Table 4-18 HSI Oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	7.92(3)	8	8.08(3)	MHz
$DuCy_{(HSI)}$	Duty cycle		45	-	55	%
ACC_{HSI}	The temperature drift of the HSI oscillator(4)	V_{DD}=3.3V, T_A = -40~105℃, Temperature drift	-3	-	3	%
		V_{DD}=3.3V, T_A = -10~85℃, Temperature drift	-1	-	1	%
		V_{DD}=3.3V, T_A = 0~70℃, Temperature drift	-1	-	1	%
$t_{SU(HSI)}$	HSI startup Time		1	-	3	μs
$I_{DD(HSI)}$	HSI power consumption		-	80	150	μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.
2. Guaranteed by design and comprehensive evaluation, not tested in production.
3. Production calibration accuracy, excluding welding effects. Welding brings about 1% frequency deviation range.
4. Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 4-19 LSI Oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	V_{DD}=3.3V, T_A = 25℃, After calibration	29	30	31	KHz

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		V_{DD} =1.8V ~5.5V, T_A = -40~105℃	24	30	36	KHz
$t_{SU(LSI)}$ (2)	LSI Startup Time		-	30	80	μs
$I_{DD(LSI)}$(2)	LSI driving current		-	0.2	-	μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40~105℃.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.8 Low-power mode wake-up time

The wake-up time listed in Table 4-20 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP or PD mode: clock source is RC oscillator
- SLEEP mode: the clock source is the clock used when entering sleep mode

The parameter test conditions in the following table are based on Table 4-4.

Table 4-20 Low-power mode wake-up time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wake up from SLEEP mode	16	HCLK(2)
t_{WUSTOP}(1)	Wake up from STOP mode	20	us
t_{WUPD}(1)	Wake up from PD mode	55	

1. The measurement of the wake-up time is from the start of the wake-up event to the user program reading the first instruction.
2. HCLK is the AHB frequency.

4.3.9 PLL characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-21 PLL characteristics

Symbol	Parameter	Num			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	20	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	48	-	72	MHz
t_{LOCK}	PLL Ready indicates signal output time	-	-	20	μs
Jitter	TIE RMS Jitter	-	40	-	pS
I_{pll}	Operating Current of PLL @48MHz VCO frequency.	-	300	500	uA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Need to pay attention to using the correct frequency multiplication factor, so that f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

4.3.10 FLASH characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

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Table 4-22 FLASH characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
t_{prog}	Word programming time(32-bit)	T_A = -40~105℃	-	175	-	μs
t_{ERASE}	Page erase time(512Bytes)	T_A = -40~105℃	-	2.27	-	ms
t_{ME}	Mass erase time	T_A = -40~105℃;	-	34.1	-	ms
I_{DD}	Current(1)	Read, f_{HCLK}=48MHz, V_{DD}=3.3V	-	2	2.4	mA
		Write, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	1.2	mA
		Erase, f_{HCLK}=48MHz, V_{DD}=3.3V	-	-	0.6	mA
		Deep standby mode, V_{DD}=3.3~3.6V	-	-	150	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Table 4-23 Flash endurance and data retention period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance(Note: erasing and writing cycle)	T_A = -40~105 ℃	100	kcycles
t_{RET}	Data retention	T_A = 105 ℃, after 1000 erasing cycle(1)	10	years

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.11 Electrical sensitivity

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-24 ESD characteristics

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, In accordance with MIL-STD-883K Method 3015.9	2	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 ℃, In accordance with ESDA/JEDEC JS-002-2018	II	1000	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Staic Latch-up

To evaluate the locking performance, two complementary static latch-up tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78E IC latch standard.

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Table 4-25 Static Latch-up characteristics

Symbol	Parameter	Conditions	Class
LU	Static Latch-up	TA = +105 ℃, conforming to JESD78E	II level A

4.3.12 I/O port characteristics

Generic input/output characteristics

The parameter test conditions in the following table are based on Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-26 I/O static characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
V_{IL}	IO Low level input voltage	5	-	-	0.3×VDD	V
		3.3	-	-	0.8	
		1.8	-	-	0.2×VDD	
V_{IH}	IO High level input voltage	5	-	0.7×VDD	-	
		3.3	-	2.0	-	
		1.8	-	0.8×VDD	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis (1)	5/3.3/1.8	-	0.1×VDD	-	V
I_{lkg}(2)	Input leakage current IIH	5/3.3/1.8	-	-	+1	μA
	Input leakage current IIL	5/3.3/1.8	-	-1	-	
V_{OH}	Output high level voltage	5	High driving I_{min}=16mA low driving I_{min} =8mA	VDD-0.8	-	V
		3.3	High driving I_{min} =8mA low driving I_{min} =4mA	2.4	-	
		1.8	High driving I_{min} =4mA low driving I_{min} =2mA	VDD-0.45	-	
V_{OL}	Output low level voltage	5	High driving I_{min} =16mA low driving I_{min} =8mA	-	0.7	
		3.3	High driving I_{min} =8mA low driving I_{min} =4mA	-	0.45	
		1.8	High driving I_{min} =4mA low driving I_{min} =2mA	-	0.4	
R_{PU}	Weak pull-up equivalent resistor	5/3.3/1.8	-	40	100	kΩ
R_{PD}	Weak pull-down equivalent resistor	5/3.3/1.8	-	40	100	kΩ
C_{IO}	I/O pin capacitance	5/3.3/1.8	-	-	10	pF

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1. The hysteresis voltage of the Schmitt trigger switching level. Guaranteed by design and comprehensive evaluation, not tested in production.
2. If there is negative current in the adjacent pin, the leakage current may be higher than the maximum value.

Input and output AC characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-27 I/O AC characteristics

VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
5V (4.5~5.5)	Low (DR=1)	Slow (SR=1)	25	3.1	3.9	6.5	5	7.2	14
			50	5.7	6.5	11	6.5	8.8	16
			100	11	13	20	10	12	21
		Fast (SR=0)	25	2.9	3.4	5.4	4.5	6.5	12
			50	5.6	6.3	10	6	8.1	14.2
			100	11	12.3	19.5	9	11.3	19.1
	High (DR=0)	Slow (SR=1)	25	1.8	2.5	4.1	4.2	6.7	13
			50	3	3.9	6.2	5	7.5	15
			100	5.6	6.5	10.2	6.4	9	17
		Fast (SR=0)	25	1.6	2.1	3.4	3.7	5.9	12
			50	2.9	3.5	5.5	4.4	6.6	13
			100	5.5	6.2	10	5.9	8	15
3.3V (2.7~3.6)	Low (DR=1)	Slow (SR=1)	25	4	5.5	11	6.6	10	20
			50	7.5	9.5	18	8.5	12	24
			100	15	17	32	13	16	31
		Fast (SR=0)	25	3.8	4.9	9.2	5.9	8.8	18
			50	7.3	8.8	16.2	7.8	10.8	21.2
			100	14.2	16.7	30.5	12	15	29
	High (DR=0)	Slow (SR=1)	25	2.4	3.7	7.2	5.5	8.5	17.1
			50	3.9	5.5	10.5	6.5	9.6	19.2
			100	7.3	9.3	17.2	8.4	12	23
		Fast (SR=0)	25	2	3.1	5.9	4.9	7.6	16
			50	3.7	4.9	9.5	5.8	8.7	18
			100	7.2	8.8	17	7.7	11	22

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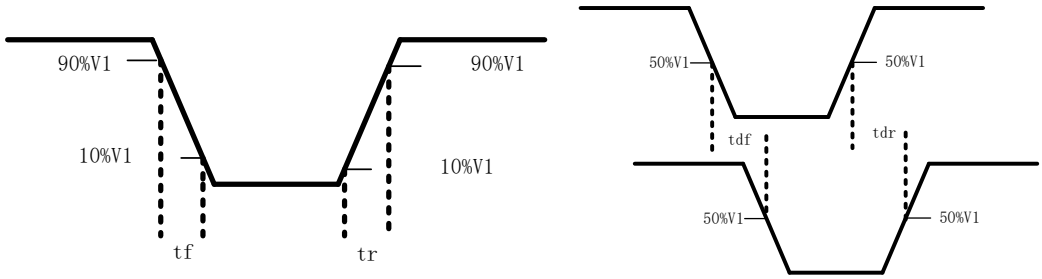
VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
1.8V (1.62~1.98)	Low (DR=1)	Slow (SR=1)	25	8	12	22	14	23	44
			50	15	20	36	18	27	52
			100	29	36	65	26	36	66
		Fast (SR=0)	25	7.5	10.5	16.4	12.25	20	40
			50	14.5	18.5	33	16.5	24.2	47
			100	28	35	62	24	33	62
	High (DR=0)	Slow (SR=1)	25	4.6	8	15.4	12	20.2	40
			50	7.6	11.8	22	14	22.5	44
			100	11.5	19.5	36	17.5	26.7	52
		Fast (SR=0)	25	4	6.9	14	10.5	18	36
			50	7.3	11	20	12.3	20	40
			100	15	18.5	33	16	25	47

Figure 4-9 I/O AC characteristic definition



4.3.13 NRST pin characteristics

NRST pin is integrated with pull-up resistor. Unless otherwise specified, the parameter test conditions in the following table are based on Table 4-4.

Table 4-28 NRST pin characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST low level input voltage	1.8V~5.5V	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	1.8V~5.5V	0.75VDD	-	-	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	1.8V~5.5V	115	220	315	mV
R_{PU}	Weak pull-up equivalent resistor (2)	1.8V~5.5V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	1.8V~2V	-	-	100	ns
		3V~3.6V	-	-	100	
		4.5V~5.5V	-	-	50	

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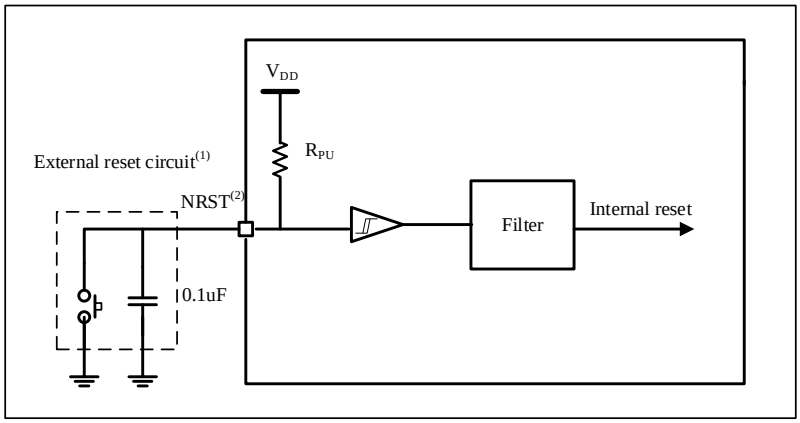
$V_{NF(NRST)}$[1]	NRST input unfiltered pulse	1.8V~2V	650	-	-	ns
		3V~3.6V	300	-	-	
		4.5V~5.5V	200	-	-	

1. Guaranteed by design, note tested in production
2. The pull-up resistor is designed as true resistor for a not switchable PMOS implementation, The resistance of this PMOS switch is very small (about 10%).

Figure 4-10 NRST pin protection recommended circuit design



1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin can be lower than the maximum $V_{IL\ (NRST)}$, otherwise the MCU cannot be reset.

4.3.14 TIM characteristics

Table 4-29 TIM [1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	fTIMxCLK= 48MHz	1	-	$t_{TIMxCLK}$
		fTIMxCLK= 48MHz	20.8	-	ns
f_{EXT} [2]	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK/2}$	MHz
		fTIMxCLK= 48MHz	0	24	MHz
Res_{TIM}	Timer resolution	fTIMxCLK= 48MHz	-	16	bit
$t_{COUNTER}$	Select the internal clock, 16-bit counter clock cycle	fTIMxCLK= 48MHz	1	65536	$t_{TIMxCLK}$
		fTIMxCLK= 48MHz	0.0208	1365	μs
t_{MAX_COUNT}	Maximum count	fTIMxCLK= 48MHz	-	65536x65536	$t_{TIMxCLK}$
		fTIMxCLK= 48MHz	-	89.478	s

1. TIMx is generic name, representing TIM1~TIM8
2. Only applicable to advanced timers and general-purpose timers, not applicable to basic timers.

4.3.15 I2C characteristics

The parameter test conditions in the following table are based on Table 4-4.

The I2C interface complies with the standard I2C communication protocol.

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But SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD is turned off, but it still exists.

Table 4-30 I2C interface characteristics

Symbol	Parameter	Standard model		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz
$th_{(STA)}$	Start condition holding time (1)	4.0	-	0.6	-	0.26	-	μs
$tw_{(SCLL)}$	SCL Clock Low Time (1)	4.7	-	1.3	-	0.5	-	μs
$tw_{(SCLH)}$	SCL clock high time (1)	4.0	-	0.6	-	0.26	-	μs
$tsu_{(STA)}$	Setup time of repeated starting conditions (1)	4.7	-	0.6	-	0.26	-	μs
$th_{(SDA)}$	SDA data hold time (1)	-	3.4	-	0.9	-	0.4	μs
$tsu_{(SDA)}$	Setup time of SDA (1)	250	-	100	-	50	-	ns
$tr_{(SDA)}$ $tr_{(SCL)}$	SDA and SCL rising time (1)	-	1000	20+0.1Cb	300	-	120	ns
$tf_{(SDA)}$ $tf_{(SCL)}$	SDA and SCL falling time (1)	-	300	20+0.1Cb	300	-	120	ns
$tsu_{(STO)}$	Stop condition setup time(1)	4.0	-	0.6	-	0.26	-	μs
$tw_{(STO:STA)}$	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
C_b	Capacity load per bus (1)	-	400	-	400	-	200	pf
$tv_{(SDA)}$	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs
$tv_{(ACK)}$	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz.To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

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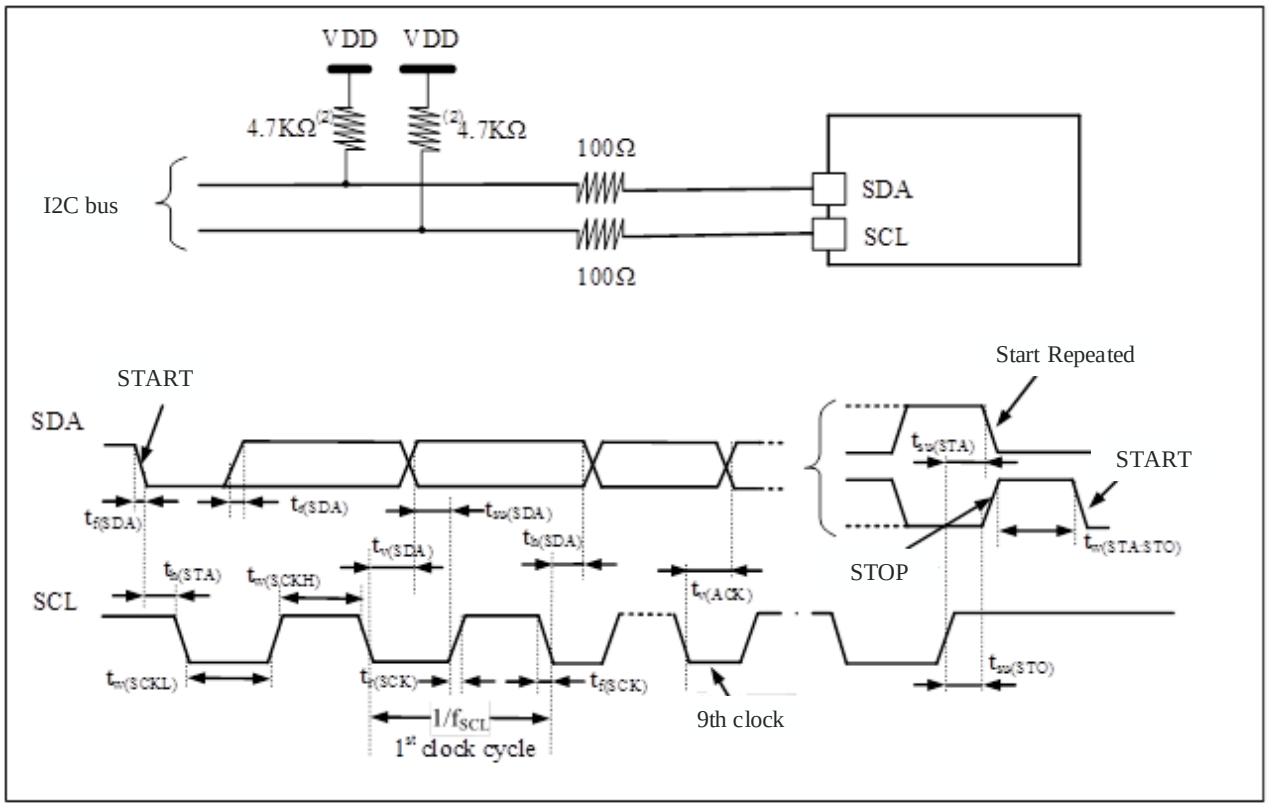
Figure 4-11 I2C bus AC waveform and measurement circuit (1)



1. The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.16 SPI/I2S characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-31 SPI characteristics (4)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	12	MHz
		Slave mode		-	12	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rising and falling time	Load capacitance: C = 30pF		-	20	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI Slave mode		45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data entry setup time	Master mode	SPI1	5	-	ns
			SPI2/3	5	-	
$t_{su(SI)}$(1)		Slave mode	SPI1	5	-	
			SPI2/3	4.5	-	

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$t_{h(MI)}$(1)	Data entry hold time	Master mode		6	-	ns
$t_{h(SI)}$(1)		Slave mode		7	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 12MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Disabled time for data output	Slave mode		2	10	ns
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after the enabled edge)	SPI1	-	13	ns
			SPI2/3	-	11.1	
$t_{v(MO)}$(1)		Master mode (after the enabled edge)	SPI1	-	8.7	
			SPI2/3	-	10.7	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after the enabled edge)		7.7	-	ns
$t_{h(MO)}$(1)		Master mode (after the enabled edge)		0	-	

2. The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.

3. The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data wire in the high resistance state.

Figure 4-12 SPI sequence diagram - slave mode and CPHA=0

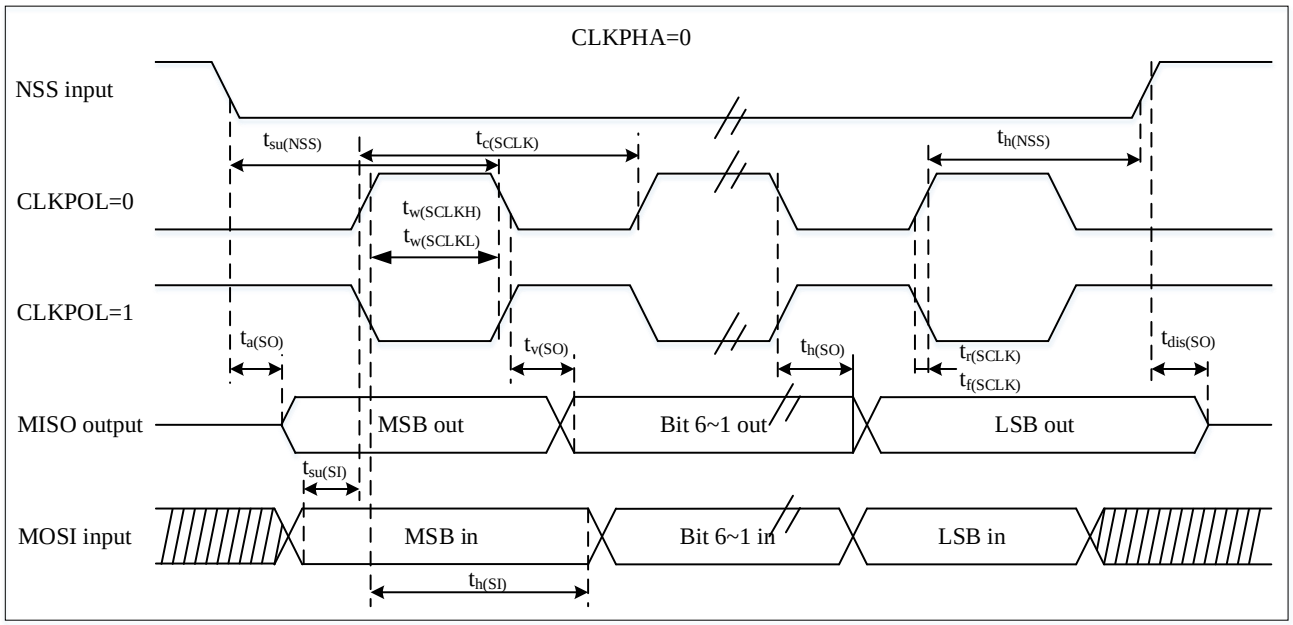

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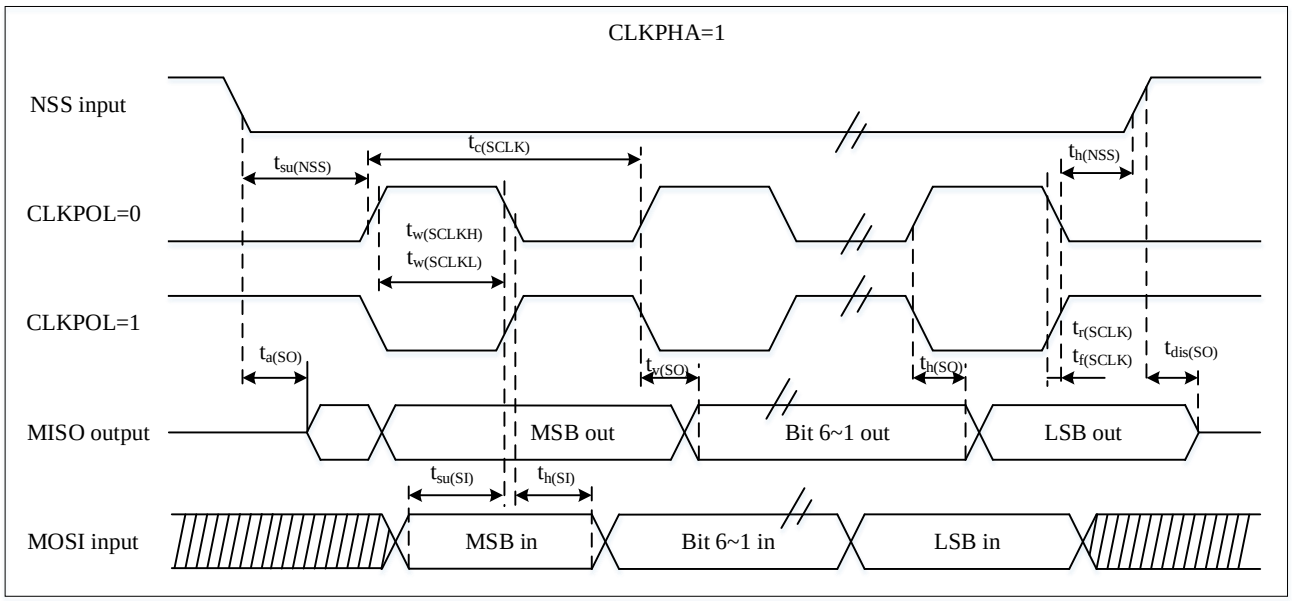
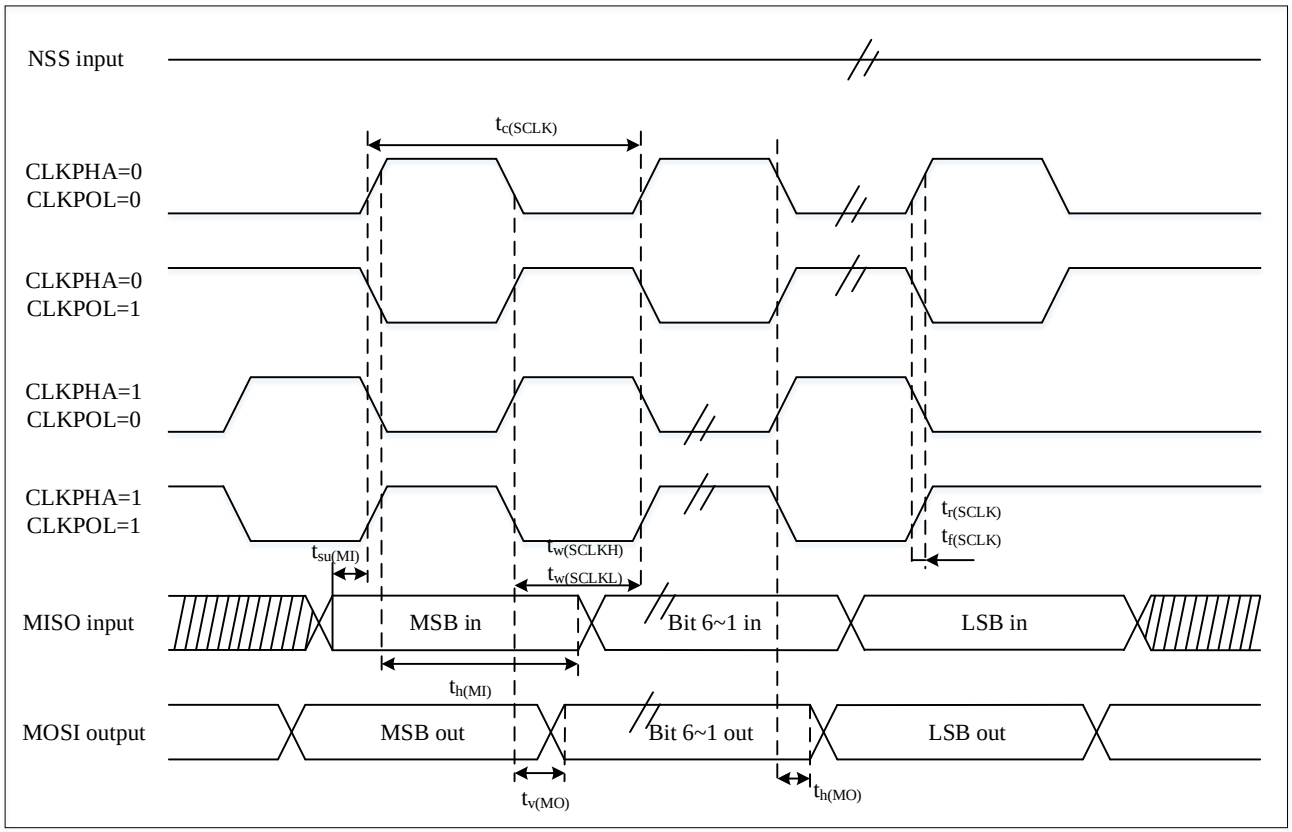
Figure 4-13 SPI sequence diagram - slave mode and CPHA=1(1)



1. The measurement points were set at the CMOS level of 0.3 V_{DD} and 0.7 V_{DD}.

Figure 4-14 SPI timing diagram-master mode (1)



1. The measurement points are set at CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

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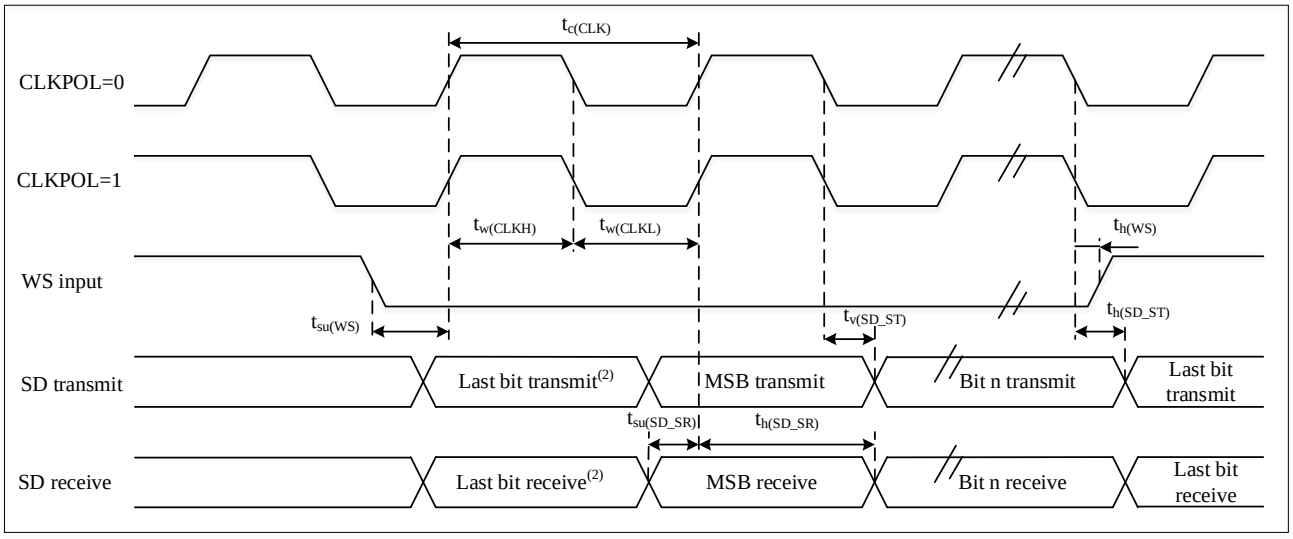
Table 4-32 I2S characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
DuCy(SCK)	I2S clock duty cycle	I2S Slave mode	30	70	%
f_{CLK} $1/t_{c(CLK)}$	I2S clock frequency	Master mode (32bit)	-	2*Fs(3)*32	Hz
		Slave mode (32bit)	-	2*Fs(3)*32	
$t_{r(CLK)}$	I2S clock rising and falling time	Load capacitance: C_L = 50pf	-	8	ns
$t_{v(WS)}$ (1)	WS validity time	Master mode	12.5	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	3.5	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	4	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, fpclk = 16mhz, audio 48khz	312.5	-	
$t_{w(CLKL)}$(1)			345	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	Master receiver	3.6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	3.8	-	
$t_{h(SD\_MR)}$(1)(2)	Data entry hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after the enabled edge)	-	29	ns
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave generator(after the enabled edge)	7.5	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	Master generator(after the enabled edge)	-	12.6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master generator(after the enabled edge)	-6.5	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Relying on f_{PCLK}.For example, if f_{PCLK}=8MHz, then T_{PCLK}=1/ f_{PCLK} =125ns.
3. F_S value audio sampling frequency, frequency range 8 KHz ~ 96 KHz.

Figure 4-15 I2S slave mode timing diagram (Philips protocol) (1)



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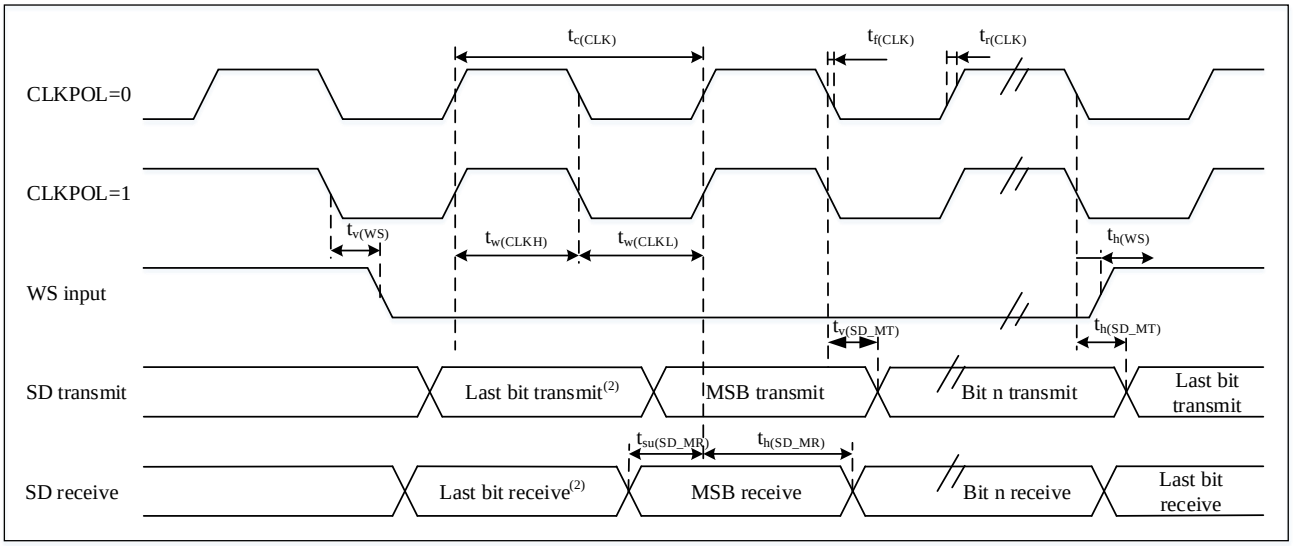
1. The measuring point is set at the CMOS level: 0. $3V_{DD}$ and 0. $7V_{DD}$.
2. Transmit/receive of the previous byte. There is no transmit/receive of this last bit before the first byte.

Figure 4-16 I2S master mode timing diagram (Philips protocol) (1)



1. The measuring point is set at the CMOS level: 0. $3V_{DD}$ and 0. $7V_{DD}$.
2. Transmit/receive of the previous byte. There is no transmit/receive of this last bit before the first byte.

4.3.17 Controller area network (CAN) interface characteristics

See Section 1 for details on the features of the input/output alternate function pins (CAN_TX and CAN_RX).

4.3.18 ADC characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-33 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Supply voltage	-	2.4	3.3	5.5	V
V_{REF+}	Positive reference voltage	-	2.4	-	VDDA	V
f_{ADC}	ADC clock frequency	-	-	-	18	MHz
f_s(1)	Sampling rate	-	0.03	-	1	Msps
V_{AIN}	Conversion voltage range	-	0	-	VREF+	V
R_{AIN}(1)	External input impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC input resistance	V_{DDA} =3.0v	-	800	-	Ω
C_{ADC}(1)	Internal sample and hold capacitor	-	-	26	30	pF
SNDR	Signal noise distortion ration	V_{DDA} =3.3v	-	68	-	dB
T_S (1)	Sampling cycle	-	6	-	-	$1/f_{ADC}$
t_{STAB} (1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV} (1)	Conversion time	-	12			$1/f_{ADC}$

1. Guaranteed by design and comprehensive evaluation, not tested in production.

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Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

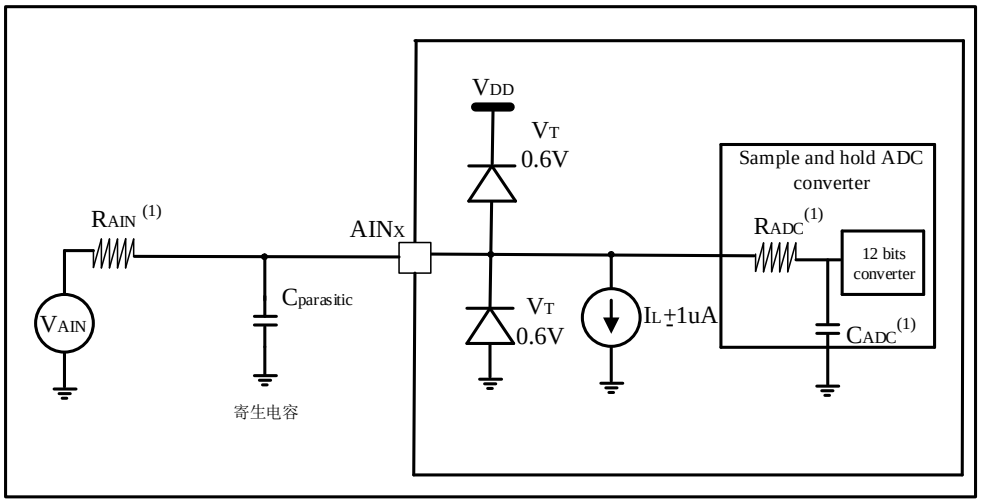
The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-34 ADC accuracy (1)

Symbol	Parameter	Conditions	Typ	Max(2)	Unit
EG	Gain error	V_{REF+} = 3.3V, T_A = 25 ℃, sample rate = 1MSPS, Vin = 0.05V_{DDA} ~ 0.95V_{DDA}	±2	±5	LSB
EO	Offset error		±0.5	±2.0	
ED	Differential linearity error		±0.6	1.5	
EL	Integral linearity error		±1.5	2.5	
ENOB	Effective number of bits		10.5	-	Bits

1. The relationship between the negative injection current and ADC accuracy: the need to avoid negative current is injected on any standard analog input pin, as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce negative injection current.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

Figure 4-17 ADC typical connection diagram



4.3.19 OPAMP characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-35 OPAMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	2.9	-	5.5	V
CMIR	Common mode voltage input range	-	0	-	V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage	-	-10	±4	10	mV
I_{LOAD}	Drive current	-	-	0.5	-	mA

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I_{DDA}	OPAMP current consumption	No load, quiescent mode	-	0.5	-	mA
CMMR	Common mode rejection ratio	-	-	70	-	dB
PSRR	Power supply rejection ratio	-	-	60	-	dB
GBW	Gain bandwidth	-	-	2.5	-	MHz
SR	Conversion rate	-		3	-	V/us
R_{LOAD}	Minimum impedance load	-	10	-	-	KΩ
C_{LOAD}	Maximum capacitive load	-	-	-	25	pF
$T_{STARTUP}$	Startup time	CLOAD ≤ 25 pf, RLOAD ≥ 10 kΩ, Follower configuration	-	3	5	μs
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 25pF, Rload = 10 KΩ	-	1	-	MHz
		GA Gain = 4, Cload = 25pF, Rload = 10 KΩ	-	0.5	-	
		GA Gain = 16, Cload = 25pF, Rload = 10 KΩ	-	0.125	-	
		GA Gain = 32, Cload = 25pF, Rload = 10 KΩ	-	0.0625	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.20 COMP characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-36 COMP characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.2	-	5.5	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	
T_{START}	Comparator startup time	normal mode		-	-	5	us
		low speed mode				15	
t_d	Propagation delay for 200 mV step with 100 mV overdrive	V_{DDA}>=2.2Vnormal mode		-	100		ns
		low speed mode			520		
V_{OFFSET}	Comparator input offset error	Full common mode range		-	±4	±20	mV
V_{hys}	Comparison of hysteresis voltage (high speed/low power consumption)	No hysteresis		-	0	-	mV
		Low hysteresis		-	10/8	-	
		Medium hysteresis		-	20/15	-	
		High hysteresis		-	30/25	-	
I_{DDA}	Comparator current consumption	High speed mode. Comparator is turned on, reference input compare voltage source(2) is turned off	Static	-	35	-	μA
			With 50 kHz ±100 mV overdrive square signal	-	36	-	

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		Low speed mode. Comparator is turned on, reference input compare voltage source(2) is turned off	Static	-	5	-	
			With 50 kHz ±100 mV overdrive square signal	-	6	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. For reference input compare voltage source. The static power is 74μA (Guaranteed by design), the maximum configurable voltage is V_{DDA}

4.3.21 Temperature sensor characteristics

The parameter test conditions in the following table are based on Table 4-4.

Table 4-37 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±2	-	℃
Avg_Slope(1)	Average slope	-	3.9	-	mV/℃
V_{25}(1)	Voltage at 25℃	-	1.3	-	V
t_{START}(1)	Startup time	-	11	22	μs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	-	1.87	6.43	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The shortest sampling time is obtained through multiple loops in the application.

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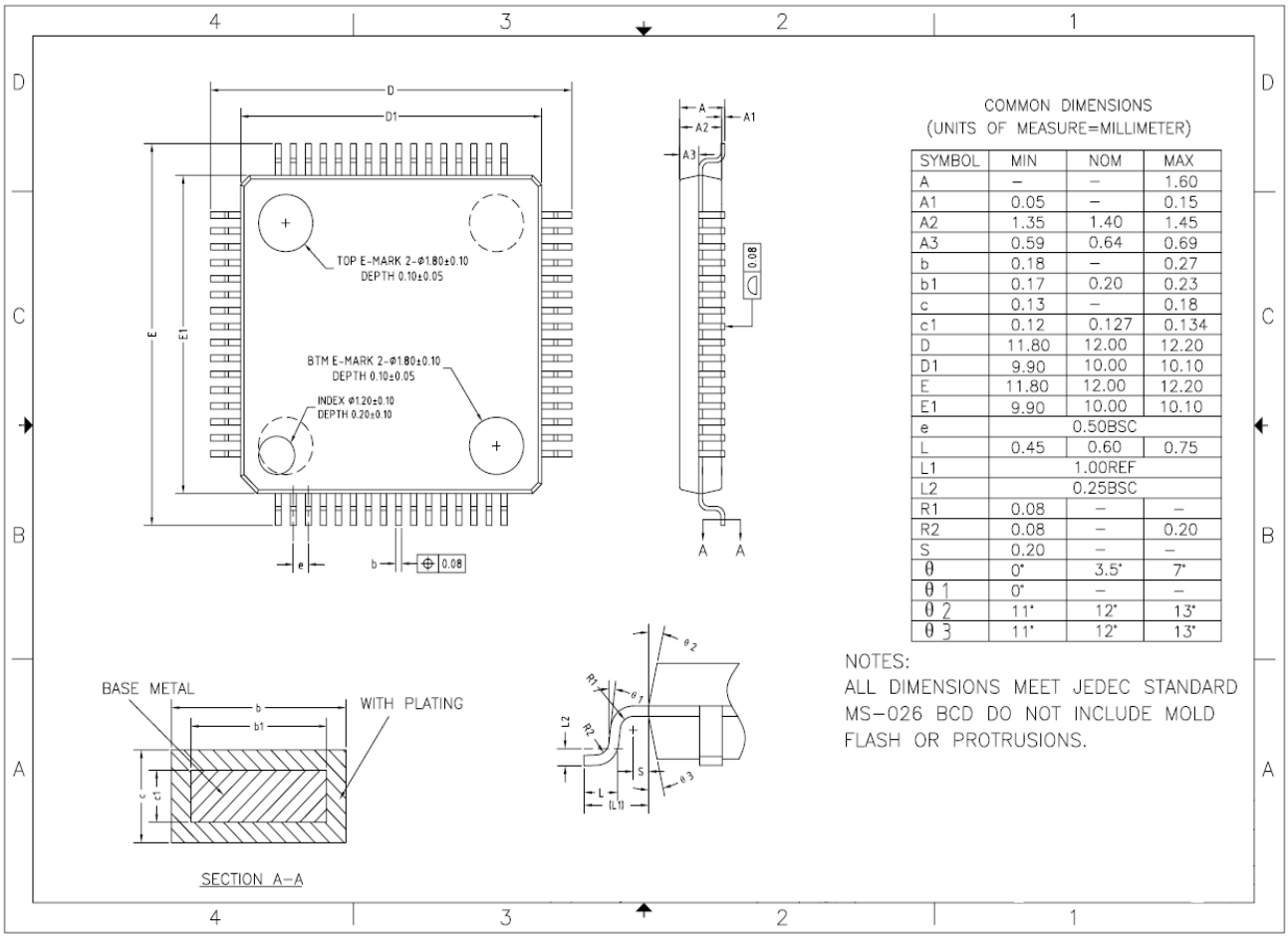
5 Package information

5.1 LQFP64

Figure 5-1 LQFP64 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-026 BCD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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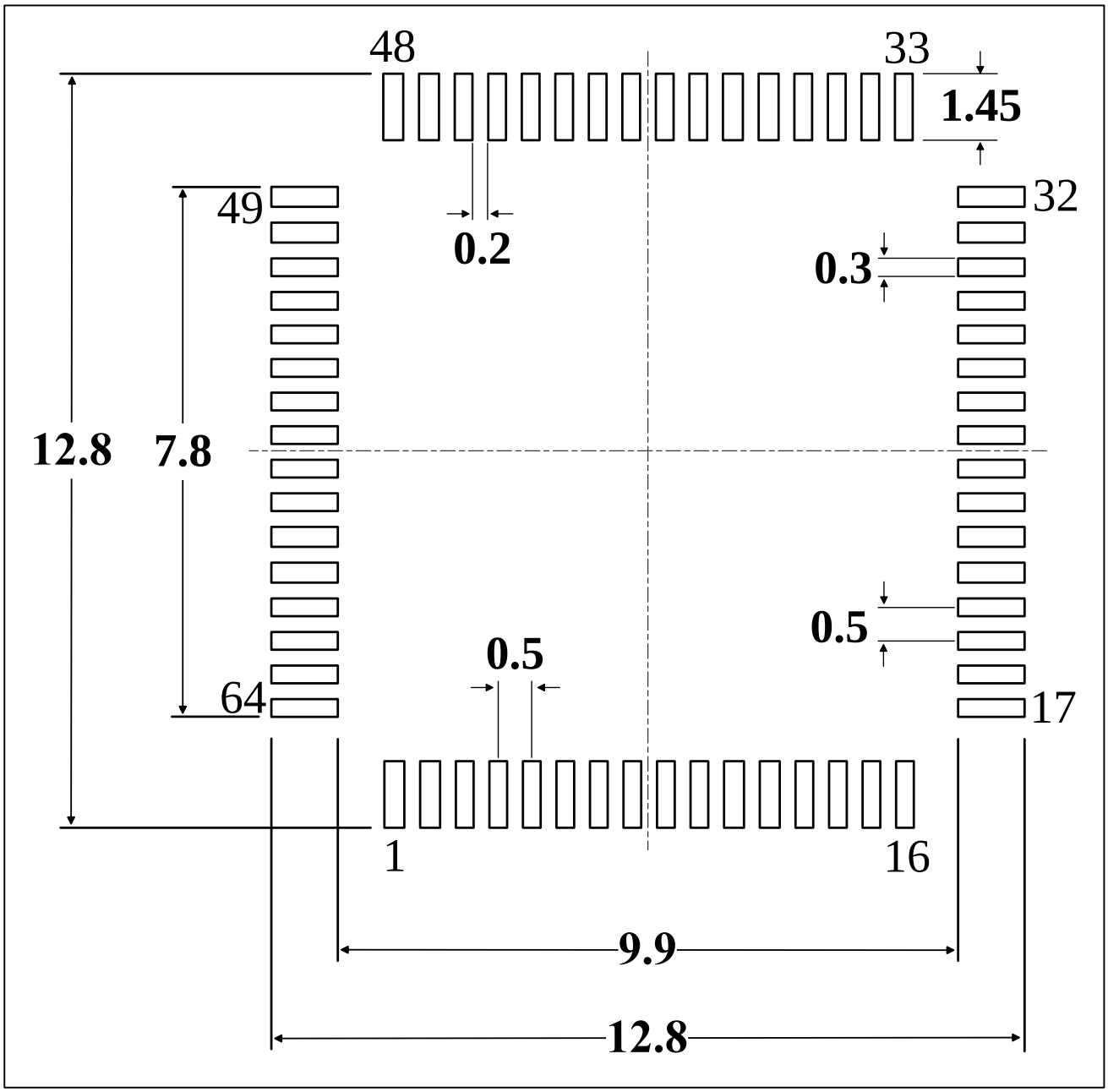
Figure 5-2 LQFP64 Recommended footprint (1)



1. Dimensions are expressed in millimeters.

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5.2 LQFP48

Figure 5-3 LQFP48 package outline

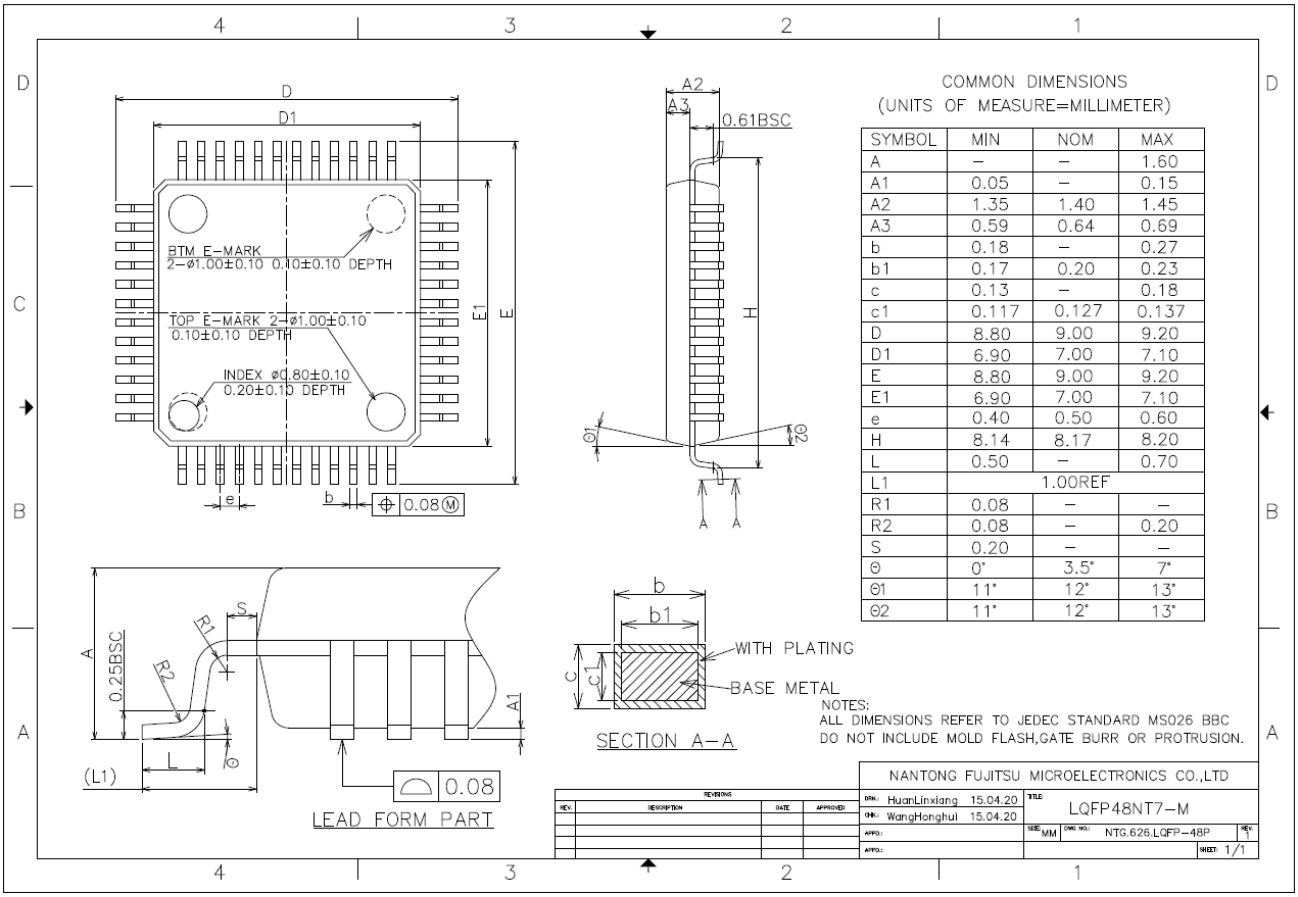

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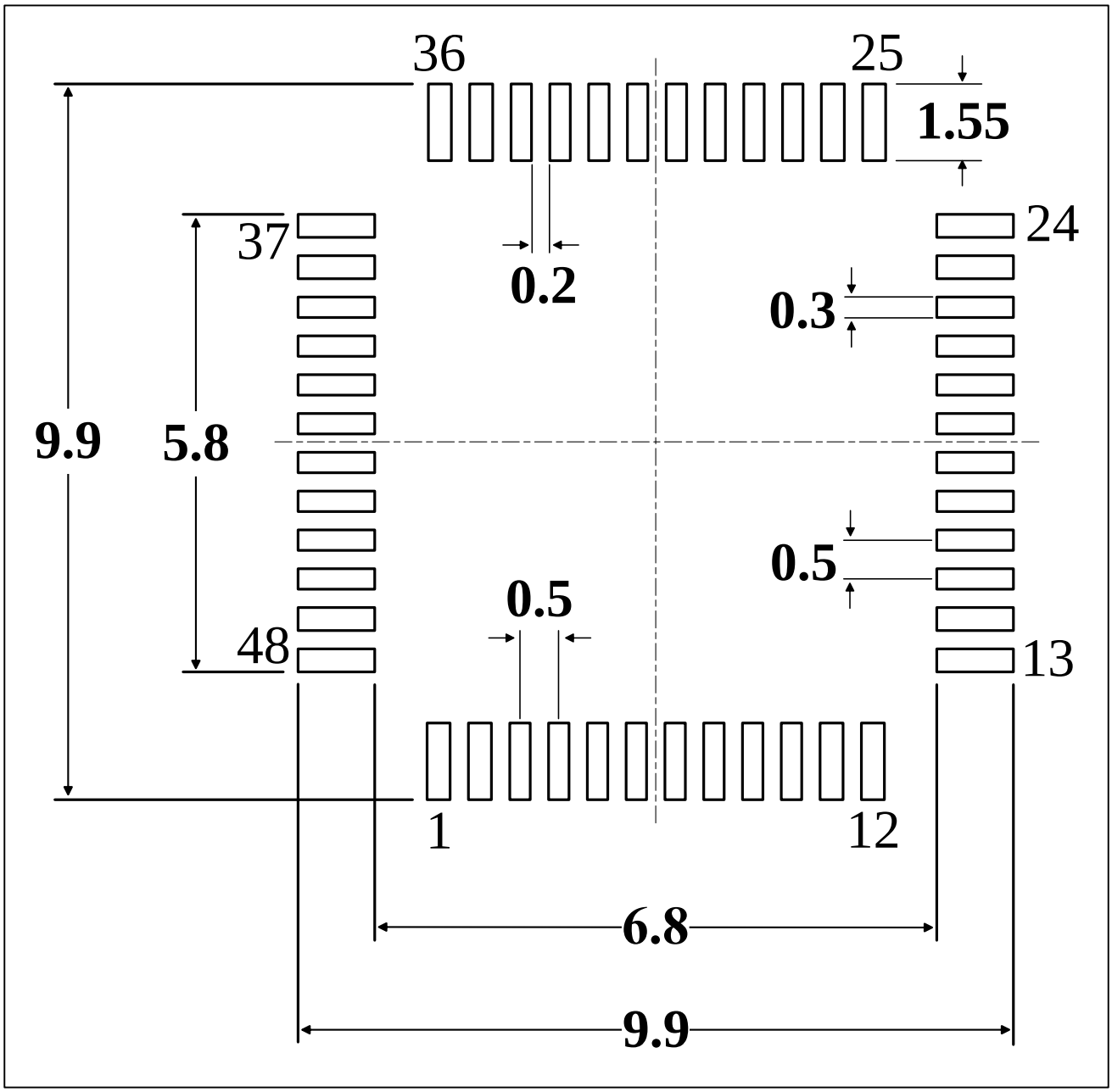
Figure 5-4 LQFP48 Recommended footprint (1)



1. Dimensions are expressed in millimeters.

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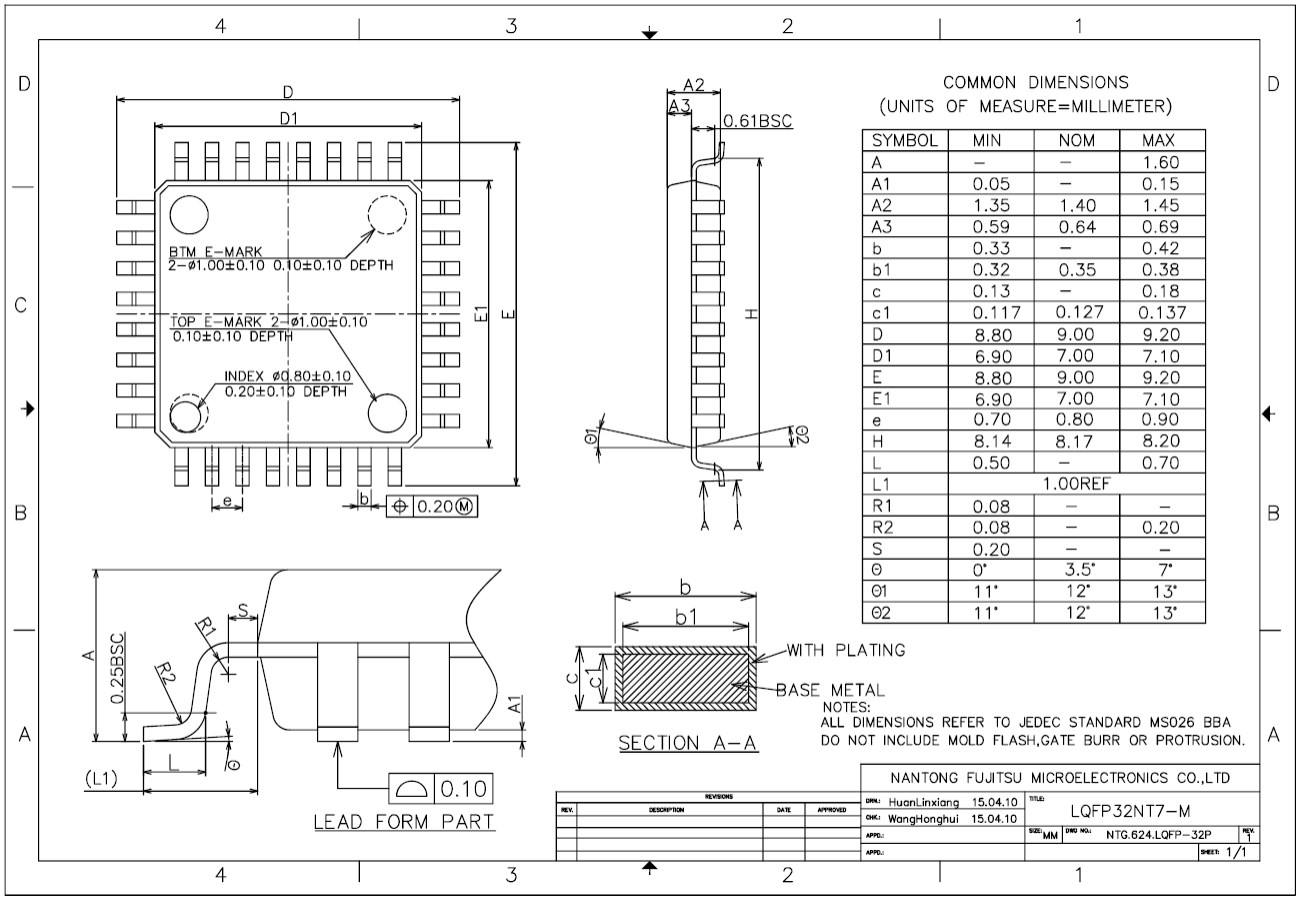
5.3 LQFP32

Figure 5-5 LQFP32 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	–	0.42
b1	0.32	0.35	0.38
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NANTONG FUJITSU MICROELECTRONICS CO.,LTD
DRN.: HuanLinxiang 15.04.10
CHK.: WangHonghui 15.04.10
APPD.:
APPD.:
TITLE: LQFP32NT7-M
SIZE: MM DWG NO.: NTG.624.LQFP-32P REV.: 1
SHEET: 1/1

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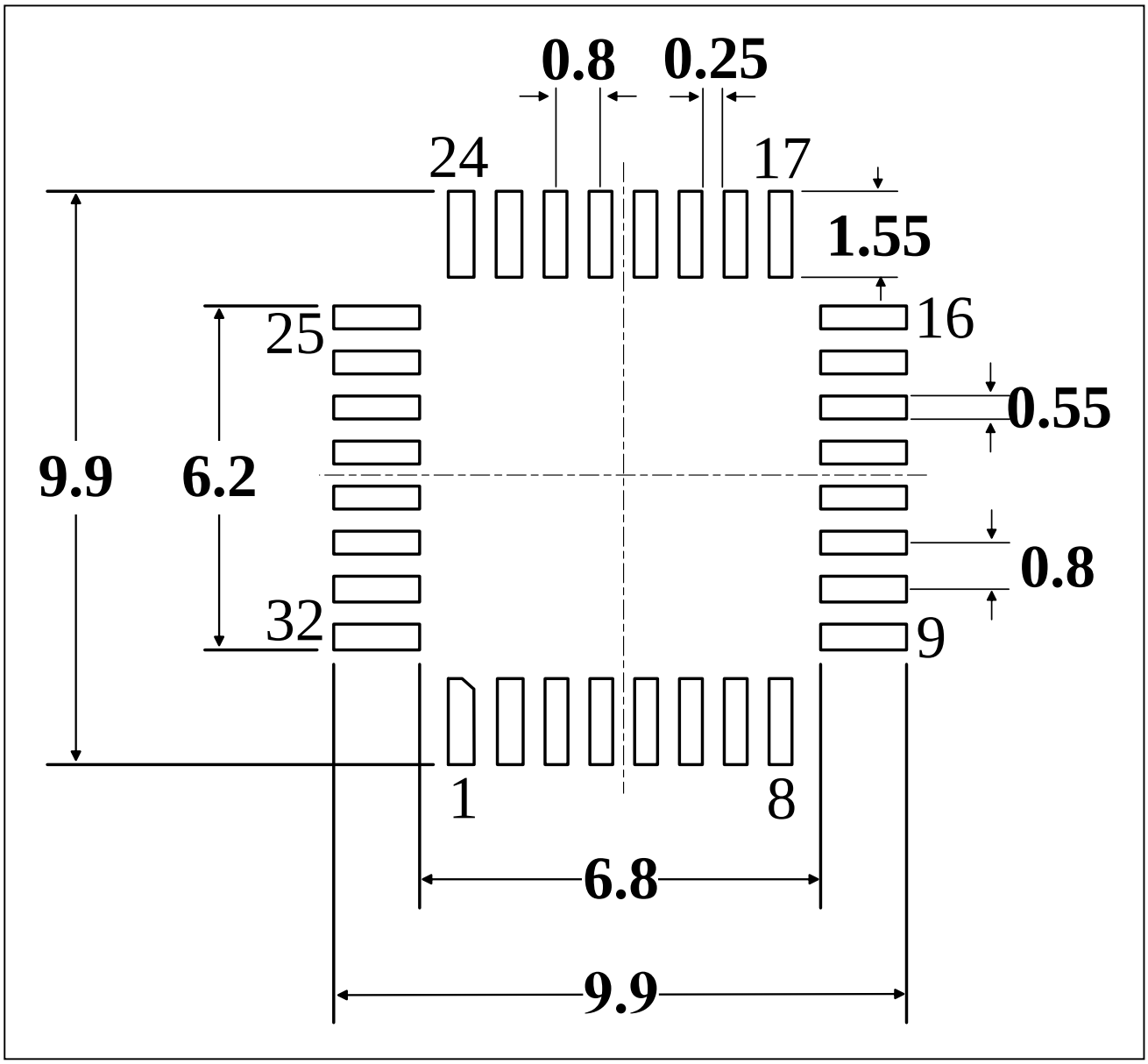
Figure 5-6 LQFP32 Recommended footprint (1)



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5.4 QFN32

Figure 5-7 QFN32 package outline

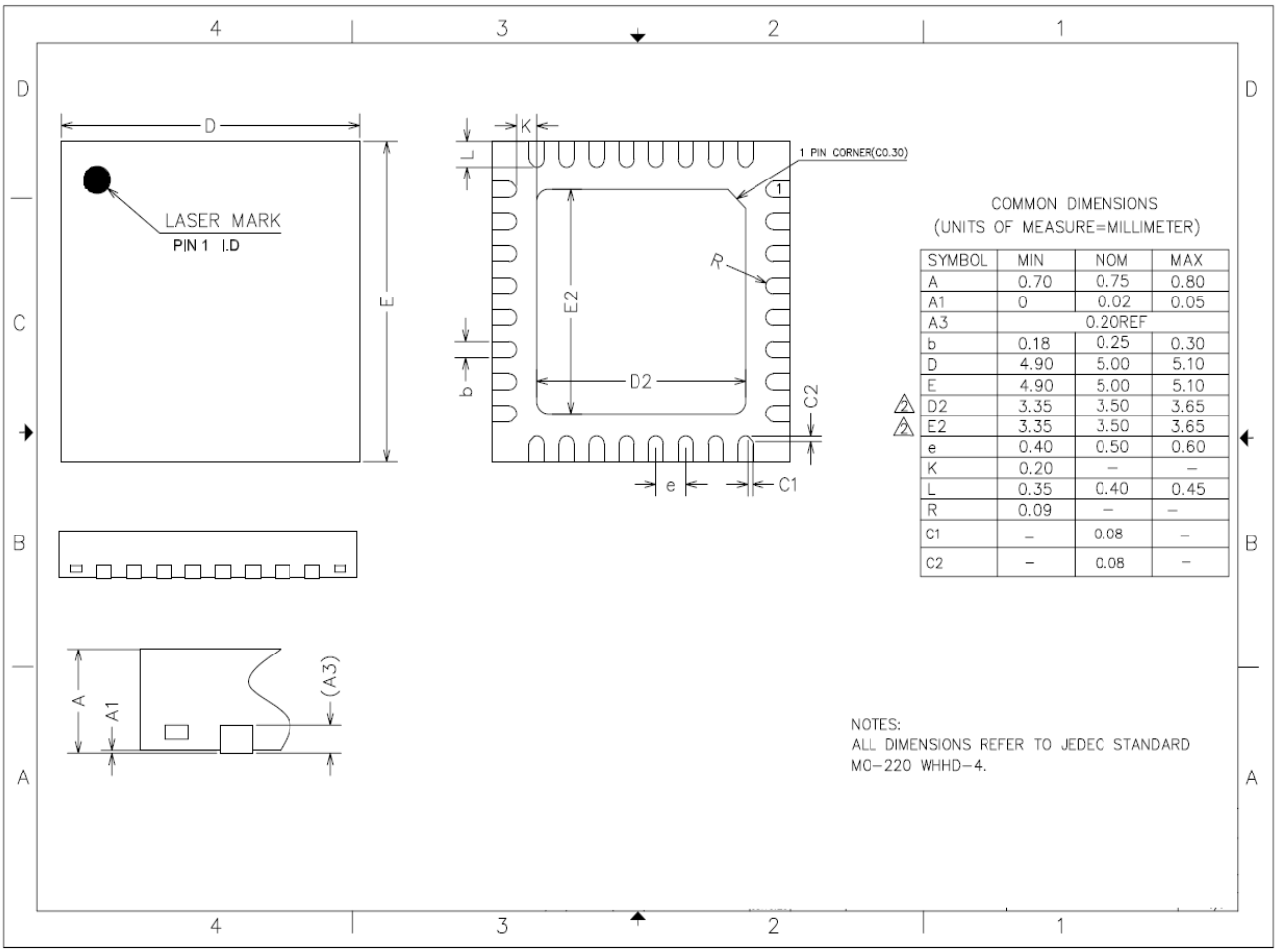

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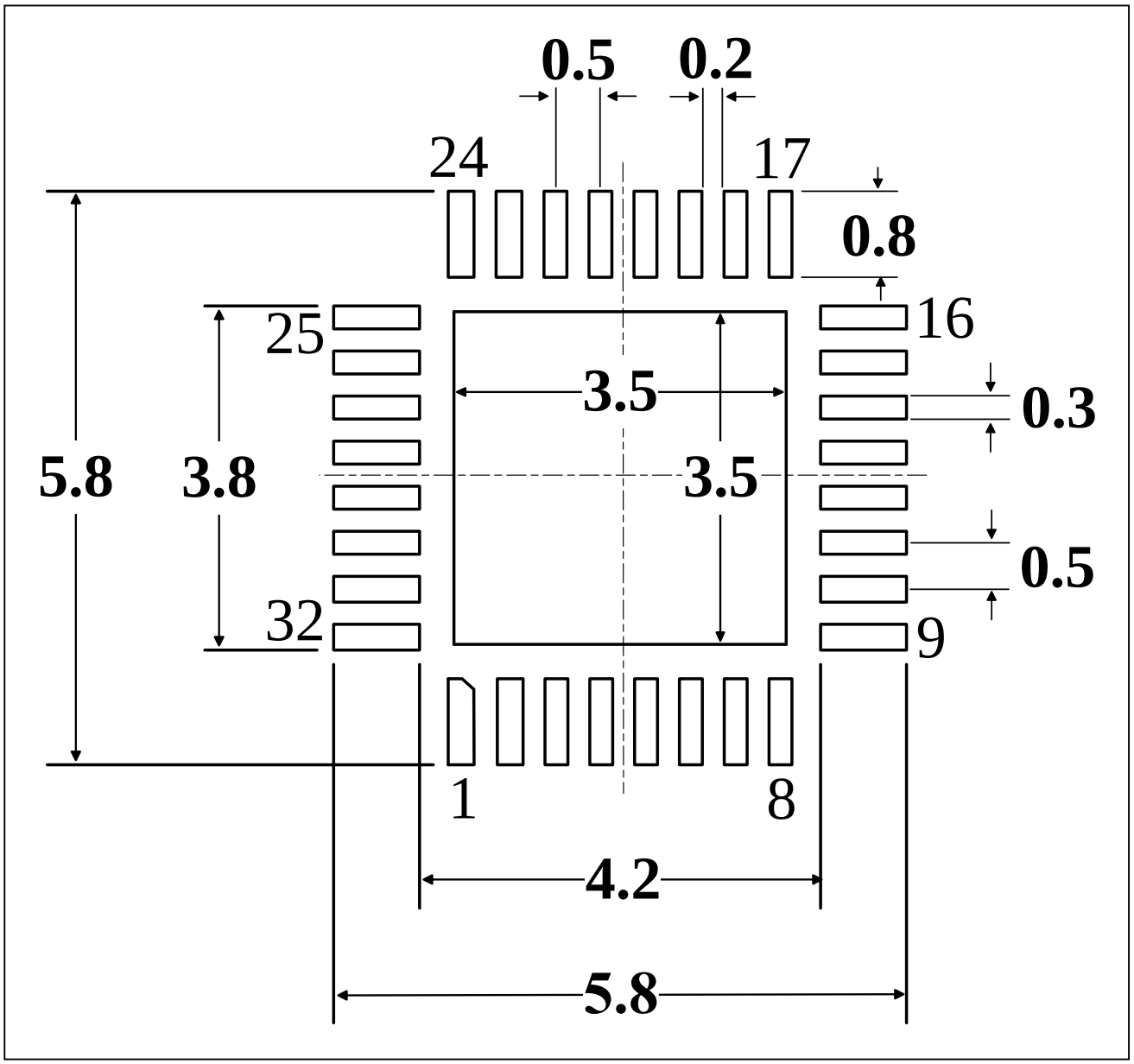
Figure 5-8 QFP32 Recommended footprint (1)



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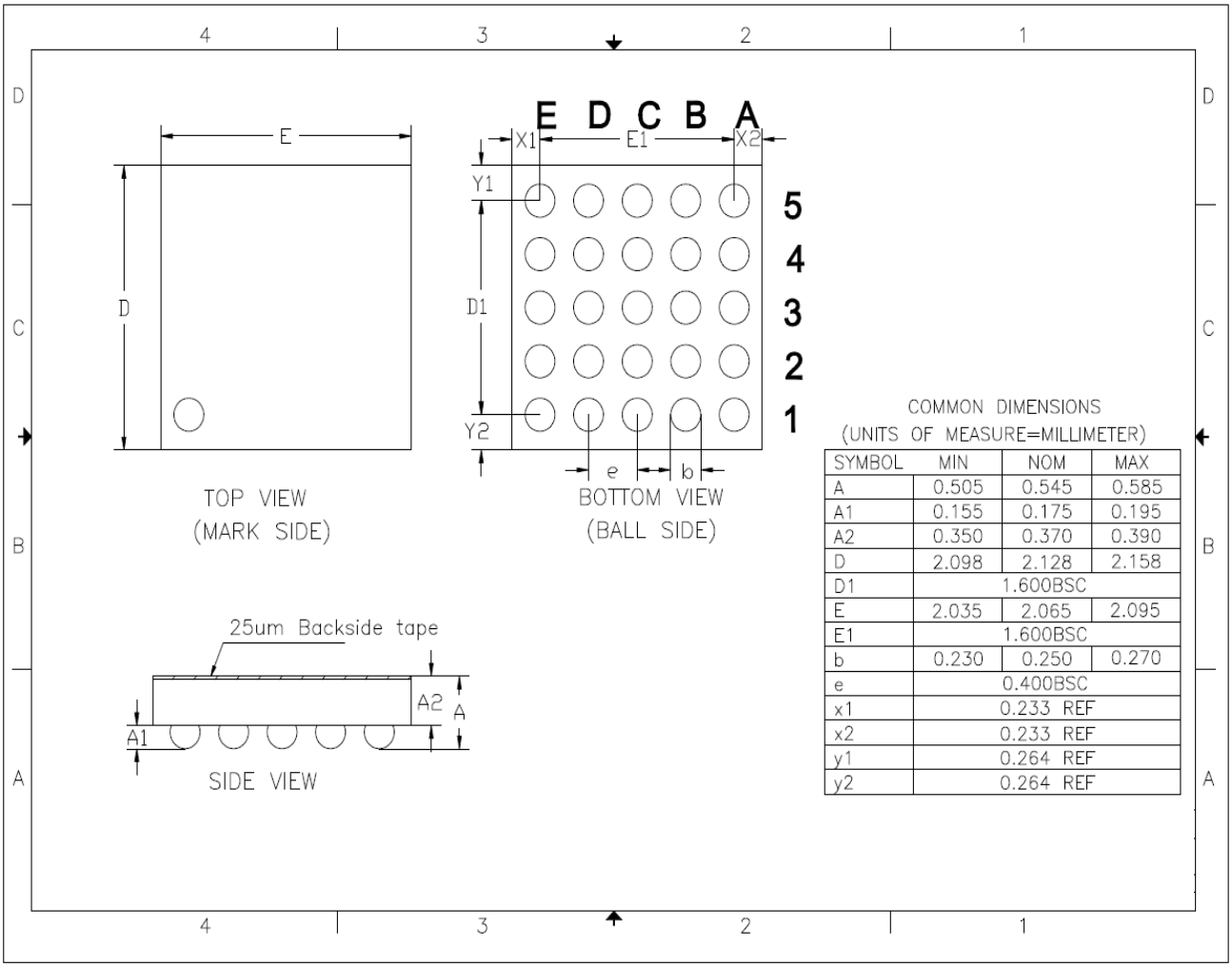
5.5 WLCSP25

Figure 5-9 WLCSP25 package outline



SYMBOL	MIN	NOM	MAX
A	0.505	0.545	0.585
A1	0.155	0.175	0.195
A2	0.350	0.370	0.390
D	2.098	2.128	2.158
D1		1.600BSC	
E	2.035	2.065	2.095
E1		1.600BSC	
b	0.230	0.250	0.270
e		0.400BSC	
x1		0.233 REF	
x2		0.233 REF	
y1		0.264 REF	
y2		0.264 REF	

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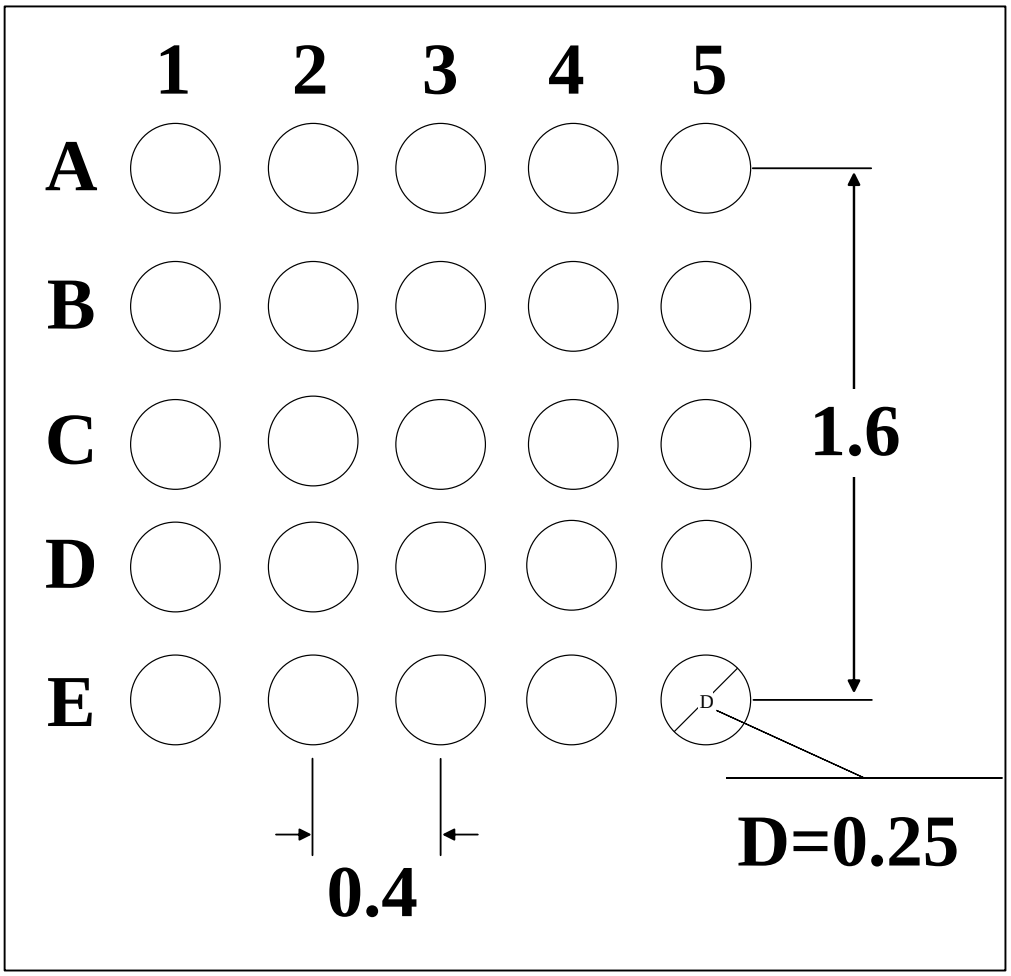
Figure 5-10 WLCSP25 Recommended footprint (1)



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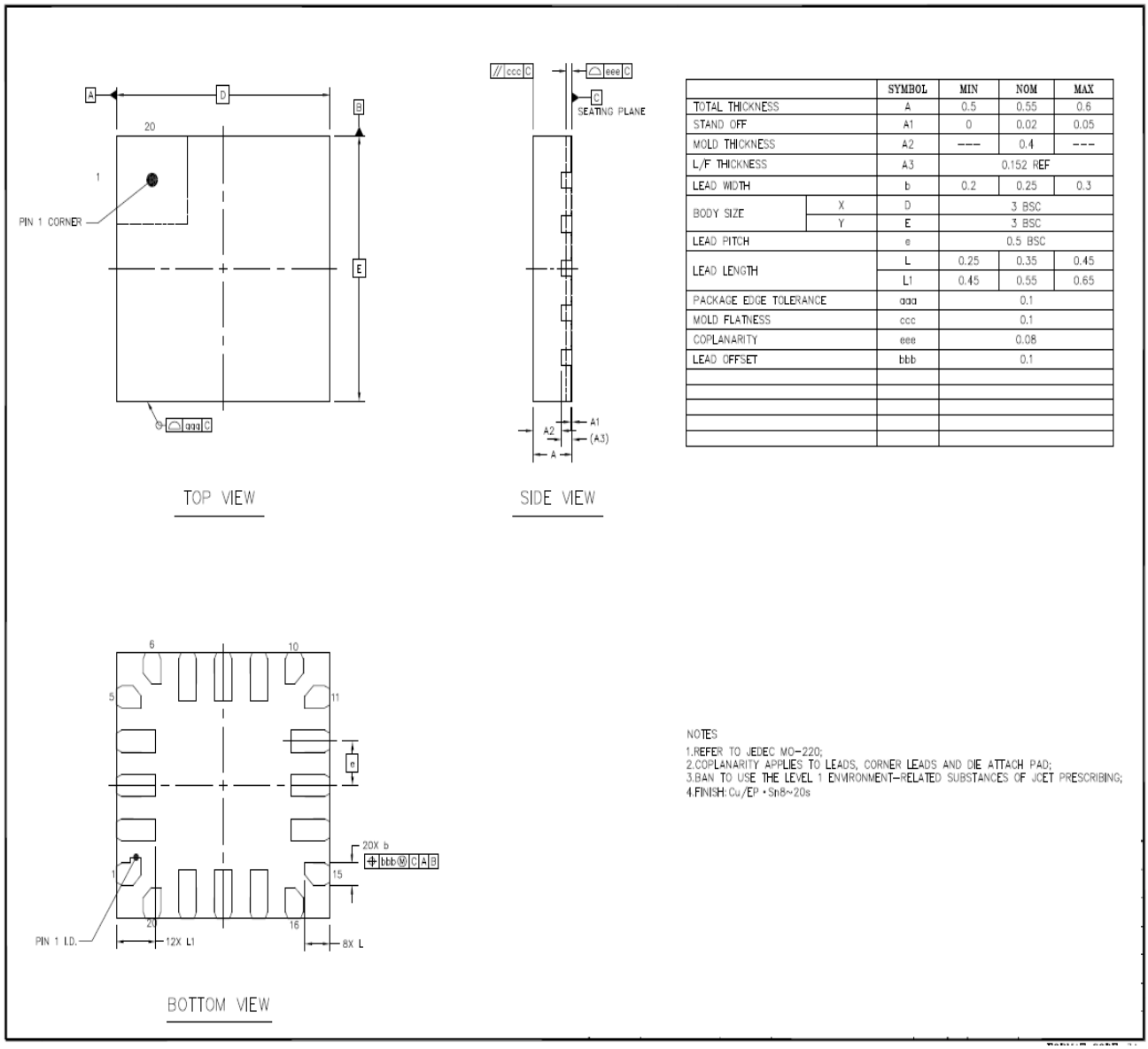
5.6 UFQFPN20

Figure 5-11 UFQFPN20 package outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JOET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

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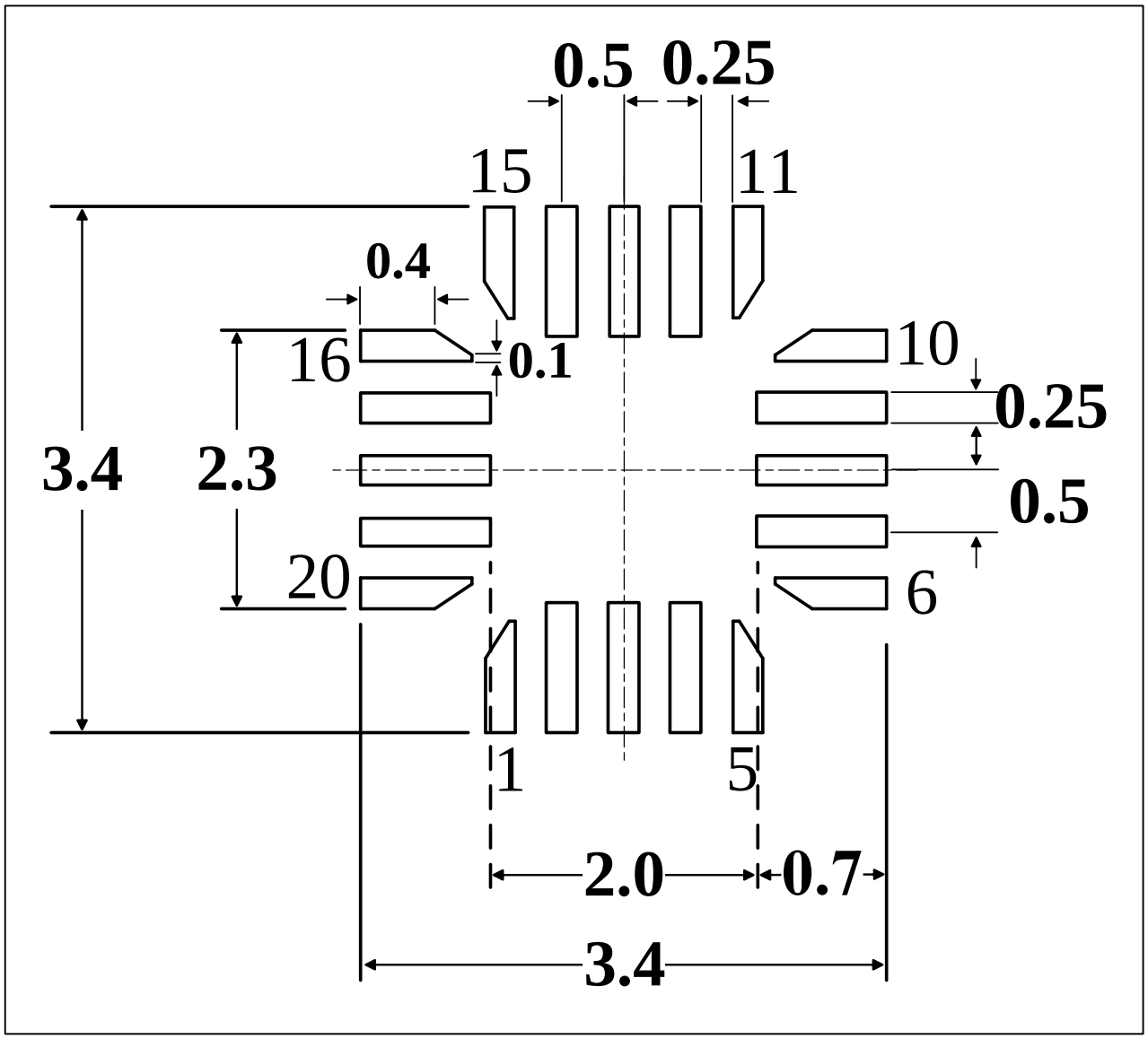
Figure 5-12 UFQFPN20 Recommended footprint (1)



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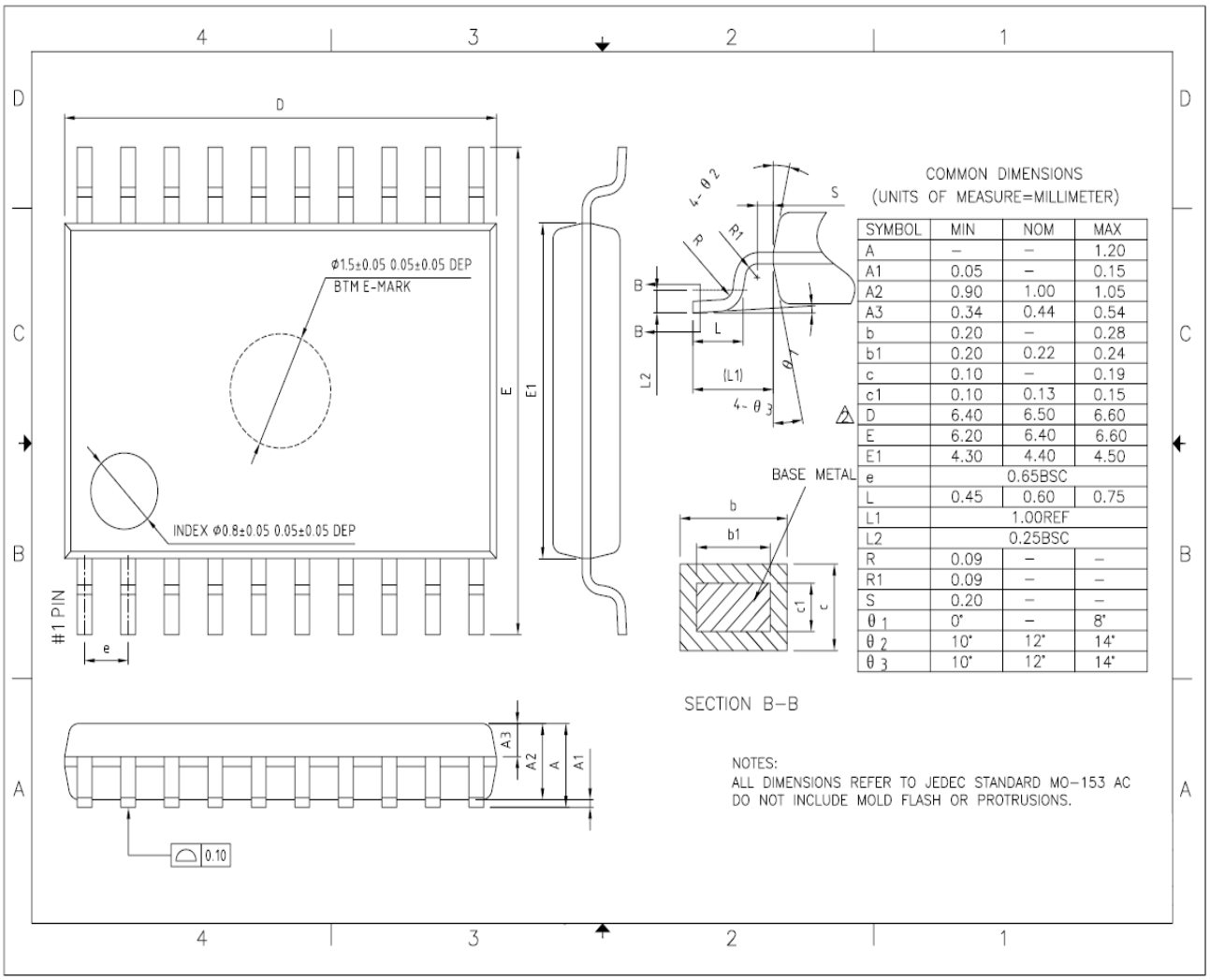
5.7 TSSOP20

Figure 5-13 TSSOP20 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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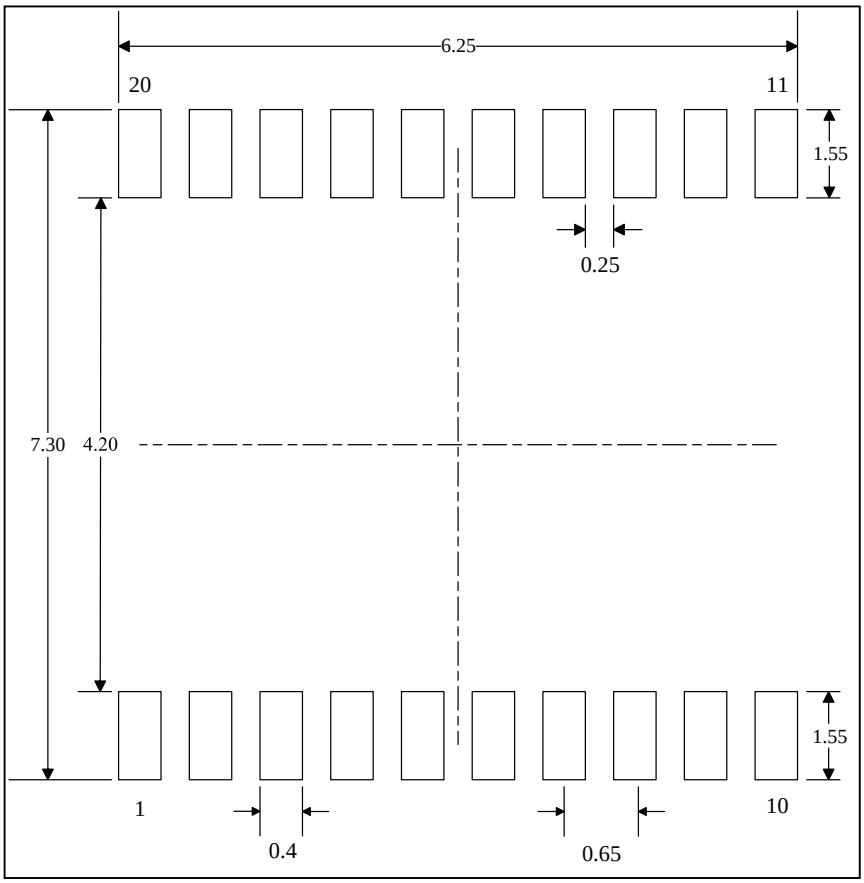
Figure 5-14 TSSOP20 Recommended footprint (1)



1. Dimensions are expressed in millimeters.

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5.8 Screen printing instructions

Figure 5-15 Screen printing instructions

Figure 5-16 LQFP64/LQFP48/LQFP32/QFN32 screen printing instructions

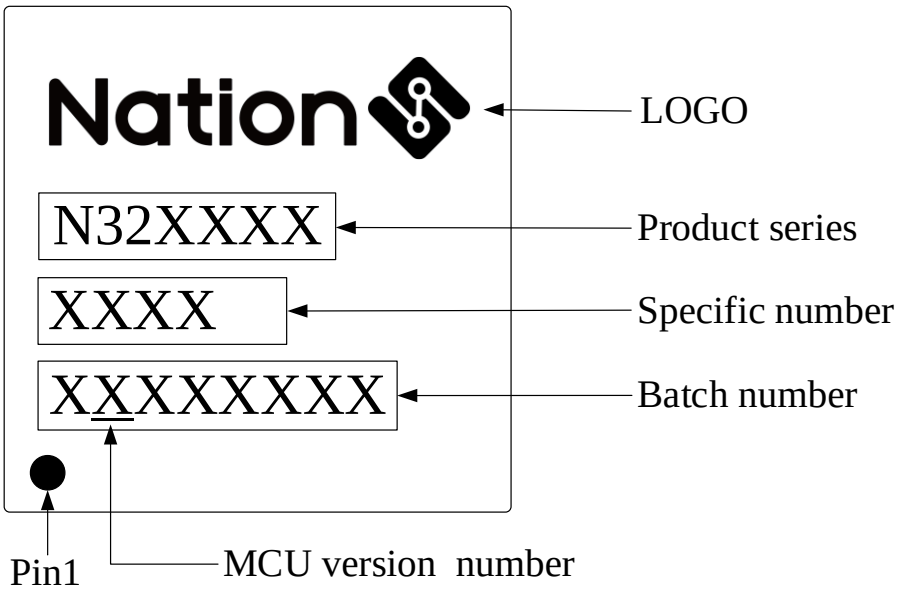

Figure 5-17 TSSOP20 screen printing instructions

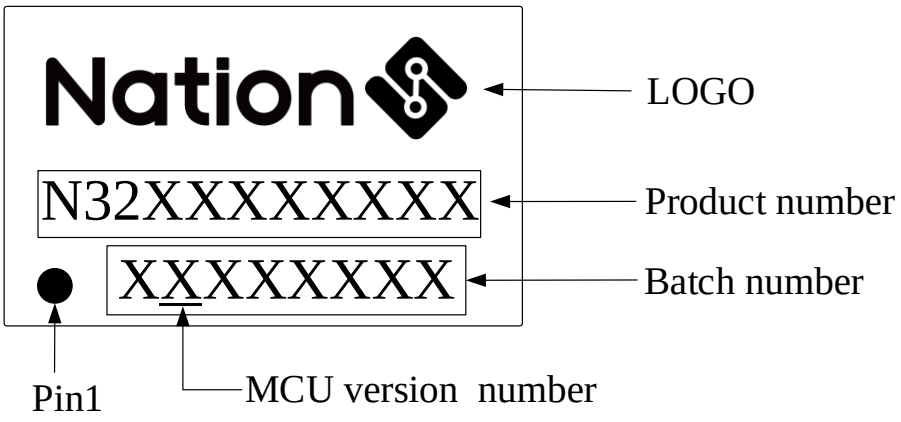

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Figure 5-18 UFQFPN20 screen printing instructions

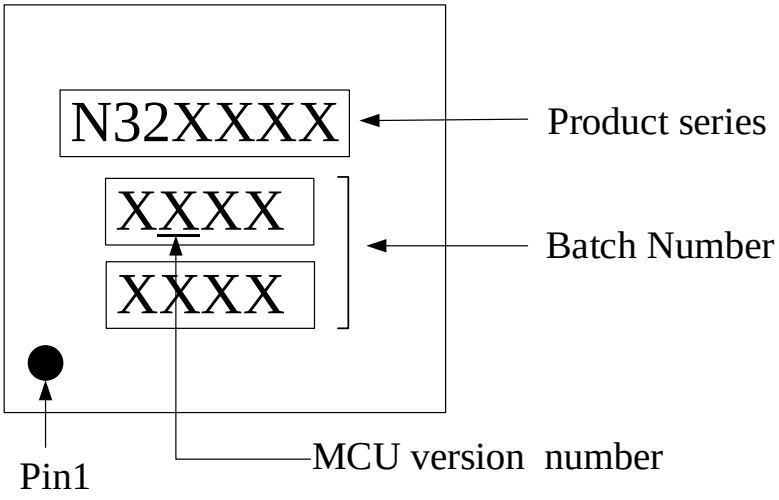
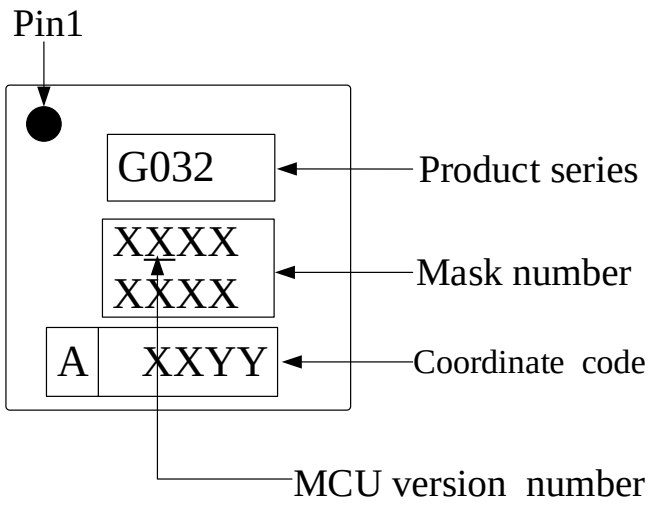


Figure 5-19 WLCSP25 screen printing instructions



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6 Ordering information

Figure 6-1 N32G032 Series Part Number Information

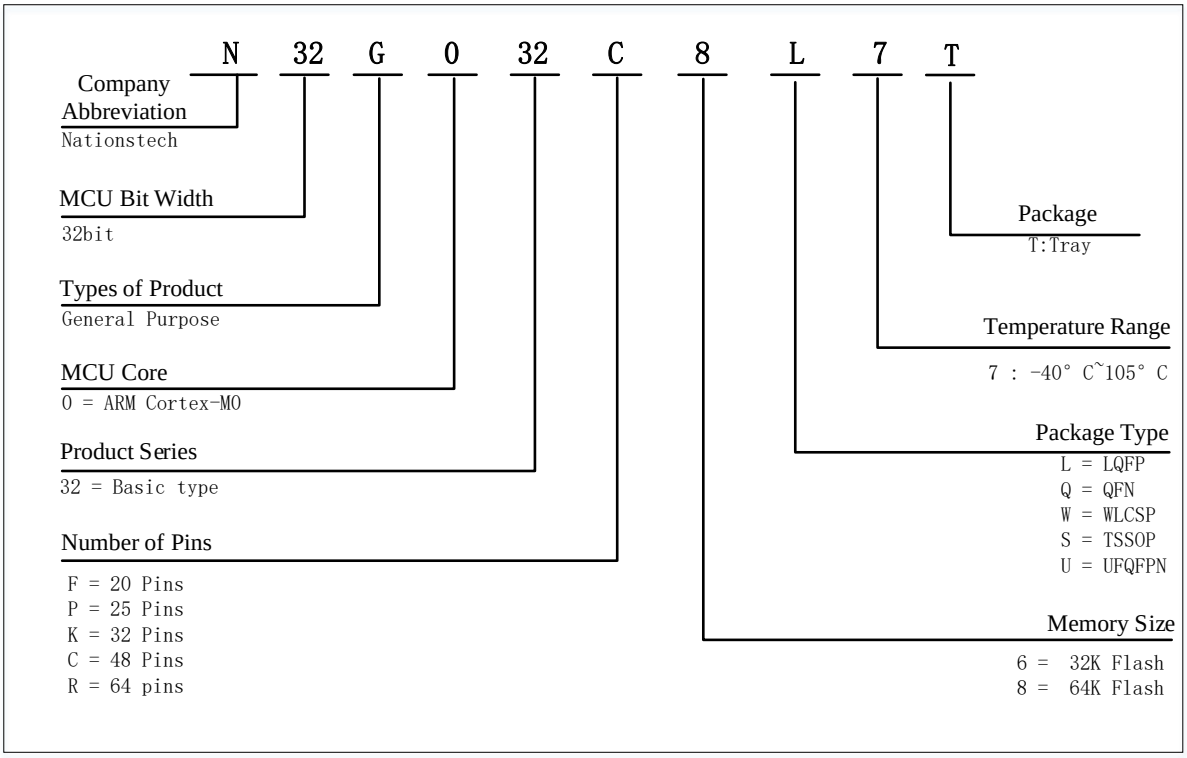

Table 6-1 N32G032 Series Ordering Code

Ordering code (1)	Package	Package size	Packaging (2)	SPQ(3)	Temperature range
N32G032F6U7	UFQFPN20	3mm x 3mm	Tray	490	-40 ℃ ~ 105 ℃
N32G032F6U7	UFQFPN20	3mm x 3mm	Reel	5000	-40 ℃ ~ 105 ℃
N32G032F6S7	TSSOP20	6.5mm x 4.4mm	Tube	70	-40 ℃ ~ 105 ℃
N32G032F6S7	TSSOP20	6.5mm x 4.4mm	Reel	3500	-40 ℃ ~ 105 ℃
N32G032F8S7	TSSOP20	6.5mm x 4.4mm	Tube	70	-40 ℃ ~ 105 ℃
N32G032F8S7	TSSOP20	6.5mm x 4.4mm	Reel	3500	-40 ℃ ~ 105 ℃
N32G032P6W7	WLCSP25	2.128mm x 2.065mm	Reel	3000	-40 ℃ ~ 105 ℃
N32G032P8W7	WLCSP25	2.128mm x 2.065mm	Reel	3000	-40 ℃ ~ 105 ℃
N32G032K6Q7	QFN32	5mm x 5mm	Tray	490	-40 ℃ ~ 105 ℃
N32G032K6Q7	QFN32	5mm x 5mm	Reel	2500	-40 ℃ ~ 105 ℃
N32G032K6L7	LQFP32	7mm x 7mm	Tray	250	-40 ℃ ~ 105 ℃
N32G032K8L7	LQFP32	7mm x 7mm	Tray	250	-40 ℃ ~ 105 ℃
N32G032C8L7	LQFP48	7mm x 7mm	Tray	250	-40 ℃ ~ 105 ℃
N32G032R8L7	LQFP64	10mm x 10mm	Tray	160	-40 ℃ ~ 105 ℃

1. For the latest detailed ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
3. Minimum packaging quantity.

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7 Version history

Date	Version	Modify
2020.6.13	V1.0	1. Initial version
2020.7.9	V1.1	1. Add parameters
2020.9.9	V1.2	1. Fix some content
2020.10.10	V1.3	1. Fix some content
2020.12.1	V1.3.1	1. Update the 32-bit programming time listed in Table 4-22 2. Update the VIL and VHL parameters in Table 4-26 3. Delete the I2S function description There is no master clock output
2021.5.12	V2.0	1. Fix some content
2021.8.6	V2.1	1. Add LPTIM description 2. Change the ADC sampling rate to a maximum of 1 MB 3. Modify Table 2-1 Comparison of timer functions 4. Modify the description in Section 2.11 5. Change the frequency division coefficient supported by ADC. 3 frequency division is not supported
2022.7.25	V2.2	1. Section 2.11 LPTIM capture / compare channel to count changed to 0 2. Section 2.18, ADC uses PLL and AHB_CLK as clock sources to increase frequency division by 3 3. Section 4.3.1 , Table 4-1 , delete two notes 4. Table 4-33 is modified in Section 4.3.18, ADC Electrical Characteristics. Table 4-34, Adding sample rate test conditions, delete note 1 5. Section 4.3.11, Table 4-24, the minimum value is changed to the maximum value 6. Section 4.3.13, Figure 4-10, the filter is at the back, the resistor is a fixed resistor 7. Section 4.3.16, Table 4-31, modify the restriction of SPI from input clock duty cycle and data output access time fpclk to 12MHz, and in Figure 4-14, modify the figure of SPI master mode 8. Modified Section 4.1.6, Figure 4-3. V_{DDA} is connected to a capacitor of 100nf+ 1uf 9. Table 4-1 , remove input voltage on 5V tolerant pins, remove original note 2 10. Section 4.3.5, delete "Can get Dhrystone 2.1 code equivalent results" 11. Figure 1-1, delete the AFEC 12. Figure 2-1, FLASH is changed to Main FLASH

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		13. Table 4-37, delete the maximum value of TL and change the typical value to +/- 2 14. Table 4-36, add note 2 for a reference input comparison voltage 15. Modify Table 4-28 16. Table 4-21, the maximum PLL ready time is changed to 20us 17. Table 4-16 and Table 4-17, load capacitance and drive current are deleted 18. Figure 4-8 Typical application of 32.768KHz crystals with graph modification 19. Tables 4-8 and 4-9, the captions are most typical 20. Table 4-5, modify the VDD rise rate 21. Table 4-2, original notes 2 and 4 are deleted 22. Section 2.25, Modify the CRC calculation time 23. Modify the descriptions in sections 4.1.1 and 4.1.2 24. In key features, change the MCO to 2, and add LSE and LSI 25. Table 4-10, add note 3, when the ADC is enabled, there is a current of 1.1mA (guaranteed by design). 26. Table 4-5, VDD upward slope is changed to 100 27. Section 4.3.6, Table 4-14 and Table 4-15 add (Bypass mode), modified in Figure 4-5 and 4-6. 28. Add N32G032K8L7 29. Modify the I2S master mode in Figure 4-16 30. Section 2.11.6, the predivision of IWDG was changed to 3 bits 31. Key features, remove programmable low voltage detection and reset 32. Delete all TSC content 33. PVD maximum and minimum value modification, gear 0-5, maximum ±100mv, gear 6-10, maximum ±120mv, gear 11-15, maximum ±160mv 34. Section 2.19, removed (or with both internal amplification and external filtering) 35. In the introduction section, delete N32G032C8Q7 and add N32G032F8S7
2023.7.31	V2.3.0	1. Section 4.3.19.Minimum operating voltage of OPA is adjusted from 2.4V to 2.9V 2. Section 4.3.2. The max value of VDD rising time rate is modified to 650
2024.1211	V2.4.0	1. Modify Figure 5-2 and 5-3 2. Chapter 5 Add recommended footprint 3. Add chapter 6 4. Delete Part number information chapter

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