N32G030 x6/x8 Product Brief

N32G030 series based on Arm® Cortex®-M0, run up to 48MHz, up to 64KB embedded flash, 8KB SRAM, integrated analog interface, 1x12bit 1Msps ADC, 1xOPAMP, 1xcomparator, integrated multi-channel U(S)ART, I2C, SPI and other digital communication interfaces.

Key feature

- **Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - Run up to 48MHz
- **Encrypted memory**
  - Up to 64KByte embedded Flash memory, supports encrypted storage, supports hardware ECC verification, data 100,000 cycling and 10 years of data retention
  - SRAM of 8KB, supporting hardware parity
- **Low-power management**
  - Stop mode: RTC Run, maximum 8KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode: support 3 IO wakeup
- **Clock**
  - HSE: 4MHz~20MHz external high-speed crystal
  - LSE: 32.768KHz external low-speed crystal
  - HSI: Internal high-speed RC OSC 8MHz
  - LSI: Internal low-speed RC OSC 30KHz
  - Built-in high-speed PLL
  - MCO: Support 2-way clock output, configurable SYSCLK, HSI, HSE, LSI, LSE, and PLL clock output that can be divided.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Support watchdog reset
- **Communication interface**
  - 3xU(S)ART, with a maximum rate of 3 Mbps, of which 2 USART interfaces (support 1xISO7816, 1xIrDA, LIN), 1 of which support low power (LPUART, the highest communication rate in this mode is 9600bps) ,Stop mode can be awakened
  - 2xSPI, up to 18 MHz, one of which supports multiplexing with I2S
  - 2xI2C, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
- **Analog interface**
  - 1x12bit 1Msps ADC , up to 12 external single-ended input channels
  - 1xOPAMP, internal programmable gain amplifier up to 32 times

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- 1xCOMP (Comparator has an internal independent 6bit DAC)

- **Up to 40 GPIOs**
- **1xDMA, 5-channel, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **1xBeeper, support complementary output, 16mA output drive capacity**
- **Timer counter**
  - 2x16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, each timer support 4 independent channels. Each timer support 3 pairs complementary PWM outputs
  - 1x16-bit general purpose timer counters, 4 independent channels, supports input capture/output compare/PWM output
  - 1x16-bit basic timer counters
  - 1x16-bit low power timer counter. support single pulse and double pulse counting function, can work in STOP mode
  - 1x24-bit SysTick
  - 1x7-bit Window Watchdog (WWDG)
  - 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Hardware Divider(HDIV)and Square Root(SQRT)**
- **Security features**
  - Flash storage encryption
  - CRC16/32 calculation
  - Support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 1.8V~5.5V
  - Operating Temperature Range: -40℃~105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - QFN32(4mm x 4mm)
  - QFN32(5mm x 5mm)
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
  - TQFP48(7mm x 7mm)

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- **Order model**

Series	Part Number
N32G030x6 N32G030x8	N32G030F6U7,N32G030F6S7 N32G030K6L7,N32G030K6Q7,N32G030K6Q7-1 N32G030K8L7, N32G030C8L7, N32G030C8T7, N32G030F8S7,N32G030K8Q7-1

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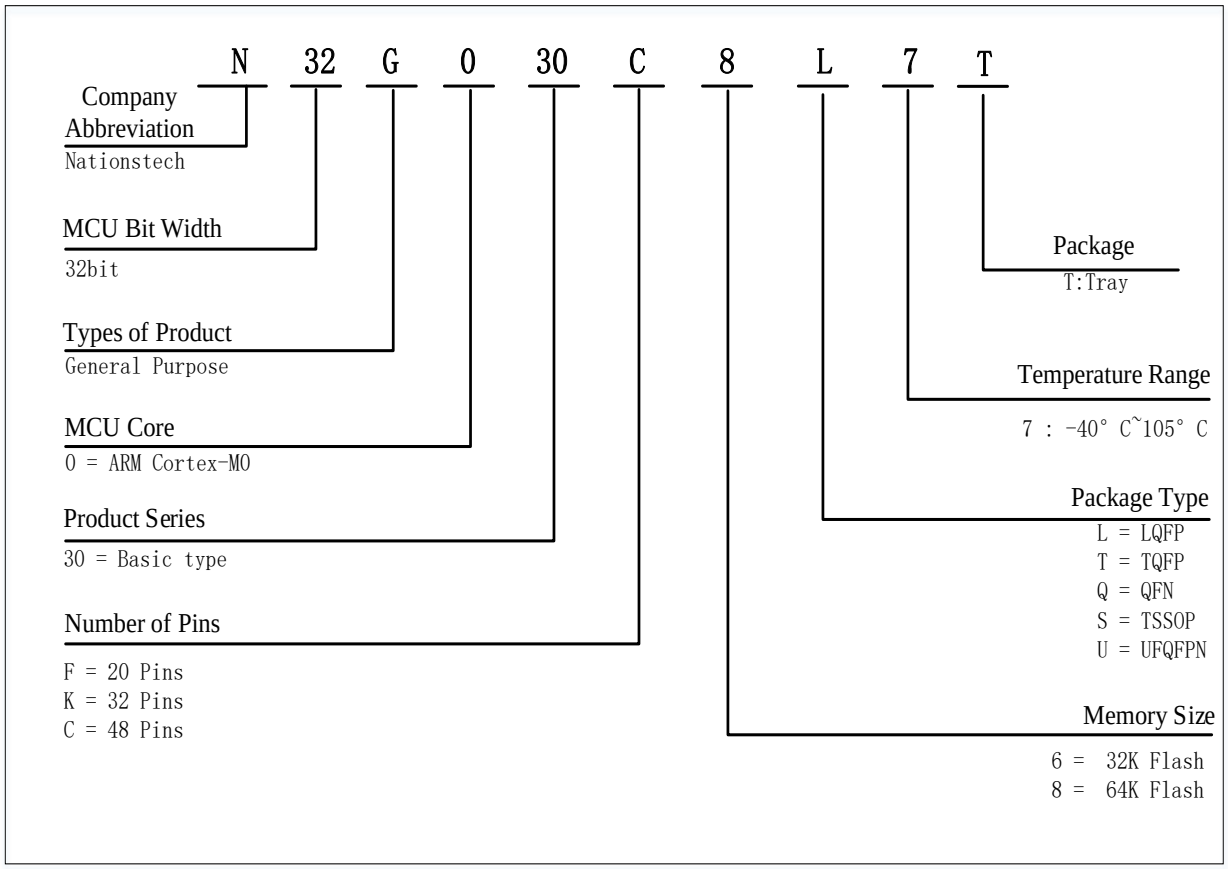
1 Part number information



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2 List of devices

Table 2-1 N32G030 Series devices features and peripheral list

Part Number		N32G030F6U7	N32G030F6S7	N32G030K6Q7	N32G030K6Q7-1	N32G030K8Q7-1	N32G030K6L7	N32G030K8L7	N32G030C8L7	N32G030C8T7	N32G030F8S7
Flash capacity (KB)		32	32	32	32	64	32	64	64	64	64
SRAM capacity (KB)		8	8	8	8	8	8	8	8	8	8
CPU frequency		ARM Cortex-M0 @48MHz									
working environment		1.8~5.5V/-40~105℃									
Timer	General	1									
	Advanced	2									
	Basic	1									
	LPTIM	1									
	RTC	1									
communication interface	SPI	2									
	I2S	1									
	I2C	2									
	USART	2									
	LPUART	1									
GPIO		16		28			26		40		16
DMA Number of Channels		5									
12bit ADC Number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel					1x12bit 12Channel		1x12bit 9Channel
OPA/COMP		1/1									
Beeper		1									
Algorithm support		CRC16/CRC32									
security protection		Read and write protection (RDP/WRP), storage encryption									
Package		UFQFPN20	TSSOP20	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)		LQFP32		LQFP48	TQFP48	TSSOP20

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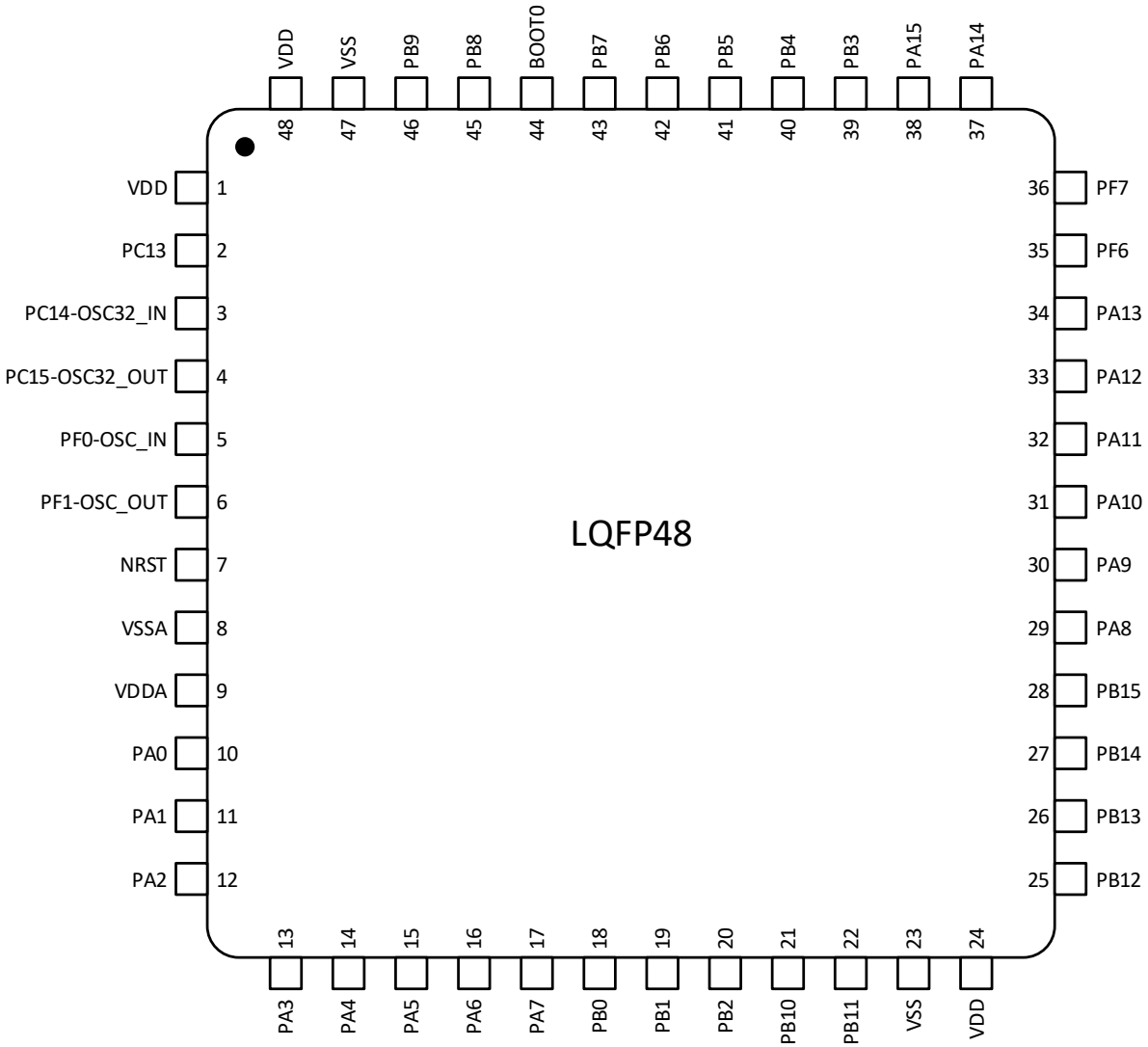
3 Package information

3.1 LQFP48

3.1.1 LQFP48 pinouts



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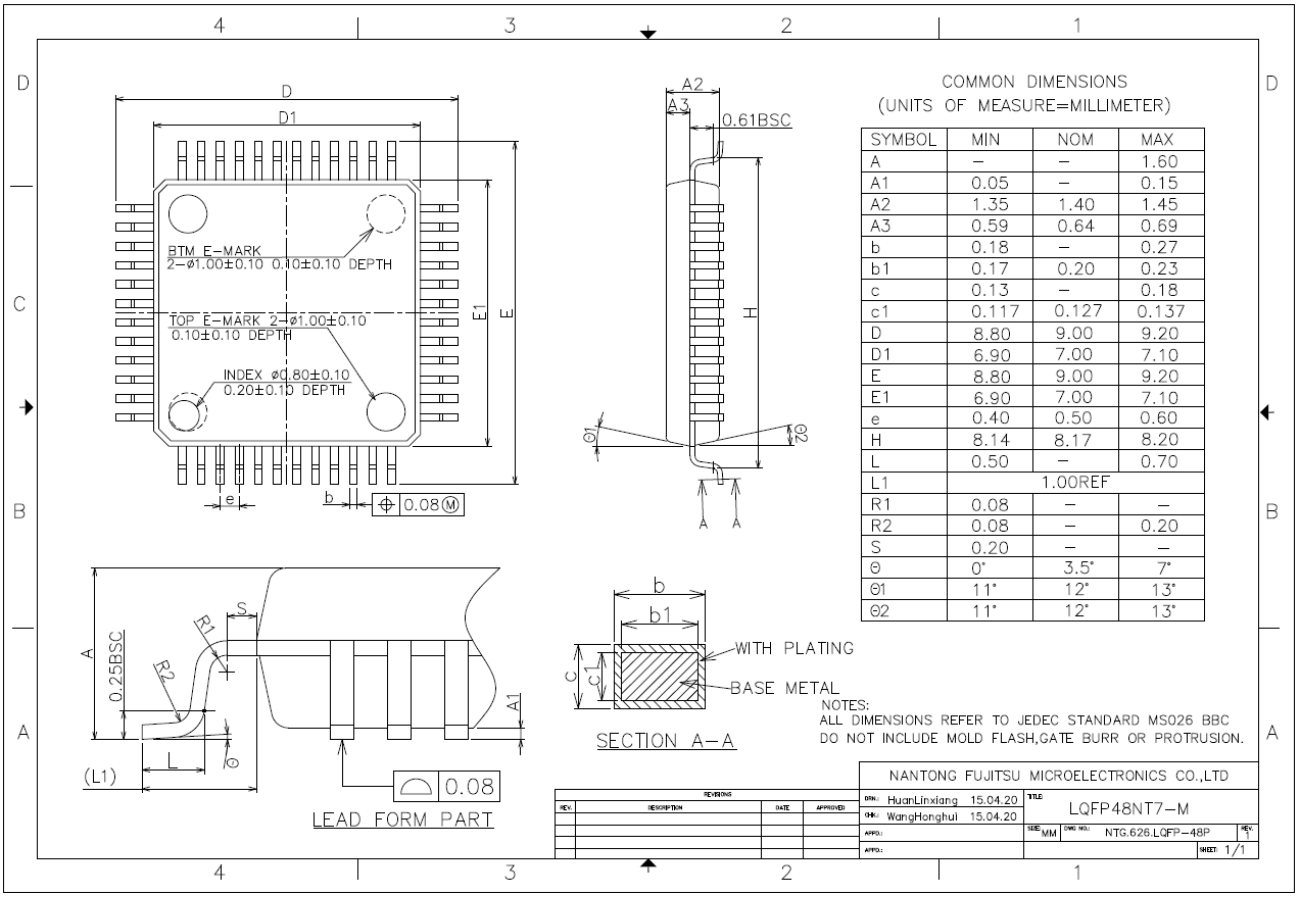
3.1.2 LQFP48 package



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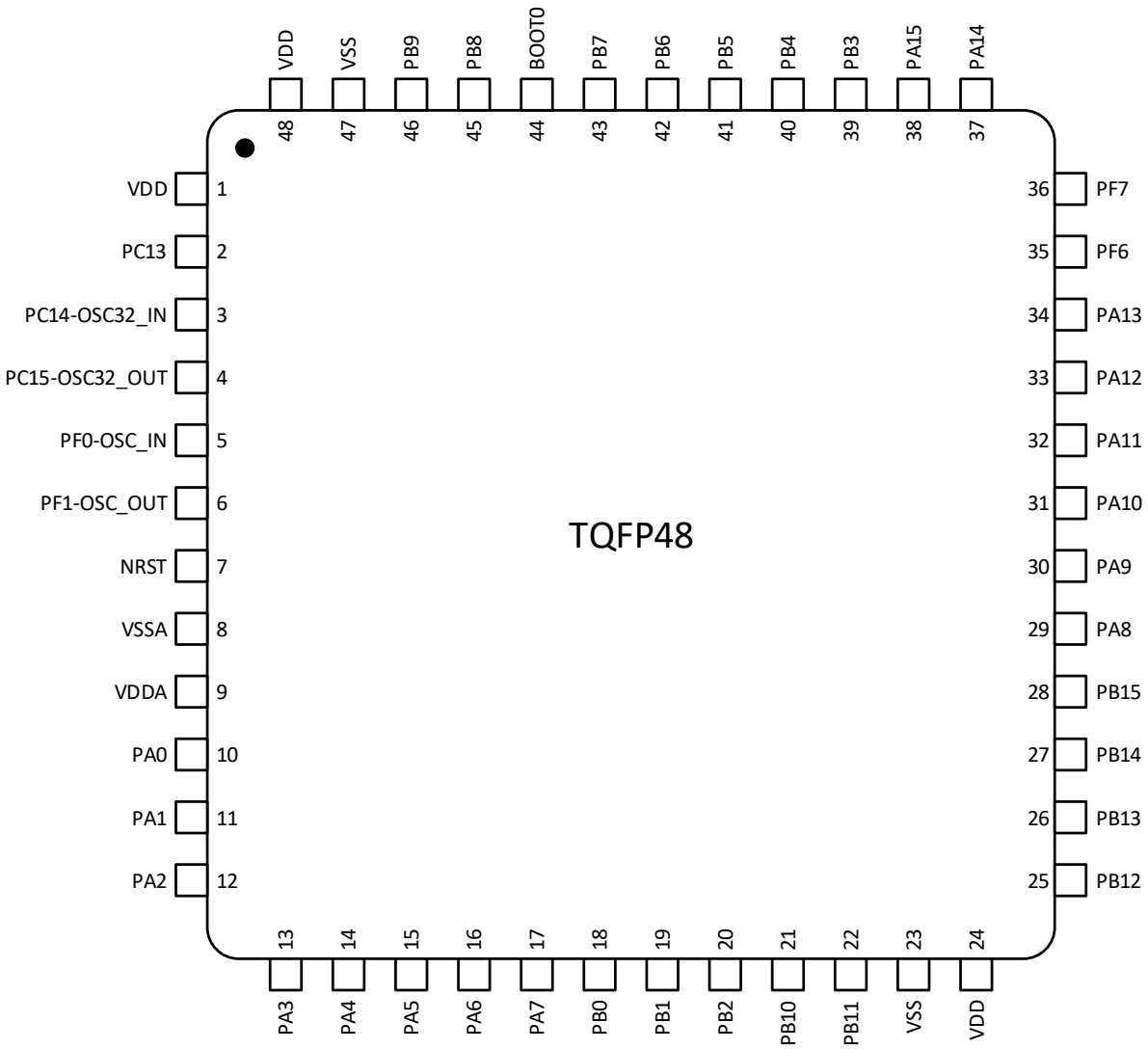
3.2 TQFP48

3.2.1 TQFP48 pinouts



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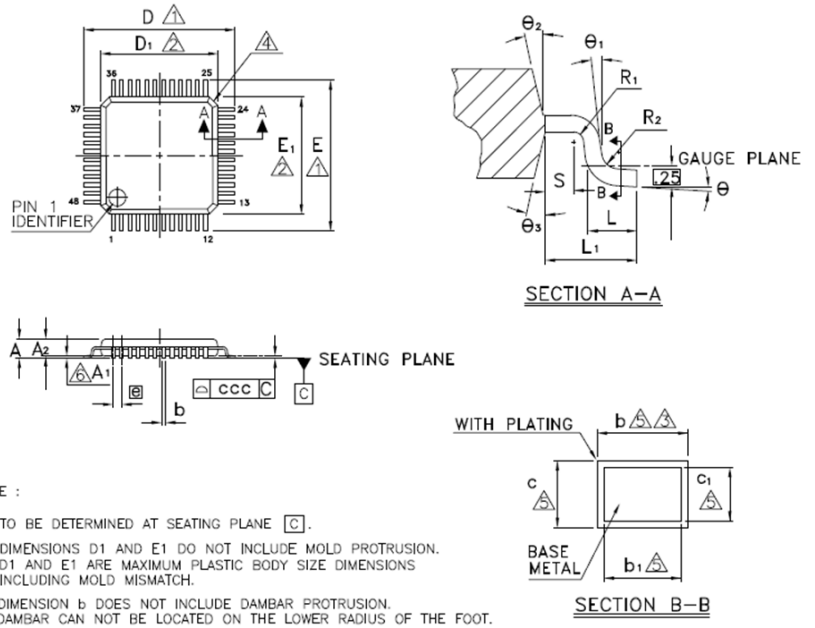
3.2.2 TQFP48 package



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

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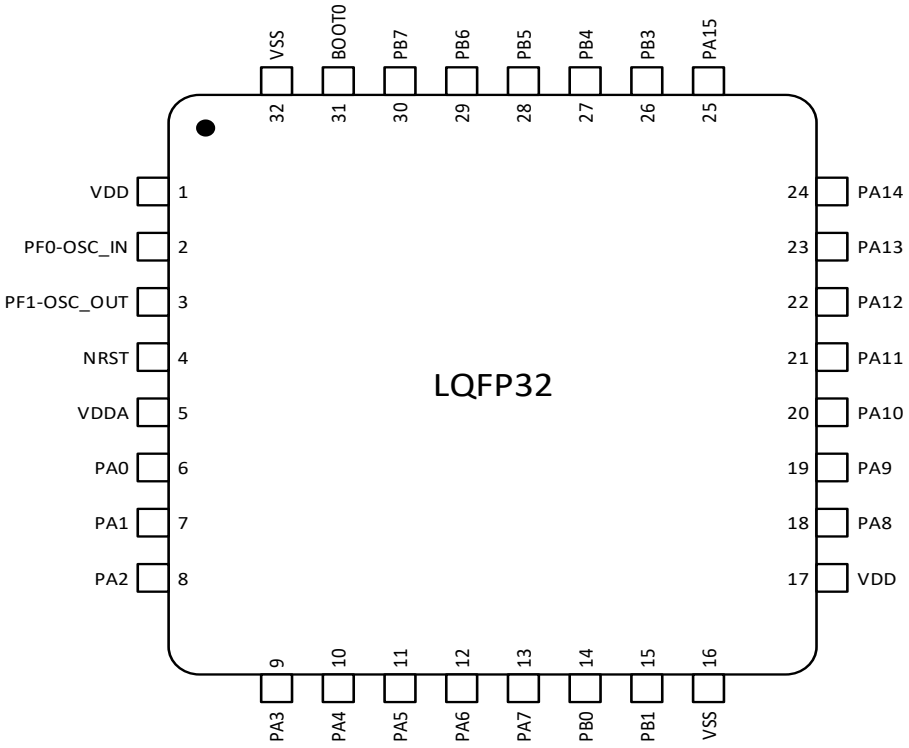
3.3 LQFP32

3.3.1 LQFP32 pinouts



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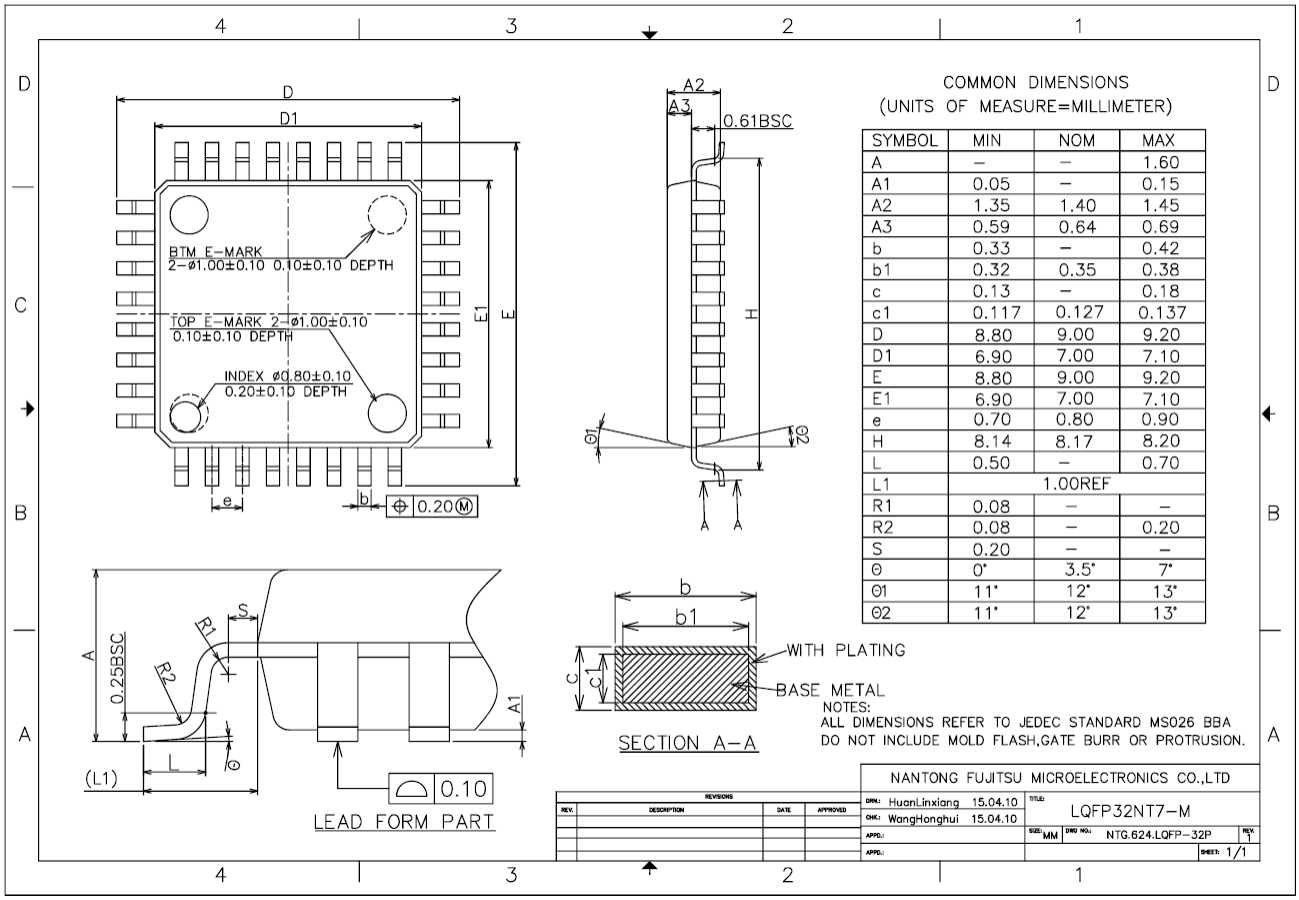
3.3.2 LQFP32 package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	–	0.42
b1	0.32	0.35	0.38
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBA
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

NANTONG FUJITSU MICROELECTRONICS CO.,LTD
DRN: HuanLinxiang 15.04.10
CHK: WangHonghui 15.04.10
APPD:
APPD:
TITLE: LQFP32NT7-M
SIZE: A MM DWG NO.: NTG.624.LQFP-32P REV: 1
SHEET: 1/1

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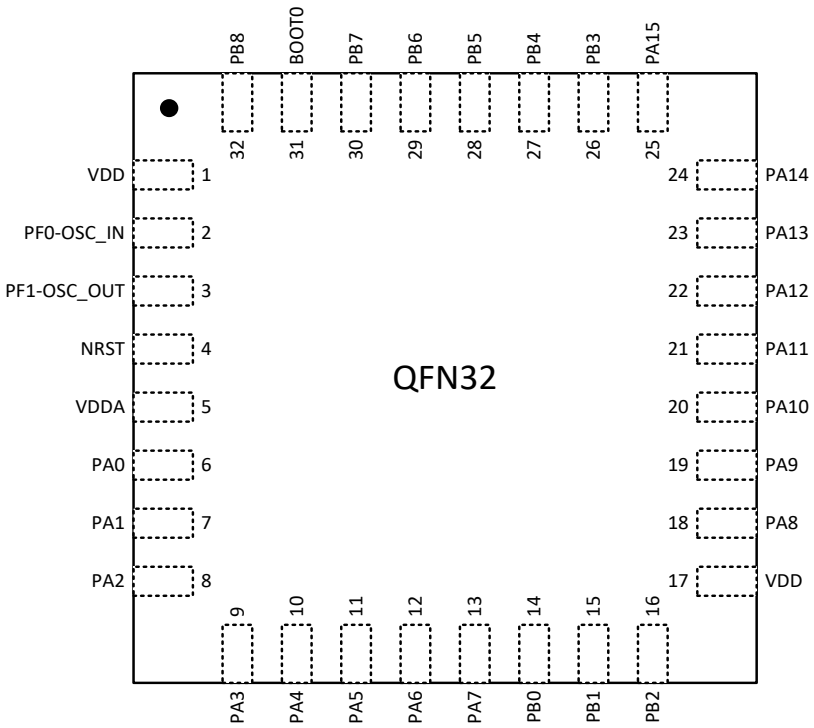
3.4 QFN32(5mmx5mm)

3.4.1 QFN32 (5mmx5mm) pinouts



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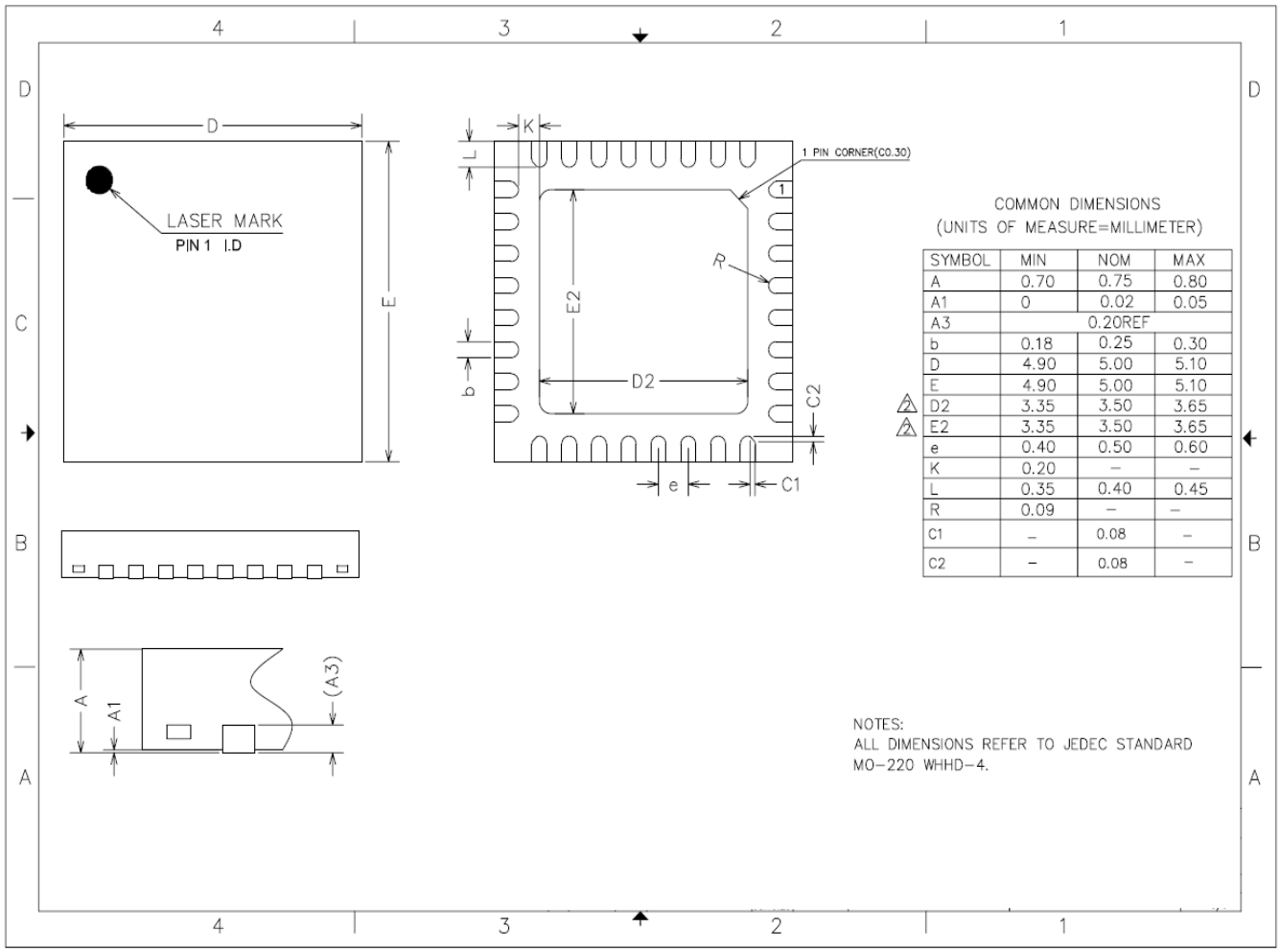
3.4.2 QFN32 (5mmx5mm) package



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
C1	–	0.08	–
C2	–	0.08	–

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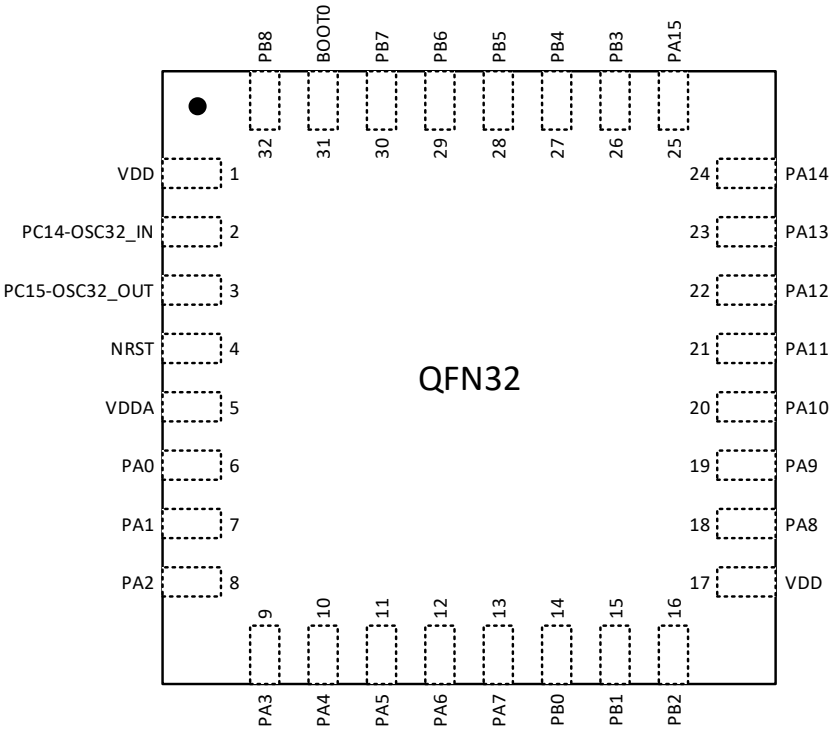
3.5 QFN32 (4mmx4mm)

3.5.1 QFN32 (4mmx4mm) pinouts



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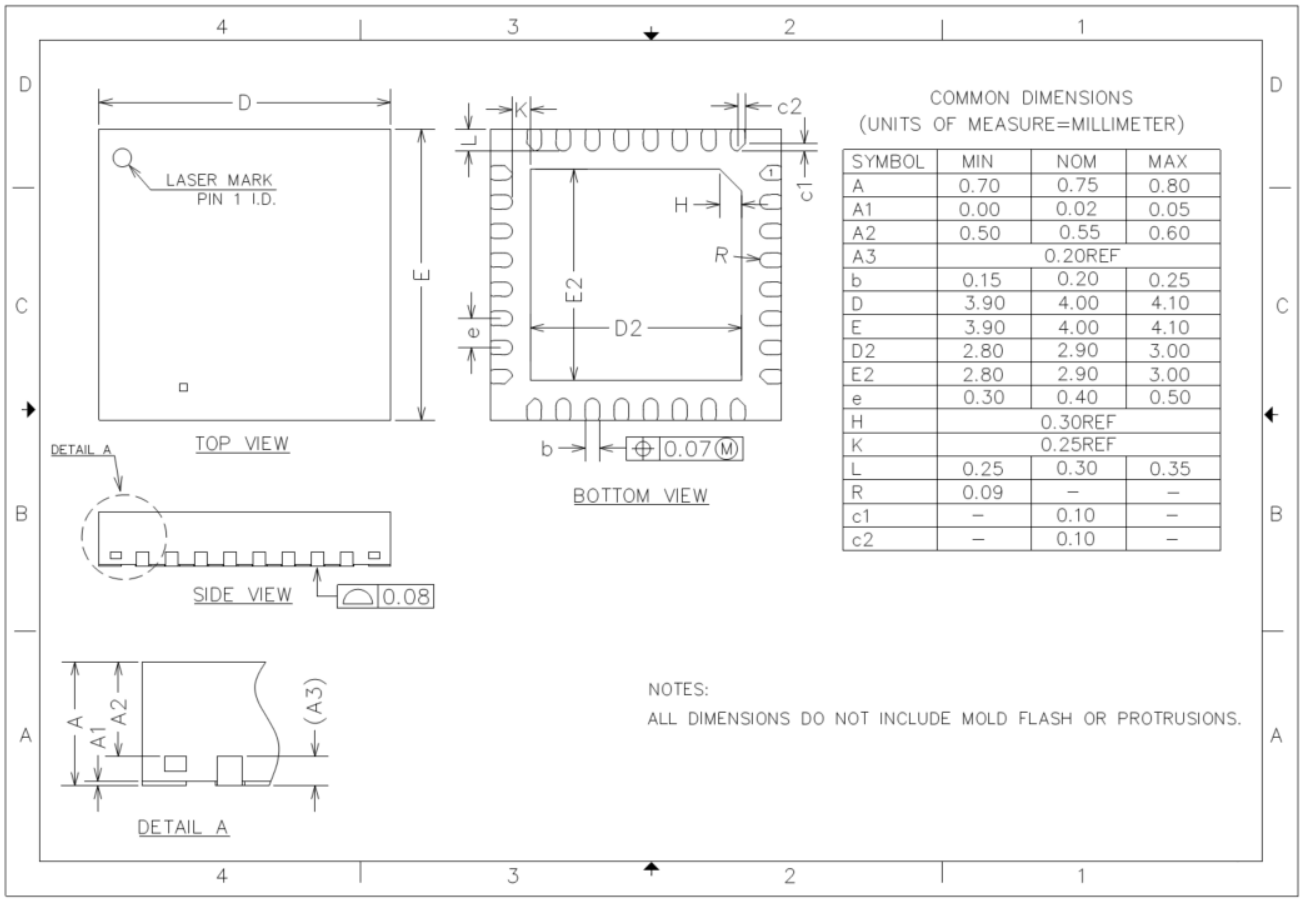
3.5.2 QFN32 (4mmx4mm) package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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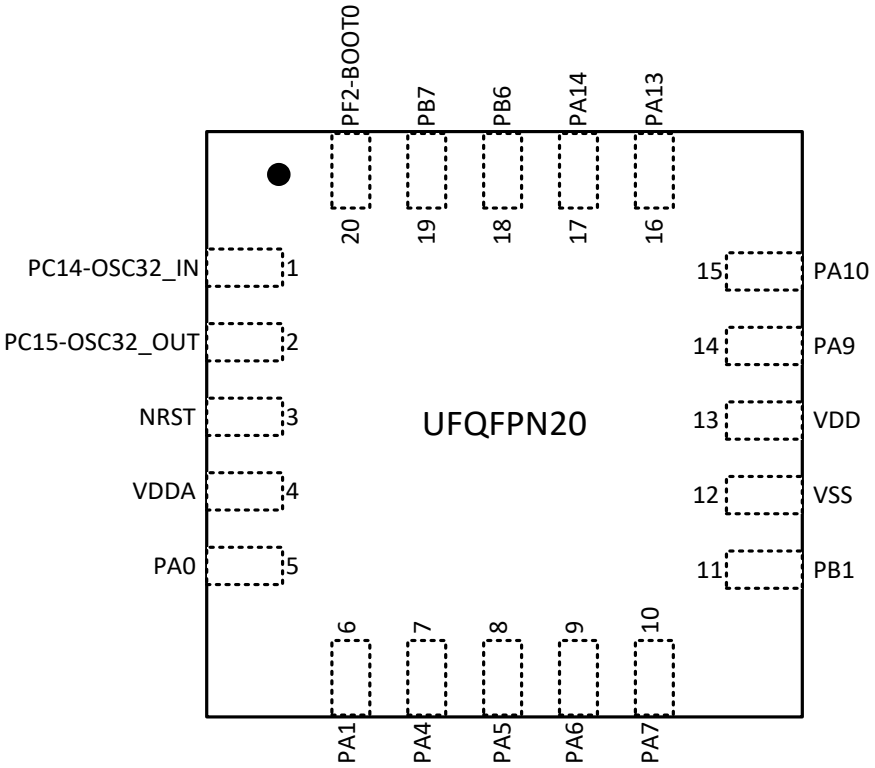
3.6 UFQFPN20

3.6.1 UFQFPN20 pinouts



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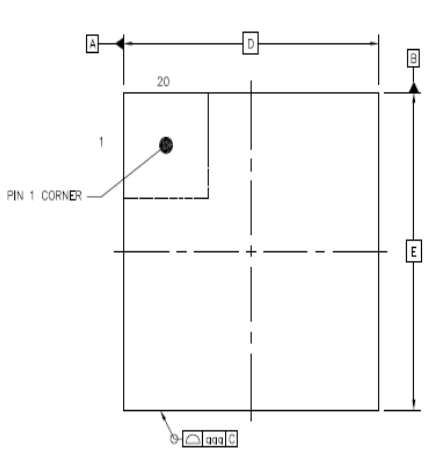
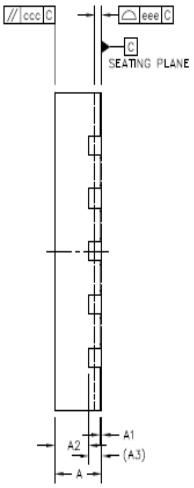
3.6.2 UFQFPN20 package

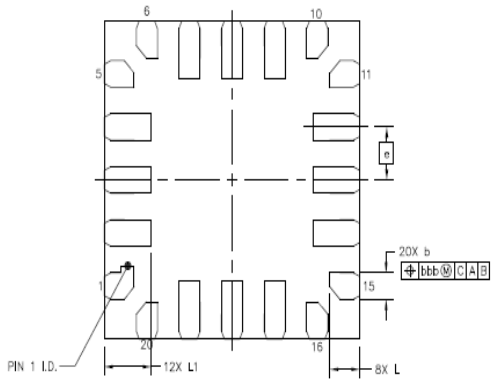


TOP VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	



BOTTOM VIEW

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JOET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

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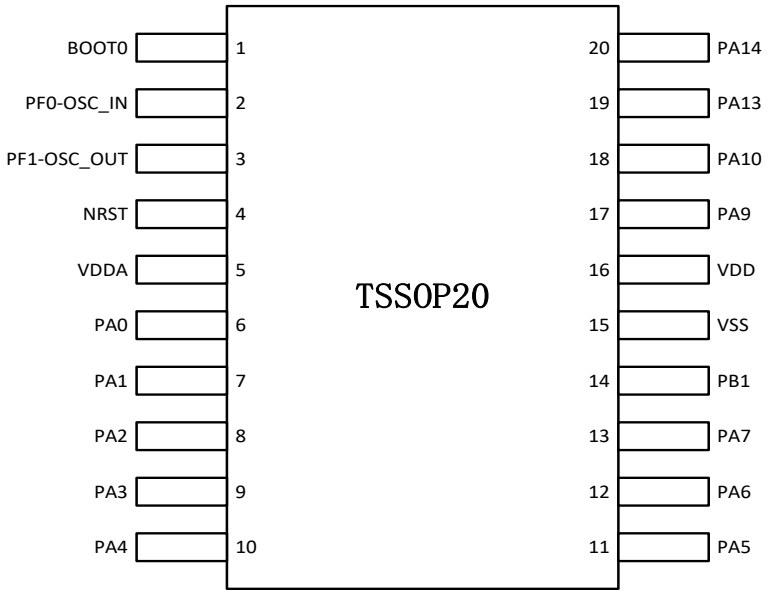
3.7 TSSOP20

3.7.1 TSSOP20 pinouts



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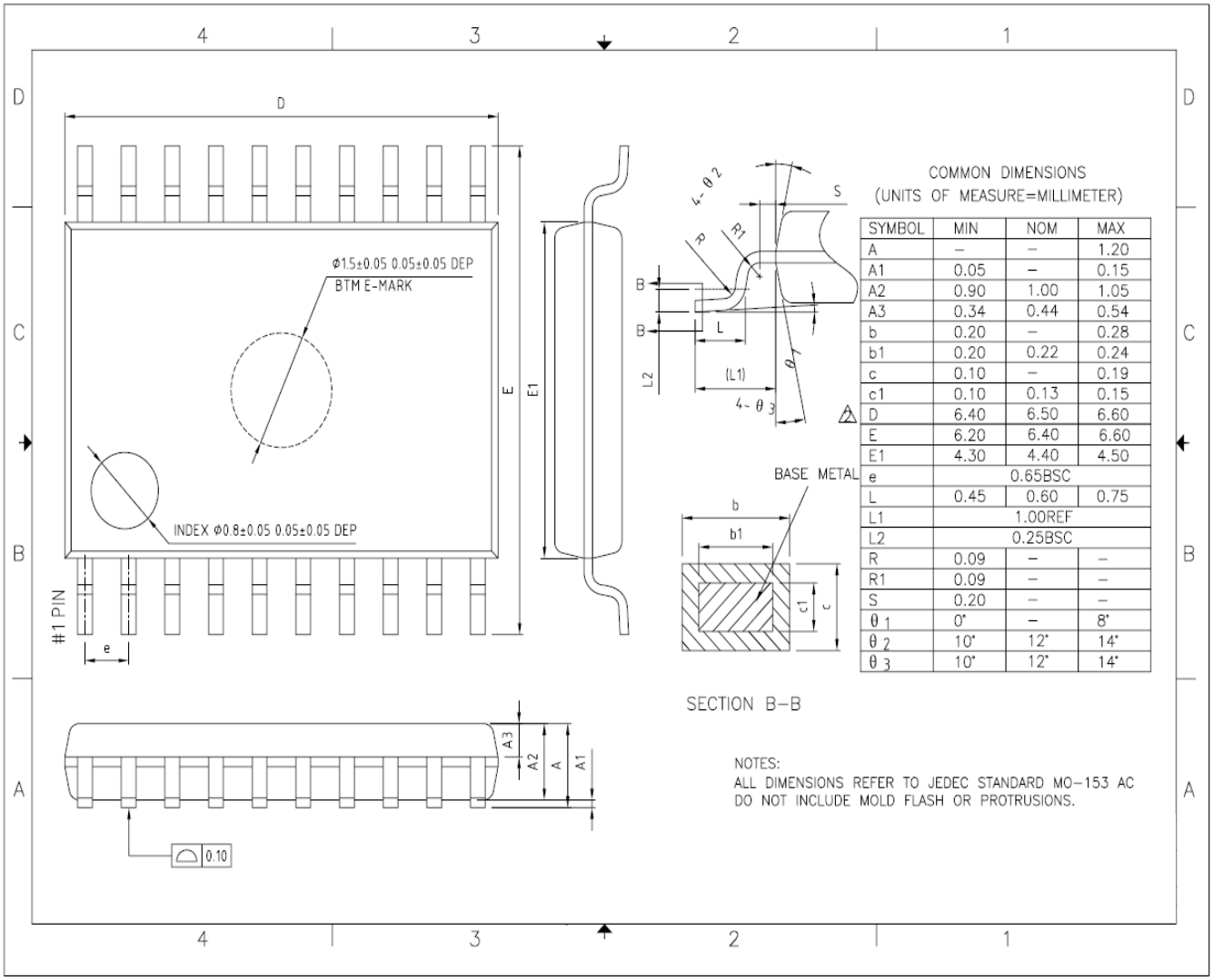
3.7.2 TSSOP20 package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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4 Revision History

Version	Date	Description
V1.0	2020.12.30	1. Initail document
V1.1	2021.08.16	1. Modified to have only 1 comparator 2. Add TQFP48 package information
V1.2	2022.3.17	1. Modify the size of retention SRAM to 8Kbyte
V1.3	2022.7.7	1. Modify the MCO to 2-way output in key feature 2. Delete reel in part number information
V1.4	2022.9.13	1. Key feature, delete programmable low level detection and reset.
V1.5.0	2023.7.31	1. Section 3.5.2. Modify package dimension of QFN32(4mmx4mm)
V1.6.0	2024.5.07	1. Section 3.1.2. Modify package dimension of LQFP48 2. Section 3.3.2. Modify package dimension of LQFP32 3. Add product model N32G030K8Q7-1

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