



N32G003 Series Errata Sheet V1.3.0

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1 Errata List

Errata overview

Errata link		Chip version
		Version B
Section 5: ADC	Section 5.1: When the ENDC flag is set, immediately read the ADC data register value for abnormal issues	•

•: there is this problem -: there is no this problem

Note: The current mass production version is version B

2 ADC

2.1 When the ENDC flag is set, immediately read the ADC data register value for abnormal issues

Description

After ENDC is set, immediately read the ADC data register, which may read the result of the previous conversion.

Resolution

1. After the ENDC flag is set, delay by 8 ADC_CK clocks before reading the ADC data register;
2. In some scenarios, the ENDCA flag is used instead of the ENDC flag.

3 Version history

Date	Version	Remark
2023.2.27	V1.0	Initial release
2025.1.6	V1.3.0	1. Added Section5.1 ADC usage problem

4 Notice

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