N32G430 Series Errata Sheet V1.3.0

Contents

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

1 Errata List

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2 Power Control (PWR)

2.1 Cannot reset from DEBUG STOP2 mode by pressing NRST button

Description

When the DBG_CTRL.STOP bit is set to 1 and the chip enters the STOP2 mode, the chip cannot be reset by pressing the NRST button.

Resolution

Before the chip enters STOP2 mode, clear the DBG_CTRL.STOP bit to 0.

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3 Timer (TIM)

3.1 TIM1/2/3/4/5/8 cannot generate compare events under certain circumstances

Description

In edge-aligned mode, in up-counting PWM1 mode, when the current PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the next PWM cycle is 0. At the moment when the PWM cycle counter is 0, although the count value = CCDATx shadow register value = 0 and OCxREF = 0, but still no compare event is generated.

Resolution

If it is not required that "the comparison event is generated at the time when the count value = the shadow register of the comparison value =0", the comparison event generated through another channel can replace the comparison event that is not generated.

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4 Serial Peripheral Interface (SPI)

4.1 I2S interface

4.1.1 PCM long frame mode

Description

When I2S works in master mode, PCM long frame mode, and the data format is "32bit" or "16bit extended to 32bit", the WS signal is one cycle per 16bit instead of 32bit.

Resolution

When I2S works in master mode and the long frame mode must be used, the 16bit data mode should be used.

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5 Real Time Clock (RTC)

5.1 RTC automatic wake up

Description

After the RTC calendar setting is completed, configure the automatic wake-up function. The time from enabling automatic wake-up to the first wake-up is smaller than the wake-up automatic reload value, and the subsequent automatic wake-up time is normal.

Resolution

Ignore the first wakeup.

5.2 The RTC wakeup event is generated before the chip enters STANDBY and cannot wake up

Description

Before the chip enters STANDBY mode, if an RTC wakeup event occurs, the chip will not wake up after entering STANDBY mode.

Resolution

None.

5.3 The RTC calendar function cannot be initialized multiple times within 1 second

Description

The RTC calendar function is initialized multiple times within 1 second, so that the RTC alarm clock interrupt cannot be generated.

Resolution

The interval between two initializations of the RTC calendar function is more than 1 second.

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5.4 The RTC triggers the TISOVF flag by mistake

Description

When the system wakes up from STANDBY mode or the IWDG times out and the system reset, the RTC may triggers the TISOVF flag by mistake probability .

Resolution

Before entering STANDBY mode or IWDG time out, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF[14:0] register for the first time, and SHOPF flag will set 1. When SHOPF flag is 0 again, configure RTC_SCTRL.SUBF[14:0] register for the second time. Note that NRST cannot be triggered during above process.

5.5 The shift operation of the RTC on the subsecond causes the current wake-up time is inaccurate

Description

When the RTC is configured to periodic wake up, performing the shift operation for subseconds before triggering the periodic wake-up will cause the current wake-up time is inaccurate, and the subsequent wake-up time will be normal.

Resolution

None

5.6 RTC_DATE register lock

Description

1. Before the system software reset, the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and the RTC_DATE register will restores the default value after the system software resets and initializes the RTC without configuration or reads the RTC_DATE register;
2. When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged;

Resolution

1. Read the RTC_DATE register before initializing the RTC;
2. After reading the RTC_SUBS or RTC_TSH shadow register, read the RTC_DATE register;

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6 GPIO and AFIO

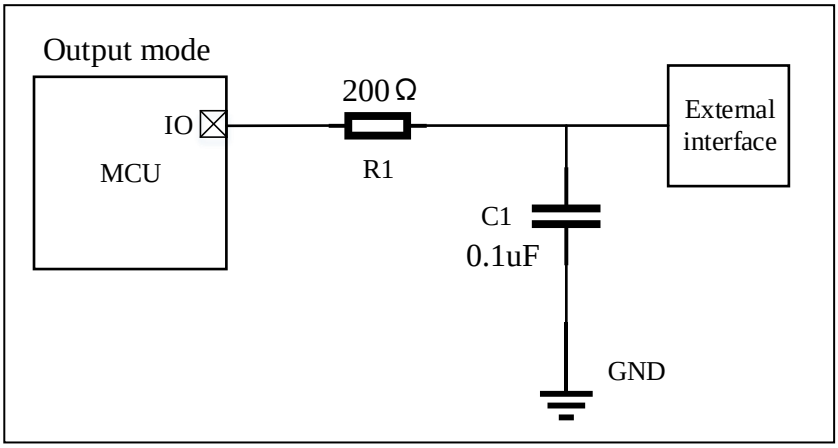
6.1 IO appeared burr during power-on

Description

When the MCU is powered on, some IOs will have burrs appeared.

Resolution

When IO is used as input, the burr has no effect on MCU; When IO is used as output, 200Ohm resistor and 0.1uF capacitor are applied for filtering.



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7 Controller Area Network (CAN)

7.1 CAN active error

Description

When the CAN is in normal mode and the CAN bit is hard synchronized,if the baud rate deviation of other nodes is too large(approaching or exceeding the synchronization segment),the CAN module is prone to generate the active error.

Workaround

D version chip solution

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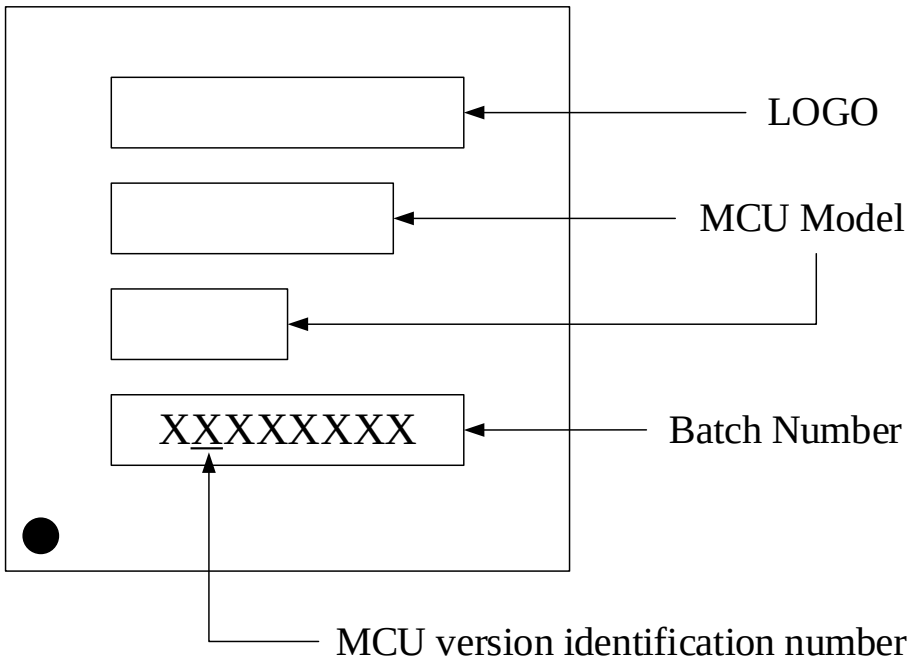
8 Marking information



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9 Version history

Date	Version	Remark
2022.5.12	V1.0	Initial release
2022.7.19	V1.1	Add section 6
2023.3.21	V1.2.0	1. Add section 7, CAN active error 2. Modify section 5.2, wakeup event instead of tamper event 3. Add section 5.4, The RTC triggers the TISOVF flag by mistake 4. Add section 5.5, The shift operation of the RTC on the subsecond causes the current wake-up time is inaccurate
2023.5.9	V1.3.0	1. Add chapter 5.6

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