N32WB452xE Product Brief

N32WB452 series is a BLE5.0 MCU chip based on 32-bit ARM Cortex-M4F + Cortex-M0 dual-core, TX/RX power consumption 3.5mA, transmit power +3dBm, receiving sensitivity -94dBm, main frequency 144MHz, support floating-point operations and DSP instructions, built-in 512KB Flash, 144KB SRAM, integrated 7xU(S)ART, 4xI2C, 3xSPI, 2xCAN 2.0B, 1x USB 2.0 FS Device, 1xSDIO, digital video interface, 2x12bit 5Msps ADC, 2x1Msps 12bit DAC, built-in cryptographic algorithm hardware acceleration engine

Main features

- **BLE5.0**
  - 2.4 GHz RF transceiver, support BLE5.0
  - High receiver sensitivity (–94dBm@BLE)
  - Programmable transmitter power, up to +3dBm
  - Built-in Balun/Matching Network
  - Receive power consumption: 3.5mA@3.0V (DCDC)
  - Transmit power consumption: 3.6mA@3.0V/0 dBm (DCDC)
- **CPU core**
  - 32-bit ARM Cortex-M4 + Cortex-M0 dual-core architecture, in which 32bit ARM Cortex-M0 is used as a co-processor dedicated to processing BLE5.0 radio frequency circuit and Bluetooth core protocol, through the internal bus and ARM Cortex-M4 core application processor communication
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply and divide instructions, support DSP instructions and MPU
  - Built-in 8KB instruction Cache, support Flash acceleration unit execution program 0 wait
  - Run up to 144MHz, 180DMIPS
- **Memory**
  - Up to 512KByte embedded Flash memory, support encrypted storage, partition management and data protection, support hardware ECC verification, 100,000 erasing times, 10 years data retention
  - 144KByte embedded SRAM (including 16KByte Retention RAM), supporting hardware parity check
- **Low power management**
  - Standby mode: 4uA, 84 backup registers are retained, all IOs are retained, optional RTC Run, 16KByte Retention SRAM retention, support VBAT pin independent power supply, 100us fast wake-up
  - Stop2 mode: 6uA, RTC Run, 16KByte Retention SRAM retention, CPU register retention, all IO retention, 40us fast wake-up
  - Stop0 mode: 150uA, RTC Run, all SRAM retained, all IO retained, 20us fast wake-up
- **Application processor clock**
  - 4MHz~32MHz external high-speed crystal

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- 32.768KHz external low-speed crystal
- Internal high-speed RC 8MHz
- Internal low-speed RC 40KHz
- Built-in high-speed PLL
- Supports one-way clock output, which can be configured with system clock, HSE, HSI, or PLL frequency division output

- **Bluetooth processor clock**
  - 32MHz external high-speed crystal
  - 32.768KHz external low-speed crystal
  - Internal high-speed RC 32MHz
  - Internal low-speed RC 32KHz
- **Reset**
  - Supports power on, power down, brown-out, and external pin reset
  - Support watchdog reset
- **Up to 65 GPIOs with multiplexing function. Most GPIO supports 5V voltage resistance.**
- **Communication interface**
  - 7x U(S)ART interfaces with speeds up to 4.5Mbps, including 3x USART interfaces (supporting ISO7816, IrDA, LIN) and 4x UART interfaces
  - 3x SPI interfaces with speeds up to 36MHz, two of which support I2S
  - 4x I2C interfaces with speeds up to1MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 1x USB2.0 Full Speed Device port
  - 2x CAN 2.0B bus interfaces
  - 1x SDIO interface, supporting SD/SDIO/MMC format
  - 1x DVP (Digital Video Port)
- **Analog interface**
  - 2x 12bit 5Msps high-speed ADCs, available in 12/10/8/6 bit mode, sampling rate up to 9Msps in 6bit mode and up to 16 external single-ended input channels, supporting differential mode
  - 2x 12bit DAC, sampling rate 1Msps
  - Support external input independent reference voltage source
  - All analog interfaces support full voltage from 1.8 to 3.6V
- **2x high-speed DMA controllers, each controller supports 8 channels, channel source address and destination address can be arbitrarily configurable**

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- **RTC real-time clock, support leap year perpetual calendar, alarm clock event, periodic wake up, support internal and external clock calibration**
- **Timing counter**
  - 2x 16bit advanced timer counters, support input capture, complementary output, orthogonal coding input and other functions, the highest control accuracy of 6.9ns;Each timer has four independent channels, three of which support 6 complementary PWM output
  - 4x 16bit general timer counters, each timer has four independent channels, support input capture/output comparison /PWM output
  - 2x 16bit basic timer counters
  - 1x 24bit SysTick
  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART and USB Bootloader
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Supports AES, DES, SHA, SM1, SM3, SM4, SM7, and MD5 algorithms
  - Flash Storage encryption, Multi-user Partition Management (MMU)
  - TRNG true random number generator
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support security startup, program encryption download, security updates
  - Support clock failure detection, anti-disassembly detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 85℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - QFN48(6mm x 6mm)
  - QFN64(8mm x 8mm)
  - QFN88(10mm x 10mm)

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1 Ordering information

Figure 1-1 N32WB452 Series Part Number Information

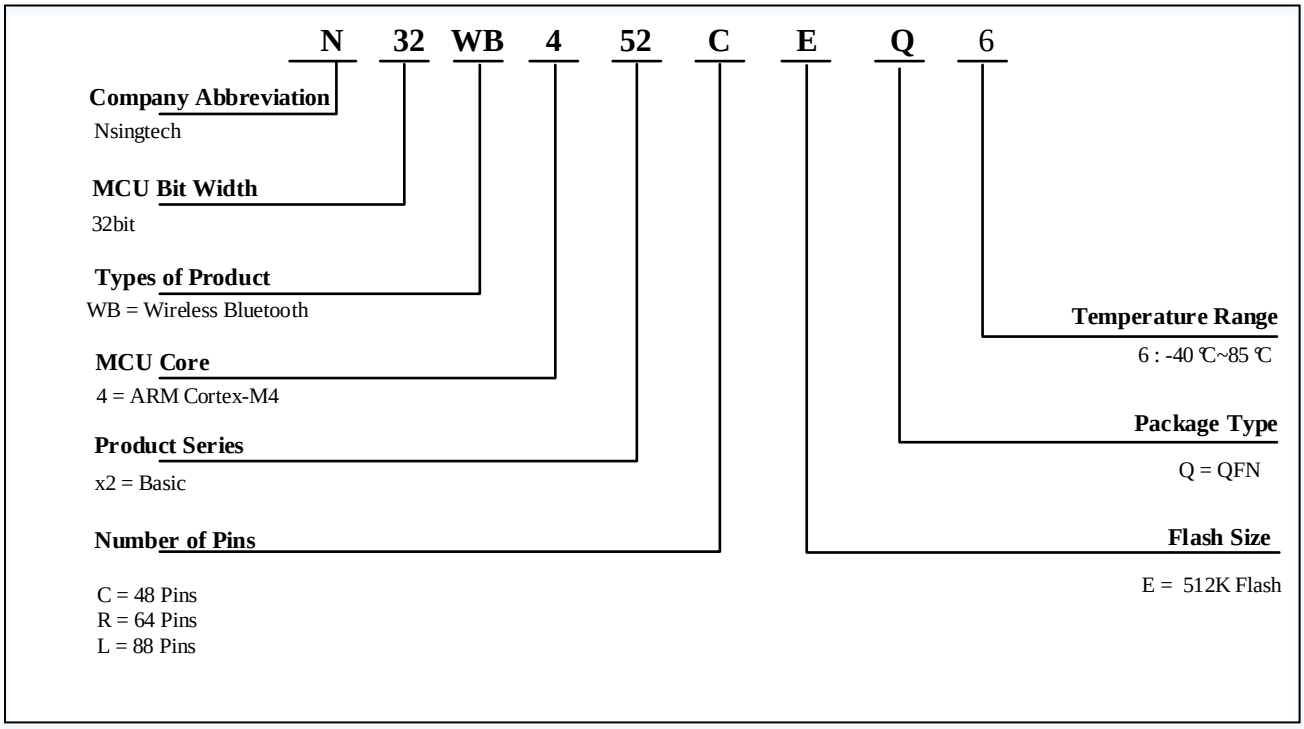

Table 1-1 N32WB452 Series Ordering Code

Ordering code (1)	Package	Package size	Packaging (2)	SPQ(3)	Temperature range
N32WB452CEQ6	QFN48	6mm*6mm	Tray	490	-40℃ ~ 85℃
N32WB452REQ6	QFN64	8mm*8mm	Tray	260	-40℃ ~ 85℃
N32WB452LEQ6	QFN88	10mm*10mm	Tray	168	-40℃ ~ 85℃

1. For the latest detailed ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact NSING.
3. Minimum packaging quantity.

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2 Product Model Resource configuration

Device type		N32WB452CE	N32WB452RE	N32WB452LE
Flash size（KB）		512	512	512
SRAM size（KB）		144	144	144
CPU frequency		ARM Cortex-M4 @144MHz,180DMIPS		
BLE Core		BLE 5.0 / ARM Cortex-M0 @ 32MHz		
Work environment		1.8~3.6V/-40~85℃		
Timer	General	4		
	Advanced	2		
	Basic	2		
Communication Interface	SPI	3		
	I2S	2		
	I2C	2	3	4
	USART	3		
	UART	2	3	4
	USB	1		
	CAN	2		
	SDIO	0		1
	DVP	0		1
GPIO		29	43	65
DMA/channel number		2/16 Channel		
12bit ADC/channel number		2/6 Channel	2/11 Channel	2/16 Channel
12bit DAC/channel number		2/2 Channel		
Algorithm support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG		
Security protection		Read/write protection（RDP/WRP）, storage encryption, partition protection, secure startup		
Package		QFN48	QFN64	QFN88

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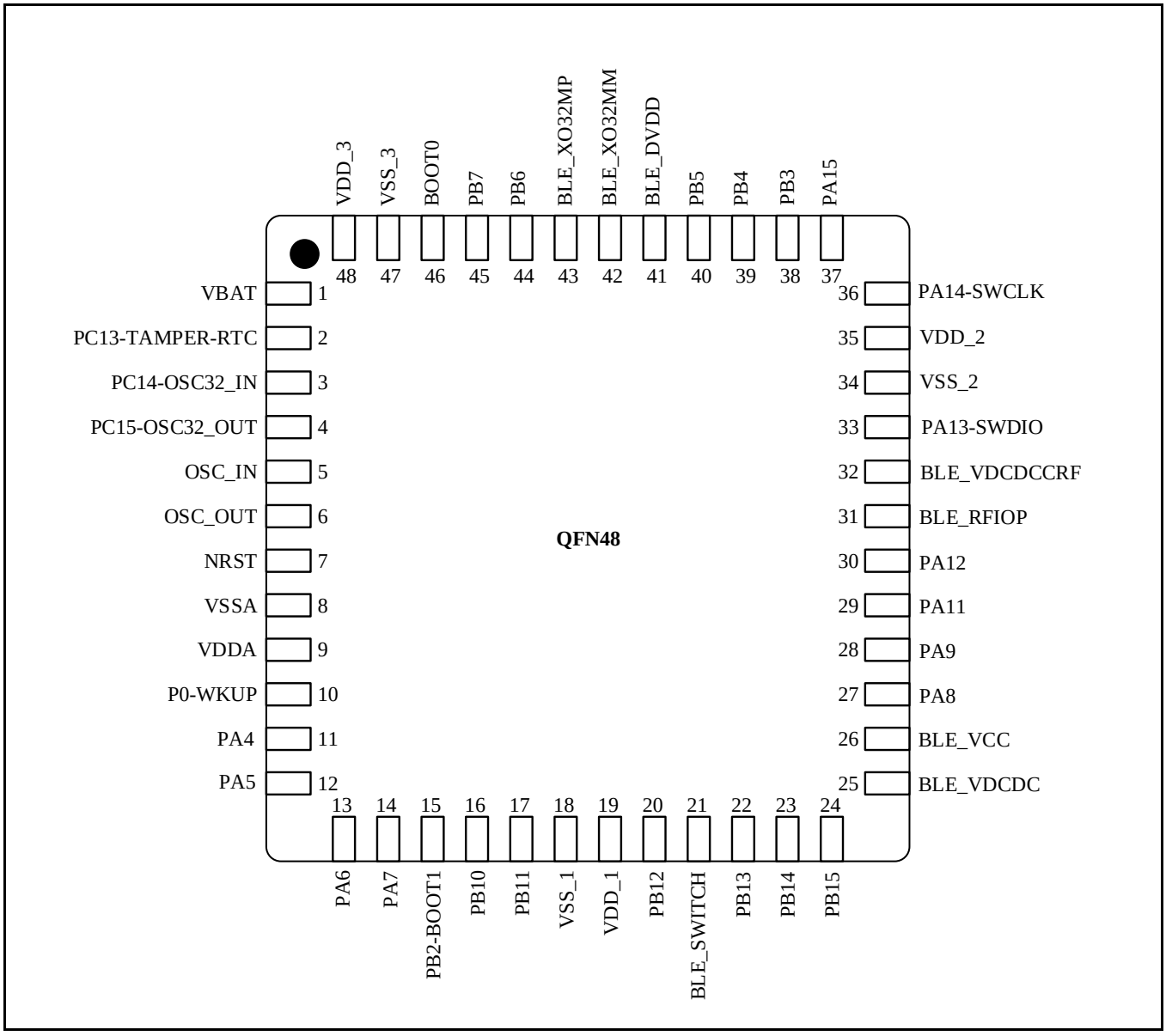
3 Package

3.1 QFN48 package

3.1.1 QFP48 pin distribution



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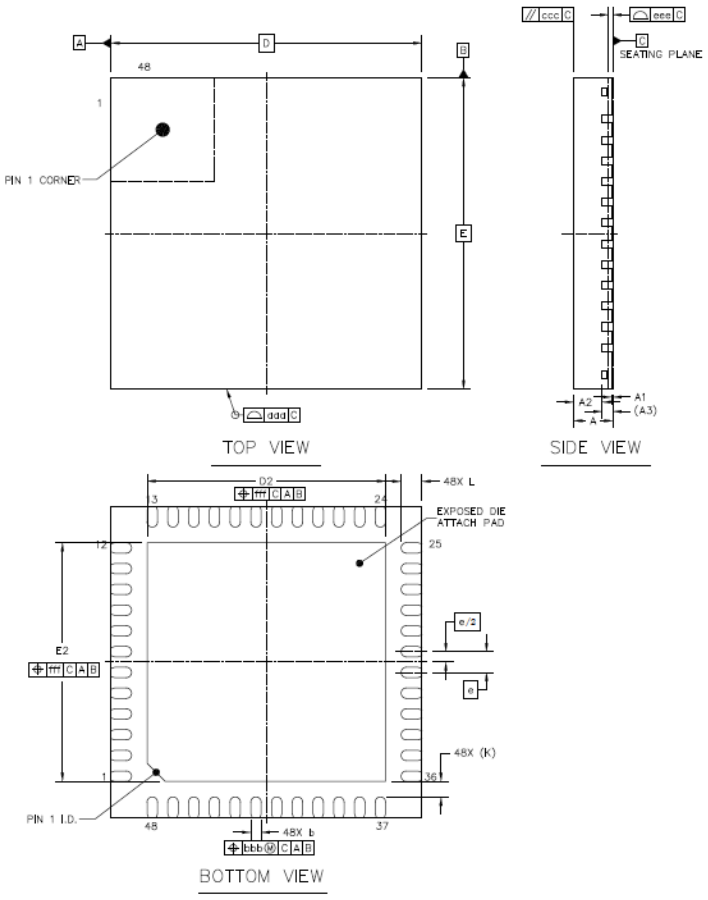
3.1.2 QFN48 package size



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.5	4.6	4.7
	Y	E2	4.5	4.6	4.7
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP *Sn8~20s

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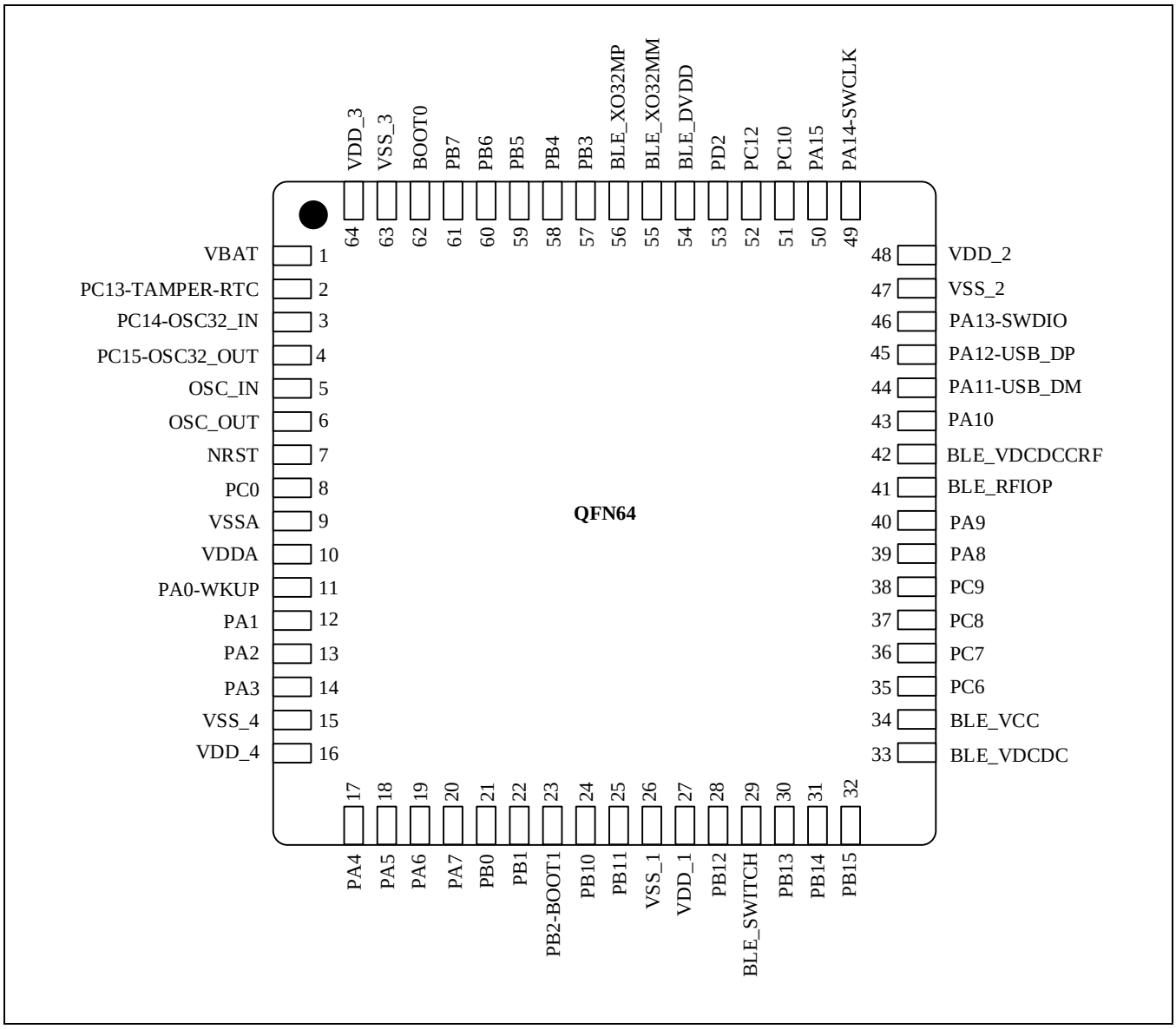
3.2 QFN64 package

3.2.1 QFN64 pin distribution



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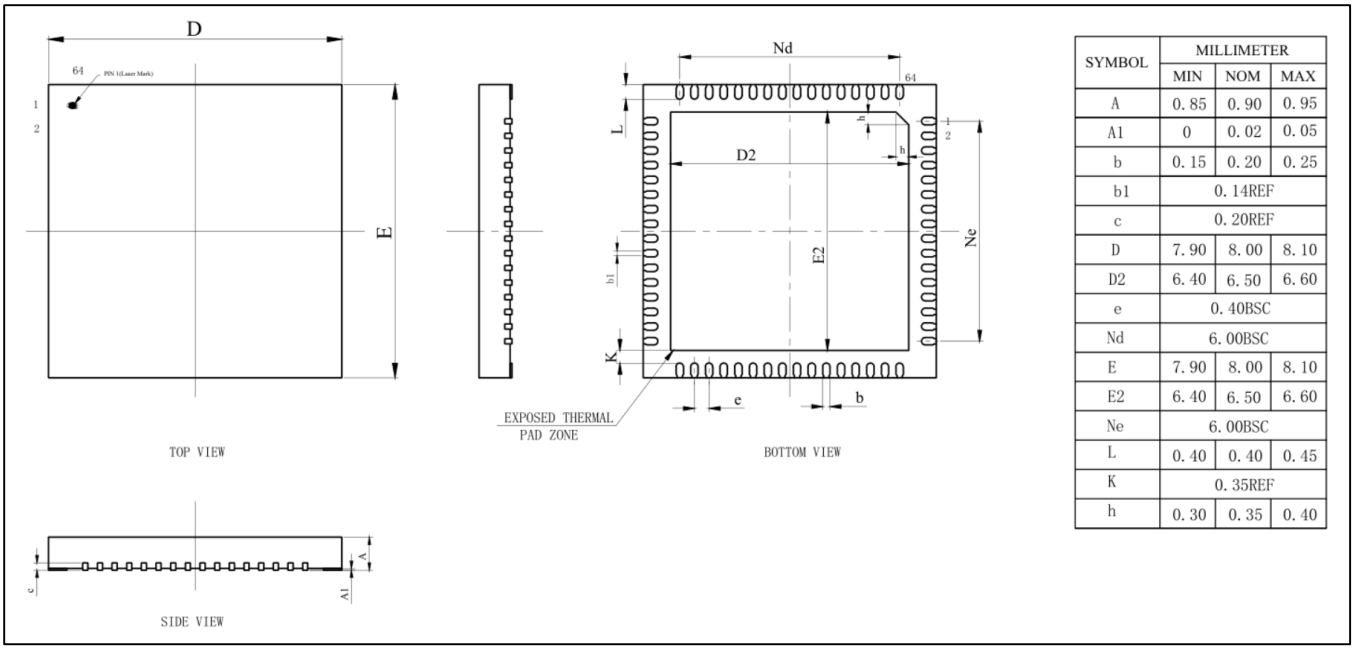
3.2.2 QFN64 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
D	7.90	8.00	8.10
D2	6.40	6.50	6.60
e		0.40BSC	
Nd		6.00BSC	
E	7.90	8.00	8.10
E2	6.40	6.50	6.60
Ne		6.00BSC	
L	0.40	0.40	0.45
K		0.35REF	
h	0.30	0.35	0.40

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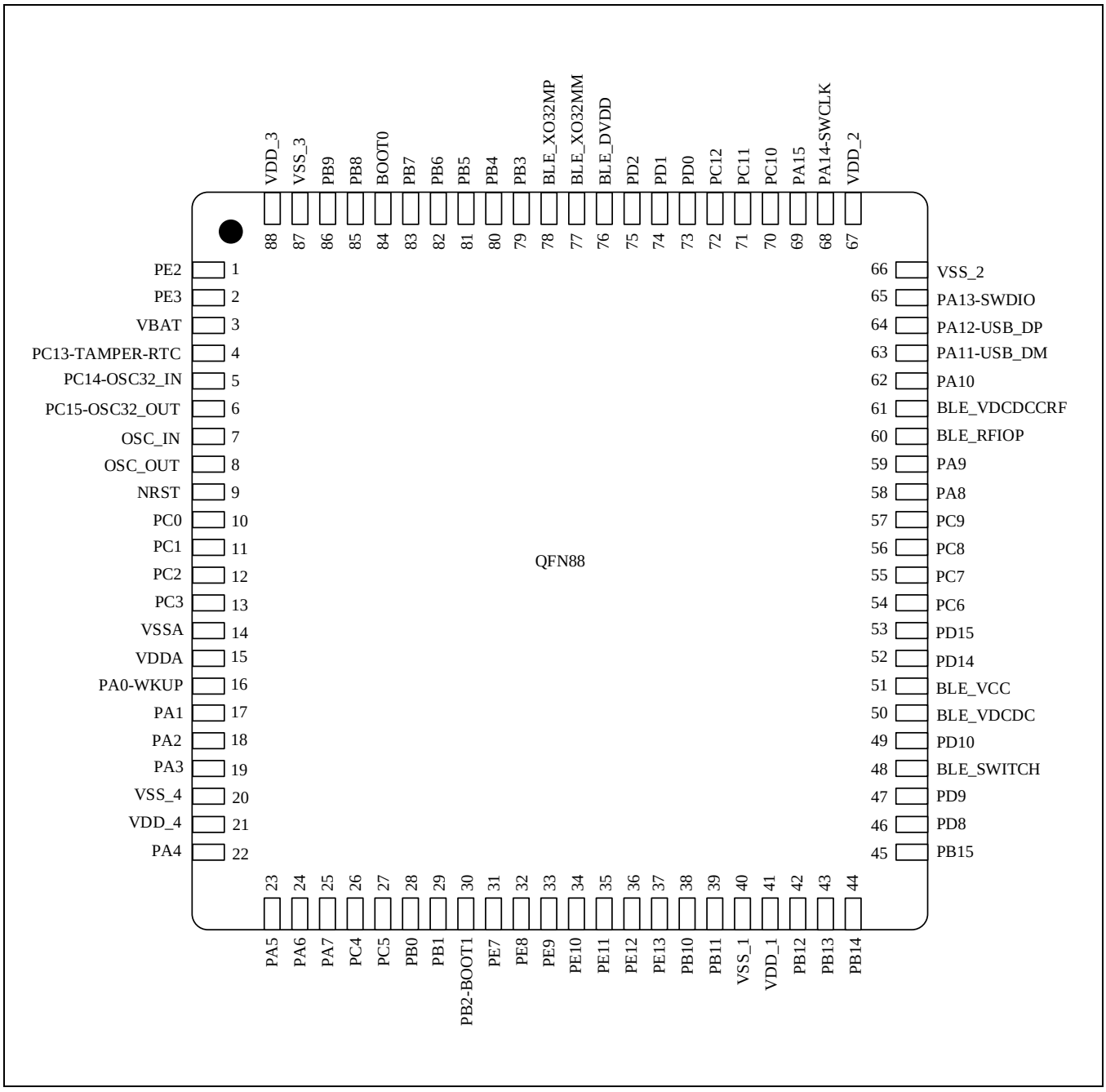
3.3 QFN88 package

3.3.1 QFN88 pin distribution



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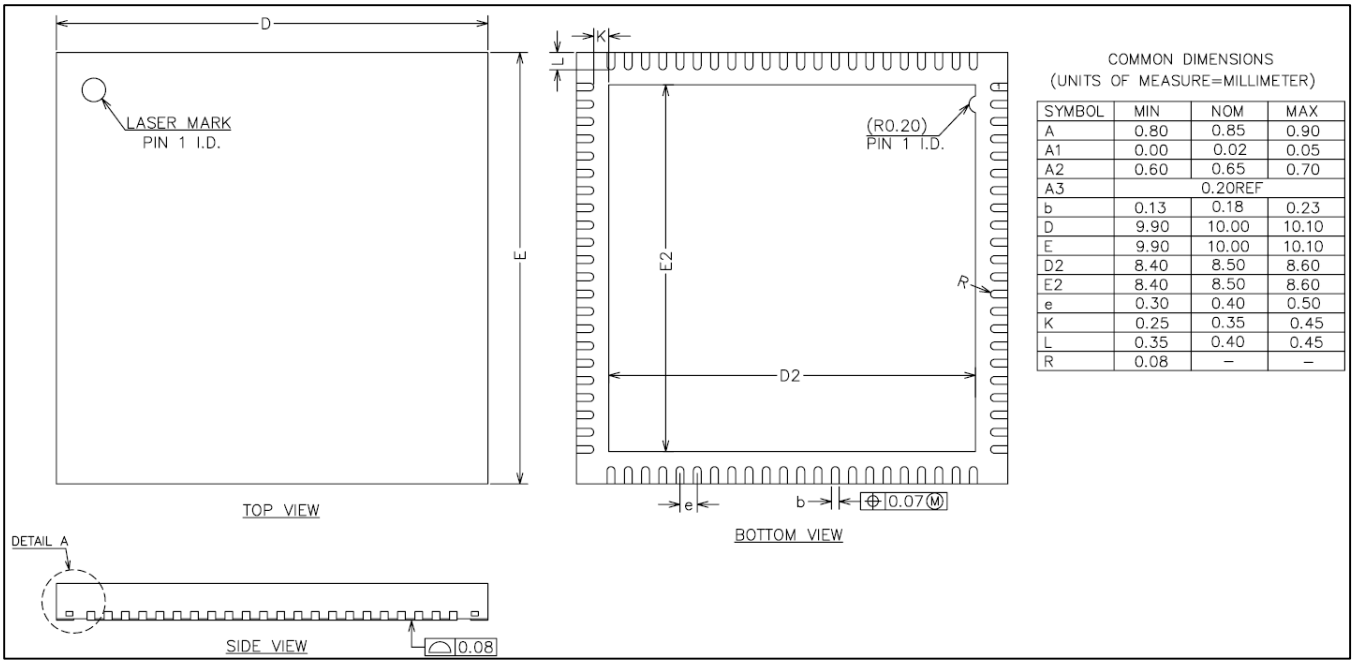
3.3.2 QFN88 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.13	0.18	0.23
D	9.90	10.00	10.10
E	9.90	10.00	10.10
D2	8.40	8.50	8.60
E2	8.40	8.50	8.60
e	0.30	0.40	0.50
K	0.25	0.35	0.45
L	0.35	0.40	0.45
R	0.08	–	–

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4 Version history

Version	The date	Note
V1.0	2020.2.12	New document
V1.1	2020.9.16	1. Modified some power consumption parameters 2. Modified the support of SD protocol
V1.1.1	2020.12.15	1. Optimize product model resource configuration instructions
V1.2	2022.04.27	1. Updated QFN48 package package drawing 2. Modify the package type that UART does not support 3. Modify resource configuration description(only 88 pins packages support DVP)
V1.3.0	2024.11.19	1. Modify Naming rules to Ordering information, modify ordering information table

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