User Guide

# N32A455 Series PLL user guide

## Introduction

The N32A455 series of microcontrollers from NSING are equipped with a built-in PLL (Phase-Locked Loop) module, which provides a clock for the system.

This document aims to help users correctly use the PLL of the N32A455 series and improve the operational stability of the PLL.



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# 1. Overview of PLL in N32A455 series

## 1.1 PLL features

- Input frequency range of Fin: 4 MHz to 32 MHz
- Input frequency range of PFD: 4 MHz to 32 MHz
- Output frequency range:
  - 32 MHz to 144 MHz
- Reference clock options:
  - HSI clock
  - HSE clock
- Power supply voltage: 1.8V-3.6V
- The PLL multiplication factor must be 8 or greater to ensure loop stability

## 1.2 Basic Working Principle of PLL

The PLL of the N32A455 series integrate a Phase Frequency Detector (PFD), Charge Pump (CP), Low-Pass Filter (LPF), Voltage-Controlled Oscillator (VCO) and other related modules. All basic building blocks as well as fully programmable frequency dividers are integrated within the core. The maximum output frequency of the PLL in the N32A455 series can reach 144MHz. They support an operating voltage range of 1.8V to 3.6V and an ambient temperature range of -40℃ to 105℃.



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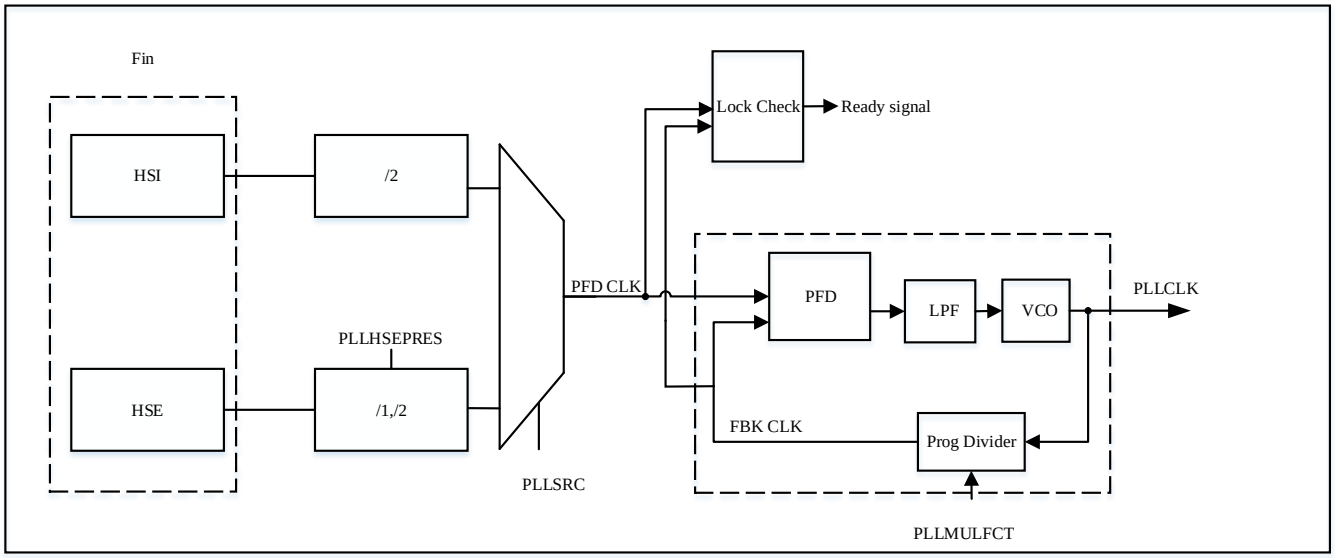




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# 2. N32A455 series PLL working mode

**PLL working mode**

| MCU power mode | PLL clock source | RCC_CFG. PLLHSERES | RCC_CTRL.PLLEN | RCC_CFG.PLLSRC |
|---|---|---|---|---|
| Run mode | HSI/2 | - | 1 | 0 |
| | HSE | PLLHSERES=0 | 1 | 1 |
| | HSE/2 | PLLHSERES=1 | 1 | 1 |
| Sleep mode | HSI/2 | - | 1 | 0 |
| | HSE | PLLHSERES=0 | 1 | 1 |
| | HSE/2 | PLLHSERES=1 | 1 | 1 |
| STOP0 mode | - | - | 0 | - |
| STOP2 mode | - | - | 0 | - |
| STANDBY mode | - | - | 0 | - |



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# 3. Precautions for Using PLL in N32A455 Series

## 3.1 PLL Configuration Process

1. Configure the PLL clock source, selecting HSI/2, HSE, or HSE/2 as the PLL clock source.
2. Configure the PLL multiplication factor.
3. Enable the PLL.
4. Wait for the PLL ready flag.
5. Switch the system clock to PLL.

Note: The PLL configuration cannot be dynamically modified. If it is necessary to modify the PLL configuration while the PLL is operating as the system clock source, the system clock source must first be switched to HSE or HSI. After the switch is completed, disable the PLL, and then execute the above configuration process (steps 1, 2, 3, 4, 5).

## 3.2 PLL Clock Sources

Reference clock for PLL PFD:

When PLLSRC=0, we select the HSI clock as the reference clock for the PLL, and its frequency is calculated as follows:

$$f_{pfd} = \frac{f_{HSI}}{2}$$

When PLLSRC=1, we select the HSE clock as the reference clock for the PLL, and its frequency is calculated as follows:

$$f_{pfd} = \frac{f_{HSE}}{\text{PLLHSEPRE} + 1}$$

Note: The PFD clock frequency range is 4 MHz ~ 32 MHz.

## 3.3 PLL Output Frequency

The PLL multiplication factor can be configured by setting RCC_CFG.PLLMULFCT[4:0]. The multiplication factor "M" is as follows:



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00000: PLL input clock ×2

00001: PLL input clock ×3

00010: PLL input clock ×4

……

11101: PLL input clock ×30

11110: PLL input clock ×31

11111: PLL input clock ×32

Note: The PLL multiplication factor must be 8 or greater to ensure loop stability.

$$f_{PLL} = M * f_{pfd}$$

The PLL output frequency range is 32 MHz to 144 MHz.



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# 4. Version History

| Version | Date | Changes |
|---|---|---|
| V1.0.0 | 2025.08.08 | Initial release |



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