ES_N32WB03x Series Errata Sheet V1.0

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Note: “ /” means this version is not applicable； “●” means this version is applicable to this erratum description.

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2 System Clock Control（RCC）

2.1 Note to use of RCC_LSCTRL register

Description

After waking up from the Sleep mode, if we operate the register RCC_CFG, the register RCC_LSCTRL will reset to the default value.

Solution

After waking up from the Sleep mode, first write in the register RCC_LSCTRL, and then operate the register RCC_CFG.

2.2 RCC_AHBRST's ADCRST bit reset ADC

Description

Setting the RCC_AHBPRST register's ADCRST bit cannot correctly reset the ADC module.

Solution

When we need to reset the ADC module, manually assign default value to all ADC module registers.

3 Lower Power Universal Asynchronous Receiver-Transmitter (LPUART)

3.1 When LSI 32K as clock source and 9600 baud rate,byte wake-up is abnormal

Description

When 32K is used as clock source for LPUART, due to indivisibility between baud rate and clock source, the baud rate will be devious, resulting in wrong byte judgement when waking up, so it cannot wake up.

Solution 1

When LSI needs to be used as LPUART clock source, it is recommended to use LSI 32.768K.

Solution 2

Use LSE as the clock source of LPUART.

4 Serial Peripheral Interface (SPI)

4.1 SPI

4.1.1 SPI baud rate setup

Description

When in the SPI master mode and CRC calibration function are enabled, and the SPI clock frequency is above 8MHz, the CRC calibration is abnormal.

Solution

When in the SPI master mode and CRC calibration function are enabled, the SPI clock frequency is no more than 8MHz.

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4.1.2 CRC calibration in slave mode

Description

When SPI works in the slave mode and has enabled CRC calibration, even the NSS pin is of high level, as long as SPI receives the clock signal, it will still conduct CRC calculation.

Solution

Before CRC calibration, clear the CRC data register first, so that the master and slave devices are synchronized in CRC calibration.

4.1.3 When the Bluetooth protocol stack is used, SPI1 interrupts and fails to respond

Description

When the Bluetooth protocol stack is enabled, the ROM interrupt vector table is used, but this interrupt vector table does not map out SPI1 interrupt callback function, so it cannot be called back.

Solution

Use DMA receiver or SPI2 module.

5 I2C Interface

5.1 Abnormal signal interference

Description

During the I2C operation process, SCL and SDA might be disturbed by glitch during communication, resulting in abnormal communication.

Solution

1. Reduce interference; (for example：adding filtering circuits such as capacitors on the I2C bus)
2. Implement a peripheral recovery mechanism; (configure SCL as an IO mode and continuously generate 9 clock pulses onto the clock bus, forcing the slave device to release its ACK bit, thereby releasing SDA to high level and restoring the bus to an idle state)
3. Use IO software to simulate I2C.

6 Key Scan (KEYSCAN)

6.1 Retention voltage requirement for KEYSCAN in Sleep mode

Description

Under the sleep mode, KEYSCAN requires higher retention voltage, or there might be the risks that KEYSCAN and EXTI3 functions cannot wake up the chip.

Solution

Increase the retention voltage . Configuration: *(uint32_t*)0x40007014 = 0x00000818.

7 ADC clock

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7.1 Configuration of ADC clock

Description

The ADC clock is HSE , if the hardware board without 32M HSE crystal and without BLE function, the ADC will be sampling anomaly .

Solution

Configure the HSI as ADC clock, configuration: *(uint32_t*)0x40011004 |= 0x40.

8 Chip Silk Screen Printing and Version Description

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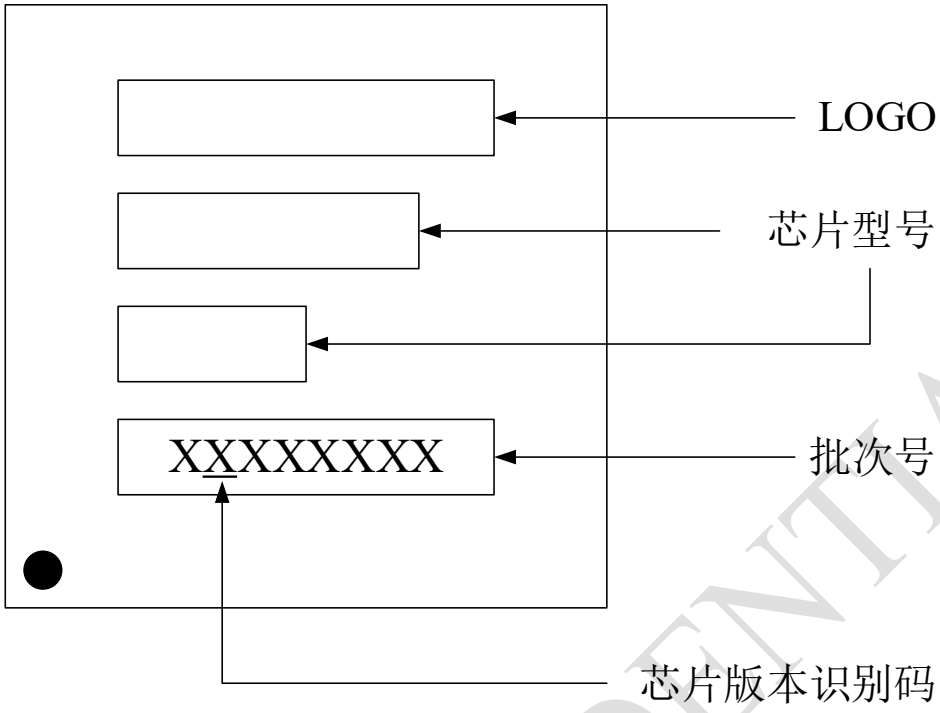

芯片型号 Chip model
批次号 Batch number
芯片版本识别码 Chip version identification code

9 Version History

Date	Version	Modification
2025/08/29	V1.0	Initial version

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