Use guide

N32G43X & N32L40X & N32L43X series MCU LSE crystal selection guide

Introduction

This document provides guidance for LSE crystal selection of N32G43X/N32L40X/N32L43X series MCU.

Contents

1. LSE crystal selection instructions

1.1 External crystal circuit

Figure 1-1 shows the typical design of LSE external crystal, where R_F feedback resistor has been designed inside the chip, so users do not need to add this resistor to the chip.

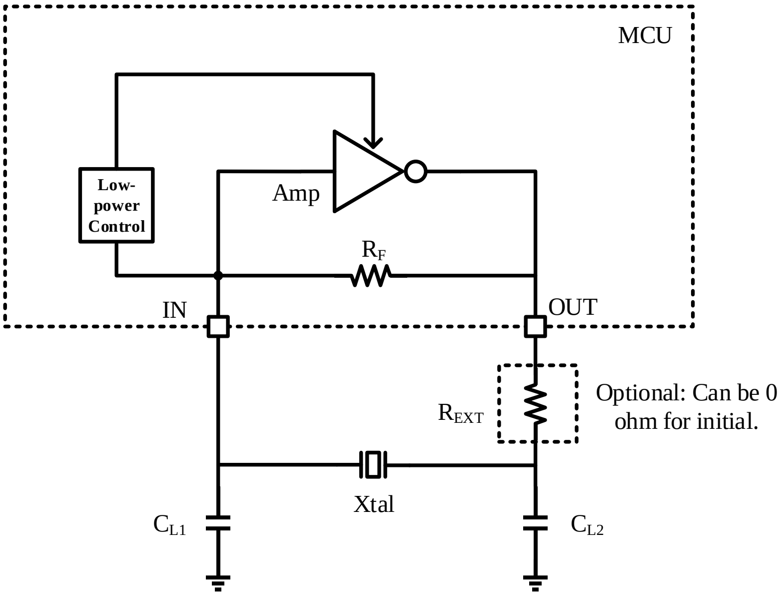

Figure 1-1 a typical application using 32.768KHz crystals1

1.2 LSE matching capacitance calculation

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768kHz crystal/ceramic resonator.In applications, crystal and load capacitors must be as close to the oscillator pins as possible to minimize output distortion and stabilization time at startup.For detailed crystal parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer.

For C_{L1} and C_{L2}, it is recommended to use ceramic capacitors to match the requirements of the crystal, C_{L1} and C_{L2} are usually the same value.

Load capacitance CL is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, which C_{stray} is the capacitance of the pin and the PCB or PCB related capacitance.

For example, if a load capacitor is selected CL=7pF crystal, and C_{stray}=1pF, so C_{L1}=C_{L2}= 12pF.

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1.3 LSE crystal test

1.3.1 LSE crystal parameter configuration

When LSE external crystal is used, void RCC_ConfigLse(uint8_t RCC_LSE, uint16_t LSE_Trim) function is called and parameter uint16_t LSE_Trim is used to configure crystal parameters, as shown in the following code example:

```
/**
 * @brief  Configures the External Low Speed oscillator (LSE).
 * @param RCC_LSE specifies the new state of the LSE.
 *   This parameter can be one of the following values:
 *     @arg RCC_LSE_DISABLE LSE oscillator OFF
 *     @arg RCC_LSE_ENABLE LSE oscillator ON
 *     @arg RCC_LSE_BYPASS LSE oscillator bypassed with external clock
 * @param LSE_Trim specifies LSE Driver Trim Level.
 */
void RCC_ConfigLse(uint8_t RCC_LSE,uint16_t LSE_Trim)
{
    //PWR DBP set 1
    /* Enable PWR Clock */
    RCC_EnableAPB1PeriphClk(RCC_APB1_PERIPH_PWR, ENABLE);
    PWR->CTRL1 |=  0x100;
    /* Check the parameters */
    assert_param(IS_RCC_LSE(RCC_LSE));
    /* Reset LSEEN LSEBYP and LSECLKSSEN bits before configuring the LSE ------------------*/
    *(__IO uint32_t*)LDCTRL_ADDR &= (~(RCC_LDCTRL_LSEEN | RCC_LDCTRL_LSEBP | RCC_LDCTRL_LSECLKSSEN));
    /* Configure LSE (RCC_LSE_DISABLE is already covered by the code section above) */
    switch (RCC_LSE)
    {
    case RCC_LSE_ENABLE:
        /* Set LSEON bit */
        *(__IO uint32_t*)LDCTRL_ADDR |= RCC_LSE_ENABLE;
        LSE_XtalConfig(LSE_Trim);
        break;
    case RCC_LSE_BYPASS:
        /* Set LSEBYP and LSEON bits */
        *(__IO uint32_t*)LDCTRL_ADDR |= (RCC_LSE_BYPASS | RCC_LSE_ENABLE);
        break;
    default:
        break;
    }
}
```

Table 1-1 lists two recommended configuration values. Different configuration values have a great influence on the final crystal properties, as follows:

1) **Low power configuration (configuration values: 0xFF) :** compared with the default configuration after the chip is powered on, this configuration enhances the LSE driver capability and supports more crystal models.
2) **Normal configuration (configuration values: 0x1FF) :** At the same time, the driving capability and steady-state operating current of the LSE are enhanced, and the crystal compatibility is further improved. This configuration value is relatively low-power configuration, and the power consumption of the crystal circuit is slightly increased.

Table 1-1 Comparison of LSE configuration values11

Configuration items	Configuration values
Low power configuration	0xFF
Normal configuration	0x1FF

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The following sections will provide the test data of different crystal parameter configuration values for customer application reference.

1.3.2 Crystal frequency test

1.3.2.1 Normal temperature frequency test

In LSE design, it is necessary to select the appropriate hardware matching capacitance and crystal configuration values.

Refer to the peripheral hardware design in Figure 1-1, select a crystal and connect the capacitor to test the crystal frequency. The crystal signal can be output to the frequency meter or other frequency testing instruments through MCO.

- Test example:

The selected crystal load capacitance CL=7pF, C_{stray} calculated at 1pF, then C_{L1}=C_{L2}= 12 pF.
(C_{stray} value of is related to different test boards, and the user can fine-tune according to the test frequency value of C_{L1} and C_{L2}).

As shown in Figure 1-2, C_{L1} and C_{L2} chip capacitance is 12pF, and the crystal output frequency of the three test plates is compared as follows.

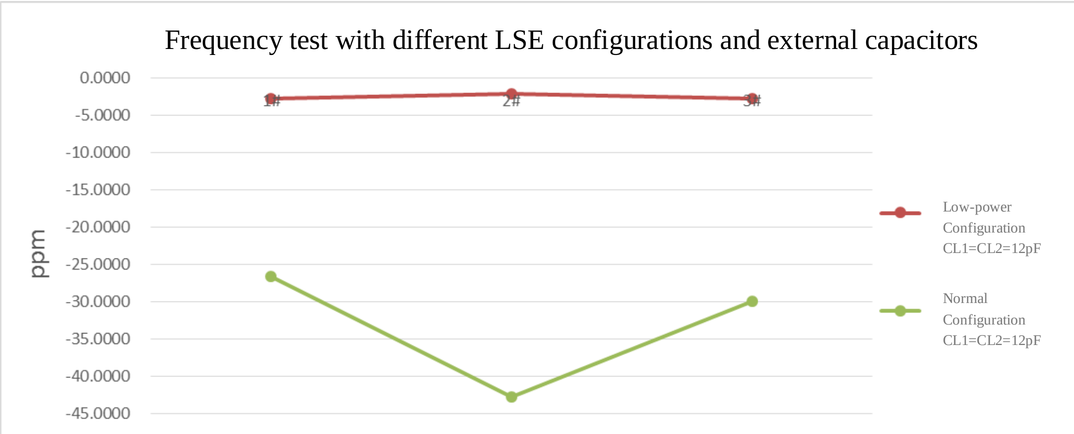

Figure 1-2 Normal temperature conditions, $C2_{L1}$=C_{L2}=12pF, LSE output frequency

As shown in Figure 1-2, the same hardware design and different configuration values have certain influence on the frequency. Under normal configuration conditions, the frequency is lower than that in low-power configuration, and is less than -20ppm. In this case, The crystal frequency can be increased by decreasing C_{L1} and C_{L2}.

As shown in Figure 1-3, C_{L1} and C_{L2} patch capacitance is adjusted from 12pF to 10pF (for the normal configuration), and the output frequency of the three test boards is compared before and after the capacitor is adjusted.

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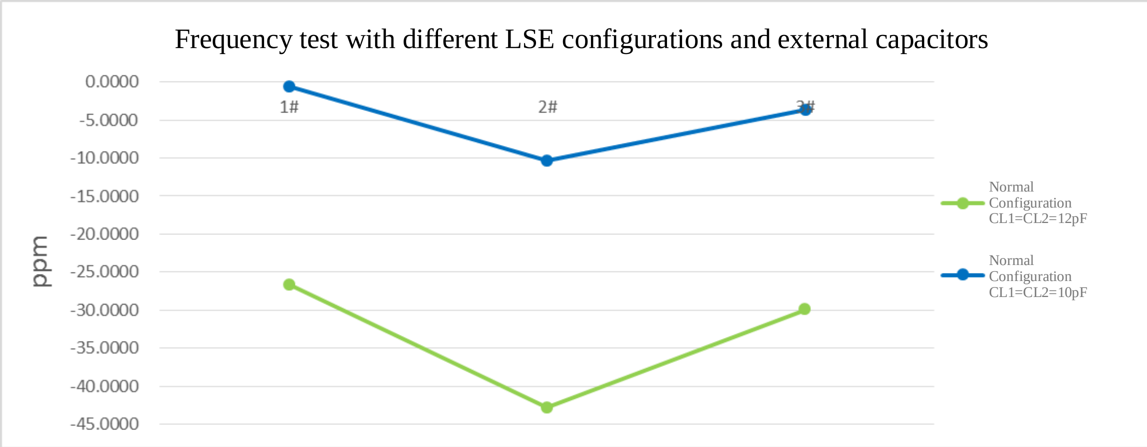

Figure 1-3 Normal temperature conditions, $C3_{L1}$!=C_{L2}, LSE output frequency (normal configuration)

1.3.2.2 High and low temperature frequency test

Refer to Figure 1-4 for the LSE output frequency in the low-power configuration at high and low temperatures.

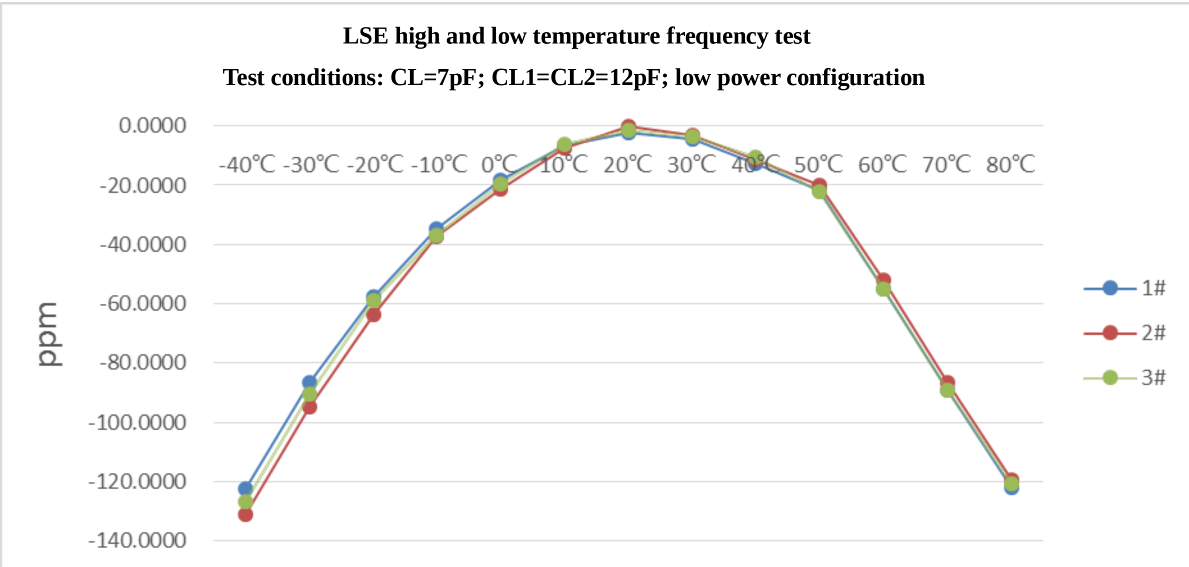

Figure 1-4 low power configuration value, LSE high and low temperature output frequency4

Refer to Figure 1-5 for the LSE output frequency in normal configuration at high and low temperature.

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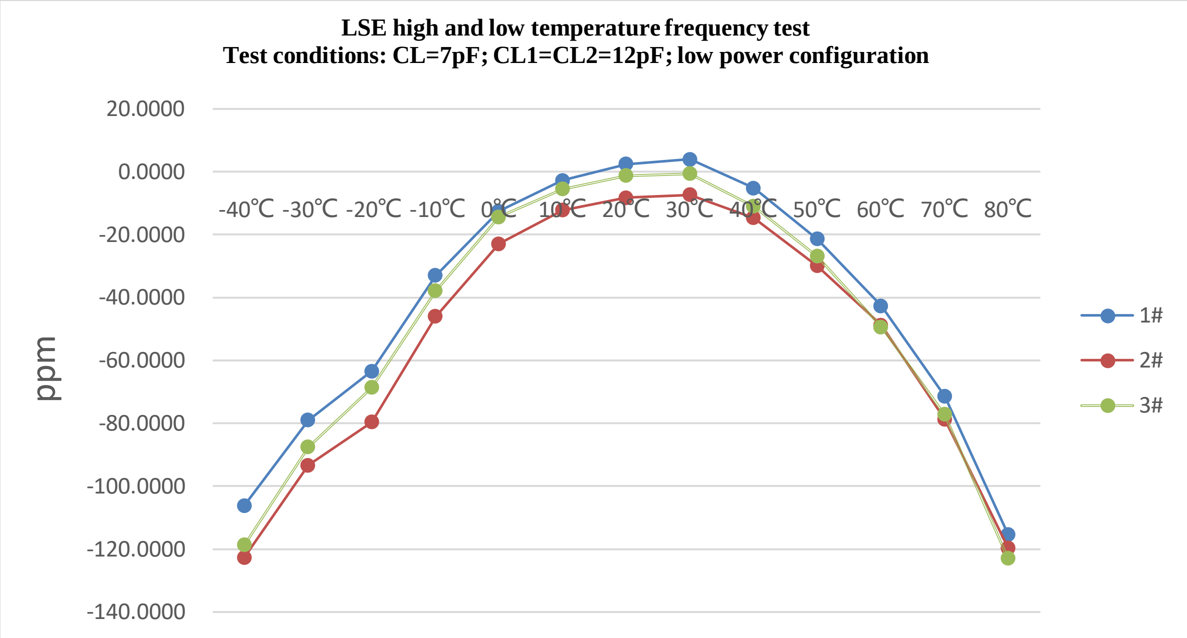

Figure 1-5 Normal configuration value, LSE high and low temperature output frequency5

1.3.3 Power consumption test

Figure 1-6 shows the power consumption of the chip in different configurations. Normal configuration compared with the low-power configuration, the power consumption in STOP2 mode increases about 0.8uA.

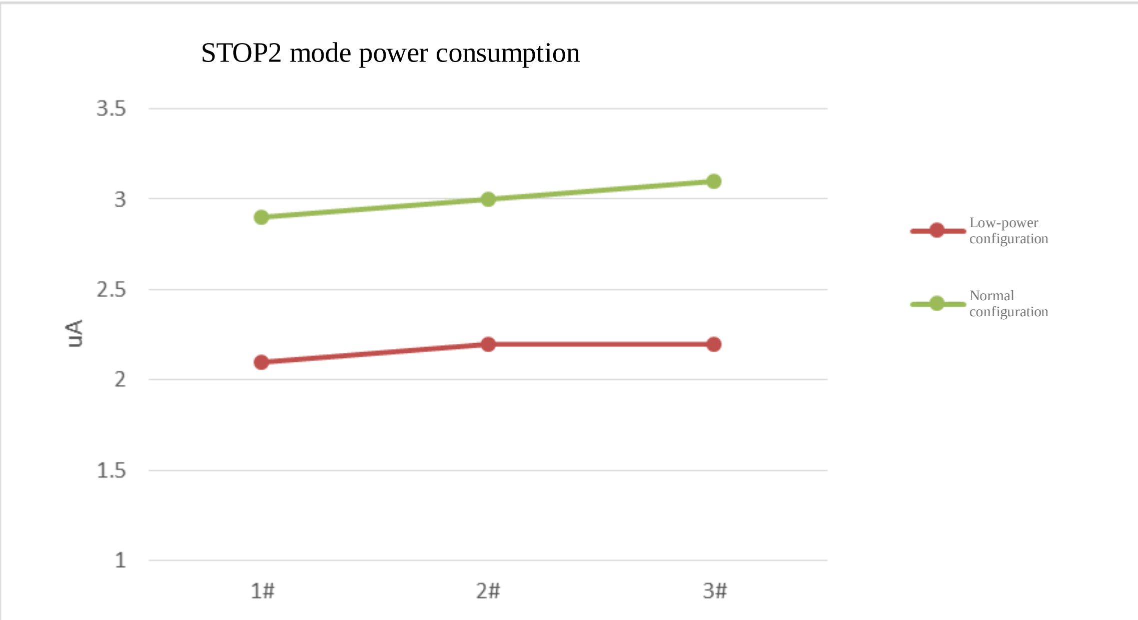

Figure 1-6 STOP2 mode power consumption under different register configuration conditions6

1.3.4 Crystal compatibility list

N32G43X/N32L40X/N32L43X series MCU when choosing external 32.768kHz crystal, it should be noted that the selected crystal can work normally in the whole temperature range.

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The crystal configuration parameters of the chip are different, and the adaptable crystal models are also different.

Refer to Table 1-2 for the crystal compatibility list for full temperature test. The crystals in this list can be compatible with both low power configuration values and normal configuration values.

Table 1-2 LSE crystal compatibility list12

No.	Crystal model	package	Manufacturer	CL (pF)	CO (pF)	ESR(max) (kΩ)	temperature range (℃)
1	TFX-04-32.768K(7PF)	1610	RIVER	7	1.3	90	-40~85
2	TFX-04-32.768K			12.5	1.3	90	
3	1TJH090DR1A0086		KDS	9	1.3	90	
4	DST1610A 32.768KHz			12.5	1.3	90	
5	X1A0001210005		EPSON	12.5	1.2	90	
6	SC-16S 32.768kHz 20PPM 12.5pF		SEIKO	12.5	1.2	90	
7	FC-12M 32.768000 kHz 7.0+20.0-20.0/X1A0000610006	2012	EPSON	7	1.3	90	
8	TJXM32768K2TGDCNT2T		TAE	12.5		70	
9	1TJG125DR1A0019		KDS	12.5	1.3	80	
10	FC-135R 32.768KHz 9PF 20PPM/ X1A0001410002	3215	EPSON	9	1.1	50	
11	FC-135 32.768KHz 9PF 20PPM/ Q13FC13500003			9	1	70	
12	FC-135 32.768KHz 12.5PF 20PPM/ Q13FC13500004			12.5	1.2	70	
13	FC-135 32.768KHz 9PF 20PPM/ FC-135 32.7680KA-AC			9	1	70	
14	SC-32S 32.768kHz 7pF 20ppm		SEIKO	7	1	70	
15	SC-32S 32.768kHz 12.5pF 20ppm			12.5	1	70	
16	SC-32S 32.768kHz 9pF 20ppm			9	1	70	
17	1TJF125DP1A000A		KDS	12.5	1.3	80	
18	7LC32768F12UC		SJK	12.5	1.2	70	
19	FC31M2-32.768-NTLLLDT		HCI	12.5	1.5	70	
20	X321532768KGD2SI		YXC	12.5	1.2	70	
21	ETST00327000JE		HOSONIC	12.5	2	70	
22	TCXM32768K2NGDCZT2T		TAE	12.5	2	80	
23	XDMCZLNDDF-0.032768MHZ		TAITIEN	12.5			
24	KFC3276812520		KYX	12.5	1.2	70	
25	F3K232768PWQAC		JYJE	12.5		70	
26	26S-32.768-12.5-10-10/B	DT26	LIMING	12.5		90	
27	MC-146 32.768KHz 9PF 20PPM/ Q13MC14610004	MC-146	EPSON	9	0.8	65	
28	MC-146 32.768KHz 12.5PF 20PPM/ Q13MC14620002			12.5	0.8	65	
29	SSP-T7-F 32.768kHz 20PPM 7pF		SEIKO	7	0.8	65	

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30	FR07S4-32.768-N07LLDT		HCI	7	0.8	65	
31	FR07S4-32.768-NTLLLDT			12.5	0.8	65	
32	TSXM32768K4KGDCZT3T		TAE	12.5	0.8	65	
33	7MC32768F12UC		SJK	12.5	1.2	70	
34	M132768PWPAC		JYJE	12.5		65	
35	CD01K032768FEPBAEAE	DT26	TKD	8	1.4	40	-20~70
36	CD01K032768ACNBAEAE			12.5	1.4	40	
37	CD01K032768DGRBAEAE			6	1.4	40	
38	Y26003271C2040DYJY		JGHC	12.5		40	
39	X206032768KGB2SC		YXC	12.5		40	
40	146-32.768-12.5-20-20/A	MC-146	LIMING	12.5			
41	7L032768NW2		HD	12.5	0.8	65	
42	X308032768KGB2SC	DT38	YXC	12.5		40	
43	CD02K032768AEPBAEAE		TKD	12.5	1.8	30	
44	WTL3T45322LZ		WTL	12.5	1.5	40	
45	SMD31327681252090	3215	JGHC	12.5	1	65	-10~60
46	S3132768072070			7	1	65	
47	DT-38 32.768KHz	DT38	KDS	12.5	1.3	30	
48	Y308327681252075		JGHC	12.5	1.1	40	

Note: Above crystal compatibility test of the chip supply voltage V_{DD}= 3.3 V.

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