N32G05x series

32-bit ARM Cortex®-M0 microcontroller

User manual V1.1.0

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Email：info@nationstech.com
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Email：info@nationstech.com
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1 Abbreviations in The Text

1.1 List of Abbreviations for Registers

The following abbreviations are used in register descriptions:

read/write(rw)	Software can read and write this bit.
read-only(r)	Software can only read this bit.
write-only(w)	Software can only write this bit, and reading this bit will return the reset value.
read/clear(rc_w1)	Software can read this bit or clear it by writing' 1', and writing' 0' has no effect on this bit.
read/clear(rc_w0)	Software can read this bit or clear it by writing' 0', and writing' 1' has no effect on this bit.
read/clear by read(rc_r)	Software can read this bit. Reading this bit will automatically clear it to' 0'. Writing' 0' has no effect on this bit.
read/set(rs)	Software can read or set this bit. Writing' 0' has no effect on this bit.
read-only write trigger(rt_w)	Software can read this bit and write' 0' or' 1' to trigger an event, but it has no effect on this bit value.
toggle(t)	Software can only flip this bit by writing' 1', and writing' 0' has no effect on this bit.
Reserved(Res.)	Reserved bit, must be kept at reset value.

1.2 Available Peripherals

For all models of N32G05x microcontroller series, the existence and number of a peripheral, please refer to the data sheet of the corresponding model.

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2 Memory and Bus Architecture

2.1 System Architecture

2.1.1 Bus Architecture

The main system consists of the following parts:

- Two main drive units:
  - Cortex®-M0 core system bus
  - General purpose DMA
- Six passive units
  - Embedded SRAM
  - Embedded Flash memory
  - ADC
  - AHB to AHB bridge, it connects some AHB devices
  - AHB to APB bridges (AHB2APB1 and AHB2APB2), which connect all APB devices

These are connected to each other through a multi-level AHB bus architecture, as shown in Figure 2-1:

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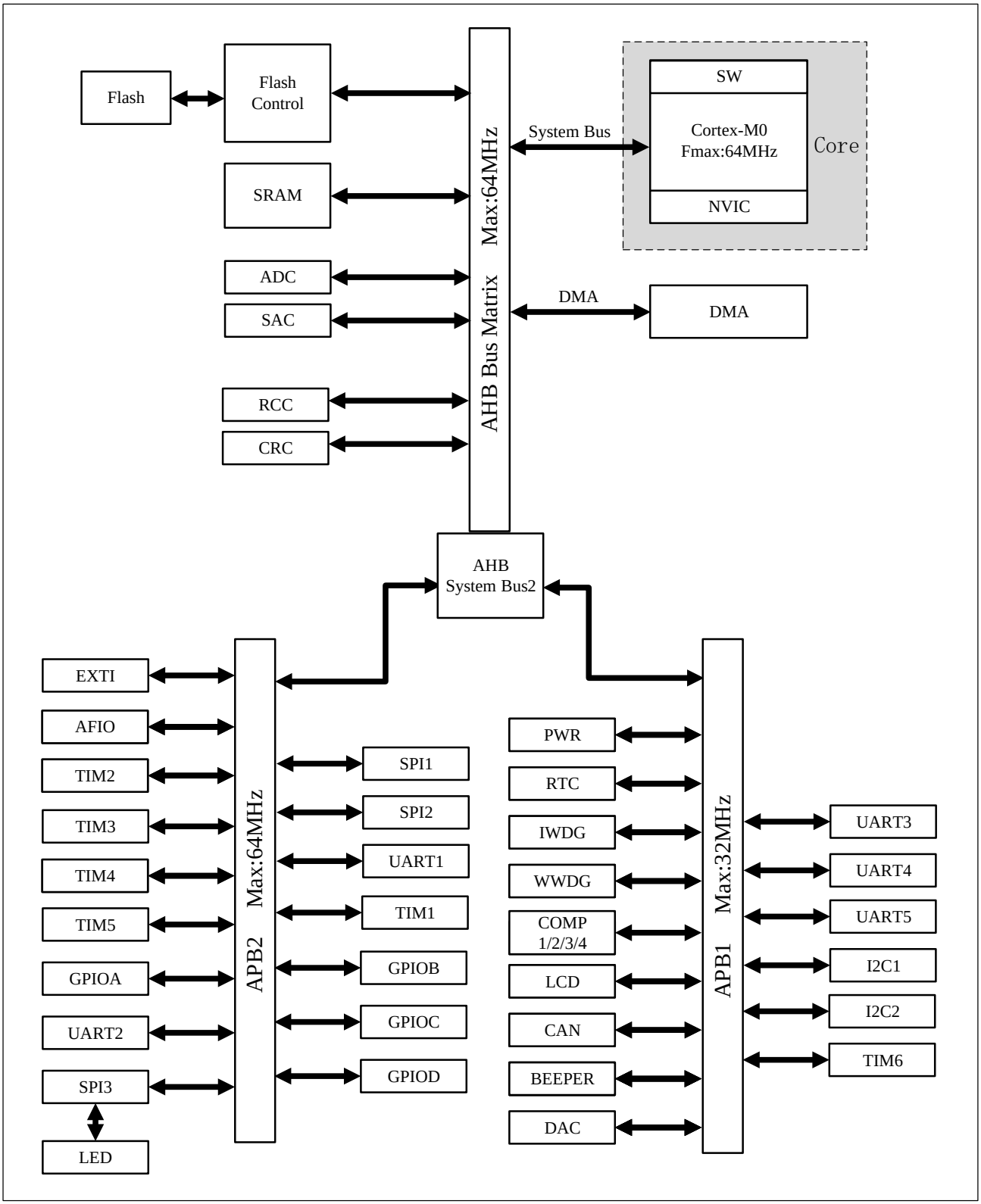
Figure 2-1 Bus Architecture



- CPU System bus: It connects the kernel Sbus of the Cortex®-M0 to bus matrix, and is used for instruction pre-fetch, data loading (constant loading and debug access) and AHB/APB peripheral access.
- DMA bus: The DMA's AHB master interface is connected to the bus matrix, which coordinates access from the kernel

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and DMA to SRAM, Flash and peripherals.

- The bus matrix coordinates access arbitration between the kernel system bus and the DMA master bus. The arbitration uses a Round Robin algorithm. The bus matrix consists of two driver components (CPU system bus, DMA bus) and seven slave components (Flash memory interface, SRAM, ADC, RCC, CRC, SAC and AHB system bus 2). AHB system bus 2 is connected to two AHB2APB Bridges.
- The system consists of two AHB2APB Bridges, i.e. AHB2APB1 and AHB2APB2. APB1 contains 15 APB peripherals and the maximum speed of PCLK is 32MHz. APB2 contains 16 APB peripherals with a maximum PCLK speed equal to 64MHz.

2.1.2 Bus Address Mapping

The address mapping includes all AHB and APB peripherals: AHB peripherals, APB1 peripherals, APB2 peripherals, Flash, SRAM, System Memory, etc. The specific mapping is as follows:

Figure 2-2 Bus Address Map

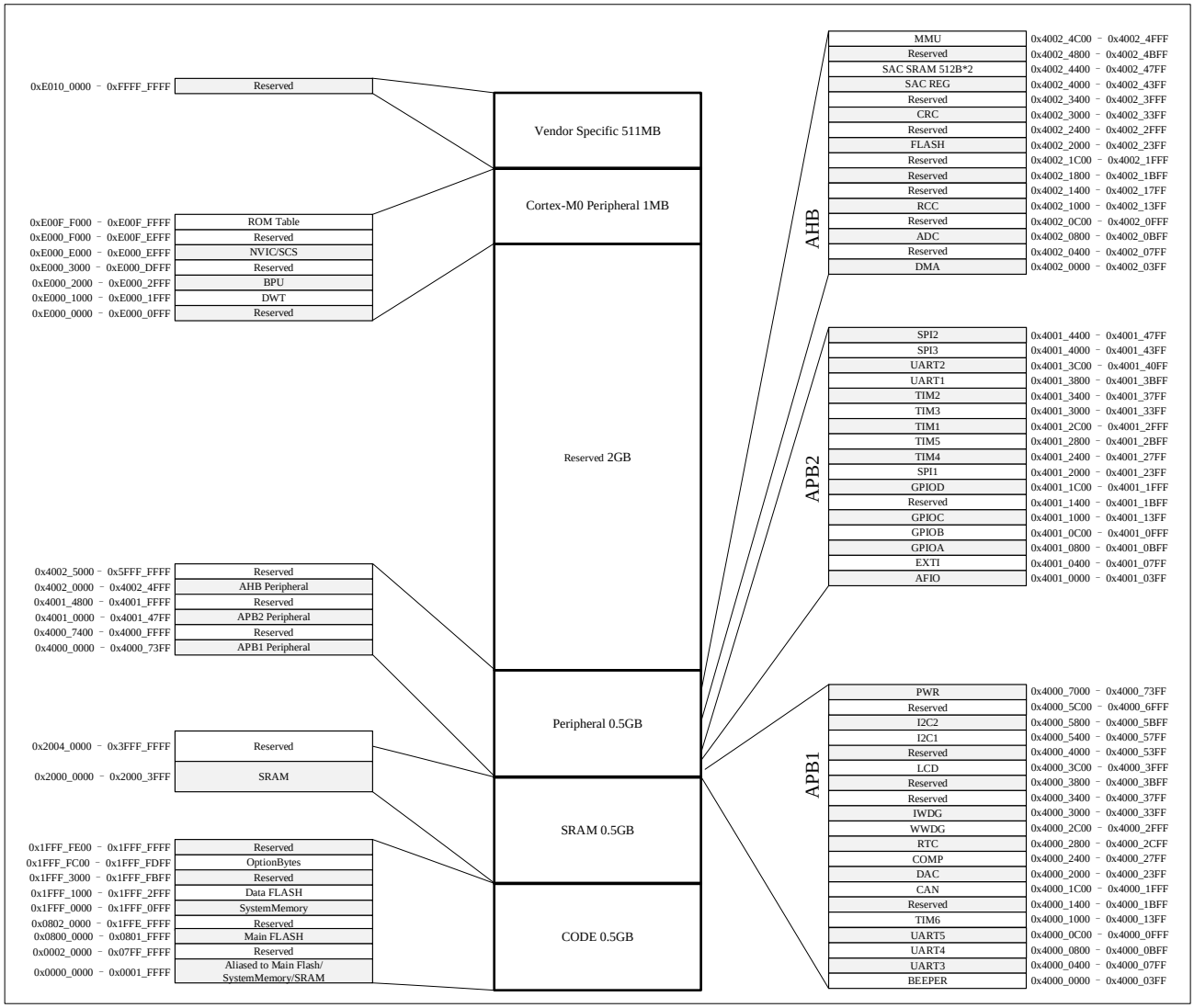

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Table 2-1 List of Peripheral Register Addresses

Address range	Peripherals	Bus
0x4002_4800 – 0x5FFF_FFFF	Reserved	AHB
0x4002_4400 – 0x4002_47FF	SAC SRAM 512B * 2	
0x4002_4000 – 0x4002_43FF	SAC REG	
0x4002_3400 – 0x4002_3FFF	Reserved	
0x4002_3000 – 0x4002_33FF	CRC	
0x4002_2400 – 0x4002_2FFF	Reserved	
0x4002_2000 – 0x4002_23FF	FLASH	
0x4002_1400 – 0x4002_1FFF	Reserved	
0x4002_1000 – 0x4002_13FF	RCC	
0x4002_0C00 – 0x4002_0FFF	Reserved	
0x4002_0800 – 0x4002_0BFF	ADC	
0x4002_0400 – 0x4002_07FF	Reserved	
0x4002_0000 – 0x4002_03FF	DMA	
0x4001_4800 – 0x4001_FFFF	Reserved	APB2
0x4001_4400 – 0x4001_47FF	SPI2	
0x4001_4000 – 0x4001_43FF	SPI3	
0x4001_3C00 – 0x4001_3FFF	UART2	
0x4001_3800 – 0x4001_3BFF	UART1	
0x4001_3400 – 0x4001_37FF	TIM2	
0x4001_3000 – 0x4001_33FF	TIM3	
0x4001_2C00 – 0x4001_2FFF	TIM1	
0x4001_2800 – 0x4001_2BFF	TIM5	
0x4001_2400 – 0x4001_27FF	TIM4	
0x4001_2000 – 0x4001_23FF	SPI1	
0x4001_1C00 – 0x4001_1FFF	GPIOD	
0x4001_1400 – 0x4001_1BFF	Reserved	
0x4001_1000 – 0x4001_13FF	GPIOC	
0x4001_0C00 – 0x4001_0FFF	GPIOB	
0x4001_0800 – 0x4001_0BFF	GPIOA	
0x4001_0400 – 0x4001_07FF	EXTI	
0x4001_0000 – 0x4001_03FF	AFIO	
0x4000_7400 – 0x4000_FFFF	Reserved	APB1
0x4000_7000 – 0x4000_73FF	PWR	
0x4000_5C00 – 0x4000_6FFF	Reserved	
0x4000_5800 – 0x4000_5BFF	I2C2	
0x4000_5400 – 0x4000_57FF	I2C1	
0x4000_4000 – 0x4000_53FF	Reserved	
0x4000_3C00 – 0x4000_3FFF	LCD	

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Address range	Peripherals	Bus
0x4000_3800 – 0x4000_3BFF	Reserved	
0x4000_3400 – 0x4000_37FF	Reserved	
0x4000_3000 – 0x4000_33FF	IWDG	
0x4000_2C00 – 0x4000_2FFF	WWDG	
0x4000_2800 – 0x4000_2BFF	RTC	
0x4000_2400 – 0x4000_27FF	COMP	
0x4000_2000 – 0x4000_23FF	DAC	
0x4000_1C00 – 0x4000_1FFF	CAN	
0x4000_1400 – 0x4000_1BFF	Reserved	
0x4000_1000 – 0x4000_13FF	TIM6	
0x4000_0C00 – 0x4000_0FFF	UART5	
0x4000_0800 – 0x4000_0BFF	UART4	
0x4000_0400 – 0x4000_07FF	UART3	
0x4000_0000 – 0x4000_03FF	BEEPER	

2.1.3 Boot Management

2.1.3.1 Boot address

During system startup, you can select the BOOT mode after the reset through the BOOT0 pin and the user option byte BOOT configuration. The value of the BOOT pin will be re-sampled after the system is reset or exits from the Power Down mode. After a startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000_0000 and executes the code from the reset vector address indicated by address 0x0000_0004. Because of the Cortex®-M0 always gets the top-of-stack value and reset vector from addresses 0x0000_0000 and 0x0000_0004, so boot is only suitable for booting from the CODE area, and address remapping is designed for boot space. There are three boot modes to choose from:

- Boot from Main Flash:
  - Main Flash memory is mapped to the boot space (0x0000_0000);
  - Main Flash memory is accessible in two address areas, 0x0000_0000 or 0x0800_0000;
- Boot from System Memory:
  - System Memory is mapped to boot space (0x0000_0000);
  - System Memory can be accessed in two address areas, 0x0000_0000 or 0x1FFF_0000;
- Boot from the embedded SRAM:
  - The embedded SRAM is mapped to boot space (0x0000_0000);
  - The embedded SRAM is accessible in two address areas, 0x0000_0000 or 0x2000_0000;

2.1.3.2 Boot configuration

Three different BOOT modes can be selected through the BOOT0 pin and the user option byte BOOT configuration.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Table 2-2 List of Boot Mode

Boot mode select pin					Boot mode	Specifies the start address for accessing memory space in boot mode		
nBOOT1	nBOOT0	BOOT0 pin	nSWBOOT0	BOOT0_CFG		Main Flash	System Memory	SRAM
X	X	0	1	1	Main Flash start	0x0000_0000 0x0800_0000	0x1FFF_0000	0x2000_0000
X	1	X	0					
1	X	1	1		System Memory Start	0x0800_0000	0x0000_0000 0x1FFF_0000	0x2000_0000
1	0	X	0					
0	X	1	1		SRAM start	0x0800_0000	0x1FFF_0000	0x0000_0000 0x2000_0000
0	0	X	0					
X	X	1	1	0	Main Flash start	0x0000_0000 0x0800_0000	0x1FFF_0000	0x2000_0000
X	1	X	0					
1	X	0	1		System Memory Start	0x0800_0000	0x0000_0000 0x1FFF_0000	0x2000_0000
1	0	X	0					
0	X	0	1		SRAM start	0x0800_0000	0x1FFF_0000	0x0000_0000 0x2000_0000
0	0	X	0					

Note: BOOT0 and GPIO are multiplexed, and there default settings during power-on are controlled by the BOOT0_CFG value.

2.1.3.3 Embedded boot loader

The embedded boot loader is stored in System Memory for reprogramming Flash Memory through UART1. The UART1 interface can run not only with an external clock (HSE) but also with the internal 8MHz oscillator (HSI). For further details, please refer to bootstrap manual.

2.1.3.4 Boot swap function

Boot swap can be used to update the secondary bootloader. Updating the secondary bootloader directly may fail due to temporary power loss or other reasons, leading to the loss of the original secondary bootloader code and causing the program to malfunction. The boot swap feature effectively prevents this issue.

Assuming the old and new secondary bootloaders are both 4KB or less in size, an example of application implementation:

- The chip defaults to starting from 0x08000000 after power-on.
- Received instructions from the host computer to program the secondary bootloader.
- The old secondary bootloader will erase the region from 0x08001000 to 0x08001FFF.
- The old secondary bootloader receives the program downloaded from the host computer and programs the new secondary bootloader into the region from 0x08001000 to 0x08001FFF.
- After the programming of the new secondary bootloader is completed, the old secondary bootloader will change the option byte USER5[7:0] to 0xF7 and perform a software reset.

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- After the software reset, the chip will boot from 0x8001000, which is the start of the new secondary boot region.
- At this point, if the new secondary bootloader detects that USER5[7:0] is not 0xFF, it will copy itself to 0x08000000. After the copying is completed, it will change USER5[7:0] to 0xFF and reset.
- After the chip reset, it will boot from 0x08000000, and the boot program will be the new secondary bootloader.

2.2 Memory System

The program memory, data memory, registers and I/O ports are organized in the same 4GB linear address space. Data bytes are stored in the memory in Little Endian format. The lowest numbered byte in a word is regarded as the least significant byte of the word, while the highest numbered byte is the most significant byte. The specifications of program memory and data memory are as follows.

2.2.1 FLASH Specification

The Flash consists of a main memory block and an information block, which are described below: (The capacity value in the following description does not include ECC)

- The maximum main memory block is 128KB, also known as main Flash memory, which contains 256 pages for storing and running user programs and storing data.
- The information area is 15.5KB, including 31 Pages, and consists of Data FLASH area (8KB), system memory area (4KB), system configuration area (3KB) and option byte area (0.5KB).
  - The Data FLASH area is 8KB, including 16 Pages, and is used for storing user data and cannot be used for code execution. It can be read, written, and erased.
  - The System Memory area is 4KB, including 8 Pages, also known as System Memory, and is used for storing and running the BOOT loader
  - The system configuration area is 3KB, including 6 Pages.
  - The Option Byte area is 0.5KB, including 1 Page, also known as Option Byte, with an effective space of 112B, Both the BOOT program and user program can read, write and erase this area.

2.2.1.1 Flash memory module organization

Both the main memory block and the information block are allocated to bus address space memory

Table 2-3 Flash Bus Address List

Memory Area	Page Name	Address Range	Size
The main memory area	Page 0	0x0800_0000 – 0x0800_01FF	0.5 KB
	Page 1	0x0800_0200 – 0x0800_03FF	0.5 KB
	Page 2	0x0800_0400 – 0x0800_05FF	0.5 KB
	⋮	⋮	⋮
	Page 255	0x0801_FE00 – 0x0801_FFFF	0.5 KB
Information area	System memory area	0x1FFF_0000 – 0x1FFF_0FFF	4KB
	Data Flash area	0x1FFF_1000 – 0x1FFF_2FFF	8KB
	System configuration area	0x1FFF_F000 – 0x1FFF_FBFF	3 KB
	Option byte area	0x1FFF_FC00 – 0x1FFF_FC6F	112B

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Email：info@nationstech.com
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Memory Area	Page Name	Address Range	Size
Memory area interface register	FLASH_AC	0x4002_2000 – 0x4002_2003	4B
	FLASH_KEY	0x4002_2004 – 0x4002_2007	4B
	FLASH_OPTKEY	0x4002_2008 – 0x4002_200B	4B
	FLASH_STS	0x4002_200C – 0x4002_200F	4B
	FLASH_CTRL	0x4002_2010 – 0x4002_2013	4B
	FLASH_ADD	0x4002_2014 – 0x4002_2017	4B
	Reserved	0x4002_2018 – 0x4002_201B	4B
	FLASH_OB	0x4002_201C – 0x4002_201F	4B
	FLASH_WRP	0x4002_2020 – 0x4002_2023	4B
	FLASH_ECC	0x4002_2024 – 0x4002_2027	4B
	Reserved	0x4002_2028 – 0x4002_2047	32B
	FLASH_USER	0x4002_2048 – 0x4002_204B	4B
	FLASH_START_ADD	0x4002_204C – 0x4002_204F	4B
	FLASH_VTOR	0x4002_2050 – 0x4002_2053	4B

The Flash memory is organized into 64-bit wide memory units, which can store codes and data constants.

Information is divided into three parts:

- The system memory area is used to store the bootloader in the system memory. The bootloader uses UART1 serial interface to program the Flash memory.
- System configuration area,contains basic information about the chip.
- The option byte area.

The writing to the main memory and information block is managed by embedded Flash programming/erasing controller.

There are two ways to protect Flash memory from illegal access (read, write and erase):

- Page write protection (WRP)
- Readout protection (RDP)

The DATA flash area only supports readout protection.

When the Flash memory write operation is executed, any read operation to the Flash memory will stall the bus, and the read operation can only be performed correctly after the write operation is completed. This means that code or data fetches cannot be made while a program/erase operation is ongoing.

When performing Flash programming operations(write or erase), the internal RC oscillator (HSI) must be turned on .

Note: In the low power consumption mode, all Flash memory operations are suspended.

2.2.1.2 **Read and write operation**

The Flash operation only supports 64-bit operation, and the Flash should be erased before the write operation, and the minimum block size for erasing is one page 0.5KB. Write operation is divided into erasing and programming phases.

When reading Flash, the number of waiting cycles for reading can be configured by the register. When using, it needs to be calculated in combination with the clock frequency of SYSCLK interface. For example, when SYSCLK <= 24MHz, the minimum number of waiting periods is 0; When 24MHz< SYSCLK <= 48MHz, the minimum number of waiting

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

periods is 1; When 48MHz< SYSCLK <=64MHz, the minimum number of waiting periods is 2.

Note: Whether number of wait periods is not zero, enable prefetch buffer can improve overall efficiency.

2.2.1.3 Unlock Flash

After reset, the Flash module is protected and cannot be written into the FLASH_CTRL register to prevent accidental operation of Flash memory due to electrical disturbances and other reasons. By writing a specific sequence of key values into the FLASH_KEY register, you can unlock the FLASH_CTRL register. The specific sequence is: Firstly, writing KEY1 = 0x45670123 in the FLASH_KEY register. Secondly, writing the key value KEY2 = 0xCDEF89AB in the FLASH_KEY register.

If there is an error in sequence or key value, a bus error will be returned and the FLASH_CTRL register will be locked until the next reset.

Software can check the FLASH_CTRL.LOCK bit to confirm whether the Flash is unlocked. If normal locking is required, software can set the FLASH_CTRL.LOCK bit to 1. After that, the Flash can be unlocked by writing the correct key sequence to the FLASH_KEY register.

2.2.1.4 Erase and program

2.2.1.4.1 Erase of main memory area and data FLASH area

The main memory area can be erased page by page or whole. The data FLASH area only can be erased by page.

- **Page Erase**

  Page Erase process:

  – Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;

  – Set the FLASH_CTRL.PER bit to '1';

  – Select the page to be erased with the FLASH_ADD register;

  – Set the FLASH_CTRL.START bit to '1';

  – Wait for the FLASH_ STS.BUSY bit to change to '0';

  – Read out the content of the erased page and verify it.

- **Mass Erase**

  Mass Erase process:

  – Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;

  – Set the FLASH_CTRL.MER bit to '1';

  – Set the FLASH_CTRL.START bit to '1';

  – Wait for the FLASH_ STS.BUSY bit to change to '0';

  – Read out all pages and verify them.

2.2.1.4.2 Main memory area and data FLASH area programming

The main memory area and data FLASH area can be programmed with 64 bits at a time. When the FLASH_CTRL.PG bit is '1', writing two words in a Flash address will start programming once; Writing any half word or byte of data will result in a bus error; Writing any single word of data will result a program error. During the programming process (the FLASH_

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

STS.BUSY bit is '1'), any operation of reading or writing the Flash memory will cause the CPU to pause until the end of the Flash programming.

Main memory and data FLASH programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Set the FLASH_CTRL.PG bit to '1';
- Write the word to be programmed at the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

Note: When the FLASH_STS.BUSY bit is '1', you cannot write to any register.

2.2.1.4.3 **Option byte erase and programming**

The option byte area is programmed differently from the main memory block. The number of option bytes is limited to 14 bytes (4 bytes for write protection, 2 bytes for readout protection, 6 byte for configuration and 2 bytes for storing user data). After unlocking the Flash, you must write KEY1 and KEY2 respectively (refer to 2.2.1.3) to the FLASH_OPTKEY register, and then set the FLASH_CTRL.OPTWE bit to '1'. At this time, the option byte area can be programmed: set the FLASH_CTRL.OPTPG bit to '1' and then write a word to the specified address.

When programming the word in the option byte area, use the low byte in the half-word and automatically calculate the high byte (the high byte is the complement of the low byte), before starting the programming operation, this ensures that the option byte and its complement are always correct.

Option byte erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTER bit to '1';
- Set the FLASH_CTRL.START bit to '1';
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the erased option byte and verify it.

Option byte area programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other Flash operations in progress;
- Set the FLASH_CTRL.OPTWE bit to '1';
- Set the FLASH_CTRL.OPTPG bit to '1';
- Writing the word to be programmed to the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

2.2.1.5 **ECC function**

The Flash module supports the ECC functionality, enabling 1-bit error correction and 2-bit detection. ECC encoding and

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

decoding (error correction and error detection) are performed automatically by the hardware. If an error is detected, an error is set and an interrupt is generated.

2.2.1.6 Instruction prefetching

The Flash module supports instruction prefetch function with the prefetch buffer size of 16B. Through instruction prefetching, the instruction execution efficiency of CPU can be improved. The instruction prefetch function can be configured to be enabled or disabled through the register, and it is enabled by default.

2.2.1.7 Option byte

Option byte block is mainly used to configure read-write protection, boot mode configuration, software/hardware watchdog and reset options when the system is in PD or STOP mode, and bus address space is allocated to the option byte block for read-write access. They consist of 14 options bytes : 4 byte for write protection, 2 bytes for readout protection, 6 byte for configuration option, 2 bytes defined by user. The option byte block also contains the complement codes corresponding to these 14 option bytes. These complement codes need to be automatically calculated by hardware when the option bytes are written in the bus, and written into Flash together, and used for verification when the option bytes are read.

By default, the option byte block is always read-accessible and write-protected. To write (program/erase) the option byte block, first unlock the Flash, then unlock the option byte: write the correct key-value sequence (KEY1 = 0x45670123, KEY2 = 0xCDEF89AB) into the FLASH_OPTKEY, and then write operation to the option byte block will be allowed. If the sequence is wrong or the key value is wrong, a bus error will be returned and the option byte will be locked until the next reset. To lock the option byte normally, write '0' to the FLASH_CTRL.OPTWE bit by software, and then the option byte can be unlocked by writing the correct key value sequence in the FLASH_OPTKEY.

After each system reset, the option byte data is read out from the option byte block and stored it in the option byte register (FLASH_OB/FLASH_USER/FLASH_WRP) with read-only property. At the same time, the option byte complement data read out together will be used to verify whether the option byte data is correct. If it does not match, an option byte error flag (FLASH_OB.OBERR) will be generated. When an option byte error occurs, the corresponding option byte is forced to 0xFF. When the option byte and its complement are both 0xFF (the state after erasing), the above verification steps are skipped and verification is not required.

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

Table 2-4 Option Byte List

Address	[63:16] Reserved	[15:8] Corresponding complement code	[7:0] Option byte
0x1FFF_FC00	-	nRDP1	RDP1
0x1FFF_FC08	-	nUSER1	USER1
0x1FFF_FC10	-	nUSER2	USER2
0x1FFF_FC18	-	nUSER3	USER3
0x1FFF_FC20	-	nUSER4	USER4
0x1FFF_FC28	-	nUSER5	USER5
0x1FFF_FC30	-	nUSER6	USER6
0x1FFF_FC38	-	nData0	Data0
0x1FFF_FC40	-	nData1	Data1
0x1FFF_FC48	-	nWRP0	WRP0
0x1FFF_FC50	-	nWRP1	WRP1
0x1FFF_FC58	-	nWRP2	WRP2
0x1FFF_FC60	-	nWRP3	WRP3
0x1FFF_FC68	-	nRDP2	RDP2

- Readout protection L1 level option byte: RDP1
  - Protect the code stored in the Flash memory;
  - When the correct value is written, it is not allowed to read the Flash memory;
  - The result of whether RDP1 is turned on or not can be inquired through FLASH_OB[1];
- User configuration option 1: USER1
  - USER1[7]: Reserved
  - USER1[6]: BOOT0_CFG configuration option, which can be queried by FLASH_OB[8]
  - USER1[5]: nSWBOOT0_SEL configuration option, which can be queried by FLASH_OB[7]
  - USER1[4]: nBOOT1 configuration option, which can be queried by FLASH_OB[6]
  - USER1[3]: nBOOT0 configuration option, which can be queried by FLASH_OB[5]
  - USER1[2]: nRST_PD configuration option, which can be queried through FLASH_OB[4]

    0: A reset occurs when PD mode is entered

    1: No reset occurs when entering PD mode
  - USER1[1]: nRST_STOP configuration option, which can be queried through FLASH_OB[3]

    0: A reset occurs when entering STOP mode

    1: No reset occurs when entering the STOP mode
  - USER1[0]: IWDG_SW configuration option, which can be queried by FLASH_OB[2]

    0: Hardware watchdog

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

1: Software watchdog

- User configuration option byte : USERx
  - USER2[3:0]: LVR power-on voltage control, which can be queried by FLASH_USER[3:0]
  - USER2[4]: LVR enable control, which can be queried by FLASH_USER[4]
  - USER2[5]: LVR reset enable control, which can be queried by FLASH_USER[5]
  - USER2[6]: LVR filter enable control, which can be queried by FLASH_USER[6]
  - USER2[7]: Reserved
  - USER3[7:0]: LVR filter counter control, which can be queried by FLASH_USER[15:8]
  - USER4[7:0]: Power-on delay reset control, which can be queried by FLASH_USER[23:16]
  - USER5[7:0]: FLASH boot start address, which can be queried by FLASH_START_ADD [7:0]
  - USER6[1:0]: Used to select the boot serial port pins, which can be queried by FLASH_OB [27:26]
- 2 bytes of user data: Datax
  - Data1 (stored in FLASH_OB[25:18]);
  - Data0 (stored in FLASH_OB [17:10]);
- Write protection option byte: WRP0 ~ 3, which can be inquired through the register FLASH _WRP [31:0]
  - WRP0: Write protection for pages 0 to 63, bit[0] corresponds to Page (0 to 7)..., bit[7] corresponds to Page (56~63);
  - WRP1: Write protection for pages 64~127, bit[0] corresponds to Page (64~71)..., bit[7] corresponds to Page (120~127);
  - WRP2: Write protection for pages 128~191, bit[0] corresponds to Page (128~135)..., bit[7] corresponds to Page (184~191);
  - WRP3: Write protection for pages 192~255, bit[0] corresponds to Page (192~199)..., bit[7] corresponds to Page (248~255);
- Readout protection L2 level option byte: RDP2
  - Add protection function on the basis of L1, refer to the detailed description of readout protection in section 2.2.1.9;
  - The result of whether RDP2 is turned on or not can be inquired through FLASH_OB [31];

2.2.1.8 **Write protection**

Write protection can be configured for all pages of the Flash main memory area (maximum 128KB), to prevent accidental write operations caused by programcrashes or electrical disturbances. The basic unit of write protection is as follows: for Page 0 to 255, every 8 pages is a basic protection unit. Write protection can be configured by setting WRP0 and WRP3 in the option byte block; After each configuration, a system reset is required for the configured value to be reloaded to take effect. If an attempt is made to program or erase a protected page, a protection error flag will be returned in the FLASH_STS.

The system information area contains the following blocks:

- The data flash block (8KB) in the system information area stores the user data and can be changed.

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Email：info@nationstech.com
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- The system memory block (4KB) in the system information area stores the boot program and cannot be changed.
- The system configuration block (3KB) in the system information area stores the basic information of the chip and cannot be changed.
- The option byte block (0.5KB) in the system information area stores the user-configurable option byte information. The write protection of the option byte block is achieved by writing 0 to the FLASH_CTRL.OPTWE bit by software, and after that, you can write the correct key value sequence to FLASH_OPTKEY to release the write protection of the option byte.

2.2.1.9 Readout protection

The user code in Flash can be protected against unauthorized reading by setting readout protection. Readout protection is set by configuring RDP bytes in the option byte block. Three different readout protection levels can be configured, as shown in the following Table

Table 2-5 Read Protection Configuration List

Read Protection Status	RDP1	nRDP1	nRDP2	RDP2
L0 level	0xA5	0x5A	RDP2! = 0xCC || nRDP2! = 0x33	
L2 level	0xXX	0xXX	0x33	0xCC
L1 level	Not the above two configurations			

- L0 level:
  - In unprotected state(RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33);
  - The main memory area, data flash area and option bytes can be read arbitrarily;
  - The main memory area, data flash area and options bytes can be programmed and erase, with configurable read/write protection.
- L1 level:
  - The corresponding ~ ((RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33)) | (RDP2 == 0xCC & nRDP2 == 0x33));
  - Only the read operation of the main memory area and data flash area from the user code is allowed, that is, the read operation of the main memory area is permitted only when the program is started from the main Flash memory in non debugging mode;
  - All main memory pages and data flash area can be programmed by code executed in main Flash memory (for functions such as IAP or data memory)
  - All main memory pages and data flash area are not allowed toperform write or erase operations in debug mode or after booting from internal SRAM (except for mass erase);
  - All functions of loading code into the embedded SRAM through JTAG/SWD remain effective, and they can be started from the embedded SRAM through JTAG/SWD, which can be used to remove readout protection;
  - When the read-protected option byte is rewritten to the unprotected L0 level, all the main memory area and data flash area will be automatically erased, and the process is as follows: (Erasing the option byte block will not result in automatic whole erasing operation, because the result of erasing is 0xFF, which is equivalent to remainingin the protection state of L1 level)

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- Write the correct key value sequence into FLASH_OPTKEY to unlock the option byte block;
- The bus initiates a command to erase the entire option byte area (Page erase);
- Bus write 0xA5 to readout protection option byte;
- Internally, automatically erase all main memory areas;
- Internally, automatically write 0xA5 to readout protection option byte;
- When the system is reset (such as software reset, etc.), the option byte block (including the new RDP value 0xA5) will be reloaded into the system, and the readout protection will be released;

- L2 level: Except that SRAM boot disabled, debug mode disabled, option byte write/page erase disabled and the protection level cannot be modified (irreversible), other features are the same as L1 level. The L2 level is realized by configuring another option byte, RDP2. No matter what the value of RDP1 is, as long as it satisfies (RDP2==0xCC & nRDP2==0x33), it is L2 level.

2.2.1.10 **Permission protection**

- Flash main memory area and data flash area permissions:
  - Under L0 level: the main memory area and flash data can be read; the write protection attributes for each page can be configured in the main memory for programming and page erasing;
  - Under L1/2 level:
    - When executed in SWD debug mode or after booting from internal SRAM, all Pages is not allowed (W/R/PE) operations;
    - All Pages can be programmed through the code executed in the main Flash memory area (implementing functions such as IAP or data memory);
    - All Pages can configure the write protection property of each Page;
    - When the L1 level is modifiedto the L0 level, all Flash main memory and data flash will be automatically erased;
- Flash option byte area permission:
  - Under the L0/L1 level:all accesses are allowed (W/R/PE);
  - Under L2 level: except for debug mode, all other modes allow read-only access to the Flash option byte area.
- Flash system memory area permissions:
  - Only the code executed in the system memory area is allowed to access (W/R/PE), the code executed in Flash and SRAM, or through the debug interface, is not allowed access to the Flash system memory area.
  - Under L1/L2 level: jumping to system memory to execute code from SRAM boot is not allowed access to the Flash system memory area (W/R/PE); in other cases, access to the Flash system memory area is allowed (W/R/PE).
- Flash system configuration area:
  - User information: reading the area is only allowed after booting or jumping to system memory.
  - ID information: this area can be read at Level 0, access is prohibited through SWD debug mode at L1/L2, and access is prohibited after booting from SRAM at L1, refer to Table 2-6 for details;

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Table 2-6 Flash Read-write-erase(1) Permission Control Table

Protect Level	Boot Mode	Main Flash				Changing A Protection Level
	Perform user / Access area	SWD	Main Flash	System Memory	SRAM	
L0 level	Flash main memory area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Change to L1 or L2 is allowed
	Data flash area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Prohibit	Read-Write-Erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Flash main memory area	Prohibit	Read-Write-Erase	Read-Write-Erase	Prohibit	Change to L0 or L2 is allowed. When changed to L0, the main memory area and data flash area are automatically erased.
	Data flash area	Prohibit	Read-Write-Erase	Read-Write-Erase	Prohibit	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	

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	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Flash main memory area	The SWD interface is disabled.	Read-write-erase	Read-write-erase	Prohibit	No modification is allowed.
	Data flash area		Read-write-erase	Read-write-erase	Prohibit	
	Flash main memory area mass erase		Allow	Allow	Allow	
	Flash option byte area		Read-only	Read-only	Read-only	
	Flash system memory area		Prohibit	Read-write-erase	Prohibit	
	SRAM (All)		Read and write	Read and write	Read and write	
protect level	Boot mode	SRAM				Changing a Protection Level
	Perform user / Access to areas	SWD	Main Flash	System Memory	SRAM	
L0 level	Flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	Change to L1 or L2 is allowed
	Data flash area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	

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	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Flash main memory area	Prohibit	Read-write-erase	Prohibit	Prohibit	Change to L0 or L2 is allowed. When changed to L0, the main memory area and data flash area are automatically erased.
	Data flash area	Prohibit	Read-write-erase	Prohibit	Prohibit	
	Flash main memory area mass erase	Allow	Allow	Prohibit	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Prohibit	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Prohibit	Prohibit	
	SRAM (All)	Read and write	Read and write	Prohibit	Read and write	
L2 level	Before 4KB of Flash main memory area	L2 protection level, cannot boot from SRAM				No modification is allowed. SWD is banned.
	After 4KB of Flash main memory area					
	Flash main memory area mass erase					
	Flash option byte area					
	Flash system memory area					
	SRAM (All)					

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protect level	Boot mode / Perform user Access to areas	System Memory				Changing a Protection Level
		SWD	Main Flash	System Memory	SRAM	
L0 level	Flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	Change to L1 or L2 is allowed
	Data flash area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Flash main memory area	Prohibit	Read-only	Read-only	Prohibit	Change to L0 or L2 is allowed. When changed to L0, the main memory area and data flash area are automatically erased.
	Data flash area	Prohibit	Read-write-erase	Read-write-erase	Prohibit	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2	Flash main		Read-	Read-write-	Read-write-	No modification

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level	memory area	The SWD interface is disabled.	write-erase	erase	erase	allowed
	Data flash area		Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase		Allow	Allow	Allow	
	Flash option byte area		Read-only	Read-only	Read-only	
	Flash system memory area		Prohibit	Read-write-erase	Prohibit	
	SRAM (All)		Read and write	Read and write	Read and write	

Note: (1)Erase here refers to Flash page erase.

2.2.2 SRAM

SRAM is mainly used for operation to store variables and data or stacks during program execution.The maximum capacity is 16KB.

SRAM supports read-write access of byte, half-word and word.

SRAM supports code execution and can run programs at full speed in SRAM. The maximum address range of SRAM is 0x2000 0000 to 0x2000 3FFF.

In PD mode, data cannot be retained in SRAM; in other operating modes (RUN/SLEEP/STOP), data can be retained normally.

The main features are as follows:

- The maximum capacity is 16KB in total.
- Supports byte/half word/word reading and writing.
- CPU/DMA can be accessed.
- The CPU BUS can be remapped to SRAM to run the program at full speed.

2.2.3 FLASH Register Description

All register operations must be performed in words (32 bits).

2.2.3.1 Flash register overview

Table 2-7 Flash Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	FLASH_AC	Reserved																										PRFTBFS	PRFTBFE	Reserved	LATENCY		

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	Reset Value																													1	1		0	0	0
004h	FLASH_KEY	FKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	FLASH_ OPTKEY	OPTKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	FLASH_STS	Reserved																												ECCERR	Reserved	EOP	WRPERR	Reserved	PGERR	Reserved	BUSY
	Reset Value																													0		0	0		0		0
010h	FLASH_CTRL	Reserved																							ECCERRITE	EOPITE	Reserved	ERRITE	OPTWE	Reserved	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
	Reset Value																								0	0		0	0		1	0	0	0		0	0	0
014h	FLASH_ADD	FADD																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	Reserved																																
01Ch	FLASH_OB	RDPRT2	Reserved							BOOT_SEL	Data1														Data0							Not Used	BOOT0_CFG	nSWBOOT0	nBOOT1	nBOOT0	nRST_PD	nRST_STOP	WDG_SW	RDPRT1	OBERR
	Reset Value	0								1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
020h	FLASH_WRP	WRPT																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
024h	FLASH_ECC	Reserved																												ECCLW								
	Reset Value																													0	0	0	0	0	0	0	0	
028h~047h	Reserved																																
048h	FLASH_USER	Reserved																															
	Reset Value																																
04Ch	FLASH_START _ADD	Reserved																												START_ADD								
	Reset Value																													1	1	1	1	1	1	1	1	
050h	FLASH_VTOR	VTOR_EN	VTOR_VALUE																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2.2.3.2 **Flash control and status registers**

For abbreviations related to register descriptions, please refer to section 1.1.

2.2.3.2.1 **Flash access control register (FLASH_AC)**

Address offset: 0x00

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Reset value: 0x0000 0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										PRFTBFS	PRFTBFE	Reserved		LATENCY	
										rw	rw			rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained.
5	PRFTBFS	Pre-fetch buffer status This bit indicates the state of the pre-fetch buffer 0: The pre-fetch buffer is disabled. 1: The pre-fetch buffer is enabled.
4	PRFTBFE	The pre-fetch buffer is enabled 0: Disables the pre-fetch buffer. 1: Enables the pre-fetch buffer.
3:2	Reserved	Reserved,the reset value must be maintained
1:0	LATENCY	Time delay These bits represent the ratio of the SYSCLK (system clock) cycle to the flash access time 00: Zero periodic delay, when 0 < SYSCLK ≤ 24MHz 01: A periodic delay, when 24MHz < SYSCLK ≤ 48MHz 10: Two periodic delay, when 48MHz < SYSCLK ≤ 64MHz 11: Reserved

2.2.3.2.2 Flash key register (FLASH_KEY)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FKEY[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FKEY[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:0	FKEY	Used to unlock the FLASH_CTRL.LOCK bit.

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2.2.3.2.3 Flash OPTKEY register (FLASH_OPTKEY)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPTKEY [31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTKEY [15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit field	Name	Description
31:0	OPTKEY	Used to unlock the FLASH_CTRL.OPTWE bit.

2.2.3.2.4 Flash status register (FLASH_STS)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ECCERR	Reserved	EOP	WRPERR	Reserved	PGERR	Reserved	BUSY
								rc_w1		rc_w1	rc_w1		rc_w1		r

Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7	ECCERR	ECC error Error reading Flash, hardware set this to '1', write '1' to clear this state.
6	Reserved	Reserved,the reset value must be maintained
5	EOP	End of the operation When the Flash operation (programming/erasing) is complete, the hardware sets this to '1' and writing '1' clears this state. *Note: EOP status is set for each successful programming or erasure.*
4	WRPERR	Write protection error When attempting to program a write protected Flash address, hardware sets this to '1' and writing '1' clears this state.
3	Reserved	Reserved,the reset value must be maintained
2	PGERR	Programming errors

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Email：info@nationstech.com
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Bit Field	Name	Description
		When trying to program to an address whose content is not '0xFFFF_FFFF', the hardware sets this to '1'. Writing '1' clears this state. *Note: Before programming, the FLASH_CTRL.START bit must be cleared.*
1	Reserved	Reserved,the reset value must be maintained
0	BUSY	Busy This bit indicates that a Flash operation is in progress.This bit is set to '1' at the start of the Flash operation; This bit is cleared to '0' at the end of the operation or when an error occurs.

2.2.3.2.5 Flash control register (FLASH_CTRL)

Address offset: 0x10

Reset value: 0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		ECCERRITE	EOPITE	Reserved	ERRITE	OPTWE	Reserved	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
		rw	rw		rw	rw		rw	rw	rw	rw		rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved,the reset value must be maintained
13	ECCERRITE	ECC error interrupt This bit allows interrupts to occur when the FLASH_STS.ECCERR bit changes to '1'. 0: Forbid interruption. 1: Interrupts are allowed.
12	EOPITE	Allow operation completion interrupt. This bit allows an interrupt to be generated when the FLASH_STS.EOP bit becomes '1'. 0: Forbid interruption. 1: Interrupts are allowed.
11	Reserved	Reserved,the reset value must be maintained
10	ERRITE	Allow error status to be interrupted This bit allows interrupts in the event of Flash errors (when FLASH_STS.PGERR/ FLASH_STS.WRPERR is set to '1'). 0: Forbid interruption. 1: Interrupts are allowed.
9	OPTWE	Allows option bytes to be written When the bit is' 1 ', programmatic manipulation of the option byte is allowed. When the correct key sequence is written to the FLASH_OPTKEY register, the

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		bit is set to '1'. Software can clear this bit.
8	Reserved	Reserved,the reset value must be maintained
7	LOCK	Lock This bit can only be written as '1'.When the bit is' 1 ', Flash and FLASH_CTRL are locked. Hardware clears this bit to '0' after detecting a correct unlock sequence. After an unsuccessful unlock operation, this bit cannot be changed until the next system reset.
6	START	Start An erase operation is triggered when the bit is' 1 '.This bit can only be set by software to '1' and cleared to '0' when FLASH_STS.BUSY changes to '1'.
5	OPTER	Erase option bytes 0: Disable option bytes erase mode; 1: Enable option bytes erase mode.
4	OPTPG	Program option bytes 0: Disable option bytes program mode; 1: Enable option bytes program mode.
3	Reserved	Reserved,the reset value must be maintained
2	MER	Mass erase 0: Disable mass erase mode; 1: Enable mass erase mode.
1	PER	Page erase 0: Disable mass erase mode; 1: Enable mass erase mode.
0	PG	Program 0: Disable Program mode; 1: Enable Program mode.

Note: Please refer to Section 2.2.1.4 for programming and erasing.

2.2.3.2.6 **Flash address register (FLASH_ADD)**

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FADD[31:16]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FADD[15:0]															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

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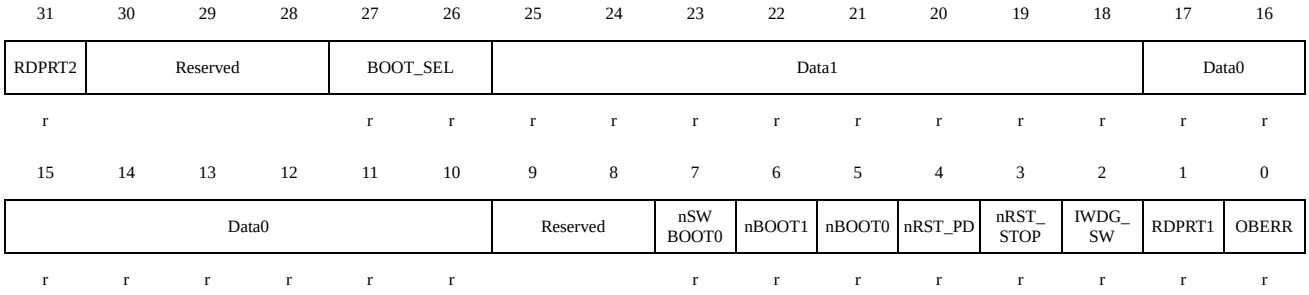
Bit Field	Name	Description
31:0	FADD	Flash memory address Select the address to program when programming and the page to erase when erasing. *Note: When the FLASH_STS.BUSY bit is '1', this register cannot be written.*

2.2.3.2.7 Flash option byte register (FLASH_OB)

Address offset: 0x1C

Reset value: 0x0FFF FFFC



Bit Field	Name	Description
31	RDPRT2	Readout protection level L2 0: Readout protection L2 is disabled. 1: Readout protection L2 is enabled. *Note: This bit is read-only.*
30:28	Reserved	Reserved,the reset value must be maintained
27:26	BOOT_SEL	BOOT serial communication pin selection 11b: PA9, PA10 (default) 00b: PB10, PB11 01b: PD10, PD11 10b: PA2, PA3
25:18	Data1[7:0]	Data1 *Note: This bit is read-only.*
17:10	Data0[7:0]	Data0 *Note: This bit is read-only.*
9	Reserved	Reserved,the reset value must be maintained
8	BOOT0_CFG	BOOT0 power-on default state 0: High level default, pulled low effective 1: Low level default, pulled high effective
7	nSWBOOT0	For the usage rules, see 2.1.3.2 Boot configuration.
6	nBOOT1	For the usage rules, see 2.1.3.2 Boot configuration.
5	nBOOT0	For the usage rules, see 2.1.3.2 Boot configuration.
4	nRST_PD	The Power Down mode is used to reset the configuration 0: A reset occurs immediately after the system enters the Power Down mode. Even if the system enters the Power Down mode, the system will be reset instead

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Bit Field	Name	Description
		of entering the Power Down mode. 1: The system does not reset after entering the Power Down mode. *Note: This bit is read-only.*
3	nRST_STOP	Enter the STOP mode to reset the configuration 0: A reset occurs immediately after entering the STOP mode. Even if the process of entering the STOP mode is executed, the system will be reset instead of entering the STOP mode. 1: No reset is generated after the STOP mode is entered. *Note: This bit is read-only.*
2	IWDG_SW	Watchdog Settings 0: Hardware watchdog. 1: Software watchdog. *Note: This bit is read-only.*
1	RDPRT1	Readout protection level L1 0: The L1 level of readout protection is disabled. 1: L1 readout protection is enabled. *Note: This bit is read-only.*
0	OBERR	Option byte error When this bit is '1', the option byte does not match its inverse. *Note: This bit is read-only.*

2.2.3.2.8 Flash write protection register (FLASH_WRP)

Address offset: 0x20

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRPT[31:16]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRPT[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:0	WRPT	Write protection This register contains the write protection option byte loaded by option byte area. 0: Write protection takes effect. 1: Write protection is invalid. *Note: These bits are read-only.*

2.2.3.2.9 Flash ECC register (FLASH_ECC)

Address offset: 0x24

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ECCLW							
								r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	ECCLW	After writing two words to a Flash address, the corresponding lower 8-bit ECC value.

2.2.3.2.10 **Flash USER register (FLASH_USER)**

Address offset: 0x48

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								POR_DELAY[7:0]							
								r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVRCNT[7:0]								Reserved	LVR FILEN	LVRRST	LVREN	LVRLS[3:0]			
r	r	r	r	r	r	r	r		r	r	r	r	r	r	r

Bit Field	Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
23:16	POR_DELAY	After triggering POR, a delay time for CPU reset. After the system initial power-up is completed, the system reset delay time of Cortex®-M0 can be configured through this bit to control the reset delay time of the core. 0x00: maximum delay time. … 0xFF: no delay. Delay time = $(1/f_{LSI}) \times (0xFF - POR_DELAY)$
15:8	LVRCNT	LVR filter control count value. 0x00: maximum filtering width ... 0xFF: no filtering Filtering width = $(1/f_{LSI}) \times (0xFF - LVRCNT)$

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Email：info@nationstech.com
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Bit Field	Name	Description
7	Reserved	Reserved,the reset value must be maintained
6	LVRFILEN	LVR filter enable. 0: LVR filter enabled. 1: LVR filter disabled.
5	LVRRST	LVR reset enable control. 0: LVR reset enabled. 1: LVR reset disabled.
4	LVREN	LVR enablement. 0: LVR enabled. 1: LVR disabled.
3:0	LVRLS	LVR voltage level selection. Value = 0x0F - LVRLS

Value	Voltage
0000	Reserved
0001	2.0v
0010	2.2v
0011	2.4v
0100	2.6v
0101	2.8v
0110	3.0v
0111	3.2v
1000	3.4v
1001	3.6v
1010	3.8v
1011	4.0v
1100	4.2v
1101	4.4v
1110	4.6v
1111	4.8v

2.2.3.2.11 **Flash boot start address register (FLASH_START_ADD)**

Address offset: 0x4C

Reset value: 0x0000 00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								START_ADD							
								r	r	r	r	r	r	r	r

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	START_ADD	FLASH boot start address (value corresponds to 1 page, decreasing) 0xFF: 0x08000000 (default) 0xFE: 0x08000200 0xFD: 0x08000400 … 0x01: 0x0801FC00 0x00: 0x0801FE00

2.2.3.2.12 **Flash VTOR register (FLASH_VTOR)**

Address offset: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VTOR_EN	VTOR_VALUE[30:16]														
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTOR_VALUE[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31	VTOR_EN	Interrupt vector remapping enable. 1: enable 0: disable
30:0	VTOR_VALUE	Used for interrupt vector remapping, storing the base address of the interrupt vector table. These bits are valid when VTOR_EN = 1. Interrupt address = VTOR_VALUE + offset address. *Note: This function is only valid when the offset address is less than 0x100.*

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

3 Power Control (PWR)

3.1 General Description

The PWR is power management unit to control status of different modules in different power modes. Its major function is to control MCU to enter different power modes and wakeup when events or interrupts happen. MCU supports the following modes: RUN, SLEEP, STOP and PD (Power Down) . PWR controls voltage regulator, Clock sources, Resets and Flash/SRAM/GPIO status in different power modes.

3.1.1 Power Supply

MCU has an external V_{DD} supply. Embedded voltage regulator is used to supply the internal 1.5V digital power supplies. Voltage regulator has two modes, normal mode and low power mode.

- V_{DD}: 2.0V~5.5V, which mainly provides power input for MR, IO and clock reset system.
- V_{DDA}: 2.0V~5.5V, which mainly provides power for most analog peripherals. For details, please refer to the electrical characteristics section of the relevant data sheet.
- VDDA and VSSA must be connected to VDD and VSS respectively.

Voltage regulator operates in several different modes, depending on the application:

- RUN mode: The voltage regulator provides power in normal power mode.
- SLEEP mode: The voltage regulator provides power in normal power mode.
- STOP mode: The voltage regulator provides power in low power mode and the output voltage can be configured to 1.5V or 1.2V by software.
- PD mode: The voltage regulator is turned off.

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Email：info@nationstech.com
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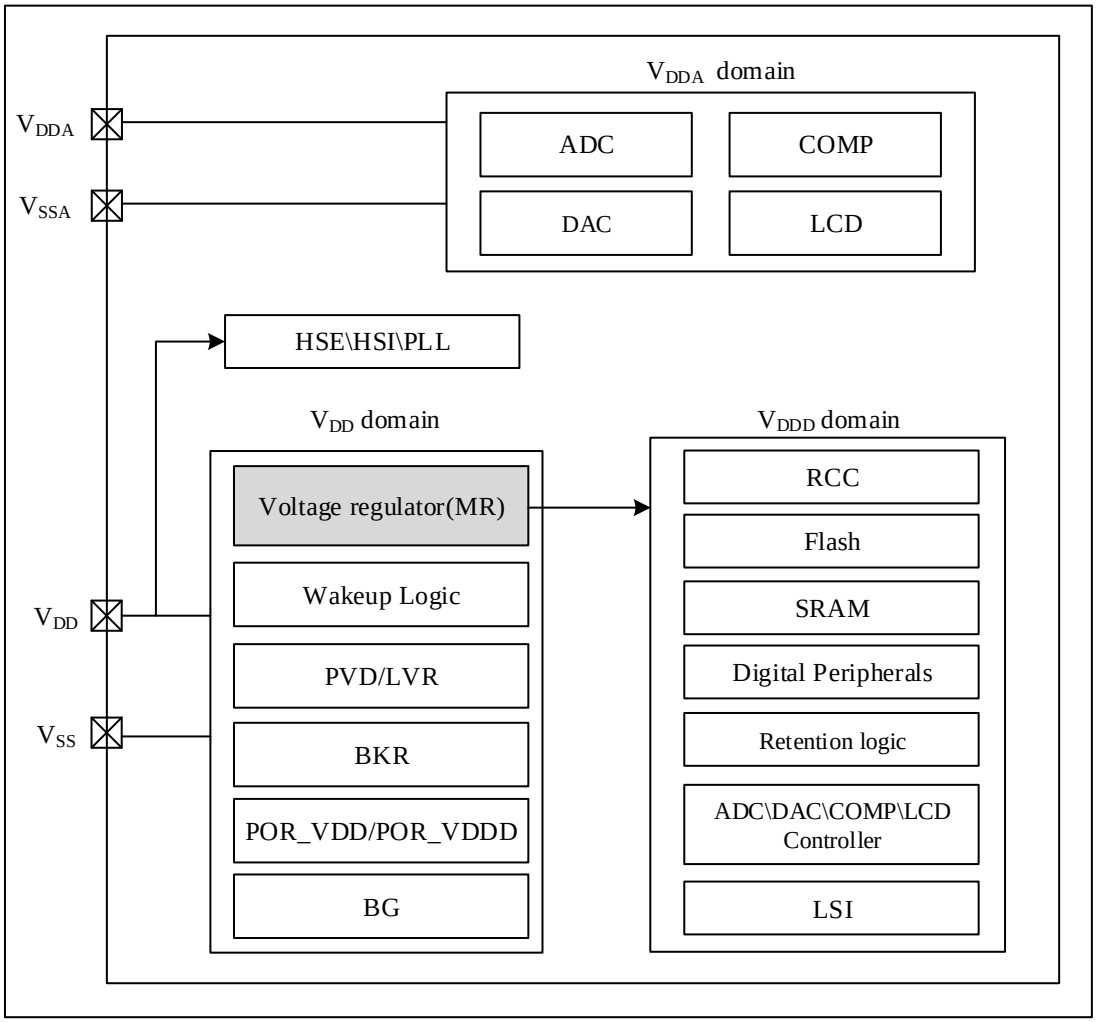
Nanshan District, Shenzhen, 518057, P.R.China

Figure 3-1 Power Supply Block Diagram



3.1.2 Power Supply Supervisor

3.1.2.1 Power on reset (POR) and power down reset (PDR)

Power on reset (POR) and power down reset (PDR) circuits are integrated inside the chip. When VDD/VDDA is below the specified limit voltage VPOR/VPDR, the system remains in a reset state without an external reset circuit. Refer to the electrical characteristics section of the data sheet for details on power-on and power-off resets.

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Email：info@nationstech.com
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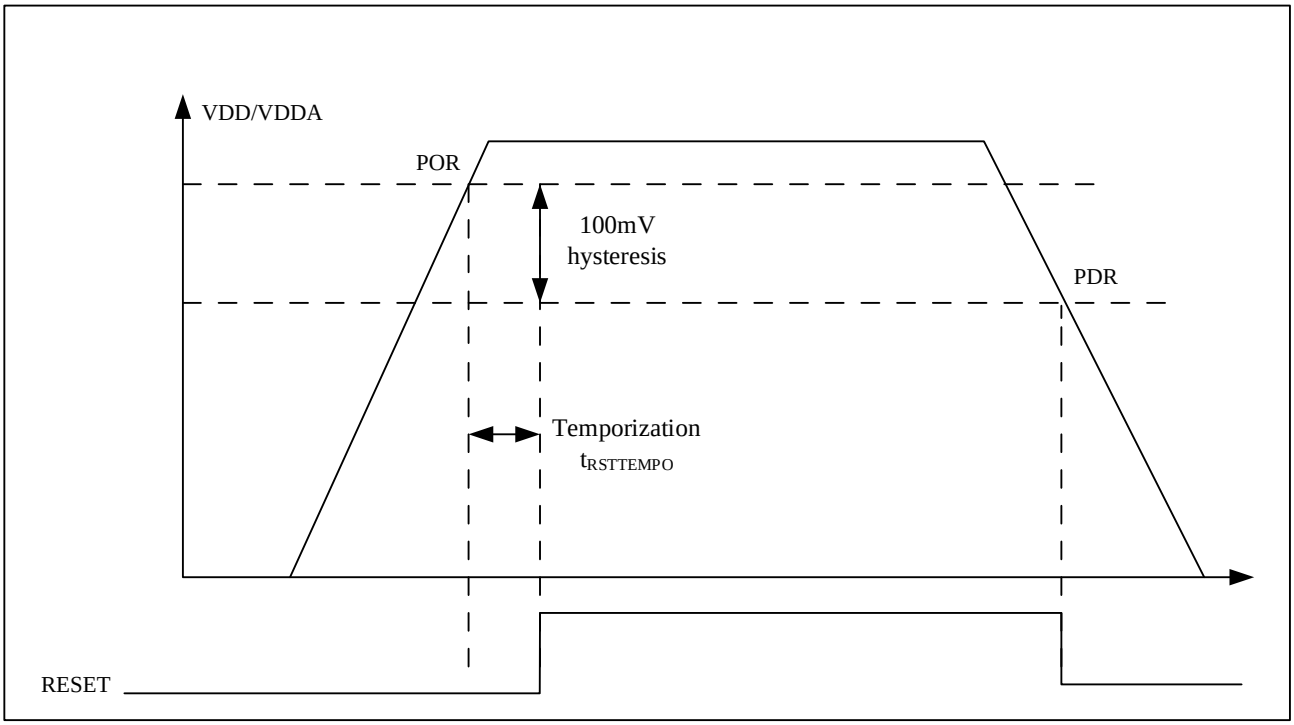
Figure 3-2 Power on Reset/Power down Reset Waveform



3.1.2.2 Programmable voltage detector (PVD)

The PVD monitors the power supply by comparing the V_{DD} voltage with the relevant bits in the power control register (PWR_CTRL). PWR_CTRL.PLS select the threshold of the monitoring voltage. Enable PVD by setting the PWR_CTRL.PVDEN.

The PWR_CTRLSTS.PVDO flag is used to indicate whether the V_{DD} is above/below the PVD voltage threshold. This event is connected internally to EXTI line16 and produces an interrupt if the interrupt is enabled in the external interrupt register. A PVD break occurs when the V_{DD} drops below the PVD threshold and/or when the V_{DD} rises above the PVD threshold, according to the rise/fall edge trigger setting of EXTI line 16. For example, this feature can be used to perform emergency shutdown tasks.

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Email：info@nationstech.com
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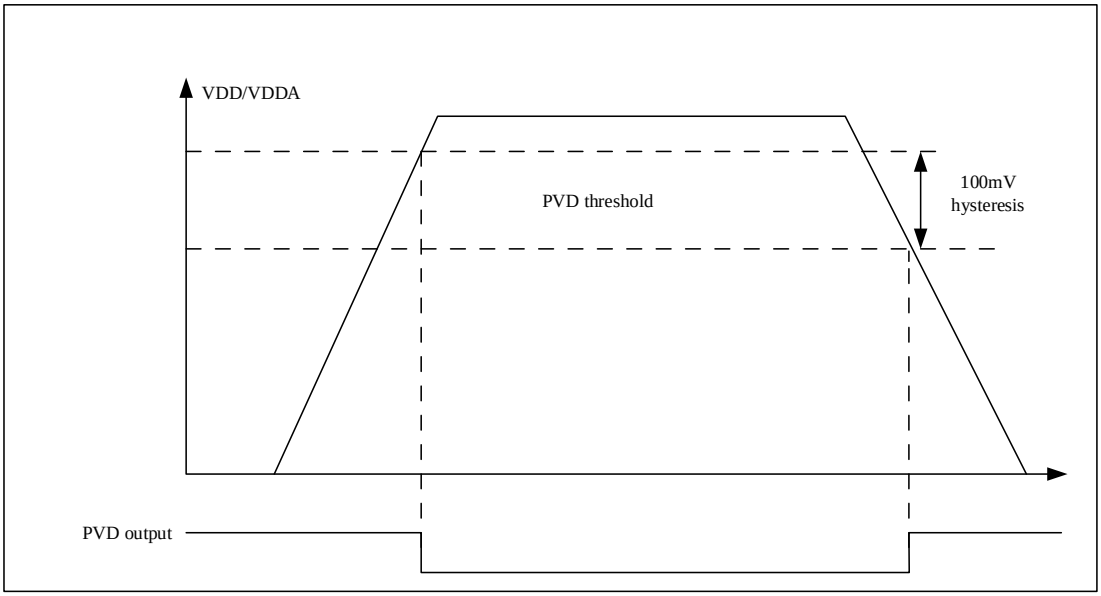
Figure 3-3 PVD Threshold Diagram



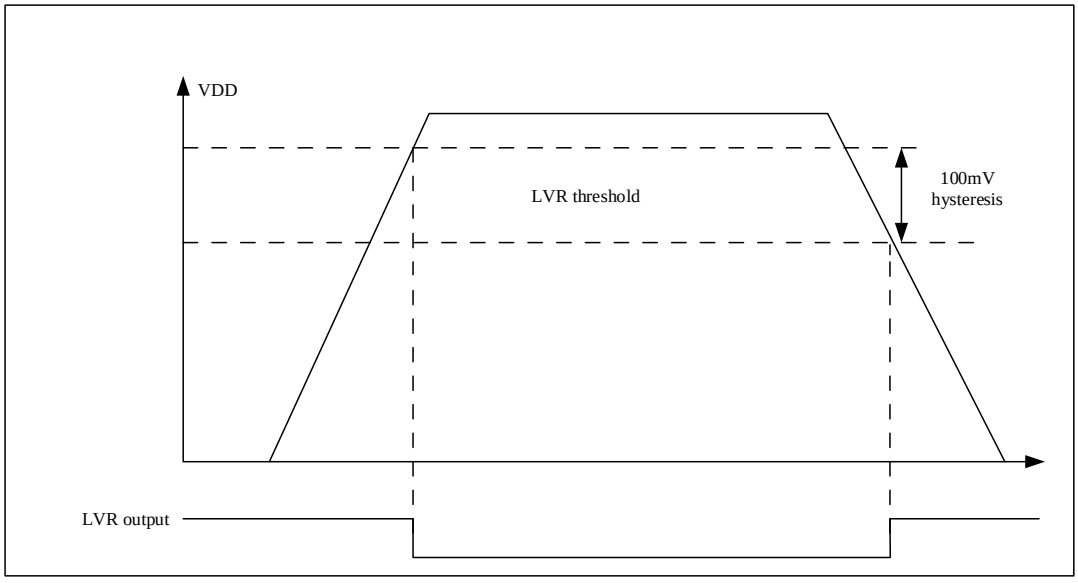
3.1.2.3 Low voltage reset (LVR)

LVR is used to detect V_{DD} voltage level. The threshold of LVR is controlled by PWR_CTRL2.LVRLS [3:0]. LVR can be enabled/disabled by PWR_CTRL2.LVREN bit.

The PWR_CTRL2.LVRO flag is used to indicate whether V_{DD} is higher or lower than LVR threshold. This event will trigger a system reset.

Note: PWR_CTRL2.LVRKEY needs to be written as A5 in order to properly read and write PWR_CTRL2[15:0] register, otherwise it defaults to the option byte configuration value.

Figure 3-4 LVR Threshold Diagram



3.2 Power Modes

The MCU has four power modes: RUN, SLEEP, STOP and PD. Different mode has different performance and power

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

consumption. A summary of MCU power modes is shown below.

Table 3-1 Power Modes

Mode	Condition	Enter	Exit
RUN	CPU is running all peripherals are configurable.	Power up, system reset, or wakeup from other power modes.	Enter SLEEP, STOPor PD mode.
SLEEP	CPU enters sleep mode all peripherals are configurable, regulator is running in normal mode;	WFI/WFE	Any interrupts wakeup event.
STOP	CPU enters deep SLEEP, peripherals clock are disabled. Voltage regulator runs in LP mode. Flash enters deep standby mode. HSE/HSI/PLL are disabled. LSI are configurable. SRAM/All registers are retained All IO are retained . After waking up, HSI is enabled, and the code continues to execute from the stopped point.	WFI/WFE: 1）SCB_SCR.SLEEPDEEP = 1, no pending interrupts/events. 2）PWR_CTRL.PDSTP = 0	Any interrupts wakeup event through EXTI, NRST, IWDG.
PD	Voltage regulator is OFF, all clocks are OFF, most IO output High-Z.	WFI/WFE： 1）SCB_SCR.SLEEPDEEP = 1, no pending interrupt/event. 2）PWR_CTRL.PDSTP = 1	WKUP0/1 rising or falling edge, NRST reset.

Note: In STOP mode, after wakeup, the code can resume and continue from stopped location.

The operating enabled status of different modules in different power consumption modes are shown in the following table:

Table 3-2 Peripheral Running Status

Main Blocks	Run/Active	Sleep	Stop mode		Power down mode	
			Status	Wakeup capability	Status	Wakeup capability
Cortex-M0	Y	-	-	-	-	-
FLASH	O	O	O	-	-	-
SRAM	Y	Y	Y	-	-	-
POR/PDR	Y	Y	Y	Y	-	-

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Email：info@nationstech.com
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LVR	O	O	O	O	-	-
PVD	O	O	O	O	-	-
DMA	O	O	-	-	-	-
UART	O	O	-	-	-	-
I2C	O	O	-	-	-	-
SPI	O	O	-	-	-	-
LED	O	O	-	-	-	-
AD Timer	O	O	-	-	-	-
GP Timer	O	O	-	-	-	-
BS Timer	O	O	O	O	-	-
HSE	O	O	-	-	-	-
HSI	O	O	-	-	-	-
LSI	O	O	O	-	-	-
PLL	O	O	-	-	-	-
IWDG	O	O	O	O	-	-
WWDG	O	O	-	-	-	-
RTC	O	O	O	O	-	-
CAN	O	O	-	-	-	-
SAC	O	O	-	-	-	-
ADC	O	O	-	-	-	-
Temperature Sensor	O	O	-	-	-	-
DAC	O	O	-	-	-	-
COMP	O	O	-	-	-	-
LCD	O	O	-	-	-	-
SysTick	O	O	-	-	-	-
CRC	O	O	-	-	-	-
GPIOs	O	O	O	O	-	2 pins

Notes:

(1) Y: Yes (Enable), O: Optional (Disabled by default, Enabled by software), -: Not available.

(2) The pins that can wake up from the PD are PA0 (WKUP0), PA1 (WKUP1), and NRST.

3.2.1 SLEEP Mode

The CPU stops, all peripherals including peripherals around the Cortex®-M0 core (such as NVIC, SysTick, etc.) can run and wake up the CPU when an interrupt or event occurs.

3.2.1.1 Entering SLEEP mode

Enter SLEEP mode by executing WFI(Wait For Interrupt) or WFE(Wait For Event) instruction with SCB_SCR.SLEEPDEEP = 0. Depending on the SCB_SCR.SLEEPONEXIT, there are two options for SLEEP mode entry:

- SLEEP-NOW: If SCB_SCR.SLEEPONEXIT = 0, the WFI or WFE instruction is executed immediately, and the system enters sleep mode immediately.
- SLEEP-ON-EXIT: If SCB_SCR.SLEEPONEXIT = 1, the system immediately enters sleep mode when exiting from the lowest priority ISR.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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3.2.1.2 Exiting SLEEP mode

If the WFI instruction is used to enter the SLEEP mode, any NVIC interrupts can wake up the device from the SLEEP mode.

If the WFE instruction is used to enter the SLEEP mode, MCU will exit the SLEEP mode immediately when the event occurs. Wake-up events can be generated in the following ways:

- Enable an interrupt in the peripheral control register instead of NVIC, and enable the SCB_SCR.SEVONPEND. When MCU resumes from WFE, the peripheral interrupt pending bit and the peripheral NVIC interrupt channel suspend bit (in NVIC interrupt clear pending register) must be cleared.
- Configure an external or internal EXTI event mode. When the MCU wakes up, it is not necessary to clear the peripheral interrupt pending bit and the peripheral NVIC interrupt channel pending bit (in the NVIC interrupt clear pending register) because the pending bit corresponding to the event line is not set. This mode provides the shortest wake-up time because there is no time spent on interrupt entry or exit.

3.2.2 STOP Mode

STOP mode is based on the Cortex®-M0 deep sleep mode combined with peripheral clock gating. The voltage regulator operates in low power mode. The output voltage can be configured as 1.5V/1.2V. The HSE/HSI/PLL are disabled. The LSI can be configured to enable. All GPIO states, SRAM and all registers are retained. Flash is in deep sleep mode. After waking up, the HSI is turned on, and the code starts from where it hangs.

3.2.2.1 Entering STOP mode

To enter the STOP mode, user needs to set SCB_SCR.SLEEPDEEP = 1 and PWR_CTRL.PDSTP = 0.

It is also possible to configure the voltage regulator low-power mode output voltage to achieve lower current consumption. In STOP mode, the voltage regulator output voltage defaults to 1.5V, and the Power-Down Reset (PDR) trigger voltage is 1.2V. When PWR_CTRL5.STPMRSEL[1:0] = '01', the regulator output voltage is 1.5V, and PWR_CTRL.PDRS[1:0] must be configured as '11' (PDR trigger voltage 1.2V). when PWR_CTRL5.STPMRSEL[1:0] = '11', the regulator output voltage is 1.2V, and PWR_CTRL.PDRS[1:0] must be configured as '10' (PDR trigger voltage 1.0V).

If a Flash operation is in progress, entering STOP mode will be delayed until the memory access is completed.

If the access to the APB area is in progress, entering the STOP mode will be delayed until the APB access is completed.

In STOP mode, the following peripherals are available:

- Independent Watchdog (IWDG): Once enabled, it will keep counting until a reset is generated.
- RTC: It can be enable by RCC_LSCTRL.RTCEN.
- TIM6/PVD peripherals can wake up.
- Internal RC oscillator (LSI RC): It can be turned on by RCC_LSCTRL.LSIEN.

ADC should be disabled when entering STOP mode to avoid unnecessary power consumption.

Note: If the application needs to disable the external clock before entering the stop mode, it must first switch the system clock to HSI and then deassert RCC_CTRL.HSEEN bit. If RCC_CTRL.HSEEN bit remains asserted and the external clock (external oscillator) is removed when entering the stop mode, the clock safety system (CSS) function must be enabled to detect any external oscillator failure.

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3.2.2.2 Exiting STOP mode

When an interrupt or wake-up event wakes up STOP mode, the HSI RC oscillator is selected as the system clock, codes resumed from suspended location. Since the voltage regulator is in low-power mode in STOP mode, it consumes more startup time. In addition, users can configure PWR_CTRL4.FLASHWKUP = 1 before entering STOP to shorten the wake-up time of Flash.

3.2.3 PD Mode

PD (Power Down) mode is based on Cortex®-M0 deep sleep mode, which can achieve lower power consumption. In this mode, the CPU, all peripherals, voltage regulator, HSE/HSI/PLL/LSI clock sources and all digital power supplies are turned off. Except for NRST/PA0/PA2, most IO ports output High-Z.

3.2.3.1 Entering PD mode

To enter the PD mode, user needs to set SCB_SCR.SLEEPDEEP = 1 and PWR_CTRL.PDSTP = 1.

If a Flash operation is in progress, entering STOP mode will be delayed until the memory access is completed.

If the access to the APB area is in progress, entering the STOP mode will be delayed until the APB access is completed.

3.2.3.2 Exiting PD mode

The MCU exits PD mode when external reset (NRST pin), rising/falling edge of WKUP pin event occurs. And all registers will be reset after waking up.

After waking up from PD mode, code execution is same as power on (boot pin is detected, reset vector is read, etc.).

3.3 Debug Support

By default, if the application set the MCU to SLEEP, STOP or PD mode while using the debug features, the debug connection will be lost. This is due to the Cortex®-M0 core losing its clock.

However, by setting some configuration bits in the DBG_CTRL register, it is possible to debug the software even when using in STOP and PD modes. If these register bits are configured, the voltage regulator and HSI will not be disabled or turned off.

3.3.1 Low Power Mode Debug Support

When debugging in low-power modes, it is essential to ensure that the FCLK of the core is turned on to provide the necessary clock for core debugging. User can debug the MCU in low power modes according to specific operations (Need to guarantee the output of FCLK in low power mode). For specific operations and features, please refer to the description of DBG_CTRL.PD and DBG_CTRL.STOP in Chapter 3.4.9.

3.3.2 Peripheral Debug Support

In addition to supporting debug in low power mode, it also supports some peripherals to stop operating in debug state (TIM1, TIM2, TIM3, TIM4, TIM5, TIM6, I2C1, I2C2, CAN, IWDG, WWDG, etc). For specific operations and features, please refer to the description of the other bit fields of the DBG_CTRL register in Chapter 3.4.9.

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Email：info@nationstech.com
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3.4 PWR Registers

3.4.1 PWR Register Overview

Table 3-3 PWR Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	PWR_CTRL	Reserved						PVDITEN	PVDFILEN	PVDCNT[7:0]								Reserved				NRSTPOL	PDRS[1:0]		PLS[3:0]				PVDEN	CLRDBGPDF	CLRWKUPF	PDSTP	IWDGRSTEN
	Reset Value							0	0	0	0	0	0	0	0	0	0					0	1	1	0	0	0	1	0	0	0	0	1
004h	PWR_CTRLSTS	Reserved																				WKUPPOL	Reserved	WKUP1EN	WKUP0EN	Reserved					PVDO	DBGPDF	WKUPF
	Reset Value																					1		0	0						0	0	0
008h	PWR_CTRL2	LVRKEY								Reserved								LVRO	Reserved			LVRLS	LVREN	LVRRSTEN	LVRFILEN	LVRCNT							
	Reset Value	0	0	0	0	0	0	0	0									0				1	0	0	0	0	0	0	0	0	0	0	0
014h	PWR_CTRL3	Reserved				NRSTFILEN	NRSTCNT											Reserved						PDRSELEN	Reserved	LSIEN	Reserved						
	Reset Value					0	0	0	0	0	0	0	0	0	0	0	0							1		0							
020h	PWR_CTRL4	Reserved																													RUNF	STBFLH	FLHWKUP
	Reset Value																														0	0	0
024h	PWR_CTRL5	Reserved																												STPMRSEL[1:0]		Reserved	
	Reset Value																													0	1		
028h	PWR_CTRL6	Reserved																												STPMREN[1:0]		Reserved	
	Reset Value																													0	0		
030h	DBG_CTRL	Reserved								TIM2STP	TIM4STP	TIM6STP	TIM5STP	I2C2TIMOUT	I2C1TIMOUT	CANSTP	Reserved		TIM3STP	Reserved		TIM1STP	WWDGSTP	IWDGSTP	Reserved						PD	STOP	SLEEP
	Reset Value									0	0	0	0	0	0	0			0			0	0	0							0	0	0

3.4.2 Power Control Register (PWR_CTRL)

Address offset: 0x00

Reset value: 0x0000 0621

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						PVDITEN	PVDFILEN	PVDCNT[7:0]							

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						rw	rw				rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				NRSTPOL	PDRS[1:0]		PLS[3:0]				PVDEN	CLRDBGPDF	CLRWKUPF	PDSTP	IWDGRSTEN
				rw	rw		rw				rw	w	w	rw	rw

Bit Field	Name	Description
31:26	Reserved	Reserved,the reset value must be maintained.
25	PVDITEN	PVD interrupt enable. 0: PVD interrupt disabled. 1: PVD interrupt enabled.
24	PVDFILEN	PVD filter enable. 0: PVD filter disabled. 1: PVD filter enabled.
23:16	PVDCNT[7:0]	PVD filter control counter value. 0x00: Not filtered ... 0xFF: Maximum filtering width Filter width = $(1/f_{LSI})$ × PVDCNT.
16:12	Reserved	Reserved,the reset value must be maintained.
11	NRSTPOL	NRST polarity select. 0: The falling edge of NRST pin. 1: The rising edge of NRST pin.
10:9	PDRS[1:0]	Adjust the V_{DDD} PDR trigger level in STOP mode. When the voltage in STOP mode falls below the set trigger level, the Power-Down Reset (PDR) will be triggered. Before configuring this register bit, PWR_CTRL3.PDRSELEN = '1' must be set first. 00: Reserved. 01: Reserved. 10: V_{DDD} PDR trigger level is 1.0V. 11: V_{DDD} PDR trigger level is 1.2V. Only V_{DDD} POR/PDR can reset this bit, if $V_{PDRS} < V_{STOP}$ values, the PDR will be triggered.
8:5	PLS[3:0]	PVD level selection. PVD threshold is controlled below:

PWR_CTRL.PLS	Voltage
0000	Reserved
0001	2.0V
0010	2.2V
0011	2.4V
0100	2.6V
0101	2.8V
0110	3.0V
0111	3.2V

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1000 3.4V 1001 3.6V 1010 3.8V 1011 4.0V 1100 4.2V 1101 4.4V 1110 4.6V 1111 4.8V
4	PVDEN	The Power voltage detector (PVD) enable. 0: PVD disabled. 1: PVD enabled.
3	CLRDBGPDF	The software writes a '1' to this bit to clear the DBGPDF status bit. Always read as 0. 0: Invalid. 1: Clear the DBGPDF status bit.
2	CLRWKUPF	Clear the wake-up bit. Always read as 0. 0: Invalid. 1: Clear WKUPF (write) after 2 system clock cycles.
1	PDSTP	Enter STOP/PD mode selection. 0: CPU output DEEPSLEEP is '1', and the chip enters STOP mode. 1: CPU output DEEPSLEEP is '1', and the chip enters PD mode.
0	IWDGRSTEN	IWDG reset enable control. 0: IWDG reset request will not generate a system reset. 1: IWDG reset request will generate a system reset.

3.4.3 Power Control Status Register (PWR_CTRLSTS)

Address offset: 0x04

Reset value: 0x0000 0800

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WKUP POL	Reserved	WKUP1 EN	WKUP0 EN	Reserved					PVDO	DBGPDF	WKUPF
				rw		rw	rw						r	r	r

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	WKUPPOL	Wakeup polarity for PA0/PA2. To wakeup PD mode by using rising edge or falling edge. Make sure disable wakeup enable before changing polarity value. 0: Falling edge.

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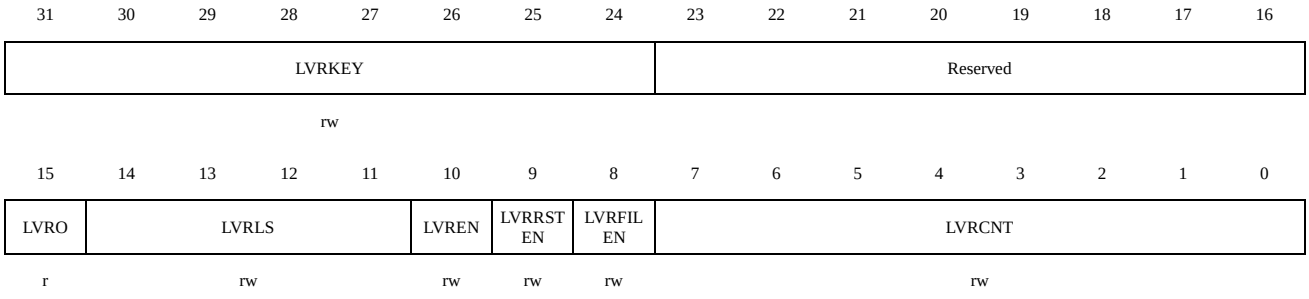
Bit Field	Name	Description
		1: Rising edge.
10	Reserved	Reserved, the reset value must be maintained.
9	WKUP1EN	WKUP pin PA2 enable control. 0: WKUP pin is used for general purpose I/O. An event on the WKUP pin does not wakeup the device from PD mode. 1: WKUP pin is used for wakeup from PD mode. *Note: this bit is reset by V_{DDD} POR Reset only.*
8	WKUP0EN	WKUP pin PA0 enable control. 0: WKUP pin is used for general purpose I/O. An event on the WKUP pin does not wakeup the device from PD mode. 1: WKUP pin is used for wakeup from PD mode. *Note: this bit is reset by VDDD POR Reset only.*
7:3	Reserved	Reserved, the reset value must be maintained.
2	PVDO	PVD output. It is valid only if PWR_CTRL.PVDEN = 1. 0: V_{DD} is higher than the PVD threshold selected with PWR_CTRL.PLS [3:0]. 1: V_{DD} is lower than the PVD threshold selected with PWR_CTRL.PLS [3:0].
1	DBGPDF	DBGPD mode status bit. When entering DBGPD mode, hardware sets this bit to '1'. Hardware clears this bit when software sets PWR_CTRL.CLRDBGPDF = 1. Only V_{DDD} POR/PDR can reset this bit. 0: Chip never entered DBGPD mode. 1: Chip has entered DBGPD mode.
0	WKUPF	DBGPD mode wake-up status bit. This bit is set by hardware after WKUP pin wakes up DBGPD mode. Hardware clears this bit when software sets PWR_CTRL.CLRWKUPF = 1. Only V_{DDD} POR/PDR can reset this bit. 0: No wakeup event occurred. 1: A wakeup event was received from the WKUP pin.

3.4.4 Power Control Register 2 (PWR_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000



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<table>
<tr><th>Bit Field</th><th>Name</th><th>Description</th></tr>
<tr><td>31:24</td><td>LVRKEY</td><td>LVR key.
Each time the software writes CTRL2[15:0], it must first write the key 0xA5 (unlocked) to this register.</td></tr>
<tr><td>23:16</td><td>Reserved</td><td>Reserved, the reset value must be maintained.</td></tr>
<tr><td>15</td><td>LVRO</td><td>LVR output.
It is valid only if PWR_CTRL2.LVREN = 1.
0: V_{DD} is higher than the LVR threshold selected by PWR_CTRL2.LVRLS [3:0].
1: V_{DD} is lower than the LVR threshold selected by PWR_CTRL2.LVRLS [3:0].</td></tr>
<tr><td>14:11</td><td>LVRLS</td><td>LVR level selection.
LVR threshold is controlled below:
<table>
<tr><th>PWR_CTRL2.LVRLS</th><th>Voltage</th></tr>
<tr><td>0000</td><td>Reserved</td></tr>
<tr><td>0001</td><td>2.0V</td></tr>
<tr><td>0010</td><td>2.2V</td></tr>
<tr><td>0011</td><td>2.4V</td></tr>
<tr><td>0100</td><td>2.6V</td></tr>
<tr><td>0101</td><td>2.8V</td></tr>
<tr><td>0110</td><td>3.0V</td></tr>
<tr><td>0111</td><td>3.2V</td></tr>
<tr><td>1000</td><td>3.4V</td></tr>
<tr><td>1001</td><td>3.6V</td></tr>
<tr><td>1010</td><td>3.8V</td></tr>
<tr><td>1011</td><td>4.0V</td></tr>
<tr><td>1100</td><td>4.2V</td></tr>
<tr><td>1101</td><td>4.4V</td></tr>
<tr><td>1110</td><td>4.6V</td></tr>
<tr><td>1111</td><td>4.8V</td></tr>
</table></td></tr>
<tr><td>10</td><td>LVREN</td><td>LVR enable.
0: LVR disabled.
1: LVR enabled.</td></tr>
<tr><td>9</td><td>LVRRSTEN</td><td>LVR reset Enable.
0: LVR reset disabled.
1: LVR reset enabled.</td></tr>
<tr><td>8</td><td>LVRFILEN</td><td>LVR filter Enable.
0: LVR filter disabled.
1: LVR filter enabled.</td></tr>
<tr><td>7:0</td><td>LVRCNT</td><td>LVR filter control count value.
0x00: Not filtered
...
0xFF: Maximum filtering width
Filter width = $(1/f_{LSI}) \times$ LVRCNT.</td></tr>
</table>

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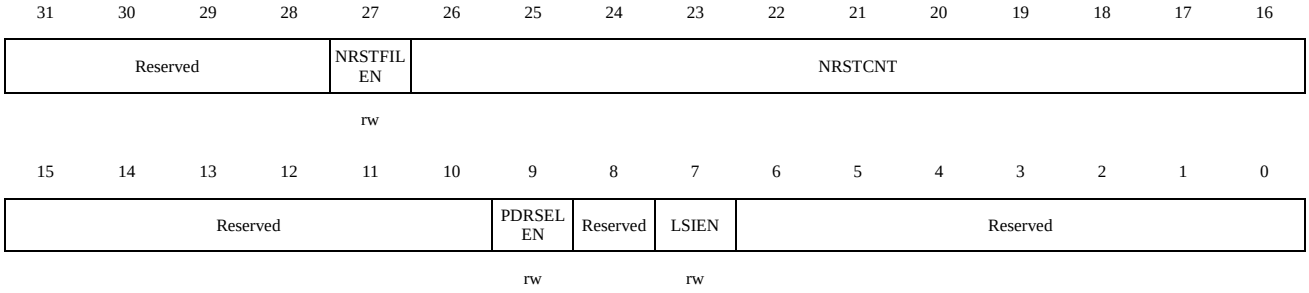
3.4.5 Power Control Register 3 (PWR_CTRL3)

Address offset: 0x14

Reset value: 0x0000 037F



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	NRSTFILEN	NRST filter Enable 0: NRST filter disabled. 1: NRST filter enabled. *Note: In STOP mode, the clock is disabled. If NRST filtering is enabled, it may cause pin reset to fail. Therefore, it is necessary to disable NRST filtering before entering STOP mode and enable it after exiting STOP mode.*
26:16	NRSTCNT	NRST filter control count value. 0x000: Not filtered …. 0x7FF: Maximum filtering width Filter width = $(1/f_{SYSCLK}) \times$ NRSTCNT.
15:10	Reserved	Reserved, the reset value must be maintained.
9	PDRSELEN	Power-Down Reset (PDR) trigger level selection enable 0: V_{DDD} PDR selection is 1.2V. 1: V_{DDD} PDR selection is controlled by PWR_CTRL.PDRS[1:0].
8	Reserved	Reserved, the reset value must be maintained.
7	LSIEN	Control PWR to enable LSI. 0: After entering STOP mode, PWR no longer request to enable LSI. 1: After entering STOP mode, PWR requests to enable LSI.
6:0	Reserved	Reserved, the reset value must be maintained.

3.4.6 Power Control Register 4 (PWR_CTRL4)

Address offset: 0x20

Reset value: 0x0000 0020

This register is write-protected. Each time the software writes to this register, it must first write the key 0x0175_3603 (unlocked) to this register.

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													RUNF	STBFLH	FLHWKUP
													r	rw	rw

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	RUNF	RUN mode flag. 0: System not in RUN mode. 1: System in RUN mode.
1	STBFLH	Flash deep standby mode enable (configurable in RUN mode) This bit is set and reset by software, or reset by hardware in STOP and PD modes. 0: After the software clears this bit, Flash exit the deep standby mode and return to the normal operating mode. 1: After the software set this bit to '1', the Flash enter deep standby mode.
0	FLHWKUP	Enable Flash fast wake-up. 0: When the chip exits from STOP mode, use Flash to wake up normally. 1: When the chip exits from STOP mode, use Flash to wake up quickly. *Note: please refer to the data sheet for the wake-up time.*

3.4.7 Power Control Register 5 (PWR_CTRL5)

Address offset: 0x24

Reset value: 0x0000 0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STPMRSEL[1:0]		Reserved	
												rw			

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:2	STPMRSEL[1:0]	After the chip enters STOP mode, V_{DDD} output voltage is selected. Before configuring this register bit, the software must first configure PWR_CTRL6.STPMREN = '11'. 00: No used. 01: V_{DDD} output voltage 1.5V. 10: Reserved. 11: V_{DDD} output voltage 1.2V.

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Bit Field	Name	Description
		This bit is reset by V_{DDD} POR only.
1:0	Reserved	Reserved, the reset value must be maintained.

3.4.8 Power Control Register 6 (PWR_CTRL6)

Address offset: 0x28

Reset value: 0x0000 0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												STPMREN[1:0]		Reserved	
												rw			

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:2	STPMREN[1:0]	V_{DDD} Output voltage selection enable. 00: Enter STOP mode, V_{DDD} Output voltage 1.5V. 01: Reserved. 10: Reserved. 11: Enter STOP mode, V_{DDD} Output voltage control by PWR_CTRL5.STPMRSEL. This bit is reset by V_{DDD} POR only.
1:0	Reserved	Reserved, the reset value must be maintained.

3.4.9 Debug Control Register (DBG_CTRL)

Address offset: 0x30

Reset value: 0x0000 0000

Only V_{DDD} POR/PDR can reset this register. Only after the Debugger is connected, the software can write access to this register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											TIM2STP	TIM4STP	TIM6STP	TIM5STP	I2C2 TIMOUT
											rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C1 TIMOUT	CANSTP	Reserved	TIM3STP	Reserved	TIM1STP	WWDG STP	IWDG STP	Reserved					PD	STOP	SLEEP
rw	rw		rw		rw	rw	rw						rw	rw	rw

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.

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Bit Field	Name	Description
20	TIM2STP	TIM2 stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of TIM2 operates normally 1: The counter of TIM2 stops operating
19	TIM4STP	TIM4 stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of TIM4 operates normally 1: The counter of TIM4 stops operating
18	TIM6STP	TIM6 stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of TIM6 operates normally 1: The counter of TIM6 stops operating
17	TIM5STP	TIM5 stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of TIM5 operates normally 1: The counter of TIM5 stops operating
16	I2C2TIMOUT	I^2C2 stops SMBUS timeout mode when core is stopped. This bit is set or cleared by software. 0: Same as normal mode operation 1: Frozen the timeout control of SMBUS
15	I2C1TIMOUT	I^2C1 stops SMBUS timeout mode when core is stopped. This bit is set or cleared by software. 0: Same as normal mode operation 1: Frozen the timeout control of SMBUS
14	CANSTP	CAN stops working when core is stopped. This bit is set or cleared by software. 0: CAN operates normally 1: CAN stops operating
13	Reserved	Reserved, the reset value must be maintained.
12	TIM3STP	TIM3 stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of TIM3 operates normally 1: The counter of TIM3 stops operating
11	Reserved	Reserved, the reset value must be maintained.
10	TIM1STP	TIM1 stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of TIM1 operates normally 1: The counter of TIM1 stops operating
9	WWDGSTP	WWDG stops operating when core enters debug state. This bit is set or cleared by software. 0: The counter of WWDG operates normally 1: The counter of WWDG stops operating
8	IWDGSTP	IWDG stops operating when core enters debug state.

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Bit Field	Name	Description
		This bit is set or cleared by software. 0: The counter of IWDG operates normally 1: The counter of IWDG stops operating
7:3	Reserved	Reserved, the reset value must be maintained.
2	PD	Debug PD mode control. Set or cleared by software. 0: (FCLK off, HCLK off) system enters PD mode, digital circuit part is unpowered. From a software point of view, exiting PD mode is the same as a power-on reset. 1: (FCLK on, HCLK on) system enters DBGPD mode, digital circuit part is powered, and FCLK clock is provided by the internal RC oscillator. In addition, the microcontroller exits DBGPD mode by generating a system reset, which is the same as a system reset.
1	STOP	Debug STOP mode control. Set or cleared by software. 0: (FCLK off, HCLK off) system enters STOP mode, clock controller disables all clocks (including HCLK and FCLK). When exiting STOP mode, the configuration of the clock is the same as after reset (Microcontroller is clocked by the 48MHz internal RC oscillator (HSI)). 1: (FCLK on, HCLK on) system enters DBGSTOP mode, FCLK clock is provided by the internal RC oscillator.
0	SLEEP	Debug SLEEP mode. Set or cleared by software. 0: (FCLK on, HCLK off) In SLEEP mode, FCLK is provided by the previously configured system clock, and HCLK is off. Since SLEEP mode does not reset the configured clock system, software does not need to reconfigure the clock system when exiting from SLEEP mode. 1: (FCLK on, HCLK on) In DBGSLEEP mode, both FCLK and HCLK clocks are provided by the previously configured system clock.

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4 Reset and Clock Control (RCC)

4.1 Reset Control Unit

N32G05x supports the following two types of reset:

- Power Reset
- System Reset

4.1.1 Power Reset

A power reset occurs in the following circumstances:

- Power-on/Power-down reset (POR/PDR reset).
- Return from PD mode.

The power reset will reset all registers. (See Figure 3-1 Power Supply Block Diagram).

The reset source in the diagram will ultimately act on the NRST pin and maintain a low level during the reset process. The reset entry vector is fixed at address 0x0000_0004. For more details, refer to Table 6-1 Vector Table.

4.1.2 System Reset

Except for the following registers, a system reset will reset all registers to their reset state.

- RCC_CTRL.HSEBP
- RCC_CTRL.HSITRIM
- RCC_LSCTRL.LSITRIM
- RCC_EMCCTRL
- RCC_CTRLSTS
- PWR_CTRL3.NRSTFILEN
- PWR_CTRL3.NRSTCNT
- PWR_CTRL.PDRS
- PWR_CTRL.NRSTPOL
- PWR_CTRLSTS.WKUPPOL
- PWR_CTRLSTS.WKUP1EN
- PWR_CTRLSTS.WKUP0EN
- PWR_CTRLSTS.DBGPDF
- PWR_CTRLSTS.WKUPF
- PWR_CTRL5.STBMRSEL
- PWR_CTRL6.STBMREN

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- DBG_CTRL
- RTC_DATE
- RTC_TSH
- RTC_SUBS
- RTC_INITSTS

A system reset is triggered when one of the following events occurs:

- A low level on the NRST pin (External Reset)
- Window Watchdog counter expiration (WWDG Reset)
- Independent Watchdog counter expiration (IWDG Reset)
- Software Reset (SW Reset)
- Low-power Management Reset
- MMU Protection Reset
- LVR Reset
- RAM Parity Error Reset
- EMC Reset
- M0 Core Lockup Reset

The reset source can be identified by checking the reset flags in the Control/Status Register (RCC_CTRLSTS).

4.1.2.1 **Software reset**

A software reset can be generated by setting the SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register. Refer to Cortex®-M0 technical reference manual for further information.

4.1.2.2 **Low-power management reset**

Low-power management reset can be generated by using the following methods:

- A low-power management reset is generated when entering PD mode: This reset is enabled by setting the nRST_PD bit in the user option bytes to 1. In this case, instead of entering PD mode, the system will reset when the process to enter PD mode is executed.
- Generate low-power management reset when entering STOP mode: This reset is enabled by setting the nRST_STOP bit in the user OptionByte. At this time, even if the process to enter STOP mode is performed, the system will be reset instead of entering STOP mode.

The system reset signal provided to the chip is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20μs for each reset source (external or internal). For external reset, the reset pulse is generated while the NRST pin is asserted low.

The Figure below shows the system reset generation circuit.

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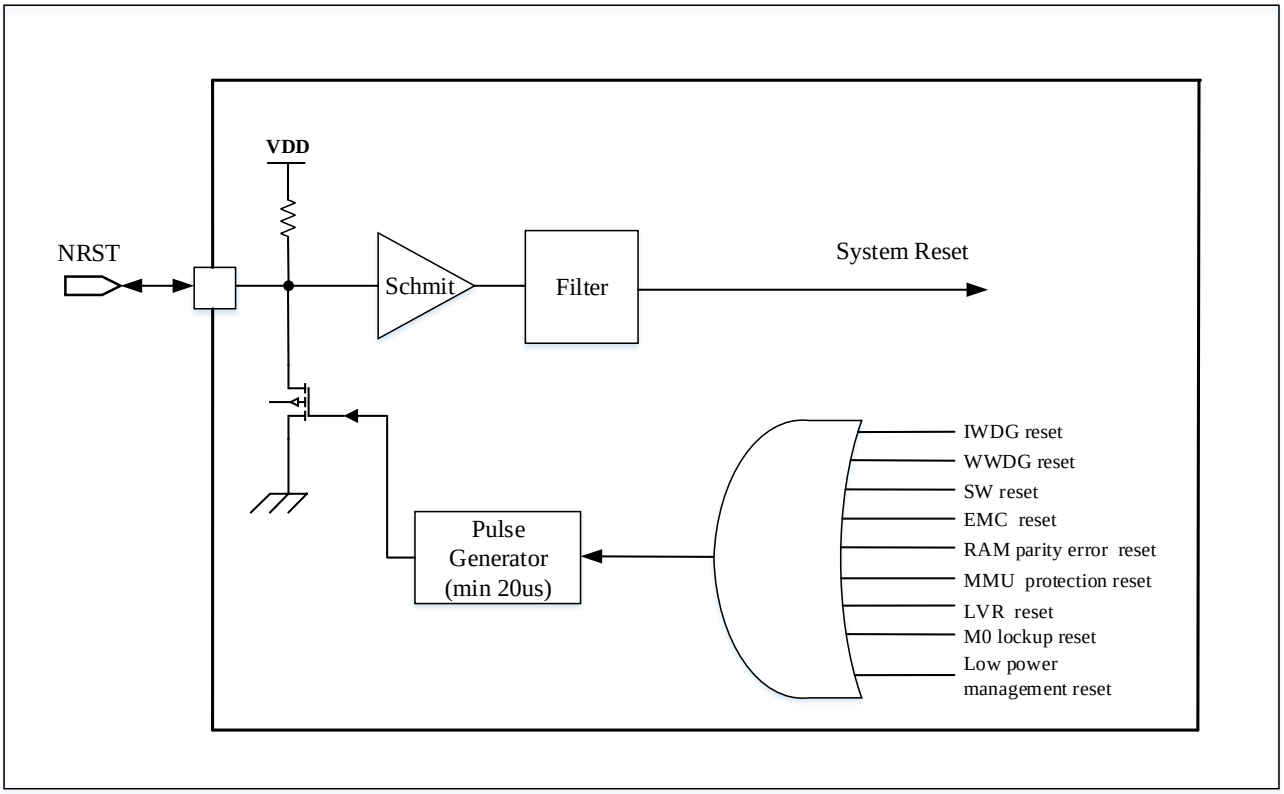
Figure 4-1 System Reset Generation



4.2 Clock Control Unit

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSI oscillator clock;
- HSE oscillator clock;
- PLL clock;
- LSI oscillator clock.

Note: Unless otherwise specified, HSI refers to the 8M high-speed internal clock. The HSI24M clock is used exclusively as a clock source for the ADC.

Each clock source can be independently turned on or off when not in use to optimize system power consumption.

Several prescalers are available to configure the frequencies of the AHB, High-speed APB (APB2), and Low-speed APB (APB1). The maximum frequency for AHB is 64 MHz, for APB2 is 64 MHz, and for APB1 is 32 MHz.

Except for the cases listed below, all peripheral clocks are derived from the peripheral clocks (AHB, APB2, APB1):

- By configuring RCC_CFG2.ADCCLKSEL, one of the following can be selected as the working clock source for the ADC:
  - HSI 24M clock
  - PLL clock
  - AHB clock (HCLK)

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- By configuring RCC_CFG2.ADC1MSEL, one of the following can be selected as the ADC1M clock source:
  - HSI clock
  - HSE clock
- By configuring RCC_CFG2.LCDCLKSEL, one of the following can be selected as the LCD clock source:
  - HSI clock divided by 8
  - HSE clock divided by 16
- By configuring RCC_CFG3.GCLKSEL, one of the following can be selected as the LED GCLK clock source:
  - HSI clock
  - HSE clock
- By configuring RCC_CFG2.TIM1CLKSEL, one of the following can be selected as the working clock source for TIM1:
  - APB2 clock (PCLK2)
  - SYSCLK clock
- By configuring RCC_CFG2.TIM6CLKSEL, one of the following can be selected as the working clock source for TIM6:
  - APB1 clock (PCLK1)
  - LSI clock

Note: When the timer clock source is PCLK, the timer clock frequency is automatically set by the hardware according to the following two cases:

- ✧ *If the corresponding APB clock prescaler is 1, the timer clock frequency is the same as the APB bus frequency.*
- ✧ *If the corresponding APB clock prescaler is not 1, the timer clock frequency is twice the APB bus frequency.*

- The clock source for IWDG and the BEEPER is the LSI oscillator.
- The clock source for the Flash memory programming interface is always the HSI clock.
- By configuring the SysTick Control and Status Register, one of the following two options can be selected as the SysTick clock source:
  - AHB Clock (HCLK) divided by 8
  - AHB Clock (HCLK)

FCLK is the free-running clock of Cortex®-M0. For more details, refer to the ARM Cortex®-M0 technical reference manual.

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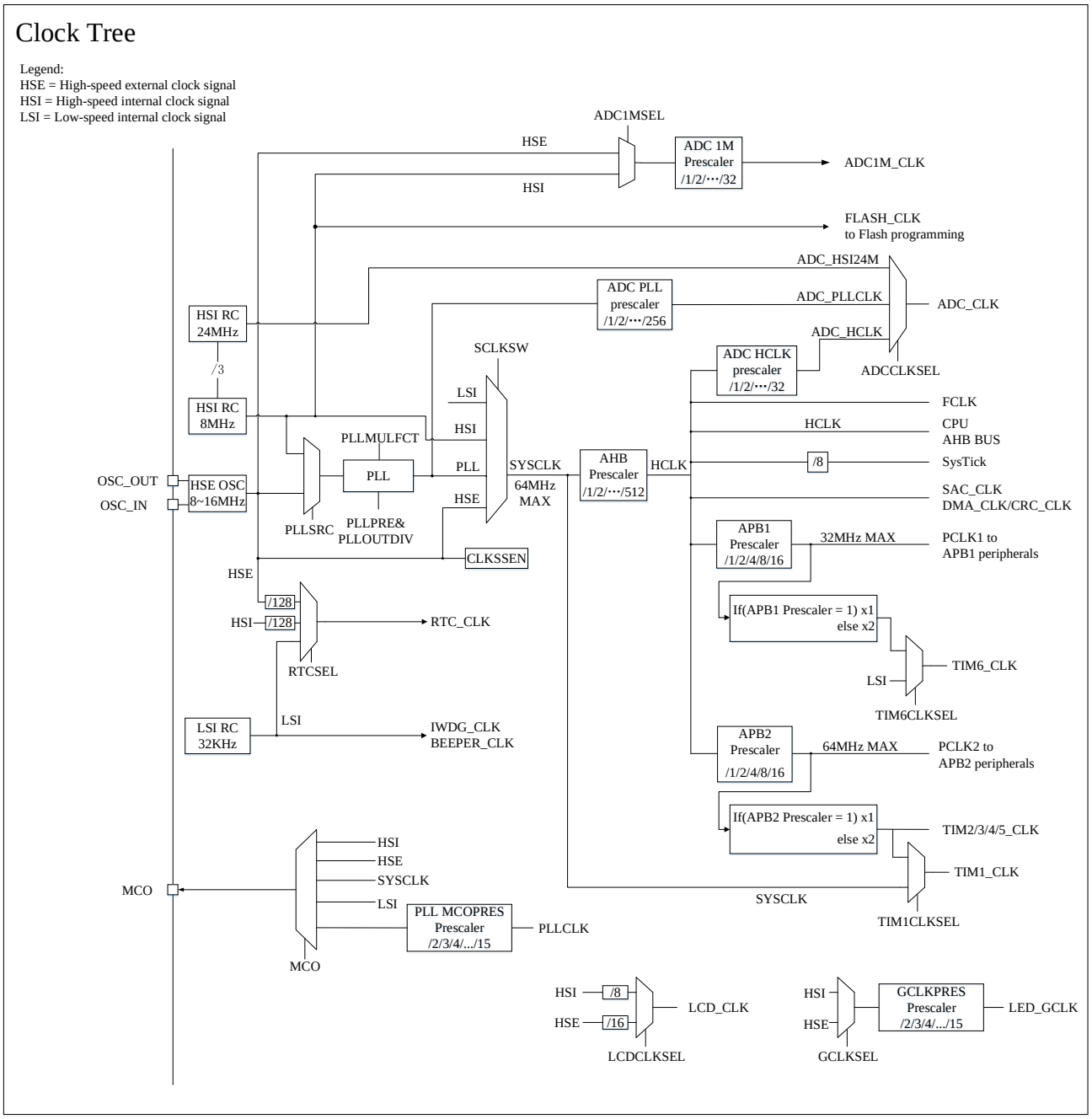
4.2.1 Clock Tree Diagram

Figure 4-2 Clock Tree



Notes:

1. *The maximum system frequency is 64MHz.*
2. *For more details about the internal and external clock source characteristics, please refer to the "Electrical Characteristics" section in the product datasheet.*

4.2.2 HSE Clock

The high-speed external clock signal (HSE) can be generated from the following two clock sources:

- HSE external crystal/ceramic resonator

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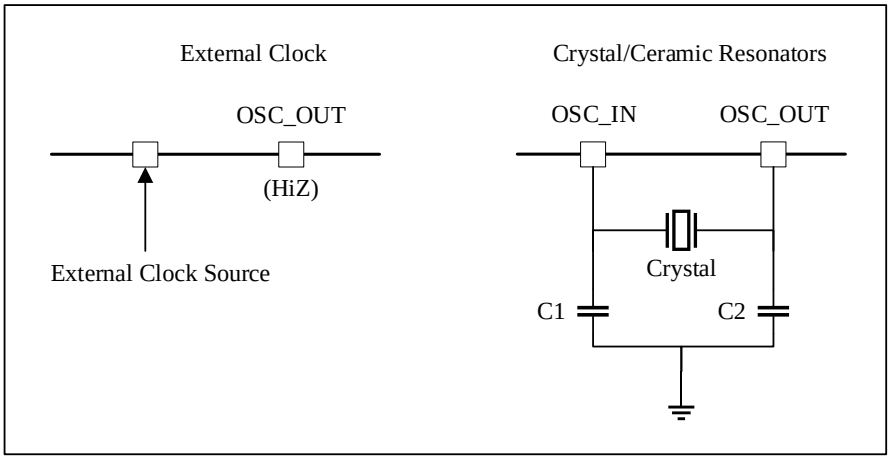
- HSE user external clock (PD14 Pin input)

In HSE bypass mode or crystal mode, RCC_CTRL.HSEEN needs to be set to 1. If RCC_CTRL.HSEEN=0, HSE will be turned off.

To reduce distortion of the clock output and shorten the start-up stablize time, the crystal/ceramic resonator and load capacitor must be placed as close as possible to the oscillator pins of the chip. The loading capacitance value must be adjusted according to the chosen oscillator.

Figure 4-3 HSE Clock Source



4.2.2.1 External clock source (HSE bypass mode)

In this mode, an external clock source must be provided. Its frequency range is 16 MHz. Users can select this mode by setting the RCC_CTRL.HSEBP and RCC_CTRL.HSEEN bits. When PD0 is used as an external clock signal (50% duty cycle square, sine or triangle wave), it must be connected to the OSC_IN pin while the OSC_OUT pin must be left floating (Hi-Z). See Figure 4-3.

4.2.2.2 External crystal/ceramic resonator (HSE crystal mode)

The 8 to 16 MHz external oscillator has the advantage of producing a more accurate main clock for the system. The associated hardware configuration is shown in See Figure 4-3. For more details, please refer to the electrical characteristics section of the datasheet.

The RCC_CTRL.HSERDF bit indicates whether the high-speed external oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock Interrupt Register (RCC_CLKINT).

HSE clock can be switched on and off by setting the RCC_CTRL.HSEEN bit.

If the user needs to change the configuration of RCC_CTRL.HSEBP during operation, it should be configured before enabling RCC_CTRL.HSEEN.

4.2.3 HSI Clock

The HSI (High-Speed Internal) clock signal is generated by an internal 8 MHz RC oscillator, which can be used directly as the system clock or as an input to the PLL. The HSI RC oscillator provides a clock source without any external components. Its startup time is shorter than that of the HSE crystal oscillator. However, even after calibration, its frequency accuracy remains relatively poor.

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Manufacturing processes cause the RC oscillator frequency to vary between different chips, which is why the HSI clock frequency of each chip is calibrated to 1% (at 25℃) before leaving the factory.

Because a user's application may be affected by variations in voltage or temperature, these factors can also impact the frequency accuracy of the RC oscillator. Users can adjust the HSI frequency using the RCC_CTRL.HSITRIM[4:0] bits.

The RCC_CTRL.HSIRDF bit indicates whether the HSI RC oscillator is stable. During startup, the HSI RC output clock will not be released until this bit is set by hardware. The HSI clock can be turned on and off by setting the RCC_CTRL.HSIEN bit.

If the HSE crystal oscillator fails, the HSI clock can serve as a backup source. Refer to Section 4.2.7 Clock Security System (CLKSS) for more details.

4.2.4 PLL Clock

The internal PLL can be used to multiply the HSI RC output clock or the HSE crystal output clock. Refer to Figure 4-4. The PLL configuration (selecting HSI or HSE as the PLL input clock, choosing the multiplier, selecting the prescaler and output divider) must be completed before activation. Once the PLL is activated, these parameters cannot be changed. The PLL can be configured using the control bits in the RCC_CTRL and RCC_CFG registers.

When switching the PLL input clock source (via the RCC_CFG.PLLSRC bit in the clock configuration register), the original clock source must be turned off only after the new clock source is ready.

If the PLL interrupt is enabled in the clock interrupt register, an interrupt request can be generated when the PLL is ready.

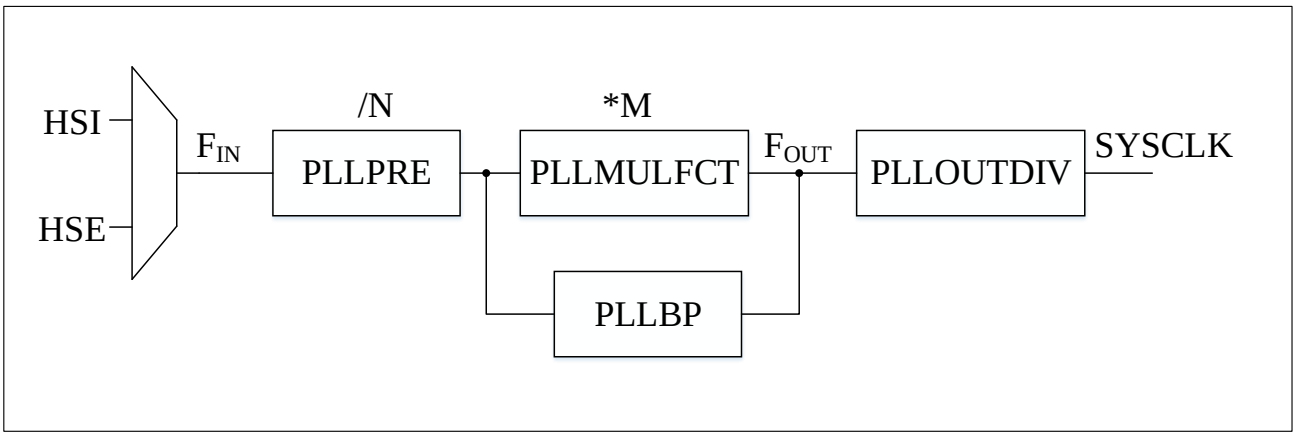
The input frequency is F_{IN}, and F_{IN} must be within the range of 4 MHz to 16 MHz. The value of F_{IN}/N must also be within the range of 4 MHz to 16 MHz.

When the PLL bypass is not enabled: the output frequency is $F_{OUT} = F_{IN} * M / N$, and F_{OUT} must be within the range of 48 MHz to 72 MHz. When the PLL bypass is enabled: $F_{OUT} = F_{IN} / N$, and F_{OUT} must be within the range of 4 MHz to 16 MHz.

The system frequency is derived from F_{OUT} divided by the prescaler, and the software must be correctly configured to avoid SYSCLK exceeding 64 MHz.

Additionally, the user can configure RCC_CTRL.PLLBP to bypass the PLL's multiplication functions.

Figure 4-4 PLL Clock Configuration



Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

4.2.5 LSI Clock

The LSI RC can clock the IWDG and AWU in STOP modes. The LSI clock frequency is about 32kHz. For further information please refer to the Electrical Characteristics section of the data sheet.

The LSI clock can be turned on or off using the RCC_CTRLSTS.LSIEN bit.

The RCC_CTRLSTS.LSIRD bit flag indicates if the LSI clock is stable. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock Interrupt Register (RCC_CLKINT).

4.2.5.1 LSI calibration

The internal low-speed oscillator (LSI) frequency error can be compensated through calibration to achieve higher accuracy for the RTC (when clocked by LSI), Beeper, and IWDG time base.

The steps for LSI calibration are as follows:

1. Turn on TIM2 and set channel 3 to input capture mode.
2. Set the TIM2_CTRL1.C3SEL bit to 1 to internally connect the LSI to channel 3 of TIM2.
3. Measure the LSI clock frequency through TIM2 capture/compare 3 events or interrupts.
4. Adjust the RCC_LSICTRL.LSITRIM[4:0] (default value 16, adjustment step size 720 Hz) according to the deviation of the measured LSI frequency from 32 kHz.

4.2.6 System Clock (SYSCLK) Selection

After a system reset, the HSI oscillator is selected as the system clock. When the clock source is used directly or indirectly through the PLL as the system clock, HSI cannot be stopped.

Switching from one clock source to another will only occur when the target clock source is ready (either after a delay to start the stabilization phase or PLL stabilization). When the selected clock source is not ready, the switching of the system clock will not occur until the target clock source is ready.

RCC_CFG.SCLKSW[1:0] are used to select the system clock source. Status bits in RCC_CTRL and RCC_LSCTRL indicate which clock is ready, and RCC_CFG indicates which clock is currently used as the system clock.

4.2.7 Clock Security System (CLKSS)

By setting the RCC_CTRL.HSECSSEN bit, the HSE clock security system is activated. Once activated, the clock detector is enabled after the start-up delay of the HSE oscillator and disabled when the HSE clock is turned off.

If HSE clock failure occurs, the HSE oscillator will be automatically turned off, a clock failure event will be sent to the brake input of the advanced timer (TIM1) and generate a clock security system interrupt (CLKSSIF). The interrupt is connected to the Cortex®-M0 Non-Maskable Interrupt (NMI), allowing software to take rescue measures in the interrupt, set and clear the interrupt.

Once the CSS is activated and the HSE clock fails, the CSS interrupt is generated and the NMI is automatically generated. The NMI will be executed continuously until the CSS interrupt pending bit is cleared. Therefore, it is necessary to clear the CSS interrupt by setting the RCC_CLKINT.CLKSSICLR bit in the NMI handler.

If the HSE oscillator is directly or indirectly used as the system clock (indirectly means: it is used as the PLL input clock, and the PLL clock is used as the system clock), the clock failure will cause a switch of the system clock to the HSI oscillator and the disabling of the external HSE oscillator. If HSE clock (divided or not) is selected as PLL input clock then upon HSE clock failure, the PLL will be turned off.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

4.2.8 RTC Clock

By programming RCC_LSCTRL.RTCSEL [1:0] bits, the RTCCLK clock source can be either the HSE/128, HSI/128 or LSI clocks.

4.2.9 Watchdog Clock

If the IWDG is started by either hardware option or software access, the LSI oscillator will be forced ON and cannot be disabled. After the LSI oscillator is stabilized, the clock is provided to the IWDG.

4.2.10 Microcontroller Clock Output (MCO)

Microcontroller Clock Output (MCO) function allows the clock signal to be output to the external MCO pin, and the corresponding GPIO port register must be configured for the corresponding function. The following five clock signals can be selected as the MCO clock:

- SYSCLK
- HSI
- HSE
- LSI
- PLL Clock Division

The clock selection is controlled by the RCC_CFG.MCO[2:0] bits.

4.3 RCC Registers

The RCC registers are accessible through AHB bus. The register descriptions are as follows.

4.3.1 RCC Register Overview

Table 4-1 RCC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RCC_CTRL	Reserved					LKUPRSTEN	PLLRDF	PLLEN	PLLOUTEN	PLLBP	HSERDTM[1:0]		CLKSSEN	HSEBP	HSERDF	HSEEN	Reserved								HSITRIM[3:0]				Reserved	HSI24MRDF	HSIRDF	HSIEN
	Reset Value						0	0	0	1	0	0	0	0	0	0	0									1	0	0	0		1	1	1
004h	RCC_CFG	MCOPRES[3:0]				MCO[2:0]			PLLSRC	PLLOUTDIV[1:0]		PLLPRE[1:0]		PLLMULFCT[3:0]				SCLKSTS2[1:0]		APB2PRES[2:0]			APB1PRES[2:0]			AHBPRES[3:0]				SCLKSTS	SCLKSW[2:0]		
	Reset Value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	RCC_CLKINT	Reserved								CLKSSICLR	Reserved	RAMPERRCLR	PLLRDICLR	HSERDICLR	HSIRDICLR	Reserved	LSIRDICLR	Reserved	RAMPERRRSTEN	RAMPERRIEN	PLLRDIEN	HSERDIEN	HSIRDIEN	Reserved	LSIRDIEN	CLKSSIF	Reserved	RAMPERRIF	PLLRDIF	HSERDIF	HSIRDIF	Reserved	LSIRDIF
	Reset Value									0		0	0	0	0		0		0	0	0	0	0		0	0		0	0	0	0		0
00Ch	RCC_APB2PRST	Reserved													TIM5RST	TIM4RST	TIM3RST	UART2RST	UART1RST	TIM2RST	TIM1RST	SPI3RST	SPI2RST	SPI1RST	Reserved			IOPDRST	IOPCRST	IOPBRST	IOPARST	Reserved	AFIORST
	Reset Value														0	0	0	0	0	0	0	0	0	0				0	0	0	0		0

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

| | | |

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								HSITRIM[3:0]				Reserved	HSI24MRDF	HSIRDF	HSIEN
								rw					r	r	rw

Bit Field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	LKUPRSTEN	M0 core lockup reset enable 0: No reset generated when the M0 core locks up 1: Reset generated when the M0 core locks up
25	PLLRDF	PLL clock ready flag This bit is set by hardware when the PLL clock is ready. 0: PLL not ready 1: PLL ready
24	PLLEN	PLL enable bit This bit is set and cleared by software. It is cleared by hardware when entering STOP or PD mode. When the PLL is used as the system clock, this bit cannot be cleared. 0: PLL disabled 1: PLL enabled
23	PLLOUTEN	PLL clock output enable bit 0: PLL clock output disabled 1: PLL clock output enabled
22	PLLBP	PLL bypass mode 0: Fout = Fin * M / N 1: Fout = Fin / N
21:20	HSERDTM[1:0]	External high-speed clock ready delay time 00: HSE ready delay 0.5 ms 01: HSE ready delay 1.0 ms 10: HSE ready delay 1.5 ms 11: HSE ready delay 2.5 ms
19	CLKSSEN	Clock security system enable bit This bit is set and cleared by software. 0: Clock detector disabled 1: Clock detector enabled if the HSE oscillator is ready
18	HSEBP	External high-speed clock bypass enable bit This bit is set and cleared by software. It can only be written when the HSE oscillator is disabled. 0: HSE oscillator bypass function disabled 1: HSE oscillator bypass function enabled *Note: This bit must be enabled together with the RCC_CTRL.HSEEN bit.*
17	HSERDF	External high-speed clock ready flag This bit is set by hardware when the HSE is ready. It is cleared after 6 HSE clock cycles when the HSEEN bit is cleared.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		0: HSE not ready 1: HSE ready
16	HSEEN	External high-speed clock enable bit This bit is set and cleared by software. It is cleared by hardware when entering STOP or PD mode. When the HSE is used directly or indirectly as the system clock, this bit cannot be cleared. 0: HSE oscillator disabled 1: HSE oscillator enabled
15:8	Reserved	Reserved, the reset value must be maintained.
7:4	HSITRIM[3:0]	Internal high-speed clock calibration value This value is written by software to calibrate the frequency of the internal HSI RC oscillator. The default value is 8, and the adjustment step size is 24 kHz. The setting value (rounded) = Current Value – (Measured HSI Frequency – Target Frequency 8000K) / (Step Size 24K);
3	Reserved	Reserved, the reset value must be maintained.
2	HSI24MRDF	Internal 24M high-speed clock ready flag This bit is set by hardware when the 24M HSI is ready, and it is used exclusively to provide a clock for the ADC. After the HSIEN bit is cleared, this bit requires 6 internal 24 MHz oscillator clock cycles to be cleared. 0: HSI not ready 1: HSI ready
1	HSIRDF	Internal 8M high-speed clock ready flag This bit is set by hardware when the 8M HSI is ready. After the HSIEN bit is cleared, this bit requires 6 internal 8 MHz oscillator clock cycles to be cleared. 0: HSI not ready 1: HSI ready
0	HSIEN	Internal high-speed clock enable This bit is set and cleared by software. It is set by hardware to enable the HSI oscillator when returning from STOP or PD mode or when an HSE failure occurs. If the HSI is used directly or indirectly as the system clock, this bit cannot be reset. 0: HSI oscillator disabled 1: HSI oscillator enabled

4.3.3 Clock Configuration Register (RCC_CFG)

Address offset: 0x04

Reset value: 0x4000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCOPRES[3:0]				MCO[2:0]			PLLSRC	PLLOUTDIV[1:0]		PLLPRE[1:0]		PLLMULFCT[3:0]			
rw				rw			rw	rw		rw		rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

SCLKSTS2[1:0]	APB2PRES[2:0]	APB1PRES[2:0]	AHBPRES[3:0]	SCLKSTS	SCLKSW[2:0]
r	rw	rw	rw	r	rw

Bit Field	Name	Description
31:28	MCOPRES[3:0]	MCO prescaler Set or cleared by software. 0010: PLL clock divided by 2 is used as the MCO clock 0011: PLL clock divided by 3 is used as the MCO clock 0100: PLL clock divided by 4 is used as the MCO clock 0101: PLL clock divided by 5 is used as the MCO clock 0110: PLL clock divided by 6 is used as the MCO clock 0111: PLL clock divided by 7 is used as the MCO clock 1000: PLL clock divided by 8 is used as the MCO clock 1001: PLL clock divided by 9 is used as the MCO clock 1010: PLL clock divided by 10 is used as the MCO clock 1011: PLL clock divided by 11 is used as the MCO clock 1100: PLL clock divided by 12 is used as the MCO clock 1101: PLL clock divided by 13 is used as the MCO clock 1110: PLL clock divided by 14 is used as the MCO clock 1111: PLL clock divided by 15 is used as the MCO clock Other values: Not allowed
27:25	MCO[2:0]	MCU clock output Set and cleared by software. 000: No clock 001: LSI clock 010: System clock 011: HSI clock 100: HSE clock 101: PLL divided clock Other values: Not allowed *Note: The clock output may be truncated when starting or switching the MCO clock source. When the system clock is output to the MCO pin, ensure that the output clock frequency does not exceed the maximum I/O pin frequency of 30 MHz.*
24	PLLSRC	PLL clock source Set or cleared by software, can only be written when the PLL is disabled. 0: HSI clock as PLL input clock 1: HSE clock as PLL input clock
23:22	PLLOUTDIV[1:0]	PLL output clock division factor Set and cleared by software. 00: No division 01: Divided by 2 10: Divided by 3 11: Divided by 4

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
21:20	PLLPRE[1:0]	PLL prescaler Can only be written when the PLL is disabled. 00: PLL input clock divided by 1 01: PLL input clock divided by 2 10: PLL input clock divided by 3 11: PLL input clock divided by 4
19:16	PLLMULFCT[3:0]	PLL multiplication factor Can only be written when the PLL is disabled. 0000: Multiply by 3 0001: Multiply by 4 0010: Multiply by 5 0011: Multiply by 6 ... 1111: Multiply by 18
15:14	SCLKSTS2[1:0]	To be used in conjunction with the SCLKSTS bit.
13:11	APB2PRES[2:0]	APB2 (high-speed APB) prescaler Set or cleared by software, configures the prescaler for the APB2 clock (PCLK2). Ensure that the APB2 clock frequency does not exceed 64 MHz. 0xx: HCLK not divided 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
10:8	APB1PRES[2:0]	APB1 (low-speed APB) prescaler Set or cleared by software, configures the prescaler for the APB1 clock (PCLK1). Ensure that the APB1 clock frequency does not exceed 32 MHz. 0xx: HCLK not divided 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
7:4	AHBPRES[3:0]	AHB prescaler Set or cleared by software, configures the prescaler for the AHB clock (HCLK). 0xxx: SYSCLK not divided 1000: SYSCLK divided by 2 1001: SYSCLK divided by 4 1010: SYSCLK divided by 8 1011: SYSCLK divided by 16 1100: SYSCLK divided by 64 1101: SYSCLK divided by 128 1110: SYSCLK divided by 256 1111: SYSCLK divided by 512
3	SCLKSTS	System clock switch status (used with SCLKSTS2 bit)

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		Set and cleared by hardware to indicate which clock source is used as the system clock. 000: HSI oscillator used as the system clock 001: HSE oscillator used as the system clock 010: PLL used as the system clock 011: LSI used as the system clock Other values: Reserved
2:0	SCLKSW[2:0]	System clock switch Set and cleared by software to select the SYSCLK source. When exiting STOP or PD mode, or when an HSE oscillator failure occurs and CLKSSEN is enabled, this bit is set by hardware to force the selection of HSI. 000: HSI selected as system clock 001: HSE selected as system clock 010: PLL selected as system clock 011: LSI selected as system clock Other values: Reserved

4.3.4 Clock Interrupt Register (RCC_CLKINT)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CLKSS ICLR	Reserved	RAMP ERRCLR	PLLRD ICLR	HSERD ICLR	HSIRD ICLR	Reserved	LSIRD ICLR
		r						w		w	w	w	w		w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	RAMPER RRSTEN	RAMP ERRIEN	PLLRD IEN	HSERD IEN	HSIRD IEN	Reserved	LSIRD IEN	CLKSSIF	Reserved	RAMP ERRIF	PLLRDIF	HSERDIF	HSIRDIF	Reserved	LSIRDIF
	rw	rw	rw	rw	rw		rw	r		r	r	r	r		r

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	CLKSSICLR	Clock security system interrupt clear bit Set to 1 by software to clear the CLKSSIF flag. 0: No effect 1: Clear the CLKSSIF interrupt flag
22	Reserved	Reserved, the reset value must be maintained.
21	RAMPERRCLR	RAM parity error interrupt clear bit Set to 1 by software to clear the RAMPERRIF flag. 0: No effect 1: Clear the RAMPERRIF interrupt flag
20	PLLRDICLR	PLL ready interrupt clear bit Set to 1 by software to clear the PLLRDIF flag.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		0: No effect 1: Clear the PLLRDIF interrupt flag
19	HSERDICLR	HSE ready interrupt clear bit Set to 1 by software to clear the HSERDIF flag. 0: No effect 1: Clear the HSERDIF interrupt flag
18	HSIRDICLR	HSI ready interrupt clear bit Set to 1 by software to clear the HSIRDIF flag. 0: No effect 1: Clear the HSIRDIF interrupt flag
17	Reserved	Reserved, the reset value must be maintained.
16	LSIRDICLR	LSI ready interrupt clear bit Set to 1 by software to clear the LSIRDIF flag. 0: No effect 1: Clear the LSIRDIF interrupt flag
15	Reserved	Reserved, the reset value must be maintained.
14	RAMPERRRSTEN	RAM parity error reset enable 0: No reset generated on RAM parity error 1: Reset generated on RAM parity error
13	RAMPERRIEN	RAM parity error interrupt enable bit Set or cleared by software to enable or disable RAM parity error interrupts. 0: Disable RAM parity error interrupt 1: Enable RAM parity error interrupt
12	PLLRDIEN	PLL ready interrupt enable bit Set or cleared by software to enable or disable PLL ready interrupts. 0: Disable PLL ready interrupt 1: Enable PLL ready interrupt
11	HSERDIEN	HSE ready interrupt enable bit Set or cleared by software to enable or disable HSE ready interrupts. 0: Disable HSE ready interrupt 1: Enable HSE ready interrupt
10	HSIRDIEN	HSI ready interrupt enable bit Set or cleared by software to enable or disable HSI ready interrupts. 0: Disable HSI ready interrupt 1: Enable HSI ready interrup
9	Reserved	Reserved, the reset value must be maintained.
8	LSIRDIEN	LSI ready interrupt enable bit Set or cleared by software to enable or disable LSI ready interrupts. 0: Disable LSI ready interrupt 1: Enable LSI ready interrupt
7	CLKSSIF	Clock security system interrupt flag Set to 1 by hardware when an issue occurs with the external HSE oscillator. 0: No clock security system interrupt due to HSE clock failure

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: Clock security system interrupt due to HSE clock failure
6	Reserved	Reserved, the reset value must be maintained.
5	RAMPERRIF	RAM parity error interrupt flag Set to 1 by hardware when RAMPERRIEN is set and a RAM parity error occurs. This bit is cleared by setting RAMPERRCLR to 1. 1: RAM parity error occurred 0: No RAM parity error occurred
4	PLLRDIF	PLL ready interrupt flag Set to 1 by hardware when PLLRDIEN is set and the PLL clock is ready. This bit is cleared by setting PLLRDICLR to 1. 0: No PLL lock causing clock ready interrupt 1: PLL lock causing clock ready interrupt
3	HSERDIF	HSE ready interrupt flag Set to 1 by hardware when HSERDIEN is set and the external high-speed clock is ready. This bit is cleared by setting HSERDICLR to 1. 0: No HSE oscillator causing clock ready interrupt 1: HSE oscillator causing clock ready interrupt
2	HSIRDIF	HSI ready interrupt flag Set to 1 by hardware when HSIRDIEN is set and the internal high-speed clock is ready. This bit is cleared by setting HSERDICLR to 1. 0: No HSI oscillator causing clock ready interrupt 1: HSI oscillator causing clock ready interrupt
1	Reserved	Reserved, the reset value must be maintained.
0	LSIRDIF	LSI ready interrupt flag Set to 1 by hardware when LSIRDIEN is set and the internal low-speed clock is ready. This bit is cleared by setting LSIRDICLR to 1. 0: No LSI oscillator causing clock ready interrupt 1: LSI oscillator causing clock ready interrupt

4.3.5 APB2 Peripheral Reset Register (RCC_APB2PRST)

Address offset: 0x0C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TIM5RST	TIM4RST	TIM3RST
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2 RST	UART1 RST	TIM2RST	TIM1RST	SPI3RST	SPI2RST	SPI1RST	Reserved			IOPDRST	IOPCRST	IOPBRST	IOPARST	Reserved	AFIORST
rw	rw	rw	rw	rw	rw	rw				rw	rw	rw	rw		rw

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	TIM5RST	TIM5 timer reset Set or cleared by software. 0: Clear reset 1: Reset TIM5
17	TIM4RST	TIM4 timer reset Set or cleared by software. 0: Clear reset 1: Reset TIM4
16	TIM3RST	TIM3 timer reset Set or cleared by software. 0: Clear reset 1: Reset TIM3
15	UART2RST	UART2 reset Set or cleared by software. 0: Clear reset 1: Reset UART2
14	UART1RST	UART1 reset Set or cleared by software. 0: Clear reset 1: Reset UART1
13	TIM2RST	TIM2 timer reset Set or cleared by software. 0: Clear reset 1: Reset TIM2
12	TIM1RST	TIM1 timer reset Set or cleared by software. 0: Clear reset 1: Reset TIM1
11	SPI3RST	SPI3 reset Set or cleared by software. 0: Clear reset 1: Reset SPI3
10	SPI2RST	SPI2 reset Set or cleared by software. 0: Clear reset 1: Reset SPI2
9	SPI1RST	SPI1 reset Set or cleared by software. 0: Clear reset 1: Reset SPI1
8:6	Reserved	Reserved, the reset value must be maintained.
5	IOPDRST	GPIO port D reset

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		Set or cleared by software. 0: Clear reset 1: Reset GPIO Port D
4	IOPCRST	GPIO port C reset Set or cleared by software. 0: Clear reset 1: Reset GPIO Port C
3	IOPBRST	GPIO port B reset Set or cleared by software. 0: Clear reset 1: Reset GPIO Port B
2	IOPARST	GPIO port A reset Set or cleared by software. 0: Clear reset 1: Reset GPIO Port A
1	Reserved	Reserved, the reset value must be maintained.
0	AFIORST	Alternate function IO reset Set or cleared by software. 0: Clear reset 1: Reset alternate function IO

4.3.6 APB1 Peripheral Reset Register (RCC_APB1PRST)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			PWRRST	DACRST	CANRST	Reserved			I2C2RST	I2C1RST	UART5 RST	UART4 RST	UART3 RST	Reserved	
			rw	rw	rw				rw	rw	rw	rw	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WWDG RST	LCDRST	Reserved	COMP RST	Reserved		BEEPRST	TIM6RST	Reserved			
				rw	rw		rw			rw	rw				

Bit Field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	PWRRST	PWR reset Set or cleared by software. 0: Clear reset 1: Reset PWR
27	DACRST	DAC reset Set or cleared by software. 0: Clear reset

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: Reset DAC
26	CANRST	CAN reset Set or cleared by software. 0: Clear reset 1: Reset CAN
25:23	Reserved	Reserved, the reset value must be maintained.
22	I2C2RST	I^2C2 reset Set or cleared by software. 0: Clear reset 1: Reset I2C2
21	I2C1RST	I^2C1 reset Set or cleared by software. 0: Clear reset 1: Reset I2C1
20	UART5RST	UART5 reset Set or cleared by software. 0: Clear reset 1: Reset UART5
19	UART4RST	UART4 reset Set or cleared by software. 0: Clear reset 1: Reset UART4
18	UART3RST	UART3 reset Set or cleared by software. 0: Clear reset 1: Reset UART3
17:12	Reserved	Reserved, the reset value must be maintained.
11	WWDGRST	Window Watchdog reset Set or cleared by software. 0: Clear reset 1: Reset Window Watchdog
10	LCDRST	LCD reset Set or cleared by software. 0: Clear reset 1: Reset LCD
9	Reserved	Reserved, the reset value must be maintained.
8	COMPRST	COMP reset Set or cleared by software. 0: Clear reset 1: Reset COMP
7:6	Reserved	Reserved, the reset value must be maintained.
5	BEEPRST	Beeper reset Set or cleared by software.

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Bit Field	Name	Description
		0: Clear reset 1: Reset Beeper
4	TIM6RST	TIM6 Timer reset Set or cleared by software. 0: Clear reset 1: Reset TIM6 Timer
3:0	Reserved	Reserved, the reset value must be maintained.

4.3.7 AHB Peripheral Clock Enable Register (RCC_AHBPCLKEN)

Address offset: 0x14

Reset value: 0x0000 0014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ADCEN	SACEN	Reserved				CRCEN	Reserved	FLITFEN	Reserved	SRAMEN	Reserved	DMAEN
			rw	rw					rw		rw		rw		rw

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCEN	ADC clock enable Set or cleared by software. 0: Disable ADC clock 1: Enable ADC clock
11	SACEN	SAC clock enable Set or cleared by software. 0: Disable SAC clock 1: Enable SAC clock
10:7	Reserved	Reserved, the reset value must be maintained.
6	CRCEN	CRC clock enable Set or cleared by software. 0: Disable CRC clock 1: Enable CRC clock
5	Reserved	Reserved, the reset value must be maintained.
4	FLITFEN	Flash interface clock enable in SLEEP mode Set or cleared by software. 0: Disable Flash interface clock in SLEEP mode 1: Enable Flash interface clock in SLEEP mode
3	Reserved	Reserved, the reset value must be maintained.
2	SRAMEN	SRAM interface clock enable in SLEEP mode

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Bit Field	Name	Description
		Set or cleared by software. 0: Disable SRAM interface clock in SLEEP mode 1: Enable SRAM interface clock in SLEEP mode
1	Reserved	Reserved, the reset value must be maintained.
0	DMAEN	DMA clock enable Set or cleared by software. 0: Disable DMA clock 1: Enable DMA clock

4.3.8 APB2 Peripheral Clock Enable Register (RCC_APB2PCLKEN)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TIM5EN	TIM4EN	TIM3EN
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2 EN	UART1 EN	TIM2EN	TIM1EN	SPI3EN	SPI2EN	SPI1EN	Reserved			IOPDEN	IOPCEN	IOPBEN	IOPAEN	Reserved	AFIOEN
rw	rw	rw	rw	rw	rw	rw				rw	rw	rw	rw		rw

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	TIM5EN	TIM5 timer clock enable Set or cleared by software. 0: Disable TIM5 timer clock 1: Enable TIM5 timer clock
17	TIM4EN	TIM4 timer clock enable Set or cleared by software. 0: Disable TIM4 timer clock 1: Enable TIM4 timer clock
16	TIM3EN	TIM3 timer clock enable Set or cleared by software. 0: Disable TIM3 timer clock 1: Enable TIM3 timer clock
15	UART2EN	UART2 clock enable Set or cleared by software. 0: Disable UART2 clock 1: Enable UART2 clock
14	UART1EN	UART1 clock enable Set or cleared by software. 0: Disable UART1 clock

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Bit Field	Name	Description
		1: Enable UART1 clock
13	TIM2EN	TIM2 timer clock enable Set or cleared by software. 0: Disable TIM2 timer clock 1: Enable TIM2 timer clock
12	TIM1EN	TIM1 timer clock enable Set or cleared by software. 0: Disable TIM1 timer clock 1: Enable TIM1 timer clock
11	SPI3EN	SPI3 clock enable Set or cleared by software. 0: Disable SPI3 clock 1: Enable SPI3 clock
10	SPI2EN	SPI2 clock enable Set or cleared by software. 0: Disable SPI2 clock 1: Enable SPI2 clock
9	SPI1EN	SPI1 clock enable Set or cleared by software. 0: Disable SPI1 clock 1: Enable SPI1 clock
8:6	Reserved	Reserved, the reset value must be maintained.
5	IOPDEN	GPIO port D clock enable Set or cleared by software. 0: Disable GPIO Port D clock 1: Enable GPIO Port D clock
4	IOPCEN	GPIO port C clock enable Set or cleared by software. 0: Disable GPIO Port C clock 1: Enable GPIO Port C clock
3	IOPBEN	GPIO port B clock enable Set or cleared by software. 0: Disable GPIO Port B clock 1: Enable GPIO Port B clock
2	IOPAEN	GPIO port A clock enable Set or cleared by software. 0: Disable GPIO Port A clock 1: Enable GPIO Port A clock
1	Reserved	Reserved, the reset value must be maintained.
0	AFIOEN	Alternate function IO clock enable Set or cleared by software. 0: Disable alternate function IO clock 1: Enable alternate function IO clock

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4.3.9 APB1 Peripheral Clock Enable Register (RCC_APB1PCLKEN)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			PWREN	DACEN	CANEN	Reserved			I2C2EN	I2C1EN	UART5 EN	UART4 EN	UART3 EN	Reserved	
			rw	rw	rw				rw	rw	rw	rw	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WWDG EN	LCDEN	COMP FILTEN	COMPEN	Reserved		BEEPEN	TIM6EN	Reserved			
				rw	rw	rw	rw			rw	rw				

Bit Field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	PWREN	Power interface clock enable Set or cleared by software. 0: Disable power interface clock 1: Enable power interface clock
27	DACEN	DAC clock enable Set or cleared by software. 0: Disable DAC clock 1: Enable DAC clock
26	CANEN	CAN clock enable Set or cleared by software. 0: Disable CAN clock 1: Enable CAN clock
25:23	Reserved	Reserved, the reset value must be maintained.
22	I2C2EN	I^2C2 clock enable Set or cleared by software. 0: Disable I2C2 clock 1: Enable I2C2 clock
21	I2C1EN	I^2C1 clock enable Set or cleared by software. 0: Disable I2C1 clock 1: Enable I2C1 clock
20	UART5EN	UART5 clock enable Set or cleared by software. 0: Disable UART5 clock 1: Enable UART5 clock
19	UART4EN	UART4 clock enable Set or cleared by software. 0: Disable UART4 clock

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Bit Field	Name	Description
		1: Enable UART4 clock
18	UART3EN	UART3 clock enable Set or cleared by software. 0: Disable UART3 clock 1: Enable UART3 clock
17:12	Reserved	Reserved, the reset value must be maintained.
11	WWDGEN	Window Watchdog clock enable Set or cleared by software. 0: Disable Window Watchdog clock 1: Enable Window Watchdog clock
10	LCDEN	LCD clock enable Set or cleared by software. 0: Disable LCD clock 1: Enable LCD clock
9	COMPFILTEN	Comparator filter clock enable 0: Disable Comparator Filter clock 1: Enable Comparator Filter clock
8	COMPEN	Comparator clock enable 0: Disable Comparator clock 1: Enable Comparator clock
7:6	Reserved	Reserved, the reset value must be maintained.
5	BEEPEN	Beeper clock enable 0: Disable Beeper clock 1: Enable Beeper clock
4	TIM6EN	TIM6 timer clock enable Set or cleared by software. 0: Disable TIM6 timer clock 1: Enable TIM6 timer clock
3:0	Reserved	Reserved, the reset value must be maintained.

4.3.10 Low Speed Clock Control Register (RCC_LSCTRL)

Address offset: 0x20

Reset value: 0x0000 0043

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
		r													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	RTCRST	RTCEN	RTCSEL[1:0]		Reserved				LSITRIM[4:0]					LSIRDF	LSIEN
	rw	rw	rw								rw			r	rw

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	RTCRST	RTC software reset Set or cleared by software. 0: Clear reset 1: Reset RTC
13	RTCEN	RTC clock enable Set or cleared by software. 0: Disable RTC clock 1: Enable RTC clock
12:11	RTCSEL[1:0]	RTC clock source selection These bits are set by software to select the RTC clock source. 00: No clock 01: Select LSI oscillator as the RTC clock 10: Select HSE oscillator divided by 128 as the RTC clock 11: Select HSI oscillator divided by 128 as the RTC clock
10:7	Reserved	Reserved, the reset value must be maintained.
6:2	LSITRIM[4:0]	Internal low-speed clock calibration value Written by software to calibrate the frequency of the internal LSI RC oscillator. Default value is 16, with an adjustment step size of 720 Hz. Setting value (rounded) = Current Value – (Measured LSI Frequency – Target Frequency 32,000 Hz) / (Step Size 720 Hz).
1	LSIRDF	Internal low-speed oscillator ready Set or cleared by hardware to indicate whether the LSI oscillator is ready. After the LSIEN bit is cleared, this bit requires 3 internal low-speed oscillator cycles to be cleared. 0: LSI not ready 1: LSI ready
0	LSIEN	Internal low-speed oscillator enable bit Set or cleared by software. 0: Disable LSI oscillator 1: Enable LSI oscillator

4.3.11 Control/Status Register (RCC_CTRLSTS)

Address offset: 0x24

Reset value: 0x0000 0018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		LVRRSTF	Reserved												
		r													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LKUP RSTF	EMCGB RSTF	EMCGBN RSTF	LPWR RSTF	WWDG RSTF	IWDG RSTF	SFTRSTF	PORRSTF	PINRSTF	MMU RSTF	RAMP ERRRSTF	RMRSTF
				r	r	r	r	r	r	r	r	r	r	r	rw

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	LVRRSTF	Low voltage reset flag Set to 1 by hardware during a low voltage reset. Cleared by writing to the RMRSTF bit. 0: No low voltage reset occurred 1: Low voltage reset occurred
29:12	Reserved	Reserved, the reset value must be maintained.
11	LKUPRSTF	M0 core lockup reset flag Set to 1 by hardware during an M0 core lockup reset. Cleared by writing to the RMRSTF bit. 0: No M0 core lockup reset occurred 1: M0 core lockup reset occurred
10	EMCGBRSTF	EMCGB reset flag Set to 1 by hardware during an EMCGB reset. Cleared by writing to the RMRSTF bit. 0: No EMCGB reset occurred 1: EMCGB reset occurred
9	EMCGBNRSTF	EMCGBN reset flag Set to 1 by hardware during an EMCGBN reset. Cleared by writing to the RMRSTF bit. 0: No EMCGBN reset occurred 1: EMCGBN reset occurred
8	LPWRRSTF	Low-power reset flag Set to 1 by hardware during a low-power reset. Cleared by writing to the RMRSTF bit. 0: No low-power reset occurred 1: Low-power reset occurred
7	WWDGRSTF	Window Watchdog reset flag Set to 1 by hardware during a window watchdog reset. Cleared by writing to the RMRSTF bit. 0: No window watchdog reset occurred 1: Window watchdog reset occurred
6	IWDGRSTF	Independent Watchdog reset flag Set to 1 by hardware during an independent watchdog reset. Cleared by writing to the RMRSTF bit. 0: No independent watchdog reset occurred 1: Independent watchdog reset occurred
5	SFTRSTF	Software reset flag Set to 1 by hardware during a software reset. Cleared by writing to the RMRSTF bit. 0: No software reset occurred 1: Software reset occurred
4	PORRSTF	POR/PDR reset flag

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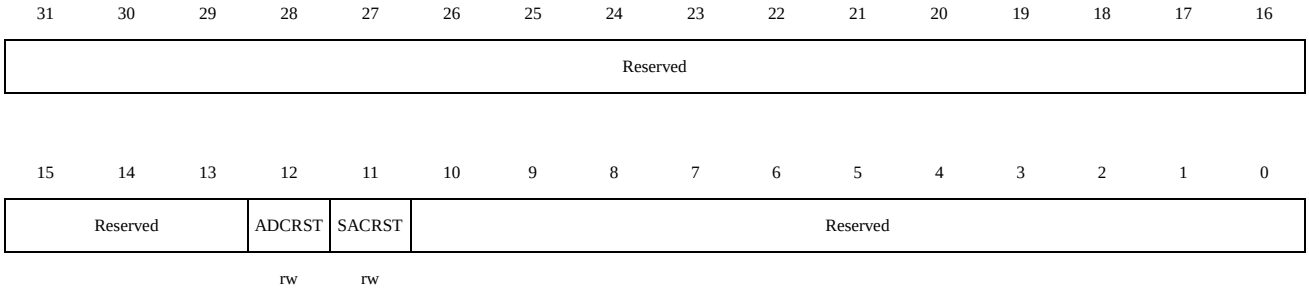
Bit Field	Name	Description
		Set to 1 by hardware during a POR/PDR reset. Cleared by writing to the RMRSTF bit. 0: No POR/PDR reset occurred 1: POR/PDR reset occurred
3	PINRSTF	PIN reset flag Set to 1 by hardware during an NRST pin reset. Cleared by writing to the RMRSTF bit. 0: No NRST pin reset occurred 1: NRST pin reset occurred
2	MMURSTF	MMU reset flag Set to 1 by hardware during an MMU reset. Cleared by writing to the RMRSTF bit. 0: No MMU reset occurred 1: MMU reset occurred
1	RAMPERRRSTF	RAM parity error reset flag Set to 1 by hardware during a RAM parity error reset. Cleared by writing to the RMRSTF bit. 0: No RAM parity error reset occurred 1: RAM parity error reset occurred
0	RMRSTF	Clear reset flags This bit is set by software to clear all reset flags. 0: No effect 1: Clear all reset flags

4.3.12 AHB Peripheral Reset Register (RCC_AHBPRST)

Address offset: 0x28

Reset value: 0x0000 0000



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCRST	ADC interface reset Set or cleared by software. 0: Clear reset 1: Reset ADC interface
11	SACRST	SAC interface reset

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Bit Field	Name	Description
		Set or cleared by software. 0: Clear reset 1: Reset SAC interface
10:0	Reserved	Reserved, the reset value must be maintained.

4.3.13 Clock Configuration Register 2(RCC_CFG2)

Address offset: 0x2C

Reset value: 0x00003800

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIM1CLKSEL	TIM6CLKSEL	Reserved		LCDCLKSEL	ADCCLKSEL[1:0]		Reserved								
rw	rw			rw	rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC1MPRE[4:0]					ADC1MSEL	Reserved	ADCPLLPRE[4:0]					ADCHPRE[3:0]			
rw					rw		rw					rw			

BitField	Name	Description
31	TIM1CLKSEL	TIM1 clock source selection This bit is set and cleared by software. 0: If the APB2 prescaler is 1, the TIM1 clock source is PCLK2; otherwise, the TIM1 clock source is PCLK2 ×2. 1: The TIM1 clock source is SYSCLK.
30	TIM6CLKSEL	TIM6 clock source selection This bit is set and cleared by software. 0: If the APB1 prescaler is 1, the TIM6 clock source is PCLK1; otherwise, the TIM6 clock source is PCLK1 ×2. 1: The TIM6 clock source is LSI.
29:28	Reserved	Reserved, the reset value must be maintained.
27	LCDCLKSEL	LCD clock source selection bit This bit is set and cleared by software. 0: Select HSI clock divided by 8. 1: Select HSE clock divided by 16.
26:25	ADCCLKSEL[1:0]	ADC working clock source selection bit This bit is set and cleared by software. 00: Select 24M HSI clock. 01: Select PLL clock. 10: Select HCLK clock. 11: Reserved.
24:16	Reserved	Reserved, the reset value must be maintained.
15:11	ADC1MPRE[4:0]	ADC 1M clock prescaler These bits are set or cleared by software to configure the prescaler for the ADC 1M

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BitField	Name	Description
		clock source. 00000: No division of the ADC 1M clock source. 00001: ADC 1M clock source divided by 2. 00010: ADC 1M clock source divided by 3. ... 11110: ADC 1M clock source divided by 31. 11111: ADC 1M clock source divided by 32.
10	ADC1MSEL	ADC 1M clock source selection Set or cleared by software. 0: Select HSI oscillator clock as the input clock for ADC 1M. 1: Select HSE oscillator clock as the input clock for ADC 1M. Note: Ensure that the HSI is enabled when switching the ADC 1M clock source.
9	Reserved	Reserved, the reset value must be maintained.
8:4	ADCPLLPRE[4:0]	ADC PLL prescaler These bits are set or cleared by software to configure the prescaler from the PLL clock to the ADC. 0xxxx: ADC PLL clock is disabled. 10000: No division of the PLL clock. 10001: PLL clock divided by 2. 10010: PLL clock divided by 4. 10011: PLL clock divided by 6. 10100: PLL clock divided by 8. 10101: PLL clock divided by 10. 10110: PLL clock divided by 12. 10111: PLL clock divided by 16. 11000: PLL clock divided by 32. 11001: PLL clock divided by 64. 11010: PLL clock divided by 128. 11011: PLL clock divided by 256. Other values: PLL clock divided by 256.
3:0	ADCHPRE[3:0]	ADC HCLK prescaler These bits are set or cleared by software to configure the prescaler from the HCLK clock to the ADC. 0000: HCLK clock divided by 1. 0001: HCLK clock divided by 2. 0010: HCLK clock divided by 4. 0011: HCLK clock divided by 6. 0100: HCLK clock divided by 8. 0101: HCLK clock divided by 10. 0110: HCLK clock divided by 12. 0111: HCLK clock divided by 16. 1000: HCLK clock divided by 32. Other values: HCLK clock divided by 32.

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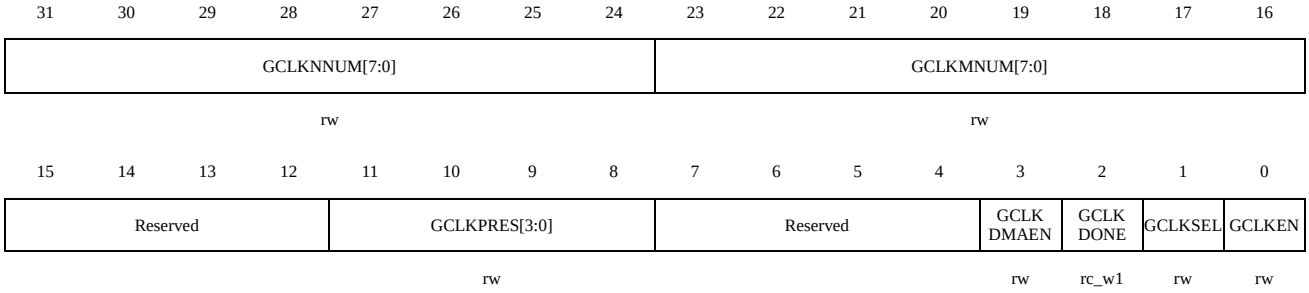
4.3.14 Clock Configuration Register 3 (RCC_CFG3)

Address offset: 0x30

Reset value: 0x7805 0000



BitField	Name	Description
31:24	GCLKNNUM[7:0]	Number of clock cycles in one period Set or cleared by software. See Section 18.3.2 for details. 0x00: N = 0 0x01: N = 1 0x02: N = 2 ... 0xFF: N = 255
23:16	GCLKMNUM[7:0]	Number of low-level clock cycles in one period Set or cleared by software. See Section 18.3.2 for details. 0x00: N = 0 0x01: N = 1 0x02: N = 2 ... 0xFF: N = 255
15:12	Reserved	Reserved, the reset value must be maintained.
11:8	GCLKPRES[3:0]	LED GCLK clock prescaler These bits are set or cleared by software to configure the prescaler for the LED GCLK clock source. 0xxxx: GCLK output disabled 1000: GCLK clock source divided by 32 1001: GCLK clock source divided by 40 1010: GCLK clock source divided by 50 1011: GCLK clock source divided by 64 1100: GCLK clock source divided by 80 1101: GCLK clock source divided by 160 Other values: GCLK clock source divided by 64
7:4	Reserved	Reserved, the reset value must be maintained.
3	GCLKDMAEN	LED GCLK DMA request enable 0: Disable LED GCLK DMA request

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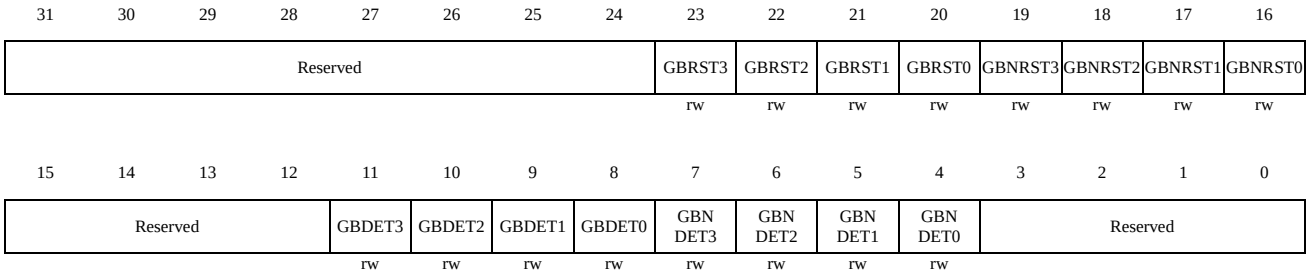
BitField	Name	Description
		1: Enable LED GCLK DMA request
2	GCLKDONE	LED GCLK Clock Output Pulse Count Completion Flag This bit is set by hardware when the number of LED GCLK clock output pulses reaches the configured value M+N. Writing a 1 to this bit clears it. 0: Output pulse count completed 1: Output pulse count not completed
1	GCLKSEL	LED GCLK clock source selection Set or cleared by software. 0: Select HSI clock 1: Select HSE clock
0	GCLKEN	LED GCLK clock enable bit Set or cleared by software. 0: Disable LED GCLK 1: Enable LED GCLK

4.3.15 EMC Control Register (RCC_EMCCTRL)

Address offset: 0x34

Reset value: 0x0000 0000



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	GBRST3	GB3 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
22	GBRST2	GB2 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
21	GBRST1	GB1 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
20	GBRST0	GB0 reset enable

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Bit Field	Name	Description
		This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
19	GBNRST3	GBN3 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
18	GBNRST2	GBN2 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
17	GBNRST1	GBN1 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
16	GBNRST0	GBN0 reset enable This bit is set and cleared by software. 0: Disable reset request 1: Enable reset request
15:12	Reserved	Reserved, the reset value must be maintained.
11	GBDET3	GB3 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
10	GBDET2	GB2 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
9	GBDET1	GB1 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
8	GBDET0	GB0 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
7	GBNDET3	GBN3 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
6	GBNDET2	GBN2 detection enable This bit is set and cleared by software. 0: Disable detection

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Email：info@nationstech.com
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Bit Field	Name	Description
		1: Enable detection
5	GBNDET1	GBN1 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
4	GBNDET0	GBN0 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
3:0	Reserved	Reserved, the reset value must be maintained.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

5 GPIO and AFIO

5.1 Overview

GPIO refers to General Purpose Input/Output, AFIO refers to Alternate Function Input/Output. The chip supports up to 61 GPIOs, divided into four groups (GPIOA/GPIOB/GPIOC/GPIOD), each group having 16 ports for A/B/C and 13 ports for group D. GPIO ports share pins with other multiplexed peripherals, allowing users to configure them flexibly according to their needs. Each GPIO pin can be independently configured as an output, input, or a multiplexed peripheral function port. Apart from analog input pins, all other GPIO pins have the capability to handle high current.

The GPIO main features:

- GPIO ports can be individually configured by software into the following modes
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog
  - Open-drain output with selectable pull-up/pull-down
  - Push-pull output with selectable pull-up/pull-down
  - Push-pull alternate function with selectable pull-up/pull-down
  - Open-drain alternate function with selectable pull-up/pull-down
- Individual bit set/clear function
- All I/O support external interrupt
- All I/O support low-power mode wake-up, with configurable rising or falling edge
  - 16 EXTI_LINEs can be used for wake-up in SLEEP or STOP mode, all I/O can be multiplexed as EXTI_LINEs
  - 3 wake-up I/Os (NRST/PA0/PA2) can be used for waking up in PD mode, with a maximum I/O filtering time of 1us
- Supports software remapping of I/O alternate functions
- Supports GPIO locking mechanism, lock state can be cleared by reset mode

Each I/O port bit can be programmed arbitrarily, but the registers must be accessed in 32-bit words (not allowing 16-bit half-word or 8-bit byte access). The following diagram illustrates the basic structure of an I/O port.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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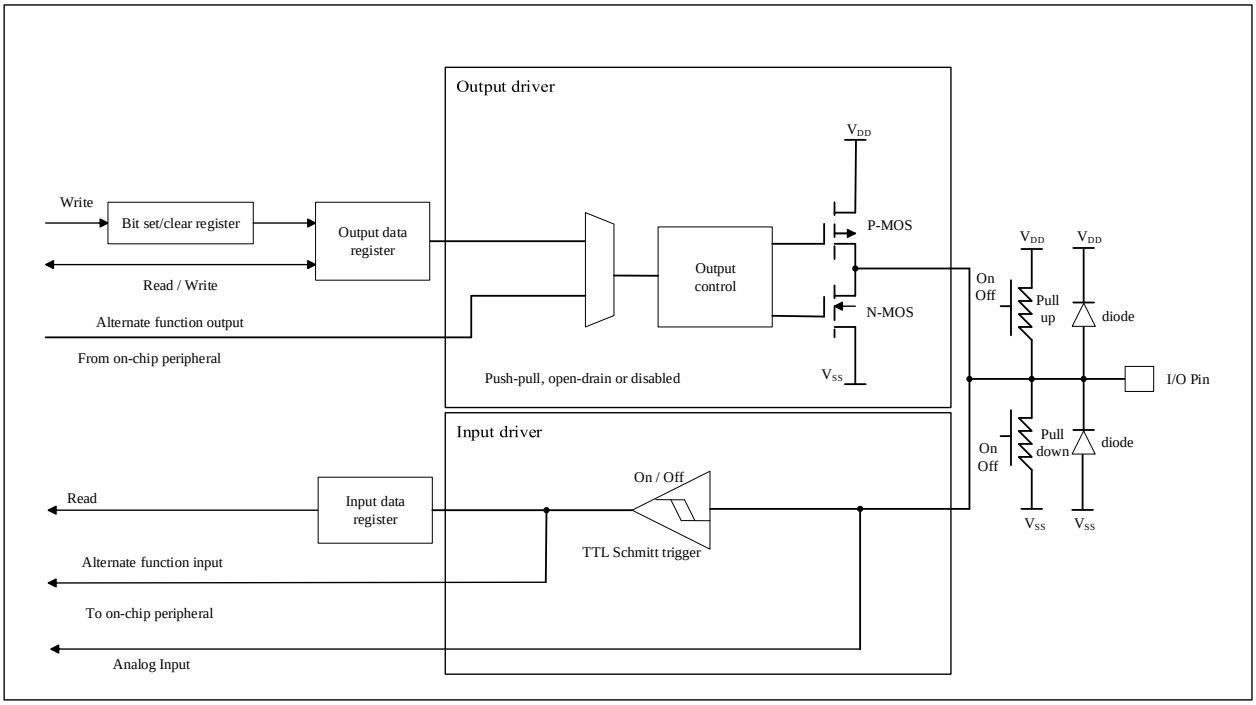
Figure 5-1 Basic Structure of I/O Ports (Fail-safe Not Supported)



5.2 Function Description

5.2.1 IO Mode Configuration

The mode control of I/O is set by configuration registers GPIOx_PMODE, GPIOx_POTYPE, and GPIOx_PUPD (x=A, B, C, D). The configurations for different operating modes are shown in the table below:

Table 5-1 I/O Relationship Between Mode and Configuration

PMODE[1:0]	POTYPE	PUPD[1:0]		I/O Configuration
01	0	0	0	General Output Push-Pull
	0	0	1	General Output Push-Pull + Pull-Up
	0	1	0	General Output Push-Pull + Pull-Down
	0	1	1	Reserved
	1	0	0	General Output Open-Drain
	1	0	1	General Output Open-Drain + Pull-Up
	1	1	0	General Output Open-Drain + Pull-Down
	1	1	1	Reserved
10	0	0	0	Push-Pull alternate function
	0	0	1	Push-Pull alternate function + Pull-Up
	0	1	0	Push-Pull alternate function + Pull-Down
	0	1	1	Reserved
	1	0	0	Open-Drain alternate function
	1	0	1	Open-Drain alternate function + Pull-Up
	1	1	0	Open-Drain alternate function + Pull-Down
	1	1	1	Reserved

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PMODE[1:0]	POTYPE	PUPD[1:0]		I/O Configuration
00	x	0	0	Input Floating
	x	0	1	Input Pull-up
	x	1	0	Input Pull-down
	x	1	1	Reserved
11	x	0	0	Analog mode
	x	0	1	Reserved
	x	1	0	
	x	1	1	

Additionally, the GPIOx_DS.DSy bit can be used to configure high/low drive strength, and the GPIOx_SR.SRy bit can be used to configure high/low slew rate.

The characteristics of I/O under different configurations are shown in the table below:

Table 5-2 Input/Output Characteristics Under Different Configurations

Characteristics	GPIO Input	GPIO Output	Analog	Peripheral alternate function
Output buffer	Disable	Enable	Disable	Configured according to the peripheral function
Schmitt trigger	Enable	Enable	Disable Output is 0	Enable
Pull-up/Pull-down	Configurable	Configurable	Disable	Configured according to the peripheral function
Open-drain	Disable	Configurable， When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO is in high-Z state.	Disable	Configurable， When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO is in high-Z state.
Push-pull	Disable	Configurable， When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO outputs 1.	Disable	Configurable， When the output data is "0", the GPIO outputs 0, and when it is "1", the GPIO outputs 1.
Input Data Register(IO Status)	RO	RO	Read Only 0	Readable
Output Data Register (Output Value)	Invalid	RW	Invalid	Readable

5.2.1.1 Input mode

When the I/O port is configured in input mode:

- Output buffer is disabled
- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register.

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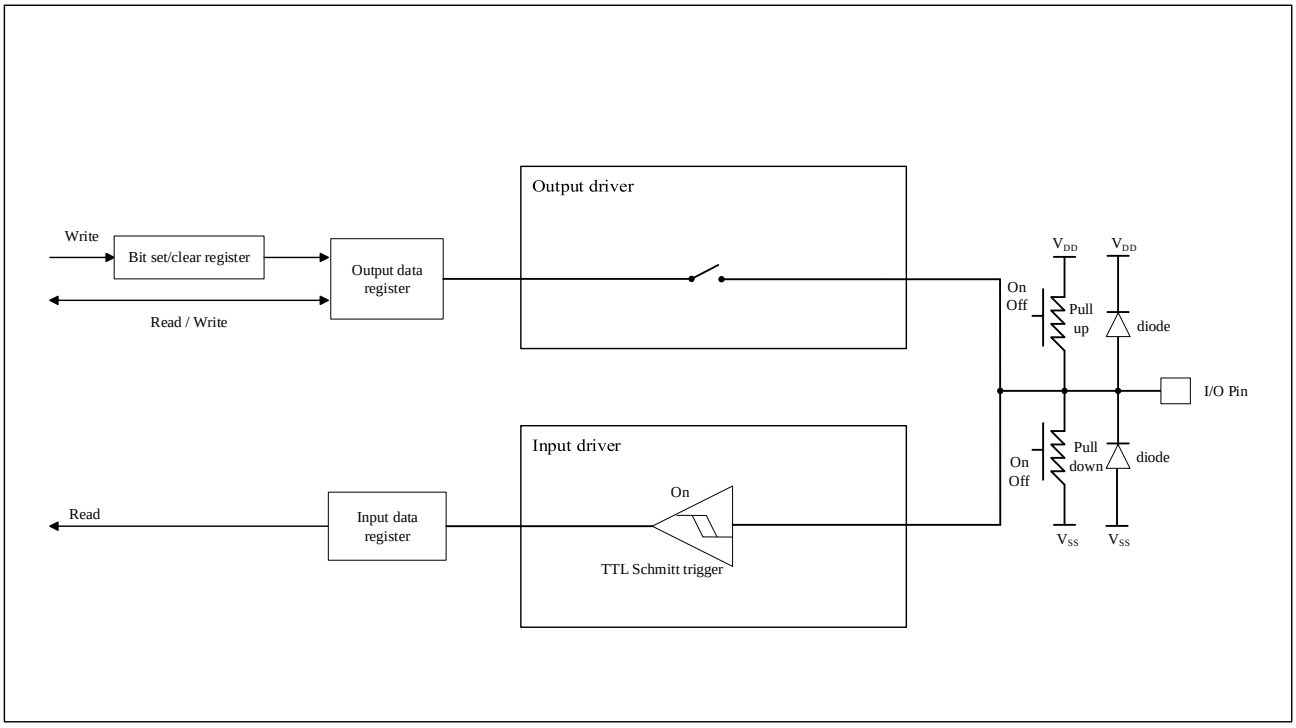
- The data present on the I/O pin is sampled into the input data register at each APB2 clock.
- Reading from the input data register retrieves the I/O status.

Figure 5-2 Input Floating/Pull-Up/Pull-Down Mode (Fail-safe Not Supported)



5.2.1.2 **Output mode**

When the I/O port is configured in output mode:

- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- Output buffer is activated
  - Open-drain mode：

    '0' in the output data register activates the N-MOS, causing the pin to output a low level

    '1' in the output data register puts the port in a high-impedance state (P-MOS is never activated)
  - Push-pull mode：

    '0' in the output data register activates the N-MOS, causing the pin to output a low level

    '1' in the output data register activates the P-MOS, causing the pin to output a high level
- The data present on the I/O pin is sampled into the input data register at each APB2 clock
- Reading from the input data register retrieves the I/O status
- Reading from the output data register retrieves the last written value

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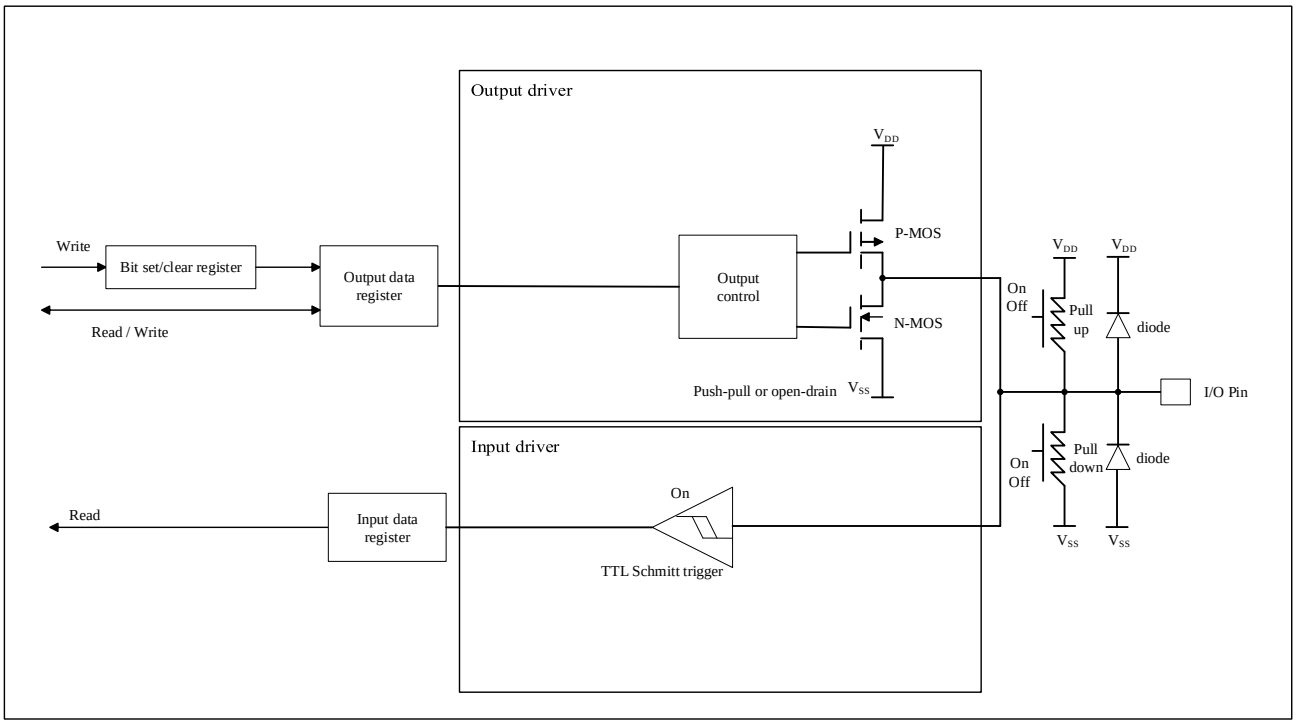
Figure 5-3 Output Mode (Fail-safe Not Supported)



5.2.1.3 **Alternate function mode**

When the I/O port is configured in alternate function mode:

- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- In open-drain or push-pull configurations, the output buffer is controlled by the peripheral
- Built-in peripheral signals drive the output buffer
- At each APB2 clock cycle, the data present on the I/O pins are sampled into the input data register
- Reading from the input data register retrieves the I/O status
- Reading from the output data register retrieves the last written value

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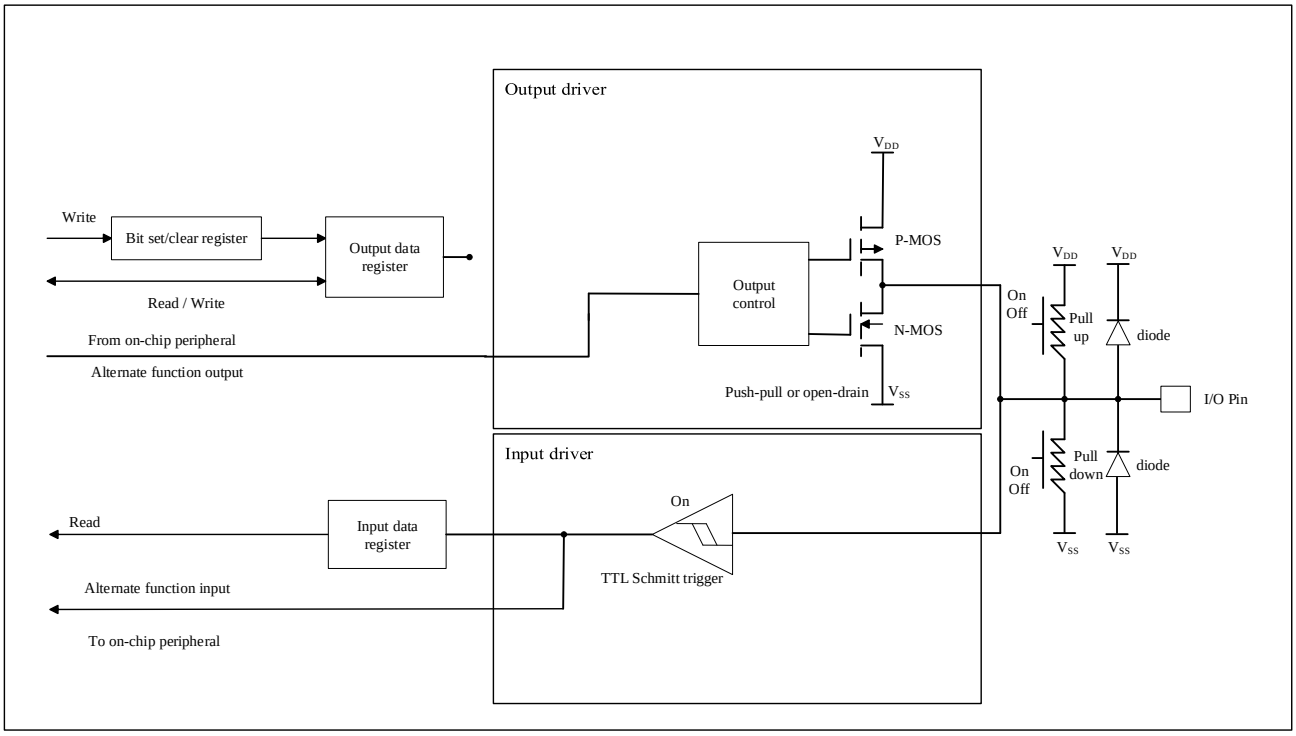
Figure 5-4 Alternate Function Mode (Fail-safe Not Supported)



5.2.1.4 **Analog function mode**

When the I/O port is configured in analog function mode:

- Pull-up and pull-down resistors are disabled
- Reading the input data register yields a value of '0'
- The output buffer is disabled
- Schmitt trigger input is disabled, and the output value is forced to '0' (achieving zero consumption on each analog I/O pin)

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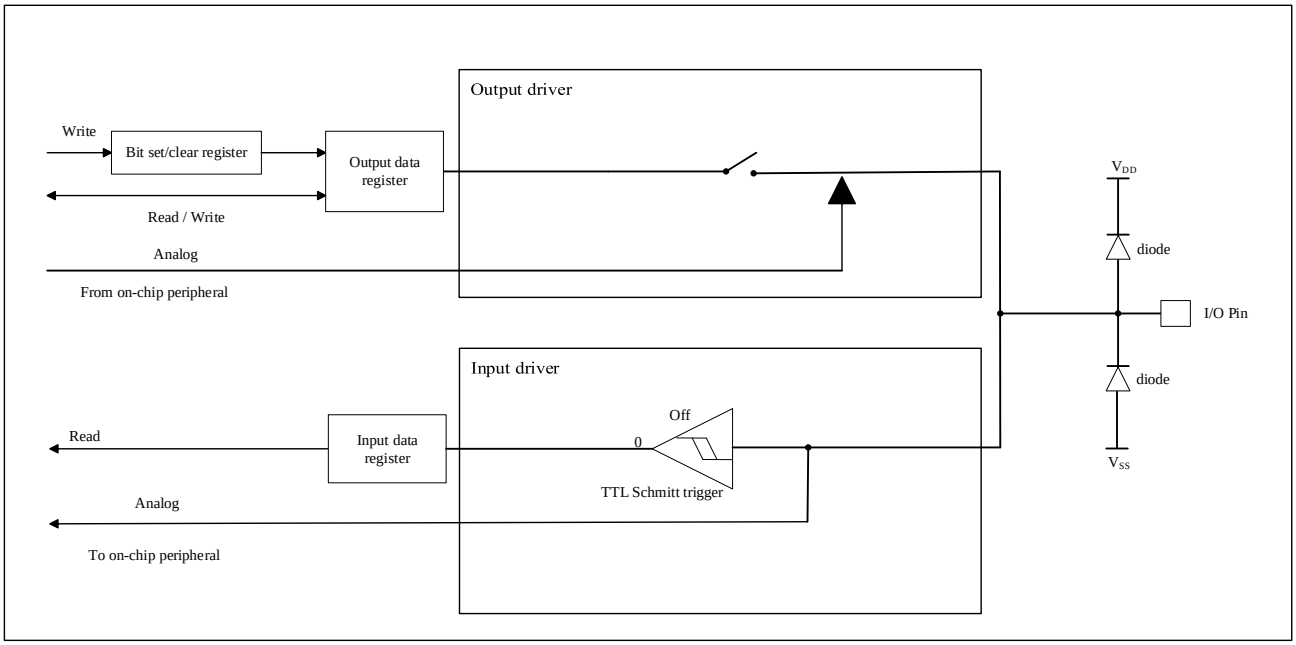
Figure 5-5 High-impedance Analog Function Mode (Fail-safe Not Supported)



5.2.2 Status After Reset

During and immediately after reset, the alternate function is not enabled, and the I/O port is configured in analog function mode.(GPIOx_PMODE.PMODEx[1:0]=2'b11). But there are a few exceptions:

- NRST has no GPIO function by default:
  - NRST is pulled up as an input
- After reset, the pins related to the debug system are configured by default as SWD interface I/O configuration:
  - PA14: SWCLK is set to input pull-down mode
  - PA13: SWDIO is set to input pull-up mode
- PA0/PD14:
  - PA0 and PD14 are set to input floating mode by default
  - PD14 is multiplexed to OSC_IN
- PD0/BOOT0:
  - During chip startup, PD0 functions as BOOT0 by default in pull-down input mode. After chip initialization, it is used as a general GPIO and configured in analog function mode.

5.2.3 Individual Bit Set and Clear

Individual bits in the data register (GPIOx_POD) can be manipulated by writing '1' to the desired bits in the bit set/clear register (GPIOx_PBSC) and bit clear register (GPIOx_PBC). This allows for individual bit operations on one or multiple bits. The bits written as '1' will be set or cleared accordingly, while the bits not written as '1' will remain unchanged. Software does not need to disable interrupts and the operation can be completed in a single APB2 write operation.

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5.2.4 External Interrupt/Wake-up Lines

All ports have external interrupt capability, which can be configured in the EXTI module as follows:

- Ports must be configured in input mode
- All ports can be configured for wake-up in SLEEP/STOP mode, supporting configurable rising or falling edges
- NRST/PA0/PA2 can be used for wake-up in PD mode, with independent wake-up enable for PA0/PA2. All three pins support configurable rising/falling edges and need to be configured before entering PD mode
- General I/O ports are connected to 16 external interrupt/event lines in the manner shown in Figure 6-2, configured by the AFIO_EXTI_CFGx register.

5.2.5 Alternate Function

When the I/O port is configured in alternate function mode, the port bit configuration registers (GPIOx_AFL/GPIOx_AFH, GPIOx_PMODE, GPIOx_POTYPE, and GPIOx_PUPD) must be configured before use. The determination of whether the alternate function is used for input or output is determined by the peripheral.

5.2.5.1 Software remapping I/O alternate function

To enhance the flexibility of multiplexed peripheral functions across different device packages, it is possible to Remapping some peripheral functions to other pins. Each I/O has up to 16 multiplexed functions (AF0~ AF15). After reset, except for PA13 and PA14, AFSELy defaults to AF15. The multiplexed I/O functions can be Remappingped by software configuration of the corresponding registers (GPIOx_AFL/AFH).

At this point, the alternate functions are no longer mapped to their original pins. For the IO Remappingping feature of peripherals, if Remappingped to a different pin, the input is multiplexed to the Remappingped pin, and the output is connected to the Remappingped location, disconnecting the original location.

5.2.5.2 SWD alternate function I/O remapping

Table 5-3 SWD Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SWDIO	PA13	AF0
SWCLK	PA14	AF0

5.2.5.3 TIMx alternate function I/O remapping

5.2.5.3.1 TIM1 alternate function I/O remapping

Table 5-4 TIM1 Alternate Function I/O Remapping

Alternate Function	IO	Remapping
TIM1_ETR	PA12	AF2
	PA14	AF2
	PA15	AF2
TIM1_BKIN	PA1	AF2
	PA5	AF3
	PA11	AF2
TIM1_CH1	PA4	AF2
	PA9	AF2

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Alternate Function	IO	Remapping
	PC12	AF2
	PD4	AF2
TIM1_CH2	PA6	AF2
	PA9	AF1
	PC12	AF1
	PD6	AF2
TIM1_CH3	PA11	AF5
	PD4	AF1
	PD8	AF2
TIM1_CH4	PA10	AF2
	PA13	AF2
	PD4	AF3
TIM1_CH1N	PA5	AF2
	PA7	AF2
	PB13	AF2
	PD5	AF2
TIM1_CH2N	PA6	AF1
	PA7	AF1
	PB14	AF2
	PD7	AF2
TIM1_CH3N	PA4	AF3
	PA9	AF3
	PB15	AF2
	PD9	AF2
TIM1_CH4N	PA11	AF4
	PA14	AF4
	PB12	AF7
	PD12	AF3

5.2.5.3.2 TIM2 alternate function I/O remapping

Table 5-5 TIM2 Alternate Function I/O Remapping

Alternate Function	IO	Remapping
TIM2_ETR	PA5	AF1
	PB9	AF2
TIM2_CH1	PA10	AF1
	PA14	AF1
	PB0	AF2
TIM2_CH2	PA11	AF1
	PB14	AF1
	PD0	AF2
TIM2_CH3	PA12	AF1
	PB12	AF2

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Alternate Function	IO	Remapping
	PC14	AF2
TIM2_CH4	PA13	AF1
	PB6	AF4
	PD14	AF2

5.2.5.3.3 TIM3 alternate function I/O remapping

Table 5-6 TIM3 Alternate Function I/O Remapping

Alternate Function	IO	Remapping
TIM3_ETR	PC5	AF2
	PC13	AF2
TIM3_CH1	PA8	AF1
	PC6	AF2
	PC11	AF2
	PD10	AF2
TIM3_CH2	PA8	AF4
	PC7	AF2
	PC11	AF1
TIM3_CH3	PC8	AF2
	PD5	AF1
	PD12	AF1
TIM3_CH4	PC9	AF2
	PD5	AF0
	PD12	AF2

5.2.5.3.4 TIM4 alternate function I/O remapping

Table 5-7 TIM4 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
TIM4_ETR	PC4	AF2
	PC12	AF3
TIM4_CH1	PA10	AF3
	PB6	AF1
	PC1	AF2
	PD11	AF2
TIM4_CH2	PA10	AF4
	PB7	AF2
	PC1	AF1
TIM4_CH3	PB7	AF1
	PB8	AF2
	PD13	AF2
TIM4_CH4	PB8	AF1
	PB9	AF1
	PD14	AF1

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5.2.5.3.5 TIM5 alternate function I/O remapping

Table 5-8 TIM5 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
TIM5_ETR	PA15	AF1
	PC8	AF1
TIM5_CH1	PA0	AF2
	PA12	AF4
	PA15	AF4
	PB5	AF2
TIM5_CH2	PA1	AF1
	PA12	AF5
	PA15	AF5
	PB5	AF1
TIM5_CH3	PA2	AF2
	PB4	AF2
	PC8	AF3
	PD13	AF1
TIM5_CH4	PA3	AF2
	PB4	AF1
	PC8	AF4
	PD13	AF3

5.2.5.4 UARTx alternate function I/O remapping

5.2.5.4.1 UART1 alternate function I/O remapping

Table 5-9 UART1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART1_TX	PA2	AF5
	PA9	AF5
	PB10	AF2
	PD10	AF4
UART1_RX	PA3	AF5
	PA10	AF5
	PB11	AF2
	PD11	AF4

5.2.5.4.2 UART2 alternate function I/O remapping

Table 5-10 UART2 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART2_TX	PA6	AF4
	PB4	AF6
	PB12	AF6
	PC2	AF6

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Alternate Function	I/O	Remapping
UART2_RX	PA7	AF4
	PB5	AF4
	PB11	AF3
	PC3	AF2

5.2.5.4.3 UART3 alternate function I/O remapping

Table 5-11 UART3 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART3_TX	PA9	AF6
	PB8	AF5
	PC10	AF5
	PD13	AF5
UART3_RX	PA8	AF5
	PB9	AF4
	PC9	AF5
	PD13	AF4

5.2.5.4.4 UART4 alternate function I/O remapping

Table 5-12 UART4 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART4_TX	PA9	AF7
	PA14	AF5
	PD5	AF4
	PD10	AF5
UART4_RX	PA10	AF8
	PA13	AF5
	PD4	AF5
	PD11	AF5

5.2.5.4.5 UART5 alternate function I/O remapping

Table 5-13 UART5 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
UART5_TX	PB8	AF4
	PB14	AF4
	PC12	AF5
	PD8	AF5
UART5_RX	PB9	AF8
	PB15	AF4
	PD5	AF6
	PD9	AF6

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5.2.5.5 I2Cx alternate function I/O remapping

5.2.5.5.1 I²C1 alternate function I/O remapping

Table 5-14 I²C1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
I2C1_SCL	PA4	AF6
	PA8	AF7
	PA12	AF6
	PB8	AF6
	PB10	AF6
	PC0	AF6
	PC5	AF6
	PC6	AF6
	PC13	AF6
	PD12	AF6
	PD15	AF6
I2C1_SDA	PA3	AF6
	PA8	AF8
	PA10	AF6
	PB9	AF6
	PB11	AF6
	PC3	AF6
	PC6	AF7
	PC7	AF6
	PD11	AF6
	PD13	AF6
	PD14	AF6
I2C1_SMBA	PA2	AF1
	PB7	AF6
	PC4	AF1
	PD4	AF6

5.2.5.5.2 I²C2 alternate function I/O remapping

Table 5-15 I²C2 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
I2C2_SCL	PA8	AF3
	PA12	AF7
	PB8	AF7
	PB10	AF7
	PC0	AF7
	PC5	AF7
	PC6	AF5
	PC10	AF6

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Alternate Function	I/O	Remapping
	PC13	AF7
	PD12	AF7
I2C2_SDA	PA8	AF2
	PA10	AF7
	PB9	AF7
	PB11	AF7
	PC11	AF7
	PC3	AF7
	PC6	AF0
	PC7	AF7
	PD11	AF7
	PD13	AF7
I2C2_SMBA	PA13	AF4
	PB13	AF0
	PC8	AF6
	PC9	AF6

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5.2.5.6 SPIx alternate function I/O remapping

5.2.5.6.1 SPI1 alternate function I/O remapping

Table 5-16 SPI1 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SPI1_ NSS	PB9	AF0
	PD0	AF0
	PD7	AF0
SPI1_ SCK	PA12	AF0
	PB10	AF0
	PB12	AF0
	PC0	AF0
	PC5	AF0
	PD6	AF0
SPI1_ MISO	PA9	AF0
	PB11	AF0
	PB12	AF5
	PC2	AF0
	PC7	AF0
	PD5	AF5
SPI1_MOSI	PA10	AF0
	PB10	AF5
	PB11	AF5
	PC3	AF0
	PC6	AF1
	PD4	AF0

5.2.5.6.2 SPI2 alternate function I/O remapping

Table 5-17 SPI2 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SPI2_ NSS	PB9	AF5
	PC1	AF0
	PC4	AF0
SPI2_ SCK	PB10	AF1
	PC0	AF1
	PC5	AF1
	PC13	AF0
SPI2_ MISO	PB12	AF1
	PC2	AF1
	PC3	AF1
	PC7	AF1
	PD10	AF1

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SPI2_MOSI	PB11	AF1
	PC2	AF5
	PC3	AF5
	PC6	AF4
	PD11	AF0

5.2.5.6.3 SPI3 alternate function I/O remapping

Table 5-18 SPI3 Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
SPI3_ NSS	PA7	AF0
	PC1	AF5
	PD2	AF0
	PD12	AF0
SPI3_ SCK	PA8	AF6
	PB10	AF4
	PC0	AF4
	PC5	AF4
SPI3_ MISO	PA1	AF0
	PA7	AF8
	PB12	AF4
	PC2	AF4
	PC7	AF4
	PD13	AF0
SPI3_MOSI	PA0	AF4
	PA9	AF4
	PB11	AF4
	PC3	AF4
	PC6	AF3

5.2.5.7 CAN alternate function I/O remapping

Table 5-19 CAN Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
CAN_RX	PA3	AF7
	PA12	AF8
	PD8	AF7
CAN_TX	PA4	AF7
	PA11	AF8
	PB3	AF4
	PD9	AF7

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5.2.5.8 COMPx alternate function I/O remapping

Table 5-20 COMP Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
COMP1_OUT	PB6	AF5
COMP1_OUT	PB8	AF8
COMP2_OUT	PA7	AF6
COMP2_OUT	PB9	AF9
COMP3_OUT	PA10	AF9
COMP3_OUT	PB4	AF5
COMP4_OUT	PC5	AF5
COMP4_OUT	PC10	AF4

5.2.5.9 BEEPER alternate function I/O remapping

Table 5-21 BEEPER Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
BEEPER_OUT1	PA13	AF7
BEEPER_OUT2	PB14	AF7
BEEPER_OUT3	PC11	AF6

5.2.5.10 RTC alternate function I/O remapping

Table 5-22 RTC Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
TAMPER1	PC13	AF3
TAMPER2	PA0	AF7
TAMPER3	PB8	AF3
RTC_REFCLK	PA1/PB15	AF7

Notes: External pull-up/pull-down resistors are required for the TAMPER pins.

5.2.5.11 LCD alternate function I/O remapping

Table 5-23 LCD Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
LCD_COM0	PD4	AF9
LCD_COM1	PD5	AF9
LCD_COM2	PD6	AF9
LCD_COM3/ LCD_SEG36	PD7	AF8
LCD_COM4/ LCD_SEG35	PD8	AF8
LCD_COM5/ LCD_SEG34	PD9	AF8
LCD_COM6/ LCD_SEG33	PD10	AF8
LCD_COM7/ LCD_SEG32	PD11	AF8
LCD_SEG0	PB0	AF7
LCD_SEG1	PB1	AF7
LCD_SEG2	PB2	AF7

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LCD_SEG3	PB10	AF9
LCD_SEG4	PB11	AF9
LCD_SEG5	PB12	AF9
LCD_SEG6	PD0	AF7
LCD_SEG7	PA14	AF8
LCD_SEG8	PA13	AF8
LCD_SEG9	PB14	AF9
LCD_SEG10	PB15	AF9
LCD_SEG11	PC8	AF8
LCD_SEG12	PA15	AF8
LCD_SEG13	PB4	AF9
LCD_SEG14	PB5	AF9
LCD_SEG15	PB6	AF9
LCD_SEG16	PB8	AF9
LCD_SEG17	PB9	AF10
LCD_SEG18	PC4	AF8
LCD_SEG19	PB7	AF9
LCD_SEG20	PC11	AF8
LCD_SEG21	PC10	AF8
LCD_SEG22	PC9	AF8
LCD_SEG23	PC5	AF8
LCD_SEG24	PC6	AF8
LCD_SEG25	PC7	AF8
LCD_SEG26	PC2	AF8
LCD_SEG27	PC3	AF8
LCD_SEG28	PC0	AF8
LCD_SEG29	PC1	AF8
LCD_SEG30	PC12	AF8
LCD_SEG31	PC13	AF8

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5.2.5.12 EVENT_OUT alternate function I/O remapping

Table 5-24 EVENTOUT Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
EVENT_OUT	PA1	AF3
	PA6	AF3
	PA7	AF3
	PA11	AF3
	PA12	AF3
	PA15	AF3
	PB0	AF3
	PB3	AF3
	PB4	AF3
	PB9	AF3
	PB10	AF3
	PB12	AF3
	PC0	AF3
	PC1	AF3
	PC2	AF3
	PC3	AF3
	PC4	AF3
	PD4	AF4
	PD5	AF3

5.2.5.13 MCO alternate function I/O remapping

Table 5-25 RCC Alternate Function I/O Remapping

Alternate Function	I/O	Remapping
MCO	PA13	AF6
	PB3	AF6
	PB14	AF6

5.2.5.14 ADC alternate function I/O remapping

External trigger sources for ADC regular conversions support PX0~PX15 (X=A、B、C、D).

5.2.6 I/O Configuration of Peripherals

Table 5-26 ADC

ADC	GPIO Configuration
ADC	Analog function mode

Table 5-27 LED

LED Pins	Configuration	GPIO Configuration
LED_COMx (x=0~9)	LED common output	Analog mode
LED_SEGx (x=0~15)	LED segment output	Analog mode
LED_GCLK	LED clock input	Push-pull alternate function

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Table 5-28 LCD

LCD Pins	Configuration	GPIO Configuration
LCD_COMx (x=0~7)	LCD common output	Analog mode + Alternate function
LCD_SEGx (x=0~36)	LCD segment output	Analog mode + Alternate function

Table 5-29 TIM1

TIM1 Pins	Configuration	GPIO Configuration
TIM1_CHx	Input capture channel x	Push-pull alternate function
	Output compare channel x	Push-pull alternate function
TIM1_CHxN	Complementary output channel x	Push-pull alternate function
TIM1_BKIN	Brake input	Push-pull alternate function
TIM1_ETR	External trigger clock input	Push-pull alternate function

Table 5-30 TIM2/3/4/5

TIM2/3/4/5 Pins	Configuration	GPIO Configuration
TIMx_CHx	Input capture channel x	Push-pull alternate function
	Output compare channel x	Push-pull alternate function
TIMx_ETR	External trigger clock input	Push-pull alternate function

Table 5-31 UART

UART Pins	Configuration	GPIO Configuration
UARTx_TX	Full-duplex mode	Push-pull alternate function
	Half-duplex synchronous mode	Push-pull alternate function + pull up
UARTx_RX	Full-duplex mode	Push-pull alternate function
	Half-duplex synchronous mode	Not used, can be used as general I/O

Table 5-32 I^2C

I^2C Pins	Configuration	GPIO Configuration
I2Cx_SCL	I^2C clock	Open-drain alternate function
I2Cx_SDA	I^2C data	Open-drain alternate function

Table 5-33 SPI

SPI Pins	Configuration	GPIO Configuration
SPIx_SCK	Master mode	Push-pull alternate function
	Slave mode	Push-pull alternate function
SPIx_MOSI	Full-duplex mode / master mode	Push-pull alternate function
	Full-duplex mode / slave mode	Push-pull alternate function
	Single-wire bidirectional data line / master mode	Push-pull alternate function
	Single-wire bidirectional data line / slave mode	Not used, can be used as general I/O
SPIx_MISO	Full-duplex mode / master mode	Push-pull alternate function
	Full-duplex mode / slave mode	Push-pull alternate function
	Single-wire bidirectional data line / master mode	Not used, can be used as general I/O
	Single-wire bidirectional data line / slave mode	Push-pull alternate function
SPIx_NSS	Hardware master/slave mode	Push-pull alternate function

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SPI Pins	Configuration	GPIO Configuration
	Software mode	Not used, can be used as general I/O

Table 5-34 CAN

CAN Pins	Configuration	GPIO Configuration
CAN_TX	CAN transmit	Push-pull alternate function
CAN_RX	CAN receive	Push-pull alternate function

Table 5-35 COMP

COMPx Pins	Configuration	GPIO Configuration
COMPx_OUT	COMP output	Push-pull alternate function
COMPx_INM	COMP negative input.	Analog mode
COMPx_INP	COMP positive input	Analog mode

Table 5-36 RTC

RTC Pins	Configuration	GPIO Configuration
RTC_REFCLK	Reference clock input	Push-pull alternate function

Table 5-37 BEEPER

BEEPER Pins	Configuration	GPIO Configuration
BEEPER_OUTx	BEEPER output	Push-pull alternate function

Table 5-38 Others

Pins	Configuration	GPIO Configuration
MCO	Clock output	Push-pull alternate function
EXTI lines	External interrupt input	Floating input + pull-up/pull-down

5.2.7 GPIO Locking Mechanism

The locking mechanism is used to freeze the IO configuration to prevent accidental changes. When a lock (LOCK) operation is performed on a port bit, the configuration of the port cannot be changed until the next reset, referring to the port configuration locking register GPIOx_PLOCK.

- GPIOx_PLOCK.PLOCKK bit will only become 1 after the correct sequence of operations w1->w0->w1->r0 (here r0 must be included); thereafter, it will only become 0 after a system reset.
- GPIOx_PLOCK.PLOCKK must be 0, indicating unlocked, in order to modify GPIOx_PLOCK.PLOCK[15:0].
- GPIOx_PLOCK.PLOCK will only be effective when writing simultaneously with a non-zero value to GPIOx_PLOCK.PLOCK[15:0] in the sequence w1->w0->w1->r0; during the sequence write, GPIOx_PLOCK.PLOCK[15:0] must not change.
- As long as GPIOx_PLOCK.PLOCKK = 0, the bits of GPIOx_PMODE / GPIOx_POTYPE / GPIOx_PUPD / GPIOx_AFL / GPIOx_AFH can be modified, unaffected by the configuration of GPIOx_PLOCK.PLOCK[15:0].
- When GPIOx_PLOCK.PLOCKK = 1, GPIOx_PMODE / GPIOx_POTYPE / GPIOx_PUPD / GPIOx_AFL / GPIOx_AFH are controlled by GPIOx_PLOCK.PLOCK[15:0]. When GPIOx_PLOCK.PLOCKy (y = 0…15) = 1, the configuration is locked and cannot be modified; when PLOCKy = 0, it can be modified.
- If the sequence operation is incorrect, the lock operation must be re-initiated with w1->w0->w1->r0.

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5.3 GPIO Registers

These peripheral registers must be accessed in 32-bit words.

5.3.1 GPIO Register Overview

GPIOA Base Address：0x4001 0800

GPIOB Base Address：0x4001 0C00

GPIOC Base Address：0x4001 1000

GPIOD Base Address：0x4001 1C00

Table 5-39 GPIO Register Overvie

Offset	Register		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	GPIOx_PMODE	x=A,B,C,D	PMODE15[1:0]		PMODE14[1:0]		PMODE13[1:0]		PMODE12[1:0]		PMODE11[1:0]		PMODE10[1:0]		PMODE9[1:0]		PMODE8[1:0]		PMODE7[1:0]		PMODE6[1:0]		PMODE5[1:0]		PMODE4[1:0]		PMODE3[1:0]		PMODE2[1:0]		PMODE1[1:0]		PMODE0[1:0]	
	Reset Value	x=A	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		x=B,C,D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
004h	GPIOx_POTYPE	x=A,B,C,D	Reserved																POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
	Reset Value	x=A,B,C,D	Reserved																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
080h	GPIOx_SR	x=A,B,C,D	Reserved																SR15	SR16	SR17	SR18	SR19	SR20	SR21	SR22	SR23	SR24	SR25	SR26	SR27	SR28	SR29	SR30
	Reset Value	x=A,B,C,D	Reserved																1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
00Ch	GPIOx_PUPD	x=A,B,C,D	PUPD15		PUPD14		PUPD13		PUPD12		PUPD11		PUPD10		PUPD9		PUPD8		PUPD7		PUPD6		PUPD5		PUPD4		PUPD3		PUPD2		PUPD1		PUPD0	
	Reset Value	x=A	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		x=B,C,D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	GPIOx_PID	x=A,B,C,D	Reserved																PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
	Reset Value	x=A,B,C,D	Reserved																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	GPIOx_POD	x=A,B,C,D	Reserved																POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
	Reset Value	x=A,B,C,D	Reserved																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	GPIOx_PBSC	x=A,B,C,D	PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0	PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0

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	Reset Value	x=A,B,C,D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	GPIOx_PLOCK	x=A,B,C,D	Reserved																PLOCKK	PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
	Reset Value	x=A,B,C,D	Reserved																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	GPIOx_AFL	x=A,B,C,D	AFSEL7[3:0]				AFSEL6[3:0]				AFSEL5[3:0]				AFSEL4[3:0]				AFSEL3[3:0]				AFSEL2[3:0]				AFSEL1[3:0]				AFSEL0[3:0]			
	Reset Value	x=A,B,C,D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
024h	GPIOx_AFH	x=A,B,C,D	AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]				AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
	Reset Value	x=A	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		x=B,C,D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
028h	GPIOx_PBC	x=A,B,C,D	Reserved																PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
	Reset Value	x=A,B,C,D	Reserved																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	GPIOx_DS	x=A,B,C,D	Reserved																DS15	DS14	DS13	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
	Reset Value	x=A,B,C,D	Reserved																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.2 GPIO Port Mode Register (GPIOx_PMODE)

Offset Address: 0x00

Reset Value: 0xEBFF FFFF (x=A); 0xFFFF FFFF (x=B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PMODE15[1:0]		PMODE14[1:0]		PMODE13[1:0]		PMODE12[1:0]		PMODE11[1:0]		PMODE10[1:0]		PMODE9[1:0]		PMODE8[1:0]	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE7[1:0]		PMODE6[1:0]		PMODE5[1:0]		PMODE4[1:0]		PMODE3[1:0]		PMODE2[1:0]		PMODE1[1:0]		PMODE0[1:0]	
rw		rw		rw		rw		rw		rw		rw		rw	

Bit Field	Name	Description
31:30 29:28 27:26 25:24	PMODEy[1:0]	GPIOx (x = A, B, C, D) PINy Mode: 00: Input Mode 01: General Output Mode 10: Alternate Function Mode

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Bit Field	Name	Description
23:22		11: Analog Mode
21:20		
19:18		
17:16		
15:14		
13:12		
11:10		
9:8		
7:6		
5:4		
3:2		
1:0		

5.3.3 GPIO Port Output Type Register (GPIOx_POTYPE)

Offset address : 0x04

Reset value : 0x0000 0000 (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	POTy	Output type of port GPIOx (x = A, B, C, D) pin PINy: 0: Push-pull output mode (post-reset state) 1: Open-drain output mode

5.3.4 GPIO Slew Rate Configuration Register (GPIOx_SR)

Offset address : 0x08

Reset value : 0x0000 FFFF (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	SRy	Slew rate configuration bits of port GPIOx (x = A, B, C, D) pin PINy 0: Fast slew rate 1: Slow slew rate

5.3.5 GPIO Port Pull-up/Pull-down Register (GPIOx_PUPD)

Offset address : 0x0C

Reset value : 0x2400 0000 (x=A); 0x0000 0000 (x=B,C,D)

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
PUPD15[1:0]	PUPD14[1:0]	PUPD13[1:0]	PUPD12[1:0]	PUPD11[1:0]	PUPD10[1:0]	PUPD9[1:0]	PUPD8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PUPD7[1:0]	PUPD6[1:0]	PUPD5[1:0]	PUPD4[1:0]	PUPD3[1:0]	PUPD2[1:0]	PUPD1[1:0]	PUPD0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	PUPDy[1:0]	Pull-up/Pull-down mode of port GPIOx (x = A, B, C, D) pin PINy: 00: No pull-up/pull-down 01: Pull-up 10: Pull-down 11: Reserved

5.3.6 GPIO Port Input Data Register (GPIOx_PID)

Offset address : 0x10

Reset value : 0x0000 0000 (x=A, B, C, D)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
Reserved

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PIDy	Input data of port GPIOx (x = A, B, C, D) pin PINy. These bits are read-only, and the read value corresponds to the status of the respective I/O port.

5.3.7 GPIO Port Output Data Register (GPIOx_POD)

Offset address : 0x14

Reset value : 0x0000 0000 (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PODy	Output data of port GPIOx (x = A, B, C, D) pin PINy These bits can be read or written by software, allowing independent configuration/clearing of the corresponding POD bits.

5.3.8 GPIO Port Bit Set/Clear Register (GPIOx_PBSC)

Offset address : 0x18

Reset value : 0x0000 0000 (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
31:16	PBCy	Clear bit y of port GPIOx (x = A, B, C, D). These bits can only be written. 0: No effect on the corresponding PODy bit. 1: Clear the corresponding PODy bit to 0. *Notes:* *1) If both PBCy and the corresponding bit of PBCy are set simultaneously, the PBCy bit takes effect.*
15:0	PBSy	Set bit y of port GPIOx (x = A, B, C, D) These bits can only be written. 0: No effect on the corresponding PODy bit. 1: Set the corresponding PODy bit to 1.

5.3.9 GPIO Port Locking Configuration Register (GPIOx_ PLOCK)

Offset address : 0x1C

Reset value : 0x0000 0000 (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															PLOCKK
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:17	Reserved	Reserved, must be maintained at reset value.
16	PLOCKK	Lock bit This bit can be read at any time, and it can only be modified through a write sequence with a lock key. 0: Port configuration lock key bit is not activated 1: Port configuration lock key bit is activated, GPIOx_PLOCK register will be locked until the next system reset. Lock key write sequence: Write 1 -> Write 0 -> Write 1 -> Read 0 -> (Read 1) The last read of 1 can be omitted, but can be used to confirm that the lock key has been activated. *Note: When performing the lock key write sequence, the value of PLOCK[15:0] cannot be changed. Any errors in the lock key write sequence will prevent the lock key from being activated.*
15:0	PLOCKy	Port GPIOx (x = A, B, C, D) pin PINy configuration lock bit. These bits can be read and written, but can only be written when PLOCKK bit is 0. 0: Configuration of the port is not locked.

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Email：info@nationstech.com
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Bit Field	Name	Description
		1: Configuration of the port is locked.

5.3.10 GPIO Alternate Function Low Configuration Register (GPIOx_AFL)

Offset address : 0x20

Reset value : 0xFFFF FFFF (x = A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL7[3:0]				AFSEL6[3:0]				AFSEL5[3:0]				AFSEL4[3:0]			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL3[3:0]				AFSEL2[3:0]				AFSEL1[3:0]				AFSEL0[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28	AFSELy[3:0]	GPIOx（x = A, B, C, D）port PINy（y = 0…7）alternate function configuration bit
27:24		0000: AF0
23:20		0001: AF1
19:16		0010: AF2
15:12		0011: AF3
11:8		0100: AF4
7:4		0101: AF5
3:0		0110: AF6
		0111: AF7
		1000: AF8
		1001: AF9
		1010: AF10
		1011: AF11
		1100: AF12
		1101: AF13
		1110: AF14
		1111: AF15
		Note: AF15 is GPIO without alternate function.

5.3.11 GPIO Alternate Function High Configuration Register (GPIOx_AFH)

Offset address : 0x24

Reset value : 0xF00F FFFF (x = A); 0xFFFF FFFF (x = B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]			
rw				rw				rw				rw			

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28 27:24 23:20 19:16 15:12 11:8 7:4 3:0	AFSELy[3:0]	GPIOx（x = A, B, C, D）port PINy（y = 0…7）alternate function configuration bit 0000: AF0 0001: AF1 0010: AF2 0011: AF3 0100: AF4 0101: AF5 0110: AF6 0111: AF7 1000: AF8 1001: AF9 1010: AF10 1011: AF11 1100: AF12 1101: AF13 1110: AF14 1111: AF15 *Note: AF15 is GPIO without* alternate function.

5.3.12 GPIO Port Bit Clear Register (GPIOx_PBC)

Offset address : 0x28

Reset value : 0x0000 0000 (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	PBCy	Clear bit y of port GPIOx (x = A, B, C, D) These bits can only be written. 0: No effect on the corresponding PODy bit.

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: Clear the corresponding PODy bit to 0.

5.3.13 GPIO Driver Strength Configuration Register (GPIOx_ DS)

Offset address : 0x2C

Reset value : 0x0000 0000 (x=A, B, C, D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS15	DS14	DS13	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	DSy	Drive strength configuration bit for pin PINy of port GPIOx (x = A, B, C, D) 0：High drive strength (16mA(5V) / 8mA (3.3V) /4mA (1.8V)) 1：Low drive strength (8mA (5V) / 4mA (3.3V) / 2mA (1.8V))

5.4 AFIO Registers

5.4.1 AFIO Register Overview

AFIO Base Address：0x4001 0000

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Table 5-40 AFIO Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	AFIO_ CFG	Reserved			TIM3CH2_RMP	Reserved				SPI3_NSS	SPI2_NSS	SPI1_NSS	Reserved					EXTI_ETRR[3:0]				Reserved							IOFLTCFG[4:0]				
	Reset Value				0					0	0	0						0	0	0	0								0	0	0	0	0
008h	AFIO_EXTI_CFG0	Reserved																EXTI3_CFG[3:0]				EXTI2_CFG[3:0]				EXTI1_CFG[3:0]				EXTI0_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	AFIO_EXTI_CFG1	Reserved																EXTI7_CFG[3:0]				EXTI6_CFG[3:0]				EXTI5_CFG[3:0]				EXTI4_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	AFIO_EXTI_CFG2	Reserved																EXTI11_CFG[3:0]				EXTI10_CFG[3:0]				EXTI9_CFG[3:0]				EXTI8_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	AFIO_EXTI_CFG3	Reserved																EXTI15_CFG[3:0]				EXTI14_CFG[3:0]				EXTI13_CFG[3:0]				EXTI12_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	AFIO_DIGEFT_CFG1	PB15DIGEFTEN	PB14DIGEFTEN	PB13DIGEFTEN	PB12DIGEFTEN	PB11DIGEFTEN	PB10DIGEFTEN	PB9DIGEFTEN	PB8DIGEFTEN	PB7DIGEFTEN	PB6DIGEFTEN	PB5DIGEFTEN	PB4DIGEFTEN	PB3DIGEFTEN	PB2DIGEFTEN	PB1DIGEFTEN	PB0DIGEFTEN	PA15DIGEFTEN	PA14DIGEFTEN	PA13DIGEFTEN	PA12DIGEFTEN	PA11DIGEFTEN	PA10DIGEFTEN	PA9DIGEFTEN	PA8DIGEFTEN	PA7DIGEFTEN	PA6DIGEFTEN	PA5DIGEFTEN	PA4DIGEFTEN	PA3DIGEFTEN	PA2DIGEFTEN	PA1DIGEFTEN	PA0DIGEFTEN
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	AFIO_DIGEFT_CFG2	PD15DIGEFTEN	PD14DIGEFTEN	PD13DIGEFTEN	PD12DIGEFTEN	PD11DIGEFTEN	PD10DIGEFTEN	PD9DIGEFTEN	PD8DIGEFTEN	PD7DIGEFTEN	PD6DIGEFTEN	PD5DIGEFTEN	PD4DIGEFTEN	Reserved	PD2DIGEFTE	PD1DIGEFTE	PD0DIGEFTEN	PC15DIGEFTEN	PC14DIGEFTEN	PC13DIGEFTEN	PC12DIGEFTEN	PC11DIGEFTEN	PC10DIGEFTEN	PC9DIGEFTEN	PC8DIGEFTEN	PC7DIGEFTEN	PC6DIGEFTEN	PC5DIGEFTEN	PC4DIGEFTEN	PC3DIGEFTEN	PC2DIGEFTEN	PC1DIGEFTEN	PC0DIGEFTEN
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.4.2 AFIO Configuration Register (AFIO_CFG)

Offset address : 0x00

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			TIM3CH2_RMP	Reserved				SPI3_NSS	SPI2_NSS	SPI1_NSS	Reserved				
			rw					rw	rw	rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	EXTI_ETRR[3:0]			Reserved							IOFLITCFG[4:0]				
	rw										rw				

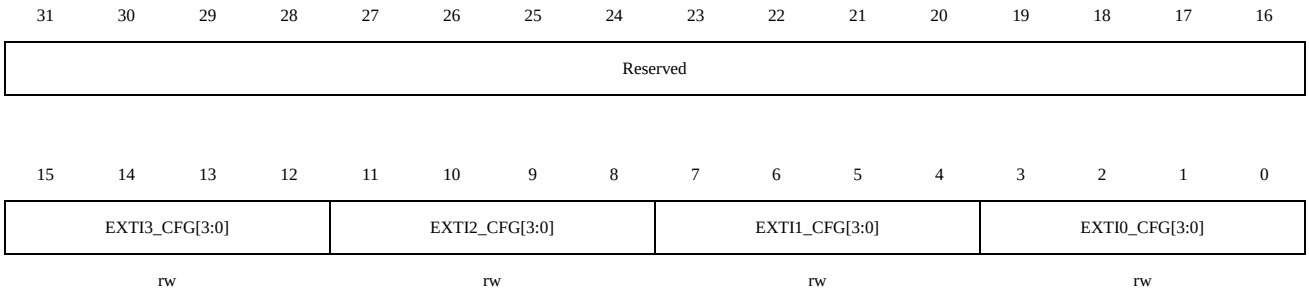
Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:24	Reserved	Reserved, must be maintained at reset value.
28	TIM3CH2_RMP	TIM3_CH2 remapping. 0: TIM3_CH2 is connected to IO 1: TIM3_CH2 is connected to LSI
27:24	Reserved	Reserved, must be maintained at reset value.
23	SPI3_NSS	SPI3 NSS mode selection bit (NSS configured as AFIO push-pull mode). 0: NSS is high impedance when idle 1: NSS is high level when idle
22	SPI2_NSS	SPI2 NSS mode selection bit (NSS configured as AFIO push-pull mode). 0: NSS is high impedance when idle 1: NSS is high level when idle
21	SPI1_NSS	SPI1 NSS mode selection bit (NSS configured as AFIO push-pull mode). 0: NSS is high impedance when idle 1: NSS is high level when idle
20:15	Reserved	Reserved, must be maintained at reset value.
14:11	EXTI_ETRR[3:0]	Select interrupt line remapping for external trigger remapping. 0000: Select EXTI0 rule for external trigger remapping 0001: Select EXTI1 rule for external trigger remapping ... 1111: Select EXTI15 rule for external trigger remapping
10:5	Reserved	Reserved, must be maintained at reset value.
4:0	IOFLITCFG[4:0]	IO filter control. 00000: Bypass filter 00001: IO filter time is 1 APB2 clock cycle 00010: IO filter time is 2 APB2 clock cycles ... 11111: IO filter time is 31 APB2 clock cycles

5.4.3 AFIO External Interrupt Configuration Register 0 (AFIO_EXTI_CFG0)

Offset address : 0x08

Reset value : 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
15:0	EXTIx_CFG[3:0]	EXTIx Configuration (x = 0 ... 3) These bits can be read and written by software to select the input source for EXTIx external interrupt. EXTi0 configuration 0001: PA0 pin 0010: PB0 pin 0100: PC0 pin 1000: PD0 pin EXTI1 configuration 0001: PA1 pin 0010: PB1 pin 0100: PC1 pin 1000: Reserved EXTI2 configuration 0001: PA2 pin 0010: PB2 pin 0100: PC2 pin 1000: Reserved EXTI3 configuration 0001: PA3 pin 0010: PB3 pin 0100: PC3 pin 1000: Reserved *Note: Cannot be combined for use, for example: Only one of the PA0, PB0, PC0, PD0 pins can trigger the EXTI0 interrupt.*

5.4.4 AFIO External Interrupt Configuration Register 1 (AFIO_EXTI_CFG1)

Offset address : 0x0C

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI7_CFG[3:0]				EXTI6_CFG[3:0]				EXTI5_CFG[3:0]				EXTI4_CFG[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	EXTIx_CFG[3:0]	EXTIx configuration (x = 4 ... 7) These bits can be read and written by software to select the input source for EXTIx external interrupt. EXTI4 configuration 0001: PA4 pin 0010: PB4 pin 0100: PC4 pin 1000: PD4 pin EXTI5 configuration 0001: PA5 pin 0010: PB5 pin 0100: PC5 pin 1000: PD5 pin EXTI6 configuration 0001: PA6 pin 0010: PB6 pin 0100: PC6 pin 1000: PD6 pin EXTI7 configuration 0001: PA7 pin 0010: PB7 pin 0100: PC7 pin 1000: PD7 pin *Note: Cannot be combined for use, for example: Only one of the PA4, PB4, PC4, PD4 pins can trigger the EXTI4 interrupt.*

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

5.4.5 AFIO External Interrupt Configuration Register 2 (AFIO_EXTI_CFG2)

Offset address : 0x10

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI11_CFG[3:0]				EXTI10_CFG[3:0]				EXTI9_CFG[3:0]				EXTI8_CFG[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.
15:0	EXTIx_CFG[3:0]	EXTIx configuration（x = 8… 11） These bits can be read and written by software to select the input source for EXTIx external interrupt. EXTI8 configuration 0001: PA8 pin 0010: PB8 pin 0100: PC8 pin 1000: PD8 pin EXTI9 configuration 0001: PA9 pin 0010: PB9 pin 0100: PC9 pin 1000: PD9 pin EXTI10 configuration 0001: PA10 pin 0010: PB10 pin 0100: PC10 pin 1000: PD10 pin EXTI11 configuration 0001: PA11 pin 0010: PB11 pin 0100: PC11 pin 1000: PD11 pin *Note: Cannot be combined for use, for example: Only one of the PA8, PB8, PC8, PD8 pins can trigger the EXTI8 interrupt.*

5.4.6 AFIO External Interrupt Configuration Register 3 (AFIO_EXTI_CFG3)

Offset address : 0x14

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI15_CFG[3:0]				EXTI14_CFG[3:0]				EXTI3_CFG[3:0]				EXTI2_CFG[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, must be maintained at reset value.

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Bit Field	Name	Description
15:0	EXTIx_CFG[3:0]	EXTIx configuration（x = 12 … 15） These bits can be read and written by software to select the input source for EXTIx external interrupt. EXTI12 configuration 0001: PA12 pin 0010: PB12 pin 0100: PC12 pin 1000: PD12 pin EXTI13 configuration 0001: PA13 pin 0010: PB13 pin 0100: PC13 pin 1000: PD13 pin EXTI14 configuration 0001: PA14 pin 0010: PB14 pin 0100: PC14 pin 1000: PD14 pin EXTI15 configuration 0001: PA15 pin 0010: PB15 pin 0100: PC15 pin 1000: PD15 pin *Note: Cannot be combined for use, for example: Only one of the PA12, PB12, PC12, PD12 pins can trigger the EXTI12 interrupt.*

5.4.7 Digital Glitch Filter Configuration Register 1 (AFIO_DIGEFT_CFG1)

Offset address : 0x18

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PB15DIGEFTEN	PB14DIGEFTEN	PB13DIGEFTEN	PB12DIGEFTEN	PB11DIGEFTEN	PB10DIGEFTEN	PB9DIGEFTEN	PB8DIGEFTEN	PB7DIGEFTEN	PB6DIGEFTEN	PB5DIGEFTEN	PB4DIGEFTEN	PB3DIGEFTEN	PB2DIGEFTEN	PB1DIGEFTEN	PB0DIGEFTEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA15DIGEFTEN	PA14DIGEFTEN	PA13DIGEFTEN	PA12DIGEFTEN	PA11DIGEFTEN	PA10DIGEFTEN	PA9DIGEFTEN	PA8DIGEFTEN	PA7DIGEFTEN	PA6DIGEFTEN	PA5DIGEFTEN	PA4DIGEFTEN	PA3DIGEFTEN	PA2DIGEFTEN	PA1DIGEFTEN	PA0DIGEFTEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	PByDIGEFTEN	Digital filter enable bit for pin PBy (y=0...15) 0: Disable digital filter 1: Enable digital filter
15:0	PAyDIGEFTEN	Digital filter enable bit for pin PAy (y=0...15) 0: Disable digital filter 1: Enable digital filter

5.4.8 Digital Glitch Filter Configuration Register 2 (AFIO_DIGEFT_CFG2)

Offset address : 0x1C

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD15DIGEFTEN	PD14DIGEFTEN	PD13DIGEFTEN	PD12DIGEFTEN	PD11DIGEFTEN	PD10DIGEFTEN	PD9DIGEFTEN	PD8DIGEFTEN	PD7DIGEFTEN	PD6DIGEFTEN	PD5DIGEFTEN	PD4DIGEFTEN	Reserved	PD2DIGEFTEN	PD1DIGEFTEN	PD0DIGEFTEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC15DIGEFTEN	PC14DIGEFTEN	PC13DIGEFTEN	PC12DIGEFTEN	PC11DIGEFTEN	PC10DIGEFTEN	PC9DIGEFTEN	PC8DIGEFTEN	PC7DIGEFTEN	PC6DIGEFTEN	PC5DIGEFTEN	PC4DIGEFTEN	PC3DIGEFTEN	PC2DIGEFTEN	PC1DIGEFTEN	PC0DIGEFTEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	PDyDIGEFTEN	Digital filter enable bit for pin PDy (y=0...15) 0: Disable digital filter 1: Enable digital filter
15:0	PCyDIGEFTEN	Digital filter enable bit for pin PCy (y=0...15) 0: Disable digital filter 1: Enable digital filter

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

6 Interrupts and Events

6.1 Nested Vectored Interrupt Controller

Features

- 32 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines).
- 4 programmable priority levels (using 2-bit interrupt priority);
- Low-latency exception and interrupt handling;
- Power management control;
- Implementation of system control registers;

The nested vectored interrupt controller (NVIC) is closely linked to the processor core, enabling low latency interrupt processing and efficient processing of late interrupts. The nested vectored interrupt controller manages interrupts including core exceptions.

6.1.1 SysTick Calibration Value Register

The system tick calibration value is fixed at 8000. When the system tick clock is set to 8MHz (the maximum value of HCLK/8), 1ms time base is generated.

6.1.2 Interrupt and Exception Vectors.

Table 6-1 Vector Table

Position	Priority	Priority Type	Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non-maskable interrupt. RCC clock security system (CSS) is connected to the NMI vector.	0x0000 0008
-	-1	Fixed	HardFault	All types of errors (fault)	0x0000 000C
-	3	Settable	SVCall	System services invoked by SWI directives	0x0000 002C
-	5	Settable	PendSV	System service requests that can be pending	0x0000 0038
-	6	Settable	SysTick	System tick timer	0x0000 003C
0	7	Settable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Settable	PVD	Power supply voltage detection (PVD) interrupt connected to EXTI line 16	0x0000 0044
2	9	Settable	RTC	RTC interrupt connected to EXTI lines 17/18/19	0x0000 0048
3	10	Settable	MMU_RAMC_ERR	MMU/RAMC_ERR global interrupt	0x0000 004C
4	11	Settable	Flash	Flash global interrupt	0x0000 0050
5	12	Settable	RCC	Reset and clock control (RCC) global interrupt	0x0000 0054

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Position	Priority	Priority Type	Name	Description	Address
6	13	Settable	EXTI0_1	The EXTI line 0~1 interrupt	0x0000 0058
7	14	Settable	EXTI2_3	The EXTI line 2~3 interrupt	0x0000 005C
8	15	Settable	EXTI4_15	The EXTI line 4~15 interrupt	0x0000 0060
9	16	Settable	SAC	SAC global interrupt	0x0000 0064
10	17	Settable	DMA_CH1_2	DMA channel 1/2 interrupt	0x0000 0068
11	18	Settable	DMA_CH3_4_5	DMA channel 3/4/5 interrupt	0x0000 006C
12	19	Settable	TIM4	TIM4 global interrupt	0x0000 0070
13	20	Settable	TIM1_BRK_UP_TRG_COM	TIM1 brakes, updates, triggers and communication interrupt	0x0000 0074
14	21	Settable	TIM1_CC	TIM1 capture/compare interrupt	0x0000 0078
15	22	Settable	CAN	CAN interrupt	0x0000 007C
16	23	Settable	TIM3	TIM3 global interrupt	0x0000 0080
17	24	Settable	UART3_4	UART3/4 global interrupt	0x0000 0084
18	25	Settable	TIM5	TIM5 global interrupt	0x0000 0088
19	26	Settable	TIM6	TIM6 global interrupt (connected to EXTI line 20)	0x0000 008C
20	27	Settable	TIM2	TIM2 global interrupt	0x0000 0090
21	28	Settable	ADC	ADC global interrupt	0x0000 0094
22	29	Settable	SPI2	SPI2 global interrupt	0x0000 0098
23	30	Settable	I^2C1	I^2C1 global interruption	0x0000 009C
24	31	Settable	I^2C2	I^2C2 global interrupt	0x0000 00A0
25	32	Settable	SPI1	SPI1 global interrupt	0x0000 00A4
26	33	Settable	UART1	UART1 global interrupt	0x0000 00A8
27	34	Settable	SPI3	SPI3 global interrupt	0x0000 00AC
28	35	Settable	UART5	UART5 global interrupt	0x0000 00B0
29	36	Settable	LCD	LCD global interrupt	0x0000 00B4
30	37	Settable	UART2	UART2 global interrupt	0x0000 00B8
31	38	Settable	COMP1_2_3_4	COMP1/2/3/4 global interrupt	0x0000 00BC

6.2 Extended Interrupt/Event Controller (EXTI)

6.2.1 Introduction

The extended interrupt/event controller contains 21 edge detection circuits that generate interrupt/event triggers. Each input line can be independently configured with pulse or pending input types, and 3 trigger event types including rising edge, falling edge or double edges, which can also be independently shielded. Interrupt requests that hold the state line in the pending register can be cleared by writing '1' in the corresponding bit of the pending register.

6.2.2 Main Features

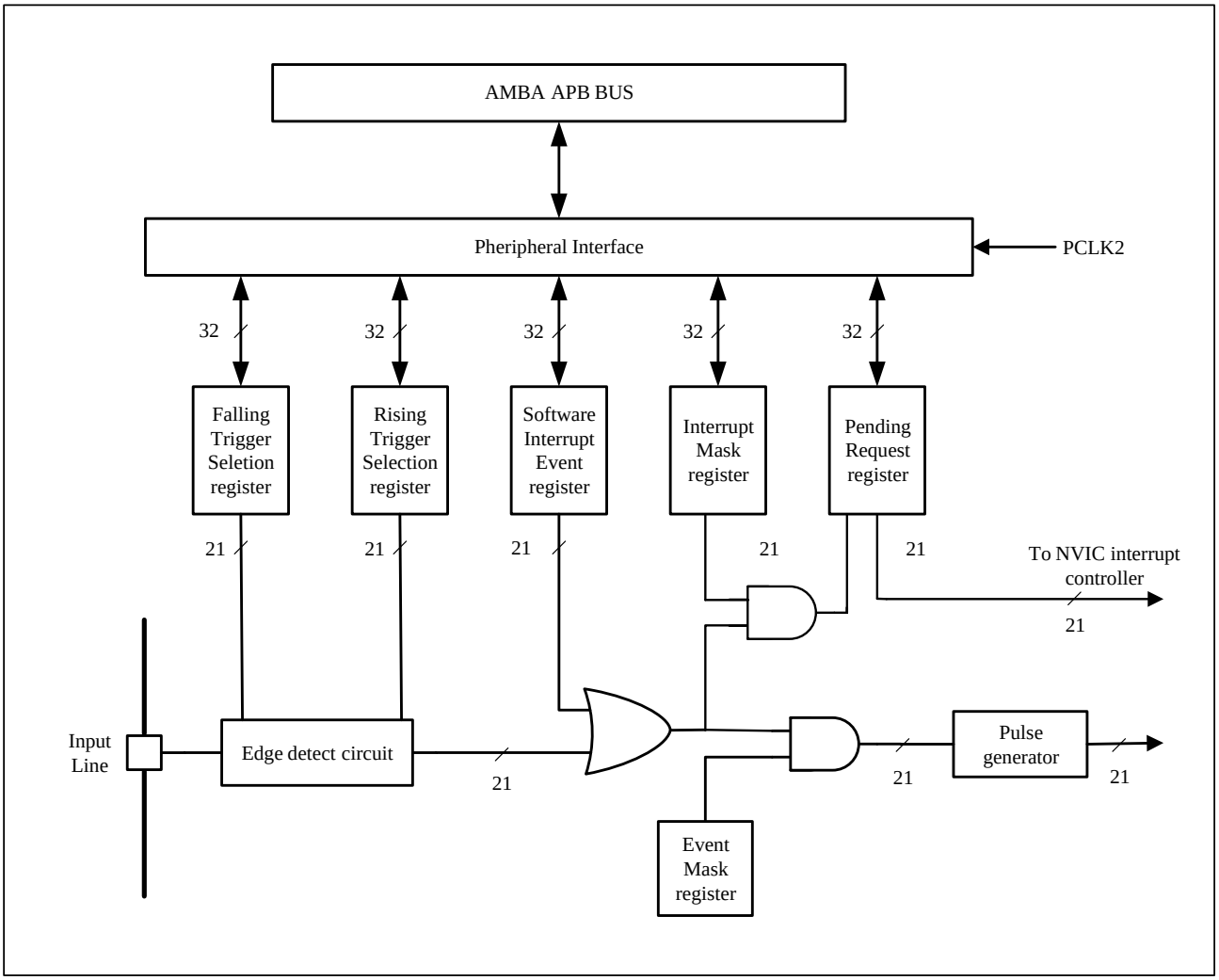
The main features of EXTI controller are as follows:

- Support 21 software interrupt/event requests.
- Interrupts/events corresponding to each input line can be configured to trigger or mask independently.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- Each interrupt line has an independent state bit.
- Support for pulse or pending input types.
- 3 trigger events are supported: rising edge, falling edge, and double edge.
- Wake up MCU to exit low power mode.

Figure 6-1 Extenal Interrupt/Event Controller Block Diagram



6.2.3 Functional Description

The EXTI contains 21 interrupt lines, 16 lines from I/O pins and 5 lines from internal modules. To generate interrupts, the NVIC interrupt channel of the extended interrupt controller must be configured to enable the appropriate interrupt lines. Select rising edge, falling edge, or double edges trigger event types by edge trigger configuration registers EXTI_RT_CFG and EXTI_FT_CFG, and write '1' to the corresponding bit of interrupt masking register EXTI_IMASK to allow interrupt requests. When a preset edge trigger polarity is detected on the external interrupt line, an interrupt request is generated and the corresponding pending bit is set to '1'. Writing '1' to the corresponding bit of the pending register clears the interrupt request.

To generate an event, the corresponding event line must be configured and enabled. According to the desired edge detection polarity, set up the rise/fall edge trigger configuration register, while writing '1' in the corresponding bit of the event masking register to allow interrupt requests. When a preset edge occurs on an event line, an event request

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

pulse is generated and the corresponding pending bit is not set to '1'.

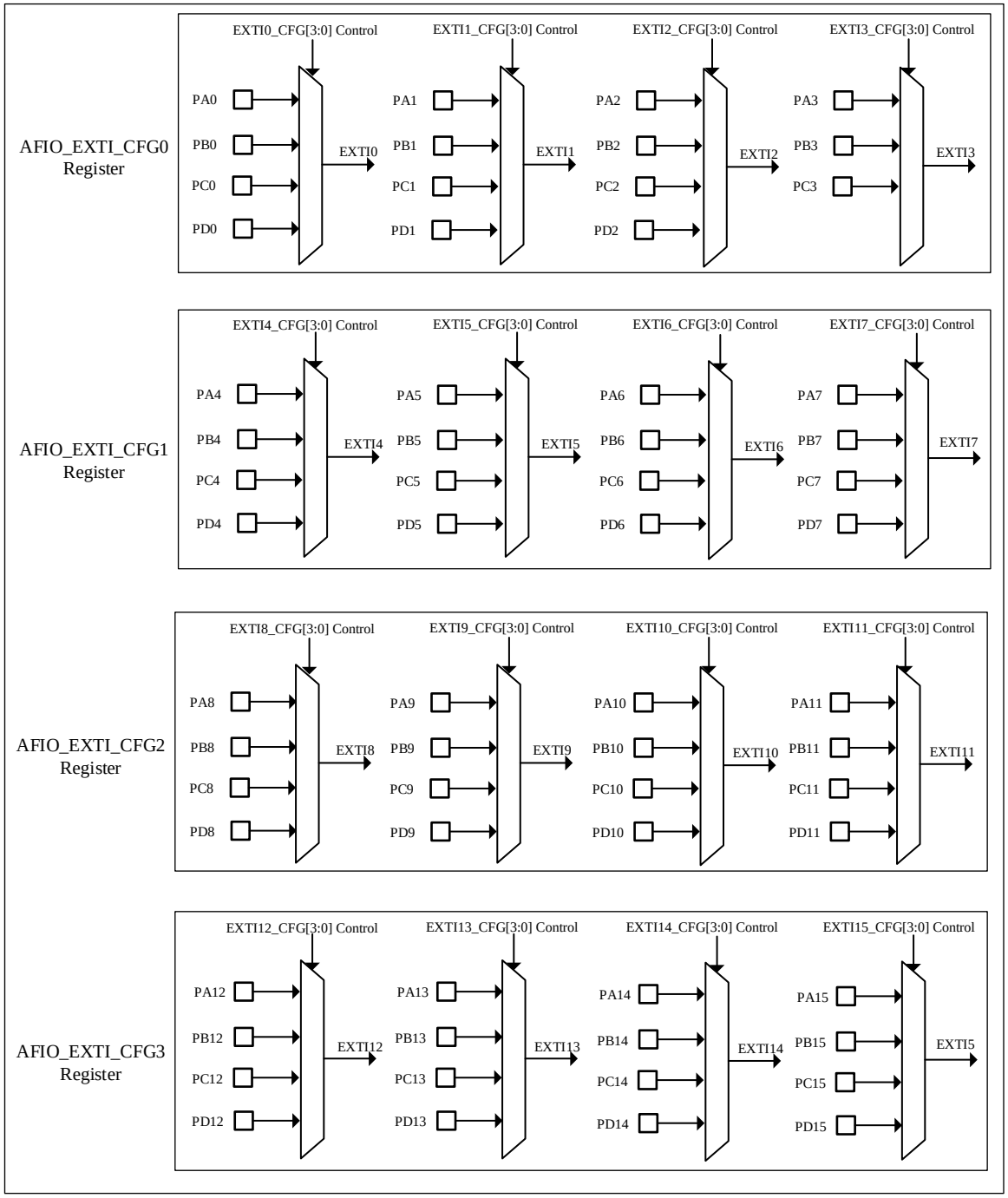
In addition, interrupt/event requests can also be generated by software by writing a '1' in the software interrupt/event register.

- Hardware interrupt configuration, select and configure 21 lines as interrupt sources as required:
  - Configure the mask bit (EXTI_IMASK) for 21 interrupt lines.
  - Configure the Trigger Selection bits of the selected interrupt line (EXTI_RT_CFG and EXTI_FT_CFG);
  - Configure the enable and mask bits of the NVIC interrupt channel corresponding to the external interrupt controller so that the requests in the 21 interrupt lines can be correctly responded to.
- Hardware event configuration: Select 21 lines as event sources as required:
  - Configure the mask bit (EXTI_EMASK) for 21 event lines.
  - Configure the Trigger Selection bits for the selected event line (EXTI_RT_CFG and EXTI_FT_CFG).
- Software interrupt/event configuration, select 21 lines as software interrupt/event lines as required:
  - Configure 21 interrupt/event line mask bits (EXTI_IMASK and EXTI_EMASK).
  - Configure the request bit of the software interrupt event register (EXTI_SWIE).

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

6.2.4 EXTI Line Mapping

Figure 6-2 External Interrupt Generic I/O Mapping



To configure external interrupts/events on the GPIO line using AFIO_EXTI_CFG1~4, the AFIO clock must be enabled first. General I/O ports are connected to 16 external interrupt/event lines as shown above. The connection mode of the other 5 EXTI lines is as follows:

- EXTI line 16 is connected to the PVD output
- EXTI line 17 is connected to the RTC alarm event
- EXTI line 18 is connected to the RTC tamper or RTC timescale Wakeup event

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- EXTI line 19 is connected to the RTC Wake up event
- EXTI line 20 is connected to the TIM6 Wake up event

6.3 EXTI Registers

6.3.1 EXTI Register Overview

Table 6-2 EXTI Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	EXTI_EMASK	Reserved											EMASK20	EMASK19	EMASK18	EMASK17	EMASK16	EMASK15	EMASK14	EMASK13	EMASK12	EMASK11	EMASK10	EMASK9	EMASK8	EMASK7	EMASK6	EMASK5	EMASK4	EMASK3	EMASK2	EMASK1	EMASK0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	EXTI_IMASK	Reserved											IMASK20	IMASK19	IMASK18	IMASK17	IMASK16	IMASK15	IMASK14	IMASK13	IMASK12	IMASK11	IMASK10	IMASK9	IMASK8	IMASK7	IMASK6	IMASK5	IMASK4	IMASK3	IMASK2	IMASK1	IMASK0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	EXTI_FT_CFG	Reserved											FT_CFG20	FT_CFG19	FT_CFG18	FT_CFG17	FT_CFG16	FT_CFG15	FT_CFG14	FT_CFG13	FT_CFG12	FT_CFG11	FT_CFG10	FT_CFG9	FT_CFG8	FT_CFG7	FT_CFG6	FT_CFG5	FT_CFG4	FT_CFG3	FT_CFG2	FT_CFG1	FT_CFG0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	EXTI_RT_CFG	Reserved											RT_CFG20	RT_CFG19	RT_CFG18	RT_CFG17	RT_CFG16	RT_CFG15	RT_CFG14	RT_CFG13	RT_CFG12	RT_CFG11	RT_CFG10	RT_CFG9	RT_CFG8	RT_CFG7	RT_CFG6	RT_CFG5	RT_CFG4	RT_CFG3	RT_CFG2	RT_CFG1	RT_CFG0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	EXTI_PEND	Reserved											PEND20	PEND19	PEND18	PEND17	PEND16	PEND15	PEND14	PEND13	PEND12	PEND11	PEND10	PEND9	PEND8	PEND7	PEND6	PEND5	PEND4	PEND3	PEND2	PEND1	PEND0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	EXTI_SWIE	Reserved											SWIE20	SWIE19	SWIE18	SWIE17	SWIE16	SWIE15	SWIE14	SWIE13	SWIE12	SWIE11	SWIE10	SWIE9	SWIE8	SWIE7	SWIE6	SWIE5	SWIE4	SWIE3	SWIE2	SWIE1	SWIE0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	EXTI_TS_SEL	Reserved																												TSSEL[3:0]			
	Reset Value																													0	0	0	0

6.3.2 EXTI Event Mask Register (EXTI_EMASK)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											EMASK20	EMASK19	EMASK18	EMASK17	EMASK16
											rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMASK15	EMASK14	EMASK13	EMASK12	EMASK11	EMASK10	EMASK9	EMASK8	EMASK7	EMASK6	EMASK5	EMASK4	EMASK3	EMASK2	EMASK1	EMASK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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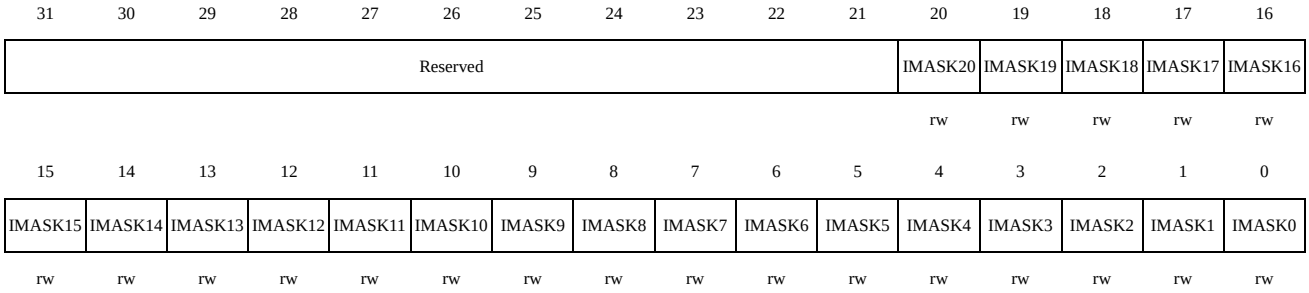
BitField	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	EMASKx	Event mask on line x (x = 0, 1, 2, …, 19, 20) 0: Masking the event requests from line x. 1: Not masking the event requests from line x.

6.3.3 EXTI Interrupt Mask Register (EXTI_IMASK)

Address offset: 0x04

Reset value: 0x0000 0000

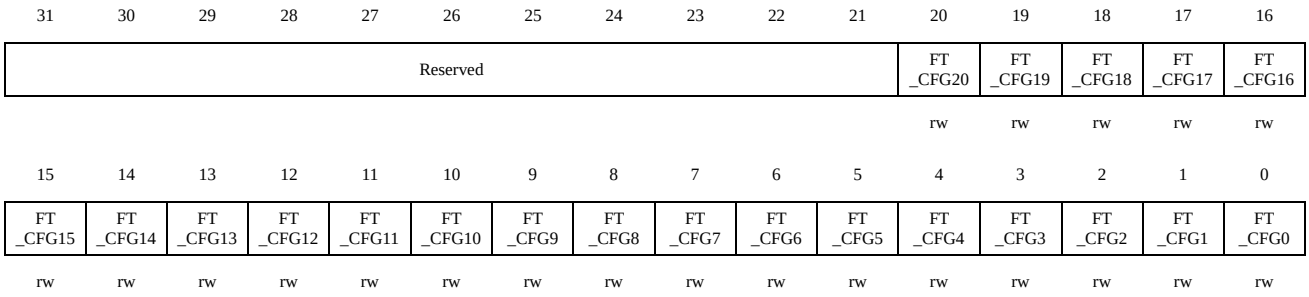


BitField	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	IMASKx	Interrupt mask on line x (x = 0, 1, 2, …, 19, 20) 0: Masking the interrupt requests from line x. 1: Not masking the interrupt requests from line x.

6.3.4 EXTI Falling Edge Trigger Configuration Register (EXTI_FT_CFG)

Address offset: 0x08

Reset value: 0x0000 0000



BitField	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	FT_CFGx	The falling edge on line x triggers the configuration bit (x = 0, 1, 2, …, 19, 20) 0: Disable falling edge triggering (interrupts and events) on input line x 1: Enable falling edge triggering (interrupts and events) on input line x

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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6.3.5 EXTI Rising Edge Trigger Configuration Register (EXTI_RT_CFG)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											RT_CFG20	RT_CFG19	RT_CFG18	RT_CFG17	RT_CFG16
											rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT_CFG15	RT_CFG14	RT_CFG13	RT_CFG12	RT_CFG11	RT_CFG10	RT_CFG9	RT_CFG8	RT_CFG7	RT_CFG6	RT_CFG5	RT_CFG4	RT_CFG3	RT_CFG2	RT_CFG1	RT_CFG0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

BitField	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	RT_CFGx	The rising edge on line x triggers the configuration bit (x = 0, 1, 2, …, 19, 20) 0: Disable rising edge triggering (interrupts and events) on input line x 1: Enable rising edge triggering (interrupts and events) on input line x

6.3.6 EXTI Pending Register (EXTI_PEND)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											PEND20	PEND19	PEND18	PEND17	PEND16
											rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEND15	PEND14	PEND13	PEND12	PEND11	PEND10	PEND9	PEND8	PEND7	PEND6	PEND5	PEND4	PEND3	PEND2	PEND1	PEND0
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

BitField	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	PENDx	Pending bit on line x (x = 0, 1, 2, …, 19, 20) 0: No pending request has occurred 1: A pending trigger request occurred This bit is set to '1' when a selected edge trigger event occurs on the external interrupt line. It can be cleared by writing '1' to the bit, or by changing the polarity of the edge detection.

6.3.7 EXTI Software Interrupt Event Register (EXTI_SWIE)

Address offset: 0x14

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											SWIE20	SWIE19	SWIE18	SWIE17	SWIE16
											rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWIE15	SWIE14	SWIE13	SWIE12	SWIE11	SWIE10	SWIE9	SWIE8	SWIE7	SWIE6	SWIE5	SWIE4	SWIE3	SWIE2	SWIE1	SWIE0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

BitField	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	SWIEx	Software interrupt on line x (x = 0, 1, 2, …, 19, 20) When the bit is' 0 ', writing '1' sets the corresponding pending bit in EXTI_PEND. If this interrupt is allowed in EXTI_IMASK and EXTI_EMASK, an interrupt will be generated. *Note: This bit can be cleared to '0' by writing '1' to clear the corresponding bit of EXTI_PEND.*

6.3.8 EXTI Timestamp Trigger Source Selection Register (EXTI_TS_SEL)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												TSSEL[3:0]			
												rw	rw	rw	rw

BitField	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	TSSEL[3:0]	Select the external interrupt input as the trigger source for the timestamp event 0000: Select EXTI0 as the trigger source of the timestamp event; 0001: Select EXTI1 as the trigger source of the timestamp event. ... 1111: Select EXTI15 as the trigger source for the timestamp event.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

7 DMA Controller

7.1 Introduction

The DMA controller can access totally 5 AHB slaves: Flash, SRAM, ADC, ABP1 and APB2. DMA Controller is controlled by CPU to perform fast data transfer from source to destination. After configuration, data can be transferred without CPU intervention. Thus, CPU can be released for other computation/control tasks or save overall system power consumption.

The main architecture of the MCU is a multi-layer AHB-Lite bus structure with round-robin arbitration scheme. DMA and CPU can access different slaves in parallel or same slaves sequentially.

DMA controller has 5 logic channels. Each logic channel is used to serve memory access requests from single or multiple peripherals. The priorities of different DMA channels are controlled by the internal arbiter.

Support user-configurable peripheral request channels.

7.2 Main Features

DMA main features:

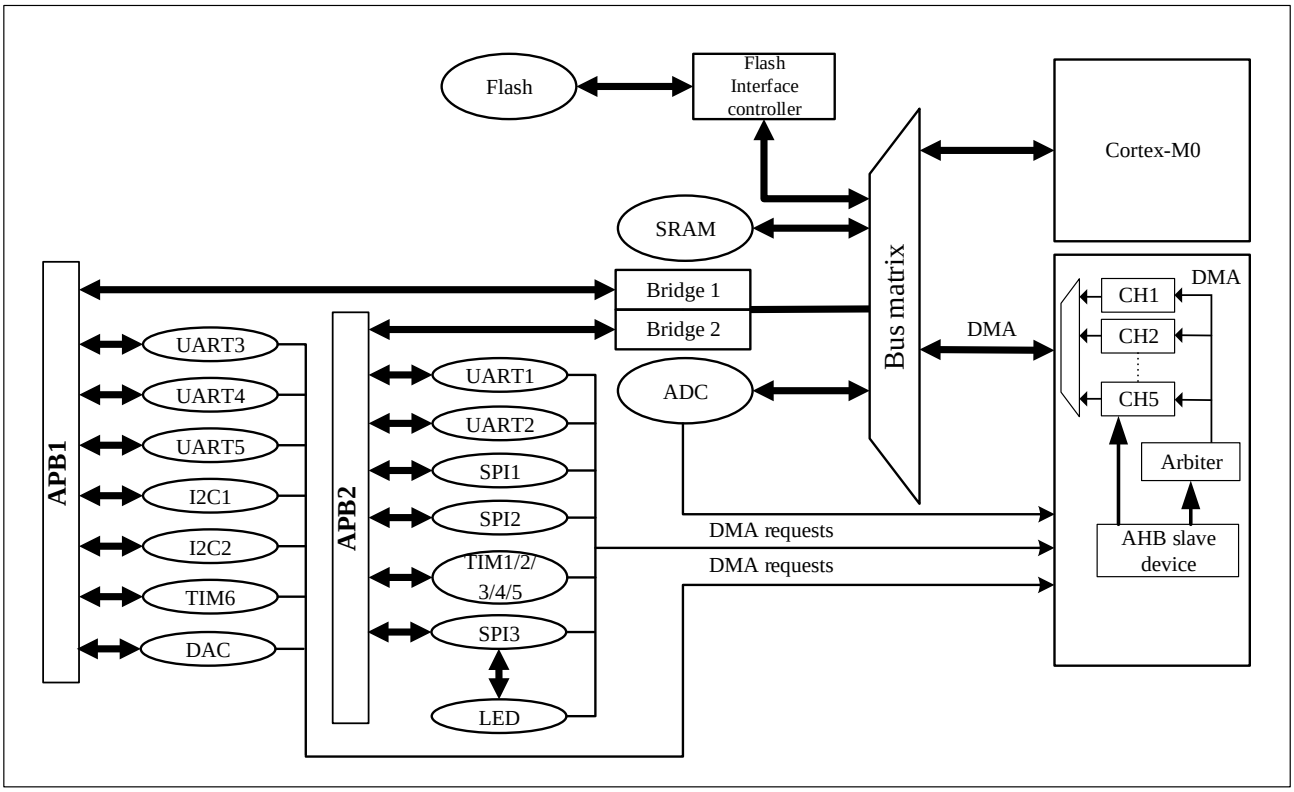
- 5 DMA channels which can be configured independently.
- Each DMA channel supports hardware requests and software triggers to initiate transfer which is configured by software.
- Each DMA channel has dedicated software priority level (DMA_CHCFGx.PRIOLVL [1:0] bits, corresponding to 4 levels of priority) which can be configured individually. Channels with the same software priority level will further compare hardware index (channel number) to decide final priority (lower index number channel will has higher priority).
- Configurable source and destination size. Address setting should correspond to data size.
- Configurable circular transfer mode for each channel.
- Each channel has 3 independent event flags and interrupts (Transfer complete, Half transfer, Transfer error), and a global interrupt flag (set by logical or of 3 events).
- Support three transfer types which are Memory-to-Memory, Memory-to-Peripheral and Peripheral-to-Memory.

  Note: Transfer of peripheral SPI to peripheral DAC can also be supported (mode configuration is peripheral to memory mode).
- Access totally 5 AHB slaves: Flash, SRAM, ADC, APB1 and APB2.
- Configurable data transmit number (0~65535).

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

7.3 Block Diagram

Figure 7-1 DMA Block Diagram



7.4 Function Description

DMA controller and Cortex®-M0 core share the same system data bus. When CPU and DMA access the same destination (RAM or peripheral) at the same time, DMA request will suspend CPU from accessing the system bus for several cycles, and the bus arbiter will perform round-robin scheduling. This allows the CPU to get at least half of the system bus (memory or peripheral) bandwidth.

7.4.1 DMA Operation

A DMA request can be triggered by hardware peripherals or software, and the DMA controller processes the request according to the priority level of the channel. The data is read from the source address according to the configured transfer address and bit width, and then the read data is stored in the destination address space. After one operation, the controller calculates the number of remaining transfers and updates the source address and the destination address for the next transfer.

Each DMA data transfer consists of three operations:

- Data access: determine the source address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and read data from the source address.
- Data storage: determine the destination address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and store the read data into the destination address space.
- Calculate the number of unfinished operations, perform a decrement operation on the DMA_TXNUMx register, and update the source and destination addresses for the next operation.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

7.4.2 Channel Priority and Arbitration

The DMA uses arbitration to handle multiple requests from different channels. The priority of each channel is programmable in the channel control register (DMA_CHCFGx).

4 levels of priority:

- Very high priority
- High priority
- Medium priority
- Low priority

By default, channel with lower index has higher priority if the programmed priority is the same.

For memory to memory transfer, re-arbitration is performed after 4 transfer operations.

For transfer related to periphery, re-arbitration is performed after each transfer operation.

7.4.3 DMA Channels and Number of Transfers

Each channel can perform DMA transfer between the specified peripheral registers and memory addresses. The number of data transferred by DMA is programmable, and the maximum supported value is 65535. The DMA_TXNUM register is decremented after each transfer.

7.4.4 Programmable Data Bit Width

Peripheral and memory transfer data width supports byte, half-word and word, which can be programmed through DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE.

When DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE are different, the DMA module aligns the data according to the below.

Table 7-1 Programmable Data Width and Endian Operation (When PINC = MINC = 1)

Source Width (bit)	Destination Width (bit)	Number Of Transfer (bit)	Source: Address / Data	Transfer Operations (R: Read, W: Write)	Destination: Address / Data
8	8	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W B0 [7:0] @0x0 2: R B1 [7:0] @0x1, W B1 [7:0] @0x1 3: R B2 [7:0] @0x2, W B2 [7:0] @0x2 4: R B3 [7:0] @0x3, W B3 [7:0] @0x3	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3
8	16	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W 00B0 [15:0] @0x0 2: R B1 [7:0] @0x1, W 00B1 [15:0] @0x2 3: R B2 [7:0] @0x2, W 00B2 [15:0] @0x4 4: R B3 [7:0] @0x3, W 00B3 [15:0] @0x6	0x0 / 00B0 0x2 / 00B1 0x4 / 00B2 0x6 / 00B3
8	32	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W 000000B0 [31:0] @0x0 2: R B1 [7:0] @0x1, W 000000B1 [31:0] @0x4 3: R B2 [7:0] @0x2, W 000000B2 [31:0] @0x8 4: R B3 [7:0] @0x3, W 000000B3 [31:0] @0xC	0x0 / 000000B0 0x4 / 000000B1 0x8 / 000000B2 0xC / 000000B3

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Source Width (bit)	Destination Width (bit)	Number Of Transfer (bit)	Source: Address / Data	Transfer Operations (R: Read, W: Write)	Destination: Address / Data
16	8	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W B0 [7:0] @0x0 2: R B3B2 [15:0] @0x2, W B2 [7:0] @0x1 3: R B5B4 [15:0] @0x4, W B4 [7:0] @0x2 4: R B7B6 [15:0] @0x6, W B6 [7:0] @0x3	0x0 / B0 0x1 / B2 0x2 / B4 0x3 / B6
16	16	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W B1B0 [15:0] @0x0 2: R B3B2 [15:0] @0x2, W B3B2 [15:0] @0x2 3: R B5B4 [15:0] @0x4, W B5B4 [15:0] @0x4 4: R B7B6 [15:0] @0x6, W B7B6 [15:0] @0x6	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6
16	32	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W 0000B1B0 [31:0] @0x0 2: R B3B2 [15:0] @0x2, W 0000B3B2 [31:0] @0x4 3: R B5B4 [15:0] @0x4, W 0000B5B4 [31:0] @0x8 4: R B7B6 [15:0] @0x6, W 0000B7B6 [31:0] @0xC	0x0 / 0000B1B0 0x4 / 0000B3B2 0x8 / 0000B5B4 0xC / 0000B7B6
32	8	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B0 [7:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B4 [7:0] @0x1 3: R BBBAB9B8 [31:0] @0x8, W B8 [7:0] @0x2 4: R BFBEBDBC [31:0] @0xC, W BC [7:0] @0x3	0x0 / B0 0x1 / B4 0x2 / B8 0x3 / BC
32	16	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B1B0 [15:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B5B4 [15:0] @0x2 3: R BBBAB9B8 [31:0] @0x8, W B9B8 [15:0] @0x4 4: R BFBEBDBC [31:0] @0xC, W BDBC [15:0] @0x6	0x0 / B1B0 0x2 / B5B4 0x4 / B9B8 0x6 / BDBC
32	32	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B3B2B1B0 [31:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B7B6B5B4 [31:0] @0x4 3: R BBBAB9B8 [31:0] @0x8, W BBBAB9B8 [31:0] @0x8 4: R BFBEBDBC [31:0] @0xC, W BFBEBDBC [31:0] @0xC	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC

Notice:

DMA always provide full 32-bits data to HWDATA[31:0] no matter what destination size it is (HSIZE still follows destination size setting for device supports byte/half-word operation). The HWDATA[31:0] follows the following rules:

- When source size is smaller than destination size, DMA fills the MSB with 0 until their sizes match and duplicates it to be 32 bits. E.g., source is 8 bits data 0x55 and destination size is 16 bits. DMA fills the source data with 0 to make it 16 bits and become 0x0055, then duplicate it to 32-bit data 0x0055_0055 and provide to HWDATA[31:0]; (if destination size is 32-bit then DMA will only pad source data with 0).
- When source size is larger or equal to destination size and smaller than 32 bits, DMA duplicates source data to 32 bits data. E.g., source data is 8 bits data 0x1F, HWDATA[31:0] =0x1F1F_1F1F. if source data is 16 bits data 0x2345, then HWDATA[31:0] = 0x2345_2345.

This ensures peripherals that only support word operation won't generate bus error and the desired data can still move to the place we want with extra bits i.e. 0 padding. If user wants to configure an 8-bit register but is aligned to a 32-bit address

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Email：info@nationstech.com
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boundary, the source size should be set to 8 bits and destination to 32 bits so extra bits will be padded with 0.

7.4.5 Peripheral/Memory Address Incrementation

DMA_CHCFGx.PINC and DMA_CHCFGx.MINC respectively control whether the peripheral address and memory address are enabled in auto-increment mode. The software cannot write (can read) the address register during transfer.

- In auto-increment mode, the next address to be transferred is automatically increased according to the data width (1, 2 or 4) after each transfer. The address of the first transfer is stored in DMA_PADDRx or DMA_MADDRx register.
- In fixed mode, the address is always fixed to the initial address.

At the end of transfer (i.e. the transfer count changes to 0), different processes will be carried out according to whether the current operation is under circular mode or not.

- In non-circular mode, DMA stops after the transfer is completed. To start a new DMA transfer, need to rewrite the transfer number in the DMA_TXNUMx register with the DMA channel disabled.
- In circular mode, at the end of the transfer, the content of the DMA_TXNUMx register will be automatically reloaded to its initial value, and the current internal peripheral or memory address register will also be reloaded to the initial base address set by the DMA_PADDRx or DMA_MADDRx register.

7.4.6 Channel Configuration Process

The detail configuration process is as below:

1. Configure interrupt mask bits, 1: enable interrupts, 0 disable interrupts.
2. Configure channel peripheral address, memory address and transfer direction.
3. Configure channel priority, 0: lowest, 3: highest.
4. Configure peripheral and memory address increment.
5. Configure channel transfer data width and the number of transfer
6. If necessary, configure circular mode.
7. If it is memory to memory, configure MEM2MEM mode (Note: configure DMA to operation in M2M mode, user needs to set corresponding channel select value to reserved value, e.g., 47).
8. Repeat steps 1 to 5 on channels 1 to 8.
9. Finally, enable the corresponding channel.

If software is used to serve interrupt, the software must enquire interrupt status register to check which interrupt occurred (software needs to write 1 to interrupt flag clear bit to clear the corresponding interrupt). Before enable channel, all interrupts corresponding to the channel should be cleared.

If the interrupt is transfer complete interrupt, software can configure the next transfer, or report to user this channel transfer is complete.

7.4.7 Flow Control

Three major flow controls are supported:

- Memory to memory

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Email：info@nationstech.com
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- Memory to peripheral
- Peripheral to memory

Flow control is controlled by two register bits in each DMA channel configuration register. Flow control is used to control source/destination and direction of DMA channel.

Table 7-2 Flow Control Table

DMA_CHCFGx.MEM2MEM	DMA_CHCFGx.DIR	Source	Destination	Transfer
1	x	Memory	Memory	AHB read to AHB write, can do back2back transfer
0	1	Memory	AHB Peripheral	AHB read to AHB write, single transfer
			APB Peripheral	AHB read to APB write, single transfer
0	0	AHB Peripheral	Memory	AHB read to AHB write, single transfer
		APB Peripheral		APB read to AHB write, single transfer

7.4.8 Circular Mode

The circular mode is used to process circular buffers and continuous data transmission (such as ADC scan mode). The DMA_CHCFGx.CIRC is used to enable this function. When the circular mode is activated, if the number of data to be transferred becomes 0, it will automatically be restored to the initial value when configuring the channel, and the DMA operation will continue.

If the user wants to turn off the circular mode, the user needs to write 0 to DMA_CHCFGx.CHEN to disable the DMA channel, and then write 0 to DMA_CHCFGx.CIRC (when DMA_CHCFGx.CHEN is 1, other bits in the DMA_CHCFGx register cannot be rewritten).

7.4.9 Error Management

DMA access to reserved address space will cause DMA transfer error. When an error occurs, the transfer error flag is set, and the hardware automatically clears the current DMA channel enable bit (DMA_CHCFGx.CHEN), and the channel operation is stopped. If the transfer error interrupt enable bit is set in the DMA_CHCFGx register, an interrupt will be generated.

7.4.10 Interrupt

- Transfer complete interrupt:

  An interrupt is generated when channel data transfer is completed. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. Interrupt status bit is cleared when interrupt flag clear bit is set.

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Email：info@nationstech.com
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- Half transfer interrupt:

  An interrupt is generated when half of the channel data is transferred. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. Interrupt status bit is cleared when interrupt flag clear bit is set.

- Transfer error interrupt:

  An interrupt is generated when bus returned error. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. Interrupt status bit is cleared when interrupt flag clear bit is set.

Table 7-3 DMA Interrupt Request

Interrupt Event	Event Flag Bit	Enable Control Bit
Half transfer	HTXF	HTXIE
Transfer complete	TXCF	TXCIE
Transfer error	ERRF	ERRIE

7.4.11 DMA Request Mapping

Totally there are 55 DMA requests from all the peripherals. To have better support with full flexibility, register bits can be used to select which DMA request is mapped to which DMA channel. The table blow show the mapping scheme of peripherals' DMA request to DMA controller's DMA channels.

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Table 7-4 DMA Request Mapping

DMA Request Source Select	Peripheral DMA Request	DMA Request Source Select	Peripheral DMA Request
sel = 0	ADC	sel = 28	TIM2_CH1
sel = 1	UART1_TX	sel = 29	TIM2_CH2
sel = 2	UART1_RX	sel = 30	TIM2_CH3
sel = 3	UART2_TX	sel = 31	TIM2_CH4
sel = 4	UART2_RX	sel = 32	TIM2_UP
sel = 5	UART3_TX	sel = 33	TIM2_TRIG
sel = 6	UART3_RX	sel = 34	TIM3_CH1
sel = 7	UART4_TX	sel = 35	TIM3_CH2
sel = 8	UART4_RX	sel = 36	TIM3_CH3
sel = 9	UART5_TX	sel = 37	TIM3_CH4
sel = 10	UART5_RX	sel = 38	TIM3_UP
sel = 11	SPI1_TX	sel = 39	TIM3_TRIG
sel = 12	SPI1_RX	sel = 40	TIM4_CH1
sel = 13	SPI2_TX	sel = 41	TIM4_CH2
sel = 14	SPI2_RX	sel = 42	TIM4_CH3
sel = 15	SPI3_TX	sel = 43	TIM4_CH4
sel = 16	SPI3_RX	sel = 44	TIM4_UP
sel = 17	I2C1_TX	sel = 45	TIM4_TRIG
sel = 18	I2C1_RX	sel = 46	TIM5_CH1
sel = 19	I2C2_TX	sel = 47	TIM5_CH2
sel = 20	I2C2_RX	sel = 48	TIM5_CH3
sel = 21	TIM1_CH1	sel = 49	TIM5_CH4
sel = 22	TIM1_CH2	sel = 50	TIM5_UP
sel = 23	TIM1_CH3	sel = 51	TIM5_TRIG
sel = 24	TIM1_CH4	sel = 52	TIM6_UP
sel = 25	TIM1_COM	sel = 53	DAC
sel = 26	TIM1_UP	sel = 54	GCLK_TRIG
sel = 27	TIM1_TRIG		

Note: Different DMA channels cannot use the same request source, otherwise only high priority channels will be triggered if multiple channels are enabled.

7.5 DMA Registers

7.5.1 DMA Register Overview

Table 7-5 DMA Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DMA_INTSTS	Reserved												ERRF5	HTXF5	TXCF5	GLBF5	ERRF4	HTXF4	TXCF4	GLBF4	ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
004h	DMA_INTCLR	Reserved												CERRF5	CHTXF5	CTXCF5	CGLBF5	CERRF4	CHTXF4	CTXCF4	CGLBF4	CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	DMA_CHCFG1	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	DMA_TXNUM1	Reserved																	NDTX[15:0]														
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	DMA_PADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	DMA_MADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	DMA_CHSEL1	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
01Ch	DMA_CHCFG2	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	DMA_TXNUM2	Reserved																	NDTX[15:0]														
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	DMA_PADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	DMA_MADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	DMA_CHSEL2	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
030h	DMA_CHCFG3	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	DMA_TXNUM3	Reserved																	NDTX[15:0]														
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	DMA_PADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	DMA_MADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	DMA_CHSEL3	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
044h	DMA_CHCFG4	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	DMA_TXNUM4	Reserved																	NDTX[15:0]														
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	DMA_PADDR4	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	DMA_MADDR4	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	DMA_CHSEL4	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
058h	DMA_CHCFG5	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05Ch	DMA_TXNUM5	Reserved																	NDTX[15:0]														
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
060h	DMA_PADDR5	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
064h	DMA_MADDR5	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
068h	DMA_CHSEL5	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0

7.5.2 DMA Interrupt Status Register (DMA_INTSTS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved												ERRF5	HTXF5	TXCF5	GLBF5
												r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRF4	HTXF4	TXCF4	GLBF4	ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19/15/11/7/3	ERRFx	Transfer error flag for channel x (x=1…5). Hardware sets this bit when transfer error happen. This bit is cleared by software by writing '1' to DMA_INTCLR.CERRFx bit. 0: Transfer error no happened on channel x. 1: Transfer error happened on channel x.
18/14/10/6/2	HTXFx	Half transfer flag for channel x (x=1…5). Hardware sets this bit when half transfer is done. This bit is cleared by software by writing '1' to DMA_INTCLR.CHTXFx bit. 0: Half transfer not yet done on channel x. 1: Half transfer was done on channel x.
17/13/9/5/1	TXCFx	Transfer complete flag for channel x (x=1…5). Hardware sets this bit when transfer is done. This bit is cleared by software by writing '1' to DMA_INTCLR.CTXCFx bit. 0: Transfer not yet done on channel x. 1: Transfer was done on channel x.
16/12/8/4/0	GLBFx	Global flag for channel x (x=1…5). Hardware sets this bit when any interrupt events happen in this channel. This bit is cleared by software by writing '1' to DMA_INTCLR.CGLBFx bit. 0: No transfer error, half transfer or transfer done event happen on channel x. 1: One of transfer error, half transfer or transfer done event happen on channel x.

7.5.3 DMA Interrupt Flag Clear Register (DMA_INTCLR)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												CERRF5	CHTXF5	CTXCF5	CGLBF5
												w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CERRF4	CHTXF4	CTXCF4	CGLBF4	CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

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Email：info@nationstech.com
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Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19/15/11/7/3	CERRFx	Clear transfer error flag for channel x (x=1…5). Software can set this bit to clear ERRF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.ERRF bit of corresponding channel.
18/14/10/6/2	CHTXFx	Clear half transfer flag for channel x (x=1…5). Software can set this bit to clear HTXF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.HTXF bit of corresponding channel.
17/13/9/5/1	CTXCFx	Clear transfer complete flag for channel x (x=1…5). Software can set this bit to clear TXCF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.TXCF bit of corresponding channel.
16/12/8/4/0	CGLBFx	Clear global event flag for channel x (x=1…5). Software can set this bit to clear GLBF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.GLBF bit of corresponding channel.

7.5.4 DMA Channel x Configuration Register (DMA_CHCFGx)

Note: The x is channel number, x = 1…5

Address offset: 0x08+20 * (x–1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	MEM2 MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	MEM2MEM	Memory to memory mode. Software can configure this channel to memory to memory transfer when it is not enabled. 0: Channel transfer between memory and peripheral. 1: Channel set to memory to memory transfer.
13:12	PRIOLVL[1:0]	Channel priority. Software can program channel priority when channel is not enable. 00: Low 01: Medium

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Email：info@nationstech.com
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Bit Field	Name	Description
		10: High 11: Very high
11:10	MSIZE[1:0]	Memory data size. Software can configure data size read/write from/to memory address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
9:8	PSIZE[1:0]	Peripheral data size. Software can configure data size read/write from/to peripheral address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
7	MINC	Memory increment mode. Software can enable/disable memory address increment mode. 0: Memory address won't increase with each transfer. 1: Memory address increase with each transfer.
6	PINC	Peripheral increment mode. Software can enable/disable peripheral address increment mode. 0: Peripheral address won't increase with each transfer. 1: Peripheral address increase with each transfer.
5	CIRC	Circular mode. Software can set/clear this bit. 0: Channel will stop after one round of transfer. 1: Channel configure as circular mode.
4	DIR	Data transfer direction Software can set/clear this bit. 0: Data transfer from Peripheral to Memory 1: Data transfer from Memory to Peripheral.
3	ERRIE	Transfer error interrupt enable. Software can enable/disable transfer error interrupt. 0: Disable transfer error interrupt of channel x. 1: Enable transfer error interrupt of channel x.
2	HTXIE	Half transfer interrupt enable. Software can enable/disable half transfer interrupt. 0: Disable half transfer interrupt of channel x. 1: Enable half transfer interrupt of channel x.
1	TXCIE	Transfer complete interrupt enable. Software can enable/disable transfer complete interrupt. 0: Disable transfer complete interrupt of channel x. 1: Enable transfer complete interrupt of channel x.
0	CHEN	Channel enable.

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Email：info@nationstech.com
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Bit Field	Name	Description
		Software can set/reset this bit. 0: Disable channel. 1: Enable channel.

7.5.5 DMA Channel x Transfer Number Register (DMA_TXNUMx)

Note: The x is channel number, x = 1…5

Address offset: 0x0C+20 * (x–1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDTX[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	NDTX	Number of data to transfer. Number of data to be transferred (0～65535). Software can read/write the number of transfers when channel is disable and it will be read only after channel enable. Every successful transfer of corresponding DMA channel will decrease this register by 1. If circular mode is enable, it will automatically reload pre-set value when it reach zero. Otherwise it will keep at zero and reset channel enable.

7.5.6 DMA Channel x Peripheral Address Register (DMA_PADDRx)

Note: The x is channel number, x = 1…5

Address offset: 0x10+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Nations Technologies Inc.
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:0	ADDR	Peripheral address. Peripheral starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.PSIZE. With DMA_CHCFGx.PSIZE equal to 01, DMA ignores bit 0 of PADDR and if DMA_CHCFGx.PSIZE equal to 10 DMA will ignore bit [1:0] of PADDR.

7.5.7 DMA Channel x Memory Address Register (DMA_MADDRx)

Note: The x is channel number, x = 1…5

Address offset: 0x14+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	ADDR	ADDR Memory address. Memory starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.MSIZE. With DMA_CHCFGx.MSIZE equal to 01, DMA ignores bit 0 of MADDR and if DMA_CHCFGx.MSIZE equal to 10 DMA will ignore bit [1:0] of MADDR.

7.5.8 DMA Channel x Channel Request Select Register (DMA_CHSELx)

Note: The x is channel number, x = 1…5

Address offset: 0x18+20 * (x–1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										CH_SEL[5:0]					
										rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	CH_SEL[5:0]	DMA channel request source selection 0x00: adc_dma …… 0x36: GCLK_TRIG For the mapping of peripheral DMA requests to DMA input request channel numbers, please refer to **Table 7-4**

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8 CRC Calculation Unit

8.1 CRC Introduction

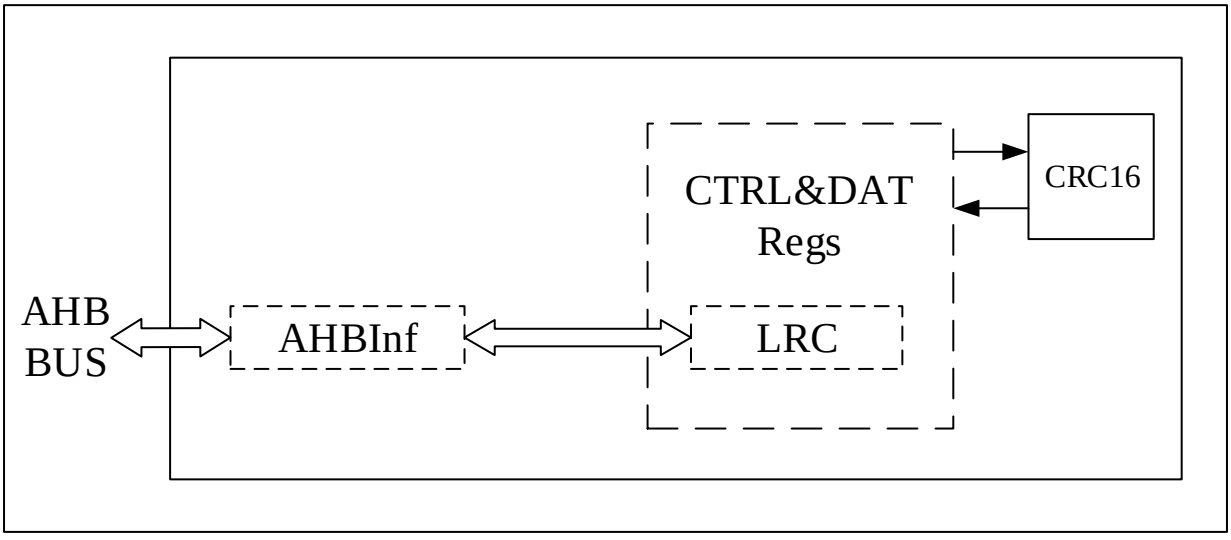
This module integrates the functions of CRC16, and the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. CRC calculation unit can calculate the signature of the software during runtime, then compare it with the reference signature generated during linktime, and then store it in the specified memory space.

8.2 CRC Main Features

- CRC16($X^{16}+X^{15}+X^2+1$)
- There are 8 bits of data to be checked and 16 bits of output check code.
- CRC calculation time: 1 AHB clock cycle (HCLK)
- The verification initial value can be configured, and endianness of the data to be verified can be configured.
- Support 8bit LRC check value generation

The following figure is the block diagram of CRC unit.

Figure 8-1 CRC Calculation Unit Block Diagram



8.3 CRC Function Description

CRC_CRC16CTRL.ENDHL controls Little Endian format or Big Endian format.

To clear the result of the last CRC operation, set CRC_CRC16CTRL.CLR to 1 or CRC_CRC16D to 0.

The initial value of CRC calculation can be configured by writing the CRC_CRC16D register. The initial value is the result of the last calculation by default.

LRC calculation is the same as CRC calculation. Both are carried out at the same time. CRC or LRC can be read out

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Nanshan District, Shenzhen, 518057, P.R.China

depending on needs. If the initial value needs to be set, the LRC register should be configured first.

8.4 CRC Software Calculation Method

In practical applications, if software calculation CRC16 is needed to match the hardware calculation result, the following content needs to be correctly configured:

- WIDTH: 16
- POLY: 0x8005
- INIT: 0x0000
- XOROUT: 0x0000
- REFIN: No
- REFOUT: No

8.5 CRC Registers

8.5.1 CRC Register Overview

The following table lists the registers and reset values of CRC.

Table 8-1 CRC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	CRC16CTRL	Reserved																													CLR	ENDHL	Reserved
	Reset Value																														0	0	
010h	CRC16DAT	Reserved																								CRC16DAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	CRC16D	Reserved																CRC16D[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LRC	Reserved																								LRCDAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0

8.5.2 CRC16 Control Register (CRC_CRC16CTRL)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													CLR	ENDHL	Reserved
													rw	rw	

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Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	CLR	Clear CRC16 results. 0: Not clear. 1: Clear to default value 0x0000. Set this bit to 1 will only maintain 1 clock cycle, hardware will clear automatically. (Software read always 0).
1	ENDHL	Data to be verified start to calculate from MSB or LSB. 0: From MSB to LSB 1: From LSB to MSB This bit is only for data to be verified.
0	Reserved	Reserved, the reset value must be maintained.

Note: 8-bits, 16-bits and 32-bits operations are supported.

8.5.3 CRC16 Input Data Register (CRC_CRC16DAT)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CRC16DAT[7:0]							
								rw							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CRC16DAT[7:0]	Data to be verified.

Note: 8-bits, 16-bits and 32-bits operations are supported.

8.5.4 CRC16 Cyclic Redundancy Check Code Register (CRC_CRC16D)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC16D[15:0]															
rw															

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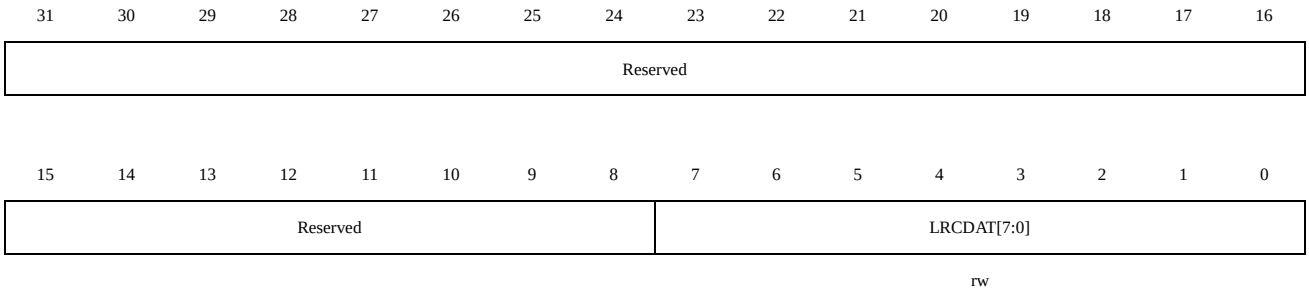
Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRC16D[15:0]	16-bit value of cyclic redundancy result data. Every time the software writes the CRC16DAT register, the 16-bit calculated data from CRC16 is updated in this register.

Note: 8-bits, 16-bits and 32-bits operations are supported (8-bit operations must be performed twice in a row to ensure that 16-bit initial values are configured properly)

8.5.5 CRC16 Result Register (CRC_LRC)

Address offset: 0x18

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	LRCDAT[7:0]	LRC check value register. Software needs to write initial value before usage. Each time data is written to CRC_CRC16DAT, it is "XOR" with the value of the CRC_LCR register. The result will be stored in CRC_LCR. Software reads the result. It should be cleared before next usage.

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Email：info@nationstech.com
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9 Advanced-control Timers (TIM1)

9.1 Introduction

The advanced control timers (TIM1) are mainly used in the following scenarios: counting the input signals, measuring the pulse width of the input signals and generating the output waveforms, etc.

Advanced-control timers have complementary output function with dead-time insertion and break function, which are suitable for motor control.

9.2 Main Features of TIM1

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- Up to 9 channels
- 4 capture/compare channels, the operating modes are PWM output, ouput compare, one-pulse mode output, input capture
- 1 break input signals with digital filter
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break signal input
- Complementary outputs with programmable dead-time
  - For TIM1, channel 1,2,3,4 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_CC5 is used for comparator blanking
- The pulse signals that can be output by TIM1 channels 4/7/8/9 can trigger ADC by configuring the rising and falling edges
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control

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Email：info@nationstech.com
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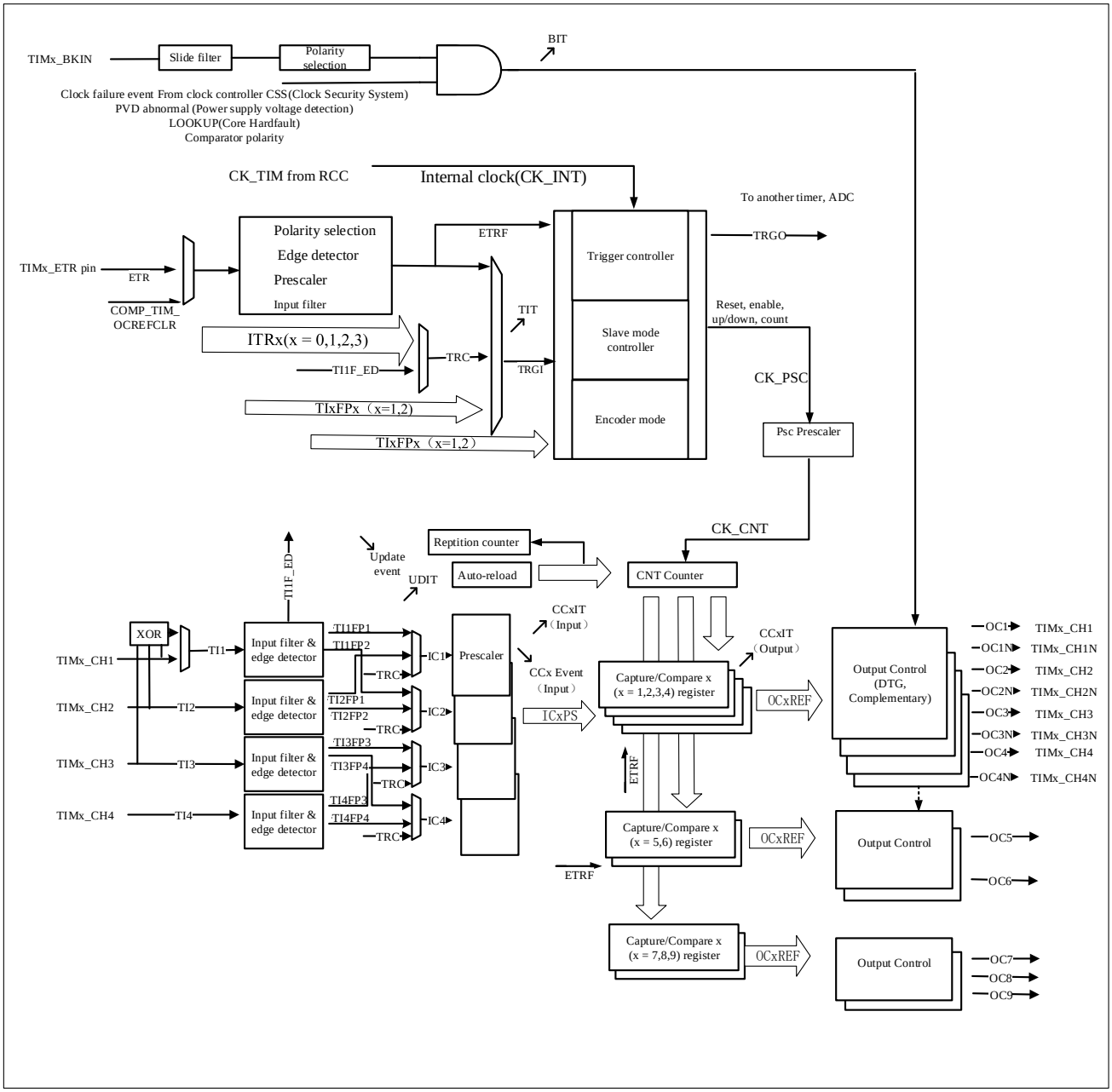
Nanshan District, Shenzhen, 518057, P.R.China

Figure 9-1 Block Diagram of TIM1



↘ *The event* ↗ *Interrupt and DMA output*

The capture channel 1 input can come from IOM or comparator output

9.3 Function Description of TIM1

9.3.1 Time-base Unit

The advanced-control timer's time-base unit mainly includes: prescaler, counter, auto-reload and repetition counter. When the time base unit is operating, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload

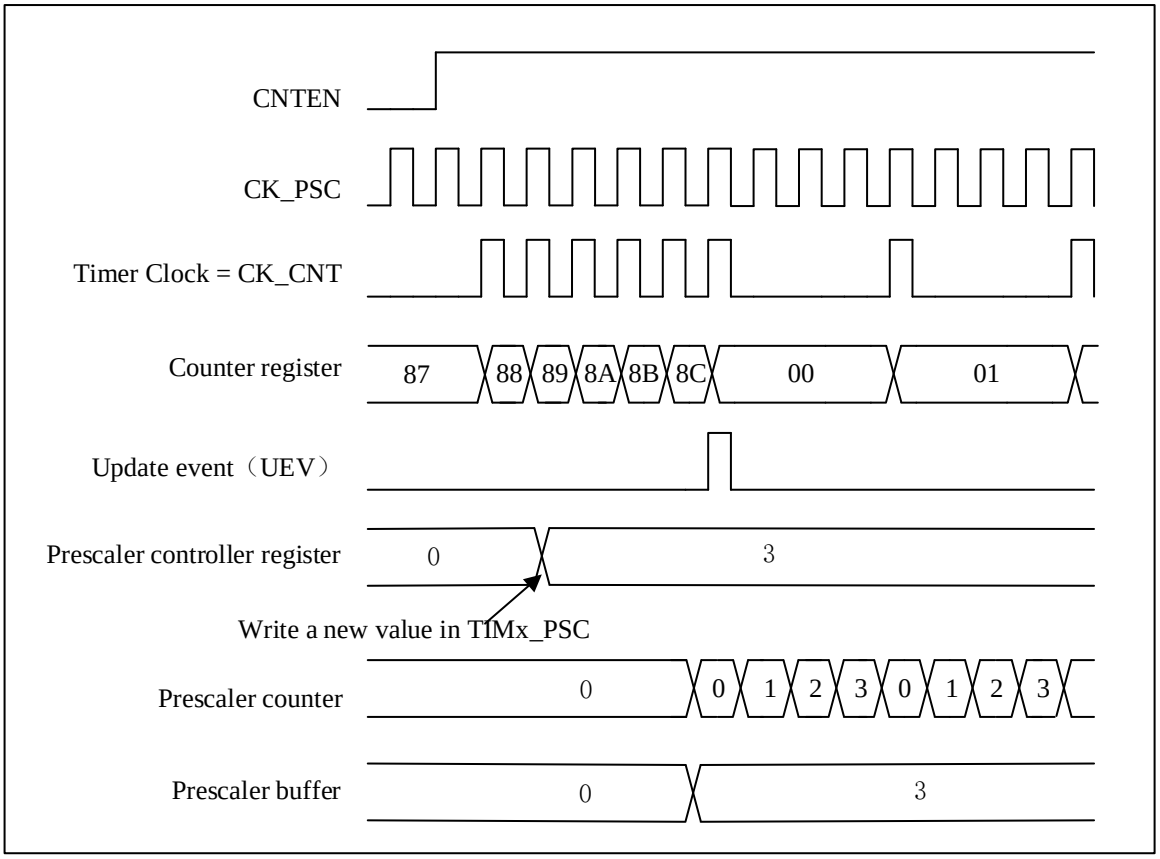
Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

register is transferred to the shadow register immediately or at each update event UEV. When TIMx_CTRL1.UPDIS=0, a counter overflow/underflow or software setting TIMx_EVTGEN.UDGN will generate an update event. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

9.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as this register is buffered. The new prescaler value is only taken into account at the next update event.

Figure 9-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



9.3.2 Counter Mode

9.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it restarts from 0 and a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will be generated, but the TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated.This is to avoid generating an update interrupt when clearing the counter.

Depending on the TIMx_CTRL1.UPRS, when an update event occurs, all registers are updated and the TIMx_STS.UDITF is set:

- The repetition counter reloads the contents of the TIMx_REPCNT

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- The auto-reload shadow registers is updated with preload value (TIMx_AR), when TIMx_CTRL1.ARPEN = 1
- The prescaler shadow register is reloaded with the preload value (TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update event by setting TIMx_CTRL1.UPDIS=1.

When an update event is generated, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior for different prescaler factors in the up-counting mode.

Figure 9-3 Timing Diagram of Up-counting, The Internal Clock Divider Factor = 2/N

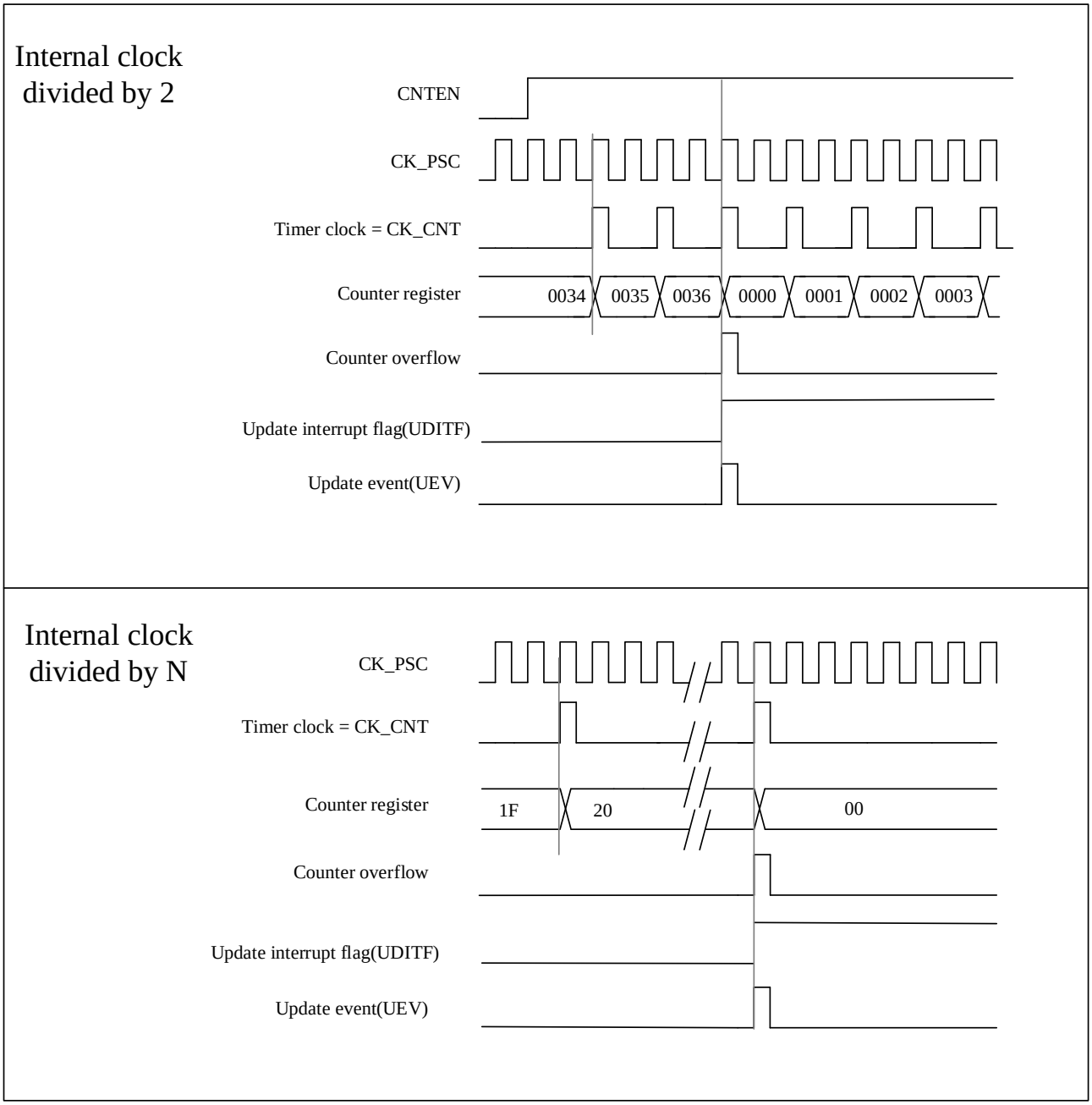

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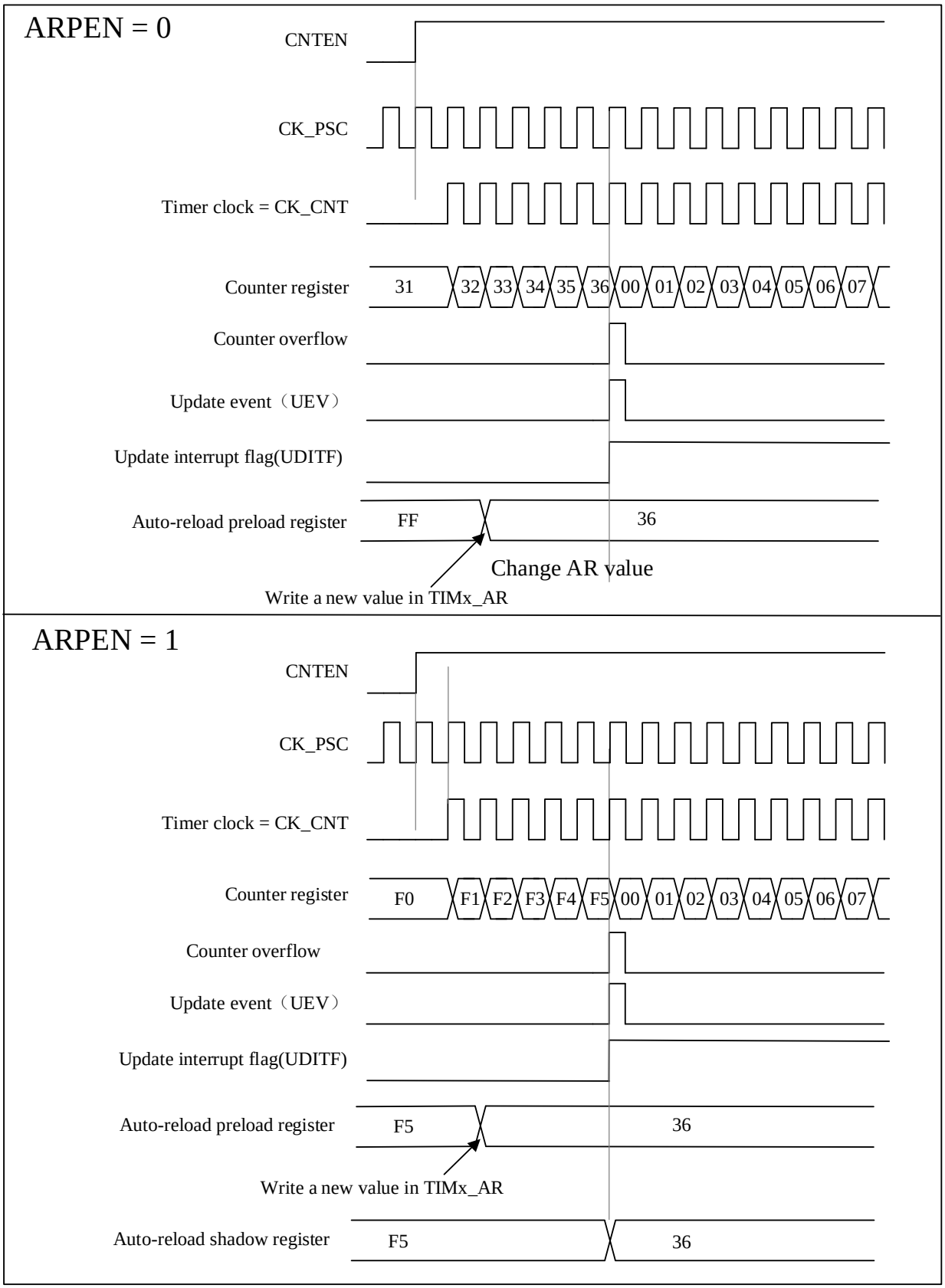
Figure 9-4 Timing Diagram of The Up-counting, Update Event When ARPEN = 0/1



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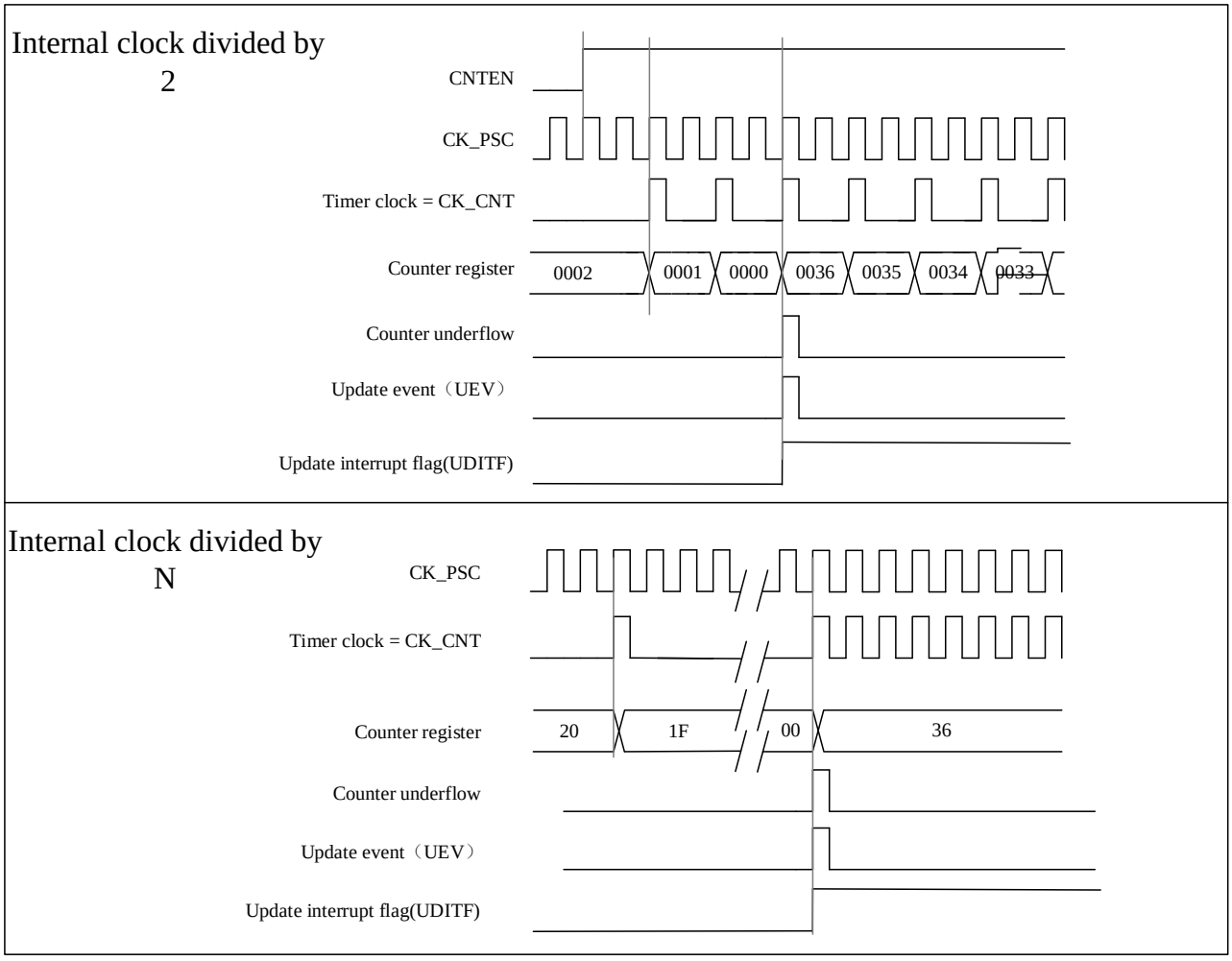
9.3.2.2 Down-counting mode

In down-counting mode, the counter will count from the value of the register TIMx_AR down to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, refer to Section 9.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different prescaler factors in the down-counting mode.

Figure 9-5 Timing Diagram of The Down-counting, Internal Clock Divided Factor = 2/N



9.3.2.3 Center-aligned mode

9.3.2.3.1 Center-aligned symmetric mode

In center-aligned symmetric mode, the counter counts from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts from the auto-reload value (TIMx_AR) down to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits cannot be written and the count direction is updated and specified by hardware. Center-aligned mode is active when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

An update event can be generated at each counter overflows and at each counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

controller). In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note: if an update is generated due to a counter overflow, the auto-reload value will be updated before the counter is reload.

Figure 9-6 Timing Diagram of the Center-aligned, Internal Clock Divided Factor = 2/N

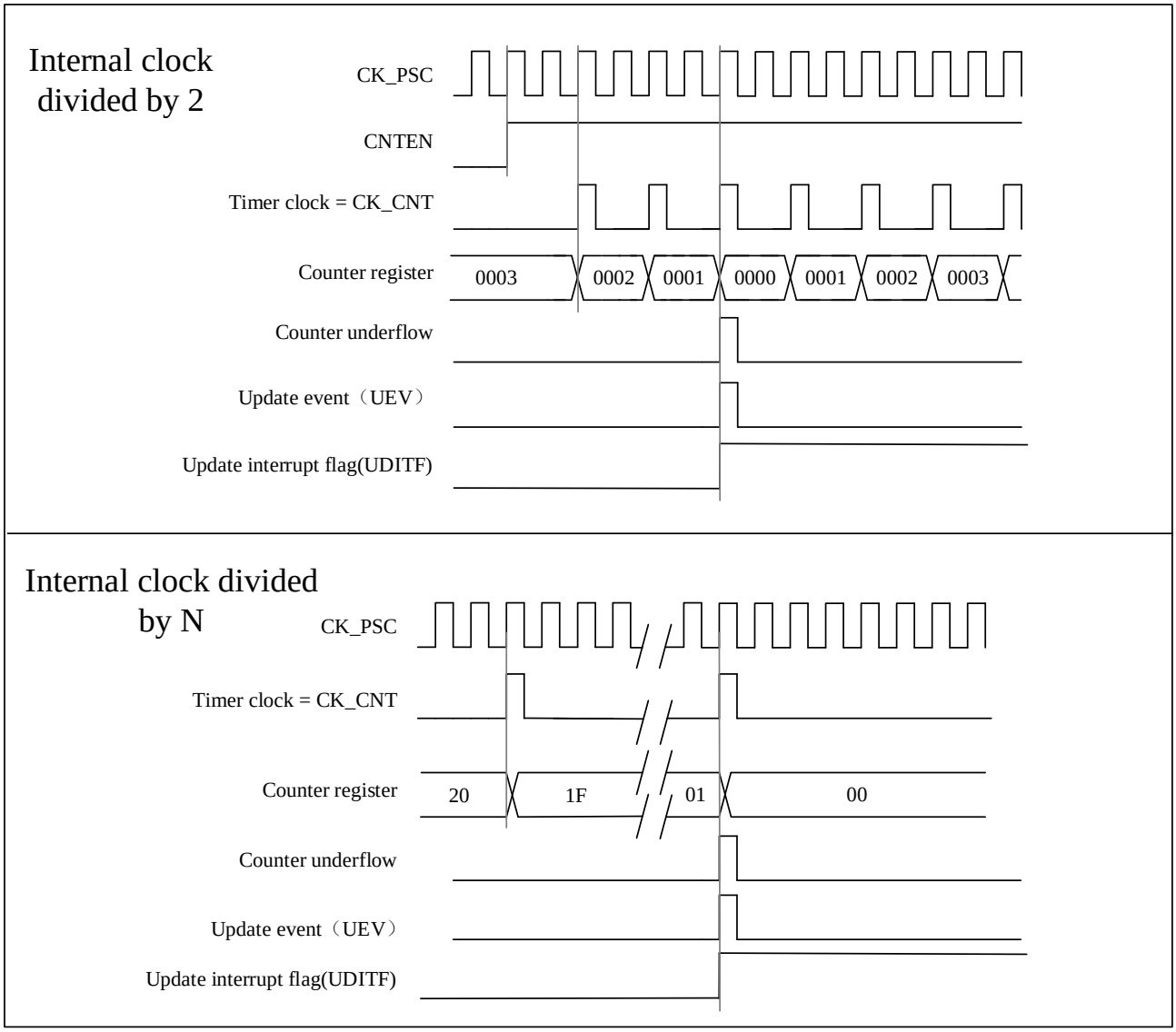

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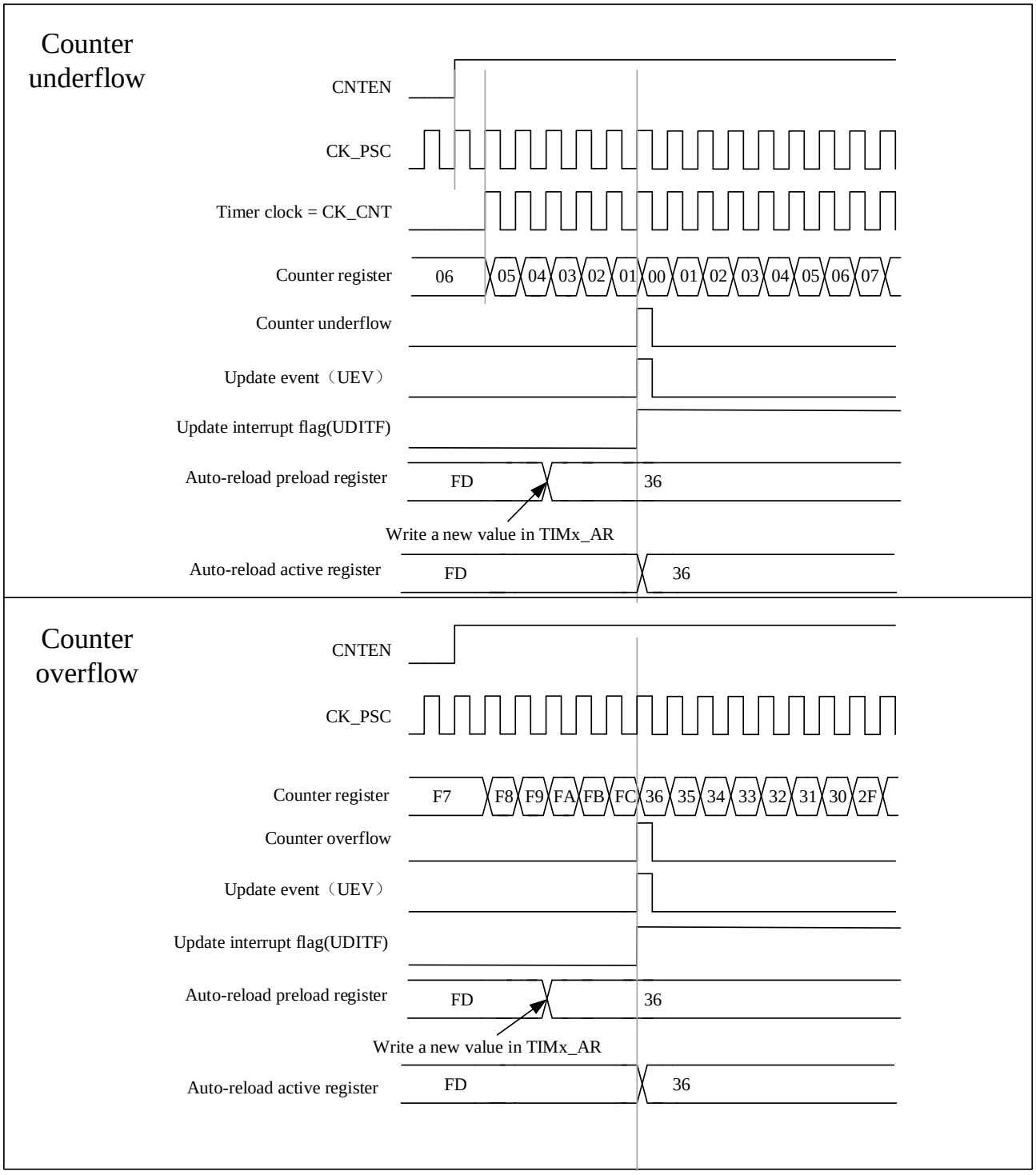
Figure 9-7 A Center-aligned Sequence Diagram That Includes Counter Overflows and Underflows (ARPEN = 1)



9.3.2.3.2 **Center-aligned asymmetric mode**

In center-aligned asymmetric mode (TIMx_CTRL1. ASYMMETRIC is 1 and TIMx_CTRL1.CAMSEL[1:0] is non-zero), the counter counts from 0 to the auto-reload value (TIMx_AR) – 1 and generates a counter overflow event, then counts from the auto-reload value down to 1 and generates a counter underflow event and then restarts counting from 0.

The TIMx_CTRL1.DIR cannot be written in this mode. It is updated by hardware and indicates the current direction

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Email：info@nationstech.com
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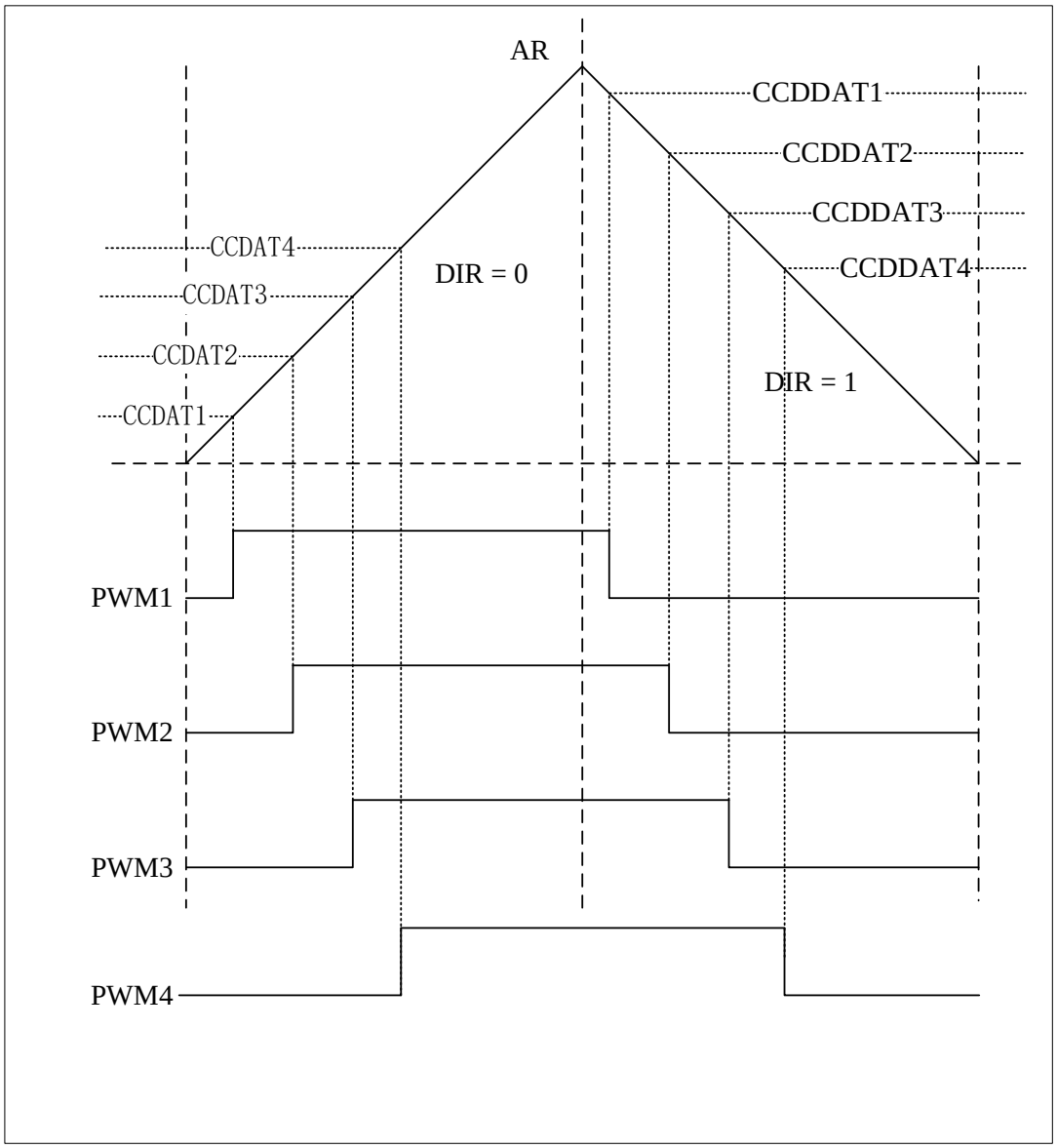
of the counter.

When the channel is not 1,2,3,4, the comparison value are compared with CCDATx. When the dead time generator is turned on, note that when DIR = 0, the dead time insertion point is at which the counter value is equal to CCDATx(x=1,2,3,4), and when DIR = 1, the dead time insertion point is at which the counter value is equal to CCDDATx(x=1,2,3,4).

An update event can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note: if an update is generated due to a counter overflow, the auto-reload value will be updated before the counter is reloaded.

Figure 9-8 The Output Waveform Corresponding to the Asymmetric Mode



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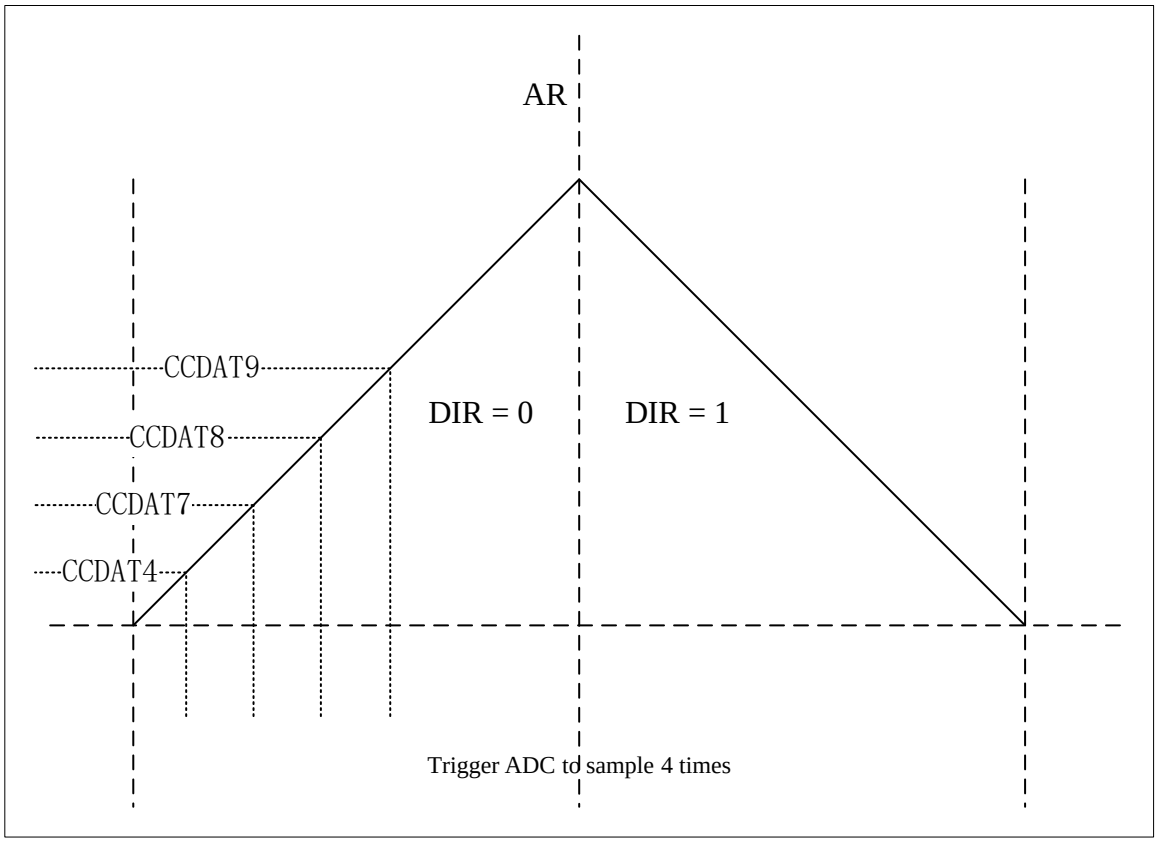
Since the triggering function of CC7/CC8/CC9 three channels is added, and the triggering function of CC4 has been modified. Here is the description of the CC4/CC7/CC8/CC9 channels triggering the ADC.

When the timer is operating in center-aligned asymmetric mode, each channel (CC4/CC7/CC8/CC9) can individually trigger the ADC only when MMSEL3 = 1.

If TIMx_CTRL1.CMODE[1:0]=00, the CCDATx.CCDAT (x=4,7,8,9) value will only trigger ADC when DIR =0.

Figure 9-9 CCDATx (x=4, 7, 8, 9), Trigger ADC When DIR = 0



If TIMx_CTRL1.CMODE [1:0]=01, CCDATx.CCDDAT (x=4) and CCDATx.CCDAT (x=7,8,9) value will only trigger ADC when DIR =1.

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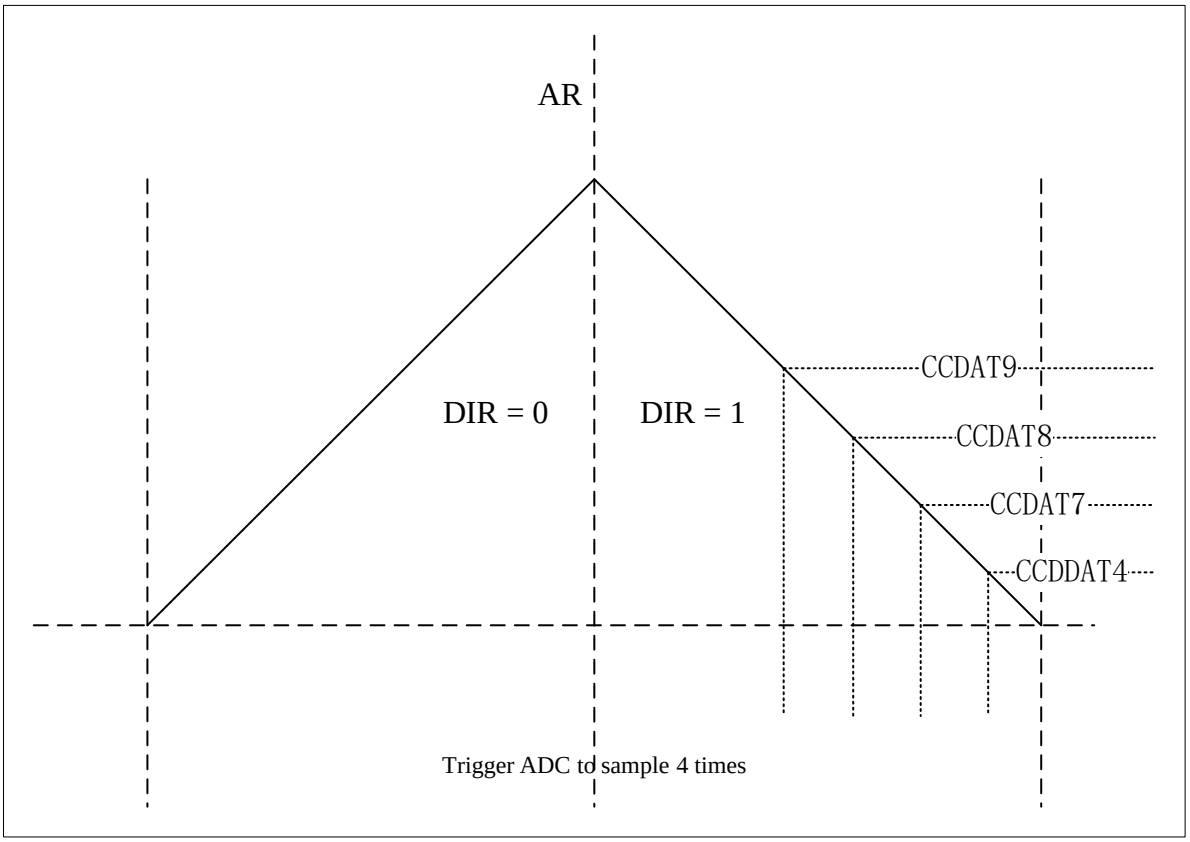
Figure 9-10 CCDATx(x=4, 7, 8, 9), Trigger ADC When DIR = 1



If TIMx_CTRL1.CMODE[1:0]=1x, the CCDATx.CCDAT and CCDATx.CCDDAT (x=4,7,8,9) value will trigger ADC when DIR =0 or DIR=1.

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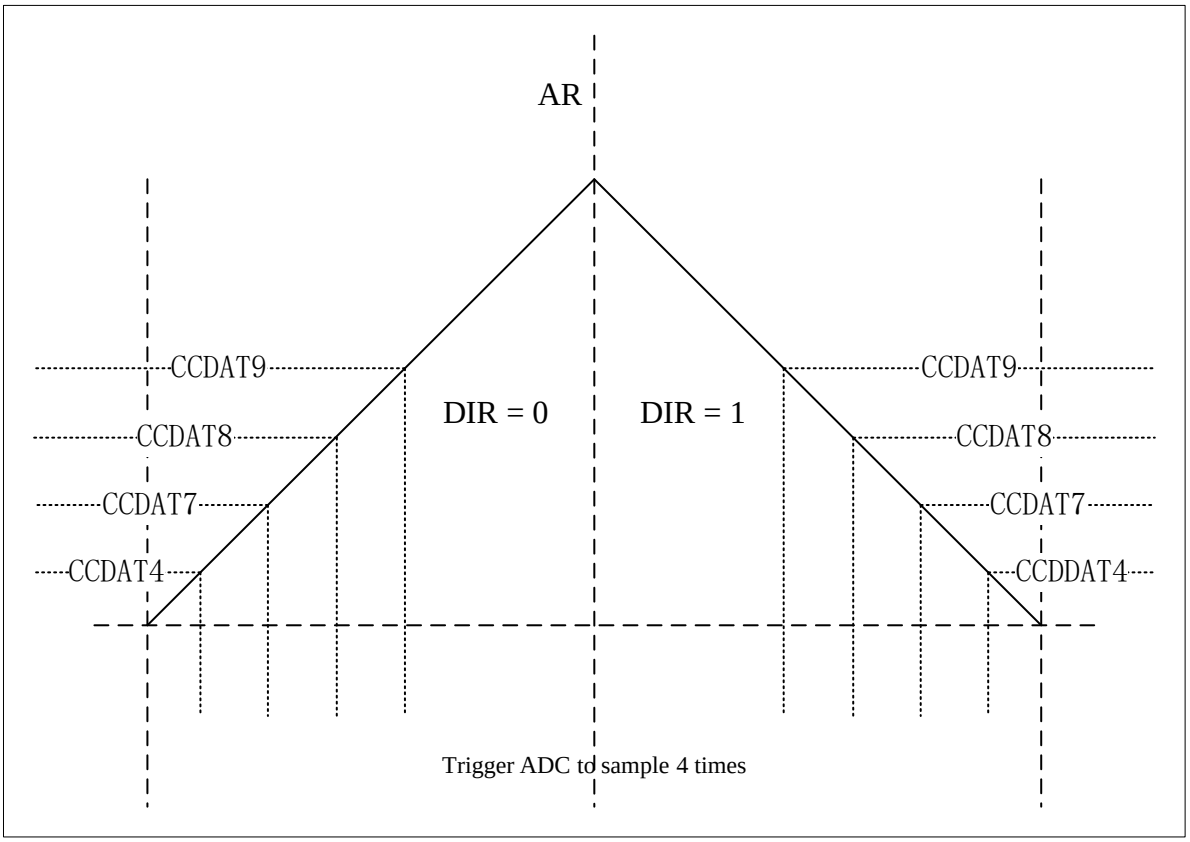
Figure 9-11 CCDATx(x=4, 7, 8, 9), Trigger ADC When DIR = 0 or DIR = 1



In the above figure, channel 4 up counting to CCDAT4 or down counting to CCDDAT4, channel 7/8/9 up counting or down counting to CCDAT7/8/9, trigger valid.

9.3.3 Repetition Counter

The basic unit of Section 9.3.1 describes the conditions for generating an update event (UEV). An update event (UEV) is actually only generated when the repetition counter reaches zero, which is valuable for generating PWM signals.

This means that data are transferred from the preload registers to the shadow registers every N+1 counter overflow or underflow, where N is the value in the TIMx_REPCNT.

The repetition counter is decremented:

- In the up-counting mode, each time the counter reaches the maximum value, an overflow occurs.
- In down-counting mode, each time the counter decrements to the minimum value, an underflow occurs.
- In center-aligned mode, each time the counter overflows or underflows.

Its repetition rate is defined by the value of the TIMx_REPCNT register.

Repetition counters feature automatic reloading. The update event (generated by setting TIMx_EVTGEN.UDGN or hardware through slave mode controller) occurs immediately, regardless of the value of the repeatition counter.

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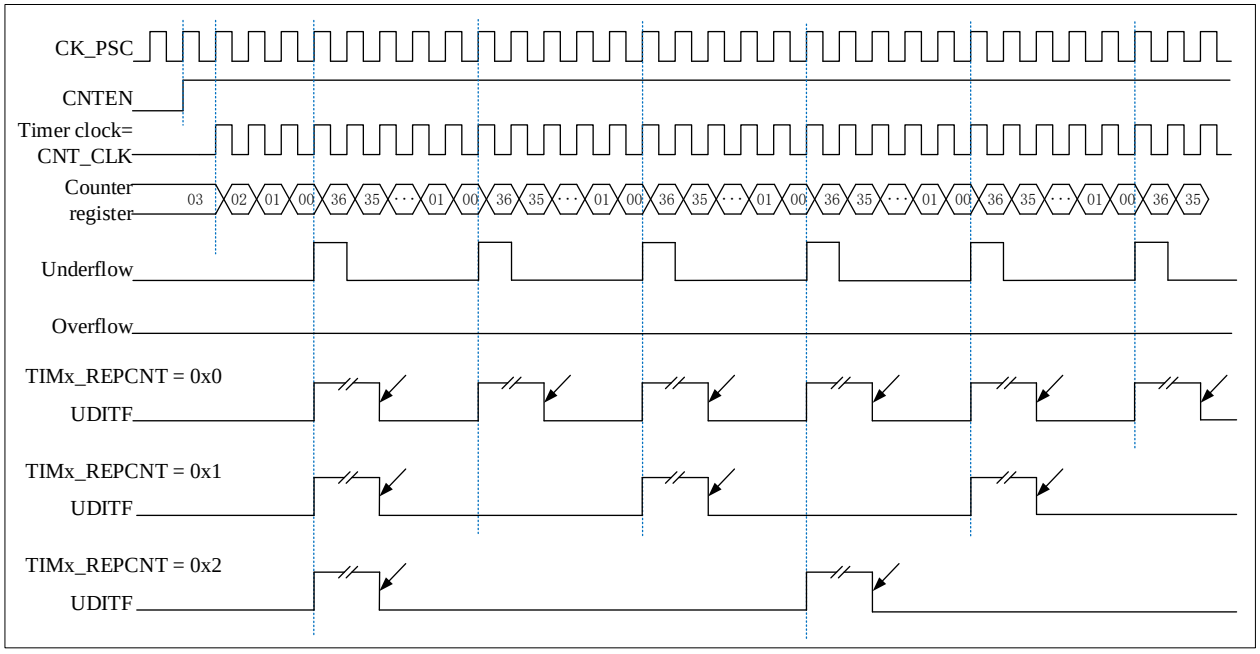
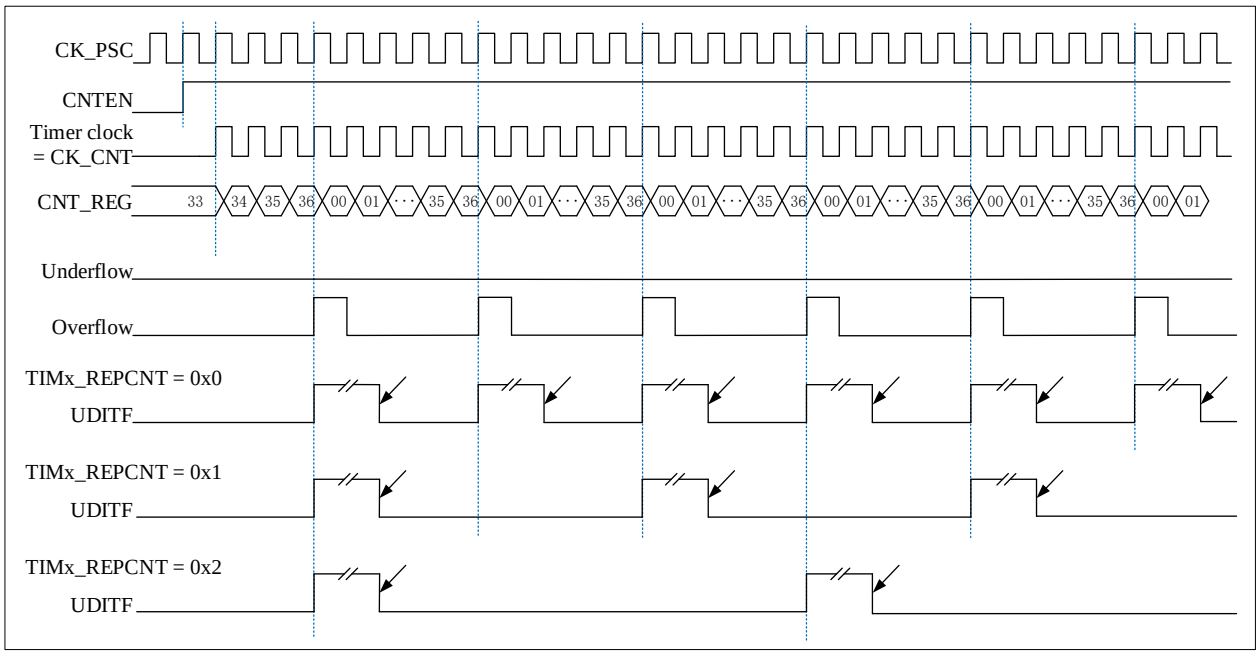
Figure 9-12 Repeat Count Sequence Diagram in Down-counting Mode



Software clear

Figure 9-13 Repeat Count Sequence Diagram in Up-counting Mode



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Nations Technologies Inc.
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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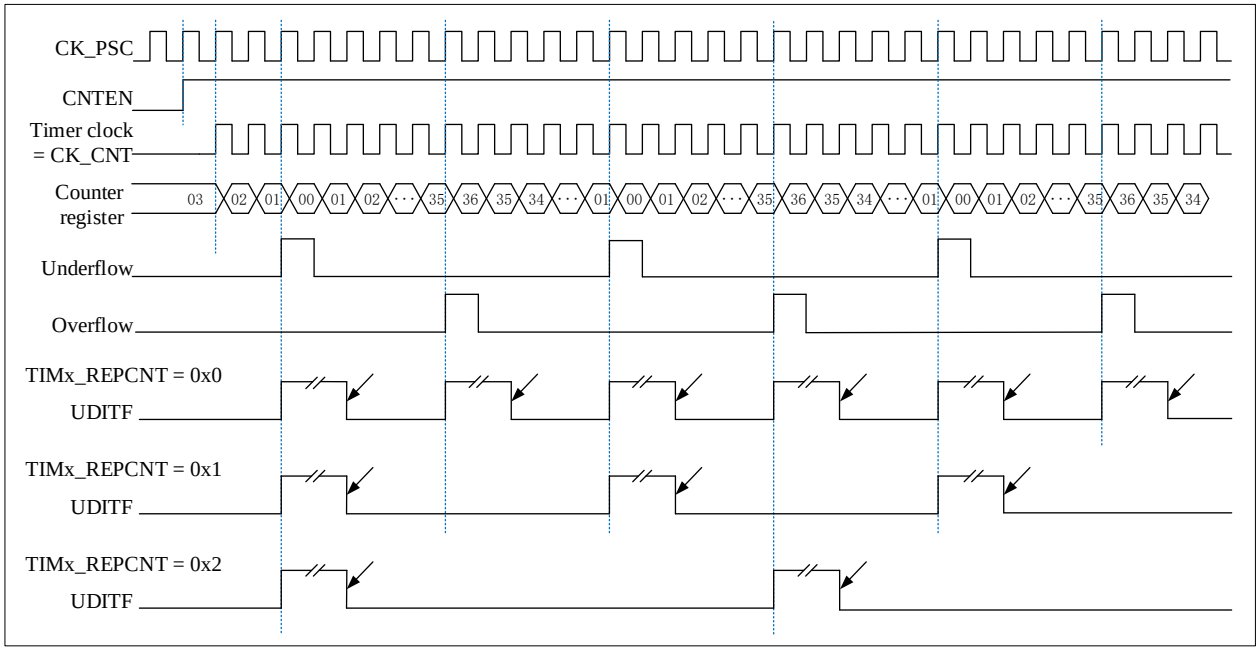
Figure 9-14 Repeat Count Sequence Diagram in Center-aligned Mode



9.3.4 Clock Selection

- The internal clock of Advanced-control timers: CK_INT
- Two kinds of external clock mode:
  - External input pin
  - External trigger input ETR
- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

9.3.4.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN, TIMx_CTRL1.DIR, TIMx_EVTGEN.UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as '1' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

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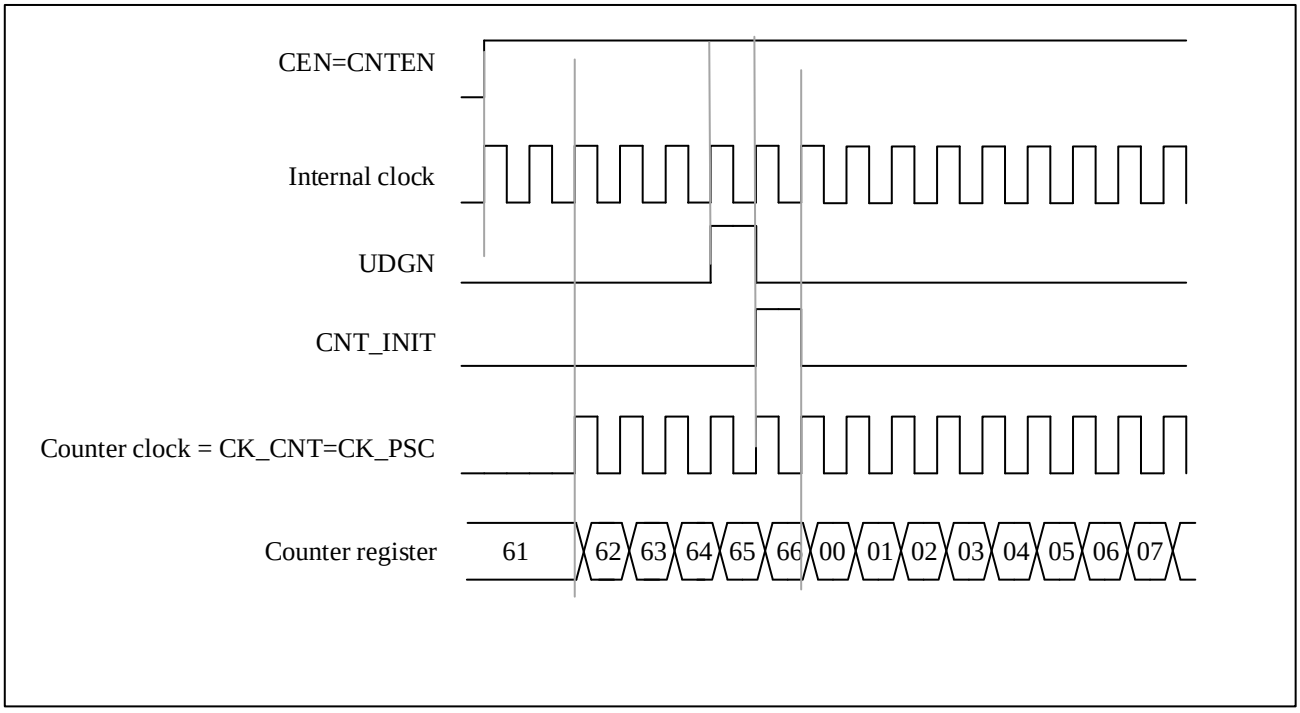
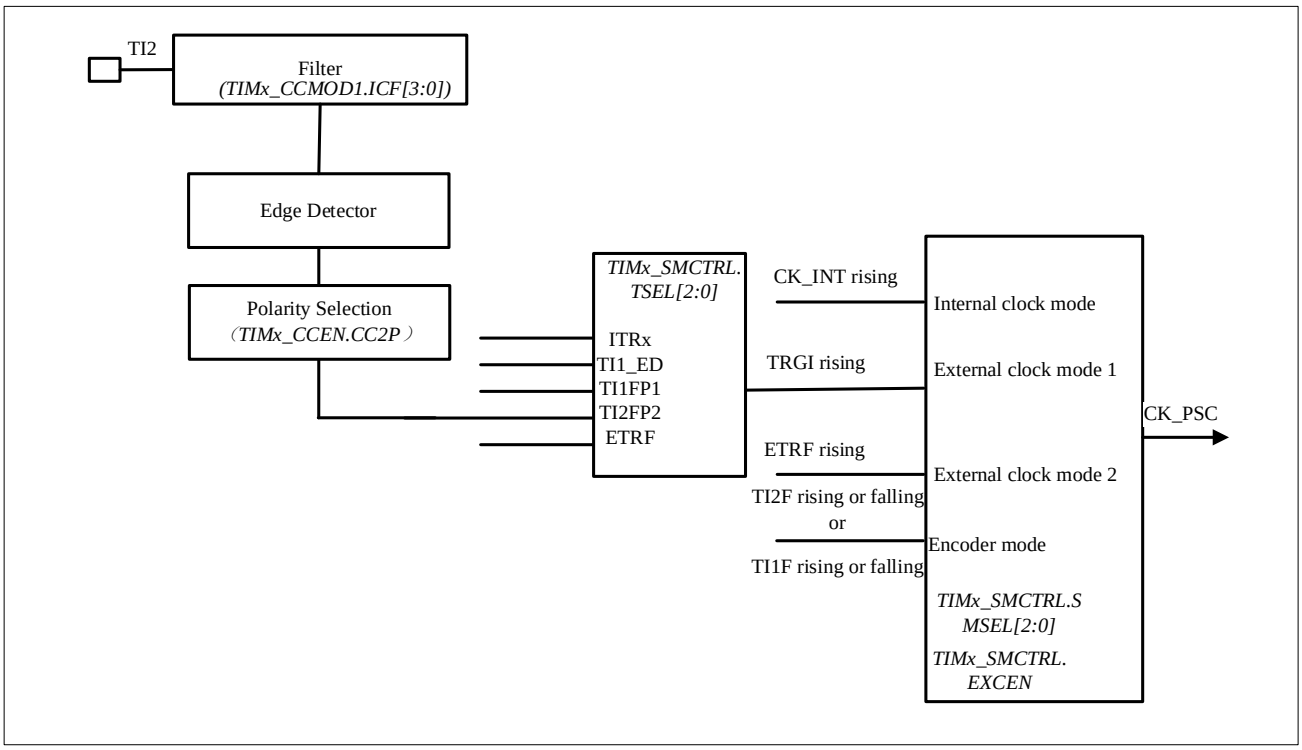
Figure 9-15 Control Circuit in Normal Mode, Internal Clock Divided By 1



9.3.4.2 External clock source mode 1

Figure 9-16 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

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For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

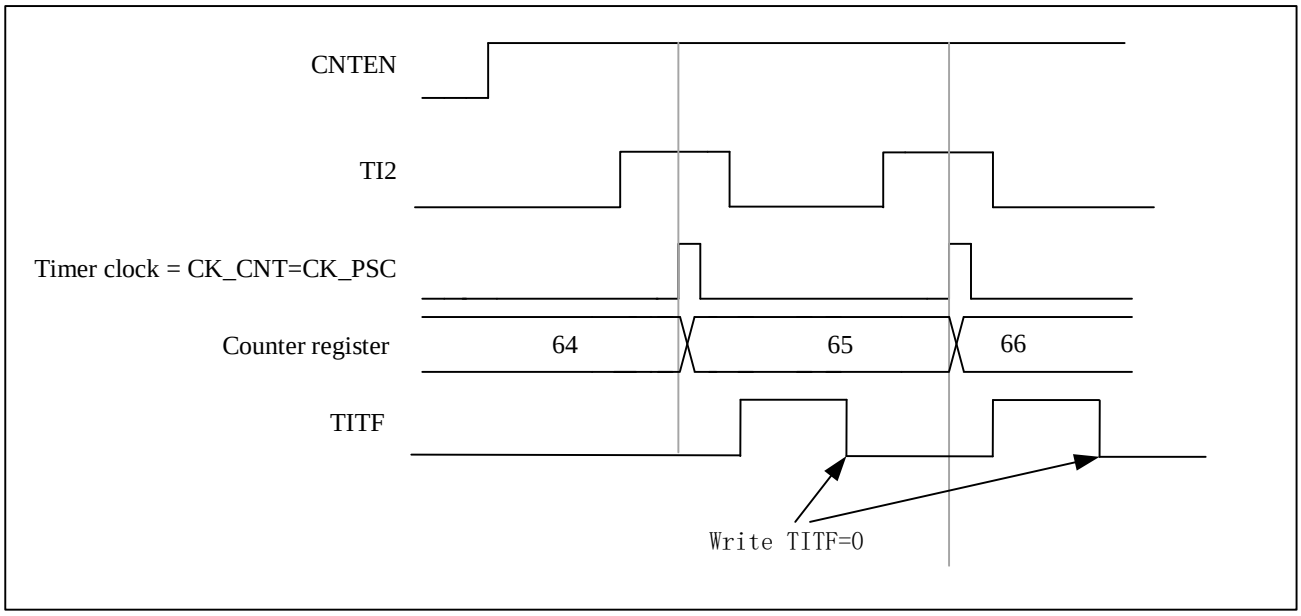
- Configure TIMx_CCMOD1.CC2SEL equal to '01', CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to '0', select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000')
- Configure TIMx_SMCTRL.SMSEL equal to '111', select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to '110', select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to '1' to start the counter

Note: the capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is set.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

Figure 9-17 Control Circuit in External Clock Mode 1



9.3.4.3 External clock source mode 2

This mode is set by configuring TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in external clock source mode 2.

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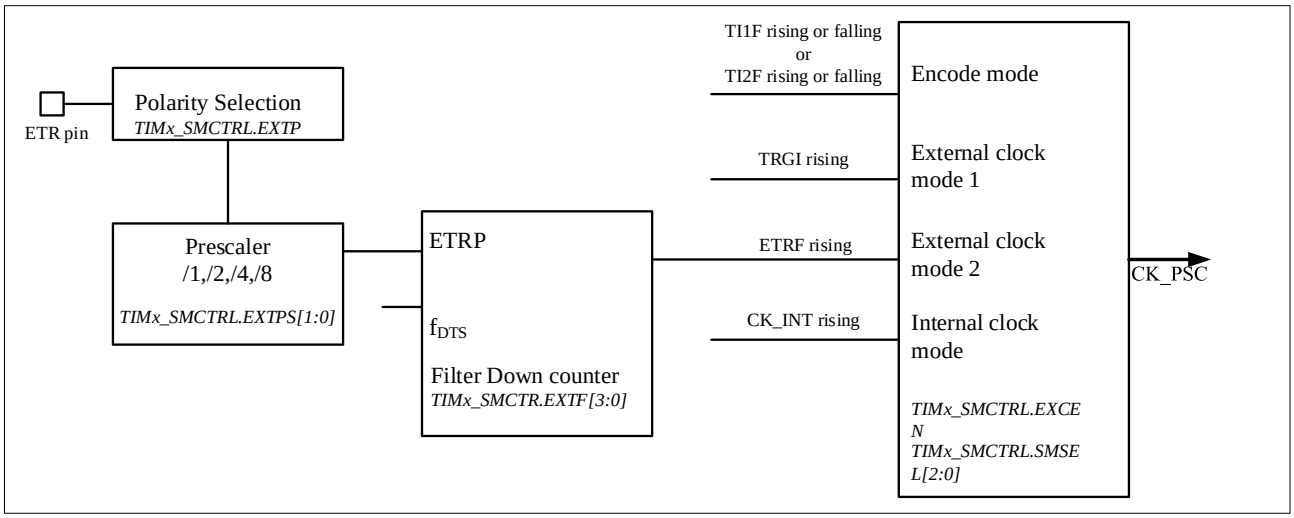
Figure 9-18 External Trigger Input Block Diagram

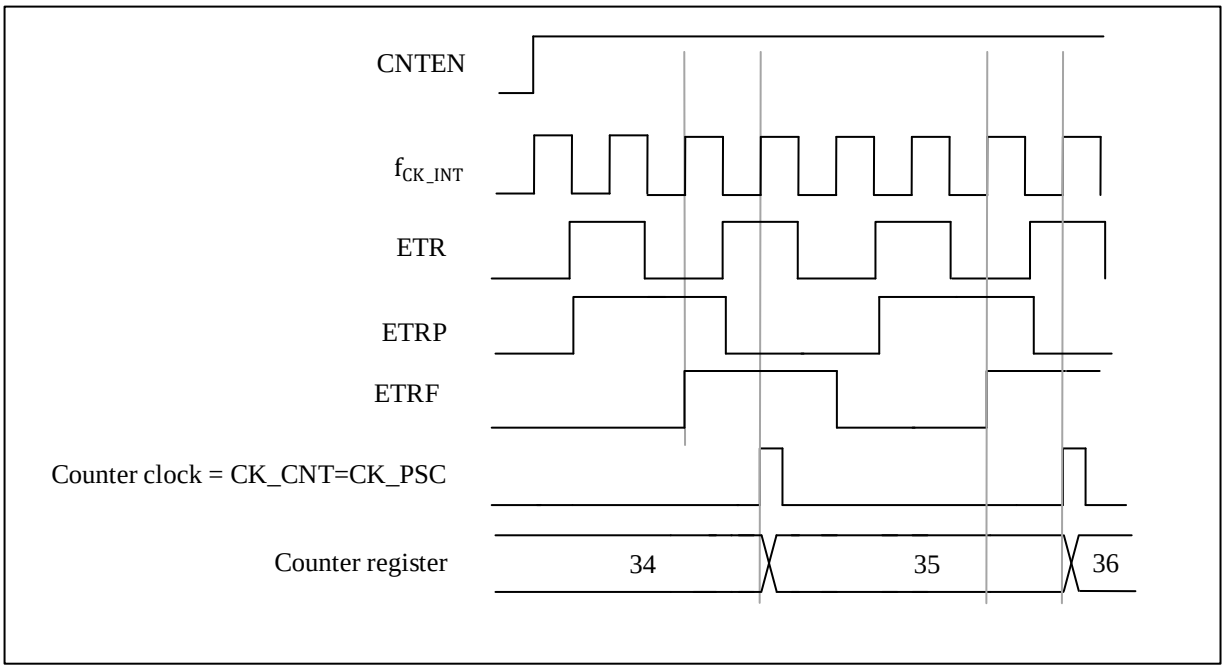


For example, use the following configuration steps to make the upcounter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', the rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock of the counter is due to a resynchronization circuit on the ETRP signal.

Figure 9-19 Control Circuit in External Clock Mode 2



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Email：info@nationstech.com
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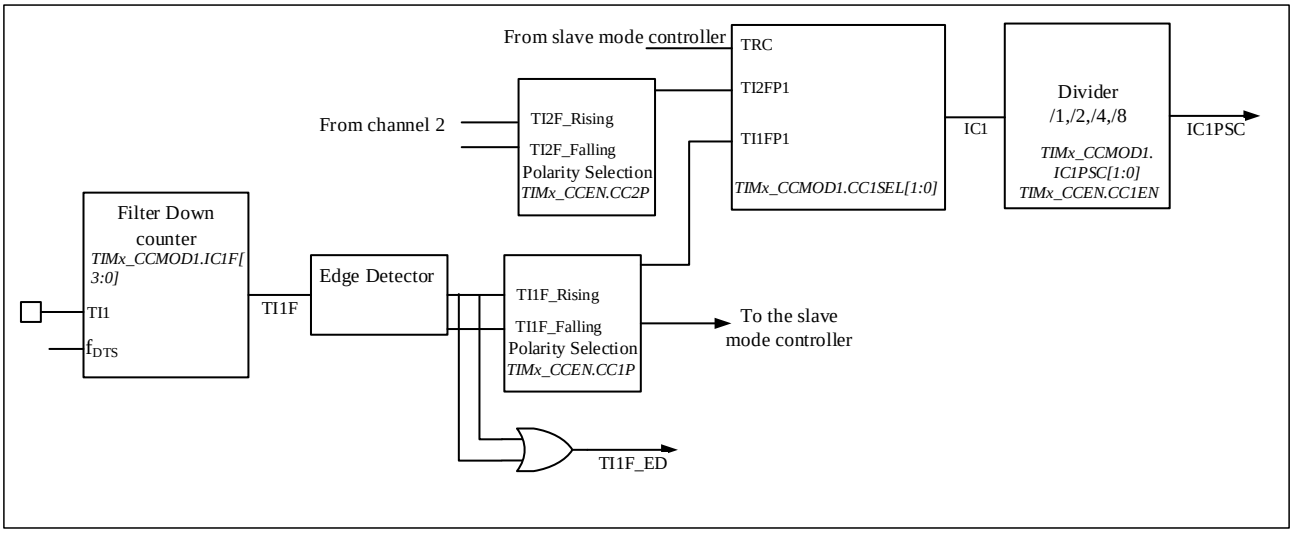
9.3.5 Capture/Compare Channels

The capture/compare channels include capture/compare registers and shadow registers. The input stage consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequencyprecaler. The following figure shows a block diagram of a capture/compare channel.

Figure 9-20 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output stage generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 9-21 Capture/Compare Channel 1 Main Circuit

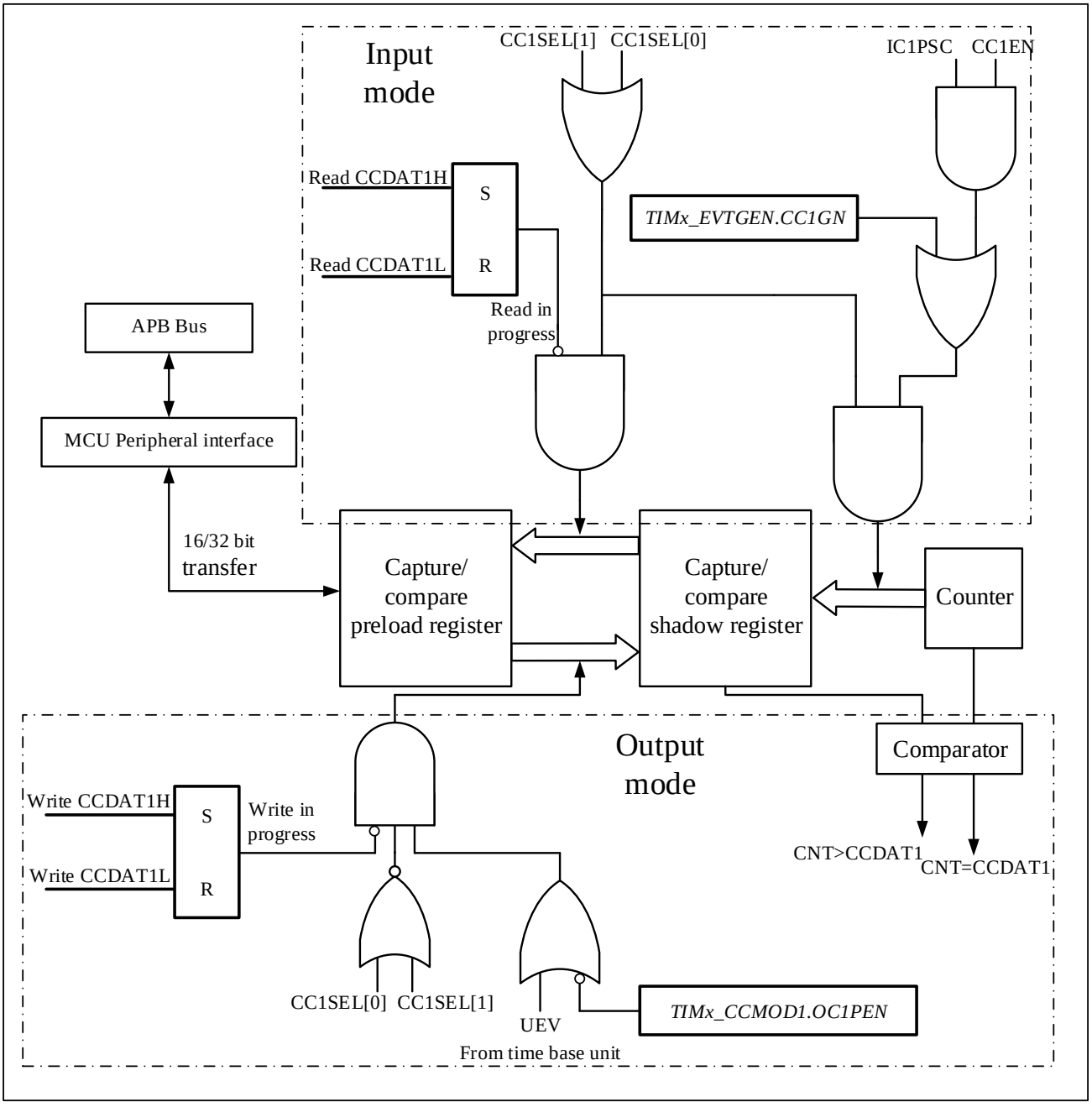

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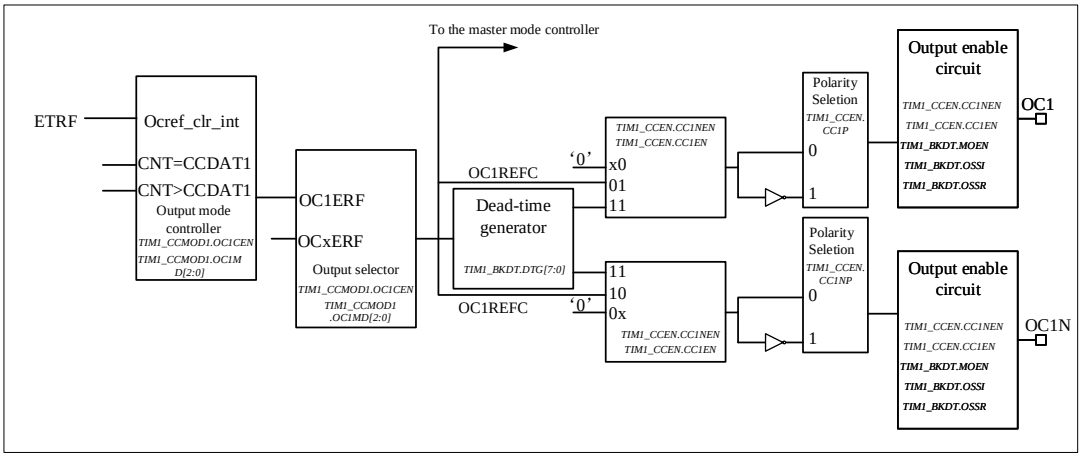
Figure 9-22 Output Part of Channelx (x= 1,2,3,4; Take Channel 1 as Example)



Reads and writes operations always access the preload registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

9.3.6 Input Capture Mode

In input capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can trigger an interrupt or DMA request if the corresponding interrupt enable is set.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already set. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Define the input filter duration required for programming:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to '0011'.

- Select the rising edge as the valid transition polarity on the TI1 channel by configuring TIMx_CCEN .CC1P=0.

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- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= ‘00’ to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = ‘1’.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

9.3.7 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to ‘01’ to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to ‘0’ to select the active polarity of filtered timer input 1(TI1FP1), active on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to ‘10’ select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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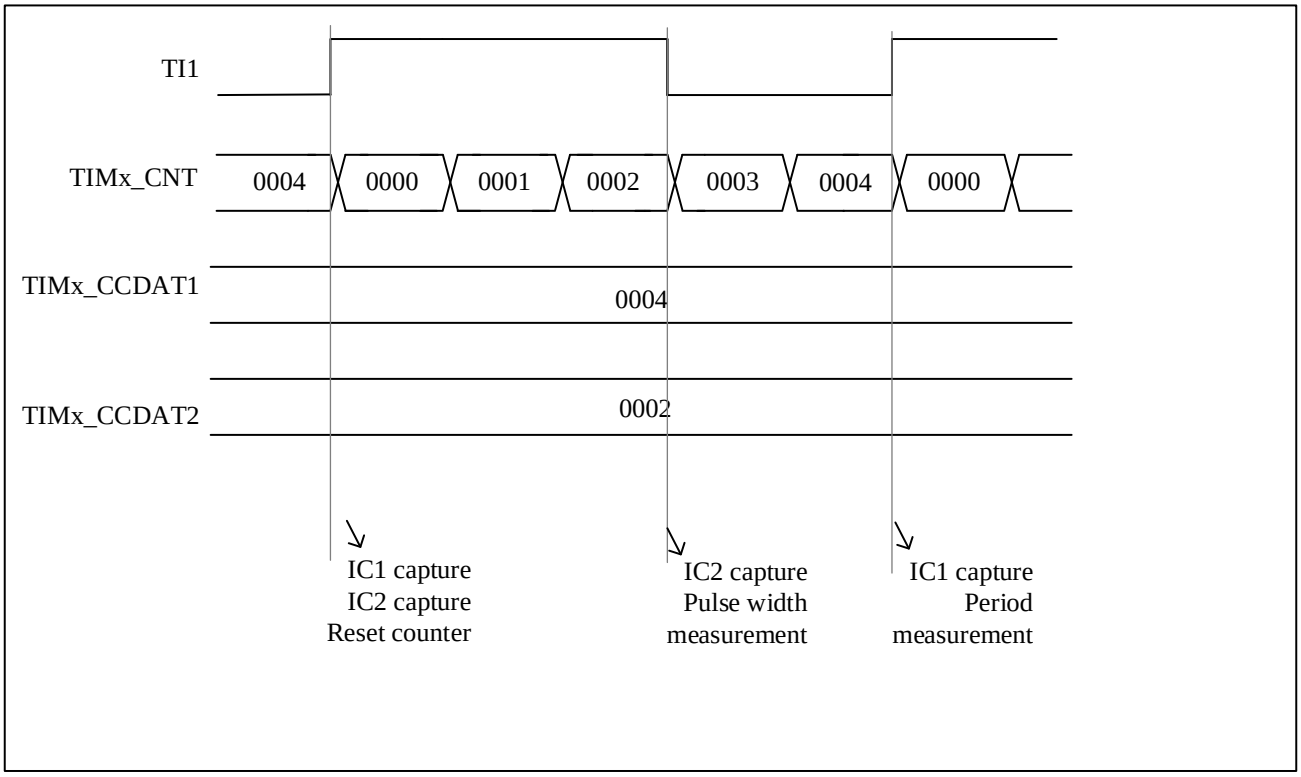
Figure 9-23 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

9.3.8 Forced Output Mode

In output mode (TIMx_CCMODx.CCxSEL=00), software can force output compare signals to active or inactive level directly.

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to low level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

9.3.9 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.
- Set TIMx_STS.CCxITF.

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- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

The TIMx_CCDATx registers can be programmed with or without preload registers using the TIMx_CCMODx.OCxPEN register.

The time resolution is one count period of the counter.

In one-pulse mode, the output compare mode can also be used to output a single pulse.

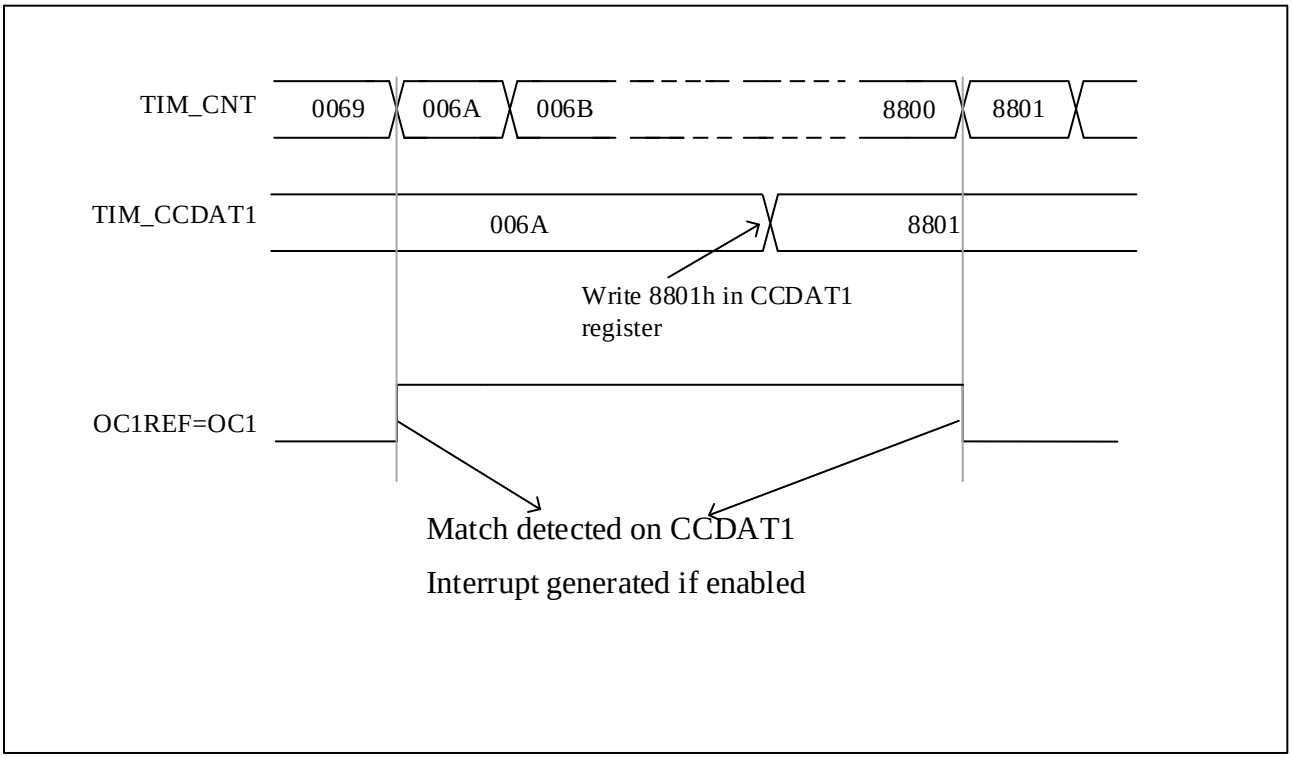
Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, write the desired data in the TIMx_AR and TIMx_CCDATxregisters.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by writting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

Figure 9-24 Output Compare Mode, Toggle on OC1



9.3.10 PWM Mode

Pulse width modulation mode is used to generate a signal with a frequency determined by the value of the TIMx_AR

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Tel：+86-755-86309900
Email：info@nationstech.com
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register and a duty cycle determined by the value of the TIMx_CCDATx register. And depending on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can select PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN, and then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can program polarity of OCx by setting TIMx_CCEN.CCxP. On the other hand, to enable the output of OCx, user need to set the combination of the value of CCxEN, CCxNEN, MOEN, OSSI, and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only when an update event occurs, the preload register will be transferred to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

9.3.10.1 **PWM center-aligned mode**

If user set TIMx_CTRL1.CAMSEL equal to 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or both when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

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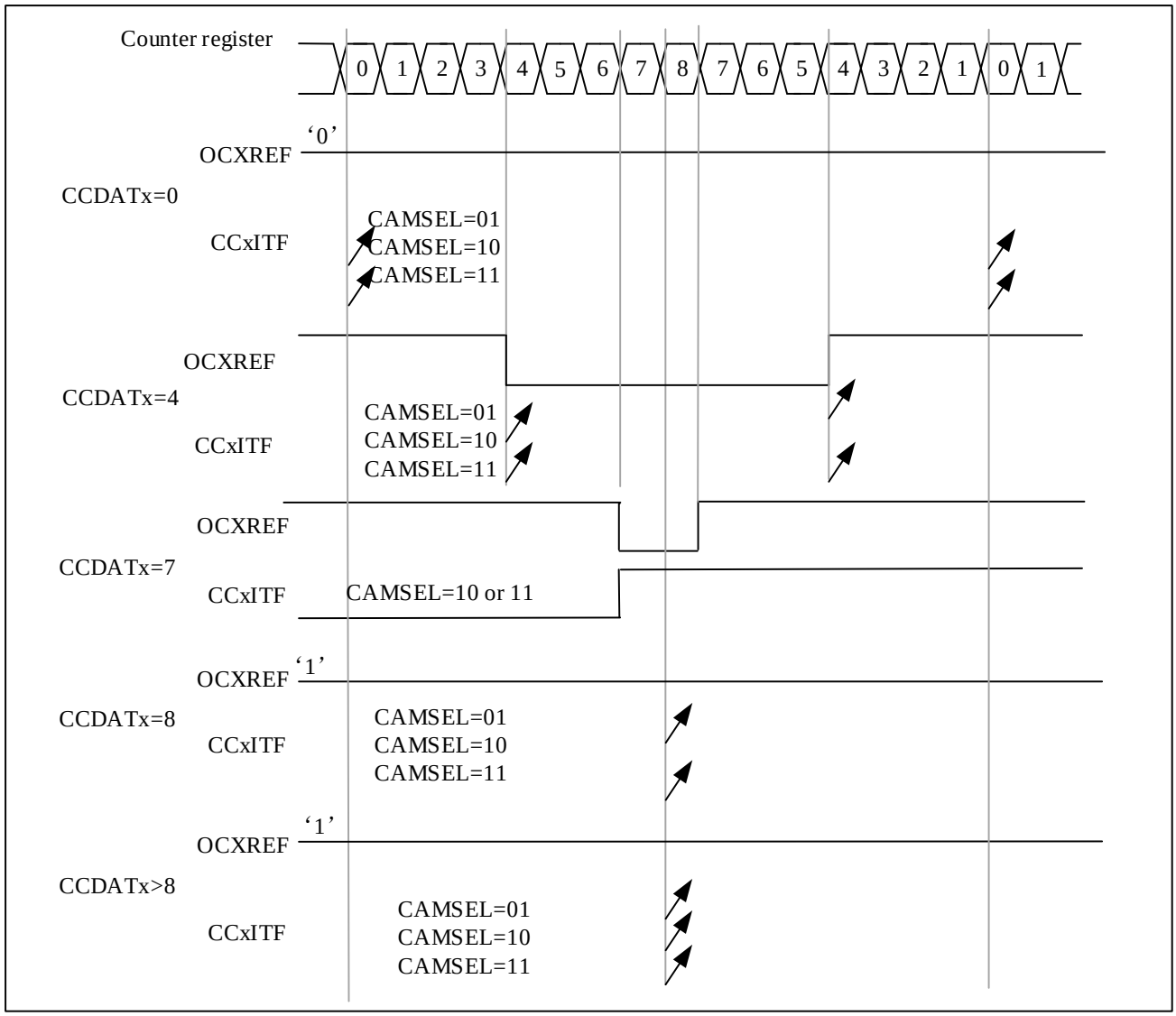
Figure 9-25 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considrations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- For safety reasons, it is recommended that users set TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and do not write the counter while it is running.

9.3.10.2 PWM center-aligned asymmetric mode

About PWM center-aligned asymmetric mode, refer to Section 9.3.2.3.2.

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Email：info@nationstech.com
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9.3.10.3 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

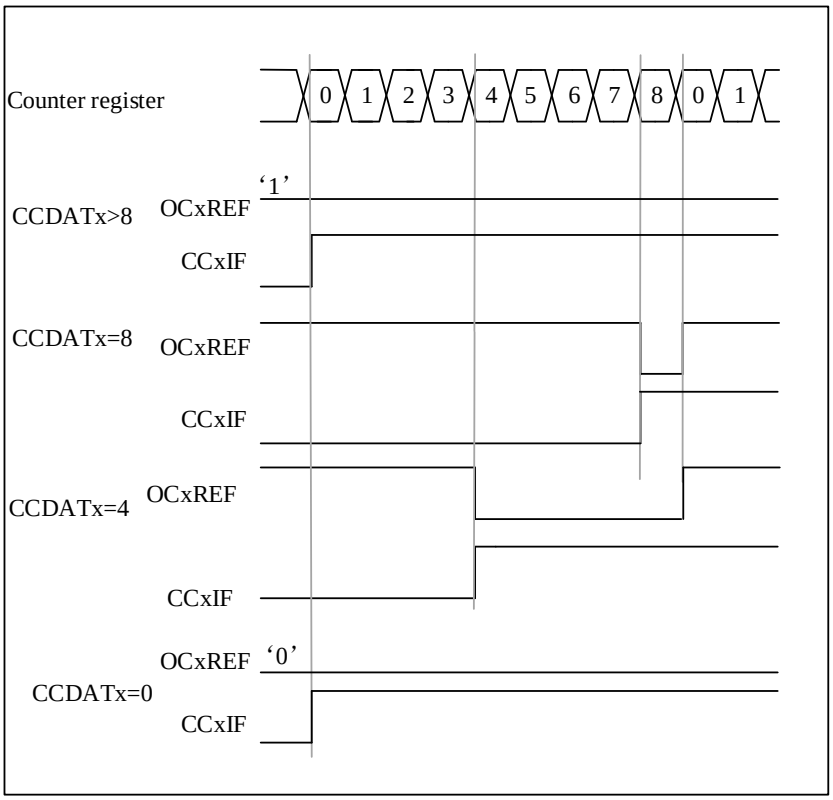
User can set TIMx_CTRL1.DIR=0 to make counter count up.

Example for PWM mode1:

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follows.

Figure 9-26 Edge-aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Example for PWM mode1:

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: if the n_{th} PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the $(n+1)_{th}$ PWM cycle is 0. At the moment when the counter is 0 in the $(n+1)_{th}$ PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

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Email：info@nationstech.com
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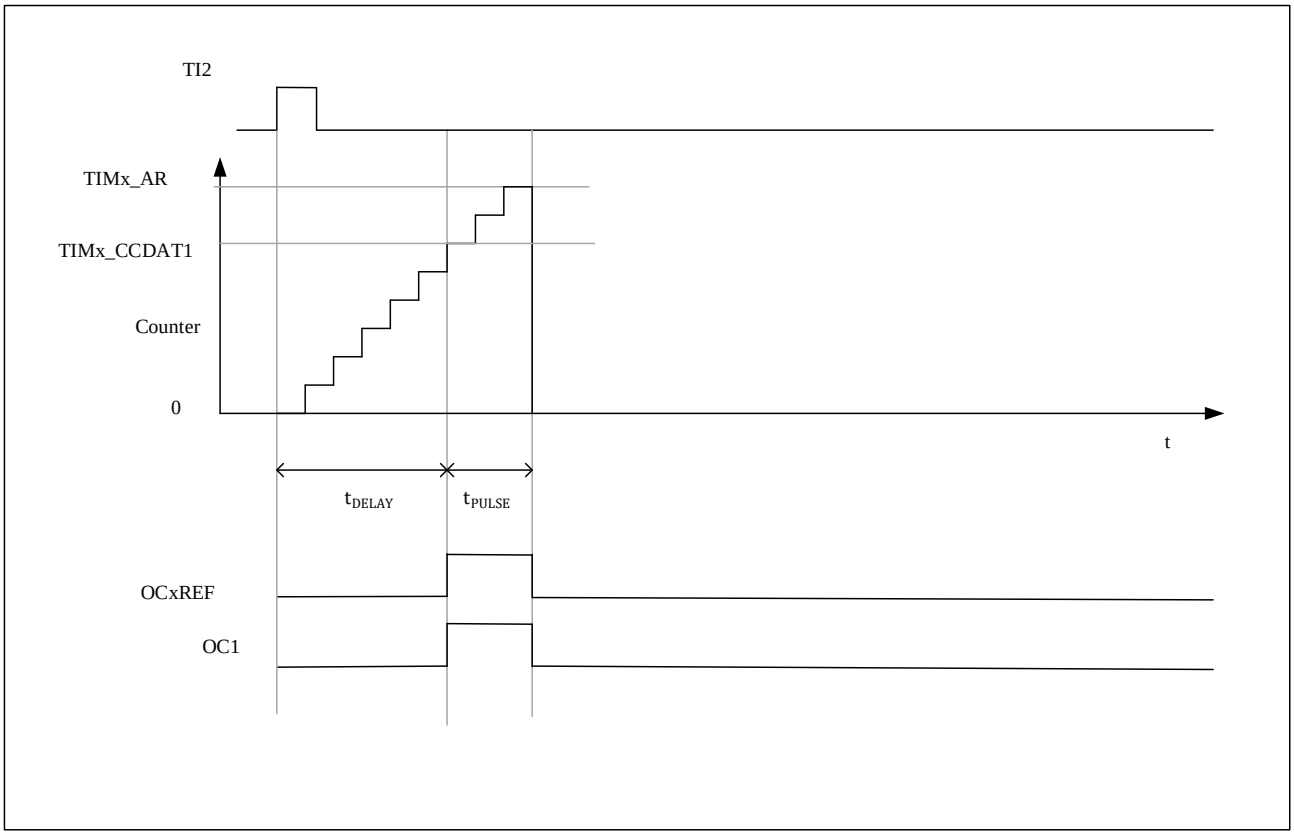
9.3.11 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 9-27 Example of One-pulse Mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= ‘01’; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= ‘0’;
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= ‘110’, TIMx_SMCTRL.SMSEL= ‘110’ (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};
5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = ‘111’ to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1.

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Email：info@nationstech.com
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9.3.11.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

9.3.12 Clearing the OCxREF signal on an external event

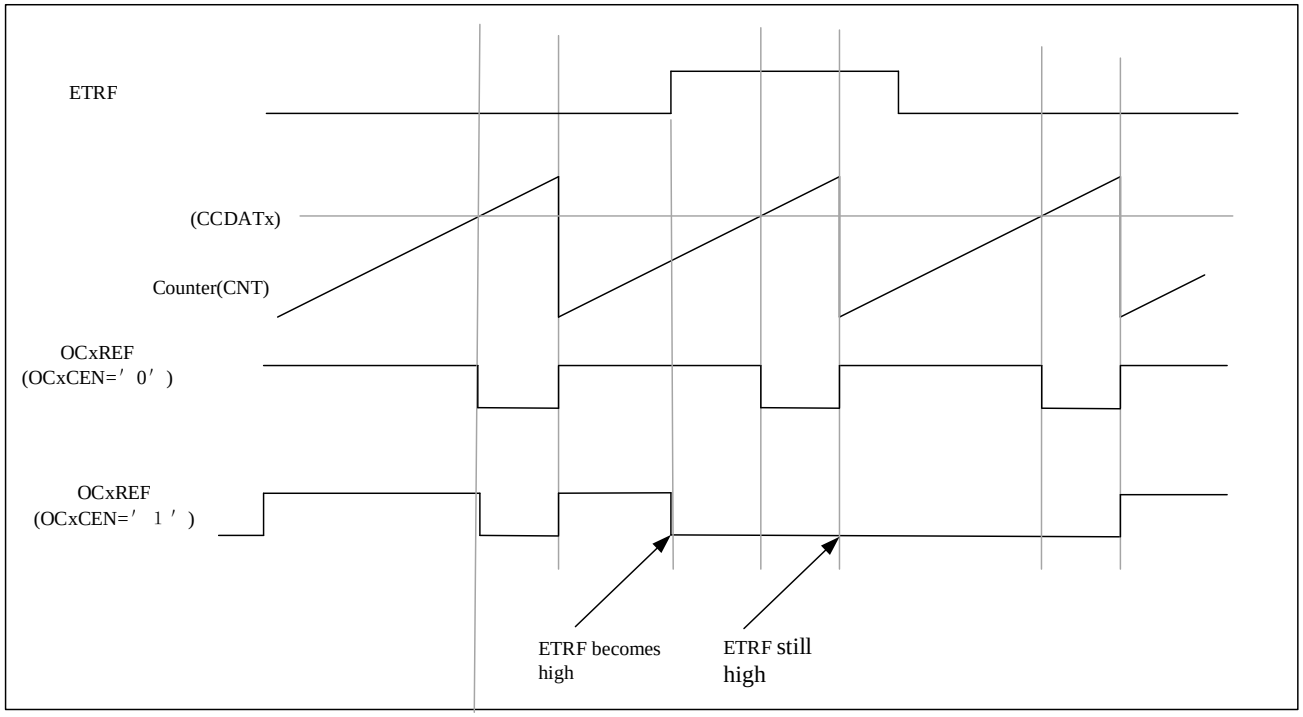
If the user sets TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only Output Compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Example: When the tim_ocref_clr_in signal is selected as ETRF, the tim_etr_in configuration is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

For example: The following diagram shows when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 9-28 Clearing the OCxREF of TIMx



9.3.13 Complementary Outputs and Dead-time Insertion

The advanced-control timer can output two complementary signals, and manage the switching-off and switching-on

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instants of outputs. This time is generally known as dead-time. User should adjust dead-time depending on the devices connected to the outputs and their characteristics.

User can select the polarity of outputs by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP. And this selection is independently for each output.

User can control the complementary signals OCx and OCxN by setting the combination of several control bits, which are TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. When switching to the IDLE state, the dead-time will be activated.

If user set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN at the same time, a dead-time will be insert. If there is a break circuit, the TIMx_BKDT.MOEN should be set too. There are 10-bit dead-time generators for each channel.

Reference waveform OCxREF can generates 2 outputs OCx and OCxN. And if OCx and OCxN are active high, the OCx ouput signal is the same as the reference signal and the OCxN output signal is the opposite of the reference signal. However, OCx output signal will be delayed relative to the reference rising edge and the OCxN output signal will be delayed relative to the reference falling edge. If the delay is greater than the width of the active OCx or OCxN output, the corresponding pulse will not generated.

The relationships between the output signals of the dead-time generator and the reference signal OCxREF are as follow.

Assume that TIMx_CCEN.CCxP=0, TIMx_CCEN.CCxNP=0, TIMx_BKDT.MOEN=1, TIMx_CCEN.CCxEN=1, TIMx_CCEN.CCxNEN=1.

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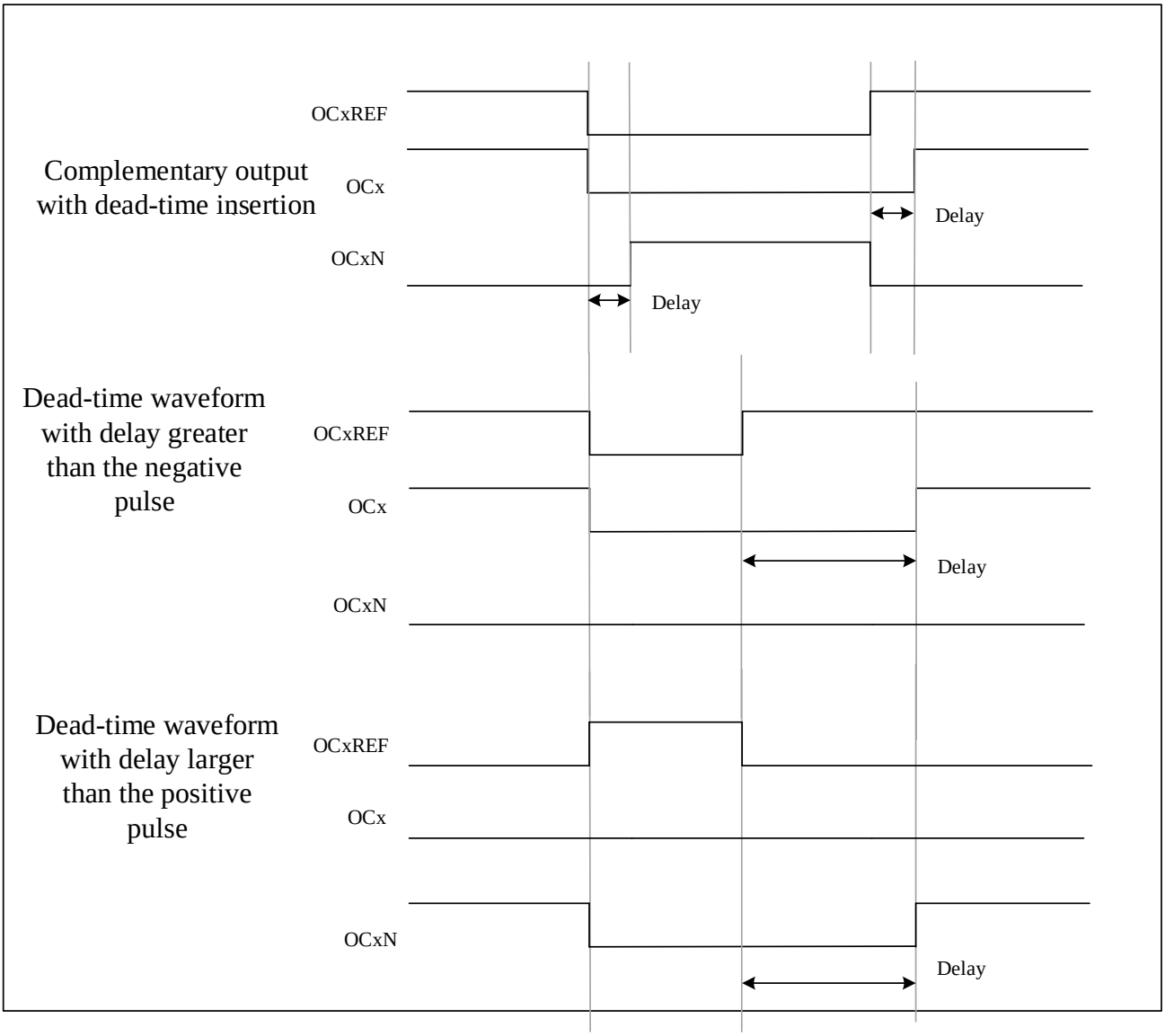
Figure 9-29 Complementary Output with Dead-time Insertion



User can set TIMx_BKDT.DTGN to programme the dead-time delay for each of the channels.

9.3.13.1 **Redirecting OCxREF to OCx or OCxN**

In output mode, user can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to re-directed OCxREF to the OCx output or to OCxN output.

Here are two ways to use this function. When the complementary remains at its inactive level, user can use this function to send a specific waveform, such as PWM or static active level. User can also use this function to set both outputs in their inactive level or both outputs active and complementary with dead-time.

If user set TIMx_CCEN.CCxEN=0 and TIMx_CCEN.CCxNEN=1, it will not complemented, and OCxN will become active when OCxREF is high. On the other hand, if user set TIMx_CCEN.CCxEN=1 and TIMx_CCEN.CCxNEN=1, OCx will become active when OCxREF is high. On the contrary, OCxN will become active when OCxREF is low.

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9.3.14 Break Function

The output enable signals and inactive levels will be modified when setting the corresponding control bits when using the break function. However, the output of OCx and OCxN cannot at the active level at the same time no matter when, that is, (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0.

When multiple break signals are enabled, each break signal constitutes an OR logic. Here are some signal which can be the source of break and break2.

Break:

- The break input pin
- A clock failure event, generated by the clock security system (CSS) in the clock controller
- A PVD failure event
- Core Hardfault event
- The output signal of the comparator
- By software through the TIMx_EVTGEN.BGN

The break circuit will be disable after reset. And the MOEN bit will be low. User can set TIMx_BKDT.BKEN to enable the break function. The polarity of break input signal can be selected by setting TIMx_BKDT.BKP. User can modify the TIMx_BKDT.BKEN and TIMx_BKDT.BKP at the same time. After user set the TIMx_BKDT.BKEN and TIMx_BKDT.BKP, there is 1 APB clock cycle delay before the configuration take effect. Therefore, user need to wait 1 APB clock cycle to read back the written bit value.

The falling edge of MOEN can be asynchronous, so a resynchronization circuit has been inserted between the actual signal and the synchronous control bit. This circuit will cause a delay between the asynchronous and the synchronous signal. When user set TIMx_BKDT.MOEN while it is low, user need to insert a delay before reading the value. Because an asynchronous signal was written but user read the synchronous signal.

The behaviors that after a break occurs are as follow:

- TIMx_BKDT.MOEN will be cleared asynchronously, and then the outputs will be put in inactive state, idle state or reset state. The state of output is selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is off.
- Once TIMx_BKDT.MOEN=0, the output of each output channel will be driven with the level programmed in TIMx_CTRL2.OIx. Timer will release the enable outputs (taken over by GPIO controller) if TIMx_BKDT.OSSI=0, otherwise it will remain high.
- If user choose to use complementary outputs, the behaviors of TIM are as follow:
  - Depends on the polarity, the outputs will be set in reset state first. It is an asynchronous option so it still works even if there is no clock provided to the timer.
  - The dead-time generator will be reactivated if the timer clock is still provided, and drive the outputs according to the value of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN after the dead-time when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0, that is, the OCx and OCxN still cannot be driven to active level at the same time. Note that the dead-time will be longer than usual because of the resynchronization on MOEN (almost 2 cycles of ck_tim).

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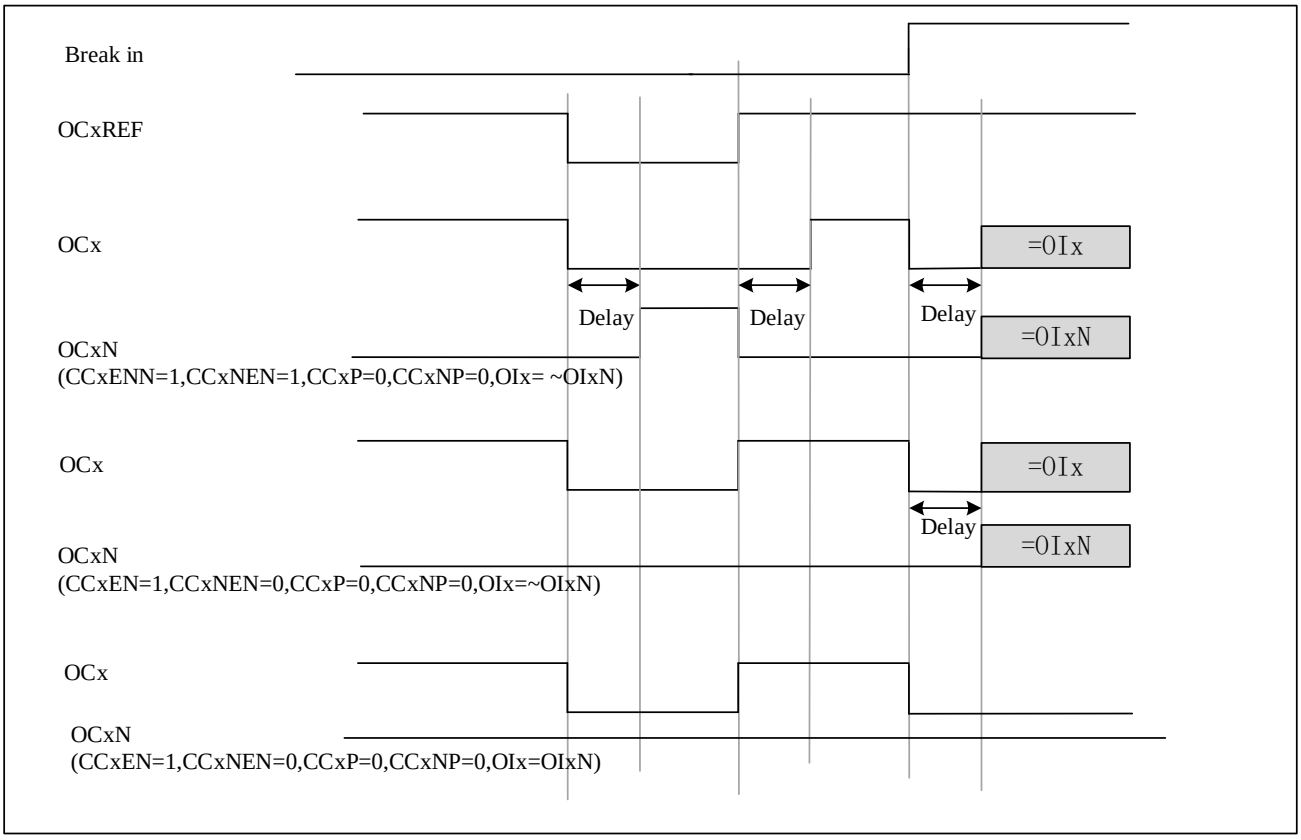
– Timer will release the output control if TIMx_BKDT.OSSI=0. Otherwise, if the enable output was high, it will remain high. If it was low, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is high.

- If TIMx_DINTEN.BIEN=1, when TIMx_STS.BITF=1, an interrupt will be generated.
- If user set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will be set automatically when the next UEV happened. User can use this to regulate. If user did not set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will remain low until been set 1 again. At this situation, user can use this for security. User can connect the break input to thermal sensors, alarm for power drivers, or other security components.
- When the break input is active, TIMx_BKDT.MOEN cannot be set automatically or by software at the same time, and the TIMx_STS.BITF cannot be cleared. Because the break inputs are active on level.

To ensure the security of application, the break circuit has the write protection function, and there is break input and output management too. It allow user to freeze some parameters, such as dead-time duration, OCx/OCxN polarities and state when disabled, OCxMD configurations, break enable and polarity. User can choose one of the 3 levels of protection to use by setting TIMx_BKDT.LCKCFG. However, the TIMx_BKDT.LCKCFG can only be written once after an MCU reset.

An example for output behavior in response to a break is as follow.

Figure 9-30 Output Behavior in Response to a Break



9.3.14.1 **Break filter**

Register TIMx_BKFR description are as follow:

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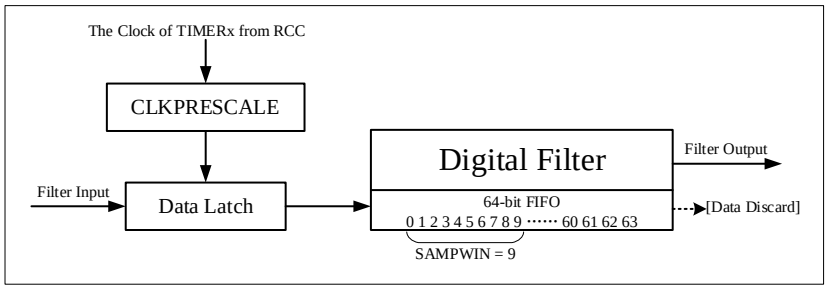
Figure 9-31 Silde Filter



- The digital filter samples break signal at the clock of TIMx from RCC, accumulating samples in a 64-bits FIFO. Only sampled data within window size defined in TIMx_BKFR.WSIZE [5:0] with maximum size 64.
- The filter outputs the majority value inside sample window which is defined by the threshold value in TIMx_BKFR.THRESH [5:0] with maximum threshold of 63. This value should be equal or more than half of window size. If neither logic 1 nor logic 0 counts inside sampling window is more than threshold, digital filter maintain previous output value.
- TIMx_BKFR.PSC [15:0] register determines sample rate of corresponding digital filter. Filter FIFO capture one sample value from input at every sample clock.
- If digital filter is off, filter input will bypass to output like a wire.

9.3.15 Debug Mode

When the microcontroller is in debug mode (the Cortex-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. Refer to Section 3.4.9 for detail.

9.3.16 TIMx and External Trigger Synchronization

TIMx can be synchronized by a trigger in slave modes (reset, trigger and gated).

9.3.16.1 **Slave mode: reset mode**

In reset mode, the trigger event can reset the counter and the prescaler updates the preload registers TIMx_AR, TIMx_CCDATx, and generates the update event UEV (TIMx_CTRL1.UPRS=0).

The following is an example of a reset mode:

- Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);
- The slave mode is selected as reset mode (TIMx_SMCTRL.SMSEL=100), and the trigger input is selected as TI1 (TIMx_SMCTRL.TSEL=101);
- Setting TIMx_CTRL1.CNTEN = 1 to start counter;

After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI1 and the actual reset of the counter is due to the resynchronization circuit on TI1 input.

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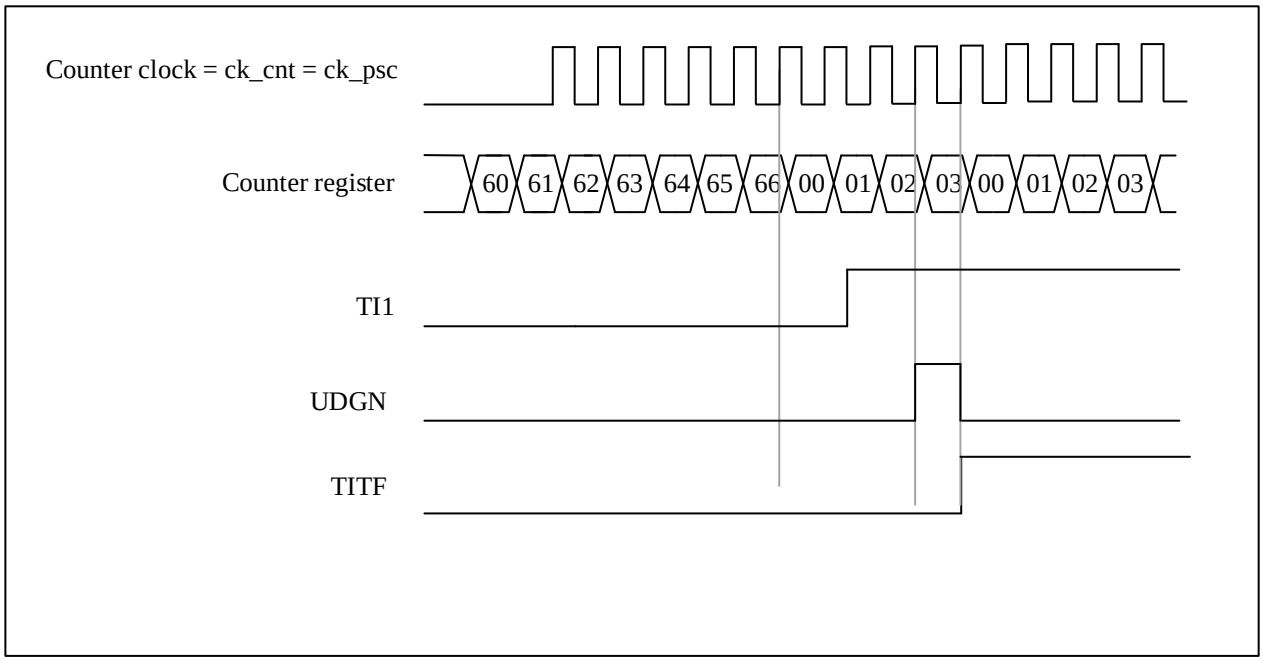
Figure 9-32 Control Circuit in Reset Mode



9.3.16.2 **Slave mode: trigger mode**

In trigger mode, the trigger event (rising edge/falling edge) of the input port can trigger the counter to start counting.

The following is an example of a trigger pattern:

- Channel 2 is configured as input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01, TIMx_CCEN.CC2P=0);
- Select from mode to trigger mode (TIMx_SMCTRL.SMSEL=110), select TI2 for trigger input (TIMx_SMCTRL.TSEL=110);

When a rising edge is detected on TI2, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI2 and the actual start of the counter is due to the resynchronization circuit on TI2 input.

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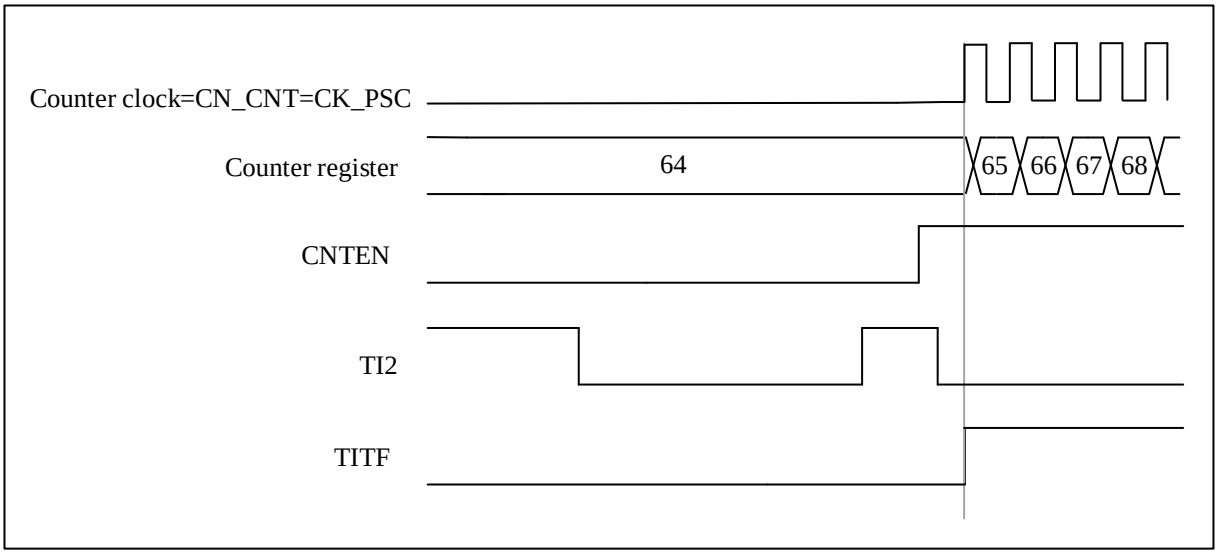
Figure 9-33 Control Circuit in Trigger Mode



9.3.16.3 **Slave mode: gated mode**

In gated control mode, the level polarity of the input port can control whether the counter counts or not.

The following is an example of a gated mode:

- Channel 1 is configured as input detection active low on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1);
- Select the slave mode as the gated mode (TIMx_SMCTRL.SMSEL=101), and select TI1 as the trigger input (TIMx_SMCTRL.TSEL=101);
- Setting TIMx_CTRL1.CNTEN = 1 to start counter

When TI1 detects that the level changes from low to high, the counter stops counting, and when TI1 detects that the level changes from high to low, the counter starts counting, and the trigger flag will be set (TIMx_STS.TITF=1) when it starts or stops counting;

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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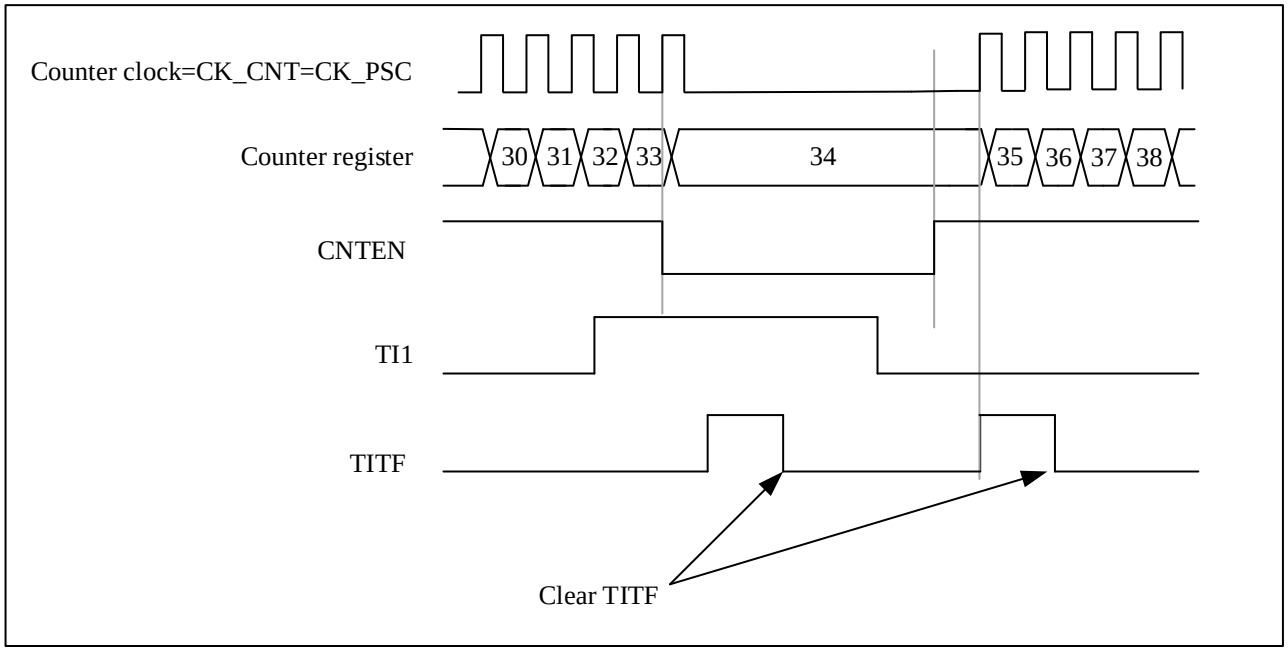
Figure 9-34 Control Circuit in Gated Mode



9.3.16.4 **Slave mode: trigger mode + external clock mode 2**

In reset mode, trigger mode and gate control mode, the counter clock can be selected as external clock mode 2, and the ETR signal is used as the external clock source input. At this time, the trigger selection needs to select non-ETRF (TIMx_SMCTRL.TSEL=111).

Here is an example:

- Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0),
- Enable external clock mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=110), select TI1 for trigger input (TIMx_SMCTRL.TSEL=101),

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and the trigger flag is set (TIMx_STS.TITF=1).

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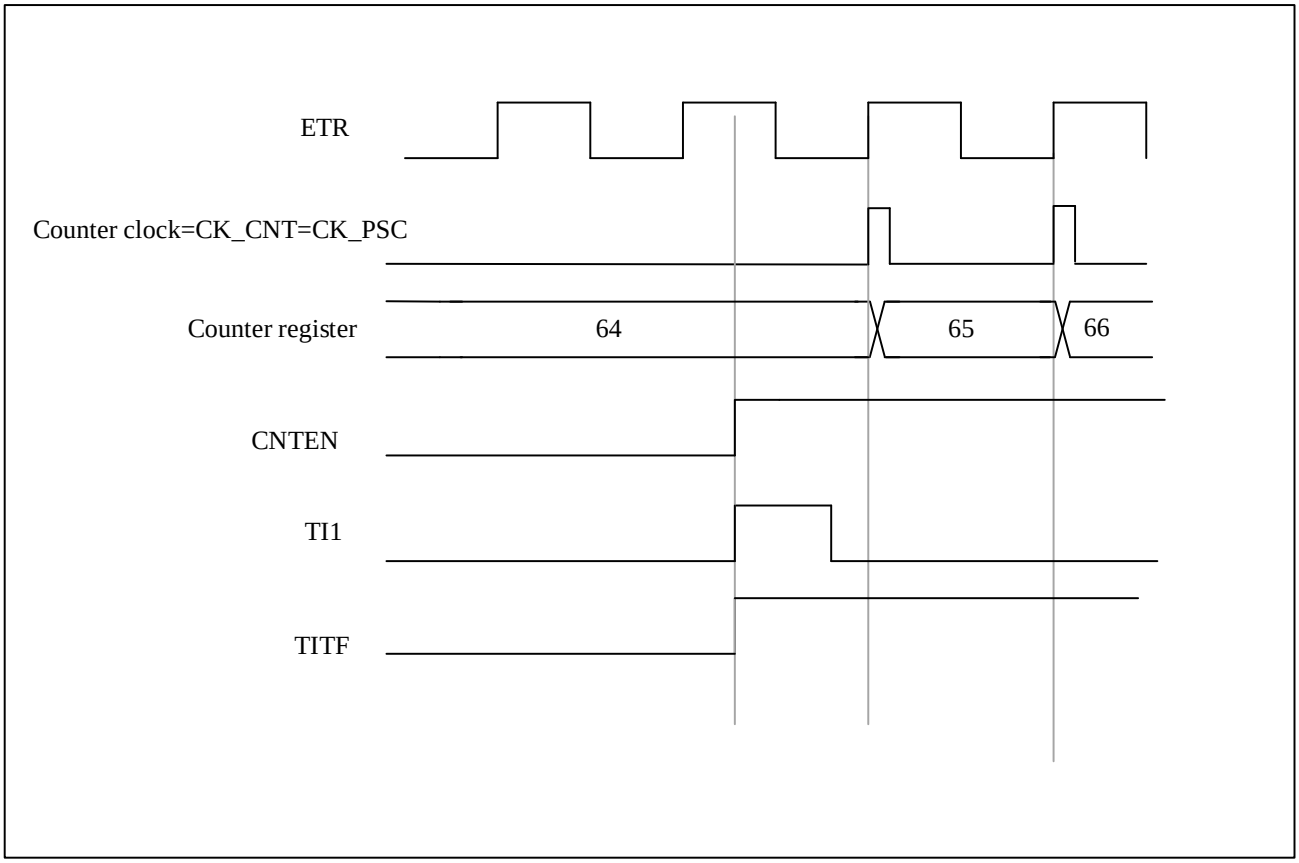
Figure 9-35 Control Circuit in Trigger Mode + External Clock Mode2



9.3.17 Timer Synchronization

All TIMx are internally interconnected for timer synchronization or chaining. Refer to Section 10.3.14 for detail.

9.3.18 Generating Six-step PWM Output

In order to modify the configuration of all channels at the same time, the configuration of the next step can be set in advance (the preloaded bits are OCxMD, CCxEN and CCxNEN). When a COM commutation event occurs, the OCxMD, CCxEN, and CCxNEN preload bits are transferred to the shadow register bits.

Methods to generate a COM commutation event:

- A software sets TIMx_EVTGEN.CCUDGN;
- Generated by hardware on the rising edge of TRGI;

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, enabling interrupts (TIMx_DINTEN.COMIEN) will generate interrupts, and enabling DMA requests (TIMx_DINTEN.COMDEN) will generate DMA requests.

The following figure shows the output timing diagram of OCx and OCxN when a COM commutation event occurs in three different configurations:

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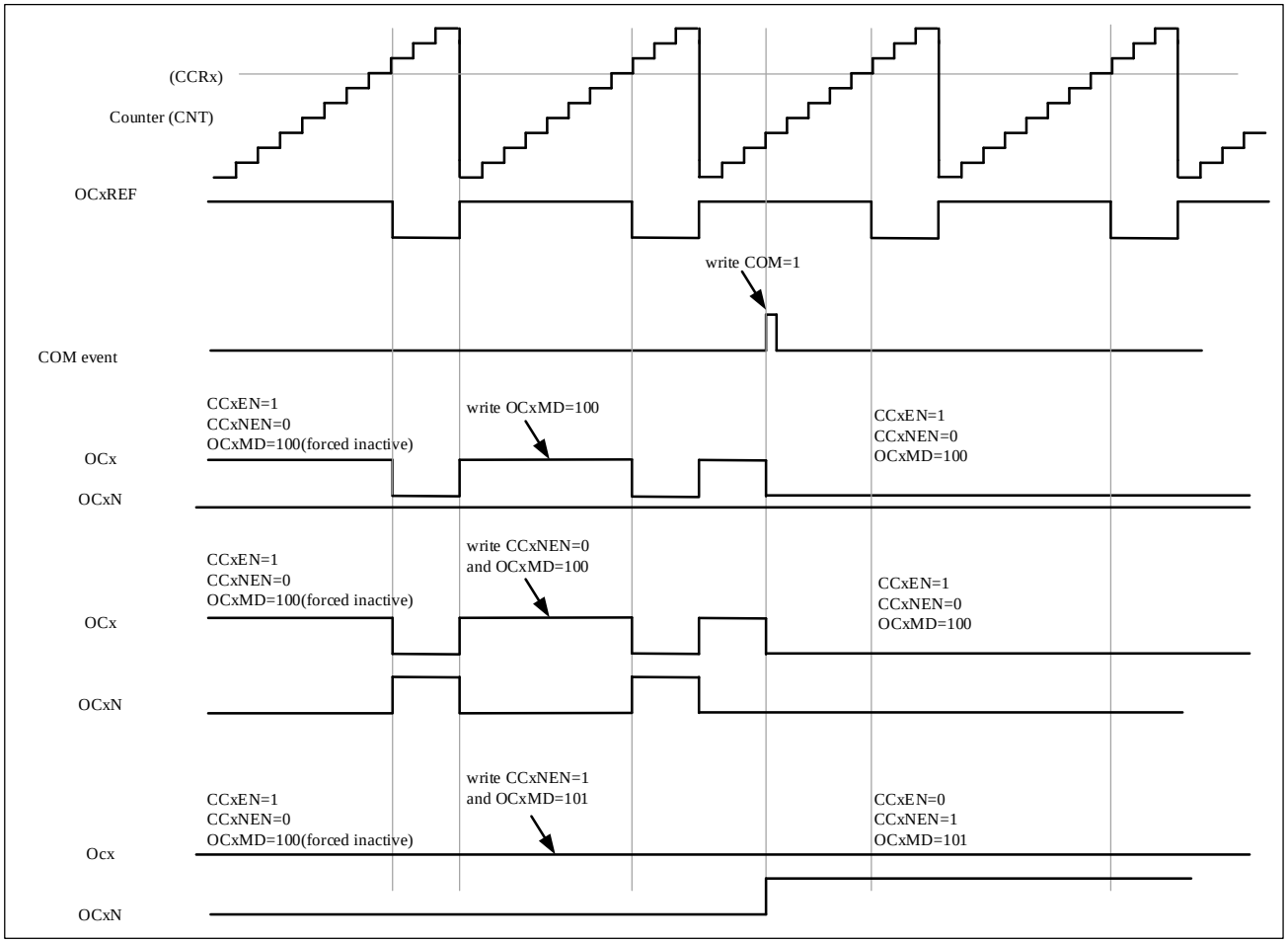
Figure 9-36 6-step PWM Generation, COM Example (OSSR=1)



9.3.19 Encoder Interface Mode

The encoder uses two inputs, TI1 and TI2 as the interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are five types of quadrature encoder counting modes:

- Encoder mode 1: The counter counts only on the edges of TI1, TIMx_SMCTRL.SMSEL = '001';
- Encoder mode 2: The counter counts only on the edges of TI2, TIMx_SMCTRL.SMSEL = '010';
- Encoder mode 3: The counter counts on the edges of both TI1 and TI2, TIMx_SMCTRL.SMSEL = '011';

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is as follows:

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Table 9-1 **The Relationship between the Counting Direction and the Encoder Signal (CC1P=CC2P=0)**

Active Edge	**Level on Opposite Signals (TI1FP1 for TI2, TI2FP2 for TI1)**	**TI1FP1 Signal**		**TI2FP2 Signal**	
		Rising	**Falling**	**Rising**	**Falling**
Counting only on TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only on TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on Both TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edge selected for triggering to suppress input jitter:

- IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= ‘01’), IC1FP1 is not inverted (TIMx_CCEN.CC1P= ‘0’);
- IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= ‘01’), IC2FP2 is not inverted (TIMx_CCEN.CC2P= ‘0’);
- The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = ‘011’);
- Enable counter TIMx_CTRL1.CNTEN= ‘1’.

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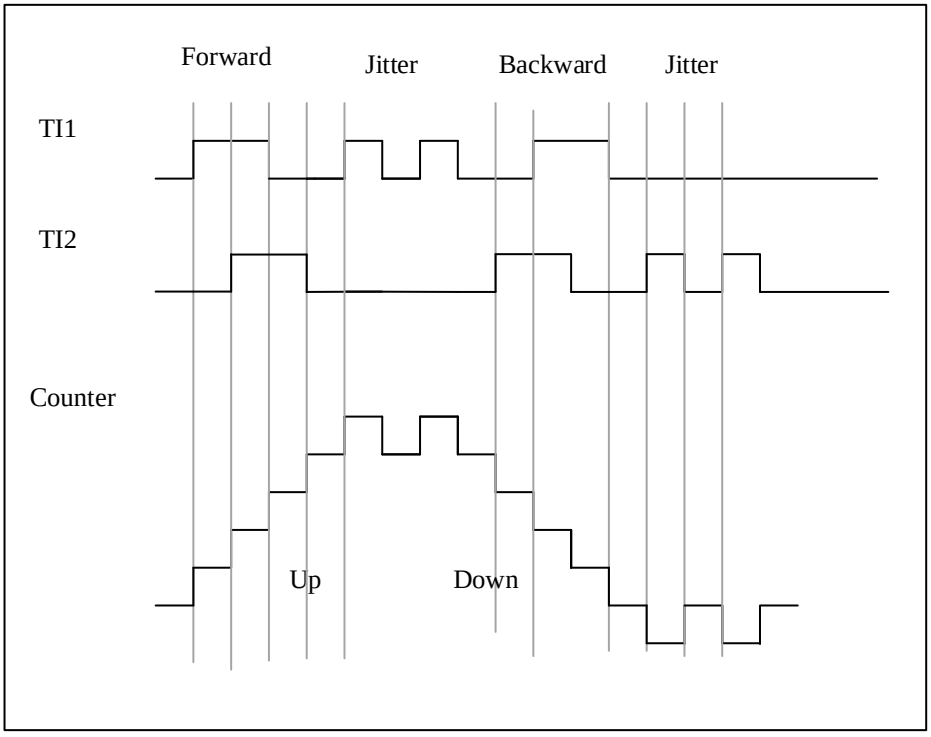
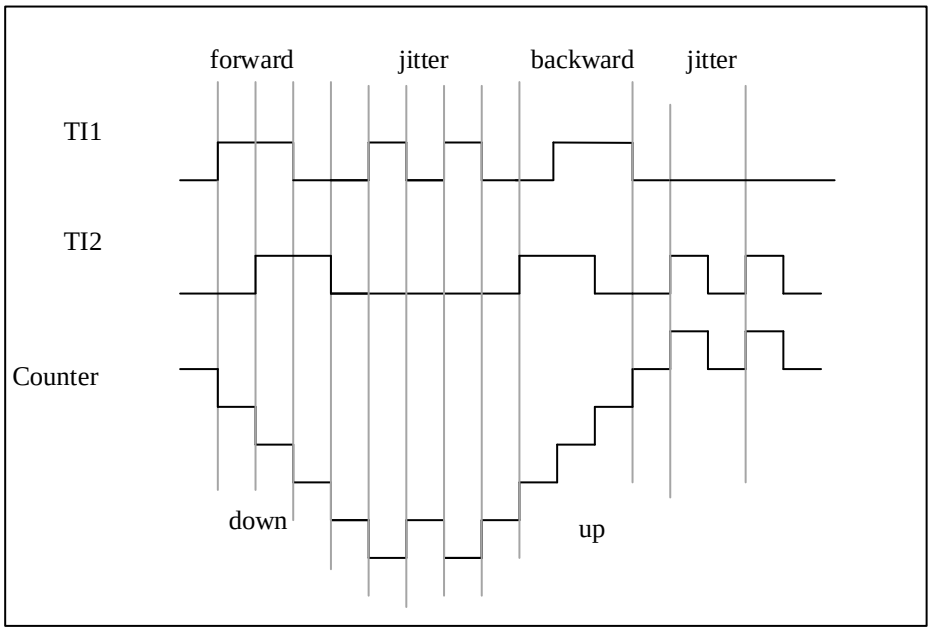
Figure 9-37 Example of Counter Operation in Encoder Interface Mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above).

Figure 9-38 Encoder Interface Mode Example with IC1FP1 Polarity Inverted



9.3.20 Interfacing with Hall Sensor

Connect the Hall sensor to the three input pins (CC1, CC2 and CC3) of the timer, and then select the XOR function to pass the inputs of TIMx_CH1, TIMx_CH2 and TIMx_CH3 through the XOR gate as the output of TI1 to channel 1 for capture signal.

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The timer needs to be configured as the reset mode in slave mode (TIMx_SMCTRL.SMSEL= ‘0100’); the edge of the trigger select TI1 triggers TI1F_ED (TIMx_SMCTRL.TSEL= ‘100’), any change in the Hall 3 inputs will trigger the counter to recount, so it is used as a time reference; the capture/compare channel 1 is configured to capture the TRC signal in capture mode (TIMx_CCMOD1.CC1SEL= ‘11’), which is used to calculate the two input time intervals, thereby reflecting the motor speed.

Select timer channel 2 to output pulses to the advanced timer to trigger the COM event of the advanced timer to update the control bits of the output PWM. The trigger selection of the advanced timer needs to select the corresponding internal trigger signal (TIMx_SMCTRL.TSEL="ITRx"), the capture/compare preload control bit needs to be configured to support preload (TIMx_CTRL2.CCPCTL=1) and support the rising edge of TRGI Trigger an update (TIMx_CTRL2.CCUSEL=1).

This example is shown in the following figure.

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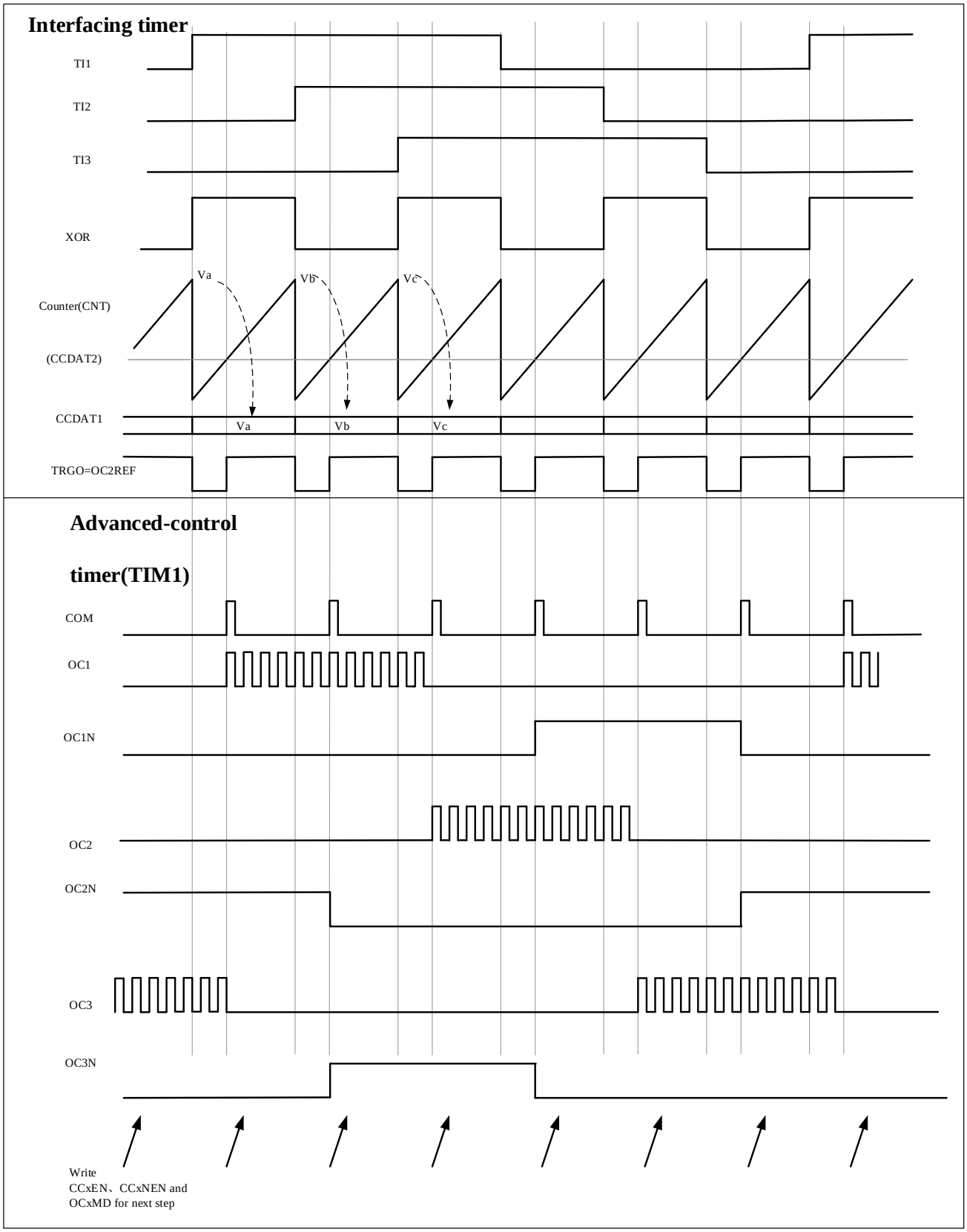
Figure 9-39 Example of Hall Sensor Interface



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9.4 TIM1 Register Description

For abbreviations used in the registers, please refer to Section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

9.4.1 Register Overview

Table 9-2 TIM1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved								ASYMMETRIC	Reserved	CMODE[1:0]		Reserved			C1SEL	COMPBKPEN	Reserved	CLRSEL	IOMBKPEN	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
	Reset Value									0		0	0				0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved								TRIG9	TRIG8	TRIG7	TRIG4	TI1SEL	CCPCTL	CCDSEL	CCUSEL	MMSEL[3:0]				Reserved	OI6	Reserved	OI5	OI4N	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0		0		0	0	0	0	0	0	0	0	0
008h	TIMx_STS	Reserved												BITF	TITF	COMITF	UDITF	Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved		CC6ITF	CC5ITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF
	Reset Value													0	0	0	0					0	0	0	0			0	0	0	0	0	0
00Ch	TIMx_EVTGEN	Reserved																				BGN	TGN	CCUDGN	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
	Reset Value																					0	0	0	0					0	0	0	0
010h	TIMx_SMCTRL	Reserved															MSMD	EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		Reserved	SMSEL[2:0]			Reserved	TSEL[2:0]		
	Reset Value																0	0	0	0	0	0	0	0	0		0	0	0		0	0	0
014h	TIMx_DINTEN	Reserved									COMIEN	TDEN	COMDEN	UDEN	BIEN	TIEN	UIEN	Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved				CC4IEN	CC3IEN	CC2IEN	CC1IEN
	Reset Value										0	0	0	0	0	0	0					0	0	0	0					0	0	0	0
018h	TIMx_CCMOD1	Reserved																OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved																IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD2	Reserved																IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCMOD3	Reserved								OC9PEN	Reserved		OC8PEN	Reserved			OC7PEN	OC6MD[2:0]			OC6CEN	OC6FEN	OC6PEN	Reserved		OC5MD[2:0]			OC5CEN	OC5FEN	OC5PEN	Reserved	
	Reset Value									0			0				0	0	0	0	0	0	0			0	0	0	0	0	0		
024h	TIMx_CCEN	Reserved								CC6P	CC6EN	Reserved		CC5P	CC5EN	Reserved		CC4P	CC4EN	CC4NP	CC4NEN	CC3P	CC3EN	CC3NP	CC3NEN	CC2P	CC2EN	CC2NP	CC2NEN	CC1P	CC1EN	CC1NP	CC1NEN
	Reset Value									0	0			0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_CCDAT1	CCDDAT1[15:0]																CCDAT1[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_CCDAT2	CCDDAT2[15:0]																CCDAT2[15:0]															

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	TIMx_CCDAT3	CCDDAT3[15:0]															CCDAT3[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	TIMx_CCDAT4	CCDDAT4[15:0]															CCDAT4[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT5	Reserved															CCDAT5[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	TIMx_CCDAT6	Reserved															CCDAT6[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	TIMx_PSC	Reserved															PSC[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	TIMx_AR	Reserved															AR[15:0]															
	Reset Value																1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
048h	TIMx_CNT	Reserved															CNT[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	TIMx_REPCNT	Reserved																							REPCNT[7:0]							
	Reset Value																								0	0	0	0	0	0	0	0
050h	TIMx_BKDT	Reserved															LCKCFG[1:0]		OSSR	OSSI	BKEN	BKP	AOEN	MOEN	DTGN[7:0]							
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	TIMx_CCDAT7	Reserved															CCDAT7[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
058h	TIMx_CCDAT8	Reserved															CCDAT8[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05Ch	TIMx_CCDAT9	Reserved															CCDAT9[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
060h	TIMx_BKFR	Reserved	THRESH[5:0]						Reserved	WSIZE[5:0]						FILTEN	PSC[15:0]															
	Reset Value		0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
094h	TIMx_DCTRL	Reserved																	DBADDR[4:0]					Reserved	DBLEN[4:0]						
	Reset Value																		0	0	0	0	0		0	0	0	0	0		
098Ch	TIMx_DADDR	Reserved															BURST[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								ASYMMETRIC	Reserved	CMODE[1:0]		Reserved			C1SEL
								rw		rw					rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPBKPEN	Reserved	CLRSEL	IOMBKPEN	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
rw		rw	rw	rw	rw	rw	rw	rw		rw	rw	rw		rw	rw

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	ASYMMETRIC	Asymmetric mode enable in center-aligned mode 0: Disabled 1: Enabled (valid when TIMx_CTRL1.CAMSEL[1:0] is non-zero, each channel will compare to CCDATx when counting up, and compare to CCDDATx when counting down) *Note: this function is only for TIM1*
22	Reserved	Reserved, the reset value must be maintained
21:20	CMODE	In center-aligned asymmetric mode, channel 4/7/8/9 trigger mode, only when TIMx_CTRL2.MMSEL3 = '1xxx', the TRGO output will be valid. 00: Up-counting to CCDAT4/7/8/9, trigger valid 01: Down-counting, channel 4 count to CCDDAT4, channel 7/8/9 count to CCDAT7/8/9, trigger valid 1x: Channel 4 up-counting to CCDAT4 or down-counting to CCDDAT4, channel 7/8/9 up-counting or down-counting to CCDAT7/8/9, trigger valid In center-aligned symmetry mode, channel 4/7/8/9 trigger mode, only when TIMx_CTRL2.MMSEL3 = '1xxx', the TRGO output will be valid. 00: Up-counting to CCDAT4/7/8/9, trigger valid 01: Down-counting to CCDAT4/7/8/9, trigger valid 1x: Up-counting or down-counting to CCDAT4/7/8/9, trigger valid
19:17	Reserved	Reserved, the reset value must be maintained
16	C1SEL	Channel 1 selection 0: Select the external CH1 (from IOM) signal. 1: Select internal CH1 (from COMP) signal.
15	COMPBKPEN	COMP break Enable 0: Enable 1: Disable
14	Reserved	Reserved, the reset value must be maintained
13	CLRSEL	OcxRef clear selection 0: Select the external Ocxclr (ETR) signal 1: Select the internal Ocxclr (from COMP) signal
12	IOMBKPEN	PVD break Enable 0: Disable 1: Enable
11	PBKPEN	PVD break Enable 0: Disable 1: Enable
10	LBKPEN	LockUp break Enable（Core Hardfault） 0: Disable 1: Enable
9	ARPEN	Auto-reload preload enable

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and DTS (clock used for dead-time generator and digital filters (ETR, TIx)) 00: tDTS = tCK_INT · 01: tDTS = 2 x tCK_INT 10: tDTS = 4 x tCK_INT 11: Reserved, do not use this configuration
5	UPDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV Enable. UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
1	DIR	Direction 0: Up-counting

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: Down-counting *Note: this bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

9.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TRIG9	TRIG8	TRIG7	TRIG4	TI1SEL	CCPCTL	CCDSEL	CCUSEL
								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved	OI6	Reserved	OI5	OI4N	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1
rw					rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	TRIG9	Enable triggering ADC when channel 9 comparison matches 0: Trigger disable 1: Trigger enable
22	TRIG8	Enable triggering ADC when channel 8 comparison matches 0: Trigger disable 1: Trigger enable
21	TRIG7	Enable triggering ADC when channel 7 comparison matches 0: Trigger disable 1: Trigger enable
20	TRIG4	Enable triggering ADC when channel 4 comparison matches 0: Trigger disable 1: Trigger enable
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	CCPCTL	Capture/compare preloaded control 0: CCxEN, CCxNEN and OCxMD bits are not preloaded. 1: CCxEN, CCxNEN and OCxMD bits are preloaded. they are updated only when a commutation

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		event COM occurs (CCUDGN bit set or rising edge on TRGI depending on CCUSEL bit) *Note: this bit only applied to channels with complementary outputs.*
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
16	CCUSEL	Capture/compare control update selection 0: If TIMx_CTRL2.CCPCTL = 1, they can only be updated by setting CCUDGN bit 1: If TIMx_CTRL2.CCPCTL = 1, they can be updated by setting CCUDGN bit or a rising edge on TRGI. *Note: this bit only applied to channels with complementary outputs.*
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 0000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 0001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). 0010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 0011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 0100: Compare - OC1REF signal is used as the trigger output (TRGO). 0101: Compare - OC2REF signal is used as the trigger output (TRGO). 0110: Compare - OC3REF signal is used as the trigger output (TRGO). 0111: Compare - OC4REF signal is used as the trigger output (TRGO). 1xxx: Compare-If the counter is center-aligned mode: The corresponding edge signal of OC4REF/OC7REF/OC8REF/OC9REF used as the trigger output (TRGO), up counting and down counting are configurable, refer specifically to the TIMx_CTRL1.CMODE. If the counter is edge alignment mode: The OC4REF signal is used as the trigger output (TRGO).
11	Reserved	Reserved, the reset value must be maintained
10	OI6	Output idle state 6 (OC6 output). Refer to TIMx_CTRL2.OI1 bit.
9	Reserved	Reserved, the reset value must be maintained
8	OI5	Output idle state 5 (OC5 output). Refer to TIMx_CTRL2.OI1 bit.
7	OI4N	Output idle state 4 (OC4N output). Refer to TIMx_CTRL2.OI1N bit.
6	OI4	Output idle state 4 (OC4 output). Refer to TIMx_CTRL2.OI1 bit.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
5	OI3N	Output idle state 3 (OC3N output). Refer to TIMx_CTRL2.OI1N bit.
4	OI3	Output idle state 3 (OC3 output). Refer to TIMx_CTRL2.OI1 bit.
3	OI2N	Output idle state 2 (OC2N output). Refer to TIMx_CTRL2.OI1N bit.
2	OI2	Output idle state 2 (OC2 output). Refer to TIMx_CTRL2.OI1 bit.
1	OI1N	Output Idle state 1 (OC1N Output) 0: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 0 1: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*
0	OI1	Output Idle state 1 0: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 0 1: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*

9.4.4 Status Register (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												BITF	TITF	COMITF	UDITF
												rc_w0	rc_w0	rc_w0	rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved		CC6ITF	CC5ITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0			rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	BITF	Break1 interrupt flag This bit is set by hardware once the break1 input is active. This bit is cleared by software when the break input becomes inactive. 0: No break1 event occurred 1: An active level has been detected on break input
18	TITF	Trigger interrupt flag When a trigger event occurs (when an effective edge is detected at the TRGI input, except in gated mode, or any edge in gated mode) the hardware sets this bit to '1'. It is cleared by software to '0'. 0: No trigger event occurred 1: Trigger interrupt pending
17	COMITF	COM interrupt flag This bit is set by hardware once a COM event is generated (when TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_CCMOD1.OCxMD have been updated). This bit is cleared by software.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		0: No COM event occurred 1: COM interrupt pending
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, and repeat counter value overflow or underflow (An update event is generated when the repeat counter equals 0). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag Refer to TIMx_STS.CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag Refer to TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag Refer to TIMx_STS.CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7:6	Reserved	Reserved, the reset value must be maintained
5	CC6ITF	Capture/Compare 6 interrupt flag Refer to TIMx_STS.CC1ITF description.
4	CC5ITF	Capture/Compare 5 interrupt flag Refer to TIMx_STS.CC1ITF description.
3	CC4ITF	Capture/Compare 4 interrupt flag Refer to TIMx_STS.CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag Refer to TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag Refer to TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **If channel CC1 is configured as an output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **If channel CC1 is configured as an input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

9.4.5 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				BGN	TGN	CCUDGN	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
				w	w	w	w					w	w	w	w

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	BGN	Break1 generation This bit can generate a break1 event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a break1 event
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
9	CCUDGN	Capture/Compare control update generation This bit is set by software. And if TIMx_CTRL2.CCPCTL = 1 at this time, the CCxEN, CCxNEN and OCxMD bits are allowed to be updated. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		Note: This bit is only valid for channels with complementary outputs.
8	UDGN	Update generation This bit is set to '1' by software and automatically cleared to '0' by hardware. This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be set to 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be set to 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If the TIMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

9.4.6 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															MSMD
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS		Reserved	SMSEL[2:0]			Reserved	TSEL[2:0]		
rw				rw	rw	rw			rw				rw		

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	MSMD	Master/slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: fSAMPLING=fDTS/8, N=6 0001: fSAMPLING=fCK_INT, N=2 1001: fSAMPLING=fDTS/8, N=8 0010: fSAMPLING=fCK_INT, N=4 1010: fSAMPLING=fDTS/16, N=5 0011: fSAMPLING=fCK_INT, N=8 1011: fSAMPLING=fDTS/16, N=6 0100: fSAMPLING=fDTS/2, N=6 1100: fSAMPLING=fDTS/16, N=8 0101: fSAMPLING=fDTS/2, N=8 1101: fSAMPLING=fDTS/32, N=5 0110: fSAMPLING=fDTS/4, N=6 1110: fSAMPLING=fDTS/32, N=6 0111: fSAMPLING=fDTS/4, N=8 1111: fSAMPLING=fDTS/32, N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: the following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 0111 and TIMx_SMCTRL.TSEL = 111).*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
7	Reserved	Reserved, the reset value must be maintained
6:4	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (refer to input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*
3	Reserved	Reserved, the reset value must be maintained
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 0xx: Internal trigger (ITRx), Select the ITR signal source based on TIMx_INSEL. 100: TI1 edge detector (TI1F_ED) 101: Filtered timer input 1 (TI1FP1) 110: Filtered timer input 2 (TI2FP2) 111: External triggered Input (ETRF) *Note: these bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*

Table 9-3 Internal trigger connection for TIMx

Slave Timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM5	TIM2	TIM3	TIM4
TIM2	TIM1	NA	TIM3	TIM4
TIM3	TIM1	TIM2	TIM5	TIM4
TIM4	TIM1	TIM2	TIM3	NA
TIM5	TIM2	TIM3	TIM4	NA

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

9.4.7 DMA/Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x14

Reset values: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									COMIEN	TDEN	COMDEN	UDEN	BIEN	TIEN	UIEN
									rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved				CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	COMIEN	COM interrupt enable 0: Disable COM interrupt 1: Enable COM interrupt
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
20	COMDEN	COM DMA request enable 0: Disable COM DMA request 1: Enable COM DMA request
19	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
18	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 terrupt 1: Enable capture/compare 3 nterrupt
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 nterrupt 1: Enable capture/compare 2 nterrupt
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 nterrupt 1: Enable capture/compare 1 nterrupt

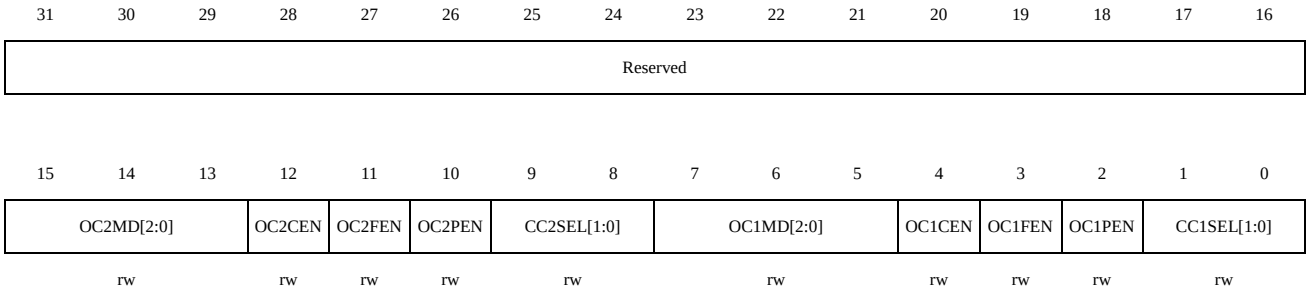
9.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by tim_ocref_clr_in input level 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high (tim_ocref_clr_in is controlled by the TIMx_CTRL1.CLRSEL register).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
1:0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Intput capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel i s configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input Capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

		The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

9.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000 0000

Refer to the description of the CCMOD1 register above.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

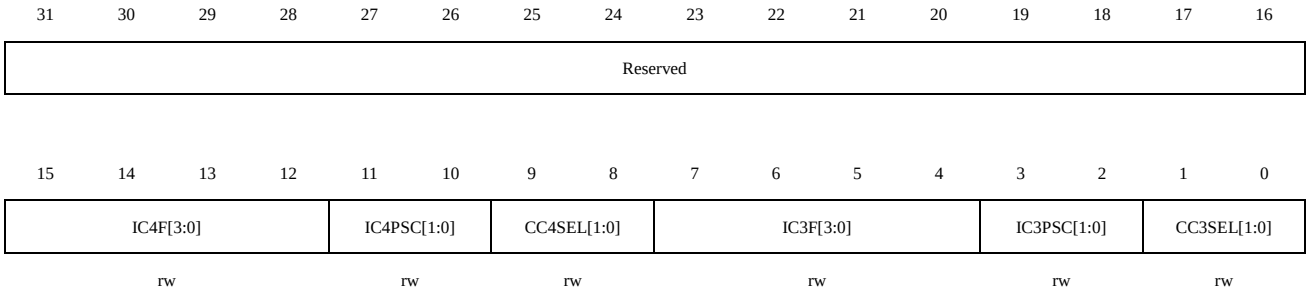
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode
12	OC4CEN	Output compare 4 clear enable

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

9.4.10 Capture/Compare Mode Register 3 (TIMx_CCMOD3)

Offset address: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							OC9PEN	Reserved			OC8PEN	Reserved			OC7PEN
							rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC6MD[2:0]			OC6CEN	OC6FEN	OC6PEN	Reserved		OC5MD[2:0]			OC5CEN	OC5FEN	OC5PEN	Reserved	
rw			rw	rw	rw			rw			rw	rw	rw		

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	OC9PEN	Output compare 9 preload enable
23:21	Reserved	Reserved, the reset value must be maintained
20	OC8PEN	Output compare 8 preload enable
19:17	Reserved	Reserved, the reset value must be maintained
16	OC7PEN	Output compare 7 preload enable
15:13	OC6MD[2:0]	Output compare 6 mode
12	OC6CEN	Output compare 6 clear enable
11	OC6FEN	Output compare 6 fast enable
10	OC6PEN	Output compare 6 preload enable
9:8	Reserved	Reserved, the reset value must be maintained
7:5	OC5MD[2:0]	Output compare 5 mode
4	OC5CEN	Output compare 5 clear enable
3	OC5FEN	Output compare 5 fast enable
2	OC5PEN	Output compare 5 preload enable
1:0	Reserved	Reserved, the reset value must be maintained

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

9.4.11 Capture/Compare Enable Register (TIMx_CCEN)

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CC6P	CC6EN	Reserved		CC5P	CC5EN	Reserved	
								rw	rw			rw	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	CC4NP	CC4NEN	CC3P	CC3EN	CC3NP	CC3NEN	CC2P	CC2EN	CC2NP	CC2NEN	CC1P	CC1EN	CC1NP	CC1NEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	CC6P	Capture/Compare 6 output polarity See TIMx_CCEN.CC1P description.
22	CC6EN	Capture/Compare 6 output enable See TIMx_CCEN.CC1EN description.
21:20	Reserved	Reserved, the reset value must be maintained
19	CC5P	Capture/Compare 5 output polarity See TIMx_CCEN.CC1P description.
18	CC5EN	Capture/Compare 5 output enable See TIMx_CCEN.CC1EN description.
17:16	Reserved	Reserved, the reset value must be maintained
15	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
14	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
13	CC4NP	Capture/Compare 4 complementary output polarity See TIMx_CCEN.CC1NP description.
12	CC4NEN	Capture/Compare 4 complementary output enable See TIMx_CCEN.CC1NEN description.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
9	CC3NP	Capture/Compare 3 complementary output polarity See TIMx_CCEN.CC1NP description.
8	CC3NEN	Capture/Compare 3 complementary output enable See TIMx_CCEN.CC1NEN description.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5	CC2NP	Capture/Compare 2 complementary output polarity See TIMx_CCEN.CC1NP description.
4	CC2NEN	Capture/Compare 2 complementary output enable See TIMx_CCEN.CC1NEN description.
3	CC1P	Capture/Compare 1 output polarity **When the corresponding channel of CC1 is in output mode:** 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: If TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. The level of OC1 depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. 1: Enable - Enable output OC1 signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N active high 1: OC1N active low
0	CC1NEN	Capture/Compare 1 complementary output enable 0: Disable - Disable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN. 1: Enable - Enable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Table 9-4 Output Control Bits of Complementary OCx and OCxN Channels with Break Function

Control Bits					Output State (1)	
MOEN	**OSSI**	**OSSR**	**CCxEN**	**CCxNEN**	**OCx Output State**	**OCxN Output State**
1	X	0	0	0	Output disabled (not driven by timer)	Output disabled (not driven by timer)
					OCx=0, OCx_EN=0	OCxN=0, OCxN_EN=0
		0	0	1	Output disabled (not driven by timer)	OCxREF + polarity
					OCx=0, OCx_EN=0	OCxN= OCxREF xor CCxNP, OCxN_EN=1
		0	1	0	OCxREF + polarity	Output disabled (not driven by timer)
					OCx= OCxREF xor CCxP, OCx_EN=1	OCxN=0, OCxN_EN=0
		0	1	1	OCxREF + polarity + dead-time, OCx_EN=1	Complementary to OCxREF + polarity + dead-time, OCxN_EN=1
		1	0	0	Output disabled (not driven by timer)	Output disabled (not driven by timer)
					OCx=CCxP, OCx_EN=0	OCxN=CCxNP, OCxN_EN=0
		1	0	1	Off-state (Output enabled with inactive state)	OCxREF + polarity
					OCx=CCxP, OCx_EN=1	OCxN= OCxREF xor CCxNP, OCxN_EN=1
		1	1	0	OCxREF + polarity	Off-state (Output enabled with inactive state)
					OCx= OCxREF xor CCxP, OCx_EN=1	OCxN=CCxNP, OCxN_EN=1
		1	1	1	OCxREF + polarity + dead-time OCx_EN=1	Complementary to OCxREF + polarity + dead-time OCxN_EN=1
0	0	X	0	0	Output disabled (not driven by timer)	
	0		0	1	Asynchronously: OCx=CCxP, OCx_EN=0, OCxN=CCxNP,OCxN_EN=0; Then if the clock is present: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0, OCx=OIx, OCxN=OIxN after a dead-time	
	0		1	0		
	0		1	1		
	1		0	0	Off-state (Output enabled with inactive state) Asynchronously: OCx=CCxP, OCx_EN=1, OCxN=CCxNP,OCxN_EN=1; Then if the clock is present: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0, OCx=OIx , OCxN=OIxN after a dead-time	
	1		0	1		
	1		1	0		
	1		1	1		

Note: (1) If both outputs of a channel are not used (CCxEN = CCxNEN = 0), OIx, OIxN, CCxP and CCxNP must all be cleared.

Note: the status of external I/O pins connected to complementary OCx and OCxN channels depends on the OCx and OCxN channel states and GPIO and AFIO registers.

9.4.12 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x28

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT1[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT1[15:0]	Capture/Compare 1 down-counting value, dedicated to center-aligned asymmetric mode. ■ CC1 channel can only configured as output: CCDDAT1 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT1[15:0]	Capture/Compare 1 value ■ CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 and CCDDAT1 are only readable. When configured as output mode, register CCDAT1 and CCDDAT1 are readable and writable.

9.4.13 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT2[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[15:0]															
rw															

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
31:16	CCDDAT2[15:0]	Capture/Compare 2 down-counting value, dedicated to center-aligned asymmetric mode ■ CC2 channel can only configured as output: CCDDAT2 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT2[15:0]	Capture/Compare 2 value ■ CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 and CCDDAT2 are only readable. When configured as output mode, register CCDAT2 and CCDDAT2 are readable and writable.

9.4.14 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT3[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT3[15:0]	Capture/Compare 3 down-counting value, dedicated to center-aligned asymmetric mode ■ CC3 channel can only configured as output: CCDDAT3 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT3[15:0]	Capture/Compare 3 value

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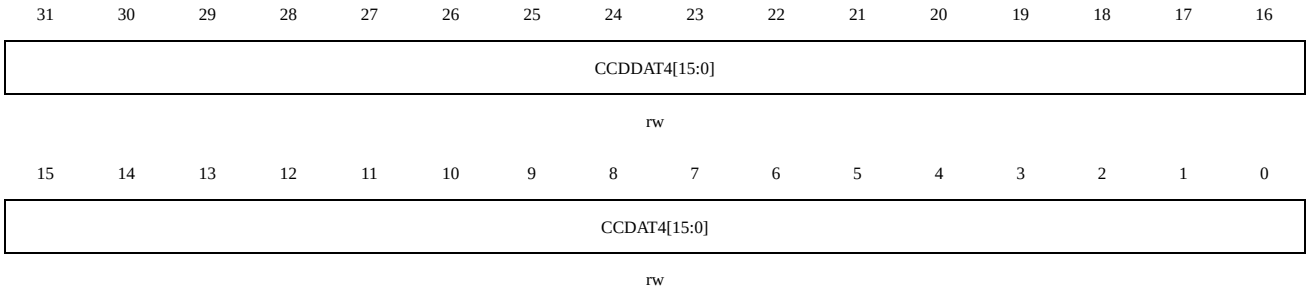
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		■ CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 and CCDDAT3 are only readable. When configured as output mode, register CCDAT3 and CCDDAT3 are readable and writable.

9.4.15 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x34

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	CCDDAT4 [15:0]	Capture/Compare 4 down-counting value, dedicated to center-aligned asymmetric mode ■ CC4 channel can only configured as output: CCDDAT4 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT4[15:0]	Capture/Compare 4 value ■ CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC4 channel is configured as input:

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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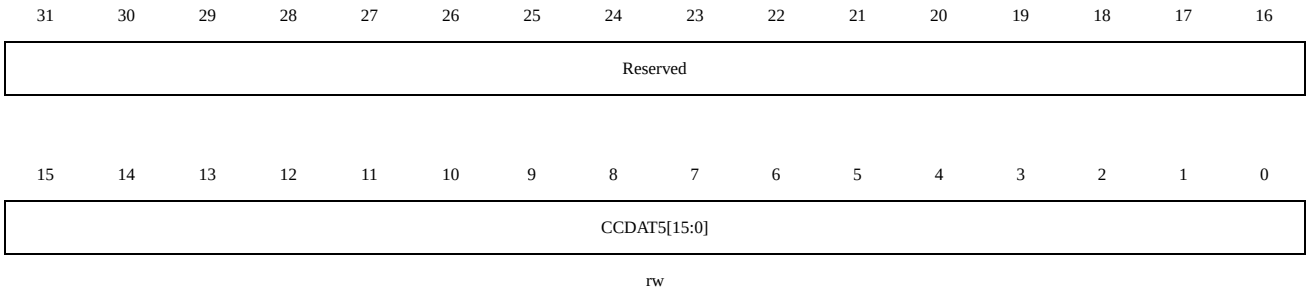
Bit Field	Name	Description
		CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 and CCDDAT4 are only readable. When configured as output mode, register CCDAT4 and CCDDAT4 are readable and writable.

9.4.16 Capture/Compare Register 5 (TIMx_CCDAT5)

Offset address: 0x38

Reset value: 0x0000 0000

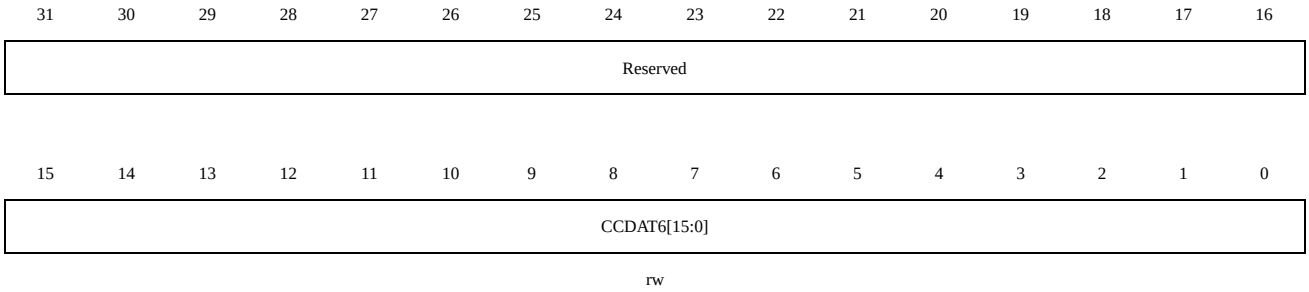


Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT5[15:0]	Capture/Compare 5 value ■ CC5 channel can only configured as output: CCDAT5 contains the value to be compared with the counter TIMx_CNT, and signal is sent out on the OC5 output. If the preload function is not selected in the TIMx_CCMOD3.OC5PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC5 is used for comparator blanking.

9.4.17 Capture/Compare Register 6 (TIMx_CCDAT6)

Offset address: 0x3C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
15:0	CCDAT6[15:0]	Capture/Compare 6 value ■ CC6 channel can only configured as output: CCDAT6 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on the OC6 output. If the preload function is not selected in the TIMx_CCMOD3.OC6PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

9.4.18 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK_CNT} = f_{CK_PSC}/$ (PSC [15:0] +1). The PSC value is loaded into the shadow register of the prescaler each time an update event occurs.

9.4.19 Auto-reload Register (TIMx_AR)

Offset address: 0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained

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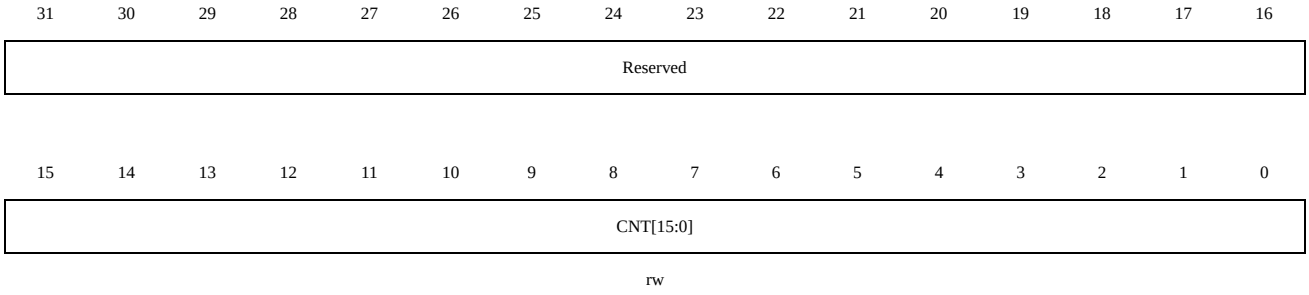
Bit Field	Name	Description
15:0	AR[15:0]	Auto-reload value AR contains the value to be loaded into the actual auto-reload register. Refer to section 10.4.1 for details on the update and action of AR. When the value for auto-reload is empty, the counter will not operate.

9.4.20 Counters (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

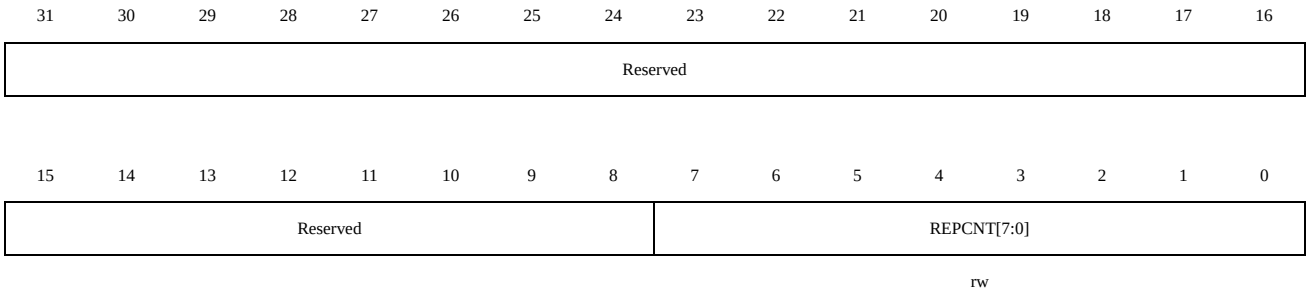


Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CNT[15:0]	Counter value

9.4.21 Repeat Count Register (TIMx_REPCNT)

Offset address: 0x4C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value Repetition counter is used to generate the update event or update the timer registers only after a given number (N+1) cycles of the counter, where N is the value of TIMx_REPCNT.REPCNT. The repetition counter is decremented at each counter overflow in up-counting mode, at each counter underflow in down-counting mode or at each counter overflow and at each counter underflow in

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		center-aligned mode. Setting the TIMx_EVTGEN.UDGN bit will reload the content of TIMx_REPCNT.REPCNT and generate an update event.

9.4.22 Break and Dead-time Registers (TIMx_BKDT)

Offset address: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCKCFG[1:0]		OSSR	OSSI	BKEN	BKP	AOEN	MOEN	DTGN[7:0]							
rw		rw	rw	rw	rw	rw	rw	rw							

Note: AOEN、BKP、BKEN、OSSI、OSSR and DTGN[7:0] bits can all be write protected depending on the LOCK configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:14	LCKCFG[1:0]	Lock configuration. This bit provides write protection to prevent software errors. These bits offer a write protection against software errors. 00: – No write protected. 01: – LOCK Level 1 TIMx_BKDT.DTGN、TIMx_BKDT.BKEN、TIMx_BKDT.BKP、TIMx_BKDT.AOEN、TIMx_CTRL2.OIx、TIMx_CTRL2.OIxN bits enable write protection. 10: – LOCK Level 2 Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection 11: – LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: After the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
13	OSSR	Off-state Selection for Run Mode This bit is used when TIMx_BKDT.MOEN=1 and the channel is a complementary output. The OSSR bit does not exist in timer without complementary outputs. 0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal = 0) 1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxEN = 1 or

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		CCxNEN = 1. Then, OC/OCN enable output signal = 1 For more details, See Section 9.4.11 capture/compare enable registers (TIMx_CCEN).
12	OSSI	Off-state selection for Idle mode This bit is used when TIMx_BKDT.MOEN=0 and the channels configured as outputs. 0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal = 0) 1: When inactive, OC/OCN outputs are forced with their with their idle level as soon as CCxEN = 1 or CCxNEN = 1. Then, OC/OCN enable output signal = 1 For more details, See Section 9.4.11 capture/compare enable registers (TIMx_CCEN).
11	BKEN	Break1 enable 0: Disable break 1 input 1: Enable break 1 input *Note: Any write to this bit requires an APB clock delay to take effect.*
10	BKP	Break1 polarity 0: Low level of the break 1 input is valid 1: High level of the break 1 input is valid *Note: Any write to this bit requires an APB clock delay to take effect.*
9	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.
8	MOEN	Main output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the break input is active. It is only valid for channels configured as outputs. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set.For more details, see Section 9.4.11 Capture/Compare enable registers (TIMx_CCEN).
7:0	DTGN[7:0]	Dead-time generator setup These bits define the dead-time duration between inserted complementary outputs. The relationship between the DTGN value and the dead time is as follows: DTGN[7:5]=0xx => DT=DTGN[7:0] $\times T_{dtgn}$， $T_{dtgn} = T_{DTS}$; DTGN[7:5]=10x => DT=(64+DTGN[5:0]) $\times T_{dtgn}$， $T_{dtgn} = 2 \times T_{DTS}$; DTGN[7:5]=110 => DT=(32+DTGN[4:0]) $\times T_{dtgn}$， $T_{dtgn} = 8 \times T_{DTS}$; DTGN[7:5]=111 => DT=(32+DTGN[4:0]) $\times T_{dtgn}$， $T_{dtgn} = 16 \times T_{DTS}$;

9.4.23 Capture/Compare Register 7 (TIMx_CCDAT7)

Offset address: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT7[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT7[15:0]	Capture/Compare 7 value ■ CC7 channel can only configured as output: CCDAT7 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC7 output. If the preload function is not selected in the TIMx_CCMOD3.OC7PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

9.4.24 Capture/Compare Register 8 (TIMx_CCDAT8)

Offset address: 0x58

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT8[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT8[15:0]	Capture/Compare 8 value ■ CC7 channel can only configured as output: CCDAT8 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC8 output. If the preload function is not selected in the TIMx_CCMOD3.OC8PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

9.4.25 Capture/Compare Register 9 (TIMx_CCDAT9)

Offset address: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT9[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT9[15:0]	Capture/Compare 9 value ■ CC7 channel can only configured as output: CCDAT9 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC9 output. If the preload function is not selected in the TIMx_CCMOD3.OC9PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

9.4.26 Break Filter Register (TIMx_BKFR)

Offset address: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC															
rw															

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold number of sample logic level to be valid, maximum 63: Threshold value for a valid logic level. Within sample window if number of logic high is more than or equal to threshold value, next logic level will be logic high. Same rule applies to logic low. If both number of 1's and 0's inside window are smaller than threshold, filter output stays unchanged. Threshold value should set to more than or equal to half of window value. Recommend threshold range is: **Minimum**: 1 pre-scale clock cycle more than ceiling value of max glitch size (in pre-scale clock cycle) and need to larger than half of window size. for example, if glitch size is 3.2*(pre-scale clock period), threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum**: floor value of minimum size of valid signal (in pre-scale clock cycle) and need to be smaller than window size. For example, if minimum message size is 3.2*(pre-scale clock period), threshold should be floor

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Bit Field	Name	Description
		(3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	Window size value for logic level check, maximum 63: Window size decides how many sampled values will take into consideration for getting next logic level. Build-in FIFO is 64 bits with maximum index 63 which can only set window size to be 63.
16	FILTEN	Filter enable 0: Disable filter 1: Enable filter
15:0	PSC[15:0]	Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a 65535 division (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the valid values of the sampling points are considered for logical level calculation.

9.4.27 DMA Control Register (TIMx_DCTRL)

Offset address: 0x94

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			DBADDR[4:0]					Reserved			DBLEN[4:0]				
			rw								rw				

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12:8	DBADDR[4:0]	DMA base address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of “DMA Base Address + 4” 00000：TIMx_CTRL1, 00001：TIMx_CTRL2, 00010：TIMx_SMCTRL, ... 10001：TIMx_BKDT, 10010：TIMx_DCTRL
7:5	Reserved	Reserved, the reset value must be maintained
4:0	DBLEN[4:0]	DMA burst length

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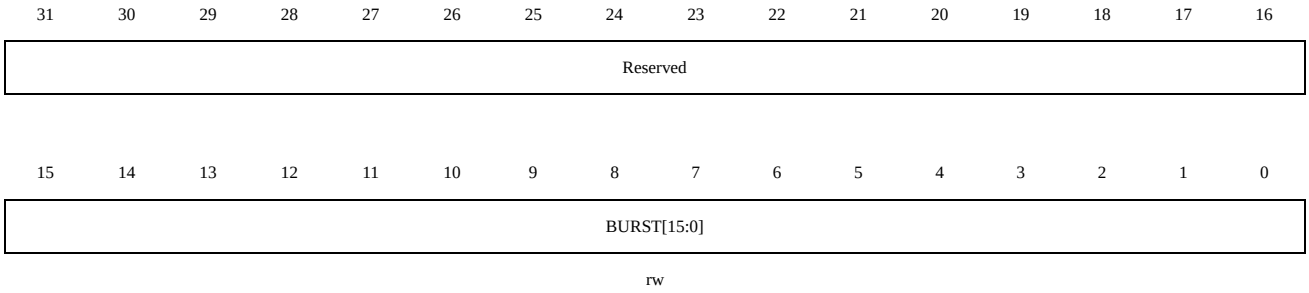
Bit Field	Name	Description
		This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 00000: 1 time transfer 00001: 2 time transfer 00010: 3 time transfer … 10001: 18 time transfer

9.4.28 DMA Transfer For Full Transfer Register (TIMx_DADDR)

Offset address: 0x98

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	BURST[15:0]	DMA Access Buffer When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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10 General-purpose Timers (TIM2/TIM3/TIM4/TIM5)

10.1 General-purpose Timers Introduction

The general-purpose timers (TIM2/ TIM3/ TIM4/ TIM5) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

10.2 Main Features of General-purpose Timers

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 up to 4 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signal.

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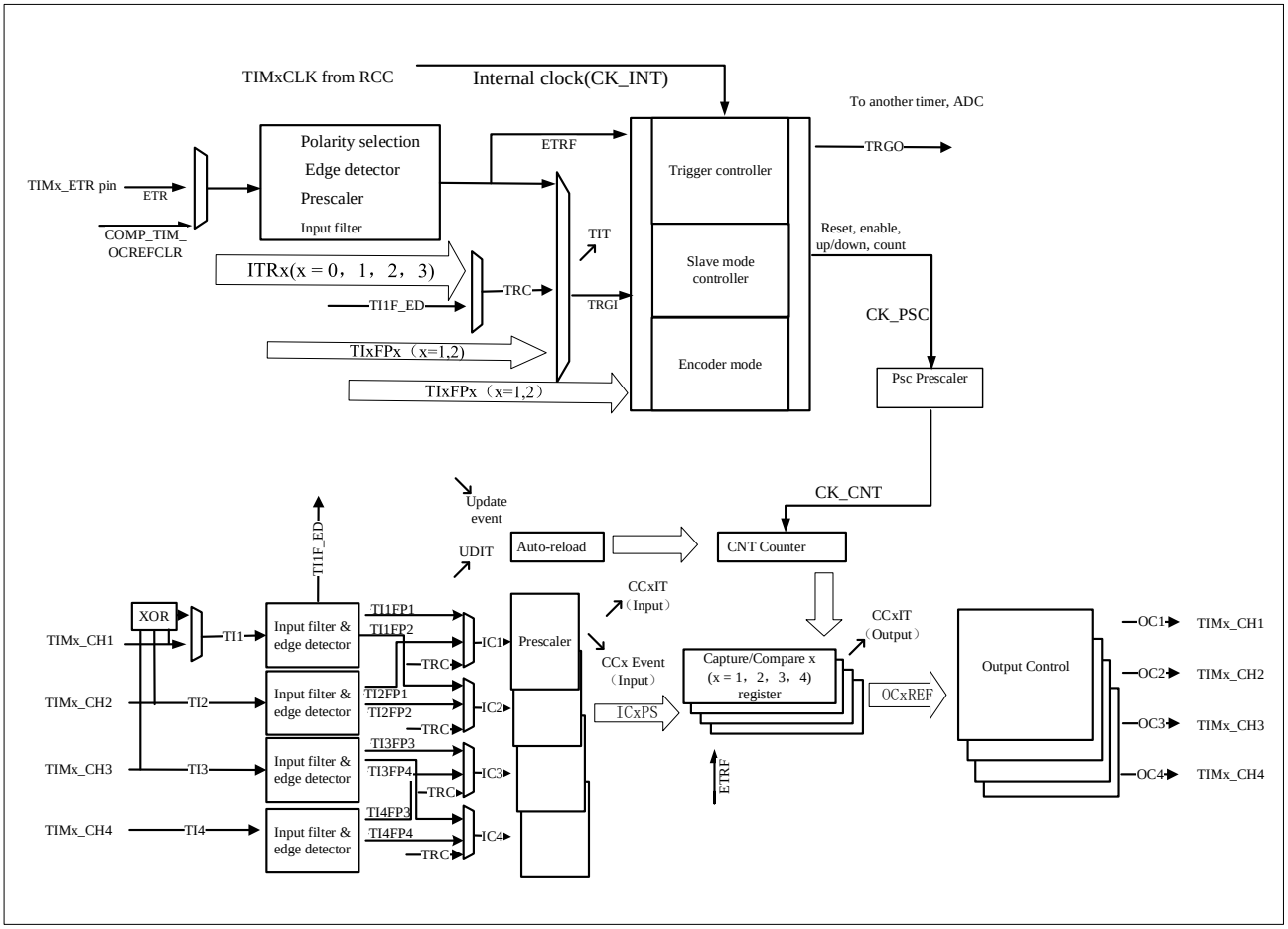
Figure 10-1 Block Diagram of TIMx



↘ *The event* ↗ *Interrupt and DMA output*

1. *For TIMx（x = 2,3,4,5）,the ETR input is from IOM or COMP output, for TIM5, the ETR input is not support.*
2. *For TIMx（x = 2,3,4,5）, The capture channel 1/2/3/4 input can come from IOM or comparator output.*
3. *For TIM2, capture channel 1 comes from IOM/COMP or HSI, capture channel 3 comes from IOM/COMP or LSI, capture channel 4 comes from IOM/COMP or HSE/128.*
4. *For each GPTIM, there is a sliding filter in front of TIMx_CH1, TIMx_CH2, TIMx_CH3 and TIMx_CH4. Sliding filter is only for IOM input, not for HSE/128, LSI, HSI input.*

10.3 General-purpose Timers Description

10.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter

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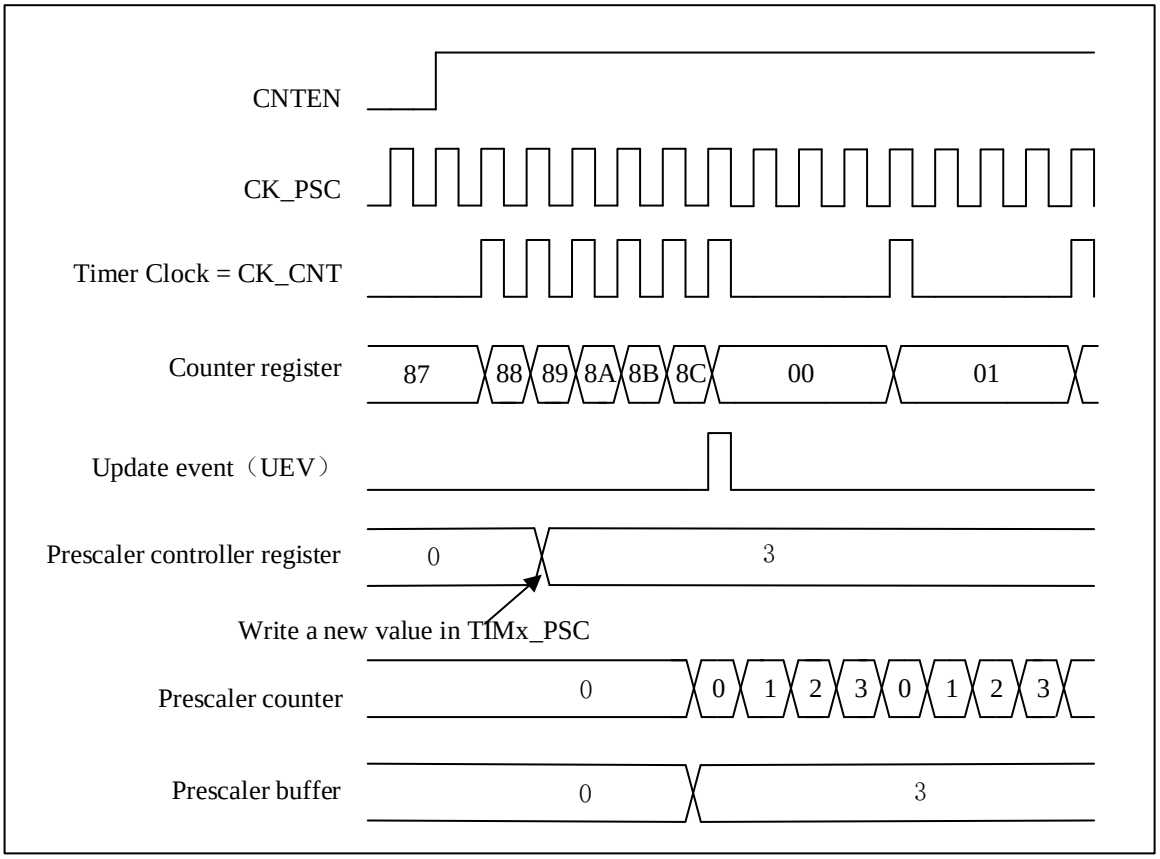
starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

10.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 10-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



10.3.2 Counter Mode

10.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value (TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value (TIMx_PSC).

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To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 10-3 Timing Diagram of Up-counting, The Internal Clock Divider Factor = 2/N

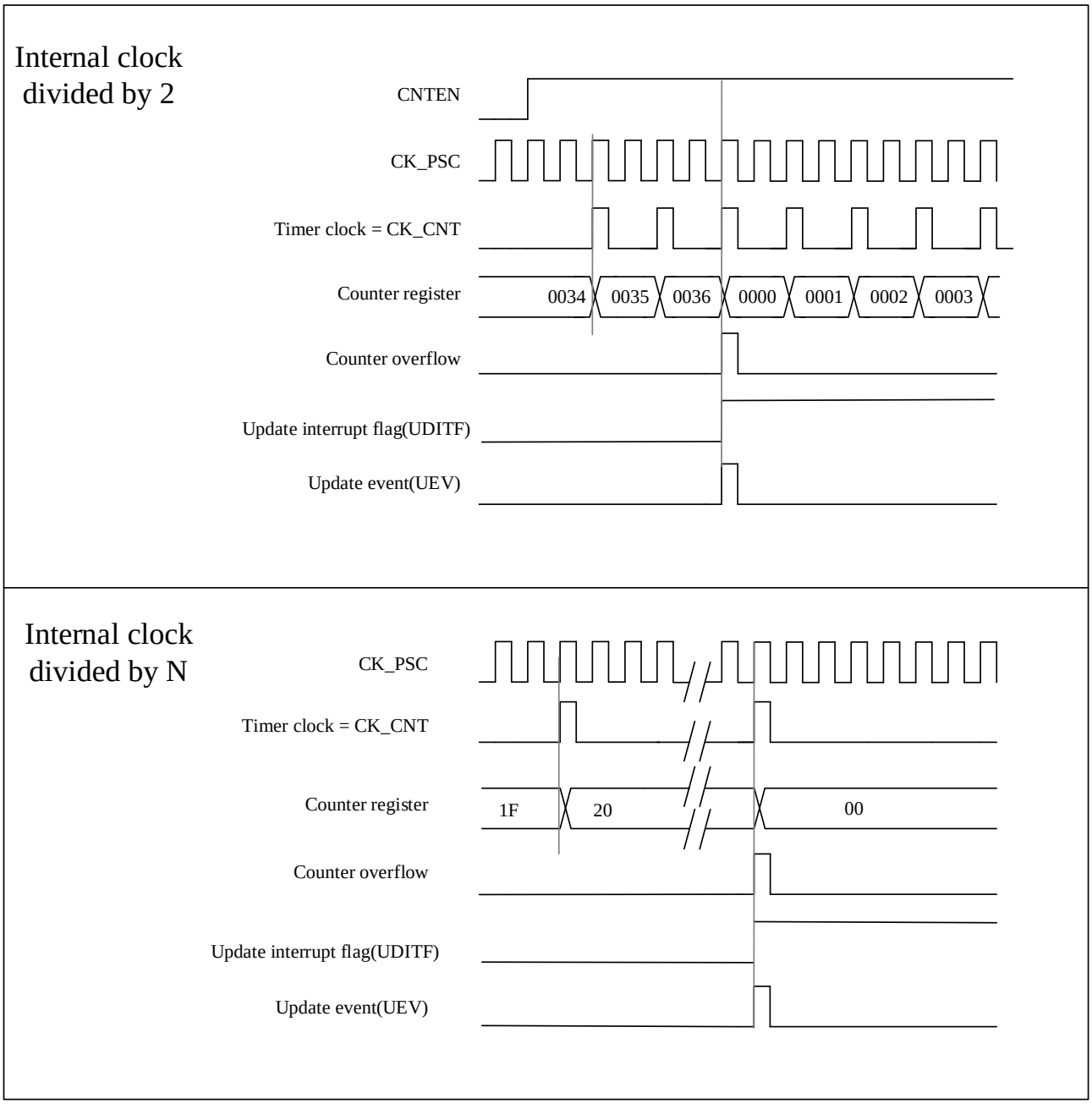

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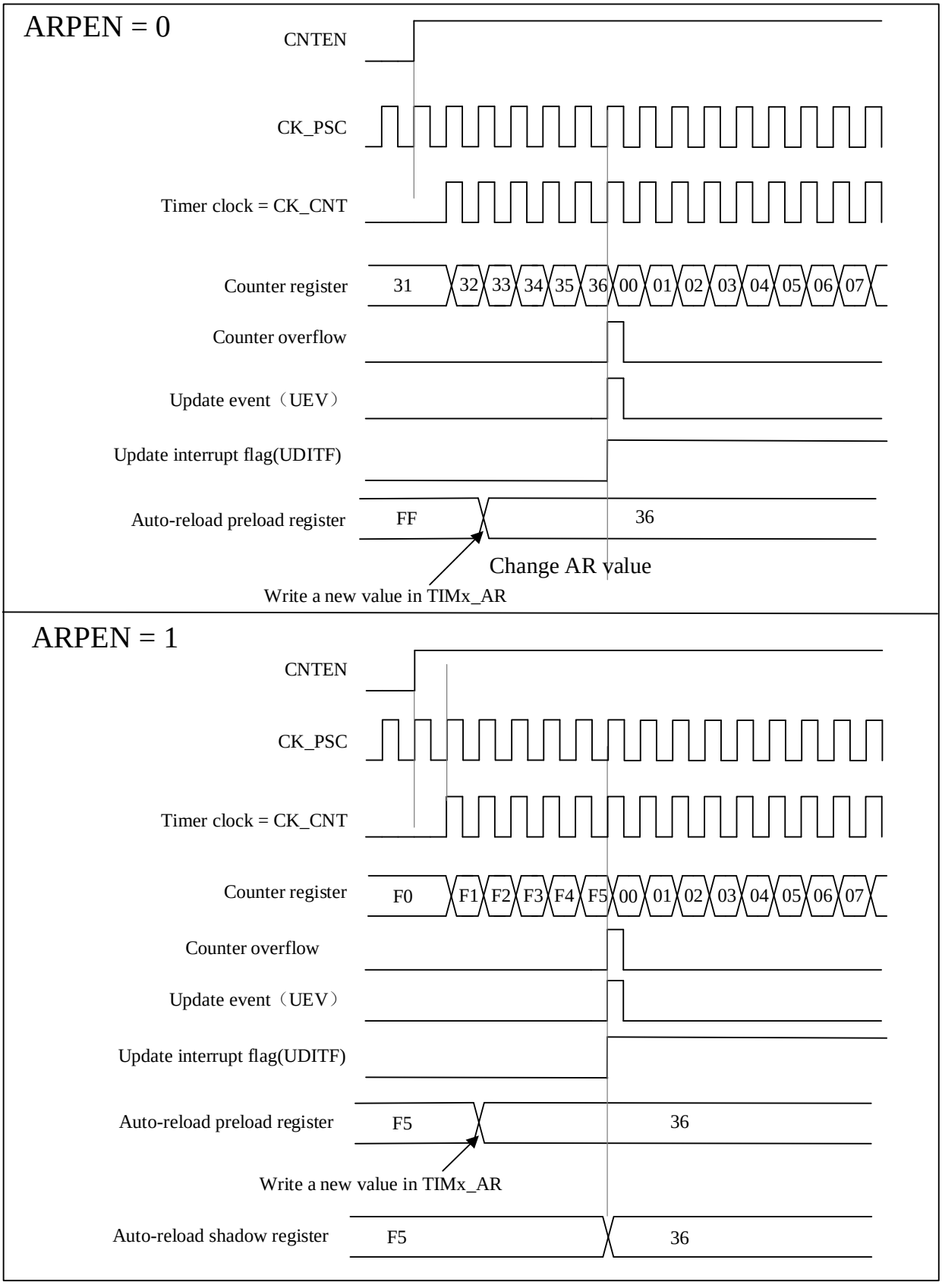
Figure 10-4 Timing Diagram of The Up-counting, Update Event When ARPEN = 0/1



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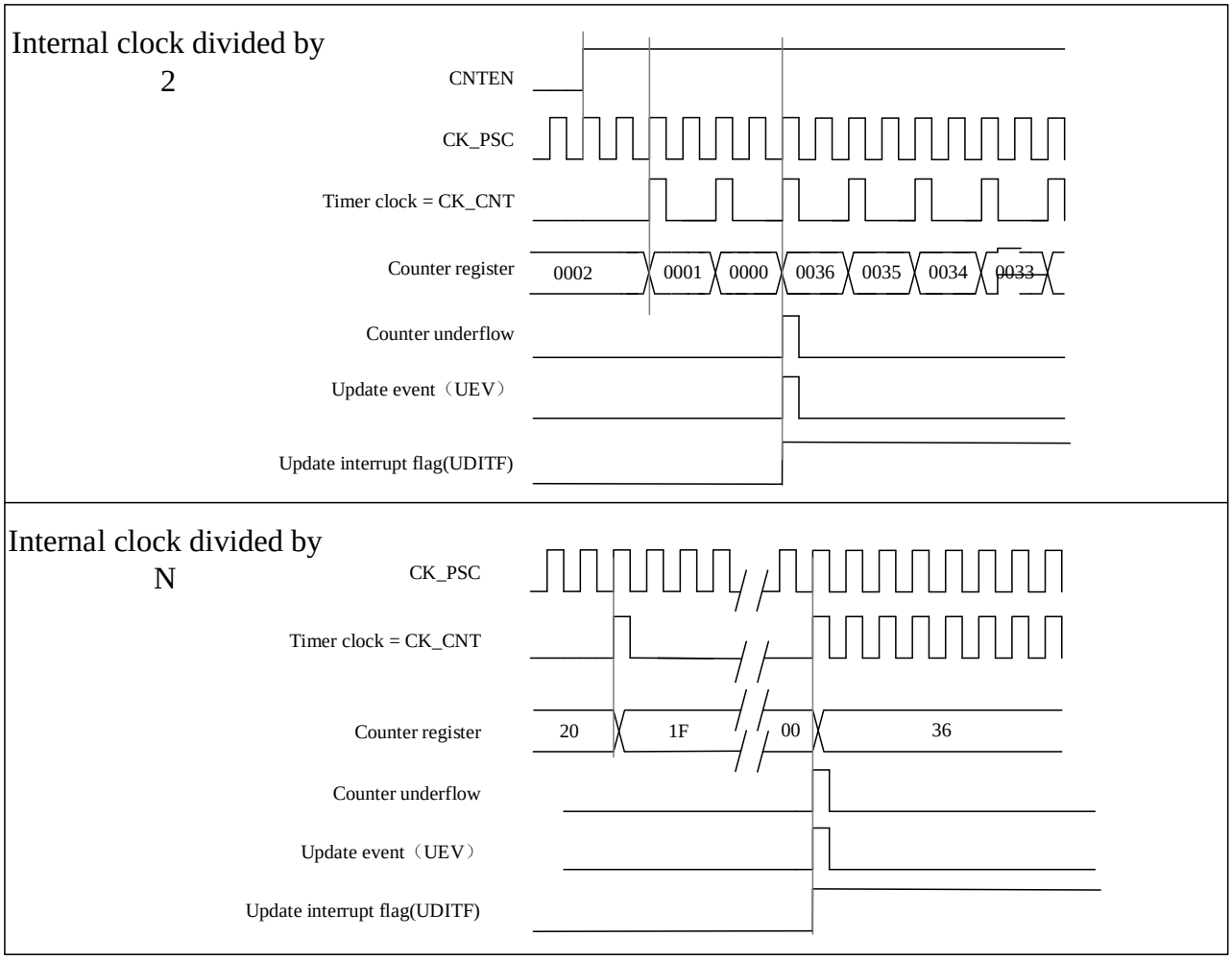
10.3.2.2 **Down-counting mode**

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see Section 10.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 10-5 Timing Diagram of the Down-counting, Internal Clock Divided Factor = 2/N



10.3.2.3 **Center-aligned mode**

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

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Note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 10-6 Timing Diagram of the Center-aligned, Internal Clock Divided Factor = 2/N

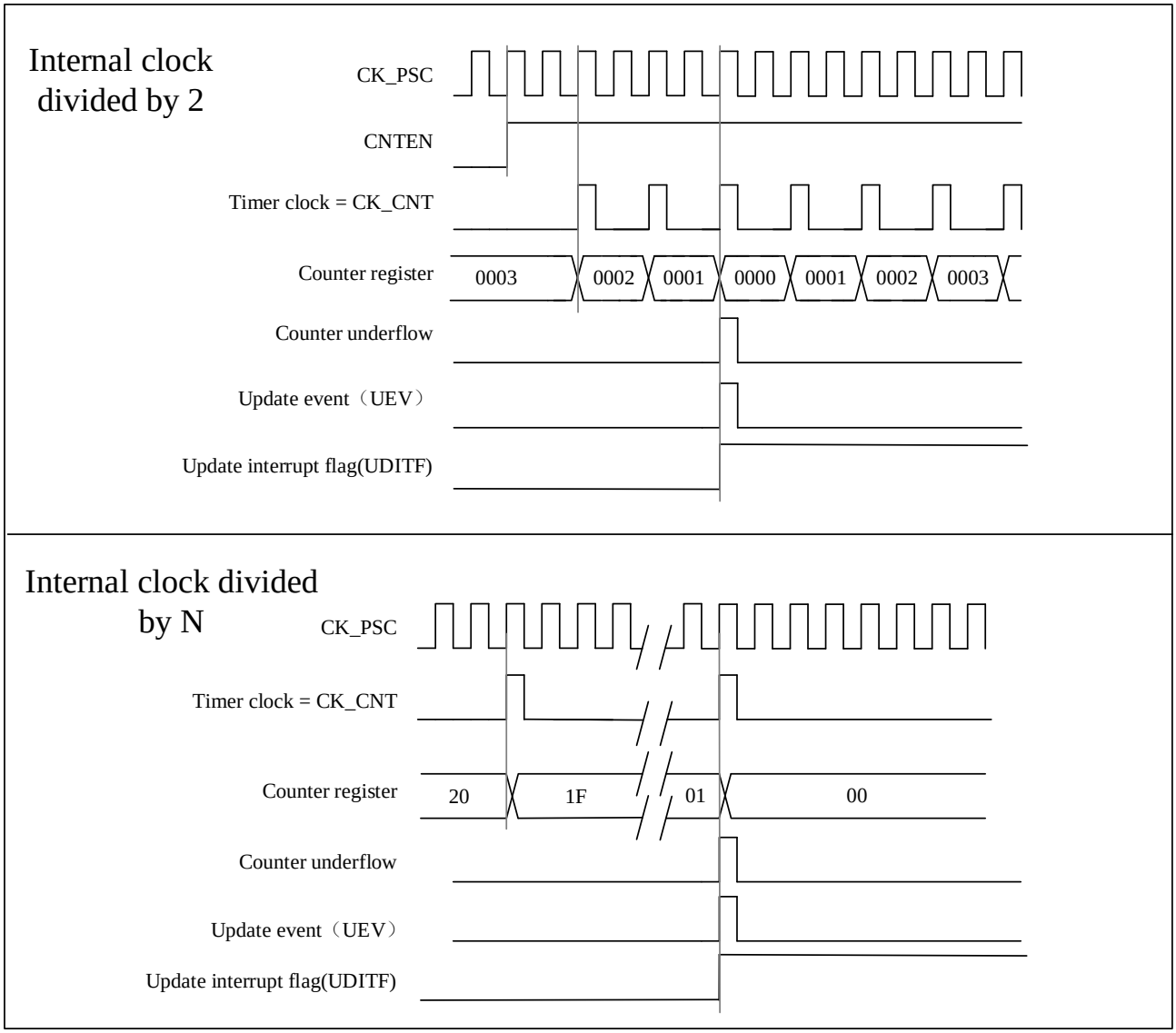

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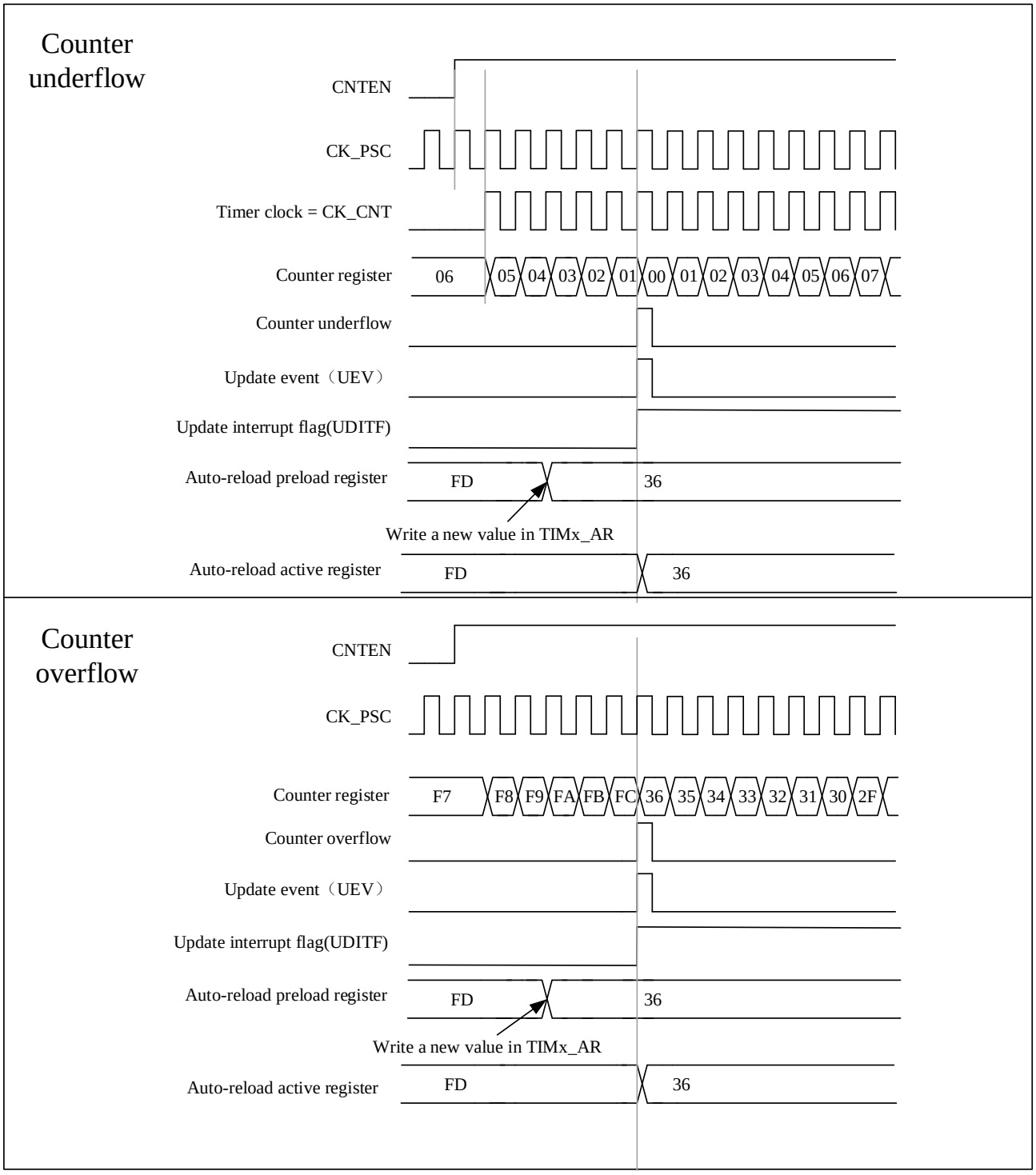
Figure 10-7 A Center-aligned Sequence Diagram That Includes Counter Overflows and Underflows (ARPEN = 1)



10.3.3 Clock Selection

- The internal clock of timers：CK_INT
- Two kinds of external clock mode:
  - External input pin

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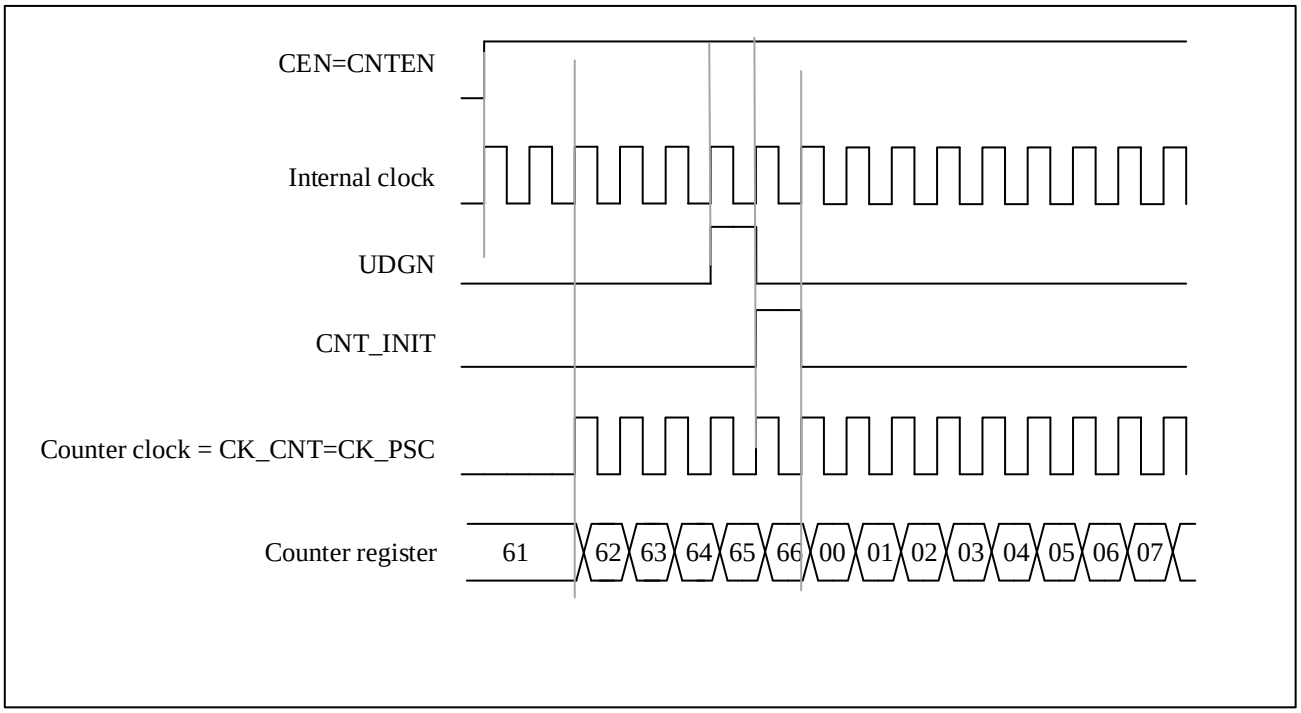
– External trigger input ETR

- Internal trigger input (ITRx) : one timer is used as a prescaler for another timer

10.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 10-8 Control Circuit in Normal Mode, Internal Clock Divided by 1



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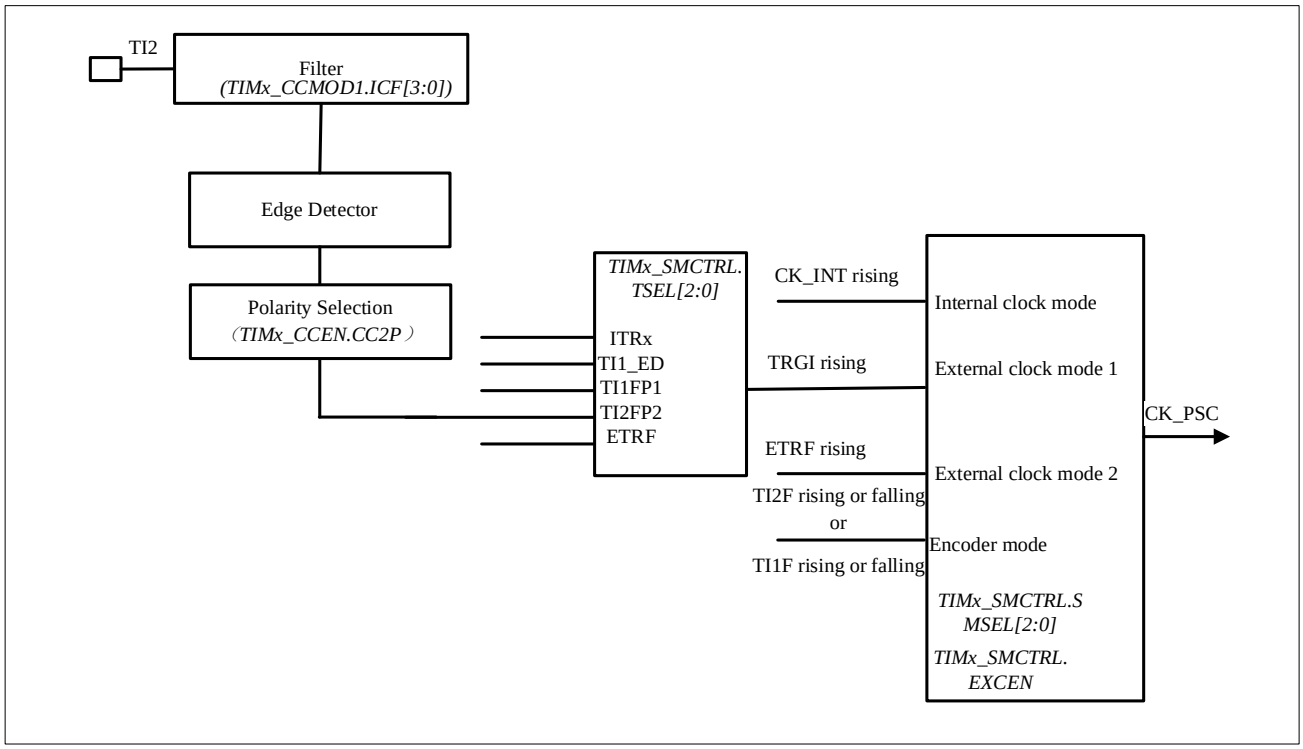
10.3.3.2 External clock source mode 1

Figure 10-9 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note：The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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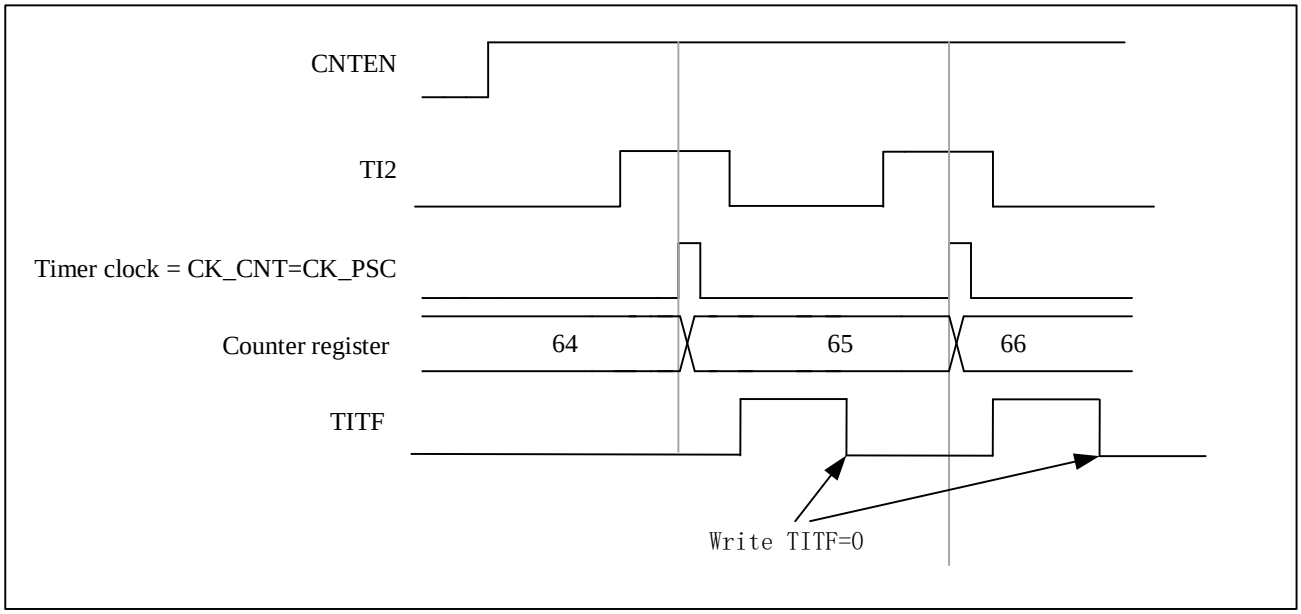
Figure 10-10 Control Circuit in External Clock Mode 1

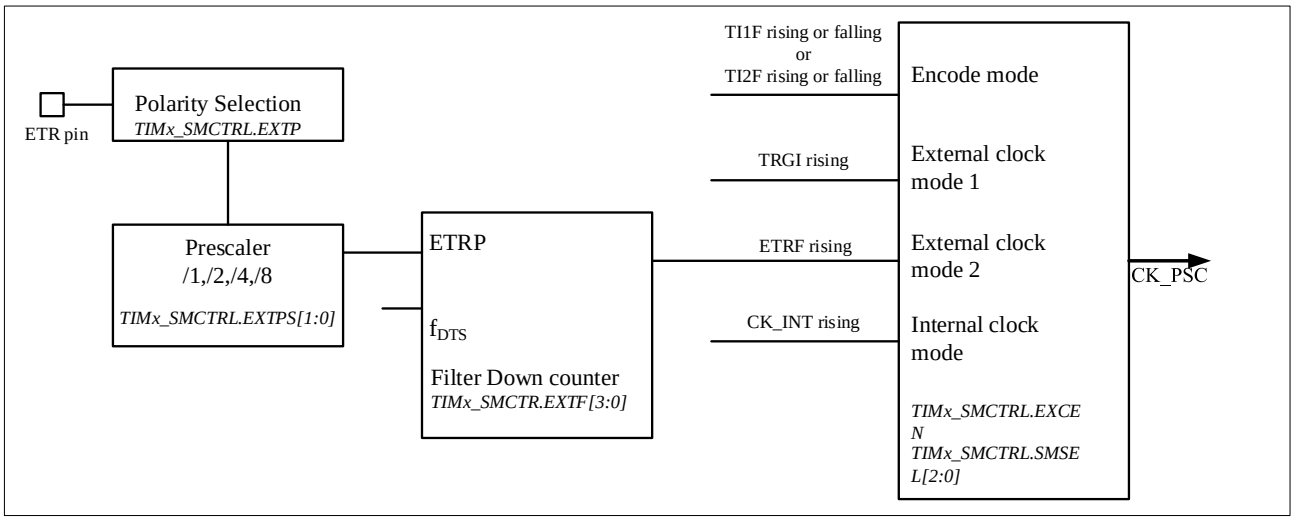


10.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 10-11 External Trigger Input Block Diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'

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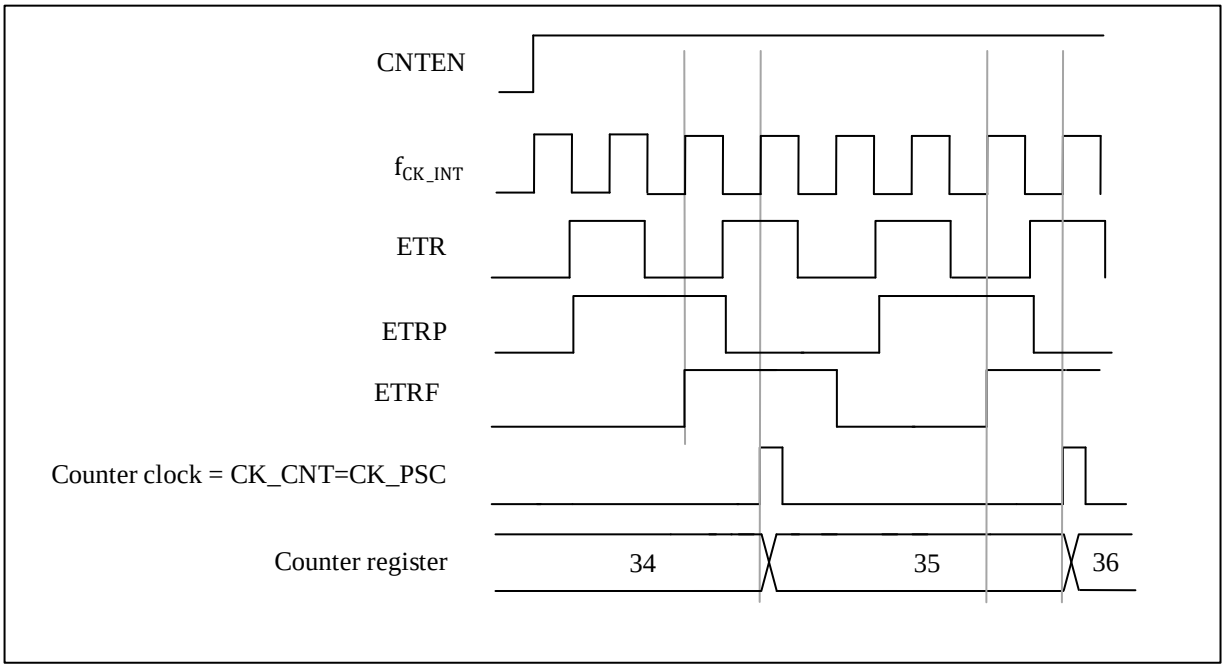
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to ‘1’

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 10-12 Control Circuit in External Clock Mode 2



10.3.4 Capture/Compare Channels

Capture/Compare channels include Capture/Compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after prescale. The following figure shows a block diagram of a capture/compare channel.

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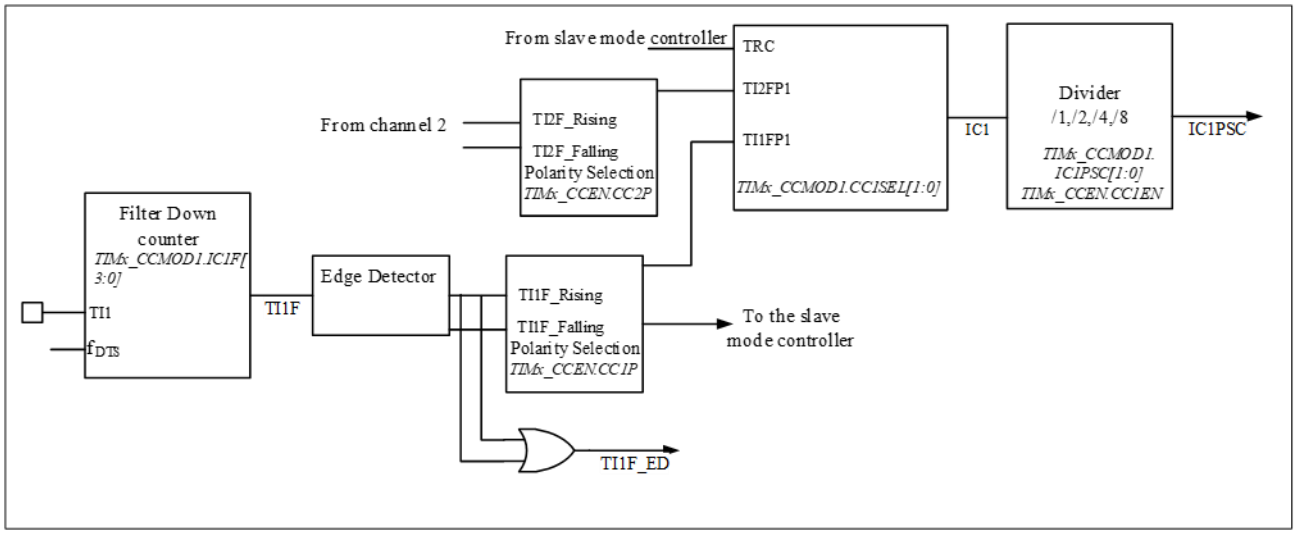
Figure 10-13 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 10-14 Capture/Compare Channel 1 Main Circuit

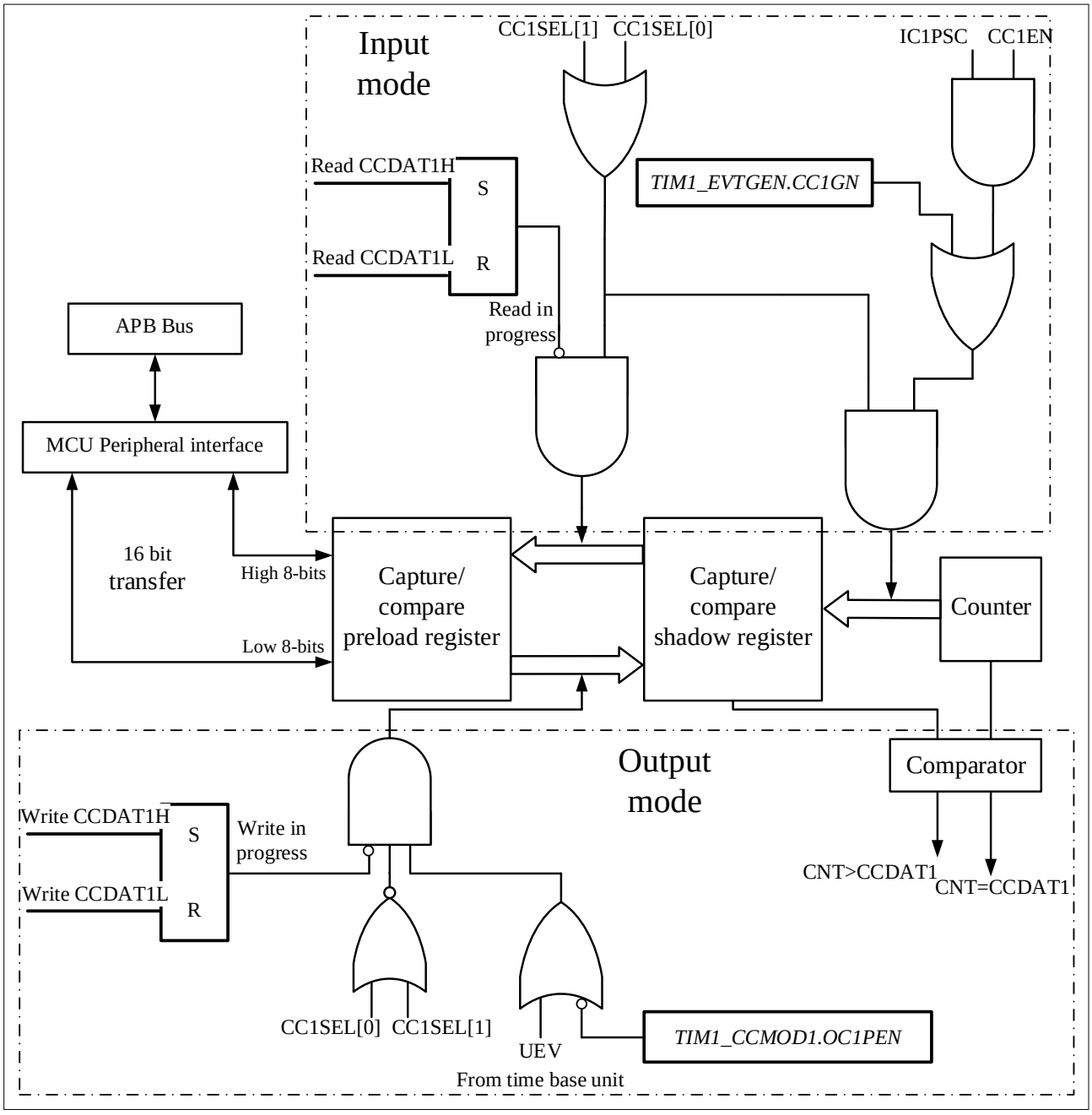

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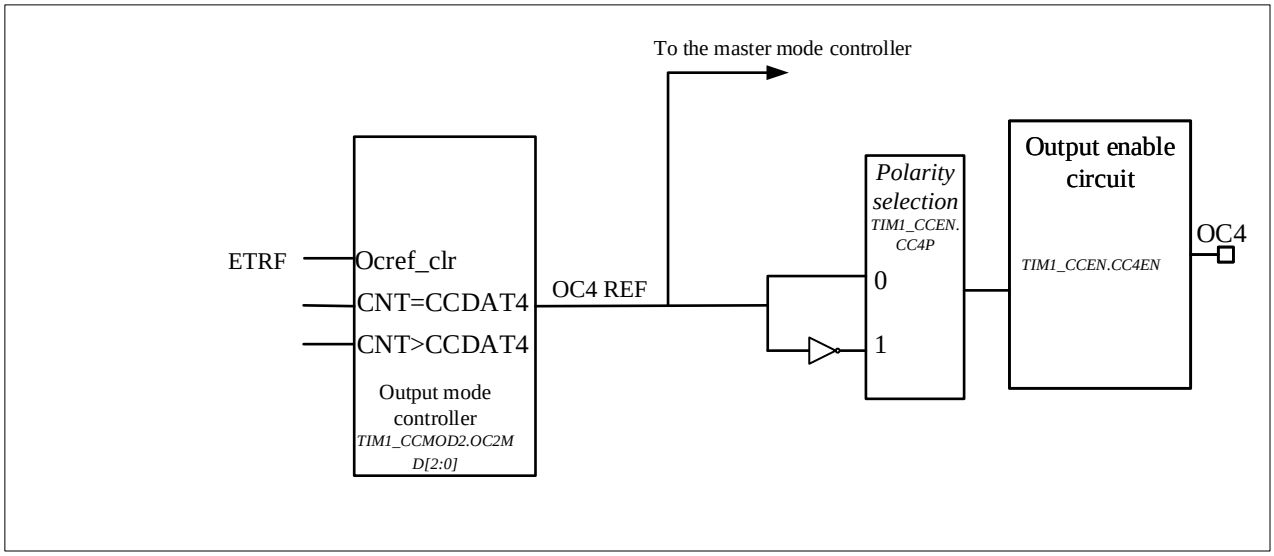
Figure 10-15 Output Part of Channelx (x = 1,2,3,4; Take Channel 4 as an Example)



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

10.3.5 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- The duration of the input filter required for programming：

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a

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filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1.IC1F to '0011'.

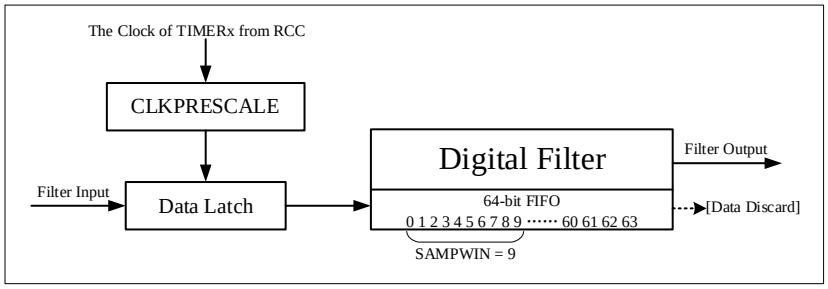
- By configuring TIMx_CCEN.CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC='00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN.CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

10.3.5.1 Channel Input Filtering

The register TIMx_CxFILT (x=1, 2, 3, 4) is described as follows:

Figure 10-16 Sliding Filtering



- Digital filters sample the channel input signal using the RCC's TIMx clock and accumulate the samples in a 64-bit FIFO. Only data sampled within the window size defined in TIMx_CxFILT.WSIZE [5:0] is considered, with a maximum window size of 64.
- The filter outputs the majority value within the sampling window, which is defined by the threshold in TIMx_CxFILT.THRESH [5:0], with a maximum threshold of 63. This value should be equal to or greater than half the window size. If the counts of logic 1 and logic 0 within the sampling window are not greater than the threshold, the digital filter maintains the previous output value.
- TIMx_CxFILT.PSC register determines the sampling rate of the corresponding digital filter. The filter FIFO captures a sample value from the input at each sampling clock.
- If the digital filter is disabled, the filter input is directly output.

10.3.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.

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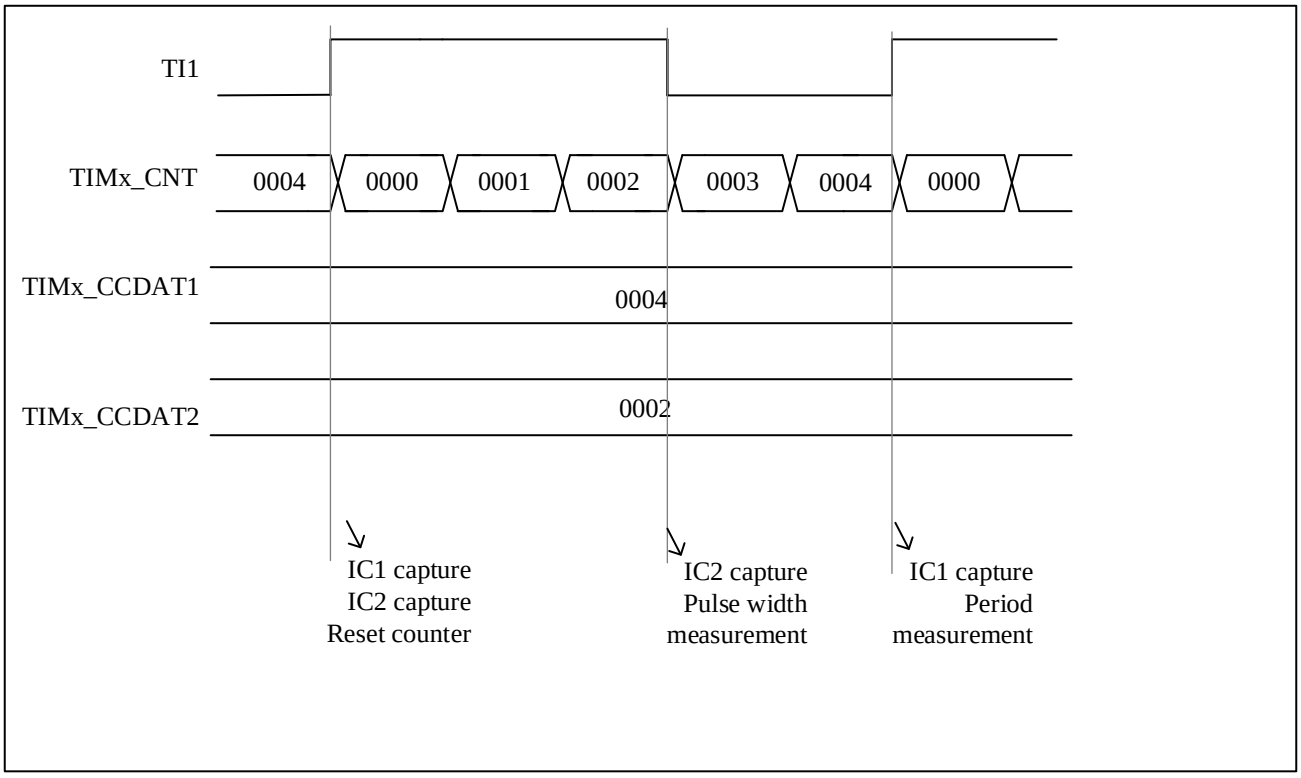
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active at the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active at the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

Figure 10-17 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

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10.3.7 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level, the OCxREF will be forced low.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

10.3.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed。

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level; if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.
- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers (TIMx_CCDATx) or not

The time resolution is one counting period of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with required data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

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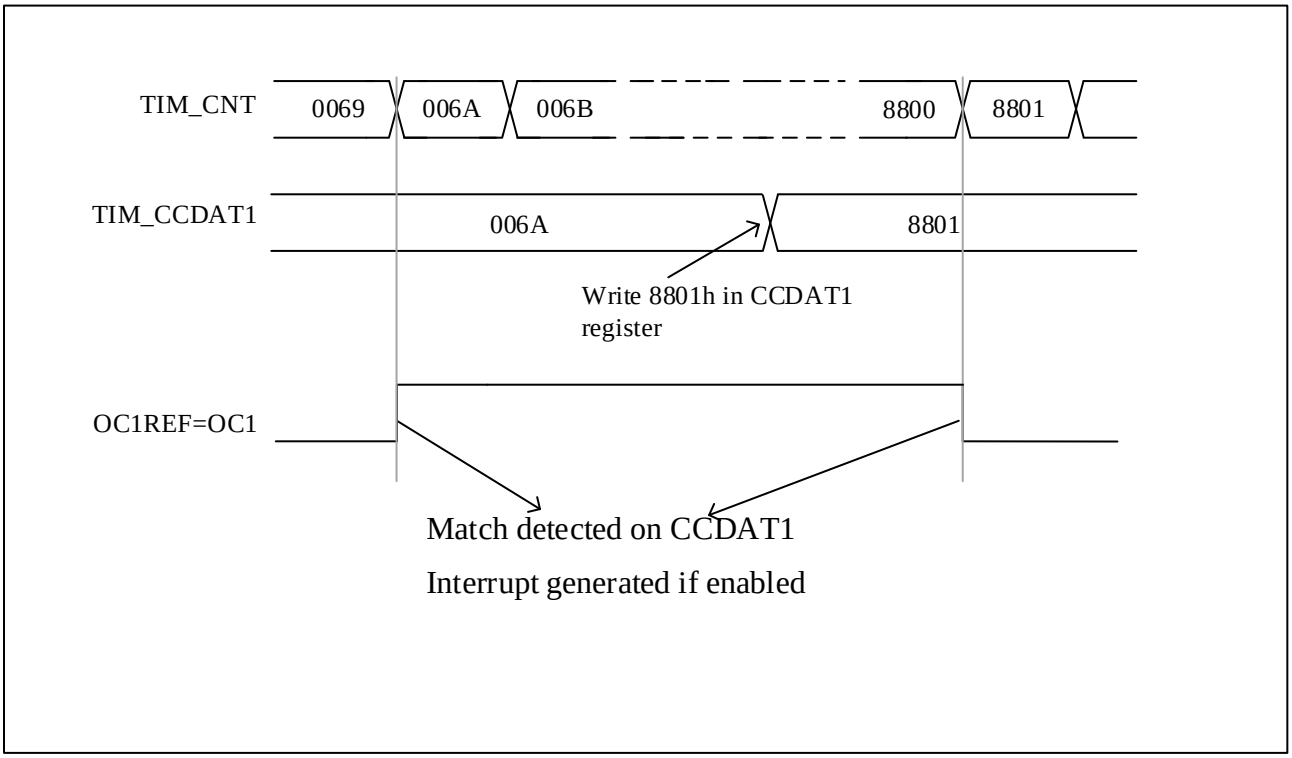
User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event

Here is an example.

Figure 10-18 Output Compare Mode, Toggle on OC1



10.3.9 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

10.3.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

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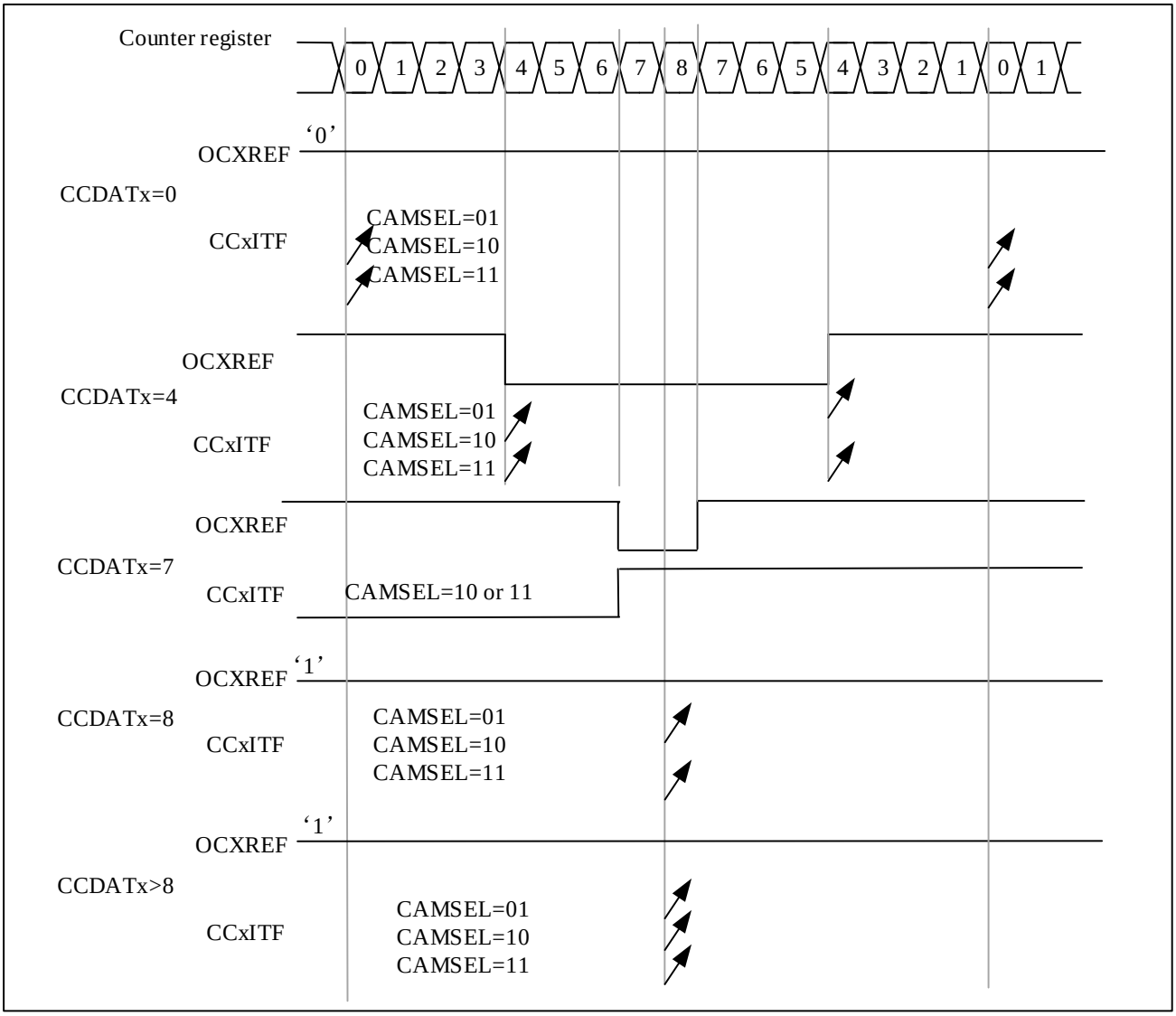
Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1.CAMSEL=01.

Figure 10-19 Center-aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considerations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some examples:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated

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- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and not writing the counter while it is running.

10.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

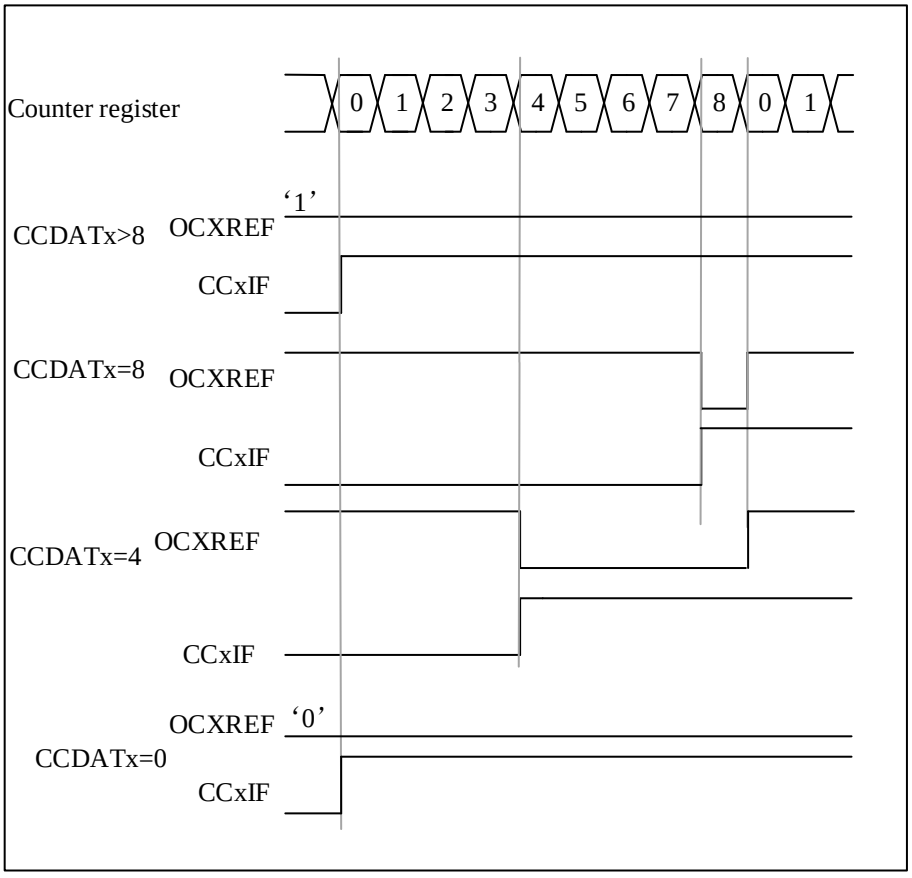
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Example for PWM mode1：

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow:

Figure 10-20 Edge-aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.
Example for PWM mode1：

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the

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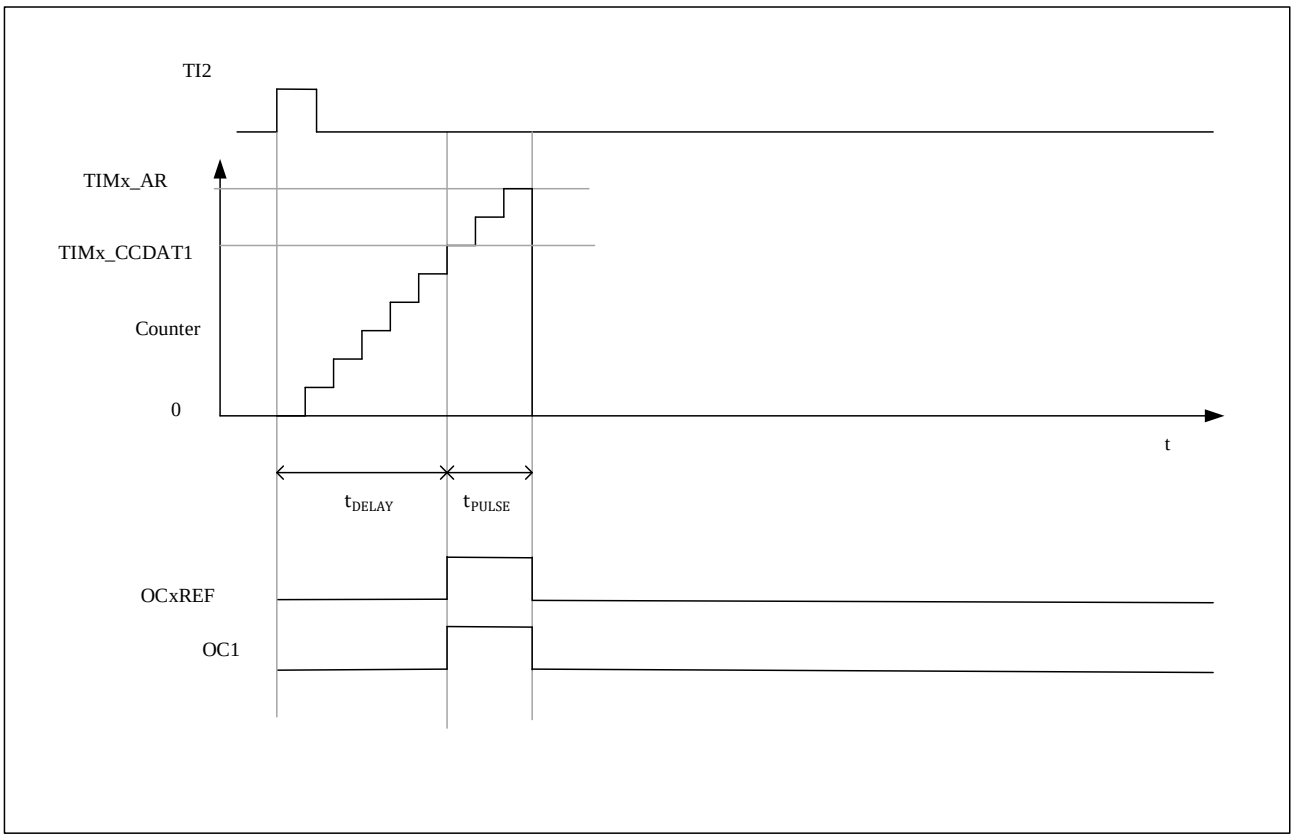
compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

10.3.10 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated

Figure 10-21 Example of One-pulse Mode



The following is an example of a one-pulse mode：

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL='01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P='0';
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL='110' (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value

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of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD='111' to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

10.3.10.1 **Special case: OCx fast enable**

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

10.3.11 Clearing The OCxREF Signal on an External Event

If user set TIMx_CCMODx.OCxCEN=1, high level of tim_ocref_clr_in input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

For example, to control the current, users can connect the ETR signal to the comparator's output. The operation of ETR is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter as needed.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

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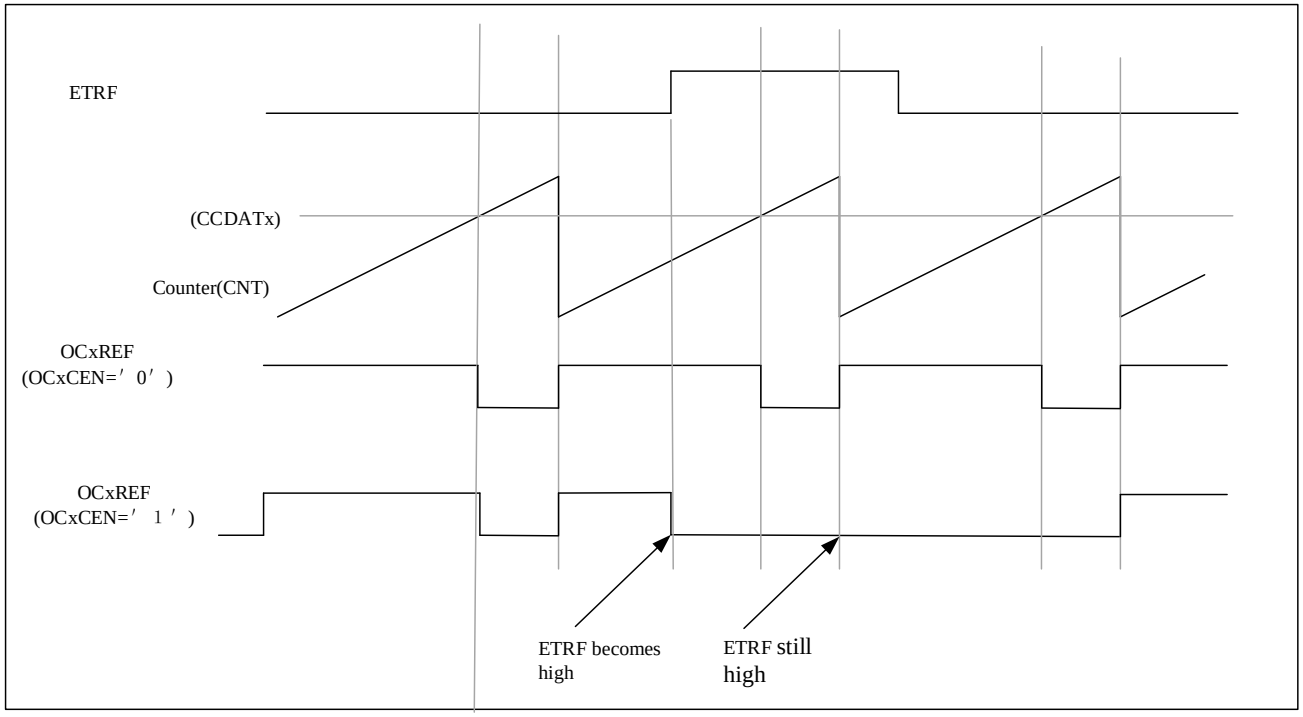
Figure 10-22 Clearing OCxREF of TIMx



10.3.12 Debug Mode

When the microcontroller is in debug mode (the Cortex-M0 core halted), depending on the DBG_CTRL.TIMx_STOP configuration, the TIMx counter can either continue to work normally or stop. For more details, refer to Section 3.4.9.

10.3.13 TIMx and External Trigger Synchronization

Same as the advanced timer, refer to Section 9.3.16.

10.3.14 Timer Synchronization

All TIMx timers are internally interconnected to each other. This implementation allows a master timer to provide trigger to reset, start, stop or provide a clock for the other slave timers. The master clock is used for internal counter and can be prescaled. Below figure shows a block diagram of timer interconnection. The synchronization function does not support dynamic change of the connection. User should configure and enable the slave timer before enabling the master timer's trigger or clock.

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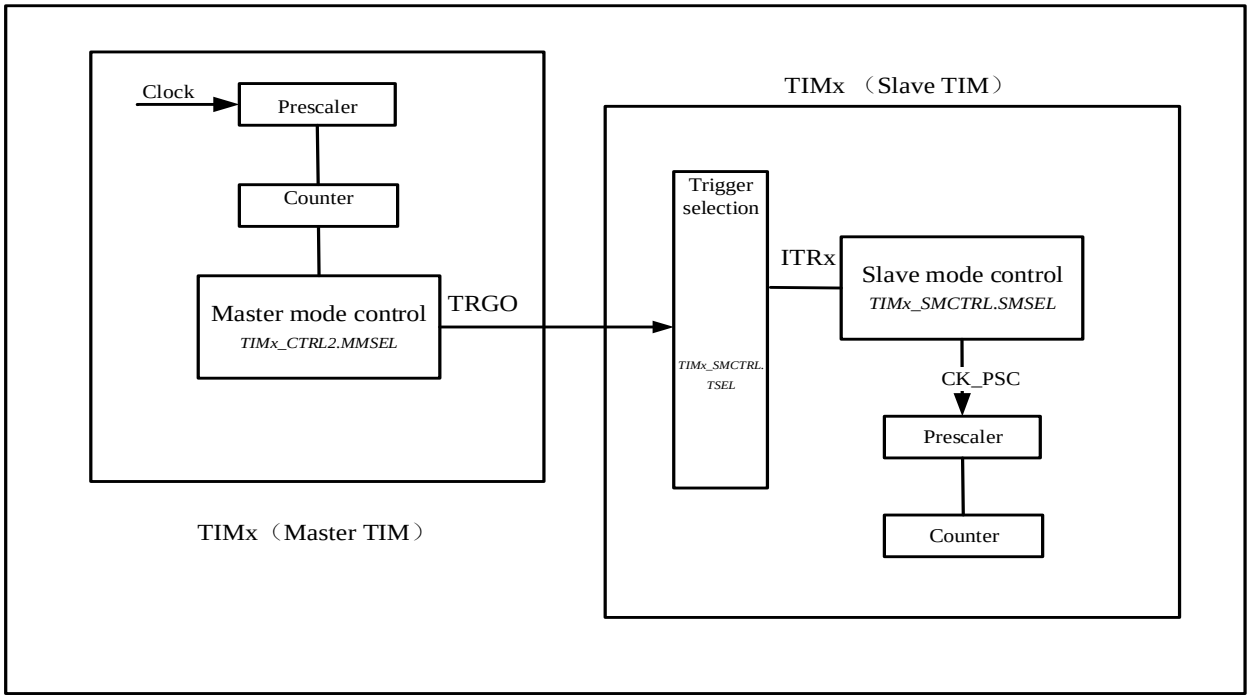
Figure 10-23 Master/Slave Timer Connection



10.3.14.1 **Master timer as a prescaler for another timer**

TIM1 acts as the prescaler for TIM2. TIM1 is master timer, and TIM2 is slave timer.

User needs to do the following steps for this configuration.

- Set TIM1_CTRL2.MMSEL=’010’ to use the update event of TIM1 as trigger output.
- Configure TIM2_SMCTRL.TSEL= ‘000’ to connect the TRGO of TIM1 to TIM2.
- Configure TIM2_SMCTRL.SMSEL = ‘111’ so that the slave mode controller will be configured in external clock mode 1.
- Start TIM2 by setting TIM2_CTRL1. CNTEN = ‘1’.
- Start TIM1 by setting TIM1_CTRL1. CNTEN = ‘1’.

Note: If user select OCx as the trigger output of TIM1 by configuring MMSEL = ‘1xx’, OCx rising edge will be used to drive TIM2.

10.3.14.2 **Master timer to enable another timer**

In this example, TIM2 is enabled by the output compare of TIM1. TIM2 counter will start to count after the OC1REF output from TIM1 is high. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK_CNT} = f_{CK_INT}/3$).

The configuration steps are shown as below。

- Set TIM1_CTRL2.MMSEL=’100’ to use the OC1REF of TIM1 as trigger output.
- Configure TIM1_CCMOD1 register to configure the OC1REF output waveform.

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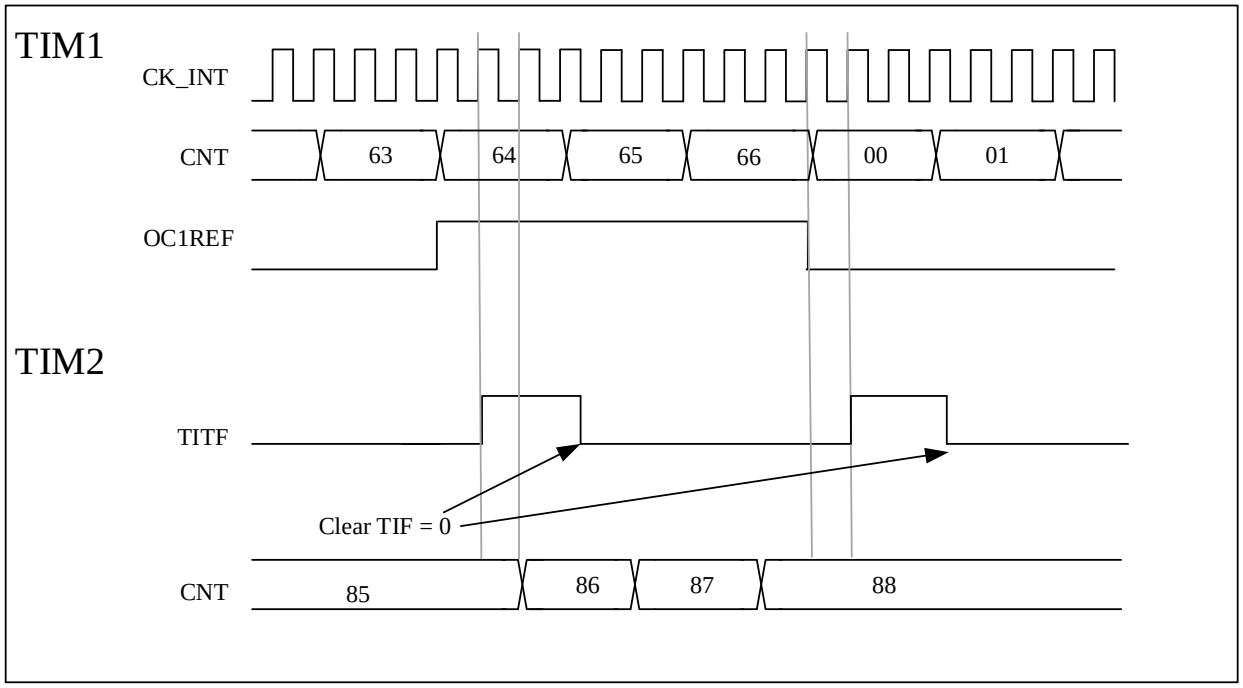
- Set TIM2_SMCTRL.TSEL = ‘000’ to connect TIM1 trigger output to TIM2.
- Set TIM2_SMCTRL.SMSEL= ‘0101’ to set TIM2 to gated mode.
- Set TIM2_CTRL1.CNTEN= ‘1’ to start TIM2.
- Set TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.

Note: The TIM2 clock is not synchronized with the TIM1 clock, this mode only affects the TIM2 counter enable signal.

Figure 10-24 TIM2 Gated by OC1REF of TIM1



In the next example, it sets the enable of TIM2 with enable signal of TIM1. Set TIM1.CTRL1.CNTEN = ‘0’ to stop TIM1. TIM2 counts on the divided internal clock only when TIM1 is enable. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK_CNT} = f_{CK_INT}/3$).

The configuration steps are shown as below:

- Set TIM1_CTRL2.MMSEL=’001’ to use the enable signal of TIM1 as trigger output.
- Set TIM2_SMCTRL.TSEL = ‘000’ to configure TIM2 to get the trigger input from TIM1.
- Set TIM2_SMCTRL.SMSEL = ‘101’ to configure TIM2 in gated mode.
- Set TIM2_CTRL1.CNTEN= ‘1’ to start TIM2.
- Set TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.
- Set TIM1_CTRL1.CNTEN= ‘0’ to stop TIM1.

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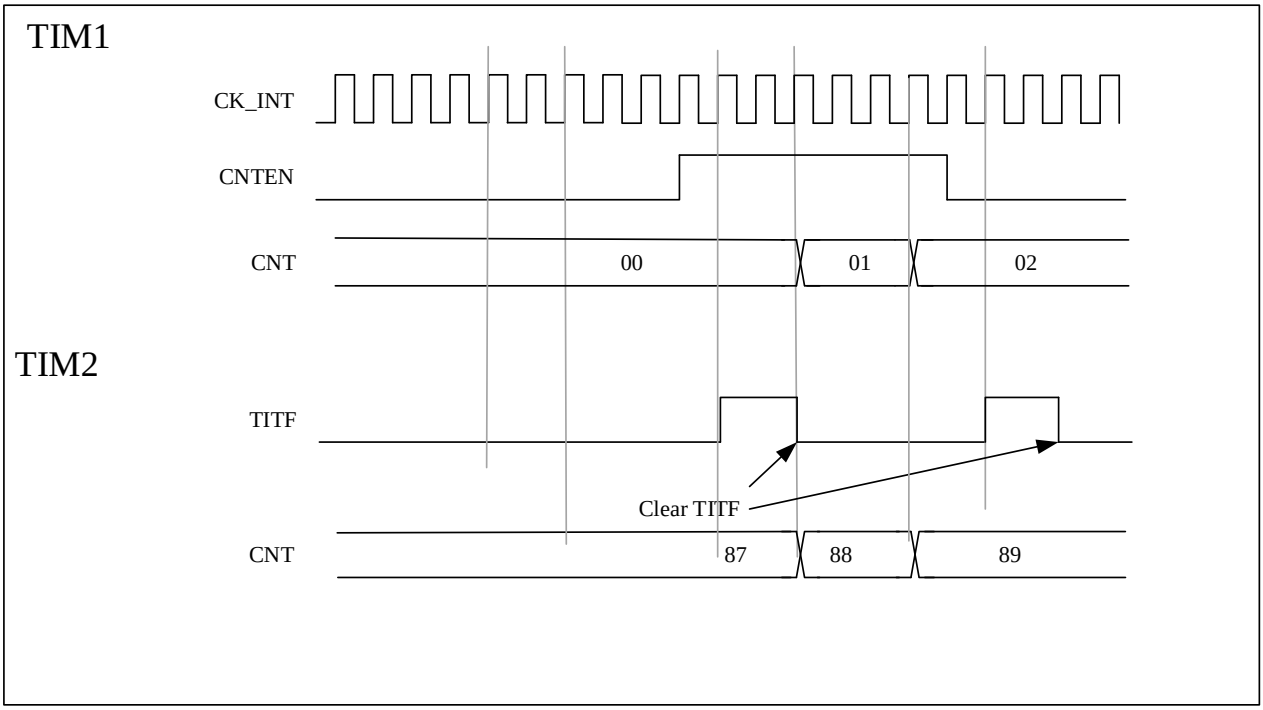
Figure 10-25 TIM2 Gated by Enable Signal of TIM1



10.3.14.3 **Master timer to start another timer**

In this example, we can use update event as trigger source. TIM1 is master, TIM2 is slave.

The configuration steps are shown as below:

- Set TIM1_CTRL2.MMSEL=’ 010’ to use the update event of TIM1 as trigger output.
- Configure TIM1_AR register to set the output period.
- Set TIM2_SMCTRL .TSEL= ‘000’ to connect TIM1 trigger output to TIM2.
- Set TIM2_SMCTRL. SMSEL = ‘110’ to set TIM2 to trigger mode.
- Set TIM1_CTRL1.CNTEN=1 to start TIM1.

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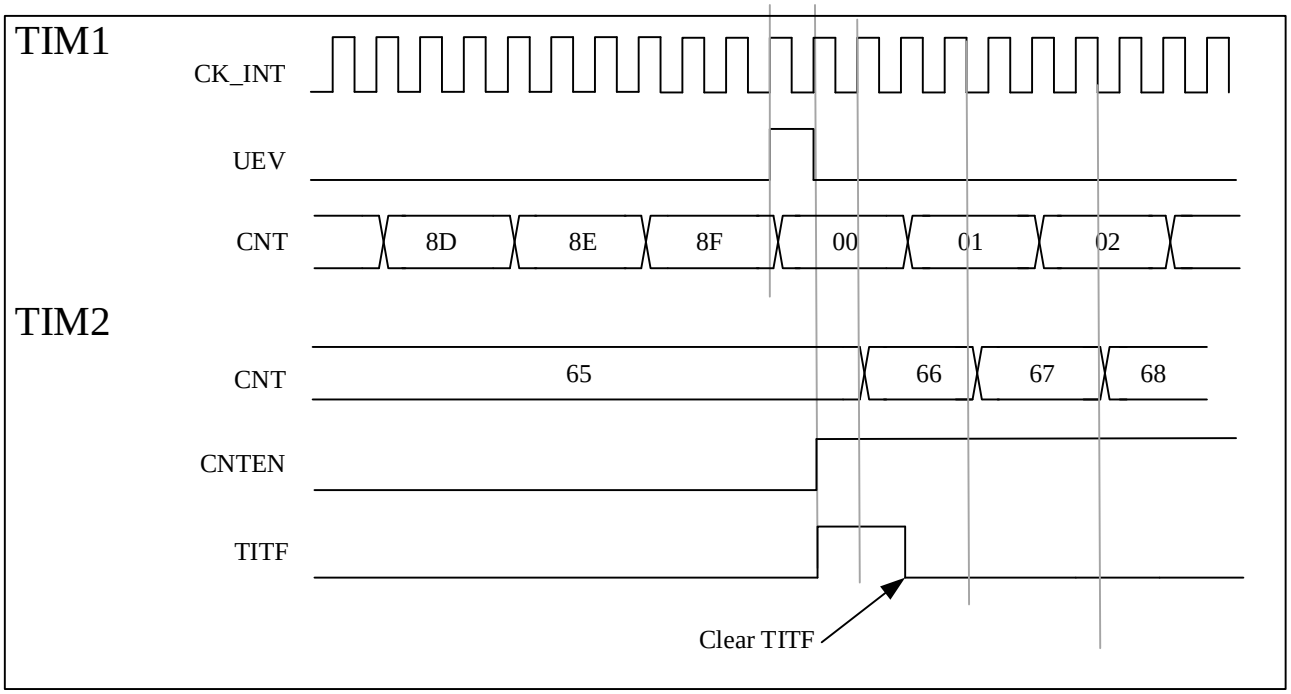
Figure 10-26 Trigger TIM2 with an Update of TIM1



10.3.14.4 **Start 2 timers synchronously using an external trigger**

In this example, TIM1 is enabled when TIM1's TI1 input rises, and TIM2 is enabled when TIM1 is enabled. To ensure the alignment of counters, TIM1 must be configured in master/slave mode. For TI1, TIM1 is the slave; for TIM2, TIM1 is the master.

The configuration steps are shown as below:

- Set TIM1.MMSEL = '001' to use the enable signal as trigger output.
- Set TIM1_SMCTRL.TSEL = '100' to configure the TIM1 to slave mode and receive the trigger input of TI1.
- Set TIM1_SMCTRL.SMSEL = '0110' to configure TIM1 to trigger mode.
- Set TIM1_SMCTRL.MSMD = '1' to configure TIM1 to master/slave mode.
- Set TIM2_SMCTRL.TSEL = '000' to connect TIM1 trigger output to TIM2.
- Set TIM2_SMCTRL.SMSEL = '110' to configure TIM2 to trigger mode.

When TI1 rising edge arrives, both timers start counting synchronously according to the internal clock, and both TITF flags are set simultaneously.

Note：The following figure shows a delay between CNTEN and CK_PSC of TIM1 in master/slave mode.

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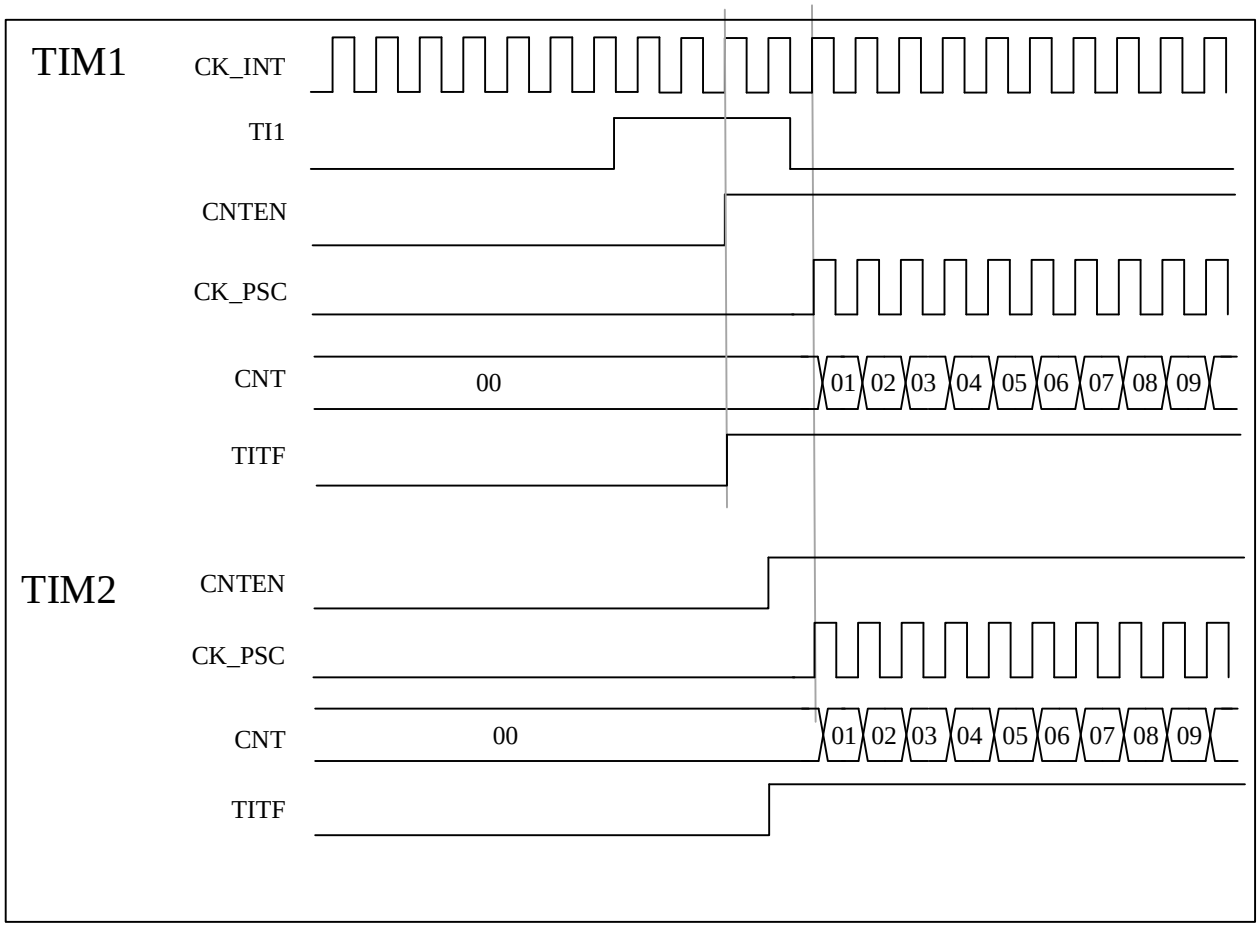
Figure 10-27 Triggers TIM1 and TIM2 Using the TI1 Input of TIM1



10.3.15 Encoder Interface Mode

The encoder uses two inputs TI1 and TI2 as an interface. And the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are five types of quadrature encoder counting modes:

- Encode Mode 1: The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘001’;
- Encode Mode 2: The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’010’;
- Encode Mode 3: The counter counts on both TI1 and TI2 edges, TIMx_SMCTRL.SMSEL = ‘011’;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in following table:

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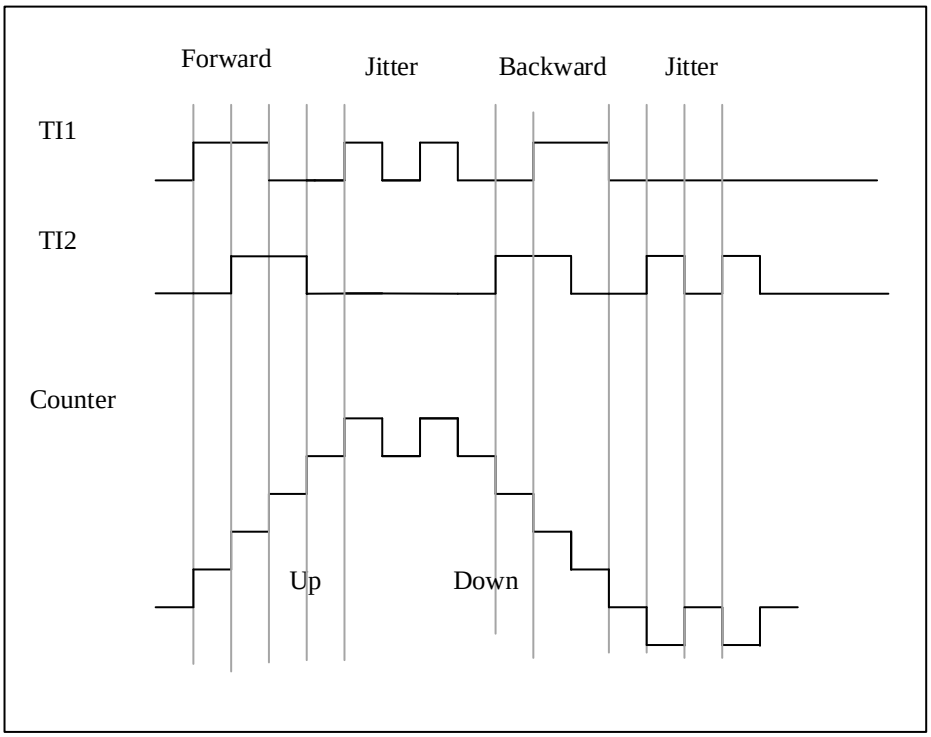
Table 10-1 The Relationship between the Counting Direction and the Encoder Signal (CC1P=CC2P=0)

Active Edge	Relative Signal Level（TI1FP1 for TI2, TI2FP2 for TI1）	TI1FP1 Signal		TI2FP2 Signal	
		Rising	Falling	Rising	Falling
Counting only at TI1	High	Counting down	Counting up	Don’t count	Don’t count
	Low	Counting up	Counting down	Don’t count	Don’t count
Counting only at TI2	High	Don’t count	Don’t count	Counting up	Counting down
	Low	Don’t count	Don’t count	Counting down	Counting up
Counting on TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edges triggering selected to suppress input jitter：

1. IC1FP1 is mapped to TI1(TIMx_CCMOD1.CC1SEL=‘01’), IC1FP1 is not inverted(TIMx_CCEN.CC1P=‘0’);
2. IC1FP2 is mapped to TI2(TIMx_CCMOD2.CC2SEL=‘01’), IC2FP2 is not inverted(TIMx_CCEN.CC2P=‘0’);
3. The input is valid on both rising and falling edges(TIMx_SMCTRL.SMSEL=‘0011’);
4. Enable counter TIMx_CTRL1.CNTEN=‘1’;

Figure 10-28 Example of Counter Operation in Encoder Interface Mode



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Email：info@nationstech.com
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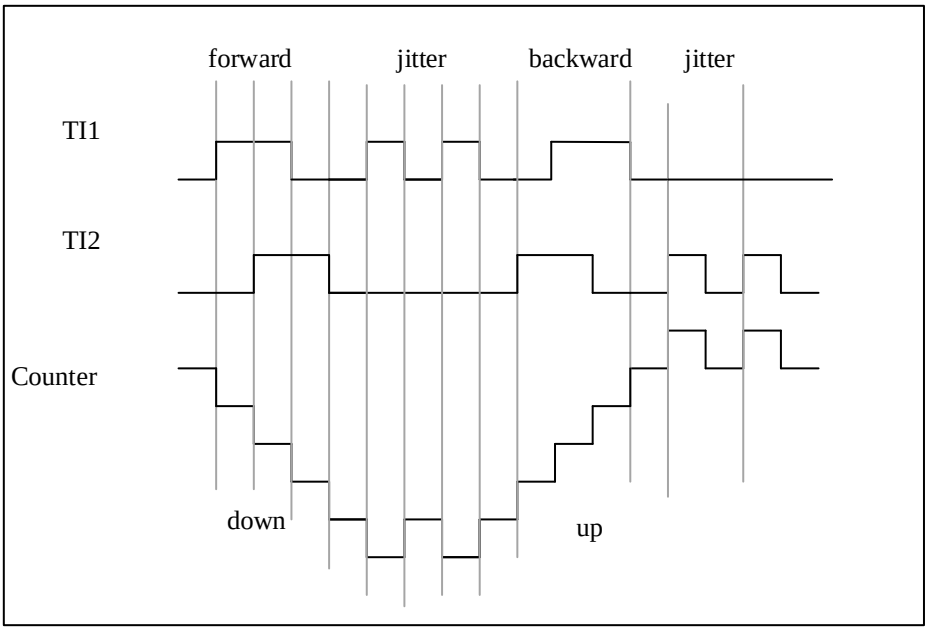
The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P='1', other configurations are the same as above)

Figure 10-29 Encoder Interface Mode Example with IC1FP1 Polarity Inverted



10.3.16 Interfacing with Hall Sensor

Please refer to Section 9.3.20.

10.4 TIMx Register Description (x=2, 3, 4, 5)

For abbreviations used in the registers, please refer to Section 1.1.

These peripheral registers can be operated as half-word (16 bits) or word (32 bits).

10.4.1 Register Overview

Table 10-2 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved												C4SEL	C3SEL	Reserved	C1SEL	Reserved		CLRSEL	IOMBKP	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
	Reset Value													0	0		0			0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved												TI1SEL	Reserved	CCDSEL	Reserved	MMSEL[2:0]				Reserved											
	Reset Value													0		0		0	0	0	0												
008h	TIMx_STS	Reserved													TITF	Reserved	UDITF	Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved				CC4ITF	CC3ITF	CC2ITF	CC1ITF
	Reset Value														0		0					0	0	0	0					0	0	0	0
00Ch	TIMx_EVTGEN	Reserved																					TGN	Reserved	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
	Reset Value																						0		0					0	0	0	0
010h	TIMx_SMCTRL	Reserved															MSMD	EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		Reserved	SMSEL[2:0]		Reserved	TSEL[2:0]			

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| | | |

| | | |

Bit Field	Name	Description
		0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs。 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and t_{DTS} (clock used for dead-time generator and digital filters (ETR, TIx)) 00: tDTS = tCK_INT · 01: tDTS = 2 x tCK_INT 10: tDTS = 4 x tCK_INT 11: Reserved, do not use this configuration
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request – Counter overflow/underflow – TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting。 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting。 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting。 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting。 *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1)*
1	DIR	Direction 0: Up-counting

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Bit Field	Name	Description
		1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

10.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												TI1SEL	Reserved	CCDSEL	Reserved
												rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved											
rw															

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input; 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	Reserved	Reserved, the reset value must be maintained
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent； 1: When an update event occurs, a DMA request for CCx is sent.
16	Reserved	Reserved, the reset value must be maintained
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits (TIMx_CTRL2. MMSEL [3:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows： x000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the later case, the signal on TRGO is delayed compared to the actual reset. x001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO

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Email：info@nationstech.com
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Bit Field	Name	Description
		except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). x010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. x011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. x100: Compare - OC1REF signal is used as the trigger output (TRGO). x101: Compare - OC2REF signal is used as the trigger output (TRGO). x110: Compare - OC3REF signal is used as the trigger output (TRGO). x111: Compare - OC4REF signal is used as the trigger output (TRGO)
11:0	Reserved	Reserved, the reset value must be maintained

10.4.4 Status Registers (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TITF	Reserved	UDITF
													rc_w0		rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved				CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0					rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred； 1: Trigger interrupt occurred.
17	Reserved	Reserved, the reset value must be maintained
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and repetition counter value overflow or underflow (when repetition counter equal to 0 an update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred

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Bit Field	Name	Description
		1: Update interrupt occurred
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag See TIMx_STS.CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred; 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7:4	Reserved	Reserved, the reset value must be maintained.
3	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode：** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

10.4.5 Event Generation Registers (TIMx_EVTGEN)

Offset address: 0x0C

Reset values: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TGN	Reserved	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
					w		w					w	w	w	w

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action No action 1: Generated a trigger event
9	Reserved	Reserved, the reset value must be maintained
8	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

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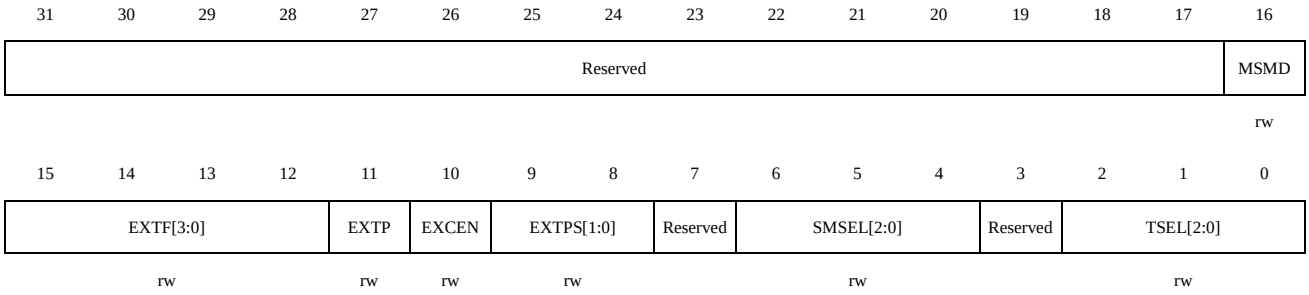
10.4.6 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x10

Reset value: 0x0000 0000



Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	MSMD	Master/slave mode 0: No effect; 1: The event on the trigger input (TRGI) is delayed to allow perfect synchronization between the current timer (via TRGO) and its slave timers. This is very useful for cases where multiple timers need to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS/8}$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS/8}$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS/16}$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS/16}$, N=6 0100: $f_{SAMPLING}=f_{DTS/2}$, N=6 1100: $f_{SAMPLING}=f_{DTS/16}$, N=8 0101: $f_{SAMPLING}=f_{DTS/2}$, N=8 1101: $f_{SAMPLING}=f_{DTS/32}$, N=5 0110: $f_{SAMPLING}=f_{DTS/4}$, N=6 1110: $f_{SAMPLING}=f_{DTS/32}$, N=6 0111: $f_{SAMPLING}=f_{DTS/4}$, N=8 1111; $f_{SAMPLING}=f_{DTS/32}$, N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note2: The following slave modes can be used simultaneously with external clock mode 2: reset*

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Email：info@nationstech.com
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Bit Field	Name	Description
		mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111'). *Note3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
7	Reserved	Reserved, the reset value must be maintained
6:4	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1。 010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*
3	Reserved	Reserved, the reset value must be maintained
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: Edge detector for TI1 (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1 (TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External trigger input (ETRF)

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Email：info@nationstech.com
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Bit Field	Name	Description
		Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.

Table 10-3 TIMx Internal Trigger Connection

Slave Timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM5	TIM2	TIM3	TIM4
TIM2	TIM1	NA	TIM3	TIM4
TIM3	TIM1	TIM2	TIM5	TIM4
TIM4	TIM1	TIM2	TIM3	NA
TIM5	TIM2	TIM3	TIM4	NA

10.4.7 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										TDEN	Reserved	UDEN	Reserved	TIEN	UIEN
										rw		rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved				CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request. 1: Enable trigger DMA request
20	Reserved	Reserved, the reset value must be maintained
19	UDEN	Update DMA request enable 0: Disable update DMA request. 1: Enable update DMA request
18	Reserved	Reserved, the reset value must be maintained
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request

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Tel：+86-755-86309900
Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: Enable capture/compare 4 DMA request
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt

10.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output. 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by tim_ocref_clr_in input level. 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high (the source of tim_ocref_clr_in is controlled by TIMx_CTRL1.CLRSEL).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		is 5 clock cycles 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output. 01: CC1 channel is configured as input, IC1 is mapped on TI1. 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Iutput capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel: 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8
3:2	IC1PSC[1:0]	Input capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 Selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

10.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000 0000

See the description of the CCMOD1 register above

Output comparison mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode
12	OC4CEN	Output compare 4 clear enable
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

10.4.10 Capture/Compare Enable Registers (TIMx_CCEN)

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN	Reserved	
rw	rw			rw	rw			rw	rw			rw	rw		

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
14	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
13:12	Reserved	Reserved, the reset value must be maintained.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enabl） See TIMx_CCEN.CC1EN description.
9:8	Reserved	Reserved, the reset value must be maintained.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5:4	Reserved	Reserved, the reset value must be maintained.
3	CC1P	Capture/Compare 1 output polarity **When the corresponding channel of CC1 is in output mode:** 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted.
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. Therefore, the output level of OC1 depends on the values of MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. 1: Enable - Enable output OC1 signal. The OC1 signal is output to the corresponding output pin, and its output level depends on the values of the MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1:0	Reserved	Reserved, the reset value must be maintained.

Table 10-4 Output Control Bits of Standard OCx Channel

CCxEN	OCx Output Status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: The state of external I/O pins connected to standard OCx channels depends on the OCx channel state and GPIO and AFIO registers.

10.4.11 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

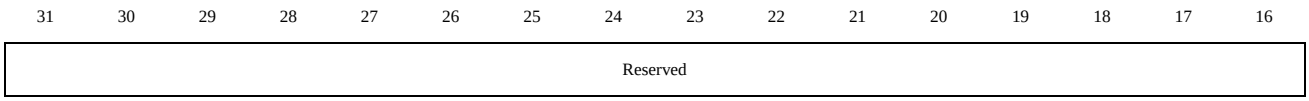
rw

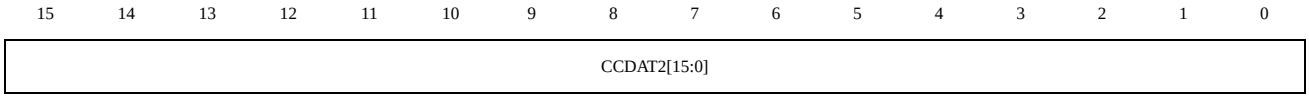
Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT1[15:0]	Capture/Compare 1 value CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

10.4.12 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x2C

Reset value: 0x0000 0000





rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT2[15:0]	Capture/Compare 2 value CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

10.4.13 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x30

Reset value: 0x0000 0000

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Email：info@nationstech.com
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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT3[15:0]	Capture/Compare 3 value CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 is only readable. When configured as output mode, register CCDAT3 is readable and writable.

10.4.14 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT4[15:0]															

rw

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT4[15:0]	Capture/Compare 4 value CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 is only readable. When configured as output mode, register CCDAT4 is readable and writable.

10.4.15 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK_CNT} = f_{CK_PSC}/ (PSC [15:0] +1)$. Each time an update event occurs, the PSC value is loaded into the active prescaler register.

10.4.16 Auto-reload Register (TIMx_AR)

Offset address: 0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															
rw															

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See Section 10.4.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

10.4.17 Counters (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CNT[15:0]	Counter value

10.4.18 Channel 1 Filter Register (TIMx_C1FILT)

Offset address: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PSC							
								rw							

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	PSC[15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 128 division (8 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations.

10.4.19 Channel 2 Filter Register (TIMx_C2FILT)

Offset address: 0x68

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PSC							
								rw							

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit

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Email：info@nationstech.com
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Bit Field	Name	Description
		(pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	PSC[15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 128 division (8 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations.

10.4.20 Channel 3 Filter Register (TIMx_C3FILT)

Offset address: 0x6C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PSC							
								rw							

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range:

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Email：info@nationstech.com
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Bit Field	Name	Description
		Minimum value: one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌜3.2⌝ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	PSC[15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 128 division (8 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations.

10.4.21 Channel 4 Filter Register (TIMx_C4FILT)

Offset address: 0x70

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH						Reserved	WSIZE						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PSC							
								rw							

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value

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Email：info@nationstech.com
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Bit Field	Name	Description
		Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	PSC[15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 128 division (8 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations.

10.4.22 Input Channel Filter Output Register (TIMx_FILTO)

Offset address: 0x74

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												C4FILTO	C3FILTO	C2FILTO	C1FILTO
												r	r	r	r

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	C4FILTO	Channel 4 filter output level status 0: Output low level; 1: Output high level;
2	C3FILTO	Channel 3 filter output level status 0: Output low level;

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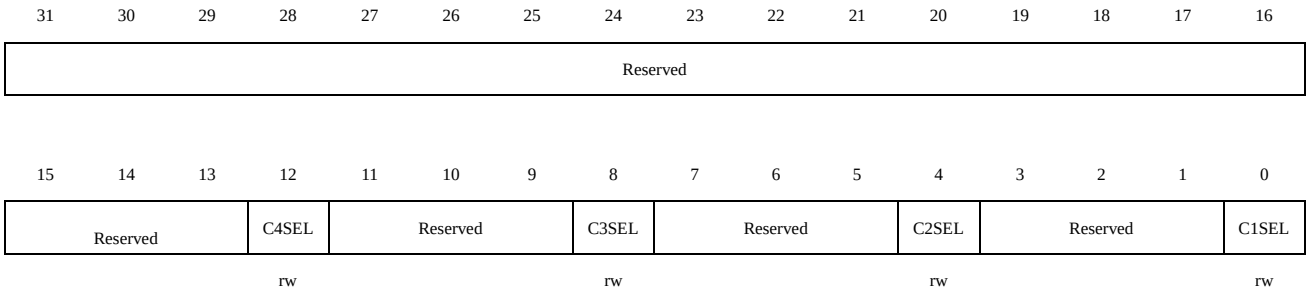
Bit Field	Name	Description
		1: Output high level;
1	C2FILTO	Channel 2 filter output level status 0: Output low level; 1: Output high level;
0	C1FILTO	Channel 1 filter output level status 0: Output low level; 1: Output high level;

10.4.23 Input Selection Register (TIMx_INSEL)

Offset address: 0x78

Reset value: 0x0000 0000



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	C4SEL	Select the input signal for input channel 4 0: select signal from IOM 1: select signal from COMP *Note: only valid for TIM2/TIM3/TIM4/TIM5*
11:9	Reserved	Reserved, the reset value must be maintained.
8	C3SEL	Select the input signal for input channel 3 0: select signal from IOM 1: select signal from COMP *Note: only valid for TIM2/TIM3/TIM4/TIM5*
7:5	Reserved	Reserved, the reset value must be maintained.
4	C2SEL	Select the input signal for input channel 2 0: select signal from IOM 1: select signal from COMP *Note: only valid for TIM2/TIM3/TIM4/TIM5*
3:1	Reserved	Reserved, the reset value must be maintained.
0	C1SEL	Select the input signal for input channel 1 0: select signal from IOM 1: select signal from COMP *Note: only valid for TIM2/TIM3/TIM4/TIM5*

10.4.24 DMA Control Register (TIMx_DCTRL)

Offset address：0x94

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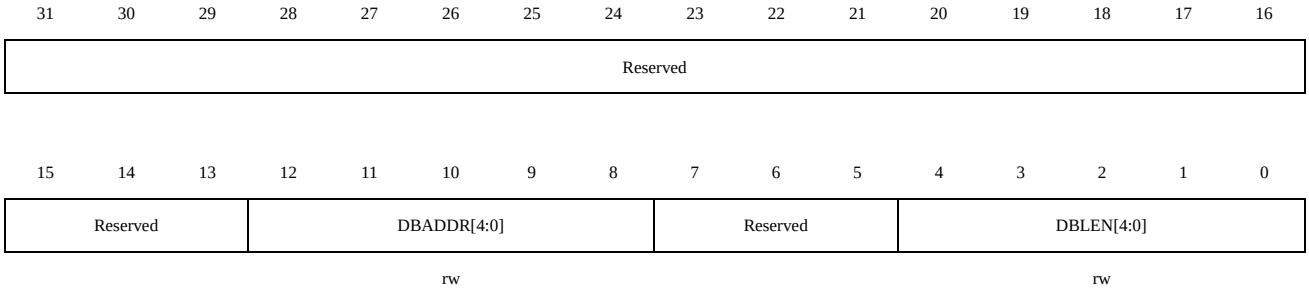
Reset value：0x0000 0000



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12:8	DBADDR[4:0]	DMA base address This Bit Field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 00000: TIMx_CTRL1, 00001: TIMx_CTRL2, 00010: TIMx_SMCTRL, ... 10001: TIMx_BKDT, 10010: TIMx_DCTRL,
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	DBLEN[4:0]	DMA burst length This Bit Field defines the number DMA will accesses (write/read) TIMx_DADDR register. 00000: 1 time transfer 00001: 2 times transfer 00010: 3 times transfer … 10001: 18 times transfer Example: We consider the following transfer: DBLEN=7, DBADDR=TIMx_CTRL1 If DBLEN=7 and DBADDR=TIMx_CTRL1 represent the address of the data to be transferred, then the address of the transfer is given by the following equation ((Address of TIMx_CTRL1) + DBADDR + (DMA index)), where DMA index = DBLEN. Adding 7 to ((Address of TIMx_CTRL1) + DBADDR) gives the address where data will be written to or read from, resulting in data transfer occurring in 7 registers starting from the address ((Address of TIMx_CTRL1) + DBADDR). If the data is set as half-word (16 bits), then the data will be transferred to all 7 registers If the data is set as bytes, the data will still be transferred to all 7 registers: the first register contains the first MSB byte, the second register contains the first LSB byte, and so on. Therefore, for the timer, the user must specify the data width to be transferred by DMA.

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Email：info@nationstech.com
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10.4.25 DMA Transfer Buffer Register (TIMx_DADDR)

Offset address: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	BURST[15:0]	DMA accessing buffer When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4; DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

11 Basic Timers (TIM6)

11.1 Introduction

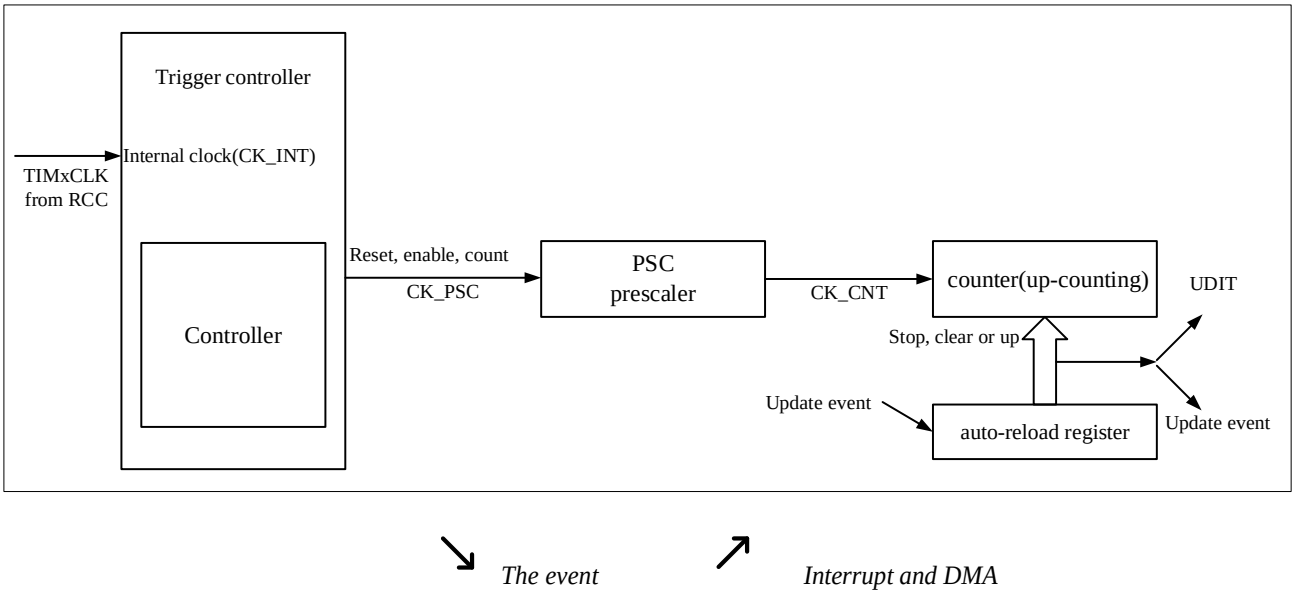
Basic timers TIM6 contain a 16-bit auto-reload counter.

11.2 Main Features

- 16-bit auto-reload up-counting counter.
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536).
- The events that generate the interrupt/DMA are as follows:
  - Update event
- Support STOP mode wake-up: When the clock source is configured as LSI, wake-up from STOP mode can be achieved by updating interrupt (connected to EXTI 20).

The block diagram of TIM6 is shown below:

Figure 11-1 Block Diagram of TIMx (x = 6)



11.3 Function Description

11.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload register. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Note: When the clock source is configured as LSI, TIMx_CNT does not support writing.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. When TIMx_CTRL1.UPDIS=0, an update event is generated when the counter reaches the overflow condition, or when the

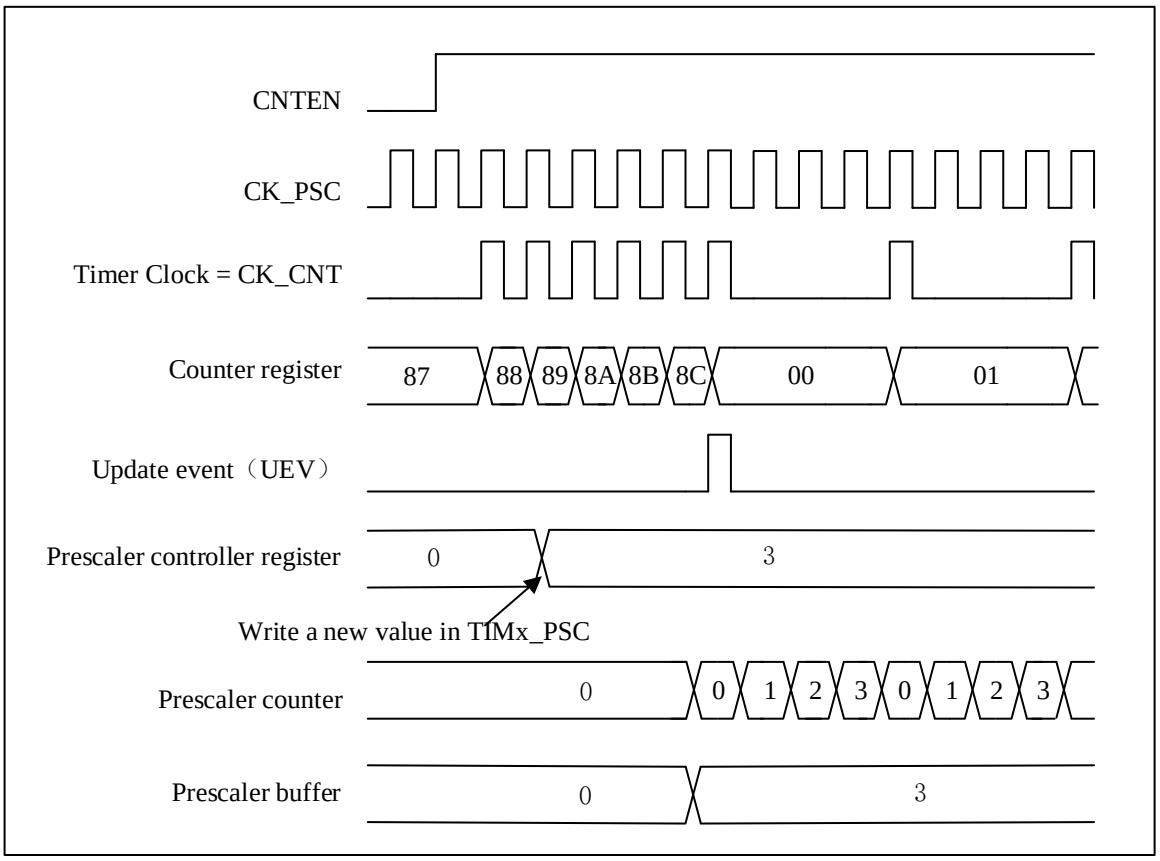
Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

TIMx_EVTGEN.UDGN bit is set by software. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

11.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 11-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



11.3.2 Counter Mode

11.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate, but TIMx_STS.UDITF will not be set by hardware. Therefore, no update interrupts or DMA update requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in TIMx_CTRL1.UPRS, when an update event occurs, TIMx_STS.UDITF is set and all registers are updated:

- Update auto-reload shadow registers with preload value (TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value (TIMx_PSC).

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Email：info@nationstech.com
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To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

In this way, when an update event occurs, the counter and the prescaler counter will also be reset to 0 (but the prescaler rate will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different clock frequencies in the up-counting mode.

Figure 11-3 Timing Diagram of Up-counting, the Internal Clock Divider Factor = 2/N

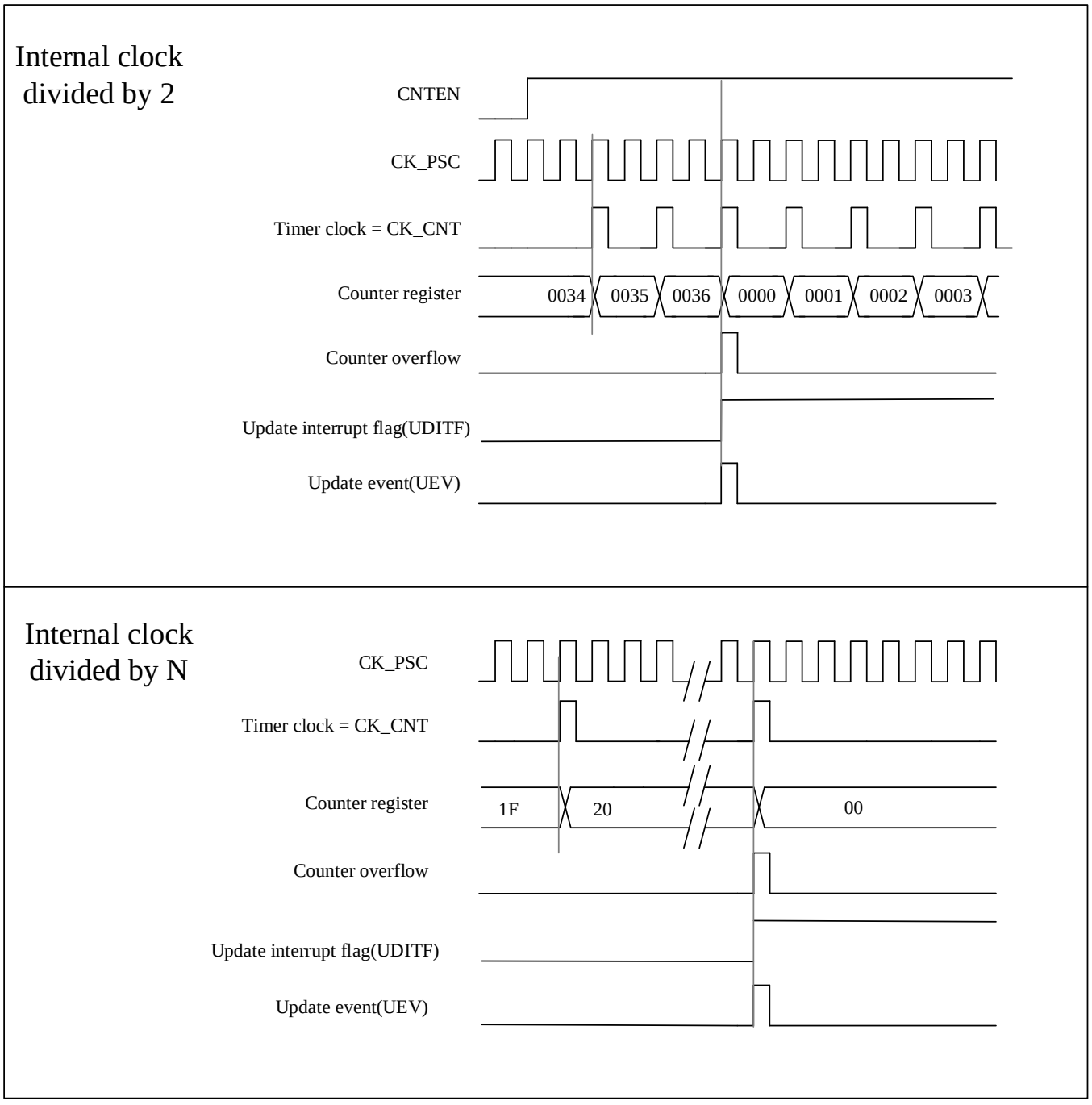

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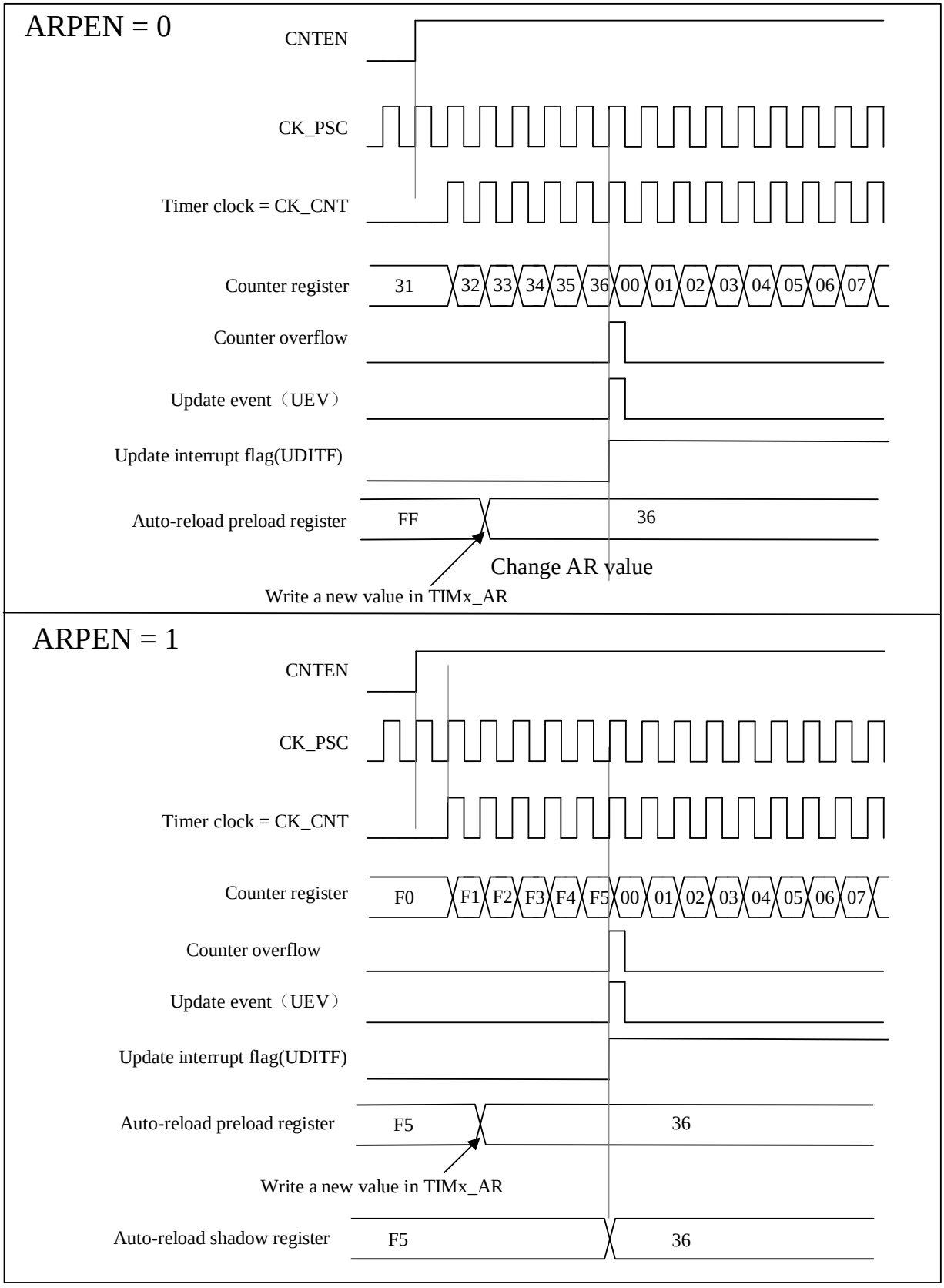
Figure 11-4 Timing Diagram of the Up-counting, Update Event When ARPEN = 0/1



Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
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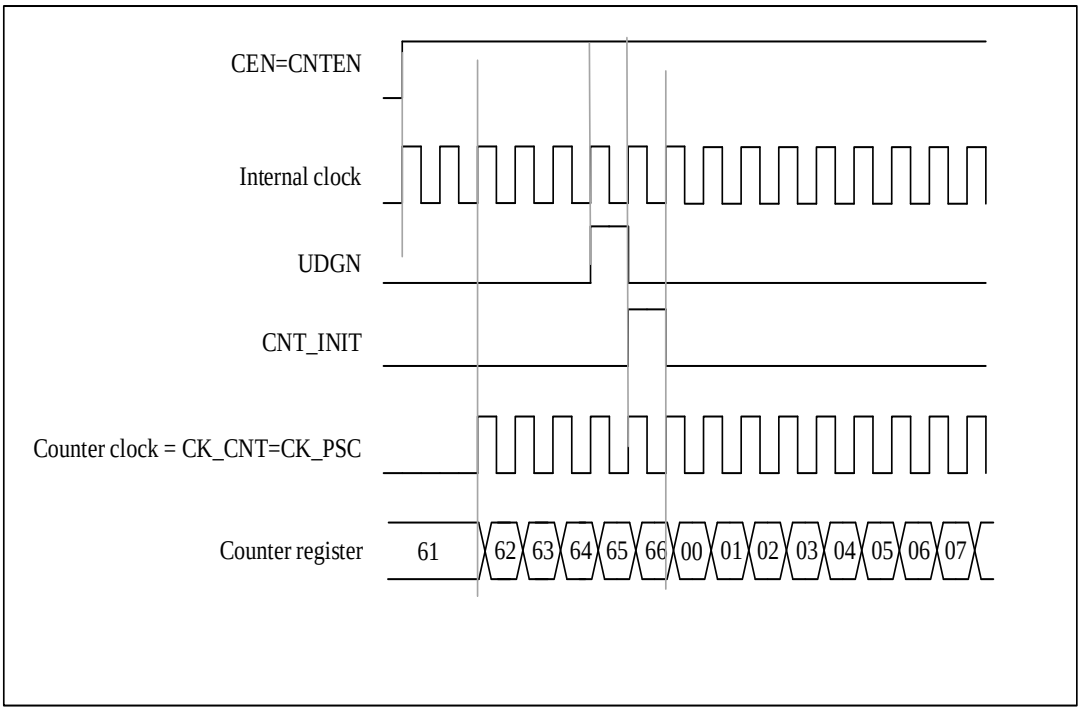
11.3.3 Clock Selection

- The internal clock of timers : CK_INT

11.3.3.1 Internal clock source (CK_INT)

It is provided that the TIMx_CTRL1.CNTEN bit is written as '1' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 11-5 Control Circuit in Normal Mode, Internal Clock Divided by 1



11.3.4 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M0 core halted), depending on the DBG_CTRL.TIM6STP bit configuration in the DBG module, the TIM6 counter can either continue to work normally or stop. For more detailed information, please refer to Section 3.4.9.

11.4 TIMx Register Description (x=6)

For abbreviations used in the registers, please refer to Section 1.1.

These peripheral registers can be operated as half-word (16 bits) or word (32 bits).

11.4.1 Register Overview

Table 11-1 Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																						ARPEN	ONEPM	Reserved		UPDIS	UPRS	Reserved			CNTEN
	Reset Value																							0	0			0	0				0
004h	TIMx_CTRL2	Reserved																MMSEL[3:0]				Reserved											
	Reset Value																	0	0	0	0												

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Email：info@nationstech.com
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008h	TIMx_STS	Reserved															UDITF	Reserved													
	Reset Value																0														
00Ch	TIMx_EVTGEN	Reserved																							UDGN	Reserved					
	Reset Value																								0						
014h	TIMx_DINTEN	Reserved													UDEN	Reserved								UIEN	Reserved						
	Reset Value														0									0							
040h	TIMx_PSC	Reserved																PSC[15:0]													
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	TIMx_AR	Reserved																AR[15:0]													
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
048h	TIMx_CNT	Reserved																CNT[15:0]													
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						ARPEN	ONEPM	Reserved		UPDIS	UPRS	Reserved			CNTEN
						rw	rw			rw	rw				rw

Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit).
7:6	Reserved	Reserved, the reset value must be maintained
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled： – Counter overflow – The TIMx_EVTGEN.UDGN bit is set Shadow registers will update with preload value。 1: Disabled UEV. No update event is generated, and the shadow registers (AR, PSC) keep

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Bit Field	Name	Description
		their values. If the TIMx_EVTGEN.UDGN bit is set, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request： – Counter overflow – The TIMx_EVTGEN.UDGN bit is set 1: If update interrupt or DMA request is enabled, only counter overflow will generate update interrupt or DMA request
3:1	Reserved	Reserved, the reset value must be maintained
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter

11.4.3 Control Register 2 (TIMx_CTRL2)

Offset address：0x04

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved											
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows： x000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. x001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO unless the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit).

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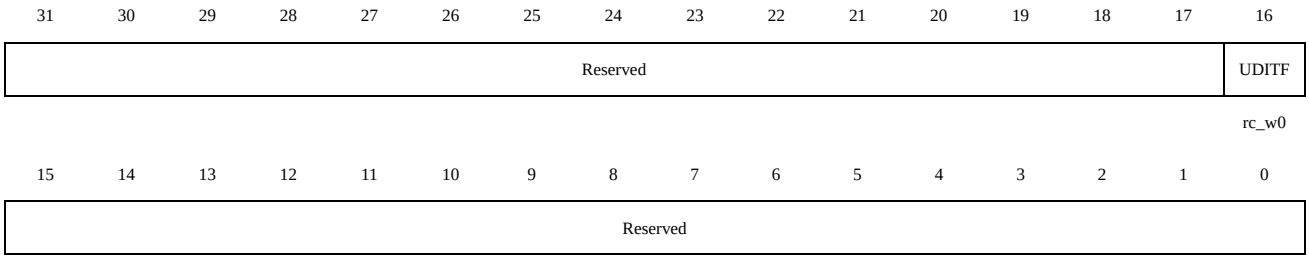
Bit Field	Name	Description
		x010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. other：Reserved.
11:0	Reserved	Reserved, the reset value must be maintained

11.4.4 Status Register (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

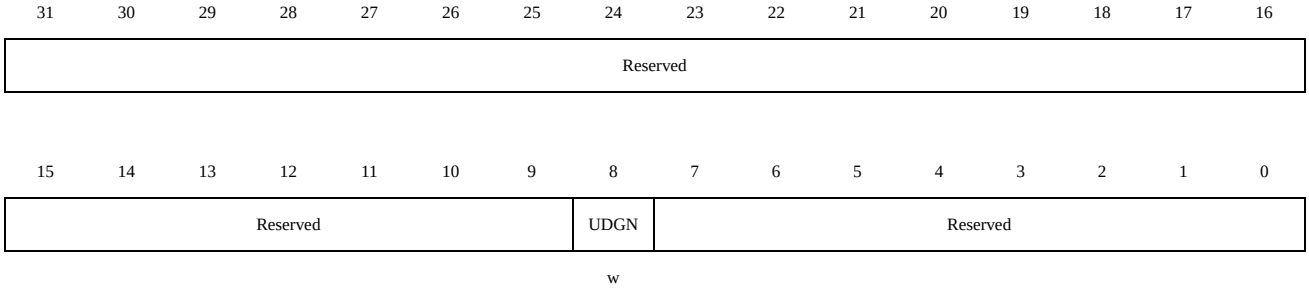


Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and counter value overflow。 –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:0	Reserved	Reserved, the reset value must be maintained

11.4.5 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x0C

Reset value: 0 x0000 0000



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Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	UDGN	Update generation Software can set this bit to update configuration register value and hardware will clear it automatically. 0: No effect. 1: Timer will restart and all shadow register will be updated. It will restart prescaler counter also.
7:0	Reserved	Reserved, the reset value must be maintained.

11.4.6 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												UDEN	Reserved		UIEN
												rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
18:17	Reserved	Reserved, the reset value must be maintained
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enable update interrupt
15:0	Reserved	Reserved, the reset value must be maintained

11.4.7 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															

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rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value PSC register value will be updated to prescaler register at update event. Counter clock frequency is input clock frequency divide PSC + 1.

11.4.8 Automatic Reload Register (TIMx_AR)

Offset address: 0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See 11.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

11.4.9 Counters (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
15:0	CNT[15:0]	Counter value

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12 Independent Watchdog (IWDG)

12.1 Introduction

The N32G05x has embedded independent watchdog (IWDG) and window watchdog (WWDG) timers to solve the problems caused by software errors. The watchdog timer is very flexible to use, which improves the security of the system and the accuracy of timing control.

The independent watchdog (IWDG) is driving by low-speed internal clock (LSI clock) running at 32 KHz, which will still running event dead loop or MCU stuck is happening. This can provide higher safety level, timing accuracy and flexibility of watchdog. It can resolve system malfunctions due to software failure by reset. The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application with relatively low timing accuracy requirements.

When the power control register PWR_CTRL.IWDGRSTEN bit is '1' and the IWDG counter reaches 0, a system reset will be generated (if this bit is '0', the IWDG will count but not reset). IWDG reset can also be used for low power wake up.

Note: This chapter is based on the system default value IWDGRSTEN = 1.

12.2 Main Features

- A 12-bit down-counter that runs independently
- RC oscillator provides an independent clock source and can operate normally in STOP mode and SLEEP mode
- Can match reset and low-power wake-up
- A system reset occurs when the down counter reaches 0x0000 (if watchdog is activated)
- Supports for the counter being frozen

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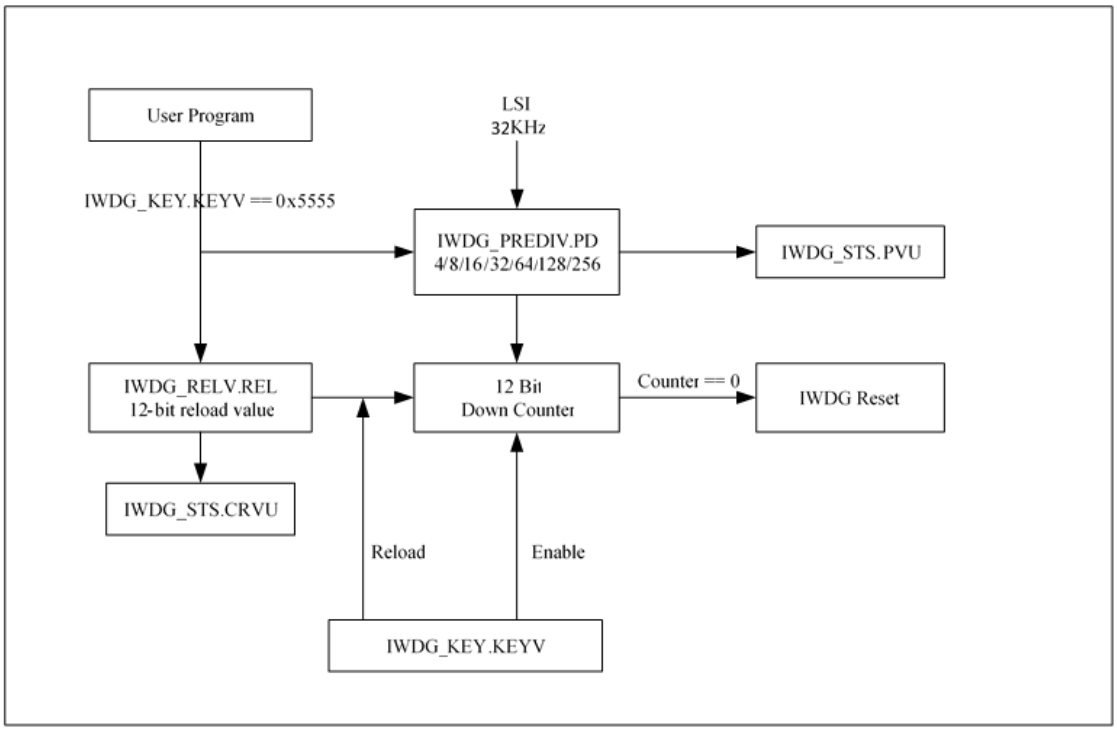
12.3 Function Description

Figure 12-1 Functional Block Diagram of The Independent Watchdog Module



To enable IWDG, we need to write 0xCCCC to IWDG_KEY.KEYV[15:0] bits. Counter starts counting down. When counter count to 0x000, it generates a reset signal (IWDG_RESET) to MCU. Other than that, as long as 0xAAAA (reload request) is written to IWDG_KEY.KEYV[15:0] bits before reset, the counter value is set to the reload value in the IWDG_RELV.REL[11:0] bits and prevents the watchdog from resetting the entire device.

If the hardware watchdog timer function is enabled through the option byte, the watchdog will automatically start running after the system is powered on and will generate a system reset, unless the software reloads the counter before it reaches '0'.

12.3.1 Register Access Protection

IWDG_PREDIV and IWDG_RELV registers are write protection. To modify the value of those two register, user needs to write 0x5555 to IWDG_KEY.KEYV[15:0] bits. Writing other value will enable write protection again. IWDG_STS.PVU indicates whether the pre-scaler value update is on going. IWDG_STS.CRVU indicates whether the IWDG is updating the reload value. The hardware sets the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit when the pre-scaler value and/or reload value is updating. After the pre-scaler value and/or reload value update is complete, the hardware clears the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit.

The reload operation (writing 0xAAAA to IWDG_KEY) will also enable the registers to become write protection again.

12.3.2 Debug Mode

In debug mode (Cortex®-M0 core stops), IWDG counter will either continue to operate normally or stop, depending on DBG_CTRL.IWDG_STOP bit in debug module. If this bit is set to '1', the counter stops. If this bit is set to '0', the counter operate normally. For details, refer to 3.3.2 Peripheral Debugging Support.

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12.3.3 IWDG Freeze

Once IWDG is enabled (no matter by hardware or software), the IWDG will not stop counting unless a system reset is generated or the IWDG is frozen.

To configure the freeze at runtime, write 0x4567 to the IWDG_KEY.KEYV[15:0] bits in RUN mode, and to configure the unfreeze at runtime, write 0x89AB to the IWDG_KEY.KEYV[15:0] bits.

Users can also configure IWDG freeze in SLEEP or STOP mode.

When IWDG is running in RUN mode, write 0xDDDD to the IWDG_FREEZE.FREEZE[15:0] register. When the MCU enters SLEEP or STOP mode, the IWDG will automatically freeze. Write 0xDDDD again to the IWDG_FREEZE.FREEZE[15:0] register to automatically unfreeze the IWDG when entering SLEEP or STOP mode, and the counter resumes operation.

When the IWDG is enabled, it will force the LSI clock to start.

12.4 User Interface

IWDG module user interface contains 4 registers: key register (IWDG_KEY), pre-scale register (IWDG_PREDIV), reload register (IWDG_RELV) and status register (IWDG_STS).

12.4.1 Operating Process

When IWDG is enabled by software (writing 0xAAAA to IWDG_KEY.KEYV[15:0] bits) or hardware (clearing FLASH_OB.WDG_SW bit), it starts counting down from 0xFFF. Down counting gap is determined by pre-scale LSI clock. Once the counter is reloaded, the new round will start from the value in IWDG_RELV.REL[11:0] instead of 0xFFF.

When program is running normally, software needs to feed IWDG before counter reaches 0 and start a new round of down counting. When counter reaches 0, this indicates program malfunction. In this case, IWDG generates a reset signal.

If user wants to configure IWDG pre-scale and reload value register, the user needs to write 0x5555 to IWDG_KEY.KEYV[15:0] first, then confirm IWDG_STS.CRVU bit and IWDG_STS.PVU bit. IWDG_STS.CRVU bit indicates reload value update is ongoing, IWDG_STS.PVU indicates pre-scale value is updating. Only when those two bit are 0 then user can update corresponding value. When update is on-going, hardware sets corresponding bit to 1. At this time, reading IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] is invalid since data needs to be synchronized to LSI clock domain. The value read from IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] will be valid after hardware clears the IWDG_STS.PVU bit or IWDG_STS.CRVU bit.

If the application uses more than one reload value or pre-scaler value, the reload value can only be changed after the IWDG_STS.CRVU bit is reset, and the pre-divider value can only be changed after the IWDG_STS.PVU bit is reset. However, after updating the pre-scaler value and reload value, or only updating the pre-scaler value, or only updating the reload value, there is no need to wait for the IWDG_STS.CRVU bit or IWDG_STS.PVU bit to be reset before continuing to execute the code (even if in low-power mode, write operations will be considered and completed).

Pre-scale register and reload register control the time that generating reset, as shown in Table 12-1.

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Table 12-1 IWDG Counting Maximum and Minimum Reset Time

Pre-Scale Factor	PD[2:0]	Min Timeout (ms) REL [11:0]=0x000	Max Timeout (ms) REL [11:0]=0xFFF
/ 4	000	0.125	512
/ 8	001	0.25	1024
/ 16	010	0.5	2048
/ 32	011	1.0	4096
/ 64	100	2	8192
/ 128	101	4	16384
/ 256	11x	8	32768

12.4.2 IWDG Configuration Process

1. Write 0x5555 to the IWDG_KEY.KEYV[15:0] bits to enable write access to the IWDG_PREDIV and IWDG_RELV registers.
2. Check the IWDG_STS.PVU bit and IWDG_STS.CRVU bit. If they are 0, proceed to the next step.
3. Configure the IWDG_PREDIV.PD[2:0] bits to select the pre-divider value.
4. Configure the IWDG_RELV.REL[11:0] bits for the reload value.
5. Write 0xAAAA to the IWDG_KEY.KEYV[15:0] bits to update the counter with the reload value.
6. Enable the IWDG by writing 0xCCCC to the IWDG_KEY.KEYV[15:0] bits via software or hardware.

If the user wants to change the pre-divider value and reload value, repeat steps 1 to 5. If not, simply feed the watchdog according to step 5.

12.5 IWDG Registers

12.5.1 IWDG Register Overview

Table 12-2 IWDG Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	IWDG_KEY	Reserved																KEYV[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	IWDG_PREDIV	Reserved																												PD[2:0]			
	Reset Value																													0	0	0	
008h	IWDG_RELV	Reserved																REL[11:0]															
	Reset Value																					1	1	1	1	1	1	1	1	1	1	1	1
00Ch	IWDG_STS	Reserved																												LPFRE	RUNF	CRVU	PVU
	Reset Value																													0	0	0	0
010h	IWDG_FREEZE	Reserved																LPFRV[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

12.5.2 IWDG Key Register (IWDG_KEY)

Address offset: 0x00

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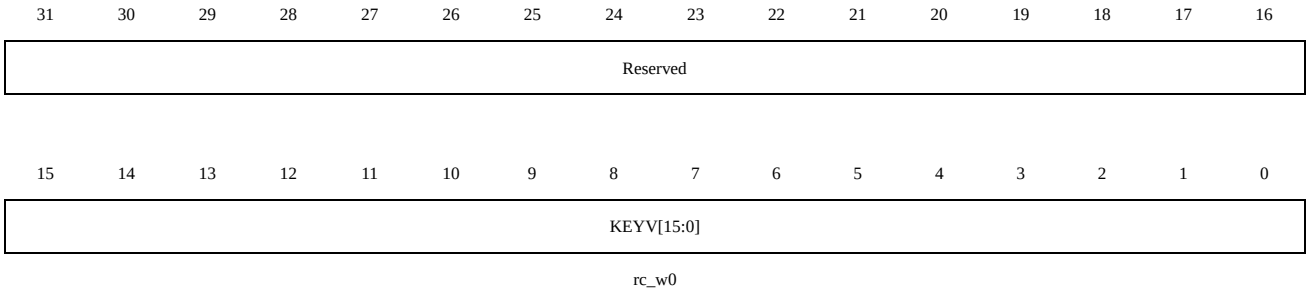
Reset value: 0x00000000

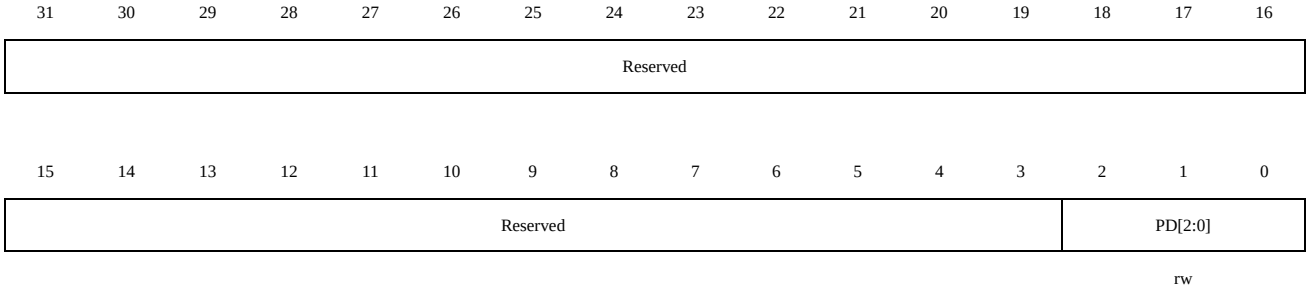


Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	KEYV[15:0]	Key value register: only certain value will serve particular function 0xCCCC: Start watch dog counter, does not have any effect if hardware watchdog is enable, (if hardware watchdog is selected, it is not limited by this command word) 0xAAAA: Reload counter with REL value in IWDG_RELV register to prevent reset. 0x5555: Disable write protection of IWDG_PREDIV and IWDG_RELV register. 0x4567: Freeze IWDG, the IWDG counter will stop in RUN mode. 0x89AB: Unfreeze IWDG, counter resume countering.

12.5.3 IWDG Pre-scaler Register (IWDG_PREDIV)

Address offset: 0x04

Reset value: 0x00000000



Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.

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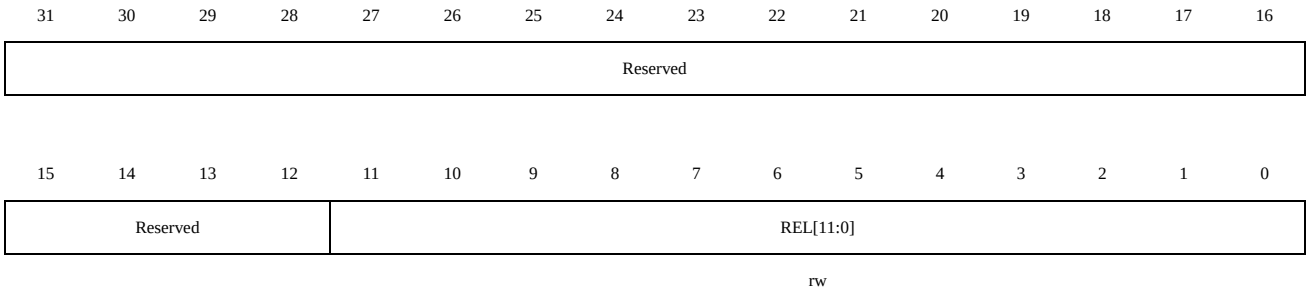
Bit Field	Name	Description
2:0	PD[2:0]	Pre-frequency division factor Pre-scaler divider: with write access protection when IWDG_KEY.KEYV[15:0] is not 0x5555. The IWDG_STS.PVU bit must be 0 otherwise PD [2:0] value cannot be changed. Divide number is as follow: 000: divider /4 001: divider /8 010: divider /16 011: divider /32 100: divider /64 101: divider /128 Other : divider /256 *Note: Reading this register will return the pre-divided value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.PVU bit is '0'.*

12.5.4 IWDG Reload Register (IWDG_RELV)

Address offset: 0x08

Reset value: 0x00000FFF



Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	REL[11:0]	Watchdog counter reload value. These bits have write protection. Defines the reload value of the watchdog counter, which is loaded to the counter every time 0xAAAA is written to IWDG_KEY.KEYV[15:0] bits. The counter then starts to count down from this value. The watchdog timeout period can be calculated from this reloading value and the clock pre-scaler value, refer to Table 12-1. This register can only be modified when the IWDG_STS.CRVU bit is '0'. *Note: Reading this register will return the reload value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.CRVU bit is '0'.*

12.5.5 IWDG Status Register (IWDG_STS)

Address offset: 0x0C

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												LPFREF	RUNFREF	CRVU	PVU
												r	r	r	r

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	LPFREF	IWDG freeze flag in low power mode.
2	RUNFREF	IWDG freeze flag in RUN mode.
1	CRVU	Watchdog reload value update flag: This bit indicates that the reload value is being updated, set by hardware, cleared by hardware. Software can only attempt to change the value of IWDG_RELV.REL[11:0] when the value of IWDG_KEY.KEYV[15:0] is 0x5555 and this bit is 0.
0	PVU	Watchdog pre-scaler value update flag: This bit indicates that the pre-scaler value is being updated, set by hardware, cleared by hardware. Software can only attempt to change the value of IWDG_PREDIV.PD[2:0] when the value of IWDG_KEY.KEYV[15:0] is 0x5555 and this bit is 0.

12.5.6 IWDG Freeze Register (IWDG_FREEZE)

Address offset: 0x10

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPRERV[15:0]															
rc_w0															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	LPRERV	Freeze/Unfreeze IWDG in low power mode 0xDDDD: Enable IWDG freeze when MCU enters SLEEP or STOP mode. Write 0xDDDD again to disable IWDG freeze when MCU enters SLEEP or STOP mode

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13 Window Watchdog (WWDG)

13.1 Introduction

The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock frequency by 4096, and whether the program operation is abnormal is detected through the configuration of the time window. Therefore, WWDG is suitable for precise timing, and is often used to monitor software failures where the application deviates from its normal operation sequence due to external interference or unforeseen logic conditions. A system reset occurs when the WWDG down counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0.

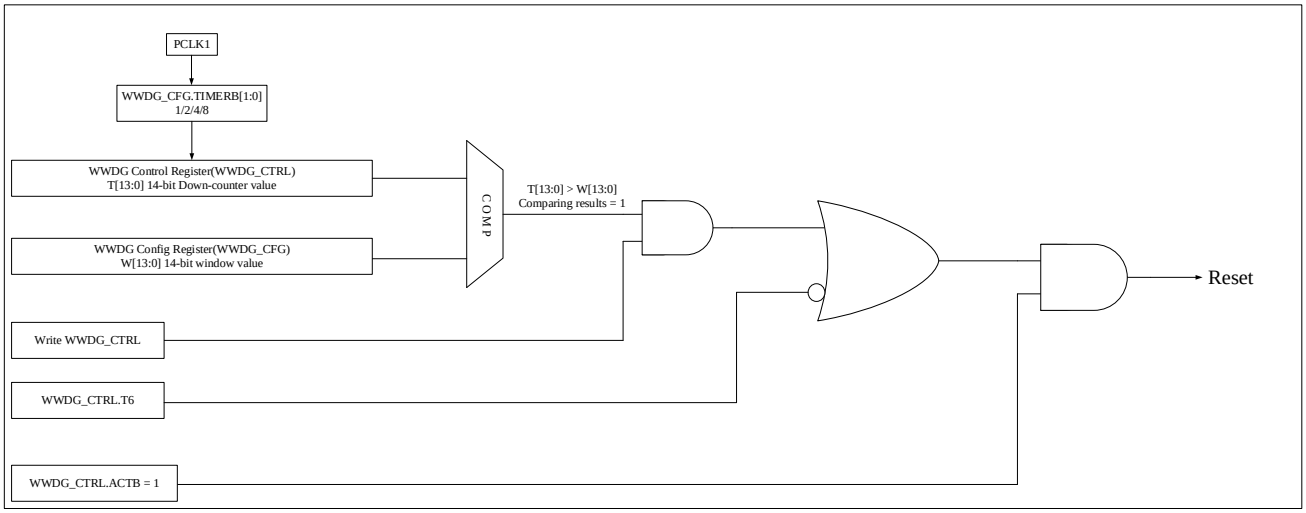
13.2 Main Features

- 14-bit independent running programmable down counter
- After WWDG is enabled, a reset occurs under the following conditions
  - The value of the down counter is less than 0x40.
  - When the down counter value is greater than the value of the window register, it is reloaded.
- Early wake-up interrupt: If the watchdog is started and the interrupt is enabled, wake-up interrupt (WWDG_CFG.EWINT) will be triggered when the count value reaches 0x40.

13.3 Function Description

If the watchdog is activated (the WWDG_CTRL.ACTB), when the 14-bit (WWDG_CTRL.T[13:0]) down-counter reaches 0x3F(WWDG_CTRL.T6 bit is cleared), or the software reloads the counter when the counter value is greater than the value of the window register, a system reset will be generated. In order to avoid system reset, the software must periodically refresh the counter value in the window during normal operation.

Figure 13-1 Watchdog Block Diagram



Set the WWDG_CTRL.ACTB bit to enable the watchdog, and thereafter, the WWDG will remain operating until reset occurs. The 14-bit down-counter runs independently, and the counter keeps counting down whether WWDG is enabled or not. Therefore, it is necessary to set one of the bits in the high 8 bits (WWDG_CTRL.T[13:6]) to 1 to prevent an immediate

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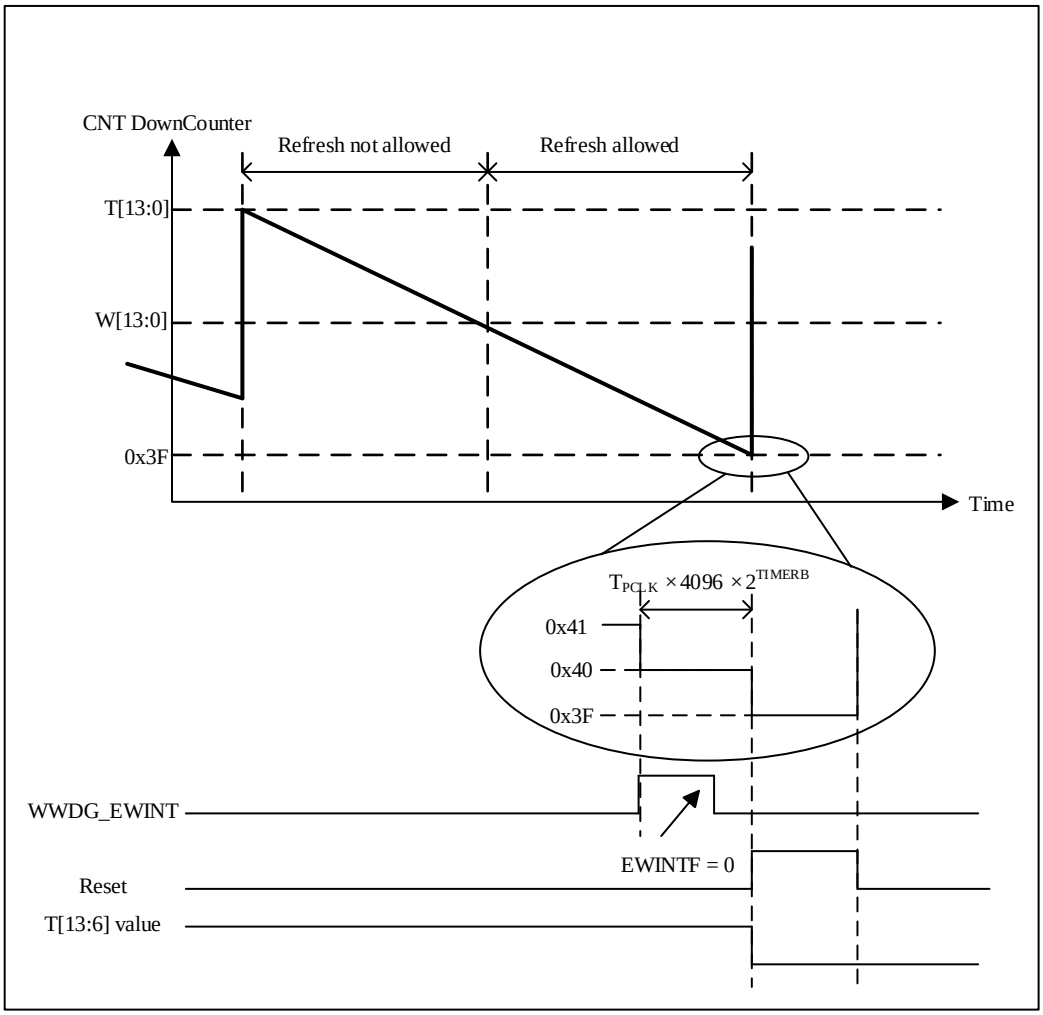
reset after enabling. The pre-scaler value set by the clock APB1 and WWDG_CFG.TIMERB[1:0] bits determines the decrement speed of the counter. WWDG_CFG.W[13:0] bits are used to set the upper limit of the window.

When the down-counter is refreshed before reaching the window register value or after WWDG_CTRL.T6 bit becomes 0, a system reset will be generated. Figure 13-2 describes the operating process of the window register.

Set the WWDG_CFG.EWINT bit to enable early wake-up interrupt. When the count-down counter reaches 0x40, an interrupt will be triggered. You can analyze the cause of software failure or save important data in the corresponding interrupt service routine (ISR), and reload the counter to prevent WWDG from resetting. Write '0' to the WWDG_STS.EWINTF bit to clear the interrupt.

13.4 Timing for Refresh Watchdog and Interrupt Generation

Figure 13-2 Refresh Window and Interrupt Timing of WWDG



Watchdog refreshing window is between WWDG_CFG.W[13:0] value (maximum value 0x3FFF) and 0x3F, refreshing outside this window will generates reset request to MCU. Counter counts down from 0x3FFF to 0x3F using scaled APB1

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clock, the maximum counting time and minimum counting time is shown in Table 13-1 (assuming APB1 clock is 32 MHz)

with calculate equation:

$$T_{WWDG} = T_{PCLK1} \times 4096 \times 2^{TIMERB} \times (T[13:0] - 0X3F + 1)$$

In which:

TWWDG: WWDG timeout

TPCLK1:APB1 clock interval in ms, minimum-maximum timeout value at PCLK1 = 32MHz

Table 13-1 Maximum and Minimum Counting Time of WWDG

TIMERB	Max Timeout Value(ms)	Min Timeout Value(μs)
0	2089	0.128
1	4178	0.256
2	8356	0.512
3	16712	1.024

13.5 Debug Mode

In debug mode (Cortex®-M0 core stops), WWDG counter will either continue to operate normally or stop, depending on DBG_CTRL.WWDG_STOP bit in debug module. If this bit is set to '1', the counter stops. If this bit is set to '0', the counter operate normally. For details, refer to 3.3.2 Peripheral Debug Support.

13.6 User Interface

13.6.1 WWDG Configuration Flow

1. Configure RCC_APB1PCLKEN.WWDGEN[11] bit to enable the clock of WWDG module.
2. Software sets WWDG_CFG.TIMERB[15:14] bits to configure pre-scale factor for WWDG.
3. Software configures WWDG_CTRL.T[13:0] bits and sets starting value of counter. To prevent immediate reset after enabling, one of the bits in the high 8 bits (WWDG_CTRL.T[13:6]) needs to be set to 1.
4. Configure WWDG_CFG.W[13:0] bits to configure upper boundary window value;
5. Set WWDG_CTRL.ACTB[14] bit to enable WWDG;
6. Software operates WWDG_STS.EWINTF[0] bit to clear wake-up interrupt flag;
7. Configure WWDG_CFG.EWINT[16] bit to enable early wake-up interrupt.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

13.7 WWDG Registers

13.7.1 WWDG Register Overview

Table 13-2 WWDG Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	WWDG_CTRL	Reserved																	ACTB	T[13:0]													
	Reset value																		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x04	WWDG_CFG	Reserved															EWINT	TIMERB[1:0]		W[13:0]													
	Reset value																0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x08	WWDG_STS	Reserved																															EWINTF
	Reset value																																0

13.7.2 WWDG Control Register (WWDG_CTRL)

Address offset: 0x00

Reset value: 0x00003FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ACTB	T[13:0]													
	rs	rw													

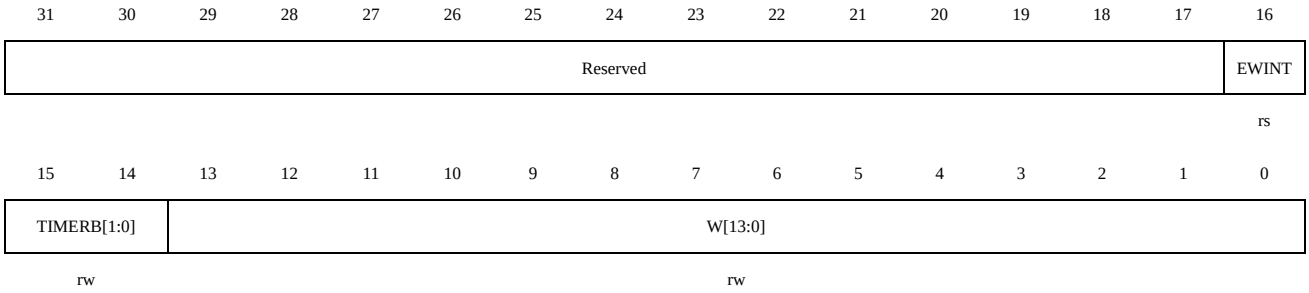
Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	ACTB	Activation bit When ACTB=1, the watchdog can generate a reset. This bit is set by software and only cleared by hardware after a reset. When ACTB = 1, the watchdog can generate a reset. 0: Disable watchdog 1: Enable watchdog
13:0	T[13:0]	These bits contain the value of the watchdog counter. It is decremented every ($4096x2^{TIMERB}$) PCLK1 cycles. A reset is produced when it rolls over from 0x40 to 0x3F (T6 becomes cleared).

13.7.3 WWDG Config Register (WWDG_CFG)

Address offset: 0x04

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Reset value: 0x00003FFF

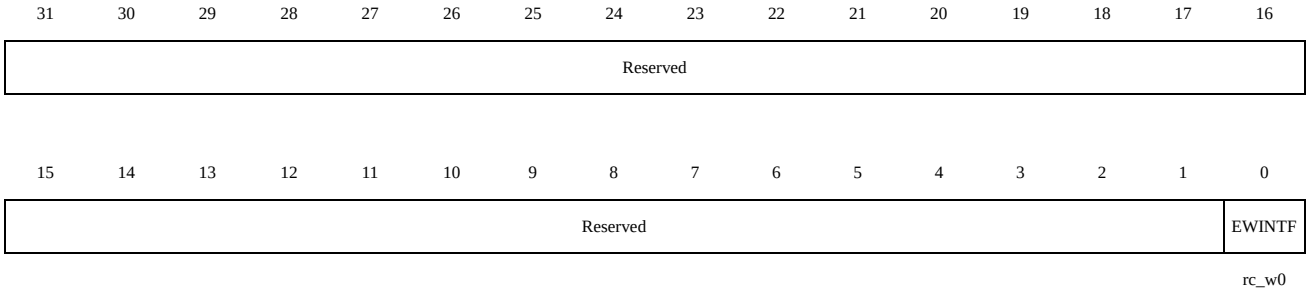


Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	EWINT	Early wake-up interrupt When this bit is set, an interrupt occurs whenever the counter reaches the value 0x40. This interrupt is only cleared by hardware after a reset.
15:14	TIMERB[1:0]	Timer base. The time base of the pre-scaler can be modified as follows: 00: CK Counter Clock (PCLK1 div 4096) div 1 01: CK Counter Clock (PCLK1 div 4096) div 2 10: CK Counter Clock (PCLK1 div 4096) div 4 11: CK Counter Clock (PCLK1 div 4096) div 8
13:0	W[13:0]	14-bit window value These bits contain the window value to be compared to the down counter.

13.7.4 WWDG Status Register (WWDG_STS)

Address offset: 0x08

Reset value: 0x00000000



Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EWINTF	Early wake-up interrupt flag This bit is set by hardware when the counter has reached the value 0x40. It must be cleared by software by writing ‘0’. A write of ‘1’ has no effect. This bit is also set if the interrupt is not enabled.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

14 Analog to Digital Conversion (ADC)

14.1 Introduction

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. It can measure 17 channel signal sources. It has 15 external and 2 internal channels. Each channel of the A/D conversion performed in single, continuous or scan mode. ADC measurements are stored (left-aligned/ right-aligned) in 16-bit data registers. The application detects the input voltage within user-defined high/low thresholds by analog watchdog and the maximum frequency of the input clock to the ADC is 24MHz.

14.2 Main Features

- Supports 1 ADC, supports single-ended inputs, and can measure 15 external and 2 internal sources
- Supports 12-bit resolution with a maximum sampling rate of 1MSPS
- ADC clock source is divided into working clock source and timing clock source
  - HSI/PLL/AHB as the ADC_CLK working clock source with a maximum frequency of 24MHz.
  - HSI/HSE as the ADC_1MCLK timing clock source for internal timing functions, and the frequency must be configured to 1MHz.
- Supports timer trigger ADC sampling
- Interrupts at the end of conversion, and simulated watchdog events
- Support 2 conversion modes
  - Single conversion
  - Continuous conversion
- Scan mode supports up to any 5 channels, and each channel has an independent result data register buffer
- All channel sampling intervals can be programmed uniformly
- Regular conversion has external triggering options
- ADC power supply requirements: 2.4V to 5.5V
- ADC input range: $0 \leq V_{IN} \leq V_{DD}$

14.3 Function Description

Below is a block diagram of an ADC module. Table 14-1 shows the description of ADC pins.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Figure 14-1 Block Diagram of ADC

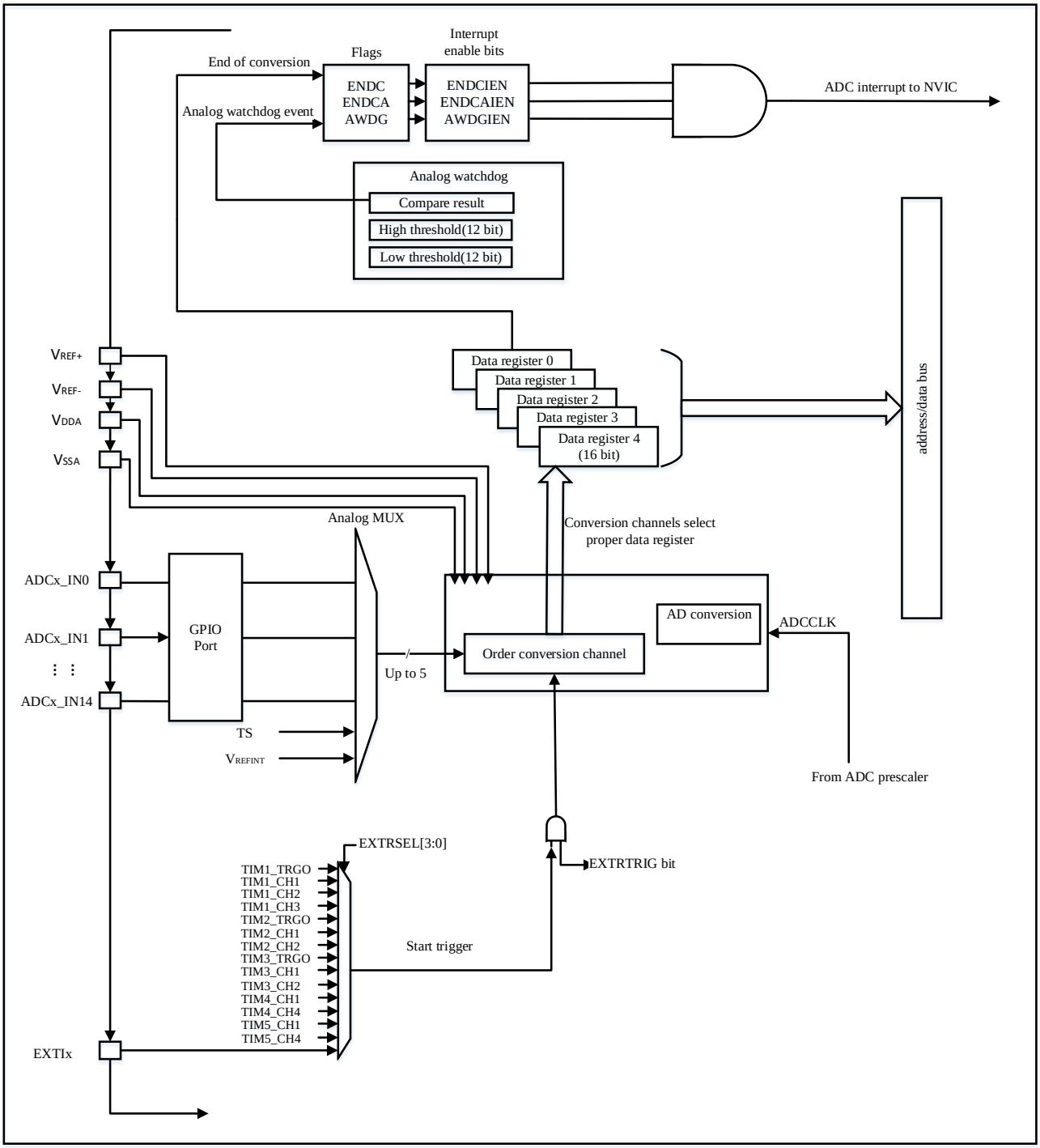


Table 14-1 ADC Pins

Name	Signal Types	Annotations
V_{REF+}	Input, positive reference voltage used by the ADC, 2.4V ≤ V_{REF+} ≤ V_{DDA} (5.5V)	Positive reference voltage
V_{DDA}	Input, analog power supply	Equivalent to V_{DD} analog power supply and: 2V ≤ V_{DD} ≤ 5.5 V
V_{SSA}	Input, analog power supply ground	Equivalent to V_{SS} analog power supply ground
ADCx_IN[14:0]	Analog input signal	15 analog external input channels

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

14.3.1 ADC Clock

An ADC requires three clocks, ADC_CLK, HCLK, and ADC_1MCLK.

- HCLK is used for the register access.
- ADC_CLK is the working clock of ADC.
- ADC_1MCLK is used for internal timing function, configured in RCC, and its frequency must be configured to 1M

Note:

(1) The ADC_CLK frequency division factor can be configured with maximum frequency of 24MHz. The ADC_CLK frequency division factor can be 1,2,3,4,6,8,10,12,24,32, 64, 128, 256.

14.3.2 ADC Switch Control

User can proceed to the next step only after the power-up process is complete by polling the ADC_CTRL3.RDY bit.

User can set the ADC_CTRL2.ON bit to turn on the ADC. When the ADC_CTRL2.ON bit is set for the first time, it wakes up the ADC from the power-off state. After a power-on delay of ADC (tSTAB), the conversion begins when the ADC_CTRL2.ON bit is set again.

The conversion can be stopped by clearing the ADC_CTRL2.ON bit and placing the ADC in power-off mode. In this mode, the ADC consumes almost no power consumption (just a few μA). Power-down state of ADC can be checked by polling the ADC_CTRL3.PDRDY bit.

When the ADC is disabled, the default mode is power-down.

14.3.3 Channel Selection

Each channel can be configured as a regular sequence. A series of conversions can be performed in any order on any number of channels. For example, the conversion can be completed in the following order: channel 3, channel 8, channel 2, channel 1, channel 0.

The regular sequence consists of multiple conversions, up to a maximum of 5. The ADC_DATx.SEQx[4:0] bits specify the regular channels and their conversion sequence. The ADC_CTRL2.LEN[2:0] bits specify the regular channel sequence length.

Note: During conversion, changes to the ADC_DATx.SEQx[4:0] are prohibited; the ADC_DATx.SEQx[4:0] bits can only be changed when the ADC is idle.

14.3.4 Internal Channel

- The temperature sensor connects to channel ADC_IN15

The VREFINT is connected with channel ADC_IN16. ADC Internal channels can be converted by regular channels.

14.3.5 Single Conversion Mode

The ADC can enter the single conversion mode by configuring ADC_CTRL2.CTU to 0. In this mode, external triggering (for regular channels only) or setting ADC_CTRL2.ON=1 (for regular channels only) can start the ADC to start conversion, and the ADC only performs signleconversion.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of conversion flag (ADC_STS.ENDC) will be set to 1. If the regular channel end of conversion interrupt enable (ADC_CTRL1.ENDCIEN) bit is set to 1, an interrupt will be generated, and the converted data will be stored in the ADC_DATx.DAT[15:0] register.

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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After single conversion, the ADC stops.

14.3.6 Continuous Conversion Mode

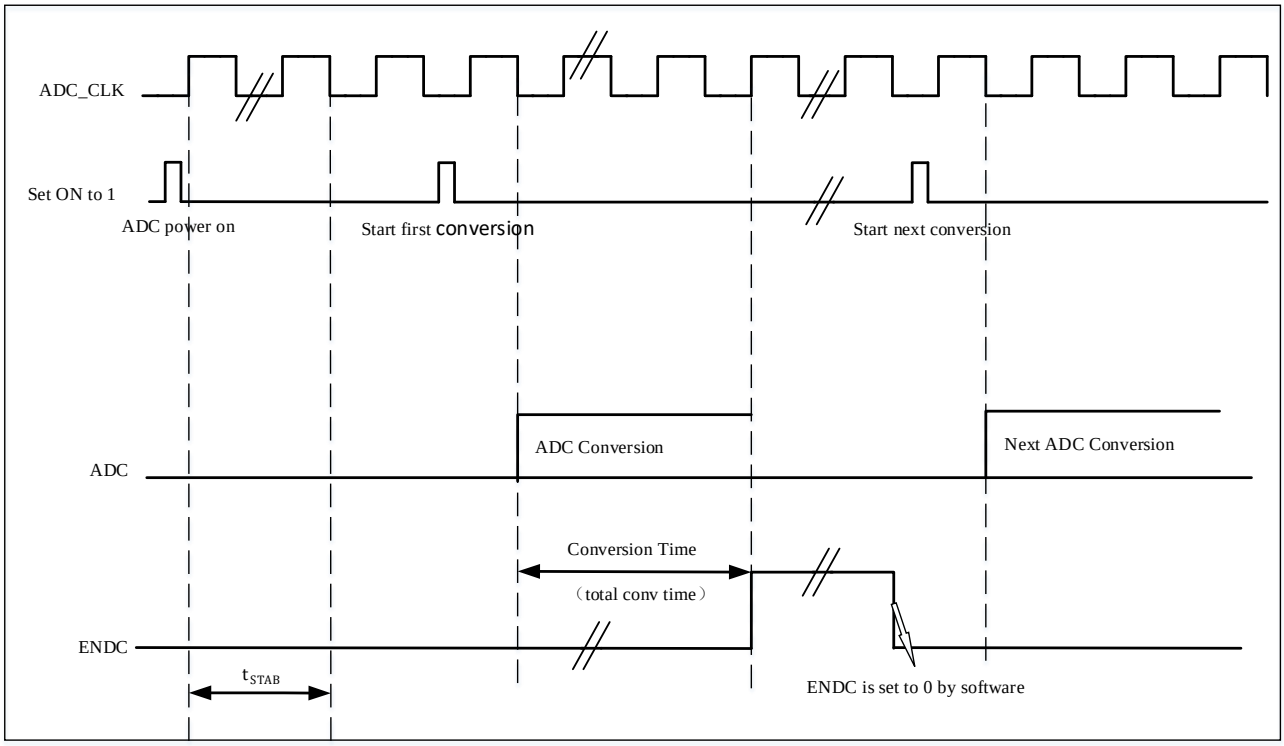
The ADC can enter the continuous conversion mode by configuring ADC_CTRL2.CTU to 1. In this mode, external triggering or setting ADC_CTRL2.ON to 1 can start the ADC conversion, and the ADC will continuously convert the selected channels.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of conversion flag (ADC_STS.ENDC) will be set to 1. If the regular channel end of conversion interrupt enable bit (ADC_CTRL1.ENDCIEN) is set to 1, an interrupt will be generated. The converted data will be stored in the ADC_DATx.DAT[15:0] register.

14.3.7 Timing Diagram

When ADC_CTRL2.ON is set to 1 for the first time, the ADC is powered on. After the ADC is powered on, the ADC needs a certain time(tSTAB) to ensure its stability. After the ADC is stabilized, ADC_CTRL2.ON is set to 1. At this time, set ADC_CTRL2.ON to 1 again through software to start the conversion. After 24 cycles, the end of conversion flag will be set to 1 after the conversion is completed.

Figure 14-2 Timing Diagram



14.3.8 Analog Watchdog

The analog watchdog can be enabled on the regular channel by setting ADC_CTRL1.AWDGERCH to 1. The high threshold of the analog watchdog can be set by configuring ADC_WDGHIGH.HTH[11:0], and the low threshold of the analog watchdog can be set by configuring ADC_WDGLOW.LTH[11:0]. The threshold of the analog watchdog independent of data alignment, because the comparison of the ADCs conversion value with the threshold is done before the alignment. When the value of ADC analog conversion is higher than the high threshold of the analog watchdog or lower than the low threshold of the analog watchdog, the analog watchdog flag (ADC_STS.AWDG) will be set to 1. If

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

ADC_CTRL1.AWDGIEN has been configured to 1, an interrupt will be generated at this time. The analog watchdog can be controlled for one or more channels by configuring ADC_CTRL1.AWDSGSGLEN and ADC_CTRL1.AWDGCH[4:0].

Table 14-2 Analog Watchdog Channel Selection

Channel	ADC_CTRL1 Register Control Bit	
	AWDGSGLEN	AWDGERCH
All regular channels	0	1
Single regular channel	1	1

14.3.9 Scan Mode

By configuring ADC_CTRL2.SCAMD to 1, the scan mode can be turned on, and the ADC will scan and convert all the channels selected in ADC_DATx.SEQx[4:0]. Each sequence can select any channel for conversion. After the conversion is started, the channels will be converted sequentially one by one, supporting up to 5 conversion sequences. If ADC_CTRL2.CTU is 1 at this time, the conversion will be restarted from the first channel of the conversion sequence after the conversion of all selected channels is completed.

14.4 Data Aligned

There are two alignment methods for data storage after conversion: left-aligned and right-aligned. The alignment can be set by the ADC_CTRL2.ALIG bit. ADC_CTRL2.ALIG = 0 is right-aligned, while ADC_CTRL2.ALIG = 1 is left-aligned, as shown in following tables.

Table 14-3 Right-align Data

0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 14-4 Left-aligne Data

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

14.5 Programmable Channel Sampling Time

Specify the number of sampling cycles of ADC in ADC_SAMPT.SAMP[4:0], and then the ADC samples the input voltage in the specified sampling cycle. For different channels, sampling intervals can be programmed uniformly. The total conversion time is calculated as follows:

$$T_{CONV} = \text{Sampling time} + 12 \text{ cycles}$$

Note: An additional 2 cycles are required for the first conversion in continuous conversion mode and for each conversion in single conversion mode.

Example:

With ADCCLK=24MHz, the sampling time is 12 cycles and resolution is 12bit, the total conversion time is "12 + 12" ADCCLK Cycles, that is:

$$T_{CONV} = 12 + 12 = 24 \text{ cycle} = 1\mu s$$

Note: All ADC channels share a channel sample time configuration.

Nations Technologies Inc.
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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14.6 Externally Triggered Conversion

For the regular sequence, software sets the ADC_CTRL2.EXTRTRIG bit to 1, then the regular channel can use the rising edge of the external event to trigger the start conversion, and then the software sets the ADC_CTRL2.EXTRSEL[3:0] bits to select the external trigger source of the regular sequence. The external trigger source selection is shown in the table below. User can start the regular channel conversion by setting ADC_CTRL2.SWSTRRCH to 1 if SWSTRRCH is seleted as the external trigger source.

Table 14-5 ADC is Used for External Triggering of Regular Channels

EXTRSEL[3:0]	Trigger Source	Type
0000	TIM1_TRGO event	Internal signal from the on-chip timer
0001	TIM1_CC1 event	
0010	TIM1_CC2 event	
0011	TIM1_CC3 event	
0100	TIM2_TRGO event	
0101	TIM2_CC1 event	
0110	TIM2_CC2 event	
0111	TIM3_TRGO event	
1000	TIM3_CC1 event	
1001	TIM3_CC2 event	
1010	TIM4_CC1 event	
1011	TIM4_CC4 event	
1100	TIM5_CC1 event	
1101	TIM5_CC4 event	
1110	EXTI line 0~15 event	External pin/internal signal from on-chip timer
1111	SWSTRRCH	Software control bit

14.7 DMA Requests

In order to avoid losing the results of regular channel conversions stored in the ADC_DAT register due to excessive data during multiple regular channel conversions, you can set the ADC_CTRL2.ENDMA bit to 1 to use the DMA. When the ADC regular channel conversion ends, a DMA request is generated. After receiving the request, the DMA will transfer the converted data from the ADC_DATx register to the destination address specified by the user.

14.8 Temperature Sensor

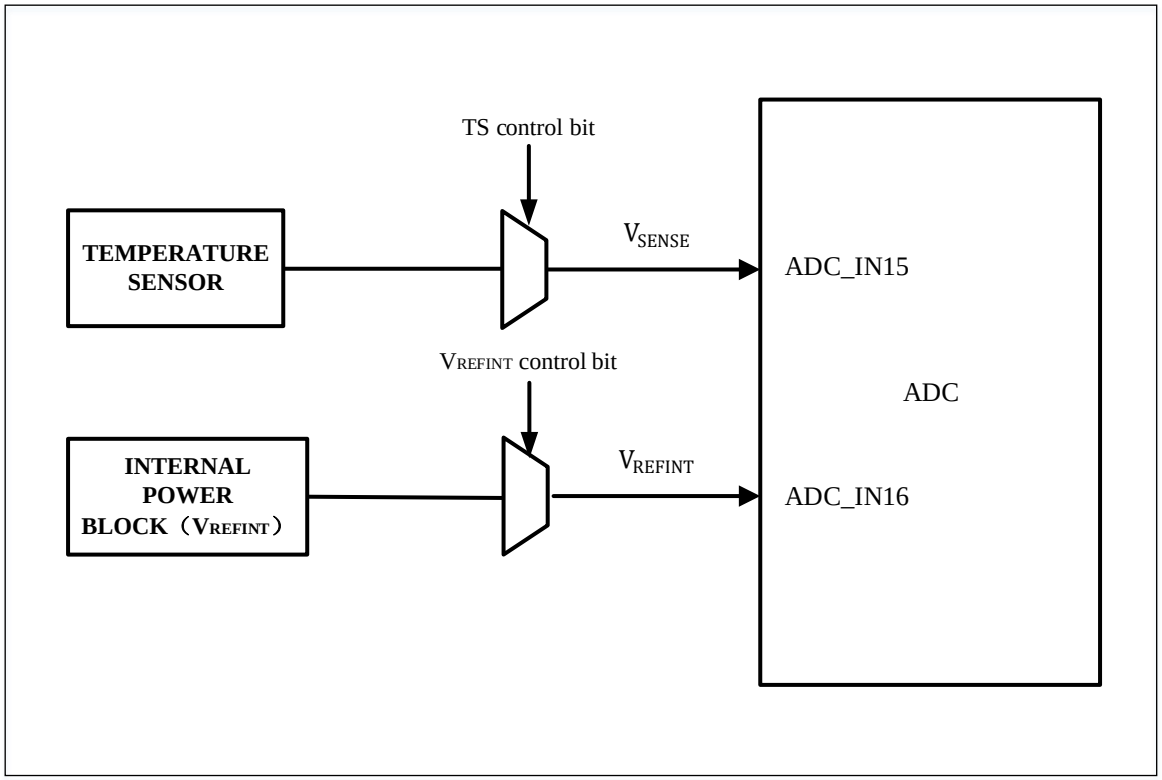
Set the ADC_CTRL2.TEMPEN bit to 1, enable the temperature sensor, and use the temperature sensor to detect the ambient temperature when the device is operating. The output voltage sampled by the temperature sensor is converted to a digital value by the ADC_IN15 channel. When the temperature sensor is operating, the recommended sampling time is 17.1us; when the temperature sensor is not operating, the ADC_CTRL2.TEMPEN bit can be cleared by software to turn off the temperature sensor to reduce power consumption. Figure 14-3 is a block diagram of a temperature sensor.

The output voltage of the temperature sensor changes linearly with temperature. Different chips will have different offsets in the temperature curve due to different production processes. Through testing, it is found that the maximum offset is 3℃. This characteristic makes the internal temperature sensor more suitable for detecting temperature changes, rather than for

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

measuring absolute temperature. When accurate temperature measurement is required, an external temperature sensor should be used.

Figure 14-3 Temperature Sensor and V_{REFINT} Diagram of The Channel



14.8.1 Temperature Sensor Using Flow

1) Configure the channel (ADC_IN15) and sampling time as 17.1us
2) Set ADC_CTRL2.TEMPEN bit to 1 to enable temperature sensor
3) Set ADC_CTRL2.ON bit to 1 to start ADC conversion (or through external trigger)
4) Read the temperature data in the ADC data register, and calculate the temperature value by the following formula:

$$\text{Temperature (℃)} = \{(V_{SENSE} - V_{Temperature}) / \text{Avg_Slope}\} + \text{Temperature} - \text{Toffset}$$

In which:

$V_{Temperature}$ = V_{SENSE} at Temperature

Toffset = 0 ℃, it represents the empirical value of temperature error compensation (in ℃)

Temperature is the calibrated temperatureAvg_Slope = temperature and V_{SENSE} average slope of a curve (mV/ ℃ or μV/°C)

Refer to the values of Avg_Slope in the electrical characteristics chapter of the datasheet.

Note: There is a settling time before the sensor wakes up from the power-off mode to the correct output of V_{SENSE}; there is also a settling time after the ADC is powered on, so in order to shorten the delay, the ADC_CTRL2.TEMPEN and ADC_CTRL2.ON bits should be set at the same time.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

14.9 ADC Interrupt

ADC interrupts can be triggered by an end of regular sequence conversion, an analog watchdog event when input voltage exceeds the threshold, any end of regular channel conversion. These interrupts have independent interrupt enable bits.

There is 1 status flag in the ADC_STS register: regular sequence channel conversion started (STR). But there is no interrupt associated with this flag in the ADC.

Table 14-6 **ADC Interrupt**

Interrupt Event	Event Flags	Enable Control Bit
Regular sequence is complete	ENDC	ENDCIEN
Exceeding the analog watchdog threshold	AWDG	AWDGIEN
Any regular channel interruption is enabled	ENDCA	ENDCAIEN

14.10 ADC Registers

14.10.1 ADC Register Overview

Table 14-7 ADC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	ADC_STS	Reserved																												ENDCA	STR	ENDC	AWDG
	Reset Value																													0	0	0	0
004h	ADC_CTRL1	Reserved																					REFSEL		AWDGEN	AWDGSGLEN	AWDGIEN	ENDCIEN	AWDGCH[4:0]				
	Reset Value																						0		0	0	0	0	0	0	0	0	0
008h	ADC_CTRL2	Reserved																	TEMPEN	ENDMA	COV_MODE	LEN[2:0]			SWSTART	EXTRTRIG	EXTRSEL[3:0]			ALIG	CONT	ON	
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	ADC_CTRL3	Reserved																										ENDCAIEN	PDRDY	RDY	BUF_READY	BUF_EN	Reserved
	Reset Value																											0	1	0	0	0	
010h	ADC_SAMP	Reserved																											SAMP[4:0]				
	Reset Value																												0	0	0	0	0
014h	ADC_WDGHIGH	Reserved																			HTH[11:0]												
	Reset Value																				1	1	1	1	1	1	1	1	1	1	1	1	1
018h	ADC_WDGLOW	Reserved																			LTH[11:0]												
	Reset Value																				0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	ADC_DAT0	Reserved											SEQ0[20:16]					DAT0[15:0]															
	Reset Value												0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	ADC_DAT1	Reserved											SEQ1[20:16]					DAT1[15:0]															
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	ADC_DAT2	Reserved											SEQ2[20:16]					DAT2[15:0]															
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	ADC_DAT3	Reserved											SEQ3[20:16]					DAT3[15:0]															
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	ADC_DAT4	Reserved											SEQ4[20:16]					DAT4[15:0]															
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

14.10.2 ADC Status Register (ADC_STS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												ENDCA	STR	ENDC	AWDG
												rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3	ENDCA	Any channel End of conversion Flag This bit is set by hardware at the end of regular channel conversion and cleared by software. 0: The conversion is not complete; 1: The conversion is complete.
2	STR	Regular channel start flag This bit is set by hardware at the start of regular channel conversion and cleared by software. 0: Regular channel conversion has not started. 1: Regular channel conversion has started.
1	ENDC	End of conversion This bit is set by hardware at the end of channel sequence conversion and cleared by software 0: the conversion is not complete. 1: The conversion is complete.
0	AWDG	Analog watchdog flag This bit is set by hardware and cleared by software when converted voltage values are outside the range defined by the ADC_WDGHIGH.HTH and ADC_WDGLOW.LTH registers. 0: No analog watchdog event occurs; 1: The analog watchdog event occurs.

14.10.3 ADC Control Register 1 (ADC_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					REFSEL	Reserved	AWDG ERCH	AWDG SGLEN	AWD GIEN	END CIEN	AWDGCH[3:0]				

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

rw rw rw rw rw rw

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	REFSEL	ADC reference source selection 0: Reference source is external V_{DDA} 1: Reference source is internal V_{REF+}.
9	Reserved	Reserved, the reset value must be maintained
8	AWDGERCH	Analog watchdog enable on regular channels This bit is set and cleared by the software. 0: Disables analog watchdog on regular channel. 1: Use analog watchdog on regular channels.
7	AWDGSGLEN	Enable the watchdog on a single channel in scan mode This bit is set and cleared by software to enable or disable analog watchdog functions on channels specified by ADC_CTRL1.AWDGCH[4:0] 0: Use watchdog on all channels. 1: Use watchdog on single channel.
6	AWDGIEN	Analog watchdog interrupt enable This bit is set and cleared by software to disallow or allow interrupt generated by analog watchdog. In scan mode, if the watchdog detects an out-of-range value, the scan is aborted only when that bit is set. 0: Disable analog watchdog interruption. 1: Enable analog watchdog interruption.
5	ENDCIEN	Interrupt enable for any channels This bit is set and cleared by the software to disallow or allow interrupts to occur after the regular channel conversion ends. 0: Disable ENDC interruption. 1: Enable ENDC interruption.
4:0	AWDGCH[4:0]	Analog watchdog channel select bits These bits are set and cleared by software. They select the input channel to be guarded by the analog watchdog. 00000: ADC analog input channel 0 00001: ADC analog input channel 1 ... 10001: ADC analog input channel 16 Reserved all other values.

14.10.4 ADC Control Register 2 (ADC_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TEMPEN	ENDMA	SCANMD	LEN[2:0]			SWSTRRCH	EXTRTRIG	EXTRSEL[3:0]				ALIG	CTU	ON
	rw	rw	rw	rw			rw	rw	rw				rw	rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
14	TEMPEN	Temperature sensor enable This bit is set and cleared by the software to enable or disable the temperature sensor channel. 0: Disables the temperature sensor. 1: Enable the temperature sensor.
13	ENDMA	Direct memory access mode This bit is set and cleared by the software. See the DMA Controller chapter for details. 0: Do not use DMA mode. 1: Use DMA mode.
12	SCANMD	Scan mode This bit is set and cleared by the software to enable or disable scan mode. In scan mode, the conversion is made by ADC_DATx.ADC_SEQx[4:0] register. 0: Disable scan mode. 1: Enable scan mode. *Note: if the ADC_CTRL1.ENDCIEN bits are set separately, ADC_STS.ENDC interrupts occur only after the last channel has been converted.*
11:9	LEN[2:0]	Regular channel sequence length These bits are written by software to define the total number of conversions in the channel conversion sequence. 000: 1 conversion 001: 2 conversions 010: 3 conversions 011: 4 conversions 100: 5 conversions
8	SWSTRRCH	Start conversion of regular channels This bit is set by software to start conversion and cleared by hardware as soon as conversion starts. It starts the conversion of a group of regular channels if SWSTRRCH is elected as trigger event by the ADC_CTRL2.EXTRSEL[3:0] bits. 0: Reset state 1: Starts conversion of regular channels
7	EXTRTRIG	External trigger conversion mode for regular channels This bit is set and cleared by software to enable or disable external triggering events that can initiate regular channel group conversion. 0: Start conversion without external events; 1: Use an external event to start the conversion.
6:3	EXTRSEL[3:0]	External event select for regular sequence

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Bit Field	Name	Description
		These bits select external events to start the regular sequence conversion The triggering configuration of ADC is as follows: 0000: Timer 1 TRGO event 0001: Timer 1 CC1 event 0010: Timer 1 CC2 event 0011: Timer 1 CC3 event 0100: Timer 2 TRGO event 0101: Timer 2 CC1 event 0110: Timer 2 CC2 event 0111: Timer 3 TRGO event 1000: Timer 3 CC1 event 1001: Timer 3 CC2 event 1010: Timer 4 CC1 event 1011: Timer 4 CC4 event 1100: Timer 5 CC1 event 1101: Timer 5 CC4 event 1110: EXTI line 1111: SWSTRRCH
2	ALIG	Data alignment This bit is set and cleared by the software. 0: Right-aligned; 1: Left-aligned.
1	CTU	Continuous conversion This bit is set and cleared by the software.If this bit is set, the conversion continues until the bit is cleared. 0: Single conversion mode. 1: Continuous conversion mode.
0	ON	A/D Converter ON/OFF This bit is set and cleared by the software.When the bit is' 0 ', writing '1' will wake the ADC from power-off mode. When the bit is '1', writing '1' starts the conversion.The application should note that there is a delay t_{STAB} between the converter is powered on and the conversion begins, refer to Figure 14-2. 0: Close ADC conversion/calibration and enter power off mode; 1: Start ADC and start conversion. *Note: if there are other bits changed in this register along with ON, the conversion will not be triggered. This is to prevent the wrong conversion from being triggered.*

14.10.5 ADC Control Register 3 (ADC_CTRL3)

Address offset: 0x0C

Reset value: 0x0000 0040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										ENDCAIEN	PDRDY	RDY	VREFRDY	VREFEN	Reserved
										rw	r	r	r	rw	

Bit Field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained.
5	ENDCAIEN	Interrupt enable for any channels This bit is set and cleared by the software to enable/disable channel conversion to end the interrupt 0: ADC_STS.ENDCA interrupt is disabled 1: ADC_STS.ENDCA interrupt is enabled
4	PDRDY	ADC power down ready 0: ADC is powered on 1: ADC is powered down
3	RDY	ADC ready 0: Not ready 1: Get ready
2	VREFRDY	VREFINT ready ADC internal input buffer ready status, software must check this status bit before measuring VREFINT 0: VREFINT not ready 1: VREFINT is ready
1	VREFEN	VREFINT enable ADC internal input buffer is enabled, software must enable this bit before measuring VREFINT 0: Disable VREFINT measurement 1: Enable VREFINT measurement
0	Reserved	Reserved,the reset value must be maintained.

14.10.6 ADC Sampling Time Register (ADC_SAMPT)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											SAMP[4:0]				
											rw				

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Email：info@nationstech.com
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Bit Field	Name	Description
31:5	Reserved	Reserved,the reset value must be maintained.
4:0	SAMP[4:0]	Channel sample time selection These bits are written by software to select the sample time for channel. During sample cycles channel selection bits must remain unchanged. 00000: 6 cycles (only set for working clock of 24MHz,the frequency of HSI is 24MHz) 00001: 8 cycles 00010: 12 cycles 00011: 14 cycles 00100: 20 cycles 00101: 26 cycles 00110: 30 cycles 00111: 42 cycles 01000: 56 cycles 01001: 72 cycles 01010: 88 cycles 01011: 120 cycles 01100: 182 cycles 01101: 240 cycles 01110: 380 cycles 01111: 760 cycles 10000: 1520 cycles 10001: 3040 cycles

14.10.7 ADC Watchdog High Threshold Register (ADC_WDGHIGH)

Address offset: 0x14

Reset value: 0x0000 0FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HTH[11:0]											
				rw											

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	HTH[11:0]	Analog watchdog high threshold These bits define the high threshold for analog watchdog.

14.10.8 ADC Watchdog Low Threshold Register (ADC_WDGLOW)

Address offset: 0x18

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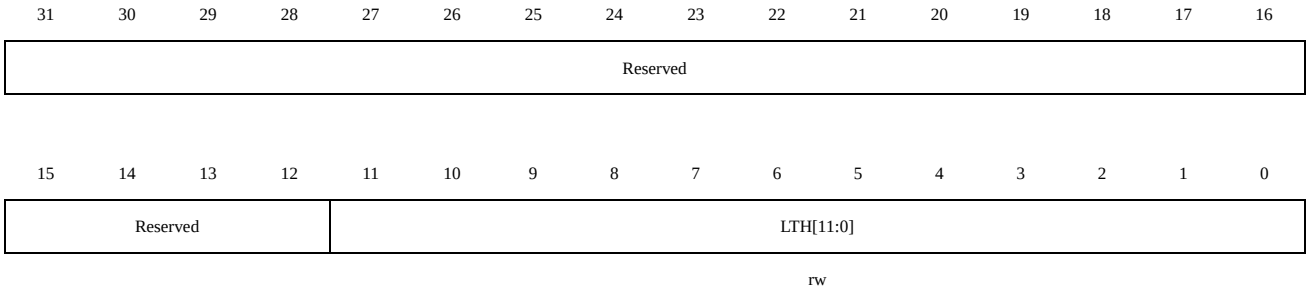
Reset value: 0x0000 0000

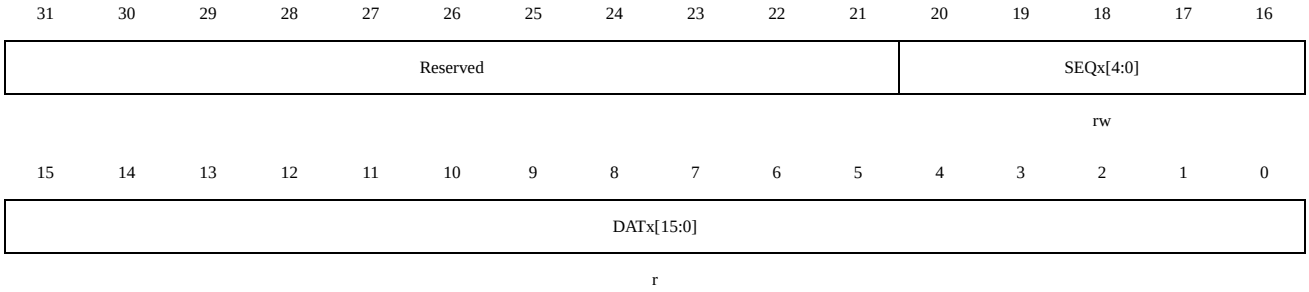


Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	LTH[11:0]	Analog watchdog low threshold These bits define the low threshold low threshold for analog watchdog.

14.10.9 ADC Regular Data Register x (ADC_DATx) (x= 0..4)

Address offset: 0x01C – 0x2C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:21	Reserved	Reserved,the reset value must be maintained.
20:16	SEQx[4:0]	Conversion channel of selecting proper data register 00000: channel 0 … 10000: channel 16 Others: reserved
15:0	DATx[15:0]	Regular data for conversions These bits are read-only and contain the conversion results of the regular channel.The data is left-aligned or right-aligned.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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15 Digital to Analog Conversion (DAC)

15.1 Introduction

DAC is a digital/analog converter, mainly digital input, voltage output.DAC data can be 8-bit or 12-bit and supports DMA functionality.When the DAC is configured in 12-bit mode, the DAC data can be right-aligned or left-aligned.When the DAC is configured in 8-bit mode, the DAC data can be right-aligned.The DAC output channel has 1, with independent converter.V_{REF+} is used as the DAC voltage reference through the pin input to make the DAC conversion data more accurate.

15.2 Main Features

- One independent DAC converter, corresponding to one output channel
- Monotonous output
- Support 8-bit or 12-bit output, data in 12-bit mode right-aligned and left-aligned two modes
- Synchronous update
- DMA support
- Noise wave, triangular waveform generation
- Input voltage reference V_{REF+}
- External event triggers the conversion
- DAC block diagram is shown in Figure 15-1. Table 15-1 shows the description of pins.

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Figure 15-1 Block Diagram of A DAC Channel

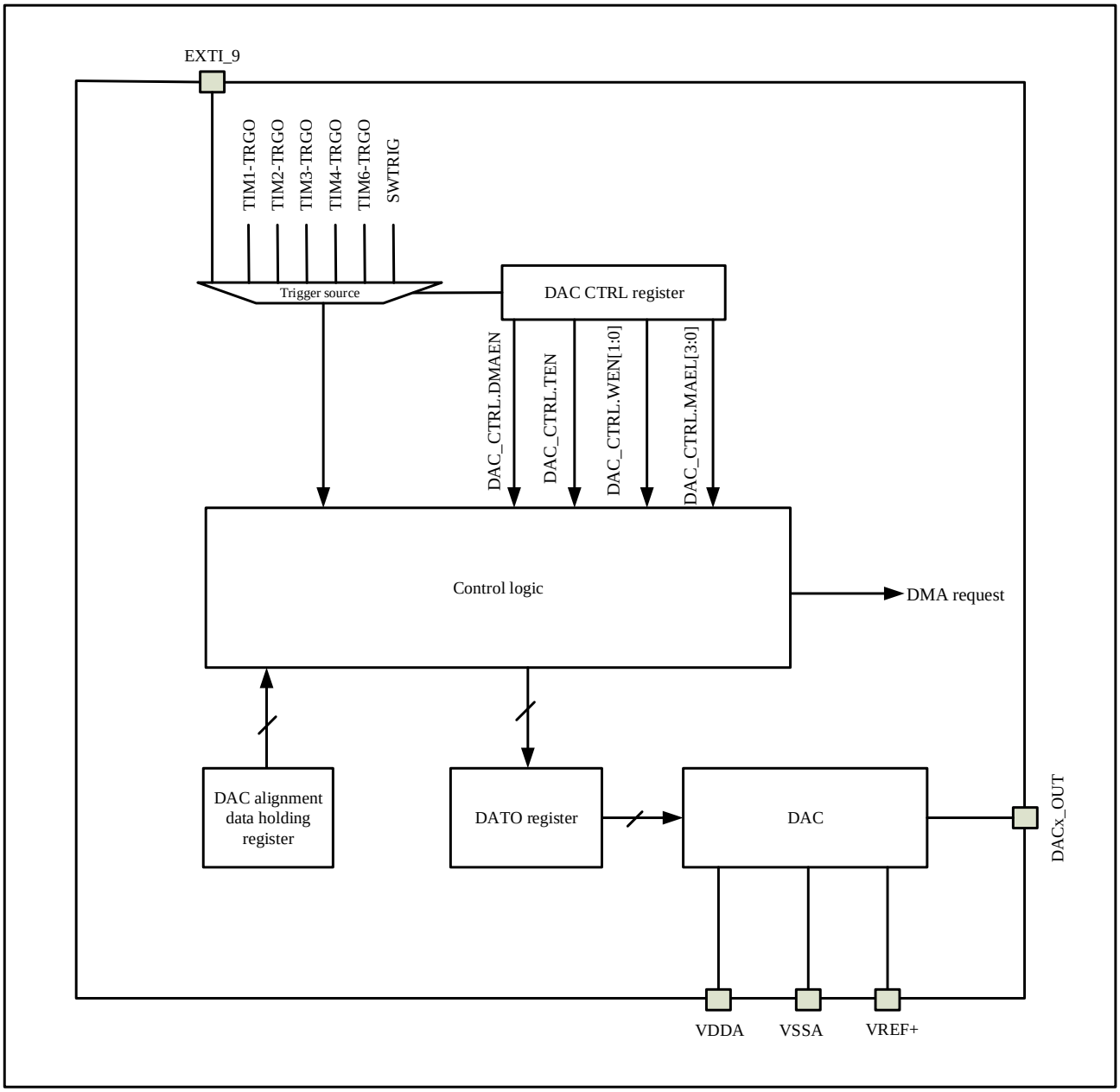

Table 15-1 DAC Pins

Name	Description	Type
V_{REF+}	The positive voltage reference used by the DAC, 2.97 V≤ V_{REF+}≤ V_{DDA}	Input, analog voltage reference
V_{DDA}	Analog power supply	Input, analog power supply
V_{SSA}	Analog power supply ground	Input, analog power supply ground
DAC_OUT	DAC analog output	Analog output signal

Note: When the DAC is enabled, PB13 needs to be configured as analog input mode. PB13 will automatically connect to the output of the DAC.

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15.3 DAC Function Description and Operation Description

15.3.1 DAC Enable

Powering on the DAC can be done by configuring DAC_CTRL.CHEN = 1. It takes some time for t_{WAKEUP} to open the DAC.

15.3.2 DAC Output Buffer

By configuring DAC_CTRL.BEN to disable or enable the output buffer of DAC, if the output buffer is enable, the output impedance is reduced, the driving ability is enhanced, and the external load can be driven without the external operational amplifier.

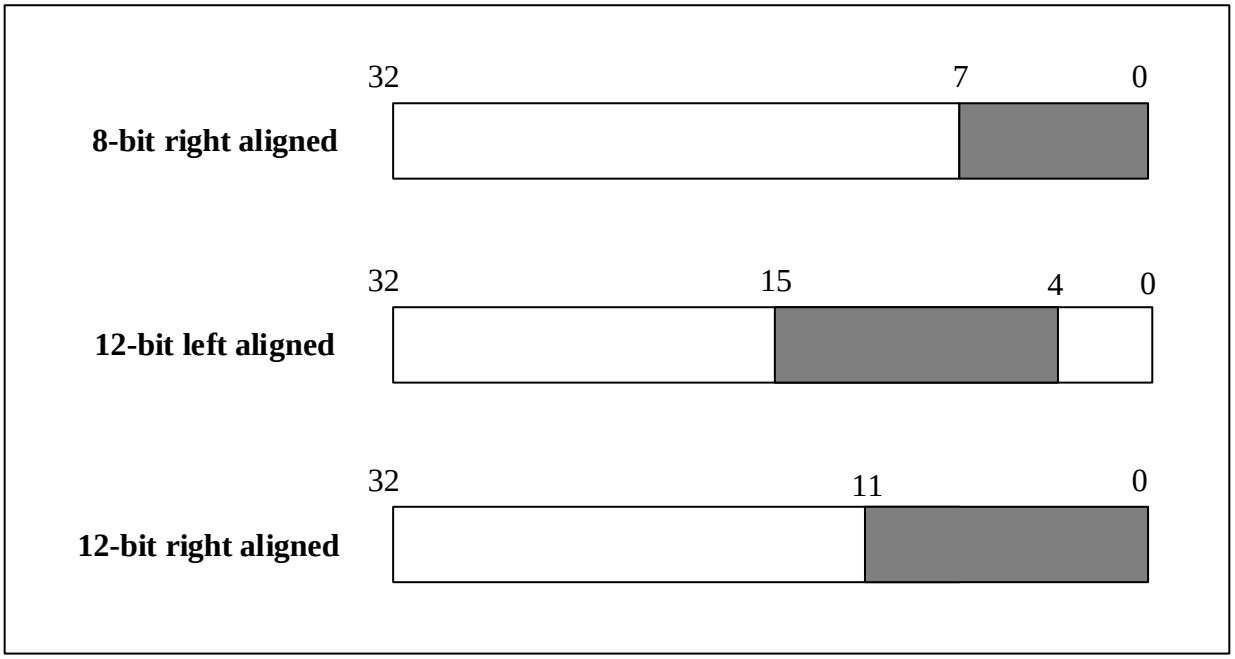
15.3.3 DAC Data Format

When the configuration data is written to the DAC_DR12CH register, the data is written to DAC_DR12CH[11:0], and the 12-bit data is right-aligned. (Actually stored in the register DACCHD[11:0] bits, DACCHD is the internal data memory register)

When the configuration data is written to the DAC_DL12CH register, the data is written to DAC_DL12CH[15:4], and the 12-bit data is left-aligned. (Actually stored in the register DACCHD[11:0] bits, DACCHD is the internal data memory register)

When the configuration data is written to the DAC_DR8CH register, the data is written to DAC_DR8CH[7:0], and the 8-bit data is right-aligned. (Actually stored in the register DACCHD[11:4] bits, DACCHD is the internal data memory register)

Figure 15-2 Data Register of Single DAC Channel Mode



15.3.4 DAC Trigger

Configure DAC_CTRL.TEN = 1 can enable external trigger of DAC, and DAC_CTRL.TSEL [2:0] is configured to select an external triggering event as the external triggering source for the DAC.

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Table 15-2 DAC External Trigger

Trigger source	Type	TSEL[2:0]
Timer 1 TRGO events	Internal signal from the on-chip timer	000
Timer 2 TRGO events		001
Timer 3 TRGO events		010
Timer 4 TRGO events		011
Timer 6 TRGO events		100
EXTI line 9	External pins	101
SWTRIG (Software Triggered)	Software control bit	110

When the DAC is triggered by timer output or the rising edge of EXTI line 9, the data in the aligned data hold register will be transferred to the DAC_DATO register. This data transfer process takes 3 APB1 clock cycles.

DAC_SOTTR.TREN = 1 can enable the DAC software trigger. When the DAC is triggered by the software, the data of the aligned data hold register will be transmitted to the DAC_DATO register.

Notes:

(1) Do not change the DAC_CTRL.TSEL[2:0] bit when the DAC is enabled.

(2) It takes 1 APB1 clock cycle for the data of the data holding register to be transferred to the DAC_DATO register when DAC is triggered by software.

15.3.5 DAC Conversion

If DAC trigger is enabled, the data in the DAC alignment data hold register will be transferred to the DAC_DATO register after three APB1 cycles according to the selected trigger event when the hardware trigger occurs. When the software trigger occurs, the data in the DAC alignment data hold register is transferred to the DAC_DATO register after one APB1 cycle.If trigger is not enabled, data in the DAC alignment data hold register is automatically transferred to the DAC_DATO register after one APB1 cycle.

After the DAC transfers data to the DAC_DATO register from its data hold register, the output is valid for the time $t_{SETTTLING}$, which is related to the supply voltage and the analog output load.

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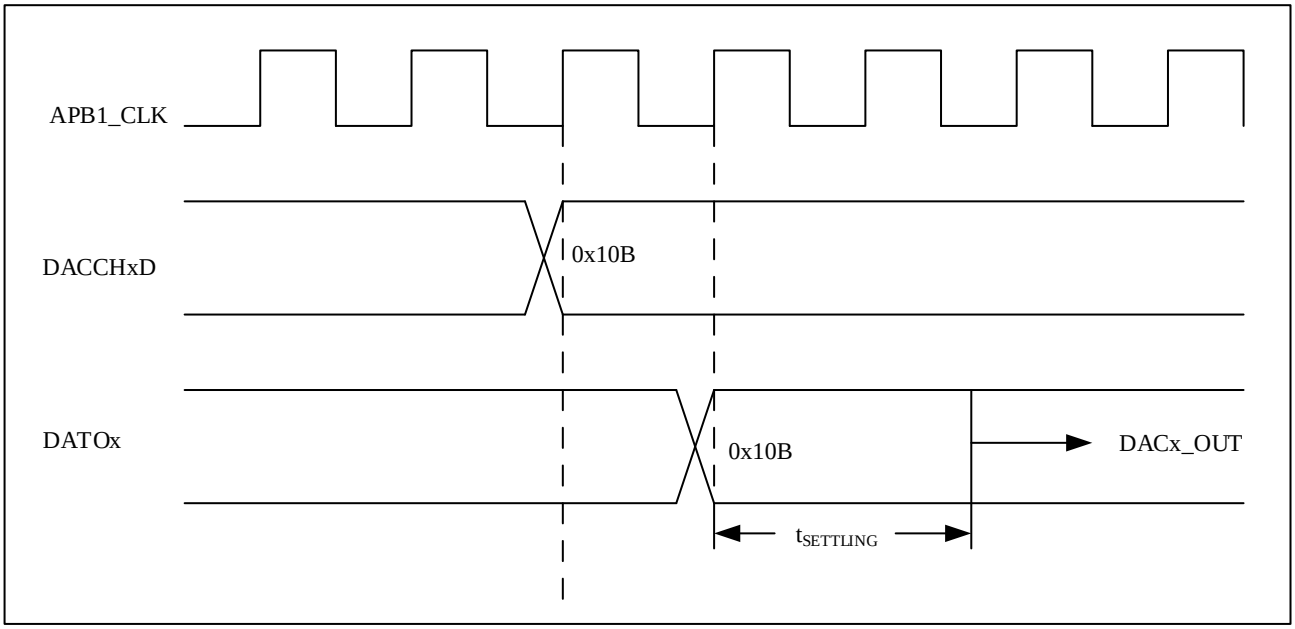
Figure 15-3 Tine Diagram of Transitions with Trigger Disable



15.3.6 DAC Output Voltage

The digital input is converted to analog voltage output by a DAC module in a linear relationship ranging from 0 to VREF+.The output voltage of DAC is calculated as follows:

DAC output = V_{REF+} * (DATO / 4095).

15.3.7 DMA Requests

DAC_CTRL1.DMAEN = 1 is configured to enable DMA function. When an external trigger occurs (not a software trigger), a DMA request is generated and the value of data hold register is then transferred to the DAC_DATO register.

Note: DMA requests for DAC have no accumulative function, and when the second external trigger occurs before the response to the first external trigger, the second DMA request cannot be processed and there is no error reporting mechanism.

15.3.8 Noise Generation

DAC can generate noise, by configuring DAC_CTRL.WEN[1:0] to '01' to turn on the noise function, by configuring DAC_CTRL.MASEL[3:0] to select which bits of the linear feedback shift register (LFSR) are masked, the value of LFSR is added to the value of the DAC alignment data holding register and written to the DAC_DATO register (overflow bits are discarded). The initial value of LFSR is 0xAAA, and the value of LFSR is updated after 3 APB1 cycles after the trigger event occurs.

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Figure 15-4 LFSR Algorithm for DAC

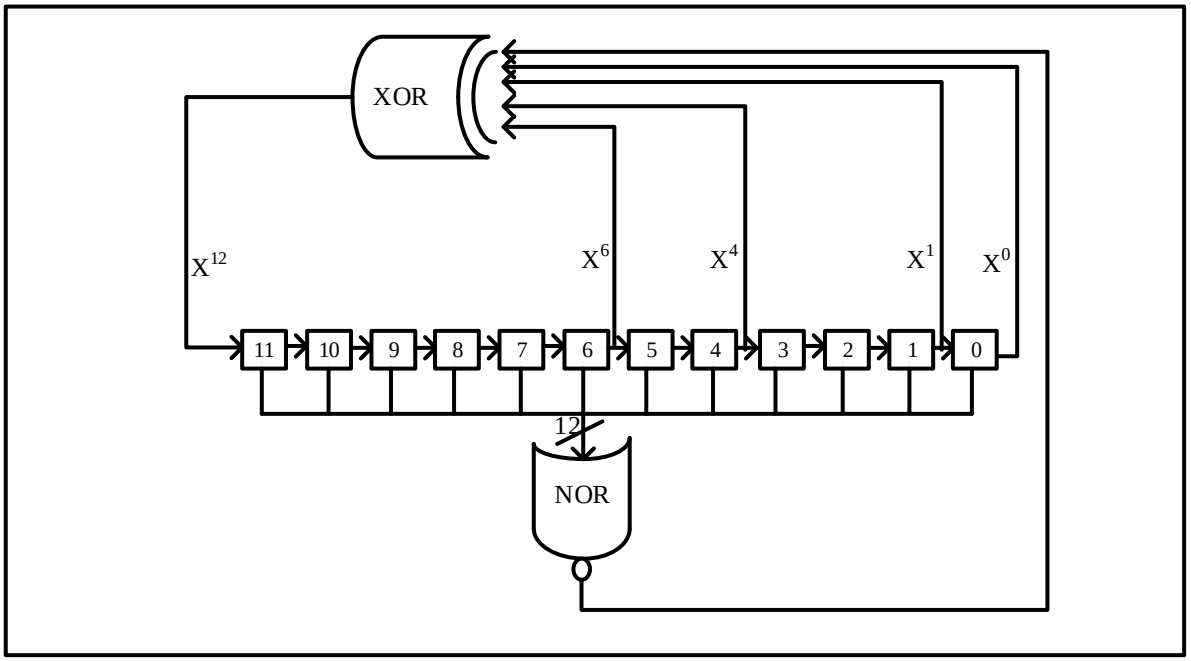
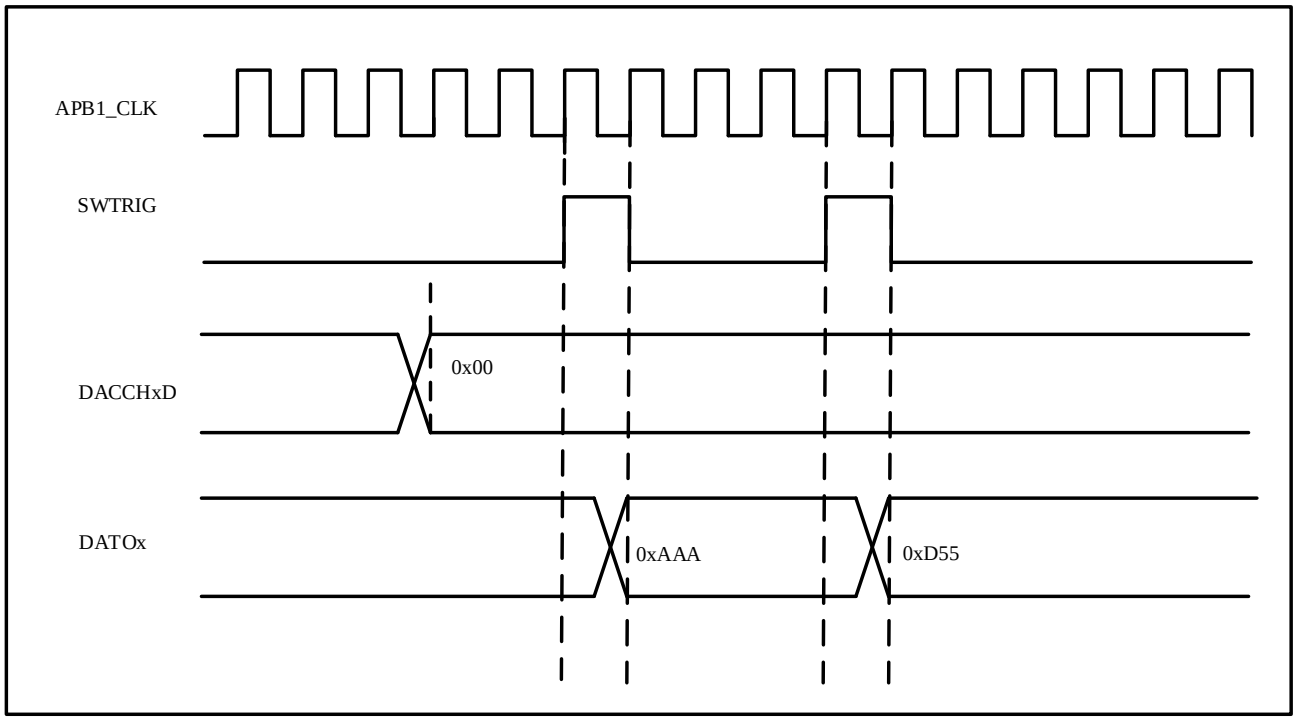


Figure 15-5 DAC Conversion with LFSR Waveform Generation (Enable Software Trigger)



Note: The DAC is configured to trigger to generate noise.

15.3.9 Triangular Wave Generation

The DAC can generate a triangular wave. The triangular wave function can be turned on by configuring DAC_CTRL.WEN[1:0] as '10', and the amplitude of the triangular wave can be selected by configuring DAC_CTRL.MASEL[3:0]. The value of the internal triangular wave counter is added to the value of the DAC alignment data holding register and written to the DAC_DATO register (overflow bits are discarded).The value of

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the triangular wave counter is updated 3 APB1 cycles after the trigger event occurs, the triangular wave counter will accumulate to the maximum amplitude value set, and then decrement to 0, and so on.

Figure 15-6 Triangle Wave Generation of DAC

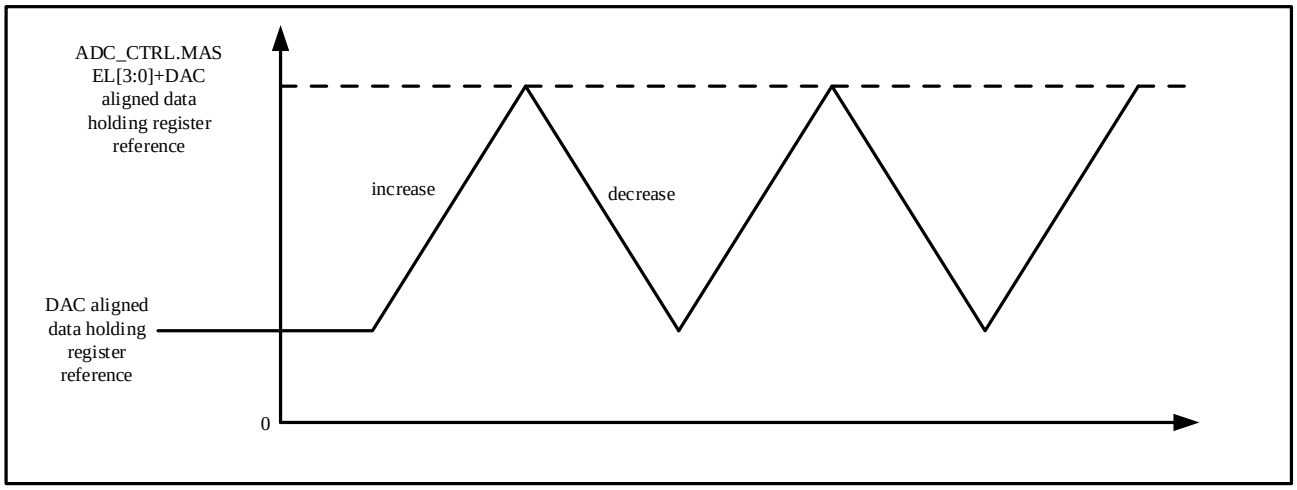
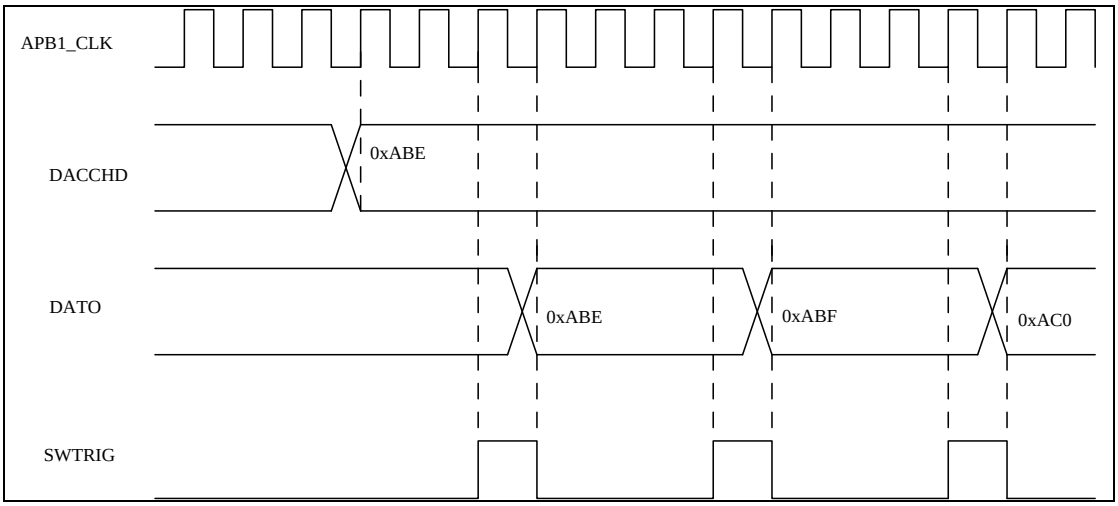


Figure 15-7 DAC Conversion with Trigonometry Generation (Enable Software Trigger)



Notes:

(1) Only when the DAC is configured to trigger, then the triangular wave can be generated

(2) DAC_CTRL.MASEL[3:0] cannot be set after DAC is enabled.

15.4 DAC Register

15.4.1 DAC Registers Overview

Table 15-3 DAC Registers Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DAC_CTRL	Reserved																	TSEL[2:0]			WEN[1:0]		Reserved	BDASEL	MASEL[3:0]				TEN	BEN	DMAEN	CHEN
	Reset Value																		0	0	0	0	0		0	0	0	0	0	0	0	0	0
004h	DAC_SOTTR	Reserved																															TREN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																																0
008h	DAC_DATO	Reserved																				DACCHDO[11:0]											
	Reset Value																																
00Ch	DAC_DR8CH	Reserved																				DACCHD[7:0]											
	Reset Value																					0	0	0	0	0	0	0	0				
010h	DAC_DL12CH	Reserved																DACCHD [11:0]												Reserved			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0				
014h	DAC_DR12CH	Reserved																				DACCHD [11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0

15.4.2 DAC Control Register (DAC_CTRL)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TSEL[2:0]			WEN[1:0]		Reserved	BDASEL	MASEL[3:0]				TEN	BEN	DMAEN	CHEN
	rw			rw			rw	rw				rw	rw	rw	rw

Bit Field	Name	Description
31:15	Reserved	Reserved,the reset value must be maintained
14:12	TSEL[2:0]	DAC triggers selection This bit is used for selection of DAC external triggers. 000：TIM1 TRGO event 001：TIM2 TRGO event 010：TIM3 TRGO event 011：TIM4 TRGO event 100：TIM6 TRGO event 101：External interrupt line 9 110：Software trigger
11:10	WEN[1:0]	DAC noise/triangular wave function selection. The bits are set to 1 and cleared by the software. 00: Disable noise and triangular wave 01: Enable the noise function 1x: Enables the triangular wave function
9	Reserved	Reserved, the reset value must be maintained.
8	BDASEL	DAC channel output buffer drive capability selection The bit is set to 1 and cleared by the software. 0: DAC buffer normal drive capability 1: DAC buffer high drive capability
7:4	MASEL[3:0]	DAC shield/amplitude selector.

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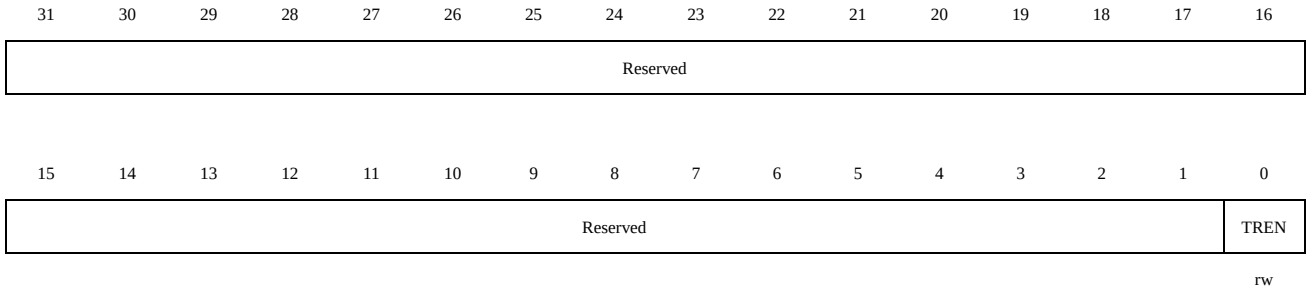
Bit Field	Name	Description
		These bits are configured by software to set the LFSR shielding bits for the noise function and the amplitude of the triangular wave. 0000: unmasked LFSR bit 0 / delta amplitude equals 1 0001: unmasked LFSR bit [1:0] / triangular amplitude is equal to 3 0010: unmasked LFSR bit [2:0] / triangular amplitude equals 7 0011: unmasked LFSR bit [3:0] / triangular amplitude equals 15 0100: unmasked LSFR bit [4:0] / triangular amplitude equals 31 0101: Unmasked LFSR bit [5:0] / triangular amplitude equals 63 0110: unmasked LFSR bit [6:0] / triangular amplitude equals 127 0111: Unmasked LFSR bit [7:0] / triangular amplitude equals 255 1000: unmasked LFSR bit [8:0] / triangular amplitude equals 511 1001: Unmasked LFSR bit [9:0] / triangular amplitude equals 1023 1010: unmasked LFSR bit [10:0] / triangular amplitude equals 2047 ≥1011: unmasked LFSR bit [11:0] / triangular amplitude is equal to 4095
3	TEN	DAC trigger on. This bit is set to 1 and cleared by the software to enable/disable DAC triggering. 0: disables DAC triggering 1: enables DAC triggering
2	BEN	Enable the DAC output cache. This bit is set to 1 and cleared by the software to enable/disable the DAC's output buffer. 0: Disable the DAC channel output buffer 1: Enable the DAC channel output buffer
1	DMAEN	DAC DMA function enable. This bit is set to 1 and cleared by software. 0: Disable DAC DMA function 1: Enable DAC DMA function
0	CHEN	DAC enable. This bit is set to 1 and cleared by the software to enable/disable the DAC. 0: disables the DAC 1: Enable the DAC

15.4.3 DAC Software Trigger Register (DAC_SOTTR)

Address offset: 0x04

Reset value: 0x0000 0000



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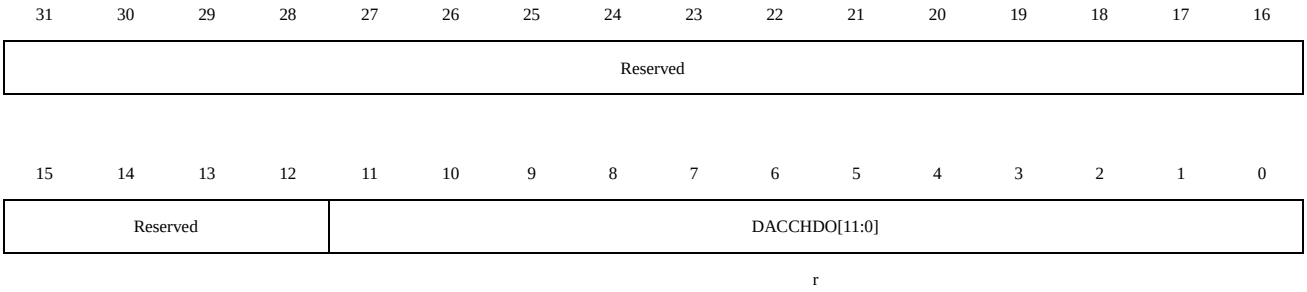
Bit Field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	TREN	DAC software trigger This bit is setting by software to enable/disable software trigger. 0: Disables the DAC software trigger. 1: Enable the DAC software trigger. *Note: After the alignment data hold register transfers data to the DAC_DATO register, this bit will be cleared by the hardware after an APB1 clock.*

15.4.4 DAC Data Output Register (DAC_DATO)

Address offset: 0x08

Reset value: 0x0000 0000

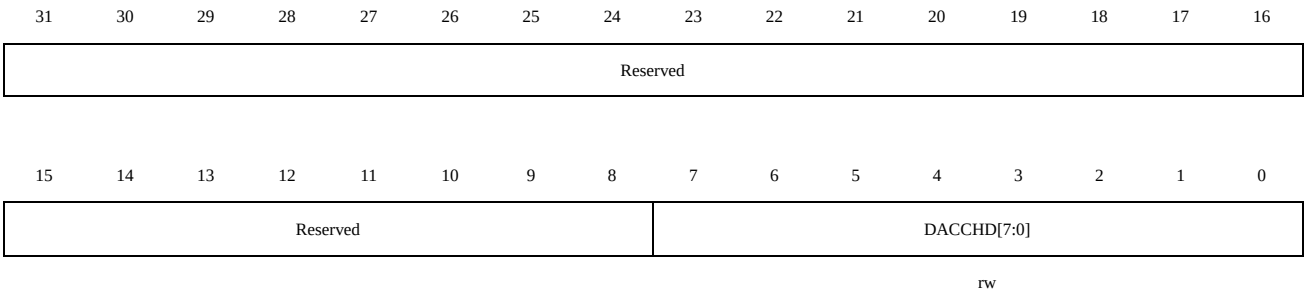


Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:0	DACCHDO[11:0]	DAC data output. These bits are read-only and represent the output data of the DAC channel

15.4.5 DAC 8-bit Right-aligned Data Hold Register (DAC_DR8CH)

Address offset: 0x0C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	DACCHD[7:0]	DAC8 bits right aligned data The bits are configured by the software and the DAC converts the data.

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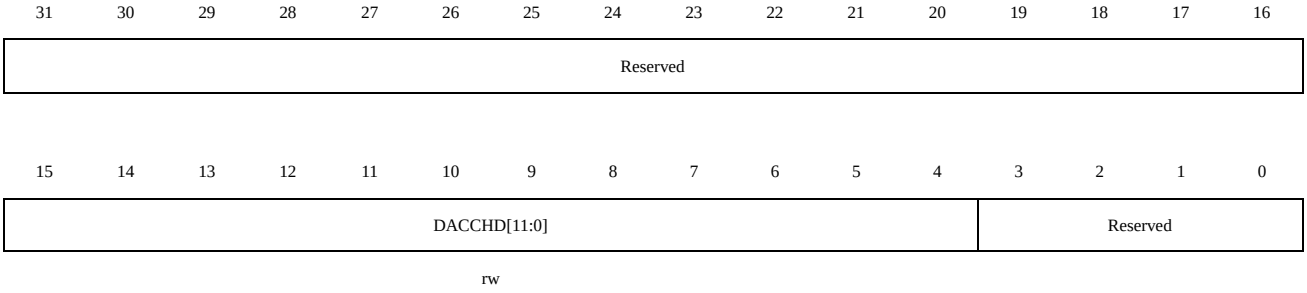
15.4.6 DAC 12-bit Left-aligned Data Hold Register (DAC_DL12CH)

Address offset: 0x10

Reset value: 0x0000 0000

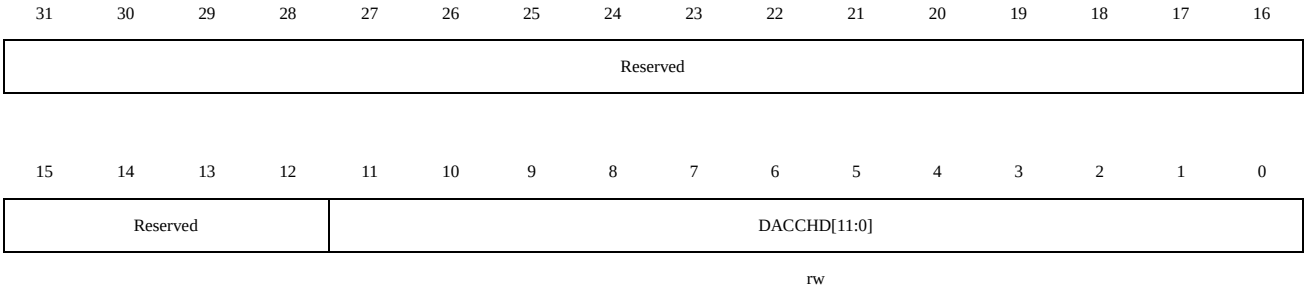


Bit Field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:4	DACCHD[11:0]	DAC12 bits left aligned data The bits are configured by the software and the DAC converts the data.
3:0	Reserved	Reserved, the reset value must be maintained.

15.4.7 DAC 12-bit Right-aligned Data Hold Register (DAC_DR12CH)

Address offset: 0x14

Reset value: 0x0000 0000



Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:0	DACCHD[11:0]	DAC12 bits right aligned data The bits are configured by the software and the DAC converts the data.

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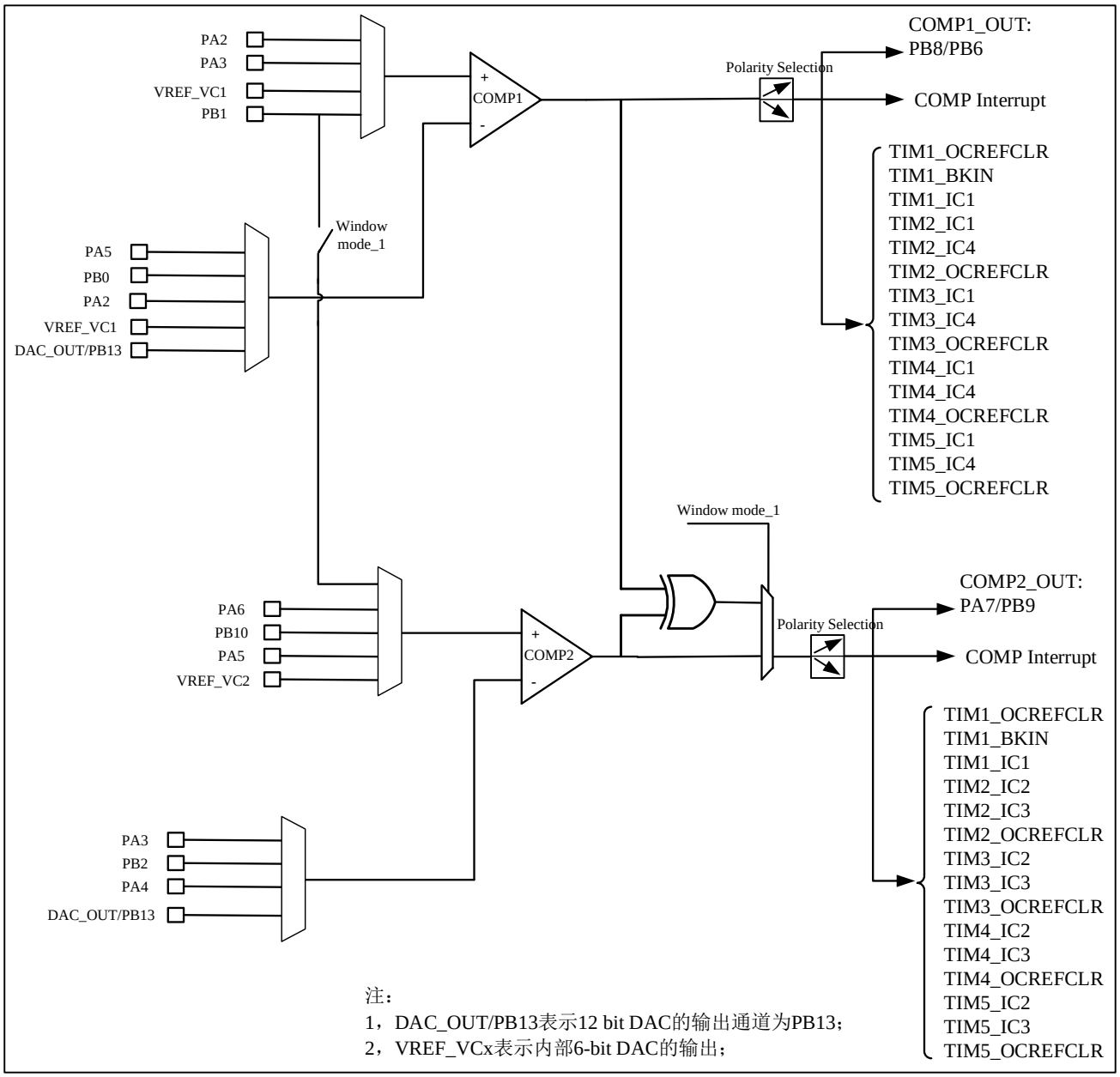
16 Comparator (COMP)

The COMP module is used to compare the analog voltages of two inputs and output high/low levels based on the comparison results.When the input voltage of "INP" is higher than the input voltage of "INM", the comparator output is high; when the input voltage of "INP" is lower than the input voltage of "INM", the comparator output is low.

16.1 COMP System Connection Block Diagram

The COMP module supports an independent comparator, which is connected to the APB bus.

Figure 16-1 COMP1 and COMP2 System Connection Diagram



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Email：info@nationstech.com
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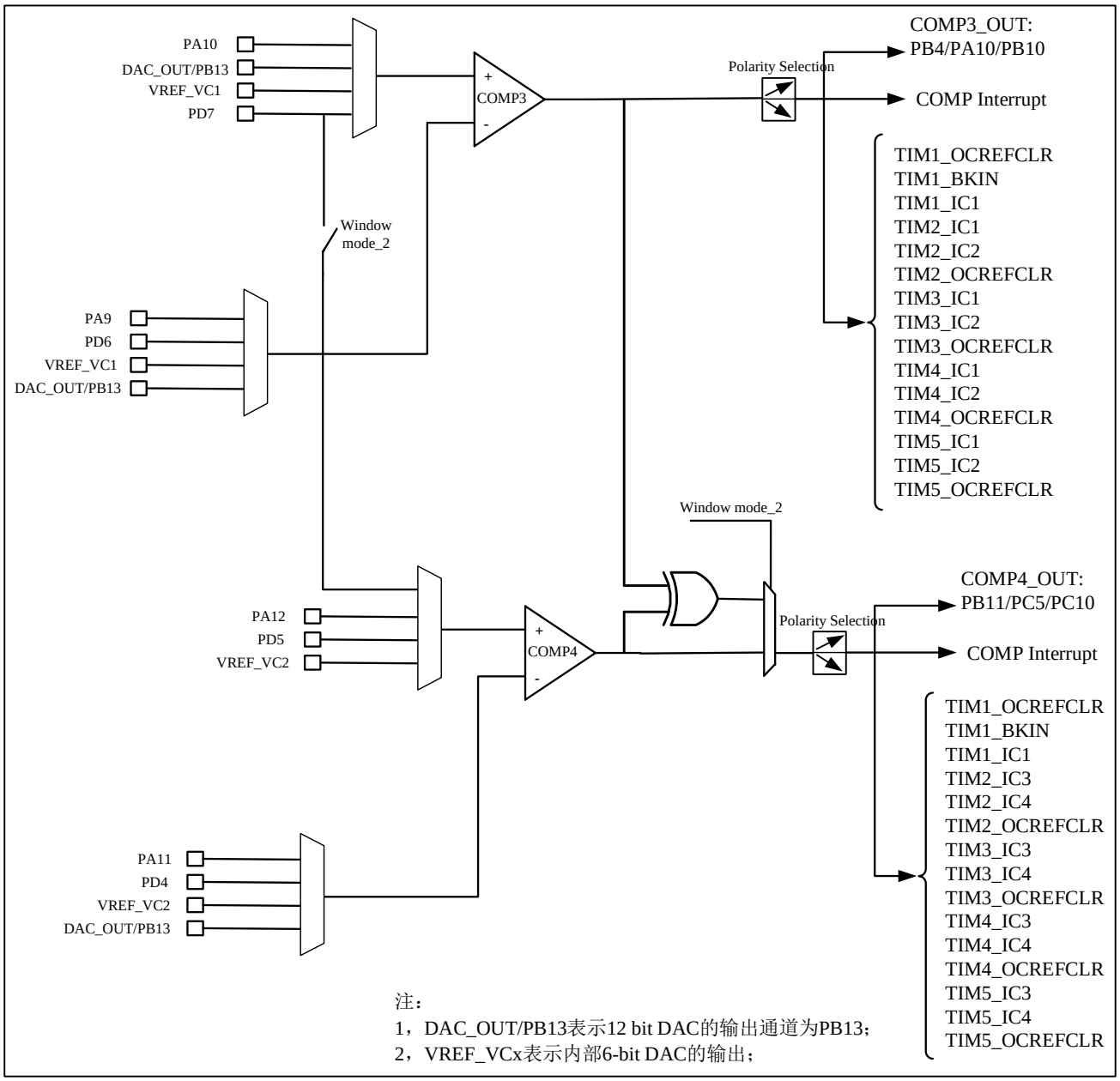
Nanshan District, Shenzhen, 518057, P.R.China

Figure 16-2 COMP3 and COMP4 System Connection Diagram



16.2 COMP Features

- One independent comparator
- Share two internal reference voltage input of 6 bit DAC
- Supports filter clock and filter reset
- Output polarity can be configured as high and low
- The hysteresis can be configured with none, low, medium, or high
- The comparison result can be output to the I/O port or trigger timer, which is used to capture events, OCREF_CLR events, brake events, and generate interrupts

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

- Input channels can select I/O ports
- Can be configured with read-only or read-write, and can be unlocked only after a reset
- Supports blanking, configurable blanking source
- COMP1/COMP2 and COMP3/COMP4 can form a window comparator.
- Wake the system from Sleep mode by generating an interrupt.
- Filter window size can be configured
- Filter threshold size can be configured
- Filter sampling frequency can be configured

16.3 COMP Configuration Precedure

The complete configuration items are as follows. If the default configuration is used, skip the corresponding configuration items.

- Configure hysteresis level COMP_CTRL.HYST[1:0].
- Configure the output polarity COMP_CTRL.POL.
- Configure input selection, comparator positive COMP_CTRL.INPSEL, negative COMP_CTRL.INMSEL.
- Configure output selection COMP_CTRL.OUTSEL[2:0].
- Configure the blanking source COMP_CTRL.BLKING[2:0].
- Configure the filter sampling window COMP_FILC.SAMPW[4:0].
- Configure the threshold COMP_FILC.THRESH[4:0] (Threshold should be greater than COMP_FILC.SAMPW[4:0]/2).
- Configure the filter sampling frequency (for timer applications, sampling frequency should be greater than 5MHz).
- Enable COMP_FILC.FILEN filter.
- Enable COMP_CTRL.EN on the comparator.

Note: For the above steps, the filter should be enabled first and then the comparator should be enabled. The comparator should be enabled after the filtering (if enabled) is configured and enabled. In addition, when the comparator control register is locked, it can only be unlocked by reset.

16.4 COMP Operating Mode

16.4.1 Window Mode

Comparators can be combined as window comparator. COMP1 and COMP2 can be combined as window comparator and share PB1. COMP3 and COMP4 can be combined as window comparator and share PD7.

16.4.2 Independent Comparator

One comparator can be configured independently to complete the comparator functions. The output of the comparator can be output to I/O ports. The comparator supports different remapping ports. And the output of the comparator can

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be selected and connected to the corresponding port by configuration.

The comparator output supports triggering events, for example, it can be configured as timer 1 brake function.

Note: Refer to the comparator interconnection for specific configuration

16.5 Comparator Interconnection

For interconnection of comparator output ports, please refer to the GPIO remapping chapter on IO multiplexing function.

The comparator OUT pins have the following configuration:

COMP1	COMP2	COMP3	COMP4
PB6	PA7	PB4	PB11
PB8	PB9	PA10	PC10
-	-	PB10	PC5

The comparator INP pins have the following configuration:

INPSEL	COMP1	COMP2	COMP3	COMP4
000	PA2	PB1	PA10	PD7
001	PA3	PA6	DAC_OUT(PB13)	PA12
010	VREF_VC1	PB10	VREF_VC1	PD5
011	PB1	PA5	PD7	VREF_VC2
100	-	VREF_VC2	-	-

The comparator INM pins have the following configuration:

INMSEL	COMP1	COMP2	COMP3	COMP4
000	PA5	PA3	PA9	PA11
001	PB0	PB2	PD6	PD4
010	PA2	PA4	VREF_VC1	VREF_VC2
011	VREF_VC1	DAC_OUT(PB13)	DAC_OUT(PB13)	DAC_OUT(PB13)
100	DAC_OUT(PB13)	-	-	-

The signals of TRIG output by the comparator have the following interconnections:

TRIG	COMP1	COMP2	COMP3	COMP4
0000	TIM1_OCrefclear	TIM1_OCrefclear	TIM1_OCrefclear	TIM1_OCrefclear
0001	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN
0010	TIM1_IC1	TIM1_IC1	TIM1_IC1	TIM1_IC1
0011	TIM2_IC1	TIM2_IC2	TIM2_IC1	TIM2_IC3
0100	TIM2_IC4	TIM2_IC3	TIM2_IC2	TIM2_IC4
0101	TIM2_OCrefclear	TIM2_OCrefclear	TIM2_OCrefclear	TIM2_OCrefclear
0110	TIM3_IC1	TIM3_IC2	TIM3_IC1	TIM3_IC3
0111	TIM3_IC4	TIM3_IC3	TIM3_IC2	TIM3_IC4
1000	TIM3_OCrefclear	TIM3_OCrefclear	TIM3_OCrefclear	TIM3_OCrefclear
1001	TIM4_IC1	TIM4_IC2	TIM4_IC1	TIM4_IC3
1010	TIM4_IC4	TIM4_IC3	TIM4_IC2	TIM4_IC4

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1011	TIM4_OCrefclear	TIM4_OCrefclear	TIM4_OCrefclear	TIM4_OCrefclear
1100	TIM5_IC1	TIM5_IC2	TIM5_IC1	TIM5_IC3
1101	TIM5_IC4	TIM5_IC3	TIM5_IC2	TIM5_IC4
1110	TIM5_OCrefclear	TIM5_OCrefclear	TIM5_OCrefclear	TIM5_OCrefclear
Other	-	-	-	-

16.6 Comparator Output

The COMP output supports the value before filtering with COMPx_CTRL.OUT and the filtered value after filtering with COMPx_CTRL.FLTOUT.

- When filtering is disabled, the output result is valid for COMPx_CTRL.OUT, while the output result is invalid for COMPx_CTRL.FLTOUT.
- When filtering is enabled, COMPx_CTRL.OUT and COMPx_CTRL.FLTOUT respectively indicate the comparator output results before and after filtering.

COMP supports interrupt response. There are two types of interrupts.

16.7 Interrupt

COMP supports interrupt response. There are two types of interrupts.

- The polarity of COMP_CTRL.POL is not reversed and the interrupt is enabled. When INPSEL > INMSEL, the comparator interrupt will be generated when COMP_CTRL.OUT is set to 1 by hardware.
- The polarity of COMP_CTRL.POL is reversed and the interrupt is enabled. When INPSEL < INMSEL, the comparator interrupt will be generated when COMP_CTRL.OUT is set to 1 by hardware.

16.8 COMP Registers

16.8.1 COMP Register Overview

Table 16-1 COMP Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
010h	COMP1_CTRL	Reserved												FLT_OUT	OUT	BLKING[3:0]			HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	COMP1_FILC	Reserved																					SAMPW [4:0]					THRESH [4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
018h	COMP1_FILP	Reserved																	CLKPSC[15:0]															
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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01Ch	Reserved																														
020h	COMP2_CTRL	Reserved			FLT_OUT	OUT	BLKING[3:0]				HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN							
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
024h	COMP2_FILC	Reserved																SAMPW [4:0]					THRESH [4:0]								FILEN	
	Reset Value																	0	0	0	0	0	0	0	0	0	0					
028h	COMP2_FILP	Reserved																														
	Reset Value																															
02Ch	Reserved																														
030h	COMP3_CTRL	Reserved			FLT_OUT	OUT	BLKING[3:0]				HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN							
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
034h	COMP3_FILC	Reserved																SAMPW [4:0]					THRESH [4:0]								FILEN	
	Reset Value																	0	0	0	0	0	0	0	0	0	0					
038h	COMP3_FILP	Reserved																														
	Reset Value																															
03Ch	Reserved																														
040h	COMP4_CTRL	Reserved			FLT_OUT	OUT	BLKING[3:0]				HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN							
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
044h	COMP4_FILC	Reserved																SAMPW [4:0]					THRESH [4:0]								FILEN	
	Reset Value																	0	0	0	0	0	0	0	0	0	0					
048h	COMP4_FILP	Reserved																														
	Reset Value																															

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| | | |

Bit Field	Name	Description
31:20	Reserved	Reserved，the reset value must be maintained
19	FLTOUT	This bit is COMP filter output state. 0: Output is low 1: Output is high
18	OUT	This read-only bit is COMP output state. 0: Output is low 1: Output is high
17:15	BLKING[2:0]	These bits select which Timer output controls the comparator 1 output blanking. 000: No blanking 001: TIM1 OC5 selected as blanking source Other configurations: reserved
14:13	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis 01: Low hysteresis 10: Medium hysteresis 11: High hysteresis
12	POL	This bit is used to invert the comparator 1 output. 0: Output is not inverted 1: Output is inverted
11:8	OUTSEL[3:0]	These bits select which Timer input must be connected with the comparator1 output. 0000：TIM1_OCrefclear 0001：TIM1_BKIN 0010：TIM1_IC1 0011：TIM2_IC1 0100：TIM2_IC4 0101：TIM2_OCrefclear 0110：TIM3_IC1 0111：TIM3_IC4 1000：TIM3_OCrefclear 1001：TIM4_IC1 1010：TIM4_IC4 1011：TIM4_OCrefclear 1100：TIM5_IC1 1101：TIM5_IC4 1110：TIM5_OCrefclear 1111：Reserved
7:5	INPSEL[2:0]	Comparator 1 non-inverting input selection. 000: PA2 001: PA3 010: VREF_VC1 011: PB1
4:1	INMSEL[3:0]	These bits allows to select the source connected to the inverting input of the

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Bit Field	Name	Description
		comparator 1. 0000：PA5 0001：PB0 0010：PA2 0011：VREF_VC1 0100：DAC_OUT/PB13
0	EN	This bit switches COMP1 ON/OFF. 0: Comparator 1 disabled 1: Comparator 1 enabled

16.8.3 COMP1 Filter Control Register (COMP1_FILC)

Address offset : 0x14

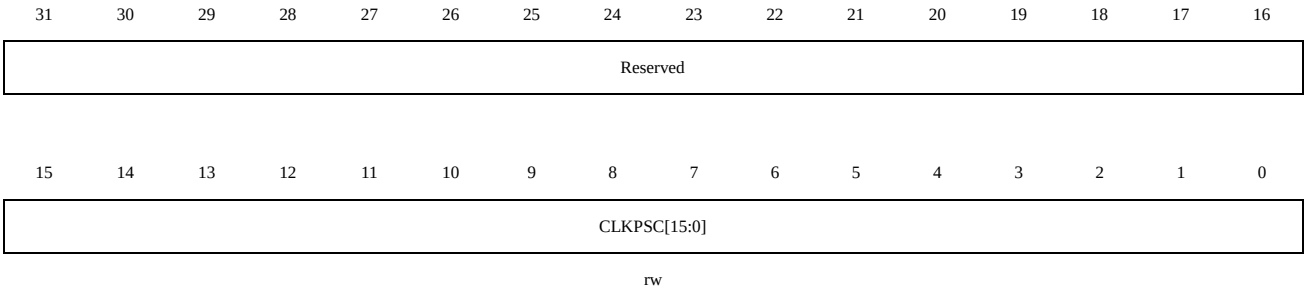
Reset value : 0x0000 0000

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Sampling window size of low pass filter, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	Low pass filter threshold, the value must be greater than SAMPW / 2
0	FILEN	Filter enable bit 0: Disable 1: Enable

16.8.4 COMP1 Filter Frequency Divsion Register (COMP1_FILP)

Address offset : 0x18

Reset value : 0x0000 0000



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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low pass filter sampling clock predivision, system clock frequency division = CLKPSC + 1. 0: Every clock 1: Every 2 clocks 2: Every 3 clocks ... 65535: Every 65536 clocks

16.8.5 COMP2 Control Register (COMP2_CTRL)

Address offset : 0x20

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												FLTOUT	OUT	BLKING[1:0]	
r												r	r	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKING[0]	HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN
rw	rw		rw	rw				rw			rw				rw

Bit Field	Name	Description
31:20	Reserved	Reserved，the reset value must be maintained
19	FLTOUT	This bit is COMP filter output state. 0: Output is low 1: Output is high
18	OUT	This read-only bit is COMP output state. 0: Output is low 1: Output is high
17:15	BLKING[2:0]	These bits select which Timer output controls the comparator 2 output blanking. 000: No blanking 001: TIM1 OC4 selected as blanking source Other configurations: reserved
14:13	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis 01: Low hysteresis 10: Medium hysteresis 11: High hysteresis
12	POL	This bit is used to invert the comparator 2 output. 0: Output is not inverted 1: Output is inverted
11:8	OUTSEL[3:0]	These bits select which Timer input must be connected with the comparator2 output.

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Bit Field	Name	Description
		0000：TIM1_OCrefclear 0001：TIM1_BKIN 0010：TIM1_IC1 0011：TIM2_IC2 0100：TIM2_IC3 0101：TIM2_OCrefclear 0110：TIM3_IC2 0111：TIM3_IC3 1000：TIM3_OCrefclear 1001：TIM4_IC2 1010：TIM4_IC3 1011：TIM4_OCrefclear 1100：TIM5_IC2 1101：TIM5_IC3 1110：TIM5_OCrefclear 1111：Reserved
7:5	INPSEL[2:0]	Comparator 2 non-inverting input selection. 000: PB1 001: PA6 010: PB10 011: PA5 100: VREF_VC2
4:1	INMSEL[3:0]	These bits allows to select the source connected to the inverting input of the comparator 2. 0000：PA3 0001：PB2 0010：PA4 0011：DAC_OUT/PB13
0	EN	This bit switches COMP2 ON/OFF. 0: Comparator disabled 1: Comparator enabled

16.8.6 COMP2 Filter Control Register (COMP2_FILC)

Address offset : 0x24

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SAMPW[4:0]					THRESH[4:0]					FILEN
					rw					rw					rw

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Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Sampling window size of low pass filter, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	Low pass filter threshold, the value must be greater than SAMPW / 2
0	FILEN	Filter enable bit 0: Disable 1: Enable

16.8.7 COMP2 Filter Frequency Divsion Register (COMP2_FILP)

Address offset : 0x28

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low pass filter sampling clock predivision, system clock frequency division = CLKPSC + 1. 0: Every clock 1: Every 2 clocks 2: Every 3 clocks ... 65535: Every 65536 clocks

16.8.8 COMP3 Control Register (COMP3_CTRL)

Address offset : 0x30

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												FLTOUT	OUT	BLKING[1:0]	
r												r	r	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKING[0]	HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN
rw	rw		rw	rw				rw			rw				rw

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Bit Field	Name	Description
31:20	Reserved	Reserved，the reset value must be maintained
19	FLTOUT	This bit is COMP3 filter output state. 0: Output is low 1: Output is high
18	OUT	This read-only bit is COMP3 output state. 0: Output is low 1: Output is high
17:15	BLKING[2:0]	These bits select which Timer output controls the comparator 3 output blanking. 000: No blanking 001: TIM1 OC4 selected as blanking source Other configurations: reserved
14:13	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis 01: Low hysteresis 10: Medium hysteresis 11: High hysteresis
12	POL	This bit is used to invert the comparator 3 output. 0: Output is not inverted 1: Output is inverted
11:8	OUTSEL[3:0]	These bits select which Timer input must be connected with the comparator3 output. 0000：TIM1_OCrefclear 0001：TIM1_BKIN 0010：TIM1_IC1 0011：TIM2_IC1 0100：TIM2_IC2 0101：TIM2_OCrefclear 0110：TIM3_IC1 0111：TIM3_IC2 1000：TIM3_OCrefclear 1001：TIM4_IC1 1010：TIM4_IC2 1011：TIM4_OCrefclear 1100：TIM5_IC1 1101：TIM5_IC2 1110：TIM5_OCrefclear 1111：Reserved
7:5	INPSEL[2:0]	Comparator 3 non-inverting input selection. 000: PA10 001: DAC_OUT/PB13 010: VREF_VC1 011: PD7
4:1	INMSEL[3:0]	These bits allows to select the source connected to the inverting input of the

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Bit Field	Name	Description
		comparator 3. 0000：PA9 0001：PD6 0010：VREF_VC1 0011：DAC_OUT/PB13
0	EN	This bit switches COMP3 ON/OFF. 0: Comparator 3 disabled 1: Comparator 3 enabled

16.8.9 COMP3 Filter Control Register (COMP3_FILC)

Address offset : 0x34

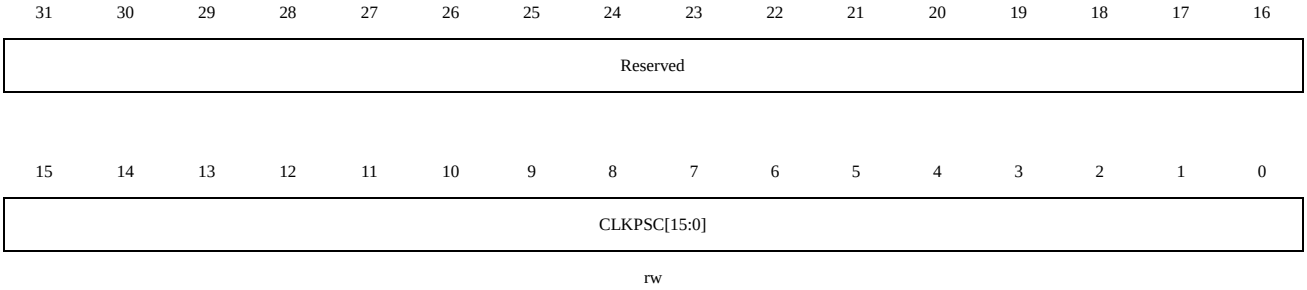
Reset value : 0x0000 0000

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Sampling window size of low pass filter, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	Low pass filter threshold, the value must be greater than SAMPW / 2
0	FILEN	Filter enable bit 0: Disable 1: Enable

16.8.10 COMP3 Filter Frequency Divsion Register (COMP3_FILP)

Address offset : 0x38

Reset value : 0x0000 0000



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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low pass filter sampling clock predivision, system clock frequency division = CLKPSC + 1. 0: Every clock 1: Every 2 clocks 2: Every 3 clocks ... 65535: Every 65536 clocks

16.8.11 COMP4 Control Register (COMP4_CTRL)

Address offset : 0x40

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												FLTOUT	OUT	BLKING[1:0]	
r												r	r	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKING[0]	HYST		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[3:0]				EN
rw	rw		rw	rw				rw			rw				rw

Bit Field	Name	Description
31:20	Reserved	Reserved，the reset value must be maintained
19	FLTOUT	This bit is COMP4 filter output state. 0: Output is low 1: Output is high
18	OUT	This read-only bit is COMP4 output state. 0: Output is low 1: Output is high
17:15	BLKING[2:0]	These bits select which Timer output controls the comparator 4 output blanking. 000: No blanking 001: TIM1 OC4 selected as blanking source Other configurations: reserved
14:13	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis 01: Low hysteresis 10: Medium hysteresis 11: High hysteresis
12	POL	This bit is used to invert the comparator 4 output. 0: Output is not inverted 1: Output is inverted
11:8	OUTSEL[3:0]	These bits select which Timer input must be connected with the comparator 4 output.

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Bit Field	Name	Description
		0000：TIM1_OCrefclear 0001：TIM1_BKIN 0010：TIM1_IC1 0011：TIM2_IC1 0100：TIM2_IC2 0101：TIM2_OCrefclear 0110：TIM3_IC1 0111：TIM3_IC2 1000：TIM3_OCrefclear 1001：TIM4_IC1 1010：TIM4_IC2 1011：TIM4_OCrefclear 1100：TIM5_IC1 1101：TIM5_IC2 1110：TIM5_OCrefclear 1111：Reserved
7:5	INPSEL[2:0]	Comparator 4 non-inverting input selection. 000: PA10 001: DAC_OUT/PB13 010: VREF_VC1 011: PD7
4:1	INMSEL[3:0]	These bits allows to select the source connected to the inverting input of the comparator 4. 0000：PA9 0001：PD6 0010：VREF_VC1 0011：DAC_OUT/PB13
0	EN	This bit switches COMP4 ON/OFF. 0: Comparator 4 disabled 1: Comparator 4 enabled

16.8.12 COMP4 Filter Control Register (COMP4_FILC)

Address offset : 0x44

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SAMPW[4:0]					THRESH[4:0]					FILEN
					rw					rw					rw

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Sampling window size of low pass filter, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	Low pass filter threshold, the value must be greater than SAMPW / 2
0	FILEN	Filter enable bit 0: Disable 1: Enable

16.8.13 COMP4 Filter Frequency Divsion Register (COMP4_FILP)

Address offset : 0x48

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low pass filter sampling clock predivision, system clock frequency division = CLKPSC + 1. 0: Every clock 1: Every 2 clocks 2: Every 3 clocks ... 65535: Every 65536 clocks

16.8.14 COMP Output Select Register (COMP_OSEL)

Address offset : 0x70

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														CMP4XO	CMP2XO
														rw	rw

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Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained
1	CMP4XO	Bit select to choose COPM2 output or the XOR output(comparison of COMP3&4) outputs 0: COMP 4 output； 1: XOR(comparison) output between results of COMP3 and COMP4
0	CMP2XO	Bit select to choose COPM2 output or the XOR output(comparison of COMP1&2) outputs 0: COMP2 Output 1: XOR(comparison) output between results of COMP1 and COMP2

16.8.15 COMP Lock Register(COMP_LOCK)

Address offset : 0x84

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4LK	CMP3LK	CMP2LK	CMP1LK
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved，the reset value must be maintained
3	CMP4LK	Write-once, software-controlled, can only be cleared by system reset. Setting this bit can make COMP4_CTRL read-only. 0: COMP4_CTRL is read-write. 1: COMP4_CTRL is read-only.
2	CMP3LK	Write-once, software-controlled, can only be cleared by system reset. Setting this bit can make COMP3_CTRL read-only. 0: COMP3_CTRL is read-write. 1: COMP3_CTRL is read-only.
1	CMP2LK	Write-once, software-controlled, can only be cleared by system reset. Setting this bit can make COMP2_CTRL read-only. 0: COMP2_CTRL is read-write. 1: COMP2_CTRL is read-only.
0	CMP1LK	Write-once, software-controlled, can only be cleared by system reset. Setting this bit can make COMP1_CTRL read-only. 0: COMP1_CTRL is read-write. 1: COMP1_CTRL is read-only.

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16.8.16 COMP Interrupt Enable Register (COMP_INTEN)

Address offset : 0x8C

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4IEN	CMP3IEN	CMP2IEN	CMP1IEN
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved，the reset value must be maintained
3	CMP4IEN	This bit controls the COMP4 interrupt enable. 0: Disabled 1: Enabled
2	CMP3IEN	This bit controls the COMP3 interrupt enable. 0: Disabled 1: Enabled
1	CMP2IEN	This bit controls the COMP2 interrupt enable. 0: Disabled 1: Enabled
0	CMP1IEN	This bit controls the COMP1 interrupt enable. 0: Disabled 1: Enabled

16.8.17 COMP Interrupt Register (COMP_INTSTS)

Address offset : 0x90

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4IS	CMP3IS	CMP2IS	CMP1IS
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved，the reset value must be maintained

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Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
3	CMP4IS	This bit indicate the interrupt status of COMP4,write 0 to clear.
2	CMP3IS	This bit indicate the interrupt status of COMP3,write 0 to clear.
1	CMP2IS	This bit indicate the interrupt status of COMP2,write 0 to clear.
0	CMP1IS	This bit indicate the interrupt status of COMP1,write 0 to clear.

16.8.18 COMP Reference Voltage Register (COMP_INVREF)

Address offset : 0x94

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		VV2TRM[5:0]						VV2EN	VV1TRM[5:0]						VV1EN
		rw						rw	rw						rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	VV2TRM[5:0]	Internal comparator 2 reference input voltage VREF level selection 0~0b'111111 corresponding to output voltage range from 0 to VDDA totally 64. For example, 7 represents（7+1）*VDDA/32 = 1/4 VDDA
7	VV2EN	VREF2 voltage scaler: 0: disable; 1: enable.
6:1	VV1TRM[5:0]	Internal comparator 1 reference input voltage VREFlevel selection 0~0b'111111 corresponding to output voltage range from 0 to VDDA totally 64. For example, 7 represents（7+1）*VDDA/32 = 1/4 VDDA
0	VV1EN	VREF1 voltage scaler: 0: disable; 1: enable.

16.8.19 COMP Output to Timer Enable Register (COMP_OTIMEN)

Address offset : 0x98

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4 OEN	CMP3 OEN	CMP2 OEN	CMP1 OEN

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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rw rw rw rw

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3	CMP4OEN	This bit controls the function of COMP4 output to the timer. 0: Disable 1: Enable
2	CMP3OEN	This bit controls the function of COMP3 output to the timer. 0: Disable 1: Enable
1	CMP2OEN	This bit controls the function of COMP2 output to the timer. 0: Disable 1: Enable
0	CMP1OEN	This bit controls the function of COMP1 output to the timer. 0: Disable 1: Enable

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

17 Liquid Crystal Display Controller (LCD)

17.1 Introduction

The LCD controller is suitable for monochrome passive Segment LCD, with a maximum of 8 common terminals (COM) and 32 Segment terminals (SEG). The specific number of terminals depends on the package of pin, refer to the data manual for details.The Segment LCD consists of several segments that can be turned visible or invisble. Each segment contains a layer of liquid crystal molecules aligned between the two electrodes.The corresponding segment is visible when a voltage greater than the threshold voltage is applied to the liquid crystal.To avoid electrophoretic effects in the liquid crystal, the segment voltage must be AC(Alternating Current).

17.2 Main Features

- Frame rate is configurable.
- Duty cycle is configurable: static, 1/2, 1/3, 1/4 and 1/8 duty cycle are supported.
- Voltage bias can be configured: static, 1/2, 1/3 and 1/4 bias are supported.
- Double buffering mechanism allows the user to update the data (pixel active/inactive information) in the display memory registers at any time.
- LCD clock source Optional: HSE/16, HSI_8M/8
- Two contrast control methods:
  - Programmable dead time (up to 7 phase periods) between frames;
  - Adjust V_{LCD} in V_{LCDmin}~ V_{LCDmax} range (when using internal step-up converter only).
- Built-in resistor network is used to generate LCD intermediate voltage, which can be configured by software to match the capacitive load of LCD panel.
- Built-in voltage output buffer
- Built-in phase inversion for reduced electromagnetic interference (EMI) and power consumption.
- Support blink function: 1, 2, 3, 4, 8 or all pixels can blink at the specified frequency (0.5Hz, 1Hz, 2Hz or 4Hz)
- Pins used for SEG and COM functions should be configured with the appropriate AFIO.

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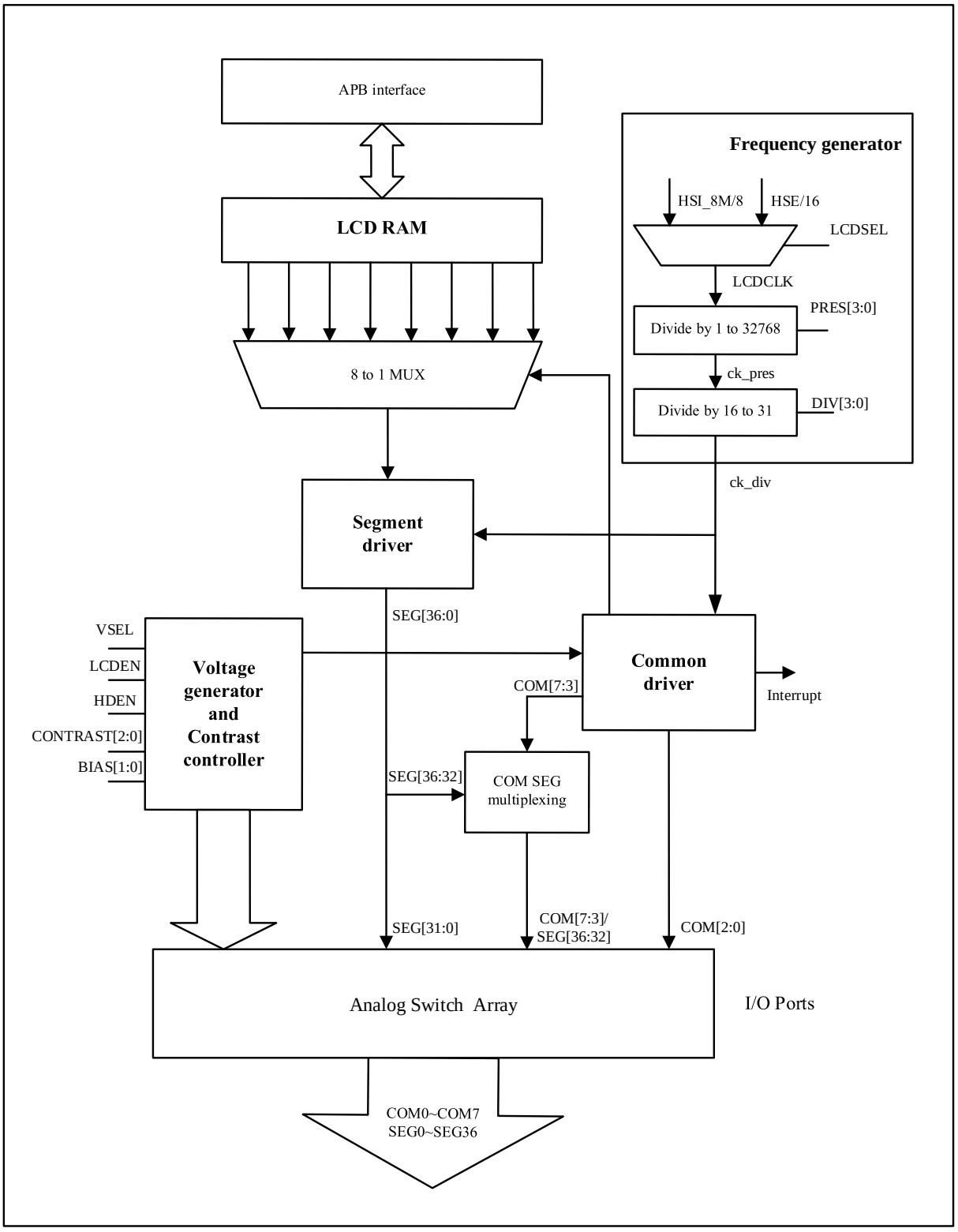
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

17.3 Functional Block Diagram

Figure 17-1 LCD Controller Block Diagram



Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

17.4 Functional Description

The LCD controller provides a fully configurable interface to support a variety of monochrome passive LCD with flexible frame frequencies. Each COM has same waveforms, but different phases. The number of COM ports depends on the duty cycle configuration, with the same waveform in a frame, but only one COM is active in each phase. LCD controllers support a variety of bias and duty cycles for a wide range of display features.

Optical contrast is the difference between the transparency of the on and off segments, that is, contrast can be defined as the difference between the RMS voltage of the on and off segments:

Optical contrast = [V_on(rms)- V_off(rms)]

Contrast also depends on the difference between the on voltage V_on(rms) and the threshold voltage V_th.

Where V_on(rms) and V_off(rms) are related to the duty cycle used to drive the display. As the number of COM terminals required to drive the LCD increases, the gap between V_on(rms) and V_off(rms) increases and the contrast decreases. In addition, for higher V_{LCD}, higher bias levels should be used to better separate V_on(rms) from V_off(rms) for better contrast.

17.4.1 Frequency Generator

The frequency generator consists of a prescaler and a 16~31 clock divider. Configure LCD_FCTRL.PRES[3:0] to select LCDCLK divided by $2^{PRES[3:0]}$. Configure LCD_FCTRL.DIV[3:0] and divide the clock further by 16 to 31 for better frequency division.

Frequency generator output clock frequency f_{ck_div} is the time base of the entire LCD controller. The f_{ck_div} is equivalent to the LCD phase frequency, rather than the frame frequency (they are equal only in case of static duty). Frame frequency (f_{frame}) is obtained from f_{ck_div} by dividing it by the number of active COM terminals (or by multiplying it for the duty cycle).

The relation between the input clock frequency (f_{LCDCLK}) of the frequency generator and its output clock frequency f_{ck_div} is:

$$f_{ck_div} = \frac{f_{LCDCLK}}{2^{PRES} \times (DIV + 16)}$$

The relation between the output clock frequency (f_{ck_div}) and the frame frequency (f_{frame}) is:

$$f_{frame} = f_{ck_div} \times \text{Duty}$$

By controlling LCD_FCTRL.BLINKF[2:0] (configurable to 0,1,2...7), blink frequency in the range of 0.5Hz, 1Hz, 2Hz or 4Hz. The relation between the output clock frequency (f_{ck_div}) and blink frequency (F_{BLINK}) is:

$$f_{BLINK} = f_{ck_div}/2^{(3+BLINKF)}$$

An example of frame rate calculation is shown in the table below:

Table 17-1 Example of Frame Rate Calculation

LCDCLK	PRES[3:0]	DIV[3:0]	Ratio	Duty	f_{frame}
1.00MHz	7	3	2432	1/8	51.4Hz
1.00MHz	8	3	4864	1/4	51.4Hz
1.00MHz	8	10	6656	1/3	50.1Hz
1.00MHz	9	3	9728	1/2	51.4Hz

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

1.00MHz	10	3	19456	static	51.4Hz

Note: in order to achieve low power consumption and high refresh rate, the frame frequency range must be within 40Hz to 100Hz.

17.4.2 Common Driver

17.4.2.1 COM Signal Bias

Bias is the voltage levels used to drive the LCD. Select COM signal bias by LCD_CTRL.BIAS[1:0], which can be configured as 1/2 bias, 1/3 bias, and 1/4 bias.

COM[n] is active at n phase, and COM pin is driven to V_{LCD} on odd frames and to V_{SS} on even frames. COM[n] is inactive in other phases, the signal amplitude is:

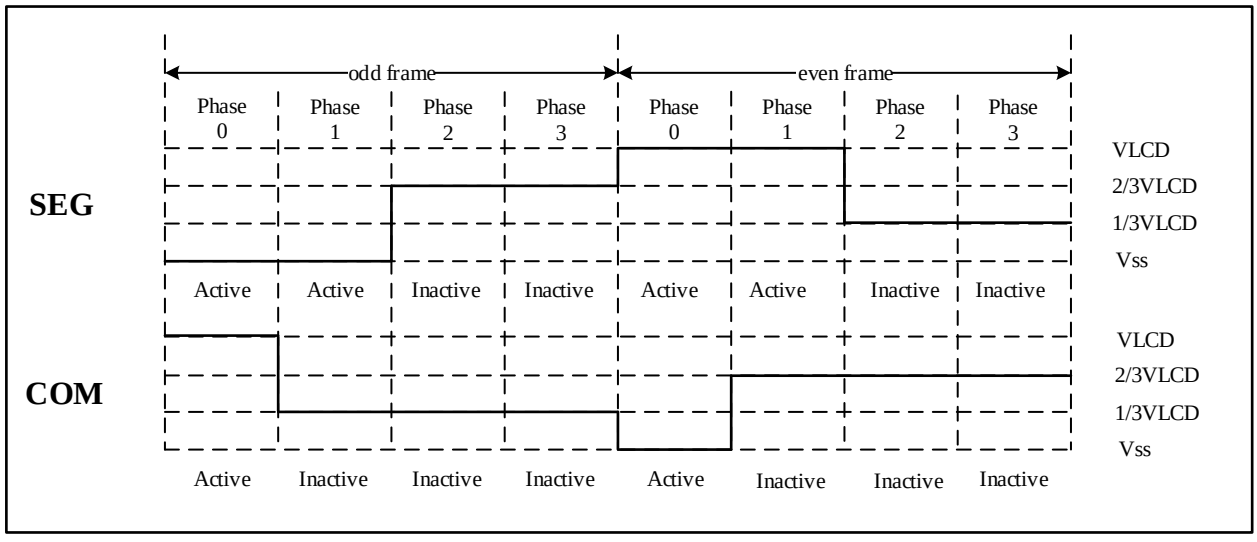
- COM pin is driven to 1/3 or 1/4 V_{LCD} on odd frames and to 2/3 or 3/4 V_{LCD} on even frames in case of 1/3 or 1/4 bias;
- COM pin is driven to 1/2 V_{LCD} on odd and even frames in case of 1/2 bias.

SEG[n] is active at n phase, and SEG pin is driven to V_{SS} on odd frames and to V_{LCD} on even frames. SEG[n] is inactive, the signal amplitude is:

- SEG pin is driven to 2/3 V_{LCD} on odd frames and to 1/3 V_{LCD} on even frames in case of 1/3 bias;
- SEG pin is driven to 1/2 V_{LCD} on odd and even frames in case of 1/4 bias;
- SEG pin is driven to V_{LCD} on odd frames and to V_{SS} on even frames in case of 1/2 bias;

A pixel is activated when both of its corresponding common and segment lines are active during the same phase: when the voltage difference between common and segment is maximum during this phase. Common signals are phase inverted in order to reduce EMI. As shown in the Figure 17-2 below, with phase inversion, there is a mean voltage of 1/2 V_{LCD} at the end of every odd cycle.

Figure 17-2 Odd-Even Frames Example(1/4 Duty Cycle, 1/3 Bias)



Note: This figure shows the state where COM0-SEG0 and COM1-SEG0 are conducting, while COM2-SEG0 and COM3-SEG0 are not conducting.

17.4.2.2 COM Signal Duty

Duty cycle is 1/(the number of common terminals on the LCD display). Select COM signal duty by

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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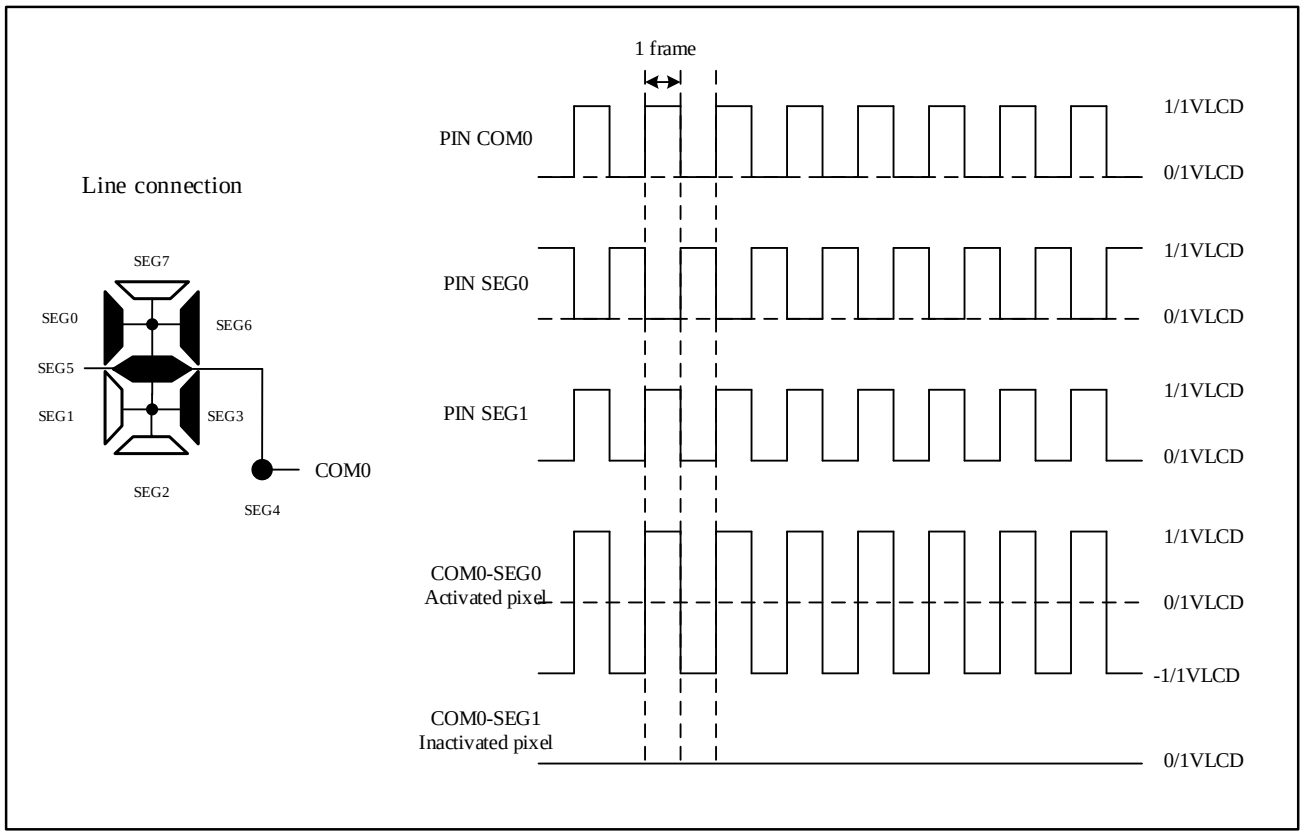
LCD_CTRL.DUTY[2:0], which can be configured as static duty, 1/2 duty, 1/3 duty, 1/4 duty, and 1/8 duty. For example, if 1/4 duty is selected with a total of four available COMs, there are four phases in a frame, where COM[0] is active during phase 0, COM[1] is active during phase 1, COM[2] is active during phase 2, and COM[3] is active during phase 3.

When static duty is selected, COM[0] is always active while COM[7:1] are not used and are driven to V_{SS}. Each frame has only one phase, so f_{frame} is equal to f_{LCD}. Static duty means that only two voltage levels are used for segment and common lines: V_{LCD} and $V_{SS.}$ A pixel is active if the corresponding SEG line has a voltage opposite to that of the COM, and inactive when the voltages are equal. In this way the LCD has maximum contrast (see Figure 17-3). In the figure below, pixel 0 is active while pixel 1 is inactive.

When the LCD_CTRL.LCDEN bit is disabled, all COM is pulled to V_{SS} and the LCD_STS.ENSTS flag becomes 0.

Figure 17-3 Example of Static Duty



17.4.2.3 Eight-to-one mux

When COM[0] is active the common driver block, it also drives the eight-to-one mux shown in Figure 17-1 in order to select the content of first two RAM register locations. When COM[7] is active, the output of the eight-to-one mux is the content of the last two RAM locations.

17.4.3 Segment Driver

If pixel n is active, the SEG[n] pin is driven to V_{SS} (indicating pixel n is active when COM[0] is active) in phase 0 of the odd frame; the SEG[n] pin is driven to V_{LCD} in phase 0 of the even frame.

If pixel n is inactive, the SEG[n] pin is driven to 2/3 (2/4) V_{LCD} in odd frames and to 1/3 (2/4) V_{LCD} in even frames. In case of 1/2 bias, if the pixel is inactive the SEG[n] pin is driven to V_{LCD} in odd frames and to V_{SS} in even frames.

When the LCD_CTRL.LCDEN bit is disabled, all SEG lines are pulled down to V_{SS}.

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Email：info@nationstech.com
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Below figure shows the waveform with different duty and bias.

Figure 17-4 1/2 Duty, 1/2 Bias

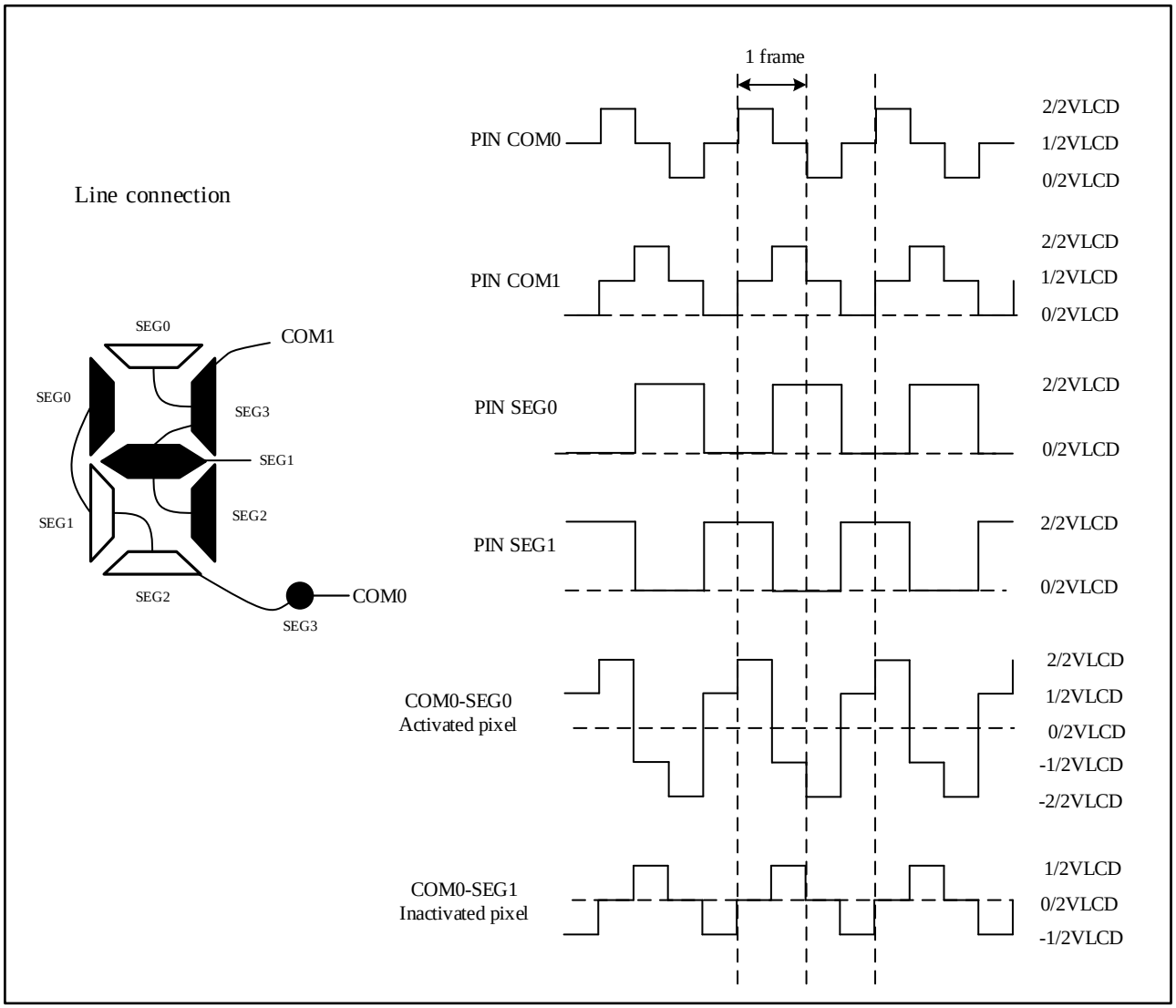

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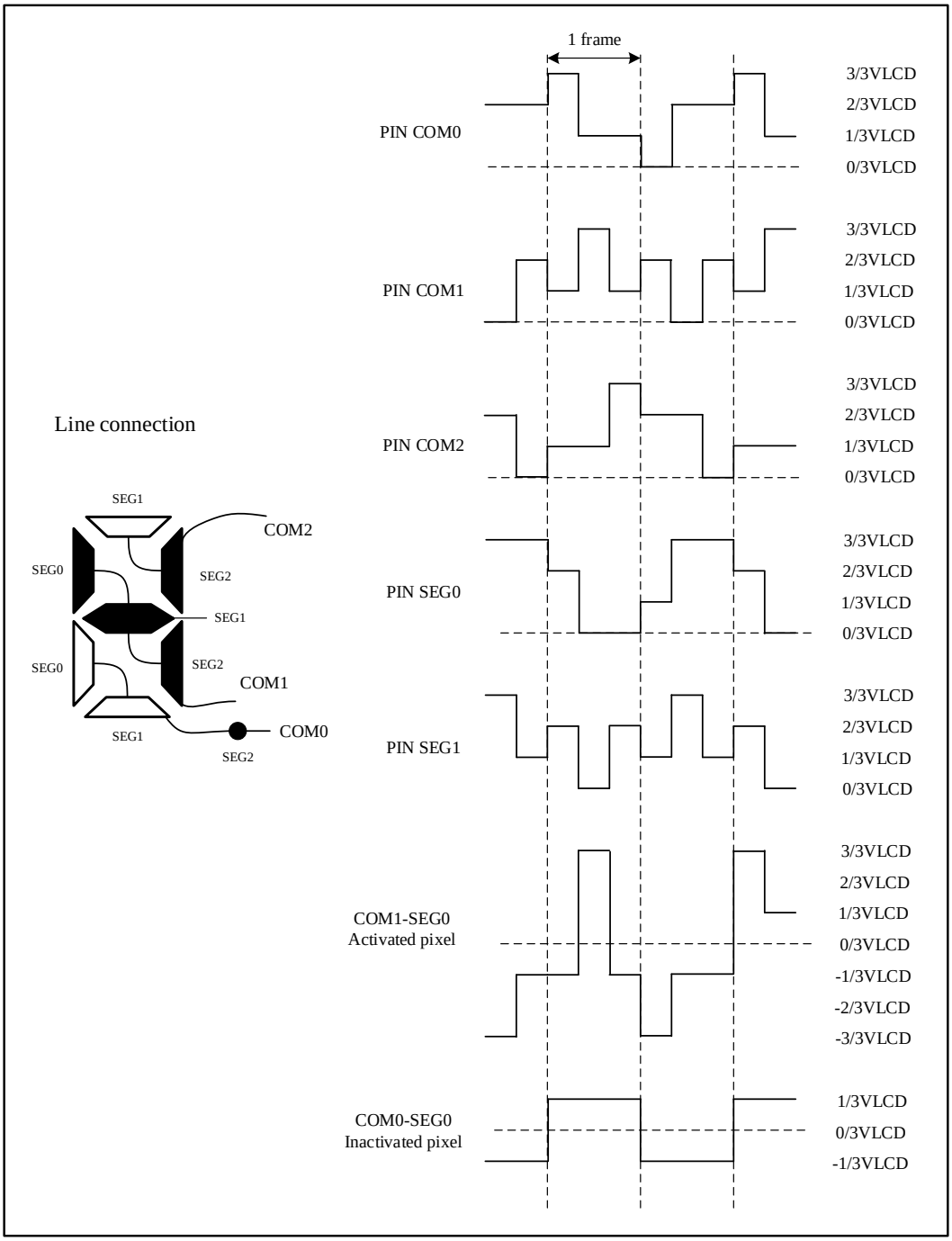
Figure 17-5 1/3 Duty, 1/3 Bias



Note: COM2-SEG0, which is not shown in the diagram, is in the conducting state.

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Figure 17-6 1/4 Duty, 1/3 Bias

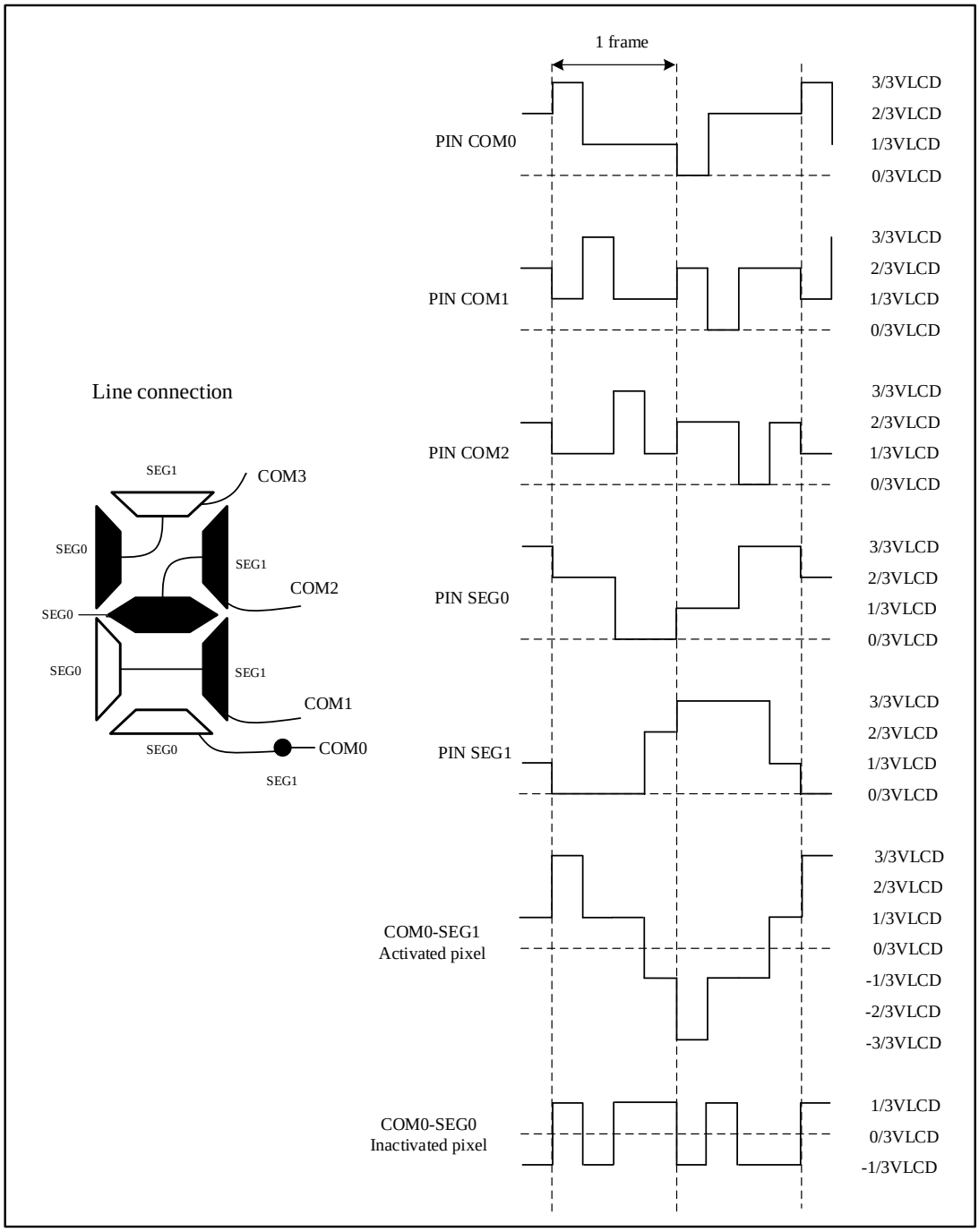

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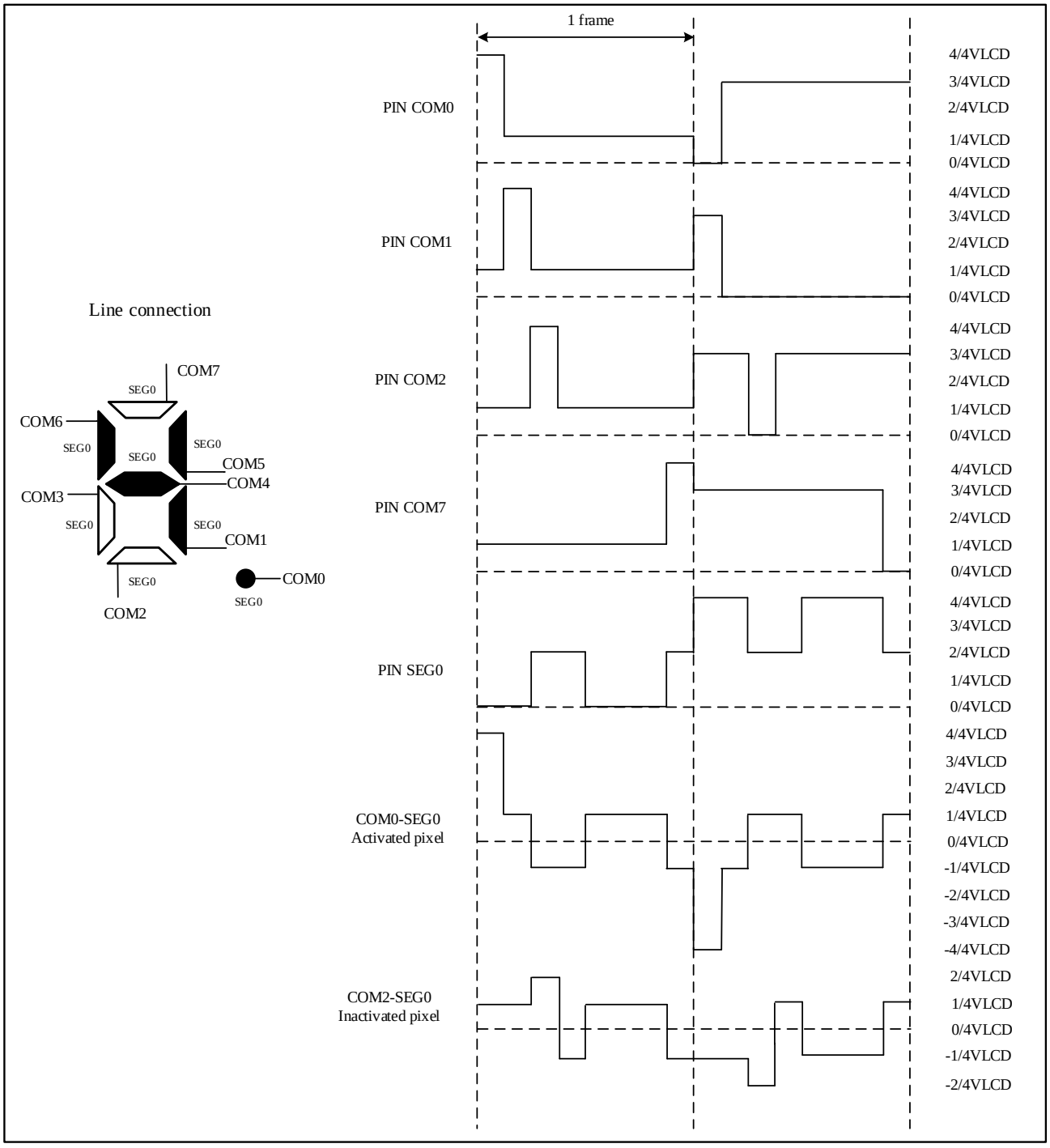
Figure 17-7 1/8 Duty, 1/4 Bias



17.4.3.1 Blink

The segment driver also implements a programmable blink feature to allow some pixels to continuously switch on at a specific frequency. The blink mode can be configured by LCD_FCTRL. BLINK[1:0], making possible to blink up to 1, 2, 3, 4, 8, or all pixels. The blink frequency is configured by using LCD_FCTRL.BLINKF[2:0] bits to divide the fck_div. Table 17-2 lists configuration examples of different blink frequencies.

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Table 17-2 Blink Frequency Configure Example

BLINKF[2:0]			ck_div			
			32Hz	64Hz	32Hz	256Hz
0	0	0	4.0Hz	N/A	N/A	N/A
0	0	1	2Hz	4.0Hz	N/A	N/A
0	1	0	1Hz	2Hz	4.0Hz	N/A
0	1	1	0.5Hz	1Hz	2Hz	4.0Hz
1	0	0	0.25Hz	0.5Hz	1Hz	2Hz
1	0	1	N/A	0.25Hz	0.5Hz	1Hz
1	1	0	N/A	N/A	0.25Hz	0.5Hz
1	1	1	N/A	N/A	N/A	0.25Hz

17.4.4 Voltage Generator and Contrast Control

17.4.4.1 Power Supply Selection

By configuring LCD_CTRL.VSEL, the LCD driver contrast control can be selected. When VSEL=1, adjustable contrast control VLCD is enabled, and the contrast can be controlled within the range of V_{LCDmin} (2.6V) to V_{LCDmax} (5.0V) using the LCD_FCTRL.CONTRAST[3:0] bits. The new value of VLCD takes effect at the beginning of a new frame. When VSEL=0, contrast control is disabled, and V_{LCD}=VDDA. In this case, contrast can be controlled by adjusting the inter-frame dead time.

17.4.4.2 Drive selection

The LCD voltage generator generates an intermediate voltage between V_{LCD} and V_{SS} through an internal resistor divider network, as shown inFigure 17-8.

Two resistive networks, one with low-value resistors (RL), and one with high-value resistors (RH) are respectively used to increase the current during transitions, and to reduce power consumption in static state.

- LCD_CTRL.LCDEN bit:

  If the LCD_CTRL.LCDEN bit is set, the LCDEN switch in the block diagram is closed. When clearing the LCD_CTRL.LCDEN bit, the LCDEN switch in the block diagram is opened at the end of the even frame in order to avoid a medium voltage level different from V_{SS} considering the entire the odd-even frame.

- LCD_FCTRL.PULSEON[2:0] bits:

  LCD_FCTRL.PULSEON[2:0] configures the time during which RL is enabled through the HDEN switch when the levels of the common and segment lines change. A short drive time leads to lower power consumption, but displays with high internal resistance may need a longer drive time to achieve satisfactory contrast.

- LCD_FCTRL.HDEN bit:

  If the LCD_FCTRL.HDEN bit and the LCD_FCTRL.PULSEON[2:0] bits are reset, the HDEN switch is opened.

  If the LCD_FCTRL.HDEN bit is reset and the LCD_FCTRL.PULSEON[2:0] bits are not 0, the HDEN switch is closed during the number of pulses defined in the LCD_FCTRL.PULSEON[2:0] bits.

  If the HDEN bit =1 in the LCD_FCTRL register, the HDEN switch is always closed.

R_{LN} and R_{HN} represent the resistor divider network for low-value resistor and high-value resistor respectively. R_{LN} divider can be always switched on using LCD_FCTRL.HDEN bit.

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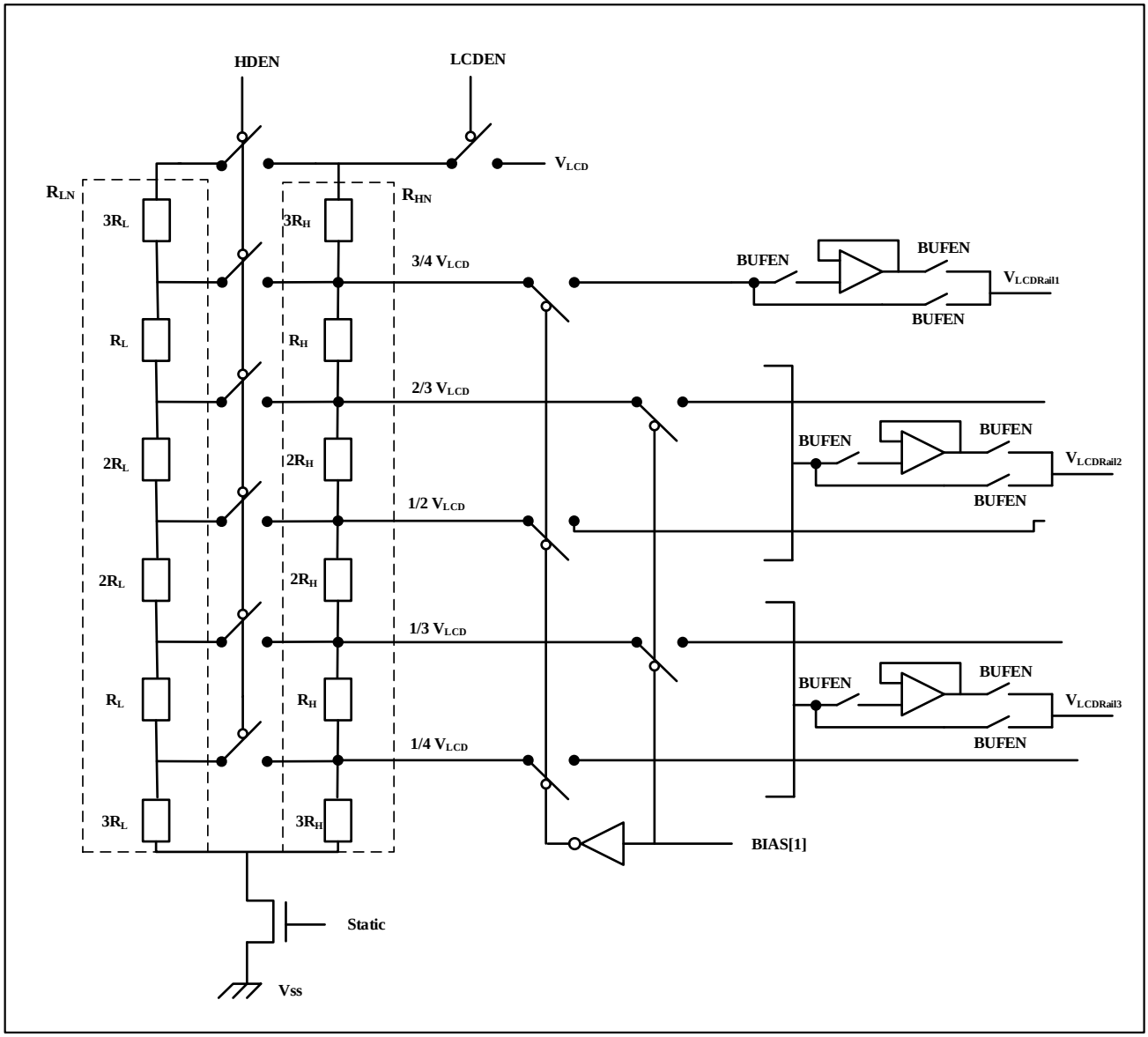
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Figure 17-8 LCD Drive Voltage Control



17.4.4.3 Voltage buffer mode

When voltage output buffers are enabled by setting LCD_CTRL.BUFEN bit (configured when LCD_CTRL.LCDEN is disabled), the high-value resistor network R_{HN} generates intermediate voltages to reduce power consumption, and the low-value resistor network R_{LN} is automatically disabled (whatever the configuration of LCD_FCTRL.HDEN bit or LCD_FCTRL.PULSEON bit). After the LCD_CTRL.LCDEN bit is set, the LCD_STS.RDY bit is automatically set after the voltage level stabilizes, and the LCD controller starts to work.

The LCD driving capability is improved as buffers prevents the LCD capacitive loads from directly loading the resistor network and interfering with its voltage generation.

17.4.4.4 Dead time

The contrast can be controlled by programming a dead time through the LCD_FCTR.DEAD[2:0] bits between each frame. COM and SEG ports are put to V_{SS} during dead time.

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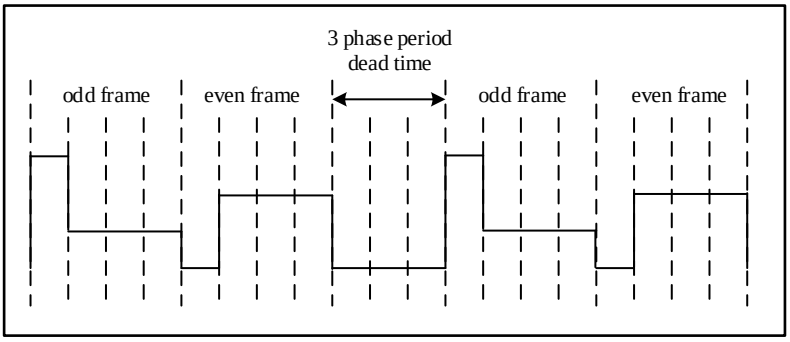
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Figure 17-9 Dead Time



17.4.5 Double-buffer Memory

The LCD controller has a built-in double-buffer memory to ensure the coherency of displayed information without having to use interrupts to control the LCD_RAM modification. The application software can access the first buffer level (LCD_RAM registers) through the APB interface. Once the software has modified the LCD_RAM registers, it sets the LCD_STS.UDR flag, and then the updated information to be moved into the second buffer level (LCD_DISPLAY) by hardware. This operation is done synchronously with the frame (at the beginning of the next frame). Until the update is completed, the LCD_RAM registers are write protected, and the LCD_STS.UDR flag stays high. Once the update is completed, another flag (LCD_STS.UDD, update display done) is set and generates an interrupt if LCD_FCTR.UDDIE is set. In the worst case, the time it takes to update LCD_DISPLAY is two frames. The update does not occur (LCD_STS.UDR =1 and LCD_STS.UDD = 0) until the display is enabled (LCD_CTRL.LCDEN = 1).

17.4.6 COM And SEG Multiplexing

All output pins include: SEG[36:0] and COM[2:0].

Depending on the duty configuration (LCD_CTRL.DUTY[2:0]), the COM and SEG output pins can have different functions:

The number of SEG pins is automatically selected by configuring LCD_CTRL.DUTY[2:0]. In static, 1/2, and 1/3 duty modes, there are up to 37 SEG pins and respectively 1, 2 and 3 COM pins. In 1/4 duty mode, there are up to 36 SEG pins and SEG[36] can be used as COM[3]; in 1/8 duty cycle mode, there are up to 32 SEG pins and SEG[36:32] can be used as COM[3:7].

All the possible ways of multiplexing the COM and SEG functions with duty and pin remapping configuration are described in the Table 17-3.

Table 17-3 COM and SEG Pins Mapping Table

DUTY	SEG × COM	MCU Output Pins	LCD Module Function
1/8	32×8	SEG[32]/COM[7]	COM[7]
		SEG[33]/COM[6]	COM[6]
		SEG[34]/COM[5]	COM[5]
		SEG[35]/COM[4]	COM[4]
		SEG[36]/COM[3]	COM[3]
		COM[2:0]	COM[2:0]
		SEG[31:0]	SEG[31:0]
1/4	36×4	SEG[32]/COM[7]	SEG[32]

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

DUTY	SEG × COM	MCU Output Pins	LCD Module Function
		SEG[33]/COM[6]	SEG[33]
		SEG[34]/COM[5]	SEG[34]
		SEG[35]/COM[4]	SEG[35]
		SEG[36]/COM[3]	COM[3]
		COM[2:0]	COM[2:0]
		SEG[31:0]	SEG[31:0]
1/3	37×3	SEG[32]/COM[7]	SEG[32]
		SEG[33]/COM[6]	SEG[33]
		SEG[34]/COM[5]	SEG[34]
		SEG[35]/COM[4]	SEG[35]
		SEG[36]/COM[3]	SEG[36]
		COM[2:0]	COM[2:0]
		SEG[31:0]	SEG[31:0]
1/2	37×2	SEG[32]/COM[7]	SEG[32]
		SEG[33]/COM[6]	SEG[33]
		SEG[34]/COM[5]	SEG[34]
		SEG[35]/COM[4]	SEG[35]
		SEG[36]/COM[3]	SEG[36]
		COM[2]	Not used
		COM[1:0]	COM[1:0]
		SEG[31:0]	SEG[31:0]
STATIC	37×1	SEG[32]/COM[7]	SEG[32]
		SEG[33]/COM[6]	SEG[33]
		SEG[34]/COM[5]	SEG[34]
		SEG[35]/COM[4]	SEG[35]
		SEG[36]/COM[3]	SEG[36]
		COM[2:1]	Not used
		COM[0]	COM[0]
		SEG[31:0]	SEG[31:0]

17.5 Working Process

LCD controller workflow is as follows:

1. Configure LCD module parameters, clock source, COM/SEG port;
2. Write the default data to LCD_RAM, and set LCD_STS.UDR by software;
3. After configuring the frame frequency and contrast, set LCD_CTRL.LCDEN to enable the LCD module;
4. If you need to adjust the contrast, you can modify LCD_FCTRL.PRES[3:0], LCD_FCTRL.DIV[3:0], LCD_FCTRL.CONTRAST[3:0], LCD_FCTRL.PULSEON[2:0], LCD_FCTRL.DEAD[2:0] or LCD_FCTRL.HDEN;
5. If you want to modify the display data, you should first check the LCD_STS.UDR flag. If LCD_STS.UDR = 1, you need to wait. If LCD_STS.UDR = 0, you can update the data into LCD_RAM registers, and then set LCD_STS.UDR

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

by software. Once LCD_STS.UDR is set, there needs to be an interval of several fck_div cycles before the next setting. The number of cycles in this interval depends on the number of COMs used, which is related to the configuration of LCD_CTRL.DUTY[2:0]. For detailed information, please refer to the table below.

6. If you wantto changethe blinking pixel and frequency, you can modify LCD_FCTRL.BLINK[1:0] and LCD_FCTRL.BLINKF[2:0].

Table 17-4 Number of Interval Cycles

The configuration of LCD_CTRL.DUTY[2:0]	Number of Interval Cycles
000: static	4
001: 1/2 duty	2
010: 1/3 duty	3
011: 1/4 duty	4
100: 1/8 duty	8

17.6 Interrupt Request

LCD interrupt request is as follows:

Table 17-5 LCD Interrupt Request

Interrupt Event	Event Flag	Interrupt Enable Control Bit	Event Flag Interrupt Clearing Method
Start of frame	LCD_STS.SOF	LCD_FCTRL.SOFIE	Write LCD_CLR.SOFCLR = 1
Update display done	LCD_STS.UDD	LCD_FCTRL.UDDIE	Write LCD_CLR.UDDCLR = 1

17.7 LCD Controller Registers

LCD registers must be read and written by 32 bits

17.7.1 LCD Controller Register Overview

Table 17-6 LCD Controller Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	LCD_CTRL	Reserved																							BUFEN	Reserved	BIAS[1:0]		DUTY[2:0]			VSEL	LCDEN
	Reset Value																								0		0	0	0	0	0	0	0
004h	LCD_FCTRL	Reserved					PRES[3:0]				DIV[3:0]				BLINK [1:0]		BLINKF[2:0]			CONTRAST[3:0]				DEAD[2:0]			PULSEON[2:0]			UDDIE	Reserved	SOFIE	HDEN
	Reset Value						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
008h	LCD_STS	Reserved																											FCRSF	RDY	UDD	UDR	SOF	ENSTS
	Reset Value																												0	0	0	0	0	0
00Ch	LCD_CLR	Reserved																													UDDCLR	Reserved	SOFCLR	Reserved
	Reset Value																													0		0	
014h	LCD_RAM1_COM0	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Nations Technologies Inc.
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LCD_RAM2_COM0	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
01Ch	LCD_RAM1_COM1	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	LCD_RAM2_COM1	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
024h	LCD_RAM1_COM2	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	LCD_RAM2_COM2	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
02Ch	LCD_RAM1_COM3	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	LCD_RAM2_COM3	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
034h	LCD_RAM1_COM4	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	LCD_RAM2_COM4	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
03Ch	LCD_RAM1_COM5	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	LCD_RAM2_COM5	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
044h	LCD_RAM1_COM6	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	LCD_RAM2_COM6	Reserved																										S36	S35	S34	S33	S32	
	Reset Value																											0	0	0	0	0	
04Ch	LCD_RAM1_COM7	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	LCD_RAM2_COM7	Reserved																														S36	S35	S34	S33	S32
	Reset Value																															0	0	0	0	0

17.7.2 LCD Control Register (LCD_CTRL)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							BUFEN	Reserved	BIAS[1:0]		DUTY[2:0]			VSEL	EN
							rw		rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	BUFEN	Voltage output buffer enable This bit is used to enable/disable the voltage output buffer for higher driving capability. 0: Output buffer disabled 1: Output buffer enabled
7	Reserved	Reserved, the reset value must be maintained.
6:5	BIAS[1:0]	Bias selector These bits determine the bias used. Value 11 is forbidden. 00: Bias 1/4 01: Bias 1/2 10: Bias 1/3 11: Reserved
4:2	DUTY[2:0]	Duty selection These bits determine the duty cycle. Values 101, 110 and 111 are forbidden. 000: Static duty 001: 1/2 duty 010: 1/3 duty 011: 1/4 duty 100: 1/8 duty Others: Reserved
1	VSEL	LCD contrast control 0: Disable contrast control, VLCD=VDDA 1: Enable contrast control, VLCD adjustable
0	LCDEN	LCD controller enable

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		This bit is set/reset by software to enable/disable the LCD controller/driver. It is cleared by software to turn off the LCD at the beginning of the next frame. When the LCD is disabled, all COM and SEG pins are driven to VSS. 0: LCD controller disabled 1: LCD controller enabled

Note: LCD_CTRL.VSEL, LCD_CTRL.DUTY, LCD_CTRL.BIAS and LCD_CTRL.BUFEN are write protected after LCD_CTRL.LCDEN is enabled. If you want to modify these bits, you must disable the LCD controller first.

17.7.3 LCD Frame Control Register (LCD_FCTRL)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					PRES[3:0]				DIV[3:0]				BLINK[1:0]		BLINKF[2]
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLINKF[1:0]		CONTRAST[3:0]			DEAD[2:0]				PULSEON[2:0]			UDDIE	Reserved	SOFIE	HDEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

Bit Field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:23	PRES[3:0]	16-bit prescaler ck_pres = LCDCLK/2^n. 0000: ck_pres = LCDCLK 0001: ck_pres = LCDCLK/2 0002: ck_pres = LCDCLK/4 ... 1111: ck_pres = LCDCLK/32768
22:19	DIV[3:0]	DIV clock divider ck_div = ck_pres/(16+n) 0000: ck_div = ck_pres/16 0001: ck_div = ck_pres/17 0002: ck_div = ck_pres/18 ... 1111: ck_div = ck_pres/31
18:17	BLINK[1:0]	Blink mode selection 00: Blink disabled 01: Blink enabled on SEG[0], COM[0] (1 pixel) 10: Blink enabled on SEG[0], all COMs (up to 8 pixels depending on the programmed duty) 11: Blink enabled on all SEGs and all COMs (all pixels)

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
16:14	BLINKF[2:0]	Blink frequency selection 000: ck_div/8 001: ck_div/16 010: ck_div/32 011: ck_div/64 100: ck_div/128 101: ck_div/256 110: ck_div/512 111: ck_div/1024
13:10	CONTRAST[3:0]	Contrast control These bits specify one of the VLCD maximum voltages (independent of VDD). It ranges from 2.60 V to 5.0V. When LCD_FCTRL.HDEN = 0: 0000: VLCD = VDD*1.00 0001: VLCD = VDD*0.97 0010: VLCD = VDD*0.94 0011: VLCD = VDD*0.90 0100: VLCD = VDD*0.87 0101: VLCD = VDD*0.84 0110: VLCD = VDD*0.80 0111: VLCD = VDD*0.77 1000: VLCD = VDD*0.74 1001: VLCD = VDD*0.70 1010: VLCD = VDD*0.67 1011: VLCD = VDD*0.64 1100: VLCD = VDD*0.61 1101: VLCD = VDD*0.58 1110: VLCD = VDD*0.54 1111: VLCD = VDD*0.50 When LCD_FCTRL.HDEN = 1: 0000: VLCD = VDD*1.00 0001: VLCD = VDD*0.96 0010: VLCD = VDD*0.92 0011: VLCD = VDD*0.88 0100: VLCD = VDD*0.84 0101: VLCD = VDD*0.80 0110: VLCD = VDD*0.76 0111: VLCD = VDD*0.73 1000: VLCD = VDD*0.70 1001: VLCD = VDD*0.66 1010: VLCD = VDD*0.63 1011: VLCD = VDD*0.60 1100: VLCD = VDD*0.57

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1101: VLCD = VDD*0.53 1110: VLCD = VDD*0.50 1111: VLCD = VDD*0.47
9:7	DEAD[2:0]	Dead time duration These bits are written by software to configure the length of the dead time between frames. During the dead time the COM and SEG voltage levels are held at 0 V to reduce the contrast without modifying the frame rate. 000: No dead time 001: 1 phase period dead time 010: 2 phase period dead time 011: 3 phase period dead time 100: 4 phase period dead time 101: 5 phase period dead time 110: 6 phase period dead time 111: 7 phase period dead time
6:4	PULSEON[2:0]	Pulse on duration These bits are written by software to define the pulse duration in terms of ck_pres pulses. 000: 0 001: 1/ck_pres 010: 2/ck_pres 011: 3/ck_pres 100: 4/ck_pres 101: 5/ck_pres 110: 6/ck_pres 111: 7/ck_pres *Note: that the pulse is never longer than one half prescaled LCD clock period.*
3	UDDIE	Update display done interrupt enable This bit is set and cleared by software. 0: LCD update display done interrupt disabled 1: LCD update display done interrupt enabled
2	Reserved	Reserved, the reset value must be maintained.
1	SOFIE	Start of frame interrupt enable This bit is set and cleared by software. 0: LCD start-of-frame interrupt disabled 1: LCD start-of-frame interrupt enabled
0	HDEN	High drive enable This bit is written by software to enable a low resistance divider. 0: Permanent high drive disabled 1: Permanent high drive enabled. *Note: When HDEN = 1, LCD_FCTRL.PULSEON[2:0] must be programmed to 001.*

Note: the LCD_FCTRL register can be modified at any time, and the new configuration takes effect at the start of the next frame (except for the LCD_FCTRL.UDDIE and LCD_FCTRL.SOFIE bits, which take effect immediately after

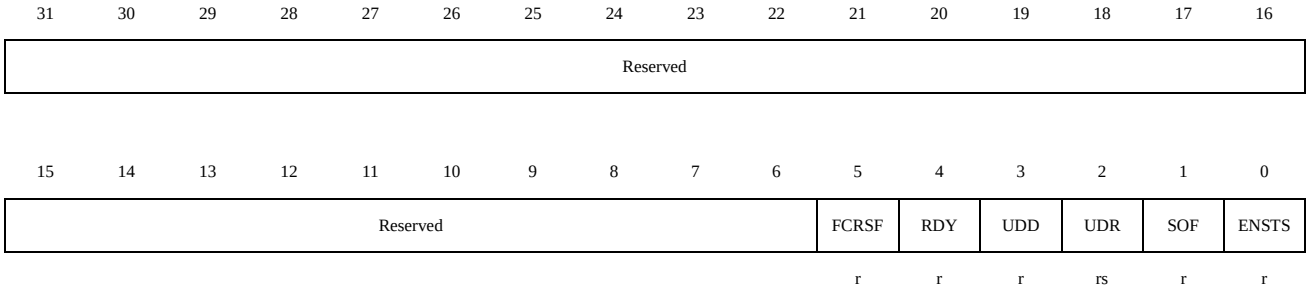
Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

modification). When LCD_CTRL.BUFEN is 1, the low resistance network is automatically disabled, and LCD_FCTRL.HDEN and LCD_FCTRL.PULSEON configurations are ignored.

17.7.4 LCD Status Register (LCD_STS)

Address offset: 0x08

Reset value: 0x0000 0020



Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	FCRSF	LCD frame control register synchronization flag This bit is set by hardware each time the LCD_FCTRL register is updated in the LCDCLK domain. It is cleared by hardware when writing to the LCD_FCR register. 0: LCD frame control register not yet synchronized 1: LCD frame control register synchronized
4	RDY	Ready flag This bit is set and cleared by hardware. It indicates the status of the stepup converter. 0: Not ready 1: Stepup converter enabled and ready to provide the correct voltage
3	UDD	Update display done This bit is set by hardware. It is cleared by writing 1 to LCD_CLR.UDDCLR. The bit set has priority over the clear. A UDD interrupt is generated if UDDIE = 1 in LCD_FCTRL. 0: No event 1: Update display request done.
2	UDR	Update display request Each time software modifies the LCD_RAM, it must set this bit to transfer the updated data to the second level buffer. 0: No effect 1: Update display request
1	SOF	Start-of-frame flag This bit is set by hardware at the beginning of a new frame. It is cleared by writing a 1 to LCD_CLR.SOFCLR. The bit clear has priority over the set. An LCD SOF interrupt is generated if LCD_FCTRL.SOFIE is set. 0: No event 1: Start-of-frame event occurred.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
0	ENSTS	LCD enabled status This bit is set and cleared by hardware. It indicates the LCD controller status. 0: LCD controller disabled 1: LCD controller enabled

17.7.5 LCD Clear Register (LCD_CLR)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												UDDCLR	Reserved	SOFCLR	Reserved
												w		w	

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	UDDCLR	Update display done clear 0: No effect on LCD_STS.UDD flag 1: Clear LCD_STS.UDD flag. Note: This bit should be manually cleared after set, otherwise, the LCD_STS.UDD bit will remain cleared to 0.
2	Reserved	Reserved, the reset value must be maintained.
1	SOFCLR	Start-of-frame flag clear 0: No effect on LCD_STS.SOF 1: Clear LCD_STS.SOF flag.
0	Reserved	Reserved, the reset value must be maintained.

17.7.6 LCD Display Memory Register (LCD_RAM1_Comx X = 0...7)

Address offset: 0x14 + x*8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:0	Sy	Display memory LCD_RAM1_COMx (x = 0…7) pixel bit (y = 0…31), each bit corresponds to one pixel of the LCD display. 0: Pixel inactive 1: Pixel active

17.7.7 LCD Display Memory Register (LCD_RAM2_Comx X = 0...7)

Offset address: 0x18 + x*8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											S36	S35	S34	S33	S32
											rw	rw	rw	rw	rw

Bit Field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4:0	Sy	Display memory LCD_RAM2_COMx (x = 0…7) pixel bit (y = 0…4), each bit corresponds to one pixel of the LCD display. 0: Pixel inactive 1: Pixel active

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

18 Light Emitting Diode (LED) Driver

18.1 Introduction

The LED is a constant current driver, supporting a maximum of 10 COM output pins and 16 SEG output pins. Each COM port can support a maximum of 8 SEGs conducting simultaneously, with each SEG supporting a constant current regulation of up to 20mA. The current regulation duty cycle ranges from 1/1 to 1/64.

18.2 Main Features

- Supports 10 x COM, 16 x SEG
- Each COM port can support a maximum of 8 SEGs conducting simultaneously, with a maximum output current of 160mA
- Supports 0.5ms, 1ms, 2ms switching for COM scanning
- COM circuit features ghosting function
- Each SEG port supports configurable 5~20mA constant current input
- Each SEG channel can be selected to operate
- Each pixel port can support 64-step PWM current adjustment
- Operating voltage range of 4.5V ~ 5.5V
- Supports SPI four-wire communication, with a maximum data transfer rate of 3MHz

18.3 LED Funtion Description and Operation Instructions

18.3.1 Control Interface

Supports 4-wire SPI slave control, including SPI_CS, SPI_CLK, SPI_MOSI, SPI_MISO, defaulting to low level in idle state; SPI_CS defaults to high level in idle state;

1. The MCU acts as the host, sending commands in “host unidirectional transmission mode”, while the LED acts as the slave, receiving commands in “slave unidirectional reception mode”;
2. The MCU acts as the host, entering the “host unidirectional reception mode” for status read back, while the LED acts as the slave, entering the “slave unidirectional transmission mode” for sending status;
3. LED SPI Interface:
    1) Clock Polarity: When idle, SCLK remains at a low level;
    2) Clock Phase: Data sampling starts from the first clock edge;
    3) Chip Select CS: When idle, CS remains at a high level; when CS is pulled low, the LED recognizes SPI_CLK; when CS is pulled high, the LED ignores SPI_CLK;

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

4) When the MCU is in the receiving state, data is sampled at the first edge, that is, data is sampled on the rising edge;

5) 16-bit data frame format, with the frame format as MSB;

6) When COM is switched, the LED SPI interface resets the sampling, reception, and shifting.

Note: When using the LED function, the chip internally defaults to using the SPI3 interface.

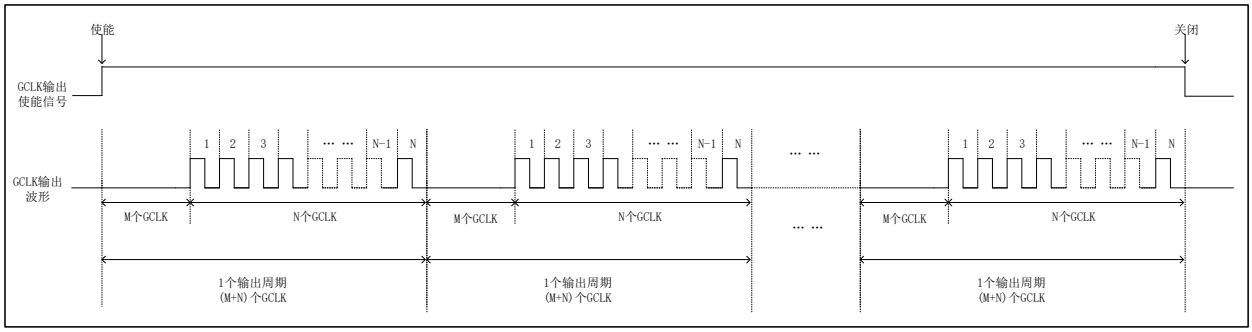
18.3.2 Clock Control

GCLK is the clock used by the LED for SEG duty cycle control and COM scanning switching.

GCLK is controlled by the MCU and output through PAD, with an output range of 50 KHz~250 KHz, typically 100 KHz.

M (number of clock cycles at low level, configured as 8 bits) + N (number of clock cycles for Clock signal, configured as 8 bits, typically 130); Formula for the time required to scan one COM: (M + N) / Ft = 1ms; (Ft is the GCLK output frequency, in KHz).

Figure 18-1 Timing Diagram of GCLK



18.3.3 Communication Protocol Format Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	*0*	*One-level command*		*Two-level command*				*DATA*							

Notes:

1. *BIT15、BIT14 represent the command header, fixed as 1b，0b ；*
2. *BIT13、BIT12 represent the One-level command, with a total of four One-level command types, as shown in the table below；*
3. *BIT11~BIT8 represent the Two-level command, ranging from 0000b to 1111b, as shown in the table；*
4. *BIT7~BIT0 represent the data field of the issued command；*

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

18.3.3.1 One-level Command Types

One-level Command Types	**Command Field Bit[13:12]**	**Description**
Basic Command	00b	This includes the following command set: "COM Forced Shutdown", "COM Scan Reset", "COM Scan Enable", "Read LED Registers", "Chip Wake-up".
Fine-tuning Command	01b	This includes the following command set: "Write SEG Fine-tuning Register", "Write RSET Fine-tuning Register", "Write BG Fine-tuning Register"
Global Command	10b	This includes the following command set: "Set SEG Operating Current & SEG Display Mode & Chip Enable/Disable", "Set the number of used COMs & the operating status of COM0~1", "Set the operating status of COM2~9", "Set the operating status of SEG0~7", "Set the operating status of SEG8~15"
Set SEG Duty Cycle Command	11b	This includes the following command set: "Set Duty Cycle of SEG0", "Set Duty Cycle of SEG1", …… "Set Duty Cycle of SEG15"

18.3.3.2 Two-level Command Types

Two-level Command Type	**Command Field Bit[15:8]**	**Description of Command Data Field Bit[7:0]**
COM Forced Shutdown	0x80	Data bits BIT[7:0]=0x00 (reserved as 0)； Function Description: 1. Force COM scan display to stop and state machine returns to the initialization state, COM-IO & SEG-IO remain in tri-state, internal analog power is turned off; 2. Registers that change: “Current scanning COM register”: BIT[3:0] becomes 0x0F, BIT[7:4] remains at 0; “SEG operating current & SEG display mode & Chip Enable/Disable”: BIT[7] becomes 0, in Disable state; 3. Configurations remain unchanged: “Fine-tuning related registers”: 8 remain unchanged; “Number of used COMs & operating status register of COM0-1”: unchanged; “Operating status register of COM2-9”: unchanged; “SEG operating current & SEG display mode & Chip Enable/Disable”: BIT[6:0] unchanged; “Operating status register of SEG0~7”: unchanged; “Operating status register of SEG8~15”: unchanged; “Duty cycle of SEG0~15”: unchanged; 4. After the COM forced shutdown, when reading the “Current scanning COM

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

		register", the return value is 0x0F;
COM Scan Reset	0x81	Data bits BIT[7:0]=0x00 (reserved as 0); Function Description: 1. The state machine of COM scan returns to the initialization state; that is, it returns to COM0 and pauses the COM scan. When GCLK is sent again, the display can be directly activated; 2. Changes in registers include: "The Current scanning COM register: BIT[3:0] becomes 0x0F, BIT[7:4] remains at 0; 3. The following registers retain their values from before the COM scan reset: "The Fine-tuning related registers": 8 remain unchanged; "The Number of used COMs & operating status register of COM0-1": unchanged; "The operating status register of COM2-9": unchanged; "The SEG operating current & SEG display mode & Chip Enable/Disable": unchanged; "The operating status register of SEG0~7": unchanged; "The operating status register of SEG8~15": unchanged; "Duty cycle of SEG0~15" : unchanged; 4. the internal analog power is turned on; 5. COM-IO & SEG-IO remain in normal operating state; 6. After the COM scan reset is completed, when reading the "Current scanning COM register", the return value is 0x0F, indicating that it is currently in the default state;
COM Scan Enable	0x82	Data bits BIT[7:0]=0x00 (reserved as 0); Function Description: 1. COM-IO & SEG-IO are automatically configured as "LED operating state" or "tri-state" based on the parameters set; 2. Configure the "Current scanning COM register": BIT[3:0] configured as 0, indicating scanning from COM0, BIT[7:4]: reserved value of 0; 3. The COM scan display is activated, starting the scan from COM0, and waiting to receive GCLK to begin displaying; 4. This command will actively trigger the transfer of LED data from the secondary cache to the primary cache once;
Read LED Registers	0x83	The MCU reads back the LED register status in two steps:

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

1. The SPI sends the “Read LED Register Instruction” command to the LED;

Data bits BIT[7:0] represent the index of the “LED Register Instruction Set” sent by the MCU to the LED, as shown in the table below:

bit[7:4]	bit[3:0]	LED Register Instruction
xx01b	0000b~0101b	Read Back SEG Fine-tuning Register Data
	0110b	Read Back RSET Fine-tuning Register Data
	0111b	Read Back BG Fine-tuning Register Data
xx10b	0000b	SEG operating current & SEG display mode & Chip Enable/Disable
	0001b	Number of used COMs & operating status register of COM0-1
	0010b	Operating status register of COM2-9
	0011b	Operating status register of SEG0~7
	0100b	Operating status register of SEG8~15
	0111b	Current scanning COM register
xx11b	0000b	Duty cycle of SEG0
	0001b	Duty cycle of SEG1
	……	……
	1111b	Duty cycle of SEG15

2. The MCU sends all 0s 16-bit data to the LED via SPI, in order to read the corresponding LED register status bit. The specific meanings of the returned status bits are as follows:

LED register instruction	**BIT[15:8]:** The valid instruction is fixed as “0x83”; **BIT[7:0]:** The meaning is as described below
Read Back BG Fine-tuning Register Data	The read-back value remains consistent with the written value

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

		Read Back RSET Fine-tuning Register Data	The read-back value remains consistent with the written value
		Read Back SEG Fine-tuning Register Data	The read-back value remains consistent with the written value
		SEG operating current & SEG display mode & Chip Enable/Disable	BIT[7]: Indicates whether the chip is in an enabled state. When BIT[7] is 0, it indicates that the chip is disabled. When BIT[7] is 1, it indicates that the chip is enabled; BIT[6]: Indicates the SEG display mode: When BIT[6] is 0, it indicates that SEG completes the display of SEG0~7 in the first 0.5ms and SEG8~15 in the next 0.5ms. When BIT[6] is 1, it indicates that SEG completes the display of SEG0~15 in 1ms. The default value of BIT[6] is 0; BIT[5]: Reserved value is 1; BIT[4:0]: indicates the setting of the SEG shared current value. BIT[4:0] = N represents (0.5*N + 5) mA (N = 0~30, N is a positive integer, stepping 0.5mA). When BIT[4:0] = 0, it represents 5mA; BIT[4:0] = 1, it represents 5.5mA; BIT[4:0] = 30, it represents 20mA;
		Number of used COMs & operating status register of COM0-1	BIT[7:6]: Indicates the number of used COMs for COM1~0 1, The data BIT[3:0] indicates the number of used COMs from COM0 to COM9. For example, BIT[3:0] = 3: indicates the use of COM0 to COM2; BIT[3:0] = 0: indicates that COM is not used; BIT[3:0] = 1: indicates the use of COM0, a total of 1 COM; BIT[3:0] = 0xA: indicates the use of COM0 to COM9, a total of 10 COMs; BIT[3:0] = 0xB~0xF are invalid and reserved; the used COM-IO is in “LED operating state”, and the unused COM-IO is in “tri-state” 2, BIT[7:6] respectively indicate the conductivity status of COM1 and COM0; where BIT[7] corresponds to COM1, and BIT[6] corresponds to COM0; (when the data bit is 1, it represents that the corresponding COM is in the selected “LED operating state”; when the data bit is 0, it represents that the corresponding COM is in the unselected “tri-state”)
		Operating status register of	BIT[7:0] respectively indicate the conductivity status of COM9-2, where BIT[0] corresponds to COM2, BIT[1] corresponds to

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Tel：+86-755-86309900
Email：info@nationstech.com
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		COM2-9	COM3, BIT[2] corresponds to COM4, BIT[3] corresponds to COM5, BIT[4] corresponds to COM6, BIT[5] corresponds to COM7, BIT[6] corresponds to COM8, BIT[7] corresponds to COM9 (when the data bit is 1, it represents that the corresponding COM is in the selected “LED operating state”; when the data bit is 0, it represents that the corresponding COM is in the unselected “tri-state”)
		Operating status register of SEG0~7	BIT[7:0]: BIT7~BIT0 respectively correspond to SGE7~SGE0. When the data bit is 1, it represents that the corresponding SEG is in the selected “operating state”; when the data bit is 0, it represents that the corresponding SEG is in the unselected “tri-state”. For example, if BIT[7:0] = 0x11, it indicates that SEG0 and SEG4 are in the selected operating state, while the other SEGs are in the unselected “tri-state”.
		Operating status register of SEG8~15	BIT[7:0]: BIT7~BIT0 respectively correspond to SGE15~SGE8. When the data bit is 1, it represents that the corresponding SEG is in the selected “operating state”; when the data bit is 0, it represents that the corresponding SEG is in the unselected “tri-state”. For example, if BIT[7:0] = 0x44, it indicates that SEG9 and SEG14 are in the selected operating state, while the other SEGs are in the unselected “tri-state”.
		Current scanning COM register	BIT[7:4]: Reserved value is 0; BIT[3:0]: The value corresponds to the currently scanning COM0~COM9; BIT[3:0]=0000b ~1001b, it is valid, 0x0F indicates the current shutdown state, other values are invalid; BIT[3:0] = 0x0F: indicates that COM is in the shutdown state or the chip is disabled; BIT[3:0] = N indicates that COM(N) is currently being scanned, where N is a positive integer from 0 to 9; Note: Before reading this data, the COM scan must be enabled, the corresponding “0x8200” command must be sent.
		Duty cycle of SEG0	BIT[7:6]: Reserved value is 0; BIT[5:0]: Represents the duty cycle parameter of SEG0; BIT[5:0] = N (where N=0~63, N is a positive integer), represents the duty cycle of SEG0 as N/63, where $63=2^6-1$; for example, BIT[5:0] = 24, represents the duty cycle of SEG0 as 24/63; for example, BIT[5:0] = 0, represents the duty cycle of SEG0 as 0/63;

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

<table>
<tr><td></td><td></td><td><table>
<tr><td></td><td>Note: Before reading this data, the COM scan must be enabled, the corresponding “0x8200” command must be sent;</td></tr>
<tr><td>Duty cycle of SEG1</td><td>The same as “Duty cycle of SEG0”</td></tr>
<tr><td>……</td><td>……</td></tr>
<tr><td>Duty cycle of SEG15</td><td>The same as “Duty cycle of SEG0”</td></tr>
<tr><td>Invalid read-back command</td><td>BIT[7:0] : Reserved value is 0;</td></tr>
</table></td></tr>
<tr><td>Read close</td><td>0x84</td><td>Read close (MISO remains low);
Data bits BIT[7:0] reserved"</td></tr>
<tr><td>Chip Wake-up</td><td>0x87</td><td>Data bits BIT[7:0] reserved.
Chip wake-up, all IOs return from tri-state to configuration state; Function Description:
1, COM-IO & SEG-IO return to normal operating state, internal analog power is turned on;
2, Registers that change:
"SEG operating current & SEG display mode & Chip Enable/Disable": BIT[7] becomes 1, in Enable state;
3, Configurations remain unchanged:
"Fine-tuning related registers": 8 remain unchanged;
"Number of used COMs & operating status register of COM0-1": unchanged;
"Current scanning COM register": unchanged;
"Operating status register of COM2-9": unchanged;
"SEG operating current & SEG display mode & Chip Enable/Disable": BIT[6:0] unchanged;
"Operating status register of SEG0~ SEG7": unchanged;
"Operating status register of SEG8~ SEG15": unchanged;
"Duty cycle of SEG0~15": unchanged;</td></tr>
<tr><td>Invalid control command</td><td>0x85, 0x86, 0x88~0x90</td><td>BIT[7:0]: Arbitrary value;
No impact on the LED;</td></tr>
<tr><td>Fine-tuning</td><td>0x90~0x95</td><td>Bit[7:0] are valid</td></tr>
</table>

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Email：info@nationstech.com
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command（1~N, N = 8）		SEG Fine-tuning Register Write Instruction (6)
	0x96	Bits[4:0] are valid, Bits[7:5] default to 0 RSET Fine-tuning Register Write Instruction
	0x97	Bits[4:0] are valid, Bits[7:5] default to 0 BG Fine-tuning Register Write Instruction
Invalid control command	0x99~0x9F	BIT[7:0]: Any value; No impact on the LED;
Set SEG operating current & SEG display mode & Chip Enable/Disable	0xA0	Set the shared current size of 16 SEGs, SEG display mode, and chip enable status. 1. Where BIT[4:0] represents setting the shared current of SEG. BIT[4:0] = N represents (0.5*N +5) mA (N = 0~30, N is a positive integer, stepping 0.5mA). BIT[4:0] = 0 represents 5mA; BIT[4:0] = 1 represents 5.5mA; BIT[4:0] = 30 represents 20mA; 2. SEG display mode: When BIT[6] is 0, it indicates that SEG completes the display of SEG0~7 in the first 0.5ms and SEG8~15 in the next 0.5ms. When BIT[6] is 1, it indicates that SEG completes the display of SEG0~15 in 1ms; the default value of BIT[6] is 0 3. BIT[7] represents the chip enable status: When BIT[7] is 0, it indicates that the chip is disabled; when BIT[7] is 1, it indicates that the chip is enabled; Data bit BIT[5] is reserved as 1 by default; 4. After enabling the chip, the LED internal constant current source and digital logic circuits are enabled, thereby turning on the LED display; 5. After disabling the chip, the LED internal constant current source is turned off, thus turning off the LED. The behavior of other registers is the same as that of setting the “COM Forced Shutdown” command. The status of other registers is as follows: The registers that change are: "Current scanning COM register": BIT[3:0] becomes 0x0F, BIT[7:4] remains at 0; "SEG operating current & SEG display mode & Chip Enable/Disable": BIT[7] becomes 0, in Disable state;" The configurations remain unchanged: "Fine-tuning related registers": 8 remain unchanged; "Number of used COMs & operating status register of COM0-1": unchanged; "Operating status register of COM2-9": unchanged; "SEG operating current & SEG display mode & Chip Enable/Disable": BIT[6:0]

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Tel：+86-755-86309900
Email：info@nationstech.com
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		unchanged; "Operating status register of SEG0~7": unchanged; "Operating status register of SEG8~15": unchanged; "Duty cycle of SEG0~15": unchanged;
Set the number of used COMs & operating status register of COM0-1	0xA1	1. The data bits BIT[3:0] indicate the number of used COMs from COM0 to COM9. For example, BIT[3:0] = 3: indicates the use of COM0 to COM2; BIT[3:0] = 0x0: indicates that COM is not used; BIT[3:0] = 0x1: indicates the use of COM0, a total of 1 COM; BIT[3:0] = 0xA: indicates the use of COM0 to COM9, a total of 10 COMs; BIT[3:0] = 0xB~0xF are invalid and reserved; the used COM-IO is in 'LED operating state', and the unused COM-IO is in 'tri-state' 2. BIT[7:6] respectively indicate the conductivity status of COM1 and COM0; where BIT[7] corresponds to COM1, and BIT[6] corresponds to COM0; 3. COM has two states, namely “LED operating state” or “tri-state”; when the data bit is 1, it represents that the corresponding COM is in the “LED operating state”; when the data bit is 0, it represents that the corresponding COM is in the “tri-state”; for example, if BIT[7] = 1, it indicates that COM1 is in the “LED operating state”.
Set the operating status of COM2-9	0xA2	1. The data represents the operating status of COM2~9. COM has two states, namely “LED operating state” or “tri-state”; 2. BIT[7:0] respectively indicate the conductivity status of COM9-2, where BIT[0] corresponds to COM2, BIT[1] corresponds to COM3, BIT[2] corresponds to COM4, BIT[3] corresponds to COM5, BIT[4] corresponds to COM6, BIT[5] corresponds to COM7, BIT[6] corresponds to COM8, BIT[7] corresponds to COM9; 3. when the data bit is 1, it represents that the corresponding COM is in the “LED operating state”; when the data bit is 0, it represents that the corresponding COM is in the “tri-state”; for example, if BIT[5] = 1, it indicates that COM7 is in the “LED operating state”
Set the operating status of SEG0~7	0xA3	BIT[7:0] represents the status of SEG[7:0]-IO in “LED operating state” or “tri-state”, where 0 represents tri-state and 1 represents LED operating state, BIT0~BIT7 respectively correspond to SEG0~SEG7; for example, if BIT[7:0] = 0x17, it indicates that SEG0, SEG1, SEG2, and SEG4 are in “LED operating state”, while others are in “tri-state”.
Set the operating status of SEG8~15	0xA4	BIT[7:0] represents the status of SEG[8:15]-IO in “LED operating state” or “tri-state”, where 0 represents tri-state and 1 represents LED operating state, BIT0~BIT7 respectively correspond to SEG8~SEG15; for example, if BIT[7:0] = 0x33, it indicates that SEG8, SEG9, SEG12 and SEG13 are in “LED operating state”, while others are in “tri-state”.
Invalid command	0xA5~0xAF	BIT[7:0]: Arbitrary value;

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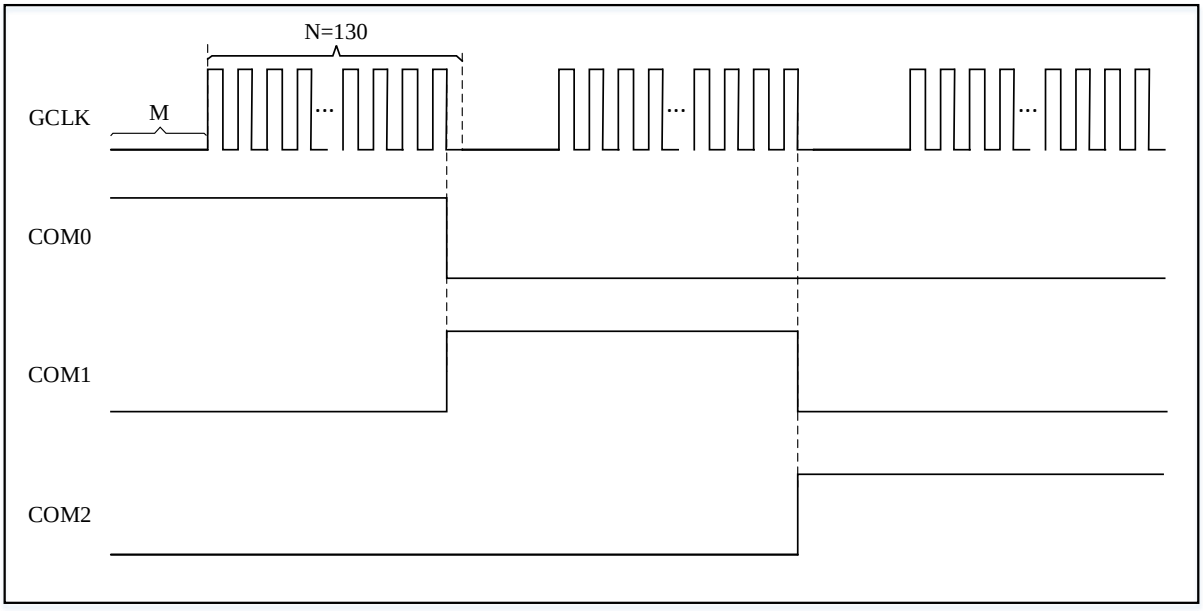
		The LED is not affected;
Set the duty cycle of SEG0	0xB0	The data represents the duty cycle parameter of SEG0, where BIT0~BIT5 are valid and BIT6~BIT7 are reserved (write invalid, read returns 2'b00); BIT[5:0] = N (N is a positive integer, ranging from 0 to 63), indicating the duty cycle of SEG0 as N/63, where 63 = 2^6 - 1; for example, BIT[5:0] = 24 represents the duty cycle of SEG0 as 24/63; for example, BIT[5:0] = 0 represents the duty cycle of SEG0 as 0/63; BIT[7:6]: Reserved value is 0;
… …	…	… …
Set the duty cycle of SEG15	0xBF	The data represents the duty cycle parameter of SEG15, where BIT0~BIT5 are valid and BIT6~BIT7 are reserved; BIT[5:0] = N (N is a positive integer, ranging from 0 to 63), indicating the duty cycle of SEG15 as N/63, where 63 = 2^6 - 1;
Invalid control command	0xC0~0xFF	BIT[7:0]: Arbitrary value; The LED is not affected;

18.3.4 LED Operating Timing

18.3.4.1 Relationship between GCLK and COM-SEG

1. When GCLK outputs 130 pulses, the LED will switch from the current COM conducting state to the next COM conducting state. The next COM after the last COM is COM0, as shown in the diagram below:

Figure 18-2 The Timing Diagram of the correspondence between GCLK and COM



2. The voltage of SEG in the inactive (inactive state) is around 3.4V, and the voltage of SEG in the active (active state) is around 1V. When the number of GCLK pulses is from the 1st to the 65th, SEG0-SEG7 will conduct simultaneously, while SEG8-SEG15 will be in the inactive state; when the number of GCLK pulses is from the 66th to the 130th, SEG0-SEG7 will be in the inactive state, and SEG8-SEG15 will be in the conducting state;

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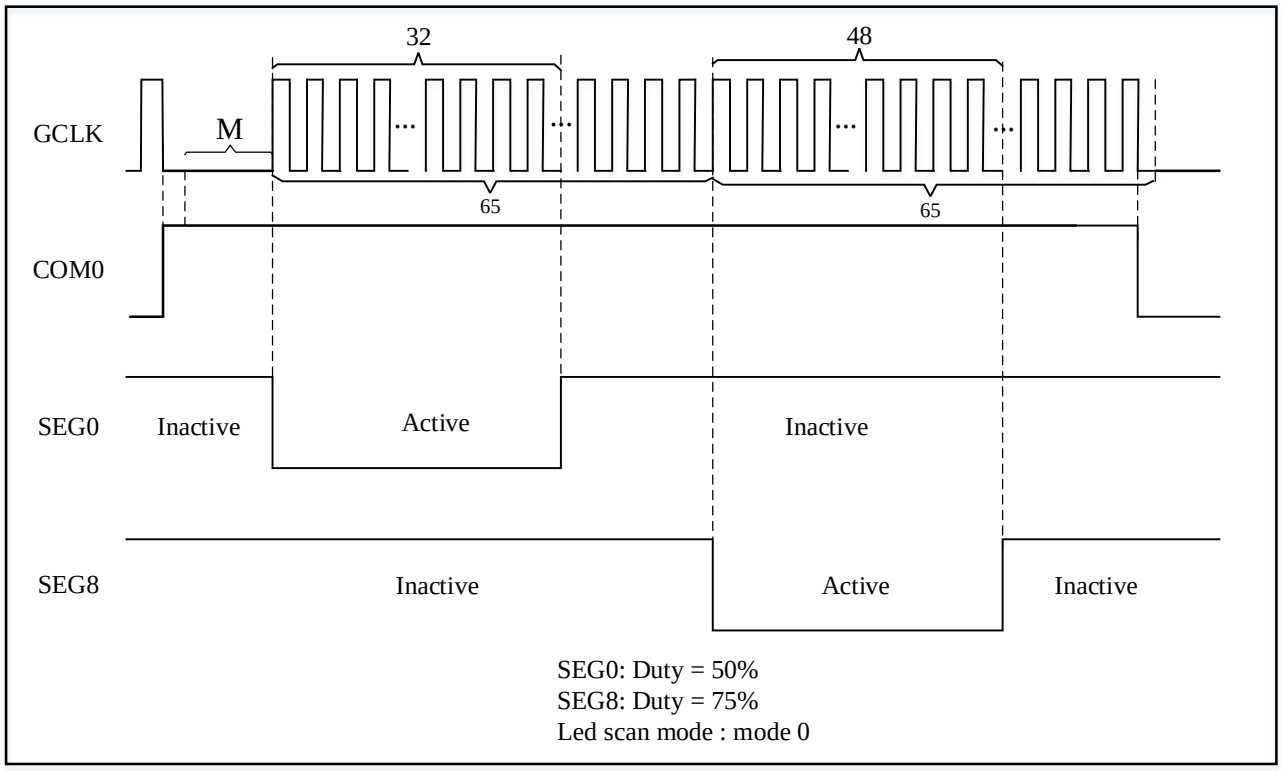
The duty cycle control of SEG mainly depends on the current number of GCLK outputs to determine whether a certain SEG should be turned off. The SEG duty cycle control is shown in the diagram below:

Figure 18-3 The Timing Diagram of GCLK and COM-SEG Control



18.3.5 LED Control Process

18.3.5.1 Power-on initialization

1. SPI3 initialization: Host unidirectional transmit-only mode, data width is 16 bits, clock polarity: SCLK remains low in idle state, clock phase: data sampling starts from the first clock edge, using hardware-controlled NSS, frame format data is MSB, communication rate is less than 3MHz;
2. DMA initialization: Source address - SRAM (the starting address of all duty cycle parameters of SEG (0-15) corresponding to COM2 (bit[7:6] is reserved, bit[5:0] is valid)), destination address - SPI DAT register, direction: memory to peripheral, data width 16 bits, memory address incrementing, peripheral address constant, transfer length - maximum 16, trigger source - completion signal of RCC's GCLK output, enable DMA transfer completion interrupt;
3. GCLK initialization: Output frequency - 130KHz, set the number of low-level clock cycles to M, set the number of clock signal cycles to N;
4. LED initialization: Send the initialization configuration to the LED through the SPI interface. After sequentially sending the COM forced shutdown and chip wake-up commands, send the global command (including configuring the number of COMs, SEG operating current & SEG display mode & chip Enable, SEG operating status), and then send the calibration-related instructions;

18.3.5.2 LED display operation process

1. Define an “The current scanning COM global variable ” (referred to as Var) within the MCU, with an initial

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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value of COM0;

2. Send the duty cycle data of SEG0~15 corresponding to COM0 to the LED by SPI
3. Send the “enable COM scanning command” by SPI;
4. Send the duty cycle data of SEG0~15 corresponding to COM1 to the LED by SPI, and enable GCLK output;
5. When the GCLK output is completed (MCU generates the GCLK output completion flag), this signal will trigger the LED to switch from COM0 to COM1. At the same time, the MCU will generate the GCLK output completion signal to trigger the DMA, and the DMA will start transferring the duty cycle data of SEG0~15 corresponding to COM2 from SRAM to the SPI_DAT register sequentially, and the SPI will automatically send this data to the LED;

In the DMA transfer completion interrupt handler, the following software processing is carried out sequentially:

- The MCU updates the source address of the DMA corresponding channel to the starting address of the duty cycle data of SEG0~15 corresponding to the next COM, while keeping the transfer count set to 16;
- Use the Var variable to determine if all currently enabled COMs have been scanned. If the scan is complete, configure Var to COM0; otherwise, set Var to the next COM;
- The MCU exits the DMA completion interrupt handler after clearing the DMA completion interrupt flag in software;

6. Repeat the operation in step 5, where the LED switches the current specific COM to the next COM, and the MCU sequentially updates the source address of the DMA corresponding channel to the starting address of the duty cycle data of SEG0~15 corresponding to the next COM (the next COM corresponding to the last COM is COM0);

18.3.5.3 LED display operation process with key scanning function

1. Define an “The current scanning COM global variable ” (referred to as Var) within the MCU, with an initial value of COM0;
2. Send the duty cycle data of SEG0~15 corresponding to COM0 to the LED by SPI;
3. Send the “enable COM scanning command” by SPI;
4. Send the duty cycle data of SEG0~15 corresponding to COM1 to the LED by SPI, and enable GCLK output;
5. When the GCLK output is completed (MCU generates the GCLK output completion flag), this signal will trigger the LED to switch from COM0 to COM1. At the same time, the MCU will generate the GCLK output completion signal to trigger the DMA, and the DMA will start transferring the duty cycle data of SEG0~15 corresponding to COM2 from SRAM to the SPI_DAT register sequentially, and the SPI will automatically send this data to the LED;

Perform the following software processing sequentially in the DMA transfer completion interrupt handler:

1) The MCU updates the source address of the DMA corresponding channel to the starting address of the duty cycle data of SEG0~15 corresponding to the next COM, while keeping the transfer count set to 16;
2) Use the Var variable to determine if all currently enabled COMs have been scanned. If the scan is complete, configure Var to COM0; otherwise, increment Var by 1;
3) The MCU exits the DMA completion interrupt handler after finally clearing the DMA completion interrupt

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

flag in software;

6. Repeat the operation in step 5, where the LED switches the current specific COM to the next COM, and the MCU sequentially updates the source address of the DMA corresponding channel to the starting address of the duty cycle data of SEG0~15 corresponding to the next COM(the next COM corresponding to the last COM is COM0). Continue this process until the display of last COM is completed(at this point, the DMA transfers the duty cycle data of SEG0~SEG15 corresponding to COM1 from SRAM to the SPI_DAT register), then proceed to step 7;
7. When the last COM scanning is completed, perform the following software processing sequentially in the DMA transfer completion interrupt handler:
   1) The MCU first turns off GCLK output, then sends the “LED forced shutdown command” via SPI;
   2) The MCU initializes the configuration of the GPIOs to be scanned (general input mode, pull-down input), completes the key scanning (reads the logic level of the scanned GPIOs), and after scanning is complete, configures the GPIOs to be scanned as high-impedance state;
   3) The MCU sends the duty cycle data of SEG0~15 corresponding to COM0 to the LED via SPI through software control;
   4) The MCU sends the “chip wake-up command” via SPI first, and then sends the “enable COM scanning command”;
   5) The MCU sends the duty cycle data of SEG0~15 corresponding to COM1 to the LED via SPI;
   6) The MCU enables GCLK output and sets Var to COM0.
   7) The MCU exits the DMA completion interrupt handler after finally clearing the DMA completion interrupt flag in software;
8. Repeat the operations of step 6 as needed.

18.3.6 Description of the Process for Reading Back LED Registers

1. Initialize the SPI as a master unidirectional transmit-only mode with a data width of 16 bits. Clock polarity: SCLK remains low in idle state, clock phase: data sampling starts from the first clock edge. Use hardware-controlled NSS, frame format data is MSB, communication rate is less than 3MHz;
2. Send a command to read a specific LED register via SPI (the DATA content of the command represents a register of a particular LED). At this point, the LED receives the command to read a specific LED register via SPI and waits for the MCU to complete steps 3 and 4 before sending the contents of the LED register to the MCU via SPI;
3. Reconfigure the SPI as a master unidirectional receive-only mode, keeping other configurations unchanged;
4. The MCU performs a receive-only operation via SPI: enables the SPI, the SPI actively sends SPI_CLK to the LED, the LED serially transmits the data of the LED register through SPI_MISO upon receiving SPI_CLK, the MCU collects the received data on the SPI_MISO pin and stores it in the SPI_DAT data register. The MCU can determine the success of data reception by checking the SPI receive flag, and then reads the data to compare it with the expected configuration values;
5. Repeat steps 1-4 to read other LED registers;

If it is necessary to end the reading of LED registers, first perform step 1, then the MCU can send a command to

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close the reading to the LED via SPI;

18.3.7 Key Scan Multiplexing

Because LED displays usually do not require high refresh rates, typically scanning one COM every 1ms. Considering that LEDs typically occupy a large amount of I/O resources, for the purpose of I/O multiplexing, users can consider performing key scanning on the SEG ports after completing the scanning of all COMs. After completing the I/O scanning, the LED can display again.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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19 I²C Interface

19.1 Introduction

The I²C(Inter-Integrated Circuit) bus is a widely used bus structure that consists of only two bidirectional lines: namely data bus SDA and clock bus SCL. All devices compatible with I²C bus can communicate directly with each other through I²C bus with these two lines.

I²C interface connects microcontroller and serial I²C bus, which can be used for communication between MCU and external I²C devices. It supports standard speed mode and fast mode with CRC calculation and verification. It also provides multi-master function to control all I²C bus specific timing, protocol, arbitration.

19.2 Main Features

- Same interface can be used for both master and slave functions
- Parallel-bus to I²C protocol converter
- Supports 7-bit/10-bit address mode and broadcast addressing
- As I²C master device, it can generate clock, start and stop signal
- As I²C slave device, it supports programmable address detection, stop bit detection function
- Supports standard speed mode(up to 100 kHz) , fast mode(up to 400 kHz) and fast plus mode(up to 1MHz)
- Supports interrupt vector: event interrupt and error interrupt share one interrupt vector
- Optional clock stretching function
- Supports DMA mode
- Optional PEC (Packet Error Check) generation and verification
- Supports SMBus 2.0 and PMBus
- Programmable analog and digital noise filters

Note: not all of the above features are included in all products. Please refer to the relevant data manual to confirm the I²C functions supported by the product.

19.3 Function Description

The I²C interface is connected to I²C bus through data pin (SDA) and clock pin (SCL) to communicate with external devices. It can be connected to standard (up to 100kHz) or fast (up to 400kHz) or fast⁺ (up to 1MHz) I²C bus. I²C module converts data from serial to parallel when receiving, and converts data from parallel to serial when transmitting. It supports interrupt mode, and user can enable or disable interrupt according to their needs.

19.3.1 SDA and SCL Line Control

The I²C module has two interface lines: serial data line (SDA) and serial clock line (SCL). Devices connecte to the bus and exchange information to each other through these two wires. Both SDA and SCL are bidirectional lines, connected to positive power supply with a pull-up resistor. When the bus is idle, both lines are high level. The output

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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of device which is connected to the bus must have open drain or open collector to provide wired-AND functionality. The data on I²C bus can reach 100 kbit/s in standard mode and 1000 kbit/s in fast mode. Since devices of different processors may be connected to the I²C bus, the levels of logic '0' and logic '1' are not fixed and depend on the actual level of VDD.

If the clock stretching is allowed, the SCL line is pulled low which can avoid the overrun error during reception and the underrun error during transmission.

For example, in the transmission mode, if the transmit data register is empty and the byte transfer finish bit is set (I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1), the I²C interface keeps the clock line low before transmission to wait for the software to read STS1 and write the data into the data register (both buffer and shift register are empty); In the receive mode, if the data register is not empty and the byte transfer finish bit is set (I2C_STS1.RXDATNE = 1, I2C_STS1.BSF = 1), the I²C interface keeps the clock line low after receiving the data byte, waiting for the software to read STS1, and then read the data register(buffer and shift register are full).

If clock stretching is disable in slave mode, if the receive data register is not empty (I2C_STS1.RXDATNE = 1) in the receive mode, and the data has not been read before receiving the next byte, an overrun error will issue and the last word byte will be discarded. In transmit mode, if the transmit data register is empty (I2C_STS1.TXDATE = 1), and no new data is written into the data register before the next byte must be sent, an underrun error will issue. The same byte will be send repeatedly. In this case, duplicate write conflicts are not controlled.

19.3.2 Software Communication Process

The data transmission of I²C device is divided into master and slave. Master is the device responsible for initializing the transmission of data on the bus and generating clock signal. At this time, any addressed device is a slave. Whether the I²C device is a master or a slave, it can transmit or receive data. Therefore, the I²C interface supports four operation modes:

- Slave transmitter mode
- Slave receiver mode
- Master transmitter mode
- Master receiver mode

After system reset, I²C works in slave mode by default. The I²C interface is configured by software to send a start bit on the bus, and then the interface automatically switches from the slave mode to the master mode. When arbitration is lost or a stop signal is generated, the interface will switched to the slave mode from the master mode.

The functional block diagram of I²C interface is shown in the figure below.

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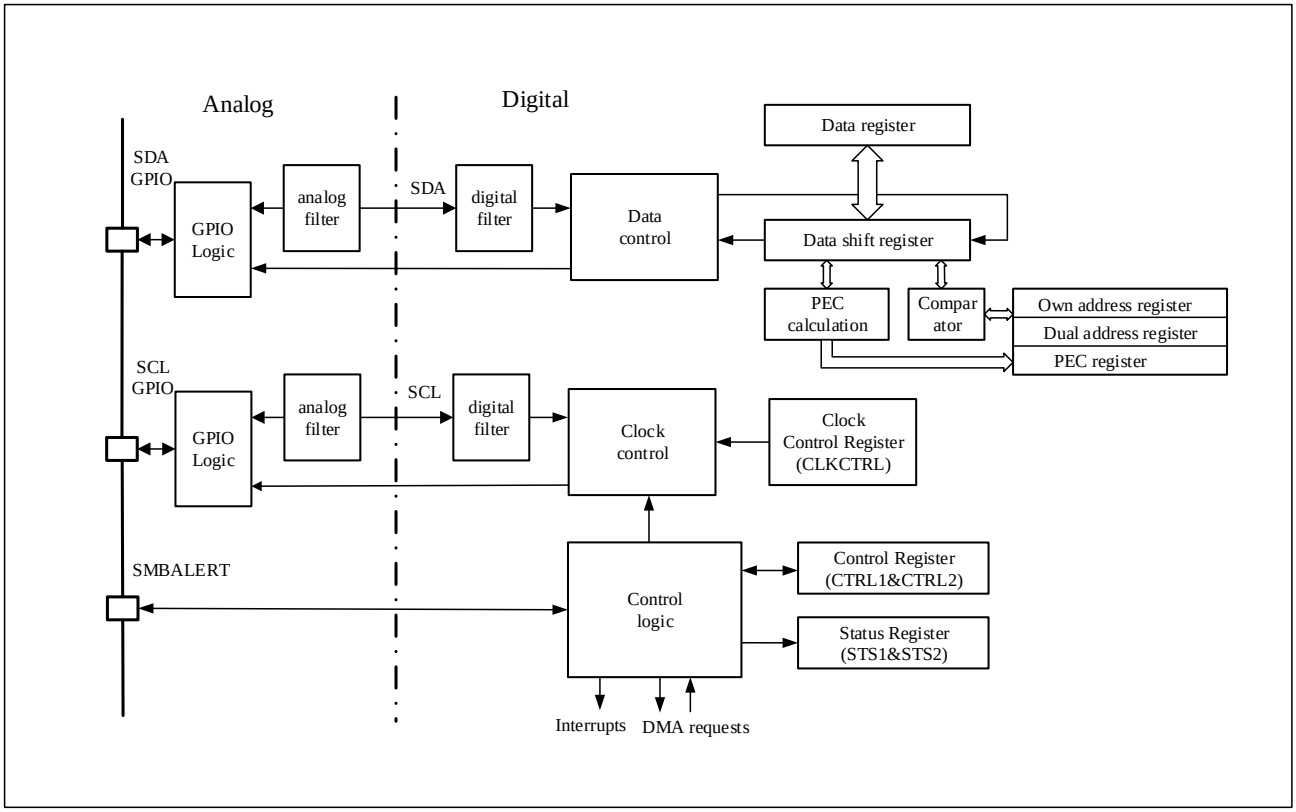
Figure 19-1 I²C Functional Block Diagram

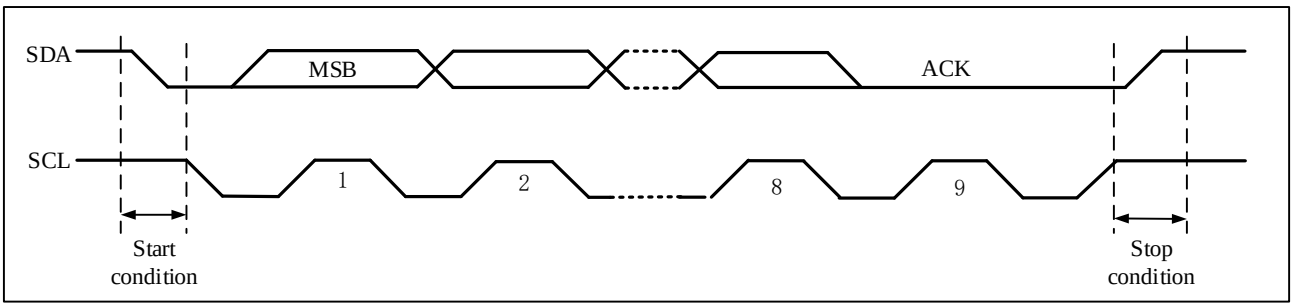


Note: in SMBus mode, SMBALERT is an optional signal. If SMBus is disabled, the signal cannot be used

19.3.2.1 Start and stop conditions

All data transfers always start with the start bit and end with the stop bit. The start and stop conditions are generated by software in the master mode. Start bit is a level conversion from high to low on SDA line when SCL is high. Stop bit is a level conversion from low to high on SDA line when SCL is high, as shown in the figure below.

Figure 19-2 I²C Bus Protocol



19.3.2.2 Clock synchronization and arbitration

The I²C module supports multi-master arbitration, which means two masters can start transferring data on an idle bus at the same time. So some mechanisms are needed to decide which master takes control of the bus, which is usually done through clock synchronization and arbitration.

I²C module has two key features:

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- SDA and SCL are open-drain circuit structures, and the signal "wire-AND" logic is realized through an external pull-up resistor.
- SDA and SCL pins will also detect the level on the pin while outputting the signal to check whether the output is consistent with the previous output, this provides the hardware basis for "Clock Synchronization" and "Bus Arbitration".

The I²C device on the bus is to output logic 0 by "grounding the line". Based on the characteristics of the I²C bus, if one device transmits logic 0 and the other transmits logic 1, then the line sees only logic 0, so there is no possibility of level conflicts on the line.

The physical connection of the bus allows the master to read data while writing data to the bus. In this way, when two masters are competing for the bus, the one that transmits logic 0 does not know the occurrence of the competition. Only the one that transmits logic 1 will find the conflict (when writing a logic 1, but read 0) and exit the competition.

Clock synchronization

Multiple masters can generate clocks on an idle bus at the same time. The high-to-low switching of the SCL line causes the devices to begin counting their low-level periods, and once the device's clock goes low, it keeps the SCL line in this state until the high-level of the clock is reached. However, if another clock is still in the low period, the low-to-high switch of this clock will not change the state of the SCL line. Therefore, the SCL line is kept low by the device with the longest low-level period. A device with a short low-level period will enter a high-level wait state.

When all related devices have counted their low-level periods, the clock line is released and goes high-level, after which there is no difference in the state of the device clock and SCL lines, and all devices will begin counting their high-level periods, the device that completes the high-level period first will pull the SCL line low again.

In this way, the low-level period of the generated synchronous SCL clock is determined by the device with the longest low-level clock period, and the high-level period is determined by the device with the shortest high-level clock period.

Arbitration

Arbitration, like synchronization, is to resolve bus control conflicts in the case of multiple masters. The arbitration process has nothing to do with the slave. When the two masters both produce a valid start bit when the bus is idle, in this case, it is necessary to decide which master will complete the data transmission. This is the process of arbitration.

Each master controller does not have the priority level of controlling the bus, which is all determined by arbitration. The bus control is determined and carried out bit by bit. They follow the principle of "low level first", that is, whoever transmits the low level first will control the bus. During the arbitration of each bit, when SCL is high, each master checks whether its own SDA level is the same as that sent by itself. In theory, if the content transmitted by two master is exactly the same, they can successfully transmit without errors. If a master sends a high level but detects that the SDA line is low, it considers that it has lost arbitration and shuts down its SDA output driver, while the other master continues to complete its own transmission.

19.3.2.3 I2C data communication process

Each I²C device is identified by a unique address. According to the device function, they can be either a transmitter or a receiver.

The I²C master is responsible for generating the start bit and the end bit in order to start and end a transmission, and is responsible for generating the SCL clock.

The I²C module supports 7-bit and 10-bit addresses, and the user can configure the address of the I²C slave through

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

software. After the I²C slave detects the start bit on the I²C bus, it starts to receive the address from the bus, and compares the received address with its own address. Once the two addresses are matched, the I²C slave will send an acknowledgement (ACK) and respond to subsequent commands on the bus: transmit or receive the requested data. In addition, if the software opens a broadcast call, the I²C slave always transmits a confirmation response to a broadcast address (0x00).

Data and address are transmitted in 8-bit width, with the most significant bit first. The 1 or 2 bytes following the start condition is the address (1 byte in 7-bit mode, 2 bytes in 10-bit mode). The address is only sent in master mode. During the 9th clock period after 8 clocks of a byte transmission, the receiver must send back an acknowledge bit (ACK) to the transmitter, as shown in the Figure 19-2 I2C Bus Protocol.

Software can enable or disable acknowledgement (ACK), and can set the I²C interface address (7-bit, 10-bit address or broadcast call address).

19.3.2.4 I2C slave transmission mode

In slave mode, the transmission reception flag bit (I2C_STS2.TRF) indicates whether it is currently in receiver mode or transmission mode. When sending data to I²C bus in transmission mode, the software should follow the following steps:

1. First, enable I²C peripheral clock and configure the related register in I2C_CTRL2, ensuring the correct I2C timing. After these two steps are completed, I²C runs in slave mode, waiting for receiving start bit and address.
2. I²C slave receives a start bit first, and then receives a matching 7-bit or 10-bit address. I²C hardware will set the I2C_STS1.ADDRF(received address and matched its own address). The software should poll this bit regularly or monitor this bit with a interrupt. After this bit is set, the software reads I2C_STS1 register and then reads I2C_STS2 register to clear the I2C_STS1.ADDRF bit. If the address is in 10-bit format, the I²C master should then generate a START and send an address header to the I²C bus. After detecting START and the following address header, the slave will continue to set I2C_STS1.ADDRF bit. The software continues to read I2C_STS1 register and read I2C_STS2 register to clear the I2C_STS1.ADDRF bit for the second time.
3. I²C enters the data sending state, and now shift register and data register I2C_DAT are all empty, so the hardware will set the I2C_STS1.TXDATE(transmitter data register empty). At this time, the software can write the first byte data to I2C_DAT register, however, because the byte of the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit is not cleared to zero. When the shift register is not empty, I²C starts to send data to I²C bus.
4. During the transmission of the first byte, the software writes the second byte to I2C_DAT. At this time, since neither the I2C_DAT register nor the shift register is empty, the I2C_STS1.TXDATE bit is cleared to 0.
5. After the first byte is transmitted, I2C_STS1.TXDATE is set again. The software writes the third byte to I2C_DAT, and at the same time, the I2C_STS1.TXDATE bit is cleared. After that, as long as there is still data to be sent and I2C_STS1.TXDATE is set to 1, the software can write a byte to I2C_DAT register.
6. During the sending of the second last byte, the software writes the last data to the I2C_DAT register to clear the I2C_STS1.TXDATE flag bit, and then the I2C_STS1.TXDATE status is no longer concerned. The I2C_STS1.TXDATE bit is set after the second last byte is sent until the stop end bit is detected.
7. According to the I²C protocol, the I²C master will not send a ACK to the last byte received. Therefore, after the last byte is sent, the I2C_STS1.ACKFAIL bit (acknowledge fail) of the I²C slave will be set to notify the software of the end of transmitting. The software writes 0 to the I2C_STS1.ACKFAIL bit to clear this bit.

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Tel：+86-755-86309900
Email：info@nationstech.com
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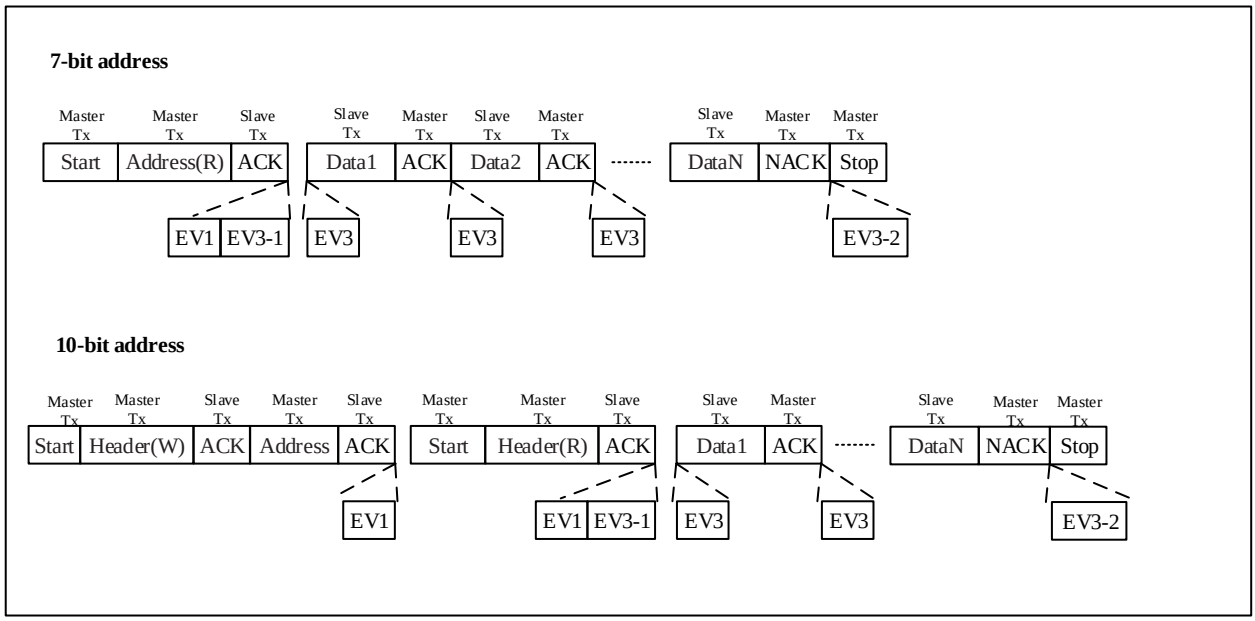
Figure 19-3 Slave Transmitter Transfer Sequence Diagram



Instructions:

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
2. EV3-1: I2C_STS1.TXDATE=1, write DAT (shift register and data register are both empty).
3. EV3: I2C_STS1.TXDATE=1, write DAT to clear the event (Shift register is not empty, while data register is empty).
4. EV3-2: I2C_STS1.ACKFAIL=1, write "0" to clear the event.

Notes:

(1) EV1 and EV3-1 event prolongs the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV3 must be completed before the end of the current byte transfer.

19.3.2.5 I^2C slave receiving mode

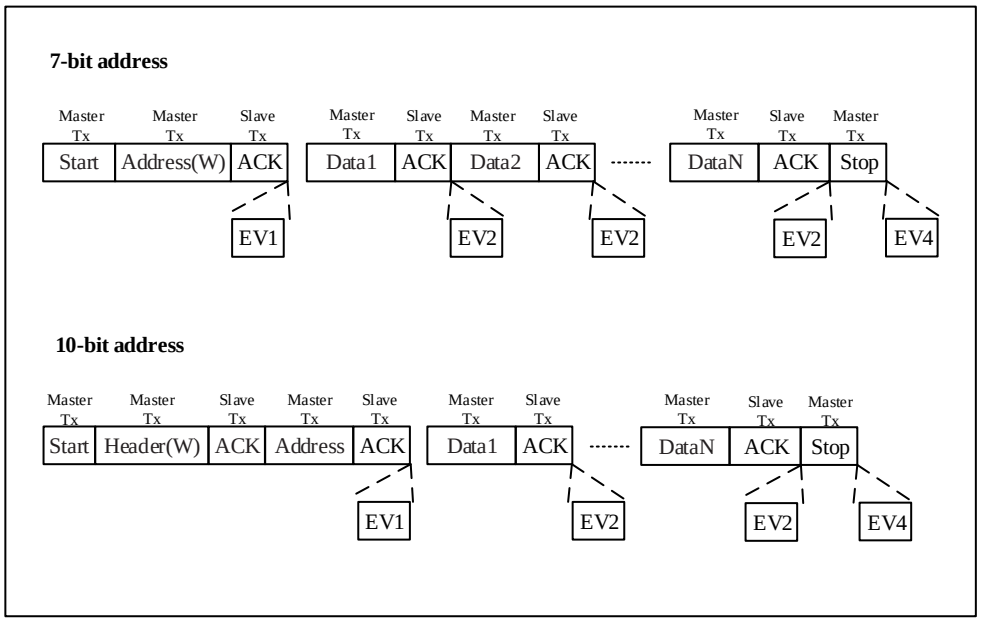
When receiving data in slave mode, the software should operate as follows:

1. First, enable I^2C peripheral clock and configure the related register in I2C_CTRL2 ensuring the correct I^2C timing. After these two steps are completed, I^2C runs in slave mode, waiting for receiving start bit and address.
2. After receiving the START condition and the matched 7-bit or 10-bit address, I^2C hardware will set I2C_STS1.ADDRF bit(the address received and matched with its own address) to 1. This bit should be detected by software polling or interrupt. After it is set, the software clears the I2C_STS1.ADDRF bit by reading I2C_STS1 register first and then I2C_STS2 register. Once the I2C_STS1.ADDRF bit is cleared, the I2C slave starts to receive data from the I^2C bus.
3. When the first byte is received, the I2C_STS1.RXDATNE bit (the received data is not empty) is set to 1 by hardware. If the I2C_CTRL2.EVTINTEN and I2C_CTRL2.BUFINTEN bits are set, an interrupt is generated. The software should check this bit by polling or interrupt. Once it is set, the software can read the first byte of I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. Note that if the I2C_CTRL1.ACKEN bit is set, after receiving a byte, the slave should generate a response pulse.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

4. At any time, as long as the I2C_STS1.RXDATNE bit is set to 1, the software can read a byte from the I2C_DAT register. When the last byte is received, I2C_STS1.RXDATNE is set to 1 and the software reads the last byte.
5. When the slave detects the STOP bit on I²C bus, I2C_STS1.STOPF is set to 1, and if the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. The software clears the I2C_STS1.STOPF bit by reading the I2C_STS1 register before writing the I2C_CTRL1 register (refer to EV4 in the following figure).

Figure 19-4 Slave Receiver Transfer Sequence Diagram



Instructions:

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
2. EV2: I2C_STS1.RXDATNE =1, read DAT to clear this event.
3. EV4: I2C_STS1.STOPF=1, read STS1 and then write the CTRL1 register to clear this event.

Notes:

(1) EV1 event prolongs the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV2 must be completed before the end of the current byte transmission.

19.3.2.6 I²C master transmission mode

In the master mode, the I²C interface starts data transmission and generates a clock signal. Serial data transmission always starts with a start condition and ends with a stop condition. When the start condition is generated on the bus through the START bit, the device enters the master mode.

When sending data to I²C bus in master mode, the software should operate as follows:

1. First, enable the I²C peripheral clock, and configure the related registers in I2C_CTRL2 to ensure the correct I²C timing. When these two steps are completed, I²C runs in the slave mode by default, waiting for receiving the start bit and address.
2. When BUSY=0, set I2C_CTRL1.STARTGEN bit to 1, and the I²C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE=1).

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

3. Once the start condition is issued, I²C hardware will set I2C_STS1.STARTBF bit(START bit flag)and then enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bit address bit or a 10-bit address bit with an address header to the I2C_DAT register to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I²C master starts transmitting addresses or address headers to I²C bus.

   In 10-bit address mode, sending a header sequence will generate the following events:

   1) I2C_STS1.ADDR10F bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, and then writes the second address byte into the DAT register.

   2) I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, followed by the STS2 register.

      Note: in the transmitter mode, the master device first transmits the header byte (11110xx0) and then transmits the lower 8 bits of the slave address. (where xx represents the highest 2 bits of the 10-bit address).

   In the 7-bit address mode, only one address byte needs to be sent out. Once the address byte is sent out:

   3) I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master device waits for reading the STS1 register once, followed by reading the STS2 register.

   Note: in the transmitter mode, the master transmits the slave address with lowest bit reset.

   Note: in 7-bit address mode, don't set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bit or 10-bit address bit is transmitted, the I²C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. The software can clear I2C_STS1.ADDRF bit by reading the I2C_STS1 register and then the I2C_STS2 register.

5. I²C enters the data transmission state. Because the shift register and the data register (I2C_DAT) are empty, the hardware sets the I2C_STS1.TXDATE bit (transmission data empty) to 1, and then the software writes the first byte of data to the I2C_DAT register. However, because the byte written into the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit will not be cleared at this time. Once the shift register is not empty, I2C starts transmitting data to the bus.

6. During the transmission of the first byte, the software writes the second byte to I2C_DAT, and I2C_STS1.TXDATE is cleared at this time. At any time, as long as there is data waiting to be transmitted and the I2C_STS1.TXDATE bit is set to 1, the software can write a byte to the I2C_DAT register.

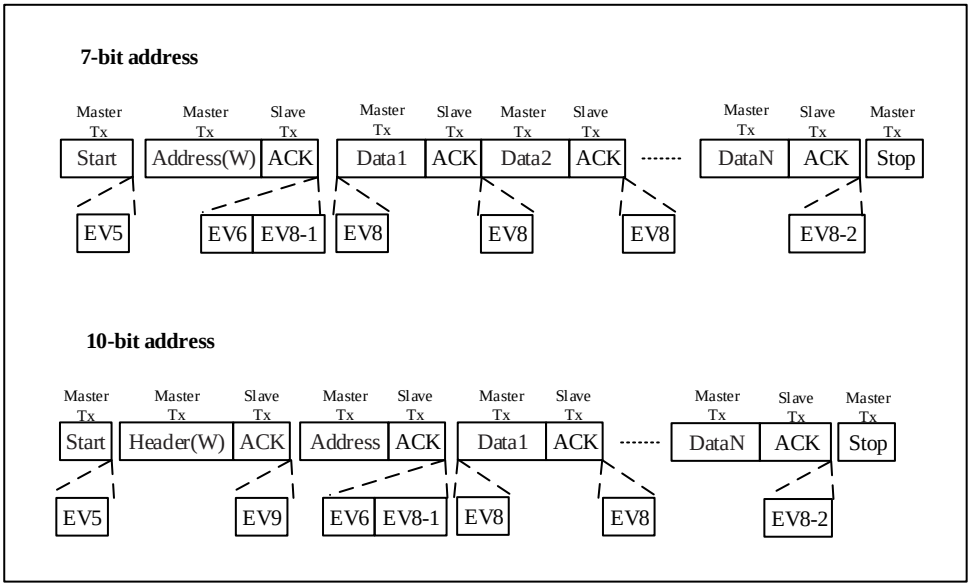
7. In the process of transmitting second last byte, the software writes the last byte to I2C_DAT to clear the I2C_STS1.TXDATE flag. After that, there is no need to care about the status of the I2C_STS1.TXDATE bit. The I2C_STS1.TXDATE bit will be set after the second last byte is transmitted, and will be cleared when the stop bit (STOP) is transmitted.

8. After the last byte is sent, because the shift register and the I2C_DAT register are empty at this time, the I2C master sets the I2C_STS1.BSF bit (byte transmission end), and the I²C interface will keep SCL low before clearing the I2C_STS1.BSF bit. After reading I2C_STS1, writing to the I2C_DAT register will clear the

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

I2C_STS1.BSF bit. The software sets the I2C_CTRL1.STOPGEN bit at this time to generate a stop condition, and then the I²C interface will automatically return to the slave mode (I2C_STS2.MSMODE bit is cleared).

Figure 19-5 Master Transmitter Transfer Sequence Diagram



Instructions:

1. EV5: I2C_STS1.STARTBF = 1, read STS1 and write the address to the DAT register to clear the event.
2. EV6: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
3. EV8_1: I2C_STS1.TXDATE = 1, write DAT register (Shift register and data register are both empty).
4. EV8: I2C_STS1.TXDATE = 1, write to DAT register will clear the event (Shift register is not empty, while data register is empty).
5. EV8_2: I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1, request to set STOP bit. These two events are cleared by the hardware when a stop condition is generated.
6. EV9: I2C_STS1.ADDR10F = 1, read STS1 and then write to DAT register to clear the event.

Notes:

(1) EV5, EV6, EV9, EV8_1 and EV8_2 event prolonged the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV8 must be completed before the end of the current byte transfer.

(3) When I2C_STS1.TXDATE or I2C_STS1.BSF bit is set, stop condition should be arranged when EV8_2 occurs.

19.3.2.7 I²C master receiving mode

The I²C interface supports BYTENUM byte control mode. In the master receiving mode, after configuring the number of bytes received, the hardware automatically ends the communication, without software intervention to configure NACK and send START/STOP conditions. Of course, normal master receive mode can be used.

In master mode, software receiving data from I²C bus should follow the following steps:

1. First, enable the I²C peripheral clock and configure the related registers in I2C_CTRL2, in order to ensure that

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

the correct I²C timing is output. After enabling and configuring, I²C runs in slave mode by default, waiting to receive the START bit and address.

Note: to enable master receive byte control, after enabling the I²C peripheral clock in this step, user need to configure the number of bytes to received through I2C_BYTENUM.BYTENUM and select the master to send START or STOP conditions after the receive is finish through I2C_BYTENUM.RXFSEL.

2. When BUSY=0, set the I2C_CTRL.STARTGEN bit, and the I²C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE bit is set to 1).

3. Once the start condition is issued, the I2C hardware sets I2C_STS1.STARTBF(START bit flag) and enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bits address or a 10-bits address with an address header to the I2C_DAT register, in order to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I2C master begins to transmit the address or address header to the I2C bus.

   In 10-bits address mode, sending a header sequence will generate the following events:

   1) When the I2C_STS1.ADDR10F bit is set to 1 by hardware, if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register, and then writes the second byte of address into the DAT register.

   2) When the I2C_STS1.ADDRF bit is set to 1 by hardware, if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register and the STS2 register in sequence.

   Note: in the receiving mode, the master device sends the header byte (11110xx0) firstly, then sends the lower 8 bits of the slave address, and then resends a start condition followed by the header byte (11110xx1) (where xx represents the highest 2 digits of the 10-bits address).

   In the 7-bits address mode, only one address byte needs to be sent, once the address byte is sent:

   3) When the I2C_STS1.ADDRF bit is set to 1 by hardware, if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device waits to read the STS1 register once, and then reads the STS2 register.

   Note: in the receiving mode, the master device sets the lowest bit as '1' when sending the slave address.

   Note: in 7-bit address mode, don't set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bits or 10-bits address is sent, the I2C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. The software clears the I2C_STS1.ADDRF bit by reading the I2C_STS1 register and the I2C_STS2 register in sequence. If in the 10-bit address mode, software should set the I2C_CTRL1.STARTGEN bit again to regenerate a START condition. After the START condition is generated, the I2C_STS1.STARTBF bit will be set. The software should clear the I2C_STS1.STARTBF bit by reading I2C_STS1 firstly and then writing the address header to I2C_DAT, and then the address header is sent to the I2C bus, and I2C_STS1.ADDRF is set to 1 again. The software should clear the I2C_STS1.ADDRF bit again by reading I2C_STS1 and I2C_STS2 in sequence.

5. After sending the address and clearing the I2C_STS1.ADDRF bit, the I2C interface enters the master receiving mode. In this mode, the I2C interface receives data bytes from the SDA line and sends them to the DAT register

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

through the internal shift register. Once the first byte is received, the hardware will set the I2C_STS1.RXDATNE bit (not empty flag bit of received data) to 1, and if the I2C_CTRL1.ACKEN bit is set to 1, an acknowledge pulse will be sent. At this time, the software can read the first byte from the I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. After that, as long as I2C_STS1.RXDATNE is set to 1, the software can read a byte from the I2C_DAT register.

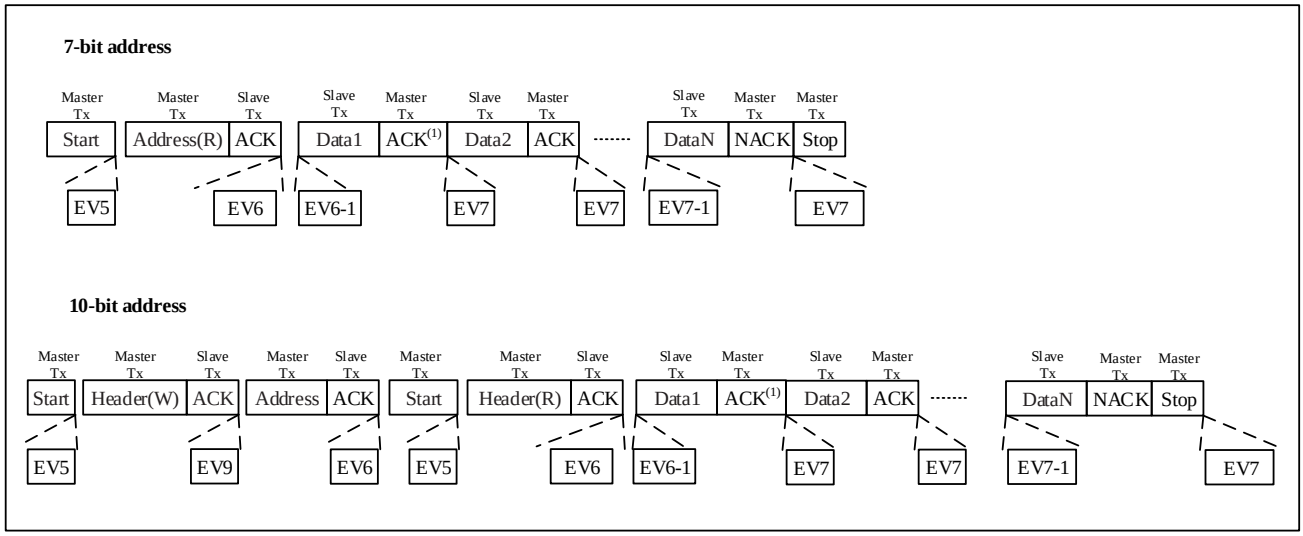
6. The master device sends a NACK after receiving the last byte from the slave device. After receiving the NACK, the slave device releases the control of SCL and SDA lines; the master device can send a stop/restart condition. In order to generate a NACK pulse after receiving the last byte, the software should clear the I2C_CTRL1.ACKEN bit immediately after receiving the second last byte (N-1). In order to generate a stop/restart condition, the software must set the I2C_CTRL1.STOPGEN bit or I2C_CTRL1.STARTGEN to 1 after reading the second last data byte. This process needs to be completed before the last byte is received to ensure that the NACK is sent for the last byte.

   Note: if the master receive byte control is enabled earlier, steps 6 and 7 can be ignored, the software only needs to read the bytes according to the receive flag, and the hardware will automatically send NACK and START/STOP conditions after the the receive is finish.

7. After the last byte is received, the I2C_STS1.RXDATNE bit is set to 1, and the software can read the last byte. Since I2C_CTRL1.ACKEN has been cleared to 0 in the previous step, I2C no longer sends ACK for the last byte, and generates a STOP bit after the last byte is sent.

Note: in normal master receive mode, the above steps require the number of bytes N>1. If N=1, step 6 should be executed after step 4, and it needs to be completed before the reception of byte is completed.

Figure 19-6 Master Receiver Transfer Sequence Diagram



Instructions:

1. EV5: I2C_STS1.STARTBF=1, read STS1 and then write the address into the DAT register to clear this event.
2. EV6: I2C_STS1.ADDRF=1, read STS1 and STS2 in sequence to clear this event. In the 10-bits master receiving mode, the I2C_CTRL1.STARTGEN should be set to 1 after this event.
3. EV6_1: There is no corresponding event flag. Just after EV6 (that is after clearing I2C_STS1.ADDRF), the generation bits for acknowledge and stop condition should be cleared.
4. EV7: I2C_STS1.RXDATNE=1, read the DAT register to clear this event.
5. EV7_1: I2C_STS1.RXDATNE =1, read the DAT register to clear this event. Set I2C_CTRL1.ACKEN=0 and

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

I2C_CTRL1.STOPGEN=1.

6. EV9: I2C_STS1.ADDR10F=1, read STS1 and then write to the DAT register to clear this event.

Notes:

(1) If a single byte is received, it is NA.

(2) EV5, EV6, and EV9 events extend the low SCL time until the corresponding software sequence ends.

(3) The EV7 software sequence shall be completed before the end of the current byte transmission.

(4) The software sequence of EV6_1 or EV7_1 shall be completed before the ACK pulse of the current transmission byte.

19.3.3 Error Conditions Description

I^2C errors mainly include bus error, acknowledge fail, arbitration loss, overrun\underrun error. These errors may cause communication failure.

19.3.3.1 Acknowledge failure(ACKFAIL)

When the interface detects that acknowledgement bit does not match the expectation, it will generate an acknowledge fail error, and I2C_STS1.ACKFAIL bit is set. An interrupt will be generated, if I2C_CTRL2.ERRINTEN bit is set to 1.

When transmitter receives a NACK, the communication must be reset: if in slave mode, hardware will release the bus; if in master mode, it must generate a stop condition from software.

19.3.3.2 Bus error(BUSERR)

When address or data is transmissing, if I^2C interface receive external stop or start condition, a bus error is generated, and I2C_STS1.BUSERR bit is set. An interrupt will be generated, if I2C_CTRL2.ERRINTEN bit is set to 1.

In master mode, the hardware does not release bus, as the same time it done not affect the current transmission status. It is up to software to abort or not the current transmission.

In slave mode, data is discarded in transmission and the bus is released by hardware. There are two situations: if an error start condition is detected, the slave device considers a restart condition and waits for an address or a stop condition. If an error stop condition is detected, the slave device operates as a normal stop condition and the hardware releases the bus.

19.3.3.3 Arbitration lost(ARLOST)

If arbitration lost is detected, an arbitration lost occurs with I2C_STS1.ARLOST bit set, and hardware release the bus. An interrupt will be generated, if I2C_CTRL2.ERRINTEN bit is set to 1.

I^2C interface will go to slave mode automatically(I2C_STS2.MSMODE bit is cleared). When the I^2C interface lost the arbitration, it can not acknowledge to its slave address in the same transfer, but it can acknowledge it after a repeat start condition from winning master.

19.3.3.4 Overrun/Underrun error(OVERRUN)

In slave mode, overrun/underrun error can easily occur if clock stretching is disable.

When I^2C interface has received a byte(I2C_STS1.RXDATNE=1), and I2C_DAT register still have previous byte has not been read, it will occurs an overrun error. In this situation, the last received data is discarded; Software should clear I2C_STS1.RXDATNE bit, and the transmitter should retransmit last byte.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

In slave transmission mode, if clock stretching is disabled, an underrun error occurs when the current byte has been sent but the data register remains empty (I2C_STS1.TXDATE=1). In this situation, the previous byte in the I2C_DAT register is transmitted repeatedly; User should make sure that in the event of an underrun error, the receiver discard repeatedly byte. The transmitter should update the I2C_DAT register at the specified time according to the I²C bus standard.

During transmitting the first byte, I2C_DAT register must be written after I2C_STS1.ADDRF bit is cleared and the before the first SCL rising edge. If no possible, receiver must discard the first byte.

19.3.4 DMA Application

DMA can generate a requests when transfer data register empty or full. DMA can write data to I²C or read data from I²C reduce the CPU overload.

Before the current byte transfers end, DMA requests must be responded. If set the DMA channel transfer data is done, DMA will send EOT(End of Transmission) to I²C, and ocurr a interrupt when enable interrupt bit.

In the master transfer mode, in EOT interrupt handler DMA request need to be disbale, and set stop condition after waiting for I2C_STS1.BSF event.

In the master receive mode, the data of received is great than or equal to 2, DMA will send a hardware signal EOT_1 in DMA transmission(byte number-1). If set I2C_CTRL2.DMALAST bit, when hardware has sent the EOT_1 next byte it will send a NACK automatically. The user can set a stop condition in the interrupt handler after the DMA transfer is completed if interrupt enable.

19.3.4.1 Transmit process

DMA mode need can be enabled by setting the I2C_CTRL2.DMAEN bit. When I2C_STS1.TXDATE bit is set, the data will send to I2C_DAT from memory block by the DMA. DMA assign a channle for I²C transmission, (x is the channel number) the following step must be opreate:

1. In the DMA_PADDRx register set the I2C_DAT register address. Data will be send to address in every I2C_STS1.TXDATE event.
2. In the DMA_MADDRx register set the memory address. Data will send to I2C_DAT address in every I2C_STS1.TXDATE event.
3. In the DMA_TXNUMx register set the number of need to be transferred.In every I2C_STS1.TXDATE event this number-1 until 0.
4. In the DMA_CHCFGx register set PRIOLVL[1:0] bit to configure the priority of channel.
5. In the DMA_CHCFGx register set DIR bit to configure when ocurrs an interrupt whether send a half data or all completed.
6. In the DMA_CHCFGx register set CHEN bit to enable transfer channel.
7. When DMA transfer data is done, DMA need send a EOT/EOT_1 signal to I²C indicate this transfer is done. If interrupt is enable, DMA ocurrs a interrrupt.

Note: If DMA is used for transmission, do not set I2C_CTRL2.BUFINTEN bit.

19.3.4.2 Receive process

DMA mode can be enabled by setting I2C_CTRL2.DMAEN bit. When data byte is received,DMA will send I²C data

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

to memory block. To set DMA channel for I²C reception, the following steps must be opreate:

1. In DMA_PADDRx register set the address of the I2C_DAT register. In every I2C_STS1.RXDATEN event, data will send from address to memory block.
2. In DMA_MADDRx register set the memory block address. In every I2C_STS1.RXDATEN event,data will send from I2C_DAT register to memory block.
3. In DMA_TXNUMx register set the number of need to be transferred. In every I2C_STS1.RXDATEN event the number-1 until 0.
4. In DMA_CHCFGx register set PRIOLVL[0:1] to configure the priority of channel.
5. In DMA_CHCFGx register clear DIR to configure when ocurrs a interrupt request whether received half data or all data is received.
6. In the DMA_CHCFGx register set CHEN bit to activate the channle.
7. When DMA tansfer data is done, DMA need to send EOT/EOT_1 signal to I2C indicate this transfer is done, if interrupt is enbale, DMA ocurrs a interrupt.

Note: If DMA is used for receiving, do not set I2C_CTRL2.BUFINTEN bit.

19.3.5 Packet Error Check(PEC)

Setting the I2C_CTRL1.PECEN bit to 1 enables the PEC function. PEC uses CRC-8 algorithm to calculate all information bytes including address and read/write bits. It can improve the reliability of communication. The CRC-8 polynomial uses by the PEC calculator is $C(x) = x^8 + x^2 + x + 1$.

In transmission mode, software sets I2C_CTRL1.PEC bit after the last I2C_STS1.TXDATE event, and then PEC will be transmitted after the last byte. While in receiving mode, software sets I2C_CTRL1.PEC bit after the last I2C_STS1.RXDATNE event, and then receives the PEC byte and compares the received PEC byte to the internally calculated PEC value. If it is not equal to the internally calculated PEC value, the receiver needs to send a NACK. If it is master receiving mode, NACK will be sent after PEC regardless of the calculated result. Note that I2C_CTRL1.PEC bit must be set before receiving the ACK pulse of the current byte.

If transmitting both DMA and PEC calculator are activated, I2C will automatically send or check the PEC value.

In transfer mode, when I²C interface receives EOT signal from DMA controller, it will automatically send PEC following the last byte. In receiving mode, when I²C interface receives an EOT_1 signal from DMA, it will automatically consider the next byte as PEC and compare it with the internally calculated PEC. It will happen a DMA request after receiving PEC.

In order to allow intermediate PEC transfer, I2C_CTRL2.DMALAST bit is used to determine whether it is the last DMA transfer. And if it does the last DMA request of the master receiver, NACK will be sent automatically after receiving the last byte.

When arbitration is lost, PEC calculation is invalid.

19.3.6 Timeout Function

SMBus has a timeout feature: if it has taken too long time during the communication, it automatically resets the device. This is the reason why SMBus has a minimum transmission rate limitation: to prevent the bus from locking up for a long time after the timeout occurs. I²C bus is essentially a "DC" bus, that is to say, if the slave is executing some subroutines and cannot respond in time while the master is accessing the slave, it can hold the clock. That can

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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remind the host that the slave is busy but does not want to give up the current communication. This session can continue after the current task of the slave is over.

N32G05X series chips support timeout configuration in both I²C mode and SMBUS mode, including SCL low timeout judgment, SCL high timeout judgment, and SDA low timeout judgment. The SCL low timeout function configures the timeout threshold through I2C_CTRL1.LTOSEL, and I2C_CTRL2.LTOEN enables the timeout judgment. When the SCL is low for more than the set threshold, I2C_STS1.SCLLTO is set to 1. At this time, if I2C_CTRL2.SCLLTOINTEN is 1, an interrupt is generated. The SCL high timeout function configures the timeout threshold through I2C_CTRL1.HTOSEL, and I2C_CTRL2.HTOEN enables the timeout judgment. It can judge the timeout. When the SCL is high for more than the set threshold, I2C_STS1.SCLHTO is set to 1. If I2C_CTRL2.SCLHTOINTEN is 1, an interrupt will be generated. The SDA low timeout function configures the timeout threshold through I2C_CTRL1.LTOSEL, and I2C_CTRL2.LTOEN enables timeout judgment. When the SDA is low for more than the set threshold, I2C_STS1.SDALTO is set to 1. If I2C_CTRL2.SDALTOINTEN is 1, an interrupt will be generated. If a session takes longer than the threshold, it means that there is a problem with the bus. At this time, all devices should be reset to eliminate this state (problem).

19.3.7 SMBus

19.3.7.1 Introduction

The System Management Bus(SMBus or SMB) is a simple single-ended two-wire bus structure. Using SMBus can communicate with other device or other parts of the system, it able to commnicate with multiple devices without other independent control wire. SMBus is a derivate of the I²C bus and provides a control bus for system and power management related tasks. If you want browse more information, please refer to the SMBus specification V2.0(http://smbus.org/specs/).

SMBus have three types of device standard.

- Master: device send command,generate clocks and stop transmmissions;
- Slave: device receive,respond to commands;
- Host: system have only one host. A device provides a master to system CPU. Host have functions of master and slave, it supports SMBus alert protocol.

SMBus is a subset of the data transmission format of the I²C specification.

Similarities between SMBus and I²C:

- Both bus protocols contain of 2 wires (a clock wire SCL and a data wire SDA), with an optional SMBus alert wire.
- The data format is similar. SMBus data format is similar to 7-bit address format of I2C(See Figure 19-2).
- Both are master-slave communication modes, and the master device provides the clock.
- Both support multi master

Differences between SMBus and I²C:

Table 19-1 Comparison Between SMBus and I²C

SMBus	I²C
Maximum transmission speed 100kHz	Maximum transmission speed 1MHz
Minimum transmission speed 10kHz	No minimum transmission speed

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Email：info@nationstech.com
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SMBus	I²C
Fixed logic level	V_{DD} determined logic level
Different address types (reserved, dynamic, etc.)	7-bit, 10-bit, and broadcast call slave address types
Different bus protocols (quick command, call handling, etc.)	No bus protocol

19.3.7.2 SMBus usage

SMBus uses the system management bus to meet lightweight communication requirements. In general, SMBus is commonly used on the computer motherboard. It is mainly used to transmit ON/OFF instructions for power unit and provide a control bus for system and power management-related tasks.

19.3.7.3 Device identification

In SMBus, any device acting as a slave device has an address called the slave address.

In order to distribute addres for each devices, it must have a unique device identifier(UDID) to distinguish devices.

19.3.7.4 Bus protocol

SMBus specification includes eight bus protocols. If user wants browse the details on protocols or SMBus address types,it can refer to the SMBus specification v2.0(http://smbus.org/specs/). User's software can device what protocols are implemented.

Every packet through the SMBus complies with the SMBus protocol predefined format. SMBus is a subset of the data transfer format of I²C specification. As long as an I²C device can be accessed through one of the SMBus protocols, it is considered to be SMBus compliant.

Note: SMBus does not support Quick command protocol.

19.3.7.5 Address resolution protocol (ARP)

The SMBus resolves address conflicts by dynamically assigning a new unique address to each slave device. This is the address resolution protocol(ARP) . The Address Resolution Protocol has the following characteristics:

Any master device can connected bus to access all devices.

SMBus physical layer arbitration enable to distribute addresses.When device power on, the device's distribute address is not change, the protocol allows address retain when device power off.

When address is distributed, there is no extra SMBus packaging cost(the cost time that access distribute address device and access fixed address device is same).

19.3.7.6 SMBus alter mode

SMBus offers a optional interrupt signal SMBALERT(like SCL and SDA, is a wire-AND signal) that devices use to extend their control capabilities at expense of a pin. SMBus broadcast call address often combine with SMBALERT. There are 2 bytes message about SMBus.

A device which only has slave function can set I2C_CTRL1.SMBALERT bit to indicate it want to communicate with host. The host handles the interrupt and accesses all SMBALERT devices through the ARA (Alert Response Address, address value 0001100x). Only those devices that pull SMBALERT low can respond to ARA. This state is identified by the I2C_STS1.SMBALERT. The 7-bit device address provided from the sending device is placed on the 7 most significant bits of the byte, the eighth bit can be either '0' or '1'.

When more than one device's SMBALERT is low, the highest priority(The smaller the address, the higher the priority)

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

can win bus communication through the standard arbitration during address transmission. If confirming the slave address, device's SMBALERT is no longer pulled low. If message transmitted completely,device's SMBALERT still is low, it means host will read ARA again. The host can periodically access the ARA when the SMBALERT signal is not used.

19.3.7.7 SMBus communication process

The communication process on SMBus is similar to that on I²C. To use the SMBus mode, you need to configure SMBus specific registers in the program, respond and process SMBus specific flag, and to implement the upper-layer protocols described in the SMBus manual.

1. At first, set I2C_CTRL1.SMBMODE bit, and configure I2C_CTRL1.SMBTYPE bit and I2C_CTRL1.ARPEN bit according to the application requirements. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=0, use the default address of the SMB device. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=1, use the SMB master header field.
2. In order to support ARP (I2C_CTRL1.ARPEN=1), in SMBus host mode (I2C_CTRL1.SMBTYPE=1), software needs to respond to the I2C_STS2.SMBHADDR bit (in SMBus slave mode, respond to I2C_STS2.SMBDADDR bit) and implement the functions according to the ARP protocol.
3. To support the SMBus warning mode, software should respond to the I2C_STS1.SMBALERT bit and implement the corresponding functions.

19.3.7.8 Noise Filter

The I²C interface standard requires the ability to filter spikes of 50ns on SCL/SDA, hence analog filter and digital filter are added in design. By default, analog filter are enable and can be disable by setting I2C_TMRISE.SCLAFENN/SDAAFENN. The spike filtering width of analog filter can be configured by setting I2C_TMRSE.SCLAFE/SDAAFW with the width of 5ns, 15ns, 25ns, 35ns. Digital filter can be enabled by setting I2C_TMRISE.SCLDFW/SDADFW to a non-zero values. The max width of digital/analog filter is (SCLDEW[3:0] or SDADFW[3:0])*T_{PCLK}. Enabling the digital filter will increase the hold time of SDA by an amount equal to (SDADFW[3:0]+1)*T_{PCLK}.

19.4 Debug Mode

When the microcontroller enters the debug mode (Cortex®-M0 core is in the stop state), configure the DBG_CTRL.I2CxSMBUS_TIMEOUT bit in the DBG module, select SMBUS timeout to continue normal work or stop. See Section 3.3.2 for details.

19.5 Interrupt Request

All I²C interrupt requests are listed in the following table.

Table 19-2 I²C Interrupt Request

Interrupt Function	Interrupt Event	Event Flag	Set Control Bit
I²C global interrupt	Start bit sent (master)	STARTBF	EVTINTEN
	Address sent (master) or address matched (slave)	ADDRF	
	10-bit header sent (master)	ADDR10F	
	Received stop (slave)	STOPF	

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Email：info@nationstech.com
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Interrupt Function	Interrupt Event	Event Flag	Set Control Bit
	Data byte transfer completed.	BSF	
	Receive buffer is not empty.	RXDATNE	EVTINTEN and BUFINTEN
	Transmit buffer is empty.	TXDATE	
	Bus error	BUSERR	ERRINTEN
	Lost arbitration (master)	ARLOST	
	Acknowledge fail	ACKFAIL	
	Overrun/underrun	OVERRUN	
	PEC error	PECERR	
	SMBus Alert	SMBALERT	
	SCL low tiomeout	SCLLTO	SCLLTOINTEN
	SCL high tiomeout	SCLHTO	SCLHTOINTEN
	SDA low tiomeout	SDALTO	SDALTOINTEN

19.6 I²C Registers

These peripheral registers can be operated by half word (16 bits) or word (32 bits)

19.6.1 I²C Register Overview

Table 19-3 I²C Register Overview

Offset	Register	32	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	I2C_CTRL1	Reserved	LTOSEL		HTOSEL		Reserved											Reserved		SWRESET	SMBALERT	PEC	ACKPOS	ACKEN	STOPGEN	STARTGEN	NOEXTEND	GCEN	PECEN	ARPEN	SMBTYPE	SMBMODE	EN
	Reset Value		0	0	0	0														0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	I2C_CTRL2	Reserved	LTOEN	HTOEN	SCLLTOINTEN	SCLHTOINTEN	SDALTOINTEN	Reserved										DMAEN	ERRINTEN	EVTINTEN	BUFINTEN	Reserved			DMALAST	Reserved	CLKFREQ[6:0]							
	Reset Value		0	0	0	0	0											0	0	0	0				0		0	0	0	0	0	0	0	0
008h	I2C_OADDR1	Reserved																ADDRMODE	Reserved					ADDR [9:8]		ADDR[7:1]							ADDR0
	Reset Value																	0						0	0	0	0	0	0	0	0	0	0
00Ch	I2C_OADDR2	Reserved																Reserved								ADDR2[7:1]							DUALEN
	Reset Value																									0	0	0	0	0	0	0	0
010h	I2C_DAT	Reserved																Reserved								DATA[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	I2C_STS1	Reserved						SCLLTO	SCLHTO	SDALTO	Reserved							Reserved	SMBALERT	Reserved	PECERR	OVERRUN	BUSERR	ARLOST	ACKFAIL	Reserved	ADDR10F	TXDATE	RXDATNE	STOPF	BSF	ADDRF	STARTBF
	Reset Value							0	0	0									0		0	0	0	0	0		0	0	0	0	0	0	0
018h	I2C_STS2	Reserved																PECVAL[7:0]								SMBHADDR	SMBDADDR	DUALFLAG	GCALLADDR	Reserved	TRF	MSMODE	BUSY
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
01Ch	I2C_CLKCTRL	Reserved																DUTY	FSMODE	Reserved	CLKCTRL[11:0]												
	Reset Value																	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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| | | |

Bit Field	Name	Description
		It can be set or cleared by software. When I2C_CTRL1.EN=0, it will be cleared by hardware. 0: SMBAlert pin go high. The response address header is followed by the NACK signal; 1: SMBAlert pin go low. The response address header is followed by the ACK signal.
11	PEC	Packet error checking It can be set or cleared by software. It will be cleared by hardware when PEC has been transferred, or by start or stop condition, or when I2C_CTRL1.EN=0. 0: No PEC transfer 1: PEC transfer. *Note: When arbitration is lost, the calculation of PEC is invalid.*
10	ACKPOS	Acknowledge/PEC Position（for data reception） It can be set or cleared by software. Or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: I2C_CTRL1.ACKEN bit determines whether to send an ACK to the byte currently being received; I2C_CTRL1.PEC bit indicates that the byte in the current shift register is PEC. 1: I2C_CTRL1.ACKEN bit etermines whether to send an ACK to the next received byte; I2C_CTRL1.PEC bit indicates that the next byte received in the shift register is PEC. *Note：* *ACKPOS bit can only be used in 2-byte receiving configuration and must be configured before receiving data.* *For the second byte of NACK, the I2C_CTRL1.ACKEN bit must be cleared after the I2C_STS1.ADDRF bit is cleared.* *To detect the PEC of the second byte, the I2C_CTRL1.PEC bit must be set after the ACKPOS bit is configured and when the ADDR event is extended.*
9	ACKEN	Acknowledge enable It can be set or cleared by software. Or when I2C_CTRL1.EN equals to 0, it will be cleared by hardware. 0: No acknowledge send; 1: Send an acknowledge after receiving a byte
8	STOPGEN	Stop generation It can be set or cleared by software. Or it will be cleared by hardware when a stop condition is detected. Or it will be set by hardware when SMBus timeout error is detected,. In the master mode: 0: No stop condition generates; 1: Generate a stop condition. In the slave mode: 0: No stop condition generates; 1: Release SCL and SDA lines after the current byte. *Note：When the STOPGEN, STARTGEN or PEC bit is set, the software should not take any write operation to I2C_CTRL1 until this bit is cleared by hardware. Otherwise, the STOPGEN, STARTGEN or PEC bits may be set twice.*
7	STARTGEN	Start generation It can be set or cleared by software. Or it will be cleared by hardware when the start condition is transferred or I2C_CTRL1.EN=0. 0: No start condition generates;

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Bit Field	Name	Description
		1: Generate a start conditions.
6	NOEXTEND	Clock stretching disable (Slave mode) This bit determines whether to pull SCL low when the data is not ready(I2C_STS1.ADDRF or I2C_STS1.BSF flag is set) in slave mode, and is cleared by software reset 0: Enable Clock stretching. 1: Disable Clock stretching.
5	GCEN	General call enable 0: Disable General call. not respond(NACK) to the address 00h; 1: Enable General call. respond(ACK) the address 00h.
4	PECEN	PEC enable 0: Disable PEC module; 1: Enable PEC module.
3	ARPEN	ARP enable 0: Disable ARP; 1: Enable ARP. If I2C_CTRL1.SMBTYPE=0, the default address of SMBus device is used. If I2C_CTRL1.SMBTYPE=1, the host address of SMBus is used.
2	SMBTYPE	SMBus type 0: Device 1: Host
1	SMBMODE	SMBus mode 0: I^2C mode; 1: SMBus mode.
0	EN	I^2C Peripheral enable 0: Disable I^2C module; 1: Enable I^2C module *Note: If this bit is cleared when the communication is in progress, the I^2C module is disabled and returns to the idle state after the current communication ends,all bits will be cleared.* *In master mode,this bit must never be cleared until the communication has ended.*

19.6.3 I^2C Control Register 2 (I2C_CTRL2)

Address offset: 0x04

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	LTOEN	HTOEN	SCLLTO INTEN	SCLHTO INTEN	SDALTO INTEN	Reserved									
	rw	rw	rw	rw	rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAEN	ERRINT EN	EVTINT EN	BUFINT EN	Reserved			DMA LAST	Reserved	CLKFREQ[6:0]						
rw	rw	rw	rw				rw		rw						

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Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	LTOEN	Low timeout function enable 0: Disable; 1: Enable. *Note: This bit can be disabled when timeout error is not required in I2C mode*
29	HTOEN	High timeout function enable 0: Disable; 1: Enable. *Note: This bit can be disabled when timeout error is not required in I2C mode*
28	SCLLTOINTEN	SCL low timeout error interrupt enable 0: When I2C_STS1.SCLLTO = 1, an interrupt is not generated; 1: When I2C_STS1.SCLLTO = 1, an interrupt is generated.
27	SCLHTOINTEN	SCL high timeout error interrupt enable This bit is cleared by software writing '0', or by hardware when I2C_CTRL1.EN=0. 0: When I2C_STS1.SCLHTO = 1, an interrupt is not generated; 1: When I2C_STS1.SCLHTO = 1, an interrupt is generated.
26	SDALTOINTEN	SDA low timeout error interrupt enable This bit is cleared by software writing '0', or by hardware when I2C_CTRL1.EN=0. 0: When I2C_STS1.SDALTO = 1, an interrupt is not generated; 1: When I2C_STS1.SDALTO = 1, an interrupt is generated.
25:16	Reserved	Reserved, the reset value must be maintained.
15	DMAEN	DMA requests enable 0: Disable DMA 1: Enable DMA
14	ERRINTEN	Event interrupt enable 0：Disable event interrupt； 1：Enable event interrupt This interrupt is generated when: I2C_STS1.BUSERR = 1 I2C_STS1.ARLOST = 1 I2C_STS1.ACKFAIL = 1 I2C_STS1.OVERRUN = 1 I2C_STS1.PECERR = 1 I2C_STS1.SMBALERT = 1
13	EVTINTEN	Event interrupt enable 0：Disable event interrupt； 1：Enable event interrupt This interrupt is generated when: I2C_STS1.STARTBF = 1 (Master) I2C_STS1.ADDR F = 1 (Master/Slave) I2C_STS1.ADD10F = 1 (Master) I2C_STS1.STOPF = 1 (Slave) I2C_STS1.BSF = 1 with no I2C_STS1.TXDATE or I2C_STS1.RXDATNE event

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
		I2C_STS1.TXDATE = 1 if I2C_CTRL2.BUFINTEN = 1 I2C_STS1.RXDATNE = 1 if I2C_CTRL2.BUFINTEN = 1
12	BUFINTEN	Buffer interrupt enable 0: When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE=1, any interrupt is not generated. 1: If I2C_CTRL2.EVTINTEN= 1,When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE= 1, interrupt will be generated.
11:9	Reserved	Reserved, the reset value must be maintained.
8	DMALAST	DMA last transfer 0: Next DMA EOT is not the last transfer 1: Next DMA EOT is the last transfer *Note: This bit is used in the master receiving mode, so that a NACK can be generated when data is received for the last time.*
7	Reserved	Reserved, the reset value must be maintained.
6:0	CLKFREQ[6:0]	I^2C Peripheral clock frequency CLKFREQ[6:0] should be the APB clock frequency to generate the correct timming. 0000000: Disable 0000001: Disable 0000010: 2MHz 0000011: 3MHz ... 0100000: 32MHz 0100001~1111101: Disable

19.6.4 I^2C Own Address Register 1 (I2C_OADDR1)

Address offset: 0x08

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR MODE	Reserved	Reserved				ADDR[9:8]		ADDR[7:1]							ADDR0
rw						rw		rw							rw

Bit Field	Name	Description
15	ADDRMODE	Addressing mode (slave mode) 0: 7-bit slave address 1: 10-bit slave address
14	Reserved	Must always be kept as' 1' by the software.
13:10	Reserved	Reserved, the reset value must be maintained.
9:8	ADDR[9:8]	Interface address 9~8 bits of the address. *Note: don't care these bits in 7-bit address mode*
7:1	ADDR[7:1]	Interface address 7~1 bits of the address.

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Email：info@nationstech.com
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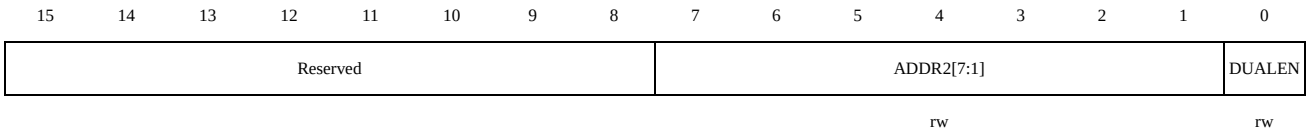
Bit Field	Name	Description
0	ADDR0	Interface address 0 bit of the address. *Note: don't care these bits in 7-bit address mode*

19.6.5 I²C Own Address Register 2 (I2C_OADDR2)

Address offset: 0x0C

Reset value: 0x0000

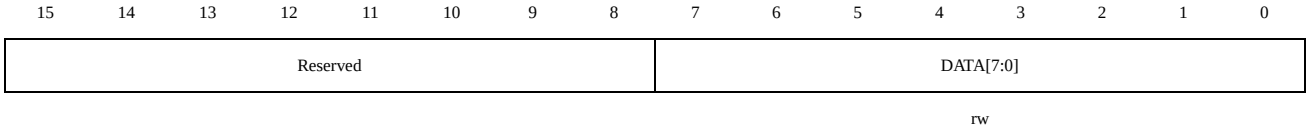


Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:1	ADDR2[7:1]	Interface address 7~1 bits of address in dual address mode.
0	DUALEN	Dual addressing mode enable 0: Disable dual address mode, only OADDR1 is recognized; 1: Enable dual address mode, both OADDR1 and OADDR2 are recognized. *Note: valid only for 7-bit address mode*

19.6.6 I²C Data Register (I2C_DAT)

Address offset: 0x10

Reset value: 0x0000



Bit Field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	DATA[7:0]	8-bit data register Send or receive data buffer. *Note: in the slave mode, the address will not be copied into the data register.* *Note: if* I2C_STS1.*TXDATE =0, data can still be written into the data register.* *Note: if the ARLOST event occurs when processing the ACK pulse, the received byte will not be copied into the data register, so it cannot be read.*

19.6.7 I²C Status Register 1 (I2C_STS1)

Address offset: 0x14

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						SCLLTO	SCLHTO	SDALTO	Reserved						
						rc_w0	rc_w0	rc_w0							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SMB ALERT	Reserved	PECERR	OVER RUN	BUSERR	ARLOST	ACKFAIL	Reserved	ADDR10F	TXDATE	RXDATNE	STOPF	BSF	ADDRF	STARTBF
	rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0		r	r	r	r	r	r	r

Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	SCLLTO	SCL low timeout error This bit is cleared by software writing ‘0’, or by hardware when I2C_CTRL1.EN=0. 0: No timeout error; 1: Timeout error occurs; Slave mode timeout: The slave device resets the communication and the hardware releases the bus. Master mode timeout: The hardware transmits a stop condition.
24	SCLHTO	SCL high timeout error This bit is cleared by software writing ‘0’, or by hardware when I2C_CTRL1.EN=0. 0: No timeout error; 1: Timeout error occurs; Slave mode timeout: The slave device resets the communication and the hardware releases the bus. Master mode timeout: The hardware transmits a stop condition.
23	SDALTO	SDA low timeout error This bit is cleared by software writing ‘0’, or by hardware when I2C_CTRL1.EN=0. 0: No timeout error; 1: Timeout error occurs; Slave mode timeout: The slave device resets the communication and the hardware releases the bus. Master mode timeout: The hardware transmits a stop condition.
22:15	Reserved	Reserved, the reset value must be maintained.
14	SMBALERT	SMBus alert Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No SMBus alert(host mode) or no SMB alert response address header sequence(slave mode); 1: SMBus alert event is generated on the pin(host mode) or receive SMBAlert response address(slave mode)
13	Reserved	Reserved, the reset value must be maintained.
12	PECERR	PEC Error in reception Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No PEC error

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: PEC error: receiver will returns NACK Whether the I2C_CTRL1.ACKEN bit is enabled
11	OVERRUN	Overrun/Underrun Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Overrun/Underrun 1: Overrun/Underrun Set by hardware in slave mode when I2C_CTRL1.NOEXTEND=1, and when receiving a new byte in receiving mode, if the data within DAT register has not been read yet, over-run occurs,the new received byte will be lost.When transferring a new byte in transfer mode, but there is not new data that has not been written in DAT register, under-run occurs which leads that the same byte will be send twice.
10	BUSERR	Bus error Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No start or stop condition error 1: Start or stop condition error
9	ARLOST	Arbitration lost (master mode) Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No arbitration lost; 1: Arbitration lost. When the interface loses control of the bus to another host, the hardware will set this bit to '1', and the I2C interface will automatically switch back to slave mode (I2C_STS2.MSMODE=0). *Note: In SMBUS mode, the arbitration of data in slave mode only occurs in the data stage or the acknowledge transfer interval (excluding the address acknowledge).*
8	ACKFAIL	Acknowledge failure Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No acknowledge failed; 1: Acknowledge failed.
7	Reserved	Reserved, the reset value must be maintained.
6	ADDR10F	10-bit header sent (Master mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No ADD10F event; 1: Master has sent the first address byte. In 10-bit address mode, when the master device has sent the first byte, the hardware sets this bit to' 1'. *Note: After receiving a NACK, the I2C_STS1.ADDR10F bit is not set.*
5	TXDATE	Data register empty (transmitters) Writing data to DAT register by software can clear this bit; Or after a start or stop condition occurs, or automatically cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is not empty;

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Email：info@nationstech.com
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Bit Field	Name	Description
		1: Data register is empty. When transmitting data, this bit is set to' 1' when the data register is empty, and it is not set at the address sending stage. If a NACK is received, or the next byte to be sent is PEC(I2C_CTRL1.PEC=1), this bit will not be set. *Note: After the first data to be sent is written, or data is written when BSF is set, the TXDATE bit cannot be cleared, because the data register is still empty.*
4	RXDATNE	Data register not empty(receivers) This bit is cleared by software reading and writing to the data register, or cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is empty; 1: Data register is not empty. During receiving data, this bit is set to' 1' when the data register is not empty, and it is not set at the address receiving stage. RXDATNE is not set when the ARLOST event occurs. *Note: When BSF is set, the RXDATNE bit cannot be cleared when reading data, because the data register is still full.*
3	STOPF	Stop detection (slave mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No stop condition is detected; 1: Stop condition is detected. After a ACK, the hardware sets this bit to' 1' when the slave device detects a stop condition on the bus. *Note: I2C_STS1.STOPF bit is not set after receiving NACK.*
2	BSF	Byte transfer finished After the software reads the STS1 register, reading or writing the data register will clear this bit; Or after sending a start or stop condition in sending mode, or when I2C_CTRL1.EN=0, this bit is cleared by hardware. 0：Byte transfer does not finish. 1：Byte transfer finished. When I2C_CTRL1.NOEXTEND =0, the hardware sets this bit to' 1' in the following cases: In receiving mode, when a new byte (including ACK pulse) is received and the data register has not been read (I2C_STS1.RXDATNE=1).In sending mode, when a new data is to be transmitted and the data register has not been written with the new data (I2C_STS1.TXDATE=1). *Note: After receiving a NACK, the BSF bit will not be set.* *If the next byte to be transferred is PEC (I2C _STS2.TRF is' 1' and I2C_CTRL1.PEC is' 1'), the BSF bit will not be set.*
1	ADDRF	Address sent (master mode) / matched (slave mode) After the STS1 register is read by software, reading the STS2 register will clear this bit, or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: Address mismatch or no address received(slave mode) or Address sending did not end(master mode);

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Tel：+86-755-86309900
Email：info@nationstech.com
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Bit Field	Name	Description
		1: Received addresses matched(slave mode) or Address sending ends(master mode) In master mode: In 7-bit address mode, this bit is set to' 1' after receiving the ACK of the address.In 10-bit address mode, this bit is set to' 1' after receiving the ACK of the second byte of the address. In slave mode: Hardware sets this bit to' 1' (when the corresponding setting is enabled) when the received slave address matches the content in the OADDR register, or a general call or SMBus device default address or SMBus host or SMBus alter is recognized. *Note: After receiving NACK, the I2C_STS1.ADDRF bit will not be set.*
0	STARTBF	Start bit (Master mode) After the STS1 register is read by software, writing to the data register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: Start condition was not sent; 1: Start condition has been sent. This bit is set to' 1' when the start condition is sent.

19.6.8 I²C Status Register 2 (I2C_STS2)

Address offset: 0x18

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PECVAL[7:0]								SMBH ADDR	SMBD ADDR	DUAL FLAG	GCALL ADDR	Reserved	TRF	MS MODE	BUSY
r								r	r	r	r		r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:8	PECVAL[7:0]	Packet error checking register Stores the internal PEC value When I2C_CTRL1.PECEN =1.
7	SMBHADDR	SMBus host header（Slave mode） Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: SMBus host address was not received; 1: when I2C_CTRL1.SMBTYPE=1 and I2C_CTRL1.ARPEN=1, SMBus host address is received.
6	SMBDADDR	SMBus device default address（Slave mode） Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: The default address of SMBus device has not been received;

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: when I2C_CTRL1.ARPEN=1, the default address of SMBus device is received.
5	DUALFLAG	Dual flag(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: Received address matches the content in OADDR1; 1: Received address matches the content in OADDR2.
4	GCALLADDR	General call address(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: No general call address was received; 1: when I2C_CTRL1.GCEN=1, general call address was received.
3	Reserved	Reserved, the reset value must be maintained.
2	TRF	Transmitter/receiver After detecting the stop condition (I2C_STS1.STOPF=1), repeated start condition or bus arbitration loss (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0, the hardware clears it. 0: Data receiving mode; 1: Data transmission mode; At the end of the whole address transmission stage, this bit is set according to the R/W bit of the address byte.
1	MSMODE	Bus busy Hardware clears this bit when a stop condition is detected. 0: No data communication on the bus; 1: Data communication on the bus. When detecting that SDA or SCL is low level, the hardware sets this bit to' 1'; *Note:This bit indicates the bus communication currently in progress, and this information is still updated when the interface is disabled (I2C_CTRL1.EN=0).*
0	BUSY	Master/slave mode Hardware clears this bit when a stop condition is detected on the bus, arbitration is lost (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0. 0: In slave mode; 1: In master mode. When the interface is in the master mode (I2C_STS1.STARTBF=1), the hardware sets this bit;

19.6.9 I²C Clock Control Register (I2C_CLKCTRL)

Address offset: 0x1C

Reset value: 0x0000

Note: the CLKCTRL register can only be set when I²C is turned off (I2C_CTRL1.EN=0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUTY	FSMODE	Reserved		CLKCTRL[11:0]											
rw	rw			rw											

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
15	DUTY	Duty cycle in fast mode 0: Tlow/Thigh = 2； 1: Tlow/Thigh = 16/9
14	FSMODE	I^2C mode selection 0: I^2C in standard mode (duty cycle default 1/1); 1: I^2C in fast mode (duty cycle configurable).
13:12	Reserved	Reserved, the reset value must be maintained.
11:0	CLKCTRL[11:0]	Clock control register in Fast/Standard mode (Master mode) This division factor is used to set the SCL clock in the master mode. • If duty cycle = Tlow/Thigh = 1/1: CLKCTRL = f_{PCLK}(Hz)/100000/2 Tlow = CLKCTRL ×T_{PCLK} Thigh = CLKCTRL ×T_{PCLK} • If duty cycle = Tlow/Thigh = 2/1: CLKCTRL = f_{PCLK}(Hz)/100000/3 Tlow = 2 ×CLKCTRL ×T_{PCLK} Thigh = CLKCTRL ×T_{PCLK} • If duty cycle = Tlow/Thigh = 16/9: CLKCTRL = f_{PCLK}(Hz)/100000/25 Tlow = 16 ×CLKCTRL ×T_{PCLK} Thigh = 9 ×CLKCTRL ×T_{PCLK} For example, if f_{PCLK}(Hz) = 8MHz, duty cycle = 1/1, CLKCTRL = 8000000/100000/2 = 0x28. *Note:* *(1) the minimum setting value is 0x04 in standard mode and 0x01 in fast mode;* *(2) T_{high}= $T_{r(SCL)}$+$T_{w(SCLH)}$. Refer to the definitions of these parameters in the data sheet for details;* *(3) T_{low}= $T_{f(SCL)}$+$T_{w(SCLL)}$, refer to the definitions of these parameters in the data sheet for details.*

19.6.10 I^2C Rise Time Register (I2C_TMRISE)

Address offset: 0x20

Reset value: 0x0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMRISE[5:0]					
										rw					

Bit Field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5:0	TMRISE[5:0]	Maximum rise time in fast/standard mode (master mode). These bits must be set to the maximum SCL rising time given in the I2C bus specification, and incremented step is 1.

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		For example, the maximum allowable SCL rise time in standard mode is 1000ns. if the value in I2C_CTRL2.CLKFREQ [5:0] is equal to 0x08(8MHz) and T_{PCLK}=125ns, 09h(1000ns/125 ns + 1) must be written in TMRISE[5:0] . If the result is not an integer, write the integer part to TMRISE[5:0] to ensure the t_{HIGH} parameter. *Note: TMRISE[5:0] can only be set when I²C is disabled (I2C_CTRL1.EN=0).*

19.6.11 I²C Master Receive Byte Register (I2C_BYTENUM)

Address offset: 0x24

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTENUMEN	RXFSEL	BYTENUM[13:0]													
rw	rw	rw													

Bit Field	Name	Description
15	BYTENUMEN	Master receive byte control enable 0: Disable 1: Enable
14	RXFSEL	Receive end send condition selection 0: master sends a STOP condition after receiving all bytes 1: master sends a START condition after receiving all bytes
13:0	BYTENUM[13:0]	Master receives bytes configuration *Note: if you need to reconfigure BYTENUM after receiving all bytes, you need to wait for I2C_STS2.BUSY is 0 and re-enabled I2C_CTRL1.ACKEN*

19.6.12 I²C Filter Control Register (I2C_GFLTRCTRL)

Address offset: 0x28

Reset value: 0x0000

Note: the GFLTRCTRLregister can only be set when I²C is turned off (I2C_CTRL1.EN=0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLAFENN	Reserved	SCLAFW[1:0]		SDAAFENN	Reserved	SDAAFW[1:0]		SCLDFW[3:0]				SDADFW[3:0]			
rw		rw		rw		rw		rw				rw			

Bit Field	Name	Description
15	SCLAFENN	SCL analog filter enable. 0: Enable 1: Disable
14	Reserved	Reserved, the reset value must be maintained.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
13:12	SCLAFW[1:0]	SCL analog filter width selection 00: 5ns 01: 15ns 10: 25ns 11: 35ns
11	SDAAFENN	SDA analog filter enable. 0: Enable 1: Disable
10	Reserved	Reserved, the reset value must be maintained.
9:8	SDAAFW[1:0]	SDA analog filter enable 0: Enable 1: Disable
7:4	SCLDFW[3:0]	SCL digital filter width selection 0000: Disable SCL digital filter Others: Filter width is SCLDFW * T_{PCLK}
3:0	SDADFW[3:0]	SDA digital filter width selection 0000: Disable SDA digital filter Others: Filter width is SDADFW * T_{PCLK}

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

20 Universal Asynchronous Receiver Transmitter (UART)

20.1 Introduction

UART is a full-duplex universal synchronous/asynchronous serial transceiver module. This interface is a highly flexible serial communication device that can perform full-duplex data exchange with external devices.

The UART has programmable transmit and receive baud rates and can communicate continuously using DMA. It also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smartcard asynchronous protocol, IrDA SIR ENDEC function.

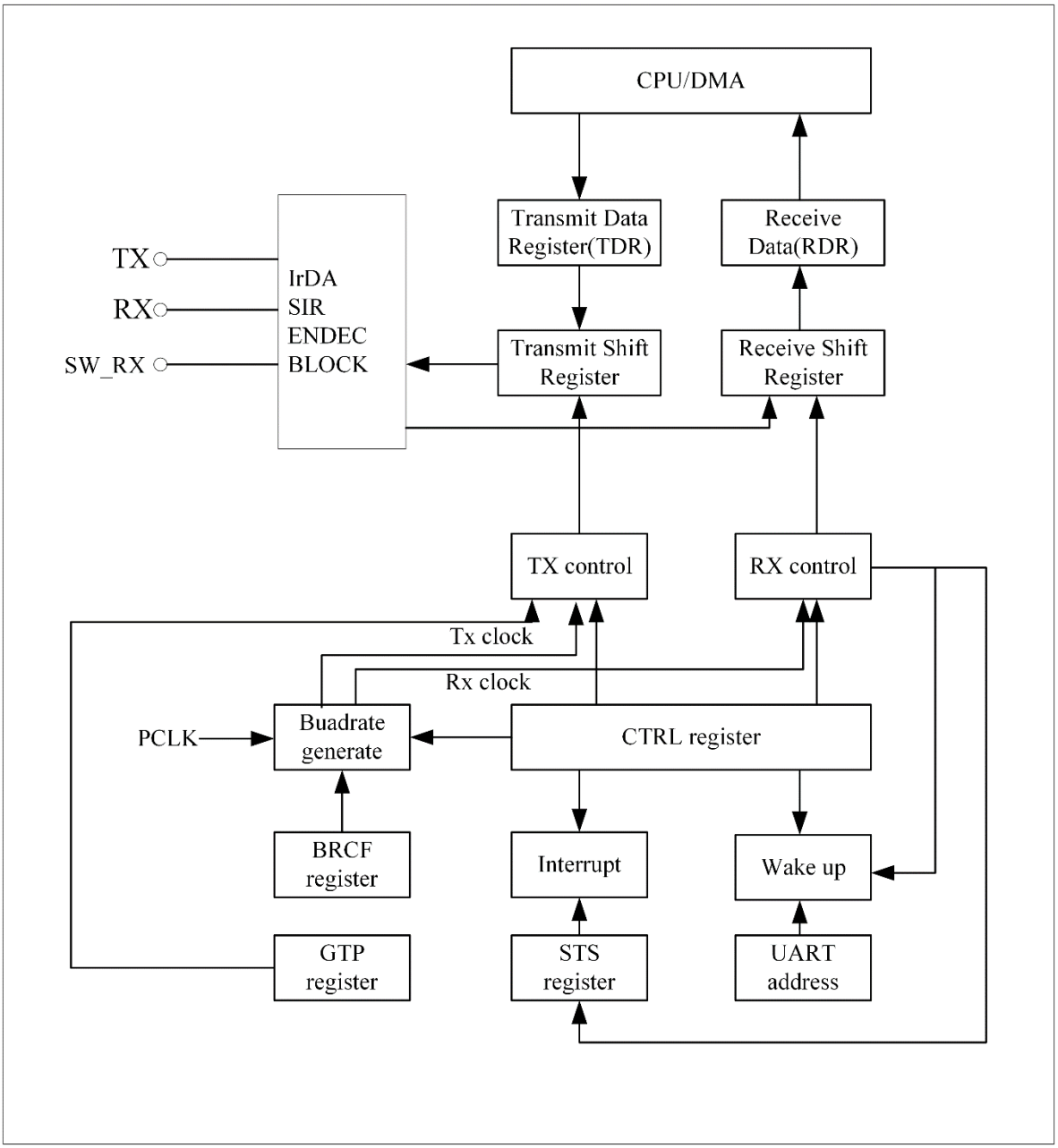
20.2 Main Features

- Support Full duplex communication
- Support Single-wire half-deplex commnication
- Baud rate programmable, up to 4Mbit/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- Support hardware generation of parity bit and check parity bit
- Support DMA receiving/transmitting
- Multi-processor communication, if the address does not match, then enter the silent mode, Wake up from silent mode via idle bus detection or address flag detection
- Supports serial infrared protocol (IrDA SIR) encoding and decoding, providing two operating modes: normal and low-power
- Support LIN mode
- Support four error detection: Overflow error, Frame error, Noise error, Parity error
- Support multiple interrupt requests: Send data register empty, Send complete, Data received, Overflow error, Bus Idle, Parity error, LIN break detection and noise flag/overflow error/frame error in multi-buffer communication.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

20.3 Functional Block Diagram

Figure 20-1 UART Block Diagram



20.4 Function Description

As shown in the Figure 20-1, the bidirectional communications of any UART need to use the RX and TX pins of the external connection. Among them, TX is the output pin for serial data transmission. When the transmitter is active and not sending data, the TX pin is pulled high. When the transmitter is inactive, the TX pin reverts to the I/O port configuration. RX is an input pin for serial data reception, data is received by the oversampling technique.

The data packets of serial communication are transmitted from the sending device to the RX interface of the receiving device through its own TX interface, and the bus is in an idle state before transmitting or receiving. Frame format is: 1 start

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

bit + 8 or 9 data bits (least significant bit first) + 1 parity bit (optional) + 0.5,1,1.5 or 2 stop bit.

Use the fractional baud rate generator to configure transmit and receive baud rates.

20.4.1 UART Frame Format

Start bit: 1 bit, active low

Data bits: Configurable via UART_CTRL1.WL as 8 or 9 bits, with the LSB first.

Stop bit: Active high.

Idle frame: A complete data frame consisting entirely of '1's, including the start bit. followed by the start bit of a data frame containing the data.

Break frame: A break frame is a complete data frame consisting of '0's, including the stop bit. at the end of the break frame, the transmitter inserts 1 or 2 more stop bits ('1') to acknowledge the start bit.

Figure 20-2 Word Length = 8 Setting

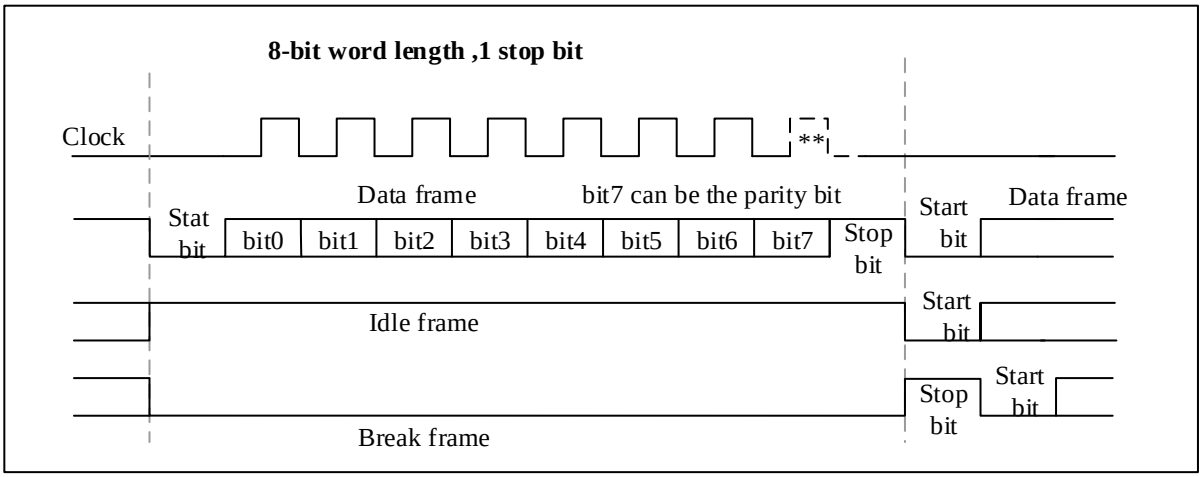
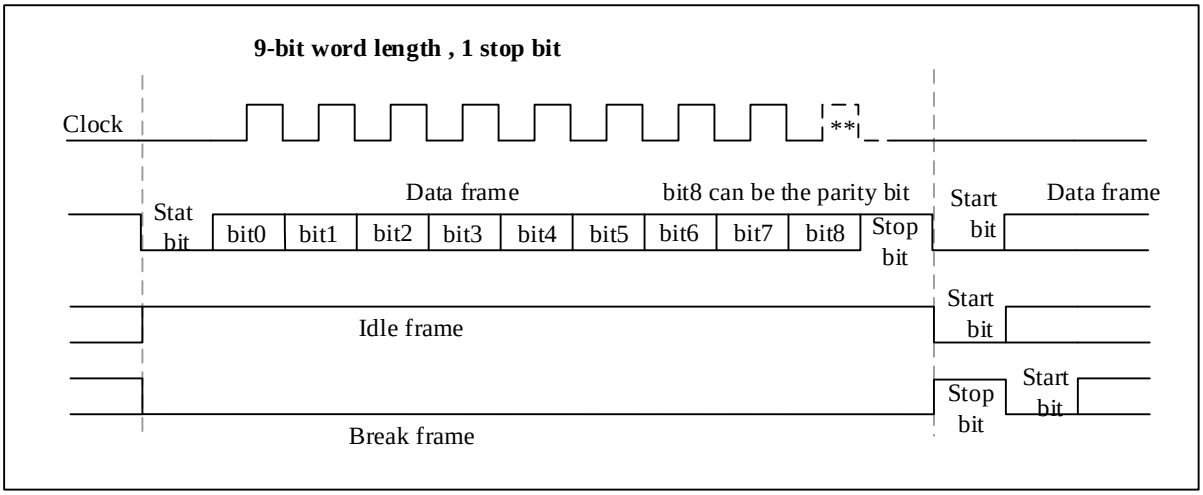


Figure 20-3 Word Length = 9 Setting



20.4.2 Transmitter

After the transmitter is enabled, the data in the transmit shift register is sent out through the TX pin.

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Nanshan District, Shenzhen, 518057, P.R.China

20.4.2.1 Idle frame

Setting UART_CTRL1.TXEN will cause the UART to transmit an idle frame before the first data frame.

20.4.2.2 Character transmission

Idle frames are followed by characters sent. Each character is preceded by a low start bit. The transmitter sends 8-bit or 9-bit data according to the configuration of the data bit length, with the least significant bit first. If UART_CTRL1.TXEN is reset during a data transfer, it will cause the baud rate counter to stop counting and the data being transferred will be corrupted.

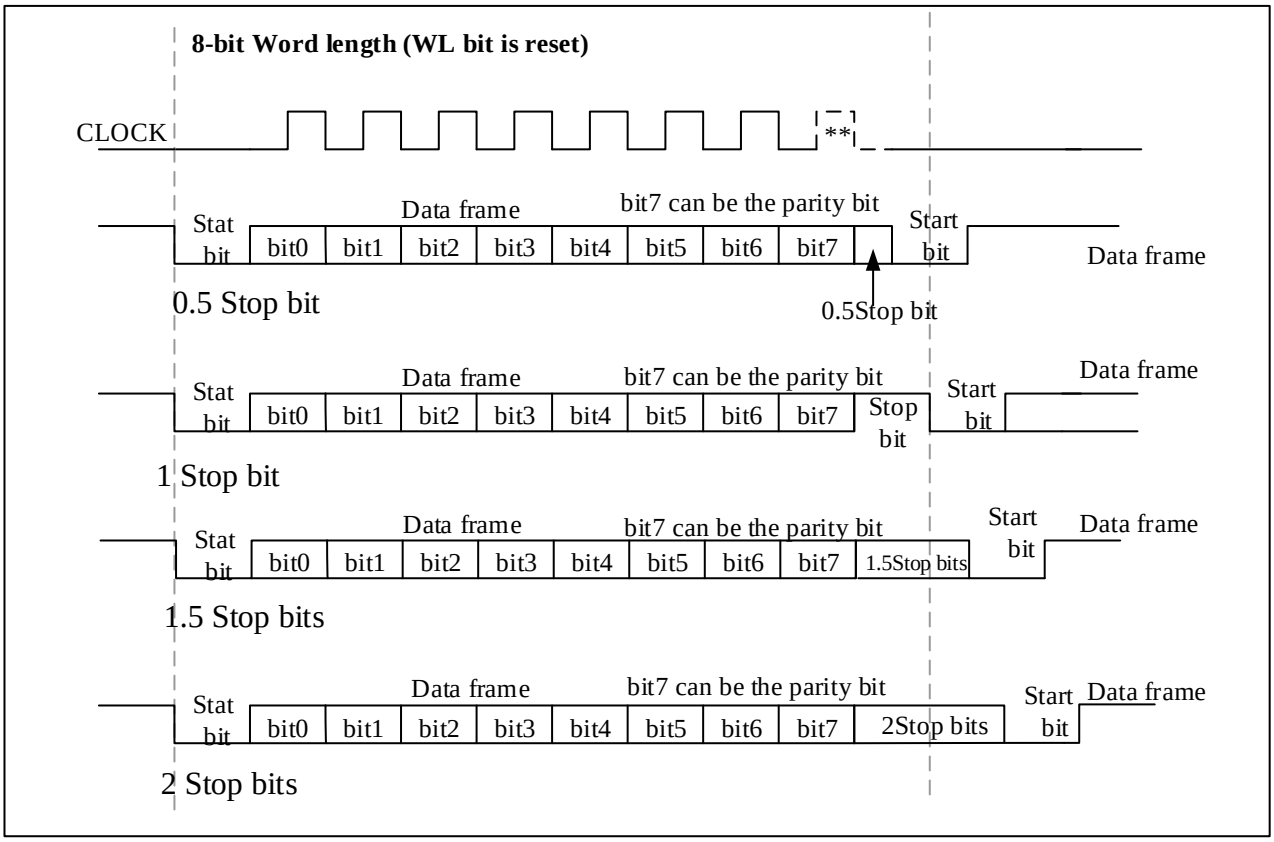
20.4.2.3 Stop bit

The characters are followed by stop bits, the number of which can be configured by setting UART_CTRL2. STPB[1:0].

Table 20-1 Stop Bit Configuration

UART_CTRL2.STPB[1:0]	Stop Bit Length (Bits)	Functional Description
00	1	Default
01	0.5	
10	2	General UART mode, single-wire mode and modem mode.
11	1.5	

Figure 20-4 Configuration Stop Bit



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Email：info@nationstech.com
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20.4.2.4 Break frame

Use UART_CTRL1.SDBRK to send the break character. When there is 8-bit data, the break frame consists of 10 bits of low level, followed by a stop bit; when there is 9-bit data, the break frame consists of 11 bits of low level, followed by a stop bit.

After the break frame is sent, UART_CTRL1.SDBRK is cleared by hardware, and the stop bit of the break frame is automatically sent. Therefore, to send a second break frame, UART_CTRL1.SDBRK should be set after the stop bit of the previous break frame has been sent.

If software resets the UART_CTRL1.SDBRK bit before starting to send the break frame, the break frame will not be sent.

20.4.2.5 Sending process

1. Enable UART_CTRL1.UEN to activate UART;
2. Configure the transmitter's baud rate, data bit length, parity bit (optional), the number of stop bits or DMA configuration;
3. Activate the transmitter (UART_CTRL1.TXEN);
4. Send each data to be sent to the UART_DAT register through the CPU or DMA, and the write operation to the UART_DAT register will clear UART_STS.TXDE;
5. After writing the last data word in the UART_DAT register, wait for UART_STS.TXC =1, which indicates the end of the transmission of the last data frame.

20.4.2.6 Single byte communication

A write to the UART_DAT register clears the UART_STS.TXDE bit.

The UART_STS.TXDE bit is set by hardware when the data in the TDR register is transferred to the transmit shift register (indicating that data is being transmitted). An interrupt will be generated if UART_CTRL1.TXDEIEN is set. At this point, the next data can be sent to the UART_DAT register because the TDR register has been cleared and will not overwrite the previous data

Write operation to UART_DAT register:

- When the transmit shift register is not sending data and is in an idle state, the data is directly put into the shift register for transmission, and the UART_STS.TXDE bit is set by hardware;
- When the transmit shift register is sending data, the data is stored in the TDR register, and after the current transmission is completed, the data is put into the shift register.

When a frame containing data is sent and UART_STS.TXDE=1, the UART_STS.TXC bit is set to '1' by hardware. An interrupt is generated if UART_CTRL1.TXCIEN is '1'. UART_STS.TXC bit is cleared by a software sequence (read UART_STS register first, then write UART_DAT register).

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Tel：+86-755-86309900
Email：info@nationstech.com
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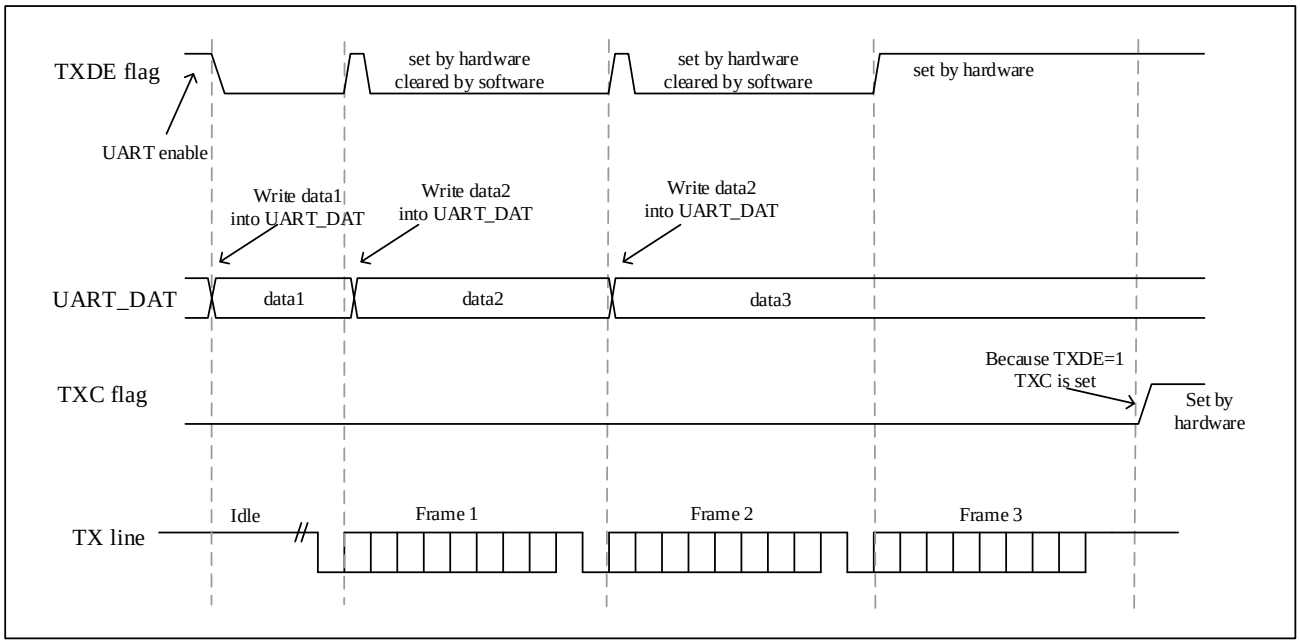
Figure 20-5 TXC/TXDE Changes During Transmission



20.4.3 Receiver

20.4.3.1 Start bit detection

When the received sampling sequence is: 1 1 1 0 X 0 X 0 X 0 0 0 0, it is considered that a start bit is detected.

The samples at the 3rd, 5th, and 7th bits, and the samples at the 8th, 9th, and 10th bits are all '0' (that is, 6 '0'), then confirm the receipt of the start bit, the UART_STS.RXDNE flag bit is set, and if UART_CTRL1.RXDNEIEN=1, an interruption occurs and will not Set the NEF noise flag.

If there are two '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are two '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, but the NE noise flag will be set.

If there are three '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are two '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, and the NE noise flag will be set.

If there are two '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are three '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, and the NE noise flag will be set

If the sampling values in the 3rd, 5th, 7th, 8th, 9th and 10th bits cannot meet the above four requirements, the UART receiver thinks that it has not received the correct start bit, and will exit the start bit detection and return to idle state and wait for falling edge.

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Email：info@nationstech.com
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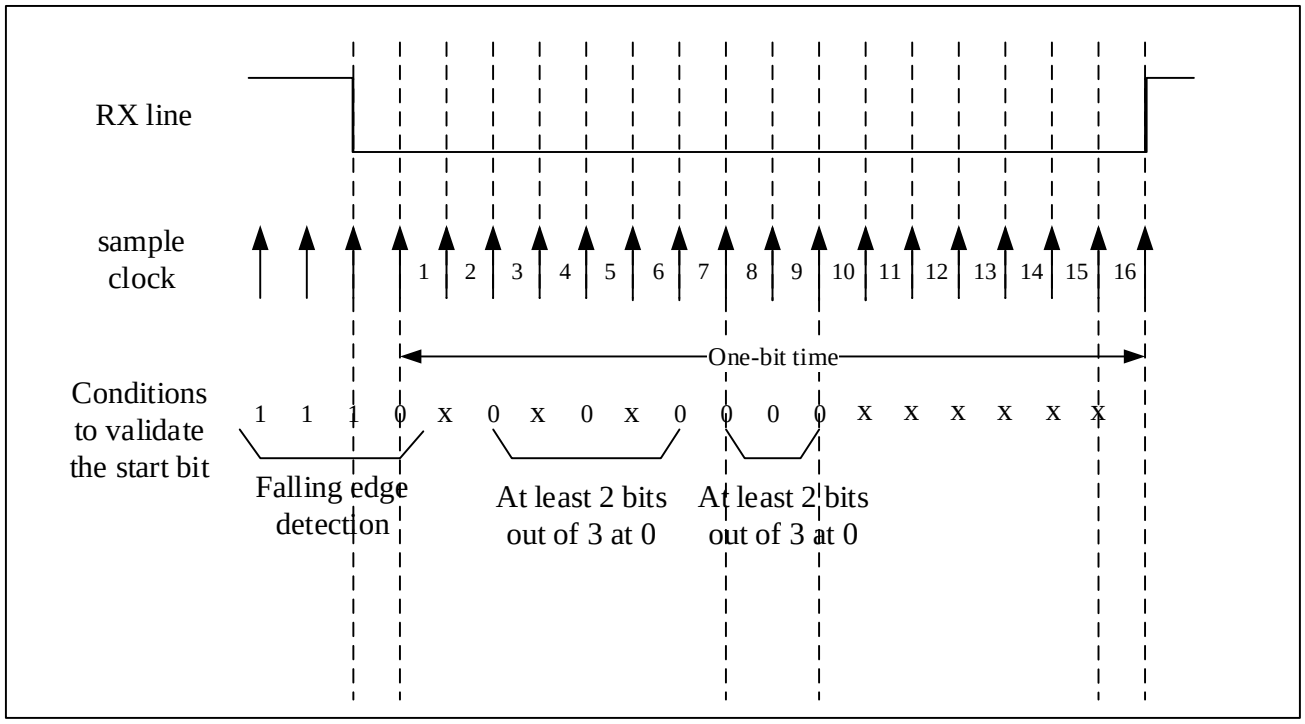
Figure 20-6 Start Bit Detection



20.4.3.2 Stop bit description

The number of data stop bits can be configured by the UART_CTRL2.STPB[1:0]. In normal mode, 1 or 2 stop bits can be selected.

1. 0.5 stop bits (receive in smartcard mode): 0.5 stop bits are not sampled. Therefore, if 0.5 stop bits is selected, framing errors and broken frames cannot be detected.
2. 1 stop bit: sampling for 1 stop bit is done on the 8th, 9th and 10th samples.
3. 1.5 stop bits: The 1.5 stop bits are sampled at points 16, 17 and 18. The 1.5 stop bits can be divided into two parts: one is 0.5 clock cycles, during which nothing happens. This is followed by the stop bit of 1 clock cycle, which is sampled at the midpoint of this period of time
4. 2 stop bits: the sampling of the 2 stop bits is completed at the 8th, 9th and 10th sampling points of the first stop position. If a frame error is detected during the first stop bit, the frame error flag is set. The second stop bit does not detect framing error. The UART_STS.RXNE flag will be set at the end of the first stop bit.

20.4.3.3 Receiver process

1. Enable UART_CTRL1.UEN to activate UART;
2. Configure the receiver's baud rate, data bit length, parity bit (optional), stop bit number or DMA configuration;
3. Activate the receiver (UART_CTRL1.RXEN) and start looking for the start bit;
4. The receiver receives 8-bit or 9-bit data according to the configuration of the data bit length, and the least significant bit of the data is first shifted from the RX pin into the receive shift register;
5. When the data of the received shift register is moved to the RDR register, UART_STS.RXDNE is set, and the data can be read out. If UART_CTRL1.RXNEIEN is 1, an interrupt will be generated;

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6. When an overflow error, noise error, or frame error is detected in the received frame, the corresponding error flag status bit will be set. If UART_CTRL1.RXEN is reset during data transmission, the data being received will be lost;
7. UART_STS.RXDNE is set after receiving data, and a read operation of UART_DAT can clear this bit.

- During multi-buffer communication mode, by performing DMA read operations on the data register, the UART RXDNE reset to zero.
- During single-buffer communication mode, by performing software read operations on the data register, the UART RXDNE reset to zero.

20.4.3.4 Idle frame detection

When an idle frame is detected, UART.STS.IDLEF is set to 1. If UARD_CTRL1.IDLEIEN is set to 1 at this time, an interrupt will be generated. UART_STS.IDLEF bit is cleared by a software sequence (read UART_STS register first, then read UART_DAT register).

20.4.3.5 Break frame detection

The frame error flag(UART_STS.FEF) is set by hardware when the receiver detects a break frame. It can be cleared by a software sequence (read UART_STS register first, then read UART_DAT register).

20.4.3.6 Framing error

A framing error occurs when a stop bit is not received and recognized at the expected time. At this time, the frame error flag UART_STS.FEF will be set by hardware, and the invalid data will be transferred from the shift register to the UART_DAT register. During single-byte communication, no interrupt framing error will be generated because it occurs with UART_STS.RXDNE and the hardware will generate an interrupt when the UART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt will be generated if the UART_CTRL3.ERRIEN bit is set.

20.4.3.7 Overrun error

When UART_STS.RXDNE is still '1', and the data currently received in the shift register needs to be transferred to the RDR register, an overflow error will be detected, and the hardware will set UART_STS.OREF. When this bit is set, the value in the RDR register is not lost, but the data in the shift register is overwritten. It is cleared by a software sequence (read UART_STS register first, then write UART_DAT register).

When an overflow error occurs, if UART_SS RXDNEIEN has been set to 1, which will generate a receive interrupt. If the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the UART_STS.OREF flag is set in multi-buffer communication mode.

20.4.3.8 Noise error

UART_STS.NEF is set by hardware when noise is detected on a received frame. It is cleared by software sequence (read UART_STS register first, then write UART_DAT register). During single-byte communication, no noise interrupt generated because it occurs with UART_STS.RXDNE and the hardware will generate an interrupt when the UART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt is generated when the UART_STS.NEF flag is set if the UART_CTRL3.ERRIEN bit is set.

Table 20-2 Data Sampling for Noise Detection

Sample Value	NE Status	Received Bits	Data Validity
000	0	0	Effective

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

001	1	0	Be invalid
010	1	0	Be invalid
011	1	1	Be invalid
100	1	0	Be invalid
101	1	1	Be invalid
110	1	1	Be invalid
111	0	1	Effective

20.4.4 Fractional Baud Rate Calculation

The baud rate of the UART can be configured in the UART_BRCF register. This register defines the integer and fractional parts of the baud rate divider. The baud rate of the transmitter and receiver should be configured to the same value. Be careful not to change the value of the UART_BRCF register during communication, because the baud rate counter will be replaced by the new value of the baud rate register

$$\text{TX / RX baud rate} = f_{PCLK} /(16 * \text{UARTDIV})$$

where f_{PCLK} is the clock provided to the peripheral

- PCLK2 is used for UART1/UART2, up to 64MHz
- PCLK1 is used for UART3/UART4/UART5, up to 32MHz.

UARTDIV is an unsigned frequency division coefficient.

20.4.4.1 UARTDIV and UART_BRCF register configuration

Example 1:

If DIV_Integer = 27, DIV_Decimal = 12 (UART_ BRCF =0x1BC), then

DIV_Integer (UARTDIV) = 27

DIV_Decimal (UARTDIV) = 12/16 = 0.75

So, UARTDIV = 27.75

Example 2:

If UARTDIV = 25.62, then：

DIV_Decimal = 16*0.62 = 9.92

Nearest integer: 10 = 0x0A

DIV_Integer = DIV_Integer (25.620) = 25 = 0x19

So, UART_ BRCF = 0x19A

Example 3:

If UARTDIV = 50.99 then：

DIV_Decimal = 16*0.99 = 15.84

Nearest integer: 16 = 0x10 => DIV_Decimal[3:0] out of configurable range, so a carry to integer is required

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Email：info@nationstech.com
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DIV_Integer = DIV_Integer (0d50.990+carry) = 51 = 0x33

So, UART_ BRCF = 0x330

Table 20-3 Error Calculation When Setting Baud Rate

Baud Rate		**f_{PCLK} = 32MHz**			**f_{PCLK} = 36MHz**		
Serial Number	Kbps	Reality	Set value in register	Error(%)	Reality	Set value in register	Error(%)
1	2.4	2.400	833.3125	0%	2.400	937.5	0%
2	9.6	9.601	208.3215	0.01%	9.600	234.375	0%
3	19.2	19.196	104.1875	0.02%	19.200	117.1875	0%
4	57.6	57.554	34.750	0.08%	57.600	39.0625	0%
5	115.2	115.108	17.375	0.08%	115.016	19.5625	0.16%
6	230.4	230.216	8.6875	0.08%	230.769	9.75	0.16%
7	460.8	463.768	4.3125	0.64%	461.538	4.875	0.16%
8	921.6	914.286	2.1875	0.79%	923.077	2.4375	0.16%
9	2250	Impossible	Impossible	Impossible	2250.000	1	0%
10	3000	Impossible	Impossible	Impossible	Impossible	Impossible	Impossible
11	4000	Impossible	Impossible	Impossible	Impossible	Impossible	Impossible
Baud Rate		**f_{PCLK} = 48MHz**			**f_{PCLK} = 64MHz**		
Serial Number	Kbps	Reality	Set value in register	Error(%)	Reality	Set value in register	Error(%)
1	2.4	2.400	1250	0%	2.400	1666.6875	0%
2	9.6	9.600	312.5	0%	9.600	416.6875	0%
3	19.2	19.200	156.25	0%	19.202	208.3125	0.01%
4	57.6	57.600	52.0625	0.04%	57.606	69.4375	0.01%
5	115.2	115.016	26.0625	0.08%	115.108	34.750	0.08%
6	230.4	230.769	13	0.16%	230.216	17.375	0.08%

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7	460.8	461.538	6.5	0.16%	460.432	8.6875	0.08%
8	921.6	923.077	3.25	0.16%	927.536	4.3125	0.64%
9	2250	2285.714	1.3125	1.59%	2285.714	1.75	1.59%
10	3000	3000.000	1.000	0%	3047.619	1.3125	1.59%
11	4000	Impossible	Impossible	Impossible	4000.000	1.000	0%

Notes: The lower the clock frequency of the CPU, the lower the error for a particular baud rate.

20.4.5 UART Receiver's Tolerance Clock Deviation

Variations due to transmitter errors (including transmitter side oscillator variations), receiver side baud rate rounding errors, receiver side oscillator variations, variations due to transmission lines (usually due to The inconsistency between the low-to-high transition timing of the transceiver and the high-to-low transition timing of the transceiver), these factors will affect the overall clock system variation. Only when the sum of the above four changes is less than the tolerance of the UART receiver, the UART asynchronous receiver can work normally.

When receiving data normally, the tolerance of UART receiver is the maximum tolerable variation, depending on the selection of data bit length and whether to use fractional baud rate division coefficient.

Table 20-4 When DIV_Decimal = 0, Tolerance of UART Receiver

WL Bit	NEF Is An Error	NEF Is Don't Care
0	3.75%	4.375%
1	3.41%	3.97%

Table 20-5 When DIV_Decimal != 0, Tolerance of UART Receiver

WL Bit	NEF Is An Error	NEF Is Don't Care
0	3.33%	4.0%
1	3.03%	3.63%

20.4.6 Parity Control

Parity can be enabled by configuring the UART_CTRL1.PCEN bit.

When the parity bit is enabled for transmission, a parity bit is generated, parity check is performed on reception.

Table 20-6 Frame Format

WL Bit	PCEN Bit	UART Frame
0	0	| Start bit | 8-bit data | Stop bit |
0	1	| Start bit | 7 bits of data | Parity bit | Stop bit |
1	0	| Start bit | 9-bit data | Stop bit |

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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1	1	| start bit | 8-bit data | parity bit | stop bit |

Even parity

Configure UART_CTRL1.PSEL to 0, and even parity can be selected.

Make the number of '1' in the transmitted data (including parity bit) be an even number. For example: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total). The receiver confirms the number of '1's in the data If it is an even number, the check is passed, indicating that no errors occurred during the transmission process. If it is not even, it means that an error has occurred, the UART_STS.PEF flag is set to '1', and if UART_CTRL1.PEIEN is enabled, an interrupt is generated.

Odd parity

Configure UART_CTRL1.PSEL to 1, you can choose odd parity.

Make the number of '1' in the transmitted data (including parity bit) be an odd number. For example: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total). The receiver confirms the number of '1's in the data If it is an odd number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an odd number, it means that an error has occurred, the UART_STS.PEF flag is set to '1', and if UART_CTRL1.PEIEN is enabled, an interrupt is generated.

20.4.7 DMA Communication

The UART supports the DMA mode using multi-buffer configuration, which can realize high-speed data communication.

20.4.7.1 DMA transmission

Set UART_CTRL3.DMATXEN to enable DMA mode when transmitting. When the UART's transmit shift register is empty (UART_STS.TXDE=1), the DMA will transfer the data from the SRAM to the UART_DAT register of the UART.

When using DMA transmission, the process of configuring the DMA channel is as follows:

1. Set the address of the data memory. When a data transfer request occurs, the transferred data will be read from this address.
2. Set the address of the UART_DAT register. When a data transfer request occurs, this address will be the destination address of the data transfer.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the current DMA channel.
6. After the data transfer is completed, the transfer complete flag (DMA_INTSTS.TXCFx) is set to 1.

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Tel：+86-755-86309900
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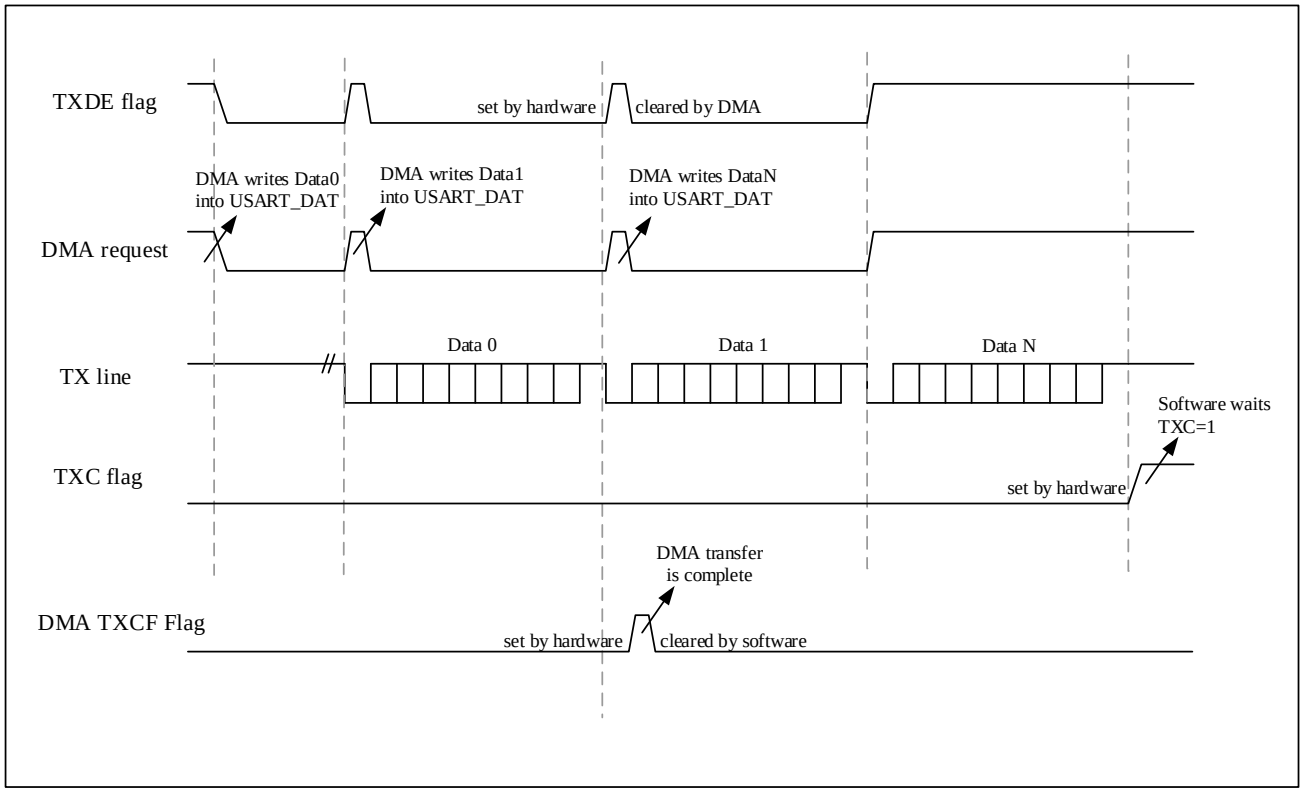
Figure 20-7 Transmission Using DMA



20.4.7.2 DMA reception

Set UART_CTRL3.DMARXEN to enable DMA mode when receiving. When a byte is received (UART_STS.RXDNE=1), the DMA will transfer the data from the UART_DAT register of the UART to the SRAM.

When using DMA reception, the process of configuring the DMA channel is as follows:

1. Set the address of the UART_DAT register. When a data transfer request occurs, this address will be the source address of the data transfer
2. Set the address of the data memory. When a data transfer request occurs, the transferred data will be written to this address
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the current DMA channel.

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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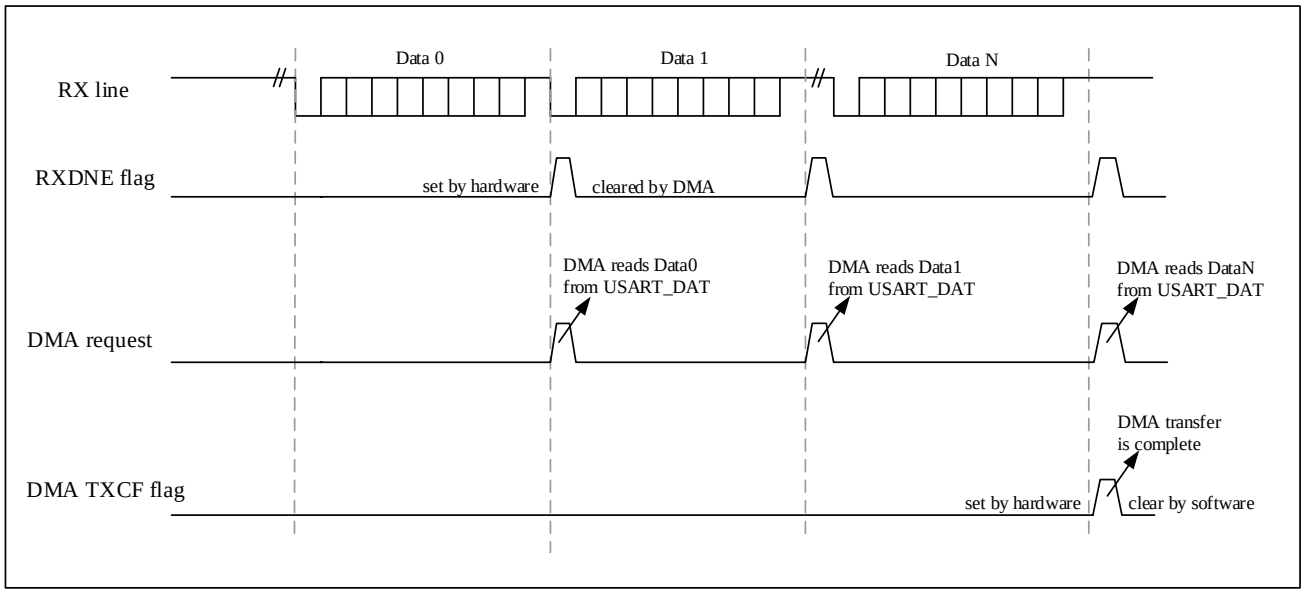
Figure 20-8 Reception Using DMA



In multi-buffer communication mode, the error flag will be set when there is a frame error, overrun error or noise error. An interrupt will be generated if the error interrupt is enabled (UART_CTRL3.ERRIEN=1).

20.4.8 Multiprocessor Communication

UART allows multiprocessor communication. When multiple processors communicate through UART, it is necessary to determine who is the master device, and the remaining processors are all slave devices. The TX output of the master device is directly connected to the RX port of all slave device. The TX outputs of the slaves are logically AND together and connected to the RX inputs of the master.

When multi-processor communication is performed, the slave devices are all in mute mode, and the host uses a specific method to wake up a slave device to be communicated when needed, so that the slave device is in an active state and transmits data with the master device.

The UART can wake up from mute mode by idle bus line detection or address mark detection.

20.4.8.1 Idle bus line detection

The idle bus line detection configuration process is as follows:

1. Configure the UART_CTRL1.WUM bit to 0, and the UART performs idle bus line detection.
2. When UART_CTRL1.RCVWU is set (which can be automatically controlled by hardware or written by software under certain conditions), UART enters mute mode. In mute mode, none of the receive status bits are set, and all receive interrupts are disabled.
3. As shown in the Figure 20-9, when an idle frame is detected, UART is woken up, and then UART_CTRL1.RCVWU is cleared by hardware. At this time, UART_STS.IDLEF is not set.

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Tel：+86-755-86309900
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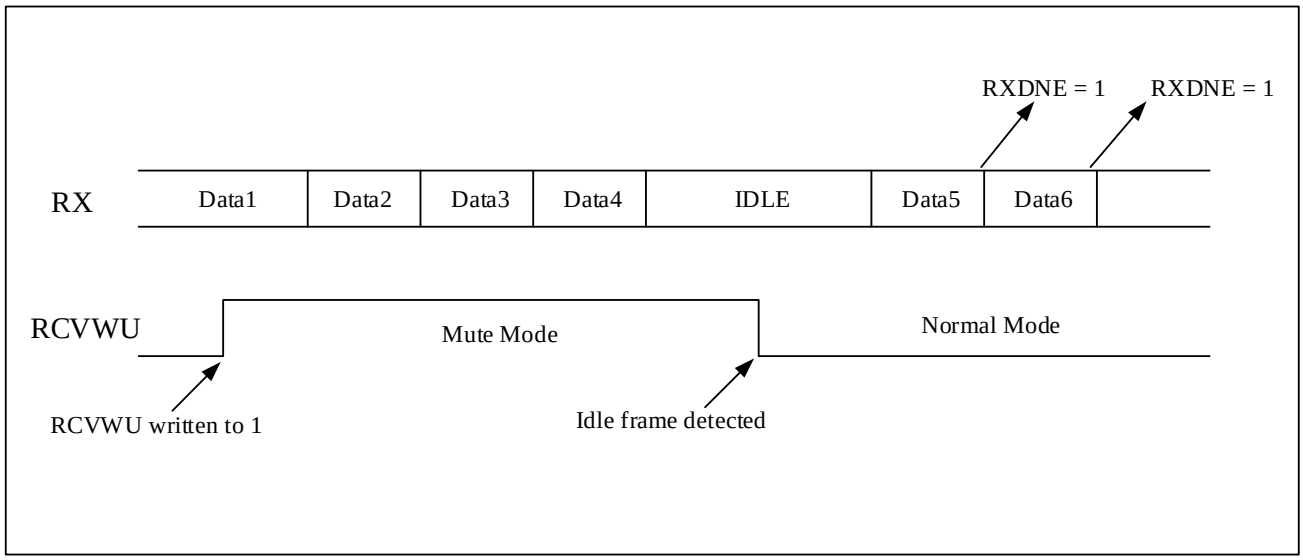
Figure 20-9 Mute Mode Using Idle Line Detection



20.4.8.2 Address mark detection

By configuring the UART_CTRL1.WUM bit to 1, the UART performs address mark detection. The address of the receiver is programmable through the UART_CTRL2.ADDR[3:0] bits. If the MSB is 1, the byte is considered as an address, otherwise it is considered as data

In this mode, the UART can enter mute mode by:

- When the receiver does not contain data, UART_CTRL1.RCVWU can be written to 1 by software, and UART enters mute mode

  Note: When the receive buffer contains no data (RXNE=0 in UART_SR), the UART_CTRL1.RCVWU bit can be written to 0 or 1. Otherwise, the write operation is ignored.

- When the received address does not match the address of the UART_CTRL2.ADDR[3:0] bits, UART_CTRL1.RCVWU is written to 1 by hardware.

In silent mode, none of the receive status bits are set and all receive interrupts are disabled.

When the address received by the receiver matches the preset address identifier, the UART is woken up and UART_CTRL1.RCVWU is cleared. The UART_STS.RXDNE bit will be set when this matching address is received. Data can then be transmitted normally.

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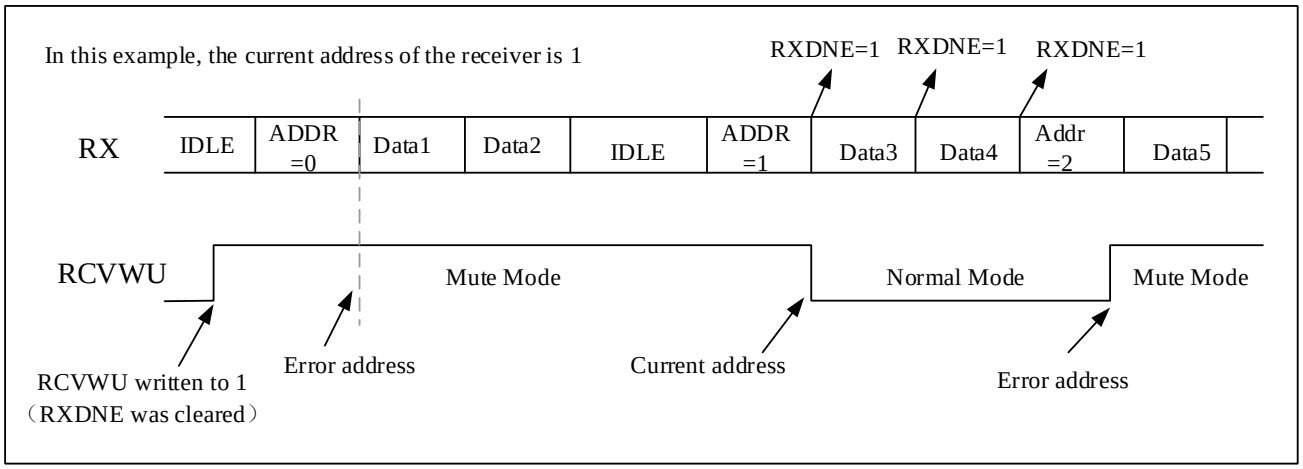
Figure 20-10 Mute Mode Detected Using Address Mark



20.4.9 Single-wire Half-duplex Mode

UART supports single-wire half-duplex communication, allowing data to be transmitted in both directions, but only allows data to be transmitted in one direction at the same time. Communication conflicts are managed by software.

Select the single wire half duplex mode by setting the UARD_CTRL3.HDMEN bit. At this time, all of the following control bits must be reset to zero: UARD_CTRL2.LINMEN、UART_CTRL3.IRDAMEN。

After the half-duplex mode is turned on, the TX pin and the RX pin are internally connected, and the RX pin is no longer used. When there is no data to be transmitted, TX is always released. Therefore, when not driven by the UART, the TX pin must be configured as a floating input or an open-drain output high.

20.4.10 Serial IrDA Infrared Encoding/Decoding Mode

UART supports the IrDA (Infrared Data Association).

Through the UART_CTRL3. IRDAMEN bit, you can choose whether to enable the infrared mode. When using the infrared function, UART_CTRL2.STPB[1:0], UART_CTRL2.LINMEN, UART_CTRL3.HDMEN these bits should be kept clear

Through the UART_CTRL3. IRDALP bit, it can be used to select normal mode or low power infrared mode.

20.4.10.1 IrDA normal mode

When UART_CTRL3.IRDALP=0, select normal infrared mode.

IrDA is a half-duplex communication protocol, so there should be a minimum delay of 10ms between sending and receiving, that uses a inverted return-to-zero modulation scheme (RZI), which uses an infrared light pulse to represent a logic '0', and the pulse width is specified as 3/16 of a bit period in normal mode, as shown in Figure 20-12 the UART only supports up to 115200bps.

The UART sends data to the SIR encoder, and the bit stream output by the UART will be modulated. A modulated stream of pulses is sent from the infrared transmitter and then received by the infrared receiver. The SIR receiver decoder demodulates it and outputs the data to the UART.

The encoder and decoder have opposite input polarities. When idle, the encoder output is low level, while the decoder input is high level. The encoder outputs a high pulse to represent logic 0 and a low level as logic 1. The decoder input is the opposite.

If the UART is sending data to the IrDA transmit encoder, then the IrDA receive decoder will ignore any data on the IrDA

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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receive line. If the UART is receiving data sent from the SIR receiver decoder, the data sent by the UART to the IrDA transmitter encoder will not be encoded.

Pulse width is programmable. The IrDA specification requires pulses to be wider than 1.41us. For pulse widths less than 2 cycles, the receiver will filter them out. PSCV is the prescaler value programmed in the UART_GTP register.

20.4.10.2 IrDA low power mode

When UART_CTRL3.IRDALP=1, select low power infrared mode.

For the transmitter, when in low power mode, the pulse width is 3 times the low power baud rate, which is a minimum of 1.42MHz. Typically this value is 1.8432MHz (1.42 MHz < PSC < 2.12 MHz).

For the receiver, the requirement for a valid signal is that the duration of the low level signal must be greater than 2 PSCV cycles.

Figure 20-11 IrDA SIR ENDEC-Block Diagram

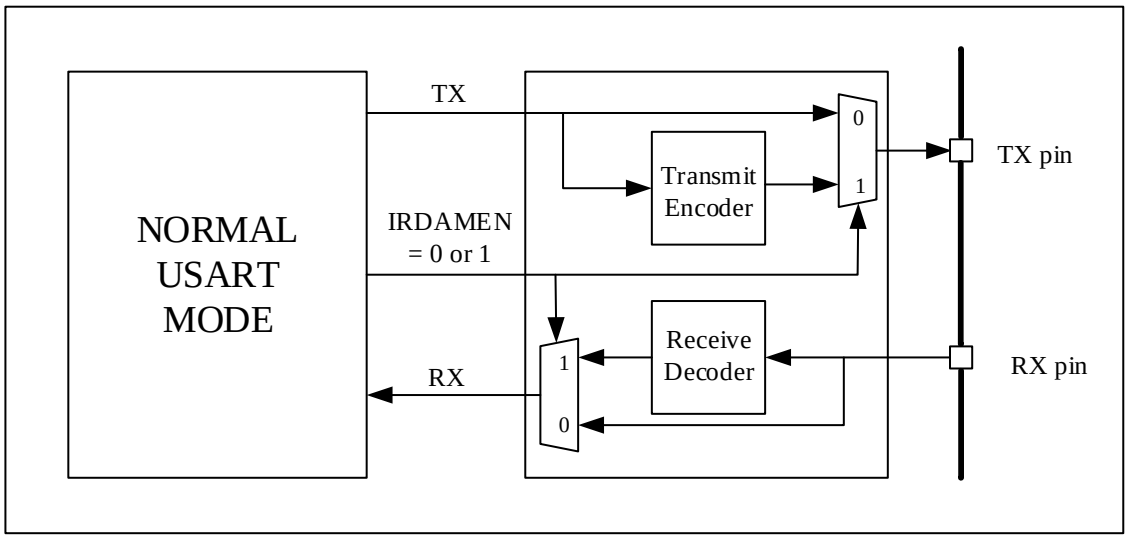
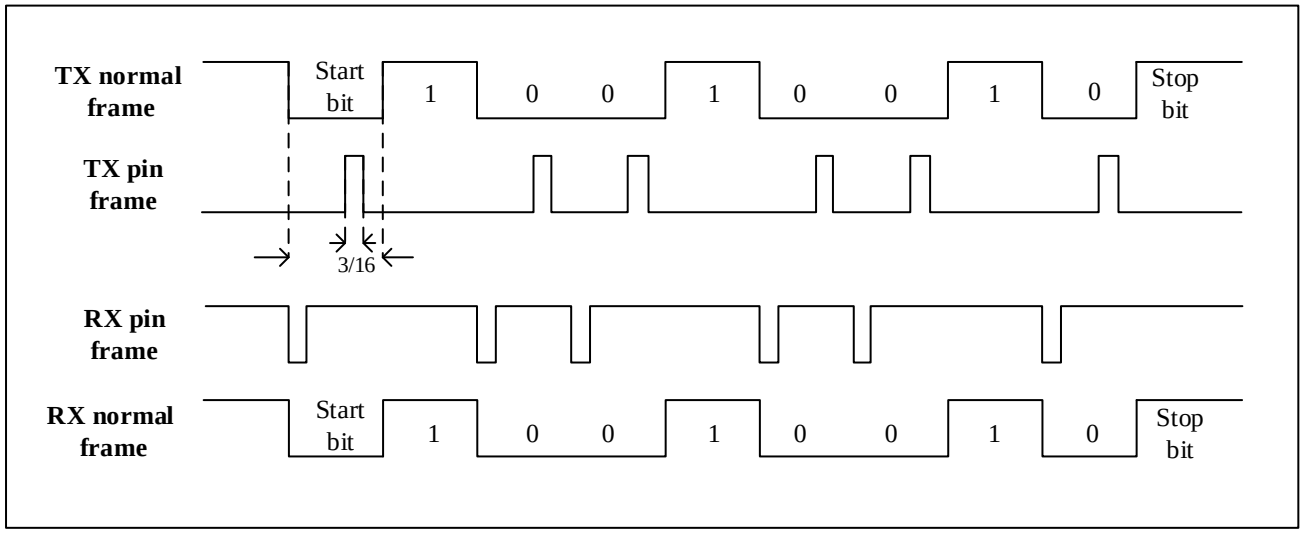


Figure 20-12 IrDA Data Modulation (3/16)-Normal Mode



20.4.11 LIN Mode

UART supports the ability of a LIN(Local interconnection Network) master to send a synchronization break and the ability

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of a LIN slave to detect a break. LIN mode can be enabled by configuring the UART_CTRL2.LINMEN bit.

Note: When using LIN mode, UART_CTRL2.STPB[1:0], UART_CTRL3.HDMEN, UART_CTRL3. IRDAMEN, these bits should be kept clear.

20.4.11.1 LIN transmission

When LIN is sent, the length of the data bits sent can only be 8 bits. By setting UART_CTRL1.SDBRK, a 13-bit '0' will be sent as the break symbol, and insert a stop bit.

20.4.11.2 LIN reception

Whether the bus is idle or during the transmission of a data frame, as long as the break frame appears, it can be detected. The break symbol detection is independent of the UART receiver.

By configuring the UART_CTRL2.LINBDL bit, 10-bit or 11-bit break character detection can be selected.

When the receiver detects the start bit, the circuit samples each subsequent bit at the 8th, 9th, and 10th oversampling clock points of each bit. When 10 or 11 consecutive bits are detected as '0' and followed by a delimiter, it means that a LIN break is detected, and UART_STS.LINBDF is set. Before confirming the break symbol, check the delimiter as it means the RX line has gone back to high level. An interrupt is generated if the LIN breaker detection interrupt (UART_CTRL2.LINBDIEN) is enabled.

If a '1' is sampled before the 10th or 11th sample point, the current detection is canceled and the start bit is searched again.

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Figure 20-13 Break Detection in LIN Mode (11-bit Break Length, The LINBDL Bit Is Set)

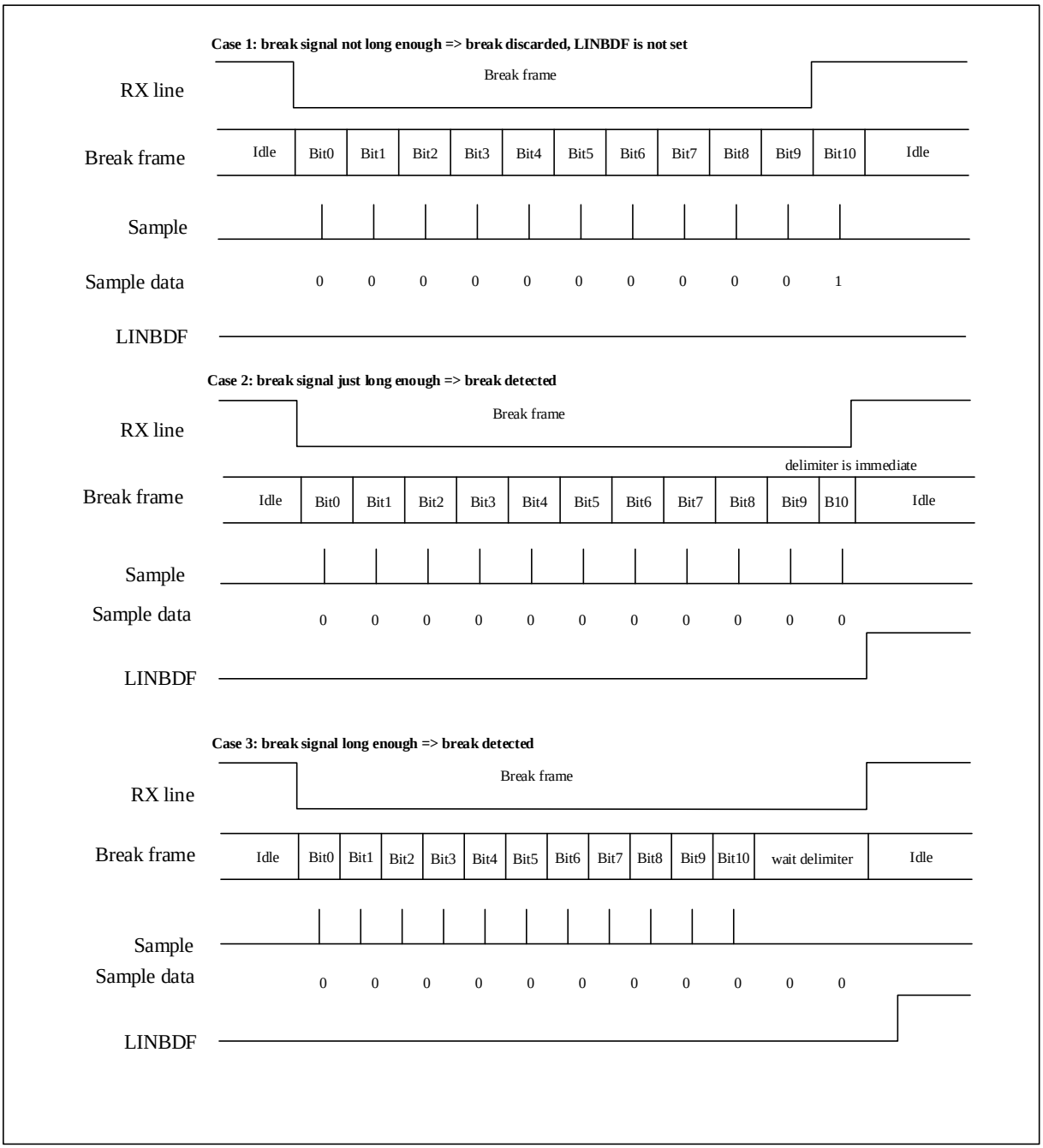

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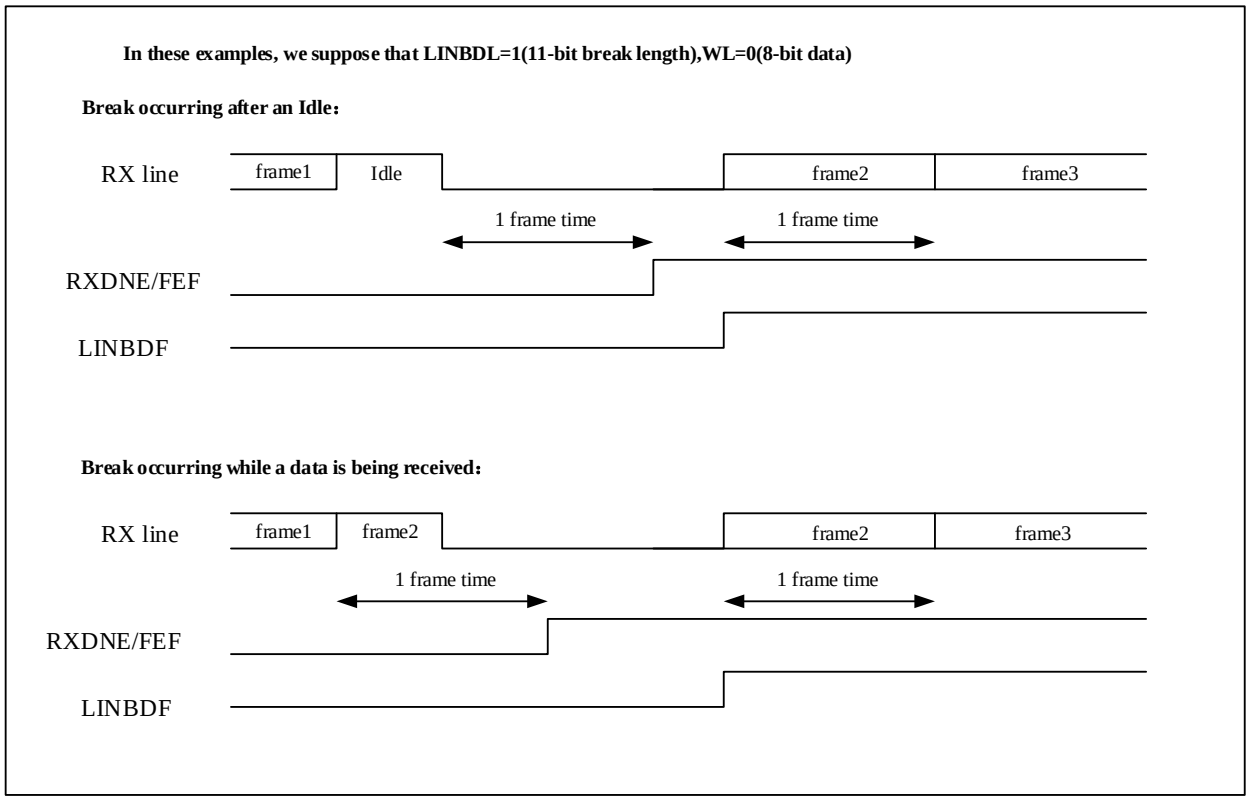
Figure 20-14 Break Detection and Framing Error Detection in LIN Mode



20.5 Interrupt Request

The various interrupt events of UART are logical OR relations, if the corresponding enable control bit is set, these events can generate their own interrupts, but only one interrupt request can be generated at the same time.

Table 20-7 UART Interrupt Request

Interrupt Function	Interrupt Event	Event Flag	Enable Bit
UART global interrupt	Transmission data register is empty.	TXDE	TXDEIEN
	Transmission complete	TXC	TXCIEN
	Receive data ready to be read	RXDNE	RXDNEIEN
	Data overrun error detected.	ORERR	
	Idle line detected	IDLEF	IDLEIEN
	Parity error	PEF	PEIEN
	Break flag	LINBDF	LINBDIEN
	Noise, overrun error and framing error in multi-buffer communication(DMA)	NEF/OREF/FEF	ERRIEN(1)

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Note:

(1) This flag bit is used only when DMA is used to receive data(UART_CTRL3.DMARXEN=1).

20.6 Mode Support

Table 20-8 UART Mode Setting (1)

Communication Mode	UART1	UART2	UART3	UART4	UART5
Asynchronous mode	Y	Y	Y	Y	Y
DMA communication mode	Y	Y	Y	Y	Y
Multiprocessor	Y	Y	Y	Y	Y
Single-wire half duplex mode	Y	Y	Y	Y	Y
IrDA infrared mode	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y

Note:

(1) Y = support this mode, N = do not support this mode.

20.7 UART Register

20.7.1 UART Register Overview

Table 20-9 UART Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	UART_CTRL1	Reserved																		SDBRK	PEIEN	TXCIEN	TXDEIEN	RXDNEIEN	IDLEIEN	WUM	RCVWU	WL	PCEN	PSEL	TXEN	RXEN	UEN
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	UART_CTRL2	Reserved																	LINBDL	LINBDIEN	LINMEN	Reserved					STPB [1:0]		Reserved	ADDR[3:0]			
	Reset Value																		0	0	0						0	0		0	0	0	0
008h	UART_CTRL3	Reserved																							IRDALP	IRDAMEN	ERRIEN	DMARXEN	DMATXEN	HDMEN	Reserved		
	Reset Value																								0	0	0	0	0	0			
00Ch	UART_STS	Reserved																FEF	NEF	OREF	PEF	LINBDF	Reserved	RXDNE	TXC	TXDE	IDLEF	Reserved					
	Reset Value																	0	0	0	0	0		0	1	1	0						
010h	UART_DAT	Reserved																							DATV[8:0]								
	Reset Value																								0	0	0	0	0	0	0	0	0
014h	UART_BRCF	Reserved																DIV_Integer[11:0]												DIV_Decimal [3:0]			

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

	Reset Value									0	0	0	0	0	0	0	0	0	0
018h	UART_GTP	Reserved														PSCV[7:0]			
	Reset Value															0	0	0	0

	Reset Value									0	0	0	0	0	0	0	0	0	0
018h	UART_GTP	Reserved														PSCV[7:0]			
	Reset Value															0	0	0	0

20.7.2 UART Control Register 1 Register (UART_CTRL1)

Address offset : 0x00

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		SDBRK	PEIEN	TXC IEN	TXDE IEN	RXDNE IEN	IDLE IEN	WUM	RCVWU	WL	PCEN	PSEL	TXEN	RXEN	UEN
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13	SDBRK	Send Break Character. The software transmits a break character by setting this bit to 1. This bit is cleared by hardware during stop bit of the break frame transmission. 0: No break character was sent. 1: Send a break character.
12	PEIEN	PE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.PEF bit is set. 0: Parity error interrupt is disabled. 1: Parity error interrupt is enabled.
11	TXCIEN	Transmit complete interrupt enable. If this bit is set to 1, an interrupt is generated when UART_STS.TXC is set. 0: Transmission completion interrupt is disabled. 1: Transmission completion interrupt is enabled.
10	TXDEIEN	TXDE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.TXDE bit is set. 0: Send buffer empty interrupt is disabled. 1: Send buffer empty interrupt is enabled.
9	RXDNEIEN	RXDNE interrupt enable If this bit is set to 1, an interrupt is generated when UART_STS.RXDNE or UART_STS.OREF is set. 0: Data buffer non-empty interrupt o and overrun error interrupt are disabled. 1: Data buffer non-empty interrupt o and overrun error interrupt are enabled.
8	IDLEIEN	IDLE interrupt enable. If this bit is set to 1, an interrupt is generated when UART_STS.IDLEF is set. 0: IDLE line detection interrupt is disabled.

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: IDLE line detection interrupt is enabled.
7	WUM	Wake up mode from mute mode. 0: Idle frame wake up. 1: Address identifier wake up.
6	RCVWU	The receiver wakes up Software can set this bit to 1 to make UART enter mute mode, and clear this bit to 0 to wake up UART. In idle frame wake-up mode (UART_CTRL1.WUM=0), this bit is cleared by hardware when an idle frame is detected. In address wake-up mode (UART_CTRL1.WUM=1), when an address matching frame is received, this bit is cleared by hardware. Or when an address mismatch frame is received, it is set to 1 by hardware. 0: The receiver is in normal operation mode. 1: The receiver is in mute mode.
5	WL	Word length. 0:8 data bits. 1:9 data bits. *Note: If data is in transit, this bit cannot be configured.*
4	PCEN	Parity control enable 0: Parity control is disabled. 1: Parity control is enabled.
3	PSEL	Parity selection. 0: even check. 1: odd check.
2	TXEN	Transmitter enable. 0: The transmitter is disabled. 1: the transmitter is enabled.
1	RXEN	Receiver enable 0: The receiver is disabled. 1: the receiver is enabled.
0	UEN	UART enable When this bit is cleared, the divider and output of UART stop working after the current byte transmission is completed to reduce power consumption. Software can set or clear this bit. 0: UART is disabled. 1: UART is enabled.

20.7.3 UART Control Register 2 Register (UART_CTRL2)

Address offset : 0x04

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LINBDL	LINBDIEN	LINMEN	Reserved					STPB[1:0]		Reserved	ADDR[3:0]			
	rw	rw	rw						rw	rw		rw	rw	rw	rw

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
14	LINBDL	LIN break detection length. This bit is used to set the length of the break frame. 0:10 bit break detection 1:11 bit break detection *Note: LINBDL can be used to control the detection length of Break Characters in LIN mode and other modes, and the detection length is the same as that in LIN mode.*
13	LINBDIEN	LIN break detection interrupt enable. If this bit is set to 1, an interrupt will be generated when UART_STS.LINBDF bit is set. 0: Disconnect signal detection interrupt is disabled. 1: Turn-off signal detection interrupt enabled
12	LINMEN	LIN mode enable 0:LIN mode is disabled 1:LIN mode enabled
11:7	Reserved	Reserved, the reset value must be maintained
6:5	STPB[1:0]	STOP bits. 00:1 stop bit. 01:0.5 stop bit. 10:2 stop bit. 11:1.5 stop bit. *Note: UART recommends using 1/2 stop bits, while 0.5/1.5 stop bits are generally used for smart card mode.*
4	Reserved	Reserved, the reset value must be maintained
3:0	ADDR[3:0]	UART address. Used in the mute mode of multiprocessor communication, using address identification to wake up a UART device. In address wake-up mode (UART_CTRL1.WUM=1), if the lower four bits of the received data frame are not equal to the ADDR[3:0] value, UART will enter the mute mode; If the lower four bits of the received data frame are equal to the ADDR[3:0] value, UART will be awakened.

20.7.4 UART Control Register 3 Register (UART_CTRL3)

Address offset : 0x08

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							IRDALP	IRDAMEN	ERRIEN	DMARXEN	DMATXEN	HDMEN	Reserved		
							rw	rw	rw	rw	rw	rw			

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8	IRDALP	IrDA low-power mode. This bit is used to select the low power consumption mode for IrDA mode. 0: Normal mode. 1: Low power mode.
7	IRDAMEN	IrDA mode enable. 0:IrDA is disabled. 1:IrDA is enabled.
6	ERRIEN	Error interrupt enable. When DMA receive mode (UART_CTRL3.DMARXEN=1) is enabled, an interrupt will be generated when UART_STS.FEF, UART_STS. OREF or UART_STS. NEF bit is set. 0: Error interrupt is disabled. 1: Error interrupt enabled.
5	DMARXEN	DMA receiver enable. 0:DMA receive mode is disabled. 1:DMA receive mode is enabled.
4	DMATXEN	DMA transmitter enable. 0:DMA transmission mode is disabled. 1:DMA transmission mode is enabled.
3	HDMEN	Half-duplex mode enable. This bit is used to enable half-duplex mode. 0: Half-duplex mode is disabled. 1: Half-duplex mode is enabled.
2:0	Reserved	Reserved, the reset value must be maintained

20.7.5 UART Status Register (UART_STS)

Address offset : 0x0C

Reset value : 0x0000 0180

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEF	NEF	OREF	PEF	LINBDF	Reserved	RXDNE	TXC	TXDE	IDLEF	Reserved					

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

r r r r rc_w0 rc_w0 rc_w0 r r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	FEF	Framing error. When the data is not synchronized or a large amount of noise is detected, and the stop bit is not received and recognized at the expected time, it will be judged that a framing error has been detected, and this bit will be set to 1. First read UART_STS, then read UART_DAT can cleared this bit. 0: No framing errors were detected. 1: A framing error or a Break Character is detected. *Note: this bit will not generate an interrupt because it appears with UART_STS.RXDNE, and the hardware will generate an interrupt when setting the UART_STS.RXDNE flag. If the currently transmitted data has both framing errors and overload errors, the hardware will continue to transmit the data and only set the UART_STS.OREF flag bit.* *In the multi-buffer communication mode, if the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the FEF flag is set.*
14	NEF	Noise error flag. When noise is detected in the received frame, this bit is set by hardware. It is cleared by the software sequence (read first UART_STS, read UART_DAT again). 0: No noise error detected. 1: Noise error detected. *Note: this bit will not generate an interrupt because it appears with UART_STS.RXDNE, and the hardware will generate an interrupt when setting the UART_STS.RXDNE flag. In the multi-buffer communication mode, if the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the NEF flag is set.*
13	OREF	Overrun error With RXDNE set, this bit is set if the UART_DAT register receives data from the shift register. When UART_CTRL3.ERRIEN bit is set, an interrupt will be generated. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No overrun error was detected. 1: Overflow error detected. *Note: In Multi Buffer Communication Mode (DMA), if the UART_CTRL3.ERRIEN bit is set, an interrupt will be generated when setting the OREF flag.*
12	PEF	Parity error. This bit is set when the parity bit of the received data frame is different from the expected check value. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No parity error was detected.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		1: Parity error detected.
11	LINBDF	LIN break detection flag. If UART_CTRL2.LINMEN bit is set, this bit is set by hardware when LIN disconnection is detected. If UART_CTRL2.LINBDIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0: LIN break character not detected. 1: LIN break character detected.
10	Reserved	Reserved, the reset value must be maintained
9	RXDNE	The Read data register not empty. This bit is set when the read data buffer receives data from the shift register. When UART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. Software can clear this bit by writing 0 to it or reading the UART_DAT register. 0: The read data buffer is empty. 1: The read data buffer is not empty.
8	TXC	Transmission complete. This bit is set to 1 after power-on reset. If UART_STS.TXDE is set, this bit is set when the current data transmission is completed. Setting UART_CTRL1.TXCIEN bit will generate an interrupt. This bit is cleared by software. 0: Transmitting did not complete. 1: Send completed.
7	TXDE	The Transmit data register empty. Set to 1 after power-on reset or data to be sent has been sent to the shift register. Setting UART_CTRL1.TXDEIEN will generate an interrupt. This bit is cleared to 0 when the software writes the data to be sent into UART_DAT. 0: Send data buffer is not empty. 1: The transmitting data buffer is empty.
6	IDLEF	IDLE line detected flag. Within one frame time, the idle state is detected at the RX pin, and this bit is set to 1. When UART_CTRL1.IDLEIEN bit is set, an interrupt will be generated. The software can clear this bit by reading UART_STS first and then reading UART_DAT. 0: No idle frame detected. 1: idle frame detected. *Note: IDLEF bit will not be set high again until UART_STS.RXDNE bit is set (that is, an idle line is detected again).*
5:0	Reserved	Reserved, the reset value must be maintained

20.7.6 UART Data Register (UART_DAT)

Address offset : 0x10

Reset value : undefined (uncertain value)

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DATV[8:0]								
							rw								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	DATV[8:0]	Data value Contains the data sent or received; Software can change the transmitted data by writing these bits, or read the values of these bits to obtain the received data. If parity is enabled, when the transmitted data is written into the register, the highest bit of the data (the 7th or 8th bit depends on UART_CTRL1.WL bit) will be replaced by the parity bit.

20.7.7 UART Baud Rate Register (UART_BRCF)

Address offset : 0x14

Reset value : 0x0000 0000

Note: When UART_CTRL1.UEN=1, this register cannot be written;The baud counter stops counting if UART_CTRL1.TXEN or UART_CTRL1.RXEN are disabled respectively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV_Integer[11:0]												DIV_Decimal[3:0]			
rw												rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:4	DIV_Integer [11:0]	Integer part of baud rate divider.
3:0	DIV_Decimal[3:0]	Fractional part of baud rate divider.

20.7.8 UART Guard Time and Prescaler Register (UART_GTP)

Address offset : 0x18

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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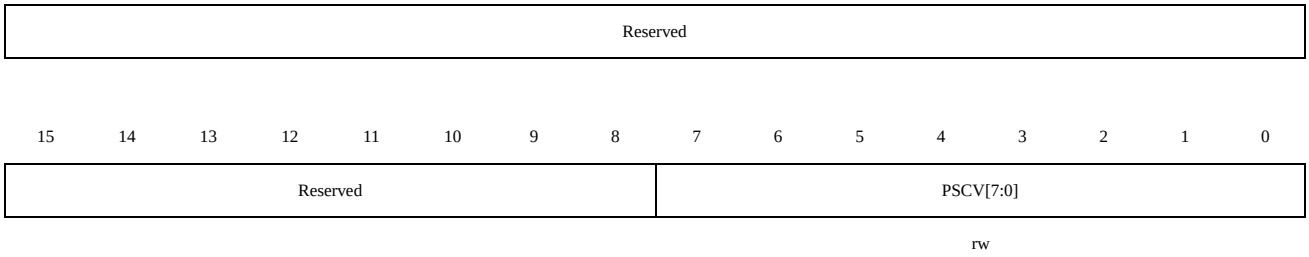
Nanshan District, Shenzhen, 518057, P.R.China



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	PSCV[7:0]	Prescaler value. In IrDA low power consumption mode: these bits are used to set the frequency division coefficient for dividing the peripheral clock (PCLK1/PCLK2) to generate low power consumption frequency. 00000000: reserved-do not write this value. 00000001: divide the source clock by 1. … 11111111: divide the source clock by 255. In IrDA normal mode: PSCV can only be set to 00000001. In Smartcard mode: PSCV[4:0] is used to set the frequency division of Smartcard clock generated by peripheral clock (PCLK1/ PCLK2). Coefficient. The actual frequency division coefficient of is twice the set value of PSCV[4:0]. 0000: reserved-do not write this value. 0001: Divide the source clock by 2. 0010: Divide the source clock by 4. … 1111: Divide the source clock by 62.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

21 CAN

21.1 Introduction

As a CAN network interface, the basic extended CAN supports CAN protocols 2.0A and 2.0B. It can efficiently process a large number of received messages and greatly reduce the consumption of CPU resources. The priority characteristics of message sending can be configured by software, and the hardware function of CAN can support time-triggered communication mode for some applications with high security requirements.

21.2 Main Features

- Baud rate supports up to 1Mbit/s
- CAN protocol 2.0A/B are supported.
- Support time-triggered communication function
- Support individual interrupt control.
- CAN Core Manages the communication between the CAN and the 512 bytes SRAM memory (see Figure 21-3)

Time triggered communication mode

- 16-bit free-running timer
- Automatic retransmission mode is prohibited.
- The last 2 data bytes of a message can be configured as the timestamp.

Transmission

- There are 3 sending mailboxes.
- Time stamp function for recording the time of sending SOF
- Software can configure the priority characteristics of sending messages.

Reception

- Filter groups support identifier list mode.
- Each CAN has two receiving FIFOs, each with a depth of 3 levels
- A total of 14 filter groups(each CAN module has its own)
- Configurable FIFO overrun handling method
- Time stamp function for recording the time of receiving SOF

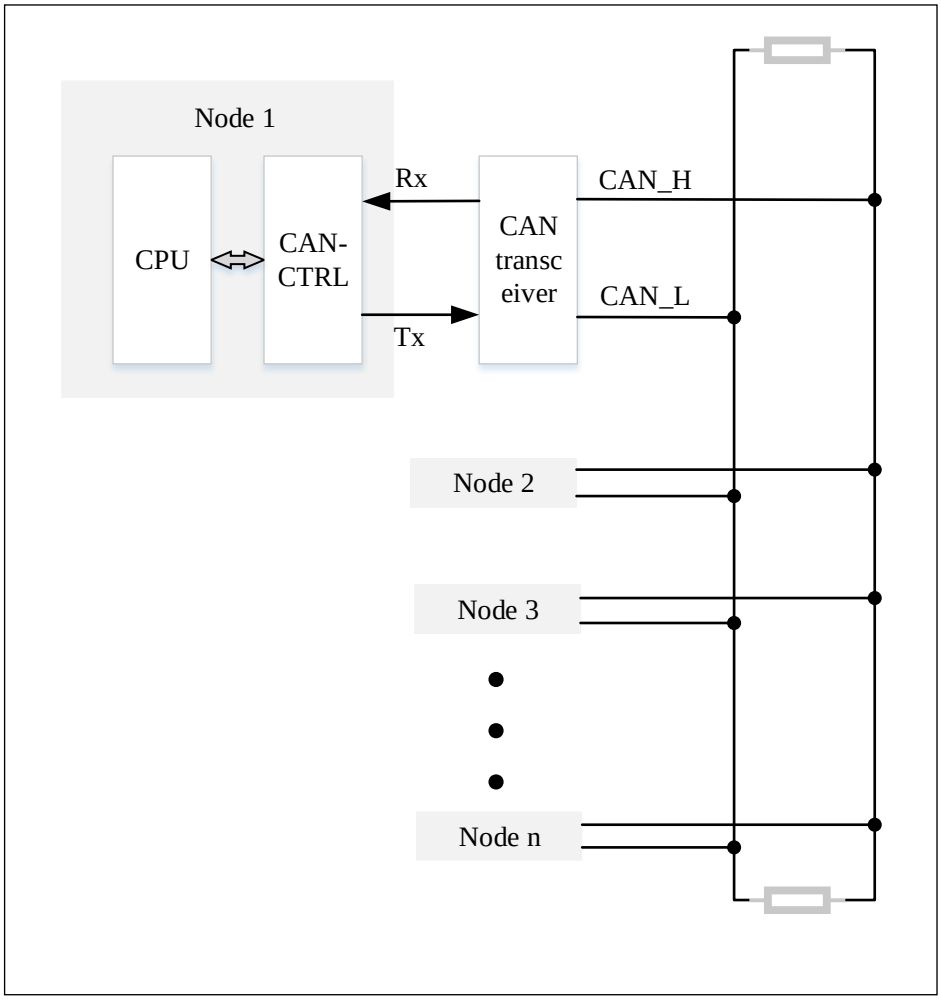
21.3 Overview of CAN

With the widespread application of CAN, the number of nodes in CAN network are growing rapidly. Multiple CAN nodes are connected through CAN network. With increase number of CAN nodes, the number of messages in CAN network also increase dramatically which will occupy lots of CPU resources. In this CAN controller, receive FIFOs and filter mechanism are added as hardware support for CPU message processing and reduce real-time response

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

requirement of CAN messages.

Figure 21-1 Topology of CAN Network



21.3.1 CAN Module

CAN module can automatically receive and transmit CAN messages, and supports standard identifiers (11 bits) and extended identifiers (29 bits).

21.3.2 CAN Operating Mode

Initialization, normal and sleep mode are three main working modes of CAN. The internal pull-up resistor of CANTX pin is activated after hardware reset, and CAN works in sleep mode to reduce power consumption.

The software can set CAN_MCTRL.INIRQ and CAN_MCTRL.SLPRQ bit to configure CAN to enter initialization or sleep mode. The software reads values of the CAN_MSTS.INIAK or CAN_MSTS.SLPAK bit to confirm whether the initialization or sleep mode is entered, at this time the internal pull-up resistor of the CANTX pin is disabled.

CAN is in normal mode when CAN_MSTS.INIAK and CAN_MSTS.SLPAK bits are both '0', and it must synchronize with CAN bus to enter normal mode. When 11 consecutive recessive bits are monitored on the CANRX pin, the CAN bus is idle and synchronization is completed.

21.3.2.1 Normal mode

After the initialization is completed, the software configures CAN to enter normal mode. Clear the

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

CAN_MCTRL.INIRQ and wait for the hardware to clear the CAN_MSTS.INIRQ bit to confirm that CAN enters normal mode. Only after the synchronization with CAN bus is completed, CAN can receive and send messages normally.

Setting the bit width and mode of the filter group must be completed when the filter is in the initialization mode (the CAN_FMC.FINITM bit is 1). Setting the initial value of the filter must be completed when it is inactive (the corresponding CAN_FA1.FAC bit is 0).

21.3.2.2 Initialization mode

The software can perform initialization configuration only when CAN is in initialization mode. Set the CAN_MCTRL.INIRQ bit and clear CAN_MCTRL.SLPRQ bit, and wait for the hardware to set the CAN_MSTS.INIAK bit to confirm that CAN enters the initialization mode. When entering the initialization mode, the register configuration will not be affected. When CAN is in initialization mode, message receiving and sending are prohibited, and the CANTX pin outputs a recessive bit (high level). To exit initialization mode, clear the CAN_MCTRL.INIRQ bit, and wait for the hardware to clear the CAN_MSTS.INIAK bit to confirm that CAN exits the initialization mode.

To perform initialization configuration for CAN by software, at least the bit time characteristic register (CAN_BTIM) and the control register (CAN_MCTRL) need to be configured. The software needs to set the CAN_FMC.FINITM bit to initialize the filter group (mode, bit width, FIFO association, activation and filter value) that configures CAN. Configuring the filter group of CAN does not necessarily need to be in initialization mode.

Specially,when CAN_FMC.FINITM=1, it is forbidden to receive messages. If you want to modify the value of the corresponding filter, you need to first clear the filter activation bit (in CAN_FA1). It is necessary to keep the unused filter group inactive (keep its CAN_FA1.FAC bit to '0').

21.3.2.3 Sleep mode (low power)

To enters sleep mode, set the CAN_MCTRL.SLPRQ bit, and wait for the hardware to set the CAN_MSTS.SLPAK bit to confirm that CAN enters sleep mode. CAN can configure to sleep modeto reduce power consumption when unused. In sleep mode, the clock of CAN stops working, but the software can still access the sending/receiving mailbox register. When CAN is in sleep mode, the CAN_MCTRL.INIRQ bit must be set and the CAN_MCTRL.SLPRQ bit must be clear at the same time so as to enter the initialization mode.

There are two situation to wake up CAN(CAN exits sleep mode):

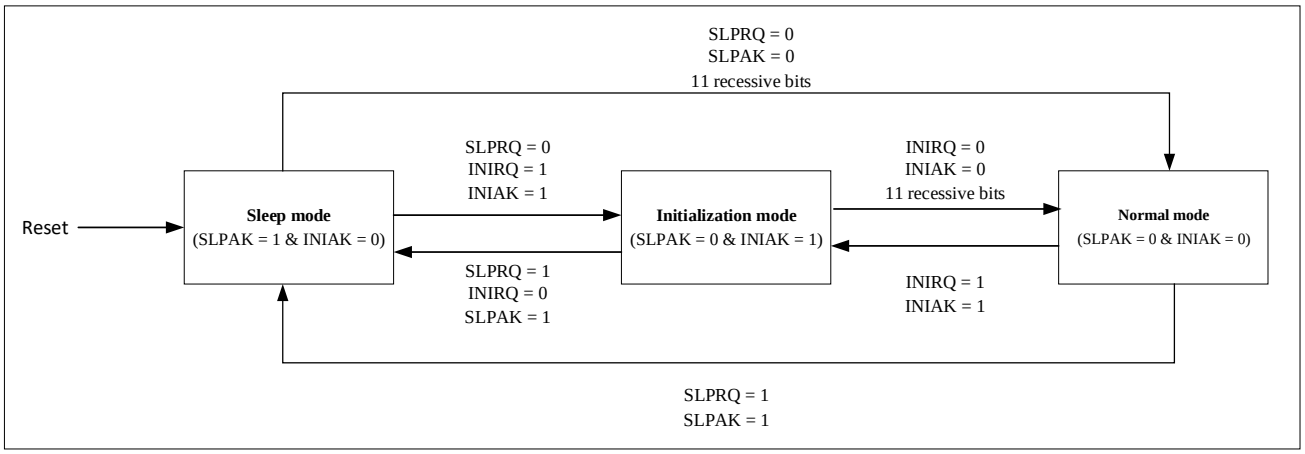
- When the CAN_MCTRL.AWKUM bit is set(enable hardware wake up automatically), once the activity of the CAN bus is detected, the hardware will automatically clear the CAN_MSTS.SLPRQ bit to wake up CAN.
- When the CAN_MCTRL.AWKUM bit is clear(enable software wake up), and wake-up interrupt occurred ,then the software must clear the CAN_MCTRL.SLPRQ bit to exit the sleep state.

If the wake-up interrupt (set the CAN_INTE.WKUITE bit) is enabled, the wake-up interrupt will be generated once the CAN bus activity is detected, regardless of whether the hardware is enabled to automatically wake up CAN.

The CAN must be synchronized with the CAN bus before entering Normal mode Wait until the CAN_MSTS.SLPAK bit cleared to confirm the sleep mode has exited.Please refer to Figure 21-2.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Figure 21-2 CAN Operating Mode



Notes: the state that the hardware sets the CAN_MSTS.INIAK or CAN_MSTS.SLPAK bit in response to a sleep or initialization request.

21.3.3 Transmit Mailbox

Applications can send messages through three sending mailboxes. The order of sending three mailbox messages is determined by the sending scheduler according to the priority of the messages, and the priority can be determined by the identifier of the messages or by the order of sending requests.

21.3.4 Receive Filter

The CAN has 14 configurable identifier filter groups. After the application configures the identifier filter group, the receiving mailbox will automatically receive the required messages and discard other messages.

21.3.5 Receive FIFO

The CAN has two receiving FIFOs, each of which can store three complete messages. No application program is needed to manage it, and it is managed by hardware.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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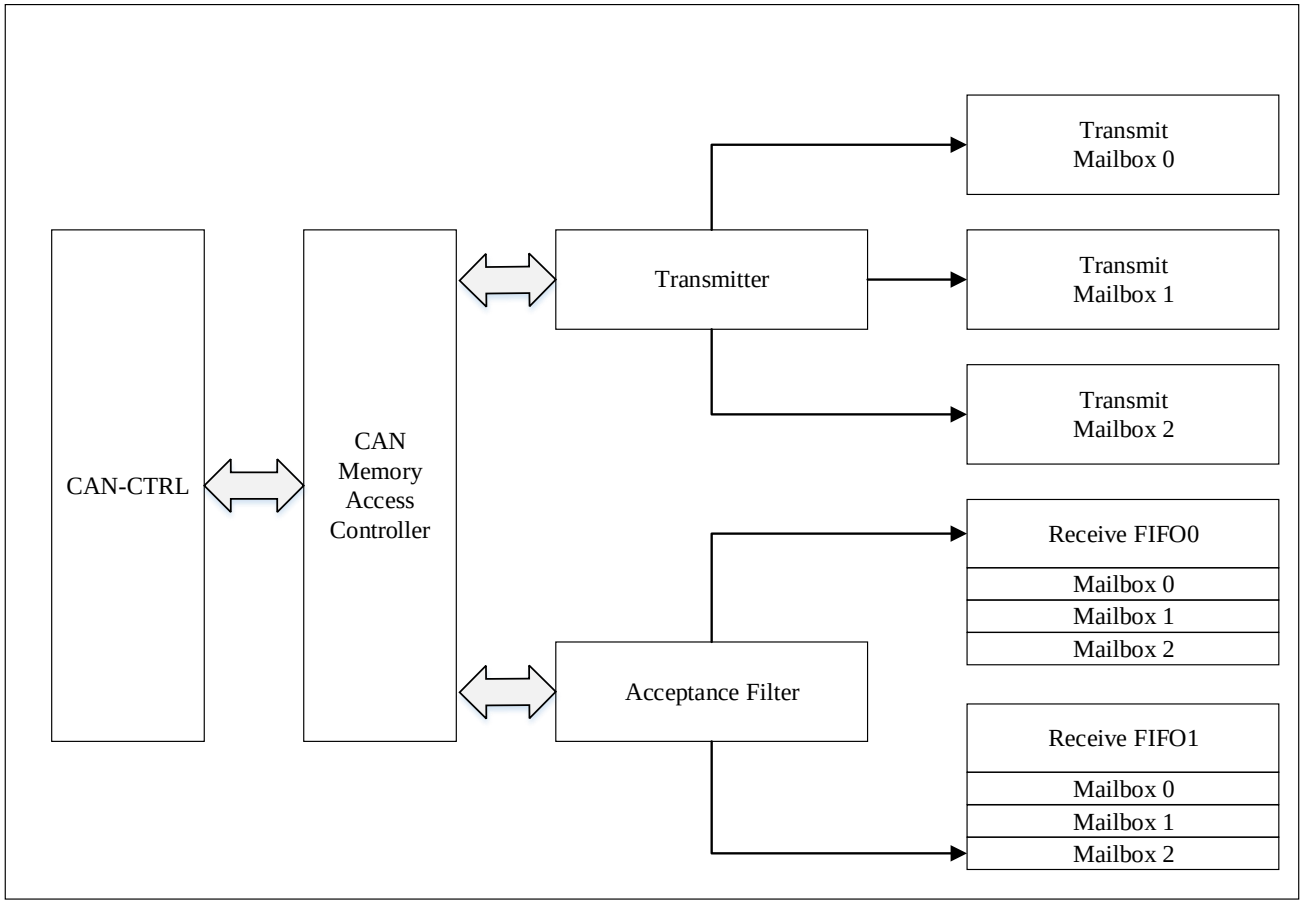
Figure 21-3 CAN Block Diagram



21.3.6 CAN Test Mode

In the initialization mode, a test mode must be selected by combining the CAN_BTIM.SLM bit and CAN_BTIM.LBM bit. After selecting a test mode, the software needs to clear the CAN_MCTRL.INIRQ bit to exit the initialization mode and enter the test mode.

21.3.6.1 Loopback mode

Loopback mode can be used for self-test. In loopback mode, CAN saves the sent message in the receiving mailbox as received message (if it can be filtered by reception). In loopback mode, CAN internally feeds back the Tx output to the Rx input, completely ignoring the actual state of the CANRX pin. The message sent can be detected on the CANTX pin. In order to avoid external influence, the CAN kernel ignores the acknowledgement error(at the moment of acknowledgement bit of data/remote frame, it does not detect whether there is an dominant bit). To enter loopback mode, the CAN_BTIM.SLM bit should be cleared and the CAN_BTIM.LBM bit should be set.

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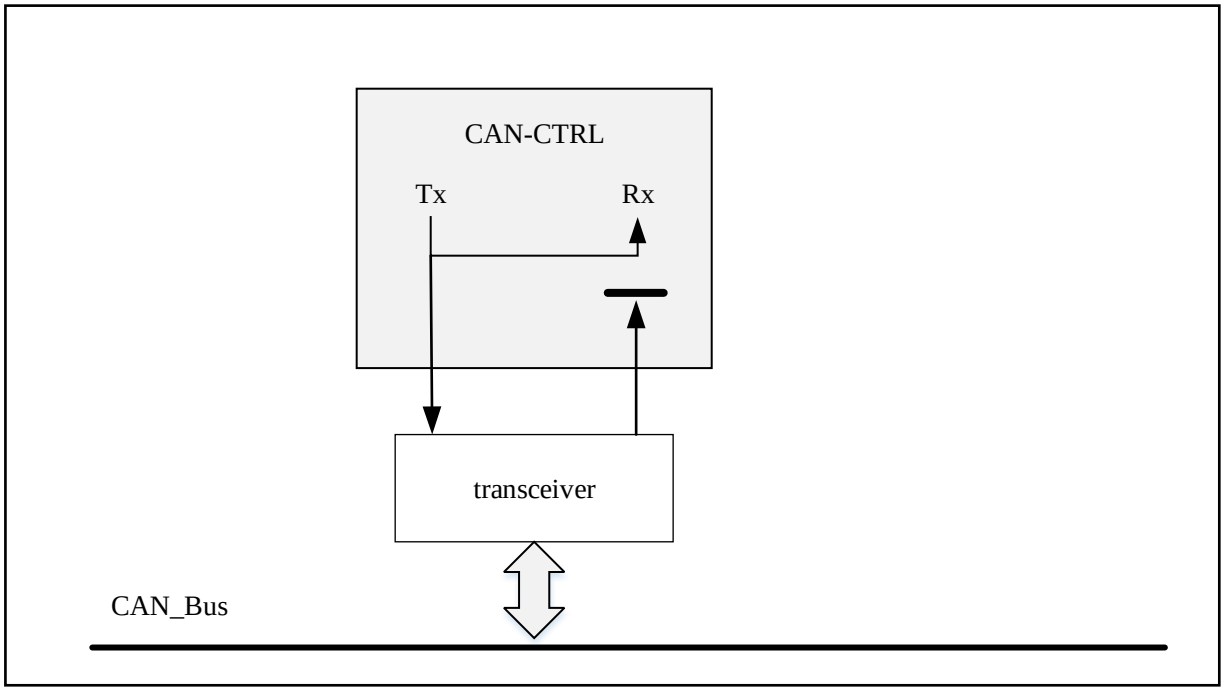
Figure 21-4 Loopback Mode



21.3.6.2 **Silent mode**

In silent mode , CAN can normally receive data frames and remote frames, but can only send recessive bits, and can't really send messages. If CAN needs to send overload flag, active error flag or ACK bit(these are dominant bits), such dominant bits are internally connected back so as to be detected by the CAN core. At the same time, the CAN bus will not be affected and still remain in the recessive bit state. Therefore, the silent mode is usually used to analyze the activity of the CAN bus, without affecting the bus because dominant bits is not actually sent to the bus.

To enter silent mode, the CAN_BTIM.SLM bit should be set and the CAN_BTIM.LBM bit should be cleared.

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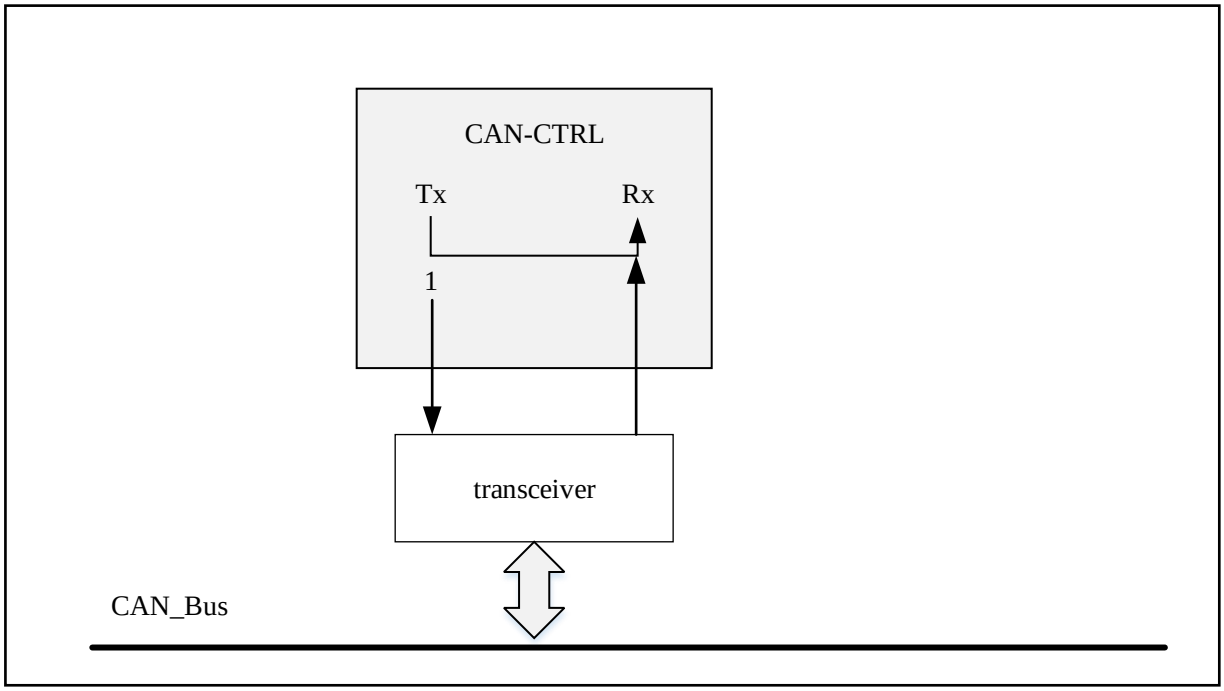
Figure 21-5 Silent Mode

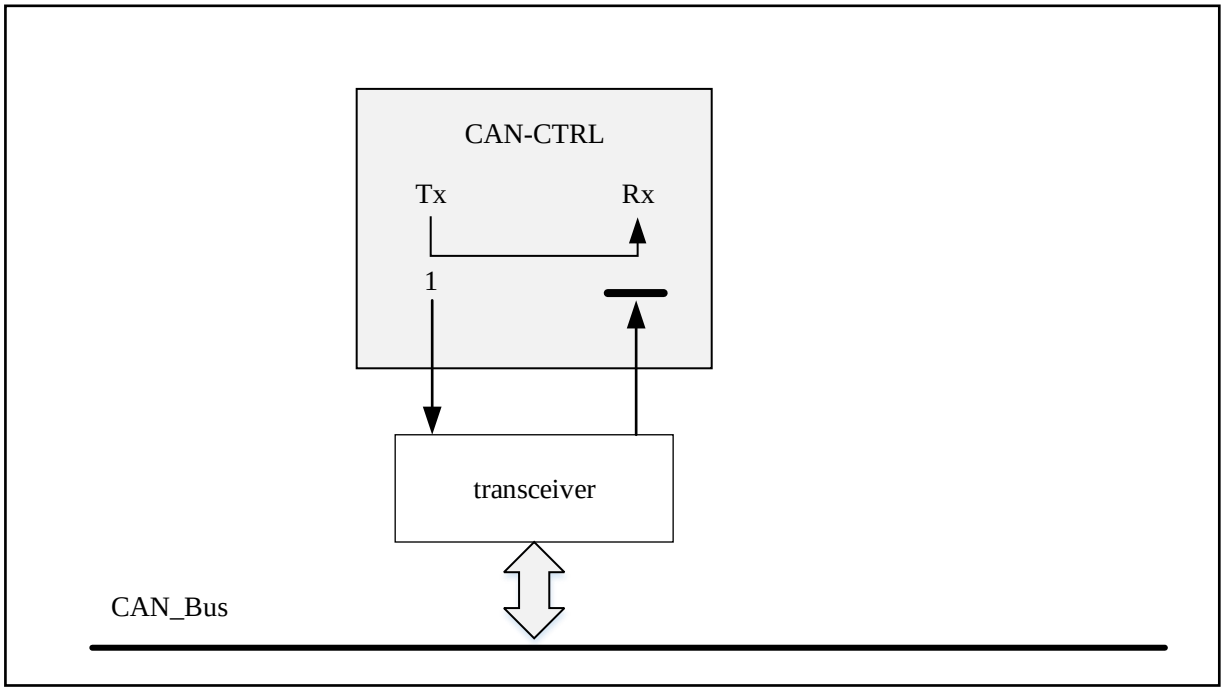


21.3.6.3 Loopback silent mode

In loopback silent mode, the CANRX pin is disconnected from the CAN bus, while the CANTX pin is driven to the recessive bit state. It can be used for "Hot Selftest" just like CAN can be tested in loop-back mode, but not affect the whole CAN system connected by CANTX and CANRX.

To enter loopback silence mode, both the CAN_BTIM.SLM bit and the CAN_BTIM.LBM bit should be set.

Figure 21-6 Loopback Silent Mode



Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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21.3.7 CAN Debug Mode

CAN can continue to work normally or stop working according to the state of the following configuration bits:

- DBG_CTRL.CAN_STOP bit of CAN in the debug support (DBG) module. See paragraph 3.3.2 Section: Peripheral debugging support.
- CAN_MCTRL.DBGF bit see paragraph 21.7.3.1 Section: CAN_MCTRL.

When the microcontroller is in debug mode, Cortex-M0 core is in a suspended state.

21.4 CAN Functional Description

21.4.1 Transmit Processing

The process of transmitting messages is as follows:

- The application program selects an empty transmitting mailbox;
- Writes the identifier, data length and data to be sent in the transmitting mailbox register;
- Set the CAN_TMIx.TXRQ bit to request transmission(after CAN_TMIx.TXRQ is set the mailbox is no longer an empty mailbox and the software has no permission to write to the mailbox register);
- The mailbox enter the pending state and wait to be the highest priority, see 21.4.1.1Transmit priority;
- Changing to the ready status once the mailbox becomes the highest priority mailbox;
- The messages in the ready mailbox is sent as soon as the CAN bus enters the idle state, then enter the transmitting state.
- Become an empty mailbox when the message in the mailbox is successfully sent;
- Hardware set the RQCPM and TXOKM bits of the corresponding mailbox in CAN_TSTS register to indicate a successful transmission.

However, if the transmission fails, the CAN_TSTS.ALSTM bit will be set to indicate that the failure is caused by arbitration or the CAN_TSTS.TERRM bit will be set to indicates that it is caused by the transmission error (for specific errors, please check the CAN_ESTS.LEC[2:0] error code bits of the error status).

21.4.1.1 **Transmit priority**

Determined by the order of transmitting requests.

Set the CAN_MCTRL.TXFP bit, and the sending mailbox can be configured as a sending FIFO. At this time, the priority of sending is determined by the order of sending requests. This mode is useful for segmented transmission.

Determined by the identifier.

According to CAN protocol, the message with the lowest identifier has the highest priority. If the values of identifiers are equal, the message with small mailbox number is sent first. When more than one sending mailbox is registered, the sending order is determined by the identifier of the message in the mailbox.

21.4.1.2 **Canceling transmitting**

Setting the CAN_TSTS.ABRQM bit can abort sending the request. If the mailbox is ready or pending, the transmitting request will be aborted immediately. If the mailbox is in the transmitting state, the request to abort may lead to two kinds of results:

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

- if the message in the mailbox fails to be sent, the mailbox becomes ready state, then the sending request is aborted, the mailbox becomes an empty mailbox and the CAN_TSTS.TXOKM bit is cleared;
- if the message in the mailbox is successfully sent, the mailbox becomes an empty mailbox, and the CAN_TSTS.TXOKM bit will be set by hardware.

Therefore, when the transmitting mailbox is in the transmitting state, regardless of the sending result, the mailbox will become an empty mailbox after the sending operation is finished.

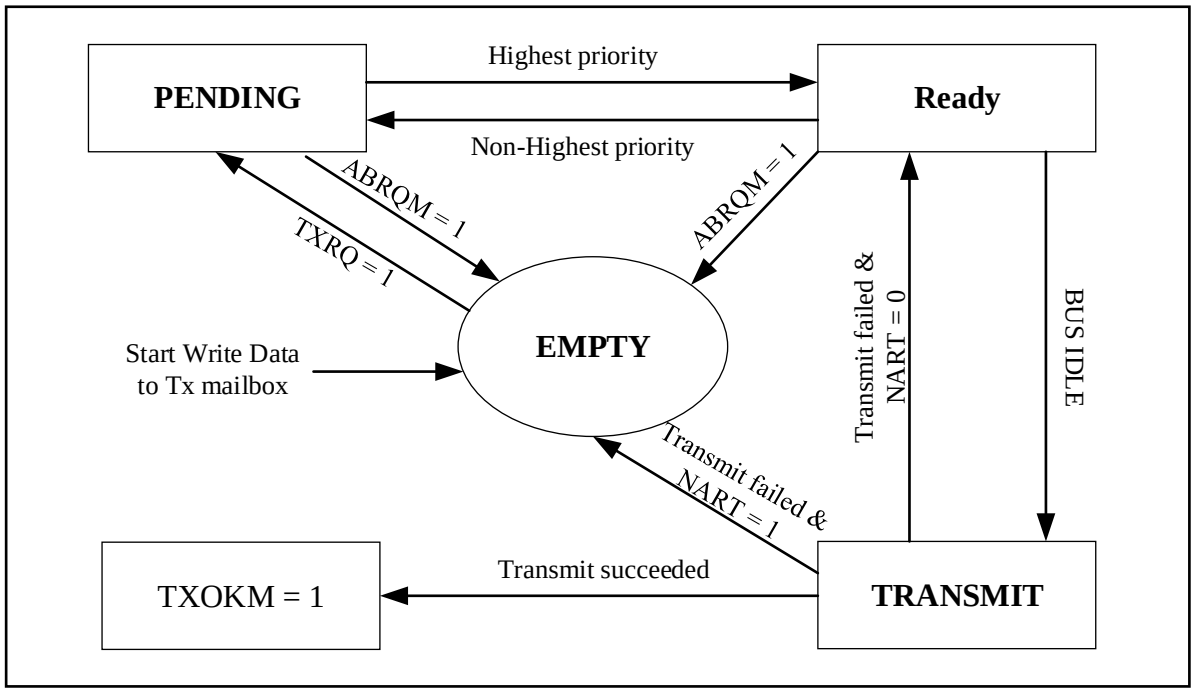
21.4.2 Time-triggered Communication Mode

The internal timer of CAN is activated in time triggered communication mode. It is incremented at each CAN bit time (see 21.4.7 Section). CAN samples the value of the internal timer at the sampling point position of the received and sent frame start bits, and the sampled value is the time stamp of the sending and receiving mailboxes. Timestamps generate form the internal timer will be stored in the CAN_RMDTx/CAN_TMDTx registers respectively.

21.4.3 Non-automatic Retransmission Mode

To enable non-automatic retransmission mode the CAN_MCTRL.NART bit should be set. This mode corresponds to the function of time-triggered communication option in CAN standard.In non-automatic retransmission mode , the transmission will only be executed once. If the transmission fails, whether due to arbitration loss or error, the hardware will not automatically send the message again.At the end of a transmission operation, the hardware judge that the transmission request has been completed, and the hardware sets the CAN_TSTS.RQCPM bit. At the same time, the transmission result can query the CAN_TSTS.TXOKM, CAN_TSTS.ALSTM and CAN_TSTS.TERRM bits.

Figure 21-7 Transmit Mailbox State



21.4.4 Receive Management

A FIFO with 3 levels depth are used to store received messages. When the application reads the FIFO output mailbox, it reads the first received message in the FIFO. FIFO is completely managed by hardware, which can simplify the application program, ensure the consistency of data and reduce the processing time of CPU.

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Email：info@nationstech.com
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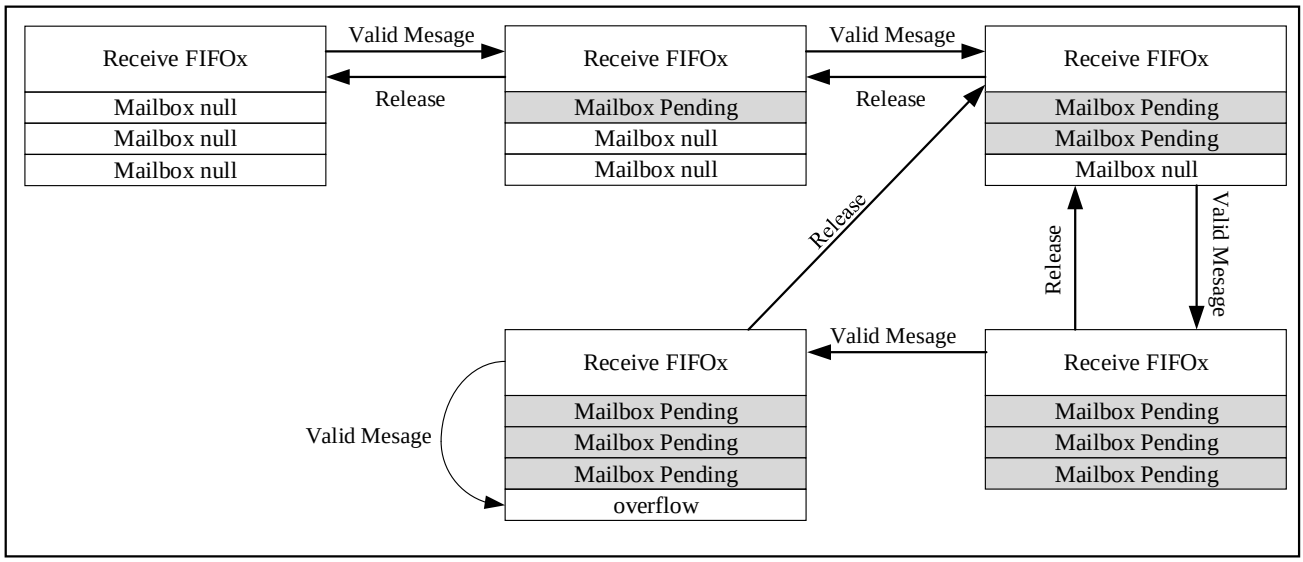
21.4.4.1 Valid messages

According to CAN protocol, when the message is correctly received (no errors are sent up to the last bit of the EOF field) and passes the identifier filtering, then the message is token as a valid message. Please refer to 21.4.5 Section: identifier filtering.

Figure 21-8 Receive FIFO State



21.4.4.2 FIFO receive

A FIFO includes mailboxes with three levels of depth, and the initial state is empty. After receiving the first valid message, one of the mailboxes will be suspended, and the hardware will set the CAN_RFF.FFMP[1:0] bits to 1 to indicate the receipt of a valid message. A valid message is received again before the mailbox is released. At this time, two mailboxes will be suspended at the same time, and the hardware will set the CAN_RFF.FFMP[1:0] bits to 2 to indicate that two valid messages are pending. As above, the third valid message will suspend all three mailboxes and set the CAN_RFF.FFMP[1:0] bits to 3.

When the three-level mailboxes of the FIFO are all suspended, receiving a valid message again will cause the mailbox to overflow and lose a message, and the hardware will set the CAN_RFF.FFOVR bit to 1 to indicate the occurrence of the event. The rules for lost messages depend on the configuration of the FIFO. If the FIFO lock function is disabled (clear the CAN_MCTRL.RFLM bit), then the last message received in the FIFO will be overwritten by the new message. In this way, the latest received message will not be discarded;If the FIFO lock function is enabled (set the CAN_MCTRL.RFLM bit), then the newly received messages will be discarded, and the software can read the first three messages in the FIFO.

21.4.4.3 FIFO release

The message stored in the FIFO will be read through the corresponding receive mailbox. The software reads the mailbox message and releases the mailbox by setting the CAN_RFR.RFOM bit to 1 , and he CAN_RFF.FFMP[1:0] bit is decremented by 1 until it is 0.

21.4.4.4 Receive related interrupts

The hardware will update the CAN_RFF.FFMP[1:0] bits when a message is stored in the receiving FIFO. If the FIFO message pending interrupt is currently enabled (the CAN_INTE.FMPITE bit is set), then the FIFO message pending interrupt request will be generated.

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Email：info@nationstech.com
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When the third message is stored ,the FIFO becomes full, then the CAN_RFF.FFULL bit will be set, and if the FIFO full interrupt is currently enabled (the CAN_INTE.FFITE bit is set), a FIFO full interrupt request will be generated.

When the FIFO overrun, the FFOVR bit will be set. If the FIFO overrun interrupt is currently enabled (the CAN_INTE.FOVITE bit is set), a FIFO overrun interrupt request will be generated.

21.4.5 Identifier Filtering

In the CAN network, when basic CAN is in the transmitter state, it broadcasts a message to each node by sending a message to the bus; when basic CAN is in the receiver state, it determines whether the node needs the message according to the identifier of the message after receiving the message. If message is vaild, CAN core copies the message to SRAM(CAN's own SRAM); If it is not needed, the message will be discarded. This process does not require software intervention. Compared with software filtering, hardware filtering reduces the CPU usage. CAN controller provides 14 configurable filter banks (0~13) with variable bit width for application programs to meet this demand. These filter banks are used to receive only those messages needed by software. Each filter bank x contains two 32-bit registers, namely CAN_FxR0 and CAN_FxR1.

21.4.5.1 **Setting of filter bit width and mode**

Each filter in a filter bank is numbered (filter number, from 0 to a certain maximum value) depending on the mode and bit width setting of the filter bank. See the figure below for the filter configuration.The filter group can be configured through the corresponding CAN_FMC register. Filter banks that are not used by the application should be kept disabled. Before configuring a filter bank, it must be set to the disabled state by clearing the CAN_FA1.FAC bit.

By setting the corresponding CAN_FS1.FSCx bit you can configure the bit width of a filter bank, see Figure 21-9.

By means of the CAN_FM1.FBx bit, the corresponding mask/identifier register can be configured to be the identifier list or identifier mask mode.The filter group should be set to work in the mask mode in order to filter out a group of identifiers. And the filter group should be set to work in identifier list mode in order to filter out an identifier.

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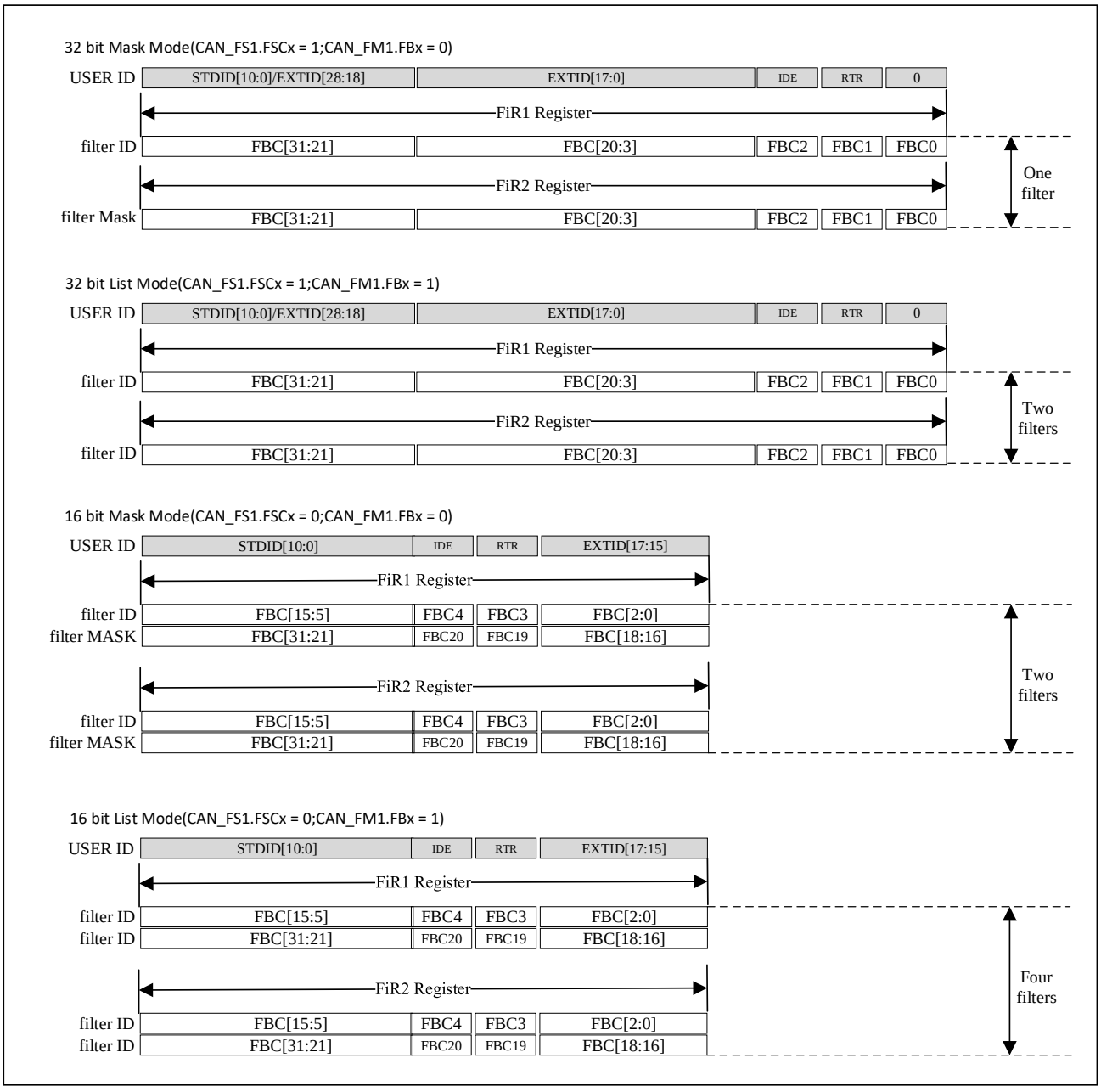
Figure 21-9 Filter Bit Width Setting-Register Organization



21.4.5.2 Variable bit width

The bit width of each filter bank can be independently configured. Each filter bank can be configured to be one 32-bit filter: including STDID[10:0], EXTID[17:0], IDE and RTRQ bits; or two 16-bit filters,:including STDID[10:0], IDE, RTRQ and EXTID[17:15] bits, see Figure 21-9. In addition, the filter can be configured in two different modes, namely, the mask mode and the identifier list mode.

Mask mode

The filter ID is used to store the identifier format, and the filter MASK is used to indicate which bits must be checked and which bits can be ignored.

Identifier list mode

The filter ID is used to store the identifier format. At this time, there is no mask for comparison, and the mask bit can

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

be used to store one more filter ID. However, at this time, the identifier of the message needs to be exactly the same as the filter ID format, otherwise it will fail to pass the filter.

21.4.5.3 Filter match index

After CAN core receives a valid message it will matching the message ID with filters one by one until there is one filter pass or all filters failed. If this message failed to pass any enabled filter then it will be discarded. Otherwise when CAN core finds the first filter that the ID can pass, it pack filter index with the CAN message and stores inside receive FIFO in SRAM according to filter setting (CAN_FFA1 decides store in which FIFO). User can find filter index in FMI [7:0] bits of CAN_RMDTx register. This filter matching index can help to identify which types of message it is in this receive FIFO.

The filter match index can be used two ways. The first one is comparing the filter match index with a series of expected values. The another is using the filter match index as an index to access the target address. When numbering filters, whether the filter group is active or not is not considered. In addition, each FIFO numbers its associated filter. Please refer to the example below.

For the filter in mask mode, the software only needs to compare the mask bits that are needed (bits that must be matched). For the filter in identifier list mode (non-screening filter), the software does not need to directly compare with the identifier.

Table 21-1 Example of Filter Numbers

Point To Fifox	Filter Group	Filter Mode	FIFO0 Filter Number
FIFO	0	32 bit mask mode	0
	2	16 bit mask mode	1/2
	5	32 bit list mode	3/4
	7	16 bit list mode	5/6/7/8
	9	32 bit list mode	9/10
	11	16 bit list mode	11/12/13/14
	13	32 bit mask mode	15
Point To Fifox	**Filter Group**	**Filter Mode**	**FIFO1 Filter Number**
FIFO1	1	32 bit list mode	0/1
	3	16 bit list mode	2/3/4/5
	4	32 bit mask mode	6
	6	16 bit mask mode	7/8
	8	32 bit mask mode	9

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	10	16 bit mask mode	10/11
	12	32 bit list mode	12/13

21.4.5.4 Filter priority rules

According to different configurations of filters, it is possible that a message identifier can be filtered by multiple filters; In this case, the filter matching serial number stored in the receiving mailbox is first determined according to bit width,32-bit-wide filters have higher priority than 16-bit-wide filters. For filters with the same bit width, then the identifier list mode takes precedence over the mask mode. If filters have the same bit width and mode, the priority is determined by the filter group number, and the filter group with lower number has the higher priority.Within a filter group,the lower the filter number,the higher the priority.

Figure 21-10 Examples of Filter Mechanisms

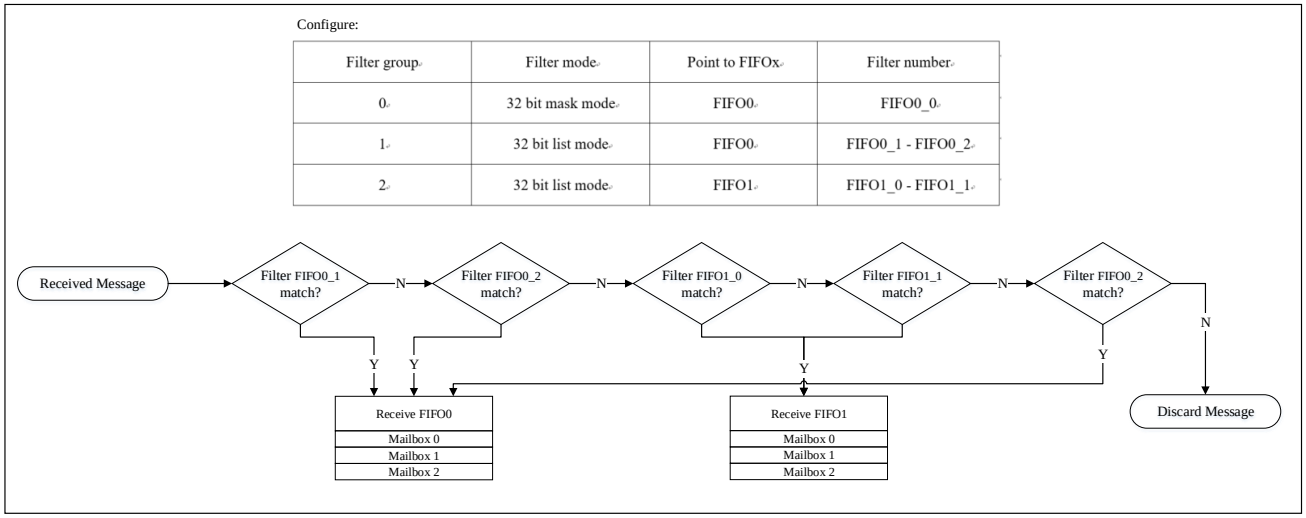

Figure 21-10 illustrates the filter rules of CAN. When receiving a message, its identifier is first compared with the filter configured in identifier list mode. If there is a match, the message will be stored in the associated FIFO, and the serial number of the matched filter will be stored in the filter matching serial number.

If there is no match, the message identifier is then compared with the filter configured in the mask mode. And the hardware will automatically discard the message without software intervention if the message identifier does not match any identifier in the filter.

21.4.6 Message Storage

A mailbox contains all information related to a message: identifier, data, control, status and time stamp information. Mailbox is the interface between software and hardware to transfer messages.

21.4.6.1 Transmit mailbox

Message should be written into an empty transmitting mailbox by software before enable the sending request. You can query the sending status through the CAN_TSTS register.

Table 21-2 Transmit Mailbox Register List

Offset From The Base Address Of The Sending Mailbox	Register Name

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0	CAN_TMIx
4	CAN_TMDTx
8	CAN_TMDLx
12	CAN_TMDHx

21.4.6.2 Receive mailbox (FIFO)

CAN_RMDTx.FMI[7:0] field can store the filter matching serial number and CAN_RMDTx.MTIM[15:0] field can store the 16-bit timestamp.The software can access the output mailbox of the receiving FIFO to read the received message. Once the software has processed the message, such as reading it out, the software should set the CAN_RFFx.RFFOM bit to release the corresponding, so as to reserve storage space for later messages.

Table 21-3 Receive Mailbox Register List

Offset From The Base Address Of The Receiving Mailbox	Register Name
0	CAN_RMIx
4	CAN_RMDTx
8	CAN_RMDLx
12	CAN_RMDHx

21.4.7 Bit Timing

The bit timing characteristic logic monitors the serial CAN bus by sampling, and adjusts its sampling point by synchronizing with the edge of the frame start bit and resynchronizing with the following edge. To avoid programming errors in software, setting the bit time characteristic register (CAN_BTIM) can only be done when CAN is initialized.

Its operation can be simply understood as dividing each nominal time into three segments: Synchronization segment (SYNC_SEG), Time period 1(BS1) and Time period 2(BS2).

Usually, it is expected that the change of bits will occur in SYNC_SEG. Its value is fixed to 1 time unit ($1 \times t_{CAN}$).

BS1 defines the position of the sampling point. It includes PROP_SEG and PHASE_SEG1 in CAN standard. Its value can be programmed into 1 to 16 time units, but in order to compensate the forward drift of phase caused by the frequency difference of different nodes in the network, it can also be automatically extended.

In BS2, it defines the location of the sending point. It stands for PHASE_SEG2 in CAN standard. Its value can be programmed into 1 to 8 time units, but it can also be automatically shortened to compensate for the negative drift of phase.

If a valid transition is detected in BS1 but not in SYNC_SEG, then the time of BS1 is extended by at most RSJW to delay the sampling point. On the contrary, if a valid transition is detected in BS2 but not in SYNC_SEG, then the time of BS2 is shortened at most RSJW to advance the sampling point.

In the above description, RSJW(the resynchronization hop width) defines the upper limit of how many time units can be extended or shortened in each bit. Its value can be programmed into 1 to 4 time units. The effective transition is defined as the first transition from the dominant bit to the recessive bit when CAN itself does not send the recessive bit.

Note:

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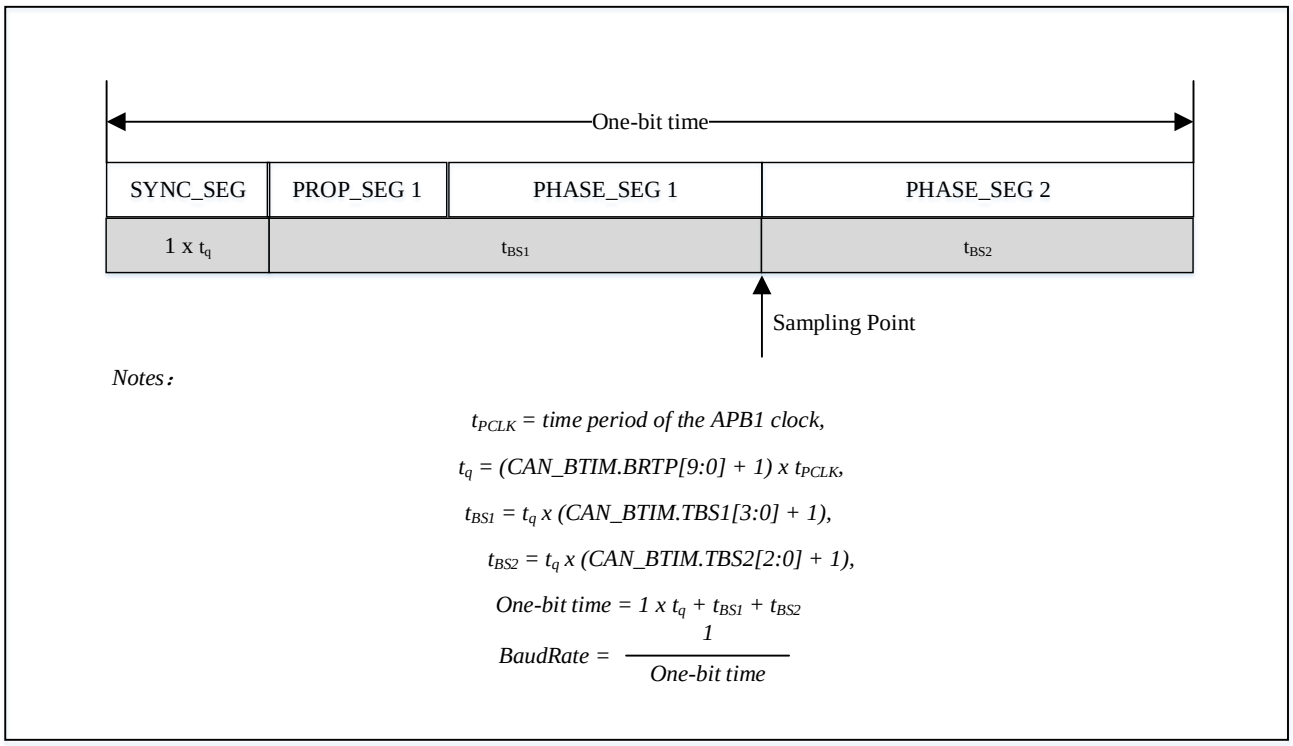
(1). The bit timing characteristics and resynchronization mechanism of CAN bits are detailed in the ISO11898 standard.

(2). In order to improve the CAN bit time accuracy, it is not recommended to use HSI as the clock source.

Figure 21-11 Bit Timing



Notes：

t_{PCLK} *= time period of the APB1 clock,*

$t_q = (CAN_BTIM.BRTP[9:0] + 1) \times t_{PCLK}$,

$t_{BS1} = t_q \times (CAN_BTIM.TBS1[3:0] + 1)$,

$t_{BS2} = t_q \times (CAN_BTIM.TBS2[2:0] + 1)$,

$One\text{-}bit\ time = 1 \times t_q + t_{BS1} + t_{BS2}$

$$BaudRate = \frac{1}{One\text{-}bit\ time}$$

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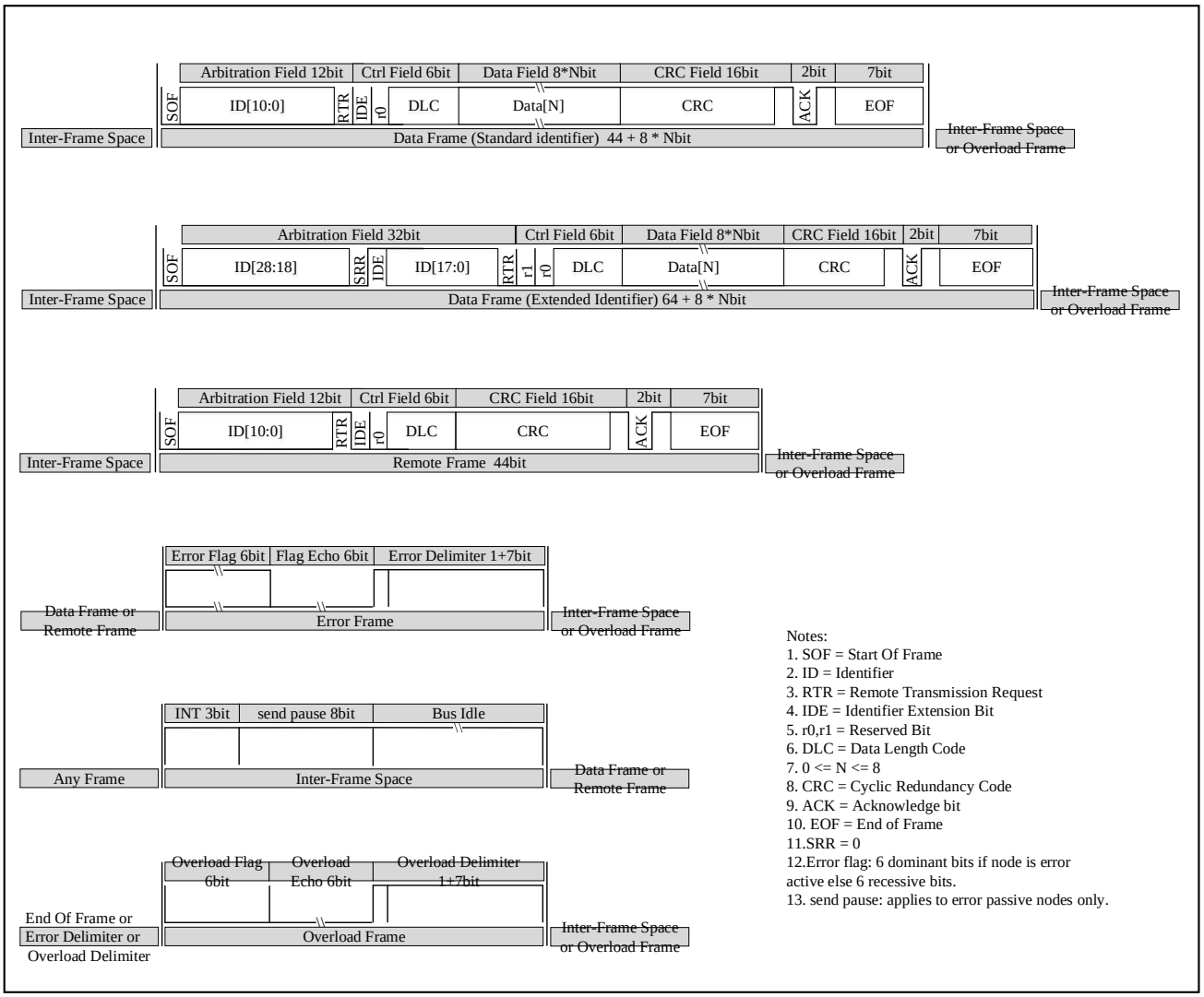
Figure 21-12 Various CAN Frames



Notes:
1. SOF = Start Of Frame
2. ID = Identifier
3. RTR = Remote Transmission Request
4. IDE = Identifier Extension Bit
5. r0,r1 = Reserved Bit
6. DLC = Data Length Code
7. 0 <= N <= 8
8. CRC = Cyclic Redundancy Code
9. ACK = Acknowledge bit
10. EOF = End of Frame
11.SRR = 0
12.Error flag: 6 dominant bits if node is error active else 6 recessive bits.
13. send pause: applies to error passive nodes only.

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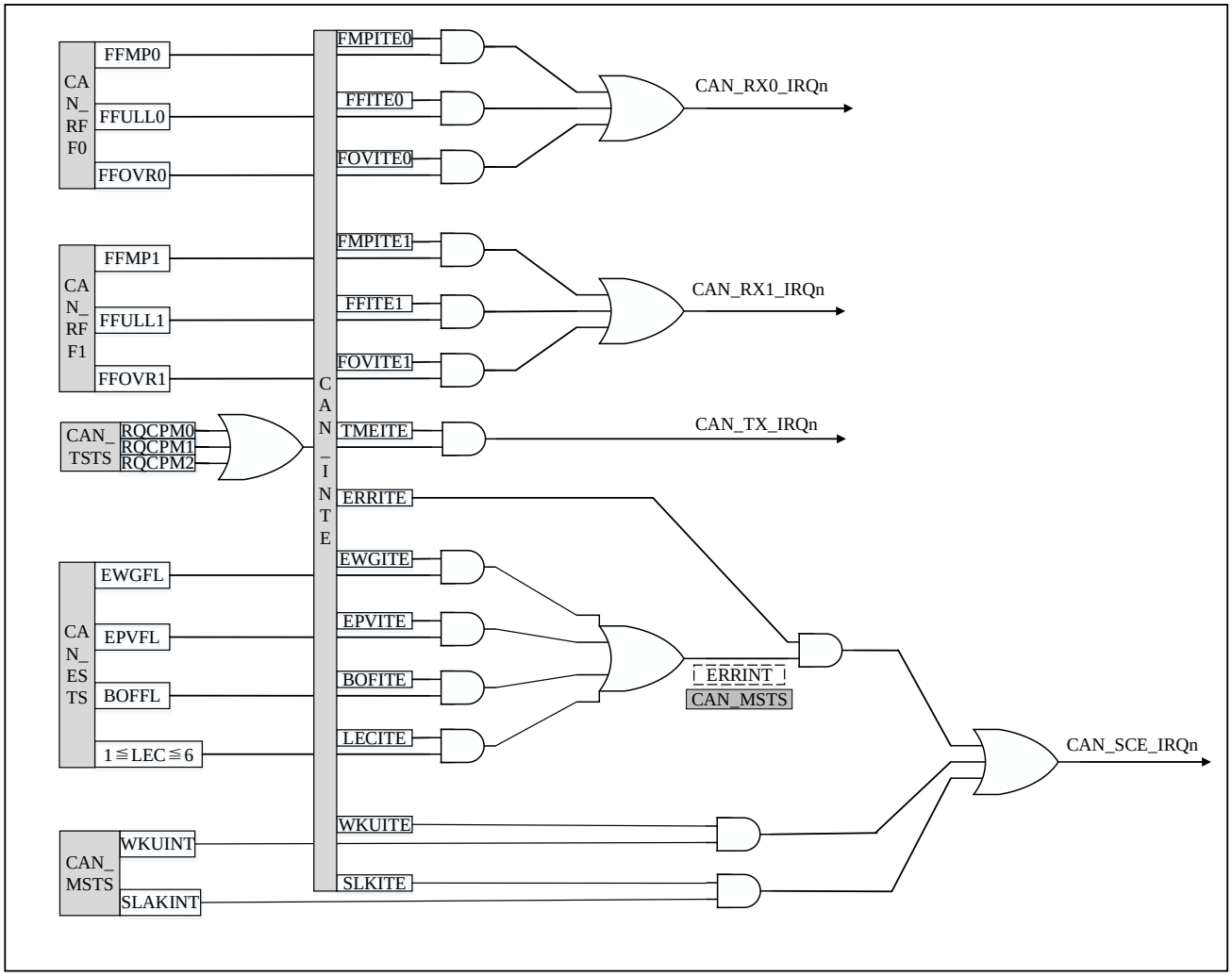
21.5 CAN Interrupt

Figure 21-13 Event Flag and Interrupt Generation



CAN has four interrupt vectors. By setting the CAN interrupt enable register (CAN_INTE), you can individually enable or disable each interrupt source. The following are the events that can generate each interrupt.

- FIFO0 interrupt(CAN_RX0_IRQn):

  FIFO0 receives a new message, and the CAN_RFF0.FFMP0 bit is not '00' ;

  When FIFO0 becomes full, and the CAN_ RFF0.FFULL0 bit is set;

  When FIFO0 overruns, and the CAN_ RFF0.FFOVR0 bit is set.

- FIFO1 interrupt(CAN_RX1_IRQn):

  FIFO1 receive a new message, and the CAN_RFF1.FFMP1 bit is not '00'.

  When FIFO1 becomes full, and the CAN_RFF1.FFULL1 bit is set.

  When FIFO1 overruns, and the CAN_ RFF1.FFOVR1 bit is set.

- Transmit interrupts(CAN_TX_IRQn):

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Transmit mailbox x becomes empty, and the corresponding CAN_TSTS.RQCPMx bit is set(x=1/2/3).

- Error and status change interrupt(CAN_SCE_IRQn):

  CAN enters sleep mode;

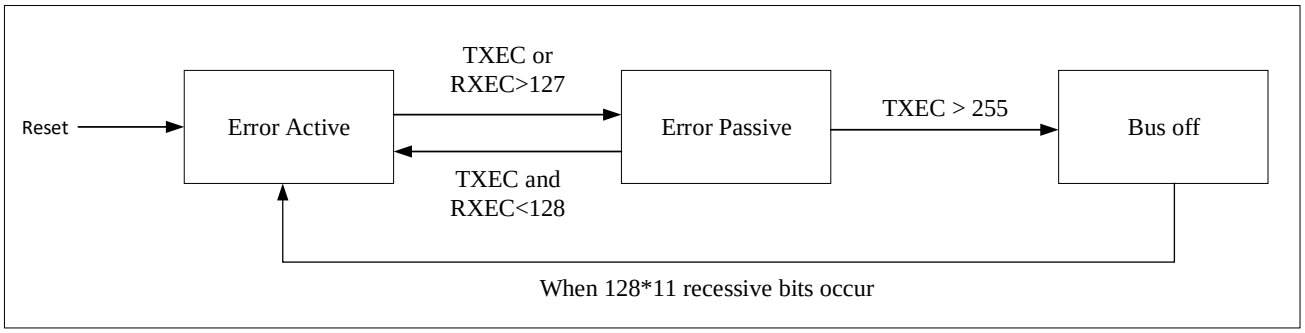
  Wake-up condition, the start of frame bit (SOF) is monitored on the CAN receiving pin.

  Error condition, please refer to the CAN error status register (CAN_ESTS) for details of the error.

21.5.1 Error Management

As described in CAN protocol, the error management is completely realized by hardware through transmitting error counter (CAN_ESTS.TXEC field) and receiving error counter (CAN_ESTS.RXEC field). The counter value will increase or decrease according to the error situation. Please refer to CAN standard if you want to know more detailed information about CAN_ESTS.TXEC and CAN_ESTS.RXEC management.

Figure 21-14 CAN Error State Diagram



Software can read out the value of the sending/receiving error counter to judge the stability of CAN network, and CAN_ESTS.LEC[2:0] bits can be read to get the detailed information of the current error status. What's more, by setting the CAN_INTE register (such as CAN_INTE. LECITE bit), the software can flexibly control the generation of interrupts when an error is detected.

21.5.2 Bus-off Recovery

When TXEC is greater than 255, the CAN_ESTS.BOFFL bit is set indicating that CAN goes bus-off. at this time, CAN can't receive and transmit messages.

In normal mode, according to the CAN_MCTRL.ABOM bit, CAN can automatically or at the request of software, recover from bus-off state, and change to error active state. If the CAN_MCTRL.ABOM bit is set, the recovery process will be started automatically after it has entered bus-off state. Otherwise, the recovery process will be started after software must request CAN to enter and then exit initialization mode. In both cases, CAN must wait for a recovery process described in CAN standard, that is 128*11 consecutive recessive bits are detected on CAN RX pin.

In initialization mode, CAN will not monitor the status of CAN RX pin, so the recovery process cannot be completed.

21.6 CAN Configuration Process

This chapter will introduce common configuration procedure of CAN while other details like functions of each mode and register bits are revealed in other part of this manual. CAN configuration flow can divided into serval phases. Some of the configurations can be changed anytime as long as prior requirements are satisfyied (e.g., filter value).

- Preparation Stage:

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- Configure RCC to enable CAN clock
- Configure RCC to enable AFIO and GPIO clock
- Write into GPIO registers to map CAN TX and CAN RX signals to desired GPIO pins.

- Basic Configuration Stage:

- After reset CAN device starts with Sleep mode.
- Exit Sleep mode by clearing CAN_MCTRL.SLPRQ bit.
- Enter Initialization mode by setting CAN_MCTRL.INIRQ bit.
- Wait for CAN_MSTS.INIAK bit become 1 (enter Initilization mode).
- Configure bit timing for CAN by writing value to CAN_BTIM.BSJW, CAN_BTIM.TBS2, CAN_BTIM.TBS1 and CAN_BTIM.BRTP bits. Baud rate of CAN bus is defined by the formula below:

$$BaudRate = \frac{1}{\big(1 + (TBS1 + 1) + (TBS2 + 1)\big) * (BRTP * t_{pclk})}$$

- Configure work mode options for CAN by writing to CAN_BTIM.SLM (silent) or CAN_BTIM.LBM in register.
- Configure CAN behavior(TTCM,ABOM,AWKUM,NART,RFLM,TXFP) through CAN_MCTRL. Most of the configuration in this register can be changed on the fly but its advised not to do so. Otherwise during few cycles, CAN behavior will become unpredictable.
- Exit Initialization mode by clearing CAN_MCTRL.INIRQ bit.
- Wait for CAN_MSTS.INIAK bit become 0 (exit Initilization mode).
- User can use filters to filter the messages they want to receive. To configure filter, user needs to write '1' to CAN_FMC.FINITM bit to request the filters to enter initialization mode. When filter is in initialization mode, CAN stops reception.
- Configure each filter for working mode (CAN_FM1), filter scale (CAN_FS1) and filter assignment (CAN_FFA1). User can also change filter value (CAN_FiRx) during this time. After completing filter configuration, clear CAN_FMC.FINITM bit to exit initialization for filters.

- For transmission:

- Enable the necessary transmit related interrupt CAN_INTE.TMEITE bit.
- Check status bits of each mailbox in CAN_TSTS. If any mailbox with TMEMx (x = 0~2) is '1', user can write the message, which is waiting for transmission, to the corresponding mailbox address. CAN_TMIx.TXRQ(x = 0~2) bit must be written to '1' after this mailbox is programed.
- After some time or after waiting for transmit interrupts, come back to check transmit status in CAN_TSTS. Repeat step 2~3 for new message transmission.

- For Reception:

- User can also change a filter value (**CAN_FiRx**) when the corresponding filter is deactivated. To deactivate certain filter, user needs to write '0' to the corresponding bit in **CAN_FA1** register.
- Configure reception related interrupts in CAN_INTE register.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- Once CAN has received message and stored them inside reception FIFO, user needs to read the corresponding FIFO on time and release reception mailbox by writing '1' to RFFOMx in register CAN_RFFx (x = 0,1).

21.7 CAN Registers

These peripheral registers must be operated as words (32 bits).

21.7.1 Register Description

21.7.1.1 Register access protection

When a CAN node is working normally, incorrect access/modification of some configuration registers may cause hardware errors in the node and temporarily interfere with the entire CAN network. Therefore, modification of the CAN_BTIM register is only allowed when the CAN core is in initialization mode.

Only when the send mailbox status bit CAN_TSTS.TMEM = 1 then the user can modify data to the send mailbox.

21.7.1.2 Control and status registers

By configuring these registers, user can: configure CAN parameters, such as operating mode and baud rate; start message transmitting; handling message reception; interrupt setting; read diagnostic information.

21.7.1.3 Mailbox register description

The transmitting and receiving mailboxes are basically the same except that the receiving mailbox is read-only and contains the CAN_RMDTx.FMI field. The transmitting mailbox is writable when it is empty.

***Notes**: the corresponding CAN_TSTS.TMEM bit is set, which means that the transmitting mailbox is empty.*

There are 3 transmitting mailboxes and 2 receiving FIFO. Each receiving FIFO has three mailboxes, and only the first received message in the FIFO can be accessed.

Each mailbox contains 4 registers:

FIFO0 contains CAN_RMI0, CAN_RMDT0, CAN_RMDL0, CAN_RMDH0;

FIFO1 contains CAN_RMI1, CAN_RMDT1, CAN_RMDL1, CAN_RMDH1;

Transmit mailbox (x) contains CAN_TMIx, CAN_TMDTx, CAN_TMDLx, CAN_TMDHx; x = 0,1,2.

21.7.1.4 Filter register description

The value of the filter can only be modified when the corresponding filter group is closed or the CAN_FMC.FINITM bit is set. In addition, only when the whole filter is set to the initialization mode (that is, CAN_FMC.FINITM=1), the settings of the filter can be modified, that is, the CAN_FM1,CAN_FS1 and CAN_FFA1 registers can be modified.

21.7.2 CAN Register Overview

Table 21-4 CAN Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	CAN_MCTRL	Reserved															DBGF	MRST	Reserved							TTCM	ABOM	AWKUM	NART	RFLM	TXFP	SLPRQ	INIRQ
	Reset Value																1	0								0	0	0	0	0	0	1	0
004h	CAN_MSTS	Reserved																				RXS	LSMP	RXMD	TXMD	Reserved			SLAKINT	WKUINT	ERRINT	SLPAK	INIAK

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

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	Reset Value																					1	1	0	0				0	0	0	1	0
008h	CAN_TSTS	LOWM[2:0]			TMEM[2:0]			CODE[1:0]		ABRQM2	Reserved			TERRM2	ALSTM2	TXOKM2	RQCPM2	ABRQM1	Reserved			TERRM1	ALSTM1	TXOKM1	RQCPM1	ABRQM0	Reserved			TERRM0	ALSTM0	TXOKM0	RQCPM0
	Reset Value	0	0	0	1	1	1	0	0	0				0	0	0	0	0				0	0	0	0	0				0	0	0	0
00Ch	CAN_RFF0	Reserved																										RFFOM0	FFOVR0	FFULL0	Reserved	FFMP0[1:0]	
	Reset Value																											0	0	0		0	0
010h	CAN_RFF1	Reserved																										RFFOM1	FFOVR1	FFULL1	Reserved	FFMP1[1:0]	
	Reset Value																											0	0	0		0	0
014h	CAN_INTE	Reserved														SLKITE	WKUITE	ERRITE	Reserved			LECITE	BOFITE	EPVITE	EWGITE	Reserved		FOVITE1	FFITE1	FMPITE1	FOVITE0	FFITE0	FMPITE0	TMEITE
	Reset Value															0	0	0				0	0	0	0			0	0	0	0	0	0	0
018h	CAN_ESTS	RXEC[7:0]								TXEC[7:0]								Reserved										LEC[2:0]			Reserved	BOFFL	EPVFL	EWGFL
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0											0	0	0		0	0	0
01Ch	CAN_BTIM	SLM	LBM	Reserved				RSJW[1:0]		Reserved	TBS2[2:0]			TBS1[3:0]				Reserved				BRTP[9:0]											
	Reset Value	0	0					0	1		0	1	0	0	0	1	1					0	0	0	0	0	0	0	0	0	0	0	0
020h - 17Fh	Reserved																																
180h	CAN_TMI0	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
184h	CAN_TMDT0	MTIM[15:0]																Reserved							TGT	Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
188h	CAN_TMDL0	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
18Ch	CAN_TMDH0	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
190h	CAN_TMI1	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
194h	CAN_TMDT1	MTIM[15:0]																Reserved							TGT	Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
198h	CAN_TMDL1	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
19Ch	CAN_TMDH1	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

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	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1A0h	CAN_TMI2	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
1A4h	CAN_TMDT2	MTIM[15:0]																Reserved							TGT	Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
1A8h	CAN_TMDL2	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1ACh	CAN_TMDH2	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1B0h	CAN_RMI0	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	Reserved
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1B4h	CAN_RMDT0	MTIM[15:0]																FMI[7:0]								Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x	x	x	x
1B8h	CAN_RMDL0	DATA3[7;0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1BCh	CAN_RMDH0	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1C0h	CAN_RMI1	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	Reserved
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1C4h	CAN_RMDT1	MTIM[15:0]																FMI[7:0]								Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x	x	x	x
1C8h	CAN_RMDL1	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1CCh	CAN_RMDH1	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1D0h - 1FFh	Reserved																																
200h	CAN_FMC	Reserved																															FINITM
	Reset Value																																1
204h	CAN_FM1	Reserved																		FB[13:0]														
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
208h	Reserved																																
20Ch	CAN_FS1	Reserved																		FSC[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
210h	Reserved																																
214h	CAN_FFA1	Reserved																		FAF[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
218h	Reserved																																
21Ch	CAN_FA1	Reserved																		FAC[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
220h	Reserved																																
224h - 23Fh	Reserved																																
240h	CAN_F0B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
244h	CAN_F0B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
248h	CAN_F1B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
24Ch	CAN_F1B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
. . .	. . .	Reserved																															
2A8h	CAN_F13B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
2ACh	CAN_F13B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

21.7.3 CAN Control and Status Register

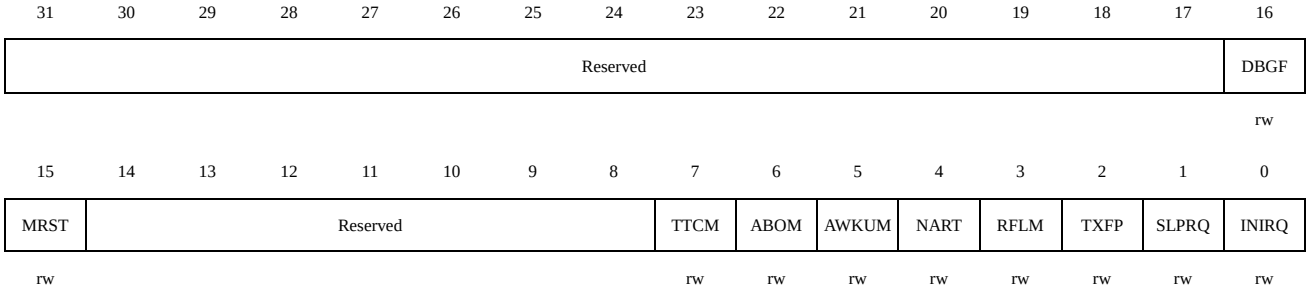
Abbreviations used in register descriptions, please refer to 1.1 section.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

21.7.3.1 CAN master control register (CAN_MCTRL)

Address: 0x00

Reset value: 0x0001 0002



Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	DBGF	Debug freeze 0: During debugging, CAN works as usual. 1: Freeze the reception/transmission of CAN during debugging. The receiving FIFO can still be read, written and controlled normally. ***Notes**: DBG_CTRL.CAN_STOP bit must be set when CAN is frozen, please refer to 21.3.7: Debugging mode.*
15	MRST	CAN software master reset 0: This peripheral works normally; 1: enforce reset CAN, after which CAN enters sleep mode and CAN_RFFx.FFMP bit and CAN_MCTRL register are initialized to their reset values. After that, the hardware automatically clears this bit.
14:8	Reserved	Reserved, the reset value must be maintained.
7	TTCM	Time triggered communication mode 0: disable time triggered communication mode; 1: enable time trigger communication mode. ***Notes**: For more information about time-triggered communication mode, please refer to 21.4.2: Time-triggered communication mode.*
6	ABOM	Automatic bus-off management This bit determines the conditions under which the CAN hardware can exit the bus-off state. 0: The process of exiting the bus-off state is that after the software sets the CAN_MCTRL.INIRQ bit and then clears it, once the hardware detects 128 consecutive 11-bit recessive bits, it exits the bus-off state; 1: Once the hardware detects 128 consecutive 11-bit recessive bits, it will automatically exit the bus-off state. ***Notes**: For more information about bus-off status, please refer to 21.5.1: Error management.*
5	AWKUM	Automatic wake up mode This bit determines whether CAN is awakened by hardware or software when it is in sleep mode.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		0: The sleep mode is awakened by the software by clearing the CAN_MCTRL.SLPRQ bit; 1: Sleep mode is automatically awakened by hardware by detecting CAN messages. At the same time of wake-up, the hardware automatically clears the CAN_MSTS.SLPRQ and CAN_MSTS.SLPAK bits.
4	NART	No automatic retransmission 0: According to the CAN standard, when the CAN hardware fails to send a message, it will automatically retransmit it until it is successfully sent; 1: CAN message is only sent once, regardless of the sending result (success, error or arbitration loss).
3	RFLM	Receive FIFO locked mode. 0: the FIFO is not locked when receiving overflows, and when the message of the receiving FIFO is not read out, the next received message will overwrite the last message; 1: FIFO is locked when receiving overflow. When the message of receiving FIFO is not read out, the next received message will be discarded.
2	TXFP	Transmit FIFO priority When there are multiple messages waiting to be sent at the same time, this bit determines the sending order of these messages. 0: Priority is determined by the identifier of the message; 1: Priority is determined by the order in which requests are sent.
1	SLPRQ	Sleep mode request The software can request the CAN to enter the sleep mode by setting this bit, and once the current CAN activity (sending or receiving messages) ends, the CAN will enter the sleep mode. Clear by software to make CAN exit sleep mode. When the CAN_MCTRL.AWKUM bit is set and the SOF bit is detected in the CAN Rx signal, the hardware clears this bit. This bit is set after reset, that is, CAN is in sleep mode after reset.
0	INIRQ	Initialization request clear this bit by software can make CAN exit from initialization mode: when CAN leaves Initialization mode and entering normal mode, it needs to detect 11 consecutive recessive bits at the receiving pin, CAN will be synchronized and ready for receiving and sending data. To this end, the hardware correspondingly the CAN_MSTS.INIAK bit is cleared. Setting this bit by software enables CAN to enter initialization mode from normal operation mode: once the current CAN activity (sending or receiving) is over, the hardware sets the CAN_MSTS.INIAK bit and CAN enters initialization mode.

21.7.3.2 **CAN master status register (CAN_MSTS)**

Address: 0x04

Reset value: 0x0000 0c02

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RXS	LSMP	RXMD	TXMD	Reserved			SLAKINT	WKUINT	ERRINT	SLPAK	INIAK
				r	r	r	r				rc_w1	rc_w1	rc_w1	r	r

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	RXS	CAN Rx signal This bit reflects the actual level of the CAN receive pin (CAN_RX).
10	LSMP	Last sample point The last sampled value of the CAN receive pin (corresponding to the value of the current receive bit).
9	RXMD	Receive mode if this bit equals to 1 indicates CAN is currently the receiver.
8	TXMD	Transmit mode if this bit equals to 1 indicates CAN is currently the transmitter.
7:5	Reserved	Reserved, the reset value must be maintained.
4	SLAKINT	Sleep acknowledge interrupt When CAN_INTE.SLKITE=1, once CAN enters sleep mode, hardware will set this bit, and then the corresponding interrupt will be triggered. When this bit is set, if the CAN_INTE.SLKITE bit is set, a state change interrupt will be generated. Software can clear this bit, and hardware also clears this bit when CAN_MSTS.SLPAK bit is cleared. ***Notes**: When CAN_INTE.SLKITE=0, this bit should not be queried, but the CAN_MSTS.SLPAK bit should be queried to know the sleep state.*
3	WKUINT	Wakeup interrupt When CAN is in sleep state, once the start of frame bit (SOF) is detected, the hardware will set this bit; And if the CAN_INTE.WKUITE bit is set, a state change interrupt is generated. This bit is cleared by software.
2	ERRINT	Error interrupt When an error is detected, a bit of the CAN_ESTS register will be set, and if the corresponding interrupt enable bit of the CAN_INTE register is also set, the hardware will set this bit; If the CAN_INTE.ERRITE bit is set, a state change interrupt is generated. This bit is cleared by software.
1	SLPAK	Sleep acknowledge This bit is set by hardware, indicating that the software CAN module is in sleep mode. This bit is the confirmation of the software request to enter sleep mode (the CAN_MCTRL.SLPRQ bit is set). Hardware clears this bit when CAN exits sleep mode (CAN leaves Sleep mode and entering normal mode,it needs to be synchronized with CAN bus). Synchronization with CAN bus here means that the hardware needs to detect 11 consecutive recessive bits on the RX pin of CAN. ***Notes**: clearing CAN_MCTRL.SLPRQ bit by software or hardware will start the process of exiting sleep mode. See the description of CAN_MCTRL.AWKUM bit for details of clearing*

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		CAN_MCTRL.SLPRQ bit.
0	INIAK	Initialization acknowledge This bit is set by hardware, indicating that the software CAN module is in initialization mode. This bit is the confirmation of the software request to enter the initialization mode (the CAN_MCTRL.INIRQ bit is set). Hardware clears this bit when CAN exits initialization mode (CAN leaves Initialization mode and entering normal mode,it needs to be synchronized with CAN bus). Synchronization with CAN bus here means that the hardware needs to detect 11 consecutive recessive bits on the RX pin of CAN.

21.7.3.3 CAN transmit status register (CAN_TSTS)

Address: 0x08

Reset value: 0x1C00 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOWM2	LOWM1	LOWM0	TMEM2	TMEM1	TMEM0	CODE[1:0]		ABRQM2	Reserved			TERRM2	ALSTM2	TXOKM2	RQCPM2
r	r	r	r	r	r	r	r	rs				rc_w1	rc_w1	rc_w1	rc_w1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABRQM1	Reserved			TERRM1	ALSTM1	TXOKM1	RQCPM1	ABRQM0	Reserved			TERRM0	ALSTM0	TXOKM0	RQCPM0
rs				rc_w1	rc_w1	rc_w1	rc_w1	rs				rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31	LOWM2	Lowest priority flag for mailbox 2 When multiple mailboxes are waiting to send messages, and the priority of mailbox 2 is the lowest, hardware sets this bit.
30	LOWM1	Lowest priority flag for mailbox 1 When multiple mailboxes are waiting to send messages, and the priority of mailbox 1 is the lowest, hardware sets this bit.
29	LOWM0	Lowest priority flag for mailbox 0 When multiple mailboxes are waiting to send messages, and the priority of mailbox 0 is the lowest, hardware sets this bit. ***Notes**: If there is only one mailbox waiting, CAN_TSTS.LOWM[2:0] is cleared*
28	TMEM2	Transmit mailbox 2 empty When there is no message waiting to be sent in mailbox 2, hardware sets this bit.
27	TMEM1	Transmit mailbox 1 empty When there is no message waiting to be sent in mailbox 1, hardware sets this bit.
26	TMEM0	Transmit mailbox 0 empty When there is no message waiting to be sent in mailbox 0, hardware sets this bit .
25:24	CODE[1:0]	Mailbox code When at least one sending mailbox is empty, these two bits represent the next empty sending mailbox number.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		When all sending mailboxes are empty, these two bits represent the sending mailbox number with the lowest priority.
23	ABRQM2	Abort request for mailbox 2 Set this bit, software can stop the sending request of mailbox 2, and hardware clears this bit when the sending message of mailbox 2 is idle. If there is no message waiting to be sent in mailbox 2, it will have no effect to set this bit.
22:20	Reserved	Reserved, hardware force is 0.
19	TERRM2	Transmission error of mailbox 2 failed. When the mailbox 2 fails to send due to an error, set this bit.
18	ALSTM2	Arbitration lost for mailbox 2 When the mailbox 2 fails to send due to the loss of arbitration, set this bit.
17	TXOKM2	Transmission OK of mailbox 2 The hardware updates this bit after each sending attempt of mailbox 2: 0: The last sending attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 2 is successfully completed, hardware sets this bit. See Figure 21-7.
16	RQCPM2	Request completed mailbox 2 When the last request (send or abort) for mailbox 2 is completed, the hardware will set this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clear this bit (the CAN_TMI2.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM2, CAN_TSTS.ALSTM2 and CAN_TSTS.TERRM2 bits) of mailbox 2 are also cleared.
15	ABRQM1	Abort request for mailbox 1 Set this bit, the software can stop the sending request of mailbox 1, and the hardware clears this bit when the sending message of mailbox 1 is idle. If there is no message waiting to be sent in mailbox 1, it will have no effect to set this bit.
14:12	Reserved	Reserved, the reset value must be maintained.
11	TERRM1	Transmission error of mailbox 1 When the mailbox 1 fails to send due to an error, set this bit.
10	ALSTM1	Arbitration lost for mailbox 1 When the mailbox 1 fails to send due to the loss of arbitration, set this bit
9	TXOKM1	Transmission OK of mailbox 1 The hardware updates this bit after each sending attempt of mailbox 1: 0: The last sending attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 1 is successfully completed, the hardware sets this bit. See Figure 21-7.
8	RQCPM1	Request completed mailbox 1 When the last request (send or abort) for mailbox 1 is completed, the hardware sets this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clears this bit (the CAN_TMI1.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM1,

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		CAN_TSTS.ALSTM1 and CAN_TSTS.TERRM1 bits) of mailbox 1 are also cleared.
7	ABRQM0	Abort request for mailbox 0 The software can stop the sending request of mailbox 0 by setting this bit , and the hardware clears this bit when the sending message of mailbox 0 is idle. If there is no message waiting to be sent in mailbox 0, it will have no effect to set this bit.
6:4	Reserved	Reserved, the reset value must be maintained.
3	TERRM0	Transmission error of mailbox 0 When the mailbox 0 fails to send due to an error, set this bit.
2	ALSTM0	Arbitration lost for mailbox 0 When the mailbox 0 fails to send due to the loss of arbitration, set this bit
1	TXOKM0	Transmission OK of mailbox 0 The hardware updates this bit after each attempt to send mailbox 0: 0: The last send attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 0 is successfully completed, the hardware sets this bit. See Figure 21-7.
0	RQCPM0	Request completed mailbox 0 When the last request (send or abort) for mailbox 0 was completed, the hardware sets this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clears this bit (the CAN_TMI0.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM0, CAN_TSTS.ALSTM0 and CAN_TSTS.TERRM0 bits) of mailbox 0 are also cleared.

21.7.3.4 **CAN receive FIFO 0 register (CAN_RFF0)**

Address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										RFFOM0	FFOVR0	FFULL0	Reserved	FFMP0[1:0]	
										rs	rc_w1	rc_w1		r	r

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	RFFOM0	Release FIFO 0 output mailbox. The software releases the output mailbox of the receive FIFO by setting this bit. If the receiving FIFO is empty, it will have no effect on setting this bit, that is, it will be meaningful to set this bit only when there is a message in the FIFO. If there are more than two messages in FIFO, because of the characteristics of FIFO, the software needs to release the output mailbox to

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		access the second message. When the output mailbox is released, the hardware clears this bit.
4	FFOVR0	FIFO 0 overrun When FIFO 0 is full, a new message is received and the message meets the filtering conditions, the hardware sets this bit. This bit is cleared by software.
3	FFULL0	FIFO 0 full When there are 3 messages in FIFO 0, the hardware sets this bit'. This bit is cleared by software.
2	Reserved	Reserved, the reset value must be maintained.
1:0	FFMP0[1:0]	FIFO 0 message pending Number of FIFO messages 0 These two bits reflect the number of messages currently stored in the receiving FIFO 0. Every time a new message is stored in the receiving FIFO 0, the hardware adds 1 to the CAN_RFF0.FFMP0. Every time the software writes '1' to the CAN_RFF0.RFFOM0 bit to release the output mailbox, CAN_RFF0.FFMP0 is decremented by 1 until it is 0.

21.7.3.5 CAN receive FIFO 1 register (CAN_RFF1)

Address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										RFFOM1	FFOVR1	FFULL1	Reserved	FFMP1[1:0]	
										rs	rc_w1	rc_w1		r	r

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	RFFOM1	Release FIFO 1 output mailbox. The software releases the output mailbox of the receive FIFO by setting this bit. If the receiving FIFO is empty, it will have no effect on setting this bit, that is, it will be meaningful to set this bit only when there is a message in the FIFO. If there are more than two messages in FIFO, because of the characteristics of FIFO, the software needs to release the output mailbox to access the second message. When the output mailbox is released, the hardware clears this bit.
4	FFOVR1	FIFO 1 overrun When FIFO 1 is full, a new message is received and the message meets the filtering conditions, the hardware sets this bit. This bit is cleared by software.
3	FFULL1	FIFO 1 full When there are 3 messages in FIFO 1, the hardware sets this bit. This bit is cleared by software.
2	Reserved	Reserved, the reset value must be maintained.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
1:0	FFMP1[1:0]	FIFO 1 message pending Number of messages in FIFO 1 These two bits reflect the number of messages stored in the current receiving FIFO 1. Every time a new message is stored in receiving FIFO 1, the hardware adds 1 to CAN_RFF1.FFMP1. Every time the software releases the output mailbox by writing '1' to CAN_RFF1.RFFOM1 bit, CAN_RFF1.FFMP1 is decremented by 1 until it is 0.

21.7.3.6 CAN interrupt enable register (CAN_INTE)

Address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														SLKITE	WKUITE
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRITE	Reserved			LECITE	BOFITE	EPVITE	EWGITE	Reserved	FOVITE1	FFITE1	FMPITE1	FOVITE0	FFITE0	FMPITE0	TMEITE
rw				rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	SLKITE	Sleep interrupt enable 0: when the CAN_MSTS.SLAKINT bit is set, no interrupt is generated; 1: when the CAN_MSTS.SLAKINT bit is set, an interrupt is generated.
16	WKUITE	Wakeup interrupt enable 0: when CAN_MSTS.WKUINT bit is set, no interrupt is generated; 1: when CAN_MSTS.WKUINT bit is set, an interrupt is generated.
15	ERRITE	Error interrupt enable 0: When there is an error registration in the CAN_ESTS register, no interrupt is generated; 1: When there is an error registration in the CAN_ESTS register, an interrupt is generated.
14:12	Reserved	Reserved, the reset value must be maintained.
11	LECITE	Last error code interrupt enable 0: When an error is detected, when the hardware sets CAN_ESTS.LEC[2:0], the CAN_MSTS.ERRINT bit is not set; 1: When an error is detected, when the hardware sets CAN_ESTS.LEC[2:0], the CAN_MSTS.ERRINT bit is set.
10	BOFITE	Bus-off interrupt enable 0: When CAN_ESTS.BOFFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: When the CAN_ESTS.BOFFL bit is set, set the CAN_MSTS.ERRINT bit.
9	EPVITE	Error passive interrupt enable 0: when CAN_ESTS.EPVFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: when CAN_ESTS.EPVFL bit is set, set the CAN_MSTS.ERRINT bit.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
8	EWGITE	Error warning interrupt enable 0: When CAN_ESTS.EWGFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: when the CAN_ESTS.EWGFL bit is set, set the CAN_MSTS.ERRINT bit.
7	Reserved	Reserved, the reset value must be maintained.
6	FOVITE1	FIFO 1 overflow interrupt enable 0: When CAN_RFF1.FFOVR bit is set, no interrupt is generated; 1: When CAN_RFF1.FFOVR bit is set, an interrupt is generated.
5	FFITE1	FIFO 1 full interrupt enable 0: When CAN_RFF1.FFULL bit is set, no interrupt is generated; 1: When CAN_RFF1.FFULL bit is set, an interrupt is generated.
4	FMPITE1	FIFO 1 message pending interrupt enable 0: When CAN_RFF1.FFMP[1:0] bits are non-0, no interrupt is generated; 1: When CAN_RFF1.FFMP[1:0] bits are not 0, an interrupt is generated.
3	FOVITE0	FIFO 0 overflow interrupt enable 0: When CAN_RFF0.FFOVR bit is set, no interrupt is generated; 1: When CAN_RFF0.FFOVR bit is set, an interrupt is generated.
2	FFITE0	FIFO 0 full interrupt enable 0: When CAN_RFF0.FFULL bit is set, no interrupt is generated; 1: When CAN_RFF0.FFULL bit is set, an interrupt is generated.
1	FMPITE0	FIFO 0 message pending interrupt enable 0: When CAN_RFF0.FFMP[1:0] bits are non-0, no interrupt is generated; 1: When CAN_RFF0.FFMP[1:0] bits are not 0, an interrupt is generated.
0	TMEITE	Transmit mailbox empty interrupt enable. 0: When CAN_TSTS.RQCPMx bit is set, no interrupt is generated; 1: When CAN_TSTS.RQCPMx bit is set, an interrupt is generated. ***Notes**: Please refer to 21.5 Section CAN interrupt.*

21.7.3.7 CAN error status register (CAN_ESTS)

Address: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXEC[7:0]								TXEC[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								LEC[2:0]			Reserved	BOFFL	EPVFL	EWGFL	
								rw	rw	rw		r	r	r	

Bit Field	Name	Description
31:24	RXEC[7:0]	Receive error counter This counter is implemented according to the receiving part of the fault definition mechanism of

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		CAN protocol. According to the standard of CAN, when receiving error, the counter is incremented by 1 or incremented by 8 according to the error condition; After each successful reception, the counter is decremented by 1, or when the value of the counter is greater than 127, its value is set to 120. When the value of this counter exceeds 127, CAN enters the error passive state.
23:16	TXEC[7:0]	Least significant byte of the 9-bit transmit error counter Similar to the above, this counter is implemented according to the sending part of the fault definition mechanism of CAN protocol.
15:7	Reserved	Reserved, the reset value must be maintained.
6:4	LEC[2:0]	The Last error code. When an error is detected on the CAN bus, the hardware is set according to the error situation. When the message is sent or received correctly, the hardware clears its value to '0'. The hardware does not use error code 7, and the software can set this value, so that the code update can be detected. 000: there is no error; 001: Bit padding error; 010: wrong Format (form); 011: Acknowledgment (ack) error; 100: recessive dislocation（CAN transmits recessive but detect dominant on the bus）; 101: dominant dislocation(CAN transmits dominant but detect recessive on the bus); 110: CRC error; 111: Set by software.
3	Reserved	Reserved, the reset value must be maintained.
2	BOFFL	Bus-off flag When going bus-off, hardware sets this bit. When the transmission error counter CAN_TSTS.TXEC overflows, that is, it is greater than 255, CAN goes bus-off. Please refer to 21.5.1 section.
1	EPVFL	Error passive flag When the number of errors reaches the threshold of error passivity, the hardware sets the bit. (The value of the receiving error counter or the sending error counter is > 127).
0	EWGFL	Error warning flag When the number of errors reaches the warning threshold, the hardware sets the bit. (The value of the receiving error counter or the sending error counter is ≥96).

21.7.3.8 **CAN bit timing register (CAN_BTIM)**

Address: 0x1C

Reset value: 0x012 0000

***Notes**: This register CAN only be accessed by software when CAN is in initialization mode.*

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SLM	LBM	Reserved				RSJW[1:0]		Reserved	TBS2[2:0]			TBS1[3:0]			
rw	rw					rw	rw		rw	rw	rw	rw	rw	rw	rw

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						BRTP[9:0]									
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31	SLM	Silent mode（debug） 0: Normal state; 1: Silent mode.
30	LBM	Loop back mode（debug） 0: Loopback mode is prohibited; 1: Loopback mode is allowed.
29:26	Reserved	Reserved, the reset value must be maintained.
25:24	RSJW[1:0]	Resynchronization jump width For resynchronization, this bit field defines the upper limit of how many time units CAN be extended or shortened by CAN hardware in each bit. $t_{RJW} = t_{CAN}$ x (RSJW[1:0] + 1).
23	Reserved	Reserved, the reset value must be maintained.
22:20	TBS2[2:0]	Time segment 2 This bit field defines how many time units time period 2 occupies. $t_{BS2} = t_{CAN}$ x (TBS2[2:0] + 1).
19:16	TBS1[3:0]	Time segment 1 This bit field defines how many time units time period 1 occupies. $t_{BS1} = t_{CAN}$ x (TBS1[3:0] + 1) For details of bit time characteristics, please refer to section 21.4.7 secton: bit time characteristics.
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	BRTP[9:0]	Baud rate prescaler This bit field defines the time length of the time unit (tq) t_q =(BRTP[9:0]+1) x t_{PCLK}

21.7.4 CAN Mailbox Register

This section describes the sending and receiving mailbox registers. For more information about register mapping, refer to 21.4.6 section: message storage.

21.7.4.1 Tx mailbox identifier register (CAN_TMIx) (x=0..2)

Address: 0x180, 0x190, 0x1A0

Reset value: 0xXXXX XXXX,X= undefined bit (except bit 0, TXRQ=0 at reset)

***Notes**: 1.This register is write-protected when the mailbox to which it belongs is waiting to be sent;*

2.This register implements the send request control function (bit 0)-the reset value is 0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

STDID[10:0]/EXTID[28:18]											EXTID[17:13]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTID[12:0]													IDE	RTRQ	TXRQ
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:21	STDID[10:0]/EXTID[28:18]	Standard identifier or extended identifier Depending on the content of CAN_TMIx.IDE bits, these bits are either standard identifiers or high bytes of extended identity.
20:3	EXTID[17:0]	Extended identifier Low byte of extended identity.
2	IDE	Identifier extension. This bit determines the type of identifier used for sending messages in the mailbox. 0: Use standard identifier; 1: Use extended identifiers.
1	RTRQ	The Remote transmission request 0: data frame; 1: Remote frame.
0	TXRQ	Transmit mailbox request It is set by the software to request to send the data of the mailbox. When the data transmission is completed and the mailbox is empty, hardware clears it.

21.7.4.2 Tx mailbox data length and time stamp register (CAN_TMDTx) (x=0..2)

When the mailbox is not empty, all bits in this register are write-protected.

Address: 0x184, 0x194, 0x1A4

Reset value: undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MTIM[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							TGT	Reserved				DLC[3:0]			
							rw					rw	rw	rw	rw

Bit Field	Name	Description
31:16	MTIM[15:0]	Message time stamp This field contains the value of the 16-bit timer at the time of sending the message SOF.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained.
8	TGT	Transmit global time This bit is valid only when the CAN is in time-triggered communication mode, that is, the CAN_MCTRL.TTCM bit is set. 0: Do not send the time stamp CAN_TMDTx.MTIM[15:0]; 1: send the time stamp CAN_TMDTx.MTIM[15:0]. In a message of length 8, the time stamp CAN_TMDTx.MTIM[15:0] is the last two bytes sent: CAN_TMDTx.MTIM[7:0] is the seventh byte and CAN_TMDTx.MTIM[15:8] is the eighth byte. They replace the data written in CAN_TMDHx[31:16] (CAN_TMDLx.DATA6[7:0] and CAN_TMDLx.DATA7[7:0]). In order to send the 2 bytes of the timestamp, DLC must be programmed to 8.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DLC[3:0]	Data length code This field specifies the data length of the data message or the data length requested by the remote frame. One message contains 0 to 8 bytes of data, which is determined by DLC.

21.7.4.3 Tx mailbox low byte data register (CAN_TMDLx) (x=0..2)

When the mailbox is not empty, all bits in this register are write-protected.

Address: 0x188, 0x198, 0x1A8

Reset value: undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA3[7:0]								DATA2[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA1[7:0]								DATA0[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:24	DATA3[7:0]	Data byte 3 Data byte 3 of the message.
23:16	DATA2[7:0]	Data byte 2 Data byte 2 of the message.
15:8	DATA1[7:0]	Data byte 1 Data byte 1 of the message.
7:0	DATA0[7:0]	Data byte 0 Data byte 0 of the message. *Notes:the message contains 0 to 8 bytes of data, starting from byte 0.*

21.7.4.4 Tx mailbox high byte data register (CAN_TMDHx) (x=0..2)

When the mailbox is not empty, all bits in this register are write protected.

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Address: 0x188, 0x198, 0x1A8

Reset value: undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA7[7:0]								DATA6[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA5[7:0]								DATA4[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:24	DATA7[7:0]	Data byte 7 Data byte 7 of the message. *Notes: If the CAN_MCTRL.TTCM bit is '1' and the CAN_TMDTx.TGT bit of this mailbox is also '1', then DATA7 and DATA6 will be replaced by TIME stamps.*
23:16	DATA6[7:0]	Data byte 6 Data byte 6 of the message.
15:8	DATA5[7:0]	Data byte 5 Data byte 5 of the message.
7:0	DATA4[7:0]	Data byte 4 Data byte 4 of the message.

21.7.4.5 **Receive FIFO mailbox identifier register (CAN_RMIx) (x=0..1)**

Address offset: 0x1B0, 0x1C0

Reset value: undefined

Notes: All receiving mailbox registers are read-only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STDID[10:0]/EXTID[28:18]											EXTID[17:13]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTID[12:0]													IDE	RTRQ	TXRQ
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:21	STDID[10:0]/EXTID[28:18]	Standard identifier or extended identifier Depending on the content of CAN_RMIx.IDE bits, these bits are either standard identifiers or high bytes of extended identity.
20:3	EXTID[17:0]	Extended identifier

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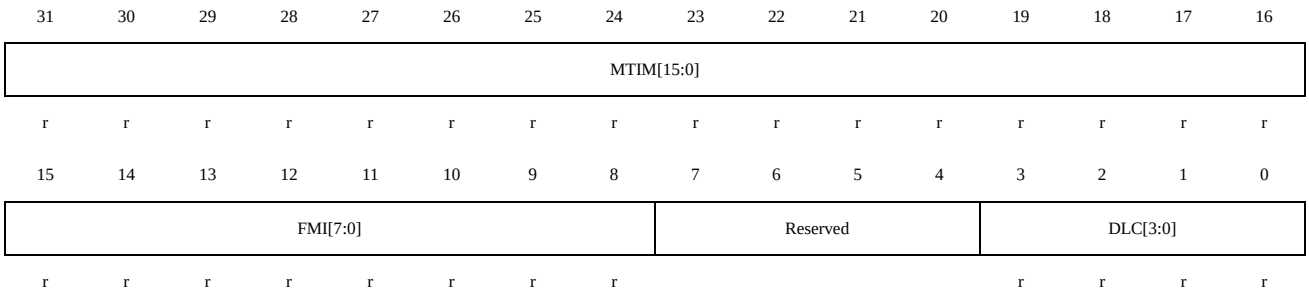
Bit Field	Name	Description
		Low byte of extended identity.
2	IDE	Identifier extension. This bit determines the type of identifier used for sending messages in the mailbox. 0: Use standard identifier; 1: Use extended identifiers.
1	RTRQ	Remote transmission request 0: data frame; 1: Remote frame.
0	Reserved	Reserved, the reset value must be maintained.

21.7.4.6 Receive FIFO mailbox data length and time stamp register (CAN_RMDTx) (x=0..1)

Address offset: 0x1B4, 0x1C4

Reset value: undefined

***Notes**: All receiving mailbox registers are read-only.*



Bit Field	Name	Description
31:16	MTIM[15:0]	Message time stamp This field contains the value of the 16-bit timer at the time of sending the message SOF.
15:8	FMI[7:0]	Filter match index Here is the filter serial number of the information transfer stored in the mailbox. For details of identifier filtering, please refer to 21.4.5 section: Identifier filtering.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DLC[3:0]	Data length code This field indicates the data length (0~8) of the received data frame. For remote frame requests, the data length DLC is always 0.

21.7.4.7 Receive FIFO mailbox low byte data register (CAN_RMDLx) (x=0..1)

Address offset: 0x1B8, 0x1C8

Reset value: undefined

***Notes**: All receiving mailbox registers are read-only.*

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DATA3[7:0]								DATA2[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA1[7:0]								DATA0[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:24	DATA3[7:0]	Data byte 3 Data byte 3 of the message.
23:16	DATA2[7:0]	Data byte 2 Data byte 2 of the message.
15:8	DATA1[7:0]	Data byte 1 Data byte 1 of the message.
7:0	DATA0[7:0]	Data byte 0 Data byte 0 of the message. Notes: the message contains 0 to 8 bytes of data, starting from byte 0.

21.7.4.8 **Receive FIFO mailbox high byte data register (CAN_RMDHx) (x=0..1)**

Address offset: 0x1BC, 0x1CC

Reset value: undefined

Note: All receiving mailbox registers are read-only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA7[7:0]								DATA6[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA5[7:0]								DATA4[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:24	DATA7[7:0]	Data byte 7 Data byte 7 of the message.
23:16	DATA6[7:0]	Data byte 6 Data byte 6 of the message.
15:8	DATA5[7:0]	Data byte 5 Data byte 5 of the message.
7:0	DATA4[7:0]	Data byte 4 Data byte 4 of the message.

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Email：info@nationstech.com
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21.7.5 CAN Filter Register

21.7.5.1 CAN filter master control register (CAN_FMC)

Address offset: 0x200

Reset value: 0x2A1C 0E01

***Notes**: The unreserved bits of this register are completely controlled by software.*

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															FINITM
															rw

Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	FINITM	Filter init mode Initialization mode settings for all filter groups. 0: The filter group works in normal mode; 1: The filter group works in initialization mode.

21.7.5.2 CAN filter mode register (CAN_FM1)

Address offset: 0x204

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FB13	FB12	FB11	FB10	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:0	FBx	Filter mode Working mode of filter group X 0: Two 32-bit registers of CAN_FiRx work in identifier mask mode;

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Bit Field	Name	Description
		1: Two 32-bit registers of CAN_FiRx work in identifier list mode.

21.7.5.3 CAN filter scale register (CAN_FS1)

Address offset: 0x20C

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FSC13	FSC12	FSC11	FSC10	FSC9	FSC8	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:0	FSCx	Filter scale configuration Bit width of filter group x (13~0). 0: The filter bit width is 2 16-bits; 1: The filter bit width is a single 32-bit.

21.7.5.4 CAN filter FIFO assignment register (CAN_FFA1)

Address offset: 0x214

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FAF13	FAF12	FAF11	FAF10	FAF9	FAF8	FAF7	FAF6	FAF5	FAF4	FAF3	FAF2	FAF1	FAF0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:0	FAFx	Filter FIFO assignment for filter x

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Email：info@nationstech.com
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Bit Field	Name	Description
		After the message is filtered by a certain filter, it will be stored in its associated FIFO. 0: the filter is associated to FIFO0; 1: the filter is associated to FIFO1.

21.7.5.5 CAN filter activation register (CAN_FA1)

Address: 0x21C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FAC13	FAC12	FAC11	FAC10	FAC9	FAC8	FAC7	FAC6	FAC5	FAC4	FAC3	FAC2	FAC1	FAC0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:0	FACx	Filter active The software sets '1' for someone to activate the corresponding filter. The corresponding filter register i(CAN_FiR[2:1]) can only be modified after the CAN_FA1.FACx bit is cleared or the CAN_FMC.FINITM bit is set. 0: The filter is disabled; 1: The filter is activated.

21.7.5.6 CAN filter i register x (CAN_FiRx) (i=0..13; x=1..2)

Address offset: 0x240h, 0x31C

Reset value: undefined

***Notes**: 14 groups of filters: i = 0 ... 13. Each group of filters consists of two 32-bit registers, CAN_FiR[2:1].*

Only when the corresponding CAN_FA1.FACx bit is cleared or the CAN_FMC.FINIT bit is set, the corresponding filter register can be modified.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FBC31	FBC30	FBC29	FBC28	FBC27	FBC26	FBC25	FBC24	FBC23	FBC22	FBC21	FBC20	FBC19	FBC18	FBC17	FBC16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FBC15	FBC14	FBC13	FBC12	FBC11	FBC10	FBC9	FBC8	FBC7	FBC6	FBC5	FBC4	FBC3	FBC2	FBC1	FBC0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:0	FBC[31:0]	Filter bits Identifier pattern Each bit of the register corresponds to the level of the corresponding bit of the expected identifier. 0: the corresponding bit is expected to be dominant; 1: The corresponding bit is expected to be recessive. Mask bit pattern Each bit of the register indicates whether the corresponding identifier register bit must be consistent with the corresponding bit of the expected identifier. 0: Don't care, this bit is not used for comparison; 1: Must match, and the incoming identifier bit must be consistent with the identifier register bit corresponding to the filter.

***Notes**: According to the different settings of filter bit width and mode, the functions of the two registers in the filter bank are different. For the mapping of filters, function description and association of mask registers, see 21.4.5 Section: identifier filtering.*

Mask/identifier register in mask mode has the same definition as register bit in identifier list mode.

See for the address of the filter bank register Table 21-4.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

22 Serial Peripheral Interface (SPI)

22.1 Introduction

SPI can operate in master mode or slave mode, supporting full-duplex and simplex high-speed communication modes, and has hardware CRC calculation capability and can be configured in multi-master mode.

22.2 Main Features

- Full-duplex and simplex synchronous mode.
- Support master mode, slave mode and multi-master mode.
- Supports 8-bit or 16-bit data frame format.
- Data bit sequence programmable.
- NSS management by hardware or software.
- Clock polarity and phase programmable.
- Transmitting and receiving support hardware CRC calculation and check.
- DMA capability for transmission and reception

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Email：info@nationstech.com
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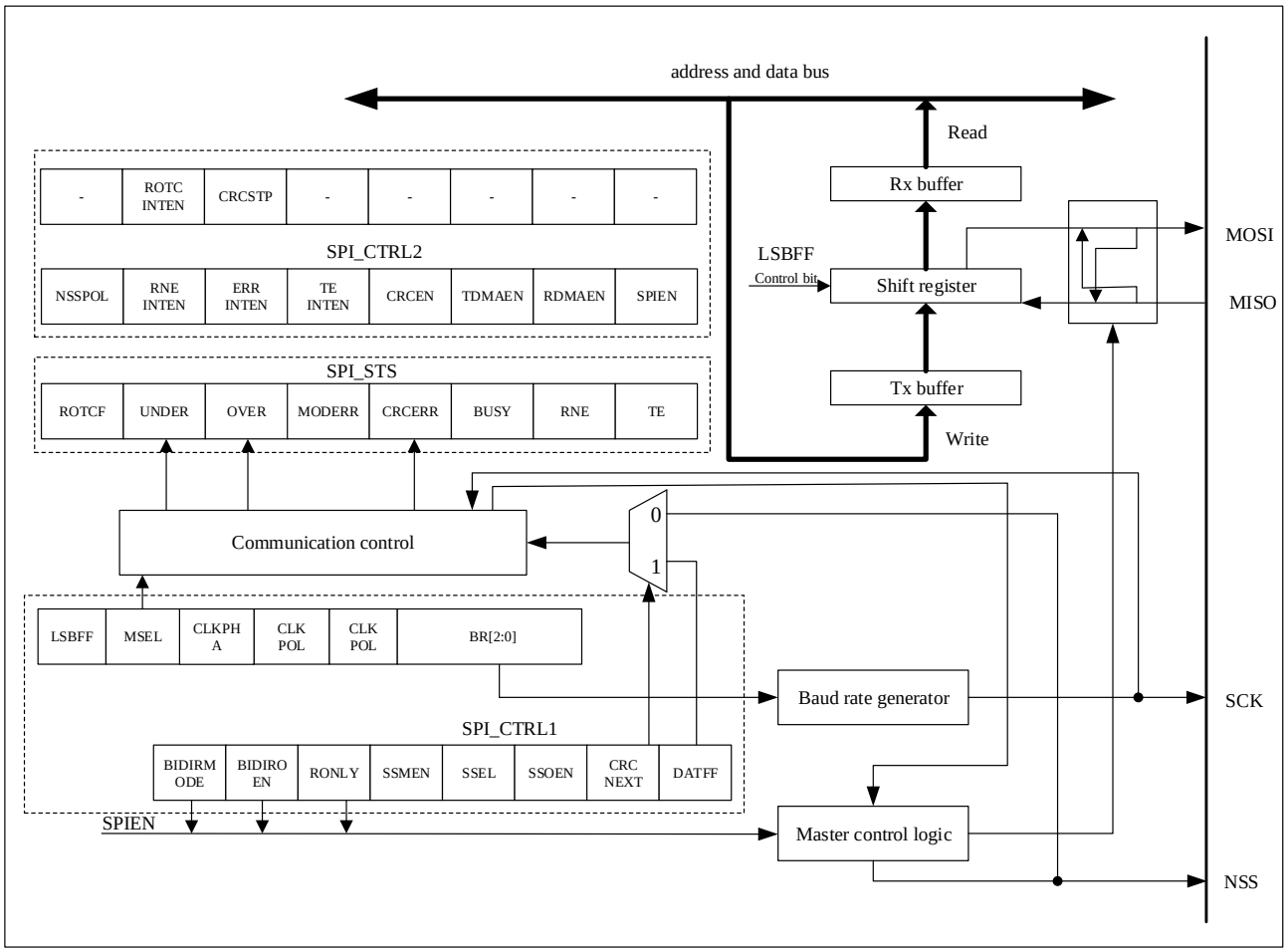
22.3 SPI Function Description

22.3.1 General Description

Figure 22-1 SPI Block Diagram



Usually, the SPI is connected to external devices through four pins:

- SCLK: serial clock pin. Serial clock signal is output from the SCLK pin of master device and input to SCLK pin of slave device.
- MISO: master input/slave output pin. Data is received from the MISO pin of master device and send by the MISO pin of slave device.
- MOSI: master output/slave input pin. Data is transmitted by the MOSI pin of master device and received from the MOSI pin of slave device.
- NSS: Slave select. There are two types of NSS pin, internal pin and external pin. If the internal pin detects a high level, SPI works in the master mode. Conversely, SPI works in the slave mode. Users can use a standard I/O pin of the master device to control the NSS pin of the slave device.

Software NSS mode

The software slave device management is enabled when SPI_CTRL1.SSMEN = 1.

The NSS pin remains free in software NSS mode. In this mode the internal NSS signal level is driven by writing the

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

SPI_CTRL1.SSEL bit (set SPI_CTRL1.SSEL=1 in master mode and set SPI_CTRL1.SSEL = 0 in slave mode).

Hardware NSS mode

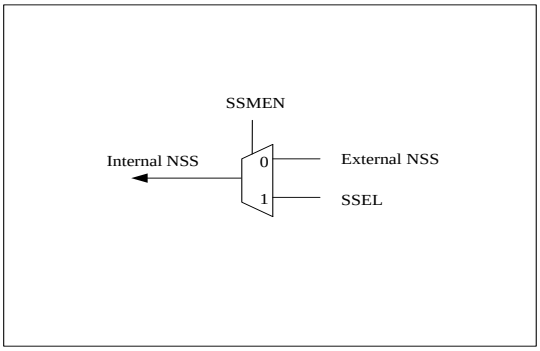
The software slave device management is disabled when SPI_CTRL1.SSMEN = 0.

NSS input mode: The NSS output of the master device is disabled (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 0), allowing operation in multi-master mode. The master should connect NSS pin to the high level and the slave should connect NSS pin to the low level during the entire data frame transfer.

NSS output mode: NSS output of the master device is enable (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 1). SPI as the master device must pull the NSS pin to low level, all device which connected to the master device and set to NSS hardware mode, will detect low level and enter the slave mode automatically. If the master device cannot pull the NSS pin to low level, device will enter the slave mode and generates the master mode fault error.

Note: The choice of software mode or hardware mode depends on whether NSS control is needed in the communication protocol. If not, you can choose the software mode, and release a GPIO pin for other purposes.

Figure 22-2 Selective Management of Hardware/Software



The following figure is an example of the interconnection of single master and single slave devices:

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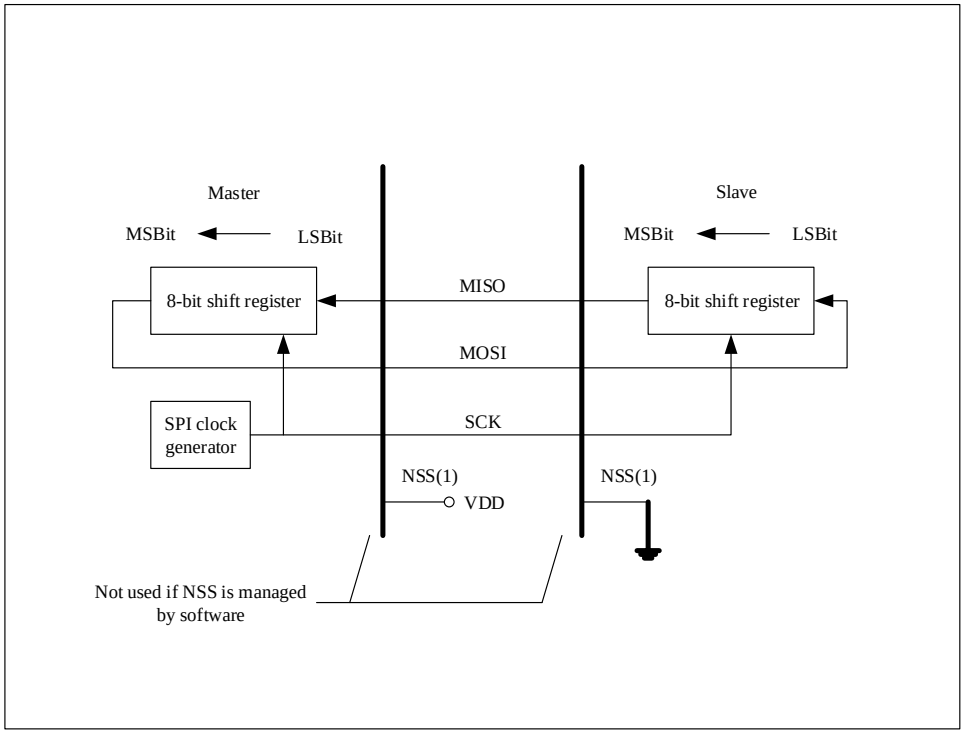
Figure 22-3 Master and Slave Applications



Note: (1)NSS pin is set as input

The master device outputs a synchronous clock signal through the SCLK pin, the MOSI pin of the master device is connected to the MOSI pin of the slave device, and the MISO pin of the master device is connected to the MISO pin of the slave device, so that data can be transferred between devices. Continuous data transfer between master and slave, sending data to slave through MOSI pin and slave sending data to master through MISO pin.

SPI timing mode

User can select the clock edge of data capture by setting SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit.

- When CLKPOL = 0, CLKPHA = 0, the SCLK pin will keep low in idle state, and the data will be sampled at the first edge, which is rising edge.
- When CLKPOL = 0, CLKPHA = 1, the SCLK pin will keep low in idle state, and the data will be sampled at the second edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 0, the SCLK pin will keep high in idle state, and the data will be sampled at the first edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 1, the SCLK pin will keep high in idle state, and the data will be sampled at the second edge, which is rising edge.

Regardless of the timing mode used, the master and slave configuration must be the same.

Figure 22-4 is the combination timing of four CLKPHA and CLKPOL bits transmitted by SPI when the SPI_CTRL1.LSBFF = 0.

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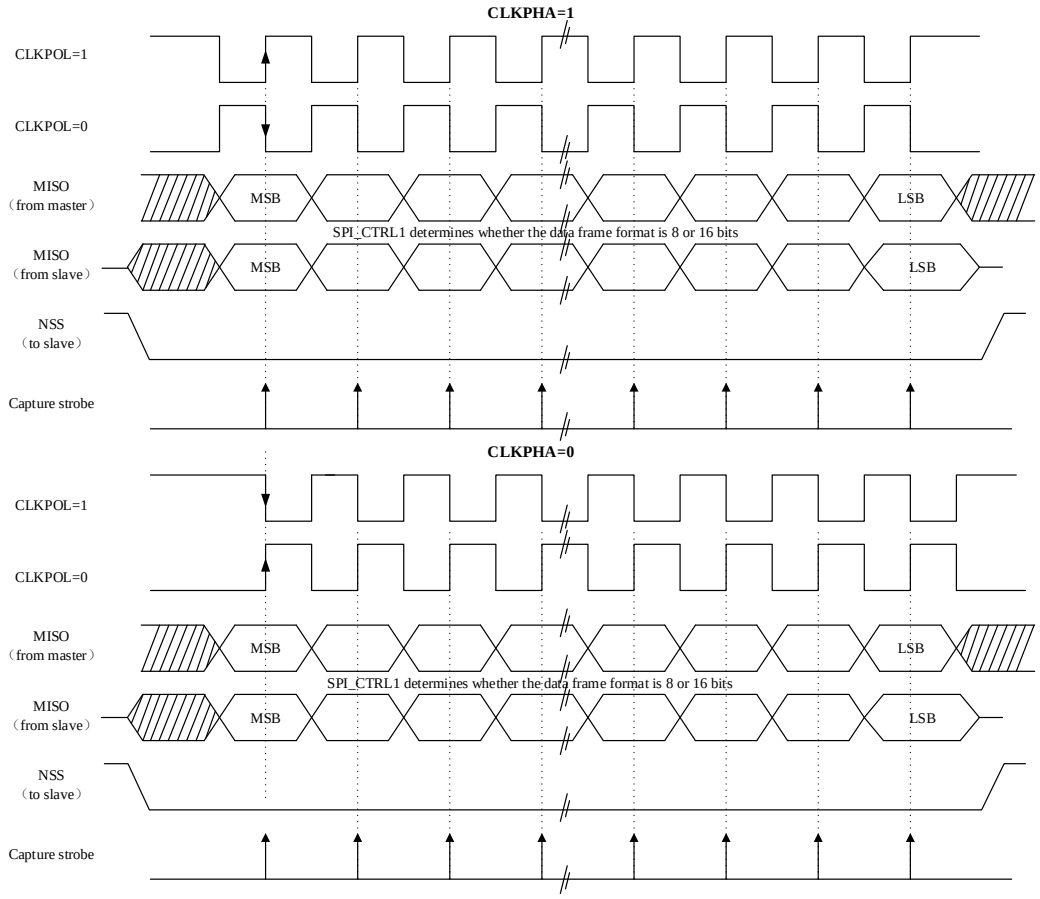
Figure 22-4 Data Clock Timing Diagram



Data format

User can selects the data order by setting the SPI_CTRL1.LSBFF bit. When SPI_CTRL1.LSBFF = 0, SPI will send the high-order data (MSB) first; When SPI_CTRL1.LSBFF = 1, SPI will send low-order data (LSB) first.

User can selects the data frame by setting the SPI_CTRL1.DATFF bit.

22.3.2 SPI Operating Mode

- **Master full duplex mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

After the first data is written to the SPI_DAT register, the transmission will start. When the first bit of the data is sent, the data bytes are loaded from the data register into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the data bits follow the MSB or LSB order are serially shifted to the MOSI pin. At the same time, the data receives on the MISO pin is serially shifted into the shift register in the same order and then loaded into the SPI_DAT register in parallel. The software operation process is as follows:

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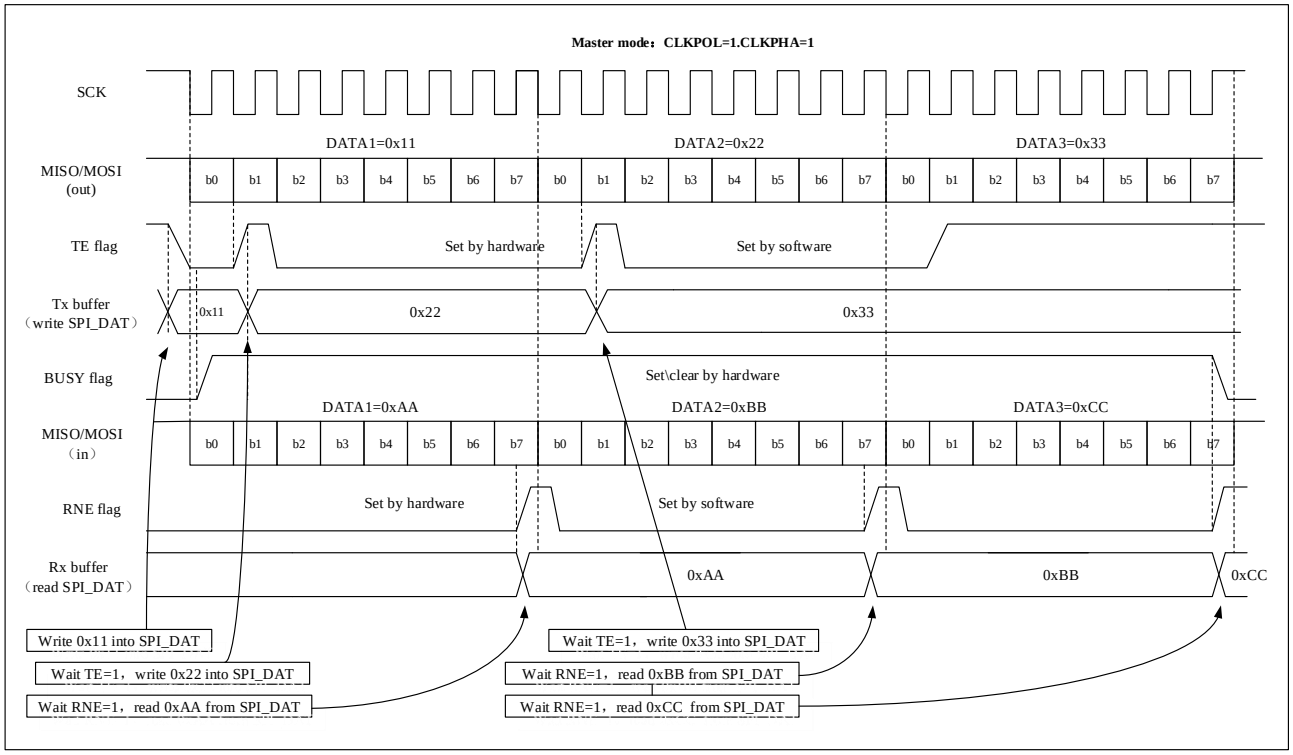
- Set SPI_CTRL2.SPIEN = 1, Enable SPI module.
- Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
- Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Wait for SPI_STS.RNE bit to be set to '1', read SPI_DAT to get the first received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT. Repeat the above operation, sending subsequent data and receiving n-1 data at the same time;
- Wait for SPI_STS.RNE bit to be set to '1' to receive the last data;
- Wait for SPI_STS.TE to be set to '1', then wait for SPI_STS.BUSY bit to be cleared and turn off SPI module.

The process of data transmitting and data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE or SPI_STS.TE flag.

Figure 22-5 TE/RNE/BUSY Behavior in Master / Full-Duplex Mode (BIDIRMODE = 0, RONLY = 0) in Case of Continuous Transfers



- **Master two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

Master two-wire unidirectional transmit-only mode is similar to master full-duplex mode. The difference is that this mode will not read the received data, so the SPI_STS.OVER bit will be set to '1', and the software will ignore it. The software operation process is as follows:

- Set SPI_CTRL2.SPIEN = 1 to enable SPI module.
- Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
- Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Repeat this operation to send subsequent data;

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Email：info@nationstech.com
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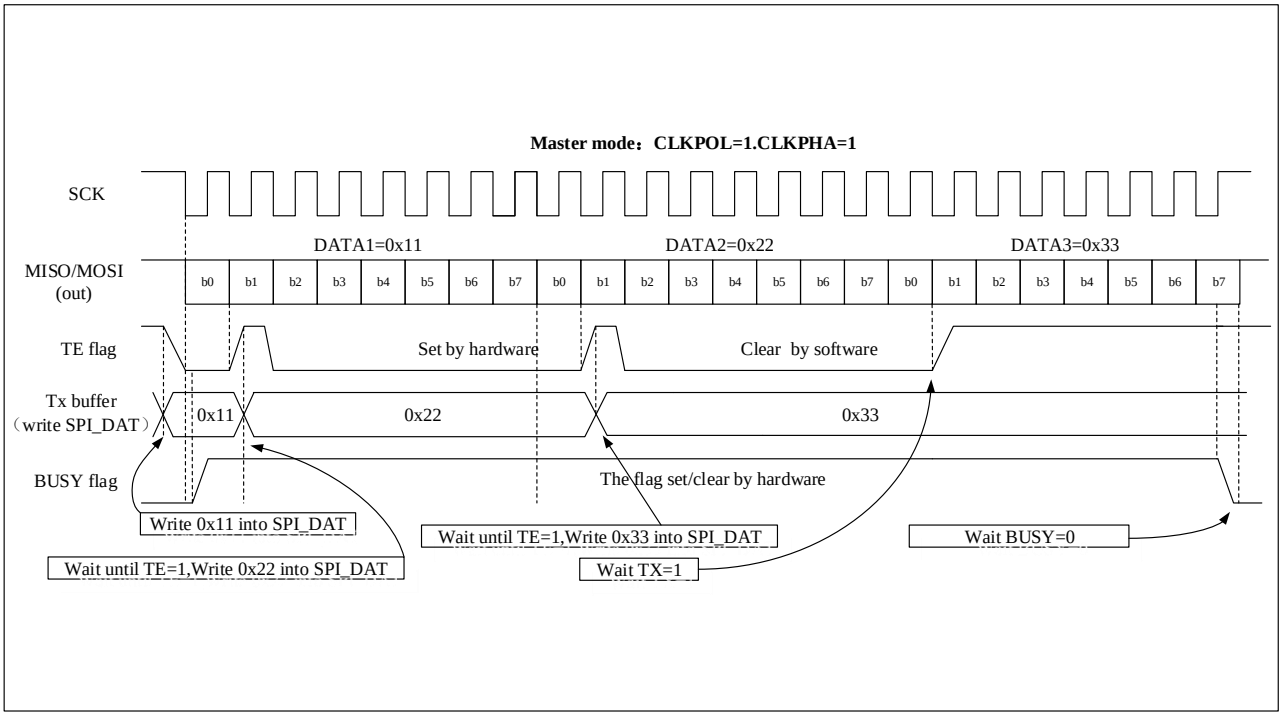
- After writing the last data to SPI_DAT, wait for SPI_STS.TE bit to set '1'; then wait for SPI_STS.BUSY bit to be cleared to complete the transmission of all data.

This process can also be implemented in the interrupt handler triggered by the rising edge of the SPI_STS.TE flag.

Figure 22-6 TXE/BSY Behavior in Master Transmit-Only Mode (BIDIRMODE = 0, RONLY = 0) in Case of Continuous Transfers



- **Master two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 1)**

When SPI_CTRL2.SPIEN = 1, the receiving process starts. The data bits from the MISO pin are sequentially shifted into the shift register and then loaded into the SPI_DAT register(receive buffer) in parallel. The software operation process is as follows:

- Set SPI_CTRL1.RONLY = 1 to enable the receive-only mode.
- In master mode, setting the SPI_CTRL2.SPIEN bit to 1 enables the SPI module, and the SCLK signal is generated immediately. Data is continuously received until the SPI is disabled (SPI_CTRL2.SPIEN = 0). In slave mode, when the master device drives the NSS signal low and generates SCLK, data is continuously received.
- Wait for SPI_STS.RNE bit to be set to '1', read the SPI_DAT register to get the received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT register. Repeat this operation to receive all data.

The process of data receiving can also be implemented in the interrupt handler generated by the rising edge of the RNE flag (SPI_STS.RNE).

Figure 22-7 RNE Behavior in Receive-Only Mode in Case of Continuous Transfers (BIDIRMODE = 0, RONLY =

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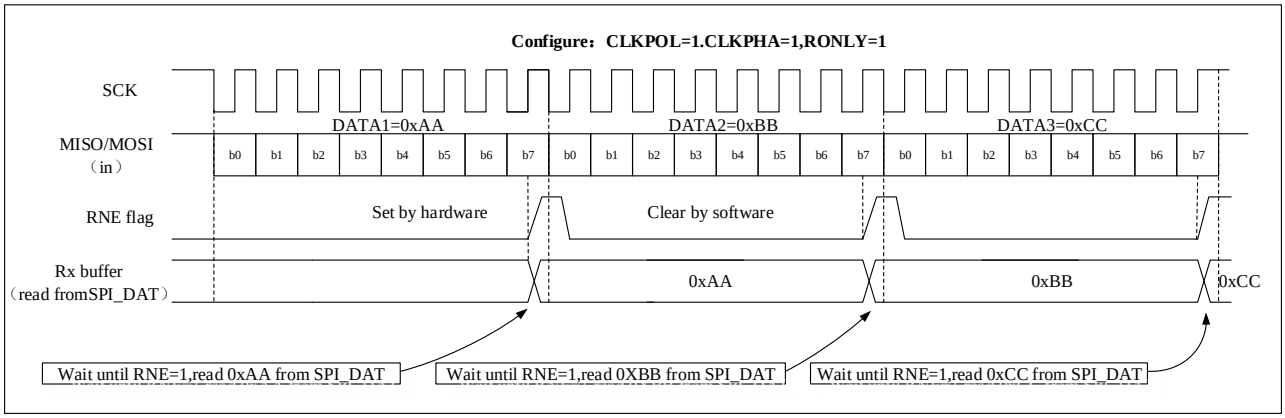
1)



- **Master one-wire bidirectional transmit mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 1, SPI_CTRL1.RONLY = 0)**

After the data is written to the SPI_DAT register (send buffer), the transmission process starts. This mode does not receive data. At the same time as the first data bit is sent, the data to be sent is loaded into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the SPI serially shifts the data bits to the MOSI pin in MSB or LSB order.

The software operation flow of the master one-wire bidirectional transmit mode is the same as that of the transmit-only mode.

- **Master one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 0, SPI_CTRL1.RONLY = 0)**

When SPI_CTRL1.SPIEN = 1 , the receiving process starts. There is no data output in this mode, the received data bits are sequentially and serially shifted into the shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel

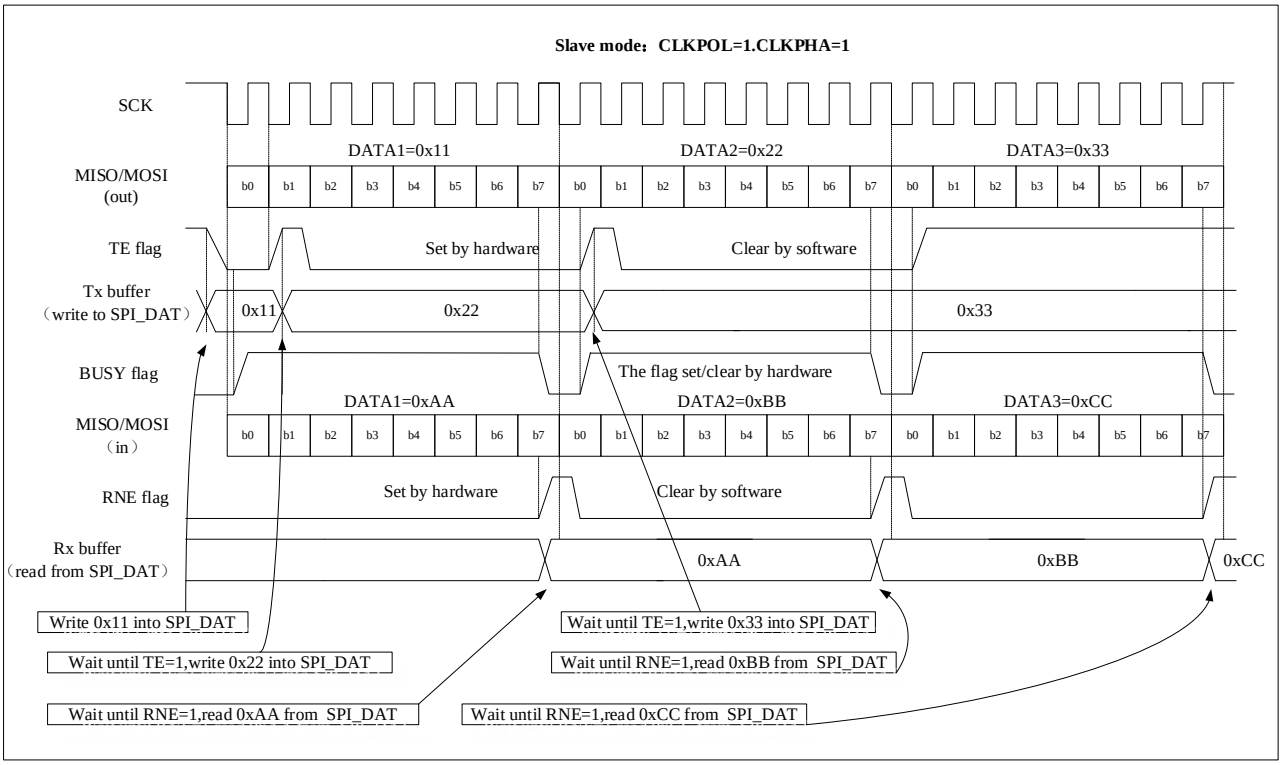
The software operation flow of the master one-wire bidirectional receive mode is the same as that of the receive-only mode.

- **Slave full duplex mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

The data transfer process begins when the slave device receives the first clock edge. Before the master device initiates data transmission, the software must ensure that the data to be sent is written to the SPI_DAT register.

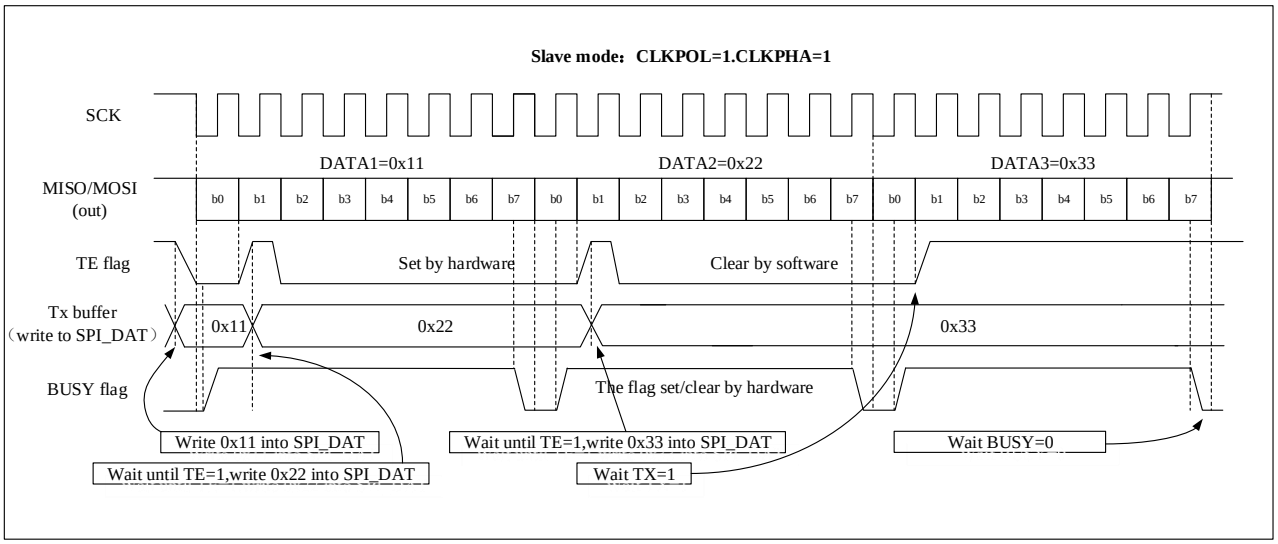
Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Figure 22-8 TE/RNE/BUSY Behavior in Slave / Full-Duplex Mode in Case of Continuous Transfers



- **Slave two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 0)**

Figure 22-9 TE/BUSY Behavior in Slave Transmit-Only Mode in Case of Continuous Transfers



- **Slave two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 1)**

The data receiving process begins when the slave device receives the clock signal and the first data bit from the MOSI pin. The received data bits are sequentially and consecutively shifted serially into an shift register and then loaded into the SPI_DAT register (receive buffer) in parallel.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- **Slave one-wire bidirectional transmit mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 1)**

When the slave device receives the first edge of the clock signal, the transmitting process starts. No data is received in this mode. Software must ensure that the data to be transmitted is written into the slave transmit register before the SPI master device starts data transfer.

- **Slave one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 0)**

Data receiving begins when the slave device receives the first clock edge and a data bit from the MOSI pin. There is no data output in this mode, the received data bits are sequentially and consecutively shifted serially into an shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel.

Note: The software operation process of the slave can refer to the master.

SPI initialization process

1) The baud rate of serial clock is defined by the SPI_CTRL1.BR[2:0] bits (this step is ignored if it is working in slave mode).
2) Select SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit to define the phase relationship between data transmission and serial clock.
3) Set SPI_CTRL1.DATFF bit to define 8-bit or 16-bit data frame format.
4) Configure the SPI_CTRL1.LSBFF bit to define the frame format.
5) Configure the NSS mode as described above for the NSS function.
6) Run mode is configured by SPI_CTRL1.MSEL bit, SPI_CTRL1.BIDIRMODE bit, SPI_CTRL1.BIDIROEN bit and SPI_CTRL1.RONLY bit.
7) Set the SPI_CTRL1.SPIEN = 1 to enable SPI.

Basic send and receive process

When SPI sends a data frame, it firstly loads the data frame from the data buffer into the shift register, and then starts to send the loaded data. When the data is transferred from the transmit buffer to the shift register, the transmit buffer empty flag is set (SPI_STS.TE = 1), and the next data can be loaded into the send buffer; if the TEINTEN bit is set (SPI_CTRL2.TEINTEN = 1), an interrupt will be generated; writing data to the SPI_DAT register will clear the SPI_STS.TE bit.

At the last edge of the sampling clock, when the data is transferred from the shift register to the receive buffer, the receive buffer non-empty flag is set (SPI_STS.RNE = 1), at this time the data is ready and can be read from the SPI_DAT register; if the receive buffer non-empty interrupt is enabled (SPI_CTRL2.RNEINTEN = 1), an interrupt will be generated; the SPI_STS.RNE bit can be cleared by reading the SPI_DAT register data.

In master mode, the transmitting process starts when data is written to the send buffer. If the next data has been written into the SPI_DAT register before the current data frame sending is completed, the continuous sending function

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

can be achieved.

In slave mode, the NSS pin is low, and when the first clock edge arrives, the transmission process begins. In order to avoid accidental data transmission, software must write data to the transmit buffer before data transmission (it is recommended to enable the SPI module before the master sends the clock).

In some configurations, when the last data is sent, the BUSY flag (SPI_STS.BUSY) can be used to wait for the end of the data sending.

Continuous and discontinuous transmission.

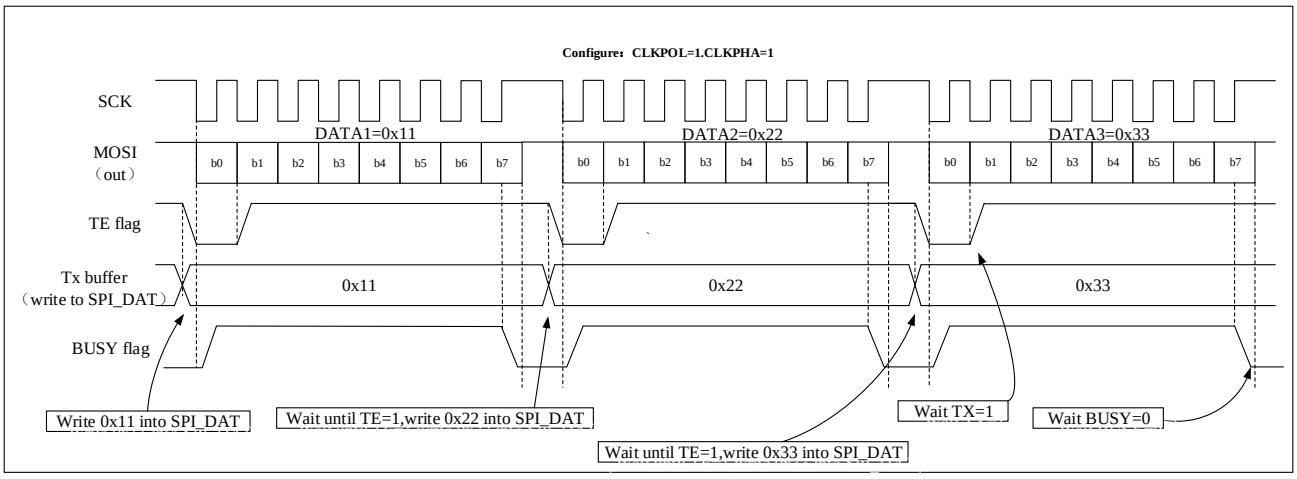
When sending data in master mode, if the software is fast enough to detect each TE (SPI_STS.TE) rising edge (or TE interrupt), and the data is written to the SPI_DAT register immediately before the end of the ongoing transmission. At this time, the SPI clock remains continuous between the transmission of data items, and the SPI_STS.BUSY bit will not be cleared, continuous communication can be achieved.

If the software is not fast enough, it will result in discontinuous communication; in this case, the SPI_STS.BUSY bit is cleared between the transmission of each data items (refer to Figure 22-10 below).

In master receive-only mode (SPI_CTRL1.RONLY = 1), communication is always continuous and the BUSY flag (SPI_STS.BUSY) is always high.

In slave mode, the continuity of communication is determined by the SPI master device. However, even if the communication is continuous, the BUSY flag (SPI_STS.BUSY) will be low for at least one SPI clock cycle between each data item (refer to Figure 22-9 below).

Figure 22-10 TE/BUSY Behavior in Non-Continuous Transmission (BIDIRMODE = 0 and RONLY = 0).



22.3.3 Status Flag

The SPI_STS register has 3 flag bits to monitor the status of the SPI:

Send buffer empty flag bit (TE)

When the send buffer is empty, the TE flag (SPI_STS.TE) is set to 1, which means that new data can be written into the SPI_DAT register. When the send buffer is not empty, the hardware will clear this flag to 0.

Receive buffer non-empty flag bit (RNE)

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

When the receive buffer is not empty, the RNE flag (SPI_STS.RNE) is set to 1, so the user knows that there is data in the receive buffer. After reading the SPI_DAT register, the hardware will set this flag to 0.

BUSY flag bit (BUSY)

When the transmission starts, the hardware sets the BUSY flag (SPI_STS.BUSY) to 1, and after the transmission ends, the hardware sets the BUSY flag to 0.

Only when the device is in the master one-wire bidirectional receive mode, the BUSY flag (SPI_STS.BUSY) will be set to 0 when the communication is in progress.

The BUSY flag (SPI_STS.BUSY) will be cleared to 0 in the following cases:

- End of transmission (except for continuous communication in master mode);
- Disable the SPI module (SPI_CTRL2.SPIEN = 0);
- The master mode error occurs (SPI_STS.MODERR = 1)

When the communication is discontinuous: the BUSY flag (SPI_STS.BUSY) is cleared to '0' between the transmission of each data item.

When communication is continuous: in master mode, the BUSY flag (SPI_STS.BUSY) remains high during the entire transfer process; In slave mode, the BUSY flag (SPI_STS.BUSY) will be low for 1 SPI clock cycle between each data item transfer. So do not use the BUSY flag to handle the sending and receiving of each data item.

22.3.4 Disabling SPI

To disable the SPI module, different operation modes require different operation steps

Master or slave full duplex mode(SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=0)

1) Wait for the RNE flag (SPI_STS.RNE) to be set to 1 and the last byte to be received;
2) Wait for the TE flag (SPI_STS.TE) to be set to 1;
3) Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
4) Turn off the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire unidirectional transmit-only mode(SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=0) or one-wire bidirectional transmit mode(SPI_CTRL1.BIDIMODE=1, SPI_CTRL1.BIDIROEN=1) for master or slave

1) After writing the last byte to the SPI_DAT register, wait for the TE flag (SPI_STS.TE) to be set to 1;
2) Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
3) Disable the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire unidirectional receive-only mode (SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=1) or one-wire bidirectional receive mode(SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIMODE=1, SPI_CTRL1.BIDIROEN=0) for master

1) Wait for the penultimate RNE (SPI_STS.RNE) to be set to 1;
2) Before closing the SPI module (SPI_CTRL1.SPIEN = 0), wait for 1 SPI clock cycle (using software delay);

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

3) Wait for the last RNE (SPI_STS.RNE) to be set before entering shutdown mode (or disabling the SPI module clock).

Two-wire unidirectional receive-only mode(SPI_CTRL1.MSEL=0, SPI_CTRL1.BIDIMODE=0, SPI_CTRL1.RONLY=1) or one-wire bidirectional receive mode(SPI_CTRL1.MSEL=0, SPI_CTRL1.BIDIMODE=1, SPI_CTRL1.BIDIROEN=0) for slave

1) The SPI module can be disabled at any time (SPI_CTRL2.SPIEN = 0), and after the current transfer is over, the SPI module will be disabled;

2) If you want to enter the shutdown mode, you must wait for the BUSY flag (SPI_STS.BUSY) to be set to 0 before entering the shutdown mode (or disable the SPI module clock).

22.3.5 SPI Communication Using DMA

Users can choose DMA for SPI data transmission, application programs can be released, and system efficiency can be greatly improved.

When the send buffer DMA is enabled (SPI_CTRL2.TDMAEN = 1), each time the TE flag (SPI_STS.TE) bit is 1, a DMA request will be generated, and the DMA will automatically write the data to the SPI_DAT register, which will clear the TE flag (SPI_STS.TE) bit.

When the receive buffer DMA is enabled (SPI_CTRL2.RDMAEN = 1), each time the RNE flag (SPI_STS.RNE) bit is set to 1, a DMA request will be generated, and the DMA will automatically read the SPI_DAT register, which will clear the RNE flag (SPI_STS.RNE) bit.

When the SPI is only used for transmitting data, only the transmit DMA channel of the SPI needs to be enabled (SPI_CTRL2.TDMAEN = 1). At this time, since the received data has not been read, the OVER flag is set to '1' (software does not need to pay attention to this flag).

When the SPI is only used for receiving data, only the receive DMA channel of the SPI needs to be enabled (SPI_CTRL2.RDMAEN = 1).

In transmit mode, after DMA has sent all the data to be sent (DMA_INTSTS.TXCF = 1), BUSY flag (SPI_STS.BUSY) can monitor to confirm whether SPI communication is over, which can avoid destroying the transmission of the last data when the SPI is turned off or enters the shutdown mode. Therefore, the software needs to wait for the TE flag (SPI_STS.TE) bit to be set to 1, and wait for the BUSY flag (SPI_STS.BUSY) bit to be set to 0.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Figure 22-11 Transmission Using DMA

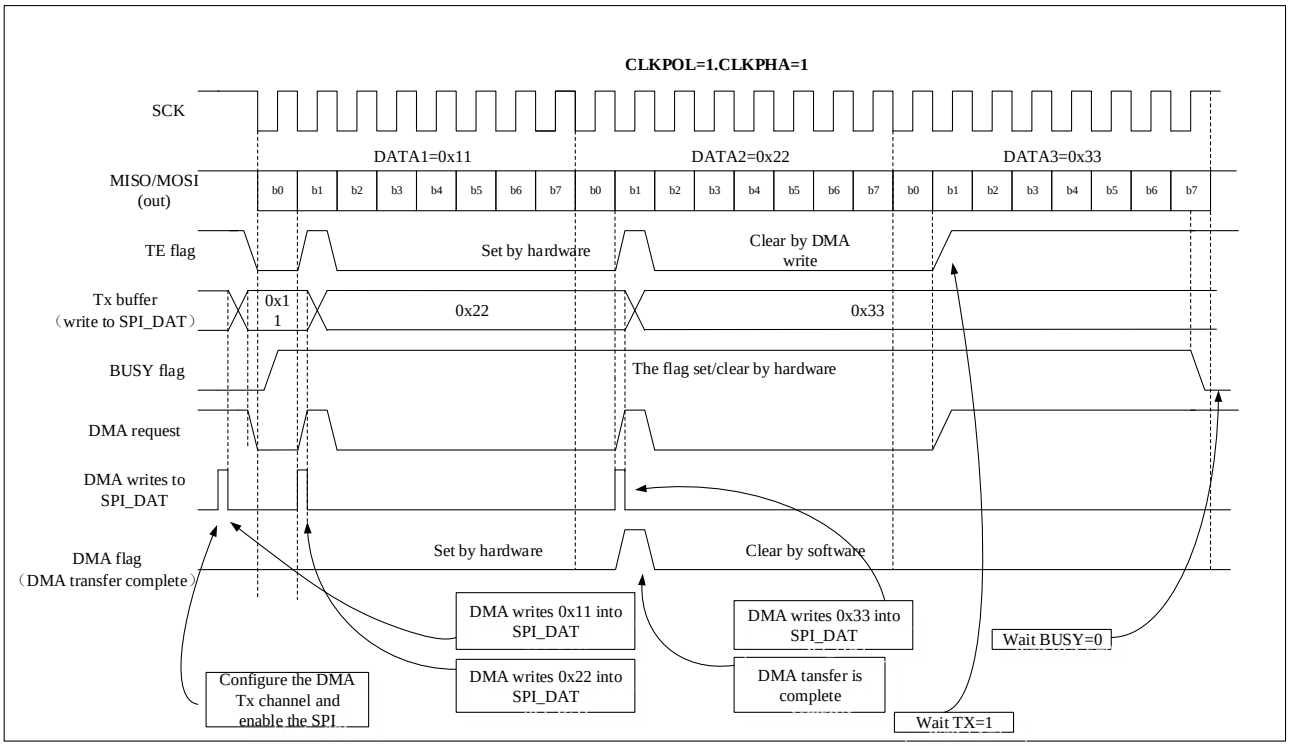
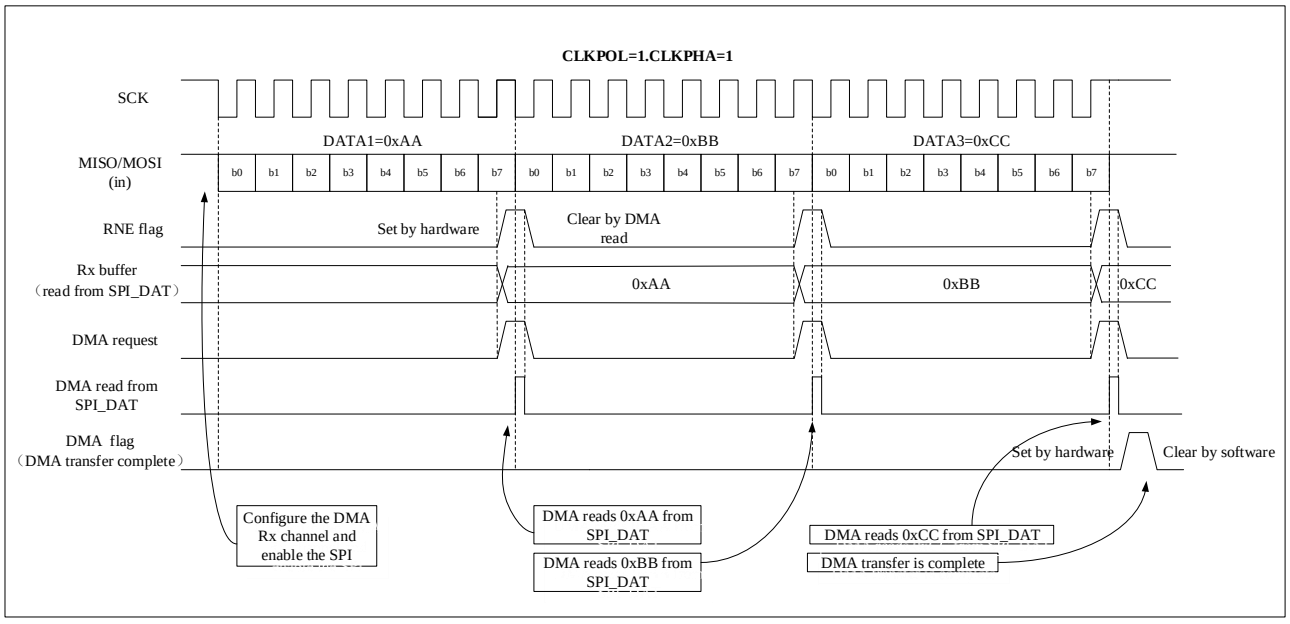


Figure 22-12 Reception Using DMA



22.3.6 CRC Calculation

SPI contains two independent CRC calculators for data transmission and reception to ensure the correctness of data transfer. Depending on the format of the transmitted and received data frames, different calculation methods are used for CRC, with CRC8 used for 8-bit data frames and CRC16 used for 16-bit data frames. The polynomial used for SPI CRC calculation is set by the SPI_CRCPOLY register, and users enable CRC calculation by setting the SPI_CTRL2.CRCEN bit.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

In transmit mode, after the final data is written to the transmit buffer, set the SPI_CTRL1.CRCNEXT bit to 1, which indicates that the hardware will start sending the CRC value (SPI_CRCTDAT value) after the data transmission is complete. During CRC transmission, the CRC calculation will stop.

In receive mode, after the second-to-last data frame is received, set the SPI_CTRL1.CRCNEXT bit to 1. Compare the received CRC with the SPI_CRCRDAT value, and if they are different, set the SPI_STS.CRCERR bit to 1. If SPI_CTRL2.ERRINTEN is set to 1, an interrupt will be generated.

To maintain synchronization of the next CRC calculation result between the master device and the slave device, the user should clear the CRC values of the master device and the slave device. Setting SPI_CTRL2.CRCEN to 1 will reset the SPI_CRCRDAT register and the SPI_CRCTDAT register. Follow the steps in the following sequence:

1. Set SPI_CTRL2.SPIEN = 0
2. Set SPI_CTRL2.CRCEN = 0
3. Set SPI_CTRL2.CRCEN = 1
4. Set SPI_CTRL2.SPIEN = 1.

Most importantly, when SPI is configured in slave mode with CRC enabled, the CRC calculation will still be performed as long as the SCLK pin has clock pulses, even if the NSS pin is high. This situation commonly occurs when the master device communicates alternately with multiple slave devices, so care must be taken to avoid CRC errors.

When hardware CRC checking is enabled (SPI_CTRL2.CRCEN = 1) and DMA is enabled, the hardware automatically completes the CRC byte transmission and reception at the end of communication.

22.3.7 Error Flag

Master mode fault (MODERR)

The following two conditions will cause the master mode fault:

- In NSS pin hardware management mode, the master device NSS pin is pulled low;
- In NSS pin software management mode, the SPI_CTRL1.SSEL bit is set to 0.
- When a master mode fault error occurs, the SPI_STS.MODERR bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1). The SPI_CTRL2.SPIEN bit and SPI_CTRL1.MSEL bit will be write protected and both are cleared by hardware. SPI is disabled and forced into slave mode.
- Performing a read or write operation on the SPI_STS register in software, followed by writing to the SPI_CTRL1 register, can clear the SPI_STS.MODERR bit (in multi-master configuration, the master's NSS pin must be pulled high first).
- Normally, the SPI_STS.MODERR bit of the slave cannot be set to 1. However, in a multi-master configuration, the slave's SPI_STS.MODERR bit may be set to 1. In this case, the SPI_STS.MODERR bit indicates that there is a multi-master collision. The interrupt routine can perform a reset or return to the default state to recover from an error state.

Overflow Error (OVER)

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

When the SPI_STS.RNE bit is set to 1, but there is still data sent into the receive buffer, an overflow error will occur. At this point, the overflow flag SPI_STS.OVER is set to 1. If the user enables the corresponding interrupt, an interrupt will be generated. All received data is lost, and the SPI_DAT register retains only the data that was previously unread.

Reading the SPI_DAT register and then the SPI_STS register in sequence can clear the SPI_STS.OVER bit.

CRC Error (CRCERR)

The CRC error flag is used to check the validity of the received data. A CRC error occurs when the received CRC value does not match the SPI_CRCRDAT value. At this time, the SPI_STS.CRCERR flag bit is set to '1', and an interrupt will be generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1).

22.3.8 SPI Interrupt

Table 22-1 SPI Interrupt Request

Interrupt Event	Event Flag	Enable Control Bit
Transmit buffer empty flag	TE	TEINTEN
Receive buffer not empty flag	RNE	RNEINTEN
Master mode fault event	MODERR	ERRINTEN
Overflow error	OVER	
CRC error	CRCERR	

22.4 SPI Registers

22.4.1 SPI Register Overview

Table 22-2 SPI Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	SPI_CTRL1	Reserved																BIDIROEN	BIDIRMODE	RONLY	SSMEN	SSEL	SSOEN	CRCNEXT	DATFF	LSBFF	MSEL	CLKPHA	CLKPOL	Reserved	BR[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
004h	SPI_CTRL2	Reserved																	ROTCINTEN	CRCSTP	Reserved					NSSPOL	ERRINTEN	RNEINTEN	TEINTEN	CRCEN	TDMAEN	RDMAEN	SPIEN
	Reset Value																		0	0						0	0	0	0	0	0	0	0
008h	SPI_STS	Reserved																			ROTCF	Reserved						OVER	MODERR	CRCERR	BUSY	RNE	TE
	Reset Value																				0							0	0	0	0	1	0
00Ch	SPI_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	SPI_CRCTDAT	Reserved																CRCTDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	SPI_CRCRDAT	Reserved																CRCRDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	SPI_CRCPOLY	Reserved																CRCPOLY[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
038h	SPI_CTRL3	Reserved																												DELAYTIME[3:0]			
	Reset Value																													0	0	0	0

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

22.4.2 SPI Control Register 1 (SPI_CTRL1)

Address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDIR MODE	BIDIR OEN	RONLY	SSMEN	SSEL	SSOEN	CRC NEXT	DATFF	LSBFF	MSEL	CLKPHA	CLKPOL	Reserved	BR[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	BIDIRMODE	Bidirectional data mode enable 0: Select the "two-wire one-way" mode. 1: Select the "one-wire bidirectional " mode.
14	BIDIROEN	Output enable in bidirectional mode Together with SPI_CTRL1.BIDIRMODE, this bit determines the transmission direction in single-line bidirectional mode. 0: Output disable (receive-only mode). 1: Output enabled (send-only mode). In master mode, the "one-wire" data line is the MOSI pin, and in slave mode, the "one-wire" data line is the MISO pin.
13	RONLY	Only receive mode This bit, together with the SPI_CTRL1.BIDIRMODE bit, determines the transfer direction in two-wire one-way mode. In the application scenario of multiple slave devices, this bit is only set to 1 by the unaccessed slave device, and only the accessed slave device can output, so as to avoid data line conflicts. 0: Full duplex (sending mode and receiving mode). 1: Disable output (receive-only mode).
12	SSMEN	Software slave device management When the SPI_CTRL1.SSMEN bit is set to 1, the NSS pin level is determined by the value of the SPI_CTRL1.SSEL bit. 0: Disable software slave device management. 1: Enable software slave device management.
11	SSEL	Internal slave device selection This bit only has meaning when the SPI_CTRL1.SSMEN bit is set. It determines the NSS level, and I/O operations on the NSS pin have no effect.
10	SSOEN	NSS output enable 0: Disable NSS output in master mode, the device can work in multi-master mode. 1: When the device is enabled, enable NSS output in the master mode, the device cannot work

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		in the multi-master device mode.
9	CRCNEXT	Send CRC next 0: The next sent value comes from the send buffer. 1: The next send value comes from the CRC register. *Note: This bit should be set immediately after the last data is written in SPI_DAT register during transmission. This bit should be set immediately after receiving the second-to-last data during reception.*
8	DATFF	Data frame format 0: 8-bit data frame format is used for sending/receiving. 1: 16-bit data frame format is used for sending/receiving. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.*
7	LSBFF	Frame format 0: Send MSB first. 1: Send LSB first. *Note: This bit cannot be changed during communication.*
6	MSEL	Master device selection 0: Configure as the slave device. 1: Configure as the master device. *Note: This bit cannot be changed during communication.*
5	CLKPHA	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.*
4	CLKPOL	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.*
3	Reserved	Reserved, the reset value must be maintained.
2:0	BR[2:0]	Baud rate control 000: $f_{PCLK}/2$ 001: $f_{PCLK}/4$ 010: $f_{PCLK}/8$ 011: $f_{PCLK}/16$ 100: $f_{PCLK}/32$ 101: $f_{PCLK}/64$ 110: $f_{PCLK}/128$ 111: $f_{PCLK}/256$ *Note: This bit cannot be changed during communication.*

22.4.3 SPI Control Register 2 (SPI_CTRL2)

Address: 0x04

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ROTC INTEN	CRCSTP	Reserved					NSSPOL	ERR INTEN	RNE INTEN	TE INTEN	CRCEN	TDMAEN	RDMAEN	SPIEN
	rw	rw						rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	ROTCINTEN	In receive-only mode, enable the transfer complete interrupt. 0: Disable the transfer complete interrupt. 1: Enable the transfer complete interrupt.
13	CRCSTP	When NSS becomes invalid, whether the CRC stop calculating immediately. 0: CRC stop calculating immediately when NSS becomes invalid. 1: As long as there is a clock, the CRC calculation continues.
12:8	Reserved	Reserved, the reset value must be maintained.
7	NSSPOL	NSS polarity control 0: NSS valid level is low. 1: NSS valid level is high.
6	ERRINTEN	Error interrupt enable When an error (SPI_STS.CRCERR, SPI_STS.OVER, SPI_STS.UNDER, SPI_STS.MODERR) is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
5	RNEINTEN	Receive buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when RNE flag (SPI_STS.RNE) is set to ‘1’.
4	TEINTEN	Transmit buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when TE flag (SPI_STS.TE) is set to '1'.
3	CRCEN	Hardware CRC check enable 0: Disable CRC calculation. 1: Enable CRC calculation. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* This bit can only be used in full duplex mode.
2	TDMAEN	Transmit buffer DMA enable When this bit is set, a DMA request is issued as soon as the TE flag (SPI_STS.TE) is set

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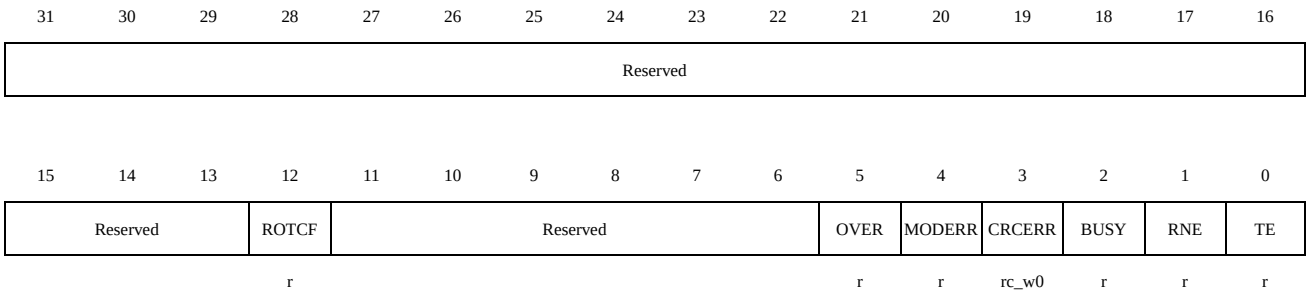
Bit Field	Name	Description
		0: Disable transmit buffer DMA. 1: Enable transmit buffer DMA.
1	RDMAEN	Receive buffer DMA enable When this bit is set, a DMA request is issued as soon as the RNE flag (SPI_STS.RNE) is set 0: Disable receive buffer DMA. 1: Enable receive buffer DMA.
0	SPIEN	SPI enable 0: Disable SPI device. 1: Enable the SPI device. *Note: When turning off the SPI device, please follow paragraph 22.3.4 Section's procedure operation.*

22.4.4 SPI Status Register (SPI_STS)

Address: 0x08

Reset value: 0x0000 0101



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ROTCF	In receive-only mode, the transfer completion status. 0: The current transfer is not yet completed. 1: The current transfer has been completed.
11:6	Reserved	Reserved, the reset value must be maintained.
5	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. This bit is set by hardware, and reading the data register first and then reading the status register will clear it. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For detailed information on software sequences, refer to section 22.3.7.*
4	MODERR	Mode error 0: No mode error. 1: A mode error occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For detailed information on software sequences, refer to section 22.3.7.*

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
3	CRCERR	CRC error flag 0: The received CRC value matches the value the SPI_CRCRDAT register value. 1: The received CRC value does not match the SPI_CRCRDAT register value. *Note: this bit is set by hardware and cleared by software by writing 0.*
2	BUSY	Busy flag 0: SPI is not busy. 1: SPI is busy communicating or the send buffer is not empty. This bit is set or reset by hardware. *Note: Special care should be taken when using this flag, as described in sections 22.3.3 and 22.3.4.*
1	RNE	Receive buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.
0	TE	The send buffer is empty 0: The send buffer is not empty. 1: The send buffer is empty.

22.4.5 SPI Data Register (SPI_DAT)

Address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
rw															

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	DAT[15:0]	Data register Data to be sent or received. The data register corresponds to two buffers: one for write (transmit buffer); The other is for read (receive buffer).Write operation writes data to transmit buffer; The read operation will return the data in the receive buffer. Note on SPI mode: According to the selection of the data frame format by the SPI_CTRL1.DATFF bit, the data transmitting and receiving can be 8-bit or 16-bit. To ensure correct operation, the data frame format needs to be determined before enabling the SPI. For 8-bit data, the buffer is 8-bit, and only SPI_DAT[7:0] is used when transmitting and receiving. When receiving, SPI_DAT[15:8] is forced to 0. For 16-bit data, the buffer is 16-bit, and the entire data register is used when transmitting and receiving, that is, SPI_DAT[15:0].

22.4.6 SPI Transmit CRC Register（SPI_ CRCTDAT）

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCTDAT[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRCTDAT	Transmit CRC register When CRC calculation is enabled, CRCTDAT[15:0] contains the CRC value calculated by the bytes sent subsequently. This register is reset when ‘1’ is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.*

22.4.7 SPI Receive CRC Register (SPI_CRCRDAT)

Address offset: 0x14

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCRDAT[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRCRDAT	Receive CRC register When CRC calculation is enabled, CRCRDAT[15:0] will contain the calculated CRC value of subsequent received bytes. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.*

22.4.8 SPI CRC Polynomial Register (SPI_CRCPOLY)

Address: 0x18

Reset value: 0x0000 0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCPOLY[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRCPOLY [15:0]	CRC polynomial register This register contains the polynomial used for the CRC calculation. The reset value is 0x0007, other values can be set according to the application.

22.4.9 SPI RX Sample Delay Register (SPI_CR3)

Address: 0x38

Reset value: 0x0000 0000

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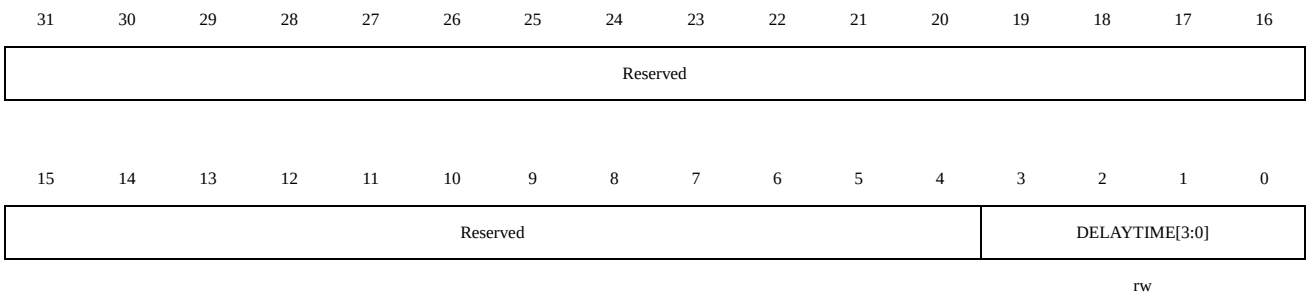

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	DELAYTIME [15:0]	Configuration of SPI master sampling delay time, after setting the value of this register, the received data will be sampled using the delayed clock. 4'b0000: Bypass, no delay processing for the sampling clock. 4'b0001: Sample the data on the MISO port after a delay of 1/2 PCLK2 cycle. 4'b0010: Sample the data on the MISO port after a delay of 1 PCLK2 cycle. 4'b0011: Sample the data on the MISO port after a delay of 3/2 PCLK2 cycle. 4'b0100: Sample the data on the MISO port after a delay of 2 PCLK2 cycle. 4'b0101: Sample the data on the MISO port after a delay of 5/2 PCLK2 cycle. 4'b0110: Sample the data on the MISO port after a delay of 3 PCLK2 cycle. 4'b0111: Sample the data on the MISO port after a delay of 7/2 PCLK2 cycle. 4'b1000: Sample the data on the MISO port after a delay of 4 PCLK2 cycle. 4'b1001: Sample the data on the MISO port after a delay of 9/2 PCLK2 cycle. 4'b1010: Sample the data on the MISO port after a delay of 5 PCLK2 cycle. 4'b1011: Sample the data on the MISO port after a delay of 11/2 PCLK2 cycle. 4'b1100: Sample the data on the MISO port after a delay of 6 PCLK2 cycle. 4'b1101: Sample the data on the MISO port after a delay of 13/2 PCLK2 cycle. 4'b1110: Sample the data on the MISO port after a delay of 7 PCLK2 cycle. 4'b1111: Sample the data on the MISO port after a delay of 15/2 PCLK2 cycle. Note: This register can only be configured in SPI master full-duplex and SPI master receive modes. Configuring this bit in other SPI modes is invalid.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

23 Real-time Clock (RTC)

23.1 Description

- The real-time clock (RTC) is an independent BCD timer/counter.
- Daylight saving time compensation supported by software.
- A periodic automatic programmable wakeup timer.
- Two 32-bit registers contain the seconds, minutes, hours, day (day of week), date (day of month), month, and year.
- Independent 32-bit register contain sub-seconds value.
- Two programmable alarms.
- Two 32-bit registers contain two programmable alarms seconds, minutes, hours, day (day of week), and date (day of month).
- Two 32-bit registers contain two programmable alarms sub-seconds.
- Digital calibration function.
- Reference clock detection: A more accurate external clock source (50 or 60Hz) can be used to improve calendar accuracy.
- Three configurable filtering and internal pull-up tamper detection events.
- Time-Stamp function.
- Multiple Wakeup sources of Interrupt/Event. These include Alarm A, Alarm B, Wakeup Timer, Time-Stamp, Tamper.
- After RTC is enabled by the RCC register and voltage remains in the operating range, RTC will not stop timing in any mode (include RUN mode, SLEEP mode, STOP mode).
- RTC provides a variety of ways to wakeup from all low-power modes (SLEEP mode, STOP mode).

23.1.1 Main features

Table 23-1 RTC Feature Support

Main Function	Description
Clock	RTC clock can be selected from LSI, HIS/128 and HSE/128 respectively
Reset	The APB interface is reset by the system. Some registers synchronized through APB in the RTC module will be reset. The following registers will be cleared when the system is reset. ● RTC_SUBS ● RTC_TSH ● RTC_DATA ● RTC_INITSTS(some bits) RTC core is reset by backup domain reset. Reset the RTC, and retain the contents of some registers in low-power mode, including: ● RTC_CTRL

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

Main Function	Description
	● RTC_PRE ● RTC_CALIB ● RTC_SCTRL ● RTC_TSSS, RTC_TST and RTC_TSD ● RTC_TMPCFG ● RTC_WKUPT ● RTC_ALRMASS/RTC_ALRMA ● RTC_ALRMBSS/RTC_ALRMB ● RTC_OPT
Calendar	Calendar consists of sub second, second, minute, hour (12 or 24 format), day (day of the week), date, month and year. These data are stored in the shadow register of APB module.
Wakeup Timer	Output “RTC_OUT” can be configured to send wakeup events to GPIO. At the same time, it also can be configured as an interrupt/event to wake up the system from SLEEP, STOP modes.
Alarm	‘RTC_OUT’ is configured to output to GPIO, and can also wake up the CPU or trigger PWR to wake up from SLEEP, STOP modes when a match occurs.
Tamper	The 3 tamper detection logic can wake up the system from SLEEP, STOP modes.
Timestamp	GPIO events can trigger the timestamp saving function. It is a source of wake-up from low-power mode. Additionally, tamper events can be a source of timestamp events.
Interrupts/Events	Alarm A/Alarm B interrupt/event Wakeup interrupt/event Timestamp interrupt/event Tamper interrupt/event

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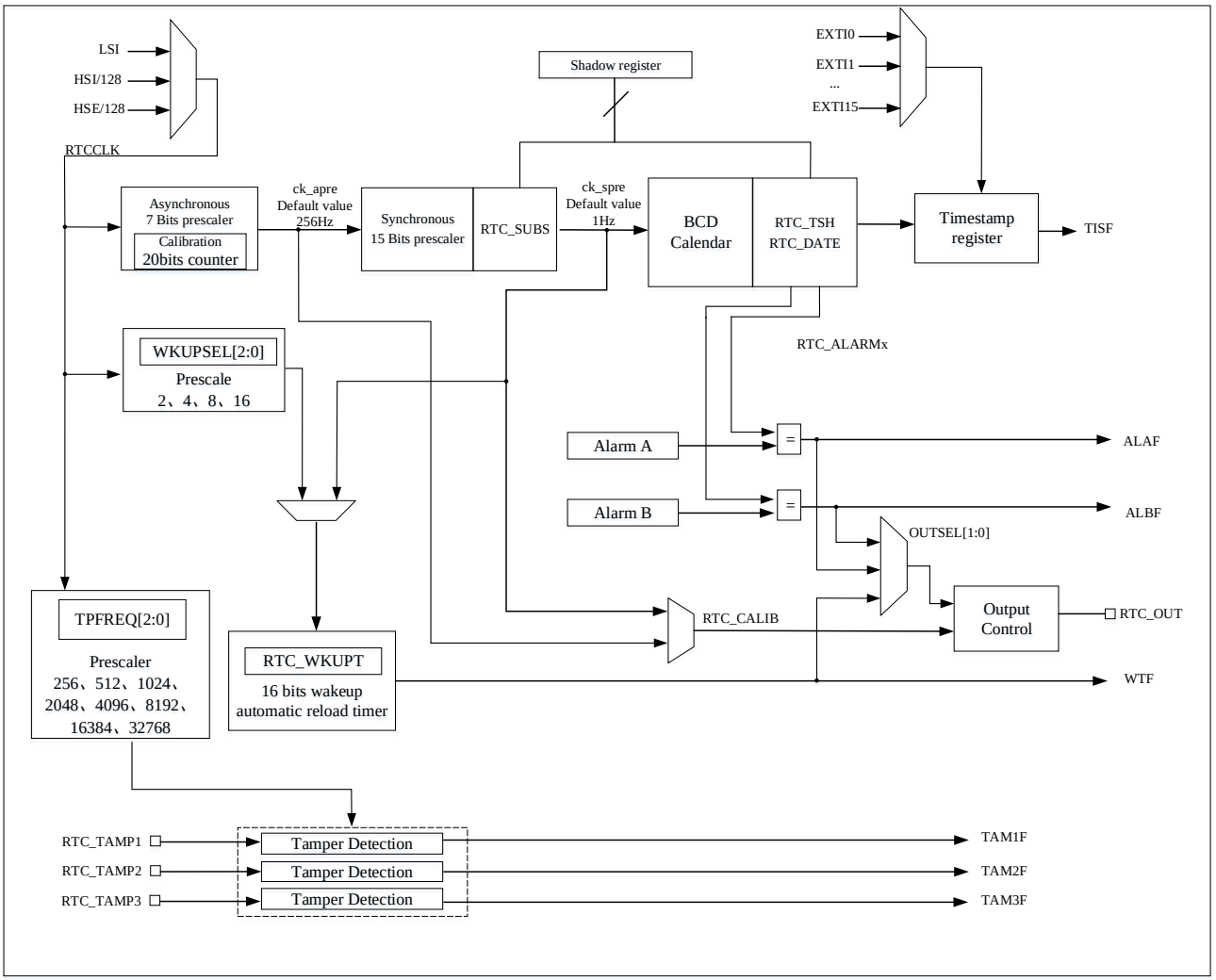
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

23.2 RTC Function Description

23.2.1 RTC Block Diagram

Figure 23-1 RTC Block Diagram



RTC includes the following functions:

- Alarm A and Alarm B event/interrupt
- Timestamp event/interrupt
- Tamper event/interrupt
- RTC output functions
  - 256 Hz or 1Hz clock output (LSI frequency is 32 kHz)
  - Alarm clock output (polarity configurable), Alarm A and Alarm B are optional.
  - Auto wakeup output (polarity configurable).
- RTC input functions:

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Email：info@nationstech.com
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- Timestamp event detection
- 50 or 60Hz reference clock input
- Tamper event detection

- Control PC13 by configuring output register:
  - Set RTC_OPT.TYPE bit to configure open-drain/push-pull output of PC13

23.2.2 GPIOs of RTC

Timestamp input come from IOM (mapped to PC13) or EXTI module, if EXTI module is needed to start, please refer to the timestamp trigger source selection register (EXTI_TS_SEL) for details.

RTC_OUT (Alarm, Wakeup event, Tamper event or calibration output (256Hz or 1Hz)) is mapped to PC13. Regardless of the configuration of PC13 GPIO pins, the pin configuration of PC13 is controlled by RTC as output.

The PC13 pin is used as the TAMPER1 tamper detection pin, the PA0 pin is used as the TAMPER2 tamper detection pin, and the PB8 pin is used as the TAMPER3 tamper detection pin.

PA1 or PB15 can be used as the RTC_REFCLKIN reference clock input pin.

23.2.3 RTC Register Write Protection

After power-up, all RTC write-protected registers will have write protection enabled. All RTC write-protected registers need to be unlocked by following the steps below:

- Write “0xCA” into RTC_WRP register.
- Write “0x53” into RTC_WRP register.

After unlocking these registers, the write protection cannot be re-enabled unless the RTC is reset by software or powered on again. The unlocking mechanism only checks the write operation to the RTC_WRP register. During the unlocking process, before unlocking, and after unlocking, writing to other registers will not affect the unlocking result.

After an RTC reset, all RTC registers are write-protected except for RTC_CTRL, RTC_WRP, RTC_TST, RTC_DATE, RTC_TSSS, RTC_TMPCFG, RTC_SUBS, RTC_OPT, and RTC_INITSTS[13:8].

23.2.4 RTC Clock and Prescaler

RTC clock source:

- LSI clock
- HSE/128 clock
- HSI/128 clock

To reduce power consumption, the prescaler is divided into an asynchronous prescaler and a synchronous prescaler. If both prescalers are used simultaneously, it is recommended to set the value of the asynchronous prescaler as large as possible.

- A 7-bit asynchronous prescaler which is given by RTC_PRE.DIVA[6:0] bits
- A 15-bit synchronous prescaler which is given by RTC_PRE.DIVS[14:0] bits

Note: The prescaler configuration must be implemented during calendar initialization.

The formula for f_{ck_apre} and f_{ck_spre} are given below:

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Email：info@nationstech.com
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$$f_{ck_apre} = \frac{f_{RTCCLK}}{RTC_PRE.DIVA[6:0]+1}$$

$$f_{ck_spre} = \frac{f_{RTCCLK}}{(RTC_PRE.DIVS[14:0]+1)*(RTC_PRE.DIVA[6:0]+1)}$$

The ck_apre clock is used to driven RTC_SUBS sub-second down counter. When it reaches 0, RTC_SUBS is reloaded with the value of RTC_PRE.DIVS[14:0].

23.2.5 RTC Calendar

There are three shadow registers, they are RTC_DATE, RTC_TSH and RTC_SUBS. The RTC time and date registers can be accessed through the shadow registers. It is also possible to access them directly to avoid the synchronization waiting time. The three shadow registers are as follow:

- RTC_DATE: set and read date
- RTC_TSH: set and read time
- RTC_SUBS: read sub-second

Every two RTCCLK cycles, the current calendar value is copied to the shadow registers, and the RTC_INITSTS.RSYF bit is set to 1. This process is not executed in low-power (stop) modes. When exiting these modes, the shadow registers update their values after 2 RTCCLK cycles.

By default, when user try to access the calendar register, it will access the contents of the shadow register instead. User can access the calendar register directly by setting the RTC_CTRL.BYPS bit.

When RTC_CTRL.BYPS=0, calendar values are from shadow registers, when reading RTC_SUBS, RTC_TSH or RTC_DATE register, it is necessary to make ensure the frequency of APB1 clock (f_{APB1}) is at least 7 times the frequency of RTC clock (f_{RTCCLK}), and APB1 clock frequency lower than RTC clock frequency is not allowed in any case. System reset will reset shadow registers.

23.2.6 Calendar Initialization and Configuration

The value of prescaler and calendar can be initialized by the following steps:

- Set the RTC_INITSTS.INITM bit to 1 to enter the initialization mode, and then wait for the RTC_INITSTS.INITF bit to be set 1.
- Set RTC_PRE.DIVS[14:0] and RTC_PRE.DIVA[6:0] value.
- Write the initial calendar values include time and date into the shadow registers (RTC_TSH and RTC_DATE) and configure the time format (12 or 24 hours) through the RTC_CTRL.HFMT bit.
- Exit initialization mode by clearing the RTC_INITSTS.INITM bit.

The values of calendar counter will automatically loaded from shadow registers after 4 RTCCLK clock cycles, then the calendar counter restarts.

Note: Before entering the initialization mode, ensure that the value of RTC_SUBS.SS[15:0] is not less than 2.

23.2.7 Calendar Reading

1. Reading calendar value when RTC_CTRL.BYPS=0

Calendar value is read from shadow registers if RTC_CTRL.BYPS=0. In order to read RTC calendar registers

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Email：info@nationstech.com
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(RTC_SUBS, RTC_TSH and RTC_DATE) correctly, APB1 clock frequency must be set greater than 7 times of RTC clock frequency. In any case, APB1 clock frequency must not be less than RTC clock frequency.

If APB1 clock frequency is not equal to or greater than 7 times of RTC clock frequency, refer to the following process to read calendar value.

- Read the data of RTC_SUBS, RTC_TSH and RTC_DATE twice.
- Compare the data read on two occasions, if they are equal, the read data can be considered correct; if they are not equal, read the data for the third time.
- The third time read data can be considered correctly.

Shadow registers (RTC_SUBS, RTC_TSH and RTC_DATE) are updated every two RTCCLK cycles. If user want to read calendar value in a short time(less than two RTCCLK cycles), RTC_INITSTS.RSYF bit must be cleared by software after the first time read.

In some cases, it is necessary to wait until RTC_INITSTS.RSYF bit is set to 1 before read calendar value.

- After waking up from the low power modes (STOP mode), clear RTC_INITSTS.RSYF bit, then wait for the RTC_INITSTS.RSYF bit to be set to 1 again..
- System reset.
- Calendar complete initialization.
- Calendar complete synchronization.

2. Reading calendar value when RTC_CTRL.BYPS=1

If RTC_CTRL.BYPS=1, read the calendar value directly from the calendar counter. The advantage of this configuration is that there is no delay in reading the calendar value after waking up from low-power mode. The disadvantage is that the data from RTC_SUBS, RTC_TSH, and RTC_DATE may not be from the same moment.

To ensure the correctness of read calendar value, it is necessary to read RTC_SUBS, RTC_TSH and RTC_DATE twice, the data read on two occasions should then be compared, and if they are equal, the read data is considered correct.

23.2.8 Calibration Clock Output

When RTC_CTRL.COEN is set to 1, the PC13 pins will output the calibration clock. If RTC_CTRL.CALOSEL=0 and RTC_PRE.DIVA[6:0]=0x7C, the frequency of RTC_CALIB is fRTCCLK / RTC_PRE.DIVA[6:0]. When the frequency of RTCCLK is 32 kHz, the calibration output is 256Hz. Due to slight jitter on the falling edge, it is recommended to use the rising edge.

When RTC_CTRL.CALOSEL=1 and "RTC_PRE.DIVS[14:0]+1" is a non-zero integer multiple of 256, the frequency of RTC_CALIB is given by the formula f_{RTCCLK}/(256 * (DIVA+1)). When the frequency of RTCCLK is 32 kHz and RTC_PRE.DIVA[6:0]=0x7C, the calibration output is 1Hz.

Note: When selecting RTC_CALIB or RTC_ALARM as the output, the RTC_OUT pin (PC13) is automatically configured as an output.

23.2.9 Programmable Alarm

RTC has 2 programmable alarms: Alarm A and Alarm B.

RTC alarm can be enabled or disabled by configuring RTC_CTRL.ALxEN bit. If the Alarm value matches the

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Email：info@nationstech.com
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Nanshan District, Shenzhen, 518057, P.R.China

calendar value, the RTC_INITSTS.ALxF flag is set to 1. If RTC_CTRL.ALxIEN is enabled, any calendar field can be selected to trigger the alarm interrupt.

Alarm Output: After configuring RTC_CTRL.OUTSEL[1:0], Alarm A or Alarm B can be mapped to the RTC_ALxRM output, and the output polarity can be configured by the RTC_CTRL.OPOL bit.

Note: When the second field is selected (RTC_ALARMx.MASK1 bit reset), RTC_PRE.DIVS[14:0] must be greater than 3 to ensure correct operation.

23.2.10 Alarm Configuration

Alarm A and Alarm B should be configured in the following below:

- Disable Alarm A/Alarm B by clearing RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit.
- Configure the Alarm x registers (RTC_ALRMxSS/RTC_ALARMx)
- Enable the Alarm A/Alarm B interrupt by setting the RTC_CTRL.ALAIEN/RTC_CTRL.ALBIEN bit to 1 (add this step as needed).
- Enable Alarm A/Alarm B by setting the RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit to 1.

23.2.11 Alarm Output

When RTC_CTRL.OUTSEL[1:0] != 0, the RTC_ALARM output function is enabled. Depending on the value of RTC_CTRL.OUTSEL[1:0], select Alarm A output, Alarm B output, or wakeup output.

The RTC_CTRL.OPOL bit controls the polarity of Alarm A, Alarm B, or wakeup output.

The RTC_OPT.TYPE bit controls the RTC_ALARM pin open-drain or push-pull output.

When selecting RTC_CALIB or RTC_ALARM output, the RTC_OUT pin (PC13) is automatically configured as an output.

23.2.12 Periodic Automatic Wakeup

A 16-bit programmable auto-reload counter can generate a periodic wakeup flag upon reaching 0. It can also extend the range of the wakeup timer to 17 bits. Enabling the periodic auto-wakeup function can be done by setting RTC_CTRL.WTEN.

There are two wake-up input clock sources can be selected:

- RTC clock (RTCCLK) divided by 2/ 4/8/16.

  Assuming RTCCLK is sourced from LSI (32kHz), the wakeup interrupt period can be configured from 125us to 32s, with resolution is 62.5us.

- Internal clock ck_spre.

  Assume ck_spre frequency is 1Hz, the available wake-up time range from 1s to 36h, and the resolution is 1 second.

  - When RTC_CTRL.WKUPSEL [2:0] = 10x, the period is range from 1s to 18h.
  - When RTC_CTRL.WKUPSEL [2:0] = 11x, the period is range from 18h to 36h.

When the RTC_CTRL.WTEN bit is set to 1, the countdown counter is running, and when it reaches 0, the RTC_INITSTS.WTF bit is set to 1. By setting the RTC_CTRL.WTIEN bit to 1, the device can exit low-power mode when the periodic wakeup interrupt is triggered and enabled.

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Periodic Wakeup Output: When RTC_CTRL.OUTSEL[1:0] selects the periodic wakeup, it can be mapped to the RTC_ALxRM output , and the RTC_OUT pin (PC13) is automatically configured as an output, and the output polarity can be configured by the RTC_CTRL.OPOL bit.

23.2.13 Wakeup Timer Configuration

The configuration of the automatic reload value for the wakeup timer is as follows:

- Disable the wakeup timer by clearing RTC_CTRL.WTEN, then wait for the RTC_INITSTS.WTWF flag to be set to 1.
- Select the wakeup timer clock by setting RTC_CTRL.WKUPSEL[2:0].
- Configure the wake-up automatic reload value by setting RTC_WKUPT.WKUPT[15:0] bits.
- Enable Wakeup interrupt by setting RTC_CTRL.WTIEN bit(this step can be selected as needed)
- Enable wakeup timer by setting RTC_CTRL.WTEN bit

23.2.14 Timestamp Function

Timestamp can be enabled by setting RTC_CTRL.TSEN bit to 1. When a timestamp event is detected on the RTC_TS pin, the calendar values of the event will be stored in the timestamp register (RTC_TSSS, RTC_TST, RTC_TSD), and RTC_INITSTS.TISF is set to 1. If RTC_CTRL.TSIEN is set to 1, a timestamp event can generate an interrupt. If a new timestamp event is detected while RTC_INITSTS.TISF is already set to 1, the hardware will set the RTC_INITSTS.TISOVF flag to 1. The timestamp registers (RTC_TST and RTC_TSD) will continue to hold the values of the previous event, meaning that the data in the timestamp registers (RTC_TST and RTC_TSD) will not change when RTC_INITSTS.TISF=1.

After the timestamp event caused by the synchronization process occurs again, RTC_INITSTS.TISF is set to 1 in 2 RTC_CLK cycles. There is no delay in the generation of RTC_INITSTS.TISOVF. This means that if two timestamp events are very close, this can cause RTC_INITSTS.TISOVF to be "1" and RTC_INITSTS.TISF to be "0". Therefore, after detecting RTC_INITSTS.TISF as "1", check the RTC_INITSTS.TISOVF bit. When RTC_TMPCFG.TPTS bit is set to 1, tamper events can trigger timestamp events.

If timestamp events are enabled, the timestamp will capture the read calendar in the timestamp registers. When tamper detection event and timestamp event are both enabled, temper detection event will also trigger timestamp capture. Timestamp events can be generated on any of the 16 GPIO ports selected by EXTI. The GPIO pins in each port are selected by setting the corresponding EXTI_TS_SEL.TSSEL[3:0] bits.

23.2.15 Tamper Detection

There are three tamper detection pins, RTC_TAMP1 pin is PC13, RTC_TAMP2 pin is PA0, and RTC_TAMP3 pin is PA8. The RTC_TAMPx pins can be used as input pins for tamper event detection. There are two detection modes, edge detection mode and level detection mode with configurable filtering function.

Tamper detection initialization

There are three tamper detection pins, each pin can be configured independently. Users need to configure tamper detection before setting the RTC_TMPCFG.TPxEN bit. When tamper detection is enabled and a tamper event is detected, if RTC_TMPCFG.TPxINTEN is set to 1, the tamper event can generate an interrupt and the RTC_INITSTS.TAMxF bit will be set to 1.

When the RTC_INITSTS.TAMxF bit is set to 1, new tamper events on the same pin cannot be detected.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Timestamp on tamper event

When the RTC_TMPCFG.TPFLT[1:0] bit is set to 0, tamper detection is set to edge detection, with the rising or falling edge controlled by the RTC_TMPCFG.TPxTRG bit. When the corresponding edge is detected, the RTC_TAMPx pin will generate a tamper detection event.

Edge detection of tamper input

When RTC_TMPCFG.TPFLT[1:0] bits are set to 1/2/3, tamper detection is set to level detection. The value of RTC_TMPCFG.TPFLT[1:0] determines the number of samples.

Before each sampling, pre-charging can be performed through the internal pull-up resistor of the tamper pin, and the pre-charging time is controlled by the RTC_TMPCFG.TPPRCH[1:0] bits. When RTC_TMPCFG.TPPUDIS is set to 1, pre-charging will be disabled.

Using RTC_TMPCFG.TPFREQ[2:0] to determine the sampling frequency of level detection can optimize the best balance between tamper detection delay and pull-up power consumption.

Level detection with filtering of RTC_TAMPx input

When RTC_TMPCFG.TPFLT[1:0] bits are set to 1/2/3, tamper detection is set to level detection. The value of RTC_TMPCFG.TPFLT[1:0] determines the number of samples.

Before each sampling, pre-charging can be performed through the internal pull-up resistor of the tamper pin, and the pre-charging time is controlled by the RTC_TMPCFG.TPPRCH[1:0] bits. When RTC_TMPCFG.TPPUDIS is set to 1, pre-charging will be disabled.

Using RTC_TMPCFG.TPFREQ[2:0] to determine the sampling frequency of level detection can optimize the best balance between tamper detection delay and pull-up power consumption.

23.2.16 Daylight Saving Time Configuration

Daylight saving time function can be controlled through RTC_CTRL.SU1H, RTC_CTRL.AD1H, and RTC_CTRL.BAKP bits. Calendar will subtract one hour when set RTC_CTRL.SU1H bit to 1, and add one hour when set RTC_CTRL.AD1H to 1. RTC_CTRL.BAKP can be used to memorize this adjustment.

23.2.17 RTC Sub-second Register Shift

When the value of calendar has a sub-second deviation compared to the external precision clock, the shift function can be used to improve the precision of calendar.

The calendar can be controlled to delay or advance by 1 second using the RTC_SCTRL.AD1S and RTC_SCTRL.SUBF[14:0] bits. The adjustment resolution is 1/(RTC_PRE.DIVS[14:0]+1), where a higher value of RTC_PRE.DIVS[14:0] indicates a higher resolution. To keep the synchronized prescaler output at 1Hz, a higher value of RTC_PRE.DIVS[14:0] means a lower value of RTC_PRE.DIVA[6:0], resulting in higher power consumption

Note: Before starting the shift operation, the user must check if the RTC_SUBS.SS[15] bit is 0.

Whenever writing to the RTC_SCTRL register, the hardware sets the RTC_INITSTS.SHOPF flag, indicating that the shift operation is in a suspended state. Once the shift operation is completed, this bit is cleared by the hardware.

23.2.18 RTC Digital Clock Precision Calibration

Digital precision calibration is achieved by adjusting the number of RTC clock pulses in the calibration period. Digital precision calibration resolution is 0.954 PPM with the range from -487.1 PPM to +488.5 PPM.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

When the input frequency is 32000 Hz, calibration period can be configured as $2^{20}/2^{19}/2^{18}$ RTCCLK cycles or 32/16/8 seconds. The precision calibration register (RTC_CALIB) indicates that there has RTC_CALIB.CM[8:0] RTCCLK clock cycles will be reduced during the specified period.

The value of RTC_CALIB.CM[8:0] represents the number of RTCCLK pulses to be reduced within a specified period. RTC_CALIB.CP can be used to increase by 488.5PPM, where every 2^{11} RTCCLK periods will insert an RTCCLK pulse

When using RTC_CALIB.CM[8:0] and RTC_CALIB.CP in combination, it can increase cycles range from -511 to +512 RTCCLK cycles, and the calibration range from -487.1 ppm to +488.5 ppm, with the resolution is about 0.954 ppm.

The valid calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * (1 + \frac{RTC_CALIB.CP*512 - RTC_CALIB.CM[8:0]}{2^n + RTC_CALIB.CM[8:0] - RTC_CALIB.CP * 512})$$

Note:n=20/19/18

Calibrate when RTC_PRE .DIVA[6:0]<3

When the asynchronous prescaler value (RTC_PRE.DIVA[6:0]) is less than 3, the RTC_CALIB.CP cannot be programmed to 1, and RTC_CALIB.CP value will be ignored if the it has been set to 1.

Assume the frequency of RTCCLK is 32000Hz, when RTC_PRE .DIVA[6:0]<3, the value of RTC_PRE.DIVS[14:0] should be decrease:

- When RTC_PRE .DIVA[6:0] =2, RTC_PRE.DIVS[14:0]=8189.
- When RTC_PRE .DIVA[6:0] =1, RTC_PRE.DIVS[14:0]=16379.
- When RTC_PRE .DIVA[6:0] =0, RTC_PRE.DIVS[14:0]=32759.

The valid calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * \left(1 + \frac{256 - RTC_CALIB.CM[8:0]}{2^n + RTC_CALIB.CM[8:0] - 265}\right)$$

Note:n=20/19/18

Verify RTC calibration

RTC outputs waveform(1Hz) for measuring and verifying RTC precision.

Up to 2 RTCCLK cycles measurement error may occur when measure the RTC frequency in a limit measurement period. If the measurement period is the same as calibration period, the error can be eliminated.

- The calibration period is 32 seconds (default).

  Using an accurate 32 second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.447ppm (0.5 RTCCLK cycles within 32 seconds).

- The calibration period is 16 seconds.

  Using an accurate 16 second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.954ppm (0.5 RTCCLK cycles within 16 seconds).

- The calibration period is 8 seconds.

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Using an accurate 8 second period to measure the 1Hz calibration output can ensure that the measurement error is within 1.907ppm (0.5 RTCCLK cycles within 8 seconds).

Dynamic recalibration

When RTC_INITSTS.INITF=0, RTC_CALIB register can be updated through following steps:

- Wait RTC_INITSTS.RECPF=0.
- A new value is written to the RTC_CALIB, then RTC_INITSTS.RECPF is automatically set to 1.
- The new calibration settings will take effect within 3 ck_apre cycles after a data write to the RTC_CALIB.

23.2.19 RTC Low Power Mode

The operating state of RTC in low power mode:

Lower Power Mode	RTC Operating State	Exit Low Power Mode
SLEEP	Normal operation	RTC interrrupt
STOP	Normal operation when RTC clock source is LSI	Alarm A, Alarm B, Periodic Wakeup, tamper event and Timestamp event

23.3 RTC Registers

23.3.1 RTC Register Overview

Table 23-2 RTC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RTC_INITSTS	Reserved															RECPF	TAM3F	TAM2F	TAM1F	TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
004h	RTC_CTRL	Reserved								COEN	OUTSEL[1:0]		OPOL	CALOSEL	BAKP	SU1H	AD1H	TSIEN	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	Reserved	HFMT	BYPS	REFCLKEN	TEDGE	WKUPSEL[2:0]		
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
008h	RTC_TSH	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SCT[2:0]			SCU[3:0]			
	Reset Value										0	0	0	0	0	0	0	Reserved	0	0	0	0	0	0	0	Reserved	0	0	0	0	0	0	0
00Ch	RTC_DATE	Reserved				YRT[3:0]				YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved	DAT[1:0]		DAU[3:0]							
	Reset Value					0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	Reserved	0	0	0	0	0	0	1
010h	RTC_WRP	Reserved																PKEY[7:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	RTC_SCTRL	AD1S	Reserved															SUBF[14:0]															
	Reset Value	0																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	RTC_SUBS	Reserved																SS[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	RTC_TST	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SET[2:0]			SEU[3:0]			
	Reset Value										0	0	0	0	0	0	0	Reserved	0	0	0	0	0	0	0	Reserved	0	0	0	0	0	0	0

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

020h	RTC_ALARMA	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	RTC_PRE	Reserved									DIVA[6:0]							Reserved	DIVS[14:0]													
	Reset Value										1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
028h	RTC_ALARMB	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	RTC_WKUPT	Reserved																WKUPT[15:0]														
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
030h	RTC_TMPCFG	Reserved				TP3MF	Reserved	TP3INTEN	TP2MF	Reserved	TP2INTEN	TP1MF	Reserved	TP1INTEN	TPPUDIS	TPPRCH[1:0]		Reserved	TPFLT[1:0]		Reserved	TPFREQ[2:0]			TPTS	TP3TRG	TP3EN	TP2TRG	TP2EN	TPINTEN	TP1TRG	TP1EN
	Reset Value					0		0	0		0	0		0	0	0	0		0	0		0	0	0	0	0	0	0	0	0	0	0	0
034h	RTC_ALRMASS	Reserved												MASKSSA[3:0]				Reserved	SSV[14:0]													
	Reset Value													0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	RTC_OPT	Reserved																														TYPE
	Reset Value																															0
03Ch	RTC_ALRMBSS	Reserved												MASKSSB[3:0]				Reserved	SSV[14:0]													
	Reset Value													0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	RTC_CALIB	Reserved																			CP	CW8	CW16	CM[8:0]								
	Reset Value																				0	0	0	0	0	0	0	0	0	0	0	0
044h	RTC_TSSS	Reserved																SSE[15:0]														
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	RTC_TSD	Reserved																MOT	WDU[2:0]			MOU[3:0]				Reserved	DAT[1:0]		DAU[3:0]				
	Reset Value																	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

23.3.2 RTC Initial Status Register (RTC_INITSTS)

Address offset: 0x00

Reset value: 0x0000 0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															RECPF
															r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAM3F	TAM2F	TAM1F	TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rw	r	rc_w0	r	r	r	r	r

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	RECPF	Recalibration pending flag The RECPF status flag is automatically set to '1' when software writes to the RTC_CALIB register, indicating that the RTC_CALIB register is blocked. After the new calibration settings are processed, this bit returns to '0'.
15	TAM3F	RTC_TAMP3 detection flag When a tamper event is detected on the RTC_TAMP3 input, the hardware sets this flag. Writing 0 through software clears it.
14	TAM2F	RTC_TAMP2 detection flag. When a tamper event is detected on the RTC_TAMP2 input, the hardware sets this flag. Writing 0 through software clears it
13	TAM1F	RTC_TAMP1 detection flag. When a tamper event is detected on the RTC_TAMP1 input, the hardware sets this flag. Writing 0 through software clears it.
12	TISOVF	The time-stamp overflow flag When a timestamp event occurs while the TISF bit has already been set to 1, the hardware sets this flag to 1. It is recommended to check and clear the TISOVF bit after clearing the TISF bit. Otherwise, if the timestamp event occurs just before clearing the TISF bit, the overflow event might be missed
11	TISF	Time-stamp flag This flag is set to '1' by hardware when a time-stamp event occurs. This flag can be cleared by software by writing 0
10	WTF	Wake up timer flag When the wake-up auto-reload counter reaches 0, the hardware sets this flag. This flag is cleared by software by writing 0. Before the WTF is set to 1 again, this flag must be cleared by software for at least 1.5 RTCCLK cycles
9	ALBF	Alarm B flag This flag is set to '1' by hardware when the time/date registers(RTC_TSH and RTC_DATE) value match the Alarm B register(RTC_ALARMB) values. This flag can be cleared by software by writing 0
8	ALAF	Alarm A flag This flag is set to '1' by hardware when the time/date registers(RTC_TSH and RTC_DATE) value match the Alarm A register(RTC_ALARMA) values. This flag can be cleared by software by writing 0
7	INITM	Enter initialization mode 0: Free operating mode 1: Enter initialization mode and set calendar time value, date value, and prescale value.
6	INITF	Initialization flag RTC is in initialization state when this bit is '1', and calendar time, date and prescale value can be updated. 0: Calendar register can not be updated 1: Calendar register can be updated

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
5	RSYF	Register synchronization flag This flag is set to '1' by hardware when the calendar value are copied into the shadow registers. This bit is cleared by hardware when in initialization mode, while a shift operation is pending (SHOPF = 1), or when in bypass shadow register mode (RTC_CTRL.BYPS = 1). This bit can also be cleared by software. It is cleared either by software or by hardware in initialization mode. 0: Calendar shadow register not yet synchronized 1: Calendar shadow register synchronized
4	INITSF	Initialization status flag This flag is set to '1' by hardware when the calendar year field is different from 0 (which is the RTC domain reset state). 0: Calendar has not been initialized 1: Calendar has been initialized
3	SHOPF	Shift operation pending flag This flag is set to '1' by hardware as soon as a shift operation is initiated by a write to the RTC_SCTRL register. It is cleared by hardware when the corresponding shift operation has been completed, note that writing to the SHOPF bit has no effect. 0: No shift operation is pending 1: A shift operation is pending
2	WTWF	Wakeup timer write flag 0: Wakeup timer configuration update is not allowed 1: Wakeup timer configuration update is allowed
1	ALBWF	Alarm B write flag This flag is set to '1' by hardware when Alarm B values can be changed, after the RTC_CTRL.ALBEN bit has been set to 0. 0: Alarm B update is not allowed 1: Alarm B update is allowed
0	ALAWF	Alarm A write flag. This flag is set to '1' by hardware when Alarm A values can be changed, after the RTC_CTRL.ALAEN bit has been set to 0. 0: Alarm A update is not allowed 1: Alarm A update is allowed

23.3.3 RTC Control Register (RTC_CTRL)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								COEN	OUTSEL[1:0]		OPOL	CALOSEL	BAKP	SU1H	AD1H
								rw	rw		rw	rw	rw	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSIEN	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	Reserved	HFMT	BYPS	REF CLKEN	TEDGE	WKUPSEL[2:0]		

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North. Nanshan District, Shenzhen, 518057, P.R.China

rw rw rw rw rw rw rw rw rw rw rw rw rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	COEN	Calibration output enable 0: Disable calibration output 1: Enable calibration output
22:21	OUTSEL[1:0]	Output selection These bits are used to select the alarm/wakeup output 00: Disable output 01: Enable Alarm A output 10: Enable Alarm B output 11: Enable Wakeup output
20	OPOL	Output polarity bit This bit is used to configure the polarity of output. 0: When the ALAF/ALBF/WTF flag is set to 1 (depending on OUTSEL [1:0]), the pin outputs a high level 1: When the ALAF/ALBF/WTF flag is set to 1 (depending on OUTSEL [1:0]), the pin outputs a low level
19	CALOSEL	Calibration output selection When COEN=1, this bit selects which signal is output on RTC_CALIB Under the conditions of RTCCLK at 32 kHz and default prescaler values (RTC_PRE.DIVA[6:0]=127 and RTC_PRE.DIVS[14:0]=255), these frequencies are valid. 0: Calibration output is 256 Hz 1: Calibration output is 1 Hz
18	BAKP	This bit can be written by the user to remember if daylight saving time changes have been applied.
17	SU1H	Subtract 1 hour (winter time change) 1 hour will be subtracted to the calendar time when the current hour value is not 0. This bit is always read as 0. Setting this bit is invalid when the current hour is 0 0: No effect. 1: Subtracts 1 hour to the current time. This can be used to change the outdoor initialization mode in winter.
16	AD1H	Add 1 hour (summer time change) When this bit is set, 1 hour can be added to the calendar time. This bit is always read as. 0: No effect. 1: Adds 1 hour to the current time. This can be used to change the outdoor initialization mode in summer.
15	TSIEN	Timestamp interrupt enable bit. 0: Disable Timestamp interrupt 1: Enable Timestamp interrupt
14	WTIEN	Wakeup timer interrupt enable

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		0: Disable wakeup timer interrupt. 1: Enable wakeup timer interrupt.
13	ALBIEN	Alarm B interrupt enable 0: Disable Alarm B interrupt 1: Enable Alarm B Interrupt
12	ALAIEN	Alarm A interrupt enable 0: Disable Alarm A interrupt 1: Enable Alarm A interrupt
11	TSEN	Timestamp enable 0: Disable timestamp 1: Enable timestamp
10	WTEN	Wakeup timer enable 0: Disable wakeup timer 1: Enable wakeup timer
9	ALBEN	Alarm B enable 0: Disable Alarm B 1: Enable Alarm B
8	ALAEN	Alarm A enable 0: Disable Alarm A 1: Enable Alarm A
7	Reserved	Reserved, the reset value must be maintained
6	HFMT	Hour format bit 0: 24 hour format 1: Am/PM format
5	BYPS	Bypass values from the shadow registers 0: Calendar values(when reading from RTC_SUBS、RTC_TSH and RTC_DATE) are copied from the shadow registers, which are refreshed every two RTCCLK cycles. 1: Calendar values(when reading from RTC_SUBS、RTC_TSH and RTC_DATE) are copied directly from the calendar counters. *Note: If the frequency of the APB1 clock falls below seven times the frequency of RTCCLK, RTC_CTRL.BYPS bit must be set to '1'*
4	REFCLKEN	RTC_REFIN reference clock detection bit (50 or 60Hz). 0: Disable RTC_REFIN detection 1: Enable RTC_REFIN detection Note: DIVS must be 0x00FF
3	TEDGE	Time-stamp event active edge 0: Generate a timestamp event on the rising edge of the RTC_TS input 1: Generate a timestamp event on the falling edge of the RTC_TS input *Note: When changing TEDGE, RTC_CTRL.TSEN must be reset to avoid accidentally setting RTC_INITSTS.TISF to 1*
2:0	WKUPSEL[2:0]	Wakeup clock selection 000: RTC clock is divided by 16 001: RTC clock is divided by 8

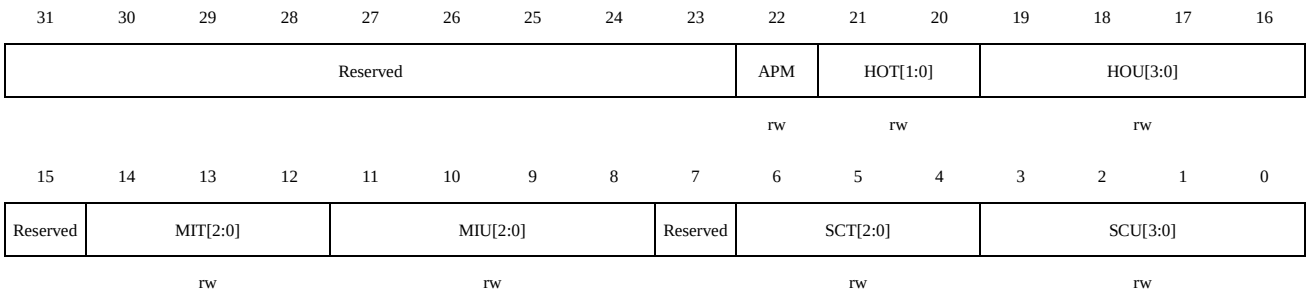
Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		010: RTC clock is divided by 4 011: RTC clock is divided by 2 10x: ck_spre (usually 1Hz) clock is selected 11x: ck_spre (usually 1Hz) clock is selected and configure the wake-up timer counter value to 216

23.3.4 RTC Calendar Time Register (RTC_TSH)

Address offset: 0x08

Reset value: 0x0000 0000

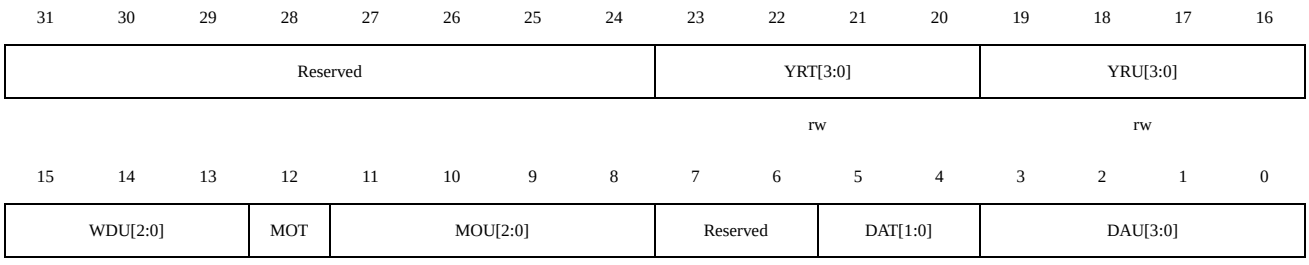


Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM format. 0:AM format or 24-hour format 1:PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT [2: 0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SCT[2:0]	Describes the second tens value in BCD format
3:0	SCU[3:0]	Describes the second units value in BCD format

23.3.5 RTC Calendar Date Register (RTC_DATE)

Address offset: 0x0C

Reset value: 0x0000 2101



Nations Technologies Inc.
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

rw rw rw rw rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	YRT[3:0]	Describes the year tens value in BCD format
19:16	YRU[3:0]	Describes the year units value in BCD format
15:13	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

23.3.6 RTC Write Protection Register (RTC_WRP)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PKEY[7:0]							
								w							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	PKEY[7:0]	Write protection key Reading this byte always returns 0x00. For detail on how to unlock RTC register write protection, see chapter RTC write protection register.

23.3.7 RTC Shift Control Register (RTC_SCTRL)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AD1S	Reserved														

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Email：info@nationstech.com
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w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SUBF[14:0]														

w

Bit Field	Name	Description
31	AD1S	Add one second 0: No impact. 1: Subtract one second to the clock/calendar This bit can only be written and read as zero. Writing to this bit does not have an impact when RTC_INITSTS.SHOPF=1.
30:15	Reserved	Reserved, the reset value must be maintained
14:0	SUBF[14:0]	Subtract a fraction of a second These bits can only be written and read as zero. Writing to these bits has no effect when RTC_INITSTS.SHOPF=1. The value written to SUBF[14:0] is added to the synchronized prescaler counter, causing a delay in the clock: delay(seconds)= (SUBF[14:0]+1) / (DIVS[14:0] + 1) The AD1S bit can be used together with the SUBF[14:0] bits "Advance (seconds)= (1 - ((SUBF[14:0]+1) / (DIVS[14:0] + 1))) *Note: The RTC_INITSTS.RSYF bit will be cleared when writing to SUBF[14:0]. When RTC_INITSTS.RSYF=1, the shadow registers have been updated to the shifted time.*

23.3.8 RTC Sub-second Register (RTC_SUBS)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS[15:0]															

r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SS[15:0]	Sub-second value. The value is the counter value of synchronous prescaler. This sub-second value is calculated by the below formula: Sub-second value = (RTC_PRE.DIVS[14:0]-SS)/(RTC_PRE.DIVS[14:0]+1)

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Email：info@nationstech.com
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Bit Field	Name	Description
		Note: SS[15:0] can be larger than RTC_PRE.DIVS[14:0] only after the shift operation is completed. In this case, the correct time/date is one second slower than the time/date indicated by RTC_TSH/RTC_DATE.

23.3.9 RTC Timestamp Time Register (RTC_TST)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rserved									APM	HOT[1:0]		HOU[3:0]			
									r	r		r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rserved	MIT[2:0]			MIU[3:0]				Rserved	SET[2:0]			SEU[3:0]			
	r			r					r			r			

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM notation 0: AM or 24-hour clock 1: PM
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

23.3.10 RTC Alarm A Register (RTC_ALARMA)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]			
rw	rw	rw		rw				rw	rw	rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			

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Email：info@nationstech.com
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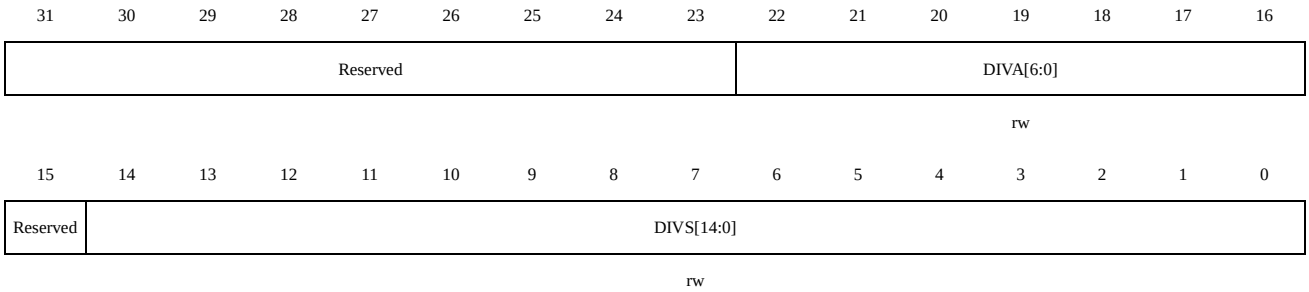
rw rw rw rw rw rw

Bit Field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

23.3.11 RTC Prescaler Register (RTC_PRE)

Address offset: 0x24

Reset value: 0x007F 00FF



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Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22:16	DIVA[6:0]	Asynchronous prescaler factor f_{ck_apre} = RTCCLK/(DIVA[6:0]+1)
15	Reserved	Reserved, the reset value must be maintained
14:0	DIVS[14:0]	Synchronous prescaler factor f_{ck_spre} = f_{ck_apre}/(DIVS[14:0]+1)

23.3.12 RTC Alarm B Register (RTC_ ALARMB)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]			
rw	rw	rw		rw				rw	rw	rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
rw	rw			rw				rw	rw			rw			

Bit Field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask

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Tel：+86-755-86309900
Email：info@nationstech.com
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Bit Field	Name	Description
		0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

23.3.13 RTC Wakeup Timer Register (RTC_WKUPT)

Address offset: 0x2C

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUPT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WKUPT[15:0]	Wake up auto-reload value bits The RTC_INITSTS.WTF flag is set every (WKUPT[15:0] + 1) ck_wut cycles when the RTC_CTRL.WTEN=1. The wakeup timer becomes 17-bits When RTC_CTRL.WKUPSEL[2]=1. *Note:* *This register change (such as the second setting or later Settings) needs to be changed in the wakeup interrupt, otherwise the changed settings will not take effect immediately, but will take effect after the next wakeup;* *In particular, when RTC_CTRL.WKUPSEL[2:0] is set to 010, the modified setting does not take effect immediately, but will take effect after wake up in the next cycle.*

23.3.14 RTC Tamper Configuration Register（RTC_TMPCFG）

Address offset：0x30

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				TP3MF	Reserved	TP3INTEN	TP2MF	Reserved	TP2INTEN	TP1MF	Reserved	TP1INTEN	TPPUDIS	TPPRCH[1:0]	
				rw		rw	rw		rw	rw		rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		TPFLT[1:0]		Reserved	TPFREQ[2:0]			TPTS	TP3TRG	TP3EN	TP2TRG	TP2EN	TPINTEN	TP1TRG	TP1EN
		rw			rw			rw	rw	rw	rw	rw	rw	rw	rw

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Email：info@nationstech.com
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Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	TP3MF	Tamper 3 mask flag. 0: Do not mask Tamper 3 events. 1: Mask Tamper 3 events. *Note: When TP3MF is set, Tamper 3 interrupt must not be enabled.*
26	Reserved	Tamper 3 non-erase bit. 0: Tamper 3 event erases backup registers. 1: Tamper 3 event does not erase backup registers
25	TP3INTEN	Tamper 3 interrupt enable bit. 0: Disables Tamper 3 interrupt when TPINTEN = 0. 1: Enables Tamper 3 interrupt.
24	TP2MF	Tamper 2 mask flag. 0: Do not mask Tamper 2 events. 1: Mask Tamper 2 events. *Note: When TP2MF is set, Tamper 2 interrupt must not be enabled*
23	Reserved	Tamper 2 non-erase bit. 0: Tamper 2 event erases backup registers. 1: Tamper 2 event does not erase backup registers
22	TP2INTEN	Tamper 2 interrupt enable bit. 0: Disables Tamper 2 interrupt when TPINTEN = 0. 1: Enables Tamper 2 interrupt.
21	TP1MF	Tamper 1 mask flag. 0: Do not mask Tamper 1 events. 1: Mask Tamper 1 events. *Note: When TP1MF is set, Tamper 1 interrupt must not be enabled*
20	Reserved	Tamper 1 non-erase bit. 0: Tamper 1 event erases backup registers. 1: Tamper 1 event does not erase backup registers
19	TP1INTEN	Tamper 1 interrupt enable bit. 0: Disables Tamper 1 interrupt when TPINTEN = 0. 1: Enables Tamper 1 interrupt
18	TPPUDIS	RTC_TAMPx pull-up disable bit. 0: Enable pre-charging of RTC_TAMPx pin before each sampling. 1: Disable pre-charging of RTC_TAMPx pin
17:16	TPPRCH[1:0]	RTC_TAMPx pre-charging duration. These bits determine the pre-charging time before each sampling. 0x0: 1 RTCCLK period 0x1: 2 RTCCLK periods 0x2: 4 RTCCLK periods 0x3: 8 RTCCLK periods
15:14	Reserved	Reserved, the reset value must be maintained
13:12	TPFLT[1:0]	RTC_TAMPx filter count. These bits determine the number of consecutive samples on a valid level.

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Email：info@nationstech.com
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Bit Field	Name	Description
		0x0: Trigger tamper event after 1 sample on a valid level 0x1: Trigger tamper event after 2 consecutive samples on a valid level 0x2: Trigger tamper event after 4 consecutive samples on a valid level 0x3: Trigger tamper event after 8 consecutive samples on a valid level
11	Reserved	Reserved, the reset value must be maintained
10:8	TPFREQ[2:0]	Tamper sampling frequency. This bit determines the frequency at which each RTC_TAMPx input is sampled. 0x0: Sample once every 32768 RTCCLKs 0x1: Sample once every 16384 RTCCLKs 0x2: Sample once every 8192 RTCCLKs 0x3: Sample once every 4096 RTCCLKs 0x4: Sample once every 2048 RTCCLKs 0x5: Sample once every 1024 RTCCLKs 0x6: Sample once every 512 RTCCLKs 0x7: Sample once every 256 RTCCLKs
7	TPTS	Enable timestamp on tamper detection event. 0: Do not save timestamp on tamper detection event 1: Save timestamp on tamper detection event TPTS remains valid even if RTC_CTRL.TSEN=0
6	TP3TRG	Tamper 3 event trigger mode. If TPFLT[1:0] != 00, Tamper detection is in level mode: 0: Low level triggers Tamper detection event. 1: High level triggers Tamper detection event. If TPFLT[1:0] = 00, Tamper detection is in edge mode: 0: Rising edge triggers Tamper detection event. 1: Falling edge triggers Tamper detection event
5	TP3EN	RTC_TAMP3 detection enable bit. 0: Disable RTC_TAMP3 input detection 1: Enable RTC_TAMP3 input detection
4	TP2TRG	Tamper 2 event trigger mode. If TPFLT[1:0] != 00, tamper detection is in level mode: 0: Low level triggers tamper detection event. 1: High level triggers tamper detection event. If TPFLT[1:0] = 00, tamper detection is in edge mode: 0: Rising edge triggers tamper detection event. 1: Falling edge triggers tamper detection event
3	TP2EN	RTC_TAMP2 detection enable bit. 0: Disable RTC_TAMP2 input detection 1: Enable RTC_TAMP2 input detection
2	TPINTEN	Tamper event interrupt enable. 0: Disable tamper interrupt 1: Enable tamper interrupt *Note: This bit enables interrupts for all tamper pin events, regardless of the*

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Email：info@nationstech.com
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Bit Field	Name	Description
		TPxINTEN level. If this bit is cleared, each tamper event interrupt can be individually enabled by setting TPxINTEN
1	TP1TRG	Tamper 1 event trigger mode. If TPFLT[1:0] != 00, tamper detection is in level mode: 0: Low level triggers tamper detection event. 1: High level triggers tamper detection event. If TPFLT[1:0] = 00, tamper detection is in edge mode: 0: Rising edge triggers tamper detection event. 1: Falling edge triggers tamper detection event.
0	TP1EN	RTC_TAMP1 detection enable bit. 0: Disable RTC_TAMP1 input detection 1: Enable RTC_TAMP1 input detection

23.3.15 RTC Alarm A Sub-second Register (RTC_ALRMASS)

Address offset: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												MASKSSB[3:0]			
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SSV[14:0]														
	rw														

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:16	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ... 0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0],

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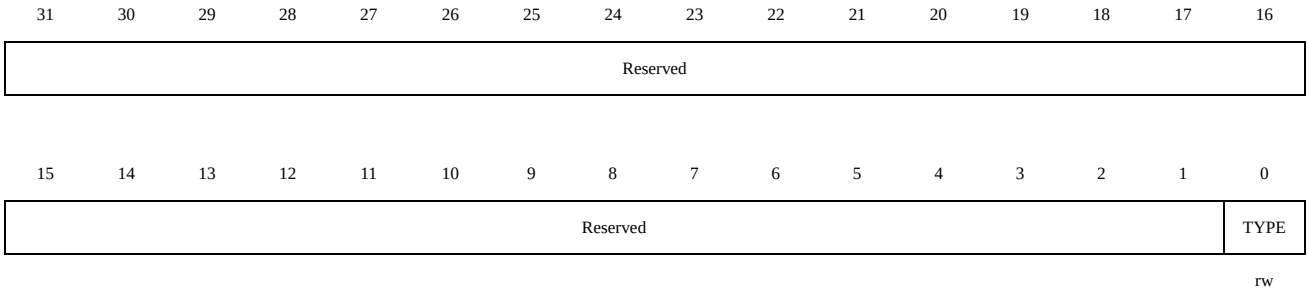
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Bit Field	Name	Description
		and bit number of compared is controlled by MASKSSB[3:0].

23.3.16 RTC Option Register (RTC_OPT)

Address offset: 0x38

Reset value: 0x0000 0000

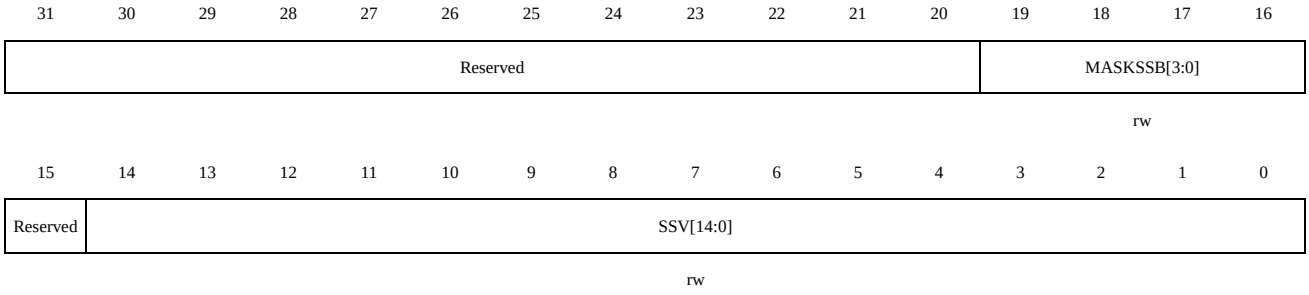


Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	TYPE	RTC_ALARM output type on PC13 0: Open-drain output 1: Push-pull output

23.3.17 RTC Alarm B Sub-second Register (RTC_ALRMBSS)

Address offset: 0x3C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:16	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ...

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Email：info@nationstech.com
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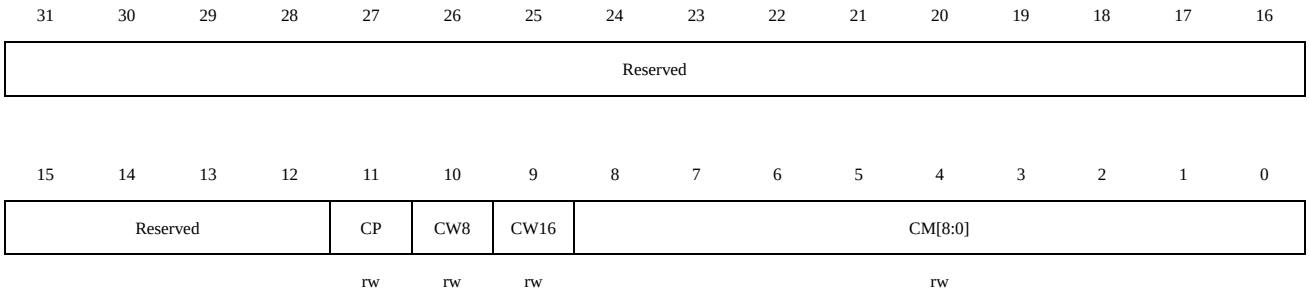
Bit Field	Name	Description
		0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and bit number of compared is controlled by MASKSSB[3:0].

23.3.18 RTC Calibration Register (RTC_CALIB)

Address offset: 0x40

Reset value: 0x0000 0000



Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	CP	Increase frequency of RTC by 488.5 ppm This feature is intended to be used along with CM[8:0]. When frequency of RTCCLK is 32768 Hz, the number of RTCCLK pulses added during a 32-second window is ((512 * CP) – CM[8:0]). 0: No add pulse. 1: One RTCCLK pulse is inserted every 211 pulses.
10	CW8	Select an 8-second calibration cycle period 0: Not effect. 1: Select an 8-second calibration period. When CW8 is set to ‘1’, the 8-second calibration cycle period is selected. Note: when CW8 = 1, CM[1:0] will always be' 00'
9	CW16	To select a 16-second calibration cycle period 0: Not effect. 1: Select a calibration period of 16 seconds. If CW8 = 1, this bit cannot be set to 1. Note: when CW16 = 1, CM[0] will always be '0'
8:0	CM[8:0]	Negative calibration bits The number of mask pulse out of 220 RTCCLK pulses. This effectively decreases the frequency of the calendar with a resolution of 0.9537 ppm.

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Tel：+86-755-86309900
Email：info@nationstech.com
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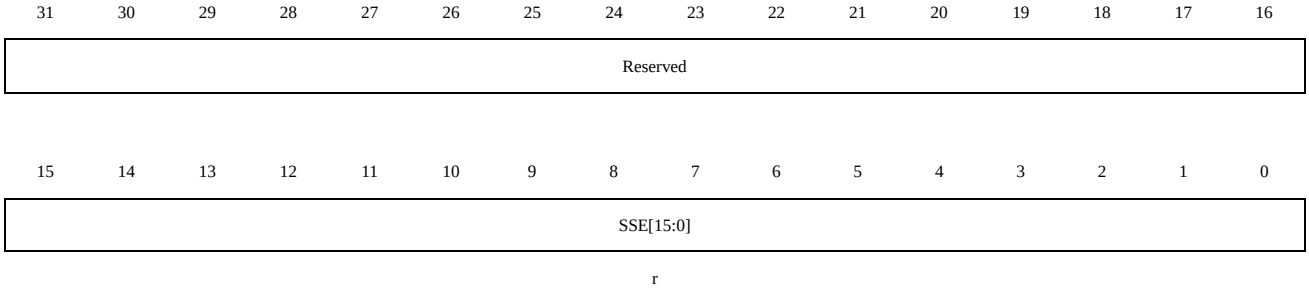
23.3.19 RTC Timestamp Sub-second Register (RTC_TSSS)

Address offset: 0x44

Reset value: 0x0000 0000

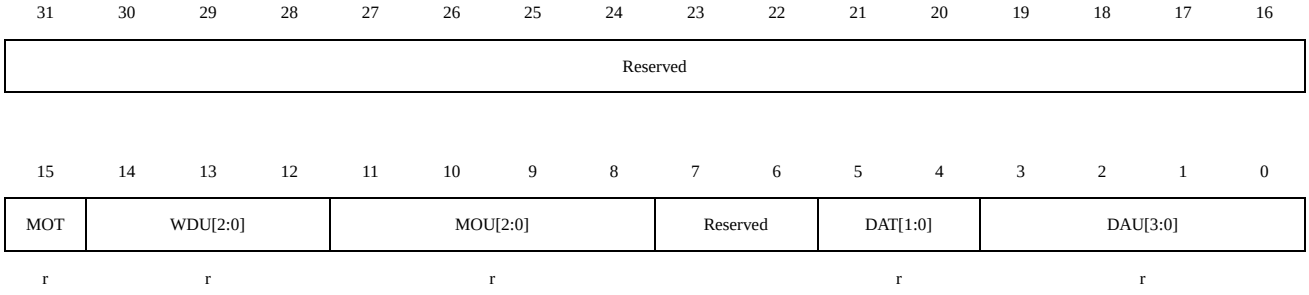


Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SSE[15:0]	Sub second value SSE[15:0] is the value in the synchronous prescaler counter. The fraction of a second is provided by the formula below: Second fraction = (RTC_PRE.DIVS[14:0] – SSE[15:0]) / (RTC_PRE.DIVS[14:0] + 1) *Note: SSE[15:0] can be larger than RTC_PRE.DIVS[14:0] only after a shift operation. In that case, the correct time/date is one second less than as indicated by RTC_TSH/RTC_DATE.*

23.3.20 RTC Timestamp Date Register (RTC_TSD)

Address offset: 0x48

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	MOT	Describes the month tens value in BCD format
14:12	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
		... 111: Sunday
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

24 Beeper

24.1 Introduction

The Beeper module can generate periodic signals to drive external passive Beepers. It is used to generate a prompt tone or an alarm sound.

24.2 Function Description

The Beeper, as an independent module, is connected to the APB1 bus with a maximum operating frequency of 32MHz. The timbre can be divided into 25 grades, and different timbres can be adjusted by configuring the relevant registers when using.

24.3 Beeper Registers

These peripheral registers must be operated in word (32-bit) mode.

24.3.1 Beeper Register Overview

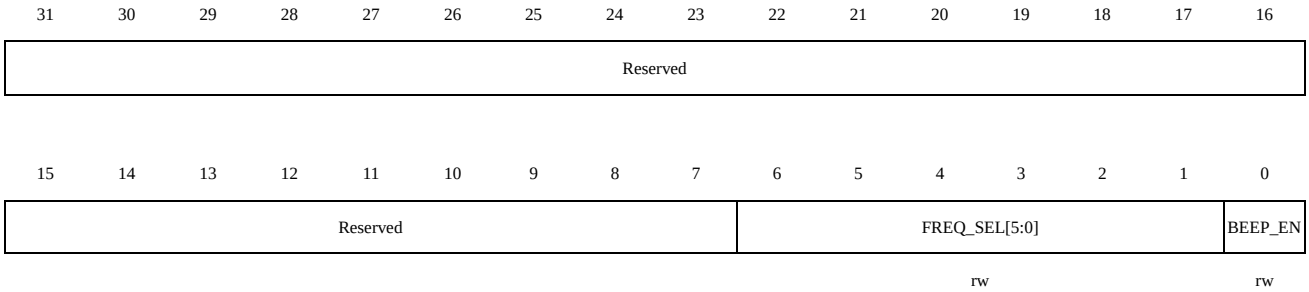
Table 24-1 Beeper Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	BEEPER_CTRL	Reserved																									FREQ_SEL[5:0]						BEEP_EN
	Reset Value																										0	0	0	0	0	0	0

24.3.2 Beeper Control Register (BEEPER_CTRL)

Address offset: 0x00

Reset value: 0x0000 0000



Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6:1	FREQ_SEL[5:0]	Beeper output frequency selection: 000000: Output frequency is 131Hz 000001: Output frequency is 147Hz 000010: Output frequency is 165Hz

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Bit Field	Name	Description
		000011: Output frequency is 175Hz 000100: Output frequency is 196Hz 000101: Output frequency is 220Hz 000110: Output frequency is 247Hz 000111: Output frequency is 262Hz 001000: Output frequency is 294Hz 001001: Output frequency is 330Hz 001010: Output frequency is 349Hz 001011: Output frequency is 392Hz 001100: Output frequency is 440Hz 001101: Output frequency is 494Hz 001110: Output frequency is 524Hz 001111: Output frequency is 588Hz 010000: Output frequency is 660Hz 010001: Output frequency is 698Hz 010010: Output frequency is 784Hz 010011: Output frequency is 880Hz 010100: Output frequency is 988Hz 010101: Output frequency is 1KHz 010110: Output frequency is 2KHz 010111: Output frequency is 4KHz 011000: Output frequency is 8KHz *Note: The output frequency is a theoretical value, the actual output may deviate due to the LSI frequency.*
0	BEEP_EN	Beeper enable 0: Beeper disabled *(Note: The Beeper output can be immediately turned off by disabling RCC_APBPCLKEN.BEEPEREN when BEEPER_EN=0.)* 1: Beeper enabled

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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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25 Debug Support (DBG)

25.1 Overview

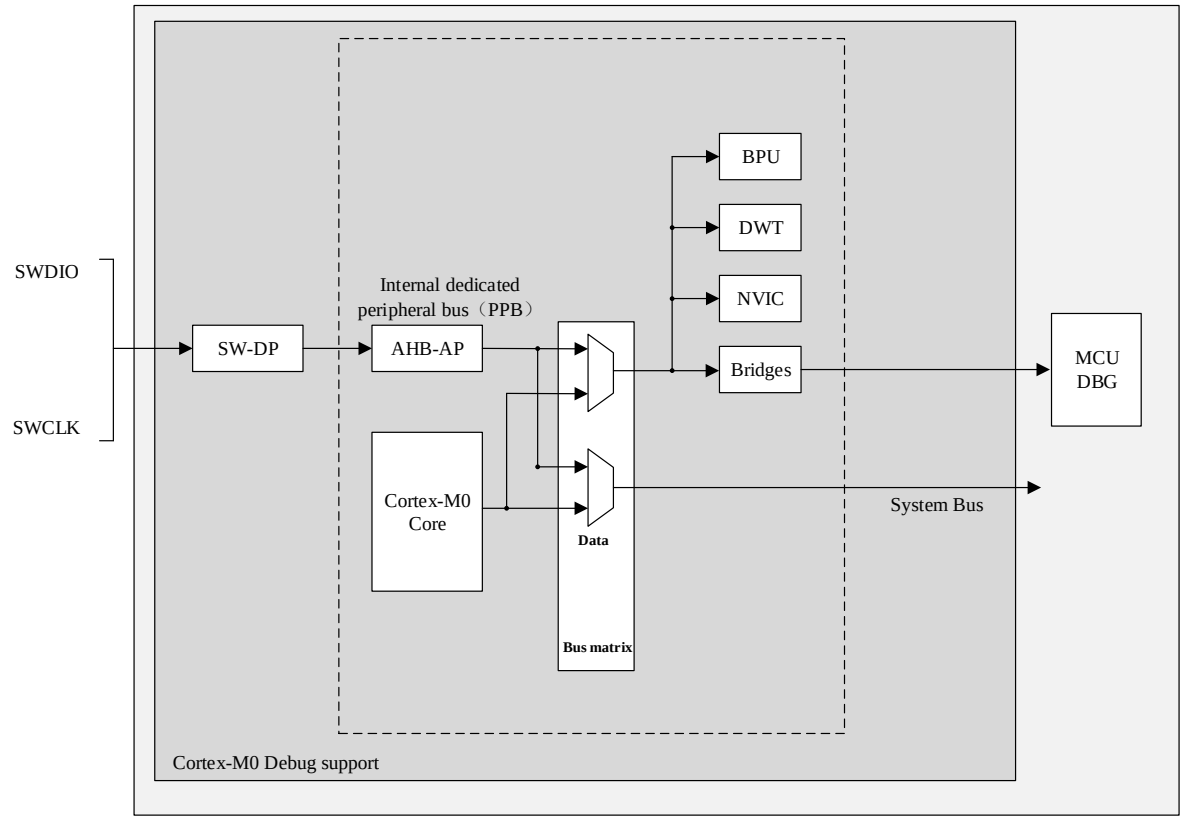
The N32G05x uses Cortex®-M0 core, which integrates hardware debugging module. It supports instruction breakpoint (stops when fetching instructions) and data breakpoint (stops when accessing data). When the core is stopped, the user can view the internal state of the core and the external state of the system. After the user's query operation is completed, the core and peripherals can be restored, and the corresponding program can continue to be executed.

The hardware debugging module of the N32G05x core can be used when it is connected to the debugger (when it is not disabled).

N32G05x supports the following debugging interfaces:

- Serial interface

Figure 25-1 N32G031 Level And Cortex®-M0 Level Debugging Block Diagram



The ARM Cortex®-M0 core hardware debugging module can provide the following debugging functions:

- SW-DP: serial debugging port
- AHP-AP: AHB access port
- BPU: breakpoint generation
- DWT: data trigger

Reference:

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Tel：+86-755-86309900
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Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

- Cortex®-M0 Technical Reference Manual (TRM)
- ARM debug interface V5 structure specification
- ARM CoreSight development tool set (r1p0 version) technical reference manual

25.2 SWD Function

The debugging tool can call the debugging function through the above-mentioned SWD debugging interface.

25.2.1 Pin Assignment

SWD (serial debug) interface consists of two pins: SWCLK (clock pin) and SWDIO (data input and output pin).

The pin assignment of SWD debug interface is shown in the following table:

Table 25-1 Debug Port Pin

Debug Port	Pin Assignment
SWDIO	PA13
SWCLK	PA14

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Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

26 Unique Device Serial Number (UID)

26.1 Introduction

The MCU series products have two embedded unique device serial numbers with different lengths, namely 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the Flash memory. The information they contain is written at the factory and ensures that each MCU is unique in any situation. They can be read by user applications or external devices through CPU or SWD interface and cannot be modified.

UID is 96 bits, which is usually used as serial number or password. When writing to Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory, and it can also be used to activate Secure Bootloader with security function.

UCID is 128 bits and complies with the definition of the Nations Technologies chip serial number. It contains information about chip production and version.

In addition to the above two device serial numbers, there is also a 32-bit DBGMCU_ID, which contains the chip version number, chip model, and Flash/SRAM capacity information.

26.2 UID Register

Start address: 0x1FFF_F910, 96 bits in length.

26.3 UCID Register

Start address: 0x1FFF_F8D0, 128 bits in length.

26.4 DBGMCU_ID Register

Start address: 0x1FFF_F920, 32 bits in length. Different bytes are arranged with the low byte first and the high byte last; within the same byte, the high bit comes first and the low bit comes last.

Table 26-1 DBGMCU_ID Bit Description

Description	Size	Remark
Chip version number	4bit	The lower 4 bits of the chip version number.
	4bit	The upper 4 bits of the chip version number.
Chip model	4bit	The upper 4 bits of the device model number. The device model consists of 12 high, middle and low bits, representing the model of the chip.
	4bit	The middle 4 bits of the device model number.
	4bit	The lower 4 bits of the device model number.
Flash capacity	4bit	Flash capacity indicator. 16KB as unit, Flash size = (N+1) * 16KB
SRAM capacity	4bit	SRAM capacity indicator. 4KB as unit, SRAM size = (N+1) * 4KB

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China

Reserved	4bit	Keep it all 1.

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Tel：+86-755-86309900
Email：info@nationstech.com
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27 Version History

Version	Date	Changes
V1.0.0	2024.7.18	Initial version
V1.1.0	2024.12.2	1. Correction of GPIO chapter table number disorder issue 2. Update the description of COM and SEG multiplexing 3. Change the description of USART in the text to UART uniformly 4. Update the read protection configuration list 5. Update the permission table SRAM to start the system memory area permission at L1 level 6. Delete the description of the 1.8V gear in the PWR_CTRL.PLS and PWR_CTRL2.LVRLS register bits 7. Added SPI3_NSS reuse definition pin PD2 8. GPOx_DS Register Description Update 9. Optimize the channel configuration process description in the DMA chapter 10. Update the block diagram in the TIM chapter, remove the words TIM1/8, remove the Chinese characters, and remove the word TIM8 from the entire text 11. Figure 9-21 Capture/Compare Channel 1 Main Circuit Diagram Update 12. Delete the output part (x=4) of channel x in Figure 9-23 13. Precautions for adding programmable channel sampling time 14. COMP Register Description Optimization 15. Optimization of LCD flicker function description 16. Add some precautions to the SPI chapter and remove the word I2S 17. Delete information related to 32.768KHz in the RTC chapter 18. Delete duplicate descriptions of SWD pins in the DBG chapter 19. Correction of Out of Order Table Numbers in GPIO Chapters 20. Delete the words' PD1/PD2 pins' from GPIO and EXTI descriptions

Nations Technologies Inc.
Tel：+86-755-86309900
Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
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Email：info@nationstech.com
Address: Nations Tower, #109 Baoshen Road, Hi-tech Park North.
Nanshan District, Shenzhen, 518057, P.R.China