N32G451 series errata sheet V1.3.0

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NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

1 Errata list

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

2 Power control (PWR)

2.1 Stop2 Mode wakes up

Description

MCU is in Stop2 mode. If NRST reset occurs at the same time when MCU is awakened, NRST cannot reset MCU, awakening takes precedence and MCU will respond to awakening first.

Workaround

Avoid NRST resetting the MCU at the same time of awakening, or NRST resetting the MCU twice in a row in a scenario where NRST resetting is required.

3 Reset and Clock Control (RCC)

3.1 System Timer (Systick)

Description

Set the CLKSOURCE control bit of the SysTick control register. If the External Reference Clock (STCLK) is set as the clock source, MCU cannot be woken up. When Use-core-clock is set as the clock source, the clock works normally.

Workaround

Set the Use-core-clock as the clock source.

3.2 Clear reset flag (RMRSTF)

Description

Execute the write RCC_CTRLSTS register RMRSTF bit opertation(clear the reset flag) will affect the RCC_BDCTRL register value.

Workaround

None.

Note

Reconfigure LSE enable and reselect RTC clock source.

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4 GPIO and AFIO

4.1 SPI NSS pin

Description

When the SPI is in the NSS software mode (SSMEN=1, SSEL=0), if the corresponding NSS pin is not utilized by the SPI and is configured in a multiplexed mode, then the NSS pin can only be used as the NSS for SPI and cannot be multiplexed for other functions.

Workaround

None

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

5 Analog/Digital Conversion (ADC)

5.1 ADC data left-align

Description

ADC single conversion mode, non-12bit precision and left aligned, the software triggers the conversion rule channel, in the ADC_DAT register, the highest invalid bit is 1.

Workaround

Retain only valid data bits or use right-aligned mode.

5.2 ADC analog watchdog

Description

When the ADC works in independent mode and converts once and the accuracy is not 12bit, the analog watchdog function is enabled, and the software triggers the conversion rule channel/injection channel. The effective bits of the analog watchdog high threshold value are set equal to the value of the ADC data register. When the invalid bits are all 0, the analog watchdog may be triggered by mistake.

Workaround

In this case, the highest position 1 of the invalid bit of the simulated watchdog high threshold is not triggered.

5.3 ADC injection channels trigger regular channel conversions

Description

When the software triggers the injection channel conversion, the regular channel conversion may be started. As a result, data is generated in ADC_DAT, and the corresponding status bit of ADC_STS regular channel conversion will be set.

Workaround

Flag bits and data generated by regular channels are ignored.

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Email: sales@nsing.com.sg

5.4 The master ADC conversion is started under the influence of the slave ADC conversion

Description:

ADC works in dual ADC mode and synchronous injection mode. Only the software triggers the regular channel conversion of the primary ADC, the regular channel conversion of the secondary ADC, and the lower 16 bits from ADC_DAT are merged into the higher 16 bits of the primary ADC_DAT

Workaround:

None

5.5 Adjacent ADC data registers are affected

Description:

Independent working mode, software triggers ADC4/2 regular channel conversion, ADC4/2 DAT register 16 bits lower content will be merged into ADC3/1 DAT register 16 bits higher.

Workaround:

None

5.6 Read ADC data register ADC_DAT (ADC_JDATx) value exception issue after the ADC ENDC (or JENDC) flag is set

Description

When the regular sequence conversion completion flag ENDC (injection sequence conversion completion flag JENDC) is set, the ADC Data Register ADC_DAT (ADC_JDATx) is read immediately, possibly with the result of the previous conversion.

Resolution

1. When the ENDC/JENDC flag is set, delay 2 ADC_CLK clocks before reading the ADC data registers (ADC_DAT/ADC_JDATx);

2. In some scenarios, use the any regular channel conversion completion flag ENDCA (any injection channel conversion completion flag JENDCA) flag instead of the ENDC (JENDCA)

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

6 Serial Peripheral Interface (SPI)

6.1 SPI interface

6.1.1 SPI baud rate setting

Description

When the baud rate control bit (BR[2:0]) is set to fPLCK/2 in SPI master mode, CRC check will fail.

Workaround

In this case, avoid setting baud rate control bit (BR[2:0]) to fPLCK/2.

6.1.2 CRC check from mode

Description

The SPI operates in slave mode and CRC verification is enabled. Even if the NSS pin is high, CRC calculations are performed whenever the SPI receives a clock signal

Workaround

Before using THE CRC check, clear the CRC data register to synchronize the CRC check between the primary and secondary devices

The clearing steps are as follows:

1. Reset the SPI enable bit (set 0)
2. Reset the CRC check bit (set 0)
3. Reset the CRC check bit (set 1)
4. Set the SPI enable bit (set 1)

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

6.2 I2S interface

6.2.1 PCM long frame mode

Description

When the I2S work in master mode, PCM long frame mode, and the data format is “32bit” or “16bit extended to 32bit”, the WS signal is cycles every 16bit instead of 32bit.

Workaround

When I2S is in master mode and long frame mode must be used, 16bit data mode should be used.

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

7 I2C interface

7.1 Software events that must be managed before the current byte transfer

Description

When EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3 events occur, the events must be processed before the current byte is transferred. Otherwise, one more byte may be read, duplicate data may be read, or data may be lost.

If the data N-1 is not read by the software before the stop signal is generated, the data N in the shift register is corrupted (moved one bit to the left).

Workaround

1. Use DMA when transferring more than one byte using I2C
2. When using I2C interrupts, the interrupt priority is set to the highest priority of the application
3. When the read data reaches the N-1 byte:

a) Check BSF is 1

b) Set SCL to GPIO open miss output and set it to 0

c) Set STOPGEN to 1

d) Read the N-1 byte

e) Set SCL to open/miss output mode for I2C multiplexing

f) Read the last byte

7.2 Considerations when reading single or double bytes at a time

Description

In host read mode, data read errors may occur when the bytes read are single or double bytes.

Workaround

1. Single byte reading:

a) Upon receipt of ADDRF

b) Set the ACKEN bit to 0

c) Clear the ADDRF bit (by reading STS1 and then STS2)

d) Set STOPGEN to 1

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Email: sales@nsing.com.sg

e) Read one byte of data.

2. Double-byte read:

a) Upon receipt of ADDRF

b) Set the ACKPOS bit to 1

c) Clear the ADDRF bit (by reading STS1 and then STS2)

d) Set the ACKEN bit to 0

e) The BSF level was 1

f) Set STOPGEN to 1

g) Read two bytes of data in a row

7.3 Use DMA in conjunction with other peripherals

Description

If other peripherals are using the same DMA controller during DMA communication, I2C communication will be abnormal

Workaround

1. Use different DMA controllers.
2. I2C turns off DMA for other peripherals during DMA communication.

7.4 STOP establishment time exceeds minimum threshold in standard mode

Description

In master mode: At a communication rate of 100K, triggering the slave's clock extension results in a STOP establishment time less than 4μs.

Workaround

Recommend reducing the communication rate to 50K or below based on the slave peripheral's timing requirements.

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

8 Universal Synchronous asynchronous Receiver (USART)

8.1 Check error flag

Description

During the receipt of a byte of data, a checksum error is detected before the stop bit is received, and the checksum error flag bit is set, during which the checksum error flag bit cannot be cleared by software (read status register, read data register again).If checksum interrupt is enabled, the checksum interrupt handler will be entered several times.

Workaround

The read buffer flag bit is set, and the error flag bit operation is performed after the data is received.

If checksum error interrupt is enabled, to avoid entering the interrupt processing function for multiple times, the checksum error interrupt is disabled when entering the checksum error interrupt for the first time. After receiving data, the checksum error interrupt is enabled again.

8.2 RTS hardware flow control

Description

When the RTS hardware flow control is enabled, the USART receives a frame of data. When the first byte of data is received, the RTS signal is automatically pulled up. If the first byte of data is not read out of the data register in time, the RTS signal is pulled down again after the next byte of data is received, and the USART waits for the next frame of data to be received.

Workaround

Read the data from the data register in time before receiving the next new data.

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

9 Debug Interface (DBG)

9.1 The Debug registers

Description

The DBGMCU_IDCODE debug register can only be accessed in debug mode (not by user programs), and the value returned by reading in user mode is 0xFF.

Workaround

Avoid using IDCODE in user applications.

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

10 Timer (TIM)

10.1 The timer repeats capture detection

Description

When an input capture is generated, if a new input capture is generated during reading of the TIMx_CCDATx (capture/compare register X) (the read operation automatically clears the capture flag bit), CCxOCF(capture/compare X repeat capture flag) may still be set.

Workaround

None

10.2 The issue of switching from another mode to 100% or 0% duty cycle PWM mode

Description

When switching from other mode(except frozen mode) to PWM1/2 mode, if the PWM duty cycle is set to 100% or 0%, the mode switch to PWM1/2 mode fail, if reconfig the PWM duty (not 0% or 100%), the mode switch to PWM1/2 mode success.

Workaround

When switching from forced active/forced inactive/set channel x to the active level on match/ set channel x to the inactive level on match mode to PWM1/2 mode with a 100% or 0% duty cycle, modify CCxP to achive the PWM with 100% or 0% duty.

When switching from toggle mode to PWM1/2 mode with a 100% or 0% duty cycle, have no solution.

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Address: 20 Science Park, #03-15/16
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Email: sales@nsing.com.sg

11 Real Time Clock (RTC)

11.1 RTC prescaler

Description

The RTC asynchronous prescaler coefficient and the synchronous prescaler coefficient cannot be set to 0, otherwise it will easily cause the RTC pre-allocation to fail.

Workaround

Avoid setting the DIVA[6:0](asynchronous pre-band) and DIVS[14:0](synchronous pre-band) registers of TRC_PRE to 0.

11.2 RTC calibration

Description

If DIVA is not 128/64/32/16/8 during RTC automatic calibration (RTC_CALIB register CP position 1), the RTC automatic calibration will not succeed.

Workaround

If RTC automatic calibration is required, the DIVA coefficient should be 128/64/32/16/8.

11.3 RTC clock

Description

If NRST reset occurs during RTC operation, RTC timing will be suspended during the reset.

Workaround

None

11.4 RTC wake up

Description

The RTC module cannot wake-up periodically in Standby mode.

Workaround

Use RTC alarm to wake-up Standby mode.

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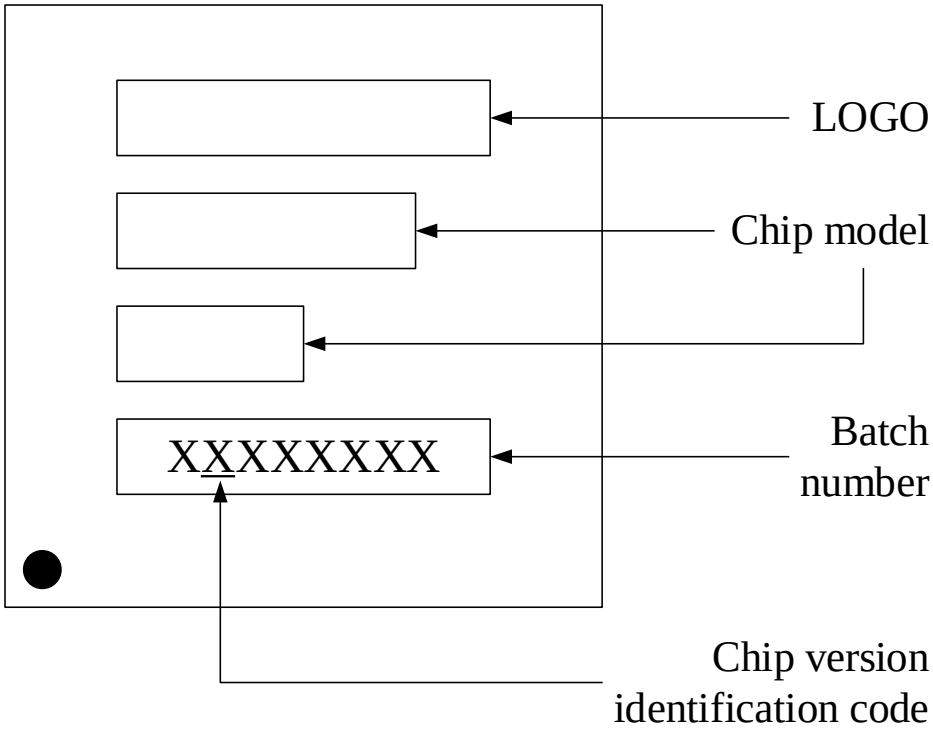
Email: sales@nsing.com.sg

12 Chip screen printing and version description



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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

13 Version history

Date	Version	Modify
2024.11.21	V1.1.0	1. The initial release
2025.06.06	V1.2.0	1. Add section 10.2
2025.09.18	V1.3.0	1. Add section 7.4 2. Modify section 10.2

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

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Email: sales@nsing.com.sg