

N32H482xE/xG

Product Brief

N32H482 series adopts a 32-bit ARM Cortex-M4F core, with a maximum operating frequency of 240MHz, supporting floating-point unit and DSP instructions. It integrates up to 512-KB embedded flash, 192-KB SRAM (including 32-KB CCM SRAM), and 4-KB Backup SRAM. It also integrates 4x 12bit 4.7Msps ADCs, 2x 12bit DAC, USB FS Device, USB HS DualRole, U(S)ART, I2C, SPI, CAN-FD, and other communication interfaces. It supports SDIO, FEMC, xSPI high-speed storage interfaces, I2S audio interface, multiple advanced control timers, general timers, basic timers, low-power timers. It also features a built-in hardware acceleration engine for cryptographic algorithms, supporting AES/TDES, SHA, SM3, SM4, MD5 algorithms, TRNG true random number generator, and CRC16/32.

Key features

CPU Core

- 32-bit ARM Cortex-M4F + FPU, single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
- Built-in 8-KB instruction Cache supporting Flash acceleration unit for zero-wait program execution
- Frequency up to 240 MHz, 300 DMIPS

Memories

- 512-KByte of embedded Flash memory with ECC
 - ◆ Supports encryption, multi-user partition and data protection
 - ◆ 10,000 erase/write cycles and 10-years data retention
- 512-KByte sFlash memory(only for N32H482VGL7), Supports 100,000 erase/write cycles and 20-years data retention
- 160-KByte of general SRAM with hardware parity checking
- 32-KByte of CCM SRAM with ECC, defaults to general SRAM after power-up, configurable as CCM SRAM
- 4-KByte of Backup SRAM with ECC available in Standby mode

Power Modes

- Run mode: 45 mA/MHz@240 MHz (peripherals off, 3.3 V@25°C)
- Stop0 mode: SRAM and all registers can be configured to retention, RTC run
- Standby mode: 6uA, all backup registers and Backup SRAM retained, all IOs retained, optional RTC run
- VBAT mode: 4uA, all backup registers and Backup SRAM retained, optional RTC run

Clock

HSE: 4MHz~32MHz high-speed external crystal oscillator



- LSE: 32.768KHz low-speed external crystal oscillator
- Built-in multiple high speed PLLs
- MCO: Supports 2-channel clock outputs, which can be configured independently as clock output
- HSI: High-speed internal RC 8MHz, -1.5% to +2% accuracy (full temperature range)
- LSI: Low-speed internal RC 32KHz, +/-10% accuracy (full temperature range)

Reset

- Supports power-on/brown-out/external pin reset
- Supports watchdog reset
- Supports programmable voltage detection

GPIOs

Up to 118 GPIOs

Communication Interfaces

- 1x USB2.0 FS Device interface, built-in PHY, supports crystal-less mode
- 6x SPI interfaces, 2x I2S interfaces, support half/full duplex mode, multiplexed with SPI interfaces
- U(S)ART interfaces
 - ◆ 4x USART interfaces (support ISO7816, IrDA, LIN)
 - ◆ 4x UART interfaces
 - ◆ TX/RX of USART3/UART5/UART8 can be mapped to all pins
- 4x I2C interfaces(Master/Slave) with speed up to 1 MHz where slave mode support dual address response
- 2x CAN-FD bus interface, TX/RX can be mapped to all pins

• High Performance Analog Interfaces

- 4x 12bit ADCs with 4.7Msps
 - ◆ Multiple precision configuration, support 12-bit, 10-bit, 8-bit, 6-bit sampling precision, resolution up to 16-bit with hardware oversample
 - ◆ Up to 16 external single-ended input channels, 3 internal single-ended input channels, support differential mode and single-ended mode
- 2x 12bit DAC with 1Msps sampling rate
 - ◆ Each DAC support 1 internal output channel and 1 external output channel
 - Support output channel buffered/unbeffered modes, supports internal output, external output, and simultaneous internal and external output.
- 1x temperature sensor

High Speed External Memory Interfaces



- 1x xSPI interface, supporting external SRAM, PSRAM and Flash, supporting XIP
- 1x FEMC (Flexible External Memory Controller) interface, supporting external SRAM, PSRAM, NOR Flash and NAND Flash, 8/16-bit data bus width configurable
- 1x SDIO interface, support SD/SDIO/MMC format
- Mathematical hardware accelerator CORDIC for motor control functions
- Built-in filter mathematical accelerator FMAC, supporting FIR, IIR filtering
- DMA Controllers
 - 2x DMA controller
 - Each controller supports 8 channels
 - Channel source address and destination address can be configured arbitrarily

RTC real-time clock

- Supports leap-year calendar, alarm event, periodic wake up
- Supports internal and external clock calibration

Timers

- 3x 16-bit advanced control timers with maximum control precision of 4.16 ns
 - ◆ Support input capture, complementary output, quadrature encoder input etc.
 - ◆ Each timer has 6 independent channels, 4 of which support 4 pairs of complementary PWM output.
- 10x 16-bit general purpose timers (GTIM1~10)
 - ◆ GTIM1~7, with a maximum control precision of 5.56ns, each timer has up to 4 independent channels, each channel supports input capture, output comparison, PWM generation, and single-pulse mode output.
 - ◆ GTIM8~10, with a maximum control precision of 4.16ns, each timer has up to 4 independent channels, each channel supports input capture, output comparison, PWM generation, and single-pulse mode output, only channel 1 supports complementary output with dead time, supports break input.
- 2x 32-bit basic timers
- 2x 16-bit low-power timer, can operate in Stop0 and Standby mode.
- 1x 24-bit SysTick timer.
- 1x 14-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)

Programming Methods

- Support SWD/JTAG debugging interface.
- Support UART and USB Bootloader

Security Features

Flash encryption, multi-user partition management unit (SMPU)



- Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Built-in hardware acceleration engine for cryptographic algorithm
- Supports AES/TDES, SHA, SM3, SM4, and MD5 algorithms
- True random number generator(TRNG)
- CRC16/32 operation
- Supports secure boot, program encryption download, secure firmware update
- Supports external clock failure detection, anti-tamper detection.

• 96-bit UID and 128-bit UCID

Operating Conditions

- Operating voltage range: 1.8V~3.6V
- Operating temperature range: -40° C $\sim 105^{\circ}$ C
- ESD: ±4KV (HBM model), ±1KV (CDM model)
- EFT: VDD (+/-4KV, level A), I/O (+/-2KV, level A)

Packages

- LQFP64($10\text{mm} \times 10\text{mm}$)
- LQFP100(14mm \times 14mm)
- LQFP144(20mm × 20mm)

Ordering Information

Reference	Part Number
N32H482xE	N32H482REL7, N32H482VEL7, N32H482ZEL7, N32H482VGL7



1 Ordering Information

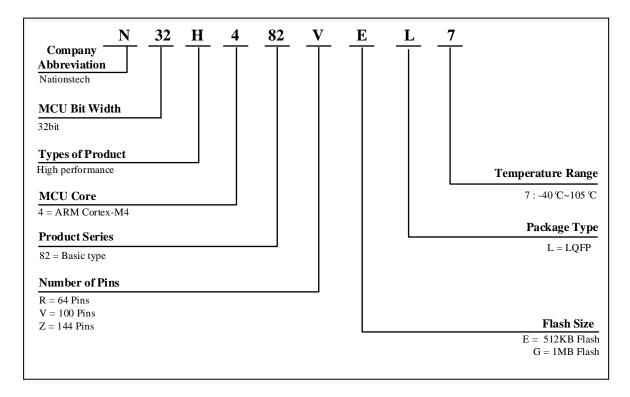


Table 1-1 N32H482 Series Ordering Code

Table 1-1 (5211402 Series Ofdering Code					
Ordering Code ⁽¹⁾	Package	Size	Packaging ⁽²⁾	$SPQ^{(3)}$	Temperature range
N32H482REL7	LQFP64	10mm x 10mm	Tray	160	-40°C ~105°C
N32H482VEL7	LQFP100	14mm x 14mm	Tray	90	-40℃~105℃
N32H482VGL7	LQFP100	14mm x 14mm	Tray	90	-40℃~105℃
N32H482ZEL7	LQFP144	20mm x 20mm	Tray	60	-40°C ~105°C

- 1. For the latest detailed-ordering information, please refer to the Selection Guide.
- 2. The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
- 3. Minimum packaging quantity.



2 Product Configurations

Table 2-1 N32H482 Series Product Configuration

Device		N32H482REL7	N32H482VEL7	N32H482VGL7	N32H482ZEL7	
Operating Condition		1.8~3.6V/-40~105°C				
CPU Frequency		ARM Cortex-M4F @240MHz, 300DMIPS				
eFlash Capacity (KB) (2)		512	512	512	512	
sFlash Capac	city (KB) (3)			512		
Total SRAM	General SRAM	160				
(KB)	CCM SRAM ⁽¹⁾	32				
(KD)	Backup SRAM	4				
	ATIM	3*16bit				
	GTIM		7*16	bit		
	GIIM		3*16	pit ⁽⁴⁾		
	BTIM	2*32bit				
Timers	LPTIM	2*16bit				
	SysTick timer	1				
	WWDG	1*14bit				
	IWDG	1*12bit				
	RTC	Yes				
	SPI/I2S	5/2		6/2		
	I2C	4				
	USART	4				
Communication	UART	4				
Interface	USB FS Device	Yes				
	USB HS DualRole	Yes				
	FDCAN	2				
	XSPI	Yes				
Memory Expansion	FEMC	No	Ye	S ⁽⁵⁾	Yes	
	SDIO	Yes				
GP	IO	54	8	5	118	
WKUI	P Pins	4	4	5	5	
DMA			2			
Number of channels		16Channel				
12bit ADC		4	2	1	4	
Number of channels		26Channel	42Ch	annel	51Channel	
12bit DAC		2				
Number of channels		2 External				
Algorithm	n Support	DES/3DES、AES、SHA1/SHA224/SHA256、SM3、SM4、MD5、CRC16/CRC32				





TRNG	Yes		
Cordic	Yes		
FMAC	Yes		
Security Protection	Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot		
Package	LQFP64	LQFP100	LQFP144

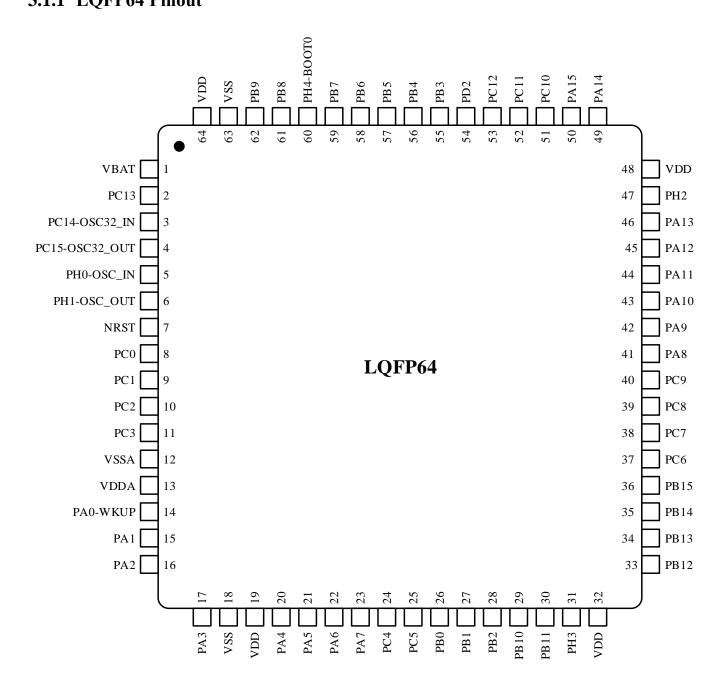
Notes:

- (1) CCM SRAM is powered up as general SRAM by default, and users can configure it as CCM SRAM.
- (2) eFlash: embedded Flash
- (3) sFLASH: SIP Flash, XSPI interface closed, only supported by N32H482VGL7. sFLASH is connected to MCU as follows:
 - a) CS# of sFLASH connects to PF0(XSPI_NSS1) of MCU;
 - b) CLK of sFLASH connects to PG13(XSPI_CLK) of MCU;
 - c) DI/IO0 of sFLASH connects to PF2(XSPI_IO0) of MCU;
 - d) DO/IO1 of sFLASH connects to PF3(XSPI_IO1) of MCU;
 - e) WP# of sFLASH connects to PF4 of MCU, HOLD# of sFLASH connects to PF5 of MCU.
- (4) Supports break input, Channel 1 supports complementary channel output.
- (5) Only supports address bus and data bus multiplexing.



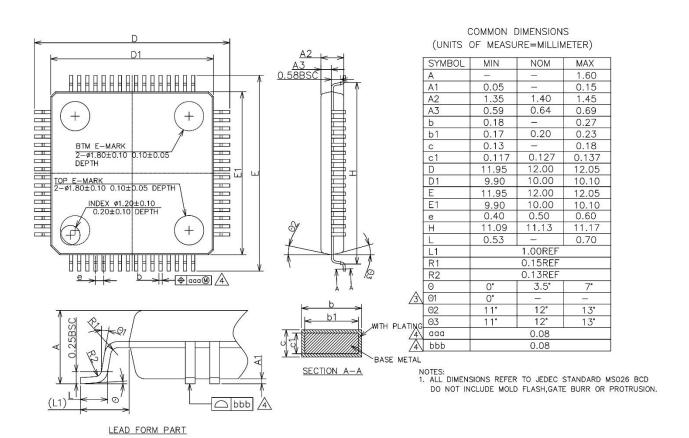
3 Package

3.1 LQFP643.1.1 LQFP64 Pinout





3.1.2 LQFP64 Package

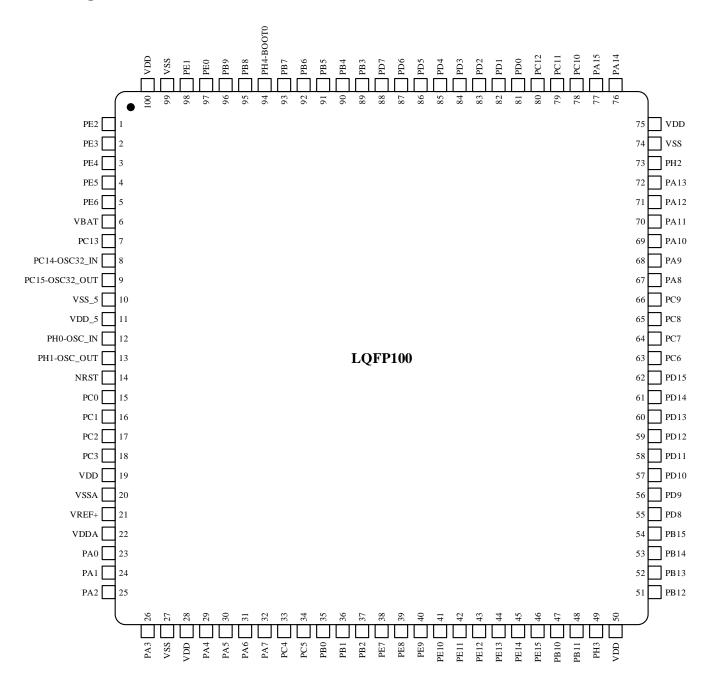


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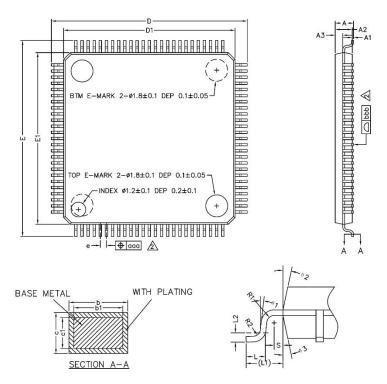
3.2 LQFP100

3.2.1 LQFP100 Pinout





3.2.2 LQFP100 Package



COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	Α		-	1.60
	A1	0.05	1-1	0.15
	A2	1.35	1.40	1.45
	A3	0.59	0.64	0.69
	Ь	0.17	_	0.27
3	b1	0.17	0.20	0.23
	С	0.13		0.18
	c1	0.12	0.127	0.134
	D	15.80	16.00	16.20
	D1	13.90	14.00	14.10
	E	15.80	16.00	16.20
	E1	13.90	14.00	14.10
3	е	0.50BSC		
	L	0.45	0.60	0.75
	L1		1.00REF	
	L2		0.25BSC	
	R1	0.08	_	
	R2	0.08	_	0.20
	s 0	0.20		6_3
3	θ	0.	3.5°	7° -
	0 1	0.	=	
	θ 2 θ 3	11°	12°	13°
	θ 3	11°	12°	13°
2	aaa	0.08		
2	bbb	0.08		

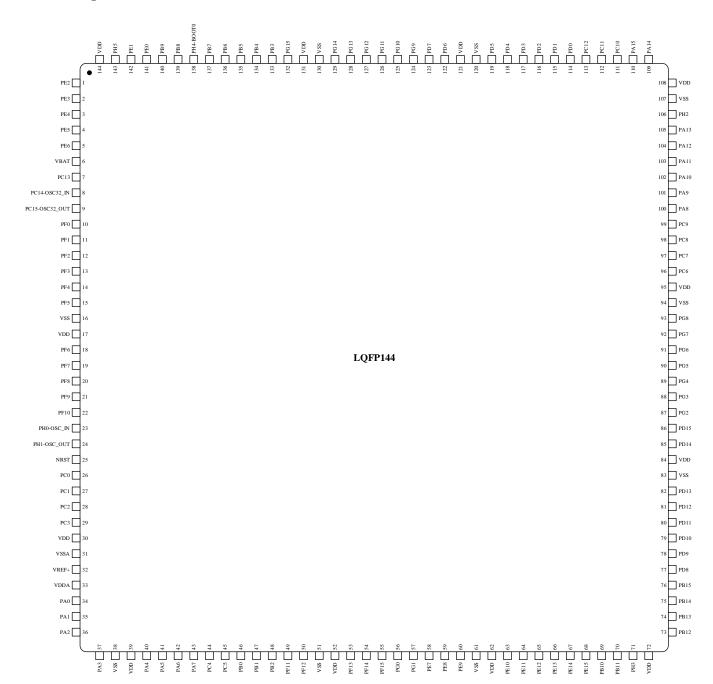
NOTES:

ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BED DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.



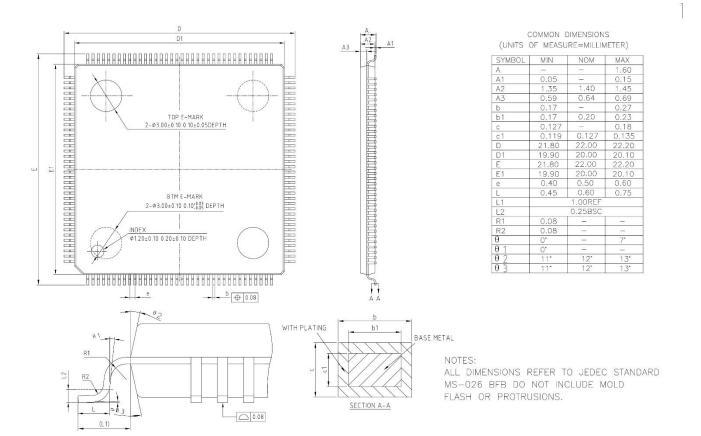
3.3 LQFP144

3.3.1 LQFP144 Pinout





3.3.2 LQFP144 Package





4 Version History

Version	Date	Changes	
V1.0.0	2024.11.12	Initial release.	
V1.1.0	2025.5.9	1. Add N32H482VGL7 model number	



5 Disclaimer

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