N32H481xE Datasheet

N32H481 series adopts a 32-bit ARM Cortex-M4F core, with a maximum operating frequency of 240MHz, supporting floating-point unit and DSP instructions. It integrates up to 512-KB embedded flash, 192-KB SRAM (including 32-KB CCM SRAM), and 4-KB Backup SRAM. It also integrates 4x 12bit 4.7Msps ADCs, 2x 12bit DAC, USB HS DualRole, U(S)ART, I2C, SPI, and other communication interfaces. It supports xSPI high-speed storage interfaces, I2S audio interface, multiple advanced control timers, general timers, basic timers, low-power timers. It also features a built-in hardware acceleration engine for cryptographic algorithms, supporting AES/TDES, SHA, SM3, SM4, MD5 algorithms, TRNG true random number generator, and CRC16/32.

Key Features

- **CPU Core**
  - 32-bit ARM Cortex-M4F + FPU, single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
  - Built-in 8-KB instruction Cache supporting Flash acceleration unit for zero-wait program execution
  - Frequency up to 240 MHz, 300 DMIPS
- **Memories**
  - 512-KByte of embedded Flash memory with ECC
    - Supports encryption, multi-user partition and data protection
    - 10,000 erase/write cycles and 10-years data retention
  - 160-KByte of general SRAM with hardware parity checking
  - 32-KByte of CCM SRAM with ECC, defaults to general SRAM after power-up, configurable as CCM SRAM
  - 4-KByte of Backup SRAM with ECC available in Standby mode
- **Power Modes**
  - Run mode: 48 mA/MHz@240 MHz (peripherals off, 3.3 V@25°C)
  - Stop0 mode: SRAM and all registers can be configured to retention
  - Standby mode: 22uA, all backup registers and Backup SRAM retained, all IOs retained, optional RTC run
- **Clock**
  - HSE: 4MHz~32MHz high-speed external crystal oscillator
  - Built-in multiple high speed PLLs
  - MCO: Supports 2-channel clock outputs, which can be configured independently as clock output
  - HSI: High-speed internal RC 8MHz, -1.5% to +2% accuracy (full temperature range)
  - LSI: Low-speed internal RC 32KHz, +/-10% accuracy (full temperature range)
- **Reset**
  - Supports power-on/brown-out/external pin reset
  - Supports watchdog reset
  - Supports programmable voltage detection
- **GPIOs**

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- Up to 56 GPIOs

- **Communication Interfaces**
  - 1x USB HS DualRole interface, built-in PHY
  - 6x SPI interfaces, 2x I2S interfaces, support half/full duplex mode, multiplexed with SPI interfaces
  - U(S)ART interfaces
    - 3x USART interfaces (support ISO7816, IrDA, LIN)
    - 4x UART interfaces
    - TX/RX of USART3/UART5/UART8 can be mapped to all pins
  - 4x I2C interfaces(Master/Slave) with speed up to 1 MHz where slave mode support dual address response
- **High Performance Analog Interfaces**
  - 4x 12bit ADCs with 4.7Msps
    - Multiple precision configuration, support 12-bit, 10-bit, 8-bit, 6-bit sampling precision, resolution up to 16-bit with hardware oversample
    - support differential mode and single-ended mode, 4 ADCs support a total of 47 external channels
  - 2x 12bit DAC with 1Msps sampling rate
    - Each DAC support 1 internal output channel and 1 external output channel
    - Support output channel buffered/unbeffered modes, supports internal output, external output, and simultaneous internal and external output.
  - 1x temperature sensor
- **High Speed External Memory Interfaces**
  - 1x xSPI interface, supporting external SRAM, PSRAM and Flash, supporting XIP
- **DMA Controllers**
  - 2x DMA controller
  - Each controller supports 8 channels
  - Channel source address and destination address can be configured arbitrarily
- **RTC real-time clock**
  - Supports leap-year calendar, alarm event, periodic wake up
- **Timers**
  - 3x 16-bit advanced control timers with maximum control precision of 4.16 ns
    - Support input capture, complementary output, quadrature encoder input etc.
    - Each timer has 4 independent channels, ATM1 supports 4 pairs of complementary PWM outputs, ATM2 and ATIM3 support 3 pairs of complementary PWM outputs.
  - 10x 16-bit general purpose timers (GTIM1~10)

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- GTIM1~7, with a maximum control precision of 5.56ns, each timer has up to 4 independent channels, each channel supports input capture, output comparison, PWM generation, and single-pulse mode output.
- GTIM8~10, with a maximum control precision of 4.16ns, each timer has up to 4 independent channels, each channel supports input capture, output comparison, PWM generation, and single-pulse mode output, only channel 1 supports complementary output with dead time, supports break input.

- 2x 32-bit basic timers
- 2x 16-bit low-power timer, can operate in Stop0 and Standby mode.
- 1x 24-bit SysTick timer.
- 1x 14-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)

- **Programming Methods**
  - Support SWD/JTAG debugging interface.
  - Support UART Bootloader
- **Security Features**
  - Flash encryption, multi-user partition management unit (SMPU)
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Built-in hardware acceleration engine for cryptographic algorithm
  - Supports AES/TDES, SHA, SM3, SM4, and MD5 algorithms
  - True random number generator(TRNG)
  - CRC16/32 operation
  - Supports secure boot, program encryption download, secure firmware update
  - Supports external clock failure detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
  - EFT: VDD (+/-4KV，level A)，I/O (+/-2KV，level A)
- **Packages**
  - LQFP64(7mm × 7mm)

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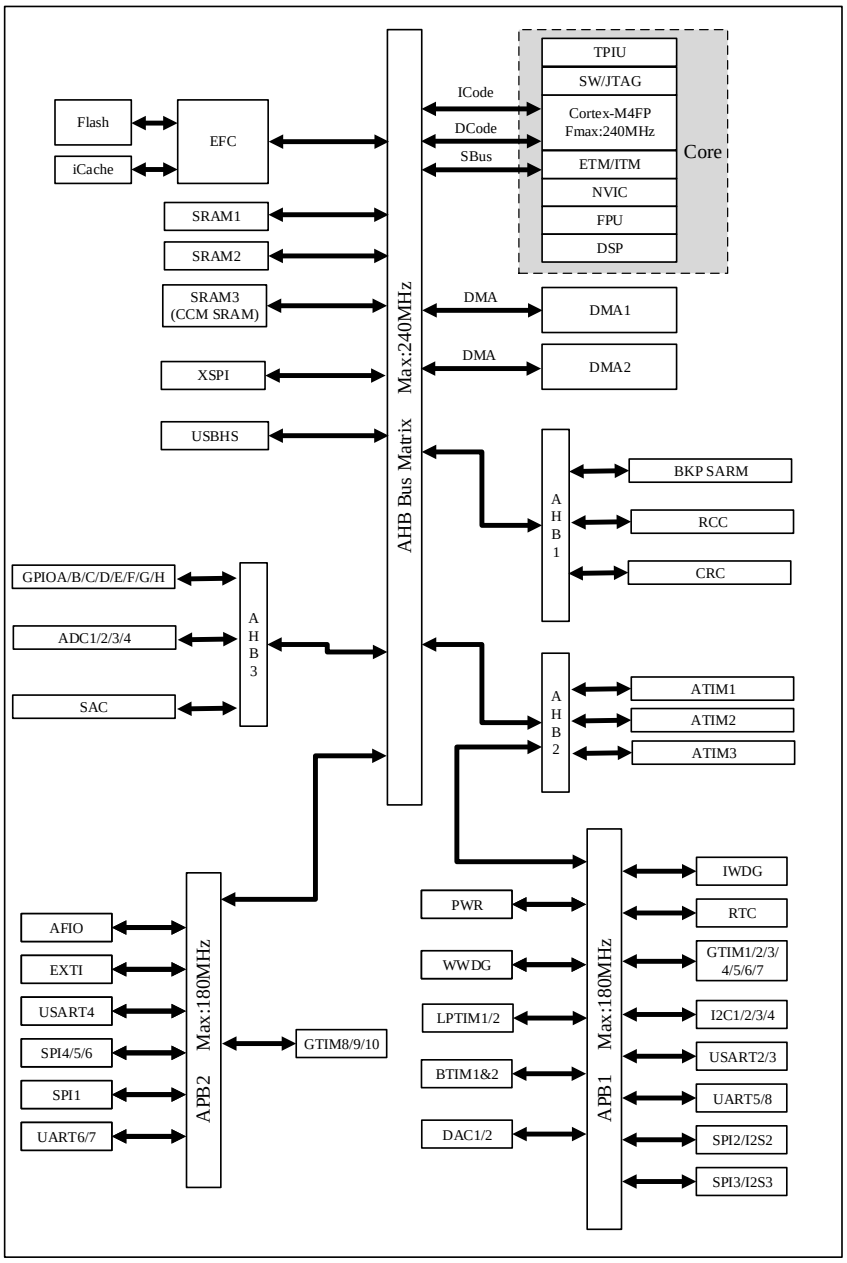
1 Introduction

The N32H481 microcontrollers series features a high-performance 32-bit ARM Cortex™-M4F core with an integrated floating point operation unit (FPU) and digital signal processing (DSP). It operates at a frequency of up to 240MHz. It integrates up to 512-KB embedded flash, 192-KB SRAM (including 32-KB CCM SRAM), and 4-KB Backup SRAM. It also integrates 4x 12bit 4.7Msps ADCs, 2x 12bit DAC, USB HS DualRole, U(S)ART, I2C, SPI, and other communication interfaces. It supports high-speed storage interfaces like xSPI , as well as I2S audio interface, The microcontroller feture multiple advanced control timers, general timers, basic timers, low-power timers. It also features a built-in hardware acceleration engine for cryptographic algorithms, supporting AES/TDES, SHA, SM3, SM4, MD5 algorithms, along with a TRNG true random number generator, and CRC16/32.

The N32H481 series products can operates reliably in the temperature range of -40 ℃ to +105 ℃ and supply voltage from 1.8V to 3.6V. It offers multiple power modes to cater to low-power applications.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32H481 Series Block Diagram



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1.1 Product Configurations

Table 1-1 N32H481 Series Product Configuration

Device		N32H481REL7K
Operating Condition		1.8~3.6V/-40~105℃
CPU Frequency		ARM Cortex-M4F @240MHz, 300DMIPS
eFlash Capacity (KB)		512
Total SRAM (KB)	General SRAM	160
	CCM SRAM(1)	32
	Backup SRAM	4
Timers	ATIM	3*16bit
	GTIM	7*16bit 3*16bit(2)
	BTIM	2*32bit
	LPTIM	2*16bit
	SysTick timer	1
	WWDG	1*14bit
	IWDG	1*12bit
	RTC	Yes
Communication Interface	SPI/I2S	6/2
	I^2C	4
	USART	3
	UART	4
	USB HS DualRole	1
Memory Expansion	XSPI	1
GPIO WKUP Pins		56 4
DMA Number of channels		2 16Channel
12bit ADC Number of channels		4 47Channel(3)
12bit DAC Number of channels		2 2 External
Algorithm Support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM3、SM4、MD5、CRC16/CRC32
TRNG		Yes
Security Protection		Read-write protection (RDP/WRP), storage encryption, partition protection, secure
Package		LQFP64

Notes:

(1) CCM SRAM is powered up as general SRAM by default, and users can configure it as CCM SRAM.

(2) Supports break input, Channel 1 supports complementary channel output.

(3) 2 ADCs multiplexed with OSC_IN and OSC_OUT, 2 ADCs multiplexed with USB_HS_DP and USB_HS_DM, 14 channels in ADC1, 16 channels in ADC2, 19 channels in ADC3, 18 channels in ADC4.

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2 Functional Overview

2.1 Processor Core

The N32H481 series integrates the ARM Cortex™-M4F processor. It features a floating-point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 300 DMIPS. At the same time, its efficient signal processing capabilities combined with low power consumption, low cost, and ease of use advantages of the Cortex-M series processors. Make it suitable for applications that need a mix of control and signal processing capabilities in an easy-to-use manner.

The ARM Cortex™-M4F 32-bit reduced instruction set processor offers outstanding code efficiency.

2.2 Memories

The N32H481 series includes embedded encrypted Flash memory and embedded SRAM. The following diagram shows the memory address mapping.

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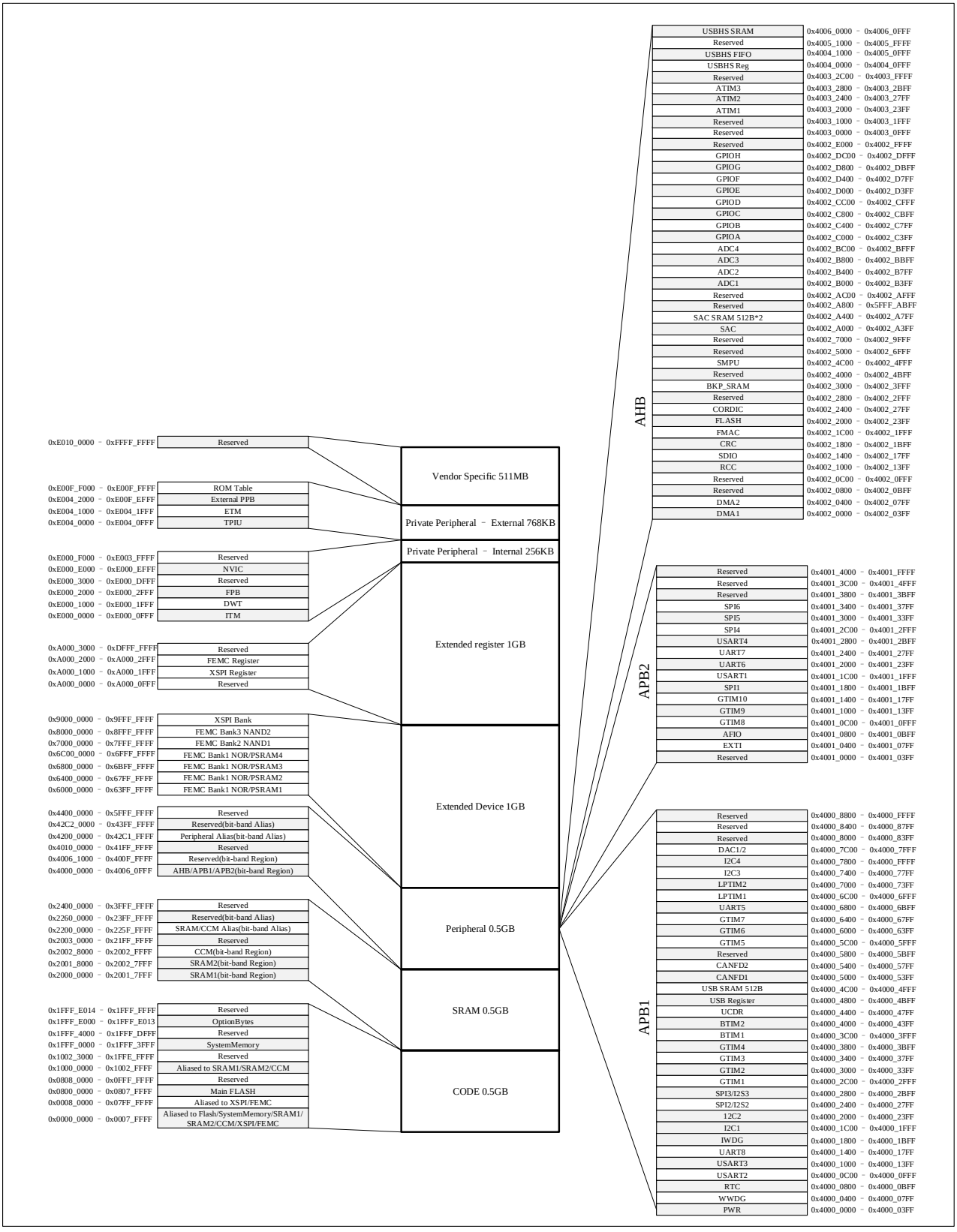
Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

The integrated encrypted Flash memory size is up to 512 Kbytes, utilized for storing programs and data. The page

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size is 8Kbytes, supporting page erasing, double-word writing, word reading, half-word reading, and byte reading operations.

It supports storage encryption protection, enabling automatic encryption during writing and automatic decryption during reading (including program execution operation).

User partition management is supported, allowing for a maximum of 3 user partitions, different users cannot access each other's data (only executable code can be accessed).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 192 Kbytes (including 160 Kbytes general SRAM and 32 Kbytes CCM SRAM) and a Backup SRAM of 4 Kbytes, as follows:

General SRAM has a maximum size of 160 Kbytes, supporting parity check.

CCM SRAM has a size of 32 Kbytes, powered up as general SRAM by default, can be configurable as CCM SRAM, supporting ECC.

BKP SRAM has a size of 4 Kbytes, can retain data in Standby mode, supporting ECC.

2.2.3 Nested Vector Interrupt Controller (NVIC)

Main features:

- Up to 102 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M4F)
- 16 programmable priority levels (four bits of interrupt priority used)
- Low-latency exception and interrupt handling
- Power management control
- Implementation of system control registers

The NVIC and the processor core interface are closely coupled, enabling low-latency interrupt processing and efficient processing of late arriving interrupts. All interrupts, including the core exceptions, are managed by the NVIC.

2.3 Extended Interrupt/Event Controller (EXTI)

The extended interrupt/event controller contains 24 edge detectors used for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. The pending register holds interrupt requests for the status lines, and the interrupt requests can be cleared by writing '1' to the corresponding bit in the pending register.

2.4 Clock System

The device offers various clock options for users to choose from, including:

- High speed internal RC oscillator (HSI) at 8 MHz
- Low speed internal RC oscillator (LSI) at 32 KHz
- High speed external crystal oscillator (HSE) ranging from 4 MHz to 32 MHz.

The system clock source can be selected from HSI, HSE, PLL, SHRTPLL, USBHS240M. Upon reset, the internal MSI clock is set as the default system clock, user can choose the external HSE clock with fail monitoring capabilites. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI. If interrupts are enabled, software can receive corresponding interrupts.

Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. The AHB has a maximum frequency of 240 MHz, APB2 has a maximum frequency of 180 MHz and APB1 has a maximum frequency of 180 MHz.

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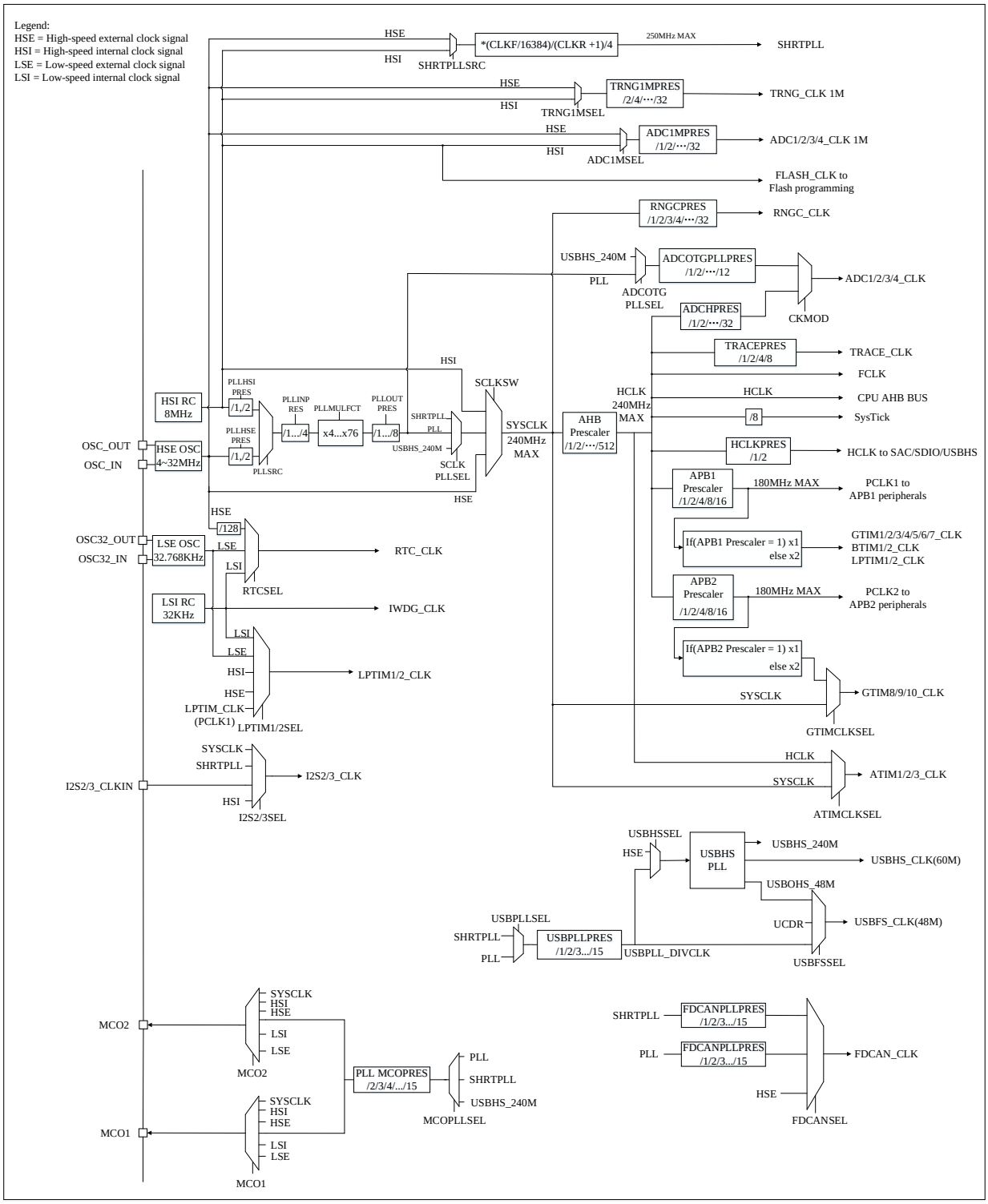
Refer to the clock tree diagram below.

Figure 2-2 Clock Tree



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2.5 Boot Modes

During startup, the BOOT mode after reset can be selected through the BOOT0 pin and option byte for BOOT configuration:

- Boot from Main Flash memory, including booting from the front bank (0x0800_0000) and rear bank (0x0804_0000) of Main Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader is stored in the system memory and can program the flash memory through USB interface.

Address remapping for physical address 0 can also be achieved by configuring RCC_BOOTREMAP.REMAPSEL[2:0]:

- Boot from xSPI external memory through remap

2.6 Power Supply Scheme

There are three external power supplies: VDD, VDDA, VREF. Among them, VDD is the chip power supply, mainly for the power supply system and clock system; VDDA is the analog peripheral power supply, mainly for the analog peripherals; VREF provides a reference power supply for the analog peripherals to provide higher accuracy.

There are five power domains, powered by external power supplies for different power domains:

- V_{DD} domain: 1.8 to 3.6V, mainly powering for MR, most GPIOs, HSE, HSI, PLL, POR/PDR, BOR, PVD, and USB PHY
- V_{DDA} domain: 1.8 to 3.6V, mainly powering for ADC, DAC, TS, etc.
- V_{DDBK} domain: 1.8 to 3.6V, mainly powering for WKUP pin, NRST, PC13/14/15, LSI, etc.
- V_{DDD} domain: 1.1 V or 0.9 V, mainly powering for CPU, AHB, APB, SRAM, FLASH, RCC, TRNG, and most peripherals
- V_{DDDBK} domain: 0.9 V or 0.8 V, mainly powering for PWR, Backup SRAM (4KB), RTC, LPTIM, WKUP pin, NRST, PC13/14/15, backup IOM, IWDG, and RCC_BDCTRL register.

2.7 Reset

POR and BOR circuits are integrated inside the device. This part of the circuit ensures that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold ($V_{POR/BOR}$), the device goes into reset state without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See **Table 4-6** for values of $V_{POR/PDR}$ and V_{PVD}.

2.9 Low Power Mode

The N32H481 series supports three low-power modes.

- SLEEP mode

In SLEEP mode, only the CPU is stopped, all peripherals remain operational and can wake up the CPU when an interrupt/event occurs.

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- STOP0 mode

STOP0 mode is based on the Cortex-M4F deep sleep mode. Achieves the lowest power consumption, while retaining the content of SRAM and registers. Most clocks in the main power domain are stopped, such as PLL, HSE, HSI.

Wakeup: The device can be woken up from STOP0 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC timestamp, RTC alarm, etc.

- STANDBY Mode

In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator. After entering STANDBY mode, most register contents will be lost, while the contents of backup registers will still be retained. The STANDBY circuitry continues to function.

Wakeup: External reset signal on NRST, IWDG reset, rising/falling edge on the WKUP pin, RTC alarm, RTC timestamp and LPTIM wake-up event can wake up the device from STANDBY mode.

2.10 Direct Memory Access (DMA)

The DMA controller can access the following slaves: Flash, SRAM1, SRAM2, CCM SRAM3, XSPI, CRC, APB1, APB2, ATIM, ADC, DAC.

The DMA controller is controlled by the CPU to perform fast data transfers from source to destination. After configuring, data can be transferred without any CPU intervention. This keeps the CPU resources free for other operations or saves overall system power consumption.

The device integrates two DMA controllers (DMA1, DMA2), each DMA supports eight channels. Each channel is dedicated to servicing memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMAchannels.

The key features are as follows:

- 16 independently configurable channels (requests): Each DMA (DMA1, DMA2) supports 8 channels
- Support memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers
- Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Each DMA channel has a dedicated software priority level (DMA_CHCFGx.PRIOLVL[1:0] bits, corresponding to 4 priority levels) that can be individually configured. Channels with the same priority level will further compare the hardware index (channel number) to determine the final priority (the channel with the lower index number has higher priority).
- Configurable source and destination transfer size (byte, half word, word). Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) and 1 global interrupt flag (set by logical OR of the 3 events) for each channel
- Access to Flash, Sram1, Sram2, CCM Sram3, XSPI, CRC, APB1, APB2, ATIM, ADC, DAC
- Programmable number of data to be transferred: up to 65536
- Support burst transfers, burst length is configurable, can be set to 1/2/3/4/5/6/7/8 units.

2.11 Real Time Clock (RTC)

The RTC consists of continuously running counters integrated with a built-in calendar clock module that provides a perpetual calendar functionality, as well as alarm interrupts and periodic interrupt.

The key features are as follows:

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- The Real-Time Clock (RTC) is an independent BCD (binary-coded decimal) timer/counter
- Software supports daylight saving time compensation
- Programmable periodic automatic wake-up timer.
- Two 32-bit registers containing hours, minutes, seconds, year, month, date, and week day
- One independent 32-bit register containing sub-seconds
- Two programmable alarms
- Two 32-bit registers containing programmed hours, minutes, seconds, year, month, date, and week day
- Two independent 32-bit registers containing programmed sub-seconds
- Digital precision calibration function
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Three configurable filtering and internal pull-up intrusion detection events
- Timestamp functionality
- 20 backup registers that can retain data in low-power mode
- Multiple interrupt/event wake-up sources, including alarm A, alarm B, wake-up timer, timestamp, and tamper event
- As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, SLEEP mode, STOP0 mode)
- The RTC provides various wake-up sources that can wake the MCU from all low-power modes (SLEEP mode, STOP0 mode, and STANDBY mode)

2.12 Timers and Watchdogs

The N32H481 series supports up to 3 advanced timers, 10 general timers, 2 basic timers, 2 low-power timers, as well as 1 independent watchdog timer, 1 window watchdog timer, and 1 SysTick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low-power timer:

Table 2-1 Comparison Of Timer Functions

Timer	Counter resolution	Counter type	Prescaler factor	Capture/compare channels	Complementary outputs
ATIM1~3	16	Up, down, up/down	Any integer between 1 and 65536	4	4(ATIM1) 3(ATIM2/3)
GTIM1~7	16	Up, down, up/down	Any integer between 1 and 65536	4	N
GTIM8~10	16	Up, down, up/down	Any integer between 1 and 65536	4	1
BTIM1~2	32	Up	Any integer between 1 and 65536	0	N
LPTIM1~2	16	Up	1、2、4、8、16、32、64、128	0	N

2.12.1 Basic Timer (BTIM1~2)

Basic timers contain a 32-bit auto-reload counter.

Main features:

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- 32-bit auto-reload up-counting counter
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- Event that generate the interrupt/DMA is as follows:
  - Update event

2.12.2 General-Purpose Timer (GTIM1~7)

The general-purpose timers (GTIM1/GTIM2/GTIM3/GTIM4/GTIM5/GTIM6/GTIM7) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-reload counters (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- GTIMx supports up to 4 channels
- Channel's working modes: PWM output, output compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control

2.12.3 General-Purpose Timer (GTIM8~10)

The general-purpose timers (GTIMx) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. The general-purpose timer features complementary output, dead-time insertion, and break functions. It is suitable for motor control.

Main features:

- 16-bit auto-reload counters (Supports up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler (the prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- GTIMx supports up to 5 channels
- 4 capture/compare channels, operating modes include: PWM output, output compare, one-pulse mode output, input capture
- 1 break input signal supporting digital filtering, used to place the timer's output signal in a safe user-selectable configuration
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event

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  - Input capture
  - Output compare
  - Break input
- Complementary outputs with programmable dead-time
  - For GTIMx, channel 1 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

2.12.4 Advanced Control Timer (ATIM1~3)

The advanced control timers (TIM1 and TIM8) is mainly used for the following purposes: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. Advanced timers have complementary output function with dead-time insertion and bracking functionality, making it suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- ATIMx supports up to 9 channels
- 4 capture/compare channels for:
  - PWM output
  - Output compare
  - One-pulse mode output
  - Input capture
- 2 break input signals supporting digital filtering
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with programmable dead-time
  - For ATIMx, channel 1,2,3,4 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position

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- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

2.12.5 Low Power Timer (LPTIM1~2)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes. LPTIM can run without internal clock source as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extremely low power consumption.

Main features:

- 16-bit up counter
- 3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources:
  - Internal clock source: LSI, HSI, HSE or APB1 clock
  - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for Pulse Counter application)
- 16-bit auto-load register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or one-shot mode counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for glitch filtering
- Configurable output (PWM)
- Configurable IO polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.12.6 SysTick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reload function
- A maskable system interrupt is generated when the counter reaches 0
- Programmable clock source

2.12.7 Watchdog (WDG)

Built-in Independent Watchdog (IWDG) and Window Watchdog (WWDG) timers are used to detect issues caused by software errors. The watchdog timers are highly flexible, enhancing system security and the accuracy of timing control.

Independent watchdog (IWDG)

The Independent Watchdog (IWDG) is driven by the low-speed internal clock (LSI clock) running at 32 kHz. It can continue to operate in the event of a deadlock or MCU freeze. This provides a higher level of security, timing accuracy, and watchdog flexibility. It can resolve system failures caused by software faults through a reset. The IWDG is best suited for applications where the watchdog needs to run as a completely independent process outside the main application but with lower timing accuracy constraints.
When the power control register PWR_CTRL2.IWDGRSTEN is set to '1', a system reset occurs when the IWDG

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counter reaches 0 (if this is set to '0', the IWDG counts but does not trigger a reset).

Main features:

- Independent 12-bit down-counter
- The RC oscillator provides an independent clock source that can operate in SLEEP, STOP0, and STANDBY modes
- Support reset and low-power wake-up
- When the down-counter reaches 0x000, the system resets (if the watchdog is activated)

Window watchdog (WWDG)

The clock of the Window Watchdog (WWDG) is derived by dividing the APB1 clock frequency by 4096. It detects abnormal program execution through the configuration of the time window. Therefore, WWDG is suitable for precise timing and is commonly used to monitor software faults that cause the application program to deviate from its normal operation sequence due to external interference or unforeseen logical conditions. When the WWDG decrementing counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0, a system reset occurs.

Main features:

- Programmable 14-bit independent down counter
- When the WWDG is enabled, a reset will occur under the following conditions:
  - The down-counter is less than 0x40
  - When the down counter value is greater than the value of the window register, reload will occur
- Early wake-up interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40

2.13 I^2C Bus Interface

The I^2C (Inter-Integrated Circuit) bus is a widely used bus structure that consists of only two bidirectional lines, namely the data line SDA and the clock line SCL. Through these two lines, all devices compatible with the I^2C bus can directly communicate with each other via the I^2C bus.

The I^2C interface connects the microcontroller and the serial I^2C bus, and can be used for communication between the MCU and external I^2C devices. The I^2C interface module implements the standard speed mode and fast mode of the I^2C protocol, with CRC calculation and verification functions, supports SMBus (System Management Bus) and PMBus (Power Management Bus). It controls all I^2C bus-specific sequencing, protocol, arbitration and timing. The I^2C interface module also supports DMA mode to effectively reduce the burden on the CPU.

Main features:

- This module can be used as master device or slave device
- Support 7-bit/10-bit addressing and general call
- As an I^2C master device, it can generate clock, start signal, and stop signal
- As an I^2C slave device, it has programmable I^2C address detection and stop bit detection functions
- Support Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz) and Fast-mode Plus (up to 1MHz)
- Supports interrupt vector, transfer complete interrupt, and error event interrupt
- Optional extend clock function
- Support DMA
- Generation or verification of configurable PEC(Packet error checking)
- Compatible with the PMBus and SMBus 2.0
- Support FIFO

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2.14 Universal Synchronous/Asynchronous Transceiver (USART)

Universal Synchronous Asynchronous Receiver Transmitter (USART) is a full-duplex serial data exchange interface that supports synchronous or asynchronous communication. It can be flexibly configured to facilitate full-duplex data exchange with a variety of external devices.

The USART interface allows configurable transmission and reception baud rates, and also supports continuous communication through DMA. USART also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smart card asynchronous protocol, IrDA SIR ENDEC function, as well as hardware flow control function.

Main features:

- Full duplex, asynchronous communication
- Single-wire half-duplex communications
- Programmable baud rate, up to 15 Mbit/s
- Configurable oversampling method by 16 or 8
- Programmable data word length (8 or 9 bits)
- Two internal FIFOs for transmit and receive data
- Configurable stop bits (1 or 2 stop bits)
- Support hardware-generated parity bit and parity bit checking
- Support hardware flow control: RTS, CTS
- Support transmission and reception via DMA
- Multiprocessor communications: If the address does not match, it enters mute mode. Wake-up from mute mode by idle line detection or address mark detection
- Support synchronous mode, allowing the user to control bidirectional synchronous serial communication in master mode
- Support asynchronous Smartcard protocol, compliant with ISO7816-3 standard
- Support IrDA (infrared data association) SIR ENDEC specifications, providing both normal and low power operation modes
- Support LIN mode
- Four error detection flags:Overflow error,Noise error,Frame error,Parity error
- Support multiple interrupt requests:Transmit data register empty,CTS flag,Transmission complete,Reception complete,Data overflow,Bus idle,Parity error,LIN mode break frame detection, and noise flags/overflow errors/frame errors in multi-buffer communications

Mode configuration:

USART modes	USART2	USART3	USART4	UART5	UART6	UART7	UART8
Asynchronous mode	Y	Y	Y	Y	Y	Y	Y
Multiprocessor communication	Y	Y	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y	Y	Y
Synchronous mode	Y	Y	Y	N	N	N	N
Half duplex (Single wire mode)	Y	Y	Y	Y	Y	Y	Y
Smartcard mode	Y	Y	Y	N	N	N	N
IrDA	Y	Y	Y	Y	Y	Y	Y
DMA	Y	Y	Y	Y	Y	Y	Y
Hardware flow control	Y	Y	Y	Y	Y	Y	Y

Note: Y = supported; N = not supported.

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2.15 Serial Peripheral Interface/inter-integrated sound interfaces (SPI/I²S)

The SPI protocol supports half-duplex, full-duplex and synchronous, serial communication with external devices. The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. It can be used for a variety of purposes, including simplex synchronous transfers on two lines with bidirectional data line, and also support hardware CRC check.

I²S is also a synchronous serial interface communication protocol. It supports four audio standards, including the Philips I²S standard, MSB and LSB alignment standards, and PCM standards. In half-duplex communication, it can operate in two modes: master and slave. When operating as a master device, it can provide clock signals to external slave devices via the interface.

The SPI main features are:

- Full-duplex and simplex synchronous transmission
- Support master, slave and multi-master mode
- 8 or 16 bit transmission frame format selection
- Programmable data order
- Hardware or software management of chip select signal
- Programmable clock polarity and phase
- Support hardware CRC calculation and check
- Support DMA transfer
- 8 bytes transmit/receive FIFO

The I²S main features are:

- Full-duplex and half-duplex synchronous transmission
- Support master, slave mode
- Supported I²S protocols:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard (with short and long frame synchronization)
- Configurable audio sampling frequency, ranging from 8KHz to 192KHz
- Programmable clock polarity (steady state)
- Data order is always MSB first
- Support DMA transfer
- Support multiple clock sources

2.16 Expanded Serial Peripheral Interface(xSPI)

xSPI is an interface used for communication with single/dual/quad/octal line SPI peripherals. It can operate in two modes: indirect and memory-mapped mode.

It supports indirect mode: all operations are performed using xSPI registers; memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory.

Main features:

- Configurable for 1/2/4/8-bit data

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- Support Single SPI/Normal SPI、DUAL SPI、QUAD SPI、Dual-QUAD、OCTAL SPI modes
- Support Motorola SPI:
  - Standard/Dual/Quad/Octal SPI
- Support SDR and DDR modes
- Support DDR transfer data mask
- Support clock stretching
- In indirect mode and memory-mapped mode, frame format and operation codes can be software configured
- Integrated FIFO for reception and transmission
- 8/16/32-bit data accesses allowed
- 16 words TX FIFO and 16 words RX FIFO
- Support DMA transfer
- XIP mode supports SPI read and write, and supports serial NOR FLASH
  - Support continuous transfer mode
  - Support data prefetch
- Support automatic decryption of executed code, meaning that the xSPI peripheral stores encrypted code, reads the encrypted code during execution, and decrypts it to plaintext for CPU execution, without affecting the access speed to the peripheral storage. The decryption can be software configurable to enable/disable, and the root key is stored in the NVR area, inaccessible to the user
- Support serial NAND FLASH and PSRAM
- When xSPI accesses external memory for read and write, after xSPI initialization, there is no need for additional configuration of xSPI between writing to and reading from external storage, allowing direct memory access (via SRAM address) for reading and writing to external memory
- Support 2 external chip select output controls in master mode; Support 1 chip select input in slave mode. All IOs multiplexed as chip select outputs in master mode can be multiplexed as chip select inputs in slave mode
- Support multi-master arbitration function

2.17 Universal Serial Bus High-Speed DualRole Interface (USB_HS_DualRole)

USB High-Speed Dual Role Interface (USB HS Dual Role), hereinafter referred to as USBHS. The USBHS controller is designed to provide a standard interface for high-speed data transfer and connecting external devices. USBHS supports both host and device modes, it contains a full-speed USB PHY internal, which can be configured as high-speed or full-speed mode, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

Main features:

- Support USB 2.0 high-speed (480Mb/s) / full-speed (12Mb/s) / low-speed (1.5Mb/s) Host mode
- Support USB 2.0 high-speed (480Mb/s) / full-speed (12Mb/s) Device mode
- Support all the four types of transfer: control transfer, bulk transfer, interrupt transfer and isochronous transfer
- USBHS contains a full-speed USB PHY internal, which supports high-speed, full-speed and low-speed operation, no more external PHY chip is needed
- Support HS SOF, FS SOF, and LS Keep-alive tokens
- SOF pulse can be output through PAD

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- SOF pulse is connected internally to the timer (TIMx)
- Support A-B device identification (ID line)
- USBHS has embedded DMA, and can be software configured for AHB bulk transfer type
- Has power-saving functions, such as stopping the system during USB suspension, shutting down digital module clocks, and managing power for PHY and DFIFO
- 4 KB dedicated RAM
- Contain 16 host channels in Host mode, each channel supports any type of USB transfer
- Built-in hardware scheduler in Host mode:
  - Up to 16 interrupt and synchronous transfer requests in the periodic hardware queue
  - Up to 16 control and bulk transfer requests in the non-periodic hardware queue
- In Host mode, it contains one RX FIFO, one periodic transfer TX FIFO, and one non-periodic transfer TX FIFO
- In Device mode, it contains 1 bidirectional control endpoint 0, as well as 8 IN endpoints and 7 OUT endpoints. IN and OUT endpoints can be configured for bulk transfer, interrupt transfer, or isochronous transfer
- In Device mode, it contains a shared RX FIFO and a TX-OUT FIFO, as well as 9 dedicated TX-IN FIFOs
- Supports soft disconnect function

Note: USBHS requires the use of a 16MHz, 19.2MHz, 20MHz, 24MHz, 26MHz, or 32MHz external crystal as a clock source.

2.18 General-Purpose Input/Output Interface (GPIO)

Up to 56 GPIOs, which can be divided into eight groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE/GPIOF/GPIOG/GPIOH). GPIO ports share pins with other multiplexed peripherals, allowing users to configure them flexibly according to requirements. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up or pull-down), or alternate peripheral function port. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up
  - Input pull down
  - Analog function
  - Open-drain output, pull-up and pull-down configurable
  - Push-pull output, pull-up and pull-down configurable
  - Push-pull alternate function, pull-up and pull-down configurable
  - Open-drain alternate function, pull-up and pull-down configurable
- Independent bit set or set functions
- All I/O support external interrupts
- All I/O support low-power mode wake-up, with configurable rising or falling edge:
  - 16 EXTI lines can be used for STOP0 mode wake-up, and all I/O can be multiplexed as EXTI

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  - PA0/PA2/PC5/PC13/PE6 can be used to wake-up from STANDBY mode
- Support software configure alternate function selection
- Support GPIO lock mechanism, can only be cleared by reset once locked

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed in 32-bit words (16-bit half-word or 8-bit byte access is not allowed).

2.19 Analog/Digital Converter (ADC)

12 bit ADC consists of a 12-bit successive approximation high-speed analog-to-digital converter. There are four ADCs, ADC1/ADC2, ADC3/ADC4 that can be combined into dual ADCs mode; ADC1/ADC2/ADC3 can be combined into triple ADCs mode. Each ADC has up to 19 multiplexed channels. A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register. The analog watchdog1/2/3 feature allow the application to detect if the input voltage goes outside the user-defined high or low thresholds, and the frequency of ADC input clock is up to 80 MHz.

Main features:

- Support 4 ADCs, support single-ended or differential inputs
  - ADC1 is connected to 14 external channels and to 3 internal channels
  - ADC2 is connected to 16 external channels and to 1 internal channels
  - ADC3 is connected to 19 external channels
  - ADC4 is connected to 18 external channels
- Support 12/10/8/6-bits resolution configurable
  - The maximum sampling rate at 12bit resolution is 4.7 MSPS
  - The maximum sampling rate at 10bit resolution is 6 MSPS
  - The maximum sampling rate at 8bit resolution is 7.2 MSPS
  - The maximum sampling rate at 6bit resolution is 9 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 240 MHz
  - PLL can be configured as a sampling clock source, up to 80 MHZ, support 1, 2, 3, 4, 6, 8, 10, 12 frequency division
  - The AHB_CLK can be configured as the sampling clock source, up to 80 MHz, and supports frequency 1, 2, 3, 4, 6, 8, 10, 12, 16, 32
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports EXTI/TIMER trigger ADC sampling
- The sampling time interval for all channels can be programmed independently
- 3 analog watchdogs per ADC
- When the ADC is ready, sampling is completed, conversion is finished, or an analog watchdog 1/2/3 event occurs, an interrupt can be triggered
- Support 4 conversion modes:
  - Single conversion

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  - Continuous conversion
  - Discontinuous mode
  - Scan mode
- Support self-calibration
- Data alignment with in-built data coherency
- Start-of-conversion can be initiated:
  - By software for both regular and injected conversions
  - By hardware triggers with configurable polarity (internal timers events or GPIO input events) for both regular and injected conversions
- Oversampling
  - 16-bit data register
  - Adjustable oversampling ratio, x2, x4, x8, x16, x32, x64, x128, x256
  - Programmable data right shift up to 8 bits
- Data preconditioning
  - Support offset compensation
  - Support gain compensation
- Multi-ADC mode
  - Dual ADC mode: ADC1 and ADC2 combined, ADC3 and ADC4 combined
  - Triple ADC mode: ADC1, ADC2, and ADC3 combined
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$

2.20 Digital/Analog Converter (DAC)

DAC is Digital-to-Analog Converter, which primarily involves digital input and voltage output. The DAC can be configured in 8-bit or 12-bit mode and may be used in conjunction with the DMA controller. In 12-bit mode, the data can be left or right-aligned. In 8-bit mode, the data can be right-aligned. Each DAC has its own converter and can perform conversions independently. In dual DAC mode, conversions can be done independently or simultaneously when both DACs are grouped (DAC1 & DAC2) together for synchronous update operations.

When the DAC output is internally connected to peripherals on the chip, the DACx_OUT pin can be used as a general-purpose input/output (GPIO). The DAC output buffer can be selectively enabled to obtain a high-drive output current.

Main features:

- Support 2 DACs, each DAC has its own converter
- An output channel for a built-in Buffer
- Configurable 8/12-bits output, configurable left or right data alignment in 12-bit mode
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- Double data DMA capability to reduce the bus activity
- Noise-wave, Triangular-wave and Saw tooth wave generation

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- DAC output supports connection to on-chip peripherals
- Buffer offset calibration
- Input voltage reference from V_{REF+}
- External triggers for conversion

2.21 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated during the link-time and generating of the software.

Main features of CRC32:

- CRC32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)
- 32-bit data to be checked and 32-bit output checksum
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- General-purpose 8-bit register
- Programmable CRC initial value

Main features of CRC16:

- CRC16 ($X^{16} + X^{15} + X^2 + 1$)
- 8-bit data to be checked and 16-bit output checksum
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- Configurable check initial value, and configurable endianness of the data to be checked
- Support 8-bit LRC checksum value generation
- Programmable CRC initial value

2.22 Secure Algorithm Co-processor (SAC)

The device features a secure algorithm co-processor, it supports a variety of international algorithms hash cryptography algorithm acceleration, which can greatly improve the speed of encryption and decryption compared with pure software algorithm.

The hardware supports the following algorithms:

- Support DES symmetric algorithms
  - DES and 3DES encryption and decryption operations are supported
  - TDES supports 2KEY and 3KEY mode
  - Support CBC and ECB mode
- Support the symmetric AES algorithm
  - Support 128bits, 192bits, or 256bits key length
  - Support CBC, ECB, and CTR mode
- Support the symmetric SM4 algorithm

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  - Support CBC, ECB mode
- Support SHA hash algorithm
  - Support SHA1, SHA244, SHA256
- Support the MD5 digest algorithm
- Support SM3 hash algorithm
- Support random number generation

Note: The SAC module operating clock is up to 180MHz, so the HCLK frequency should not exceed 180MHz to avoid abnormal operation of the SAC module.

2.23 Unique Device Serial Number (UID)

The N32H481 series products have two built-in unique device serial numbers of different lengths, which are 96-bit unique device ID (UID) and 128-bit unique customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32H481 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory. It can also be used to activate Secure Bootloader with security functions.

The UCID is 128-bit, which complies with the definition of Nations technology chip serial number. It contains the information related to chip production and version.

2.24 Serial Single-Wire JTAG Debug Port (SWJ-DP)

The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

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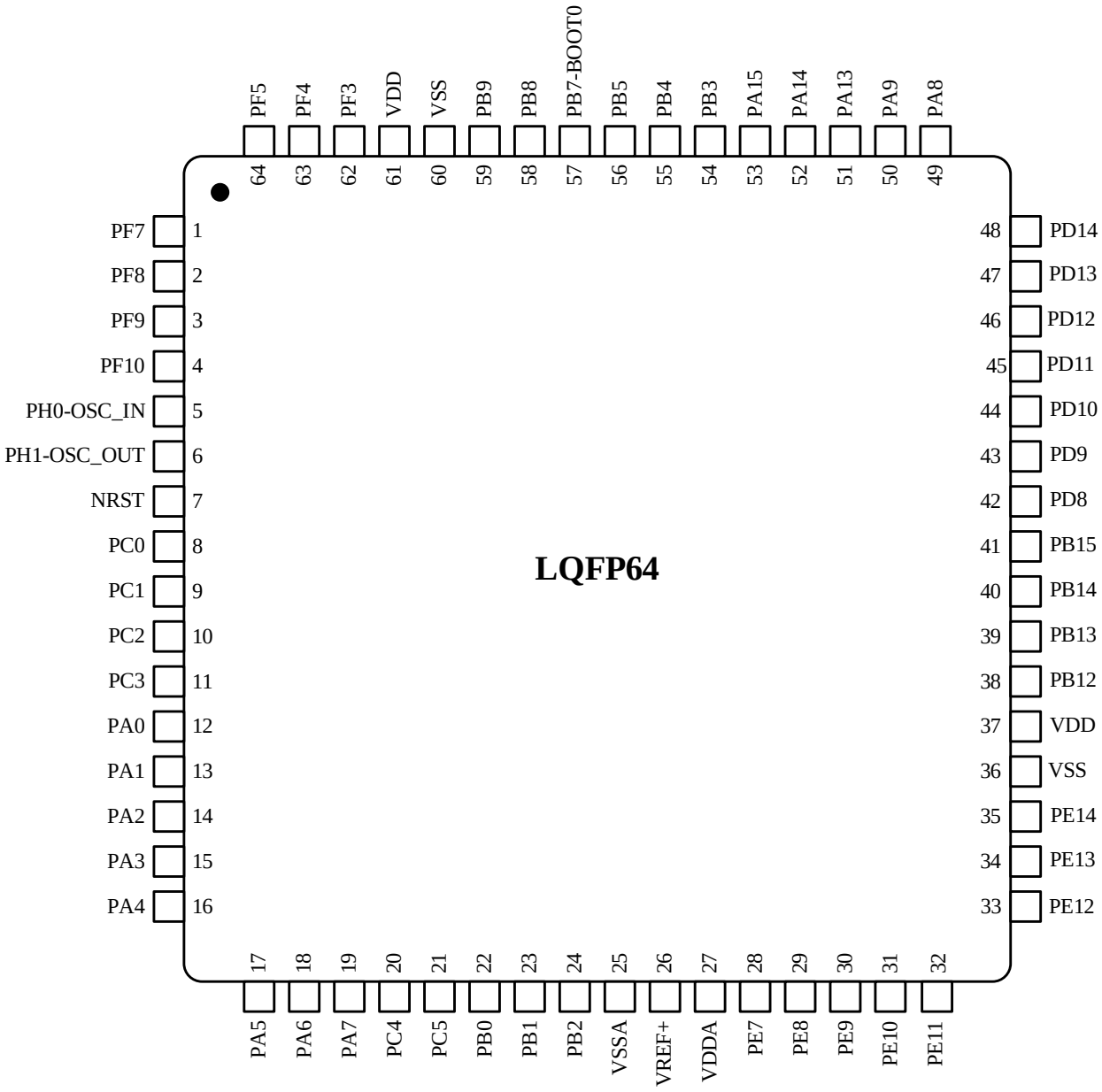
3 Pinouts and Pin Description

3.1 Pinouts

3.1.1 LQFP64

Figure 3-1. N32H481 Series LQFP64 Pinout



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3.2 Pin Description

Table 3-1 Pin Description

LQFP64	Pin type(1)	IO structure(2)	Fail-safe(3)	Pin name (function after reset)	Alternate functions	Additional functions
1	I/O	FTa	Y	PF7	GTIM7_CH1 ATIM3_BKIN GTIM4_CH2 XSPI_IO2 SPI5_SCK UART7_TX GTIM8_ETR EVENTOUT	ADC1_IN15
2	I/O	FTa	Y	PF8	GTIM9_CH1 ATIM3_BKIN2 GTIM4_CH3 XSPI_IO0 SPI5_MISO EVENTOUT	ADC2_IN1
3	I/O	FTa	Y	PF9	GTIM10_CH1 ATIM3_BKIN GTIM8_CH1 SPI2_SCK GTIM4_CH4 XSPI_IO1 SPI5_MOSI EVENTOUT	ADC4_IN17
4	I/O	FTa	Y	PF10	ATIM3_BKIN2 GTIM8_CH2 SPI2_SCK XSPI_CLK EVENTOUT	ADC4_IN0
5	I/O	FTa	Y	PH0-OSC_IN	I2C2_SDA SPI2_NSS/I2S2_WS ATIM1_CH3N USART2_RX GTIM5_CH3 ATIM3_CH1N EVENTOUT	OSC_IN ADC1_IN10
6	I/O	FTa	Y	PH1-OSC_OUT	I2C2_SCL SPI2_SCK/I2S2_CK USART2_TX GTIM5_CH4 ATIM3_CH2N EVENTOUT	OSC_OUT ADC2_IN10
7	I/O	RST	Y	NRST	-	-
8	I/O	FTa	Y	PC0	LPTIM1_IN1 ATIM1_CH1 UART7_RX I2C3_SCL USART4_TX XSPI_RXDS GTIM10_CH1 EVENTOUT	ADC12_IN6

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9	I/O	FTa	Y	PC1	LPTIM1_OUT ATIM1_CH2 UART7_TX XSPI_IO4 SPI3_MOSI/I2S3_SD SPI2_MOSI/I2S2_SD I2C3_SDA USART4_RX GTIM10_CH2 EVENTOUT	ADC12_IN7
10	I/O	FTa	Y	PC2	SPI2_MISO I2S2_AUX_SD LPTIM1_IN2 ATIM1_CH3 ATIM3_CH2 XSPI_IO5 SPI3_NSS/I2S3_WS GTIM10_CH3 UAR7_TX EVENTOUT	ADC12_IN8
11	I/O	FTa	Y	PC3	SPI2_MOSI/I2S2_SD LPTIM1_ETR ATIM1_CH4 ATIM1_BKIN2 XSPI_IO6 SPI3_SCK/I2S3_CK GTIM10_CH4 UAR7_RX EVENTOUT	ADC12_IN9
12	I/O	FTa	Y	PA0-WKUP1	USART2_CTS UART6_TX GTIM1_CH1_ETR GTIM4_CH1 ATIM2_ETR ATIM2_BKIN SPI3_MISO ATIM3_CH3N EVENTOUT	ADC12_IN3 WKUP1 RTC_TAMP2
13	I/O	FTa	Y	PA1	USART2_RTS_DE UART6_RX GTIM4_CH2 GTIM1_CH2 RTC_REFIN GTIM8_CH1N SPI4_MOSI SPI3_MOSI/I2S3_SD SPI6_SCK ATIM3_CH4N EVENTOUT	ADC12_IN4
14	I/O	FTa	Y	PA2	USART2_TX GTIM4_CH3 GTIM5_CH1 GTIM1_CH3 GTIM8_CH1_ETR XSPI_NSS0 UART7_TX I2S_CKIN SPI6_NSS EVENTOUT	ADC1_IN5 WKUP3 LSCO

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15	I/O	FTa	Y	PA3	USART2_RX GTIM4_CH4 GTIM5_CH2 GTIM1_CH4 GTIM8_CH2 XSPI_CLK UART7_RX I2S2_MCK MCO2 EVENTOUT	ADC1_IN2
16	I/O	TTa	Y	PA4	SPI1_NSS SPI3_NSS/I2S3_WS USART2_CK OTG_HS_SOF GTIM2_CH2 XSPI_NSS1 I2C2_SCL SPI6_MISO GTIM7_CH1 LPTIM2_IN2 EVENTOUT	ADC2_IN17 DAC1_OUT
17	I/O	TTa	Y	PA5	SPI1_SCK GTIM1_CH1_ETR ATIM2_CH1N XSPI_CLK I2C2_SDA SPI6_MOSI XSPI_IO0 GTIM7_CH2 EVENTOUT	ADC2_IN13 DAC2_OUT
18	I/O	TTa	Y	PA6	SPI1_MISO ATIM2_BKIN GTIM9_CH1 GTIM2_CH1 ATIM1_BKIN XSPI_IO3 UART7_CTS I2S2_MCK XSPI_IO0 EVENTOUT	ADC2_IN0
19	I/O	TTa	Y	PA7	SPI1_MOSI ATIM2_CH1N GTIM7_CH1 GTIM2_CH2 ATIM1_CH1N GTIM10_CH1 XSPI_IO2 XSPI_IO1 MCO1 GTIM9_CH2 EVENTOUT	ADC2_IN2
20	I/O	FTa	Y	PC4	ATIM1_ETR I2C2_SCL XSPI_IO7 XSPI_IO2 UART7_TX I23_SCL LPTIM2_OUT ATIM3_CH3N EVENTOUT	ADC2_IN5

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21	I/O	FTa	Y	PC5	GTIM8_BKIN ATIM1_CH4N XSPI_IO3 UART7_RX I2C3_SDA GTIM5_ETR EVENTOUT	ADC2_IN11 WKUP4
22	I/O	FTa	Y	PB0	GTIM2_CH3 ATIM2_CH2N ATIM1_CH2N XSPI_IO1 SPI5_SCK SPI3_MOSI/I2S3_SD USART4_TX EVENTOUT	ADC3_IN12 ADC1_IN1
23	I/O	FTa	Y	PB1	GTIM2_CH4 ATIM2_CH3N ATIM1_CH3N XSPI_IO0 UART7_RTS_DE SPI5_NSS USART4_RX EVENTOUT	ADC1_IN12 ADC3_IN1
24	I/O	FTa	Y	PB2	RTC_OUT2 LPTIM1_OUT GTIM4_CH1 ATIM3_CH1 I2C3_SMBA XSPI_IO5 GTIM1_CH4 SPI3_MOSI/I2S3_SD UART6_TX SPI1_NSS GTIM6_ETR EVENTOUT	ADC2_IN12
25	-	-	-	VSSA/VREFN	-	-
26	-	-	-	VREFP	-	-
27	-	-	-	VDDA	-	-
28	I/O	FTa	Y	PE7	ATIM1_ETR UART7_RX UART6_RX SPI1_SCK GTIM4_CH2 GTIM9_CH4 EVENTOUT	ADC3_IN4
29	I/O	FTa	Y	PE8	ATIM1_CH1N GTIM4_CH3 UART7_TX SPI1_MISO EVENTOUT	ADC34_IN6
30	I/O	FTa	Y	PE9	ATIM1_CH1 GTIM4_CH4 SPI1_MOSI EVENTOUT	ADC3_IN2

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31	I/O	FTa	Y	PE10	ATIM1_CH2N XSPI_CLK SPI2_NSS/I2S2_WS ATIM1_CH1N GTIM2_CH1 GTIM9_CH1 USART4_TX EVENTOUT	ADC34_IN14
32	I/O	FTa	Y	PE11	ATIM1_CH2 SPI4_NSS XSPI_NSS0 SPI5_NSS SPI2_SCK/I2S2_CK USART4_RX EVENTOUT	ADC34_IN15
33	I/O	FTa	Y	PE12	ATIM1_CH3N SPI4_SCK XSPI_IO0 SPI5_SCK SPI2_MISO GTIM7_CH4 EVENTOUT	ADC34_IN16
34	I/O	FTa	Y	PE13	ATIM1_CH3 SPI4_MISO XSPI_IO1 SPI5_MISO SPI2_MOSI/I2S2_SD EVENTOUT	ADC3_IN3
35	I/O	FTa	Y	PE14	ATIM1_CH4 SPI4_MOSI ATIM1_BKIN2 XSPI_IO2 SPI5_MOSI EVENTOUT	ADC4_IN5
36	S	-	-	VSS	-	-
37	S	-	-	VDD	-	-
38	I/O	FTa	Y	PB12	SPI2_NSS/I2S2_WS I2C2_SMBA USART3_CK ATIM1_BKIN OTG_HS_ID GTIM4_ETR UART7_RTS_DE SPI4_NSS GTIM9_CH3 EVENTOUT	ADC1_IN11 ADC4_IN1
39	I/O	FTa	Y	PB13	SPI2_SCK/I2S2_CK USART3_CTS ATIM1_CH1N UART7_CTS SPI4_SCK ATIM1_CH2 GTIM10_CH2 GTIM9_CH4 EVENTOUT	USB_HS_VBUS ADC3_IN5

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40	I/O	FTa	N	PB14	SPI2_MISO ATIM1_CH2N GTIM8_CH1 ATIM2_CH2N I2S2_AUX_SD GTIM9_CH2 USART4_CK EVENTOUT	USB_HS_DM ADC4_IN4 ADC1_IN0
41	I/O	FTa	N	PB15	SPI2_MOSI/I2S2_SD ATIM1_CH3N ATIM2_CH3N GTIM8_CH2 GTIM8_CH1N ATIM2_CH4 UART8_CTS EVENTOUT	USB_HS_DP RTC_REFIN ADC2_IN15 ADC4_IN3
42	I/O	FTa	Y	PD8	SPI3_NSS/I2S3_WS ATIM1_CH3 GTIM10_CH1 EVENTOUT	ADC4_IN12
43	I/O	FTa	Y	PD9	SPI3_SCK/I2S3_CK ATIM1_CH3N GTIM9_CH3 GTIM7_ETR GTIM10_CH2 EVENTOUT	ADC4_IN13
44	I/O	FTa	Y	PD10	USART3_CK ATIM1_CH4 ATIM3_ETR EVENTOUT	ADC34_IN7
45	I/O	FTa	Y	PD11	USART3_CTS GTIM4_ETR I2C4_SMBA SPI3_MISO USART4_TX I2C1_SCL GTIM10_CH3 EVENTOUT	ADC34_IN8
46	I/O	FTa	Y	PD12	GTIM3_CH1 SPI3_MOSI/I2S3_SD GTIM6_CH1 EVENTOUT	ADC34_IN9
47	I/O	FTa	Y	PD13	GTIM3_CH2 XSPI_RXDS GTIM6_CH2 EVENTOUT	ADC34_IN10
48	I/O	FTa	Y	PD14	GTIM3_CH3 I2C4_SCL ATIM2_CH1 GTIM10_CH4 GTIM6_CH3 EVENTOUT	ADC34_IN11
49	I/O	FTa	Y	PA8	MCO1 ATIM1_CH1 I2C3_SCL I2C2_SDA I2S2_MCK I2C2_SMBA GTIM3_ETR EVENTOUT	ADC3_IN18

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50	I/O	FTa	Y	PA9	ATIM1_CH2 I2C3_SMBA I2C2_SCL I2S3_MCK GTIM8_BKIN GTIM1_CH3 SPI2_SCK/I2S2_CK I2C4_SCL I2C1_SCL EVENTOUT	ADC4_IN18
51	I/O	FT	Y	PA13	JTMS-SWDIO GTIM9_CH1N I2C4_SCL I2C1_SCL IR_OUT USART3_CTS GTIM3_CH3 UART6_TX GTIM8_CH3 EVENTOUT	-
52	I/O	FT	Y	PA14	JTCK-SWCLK LPTIM1_OUT I2C4_SMBA I2C1_SDA ATIM2_CH2 ATIM1_BKIN USART2_TX UART6_RX GTIM8_CH4 EVENTOUT	-
53	I/O	FT	Y	PA15	JTDI SPI3_NSS/I2S3_WS GTIM1_CH1_ETR SPI1_NSS ATIM2_CH1 I2C1_SCL USART2_RX UART6_RTS_DE ATIM1_BKIN USART2_CTS ATIM2_CH1N ATIM3_ETR EVENTOUT	-
54	I/O	FT	Y	PB3	JTDO SPI3_SCK/I2S3_CK GTIM1_CH2 SPI1_SCK GTIM3_ETR ATIM2_CH1N USART2_TX GTIM2_ETR I2C2_SDA USART2_RTS_DE ATIM2_BKIN EVENTOUT	-
55	I/O	FT	Y	PB4	NJTRST SPI3_MISO GTIM2_CH1 SPI1_MISO I2S3_AUX_SD	—

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					GTIM9_CH1_ETR ATIM2_CH2N USART2_RX GTIM10_BKIN I2C3_SDA ATIM2_ETR LPTIM2_IN1 USART2_TX EVENTOUT	
56	I/O	FT	Y	PB5	I2C1_SMBA GTIM2_CH2 SPI1_MOSI SPI3_MOSI/I2S3_SD GTIM9_BKIN ATIM2_CH3N USART2_CK I2C3_SDA GTIM10_CH1 LPTIM1_IN1 UART5_CTS USART2_RX EVENTOUT	—
57	I/O	FT	Y	PB7-BOOT0	I2C1_SDA GTIM3_CH2 GTIM10_CH1N ATIM2_BKIN GTIM2_CH4 I2C4_SDA LPTIM1_IN2 UART6_CTS EVENTOUT	PVD_IN
58	I/O	FT	Y	PB8	GTIM3_CH3 GTIM6_CH1 I2C1_SCL GTIM9_CH1 ATIM2_CH2 ATIM1_BKIN SPI5_MOSI FMEC_NWAIT GTIM9_CH4 EVENTOUT	-
59	I/O	FT	Y	PB9	SPI2_NSS/I2S2_WS GTIM3_CH4 GTIM7_CH1 I2C1_SDA GTIM10_CH1 ATIM2_CH3 ATIM1_CH3N EVENTOUT	IR-OUT
60	S	-	-	VSS	-	-
61	S	-	-	VDD	-	-
62	I/O	FTa	Y	PF3	ATIM3_CH4 I2C3_SCL XSPI_IO1 EVENTOUT	ADC3_IN17

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63	I/O	FTa	Y	PF4	ATIM3_CH1N I2C3_SDA XSPI_IO2 GTIM5_CH1 I2C3_SCL EVENTOUT	ADC3_IN0
64	I/O	FTa	Y	PF5	ATIM3_CH2N XSPI_IO3 GTIM5_CH2 I2C3_SDA EVENTOUT	ADC3_IN13

Notes:

1. *I = input, O = output, S = power supply.*
2. *FT: 5V toleran; FTa: 5V tolerant, support analog peripherals.*
3. *Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.*
4. *The RTS_DE, TX, and RX signals of USART3, UART5 and UART8 can be mapped to any IO.*

The ADC12_INx mentioned in the pin name annotations in the table indicates that this pin can be either ADC1_INx or ADC2_INx. For example, ADC12_IN9 means that this pin can be configured as ADC1_IN9 or ADC2_IN9.

Similarly, the ADC34_INx mentioned in the pin name annotations in the table indicates that this pin can be either ADC3_INx or ADC4_INx.

In the pin PA0 of the table, the multiplexing function GTIM1_CH1_ETR means that this function can be configured as GTIM1_TI1 or GTIM1_ETR. Similarly, for PA15, the remapping multiplexing function name GTIM1_CH1_ETR has the same meaning.

For the FT ports in the table, it is necessary to ensure that the voltage difference between the IO voltage and the power supply voltage is less than 3.6V.

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4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and Maximum Values

The minimum and maximum values in the Beta version are based on design simulations.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3∑).

4.1.2 Typical Values

Unless otherwise specified, typical data are based on T_A = 25 ℃ and V_{DD} = 3.3V (for the 1.8V ≤ V_{DD} ≤ 3.6V voltage range). These data are for design guidance only and not tested.

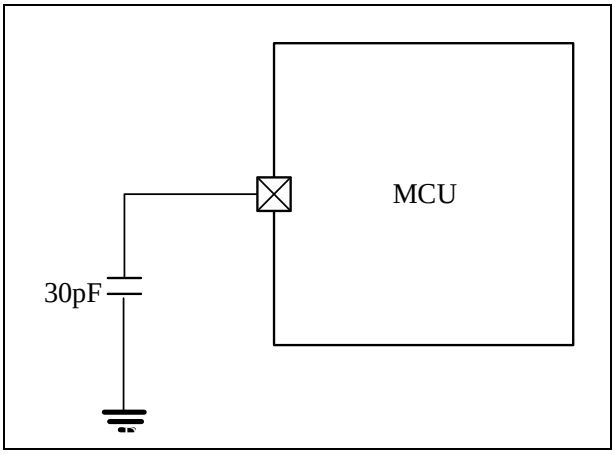
4.1.3 Typical Curves

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading Capacitor

The load conditions for measuring pin parameters are shown Figure 4-1:

Figure 4-1 Load Conditions Of Pins



4.1.5 Pin Input Voltage

The measurement of the input voltage on the pin is shown Figure 4-2:

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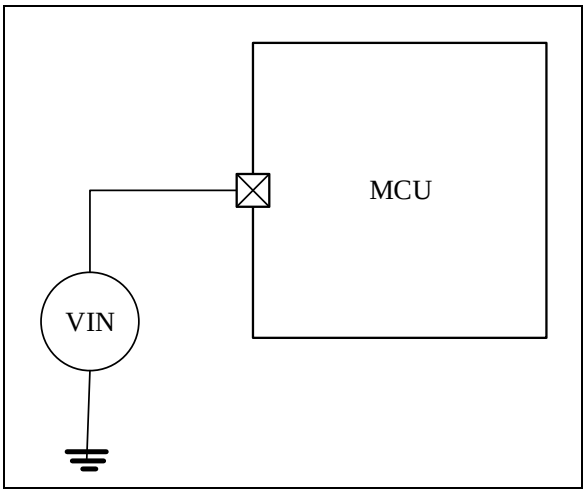
Figure 4-2 Pin Input Voltage



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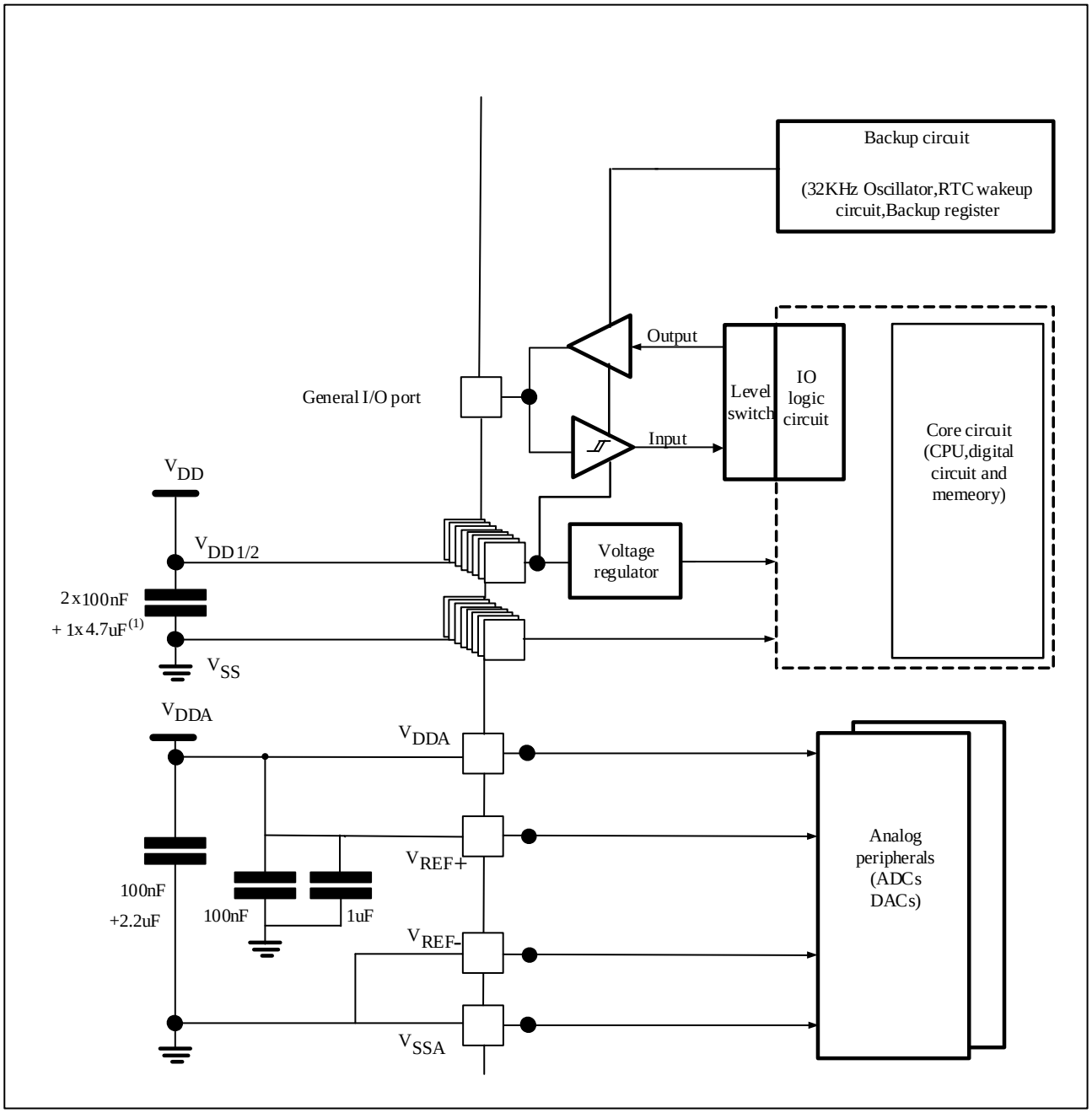
4.1.6 Power Supply Scheme

Figure 4-3 Power Supply Scheme



Note:

(1) The 4.7μF capacitor in the above diagram must be connected to the specified VDD. The specified VDD for LQFP64 is Pin 61.

(2) The above figure shows the application scenario of VREF+ output, when VREF+ selects the external way it is necessary to change the 1uF capacitor to 2.2uF capacitor.

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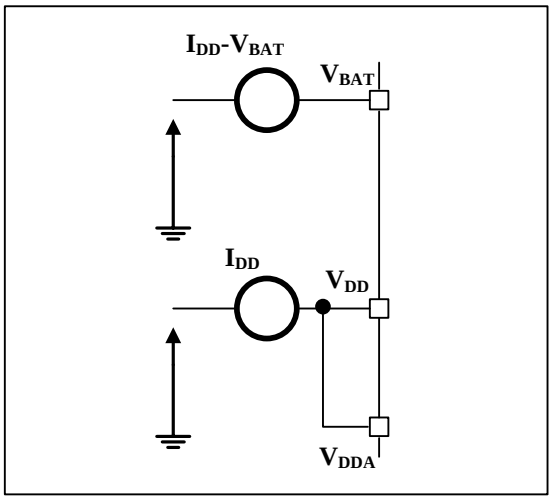
4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins(3)	V_{SS} - 0.3	5.5	
	Input voltage on other pins(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		-

Notes:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

(2) V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

(3) When a 5V tolerant pin inputs 5.5V, VDD cannot be lower than 2.25V.

Table 4-2 Current Characteristics

Symbol	Describe	Max (1)	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1) (4)	400	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1) (4)	400	
I_{IO}	Output current sunk by I/O and control pins	12	
	Output current source by I/O and control pins	-12	
$I_{INJ(PIN)}$(2)(3)	Injection current on NRST pin	-5/0	
	Injection current on other pins	+/-5	

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Notes:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

(2) When $V_{IN}>V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Refer to Table 4-1 for voltage characteristics.

(3) Reverse injection current can interfere with the analog performance of the device. See section 4.3.2026.

(4) When the maximum current occurs, the maximum allowable voltage drop of VDD is 0.1VDD.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	- 65 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	240	MHz
f_{PCLK}	Internal APB1/2 clock frequency	-	0	180	
V_{DDA}	Analog operating of working voltage	Must be the same potential as V_{DD}(1)	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃
T_J	Junction temperature range	7 suffix version	-40	125	℃

(1) It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

4.3.2 Operating Conditions at Power-on and Power-down

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating Conditions At Power-On And Power-Down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	20	∞	μs/V
	V_{DD} fall time rate		80	∞	

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-6 Features Of Embedded Reset And Power Control Modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (MSB of PWR_CTRL is 0)	PRS[2:0]=000 (rising edge)	2.09	2.18	2.27	V
		PRS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PRS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PRS[2:0]=001 (falling edge)	2.09	2.18	2.27	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PRS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PRS[2:0]=010 (falling edge)	2.19	2.28	2.37	V
		PRS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PRS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PRS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PRS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PRS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PRS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PRS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PRS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PRS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PRS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
	Programmable voltage detector level selection (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	1.7	1.78	1.85	V
		PRS[2:0]=000 (falling edge)	1.61	1.68	1.75	V
		PRS[2:0]=001 (rising edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (falling edge)	1.7	1.78	1.85	V
		PRS[2:0]=010 (rising edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (falling edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (rising edge)	2	2.08	2.16	V
		PRS[2:0]=011 (falling edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (rising edge)	3.15	3.28	3.41	V
		PRS[2:0]=100 (falling edge)	3.05	3.18	3.31	V
		PRS[2:0]=101 (rising edge)	3.24	3.38	3.52	V
		PRS[2:0]=101 (falling edge)	3.15	3.28	3.41	V
		PRS[2:0]=110 (rising edge)	3.34	3.48	3.62	V
		PRS[2:0]=110 (falling edge)	3.24	3.38	3.52	V
		PRS[2:0]=111 (rising edge)	3.44	3.58	3.72	V
		PRS[2:0]=111 (falling edge)	3.34	3.48	3.62	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
V_{POR}	VDD power on/power down reset threshold	-	-	1.66/1.58	-	V
V_{BOR}	BOR power on/off reset threshold	BOR_LVL[2:0]=000 (rising edge)	-	1.66	-	V
		BOR_LVL[2:0]=000 (falling edge)	-	1.62	-	V
		BOR_LVL[2:0]=001 (rising edge)	-	2.1	-	V
		BOR_LVL[2:0]=001 (falling edge)	-	2	-	V
		BOR_LVL[2:0]=010 (rising edge)	-	2.3	-	V
		BOR_LVL[2:0]=010 (falling edge)	-	2.2	-	V
		BOR_LVL[2:0]=011 (rising edge)	-	2.6	-	V
		BOR_LVL[2:0]=011 (falling edge)	-	2.5	-	V
		BOR_LVL[2:0]=100 (rising edge)	-	2.9	-	V
		BOR_LVL[2:0]=100 (falling edge)	-	2.8	-	V
$T_{RSTTEMPO}$(1)	Reset duration	-	-	0.8	4	ms

(1) Guaranteed by design, not tested in production.

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4.3.4 Embedded Reference Voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in **Table 4-4**.

Table 4-7 Internal Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃< T_A< +105℃	1.164	1.2	1.236	V
$T_{S\_vrefint}$(1)	The sampling time of the ADC when reading the internal reference voltage	-	-	5.1	17.1(2)	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	VDD = 3.3V -40℃< T_A< +105℃	-14	-	14	mV

Notes:

(1) The shortest sampling time is obtained through multiple loops in the application.

(2) Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, toggle rate of I/O pins, program location in memory, and executed code.

The measurement method of current consumption is described in **Figure 4-4**.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum Current Consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting period from 0 to 40 MHz, 1 waiting period from 40 to 80 MHz, 2 waiting periods from 80 to 120 MHz, 3 waiting periods from 120 to 160 MHz, 4 waiting periods from 160 to 200 MHz, 5 waiting periods from 200 to 240 MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$.
- VDD is 3.63V, ambient temperature is 105℃

The parameters given in Table 4-8 and Table 4-9 are based on tests at the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Maximum Current Consumption In Operating Mode Where Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)				Unit
				T_A = -40℃	T_A = 25℃	T_A = 85℃	T_A = 105℃	
I_{DD}	Supply current in operation mode	External clock(2), enable all peripherals	240MHz	95.22	98.31	111.87	122.34	mA
			180MHz	73.81	76.65	89.52	99.68	
			120MHz	53.10	55.71	67.92	77.76	
			60MHz	29.79	32.12	43.73	53.27	
			240MHz	31.21	33.86	45.19	54.81	

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		External clock(2), disable all peripherals	180MHz	24.73	27.23	38.20	47.72	
			120MHz	18.52	20.82	31.48	40.84	
			60MHz	10.96	13.10	23.73	32.94	

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) Enable PLL when f_{HCLK} > 8MHz.

Table 4-9 Maximum Current Consumption In Sleep Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)				Unit
				T_A = -40℃	T_A = 25℃	T_A = 85℃	T_A = 105℃	
I_{DD}	Supply current in sleep mode	External clock(2), enable all peripherals	240MHz	85.66	88.57	101.66	112.03	mA
			180MHz	66.45	69.16	81.69	91.73	
			120MHz	48.20	50.68	62.69	72.43	
			60MHz	27.17	29.42	40.89	50.37	
		External clock(2), disable all peripherals	240MHz	19.26	21.48	32.59	41.85	
			180MHz	15.45	17.61	28.59	37.81	
			120MHz	11.65	13.75	24.58	33.75	
			60MHz	7.64	9.67	20.41	29.48	

Notes:

(1) Based on comprehensive evaluation result, not tested in production.

(2) Enable PLL when f_{HCLK} > 8MHz.

4.3.5.2 Current consumption in Low-Power Mode

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disable unless otherwise noted.

Table 4-10 Typical Current Consumption In Low Power Mode(2)

Symbol	Parameter	Conditions	Typ (1)				Unit
			T_A = -40℃	T_A =25℃	T_A =85℃	T_A =105℃	
I_{DD}	Supply current in STOP0 mode	Regulator in run mode, RTC on, IWDG off, Backup SRAM hold	1.3	2.84	13	21.84	mA
		Regulator in LP mode, RTC on, IWDG off, Backup SRAM hold	0.87	1.67	7.72	13.24	
I_{DD}	Supply current in STANDBY mode	RTC on, IWDG off, BackupSRAM hold	17.4	18.7	29.4	44	uA
		RTC off, IWDG off, BackupSRAM hold	17.3	18.6	29.3	44	
		RTC off, IWDG off, BackupSRAM not holding	17.3	18.6	29.4	44.1	

(1) Based on comprehensive evaluation result, not tested in production.

(2) Based on the results of Version B chip test

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Table 4-11 Typical Current Consumption In Low Power Mode(2)

Symbol	Parameter	Conditions	Typ (1)				Unit
			T_A = -40℃	T_A =25℃	T_A =85℃	T_A =105℃	
I_{DD}	Supply current in STOP0 mode	Regulator in run mode, RTC on, IWDG off, Backup SRAM hold	1.3	2.84	13	21.84	mA
		Regulator in LP mode, RTC on, IWDG off, Backup SRAM hold	0.87	1.67	7.72	13.24	
I_{DD}	Supply current in STANDBY mode	RTC on, IWDG off, BackupSRAM hold	2.8	3.9	16.3	31.3	uA
		RTC off, IWDG off, BackupSRAM hold	2.7	3.8	16.2	31.4	
		RTC off, IWDG off, BackupSRAM do not hold	2.6	3.7	16.2	31.4	

(1) Based on comprehensive evaluation result, not tested in production.

(2) Based on the results of Version B chip test

4.3.5.3 Peripheral current consumption

Table 4-12 Peripheral current consumption

Bus	Peripheral	Typ	Unit
AHB	DMA1	4.47	µA/MHz
	DMA2	4.12	
	XSPI	14.45	
	USBHS	23.75	
AHB1	BKP SRAM	0.41	µA/MHz
	CRC	0.83	
AHB2	ATIM1	10.17	µA/MHz
	ATIM2	10.82	
	ATIM3	10.69	
AHB3	GPIOA	45.33	µA/MHz
	GPIOB	45.82	
	GPIOC	46.06	
	GPIOD	44.89	
	GPIOE	45.41	
	GPIOF	45.81	
	GPIOG	44.98	
	GPIOH	44.52	
	ADC1	17.54	
	ADC2	14.06	
	ADC3	14.90	
	ADC4	14.66	

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	SAC	2.49	
APB1	DAC1	4.64	µA/MHz
	DAC2	4.64	
	I2C1	6.40	
	I2C2	6.80	
	I2C3	6.77	
	I2C4	6.40	
	LPTIM1	3.91	
	LPTIM2	4.83	
	UART5	5.39	
	UART8	5.53	
	GTIM1	9.61	
	GTIM2	8.85	
	GTIM3	9.38	
	GTIM4	11.60	
	GTIM5	11.47	
	GTIM6	11.61	
	GTIM7	11.65	
	UCDR	5.55	
	BTIM1	6.56	
	BTIM2	6.38	
	SPI2/I2S2	6.64	
	SPI3/I2S3	6.48	
	USART2	6.62	
	USART3	6.85	
	RTC	3.26	
	WWDG	3.70	
	PWR	4.60	
APB2	SPI1	5.14	µA/MHz
	SPI4	5.28	
	SPI5	4.77	
	SPI6	4.82	
	USART1	6.83	
	USART4	9.17	
	UART6	5.51	
	UART7	5.51	
	GTIM8	13.50	
	GTIM9	13.36	
	GTIM10	13.62	

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4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Source (HSE)

The characteristic parameters given in the following table are measured using a high-speed external clock source (Bypass mode), and the ambient temperature and supply voltage meet the conditions specified in **Table 4-4**.

Table 4-13 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	1	8	50	MHz
V_{HSEH}	OSC_IN Input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$	Time when OSC_IN is high or low(1)		16	-	-	ns
$t_{r(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$t_{f(HSE)}$						
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-1	-	+1	μA

(1) Guaranteed by design, not tested in production.

4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

4.3.7.1 High Speed Internal (HSI) RC Oscillator

Table 4-14 HSI Oscillator Characteristics (1) (2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	V_{DD}=3.3V, T_A = 25℃, after calibration	7.96(3)	8	8.04(3)	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	V_{DD}=3.3V, T_A = -40~105℃	-1.5	-	2	%
		V_{DD}=3.3V, T_A = -20~85℃	-0.8	-	1.5	%
		V_{DD}=3.3V, T_A = 0~70℃	-0.5	-	1.3	%
$t_{SU(HSI)}$	HSI oscillator start time	-	-	-	6	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	120	μA

Notes:

(1) V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.

(2) Guaranteed by design, not tested in production.

(3) Production calibration accuracy, excluding soldering effects. Soldering introduces a frequency deviation range of approximately ±1%.

(4) Frequency deviation includes the effects of soldering, data is from sample testing, not tested in production.

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4.3.7.2 Low Speed Internal (LSI) RC Oscillator

Table 4-15 LSI Oscillator Characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25℃ calibration, V_{DD} = 3.3V	-	32	-	KHz
		V_{DD} = 1.8 V to 3.6 V, T_A = - 40 ~ 105 ℃	28.8	32	35.2	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time	-	-	60	84	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.6	-	μA

Notes:

(1) V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.

(2) Guaranteed by characterization results, not tested in production.

4.3.8 Wake Up Time from Low Power Mode

The wake-up time listed in **Table 4-16** is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP0 or STANDBY mode: clock source is RC oscillator
- SLEEP mode: The clock source is the clock used to enter SLEEP mode

All times were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-16 Wake Time In Low Power Mode

Symbol	Parameter	Typ(1)	Unit
$t_{WUSLEEP}$	Wake up from SLEEP mode	6	Cycles
$t_{WUSTOP0}$	Wake up from STOP0 mode (regulator in run mode)	20	μs
	Wake up from STOP0 mode (regulator in low power mode)	22	μs
$t_{WUSTDBY}$	Wake up from STANDBY mode	100	μs

(1) The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.

4.3.9 PLL Characteristics

The parameters listed in **Table 4-17** are measured when the ambient temperature and power supply voltage meet the conditions in **Table 4-4**

Table 4-17 PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
f_{PLL_IN}	PLL PFD input clock(2)	4	8	50	MHz
	PLL Input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL output clock(2)	32	-	240	MHz
t_{LOCK}	PLL Ready indicates signal output time(3)	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @240MHz	-	5	-	ps
I_{PLL}	Operating Current of PLL @240MHz VCO frequency.	-	-	1500	uA

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) The correct configuration coefficients need to be used so that the f_{PLL_OUT} is within the allowable range according to the PLL input

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clock frequency.

Table 4-18 SHRTPLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
$f_{SHRTPLL\_IN}$	SHRTPLL input clock(2)	4	8	50	MHz
	SHRTPLL Input clock duty cycle	40	50	60	%
$f_{SHRTPLL\_OUT}$	SHRTPLL output clock(2)	75(3)	-	250(3)	MHz
t_{LOCK}	SHRTPLL Ready indicates signal output time(3)	10	62.5	125	μs
Jitter	RMS cycle-to-cycle jitter @250MHz	-	100	-	±ps
$I_{SHRTPLL}$	Operating Current of PLL @250MHz VCO frequency.	-	9.2	-	mA

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) The correct configuration coefficients need to be used so that the$f_{SHRTPLL_OUT}$ is within the allowable range according to the SHRTPLL input clock frequency.

4.3.10 FLASH Memory Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-19 Flash Memory Characteristics

Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
tprog	64-bit programming time	T_A = - 40 ~ 105 ℃, double word mode	-	40	-	μs
		T_A = - 40 ~ 105 ℃, buffer program mode	-	19	-	
t_{ERASE}	Page (2K bytes) erasure time	T_A = - 40 ~ 105 ℃	-	10	20	ms
t_{ME}	Mass erase time	T_A = - 40 ~ 105 ℃	-	10	20	ms
I_{DD}	The power supply current	Read mode, f_{HCLK} = 240 MHz, 4 waiting cycles, V_{DD} = 3.3V	-	4.2	5.45	mA
		Write mode, f_{HCLK} = 240 MHz, V_{DD} = 3.3V	-	6.5	-	mA
		Erase mode, f_{HCLK} = 240 MHz, V_{DD} = 3.3V	-	4.5	-	mA
		Power-down/stop mode, V_{DD} = 3.3~3.6V	-	0.05	4.65	μA
Vprog	Programming voltage	-	1.8	3	3.6	V

Note:

(1) Guaranteed by design, not tested in production.

Table 4-20 Flash Endurance And Data Retention Life

Symbol	Parameter	Condition	Min (1)	Unit
N_{END}	Endurance (note: erasure times)	T_A = -40~105 ℃, Flash size is 512 KB	10	Kcycle
t_{RET}	Data retention period	10 kcycle(2) at T_A = 85 ℃	20	Years
		10 kcycle(2) at T_A = 105 ℃	15	
		10 kcycle(2) at T_A = 125 ℃	10	

(1) Based on comprehensive evaluation, not tested in production.

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4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD，ES，LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-21 Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Max (1)	Unit
$V_{ESD(HBM)}$(2)	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 ℃, In accordance with ESDA/JEDEC JS-002-2018	C3	1000	

(1) Based on comprehensive evaluation, not tested in production.

Electromagnetic susceptibility (EMS)

Table 4-22 EMS Features

Symbol	Parameter	Condition	Level
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD = 3.3V, LQFP144,TA = 25℃, HCLK = 240MHz, conforms to IEC 61000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	VDD = 3.3V, LQFP144,TA = 25℃, HCLK = 240MHz, conforms to IEC 61000-4-4	4A
	Fast transient voltage burst and capacitively coupled clamping limits to be applied on I/O pins to induce a functional disturbance	VDD = 3.3V, LQFP144,TA = 25℃, HCLK = 240MHz, conforms to IEC 61000-4-4	4A

Static latch-up (LU)

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78A IC latch standard.

Table 4-23 Static Latch-Up

Symbol	Parameter	Condition	Type	Max (1)
LU	Static lock-up class	T_A= +125 ℃, in accordance with JESD 78E	II class A	±200mA, 1.5*VDDMAX

(1) Tested on normal temperature conditions.

4.3.12 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in **Table 4-4**. All I/O ports are CMOS and TTL compatible.

Table 4-24 I/O Static Characteristics

Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit

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V_{IL}	Input low level voltage	V_{DD}=3.3V	Vss	-	0.8	V
		V_{DD}=2.5V	Vss	-	0.7	
		V_{DD}=1.8V	Vss	-	0.3*V_{DD}	
V_{IH}	Input high level voltage	V_{DD}=3.3V	2	-	V_{DD}	
		V_{DD}=2.5V	1.7	-	V_{DD}	
		V_{DD}=1.8V	0.7*V_{DD}	-	V_{DD}	
Vhys	Schmidt trigger voltage hysteresis (1)	V_{DD}=3.3V	200	-	-	mV
		V_{DD}=2.5V	200	-	-	
		V_{DD}=1.8V	0.1*V_{DD}(2)	-	-	
I_{lkg}	Input leakage current(3)	V_{DD}=Maximum	-1	-	1	µA
		V_{PAD}=0 or V_{PAD}=V_{DD}(5)				
R_{PU}	Weak pull-up equivalent resistor (4)	VDD=3.3v,V_{IN}= Vss	80	-	220	kΩ
		VDD=1.8~3.3v,V_{IN}= Vss	60	-	500	kΩ
R_{PD}	Weak pull-down equivalent resistor (4)	VDD=3.3v,V_{IN}= VDD	80	-	220	kΩ
		VDD=1.8~3.3v,VIN= VDD	60	-	500	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Notes:

(1) The hysteresis voltage of Schmitt trigger switching level. Based on comprehensive evaluation, not tested in production.

(2) At least 100mV.

(3) If there is reverse current injection from adjacent pins, the leakage current may be higher than the maximum value.

(4) Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

(5) V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

Output driving current

GPIO (universal input/output port) can absorb or output up to +/-12mA current. In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in Section 4.2.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating value I_{VDD} (Table 4-2)
- The sum of the currents sourced by all the I/Os on Vss, plus the maximum consumption of the MCU sourced on Vss, cannot exceed the absolute maximum rating value I_{VSS} (Table 4-2)

Output voltage

Unless otherwise specified, the parameters listed in **Table 4-26** were measured using ambient temperature and V_{DD} supply voltage in accordance with **Table 4-4**. All I/O ports are CMOS and TTL compatible

Table 4-25 IO Output Drive Capability Characteristics(1)

Drive Capability	I_{OH}, VDD=3.3V	I_{OL}, VDD=3.3V	I_{OH}, VDD=2.5V	I_{OL}, VDD=2.5V	I_{OH}, VDD=1.8V	I_{OL}, VDD=1.8V	Unit
2	-2	2	-1.5	1.5	-1	1	mA
4	-4	4	-3	3	-2	2	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7	8	mA

(1) Guaranteed by design, not tested in production.

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Table 4-26 Output Voltage Characteristics(3)

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD}=3.3V，I_{OL}(4)= 2/4/8/12	V_{SS}	0.4	V
		V_{DD}=2.5V，I_{OL}(4)= 2/4/8/12	V_{SS}	0.4	
		V_{DD}=1.8V，I_{OL}(4)= 2/4/8/12	V_{SS}	0.2*V_{DD}	
V_{OH}(2)	Output high level	V_{DD}=3.3V，I_{OH}(4)= 2/4/8/12	2.4(5)	V_{DD}	
		V_{DD}=2.5V，I_{OH}(4)= 2/4/8/12	1.8(5)	V_{DD}	
		V_{DD}=1.8V，I_{OH}(4)= 2/4/8/12	0.8*V_{DD}	V_{DD}	

Notes:

(1) The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.

(2) The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.

(3) Data based on characterization results, not tested in production

(4) Actual drive capability see Table 4-25.

(5) PC13, PC14, PC15 are not within this range.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in **Figure 4-5** and **Table 4-27** respectively.

Unless otherwise specified, the parameters listed in **Table 4-27** were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-27 Input/Output AC Characteristics (1)

DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=5pF,V_{DD}=3.3V	-	75	MHz
			C_L=5pF,V_{DD}=2.5V	-	50	
			C_L=5pF,V_{DD}=1.8V	-	30	
	$t_{(IO)out}$	Output delay	C_L=5pF,V_{DD}=3.3V	-	3.7	ns
			C_L=5pF,V_{DD}=2.5V	-	4.8	
			C_L=5pF,V_{DD}=1.8V	-	7.2	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns
10 (4mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=10pF,V_{DD}=3.3V	-	90	MHz
			C_L=10pF,V_{DD}=2.5V	-	60	
			C_L=10pF,V_{DD}=1.8V	-	40	
	$t_{(IO)out}$	Output delay	C_L=10pF,V_{DD}=3.3V	-	3.5	ns
			C_L=10pF,V_{DD}=2.5V	-	4.5	
			C_L=10pF,V_{DD}=1.8V	-	6.8	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
01 (8mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=20pF,V_{DD}=3.3V	-	100	MHz
			C_L=20pF,V_{DD}=2.5V	-	75	
			C_L=20pF,V_{DD}=1.8V	-	50	
	$t_{(IO)out}$	Output delay	C_L=20pF,V_{DD}=3.3V	-	3.5	ns
			C_L=20pF,V_{DD}=2.5V	-	4.8	
			C_L=20pF,V_{DD}=1.8V	-	6.6	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
11 (12mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=30pF,V_{DD}=3.3V	-	120	MHz
			C_L=30pF,V_{DD}=2.5V	-	90	
			C_L=30pF,V_{DD}=1.8V	-	60	
	$t_{(IO)out}$	Output delay	C_L=30pF,V_{DD}=3.3V	-	3.4	ns

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DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
			C_L=30pF,V_{DD}=2.5V	-	4.3	
			C_L=30pF,V_{DD}=1.8V	-	6.4	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	

Notes:

(1) The speed of the I/O port can be configured via PMODEy [1:0]. Refer to the N32H481 user manual for instructions on configuring registers for GPIO ports.

*(2) The maximum frequency is defined in **Figure 4-5**.*

Figure 4-5 Definition Of Input/Output AC Characteristics

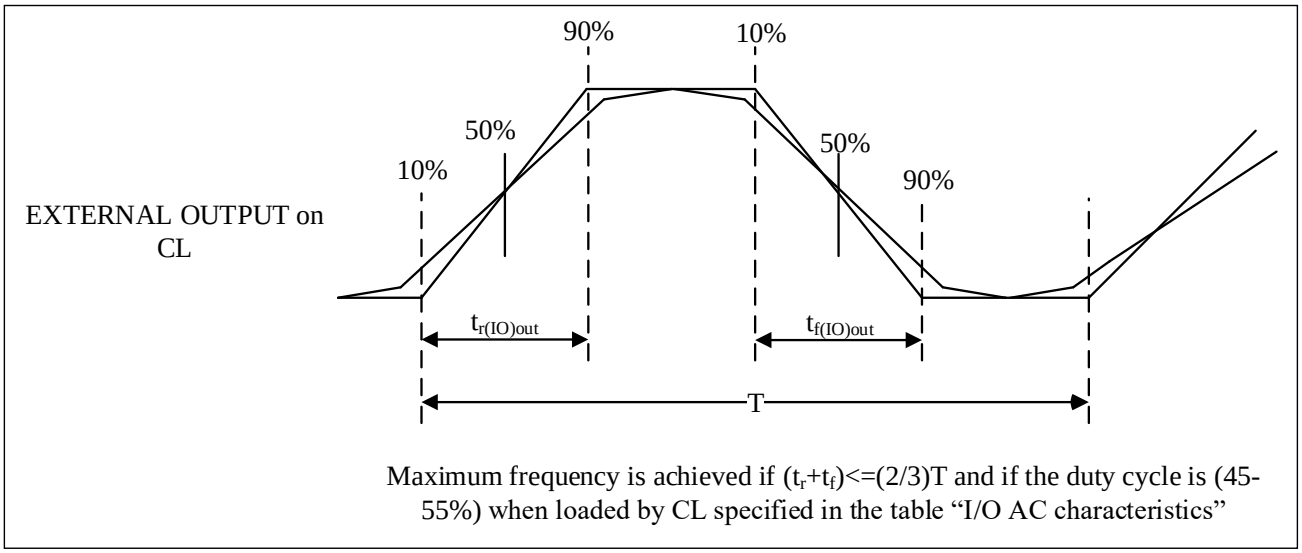
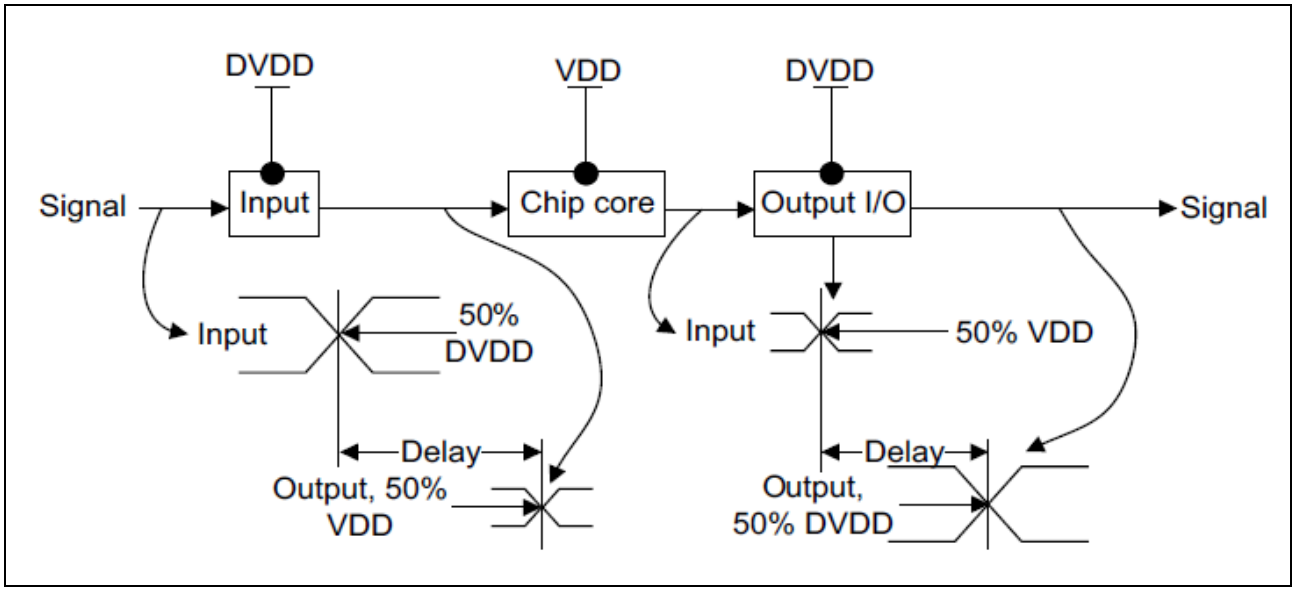


Figure 4-6 Transmission Delay



4.3.13 NRST Pin Characteristics

The NRST pin input driver uses the CMOS process, which is connected to an unbreakable pull-up resistor, R_{PU} (see **Table 4-28**). Unless otherwise specified, the parameters listed in **Table 4-28** were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

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Table 4-28 NRST Pin Characteristics

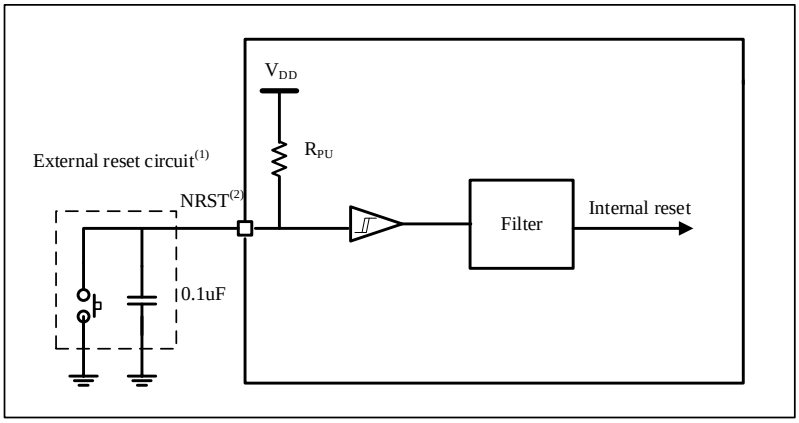
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	V_{SS}	-	0.3*V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.7*V_{DD}	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance(2)	V_{IN}= V_{SS}	30	50	80	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	VDD=3.3V	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	VDD=3.3V	300	-	-	ns

Notes:

(1) Guaranteed by design, not tested in production.

(2) The pull-up resistor is designed as a real resistor in series for a switchable PMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-7 Recommended NRST Pin Protection



Notes:

(1) Acts as a filter.

*(2) The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in **Table 4-28**, otherwise the MCU cannot be reset.*

4.3.14 Timer Characteristics

The parameters listed in **Table 4-29**, **Table 4-30**, **Table 4-31**, **Table 4-32** are guaranteed by design, not tested in production.

See section 4.3.12 for details on the features of the I/O alternate function pins (output comparison, input capture, external clock, PWM output).

Table 4-29 ATIM1/2/3 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	4.16	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 240MHz	0	120	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	0.00416	273	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$

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Symbol	Parameter	Condition	Min	Max	Unit
		$f_{TIMxCLK}$= 240MHz	-	17.9	s

(1) Guaranteed by design, not tested in production.

Table 4-30 GTIM1/2/3/4/5/6/7 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	8.33	-	ns
		$f_{TIMxCLK}$= 180MHz	5.56	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 120MHz	0	60	MHz
		$f_{TIMxCLK}$= 180MHz	0	90	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	0.00833	546	µs
		$f_{TIMxCLK}$= 180MHz	0.00556	364	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	-	35.8	s
		$f_{TIMxCLK}$= 180MHz	-	23.9	s

(1) Guaranteed by design, not tested in production.

Table 4-31 GTIM8/9/10 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	4.16	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 240MHz	0	120	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	0.00416	273	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	-	17.9	s

(1) Guaranteed by design, not tested in production.

Table 4-32 LPTIMER1/2 Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Maximum possible count	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	8.33	-	ns
f_{EXT}	Maximum possible count	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 120MHz	0	60	MHz
Res_{TIM}	Maximum possible count	-	-	16	bit
$t_{COUNTER}$	Maximum possible count	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	0.00833	546	µs
t_{MAX_COUNT}	Maximum possible count	-	-	128x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	-	69.9	ms

(1) Guaranteed by design, not tested in production.

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4.3.15 Watchdog Characteristics

Table 4-33 IWDG Counting Maximum And Minimum Reset Time (LSI = 32 Khz)

Prescaler	PD[2:0]	Min timeout RL[11:0] = 0	Max timeout RL[11:0] = 0xFFF	Unit
/4	000	0.125	512	ms
/8	001	0.25	1024	
/16	010	0.5	2048	
/32	011	1.0	4096	
/64	100	2.0	8192	
/128	101	4.0	16384	
/256	11x	8.0	32768	

(1) Guaranteed by design, not tested in production.

Table 4-34 WWDG Counting Maximum And Minimum Reset Time (PCLK1 = 120 Mhz)

Prescaler	TIMERB[1:0]	Min timeout	Max timeout	Unit
/1	0	0.0341	556.92	ms
/2	1	0.0682	1113.84	
/3	2	0.136	2227.68	
/4	3	0.273	4455.36	

(1) Guaranteed by design, not tested in production.

4.3.16 I²C Interface Characteristics

Unless otherwise specified, the parameters listed in **Table 4-35** were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

The I²C interface of the N32H481 product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open-drain pins, and when configured for open-drain output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in **Table 4-35**. See Section 4.3.12 for details about the features of the input/output alternate function pins (SDA and SCL).

Table 4-35 I²C Interface Characteristics(1)

Symbol	Parameter	Standard mode		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data hold time	300	-	300	-	0	-	μs
$t_{su(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns

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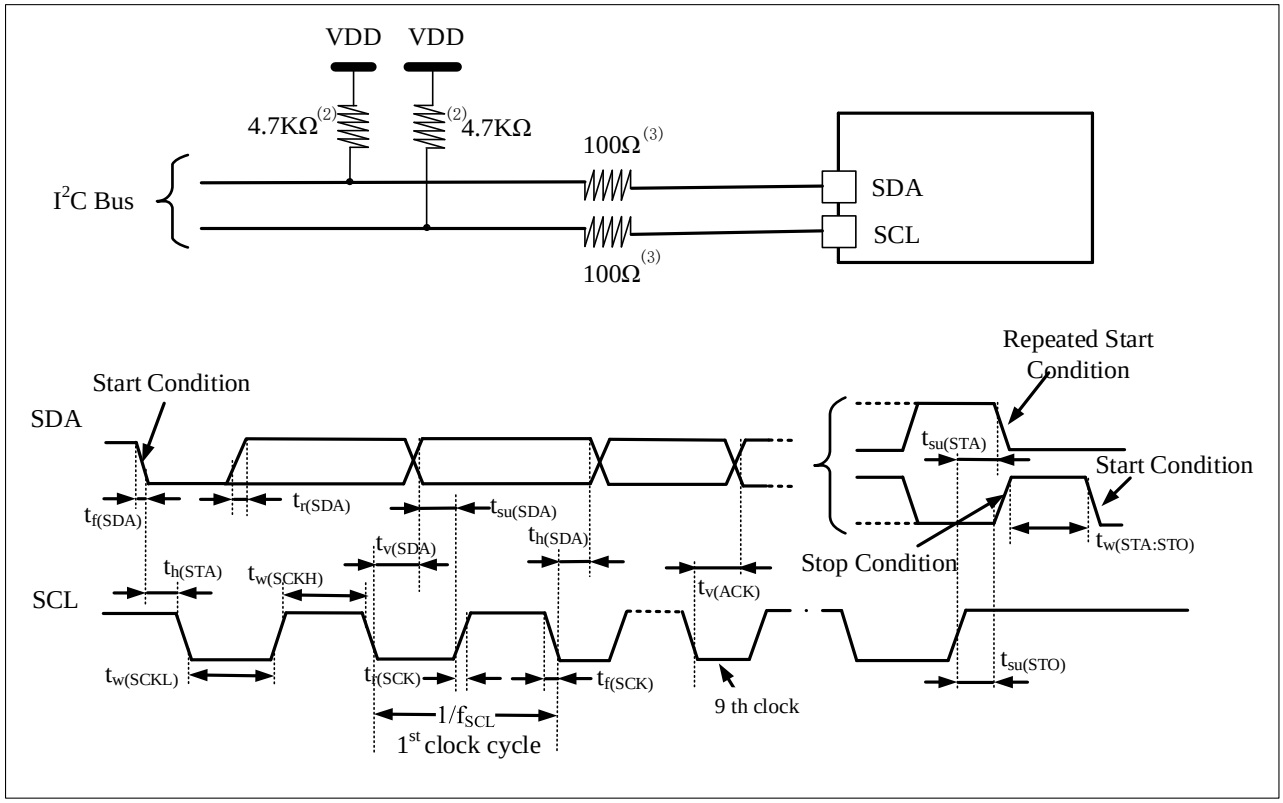
Symbol	Parameter	Standard mode		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	µs
Cb	Capacitive load per bus	-	400	-	400	-	550	pf
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	µs
$t_{v\ (ACK)}$	Response time	-	3.45	-	0.9	-	0.45	µs
t_{SP}	Spike pulse width to be suppressed by the input filter	-	-	0	50	0	50	ns

(1) Guaranteed by design, not tested in production.

Figure 4-8 I²C Bus AC Waveform And Measuring Circuit (1)



Notes:

(1) The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

(2) The pull-up resistance depends on the I²C interface speed.

(3) The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.17 SPI/I²S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in **Table 4-36** and the I²S parameters listed in **Table 4-37** are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

See Section 4.3.12 for details on the characteristics of the I/O multiplexed pins (NSS, SCLK, MOSI, MISO for SPI,

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WS, CLK, SD for I²S).

Table 4-36 SPI Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	-	60	MHz
		Slave mode	-	-	40	
DuCy(SCK)	SPI from the input clock duty cycle	SPI slave mode	45	50	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Master mode	$t_{SCLK}/2$	-	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$t_{SCLK}/2$	-	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode	$t_{SCLK}/2$ - 1	$t_{SCLK}/2$	$t_{SCLK}/2$ + 1	
$t_{su(MI)}$(1)	Data entry setup time	Master mode	3	-	-	
$t_{su(SI)}$(1)		Slave mode	3.5	-	-	
$t_{h(MI)}$(1)	Data entry hold time	Master mode	2.5	-	-	
$t_{h(SI)}$(1)		Slave mode	2	-	-	
$t_{a(SO)}$(1)(2)	Data entry hold time	Slave mode	9	-	$2*t_{SCLK}/2$	
$t_{dis(SO)}$(1)(3)	Data entry hold time	Slave mode	9	-	16	
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after enable edge)	-	9	13	
$t_{v(MO)}$(1)		Master mode (after enable edge)	-	3	5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	5	-	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	0	-	-	

Notes:

(1) Guaranteed by design, not tested in production.

(2) The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.

(3) The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-9 SPI Timing Diagram-Slave Mode And CPHA=0

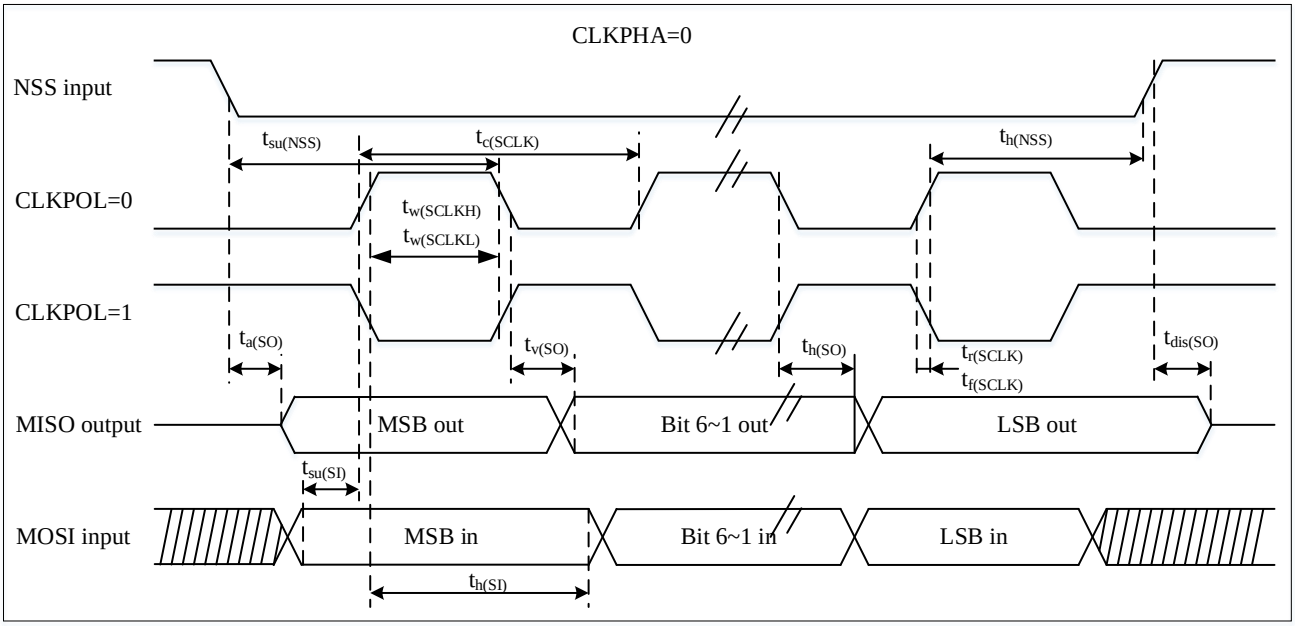

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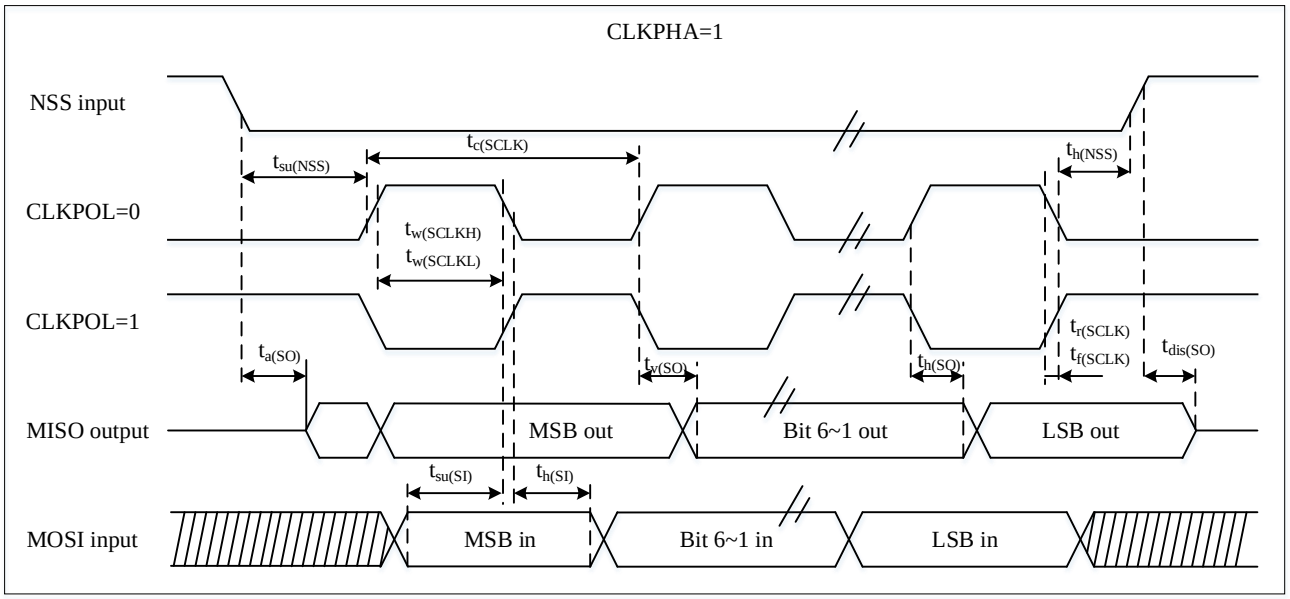
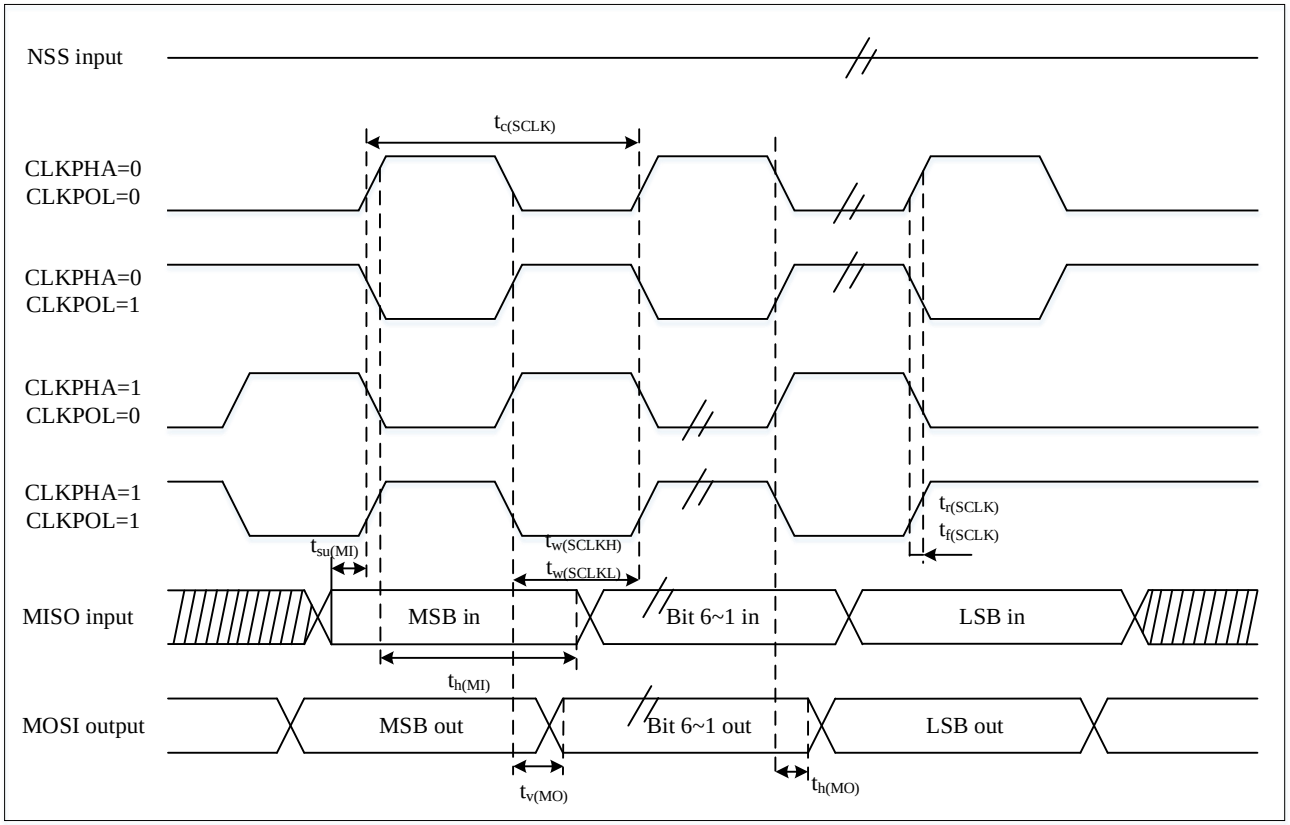
Figure 4-10 SPI Timing Diagram-Slave Mode And CPHA=1 (1)



(1) The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-11 SPI Timing Diagram-Master Mode (1)



(1) The measuring point is set at the CMOS level: 0.3V and $0.7V_{DD}$.

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Table 4-37 I²S Characteristics (1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{MCLK}	I²S main clock frequency	Master mode		256x8K	256Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I²S clock frequency	Master mode (32 bit)		-	64Fs(3)	
		Slave mode (32 bit)		-	64Fs(3)	
DuCy(SCK)	I²S input clock duty cycle	I²S slave mode		30	70	%
$t_{v(WS)}$ (1)	WS valid time	Master mode	I2S2	-	6	
			I2S3	-	6	
$t_{h(WS)}$(1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	2		
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	7	-	
			I2S3	7	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I2S2	0	-	
			I2S3	0	-	
$t_{w(CLKH)}$(1)	CLK high and low times	Master mode, f_{PCLK} = 16MHz, audio 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	I2S2	6	-	
			I2S3	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S2	7	-	
			I2S3	7	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	I2S2	0	-	
			I2S3	0		
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S2	1	-	
			I2S3	1		
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	I²S2	-	15	
			I²S3	-	15	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	I²S2	4	-	
			I²S3	4	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	6	
			I2S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge))	I2S2	0	-	
			I2S3	0	-	

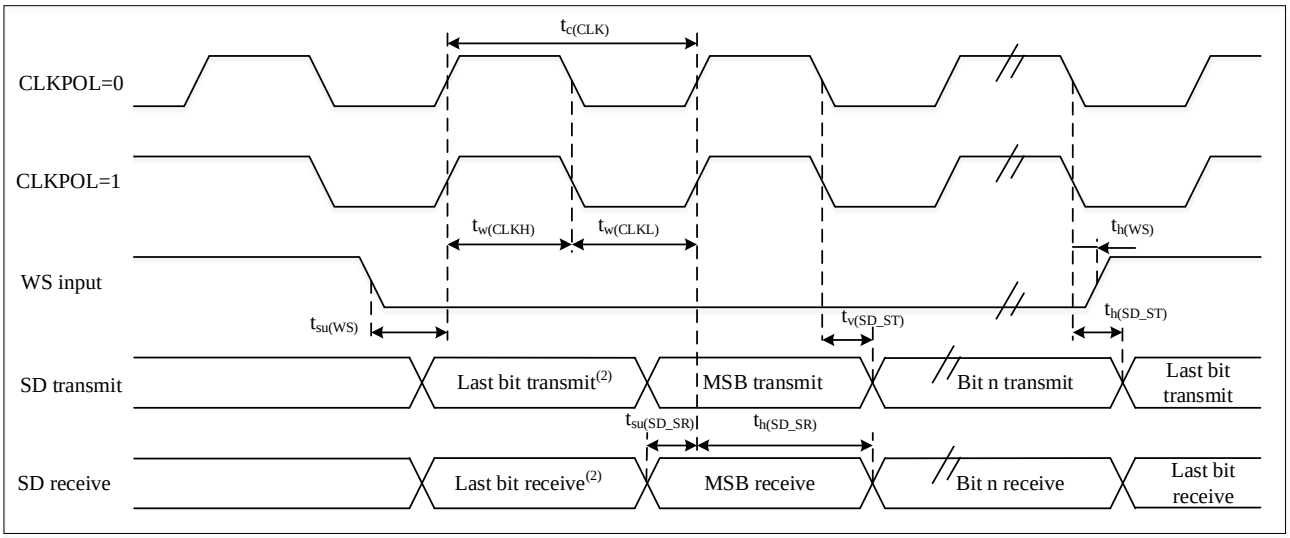
Notes:

(1) Guaranteed by design, not tested in production.

(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK}=1/f_{PCLK} =125ns.

(3) Audio signal sampling frequency.

Figure 4-12 I²S Slave Mode Timing Diagram (Philips Protocol) (1)



Notes:

(1) The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

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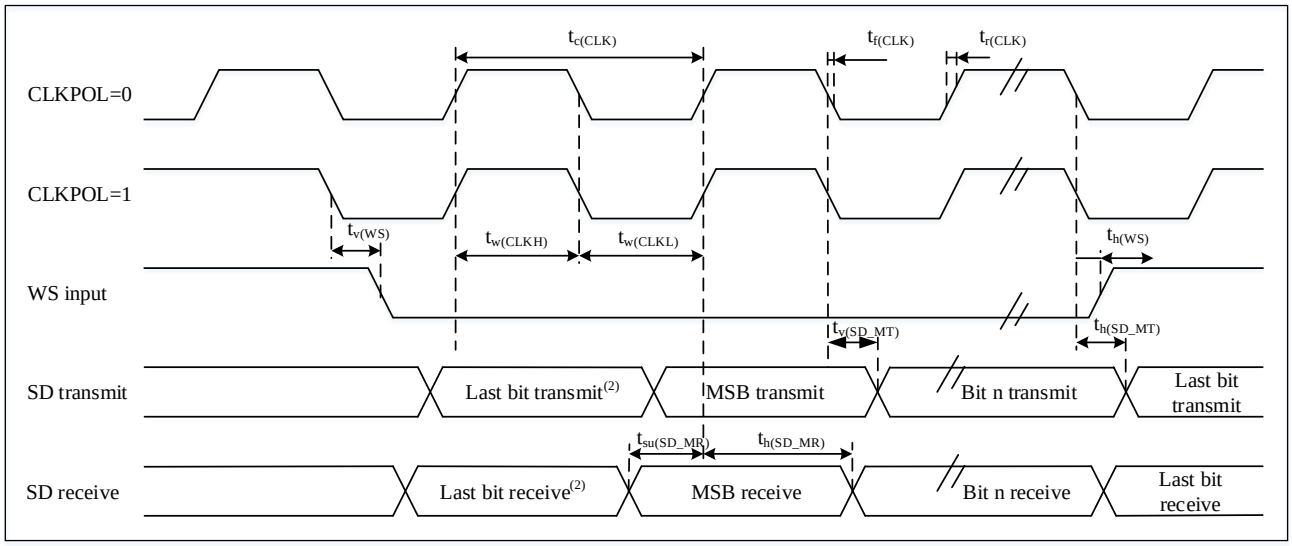
(2) Transmit/receive of the last byte.There is no least significant transmit/receive before the first byte.

Figure 4-13 I²s Master Mode Timing Diagram (Philips Protocol) (1)



Notes:

(1) The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

(2) Send/receive of the last byte. There is no least significant send/receive before the first byte.

4.3.18 xSPI Characteristics

Table 4-38 Characteristics Of XSPI In SDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$		$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	
$t_{s(IN)}$	Data input setup time	2.5	-	-	ns
$t_{h(IN)}$	Data input hold time	5.5	-	-	ns
$t_{v(OUT)}$	Data output valid time	-	2.5	3.5	ns
$t_{h(OUT)}$	Data output hold time	2.5	-	-	ns

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Figure 4-14 Timing Of XSPI In SDR Mode

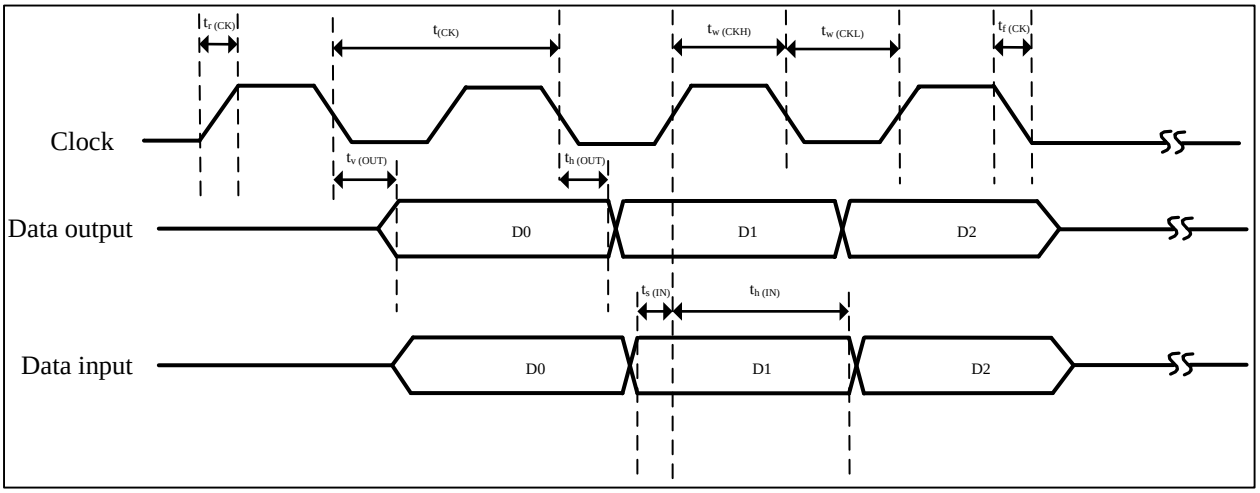

Table 4-39 Features Of XSPI In DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$		$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	ns
$t_{sf(IN)}$	Data input setup time	3	-	-	ns
$t_{sr(IN)}$		5	-	-	ns
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time	2	-	-	ns
$t_{vf(OUT)}$;$t_{vr(OUT)}$	Data output valid time	-	-	5	ns
$t_{hf(OUT)}$;$t_{hr(OUT)}$	Data output hold time	4	-	-	ns

Figure 4-15 Timing Of XSPI In DDR Mode

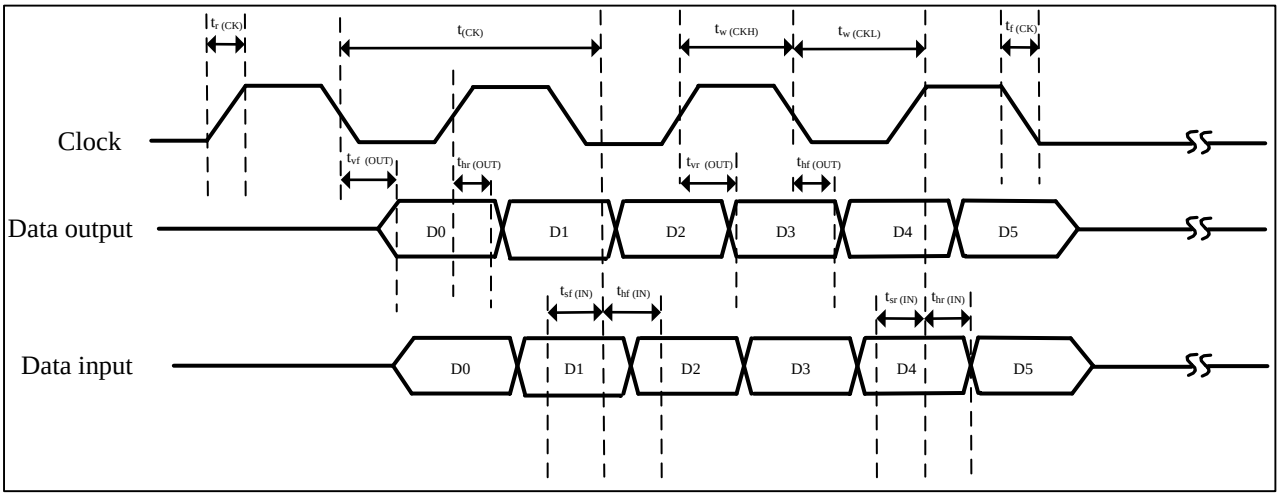

Table 4-40 Features Of XSPI In RXDS Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	t(CK)/2-0.5	-	t(CK)/2	ns
$t_{w(CKL)}$		t(CK)/2-0.5	-	t(CK)/2	
$t_{v(CLK)}$	clock valid time	-	-	t(CK)+2	

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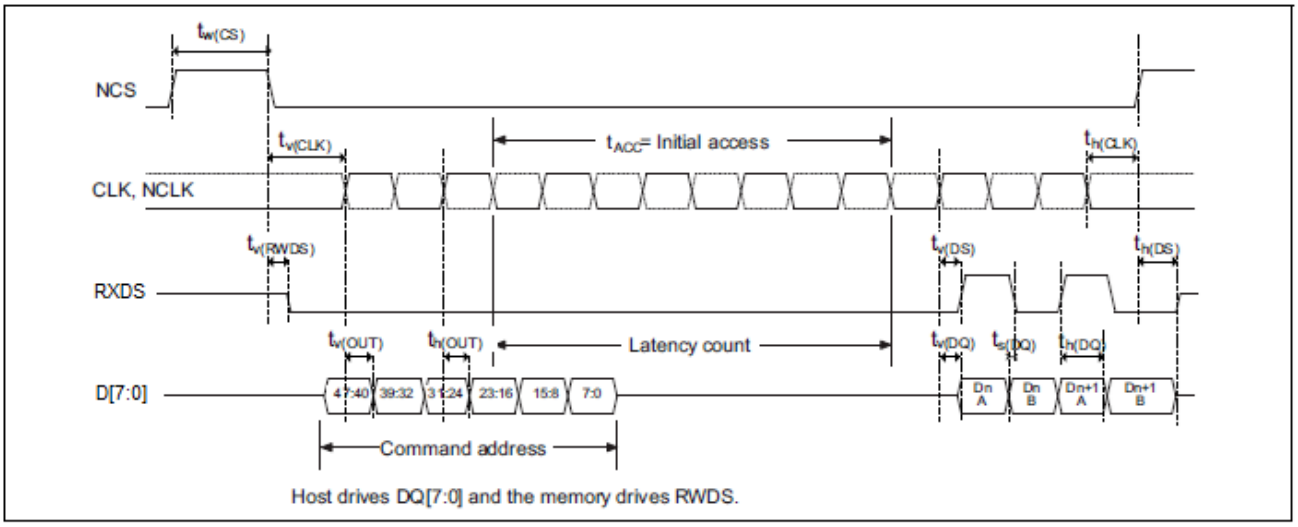
$t_{h(CLK)}$	clock high time	t(CK)+0.5	-	-	
$t_{w(CS)}$	chip select high time	3*t(CK)	-	-	
$t_{v(DQ)}$	Data input valid time	0	-	-	
$t_{v(DS)}$	Data selection input valid time	0	-	-	
$t_{h(DS)}$	Data selection input hold time	0	-	-	
$t_{v(RWDS)}$	Data selection output valid time	-	-	3*t(CK)	
$t_{sf(DQ)}$;$t_{sr(DQ)}$	Input data setup time	3	-	-	ns
$t_{hf(DQ)}$; $t_{hr(DQ)}$	Input data hold time	2	-	-	ns
$t_{vf(OUT)}$;$t_{vr(OUT)}$	Output data setup time	-	6	7	ns
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Output data hold time	3.5	-	-	ns

Figure 4-16 Timing Of XSPI In RXDS Mode



4.3.19 USB_HS_DualRole Characteristics

Table 4-41 USBHS DC Electrical Characteristics

Symbol		Parameter	Condition	Min	Typ	Max	Unit
VDD (1)		USB operating voltage	-	3	-	3.6	V
LS/FS FUNCTIONALITY							
Input levels(1)	VDIFS	Differential input sensitivity (FS/LS)	-	0.2	-	-	V
	VCMFS	Differential common mode range (FS/LS)	Includes V_{DI} range	0.8	-	2.5	
	VILSE	Single ended receive low voltage(FS/LS)	-	-	-	0.8	
	VIHSE	Single ended receive high voltage(FS/LS)	-	2.0	-	-	
Output levels(1)	VOLFS	Static output level low (FS/LS)	RL of 1.5kΩ to 3.6V	-	-	0.3	
	VOHFS	Static output level high (FS/LS)	RL of 15 kΩ to VSS	2.8	3.3	3.6	
RPD(1)		USBHS_DM/DP	VIN = VDD	-	15	-	kΩ

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RPU(1)		USBHS_DM/DP	VIN = VSS	-	1.5	-	
ZHSDRV(1)		Driver output impedance	Steady-state driving	-	45	-	Ω
HS FUNCTIONALITY							
Input levels(1)	DIHS	Differential input sensitivity (HS)	-	0.1	-	-	V
	VCMHS	Differential common mode range (HS)	-	-50	-	500	mV
	VHSSQ	HS overshoot detection threshold	-	100	-	150	
	VHSDSC	HS dropout threshold	-	525	-	625	
Output levels(1)	VOLHS	High-speed low-level output voltage	45Ω	-10	-	10	
	VOHHS	High-speed high-level output voltage	45Ω	360	400	440	

Notes:

(1) Guaranteed by design, not tested in production.

Table 4-42 USB Dynamic Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{FR}	Rising time (FS/LS)	C_L = 50 pF	4	-	20	ns
T_{HSR}	Differential rising time (HS)	-	500	-	-	ps
T_{FF}	Falling time (FS/LS)	C_L = 50 pF	4	-	20	ns
T_{HSF}	Differential falling time (HS)	-	500	-	-	ps
v_{CRS}	Output single-ended crosstalk voltage (FS/LS)	-	1.3	-	2	V

Notes:

(1) Guaranteed by design, not tested in production.

4.3.20 Electrical Parameters of 12 bit Analog-to-Digital Converter (ADC)

Unless otherwise specified, the parameters in **Table 4-43** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Note: It is recommended to perform a calibration at each power-on.

Table 4-43 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	The power supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	-	-	80	MHz
f_s	Sampling rate(1)	VDDA ≥ 2.4V	-	-	4.7	Msps
		1.8V ≤ VDDA < 2.4V	-	-	4	
V_{AIN}	Switching voltage range(2)	-	0 (V_{SSA} or V_{REF-} Connect to ground)	-	V_{REF+}	V
R_{ADC}	Sampling switch resistance	2.4~3.3V	-	-	300	ohm
		1.8~2.4V	-	-	480	
C_{ADC}	Internal sampling and holding capacitors	-	-	5	-	pF
SNDR	Singal noise distortion ration	-	-	65	-	dBFS
T_{cal}	The calibration time	-	82			$1/f_{ADC}$

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_S	Sampling time	fADC = 80 MHz(fast channel)	0.0563	-	7.52	μs
		fADC = 80 MHz(slow channel)	0.0625		8.35	
T_S(1)	Sampling cycles	fADC = 80 MHz(fast channel)	0.0938	-	7.52	$1/f_{ADC}$
		fADC = 80 MHz(slow channel)	4.5	-	601.5	
Ts	Power on time	-	4.5	-	601.5	μs
t_{CONV}(2)	Total conversion time (including sampling time)	-	8~614 (Sampling T_S + 6.5/8.5/10.5/12.5 for successive approximation)			$1/f_{ADC}$

Notes:

(1) Guaranteed by design, not tested in production.

(2) According to different packages, V_{REF+} connected to V_{DDA} internally, and V_{REF-} connected to V_{SSA} internally.

(3) Sampling time/sampling rate is related to the input impedance Rin. The correspondence between the maximum input impedance Rin and the sampling time is shown in Table 4-44.

Table 4-44 ADC Sampling Time(1)

Resolution	Rin（kΩ）	Minimum Sampling Time (ns)			
		Vdda=2.4V to 3.6V , Vddd=1.1 V, selrange_ldo=L, Tjunction=125 ℃, fclk=80 MHz		Vdda=1.8V to 2.4V, Vddd=1.1 V, selrange_ldo=L, Tjunction=125 ℃, fclk=80 MHz.	
		Fast Channel	Slow Channel	Fast Channel	Slow Channel
12-bit	0.14	45.0	73.0	79.0	103.0
	0.6	79.0	103.0	300.0	345.0
	4.6	300.0	345.0	576.0	651.0
	9.5	576.0	651.0	1131.0	1257.0
	19	1131.0	1257.0	2776.0	3051.0
	48	2776.0	3051.0	5475.0	5982.0
10-bit	0.14	39.0	61.0	64.0	88.0
	0.6	64.0	88.0	250.0	357.0
	4.6	250.0	357.0	478.0	540.0
	9.5	478.0	540.0	935.0	1040.0
	19	935.0	1040.0	2294.0	2526.0
	48	2294.0	2526.0	4532.0	4963.0
8-bit	0.14	33.0	50.0	52.0	71.0
	0.6	52.0	71.0	202.0	234.0
	4.6	202.0	234.0	391.0	457.0
	9.5	391.0	457.0	800.0	1012.0
	19	800.0	1012.0	1838.0	2027.0
	48	1838.0	2027.0	3632.0	3984.0
6-bit	0.14	27.0	40.0	41.0	56.0
	0.6	41.0	56.0	153.0	177.0
	4.6	153.0	177.0	292.0	330.0
	9.5	292.0	330.0	569.0	642.0
	19	569.0	642.0	1435.0	1666.0
	48	1435.0	1666.0	3001.0	3919.0

Notes:

(1) Guaranteed by design, not tested in production.

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Table 4-45 ADC Accuracy-Limited Test Conditions (1) (2)

Symbol	Parameter	Condition	Typ	Max (3)	Unit
ET(4)	Comprehensive error	f_{HCLK} = 240MHz, f_{ADC} = 240MHz, sample Rate = 1.75M SPS, V_{DDA} = 3.3V, T_A = 25 ℃ Measurements are made after the ADC is calibrated $V_{REF+} = V_{DDA}$	1.3	5	LSB
EO(4)	Offset error		1	3	
ED	Differential linear error		1	2.2	
EL	Integral linear error		2	3	

Notes:

(1) The DC accuracy of the ADC is measured after internal calibration.

(2) ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin.It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current.

*(3) The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in **Table 4-2***

(4) Based on comprehensive evaluation, not tested in production.

Figure 4-17 ADC Precision Characteristics

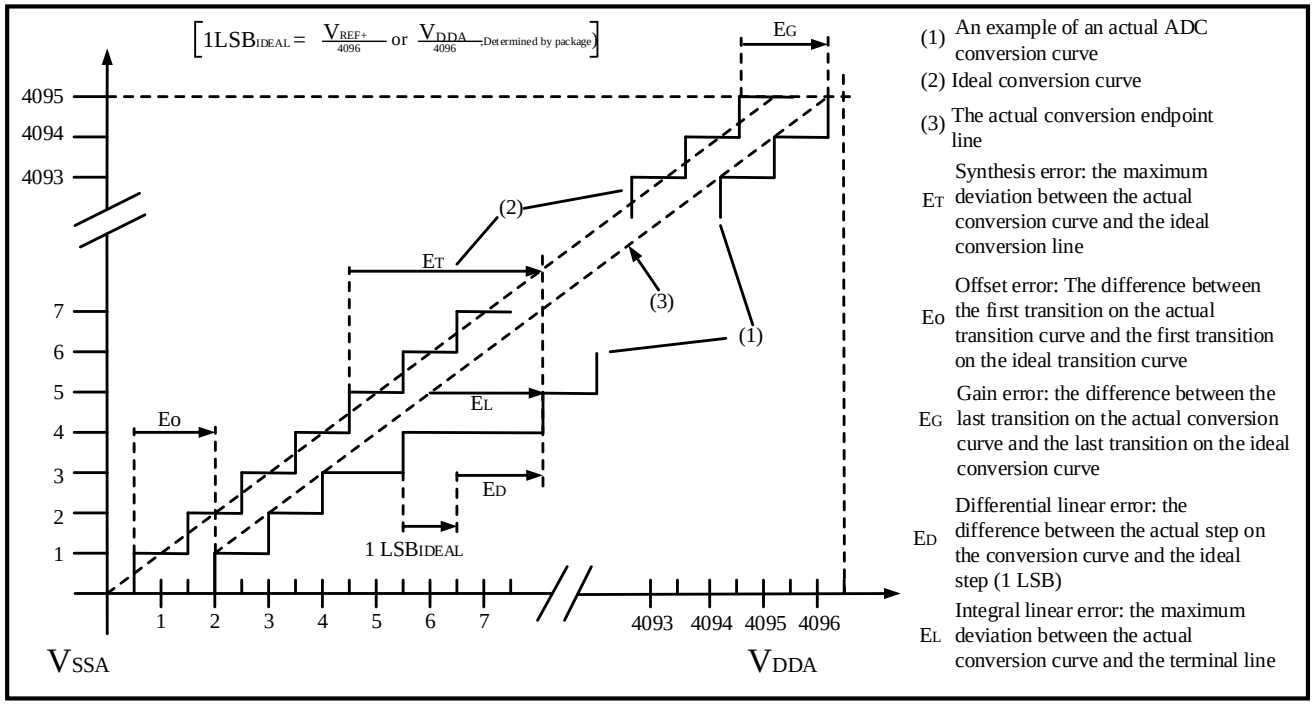

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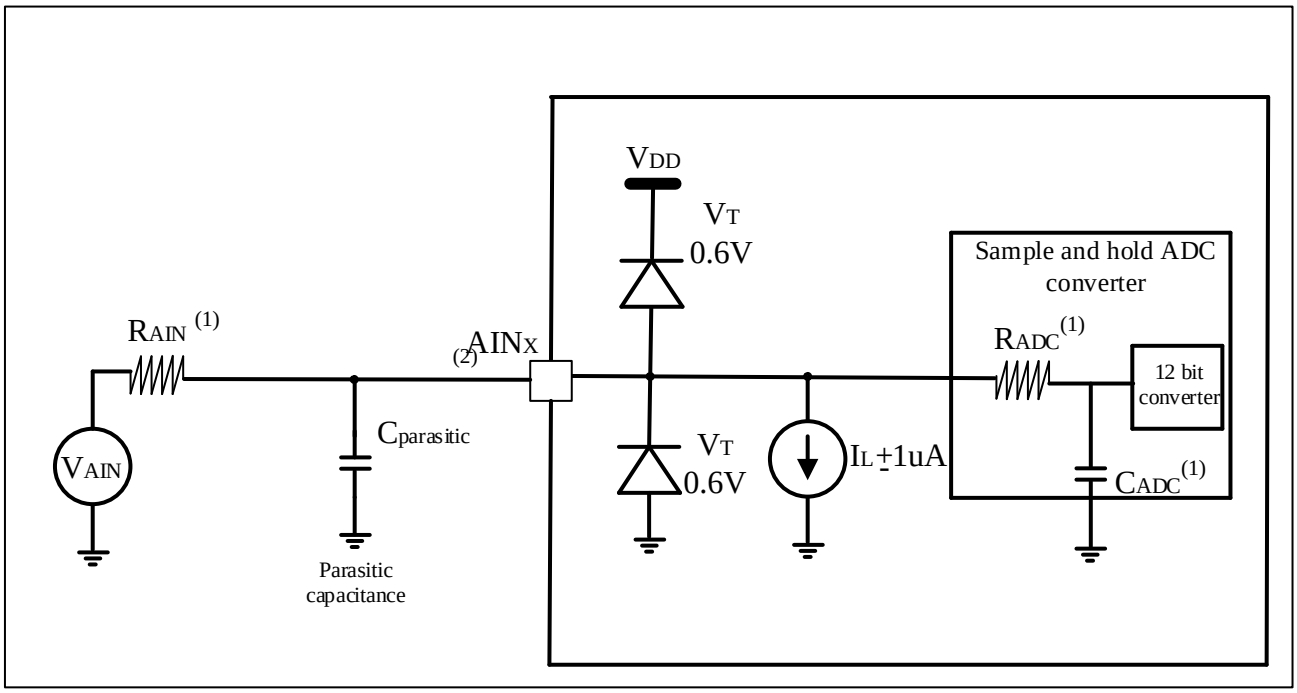
Figure 4-18 Typical Connection Diagram Using ADC



Notes:

(1) For values of R_{AIN}, R_{ADC}, and C_{ADC}, see Table 4-43.

(2) $C_{parasitic}$ indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF).A larger $C_{parasitic}$ value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC} from medine.

4.3.21 12-bit DAC Electrical Parameters

Unless otherwise specified, the parameters of **Table 4-46** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions of **Table 4-4**.

Table 4-46 DAC 1MSPS Characteristics(1)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	DAC output buffer disabled, output only internally connected		2.4	-	3.6	V
V_{REF+}	Positive reference voltage	DAC output buffer disabled, output only internally connected		2.4	-	VDDA	
V_{REF-}	Negative reference voltage	-		VSSA			
R_L	Resistive load with buffer enable	DAC output Buffer enable	Connected to VSSA	5	-	-	kΩ
			Connected to VDDA	25	-	-	
Ro	Impedance output	DAC output buffer disable		10.3	12.3	15.7	kΩ
C_L	Capacitive load	-		-	-	50	pF
DAC_OUT	DAC_OUT output voltage	Output buffer enable		0.2	-	V_{REF+} - 0.2	V
		Output buffer disable		0	-	V_{REF+}	-
I_{DD}	Static mode (standby mode)	-		-	425	600	μA

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	DAC DC consumption ($V_{DDD+}V_{DDA+}V_{REF+}$)	-	-	500	700	μA
$t_{SETTLING}$	Settling time (full range: 12-bit input code transitioning from minimum value to maximum value, DAC_OUT reaching its final value within ±1 LSB)	DAC buffer enable, CL ≤ 50 pF,RL ≥ 5 kΩ	-	3	4.1	μs
		DAC buffer disable	-	2.1	2.6	
t_{WAKEUP}	Wake-up time from shutdown state (from enabling DAC to DAC_OUT reaching its final value within ±1 LSB)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ	-	4.2	7.5	μs
		DAC buffer disable, CL ≤ 10 pF	-	2.1	5	
PSRR	Power supply rejection ratio (relative to V_{DD}33A) (static DC measurement)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ	-	-80	-28	dB
TW_to_W	The minimum time between two consecutive writes to the DACx_DATO register to ensure that small changes in the input code result in the correct DAC_OUT(1 LSB)。DACxy_CTRL.EXOUT = 1, DACxy_CTRL. BxEN = 1	CL ≤ 50 pF, RL ≥ 5 kΩ	1	-	-	μs
	DACxy_CTRL.EXOUT = 1, DACxy_CTRL. BxEN = 0 or DACxy_CTRL.INOUT = 1, DACxy_CTRL. BxEN = 0	CL ≤ 10 pF	1.4	-	-	
Voffset	Middle code offset for 1 trim code step	VREF+ =3.6V	-	-	1500	μV
$I_{DDA(DAC)}$	DAC consumption from VDDA	DAC buffer enable, No load, input mid-value 0x800	-	325	500	μA
		DAC buffer enable, No load, input max-value 0xF1C	-	450	670	
		DAC buffer disable, No load, input mid-value 0x800	-	-	0.25	
$I_{DDV(DAC)}$	DAC consumption from VREF+	DAC buffer enable, No load, input mid-value 0x800	-	185	240	μA
		DAC buffer enable, No load, input max-value 0xF1C	-	340	400	
		DAC buffer disable, No load, input mid-value 0x800	-	155	205	
DNL	Nonlinear distortion (deviation between two consecutive codes)	-	-	-	±2	LSB
INL	Nonlinear accumulation (deviation measured at code i from the line connecting code 0 and code 4095)	-	-	-	±6	LSB
Offset	Offset error (value measured at code 0x800)	Output buffer enable,CL ≤ 50 pF,RL ≥ 5 kΩ, VREF+ =3.6V	-	-	±12	LSB
		Output buffer enable,CL ≤ 50 pF,RL ≥ 5 kΩ, VREF+ =1.8V	-	-	±25	
		Output buffer disable,CL ≤ 50 pF, noRL	-	-	±8	
Gain Error	Gain error	-	-	±0.5	-	%

(1) Guaranteed by design, not tested in production.

4.3.22 Voltage Reference Buffer (VREFBUF) Characteristics

Unless otherwise specified, the parameters in **Table 4-47** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

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Table 4-47 VREFBUF Characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V_{REFBUF_OUT}	Voltage reference output	VRS= 00，T_A=25℃	2.044	2.048	2.052	
		VRS= 01，T_A=25℃	2.496	2.5	2.504	
		VRS= 10，T_A=25℃	2.896	2.9	2.904	
TRIM	Trim step resolution	-	-	±0.05	±0.1	%
CL	Load capacitor	-	0.5	1	2	µF
PSRR	Power supply rejection	DC	48.9	74.7	-	dB
		100KHz	25	40	-	
t_{START}	Start-up time	CL =1 µF	-	500	650	µs
$I_{DDA(VREFBUF)}$	VREFBUF consumption from VDDA	Iload <= 10 mA	-	45	80	µA

Note: (1)Guaranteed by design, not tested in production.

4.3.23 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in **Table 4-48** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Table 4-48 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±3	℃
Avg_Slope(1)	Average slope	-3.7	-4	-4.3	mV/℃
V_{25}(1)	Voltage at 25℃	-	1.32	-	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(3)	ADC sampling time when reading the tempearture	-	-	3	µs

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Shortest sampling time can be determined in the application by multiple iterations.

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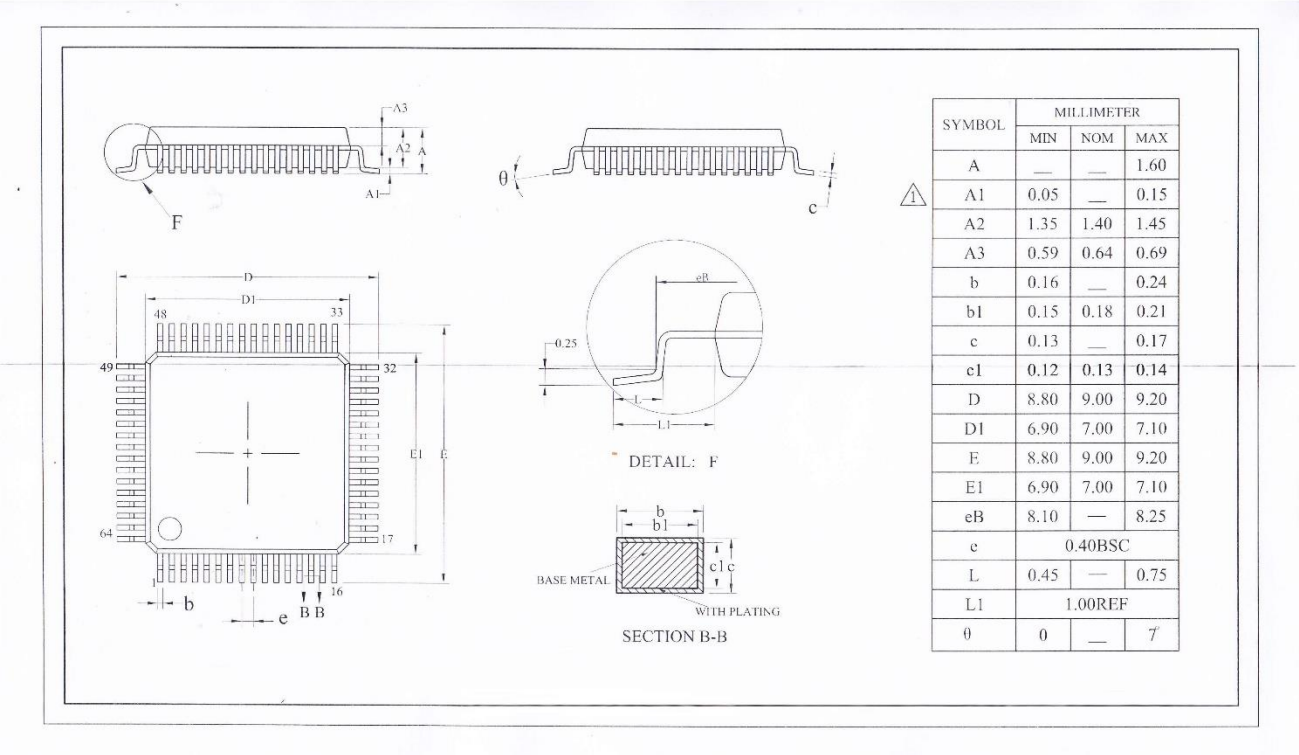
5 Packages

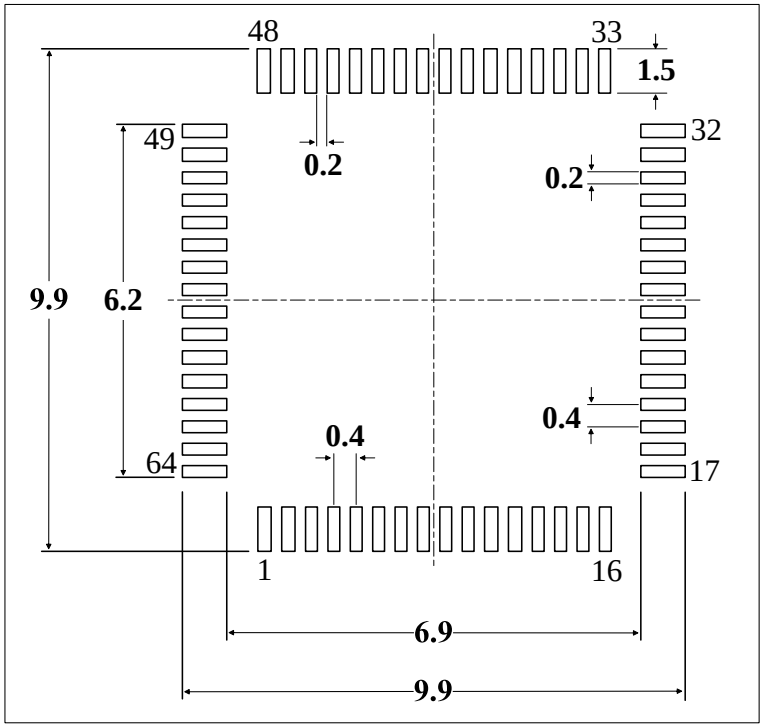
5.1 LQFP64

Figure 5-1 LQFP64 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	—	0.24
b1	0.15	0.18	0.21
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.40BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 5-2 LQFN64 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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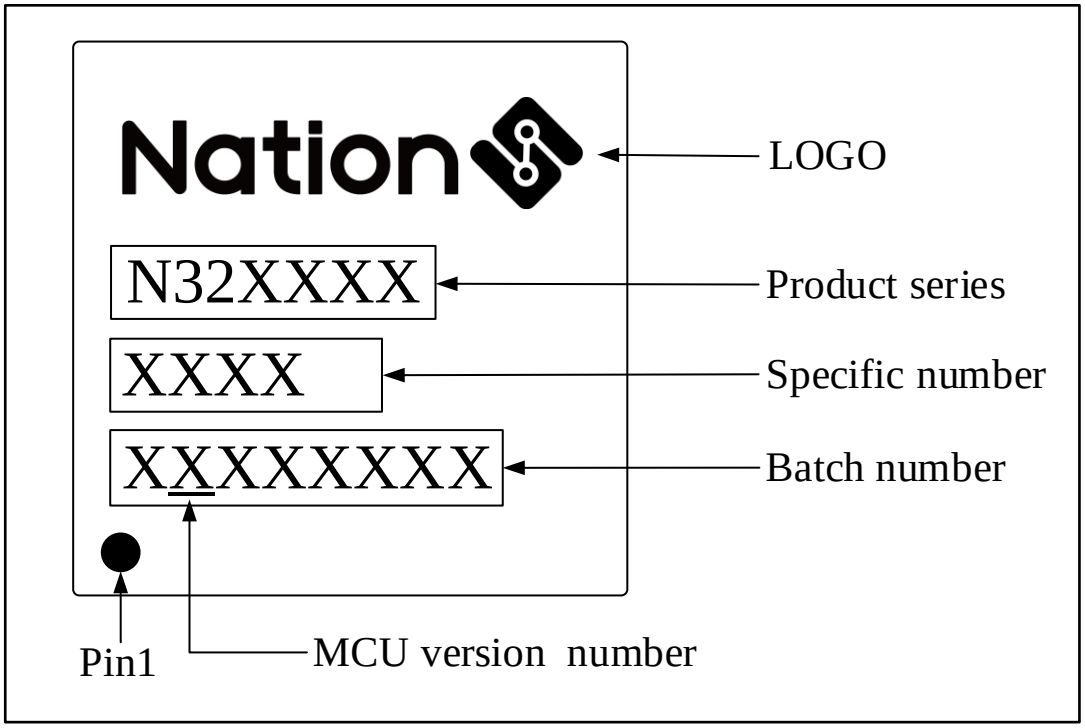
6 Marking Information

Figure 6-1 Marking Information



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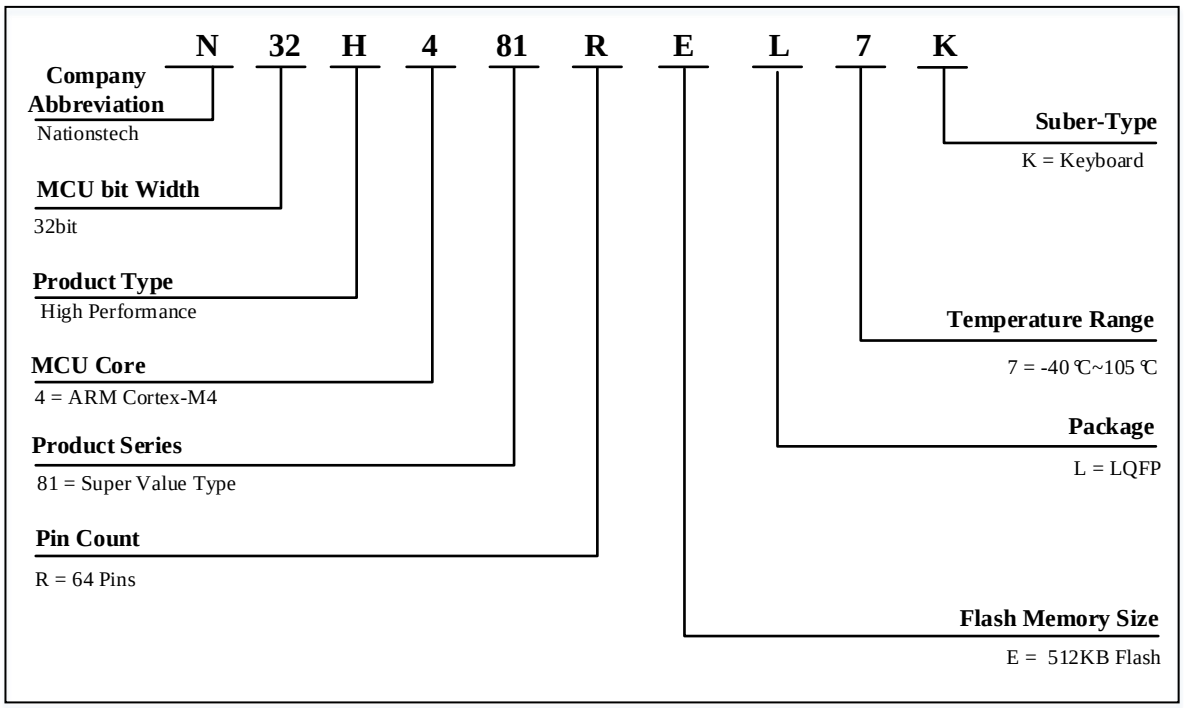
7 Ordering Information

7.1 Naming Convention

Figure 7-1 N32H481 Series Part Number Information



7.2 Ordering code

Table 7-1 N32H481 Series Ordering Code

Ordering Code(1)	Package	Size	Packaging(2)	SPQ(3)	Temperature range
N32H481REL7K	LQFP64	7mm x 7mm	Tray	250	-40℃～105℃

1. For the latest detailed-ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
3. Minimum packaging quantity.

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8 Version History

Date	Version	Changes
2025.5.9	V1.1.0	Initial release.
2025.8.28	V1.2.0	1. Modify Table 4-32 LPTIM Maximum Possible Counting Characteristics 2. Section 3.2: Modify PB14/PB15 pins to not support Fail safe 3. Modify Table 4-14 ACC_{HSI} Characteristics

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