N32H76x/78x series

Advanced ARM®-based 32-bit MCUs

User manual V1.1.0

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

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1 Abbreviations In The Text

1.1 Describes The List Of Abbreviations Used In The Register Table

The following abbreviations are used in the description of registers:

read/write(rw)	Software can read and write this bit.
read-only(r)	Software can only read this bit.
write-only(w)	Software can only write this bit, and reading this bit will return the reset value.
read/clear(rc_w1)	Software can read this bit or clear it by writing' 1', and writing' 0' has no effect on this bit.
read/clear(rc_w0)	Software can read this bit or clear it by writing' 0', and writing' 1' has no effect on this bit.
read/clear by read(rc_r)	Software can read this bit. Reading this bit will automatically clear it to' 0'. Writing' 0' has no effect on this bit.
read/set(rs)	Software can read or set this bit. Writing' 0' has no effect on this bit.
read/set by read (rs_r)	Software can read this bit. Reading this bit automatically sets it to 1. Writing this bit has no effect on the bit value
read-only write trigger(rt_w)	Software can read this bit and write' 0' or' 1' to trigger an event, but it has no effect on this bit value.
read-write, automatic clear(rw1_ac)	Read-Write, automatic clear this bit: Writing '1' to wait for the operation to complete will automatically clear the bit. Writing' 0' has no effect on this bit..
toggle(t)	Software can only flip this bit by writing' 1', and writing' 0' has no effect on this bit.
Reserved(Res.)	Reserved bits, the default value must be kept unchanged.

1.2 Available Peripherals

For all models of N32H76x, N32H78x microcontroller series, the existence and number of a peripheral, please refer to the data sheet of the corresponding model.

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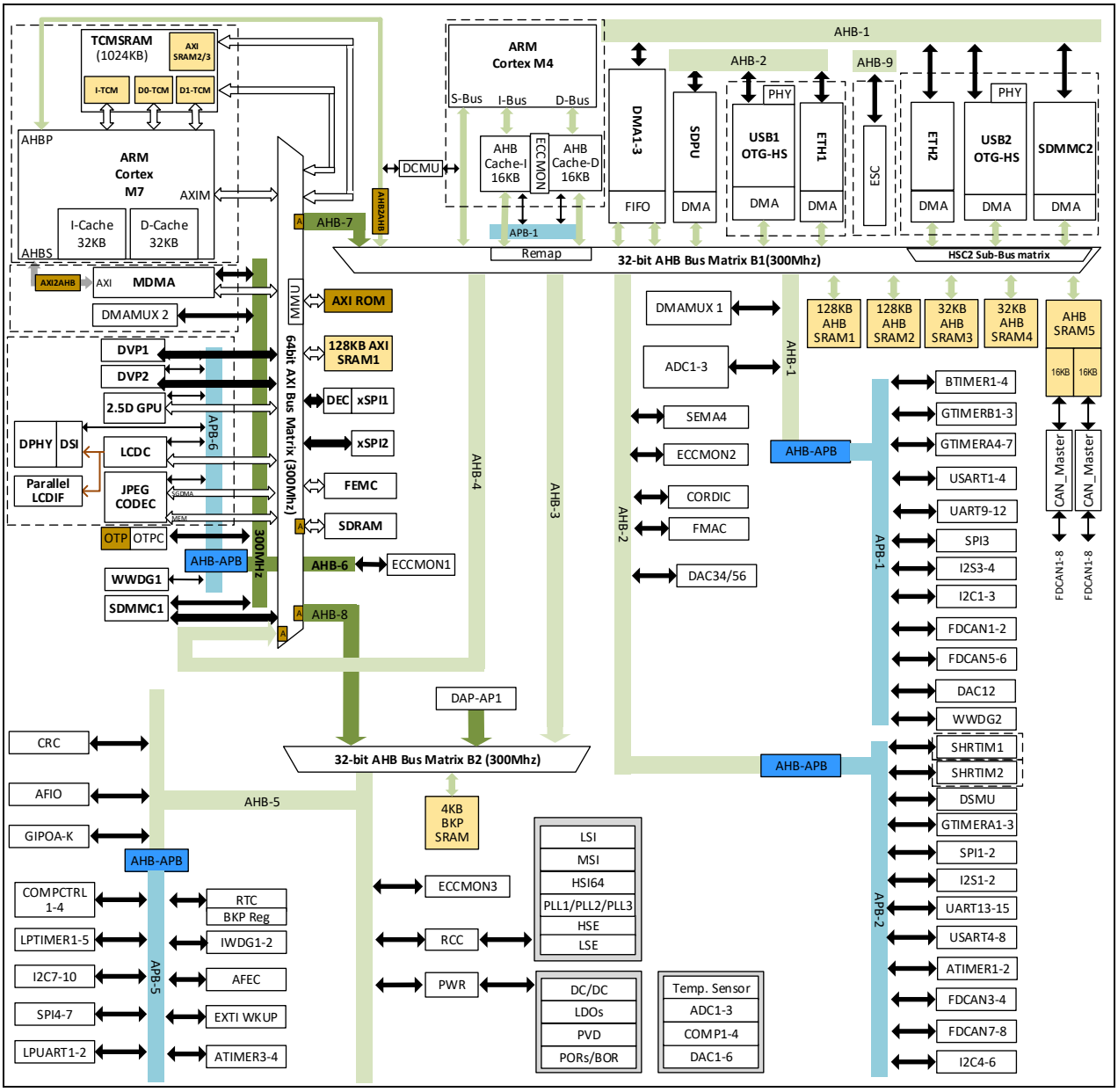
2 Memory and Bus Architecture

2.1 System Architecture

N32H7xx is a high-performance microcontroller that is built on a high-performance ARM Cortex-M7 32-bit RISC core and a low power ARM Cortex-M4 32-bit RISC core operating at 600MHz and 300MHz respectively.

It embeds multiple bus matrices as shown in Figure 2-1. This allows to reach the best compromise between performance and power consumption. This also enables efficient simultaneous operation of high-speed peripherals and removes bus congestion when several masters are simultaneously active (different masters located in separated bus matrices).

Figure 2-1 System Architecture of N32H7xx



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2.1.1 Bus Matrix Interconnections

N32H7xx features three separate bus matrices:

- 64-bit AXI bus matrix: It has a high-performance capability and is dedicated to operations requiring high bandwidth. High-bandwidth peripherals are connected to AXI bus. For more details, refer to chapter 2.1.2.1.
- 32-bit AHB bus matrix 1: communication peripherals and timers are connected to these bus matrices. For more details, refer to chapter 2.1.2.2.1.
- 32-bit AHB bus matrix 2: reset, clock control, power management and GPIOs are located in this domain. Some low-power IPs such as LPUART/LPTIM/COMPCTRL/RTC/IWDG/EXTI are added in this domain for wakeup purposes. Multiple timers and communication IPs are also included for such applications where CM7 are active whereas CM4, AHB bus matrix 1 and its peripherals can be disabled for power reduction. For more details, refer to chapter 2.1.2.2.2.

All bus matrices and CM4 can run up to 300 MHz while the CM7 CPU, the ITCM-RAM and the DTCM-RAM can run up to 600 MHz. All bus matrices are connected together by means of inter-domain buses to allow a master located in a given domain to have access to a slave located in another domain.

Figure 2-1 shows the bus-master-to-bus-slave interconnections of N32H7xx, which allows interconnecting bus masters with bus slaves. For more details of all bus masters and slaves, refer to Figure 2-2.

Figure 2-2 Bus Architecture of N32H7xx

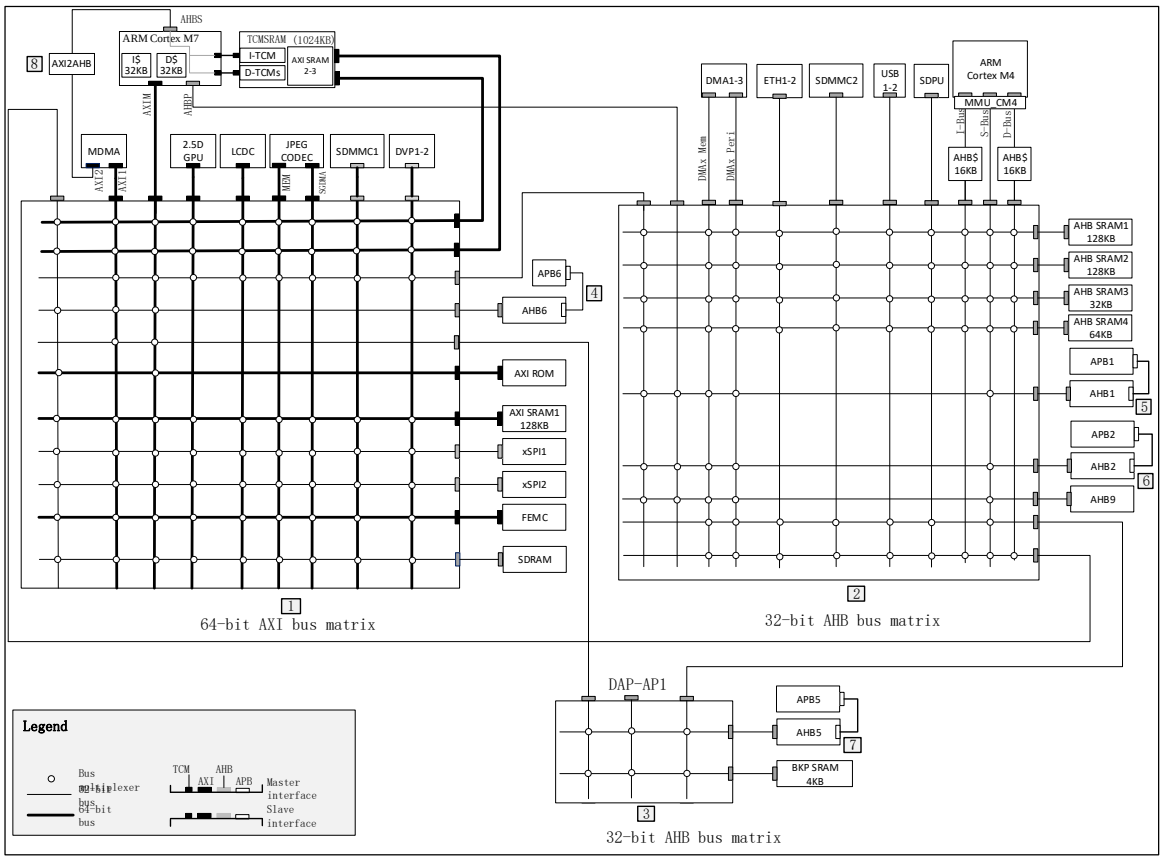

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Table 2-1 Bus-master-to-bus-slave interconnections

	Cortex M7 - AXIM	Cortex M7 - ITCM	Cortex M7 - DTCM	Cortex M7 - AHBP	MDMA – AXI 1	MDMA – AXI 2	LCDC/GPU	JPEG CODEC		SDMMC1	DVP1-2	Cortex M4 – I-Bus	Cortex M4 – D-Bus	Cortex M4 – S-Bus	DMA1-3 (MBus)	DMA1-3 (PBus)	ETH1-2/USB1-2	SDMMC2/SDPU	DAP-AP1
ITCM	-	D	-	-	-	8	-	-		-	-	-	-	-	-	-	-	-	-
DTCM	-	-	D	-	-	8	-	-		-	-	-	-	-	-	-	-	-	-
AHB-6 Peri	1	-	-	-	1	-	-	-		-	-	21	21	21	21	21	21	21	-
APB-6 Peri	14	-	-	-	14	-	-	-		-	-	214	214	214	214	214	214	214	-
AXI ROM	1	-	-	-	-	-	-	-		-	-	21	21	-	-	-	-	-	-
AXI SRAM1-3	1	-	-	-	1	-	1	1		1	1	21	21	21	21	21	21	21	-
xSPI1	1	-	-	-	1	-	1	1		1	1	21	21	21	21	21	21	21	-
xSPI2	1	-	-	-	1	-	1	1		1	1	21	21	21	21	21	21	21	-
FEMC	1	-	-	-	1	-	1	1		1	1	21	21	21	21	21	21	21	-
SDRAM	1	-	-	-	1	-	1	1		1	1	21	21	21	21	21	21	21	-
AHBSRAM 1-5	12	-	-	-	12	-	12	12		12	12	2	2	2	2	2	2	2	-
AHB9-Peri				2	12	-	12	12		12	12	-	-	2	2	2			
AHB-1 Peri	-	-	-	2	12	-	12	12		12	12	-	-	2	2	2	-	-	-
APB-1 Peri	-	-	-	25	125	-	125	125		125	125	-	-	25	25	25	-	-	-
AHB-2 Peri	-	-	-	2	12	-	12	12		12	12	-	-	2	2	2	-	-	-
APB-2 Peri	-	-	-	26	126	-	126	126		126	126	-	-	26	26	26	-	-	-
AHB-5 Peri	13	-	-	-	13	-	-	-		-	-	-	-	23	23	23	-	-	3
APB-5 Peri	137	-	-	-	137	-	-	-		-	-	-	-	237	237	237	-	-	3
BKP RAM	13	-	-	-	13	-	-	-		-	-	-	-	23	23	23	23	23	3

***Bold**: 64-bit, plain: 32-bit*

Access possibility and utility: Any figure = access possible, "-" = access not possible, shading = access useful/usable

Access path: D=direct, 1=via AXI bus matrix, 2=via AHB bus matrix 1, 3=via AHB bus matrix 2, 4=via AHB/APB bridge 1(AHB6 to APB6),5=via AHB/APB bridge 2(AHB1 to APB1), 6=via AHB/APB bridge 3 (AHB2 to APB2), 7=via AHB/APB bridge 4 (AHB5 to APB5), 8=via AXI2AHB bridge to AHBS of Cortex®-M7

Multi-digit numbers = interconnect path goes through more than one matrix or/and bridge, in the order of the digits

2.1.2 Bus Matrices

2.1.2.1 AXI Bus Matrix

2.1.2.1.1 Introduction

The AXI bus matrix is based on the Arm® CoreLink™ NIC-400 Network Interconnect and ARM AXI4 to AHB-Lite Bridge (AAB). The NIC-400 AXI interconnect has ten initiator ports, or ASIBs (AMBA slave interface blocks), and

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eleven target ports, or AMIBs (AMBA master interface blocks). The ASIBs are connected to the AMIBs via an AXI switch matrix. Each ASIB is a slave on an AXI bus or AHB. Similarly, each AMIB is a master on an AXI or AHB bus. Where an ASIB or AMIB is connected to an AHB, it converts between the AHB and the AXI protocol.

2.1.2.1.2 Main features

- 64-bit AXI Interconnect with ten ASIBs and eleven AMIBs
- AHB to AXI bridge function is built into the AMIBs
- AXI to AHB protocol conversion between ASIBs and connected slaves
- Programmable traffic priority management
- Software configurable via GPV (Global Programmer View)

2.1.2.1.3 Functional Descriptions

Bus masters

- ARM Cortex-M7 64-bit AXI bus
- MDMA 64-bit AXI bus
- GPU 64-bit AXI bus
- LCD Controller (LCDC) 64-bit AXI bus
- JPEG CODEC SGDMA 64-bit AXI bus
- JPEG CODEC MEM 64-bit AXI bus
- SDMMC1 64-bit AHB bus
- DVP1 64-bit AHB bus
- DVP2 64-bit AHB bus
- Inter-domain AHB4 bus, a 32-bit AHB bus that connects AHB bus matrix 1 to AXI bus matrix

Table 2-2 summarizes the characteristics of the 10 ASIBs of the AXI interconnect.

Table 2-2 ASIB Configuration

Master	Name	Protocol	Bus width	R/W Issuing Capability
M1	CM7 AXIM	AXI4	64	7/32
M2	MDMA	AXI4	64	16/16
M3	GPU	AXI3	64	8/8
M4	LCDC	AXI4	64	16/1
M5	JPEG-SGDMA	AXI4	64	16/2
M6	JPEG-MEM	AXI4	64	3/3
M7	SDMMC1	AHB	64	1/1
M8	DVP1	AHB	64	1/1
M9	DVP2	AHB	64	1/1
M10	AHB4	AHB	32	1/1

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Bus slaves

- Embedded AXI ROM (Read Only Memory)
- 128KB AXI SRAM
- Up to 512KB AXI SRAM 2 (Shared with TCM, configurable by software)
- Up to 512KB AXI SRAM 3 (Shared with TCM, configurable by software)
- 2 xSPI memory interfaces on 32-bit AHB bus access
- FEMC memory interface on the AXI bus accessed by 64 bits
- SDRAM memory interface on the AHB bus accessed by 32 bits
- Inter-domain AHB7 bus, a 32-bit AHB bus that connects AXI bus matrix to AHB bus matrix 1
- Inter-domain AHB8 bus, a 32-bit AHB bus that connects AXI bus matrix to AHB bus matrix 2
- AHB6 peripherals including AHB-to-APB bridge and APB6 peripherals

Table 2-3 summarizes the characteristics of the 11 AMIBs of the AXI interconnect.

Table 2-3 AMIB Configuration

Slave	Name	Protocol	Bus width	R/W/Total Acceptance
S1	AXI ROMC	AXI3	64	1/1/1
S2	AXI SRAM1	AXI3	64	1/2/3
S3	AXI SRAM2	AXI3	64	1/2/3
S4	AXI SRAM3	AXI3	64	1/2/3
S5	xSPI1	AXI4(1)	32	2/2/4
S6	xSPI2	AXI4(1)	32	2/2/4
S7	FEMC	AXI3	64	3/3/3
S8	SDRAM	AXI4(1)	32	2/2/4
S9	AHB6	AXI4(1)	32	2/2/4
S10	AHB7	AXI4(1)	32	2/2/4
S11	AHB8	AXI4(1)	32	2/2/4

(1) Conversion to AHB protocol is done by AAB sitting between respective AMIBs and connected slaves.

Quality of Service (QoS)

The AXI interconnect uses a priority-based arbitration when two ASIB simultaneously attempt to access the same AMIB. Each ASIB has programmable read channel and write channel priorities, known as QoS, from 0 to 15, such that the higher the value, the higher the priority. The read channel QoS value is programmed in the corresponding read QoS register (xxx.read_qos), and the write channel in the corresponding write QoS register (xxx.write_qos). The default QoS value for all channels is 0 (lowest priority).

If two coincident transactions arrive at the same AMIB, the higher priority transaction passes before the lower priority. If the two transactions have the same QoS value, then a least- recently-used (LRU) priority scheme is adopted.

The QoS values should be programmed according to the latency requirements for the application. Setting a higher

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priority for an ASIB ensures a lower latency for transactions initiated by the associated bus master. This can be useful for real-time-constrained tasks, such as graphics processing (GPU/LCDC/DVP/JPEG). Assigning a high priority to masters that can make many and frequent accesses to the same slave (such as the Cortex-M7 CPU) can block access to that slave by other lower-priority masters.

Global programmer view (GPV)

The GPV contains configuration registers for the AXI interconnect. These registers are only accessible by the Cortex-M7 CPU.

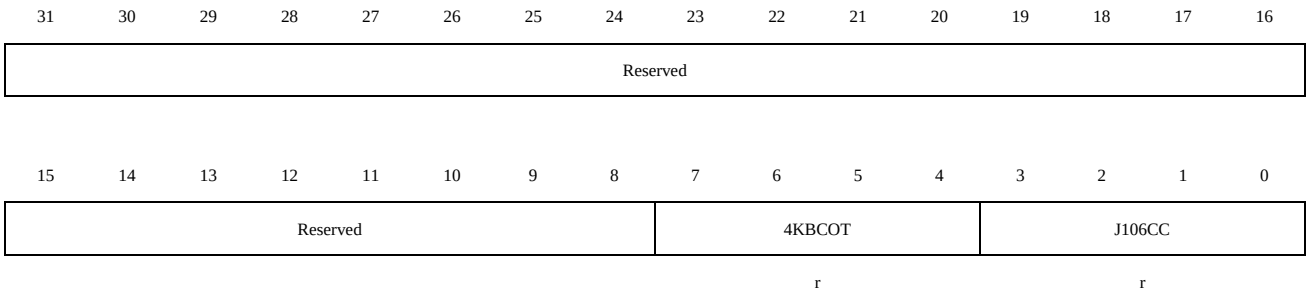
2.1.2.1.4 GPV Interconnect Registers

Note that only 32-bit word access is allowed. Unaligned access is not allowed.

2.1.2.1.4.1 Periph ID 4(GPV_FERID4)

Address offset: 0x00001fd0

Reset value: 0x4

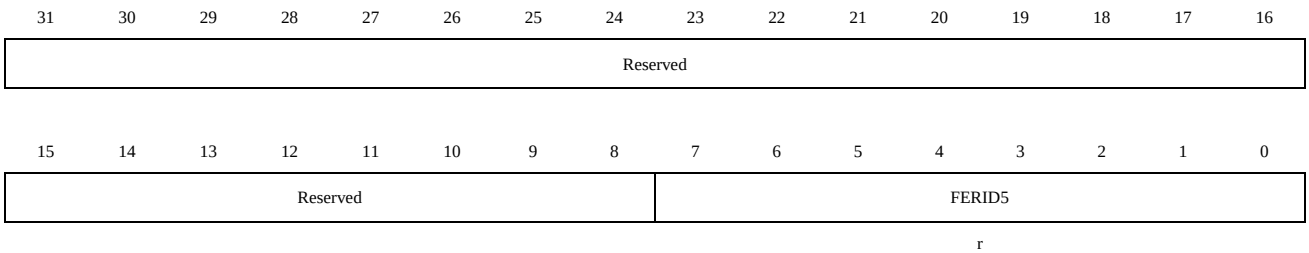


Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:4	4KBCOT	4KB count, register size 0x0: NA
3:0	J106CC	JEP106 continuation code 0x4: ARM

2.1.2.1.4.2 Periph ID 5(GPV_FERID5)

Address offset: 0x00001fd4

Reset value: 0x0



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Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	FERID5	Reserved

2.1.2.1.4.3 Periph ID 6(GPV_FERID6)

Address offset: 0x00001fd8

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FERID6							
								r							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	FERID6	Reserved

2.1.2.1.4.4 Periph ID 7(GPV_FERID7)

Address offset: 0x00001fdc

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FERID7							
								r							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	FERID7	Reserved

2.1.2.1.4.5 Periph ID 0(GPV_FERID0)

Address offset: 0x00001fe0

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PNUML							
								r							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	PNUML	Part Number [7:0]. 0x00: Part number = 0x400

2.1.2.1.4.6 Periph ID 1(GPV_FERID1)

Address offset: 0x00001fe4

Reset value: 0xB4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								J106IDL				PNUMH			
								r				r			

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:4	J106IDL	JEP106 Identity [3:0] 0xB: ARM JEDEC code
3:0	PNUMH	part number [11:8] 0x4: Part number = 0x400

2.1.2.1.4.7 Periph ID 2(GPV_FERID2)

Address offset: 0x00001fe8

Reset value: 0x06B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PREV				J106CF	J106IDH		

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r	r	r

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:4	PREV	Part Revision 0x6
3	J106CF	JEP106 code flag 0x1: JEDEC allocated code
2:0	J106IDH	JEP106 Identity [6:4]. 0x3: ARM JEDEC code

2.1.2.1.4.8 Periph ID 3(GPV_FERID3)

Address offset: 0x00001fec

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CVER				CMODI			
								r				r			

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:4	CVER	Customer Version 0x0: None
3:0	CMODI	Customer Modification 0x0: None

2.1.2.1.4.9 Comp ID 0(GPV_COMID0)

Address offset: 0x00001ff0

Reset value: 0x0D

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PREAM1							

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Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	PREAM1	Preamble bit [7:0] 0xD: common ID value

2.1.2.1.4.10 Comp ID 1(GPV_COMID1)

Address offset: 0x00001ff4

Reset value: 0xF0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								COMPC				PREAM2			
								r				r			

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:4	COMPC	component class 0xF: Generic IP component class
3:0	PREAM2	preamble[11:8] 0x0: Common ID value

2.1.2.1.4.11 Comp ID 2(GPV_COMID2)

Address offset: 0x00001ff8

Reset value: 0x05

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PREAM3							
								r							

Bit field	Name	Description

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31:8	Reserved	Reserved,the reset value must be maintained
7:0	PREAM3	Preamble bit [19:12] 0x05: common ID value

2.1.2.1.4.12 Comp ID 3(GPV_COMID3)

Address offset: 0x00001ffc

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PREAM4							
								r							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	PREAM4	Preamble [27:20].

2.1.2.1.4.13 AXI ROM issuing functionality modification register (GPV_AXIROM_IFMOD)

Address offset: 0x00002008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

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0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.14 AXISRAM1 issuing functionality modification register (GPV_AXISRAM1_IFMOD)

Address offset: 0x00003008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.15 AXISRAM2 issuing functionality modification register (GPV_AXISRAM2_IFMOD)

Address offset: 0x00004008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC

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															rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.16 XSPI1 issuing functionality modification register (GPV_XSPI1_IFMOD)

Address offset: 0x00005008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

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2.1.2.1.4.17 XSPI2 issuing functionality modification register (GPV_XSPI2_IFMOD)

Address offset: 0x00006008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.18 FEMC issuing functionality modification register (GPV_FEMC_IFMOD)

Address offset: 0x00007008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability

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		Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.19 SDRAM issuing functionality modification register (GPV_SDRAM_IFMOD)

Address offset: 0x00008008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.20 AHBP6 issuing functionality modification register (GPV_AHBP6_IFMOD)

Address offset: 0x00009008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.21 AHBP7 issuing functionality modification register (GPV_AHBP7_IFMOD)

Address offset: 0x0000a008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

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0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.22 AHBP8 issuing functionality modification register (GPV_AHBP8_IFMOD)

Address offset: 0x0000b008

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.23 CM7 AXIM read QoS (GPV_M7AXIM_RQOS)

Address offset: 0x00042100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	RQOS
	rw

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.24 CM7 AXIM write QoS (GPV_ M7AXIM _WQOS)

Address offset: 0x00042104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WQOS	
														rw	

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.25 CM7 AXIM Issuing functionality modification register (GPV_ M7AXIM _IFMOD)

Address offset: 0x00042108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

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Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.26 MDMA read QoS (GPV_MDMA_RQOS)

Address offset: 0x00043100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.27 MDMA write QoS (GPV_ MDMA_WQOS)

Address offset: 0x00043104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			

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rw

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.28 MDMA Issuing functionality modification register (GPV_ MDMA_IFMOD)

Address offset: 0x00043108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.29 GPU read QoS (GPV_ GPU_RQOS)

Address offset: 0x00044100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.30 GPU write QoS (GPV_ GPU_WQOS)

Address offset: 0x00044104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.31 GPU Issuing functionality modification register (GPV_ GPU_IFMOD)

Address offset: 0x00044108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

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Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.32 LCDC read QoS (GPV_ LCDC_RQOS)

Address offset: 0x00045100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.33 LCDC write QoS (GPV_ LCDC_WQOS)

Address offset: 0x00045104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
												rw			

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Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.34 LCDC Issuing functionality modification register (GPV_ LCDC_IFMOD)

Address offset: 0x00045108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.35 JPEG SGDMA read QoS (GPV_JPEGSD_RQOS)

Address offset: 0x00046100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	RQOS
	rw

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.36 JPEG SGDMA write QoS (GPV_ JPEGSD_WQOS)

Address offset: 0x00046104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WQOS	
														rw	

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.37 JPEG SGDMA Issuing functionality modification register (GPV_ JPEGSD_IFMOD)

Address offset: 0x00046108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

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Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.38 JPEG MEM read QoS (GPV_JPEGM_RQOS)

Address offset: 0x00047100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.39 JPEG MEM write QoS (GPV_ JPEGM_WQOS)

Address offset: 0x00047104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
												rw			

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Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.40 JPEG MEM issuing functionality modification register (GPV_ JPEGM_IFMOD)

Address offset: 0x00047108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.41 SDMMC1 read write INCR register (GPV_ SDMMC1_RWINCR)

Address offset: 0x00048028

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	WINCR	RINCR
	rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WINCR	0: Write fixed-length bursts to AXI fixed-length bursts, and only the last AHB-Lite write data beat receives the AXI buffered response for the whole AHB-Lite transaction. Write INCR bursts to a series of AXI singles, and each AHB-Lite write beat is acknowledged with the AXI buffered write response. 1: Converts all AHB-Lite write transactions to a series of single beat AXI transactions, and each AHB-Lite write beat is acknowledged with the AXI buffered write response.
0	RINCR	0: Read fixed-length bursts to AXI fixed-length bursts. Read INCR bursts to a series of AXI singles. 1: Converts all AHB-Lite read transactions to a series of single beat AXI transactions.

2.1.2.1.4.42 SDMMC1 read QoS (GPV_ SDMMC1_RQOS)

Address offset: 0x00048100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.43 SDMMC1 write QoS (GPV_ SDMMC1_WQOS)

Address offset: 0x00048104

Reset value: 0x0

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
														rw	

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.44 SDMMC1 issuing functionality modification register (GPV_ SDMMC1_IFMOD)

Address offset: 0x00048108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.45 DVP1 read write INCR register (GPV_ DVP1_RWINCR)

Address offset: 0x00049028

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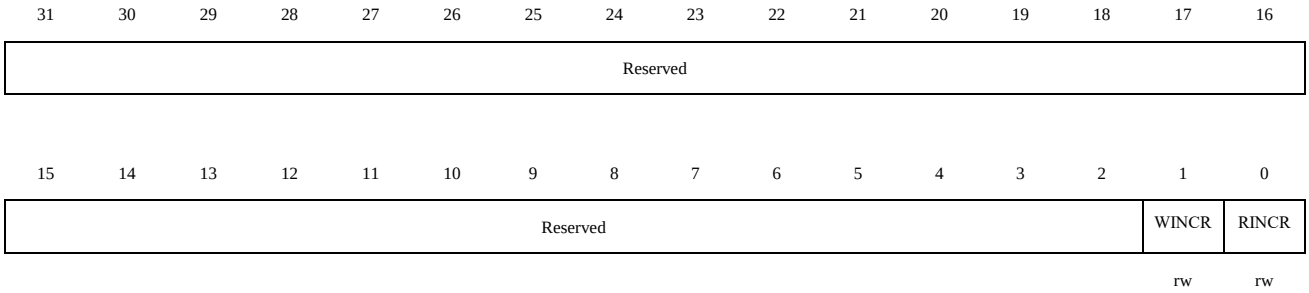
Reset value: 0x0

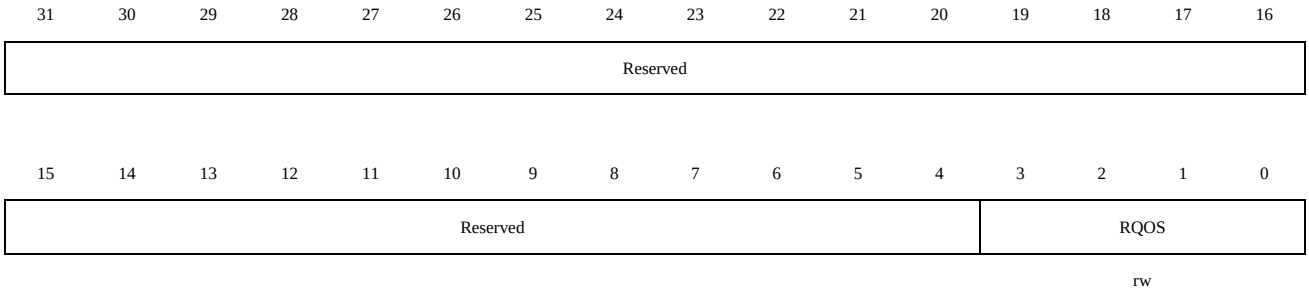


Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WINCR	0: Write fixed-length bursts to AXI fixed-length bursts, and only the last AHB-Lite write data beat receives the AXI buffered response for the whole AHB-Lite transaction. Write INCR bursts to a series of AXI singles, and each AHB-Lite write beat is acknowledged with the AXI buffered write response. 1: Converts all AHB-Lite write transactions to a series of single beat AXI transactions, and each AHB-Lite write beat is acknowledged with the AXI buffered write response.
0	RINCR	0: Read fixed-length bursts to AXI fixed-length bursts. Read INCR bursts to a series of AXI singles. 1: Converts all AHB-Lite read transactions to a series of single beat AXI transactions.

2.1.2.1.4.46 DVP1 read QoS (GPV_ DVP1_RQOS)

Address offset: 0x00049100

Reset value: 0x0



Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

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2.1.2.1.4.47 DVP1 write QoS (GPV_ DVP1_WQOS)

Address offset: 0x00049104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.48 DVP1 issuing functionality modification register (GPV_DVP1_IFMOD)

Address offset: 0x00049108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose:

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		0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.49 DVP2 read write INCR register (GPV_DVP2_RWINCR)

Address offset: 0x0004a028

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WINCR	RINCR
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WINCR	0: Write fixed-length bursts to AXI fixed-length bursts, and only the last AHB-Lite write data beat receives the AXI buffered response for the whole AHB-Lite transaction. Write INCR bursts to a series of AXI singles, and each AHB-Lite write beat is acknowledged with the AXI buffered write response. 1: Converts all AHB-Lite write transactions to a series of single beat AXI transactions, and each AHB-Lite write beat is acknowledged with the AXI buffered write response.
0	RINCR	0: Read fixed-length bursts to AXI fixed-length bursts. Read INCR bursts to a series of AXI singles. 1: Converts all AHB-Lite read transactions to a series of single beat AXI transactions.

2.1.2.1.4.50 DVP2 read QoS (GPV_ DVP2_RQOS)

Address offset: 0x0004a100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

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Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.51 DVP2 write QoS (GPV_ DVP2_WQOS)

Address offset: 0x0004a104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.52 DVP2 Issuing functionality modification register (GPV_ DVP2_IFMOD)

Address offset: 0x0004a108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose:

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		0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.1.4.53 AHB4 IB bypass merge register (GPV_AHB4IB_BM)

Address offset: 0x0004b024

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															BM
															rw

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	BM	If BM is asserted, the network does not alter any transactions that can pass through legally without alteration.

2.1.2.1.4.54 AHB4 IB Read write INCR register (GPV_AHB4IB_RWINCR)

Address offset: 0x0004b028

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WINCR	RINCR
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained

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1	WINCR	0: Write fixed-length bursts to AXI fixed-length bursts, and only the last AHB-Lite write data beat receives the AXI buffered response for the whole AHB-Lite transaction. Write INCR bursts to a series of AXI singles, and each AHB-Lite write beat is acknowledged with the AXI buffered write response. 1: Converts all AHB-Lite write transactions to a series of single beat AXI transactions, and each AHB-Lite write beat is acknowledged with the AXI buffered write response.
0	RINCR	0: Read fixed-length bursts to AXI fixed-length bursts. Read INCR bursts to a series of AXI singles. 1: Converts all AHB-Lite read transactions to a series of single beat AXI transactions.

2.1.2.1.4.55 AHB4 IB read QoS (GPV_ AHB4IB_RQOS)

Address offset: 0x0004b100

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RQOS			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	RQOS	Read channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.56 AHB4 IB write QoS (GPV_ AHB4IB_WQOS)

Address offset: 0x0004b104

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												WQOS			
												rw			

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Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	WQOS	Write channel QoS Setting 0x0: Lowest Priority 0xF: Highest Priority

2.1.2.1.4.57 AHB4 IB Issuing functionality modification register (GPV_ AHB4IB_IFMOD)

Address offset: 0x0004b108

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														WIC	RIC
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	WIC	Write issuing capability Set the write issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one
0	RIC	Read issuing capability Set the read issuing capability of the preceding switch arbitration scheme to 1. The register bits are active HIGH and have the following purpose: 0: Normal issuing capability 1: force issuing capability to one

2.1.2.2 AHB Bus Matrices

2.1.2.2.1 AHB Bus Matrix 1

AHB bus matrix 1 consists of 17 masters and 10 slaves as shown in Figure 2-2. When multiple masters are requesting to access to the same slave at the same time, the round-robin scheduling mechanism will be used for access arbitration

Bus masters

- ARM Cortex-M4 I-bus
- ARM Cortex-M4 D-bus
- ARM Cortex-M4 S-bus

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- DMA1-3 P-bus
- DMA1-3 M-bus
- ETH1-2 master bus
- USB1-2 master bus
- SDMMC2 master bus
- ARM Cortex-M7 AHBP bus
- Inter-domain AHB7 bus, a 32-bit AHB bus that connects AXI bus matrix to AHB bus matrix 1
- SDPU master bus

Bus slaves

- 128KB AHB SRAM 1
- 128KB AHB SRAM 2
- 32KB AHB SRAM 3
- 32KB AHB SRAM 4
- 32KB AHB SRAM 5
- AHB1 peripherals including AHB2APB1 bridge and APB1 peripherals
- AHB2 peripherals including AHB2APB2 bridge and APB2 peripherals
- Inter-domain AHB3 bus, a 32-bit AHB bus that connects AHB bus matrix 1 to AHB bus matrix 2
- Inter-domain AHB4 bus, a 32-bit AHB bus that connects AHB bus matrix 1 to AXI bus matrix
- AHBP9 peripheral including only ESC

2.1.2.2.2 AHB Bus Matrix 2

AHB bus matrix 2 consists of 3 masters and 2 slaves as shown in Figure 2-2. When multiple masters are requesting to access to the same slave at the same time, the round-robin scheduling mechanism will be used for access arbitration

Bus masters

- Inter-domain AHB8 bus, a 32-bit AHB bus that connects AXI bus matrix to AHB bus matrix 2
- Inter-domain AHB3 bus, a 32-bit AHB bus that connects AHB bus matrix 1 to AHB bus matrix 2
- DAP-AP1, debug access port AP1 that allows debuggers to access peripherals connected to AHB bus matrix 2 including DBGMCU

Bus slaves

- 4KB Backup SRAM
- AHB5 peripherals including AHB2APB5 bridge and APB5 peripherals

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2.1.3 Bus Bridges

To allow peripherals with different types of buses to communicate with each other, there is a number of bus-to-bus bridges in the system.

AHB to APB Bridge

The system consists of four AHB2APB bridges: AHB2APB1, AHB2APB2, AHB2APB5 and AHB2APB6. This is to allow peripherals on respective APB buses to connect to its respective AHB bus.

AXI to AHB Bridge

The system consists of one AXI2AHB bridge. This bridge is used to convert AXI signals from MDMA to AHB for accessing CM7 TCM memories via the AHBS port.

AHB to AHB Bridge

The system consists of two AHB2AHB bridges. One is to cross AHB signals from CM7 AHBP bus under CM7 core clock domain to the AHB bus matrix 1 clock domain and another is to isolate timing from AHB bus matrix 1 domain to AHB bus matrix 2 domain.

2.1.4 AHB Caches

As Cortex-M4 does not have internal caches, to improve Cortex-M4 CPU performance when accessing memories with big wait states such as external Flash memories, AHB caches are employed to stand between Cortex-M4 I-bus/D-bus and AHB bus matrix 1. Note that Cortex-M4 CPU accessing AHB SRAM1-5 does not incur any wait states, thus caches are bypassed for such accesses.

Refer to Arm®CoreLink™ AHB Cache Techinical Reference Manual for more details.

2.1.4.1 AHB Instruction Cache

The instruction cache sits between Cortex-M4 I-bus and AHB Bus matrix 1. Frequently used data is copied to the cache for future access without wait state, hence minimizes instruction fetch accesses to external memories which incurs long latency.

2.1.4.2 AHB Data Cache

The data cache sits between Cortex-M4 D-bus and AHB Bus matrix 1. With the same mechanism, it can improve CPU performance especially when literal load occurs during a stall of previous instruction fetch to the same memory.

2.1.4.3 Parity Monitor

For data integrity, parity check is employed for these AHB Caches. Parity errors of 16 banks in AHB Caches (iCache/dCache) are monitored by AHB_CACHE_PARMON module. Each cache has 8 banks including 4 data RAMs and 4 TAG RAMs.

As shown in Table 2-4, first 2KB of register map is allocated for 8 banks in AHB iCache. The remaining 2KB of register map is allocated for 8 banks in AHB dCache. Data RAM is byte write enable, hence parity check is done per byte basis, whereas tag TAM is full 22-bit data write, hence the parity check is done per 22-bit data basis. Note that only the first bit PAR_ON of Control Register is commonly used to enable parity check for all 16 banks of AHB iCache and dCache.

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Table 2-4 Parity monitor mapping for AHB instruction and data caches

Monitoring units	SRAM (size)	Index (n)	Address Offset
1 (iCache)	Data RAM 0 (1024x32) with 32-bit data and 4-bit parity code	1	0x000
	Data RAM 1 (1024x32) with 32-bit data and 4-bit parity code	2	
	Data RAM 2 (1024x32) with 32-bit data and 4-bit parity code	3	
	Data RAM 3 (1024x32) with 32-bit data and 4-bit parity code	4	
	TAG RAM 0 (128x22) with 22-bit data and 1-bit parity code	5	
	TAG RAM 1 (128x22) with 22-bit data and 1-bit parity code	6	
	TAG RAM 2 (128x22) with 22-bit data and 1-bit parity code	7	
	TAG RAM 3 (128x22) with 22-bit data and 1-bit parity code	8	
2 (dCache)	Data RAM 0 (1024x32) with 32-bit data and 4-bit parity code	1	0x800
	Data RAM 1 (1024x32) with 32-bit data and 4-bit parity code	2	
	Data RAM 2 (1024x32) with 32-bit data and 4-bit parity code	3	
	Data RAM 3 (1024x32) with 32-bit data and 4-bit parity code	4	
	TAG RAM 0 (128x22) with 22-bit data and 1-bit parity code	5	
	TAG RAM 1 (128x22) with 22-bit data and 1-bit parity code	6	
	TAG RAM 2 (128x22) with 22-bit data and 1-bit parity code	7	
	TAG RAM 3 (128x22) with 22-bit data and 1-bit parity code	8	

2.1.4.4 Parity Monitor Registers

AHB_CACHE_PARMON registers can be accessed by bytes, half-words (16 bits) or words (32 bits). Note that "*n*" represents the index number of the respective RAM as shown in the Table 2-4。

2.1.4.4.1 AHB_CACHE_PARMON Control Register 1(AHB_CACHE_PARMON _CTRL1)

Address Offset: 0x00

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Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	PEINTEN								Reserved						
	rw														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															PMEN
															rw

Bit Field	Field Name	Description
31	Reserved	Reserved,the reset value must be maintained
30:23	PEINTEN[7:0]	Parity Error detection interrupt enable bit: 0: interrupt is disabledsss 1: interrupt is enabled

bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
DataSram0	DataSram1	DataSram2	DataSram3	TagSram0	TagSram1	TagSram2	TagSram3

22:1	Reserved	Reserved,the reset value must be maintained
0	PMEN	Parity monitor enable bit: 0: Parity monitor is disabled 1: Parity monitor is enabled Note that only PMEN bit in the first monitoring unit is used to enable/disable partity for all SRAM banks in both AHB iCache and dCache. The second monitoring unit's PMEN bits are not used.

2.1.4.4.2 AHB_CACHE_PARMON Control Register 2(AHB_CACHE_PARMON _CTRL2)

Address Offset: 0x04

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	PFOEN								Reserved						
	rw														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Field Name	Description

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31	Reserved	Reserved,the reset value must be maintained
30:23	PFOEN[5:0]	Parity error flag output enable. Each bit corresponds to a different memory, the corresponding memory for each bit refer to AHB_CACHE_PARMON _CTRL1.PEINTEN. 1: PFOEN is output 0: Disabled. Note: When it is enabled, the output will remain active (HIGH) until all PFOEN are cleared.
22:0	Reserved	Reserved,the reset value must be maintained

2.1.4.4.3 AHB_CACHE_PARMON Error Injection Register (AHB_CACHE_PARMON _EINJ)

Address Offset: 0x08

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECSELTR3		ECSELTR2		ECSELTR1		ECSELTR0		ECSELDR3		ECSELDR2		ECSELDR1		ECSELDR0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERICTR3		ERICTR2		ERICTR1		ERICTR0		ERICDR3		ERICDR2		ERICDR1		ERICDR0	
rw		rw		rw		rw		rw		rw		rw		rw	

Bit Field	Field Name	Description
31:30	ECSELTR3[1:0]	Error event capture selection for TAG RAM3 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
29:28	ECSELTR2[1:0]	Error event capture selection for TAG RAM2 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
27:26	ECSELTR1[1:0]	Error event capture selection for TAG RAM1 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
25:24	ECSELTR0[1:0]	Error event capture selection for TAG RAM0 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.

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23:22	ECSELDR3[1:0]	Error event capture selection for DATA RAM3 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
21:20	ECSELDR2[1:0]	Error event capture selection for DATA RAM2 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
19:18	ECSELDR1[1:0]	Error event capture selection for DATA RAM1 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
17:16	ECSELDR0[1:0]	Error event capture selection for DATA RAM0 x0: Capture first encounter of parity error event. x1: Not captured Note: Changing from one mode to another mode, the corresponding Flags will be cleared.
15:14	ERICTR3 [1:0]	Error injection control for TAG RAM3 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output
13:12	ERICTR2 [1:0]	Error injection control for TAG RAM2 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output
11:10	ERICTR1 [1:0]	Error injection control for TAG RAM1 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output
9:8	ERICTR0 [1:0]	Error injection control for TAG RAM0 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output
7:6	ERICDR3 [1:0]	Error injection control for DATA RAM3 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output
5:4	ERICDR2[1:0]	Error injection control for DATA RAM2 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output
3:2	ERICDR1[1:0]	Error injection control for DATA RAM1 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output

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		11: 2-bit errors are injected to 32-bit memory output
1:0	ERICDR0 [1:0]	Error injection control for DATA RAM0 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output

2.1.4.4.4 AHB_CACHE_PARMON Interrupt Flag Shadow Register (AHB_CACHE_PARMON _INTFS)

Address Offset: 0x0C

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								PEIF							
								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Field Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
23:16	PEIF[7:0]	parity error detection interrupt pending flag Each bit corresponds to a different memory, the corresponding memory for each bit refer to AHB_CACHE_PARMON _CTRL1.PEINTEN.
15:0	Reserved	Reserved,the reset value must be maintained

2.1.4.4.5 AHB_CACHE_PARMON Mermory x Interrupt Flag Register (AHB_CACHE_PARMON _INTFx, x=1~8)

Address Offset: (5x-1) *4, x=1~8

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PEDCIFR	Reserved		
												rc_w1			

Bit Field	Field Name	Description

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31:4	Reserved	Reserved,the reset value must be maintained
3	PEDCIFR	Parity error detection and correction interrupt pending flag on read access. 0: the above error is not detected 1: the above error is detected Write "1" to this bit to clear this flag. An interrupt will be generated when this is set and its corresponding interrupt enable bit (PEINTEN) is set.
2:0	Reserved	Reserved,the reset value must be maintained

2.1.4.4.6 AHB_CACHE_PARMON Mermory x ECC Fail Event Address Register (AHB_CACHE_PARMON _FEADRx, x=1~8)

Address Offset: (5x) *4, x=1~8

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PEAD	Reserved	PER	Reserved	FEADR											
rc_w1	rc_w1	rc_w1	rc_w1	r											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEADR															
r															

Bit Field	Field Name	Description
[31]	PEAD	Parity error event and failing address detected Refer to ECSELDRx or ECSELTRx register for error event capture rules. This bit is set to "1" by hardware, which indicates the error event is detected and its associated failing address, the data and the code are captured to FEADR, PEDAT and PECODregisters respectively. Note: Write "1" to clear this bit, and at the same time it will clear FEAD if they are set. This bit will also be cleared if ECSELDRx or ECSELTRx value is changed.
[30]	Reserved	Reserved,the reset value must be maintained
29	PER	Parity error event in read This bit is working together with PEAD. This bit is set to "1" by hardware if the captured Error event is in Read Access. Note: Write "1" to clear this bit, and at the same time it will clear FEAD if they are set. This bit will also be cleared if ECSELDRx or ECSELTRx value is changed.
28	Reserved	Reserved,the reset value must be maintained
27:0	FEADR	Failing event address. It is read only. It is only *valid when PEAD is set to "1". This register will be locked until FEAD are clear.*

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		Note that this address is local to respsective memory, not the bus address. *Only the first 10-bit address is valid for data RAMx, whereas the first 7-bit address is valid for tag RAMx.* *For data RAMx:*Fail Addr={ FEADR [9:0] } *For tag RAMx:*Fail Addr={ FEADR [6:0] }

2.1.4.4.7 AHB_CACHE_PARMON Mermory x ECC Fail Event Data Register (AHB_CACHE_PARMON _FEDATx, x=1~8)

Address Offset: (5x+1) *4, x=1~8

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PEDAT															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFDAT															
r															

Bit Field	Field Name	Description
31:0	PEDAT	Parity error data low This data register is to store the lower DW-bit error data when the error event is captured. The value is only valid when PFAD is set to "1". This register will be locked until PFAD are clear. For DATA RAMx, 32 bits are vaild For TAG RAMx, 22 bits are vaild

2.1.4.4.8 AHB_CACHE_PARMON Mermory x ECC Fail Event ECC Code Register (AHB_CACHE_PARMON _FECODx, x=1~8)

Address Offset: (5x+3) *4, x=1~8

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PECOD															
r															

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Bit Field	Field Name	Description
31:16	Reserved	
3:0	PECOD	Parity error code This data register is to store the parity code when the error event is captured. The value is only valid when PEAD is set to "1". Note: This register will be locked until PEAD are clear. For DATA RAMx, 4 bits are vaild For TAG RAMx, 1 bit is vaild

2.1.5 CPU Buses

Cortex-M7 AXI Master Bus

Cortex-M7 CPU uses a 64-bit wide AXI4 master interface to access all memories (excluding I/DTCM) and peripherals (except AHB1/AHB2/AHB9/APB1/APB2 peripherals). The AXI bus connects the CPU to the AXI bus matrix.

Cortex-M7 ITCM Bus

Cortex-M7 CPU uses the 64-bit ITCM bus for fetching instructions as well as accessing data in the ITCM memory without wait states. Critical code or function should be put into ITCM for high performance.

Cortex-M7 DTCM Bus

Cortex-M7 CPU uses the 2x32-bit DTCM bus for accessing data in the DTCM memory. The 2x32-bit DTCM bus allows load/load and load/store instruction pairs to be dual-issued on the DTCM memory. It can also fetch instructions.

Cortex-M7 AHBS Bus

Cortex-M7 CPU uses this 32-bit AHBS bus to enable MDMA controller to access the ITCM and DTCM.

Cortex-M7 AHBP Bus

Cortex-M7 CPU uses this 32-bit AHBP bus to access AHB1/AHB2/AHB9/APB1/APB2 peripherals via the AHB bus matrix 1.

Cortex-M4 I-bus

Cortex-M4 CPU uses the 32-bit I-bus to access instructions, via AHB bus matrix 1, in the code region from 0x0000_0000 to 0x1FFF_FFFF: AHB SRAM1-5, AXI SRAM1-3, BOOTROM, BOOTPATCH and xSPI1/2 Flash Memory.

Cortex-M4 D-bus

Cortex-M4 CPU uses the 32-bit D-bus to access data and literals, via AHB bus matrix 1, in the code region from 0x0000_0000 to 0x1FFF_FFFF: AHB SRAM1-5, AXI SRAM1-3, BOOTROM, BOOTPATCH and xSPI1/2 Flash Memory.

Cortex-M4 S-bus

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Cortex-M4 CPU uses the 32-bit S-bus, via AHB bus matrix 1, to access all memories and peripherals in the device map addressed above 0x2000_0000. It can also handle instruction fetching, but with less efficiency than I-bus.

2.1.6 Bus master peripherals

MDMA controller

The MDMA has two bus masters:

- An AXI 64-bit bus, connected to the AXI bus matrix, to access all internal and external memories, except ITCM/DTCM memories.
- Another AXI 64-bit bus, connected to Cortex-M7 CPU AHBS port, via AXI2AHB bridge, to access ITCM and DTCM memories

The MDMA is designed to transfer data between memories with the support of linked list transfers that can perform a chained list of transfers without CPU intervention.

GPU

GPU (Graphic Processing Unit) has a 64-bit AXI master bus, connected to AXI Bus matrix, to access internal and external memories for graphic operations.

LCDC

LCDC Display Controller (LCDC) uses a 64-bit bus, connected to the AXI bus matrix, to access internal or external memories for fetching image/video data.

JPEG CODEC

JPEG (Joint Photographic Experts Group) Codec (Coder/decoder) utilizes 2 64-bit buses as follows:

- 64-bit SGDMA (Scatter-Gather DMA) bus, connected to the AXI bus matrix, to access internal or external memories for image/video compression/de-compression
- 64-bit MEM bus, connected to the AXI bus matrix, to access internal or external memories for temporary buffering of raster-to-block/block-to-raster conversion operation

SDMMC1

SDMMC1 uses a 64-bit AHB bus, connected to the AXI bus matrix, to access internal or external memories for data storage.

SDMMC2

SDMMC2 uses a 32-bit AHB bus, connected to the AHB bus matrix 1, to access internal or external memories for data storage.

DVP1-2

DVP1-2 uses a 64-bit AHB bus, connected to the AXI bus matrix, to access internal or external memories for frame buffering.

DMA1-3

DMA1-3 has 2 32-bit buses – memory and peripheral buses, connected to AHB bus matrix 1.

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The memory bus allows data transfer between memories.

The peripheral bus allows data transfer between peripherals and memories.

ETH1-2

ETH1-2 uses a 32-bit AHB bus, connected to the AHB bus matrix 1, to access internal or external memories for data storage.

USB1-2

USB1-2 uses a 32-bit AHB bus, connected to the AHB bus matrix 1, to access internal or external memories for data storage.

SDPU

SDPU uses a 32-bit AHB bus, connected to the AHB bus matrix 1, to access internal or external memories for data storage.

2.2 Memory Organization

2.2.1 Introduction

N32H7xx memory is organized within the same linear 4GB address space including code memory, data memory, registers and IO ports. It's aligned in Little Endian format. The whole memory is divided into 9 main blocks as shown in Table 2-5.

2.2.2 Memory map and register addressing

Table 2-5 N32H7xx Memory map and default memory attributes

Region	Start Address	End Address	Size	Cortex M7	Cortex M4
Vendor Specific	0xE010_0000	0xFFFF_FFFF	511MB	Reserved	Reserved
Private Peripheral (External)	0xE00F_F000	0xE00F_FFFF	4KB	PPB ROM Table	ROM Table
	0xE00F_E000	0xE00F_EFFF	4KB	Processor ROM table	External PPB
	0xE00F_D000	0xE00F_DFFF	4KB	System ROM table	
	0xE004_3000	0xE00F_CFFF	744KB	External PPB	
	0xE004_2000	0xE004_2FFF	4KB	CTI	
	0xE004_1000	0xE004_1FFF	4KB	ETM	ETM
	0xE004_0000	0xE004_0FFF	4KB	TPIU	TPIU
Private Peripheral (Internal)	0xE000_F000	0xE003_FFFF	196KB	Reserved	Reserved
	0xE000_E000	0xE000_EFFF	4KB	M7 peripherals (SCS/NVIC/MPU/FPU)	M4 peripherals (SCB/ST/NVIC/MPU/FPU)
	0xE000_3000	0xE000_DFFF	44KB	Reserved	Reserved
	0xE000_2000	0xE000_2FFF	4KB	FPB	FPB
	0xE000_1000	0xE000_1FFF	4KB	DWT	DWT

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Region	Start Address	End Address	Size	Cortex M7	Cortex M4
	0xE000_0000	0xE000_0FFF	4KB	ITM	ITM
External Devices	0xD000_0000	0xDFFF_FFFF	256MB	SDRAM 2	
	0xCC00_0000	0xCFFF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 4)	
	0xC800_0000	0xCBFF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 3)	
	0xC400_0000	0xC7FF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 2)	
	0xC000_0000	0xC3FF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 1)	
	0xB000_0000	0xBFFF_FFFF	256MB	FEMC NAND Flash Memory bank 2	
	0xA000_0000	0xAFFF_FFFF	256MB	FEMC NAND Flash Memory bank 1	
External Memories (WT)	0x9000_0000	0x9FFF_FFFF	256MB	xSPI2	
	0x8000_0000	0x8FFF_FFFF	256MB	xSPI1	
External Memories (WBWA)	0x7000_0000	0x7FFF_FFFF	256MB	Reserved	
	0x6C00_0000	0x6FFF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 4 (or remap of SDRAM 1 bank 4)	
	0x6800_0000	0x6BFF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 3 (or remap of SDRAM 1 bank 3)	
	0x6400_0000	0x67FF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 2 (or remap of SDRAM 1 bank 2)	
	0x6000_0000	0x63FF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 1 (or remap of SDRAM 1 bank 1)	
Peripherals	0x4000_0000	0x5FFF_FFFF	512MB	Peripherals (Refer to)	
RAM (WBWA)	0x3810_0000	0x3FFF_FFFF	127MB	Reserved	
	0x3800_1000	0x380F_FFFF	1020KB	Reserved	
	0x3800_0000	0x3800_0FFF	4KB	Backup SRAM	
	0x3010_0000	0x37FF_FFFF	127MB	Reserved	
	0x3005_8000	0x300F_FFFF	672KB	Reserved	
	0x3005_0000	0x3005_7FFF	32KB	AHB SRAM 5	
	0x3004_8000	0x3004_FFFF	32KB	AHB SRAM 4	
	0x3004_0000	0x3004_7FFF	32KB	AHB SRAM 3	
	0x3002_0000	0x3003_FFFF	128KB	AHB SRAM 2	
	0x3000_0000	0x3001_FFFF	128KB	AHB SRAM 1	
	0x2420_0000	0x2FFF_FFFF	190MB	Reserved	
	0x2412_0000	0x241F_FFFF	896KB	Reserved	
	0x240A_0000	0x2411_FFFF	512KB	AXI SRAM 3(3)	
	0x2402_0000	0x2409_FFFF	512KB	AXI SRAM 2(3)	
	0x2400_0000	0x2401_FFFF	128KB	AXI SRAM 1	

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Region	Start Address	End Address	Size	Cortex M7	Cortex M4
	0x2010_0000	0x23FF_FFFF	63MB	Reserved	
	0x2000_0000	0x200F_FFFF	1MB	DTCM	Reserved
Code (WT)	0x1FFF_C000	0x1FFF_FFFF	16KB	Reserved	
	0x1FFF_A000	0x1FFF_BFFF	8KB	Reserved	
	0x1FFF_8000	0x1FFF_9FFF	8KB	Option Byte (OB_FLASH)	
	0x1FFF_0000	0x1FFF_7FFF	32KB	Boot ROM (Bootloader)	
	0x1FFC_0000	0x1FFE_FFFF	838KB	Reserved	
	0x1FF0_0000	0x1FF1_BFFF	122KB	BOOTPATCH	
	0x1900_0000	0x1FEF_FFFF	127MB	Reserved	
	0x1700_0000	0x18FF_FFFF	32MB	xSPI2 BANK1/2(Alias) (2)	
	0x16FE_0000	0x16FF_FFFF	128KB	Reserved	
	0x1500_0000	0x16FD_FFFF	31.875MB	xSPI1 BANK1/2(Alias) (2)	
	0x1420_0000	0x14FF_FFFF	14MB	Reserved	
	0x1412_0000	0x141F_FFFF	896KB	Reserved	
	0x140A_0000	0x1411_FFFF	512KB	AXI SRAM 3(3) (Alias) (2)	
	0x1402_0000	0x1409_FFFF	512KB	AXI SRAM 2(3) (Alias) (2)	
	0x1400_0000	0x1401_FFFF	128KB	AXI SRAM 1 (Alias) (2)	
	0x1020_0000	0x13FF_FFFF	62MB	Reserved	
	0x1005_8000	0x101F_FFFF	1632KB	Reserved	
	0x1005_0000	0x1005_7FFF	32KB	AHB SRAM 5 (Alias) (2)	
	0x1004_8000	0x1004_FFFF	32KB	AHB SRAM 4 (Alias) (2)	
	0x1004_0000	0x1004_7FFF	32KB	AHB SRAM 3 (Alias) (2)	
	0x1002_0000	0x1003_FFFF	128KB	AHB SRAM 2 (Alias) (2)	
	0x1000_0000	0x1001_FFFF	128KB	AHB SRAM 1 (Alias) (2)	
	0x0010_0000	0x0FFF_FFFF	255MB	Reserved	
	0x0000_0000	0x000F_FFFF	1MB	ITCM	INIT VTOR REMAP(1)

(1) Remapped using MMU_M4_BOOT_ADDR programmed by bootloader (CM7) during boot up

(2) Alias to maintain CM4 Harvard architecture where its code and data are accessed separately. Only available for CPUs.

(3) Size can be changed at boot/run time by OTP or software configuration.

For detailed addressing of peripherals, refer to the following table.

Table 2-6 N32H7xx peripheral addressing

Start Address	End Address	Size	Bus	Peripheral Registers
0x5810_0000	0x5FFF_FFFF	127MB	AHB5	Reserved
0x5803_9000	0x580F_FFFF	796KB		Reserved
0x5803_8000	0x5803_8FFF	4KB		Reserved
0x5803_7000	0x5803_7FFF	4KB		Reserved

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0x5803_6000	0x5803_6FFF	4KB		ECCMON3
0x5803_5800	0x5803_5FFF	2KB		Reserved
0x5803_5400	0x5803_57FF	1KB		DBGMCU
0x5803_5000	0x5803_53FF	1KB		GPIOK
0x5803_4C00	0x5803_4FFF	1KB		GPIOJ
0x5803_4800	0x5803_4BFF	1KB		GPIOI
0x5803_4400	0x5803_47FF	1KB		GPIOH
0x5803_4000	0x5803_43FF	1KB		GPIOG
0x5803_3C00	0x5803_3FFF	1KB		GPIOF
0x5803_3800	0x5803_3BFF	1KB		GPIOE
0x5803_3400	0x5803_37FF	1KB		GPIOD
0x5803_3000	0x5803_33FF	1KB		GPIOC
0x5803_2C00	0x5803_2FFF	1KB		GPIOB
0x5803_2800	0x5803_2BFF	1KB		GPIOA
0x5803_2400	0x5803_27FF	1KB		AFIO
0x5803_2000	0x5803_23FF	1KB		CRC
0x5803_1000	0x5803_1FFF	4KB		PWR
0x5803_0000	0x5803_0FFF	4KB		RCC
0x5800_5C00	0x5802_FFFF	169KB		Reserved
0x5800_5800	0x5800_5BFF	1KB		LPTIMER5
0x5800_5400	0x5800_57FF	1KB		RTC
0x5800_5000	0x5800_53FF	1KB		IWDG2
0x5800_4C00	0x5800_4FFF	1KB		IWDG1
0x5800_4800	0x5800_4BFF	1KB	APB5	COMPCTRL(COMP1-4)
0x5800_4400	0x5800_47FF	1KB		ATIMER4
0x5800_4000	0x5800_43FF	1KB		ATIMER3
0x5800_3C00	0x5800_3FFF	1KB		I2C10
0x5800_3800	0x5800_3BFF	1KB		I2C9

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0x5800_3400	0x5800_37FF	1KB		I2C8
0x5800_3000	0x5800_33FF	1KB		I2C7
0x5800_2C00	0x5800_2FFF	1KB		SPI7
0x5800_2800	0x5800_2BFF	1KB		SPI6
0x5800_2400	0x5800_27FF	1KB		SPI5
0x5800_2000	0x5800_23FF	1KB		SPI4
0x5800_1C00	0x5800_1FFF	1KB		LPTIMER4
0x5800_1800	0x5800_1BFF	1KB		LPTIMER3
0x5800_1400	0x5800_17FF	1KB		LPTIMER
0x5800_1000	0x5800_13FF	1KB		LPTIMER1
0x5800_0C00	0x5800_0FFF	1KB		LPUART2
0x5800_0800	0x5800_0BFF	1KB		LPUART1
0x5800_0400	0x5800_07FF	1KB		AFEC
0x5800_0000	0x5800_03FF	1KB		EXTI WKUP
0x5120_0000	0x57FF_FFFF	110MB	AHB6	Reserved
0x5112_1000	0x511F_FFFF	892KB		Reserved
0x5112_0800	0x5112_0FFF	2KB		MDMA_WRAPPER
0x5112_0000	0x5112_07FF	2KB		DMAMUX 2 (MDMA)
0x5111_C000	0x5111_FFFF	16KB		Reserved
0x5111_8000	0x5111_BFFF	16KB		OTPC
0x5111_0400	0x5111_7FFF	31KB		Reserved
0x5111_0100	0x5111_03FF	768B		Reserved
0x5111_0000	0x5111_00FF	256B		SDMMC1
0x5110_7400	0x5110_FFFF	35KB		Reserved
0x5110_7000	0x5110_73FF	1KB		SDMMC1_CFG
0x5110_6000	0x5110_6FFF	4KB		SDRAM
0x5110_5000	0x5110_5FFF	4KB		MMU
0x5110_4000	0x5110_4FFF	4KB		ECCMON1

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0x5110_2000	0x5110_3FFF	8KB		MDMA
0x5110_1000	0x5110_1FFF	4KB		xSPI2
0x5110_0000	0x5110_0FFF	4KB		xSPI1
0x5100_0000	0x510F_FFFF	1MB		GPV
0x5010_0000	0x50FF_FFFF	15MB		Reserved
0x500A_0000	0x500F_FFFF	384KB		Reserved
0x5009_1000	0x5009_FFFF	60KB		Reserved
0x5009_0800	0x5009_0FFF	2KB		JPEG CTRL
0x5009_0400	0x5009_07FF	1KB		JPEG P2H SGDMA
0x5009_0000	0x5009_03FF	1KB		JPEG BRC
0x5008_0800	0x5008_FFFF	62KB		Reserved
0x5008_0000	0x5008_07FF	2KB		JPEG DEC
0x5007_0800	0x5007_FFFF	62KB		Reserved
0x5007_0400	0x5007_07FF	1KB		JPEG H2P SGDMA
0x5007_0000	0x5007_03FF	1KB		JPEG RBC
0x5006_0000	0x5006_FFFF	64KB	APB6	JPEG ENC
0x5004_D000	0x5005_FFFF	76KB		Reserved
0x5004_C000	0x5004_CFFF	4KB		FEMC
0x5004_B000	0x5004_BFFF	4KB		TCMSRAMC
0x5004_AC00	0x5004_AFFF	1KB		DSIHOST_WRAPPER
0x5004_A800	0x5004_ABFF	1KB		WWDG1
0x5004_A000	0x5004_A7FF	2KB		LCDC
0x5004_9000	0x5004_9FFF	4KB		DVP2
0x5004_8000	0x5004_8FFF	4KB		DVP1
0x5004_4000	0x5004_7FFF	16KB		Reserved
0x5004_0000	0x5004_3FFF	16KB		2.5D GPU
0x5000_0000	0x5003_FFFF	256KB		DSI-Host
0x4020_0000	0x4FFF_FFFF	254MB	AHB2	Reserved

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0x4014_0400	0x401F_FFFF	767KB		Reserved
0x4014_0000	0x4014_03FF	1KB		USBCTRL1_WRAPPER
0x4010_0000	0x4013_FFFF	256KB		USBCTRL1
0x400F_9000	0x400F_FFFF	28KB		Reserved
0x400F_8000	0x400F_8FFF	4KB		DCMUB (CM4)
0x400F_7000	0x400F_7FFF	4KB		DCMUA (CM7)
0x400F_6000	0x400F_6FFF	4KB		SEMA4
0x400F_4000	0x400F_5FFF	8KB		ETH1
0x400F_2000	0x400F_3FFF	8KB		SDPU
0x400F_1C00	0x400F_1FFF	1KB		DAC56
0x400F_1800	0x400F_1BFF	1KB		DAC34
0x400F_1400	0x400F_17FF	1KB		FMAC
0x400F_1000	0x400F_13FF	1KB		CORDIC
0x400F_0000	0x400F_0FFF	4KB		ECCMON2
0x400D_FC00	0x400E_FFFF	65KB	APB2	Reserved
0x400D_F800	0x400D_FBFF	1KB		UART15
0x400D_F400	0x400D_F7FF	1KB		UART14
0x400D_F000	0x400D_F3FF	1KB		UART13
0x400D_EC00	0x400D_EFFF	1KB		USART8
0x400D_E800	0x400D_EBFF	1KB		USART7
0x400D_E400	0x400D_E7FF	1KB		USART6
0x400D_E000	0x400D_E3FF	1KB		USART5
0x400D_DC00	0x400D_DFFF	1KB		I2C6
0x400D_D800	0x400D_DBFF	1KB		I2C5
0x400D_D400	0x400D_D7FF	1KB		I2C4
0x400D_D000	0x400D_D3FF	1KB		GTIMERA3
0x400D_CC00	0x400D_CFFF	1KB		GTIMERA2
0x400D_C800	0x400D_CBFF	1KB		GTIMERA1

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0x400D_C400	0x400D_C7FF	1KB		SPI2
0x400D_C000	0x400D_C3FF	1KB		SPI1
0x400D_BC00	0x400D_BFFF	1KB		I2S2
0x400D_B800	0x400D_BBFF	1KB		I2S1
0x400D_B400	0x400D_B7FF	1KB		ATIMER2
0x400D_B000	0x400D_B3FF	1KB		ATIMER1
0x400D_A000	0x400D_AFFF	4KB		DSMU
0x400D_9000	0x400D_9FFF	4KB		SHRTIM2
0x400D_8000	0x400D_8FFF	4KB		SHRTIM1
0x400D_1000	0x400D_7FFF	28KB		Reserved
0x400D_0C00	0x400D_0FFF	1KB		FDCAN 8
0x400D_0800	0x400D_0BFF	1KB		FDCAN 7
0x400D_0400	0x400D_07FF	1KB		FDCAN 4
0x400D_0000	0x400D_03FF	1KB		FDCAN 3
0x400C_0400	0x400C_FFFF	63KB		Reserved
0x400C_0000	0x400C_03FF	1KB	AHB9	ESC_WRAPPER
0x400B_0000	0x400B_FFFF	64KB		ESC
0x400A_8000	0x400A_FFFF	32KB		Reserved
0x400A_0400	0x400A_7FFF	31KB		Reserved
0x400A_0000	0x400A_03FF	1KB		USBCTRL2 WRAPPER
0x4006_0000	0x4009_FFFF	256KB		USBCTRL2
0x4005_0400	0x4005_FFFF	63KB		Reserved
0x4005_0100	0x4005_03FF	768B		Reserved
0x4005_0000	0x4005_00FF	256B		SDMMC2
0x4004_A400	0x4004_FFFF	23KB		Reserved
0x4004_A000	0x4004_A3FF	1KB		SDMMC2_CFG
0x4004_9800	0x4004_9FFF	2KB	AHB1	Reserved
0x4004_9400	0x4004_97FF	1KB		Reserved

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0x4004_9000	0x4004_93FF	1KB		Reserved
0x4004_8800	0x4004_8FFF	2KB		Reserved
0x4004_8400	0x4004_87FF	1KB		Reserved
0x4004_8000	0x4004_83FF	1KB		Reserved
0x4004_7400	0x4004_7FFF	3KB		Reserved
0x4004_7000	0x4004_73FF	1KB		DMA3
0x4004_6C00	0x4004_6FFF	1KB		DMA2
0x4004_6800	0x4004_6BFF	1KB		DMA1
0x4004_6400	0x4004_67FF	1KB		DMAMUX1 (DMA1-3)
0x4004_6000	0x4004_63FF	1KB		Reserved
0x4004_5000	0x4004_5FFF	4KB		AHB_CACHE_PARMON
0x4004_4C00	0x4004_4FFF	1KB		Reserved
0x4004_4800	0x4004_4BFF	1KB		ADC3
0x4004_4400	0x4004_47FF	1KB		ADC2
0x4004_4000	0x4004_43FF	1KB		ADC1
0x4004_2000	0x4004_3FFF	8KB		ETH2
0x4004_0000	0x4004_1FFF	8KB		Reserved
0x4001_1400	0x4003_FFFF	187KB		Reserved
0x4001_1000	0x4001_13FF	1KB		Reserved
0x4001_0C00	0x4001_0FFF	1KB		BTIMER4
0x4001_0800	0x4001_0BFF	1KB		BTIMER3
0x4001_0400	0x4001_07FF	1KB		Reserved
0x4001_0000	0x4001_03FF	1KB	APB1	WWDG2
0x4000_FC00	0x4000_FFFF	1KB		DAC12
0x4000_F800	0x4000_FBFF	1KB		I2S4
0x4000_F400	0x4000_F7FF	1KB		I2S3
0x4000_F000	0x4000_F3FF	1KB		I2C3
0x4000_EC00	0x4000_EFFF	1KB		I2C2

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0x4000_E800	0x4000_EBFF	1KB		I2C1
0x4000_E400	0x4000_E7FF	1KB		SPI3
0x4000_E000	0x4000_E3FF	1KB		UART12
0x4000_DC00	0x4000_DFFF	1KB		UART11
0x4000_D800	0x4000_DBFF	1KB		UART10
0x4000_D400	0x4000_D7FF	1KB		UART9
0x4000_D000	0x4000_D3FF	1KB		USART4
0x4000_CC00	0x4000_CFFF	1KB		USART3
0x4000_C800	0x4000_CBFF	1KB		USART2(1)
0x4000_C400	0x4000_C7FF	1KB		USART1(1)
0x4000_C000	0x4000_C3FF	1KB		GTIMERA7
0x4000_BC00	0x4000_BFFF	1KB		GTIMERA6
0x4000_B800	0x4000_BBFF	1KB		GTIMERA5
0x4000_B400	0x4000_B7FF	1KB		GTIMERA4
0x4000_B000	0x4000_B3FF	1KB		GTIMERB3
0x4000_AC00	0x4000_AFFF	1KB		GTIMERB2
0x4000_A800	0x4000_ABFF	1KB		GTIMERB1
0x4000_A400	0x4000_A7FF	1KB		BTIMER2
0x4000_A000	0x4000_A3FF	1KB		BTIMER1
0x4000_9000	0x4000_9FFF	4KB		AHB dCache
0x4000_8000	0x4000_8FFF	4KB		AHB iCache
0x4000_1000	0x4000_7FFF	28KB		Reserved
0x4000_0C00	0x4000_0FFF	1KB		FDCAN 6
0x4000_0800	0x4000_0BFF	1KB		FDCAN 5
0x4000_0400	0x4000_07FF	1KB		FDCAN 2
0x4000_0000	0x4000_03FF	1KB		FDCAN 1

(1) Even though USART1/2 are in APB1 region, their bus clocks can be as high as AHB1 hclk. This is to support high baud rate up to 25Mbps.

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2.3 N32Hxxx memories

2.3.1 Introduction

N32Hxxx feature an embedded scattered SRAM of different sizes, SIP (Silicon-in-Package) Flash and external memory interfaces such as FEMC, SDRAM, and xSPI2. The scattered architecture configuration gives the flexibility to partition the memory resources following the application requirements in order to obtain the right performance trade-off versus application code size, data size, and power saving. In addition, an embedded ROM is used as an initial bootloader and secure boot, whereas an embedded OTP is used for non-volatile system and user configuration.

2.3.2 Embedded SRAM

N32Hxxx devices include a large internal RAM of up to 1484KB divided into up to eleven blocks and scattered in four domains.

TCM RAMs located in the Cortex-M7 CPU core domain

RAMs located in this domain are the following:

- Up to 1MB of instruction RAM (ITCM-RAM)

  ITCM RAM is mapped at address 0x0000 0000. It can only be accessed by Cortex-M7 CPU core and MDMA (even if CPU is in sleep mode). It is accessible by the CPU through ITCM bus and by the MDMA through the AHBS bus of the core. It is accessible by the Cortex-M7 by bytes, half-words (16 bits), words

  (32 bits) or double words (64 bits). The ITCM-RAM can be accessed at the maximum CPU clock frequency without wait states.

  The ITCM-RAM size can be increased up to 1MB with a granularity of 128KB at the expense of DTCM-RAM and AXI-SRAM2/3.

- Up to 1MB of data RAM (DTCM-RAM)

  It is split into two DTCM-RAMs with 32-bit access each. Both memories are connected respectively to the D0TCM and D1TCM ports of the Cortex-M7 as shown in Figure 2-2 and can be used in parallel (for load/store operations) thanks to the Cortex- M7 dual issue capability.

  The DTCM-RAM is mapped on the DTCM interface at address 0x2000 0000. It be accessed by the Cortex-M7 through the DTCM bus and by the MDMA through the AHBS bus of the Cortex-M7. It is accessible by the Cortex-M7 by bytes, half-words (16 bits), words (32 bits) or double words (64 bits).

  The DTCM-RAM is accessible at the maximum Cortex-M7 clock speed without any latency. Concurrent accesses to the DTCM-RAM by the Cortex-M7 and the MDMA as well as their priorities can be handled by the slave control register of the Cortex-M7 itself (CM7_AHBSCR register). A higher priority can be given to the Cortex-M7 to access the DTCM-RAM versus the MDMA. For more details of this register, refer to Arm Cortex-M7 processor - technical reference manual.

RAMs located in the AXI bus domain

RAMs located in the AXI bus domain are as follows:

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- 128KB of AXI SRAM 1

  The AXI SRAM 1 is mapped at address 0x2400 0000. It can be accessed by all masters located only in AXI and AHB bus matrix 1 domain through the AHB inter-domain bus AHB4. The DAP-AP1 master located in AHB bus matrix 2 domains cannot access this memory.

  The AXI SRAM 1 is connected to the AXI bus matrix through a 64-bit wide AXI bus and can be accessed as bytes (8 bits), half-words (16 bits), full-words (32 bits) or double-words (64 bits). Refer to Table 2-1 for all the possible AXI SRAM 1 accesses. The AXI SRAM can be used for read/write data storage as well as for code execution. It is accessed at the same frequency as the AXI bus matrix (up to 300MHz).

- Up to 512KB of AXI RAM 2 (shared with ITCM and DTCM)

  It can be shared between I/DTCM or AXI SRAM 2 with a 128-Kbyte granularity. When used as AXI SRAM 2, it is accessed as the AXI SRAM, except that it is mapped at address 0x2402 0000 contiguous to the fixed AXI SRAM 1. It can be accessed as bytes (8 bits), half-words (16 bits), full-words (32 bits) or double-words (64 bits).

  This feature can be configured through the TCM_SZ_CFG_OTP option byte or software configuration in TCM. Refer to TCM chapter 2.5 for more details.

- Up to 512KB of AXI RAM 3 (shared with ITCM and DTCM)

  It can be shared between I/DTCM or AXI SRAM 3 with a 128-Kbyte granularity. When used as AXI SRAM 4, it is accessed as the AXI SRAM, except that it is mapped at address 0x240A 0000 contiguous to the AXI SRAM 2. It can be accessed as bytes (8 bits), half-words (16 bits), full-words (32 bits) or double-words (64 bits).

  This feature can be configured through the TCM_SZ_CFG_OTP option byte or software configuration in TCM. Refer to TCM chapter 2.5 for more details.

RAMs located in the AHB bus domain 1

The AHB SRAM1, SRAM2, SRAM 3, SRAM 4, and SRAM5 can be accessed by all masters located only in the AXI and AHB bus matrix 1 through the AHB inter-domain bus AHB7. They are accessible by bytes, half-words (16 bits) or words (32 bits). Refer to Table 2-1 for possible SRAM1-5 accesses. They can be used for read/write data storage as well as code execution. These memories are accessed at the AHB bus matrix frequency (up to 300MHz). Each memory has its own AHB bus that connects it to the AHB bus matrix. This enables removing bus contention and keeping high system performance when it is concurrently accessed by more than one master.

Below are the AHB SRAM base addresses:

- The AHB SRAM1 of up to 128 Kbytes is mapped at address 0x3000 0000.
- The AHB SRAM2 of up to 128 Kbytes is mapped at address 0x3002 0000.
- The AHB SRAM3 of 32 Kbytes is mapped at address 0x3004 0000.
- The AHB SRAM4 of 32 Kbytes is mapped at address 0x3004 8000.
- The AHB SRAM5 of 32 Kbytes is mapped at address 0x3005 0000.

The above SRAMs can be used by local DMAs (located in the AHB bus matrix 1 domain) as buffers for data from/to peripherals in that domain. Data can be transferred to the AHB bus matrix 1 domain at the end of a transfer using

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MDMA for Cortex-M7 high-speed processing. In addition, AHB SRAM 5 is split into 2 banks and can be shared with FDCAN1-8 as their local RAMs in such applications that required for frame data buffering.

RAMs located in the AHB bus domain 2

Backup SRAM, located in the AHB bus domain 2, can be accessed by most of masters located only in the AXI and AHB bus matrix 1 through the AHB inter-domain bus AHB3 and AHB8 at the base address of 0x3800 0000. Refer to Table 2-1 for possible Backup SRAM accesses. It can be accessed by bytes, half-words (16 bits) or words (32 bits).

All internal system RAMs includes error correction code (ECC). ECC can be programmable through respective ECC monitor modules. Refer to ECCMON chapter for more details.

2.3.3 Embedded ROM

N32Hxxxx feature an embedded ROM of 32KB. It consists of a small bootloader that will allow the chip to boot up from other sources such as external Flash.

The embedded ROM is mapped at address 0x1FFF 0000. It is divided into 2 parts: secure code and API. Secure code can only be accessed by Cortex-M7 whereas API region can be accessed by both Cortex M7 and Cortex-M4 CPUs.

The AXI ROM is connected to the AXI bus matrix through a 64-bit wide AXI bus and can be accessed as bytes (8 bits), half-words (16 bits), full-words (32 bits) or double-words (64 bits). It is accessed at the same frequency as the AXI bus matrix (up to 300MHz).

ROM is protected by ECC. Refer to chapter 2.4.

2.3.4 Embedded OTP

N32Hxxxx feature an embedded OTP of 4KB. It is used to store non-volatile information and configurations.

- Manufacturing data: Memory repair, analog trim, chip ID, etc.
- Boot configuration
- Key and security sensitive information (Nations secret keys, etc.)
- User configuration such as option bytes

It is not directly mapped but indirectly accessed via 32-bit AHB6 bus, connected to AXI bus matrix. Only 32-bit access is allowed.

2.3.5 SIP FLASH

Some of N32Hxxx devices feature a SIP Flash device with the size of up to 32MB as shown in Table 2-7.

The first 128KB is used as follows:

- BOOTPATCH: up to 112KB in size, used as a patch for BOOTROM API update
- OB_FLASH: up to 8KB in size, used for non-volatile configuration by end users depending on application requirements

Remaining is used for user application code.

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Table 2-7 SIP Flash memory organization

Name	Size (KB)	Physical Address		Bus Address	
		Begin	End	Begin	End
BOOTPATCH	112	0x80000000	0x8001BFFF	0x1FF00000	0x1FF1BFFF
OB_FLASH	8	0x8001C000	0x8001DFFF	0x1FFF8000	0x1FFF9FFF
Reserved	8	0x8001E000	0x8001FFFF	0x1FFFA000	0x1FFFBFFF
Flash Main (User App)	Max. 3968	0x80020000	0x803FFFFF	0x15000000	0x153DFFFF

Table 2-8 SIP Flash Main bank addressing

Flash Size (KB) [1]	Physical Address		Bus Address	
	Begin	End	Begin	End
2048	0x80020000	0x801FFFFF	0x15000000	0x151DFFFF
4096	0x80020000	0x803FFFFF	0x15000000	0x153DFFFF

(1) First 128KB always is fixed to be used as BOOTPATCH/OB_FLASH.

2.3.6 External Memories

In addition to the internal memories and storage controllers such as USB and SDMMC, users can extend N32Hxxx memories with the flexible memory controller (FEMC), SDRAM controller, and xSPI controller as shown in Table 2-9.

FEMC SRAM/PSRAM/NOR FLASH

Four external memory banks of 64MB each are dedicated to the FEMC SRAM/PSRAM/NOR Flash, starting from 0x6000 0000.

FEMC NAND FLASH

Two banks of FEMC NAND memories are mapped at 0xA000 0000 with maximum size of up to 256MB per bank.

SDRAM

Up to two SDRAM devices can be supported with up to 256MB per bank. The base address for SDRAM 1 is 0xC000 0000 whereas SDRAM 2 is mapped at 0xD000 0000. SDRAM 1 mapping can be swapped with FEMC SRAM/PSRAM/NOR FLASH via FEMC_CR register.

xSPI Flash Memories

xSPI interface is a specialized communication interface targeting single, dual or quad SPI Flash memories. It can extend the internal Flash memory by 256MB per instance and can be used to store data such as images in graphical applications or to contain code to execute the user application.

Table 2-9 External memory mapping

Start Address	End Address	Size	Memory Allocation
0xD000_0000	0xDFFF_FFFF	256MB	SDRAM 2
0xCC00_0000	0xCFFF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 4)
0xC800_0000	0xCBFF_FFFF	64MB	SDRAM 1

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Start Address	End Address	Size	Memory Allocation
			(or remap of FEMC SRAM/NOR/PSRAM bank 3)
0xC400_0000	0xC7FF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 2)
0xC000_0000	0xC3FF_FFFF	64MB	SDRAM 1 (or remap of FEMC SRAM/NOR/PSRAM bank 1)
0xB000_0000	0xBFFF_FFFF	256MB	FEMC NAND Flash Memory bank 2
0xA000_0000	0xAFFF_FFFF	256MB	FEMC NAND Flash Memory bank 1
0x9000_0000	0x9FFF_FFFF	256MB	xSPI2
0x8000_0000	0x8FFF_FFFF	256MB	xSPI1
0x7000_0000	0x7FFF_FFFF	256MB	Reserved
0x6C00_0000	0x6FFF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 4 (or remap of SDRAM 1 bank 4)
0x6800_0000	0x6BFF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 3 (or remap of SDRAM 1 bank 3)
0x6400_0000	0x67FF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 2 (or remap of SDRAM 1 bank 2)
0x6000_0000	0x63FF_FFFF	64MB	FEMC SRAM/NOR/PSRAM bank 1 (or remap of SDRAM 1 bank 1)

2.4 ECC Monitoring (ECCMON)

2.4.1 Introduction

N32Hxxx provides a RAM/ROM ECC monitoring unit that observes ECC status and informs application software if there is any ECC error occurs during the RAM/ROM access.

2.4.2 Main features

Embedded SRAMs/ROM are protected by ECC. The ECC mechanism is based on SECDED algorithm. It support single-bit and double-bit error detection as well as single-bit error correction.

- ECC bits added per 32-bit word
- ECC bits added per 64-bit word for ITCM-RAM and AXI-SRAM1

ECC is checked if enabled at each memory read access or partial RAM word write operation.

The ECCMON supports the following features:

- Programmable ECC enable
- Bypass temporary data register (only applicable to AHB SRAMs)
- 1-bit/2-bit error injection

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- ECC fail event interrupt generation
- Memory failing address/data identification
- ECC error event outputs

2.4.3 Functional Description

2.4.3.1 Block diagram

An RAM/ROM ECC Controller is attached to each RAM/ROM region in N32Hxxx. It performs the followings

- ECC encoding: ECC code computation and writing into SRAM
- ECC decoding: memory data loading and ECC code decoding for error detection
- Error detection: single-bit and double-bit error correction
- Error correction: single-bit error correction
- Efficient partial write access: RAM ECC controller performs read-modify-write on partial write accesses. To efficiently handle the partial write access in such applications that data is written on a byte basis within a loop, the read-modify-write data will be temporarily held to a 32-bit buffer until the full word write to the same address is complete before writing into SRAM. Otherwise, the data in the buffer will be written back to the memory at the next access if the access is read, or write with the different word address. This feature is programmable by software.
- Error injection: single-bit and double-bit error injection for debug and testing purposes

A dedicated ECCMON is associated with each RAM domain (refer to chapter 2.4.3.2 ECCMON mapping). This allows the collection of ECC statuses from all RAM/ROM ECC Controllers and provides a mechanism for CPU to check ECC status.

Figure 2-3 shows the block diagram of an ECCMON module. ECCMON modules collects ECC statuses from RAM/ROM ECC controllers as follows:

- s*_ecc_wr_e1: single bit error indication during partial write operation. Only applied for RAM.
- s*_ecc_rd_e1: single bit error indication during read operation
- s*_ecc_wr_e2: double bit error indication during partial write operation. Only applied for RAM.
- s*_ecc_rd_e2: double bit error indication during partial write operation
- s*_ecc_adr: failing address
- s*_ecc_ddt: failing data
- s*_ecc_edt: failing ECC code

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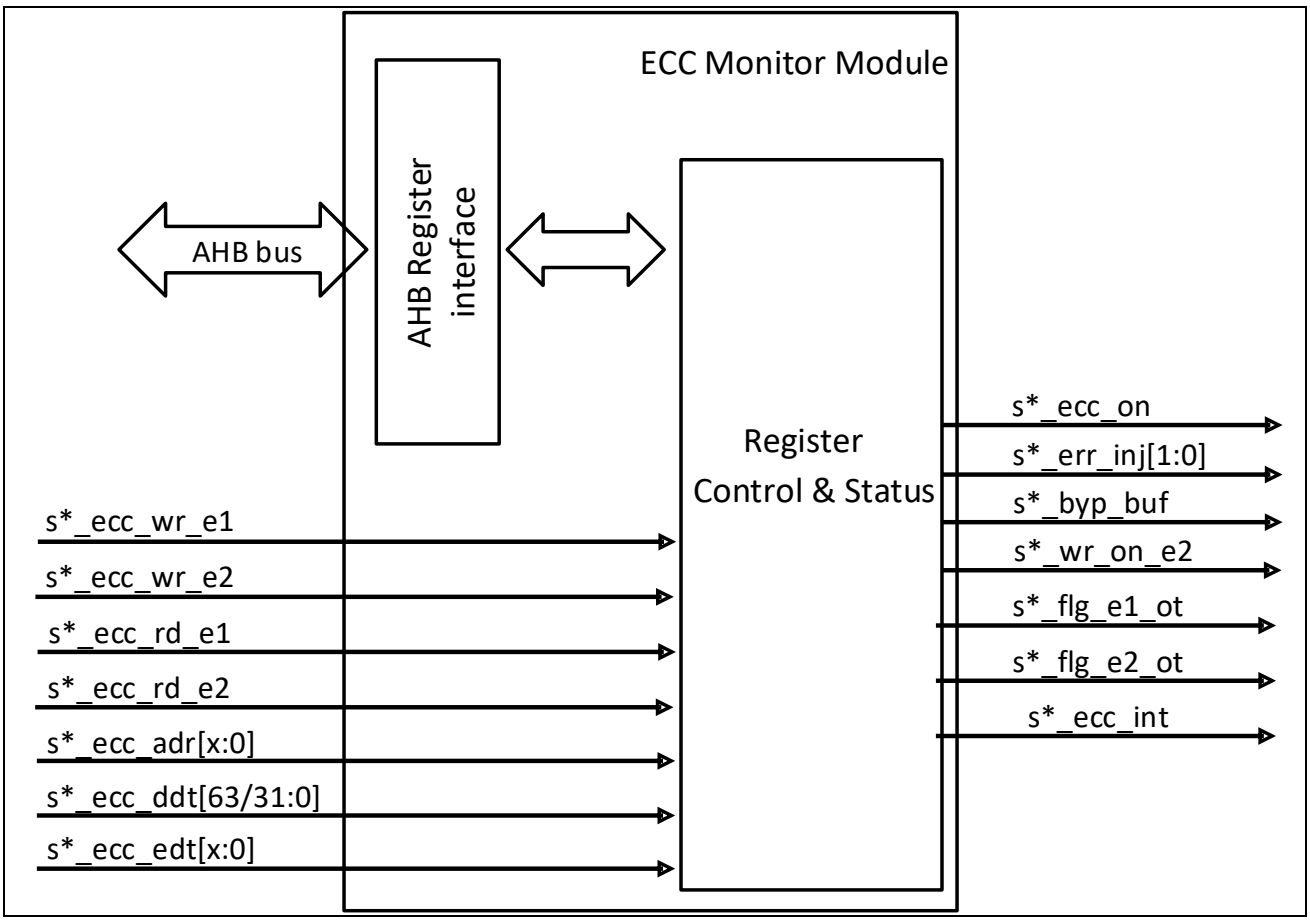
Figure 2-3 Block diagram of ECCMON module



In addition, ECCMON provides the following controls to RAM/ROM ECC Controllers:

- s*_ecc_on: enable ECC encoding and decoding, programmable by software
- s*_err_inj: error injection for debug and testing purposes
- s*_byp_buf: optionally bypass the temporary data buffer in AHB RAM ECC controller
  - If s*_byp_buf bit is set to "0" (by default), during the partial write, the read-modify-write data will be temporarily written to a 32-bit buffer instead of RAM. If s*_byp_buf bit is set to "1", every partial write triggers read-modify-write to the memory directly.
- s*_wr_on_e2: an option to over-write the data when 2-bit ECC error is detected on read-modify-write access; by default the over-write is bypassed. That means for that 32-bit word will be remained unchanged, no write operation is taken place. This is only applied for RAM.

2.4.3.2 ECCMON monitor mapping

N32Hxxx includes 3 ECCMON units. The inputs from RAM/ROM ECC controllers are mapped as described in Table 2-10. The ECC status and control registers are described in chapter 2.4.1.

Table 2-10 ECCMON mapping

ECCMON units	Monitoring number	SRAM	Index (n)	Address Offset

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ECCMON1	1	AXI ROM with 64-bit data and 8-bit ECC code	1	0x000
		AXI SRAM1 with 64-bit data and 8-bit ECC code	2	
	2	AXI SRAM2 with 64-bit data and 7-bit ECC code per 32-bit word (arranged as 16-bit ECC in ECCMON registers)	1	0x400
		AXI SRAM3 with 64-bit data and 7-bit ECC code per 32-bit word (arranged as 16-bit ECC in ECCMON registers)	2	
	3	ITCM SRAM with 64-bit data and 8-bit ECC	1	0x800
	4	D0TCM with 32-bit data and 7-bit ECC code	1	0xC00
		D1TCM with 32-bit data and 7-bit ECC code	2	
ECCMON2	NA	AHB SRAM1 with 32-bit data and 7-bit ECC code	1	0x000
		AHB SRAM2 with 32-bit data and 7-bit ECC code	2	
		AHB SRAM3 with 32-bit data and 7-bit ECC code	3	
		AHB SRAM4 with 32-bit data and 7-bit ECC code	4	
		AHB SRAM5 bank 1 with 32-bit data and 7-bit ECC code	5	
		AHB SRAM5 bank 2 with 32-bit data and 7-bit ECC code	6	
ECCMON3	NA	Backup SRAM with 32-bit data and 7-bit ECC code	1	0x000

2.4.4 ECCMON registers

ECCMON registers can be accessed by bytes, half-words (16 bits) or words (32 bits). Note that "*n*" represents the index number of the respective memory as shown in the Table 2-10.

2.4.4.1 ECCMON Control Register 1(ECCMON_CTRL1)

Address Offset: 0x00

Reset value: 0x01(only ECCMON1P1) , 0x0(except ECCMON1P1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	E2INTEN	Reserved	E1INTEN
	rw		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Reserved	TDRBYP	Reserved	ECCEN
	rw		rw

Bit Field	Field Name	Description
31:30	Reserved	Reserved,the reset value must be maintained
29:24	E2INTEN[5:0]	ECC 2-bit Error detection and correction interrupt enable Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. 0: interrupt is disabled 1: interrupt is enabled
23:22	Reserved	Reserved,the reset value must be maintained
21:16	E1INTEN[5:0]	ECC 1-bit Error detection and correction interrupt enable Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. 0: interrupt is disabled 1: interrupt is enabled
15:14	Reserved	Reserved,the reset value must be maintained
13:8	TDRBYP[5:0]	Temporary data register bypass control Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. 0: the temporary data register is used to temporarily store read-modify-write data on partial write access 1: the temporary data register is bypassed, the read-modify-write data is written back the memory Note: this is only applied for ECCMON2 and ECCMON3
7:6	Reserved	Reserved,the reset value must be maintained
5:0	ECCEN[5:0]	ECC enable 0: ECC is disabled 1: ECC is enabled Default is disabled for all, except ROM. The corresponding memory for each bit as follows:

	ECCMON1P1	ECCMON1P2	ECCMON1P3	ECCMON1P4	ECCMON2	ECCMON3
bit 0	AXI ROM	AXI SRAM2	ITCM SRAM	D0TCM	AHB SRAM1	Backup SRAM

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		bit 1	AXI SRAM1	AXI SRAM3	Reserved	D1TCM	AHB SRAM2	Reserved
		bit 2	Reserved	Reserved	Reserved	Reserved	AHB SRAM3	Reserved
		bit 3	Reserved	Reserved	Reserved	Reserved	AHB SRAM4	Reserved
		bit 4	Reserved	Reserved	Reserved	Reserved	AHB SRAM5 bank1	Reserved
		bit 5	Reserved	Reserved	Reserved	Reserved	AHB SRAM5 bank2	Reserved

2.4.4.2 ECCMON Control Register 2(ECCMON_CTRL2)

Address Offset: 0x04

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		E2FOEN						Reserved		E1FOEN					
		rw								rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										WROE2EN					
										rw					

Bit Field	Field Name	Description
31:30	Reserved	Reserved,the reset value must be maintained
29:24	E2FOEN[5:0]	ECC 2-bit error flag output enable. Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. 1: (E2DCIFR | E2DCIFW) is output to S*n*_FLG_E2_OT port. 0: Disabled. Note: When it is enabled the output will remain active (HIGH) until all E2DCIFR and E2DCIFW are cleared.
23:22	Reserved	Reserved,the reset value must be maintained
21:16	E1FOEN[5:0]	ECC 1-bit error flag output enable. Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN.

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		1: (E1DCIFR | E1DCIFW) is output to S*n*_FLG_E1_OT port. 0: Disabled. Note: When it is enabled, the output will remain active (HIGH) until all E1DCIFR and E1DCIFW are cleared.
15:6	Reserved	Reserved,the reset value must be maintained
5:0	WROE2EN[5:0]	Partial write on ECC 2-bit enable Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. 1: allow partial write to perform read-modify-write to the memory while ECC 2-bit error is detected. 0: not to allow partial write to over write the data if ECC 2-bit error is detected.

2.4.4.3 ECCMON Error Injection Register (ECCMON_EINJ)

Address Offset: 0x08

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				ECSEL6		ECSEL5		ECSEL4		ECSEL3		ECSEL2		ECSEL1	
				rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				ERICTR6		ERICTR5		ERICTR4		ERICTR3		ERICTR2		ERICTR1	
				rw		rw		rw		rw		rw		rw	

Bit Field	**Field Name**	**Description**
31:28	Reserved	Reserved,the reset value must be maintained
27:26	ECSEL6[1:0]	ECC error event capture selection for memory 6- AHB SRAM5 bank2 00: Capture first encounter of ECC error event. It can be 1-bit or 2-bit ECC error event. 01: Capture first encounter of 1-bit ECC error event only. 10: Capture first encounter of 2-bit ECC error event only. 11: No capture. Note: Changing from one mode to another mode, the corresponding Flags, EER, EEW, E1EAD and E2EAD will be cleared.this is only applied for ECCMON2
25:24	ECSEL5[1:0]	ECC error event capture selection for memory 5- AHB SRAM5 bank1 00: Capture first encounter of ECC error event. It can be 1-bit or 2-bit ECC error event. 01: Capture first encounter of 1-bit ECC error event only. 10: Capture first encounter of 2-bit ECC error event only. 11: No capture.

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		Note: Changing from one mode to another mode, the corresponding Flags, EER, EEW, E1EAD and E2EAD will be cleared.this is only applied for ECCMON2
23:22	ECSEL4[1:0]	ECC error event capture selection for memory 4- AHB SRAM4 00: Capture first encounter of ECC error event. It can be 1-bit or 2-bit ECC error event. 01: Capture first encounter of 1-bit ECC error event only. 10: Capture first encounter of 2-bit ECC error event only. 11: No capture. Note: Changing from one mode to another mode, the corresponding Flags, EER, EEW, E1EAD and E2EAD will be cleared.this is only applied for ECCMON2
21:20	ECSEL3[1:0]	ECC error event capture selection for memory 3- AHB SRAM3 00: Capture first encounter of ECC error event. It can be 1-bit or 2-bit ECC error event. 01: Capture first encounter of 1-bit ECC error event only. 10: Capture first encounter of 2-bit ECC error event only. 11: No capture. Note: Changing from one mode to another mode, the corresponding Flags, EER, EEW, E1EAD and E2EAD will be cleared.this is only applied for ECCMON2
19:18	ECSEL2[1:0]	ECC error event capture selection for memory 2 00: Capture first encounter of ECC error event. It can be 1-bit or 2-bit ECC error event. 01: Capture first encounter of 1-bit ECC error event only. 10: Capture first encounter of 2-bit ECC error event only. 11: No capture. Note: Changing from one mode to another mode, the corresponding Flags, EER, EEW, E1EAD and E2EAD will be cleared.this is only applied for ECCMON1 and ECCMON2 For the memory corresponding to each ECCMON ,refer to ERICTR2
17:16	ECSEL1[1:0]	ECC error event capture selection for memory 1 00: Capture first encounter of ECC error event. It can be 1-bit or 2-bit ECC error event. 01: Capture first encounter of 1-bit ECC error event only. 10: Capture first encounter of 2-bit ECC error event only. 11: No capture. Note: Changing from one mode to another mode, the corresponding Flags, EER, EEW, E1EAD and E2EAD will be cleared. For the memory corresponding to each ECCMON ,refer to ERICTR1
15:12	Reserved	Reserved,the reset value must be maintained
11:10	ERICTR6[1:0]	Error injection control for memory 6- AHB SRAM5 bank2 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output Note: this is only applied for ECCMON2
9:8	ERICTR5[1:0]	Error injection control for memory 5- AHB SRAM5 bank1 00: no error injection 01 or 10: 1-bit error is injected to 32-bit memory output 11: 2-bit errors are injected to 32-bit memory output

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<table>
<tr><td></td><td></td><td>Note: this is only applied for ECCMON2</td></tr>
<tr><td>7:6</td><td>ERICTR4[1:0]</td><td>Error injection control for memory 4- AHB SRAM4
00: no error injection
01 or 10: 1-bit error is injected to 32-bit memory output
11: 2-bit errors are injected to 32-bit memory output
Note: this is only applied for ECCMON2</td></tr>
<tr><td>5:4</td><td>ERICTR3[1:0]</td><td>Error injection control for memory 3- AHB SRAM3
00: no error injection
01 or 10: 1-bit error is injected to 32-bit memory output
11: 2-bit errors are injected to 32-bit memory output
Note: this is only applied for ECCMON2</td></tr>
<tr><td>3:2</td><td>ERICTR2[1:0]</td><td>Error injection control for memory 2
00: no error injection
01 or 10: 1-bit error is injected to 32-bit memory output
11: 2-bit errors are injected to 32-bit memory output
Note: this is only applied for ECCMON1 and ECCMON2
<table>
<tr><th></th><th>ECCMON1P1</th><th>ECCMON1P2</th><th>ECCMON1P4</th><th>ECCMON2</th></tr>
<tr><td>memory</td><td>AXI SRAM1</td><td>AXI SRAM3</td><td>D1TCM</td><td>AHB SRAM2</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>ERICTR1[1:0]</td><td>Error injection control for memory 1
00: no error injection
01 or 10: 1-bit error is injected to 32-bit memory output
11: 2-bit errors are injected to 32-bit memory output
<table>
<tr><th></th><th>ECCMON1P1</th><th>ECCMON1P2</th><th>ECCMON1P3</th><th>ECCMON1P4</th><th>ECCMON2</th><th>ECCMON3</th></tr>
<tr><td>memory</td><td>AXI ROM</td><td>AXI SRAM2</td><td>ITCM SRAM</td><td>D0TCM</td><td>AHB SRAM1</td><td>Backup SRAM</td></tr>
</table></td></tr>
</table>

2.4.4.4 ECCMON Interrupt Flag Shadow Register (ECCMON_INTFS)

Address Offset: 0x0C

Reset value: 0x0

Bit Field	Field Name	Description

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31:22	Reserved	Reserved,the reset value must be maintained
21:16	E2DCIF[5:0]	ECC 2-bit error detected and corrected interrupt pending flag Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. This bit is ECC 2-bit error detection interrupt pending flag shadow register. It is set to "1" while either E2DCIFR or E2DCIFW is set to "1".
15:6	Reserved	Reserved,the reset value must be maintained
5:0	E1DCIF[5:0]	ECC 1-bit error detected and corrected interrupt pending flag Each bit corresponds to a different memory, the corresponding memory for each bit refer to ECCMON_CTRL1.ECCEN. This bit is ECC 1-bit error detection and correction interrupt pending flag shadow register. It is set to "1" while either E1DCIFR or E1DCIFW is set to "1".

2.4.4.5 ECCMON Mermory x Interrupt Flag Register (ECCMON_INTFx, x=1~n)

Address Offset: (5x-1) *4, x=1~n

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												E2DCIFR	E1DCIFR	E2DCIF	E1DCIF
												rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Field Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3	E2DCIFR	ECC 2-bit error detection and correction interrupt pending flag on read access. 0: the above error is not detected 1: the above error is detected Write "1" to this bit to clear this flag. An interrupt will be generated when this is set and its corresponding interrupt enable bit (E2INTEN) is set.
2	E1DCIFR	ECC 1-bit error detection and correction interrupt pending flag on read access. 0: the above error is not detected 1: the above error is detected Write "1" to this bit to clear this flag. An interrupt will be generated when this is set and its corresponding interrupt enable bit (E2INTEN) is set.

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1	E2DCIFW	ECC 2-bit error detection and correction interrupt pending flag on partial write access. 0: the above error is not detected 1: the above error is detected Write "1" to this bit to clear this flag. An interrupt will be generated when this is set and its corresponding interrupt enable bit (E2INTEN) is set.
0	E1DCIFW	ECC 1-bit error detection and correction interrupt pending flag on partial write access. 0: the above error is not detected 1: the above error is detected Write "1" to this bit to clear this flag. An interrupt will be generated when this is set and its corresponding interrupt enable bit (E1INTEN) is set.

2.4.4.6 ECCMON Mermory x ECC Fail Event Address Register (ECCMON_FEADRx, x=1~n)

Address Offset: (5x) *4, x=1~n

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E2EAD	E1EAD	EER	EEW	EFADR											
rc_w1	rc_w1	rc_w1	rc_w1	r											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFADR															
r															

Bit Field	Field Name	Description
[31]	E2EAD	ECC 2-bit error event and failing address detected Refer to ECSELx register for ECC error event capture rules. This bit is set to "1" by hardware, which indicates the ECC 2-bit error event is detected and its associated failing address, the data and the ECC code are captured to EFADR, ERDAT and ERCOD registers respectively. Note: Write "1" to clear this bit, and at the same time it will clear EER and EEW if they are set. This bit will also be cleared if ECSELx value is changed.
[30]	E1EAD	ECC 1-bit error event and failing address detected Refer to ECSELx register for ECC error event capture rules. This bit is set to "1" by hardware, which indicates the ECC 1-bit error event is detected and its associated failing address, the data and the ECC code are captured to EFADR, ERDAT and ERCOD registers respectively. Note: Write "1" to clear this bit, and at the same time it will clear EER and EEW if they are set. This bit will also be cleared if ECSELx value is changed.
29	EER	ECC error event in read

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		This bit is working together with E1EAD and E2EAD. This bit is set to "1" by hardware if the captured Error event is in Read Access. Note: Write "1" to clear this bit, and at the same time it will clear E1EAD and E2EAD if they are set. This bit will also be cleared if ECSELx value is changed.
28	EEW	ECC error event in partial write This bit is working together with E1EAD and E2EAD. This bit is set to "1" by hardware if the captured Error event is in Partial Write Access. Note: Write "1" to clear this bit, and at the same time it will clear E1EAD and E2EAD if they are set. This bit will also be cleared if ECSELx value is changed.
27:0	EFADR	ECC failing event address This register is to store ECC failing event address. It is read only. It is only valid when either E1EAD or E2EAD is set to "1". This register will be locked until both E1EAD and E2EAD are clear. Note that this address is local to respsective memory, not the bus address. For AXI SRAM2(64bit) : Fail Addr={ EFADR [27:0],3'h0}+ AXI_SRAM2_base(0x24020000) For AHB SRAM3(32bit) : Fail Addr={ EFADR [27:0],2'h0}+ AHB_SRAM2_base(0x300A0000)

2.4.4.7 ECCMON Mermory x ECC Fail Event Data low Register (ECCMON_FEDATLx, x=1~n)

Address Offset: (5x+1) *4, x=1~n

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERDATL															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERDATL															
r															

Bit Field	Field Name	Description
31:0	ERDATL	ECC error data low This data register is to store t lower 32-bit error data when the ECC error event is captured. The value is only valid when either E1EAD or E2EAD is set to "1". This register will be locked until both E1EAD and E2EAD are clear.

2.4.4.8 ECCMON Mermory x ECC Fail Event Data High Register (ECCMON_FEDATHx, x=1~n)

Address Offset: (5x+2) *4, x=1~n

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERDATH															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERDATH															
r															

Bit Field	Field Name	Description
31:0	ERDATH	ECC error data high This data register is to store the higher 32-bit error data when the ECC error event is captured. The value is only valid when either E1EAD or E2EAD is set to "1". This register will be locked until both E1EAD and E2EAD are clear.

2.4.4.9 ECCMON Mermory x ECC Fail Event ECC Code Register (ECCMON_FECODx, x=1~n)

Address Offset: (5x+3) *4, x=1~n

Reset value: 0x0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERCOD															
r															

Bit Field	Field Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	ERCOD	ECC error code This data register is to store the ECC code when the ECC error event is captured. The value is only valid when either E1EAD or E2EAD is set to "1". Note: This register will be locked until both E1EAD and E2EAD are clear. For AXI ROM , AXI SRAM1and ITCM SRAM, 8 bits are vaild For AXI SRAM 2 and 3, 16 bits are vaild and ECC code is arranged as follows: {1'b0, upper_32bit_ecc,1'b0,lower_32bit_ecc} For other memories, 7 bits are vaild

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2.5 Tightly Coupled Memory Controller (TCMC)

2.5.1 Introduction

Tightly Coupled Memory (TCM) is special ARM caching unit design for reducing unpredictability of traditional cache. Traditional cache can provide data or instruction fast when request package hits on cache but needs more reading time when it misses in cache. This makes the access time to certain instruction or data become unpredictable, mostly depending on replacement policy and cache size. TCM is used to solve this problem and making access to certain information more predictable and accelerate specific application. User can put instructions or data for specific function inside TCM and those instruction/data will never be replaced. ARM suggest user to put instruction/data that rely on time-predictability in TCM, e.g. instruction handling, camera image process program and automotive response instruction.

ARM Cortex-CM7® (CM7) provides two types of TCM (ITCM and DTCM) and three TCM interface (ITCM, D0TCM, D1TCM). Instruction TCM (ITCM) and Data TCM (DTCM) are dedicated for storing different types of data.

When using external TCM, user can just connect SRAM to TCM interface and configure CM7 core accordingly to enable TCM feature of CM7. It needs to have the instruction and data loaded into TCM SRAM before CM7 read them for execution.

In this chip, we are using external TCM and this TCM controller is bridging between CM7 TCM interface and SRAM banks. There are 1024KB of SRAM that can be configure as ITCM, DTCM in granularity of 128 KB, rest of the memory space will allocate to two AXI SRAM2/3. TCM controller also supports ECC function for data protection. SRAM banks that serve as TCM will run at CM7 CPU clock, the rest of SRAM bank (if any) will be used as normal AXI SRAM and running under AXI clock.

2.5.2 Main Features

The main features supported by TCMC are shown below:

- Up to 1024KB TCM SRAM
- Interfaces: 64-bit I-TCM, 2x32-bit D-TCM, 64-bit AXI
- TCM can be configured as ITCM, DTCM or AXI SRAM2/3

  The size can be configured by the user in granularity of 128 KB.
- The maximum access speed is equal to CPU run clock, up to 600MHz
- Support Byte/Halfword/Word read and write
- Support ECC (Error Correction Code)

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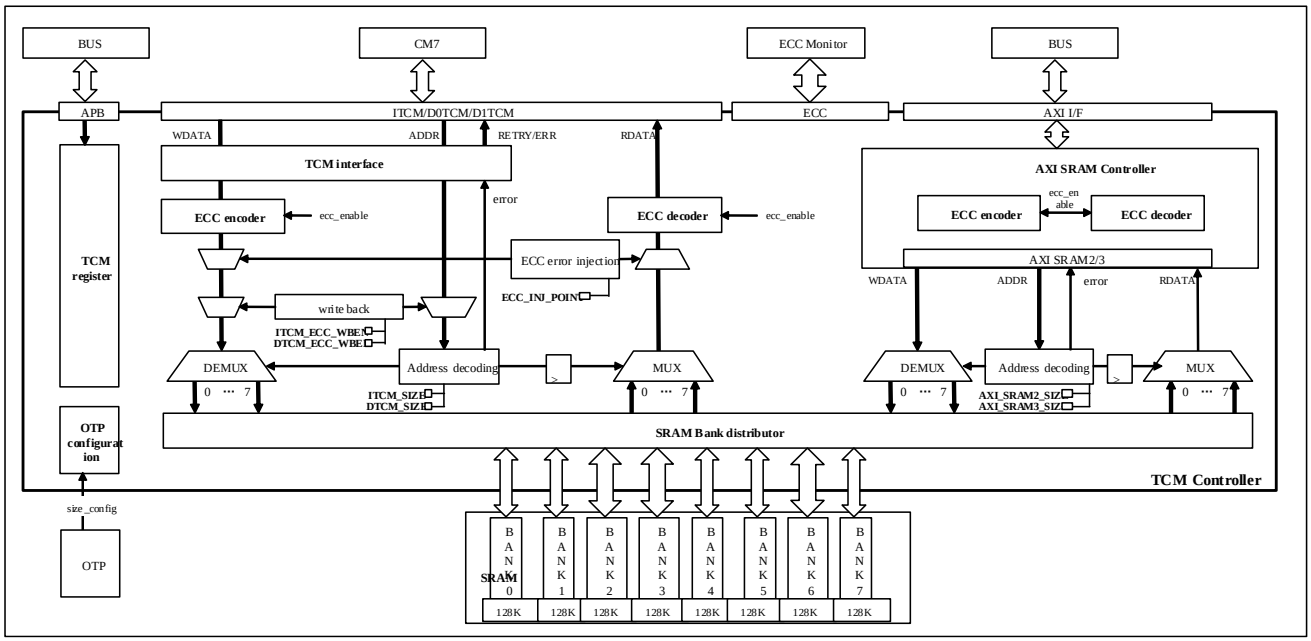
2.5.3 Block Diagram

The block diagram of TCM controller is shown below:

Figure 2-4 TCM Controller Block Diagram



TCM register is used to configure the TCM size (AXI SRAM2/3 size will be auto calculated after TCM size defined). At system boot up time, the size can be configured by **OTP configuration**. User can also configure ECC-related functions (Write back, Error injection) by TCM register via APB interface.

ITCM/D0TCM/D1TCM interfaces are used for TCM access. They are connected directly to CM7 and therefore, CM7 can access the data from TCM quickly. TCM controller implements **ECC encoder/decoder** to support ECC function. ECC configuration is performed via ECC Monitor.

Beside TCM controller, it instances a special **AXI SRAM controller** to manage the access to AXI SRAM2 and SRAM3. This controller also support ECC function with embedded ECC encoder/decoder. See the chapter of ECC Monitor for more detail of ECC.

After configuring the TCM size, each ITCM/D0TCM/D1TCM/AXI SRAM2/AXI SRAM3 will be assigned to specific and unique SRAM banks for accessing. It is performed by **SRAM bank distributor** logic block. See Table 2-11 for detail of this assignment.

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2.5.4 Function Description

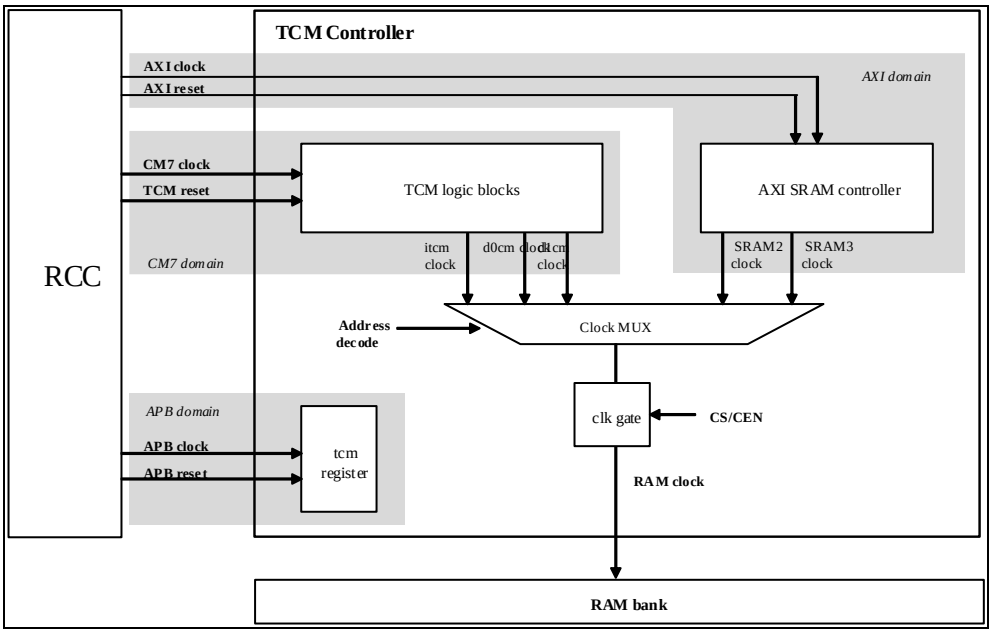
2.5.5 Clock and Reset

There are 3 clock domains:

1. CM7 domain: It is used for TCM access. Maximum clock frequency is 600Mhz.
2. AXI Bus domain: It is used for AXI SRAM2/3 access. Maximum clock frequency is 300Mhz.
3. APB Bus domain: It is used for APB register configuration. Maximum clock frequency is 150Mhz.

Figure 2-5 shows the clock/reset domain structure of TCM controller.

Figure 2-5 Clock and reset domains



2.5.6 Size configuration

ITCM and DTCM size can be changed by setting different value in TCM register. There are 1024 KB SRAM space available for allocation. For DTCM, D0TCM has the same size with D1TCM that is half of DTCM size. Thus, if DTCM is 128 KB, D0TCM and D1TCM will occupy 64 KB for each. The sum of ITCM and DTCM size should not exceed 1024 KB.

When system boot up, TCM controller will load default setting value from user configuration (from OTP). If user wants to switch to another configuration, first needs to make sure there are no access from CM7 and AXI bus. As CM7 might issue speculative access, user must disable TCM before TCM reconfiguration. Then user can write new size configuration to TCM register through APB bus. Size mapping is shown in Table 2-11 with step of 128 KB. TCM sets CSA bit in TCMC_CTR register if sum of ITCM and DTCM size is less than or equal to 1024 KB. Otherwise, CSA in TCMC_CTR register will be keep L. User needs to check size status each time after configure new size or system boot up. After confirm the size configuration is correct, user can start DMA operation to move instructions or data into TCM. Any operation issued to TCM and AXI SRAM2/3 when CSA=L will be illegal and

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unpredictable.

After configuring ITCM and DTCM size according to requirement, TCM controller calculates AXI SRAM 2/3 size using formula below:

- (ITCM size + DTCM size) <= 512KB:
  - AXI SRAM 3 size = 512KB – (ITCM size + DTCM size)
  - AXI SRAM 2 size = 512KB
- (ITCM size + DTCM size) > 512KB:
  - AXI SRAM 3 size = 0 KB
  - AXI SRAM 2 size = 1024KB – (ITCM size + DTCM size)

The SRAM banks are distributed as following order: ITCM → DTCM → AXI SRAM 3 → AXI SRAM 2.

NOTE: This order is different from the system memory map's order.

Size configuration is shown detail in Table 2-11.

Table 2-11 TCM size configuration mapping

ITCMS bit setting	DTCMS bit setting	ITCM Size	DTCM Size	AXI SRAM3 Size	AXI SRAM2 Size	SRAM Bank distribution							
						bank0	bank1	bank2	bank3	bank4	bank5	bank6	bank7
0000	0000	0 KB	0 KB	512 KB	512 KB	R3	R3	R3	R3	R2	R2	R2	R2
0001	0000	128 KB	0 KB	384 KB	512 KB	I	R3	R3	R3	R2	R2	R2	R2
0010	0000	256 KB	0 KB	256 KB	512 KB	I	I	R3	R3	R2	R2	R2	R2
0011	0000	384 KB	0 KB	128 KB	512 KB	I	I	I	R3	R2	R2	R2	R2
0100	0000	512 KB	0 KB	0 KB	512 KB	I	I	I	I	R2	R2	R2	R2
0101	0000	640 KB	0 KB	0 KB	384 KB	I	I	I	I	I	R2	R2	R2
0110	0000	768 KB	0 KB	0 KB	256 KB	I	I	I	I	I	I	R2	R2
0111	0000	896 KB	0 KB	0 KB	128 KB	I	I	I	I	I	I	I	R2
1000	0000	1024 KB	0 KB	0 KB	0 KB	I	I	I	I	I	I	I	I
0000	0001	0 KB	128 KB	384 KB	512 KB	D	R3	R3	R3	R2	R2	R2	R2
0001	0001	128 KB	128 KB	256 KB	512 KB	I	D	R3	R3	R2	R2	R2	R2
0010	0001	256 KB	128 KB	128 KB	512 KB	I	I	D	R3	R2	R2	R2	R2
0011	0001	384 KB	128 KB	0 KB	512 KB	I	I	I	D	R2	R2	R2	R2
0100	0001	512 KB	128 KB	0 KB	384 KB	I	I	I	I	D	R2	R2	R2

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0101	0001	640 KB	128 KB	0 KB	256 KB	I	I	I	I	I	D	R2	R2
0110	0001	768 KB	128 KB	0 KB	128 KB	I	I	I	I	I	I	D	R2
0111	0001	896 KB	128 KB	0 KB	0 KB	I	I	I	I	I	I	I	D
0000	0010	0 KB	256 KB	256 KB	512 KB	D	D	R3	R3	R2	R2	R2	R2
0001	0010	128 KB	256 KB	128 KB	512 KB	I	D	D	R3	R2	R2	R2	R2
0010	0010	256 KB	256 KB	0 KB	512 KB	I	I	D	D	R2	R2	R2	R2
0011	0010	384 KB	256 KB	0 KB	384 KB	I	I	I	D	D	R2	R2	R2
0100	0010	512 KB	256 KB	0 KB	256 KB	I	I	I	I	D	D	R2	R2
0101	0010	640 KB	256 KB	0 KB	128 KB	I	I	I	I	I	D	D	R2
0110	0010	768 KB	256 KB	0 KB	0 KB	I	I	I	I	I	I	D	D
0000	0011	0 KB	384 KB	128 KB	512 KB	D	D	D	R3	R2	R2	R2	R2
0001	0011	128 KB	384 KB	0 KB	512 KB	I	D	D	D	R2	R2	R2	R2
0010	0011	256 KB	384 KB	0 KB	384 KB	I	I	D	D	D	R2	R2	R2
0011	0011	384 KB	384 KB	0 KB	256 KB	I	I	I	D	D	D	R2	R2
0100	0011	512 KB	384 KB	0 KB	128 KB	I	I	I	I	D	D	D	R2
0101	0011	640 KB	384 KB	0 KB	0 KB	I	I	I	I	I	D	D	D
0000	0100	0 KB	512 KB	0 KB	512 KB	D	D	D	D	R2	R2	R2	R2
0001	0100	128 KB	512 KB	0 KB	384 KB	I	D	D	D	D	R2	R2	R2
0010	0100	256 KB	512 KB	0 KB	256 KB	I	I	D	D	D	D	R2	R2
0011	0100	384 KB	512 KB	0 KB	128 KB	I	I	I	D	D	D	D	R2
0100	0100	512 KB	512 KB	0 KB	0 KB	I	I	I	I	D	D	D	D
0000	0101	0 KB	640 KB	0 KB	384 KB	D	D	D	D	D	R2	R2	R2
0001	0101	128 KB	640 KB	0 KB	256 KB	I	D	D	D	D	D	R2	R2
0010	0101	256 KB	640 KB	0 KB	128 KB	I	I	D	D	D	D	D	R2
0011	0101	384 KB	640 KB	0 KB	0 KB	I	I	I	D	D	D	D	D
0000	0110	0 KB	768 KB	0 KB	256 KB	D	D	D	D	D	D	R2	R2
0001	0110	128 KB	768 KB	0 KB	128 KB	I	D	D	D	D	D	D	R2
0010	0110	256 KB	768 KB	0 KB	0 KB	I	I	D	D	D	D	D	D
0000	0111	0 KB	896 KB	0 KB	128 KB	D	D	D	D	D	D	D	R2
0001	0111	128 KB	896 KB	0 KB	0 KB	I	D	D	D	D	D	D	D
0000	1000	0 KB	1024 KB	0 KB	0 KB	D	D	D	D	D	D	D	D

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I – ITCM, D – DTCM, R2 – AXI SRAM 2, R3 – AXI SRAM 3

See chapter 2.5.9 Programming Guide for more detail of size configuration flow.

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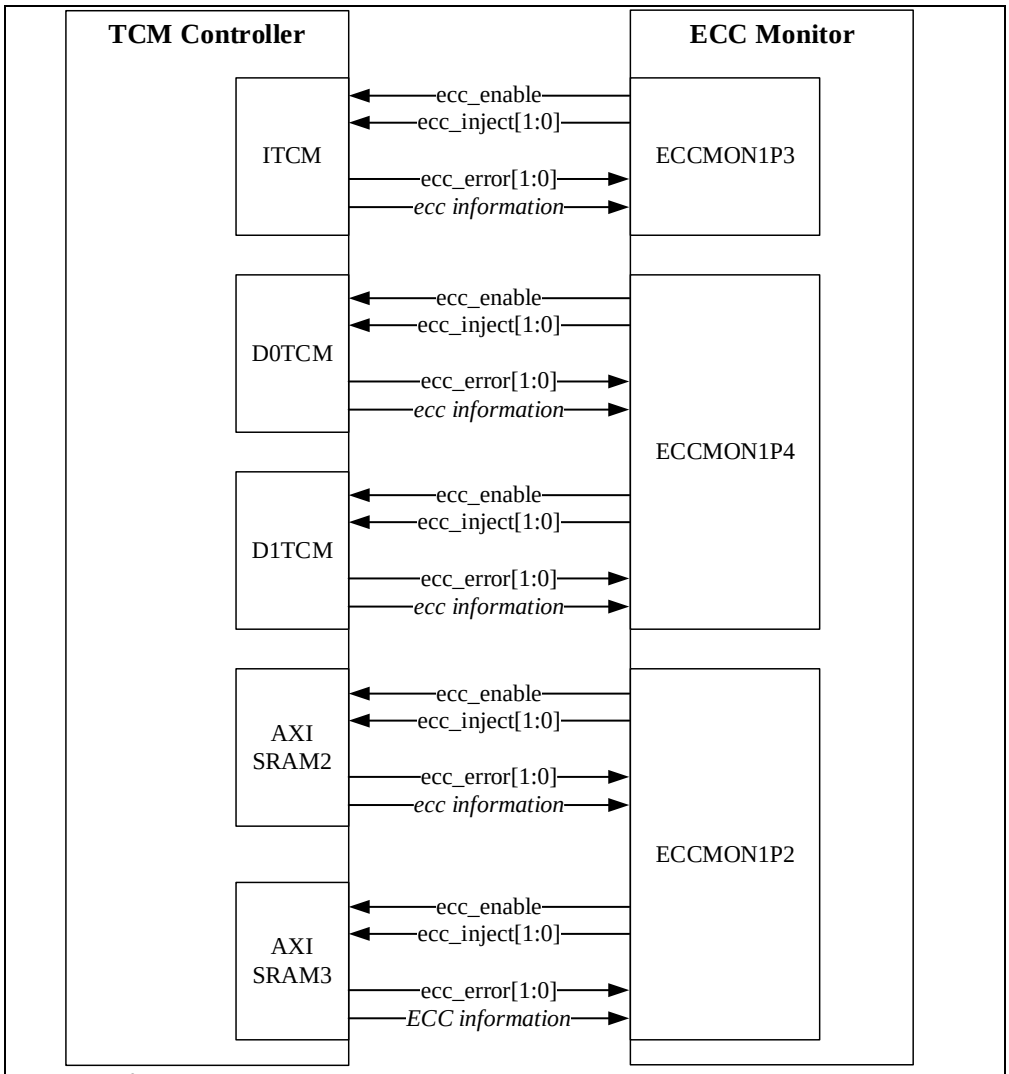
2.5.7 ECC function

TCM controller supports ECC (Error correction code) for the TCM or AXI SRAM2/3 access. This function is enabled by ECC Monitor and provides the ECC information to that module. User can also inject the error bit for ECC test via ECC Monitor. Figure 2-6 shows the connection between TCM Controller and ECC Monitor.

Figure 2-6 TCM Controller and ECC Monitor connection



TCM controller is using ECC encoder and decoder that are pure combination logic capable of single-bit error correction and dual-bit error detection (SECDED) with error injection function. ECC function enable signals are from ECC monitor (ECCMON). If ECC function of corresponding interface is enabled (for TCM only), program will be only conducted in whole word base (all byte-lanes are valid). User needs to enable RMW feature of CM7 when ECC is enabled. When there are ECC error, TCM controller outputs ECC error types, address, data and corresponding ECC code to ECC monitor. It also returns the RETRY signal to CM7 so that CM7 can be aware of the wrong read data and decide to discard that data or attempt to issue another read. ITCM, D0TCM/D1TCM and AXI SRAM2/3 have dedicated ECC encode/decode logic.

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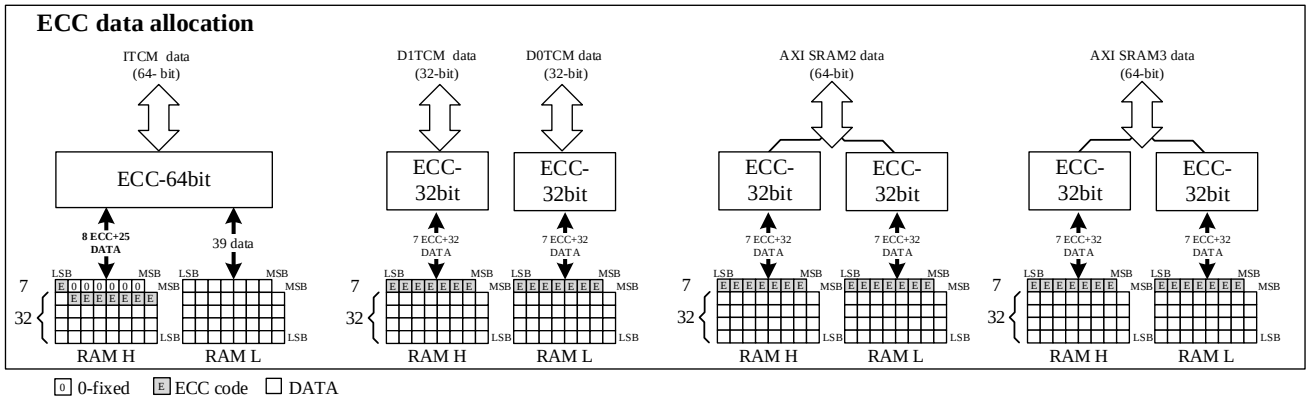
AXI interfaces are 64 bits bus, but they are stored in form of two 32-bit data inside SRAM. Each part of 32-bit supports 7 bits ECC code. AXI ECC code is calculated by AXI interface and stored in 2*(7 ECC+32 Data) bits format in SRAM. D0TCM and D1TCM data are stored in 32-bit with 7-bit ECC for each. However, ITCM is also 64 bits data, but it was encoded with only 8 bits ECC code. The data structure of ECC encoded data is shown in Figure 2-7.

Figure 2-7 ECC data allocation



When ECC is disabled (ECCMON_CTR1.ECCEN=0), ECC part of SRAM will not be touched, user cannot access this area. When ECC function is enabled (ECCMON_CTR1.ECCEN=1), it needs to reprogram data before reading data, if not, reading old data without ECC protect might either get wrong data or trigger unexpected ECC error.

NOTE-1: When ECC function is enabled, TCM controller always treats the data as whole word (all byte-lanes are valid) regardless of the data strobe information from CM7 access.

NOTE-2: This controller does not support ECC with 3 or more error bit. If this scenario occurs, the data may be unpredictable.

See chapter 2.5.9 Programming Guide for more detail of size configuration flow.

2.5.7.1 ECC write back

TCM controller issues the RETRY signal once whenever ECC error detected. This will make data provided to CM7 invalid and not causing any error due to wrong data. After CM7 receives RETRY signal, CM7 might come and fetch the data sometime in the future or not. In the case of 1-bit error, it can be corrected and hence, in order to make sure next time CM7 will get the correct data, TCM controller will write back ECC corrected data to SRAM.

By default this function is enabled, but it can be configured to disable it by the bits DTCMEWEN, ITCMEWEN of TCMC_CTR register.

NOTE-1: If there is another write access with same address issued at the time of write-back, the write-back is discarded. This guarantees the data of that write is not lost.

NOTE-2: This function is not applied for case of 2-bit error detection.

NOTE-3: This function is not applied for the access of AXI SRAM2/3.

2.5.7.2 ECC error injection

TCM controller supports error injection function when ECC is enabled (ECCMON_CTR1.ECCEN=1). This function

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is performed by 2-bit ECC error injection signal (ECCMON_EINJ.ERICTRn[1:0]) that is configured from ECC Monitor. Each bit will invert one corresponding data bit, which results the data seems be corrupted and ECC error (ECCMON_INTFS.EnDCIF[1:0]) is reported to ECC Monitor. Table 2-12 shows the position of data bit which is inverted by that ECC error injection signal.

Table 2-12 TCM ECC error injection

Interface	ECC error injection signal value	Data	ECC error type
ITCM (64-bit)	00	Unchanged	No error
	01	Bit [5] is inverted, Others: Unchanged	1-bit error detected
	10	Bit [20] is inverted, Others: Unchanged	1-bit error detected
	11	Bit [5] and bit [20] are inverted, Others: Unchanged	2-bit error detected
D0TCM (32-bit)	00	Unchanged	No error
	01	Bit [1] is inverted, Others: Unchanged	1-bit error detected
	10	Bit [18] is inverted, Others: Unchanged	1-bit error detected
	11	Bit [1] and bit [18] are inverted, Others: Unchanged	2-bit error detected
D1TCM (32-bit)	00	Unchanged	No error
	01	Bit [3] is inverted, Others: Unchanged	1-bit error detected
	10	Bit [6] is inverted, Others: Unchanged	1-bit error detected
	11	Bit [3] and bit [6] are inverted, Others: Unchanged	2-bit error detected
AXI SRAM2 (2 x 32-bit)	00	Unchanged	No error
	01	Bits [6] (of both lower 32-bit and higher 32-bit part) are inverted, Others: Unchanged	1-bit error detected
	10	Bits [25] (of both lower 32-bit and higher 32-bit part) are inverted, Others: Unchanged	1-bit error detected
	11	Bit [6] and bit [25] (of both lower 32-bit and higher 32-bit part) are inverted, Others: Unchanged	2-bit error detected
AXI SRAM3 (2 x 32-bit)	00	Unchanged	No error
	01	Bits [6] (of both lower 32-bit and higher 32-bit part) are inverted, Others: Unchanged	1-bit error detected
	10	Bits [25] (of both lower 32-bit and higher 32-bit part) are inverted, Others: Unchanged	1-bit error detected
	11	Bit [6] and bit [25] (of both lower 32-bit and higher 32-bit part) are inverted, Others: Unchanged	2-bit error detected

For TCM access, the ECC error bit can be injected into both write data path or read data path, which can be configured by ECCINJP bit of TCMC_CTR register:

- ECCINJP = 0 (default): injected on read data path. The inversion logic is performed before the ECC Decoder (see Figure 2-4). This mode, the data on SRAM are always correct data (not corrupted), therefore, the write-back data is performed in case of 1-bit error correction becomes meaningless. User can use this mode if only test the ECC error detection without write back function test.

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- ECCINJP = 1: injected on write data path. The inversion logic is performed after the ECC Encoder (see Figure 2-4) and therefore, the data on SRAM are wrong data (corrupted). In case of 1-bit error, the write back function can make the SRAM data correct again. User can use this mode to test ECC error detection with the write back function.

2.5.8 Interrupts

There is no interrupt signal of this controller. However, the following errors signal from this controller can be associated with an interrupt, which is defined by other modules (CM7, ECC Monitor):

1. TCM access error response
2. AXI SRAM 2,3 access error response
3. ECC error detection

2.5.9 Programming Guide

2.5.9.1 Size configuration flow

Configure TCM size during system boot up:

1. Prepare TCM size setting with OTP configuration.
2. After system boot up completed, check the bit CSA of TCMC_CTR register:
   2.1. If CSA = L: TCM size setting is illegal, invoke an error or interrupt to upper system and does not access TCM, or AXI SRAM2, 3 this time.
   2.2. If CSA = H: TCM size setting is valid. Re-check the size configuration by reading the bits DTCMS, ITCMS, ARAM2S, ARAM3S of TCMC_CTR register. If the sizes are correct, user can start to access TCM or AXI SRAM2, 3.

Configure TCM size via APB bus (for NATIONS Secure BOOTROM only):

1. Make sure there is no remain access to TCM and AXI SRAM2,3.
2. Configure TCM size by setting the bit DTCMS, ITCMS of TCMC_CTR register.
3. Check the bit CSA of TCMC_CTR register.
   3.1. If CSA = L: TCM size setting is illegal, invoke an error or interrupt to upper system and does not access TCM, or AXI SRAM2, 3 this time. Re-try from step 2.
   3.2. If CSA = H: TCM size setting is valid. Re-check the size configuration by reading the bits DTCMS, ITCMS, ARAM2S, ARAM3S of TCMC_CTR register. If the sizes are correct, user can start to access TCM or AXI SRAM2, 3.

NOTE: Only Secure BOOTROM can configure TCM size via APB bus. Users can only program TCM_SZ_CFG_PRG register in MMU and call NATIONS secure BOOTROM to proceed with security operations before programming TCMC_CTR. Refer to security management's chapter for more information.

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2.5.9.2 ECC injection test flow

ITCM 1-bit error injection without write-back function test:

1. Configure ECC Monitor to enable ECC: ECCMON_CTR1.ECCEN = 1, ECCMON_EINJ.ERICTRn = 01 or 10.
2. Set ECCINJP = 0 *(read data path injection)*
3. Set ITCMEWEN = 0 or 1 (*any*)
4. Issue a write access to ITCM *(address A)*
5. Issue a read access to ITCM *(address A)*. Check if read data is wrong (*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor

ITCM 1-bit error injection with write-back function test:

1. Configure ECC Monitor to enable ECC: ECCMON_CTR1.ECCEN = 1, ECCMON_EINJ.ERICTRn = 01 or 10.
2. Set ECCINJP = 1 *(write data path injection)*
3. Issue a write access to ITCM *(address A)*
4. Set ITCMEWEN = 0 *(disable write back function first)*
5. Issue a read access to ITCM *(address A)*. Check if read data is wrong (*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor
6. Issue the read access to ITCM *(address A)* again. Check if read data is still wrong (*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor
7. Set ITCMEWEN = 1 (*enable write back function)*
8. Issue a read access to ITCM *(address A)*. Check if read data is wrong (*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor
9. Issue the read access to ITCM *(address A)* again. Check if read data is correct and no ECC error.

ITCM 2-bit error injection test:

1. Configure ECC Monitor to enable ECC: ECCMON_CTR1.ECCEN = 1, ECCMON_EINJ.ERICTRn = 11.
2. Set ECCINJP = 0 or 1 (*any*)
3. Set ITCMEWEN = 0 or 1 (*any*)
4. Issue a write access to ITCM *(address A)*
5. Issue a read access to ITCM *(address A)*. Check if read data is wrong (*2-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor
6. Issue the read access to ITCM *(address A)* again. Check if read data is still wrong(*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor

Above flows are similar for D0TCM, D1TCM ECC error injection test with setting DTCMEWEN instead.

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AXI SRAM2/3 with 1-bit error injection test:

1. Configure ECC Monitor to enable ECC: ECCMON_CTR1.ECCEN = 1, ECCMON_EINJ.ERICTRn = 01 or 10.
2. Issue a write access to AXI SRAM2 or 3*(address A)*
3. Issue a read access to AXI SRAM2 or 3 *(address A).* Check if read data is wrong (*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor
4. Issue the read access to AXI SRAM2 or 3 *(address A)* again. Check if read data is still wrong (*1-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor.

AXI SRAM2/3 with 2-bit error injection test:

1. Configure ECC Monitor to enable ECC: ECCMON_CTR1.ECCEN = 1, ECCMON_EINJ.ERICTRn = 11.
2. Issue a write access to AXI SRAM2 or 3*(address A)*
3. Issue a read access to AXI SRAM2 or 3 *(address A).* Check if read data is wrong (*2-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor
4. Issue the read access to AXI SRAM2 or 3 *(address A)* again. Check if read data is still wrong (*2-bit error, see* Table 2-12) and ECC error is invoked to ECC Monitor.

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2.5.10 Registers

This controller has one register (TCMC_CTR) as described below:

2.5.10.1 TCMC control register (TCMC_CTR)

Address offset: 0x00

Reset value: 0x44E0E000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ARAM3S				ARAM2S				DTCMEWEN	Reserved			DTCMS			
ro				ro				ro				ro			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ITCMEWEN	Reserved			ITCMS				Reserved		CSA	Reserved			ECCINJP	Reserved
ro				ro						ro				ro	

Bits	Name	Description
31:28	ARAM3S	AXI SRAM 3 size display. Once ITCM and DTCM size are set, SRAM size will be updated after 1 APB clock cycle. Size Mapping is shown as follow (step of 128 KB): 0000: 0 KB 0001: 128 KB 0010: 256 KB …… 0111: 896 KB 1000: 1024 KB Other than above: Invalid
27:24	ARAM2S	AXI SRAM 2 size display. Once ITCM and DTCM size are set, SRAM size will be updated after 1 APB clock cycle. Size Mapping is shown as follow (step of 128 KB): 0000: 0 KB 0001: 128 KB 0010: 256 KB …… 0111: 896 KB 1000: 1024 KB Other than above: Invalid
23	DTCMEWEN	DTCM ECC write-back enable 0: Write-back disable 1: Write-back enable This bit is used for 1-bit ECC detection on the access to D0TCM or D1TCM.
22:20	Reserved	Reserved,the reset value must be maintained

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19:16	DTCMS	DTCM Size setting. Size Mapping is shown as follow (step of 128 KB): 0000: 0 KB 0001: 128 KB 0010: 256 KB …… 0111: 896 KB 1000: 1024 KB Other than above: Invalid
15	ITCMEWEN	ITCM ECC write-back enable 0: Write-back disable 1: Write-back enable This bit is used for 1-bit ECC detection on the access to ITCM.
14:12	Reserved	Reserved,the reset value must be maintained
11:8	ITCMS	ITCM Size setting. Size Mapping is shown as follow (step of 128 KB): 0000: 0 KB 0001: 128 KB 0010: 256 KB …… 0111: 896 KB 1000: 1024 KB Other than above: Invalid
7:6	Reserved	Reserved,the reset value must be maintained
5	CSA	Configurable size accepted Indication of size configuration has been accepted by TCM controller. This bit is update by hardware. After SMU flow done or configuring new size, user can read this register to confirm that the size configuration is correct and accepted by TCM controller. 0: configuration is incorrect and not accepted by TCM yet. 1: configuration is correct and accepted by TCM controller. Any operation issued to TCM and SRAM2/3 when CSA=L will be illegal and unpredictable.
4:2	Reserved	Reserved,the reset value must be maintained
1	ECCINJP	ECC injection position setting for TCM access 0: ECC is injected on read data path, before ECC Decoder 1: ECC is injected on write data path, after ECC Encoder When injected on read data path, it does not corrupt the write data to memory data, but write-back function cannot be tested. When injected on write data path, it corrupts the write data to memory data and write-back function can be tested.
0	Reserved	Reserved,the reset value must be maintained

NOTE: This register can be only configured by NATIONS SECURE BOOTROM.

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3 Power control (PWR)

3.1 Introduction

The Power Control section defines the supply structure of the chip, low power techniques implementation, power modes transition control and clock control. The power supply structure, PWR hardware and software run in both CPUs work together to make performance of the chip with as close as possible to the power required.

The low power techniques implemented in the chip includes: Power gating, Voltage scaling, Clock gating, Clock frequency scaling, Low power modes of CPUs and peripherals: CPU sleep/deep sleep; SRAMs power gating; low power modes of DCDC, SRAM, OTP etc.

3.2 Main Features

The main features supported by PWR are shown below:

- Power supplies and supply domains
  - Core domains (VCORE)
  - VDD domain
  - Backup domain (VDDBK, VDDDBK)
  - Retention domain (VDDDRET)
  - Analog domain (VDDA)
- System supply voltage regulation
  - SMPS step-down converter(DCDC)
  - Main Low DropOut Regulator(LDO)
- Peripheral supply regulation
  - USB regulator
  - DSI regulator
  - PLL regulator
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor
  - AVD monitor
  - VBAT thresholds

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- Power management
  - VBAT battery charging
  - Operating modes
  - Voltage scaling control
  - Low-power modes

3.3 Block Diagram

The power supply network for the chip is depicted below.

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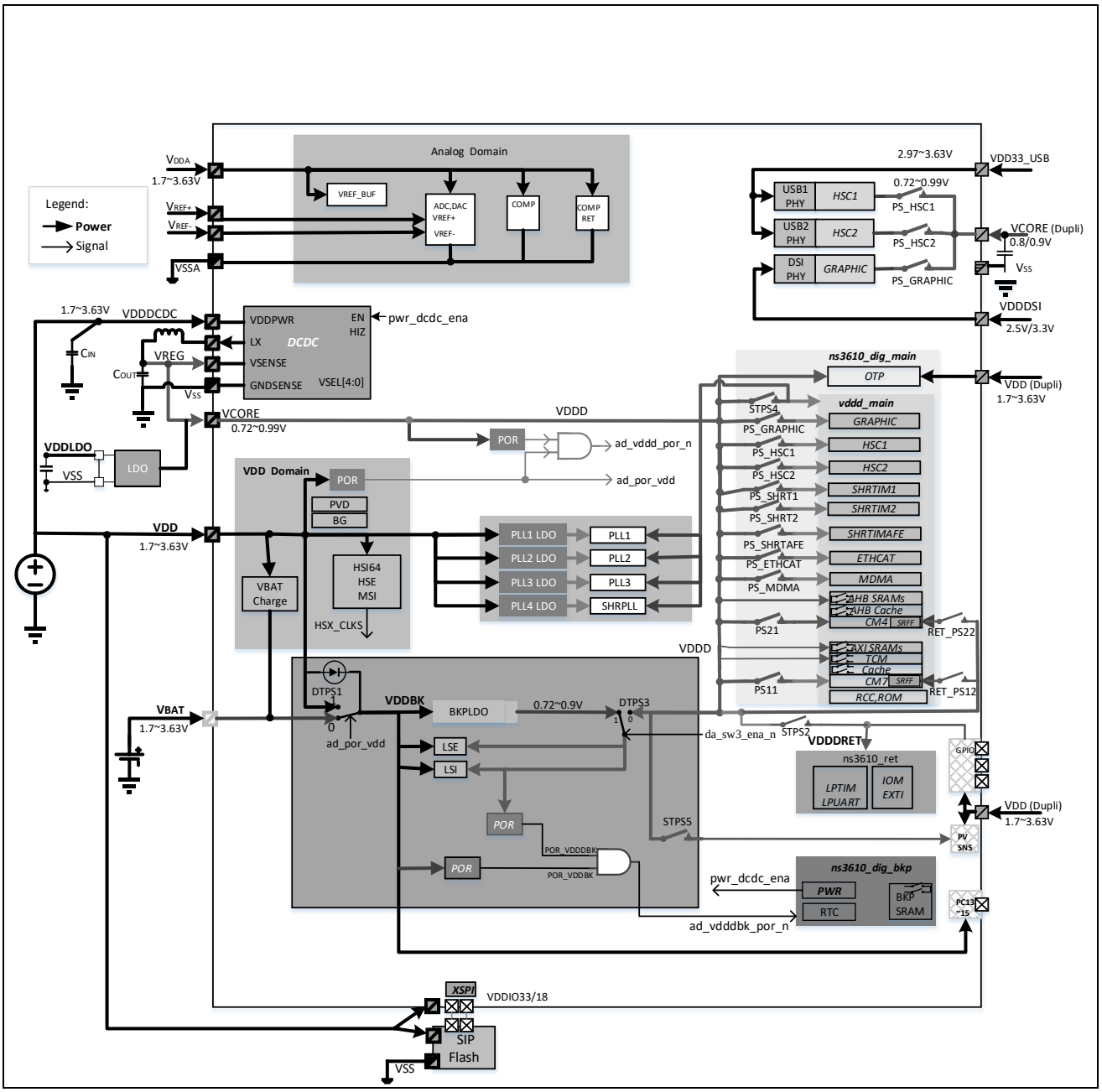
Figure 3-1 Chip supply structure



The power and ground pins at chip top are described in Table 3-1. The main supply pads for the chip are VDDDCDC, VDD and VDDA.

Table 3-1 Power and Ground at chip top

Name	direction	Voltage(V)	Description
VDD	Input	1.62~3.63V	Main I/O and V_{DD} domain supply input
VDDA	Input	1.62~3.63V	External analog power supply for analog peripherals
VREF+,VREF-	Input	3.3, 0	External reference voltage for ADCs and DAC
VBAT	Input	1.62~3.63V	Backup battery supply input

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VDDDCDC	Input	1.62~3.63V	DCDC supply input
VLXDCDC	Input	0.72~0.99	DCDC supply output
VFBDCDC	Input	0.72~0.99	DCDC feedback voltage sense
VSSDCDC	Input	0	DCDC ground
VCORE	Input/Onput	0.8/0.9	Digital core domain supply
VDD1P8	Input	1.8	1.8V SIP Flash Supply
VDD33USB	Input/Onput	3.3	USB regulator supply output
VSS	Input	0	Main ground
VDDDSI	Input	2.5/3.3	DSI PHY analog voltage input
VCAPDSI	Input	0.8/0.9	DSI PHY digital supply input

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3.4 Function Description

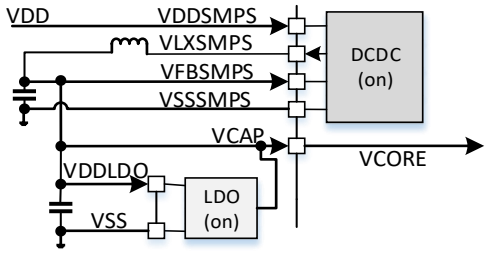
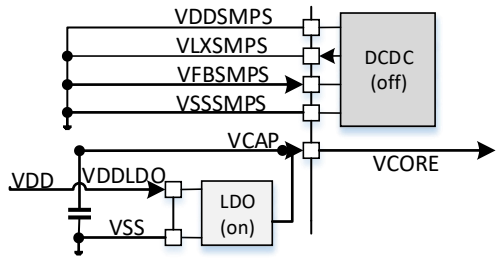
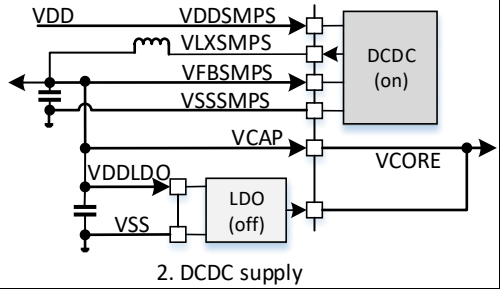
3.4.1 Digital main VCORE supply modes

The digital main supply, VCORE can be supplied from SIP LDO, embedded DCDC regulator or directly from an external supply.

There are four valid supply mechanism are supported for the chip as shown below.

Mode 0 is the default transitional mode only valid at chip power up. Software must configure the supply mode with PWR_SYSCTRL4 after boot.

Table 3-2 Chip VCORE supply modes

mode	MLDOEN	DCDCEN	DCDCFRCEN	VCORESRC	Connection diagram	description
0	1	1	0	0	 0*. Both LDO and DCDC supply	This is a transient power mode at VDDD power up, where both SMPS DCDC and LDO are enabled. After CM7 boot up, the supply mode should be configured to one of the valid supply configurations (1,2,3) below. **Note**: The external supply connection can be any valid supply mode 1,2,3. Here mode 2 used for illustration.
1	1	0	0	0	 1. LDO supply	Main LDO supply VCORE. DCDC is disabled. All DCDC pads are grounded.
2	0	1	0 OR 1	0	 2. DCDC supply	DCDC supply VCORE LDO is disabled. VDDLDO can be connected to DCDC output VFBSMPS or ground. When DCDC_FON =1, the DCDC will be kept on in low

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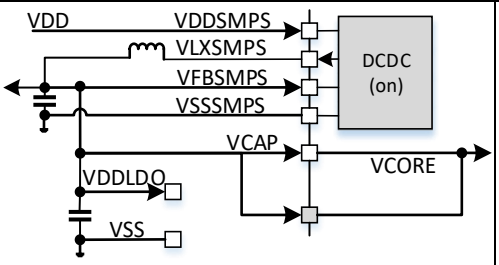
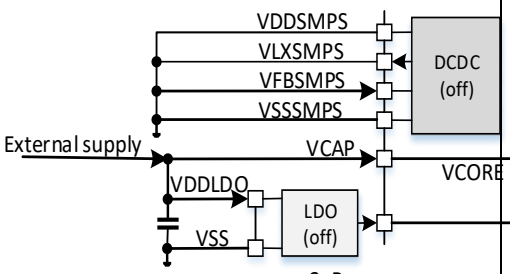
						power modes and output voltage same as Run mode setting.
2’	0	1	0 OR 1	0	 2'. DCDC supply	Same configuration as mode 2, DCDC supply VCORE, but **No LDO**. VDDLDO The pad for LDO output should be double-bounded with pin VCAP.
3	0	0	0	1	 3. Bypass	External supply supplies VCORE directly. Both DCDC and LDO are disabled.
All other combinations of supply are invalid.					If the software attempts to write invalid configurations other than modes 1, 2, or 3, the register bits for the mode configuration will remain locked in mode 0 until a system reset clears the lock.	

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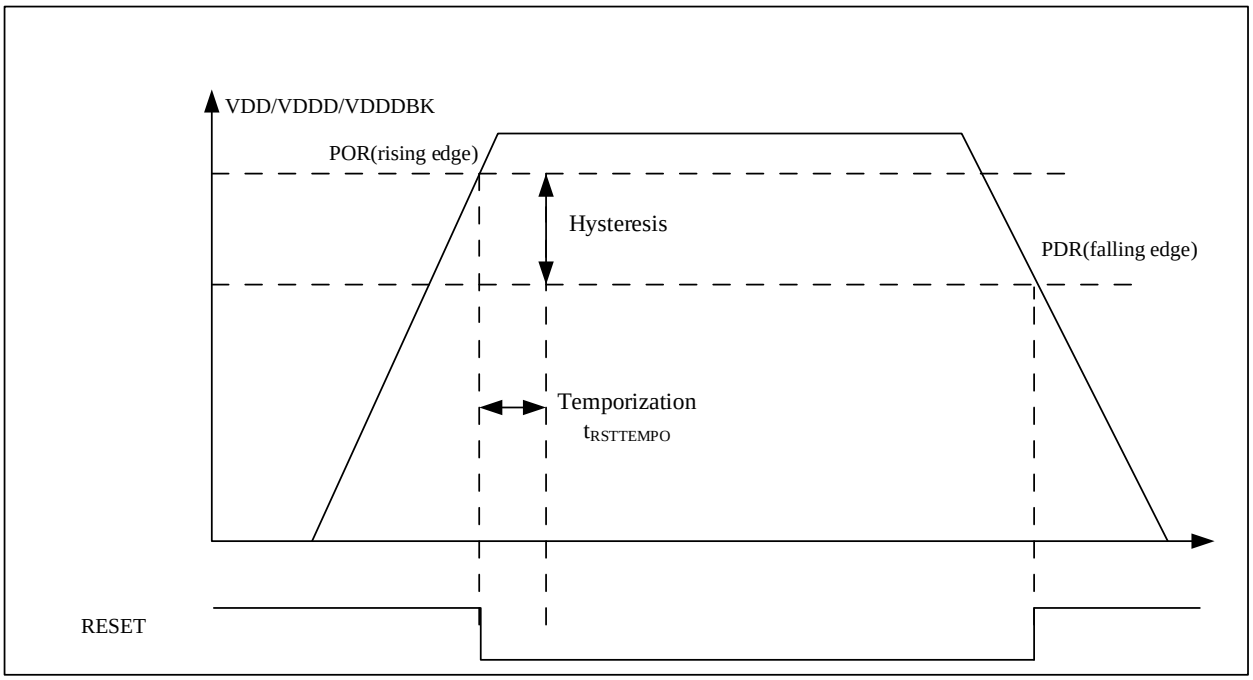
3.4.2 Power Supply Supervisor

3.4.2.1 Power on reset (POR) and power down reset (PDR)

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally in the chip. It can operate at a minimum voltage of 1.68V when the POR/PDR is used to monitor the VDD power supply. There is no need for an external reset circuit; the chip will remain in a reset state when VDD , VDDD or VDDDBK falls below the specified threshold (VPOR/PDR).

For detailed information on the switch power reset threshold, please refer to the Electrical Characteristics section of the relevant datasheet.

Figure 3-2 Power On Reset and Power Down Reset Waveform



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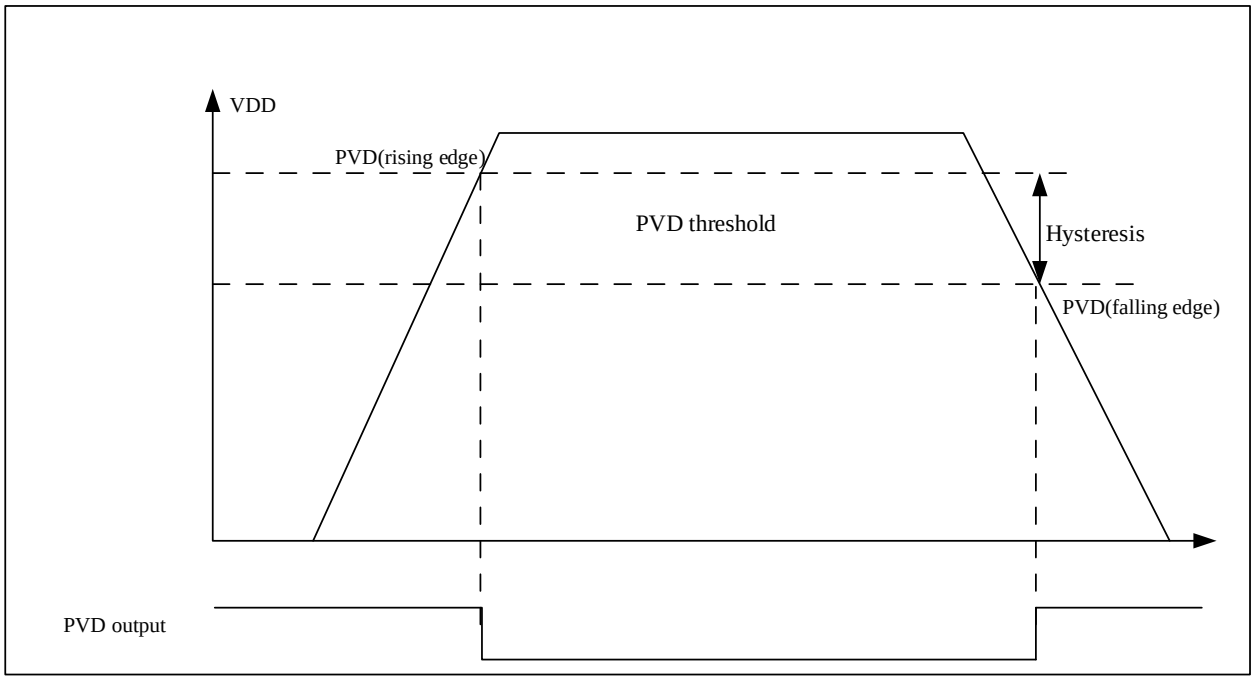
3.4.2.2 Programmable voltage detector (PVD)

The PVD can be used to monitor the VDD power supply by comparing it with the threshold set by the AFEC_CTRL.PRS[3:0] bits in the power control register. Enable the PVD by setting PWR_SYSCTRL1.PVDEN.

The PWR_SYSCTRLSTS.PVDO flag is used to indicate whether VDD is above/below the PVD voltage threshold. This event is internally connected to external interrupt line 16, and if the interrupt is enabled in the external interrupt register, an interrupt will be generated. Depending on the rising/falling edge trigger setting of external interrupt line 16, a PVD interrupt will occur when VDD falls below the PVD threshold or rises above it. For example, this feature can be used to perform emergency shutdown tasks.

Figure 3-3 PVD Threshold Waveform



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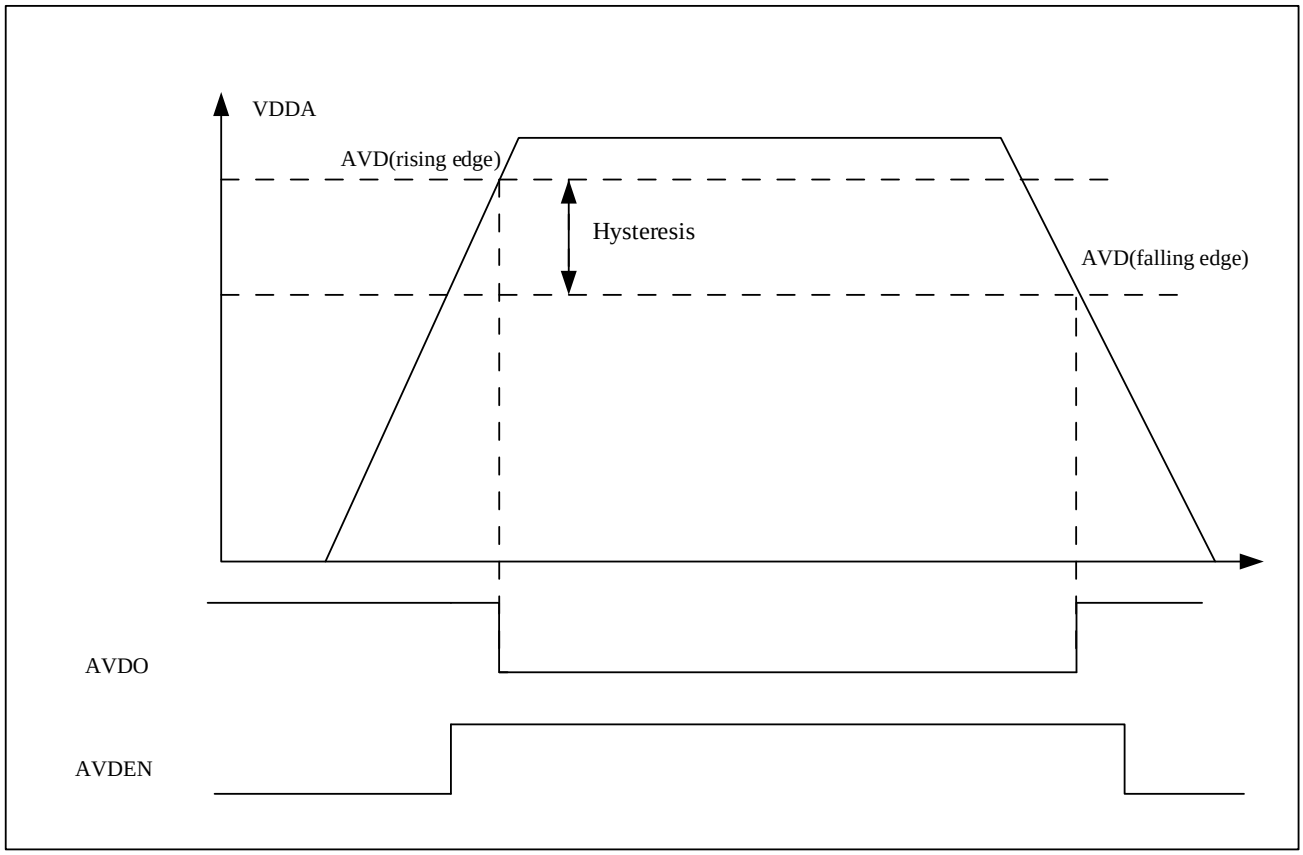
3.4.2.3 Analog voltage detector (AVD)

The AVD can be used to monitor the VDDA supply by comparing it to a threshold selected by the AFEC.ALS[3:0] bits in the AFEC control register.

The AVD is enabled by setting the PWR_SYSCTRL1.AVDEN bit. An PWR_SYSCTRLSTS.AVDO flag is available to indicate whether VDDA is higher or lower than the AVD threshold. This event is internally connected to the EXTI and can generate an interrupt if enabled through the EXTI registers. The AVDO interrupt can be generated when VDDA drops below the AVD threshold and/or when VDDA rises above the AVD threshold depending on EXTI rising/falling edge configuration. As an example the service routine could indicate when the VDDA supply drops below a minimum level.

Figure 3-4 AVD Threshold Waveform



Note: For thresholds and hysteresis values, please refer to the datasheets.

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3.4.2.4 Brown out reset(BOR)

During power-up, the Brown-Out Reset (BOR) will keep the device in a reset state until VDD reaches the specified VBOR threshold.

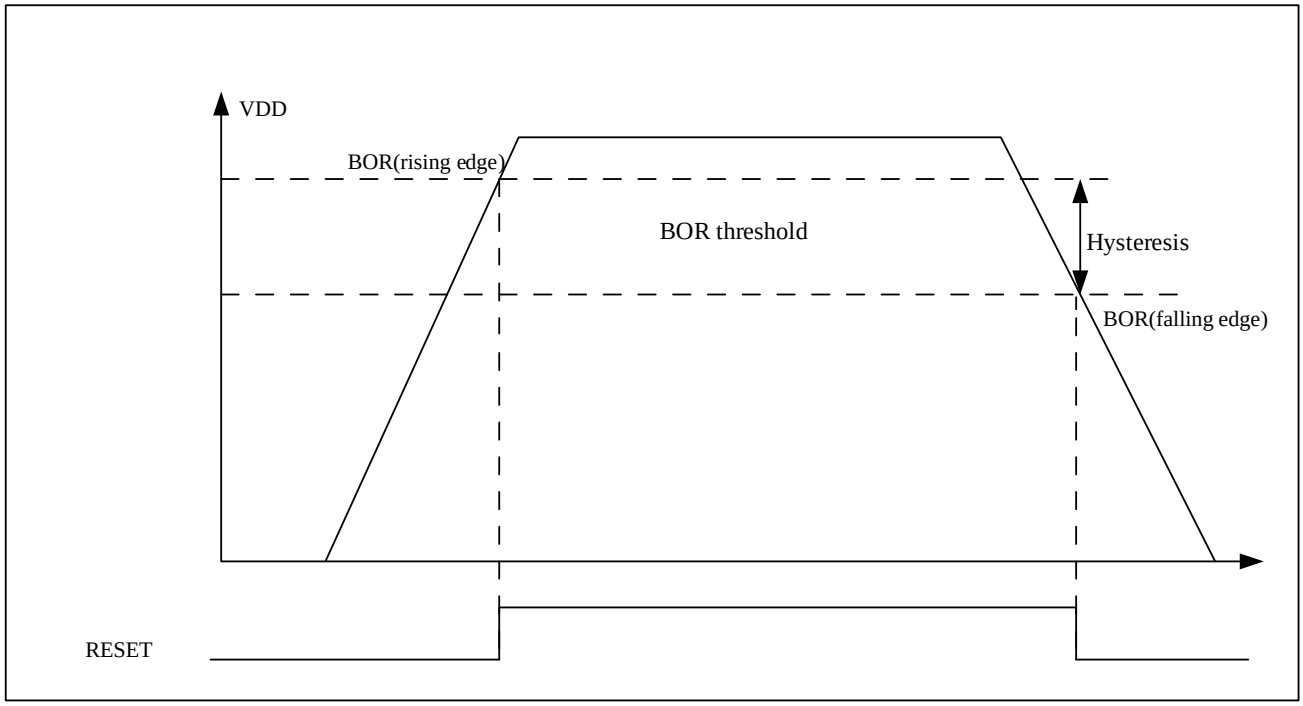
V_{BOR} is configured through option bytes and offers a choice of 7 V_{BOR} thresholds.

- BOR level 0 - reset level threshold 1.67V (release level threshold 1.72V)
- BOR level 1 - reset level threshold 1.8V (release level threshold 1.9 V)
- BOR level 2 - reset level threshold 2.1V (release level threshold 2.2 V)
- BOR level 3 - reset level threshold 2.4V (release level threshold 2.5V)
- BOR level 4 - reset level threshold 2.7V (release level threshold 2.8V)
- BOR level 5 - reset level threshold 3.0V (release level threshold 3.1V)
- BOR level 6 - reset level threshold 3.35 V (release level threshold 3.45 V)

When the power supply voltage (VDD) drops below the selected V_{BOR} threshold, the device will be reset.

Disabling BOR can be achieved by programming the device option bytes. To disable the BOR function, VDD must be higher than V_{BOR0} to initiate device option byte programming, and then the power-down reset (PDR) must monitor the power-down process

Figure 3-5 BOR Threshold Waveform



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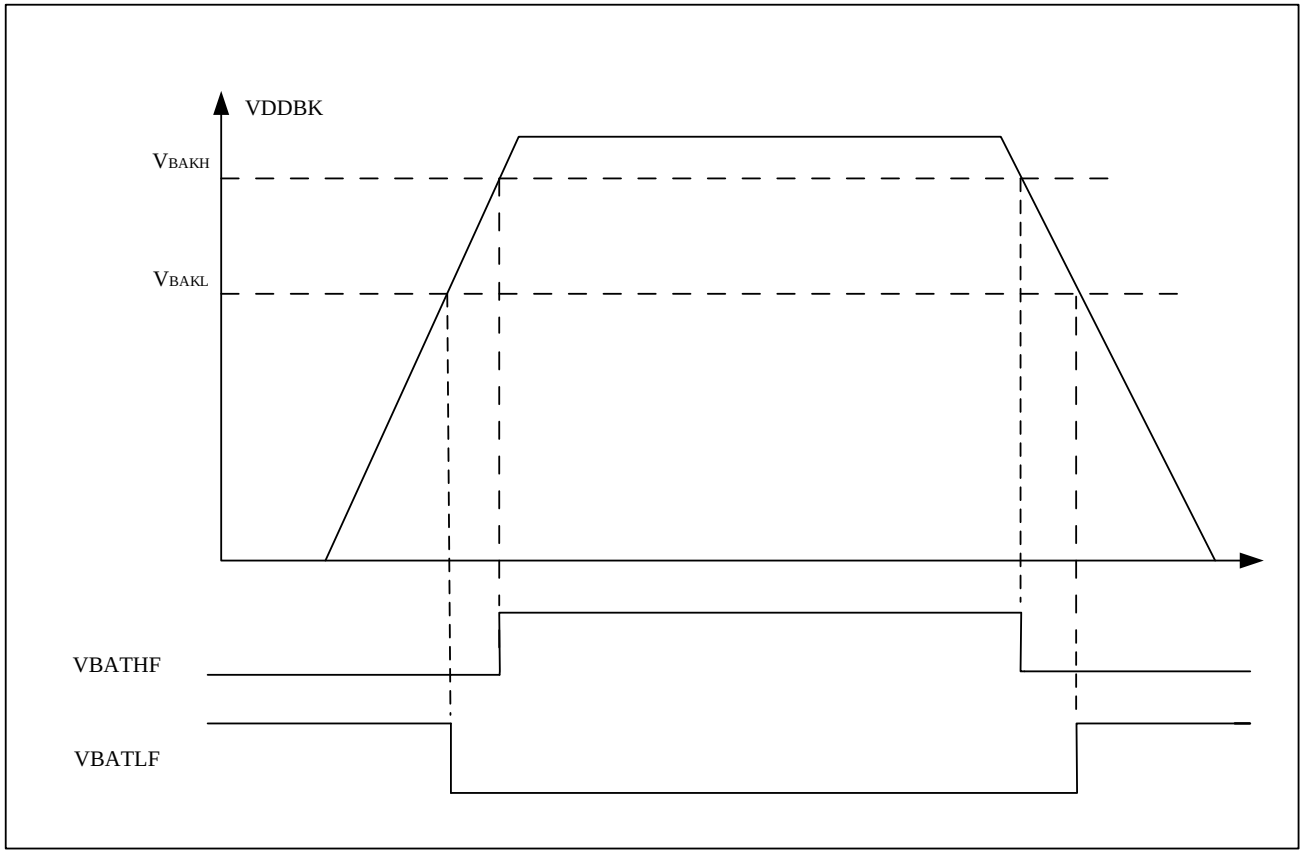
3.4.2.5 Battery voltage thresholds

There is an internal power switch, which can select the voltage source of Backup domain V_{BAT} or V_{DD} The supply voltage for Backup domain (VDDBK) can be monitored with a top voltage and a bottom voltage (V_{BAKH} and V_{BAKL}), when VABTMEN bit is set, if VDDBK is over V_{BAKH} or lower than V_{BAKL}, the flag bit V_{BATHF} / V_{BATLF} will set. Backup domain voltage thresholds, as is shown in Figure 3-6.

V_{BAKH} and V_{BAKL} are connected to RTC tamper signals (see Chapter: Real-time clock (RTC)).

Note: When the device does not operate in V_{BAT} mode, the battery voltage monitoring checks V_{DD} level.

Figure 3-6 Waveform of the Backup domain voltage thresholds



Note: For thresholds values, please refer to the datasheets.

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3.4.3 Power Modes

The power modes of the chip are composed of two parts: the CPU power modes and System power modes.

3.4.3.1 CPU domain power modes

The two CPUs power modes are independent. They are controlled separately by their own CPU control state machine.

Each of the CPUs has the following power modes.

- CPU domain Run mode (Cn_RUN)

  CPU is running. Power and CPU Clocks are on. Peripherals clock gating optional by Software.

- CPU domain domain Sleep mode (Cn_SLP)

  The CPU clock is gated off. SLEEP from Coretex-M cores is asserted, but SLEEPDEEP is not asserted. Peripherals can run or clock gated by Software if both CPUs agree to gate off the clock of a specific periphral.

- CPU domain Stop0 mode (Cn_STP0)

  The CPU clock is gated off. SLEEPDEEP from Coretex-M cores is asserted. Peripherals can be clock gated by software of the other CPU alone.

  System power mode depends on the power status of the other CPU.

- CPU domain Stop2 mode (Cn_STP2)

  The CPU is allowed to go Retention mode for power saving. System power mode depends on the power status of the other CPU.

- CPU domain Standby mode (Cn_STBY)

  The CPU is allowed to go Standby mode for power saving. System power mode depends on the power status of the other CPU.

Depends on the CPU interface signals Cn_SLEEP and Cn_SLEEPDEEP, and CPU configurable registers Cn_PDDS and Cn_STOP2S, CPU domain enter a specific state according to the table blew

Table 3-3 CPU domain power mode control signals

Power Modes	Cn_PDDS	Cn_STOP2S
Cn_RUN	X	X
Cn_SLP	X	X
Cn_STP0	0	0
Cn_STP2	0	1
Cn_STBY	1	X

After power up, the system go into RUN mode once the POR_BKP is released. CM7 domain also go into RUN mode after POR_main is released.

CM4 domain will stay in STANDBY for CM7 only models. Otherwise, CM4 domain goes to RUN mode after POR_main is released.

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Power mode transitions of the two CPUs between RUN and the CPU low power modes runs independently. While the power mode transition between RUN and the system low power modes depends on the power mode of both the CPUs.

Coretex-M7 and Coretex-M4 processors each has two sleep modes:

1. Normal Sleep
2. Deep Sleep

The value of SCR.SLEEPDEEP decides if the processor goes to Normal Sleep or Deep Sleep mode. Transition from Cn_RUN mode to low power modes is always initiated by software with execution of the WFI(Wait-for-Event), WFE(Wait-for-Interrupt) or Sleep-on-Exit instructions. If the software decides to go to Normal Sleep mode, it will assert Sleep mode only, it does not assert the CPU output sleepdeep.

Power mode transition of chip system and CPUs is depicted in the figure below.

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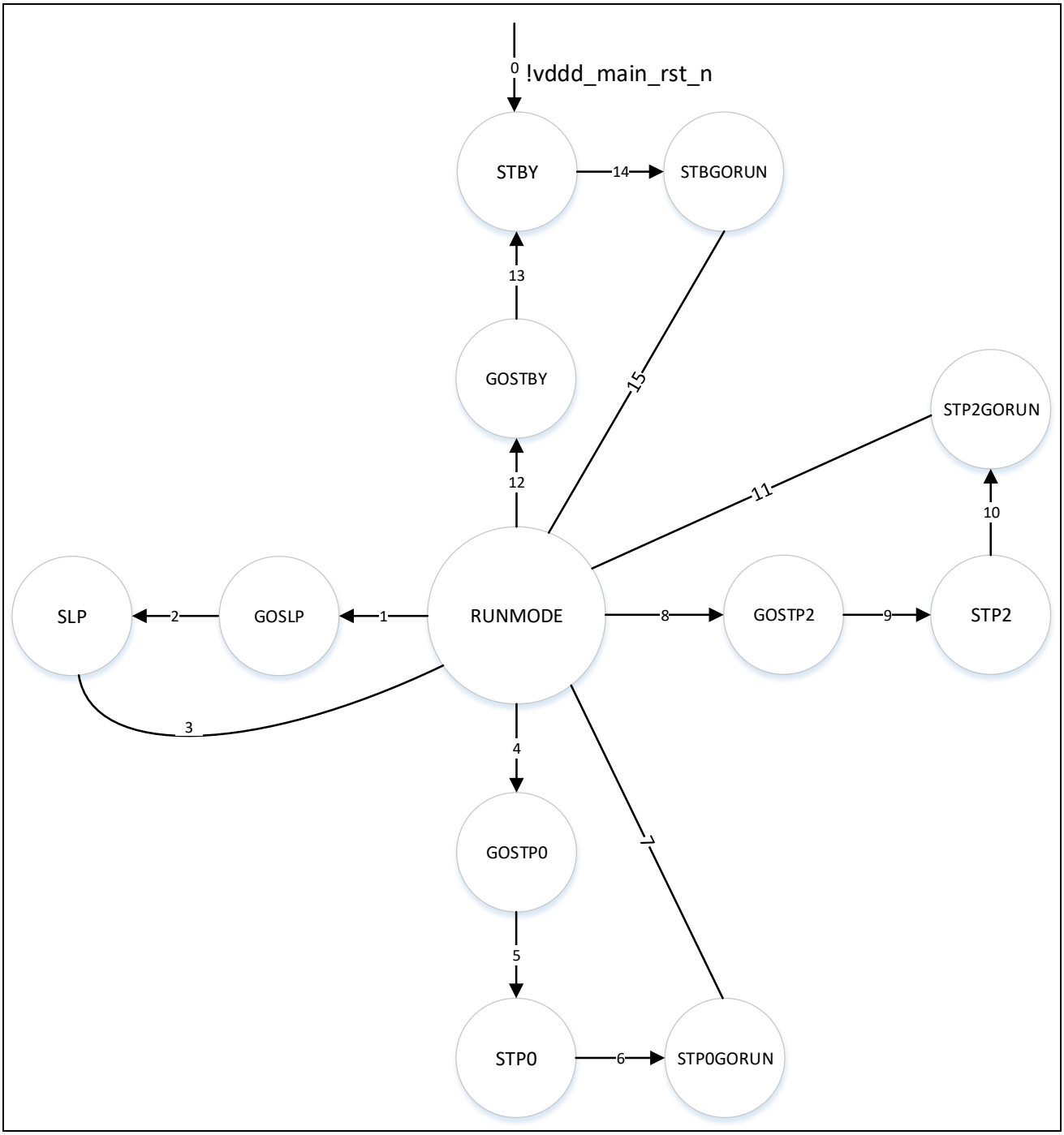
Figure 3-7 CPU Domain power mode transition diagram



The table below shows the CPU low power states transition conditions.

Table 3-4 CPU low power mode transition conditions

CPU power mode	Enter	Exit
Cn_SLP	Cn_SLEEP && ! Cn_SLEEPDEEP	Interrupt | Event | Debug request
Cn_STP0	Cn_SLEEPDEEP and LPM1==1	EXTI Wkup | NRST

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Cn_STP2	Cn_SLEEPDEEP and LPM1==2	EXTI Wkup | NRST
Cn_STBY	Cn_SLEEPDEEP and LPM1==3	WUP_IO | RTC | NRST

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3.4.3.2 System Power Modes

Depends on the power modes of the two CPUs described above and the wakeup sources for the low power operation modes, the chip can work in system power modes described below:

- System Run mode(S_RUN):

After power up, the chip goes to S_RUN mode immediately. If any of the two CPUs is in Cn_RUN or Cn_SLP mode, the chip stays in RUN mode.

- System Stop0 mode(S_STP0):

If any of the two CPUs goes to STOP mode, and the other CPU is in a power mode the is in Cn_STP0, Cn_STP2 or Cn_STBY mode.

In hardware power control mode, all peripherals in Core Domain are clock gated. In software power control mode, clock gating of the peripherals

- System STOP2 mode(S_STP2):

If One of the CPUs is transitioning into Cn_STBY, and the other CPU is in Cn_STP2 or Cn_STBY mode, the chip system power mode will change to S_STP2. Otherwise, if the other CPU is in Cn_STP mode, the system will go into S_STP0.

- System Standby mode(S_STBY):

Only when both the CPUs are in CN_STB mode, the system power mode will go S_STB.

Table 3-5 Chip components Power status at different Power Modes

Power Modes			Main Domain			Ret Domain	Bkp Domain
CPU1	CPU2	SYSTEM	CPU1 Domain	CPU2 Domain	Periph		
RUN/SLP	RUN/SLP	SRUN_C1RUN_C2RUN	ON/HCG[1]	ON/HCG	SWPCG[3]	ON	ON
STP0	RUN/SLP	SRUN_C1STP0_C2RUN	HWCG[2]	ON/HCG	SWPCG		
STP2	RUN/SLP	SRUN_C1STP2_C2RUN	Retention	ON/HCG	SWPCG		
STBY	RUN/SLP	SRUN_C1STBY_C2RUN	OFF	ON/HCG	SWPCG		
RUN/SLP	STP0	SRUN_C1RUN_C2STP0	ON/HCG	HWCG[4]	SWPCG		
RUN/SLP	STP2	SRUN_C1RUN_C2STP2	ON/HCG	Retention	SWPCG		
RUN/SLP	STBY	SRUN_C1RUN_C2STBY	ON/HCG	OFF	SWPCG		
STP0	STP0	SSTP0_C1STP0_C2STP0	HWCG	HWCG	HWCG	ON	
STP2	STP0	SSTP0_C1STP2_C2STP0	Retention	HWCG			
STBY	STP0	SSTP0_C1STBY_C2STP0	OFF	HWCG			
STP0	STP2	SSTP0_C1STP0_C2STP2	HWCG	Retention			
STP0	STBY	SSTP0_C1STP0_C2STBY	HWCG	OFF			
STP2	STP2	SSTP2_C1STP2_C2STP2	Retention	Retention	OFF	ON	
STBY	STP2	SSTP2_C1STBY_C2STP2	OFF	Retention			
STP2	STBY	SSTP2_C1STP2_C2STBY	Retention	OFF			
STBY	STBY	SSTBY_C1STBY_C2STBY	OFF	OFF	OFF	OFF	

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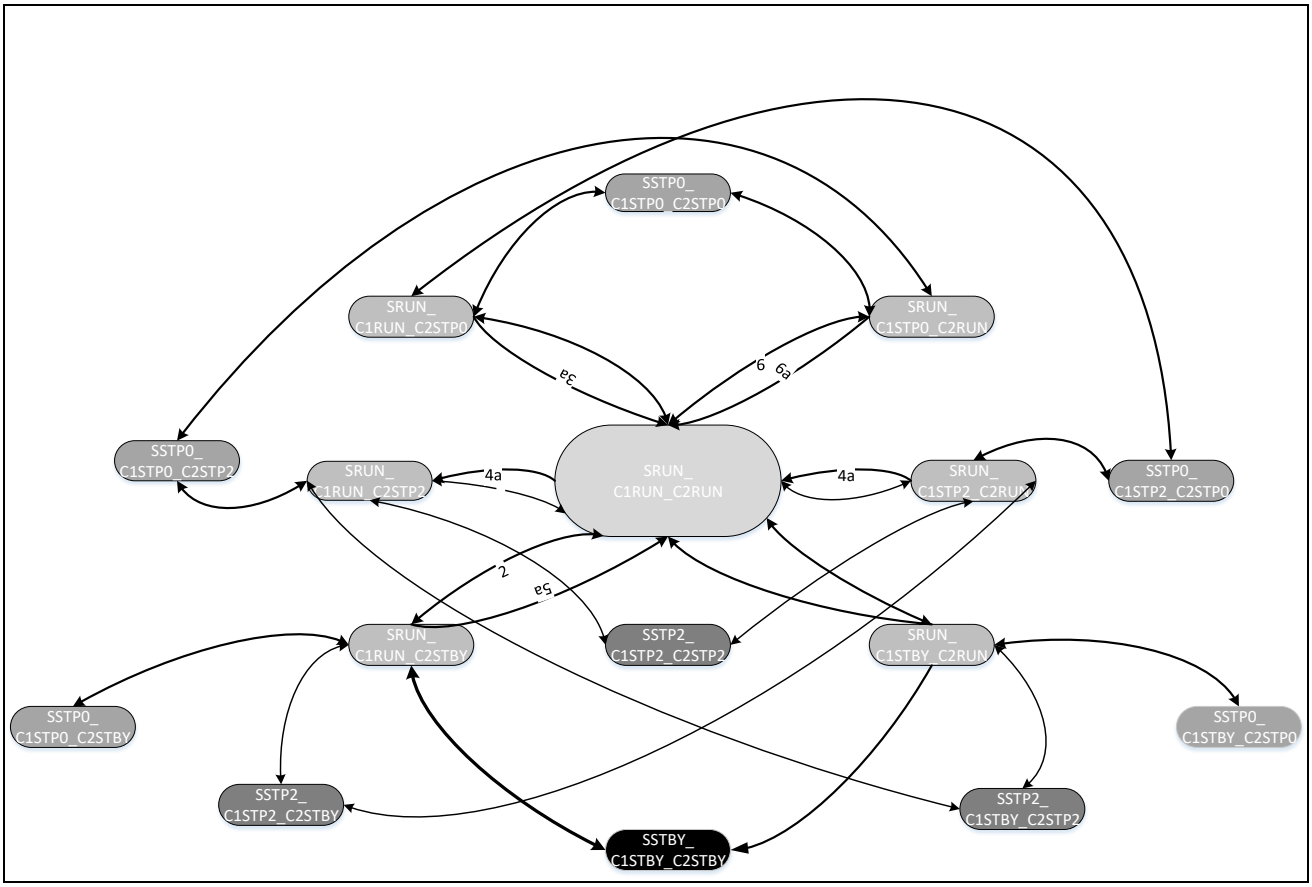
STBY	STBY	VBAT	OFF	OFF	OFF	OFF	ON

Notes:

1. *CPU HCLK is gated by RCC in Cn_SLP mode.*
2. *In software control mode, all core domain peripherals are controlled by software in Cn_RUN, Cn_SLP and Cn_STP mode. In hardware control mode, clock for a peripheral is switched off based on power mode by HW.*
3. *SWPCG = Software controlled Power or Clock Gating. In system Run SRUN_C1XXX_C2XXX modes, Clock and power gating are controlled by Software.*
4. *HWCG = Hardware Clock Gating.*

Depends on the power state of every CPU M7 and M4 sytem power mode transition is shown below.

Figure 3-8 System power mode transition



The table below shows the System low power states transition

Table 3-6 System low power mode transition conditions

Chip power mode	Enter	Exit
S_STP0	~(c2_run | c2_slp) & c1_stp OR ~(c1_run | c1_slp) & c2_stp	EXTI1 or EXTI2 Wkup or NRST

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S_STP2	~(c2_ret | c2_stb) & c1_ret OR (c1_ret | c1_stb) & c2_ret	EXTI1 or EXTI2 Wkup or NRST
S_STBY	c1_stb & c2_stb	WUP_IO | RTC | NRST

3.5 Programming Guide

This section provides the guide for power related controlling of different blocks or sub-domains.

3.5.1 Delayed CM7 boot after smu_flow_done

One user configurable delay from smu_flow_done to CM7 boot can be added if NVR bit smu2pwr_dly_en (OTPC_PWR_OTP_DLY_CFG1_LSB_BKP) is set to '1'. If enabled, the extra delay is added every time CM7 wakes up from STANDBY mode, including the initial power up.

The delay inserted here is based on an eight-bit counter on LSI clock and NVR configuration OTPC_PWR_OTP_DLY_CFG1_LSB_BKP[0].

The max delay can be added here is ~(256+2)*(1/30KHz) = 8.6ms.

3.5.2 OTP power control

OTP core power is shut down (enter OTP Deep Standby mode) when the system is in Standby mode or OTP_STP2_DSTBY register is set to 1 by software.

OTP can also be forced to Standby or Deep Standby when the chip is in RUN mode, by congfiguring PWR_SYSCTRL2.OTP_FRCSTB, PWR_SYSCTRL2.OTP_FRCDSTB respectively with software.

Table 3-7 OTP power mode control

Chip power Mode	OTP mode	Comments
RUN	Can enter Standby or Deep Standby power mode by Softeare	By setting the registers below respectively: PWR_SYSCTRL2.OTP_FRC_STBY, PWR_SYSCTRL2.OTP_FRC_DSTBY
STP0	Can enter Standby or Deep Standby power mode by PWR when entering low power mode.	By setting the registers below respectively before entering STOP0: PWR_SYSCTRL2.OTP_STB_INSTP0, PWR_SYSCTRL2.OTP_DSTB_INSTP0
STP2	Can enter Standby or Deep Standby power mode by PWR when entering STOP2 mode.	By setting the registers below respectively before entering STOP2: PWR_SYSCTRL2.OTP_STB_INSTP2, PWR_SYSCTRL2.OTP_DSTB_INSTP2
STBY	Enter Standby mode by PWR	

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3.5.3 nRST_STOP and nRST_STBY

nRST_STOP and nRST_STBY are NVR bits from OTP. They are low-active.

If nRST_STOP is low when the system is to enter STOP0/STOP2 mode, the system doesn't go to STOP mode，instead PWR sends a request and RCC generates a system reset;

If nRST_PD is low when the chip is to enter Standby mode, the system does not go to Standby mode, instead PWR sends a request and RCC generates a system reset.

3.5.4 SRAM power-saving modes

The SRAMs, including TCM, AXI SRAMs, Caches for CM7, AHB SRAMs, and AHB caches for CM4, are equipped with power gating capabilities. These memories can function in various power-saving modes determined by specific settings or internal control logic. The operational modes can be adjusted to optimize power consumption and performance based on the system requirements.

Table 3-8 SRAM power-saving modes defination

Power mode	Memory Power Mode	Wake-up time	Memory Contents	Note
Chip Enable	Very high	-	Not corrupted	SRAM in operation mode, can be read/written
Chip Disable	Very high	Very short	Not corrupted	SRAM disabled; cannot be read/writtern. Can be accessed immediately after enabling.
Selective Precharge	High	Short	Retained	SRAM in precharge mode. Must switch to Chip Disable mode before entering and exiting.
Retention 1	Medium	Medium	Retained	Memory retained with higher leakage but shorter wake-up time
Retention 2	Low	Long	Retained	Memory retained with lower leakage than Retention 1, but longer wake-up time.
Power Down	Very low	Very long	Corrupted	Power gated.

3.5.5 TCM power control in CM7 power modes

The power control of TCM in different CM7 power modes is listed in the table below.

Table 3-9 TCM memory power mode and control

CM7 Power mode	Memory Power Mode	Memory Power Mode Control
C1_Run/Slp	Chip Enable	Dynamic hardware control (not control by software)
	Chip Disable	Dynamic hardware control (not control by software)
C1_STP0	Chip Disable	Control reg PWR_M7MEMLPCTRL.MEM_PGSTP0EN =0 PWR_M7MEMLPCTRL.MEM_RETSTP0EN =0
	Selective/Precharge	PWR_M7MEMLPCTRL.MEM_PGSTP0EN =0 PWR_M7MEMLPCTRL.MEM_RETSTP0EN =1

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	Retention 1	PWR_M7MEMLPCTRL.MEM_PGSTP0EN =1 PWR_M7MEMLPCTRL.MEM_RETSTP0EN =1 PWR_M7TCMRET1Nx.M7TCM_RET1Nx[31:0]=0 PWR_M7TCMRET2Nx.M7TCM_RET2Nx[31:0]=1
	Retention 2(Caches can only be in Retention mode1, TCM can be set to Retention mode 2)	PWR_M7MEMLPCTRL.MEM_PGSTP0EN =1 PWR_M7MEMLPCTRL.MEM_RETSTP0EN =1 PWR_M7TCMRET1Nx.M7TCM_RET1Nx[31:0]=1 PWR_M7TCMRET2Nx.M7TCM_RET2Nx[31:0]=0
C1_STP2	Retention 1	PWR_M7TCMRET1Nx.M7TCM_RET1Nx[31:0]=0 PWR_M7TCMRET2Nx.M7TCM_RET2Nx[31:0]=1
	Retention 2	PWR_M7TCMRET1Nx.M7TCM_RET1Nx[31:0]=1 PWR_M7TCMRET2Nx.M7TCM_RET2Nx[31:0]=0
	Power Down	PWR_M7TCMRETxN0.M7TCM_RETxN0 [31:0]= 0 PWR_M7TCMRETxN1.M7TCM_RETxN1[31:0]= 0
C1_STBY	Power Down	TCM SRAMs are powered down by the PWR haredware when CM7 enters Standby mode.

3.5.6 TCM Partial Power Down

The 64 pieces of TCM/AXI SRAMs are all powered on at power-up. They can be partially powered down in RUN mode, by setting PWR_M7TCMPGx.TCM_PG0/PWR_M7TCMPGx.TCM_PG1 [n] to '1'. The corresponding TCM piece is powered down immediately after software set the PG bit to '1'.

Powering down a section of TCM's SRAM essentially involves removing one link from the daisy chain formed by the SRAMs. To avoid affecting other SRAMs in the chain, it is necessary to first reconnect the remaining SRAMs into the daisy chain, isolating the SRAM you wish to power down. Then, proceed to power it off. the following sequence should be followed when the software applying PG to a certain piece of TCM SRAM.

1. Software program PWR_M7TCMPG0/1.TCM_PGx[n] to 1, TCM piece [n] will be powered down.
2. PWR needs to synchronize the PWR_M7TCMPG0/1.TCM_PGx[n] to pwr_cpu_clk of CM7.
3. Bypass PWR_M7TCMRDYx.TCM_NRDY[n] of TCM piece [n] to the prydn of upstream link of the chain.
4. Power down the TCM piece [n].

Notes: Only one piece of SRAM can be powered down at a time. If multiple pieces need to be powered down, they need to be done one by one following the sequence above. The timing sequence of the steps is gurateed by hardware.

The process for powering up is: start by powering on the SRAM piece, wait for the corresponding power ready bit asserted, then connect it back into the corresponding position in the daisy chain.

1. Software program PWR_M7TCMPG0/1.TCM_PGx[n] to 0, TCM piece [n] will be powered on.
2. PWR needs to synchronize the PWR_M7TCMPG0/1.TCM_PGx[n] to pwr_cpu_clk of CM7.
3. PWR_M7TCMRDYx.TCM_NRDY[n] of TCM piece [n] change to 0, indicating it is powered on.

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4. Insert the memory piece back to the daisy chain to its place.

The timing sequence is guaranteed by hardware. If multiple pieces need to be powered up, Software should read register PWR_M7MEMLPSTS.TCMRDY equals to 1, before enabling the next piece.

The TCM memory pieces powered down by software during C1_RUN mode stays powered down in STOP0 mode. After wake-up from STOP0 mode, they stay powered-down by default； Software should configure the respective PWR_M7TCMPG0/1.TCM_PGx[n] to ‘0’ to power up the TCM piece [n].

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3.5.7 System Memory power mode and control

System memory comprises AHB SRAM1, AHB SRAM2, AHB SRAM3, AHB SRAM4, AHB SRAM5s1, AHB SRAM5s2, and AXI SRAM1. The power management of system memories in various system power modes is outlined in the table provided below.

Table 3-10 Memory power mode and control

Power mode	Memory Power Mode	Memory Power Mode Control
Run/Sleep	Chip Enable	Dynamic hardware control (not control by software)
	Chip Disable	Dynamic hardware control (not control by software)
STOP0	Chip Disable	PWR_SYSMEMLPCTRL.MEM_PGSTP0EN =0 and PWR_SYSMEMLPCTRL.MEM_RETSTP0EN =0
	Selective/Precharge	PWR_SYSMEMLPCTRL.MEM_PGSTP0EN =0 and PWR_SYSMEMLPCTRL.MEM_RETSTP0EN =1
	Retention 1	PWR_SYSMEMLPCTRL.MEM_PGSTP0EN =1 and PWR_SYSMEMLPCTRL.MEM_RETSTP0EN =1
STOP2	Retention 1	PWR_SYSMEMLPCTRL.AHBSRAMx_RET1n_EN=1 PWR_SYSMEMLPCTRL.AXISRAM_RET1n_EN=0
	Retention 2	PWR_SYSMEMLPCTRL.AHBSRAMx_RET1n_EN=0 PWR_SYSMEMLPCTRL.AHBSRAMx_RET2n_EN=1 PWR_SYSMEMLPCTRL.AXISRAM_RET1n_EN=0 PWR_SYSMEMLPCTRL.AXISRAM_RET2n_EN=1
	Power Down	PWR_SYSMEMLPCTRL.AHBSRAMx_RET1n_EN=0 PWR_SYSMEMLPCTRL.AHBSRAMx_RET2n_EN=0 PWR_SYSMEMLPCTRL.AXISRAM_RET1n_EN=0 PWR_SYSMEMLPCTRL.AXISRAM_RET2n_EN=0
Standby	Power Down	All system memories will enter Power Down mode when the chip transitions to System Standby power mode

Notes:

1. *PWR_M7MEMLPCTRL.MEM_RETSTP0EN/PWR_M4MEMLPCTRL.MEM_RETSTP0EN/ PWR_SYSMEMLPCTRL.MEM_RETSTP0EN, the same control shared by all memories in M7/M4/SYSTEM memory.*

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3.5.8 CM7 I/D cache power control

The power state of the CM7 embedded I/D Caches is not controlled separately; instead, they are switched on or off together with the CM7 Core.

3.5.9 CM4 I/D cache power control

CM4 AHB I/D caches can be powered off by software together. The power control of I/D caches is based on the AHB Low-Power Interface Q channel bus protocol.

To set the I/D-Cahce in quiescence，CM4 need to send quiescence request command;

To wake up I/D-Cahce from quiescence，CM4 need to send quiescence wakeup command;

A dedicate FSM inside PWR is used to handle the LPI Q-channel handshaking for ICache and DCache respectively.

3.5.10 BKP SRAM power control

The 64KB Backup SRAM remains in Chip Disable mode during system STOP0 and STOP2 modes. In System Standby and VBAT mode, the BKP SRAM can be in Retention 1 mode or Power-down mode depending on software configuration. Refer to the table below for more information.

STBY	Retention 1	BKP SRAM enter Retention 1 mode If PWR_M7CTRL2.BSRSTBRET =1 or PWR_M4CTRL2.BSRSTBRET =1 When system is in S_STBY mode.
	Power Down	BKP SRAM enter Power-down mode if PWR_M7CTRL2.BSRSTBRET = 0 and PWR_M4CTRL2.BSRSTBRET =0 When system is in S_STBY mode.
VBAT	Retention 1	BKP SRAM enter Retention 1 mode if PWR_M7CTRL2.BSRSTBRET =1 or PWR_M4CTRL2.BSRSTBRET =1 When system is in VBAT mode.
	Power Down	BKP SRAM enter Power-down mode if PWR_M7CTRL2.BSRSTBRET = 0 and PWR_M4CTRL2.BSRSTBRET =0 When system is in VBAT mode.

3.5.11 DBG low power modes

Low power modes can be debugged when setting corresponding DBG_MCU registers according to the following

Control Signal	Reg in DBG	meaning
DBGSTBY_CM7	DBG_CTRL[5]	0: CM7 enters normal CSTANDBY mode.

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		1: CM7 enters DBGSTBY
DBGSTOP_CM7	DBG_CTRL[4]	0: CM7 enters normal CSTP0/CSTP2 mode. 1: CM7 enters DBGSTP0/DBGSTP2 mode.
DBGSLEEP_CM7	DBG_CTRL[3]	0: CM7 enters normal Sleep mode. 1: CM7 enters DBGSLP
DBGSTBY_CM4	DBG_CTRL[2]	0: CM4 enters normal CSTANDBY mode. 1: CM4 enters DBGSTBY
DBGSTOP_CM4	DBG_CTRL[1]	0: CM4 enters normal CSTP0/CSTP2 mode. 1: CM4 enters DBGSTP0/DBGSTP2 mode.
DBGSLEEP_CM4	DBG_CTRL[0]	0: CM4 enters normal Sleep mode. 1: CM4 enters DBGSLP

When Enter DBG low power modes, power / clock will not be switched off as norm low power modes. Debugger can still access the reigsters of CPU core or Peripheral.

Only the wake-up sources for the normal low power modes can wake-up the corresponding DBG low power modes. E.g. a normal interrupt for sleep wakeup should not wake-up DBGSTP0, DBGSTP2 or DBGSTBY.

CSTP0 and CSTP2 share the same control bit DBG_STOP_CM7/DBTSTOP_CM4.

The two CPU cores DBG low power modes are controlled independently. i.e. CM7 can be in a DBG low power mode while the CM7 can be in normal power modes.

When PWR main FSM exits from DBGSTBY mode, PWR sends a request and RCC generates a system reset.

The table below lists conditions for transitions around DBGSLP, DBGSTP0, and DBGSTBY.

No.	FROM	TO	CONDITION	DESCRIPTION
1	RUNMODE	DBGSLP	SLEEP&DBG_SLEEP	The system goes to DBGSLP mode
2	DBGSLP	RUNMODE	INTERRUPT/EVENT	The system wakeups from DBGSLP mode
3	RUNMODE	DBGSTP0	SLEEPDEEP &~PDDS & DBG_STP0	The system goes to DBGSTP0 mode
4	DBGSTP0	RUNMODE	EXTI	The system wakeups from DBGSTP0 mode
5	RUNMODE	DBGSTP0	SLEEPDEEP &~PDDS & DBG_STP2	The system goes to DBGSTP2 mode
6	DBGSTP2	RUNMODE	EXTI	The system wakeups from DBGSTP2 mode
7	RUNMODE	DBGSTBY	SLEEPDEEP &PDDS & DBG_STBY	The system goes to DBGPD mode
8	DBGSTBY	DBGSTBYGORUN	dbg_pd_wakeup	The system wakes up from DBGPD mode.
9	DBGPDGORUN	POWRON	-	In DBGPDGORUN state, RCC generates low power reset, and PWR main FSM goes to reset state POWRON

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3.5.12 Power Control of Graphics domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain. GPU, JPEC, LCDC and DVP are grouped into Graphics domain. Power of the Graphics domain and the memories of consisting IPs are controlled separately. The memory has only On or Off state, no retention mode is used for the IP's memory.

The power control of Graphics domain is described below

3.5.12.1 Power on Graphics domain

To power on Graphics domain, follow the steps below:

1. If GPU needs to work, write PWR_IPMEMCTRL.GPU_PGEN=0 to switch on the power of GPU memories. Then poll the value of PWR_IPMEMSTS.GPU_PRDY until it is '1', to make sure GPU memory power is on.
2. If LCDC needs to work, write PWR_IPMEMCTRL.LCDC_PGEN =0 to switch on the power of LCDC memories. Then poll the value of PWR_IPMEMSTS.LCDC_PRDY until it is '1', to make sure LCDC memory power is on.
3. If JPEG needs to work, write PWR_IPMEMCTRL.JEPG_PGEN =0 to switch on the power of JEPG memories. Then poll the value of PWR_IPMEMSTS.JEPG_PRDY until it is '1', to make sure JEPG memory power is on.
4. If MIPI DSI needs to work, write PWR_IPMEMCTRL.DSI_PGEN =0 to switch on the power of DSI memories. Then poll the value of PWR_IPMEMSTS.DSI_PRDY until it is '1', to make sure DIS memory power is on.
5. If DVP needs to work, write PWR_IPMEMCTRL.DVP_PGEN =0 to switch on the power of DVP memories. Then poll the value of PWR_IPMEMSTS.DVP_PRDY until it is '1', to make sure LCDC memory power is on.
6. Set PWR_SYSCTRL3.GRCPSWACK1 =1 will reduce the power up time of Graphics domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
7. Set PWR_SYSCTRL3.GRC_PGEN = 1, this will switch on the power to Graphics domain.
8. Poll the value of PWR_SYSCTRL3.GRC_PWRRDY, until it reads 1.
9. Set PWR_SYSCTRL3.GRC_FUCEN = 1, which will bring Graphics domain out of reset state.
10. Set PWR_SYSCTRL3.GRC_ISNEN=1, to remove isolation on Graphics output signals.

3.5.12.2 Power off Graphics domain

To power off Graphics domain, follow the steps below:

1. Clear PWR_SYSCTRL3.GRC_ISNEN =0, to apply isolation on Graphics domain output signals.
2. Clear PWR_SYSCTRL3.GRC_FUCEN = 0, which will bring Graphics domain to reset state.
3. Clear PWR_SYSCTRL3.GRC_PGEN =0, this will switch off the power to Graphics domain.
4. Poll the value of PWR_SYSCTRL3.GRC_PWRRDY, until it reads 0.

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5. If GPU was working, write PWR_IPMEMCTRL.GPU_PGEN =1 to switch off the power of GPU memories. Then poll the value of PWR_IPMEMSTS.GPU_PRDY until it is ‘0’, to make sure GPU memory power is off
6. If LCDC was working, write PWR_IPMEMCTRL.LCDC_PGEN =1 to switch off the power of LCDC memories. Then poll the value of PWR_IPMEMSTS.LCDC_PRDY until it is ‘0’, to make sure LCDC memory power is off
7. If JPEG was working, write PWR_IPMEMCTRL.JEPG_ PGEN =1 to switch off the power of JPEG memories. Then poll the value of PWR_IPMEMSTS.JEPG_PRDY until it is ‘0’, to make sure JEPG memory power is off.
8. If MIPI DSI was working, write PWR_IPMEMCTRL.DSI_PGEN =1 to switch off the power of MIPI DSI memories. Then poll the value of PWR_IPMEMSTS.DSI_PRDY until it is ‘0’, to make sure DSI memory power is off.
9. If DVP was working, write PWR_IPMEMCTRL.DVP_PGEN =1 to switch off the power of DVP memories. Then poll the value of PWR_IPMEMSTS.DVP_PRDY until it is ‘0’, to make sure DVP memory power is off

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3.5.13 Power Control of HSC1 domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain. USB1, ETH1 are grouped into HSC1 domain.

Power of the HSC1 domain and the memories of consisting IPs are controlled separately. The memories have only On or Off state, no retention mode is used for the IPs' memory.

The power control of HSC1 domain is described below

3.5.13.1 Power on HSC1 domain

To power on HSC1 domain, follow the steps below:

1. If USB1 needs to work, write PWR_IPMEMCTRL.USB1_PGEN=0 to switch on the power of USB1 memories. Then poll the value of PWR_IPMEMSTS.USB1_PRDY until it is '1', to make sure USB1 memory power is on.
2. If ETH1 needs to work, write PWR_IPMEMCTRL.ETH1_PGEN=0 to switch on the power of ETH1 memories. Then poll the value of PWR_IPMEMSTS.ETH1_PRDY until it is '1', to make sure ETH1 memory power is on
3. Set PWR_SYSCTRL3.HSC1_PSWACK1 =1 will reduce the power up time of HSC1 domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
4. Set PWR_SYSCTRL3.HSC1_PGEN = 1, this will switch on the power to HSC1 domain.
5. Poll the value of PWR_SYSCTRL3.HSC1_PWRRDY, until it reads 1.
6. Set PWR_SYSCTRL3.HSC1_FUCEN = 1, which will bring HSC1 domain out of reset state.
7. Set PWR_SYSCTRL3.HSC1_ISNEN =1, to remove isolation on Graphics output signals.

3.5.13.2 Power off HSC1 domain

To power off HSC1 domain, follow the steps below:

1. Clear PWR_SYSCTRL3.HSC1_ISNEN =0, to apply isolation on HSC1 domain output signals.
2. Clear PWR_SYSCTRL3.HSC1_FUCEN = 0, which will bring HSC1 domain to reset state.
3. Clear PWR_SYSCTRL3.HSC1_PGEN=0, this will switch off the power to HSC1 domain.
4. Poll the value of PWR_SYSCTRL3.HSC1_PWRRDY, until it reads 0.
5. If USB1 was working, write PWR_IPMEMCTRL.USB1_PGEN=1 to switch off the power of USB1memories. Then poll the value of PWR_IPMEMSTS.USB1_PRDY until it is '0', to make sure USB1 memory power is off.
6. If ETH1 was working, write PWR_IPMEMCTRL.ETH1_PGEN=1 to switch off the power of ETH1 memories. Then poll the value of PWR_IPMEMSTS.ETH1_PRDY until it is '0', to make sure ETH1 memory power is off.

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3.5.14 Power Control of HSC2 domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain.

USB2, ETH2 and SDMMC2 are grouped into HSC2 domain. The power control of HSC2 domain is described below

Power of the HSC2 domain and the memories of consisting IPs are controlled separately. The memories has only On or Off state, no retention mode is used for the IPs' memory.

The power control of HSC2 domain is described below

3.5.14.1 Power on HSC2 domain

To power on HSC2 domain, follow the steps below:

1. If USB2 needs to work, write PWR_IPMEMCTRL.USB2_PGEN=0 to switch on the power of USB2 memories. Then poll the value of PWR_IPMEMSTS.USB2_PRDY until it is '1', to make sure USB2 memory power is on.
2. If ETH2 needs to work, write PWR_IPMEMCTRL.ETH2_PGEN=0 to switch on the power of ETH2 memories. Then poll the value of PWR_IPMEMSTS.ETH2_PRDY until it is '1', to make sure ETH2 memory power is on.
3. If SDMMC2 needs to work, write PWR_IPMEMCTRL.SDMMC2_PGEN=0 to switch on the power of SDMMC2 memories. Then poll the value of PWR_IPMEMSTS.SDMMC2_PRDY until it is '1', to make sure SDMMC2 memory power is on.
4. Set PWR_SYSCTRL3.HSC2_PSWACK1 =1 will reduce the power up time of HSC2 domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
5. Set PWR_SYSCTRL3.HSC2_PGEN = 1, this will switch on the power to HSC2 domain.
6. Poll the value of PWR_SYSCTRL3.HSC2_PWRRDY, until it reads 1.
7. Set PWR_SYSCTRL3.HSC2_FUCEN = 1, which will bring HSC2 domain out of reset state.
8. Set PWR_SYSCTRL3.HSC2_ISNEN =1, to remove isolation on HSC2 output signals.

3.5.14.2 Power off HSC2 domain

To power off HSC2 domain, follow the steps below:

1. Clear PWR_SYSCTRL3.HSC2_ISNEN =0, to apply isolation on HSC2 domain output signals.
2. Clear PWR_SYSCTRL3.HSC2_FUCEN = 0, which will bring HSC2 domain to reset state.(like a PDR)
3. Clear PWR_SYSCTRL3.HSC2_PGEN=0, this will switch off the power to HSC2 domain.
4. Poll the value of PWR_SYSCTRL3.HSC2_PWRRDY, until it reads 0. (Better to check, not compulsory.)
5. If USB2 was working, write PWR_IPMEMCTRL.USB2_PGEN=1 to switch off the power of USB2 memories. Then poll the value of PWR_IPMEMSTS.USB2_PRDY until it is '0', to make sure USB2 memory power is off
6. If ETH2 was working, write PWR_IPMEMCTRL.ETH2_PGEN=1 to switch off the power of ETH2 memories. Then poll the value of PWR_IPMEMSTS.ETH2_PRDY until it is '0', to make sure ETH2 memory power is off.
7. If SDMMC2 was working, write PWR_IPMEMCTRL.SDMMC2_PGEN=1 to switch off the power of

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SDMMC2 memories. Then poll the value of PWR_IPMEMSTS.SDMMC2_PRDY until it is '0', to make sure SDMMC2 memory power is off.

3.5.15 Power Control of MDMA domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain.

MDMA is set as an independent domain. The power control of MDMA domain is described below.

3.5.15.1 Power on MDMA domain

To power on MDMA domain, follow the steps below:

1. Set PWR_MDMACTRL.MDMA_PSWACK1 =1 will reduce the power up time of MDMA domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
2. Set PWR_MDMACTRL.MDMA_PGEN = 1, this will switch on the power to MDMA domain.
3. Poll the value of PWR_MDMACTRL.MDMA_PWRRDY, until it reads 1.
4. Set PWR_MDMACTRL.MDMA_FUCEN = 1, which will bring MDMA domain out of reset state.
5. Set PWR_MDMACTRL.MDMA_ISNEN =1, to remove isolation on MDMA output signals.

3.5.15.2 Power off MDMA domain

To power off MDMA domain, follow the steps below:

1. Clear PWR_MDMACTRL.MDMA_ISONEN =0, to apply isolation on MDMA output signals.
2. Clear PWR_MDMACTRL.MDMA_FUCEN = 0, which will bring MDMA domain to reset state.
3. Clear PWR_MDMACTRL.MDMA_PGEN=0, this will switch off the power to MDAM domain.
4. Poll the value of PWR_MDMACTRL.MDMA_PWRRDY, until it reads 0.

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3.5.16 Power Control of ESC domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain.

ESC is set as an independent domain. The power control of ESC domain is described below

3.5.16.1 Power on ESC domain

To power on ESC domain, follow the steps below:

1. Write 0 to PWR_IPMEMCTRL.ESC_PGEN, to switch on the power of ESC memories.
2. Poll the value of PWR_IPMEMSTS.ESC_PRDY until it is '1', to make sure ESC memory power is ready.
3. Set PWR_ESCCTRL.ESC_PSWACK1 =1 will reduce the power up time of ESC domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
4. Set PWR_ESCCTRL.ESC_PGEN = 1, this will switch on the power to ESC domain.
5. Poll the value of PWR_ESCCTRL.ESC_PWRRDY, until it reads 1.
6. Set PWR_ESCCTRL.ESC_FUCEN = 1, which will bring ESC domain out of reset state.
7. Set PWR_ESCCTRL.ESC_ISNEN =1, to remove isolation on ESC output signals.

3.5.16.2 Power off ESC domain

To power off ESC domain, follow the steps below:

1. Clear PWR_ESCCTRL.ESC_ISNEN =0, to apply isolation on ESC output signals.
2. Clear PWR_ESCCTRL.ESC_FUCEN = 0, which will bring ESC domain to reset state.
3. Clear PWR_ESCCTRL.ESC_PGEN=0, this will switch off the power to ESC domain.
4. Poll the value of PWR_ESCCTRL.ESC_PWRRDY, until it reads 0.
5. Write 1 to PWR_IPMEMCTRL.ESC_PGEN, to switch of the power of ESC memories.
6. Poll the value of PWR_IPMEMSTS.ESC_PRDY until it is '0', to make sure ESC memory power is off.

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3.5.17 Power Control of SHRT_AFE domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain.

The two SHRTIMERs share the same analog front end SHRT_AFE. SHRTIM_AFE, SHRT1 and SHRT2 are there power domains that can be controlled separately.

3.5.17.1 Power on SHRT_AFE domain

If any domain SHRT1 or SHRT2 is powered on, SHRT_AFE should be powered on first.

To power on SHRTA domain, follow the steps below:

1. Set PWR_SHRTIMCTRL.SHRA_PSWACK1 =1 will reduce the power up time of SHRT_AFE domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
2. Set PWR_SHRTIMCTRL.SHRA_PGEN = 1, this will switch on the power to SHRT_AFE domain.
3. Poll the value of PWR_SHRTIMCTRL.SHRA_PWRRDY, until it reads 1.
4. Set PWR_SHRTIMCTRL.SHRA_FUCEN = 1, which will bring SHRT_AFE domain out of reset state.
5. Set PWR_SHRTIMCTRL.SHRA_ISO_EN_N=1, to remove isolation on SHRT_AFE output signals.

3.5.17.2 Power off SHRT_AFE domain

Only both SHRT1 and SHRT2 are powered off, SHART_AFE can be powered off.

To power off SHRT_AFE domain, follow the steps below:

1. Clear PWR_SHRTIMCTRL.SHRA_ISONEN =0, to apply isolation on SHRT_AFE output signals.
2. Clear PWR_SHRTIMCTRL.SHRA_FUCEN = 0, which will bring SHRT_AFE domain to reset state.
3. Clear PWR_SHRTIMCTRL.SHRA_PGEN=0, this will switch off the power to SHRT_AFE domain.
4. Poll the value of PWR_SHRTIMCTRL.SHRA_PWRRDY, until it reads 0.

3.5.18 Power Control of SHRT1 domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain.

The two SHRTIMERs share the same analog front end SHRT_AFE. SHRTIM_AFE, SHRT1 and SHRT2 are there power domains that can be controlled separately. If any domain SHRT1 or SHRT2 is powered on, SHRT_AFE is powered on. Only both SHRT1 and SHRT2 are powered off, SHART_AFE can be powered off.

3.5.18.1 Power on SHRT1 domain

If SHART_AFE is not powered on yet, follow steps of 3.5.17.1 to power on SHART_AFE first.

To power on SHRT1 domain, follow the steps below:

1. Set PWR_SHRTIMCTRL.SHR1_PSWACK1 =1 will reduce the power up time of SHRT1 domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.

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2. Set PWR_SHRTIMCTRL.SHR1_PGEN = 1, this will switch on the power to SHRT1 domain.
3. Poll the value of PWR_SHRTIMCTRL.SHR1_PWRRDY, until it reads 1.
4. Set PWR_SHRTIMCTRL.SHR1_FUCEN = 1, which will bring SHRT1 domain out of reset state.
5. Set PWR_SHRTIMCTRL.SHR1_ISNEN_N=1, to remove isolation on SHRT1 output signals.

3.5.18.2 Power off SHRT1 domain

To power off SHRT1 domain, follow the steps below:

1. Clear PWR_SHRTIMCTRL.SHR1_ISNEN =0, to apply isolation on SHRT1 output signals.
2. Clear PWR_SHRTIMCTRL.SHR1_FUCEN = 0, which will bring SHRT1 domain to reset state.
3. Clear PWR_SHRTIMCTRL.SHR1_PGEN=0, this will switch off the power to SHRT1 domain.
4. Poll the value of PWR_SHRTIMCTRL.SHR1_PWRRDY, until it reads 0.
5. If SHRT1 is not in use, SHART_AFE can be powered off following steps of 3.5.17.2 .

3.5.19 Power Control of SHRT2 domain

Power on and power off of functional sub-domains is solely by software. Either CM7 or CM4 can control the power of any sub-domain.

The two SHRTIMERs share the same analog front end SHRT_AFE. SHRTIM_AFE, SHRT1 and SHRT2 are there power domains that can be controlled separately. If any domain SHRT1 or SHRT2 is powered on, SHRT_AFE is powered on. Only both SHRT1 and SHRT2 are powered off, SHART_AFE can be powered off.

3.5.19.1 Power on SHRT2 domain

If SHART_AFE is not powered on yet, follow steps of 3.5.17.1 to power on SHART_AFE first.

To power on SHRT2 domain, follow the steps below:

1. Set PWR_SHRTIMCTRL.SHR2_PSWACK1 =1 will reduce the power up time of SHRT2 domain with a higher inrush current. It's recommended to keep the default value (0) to control the inrush.
2. Set PWR_SHRTIMCTRL.SHR2_PGEN = 1, this will switch on the power to SHRT2 domain.
3. Poll the value of PWR_SHRTIMCTRL.SHR2_PWRRDY, until it reads 1.
4. Set PWR_SHRTIMCTRL.SHR2_FUCEN = 1, which will bring SHRT2 domain out of reset state.
5. Set PWR_SHRTIMCTRL.SHR2_ISNEN =1, to remove isolation on SHRT2 output signals.

3.5.19.2 Power off SHRT2 domain

To power off SHRT2 domain, follow the steps below:

1. Clear PWR_SHRTIMCTRL.SHR2_ISNEN =0, to apply isolation on SHRT2 output signals.
2. Clear PWR_SHRTIMCTRL.SHR2_FUCEN = 0, which will bring SHRT2 domain to reset state.
3. Clear PWR_SHRTIMCTRL.SHR2_PGEN=0, this will switch off the power to SHRT2 domain.

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4. Poll the value of PWR_SHRTIMCTRL.SHR2_PWRRDY, until it reads 0.

If SHRT2 is not in use, SHART_AFE can be powered off following steps of 3.5.17.2 .

3.5.20 Power Control of FMAC

FMAC resides in VDDD_MAIN domain. FMAC block is powered on and off with VDDD, controlled by PWR hardware. The power state of the FMAC memory is solely controlled by software.

3.5.20.1 Power on FMAC memory

To enable the use of FMAC in the application, follow the steps below to power on the FMAC memory first.

1. Write '0' to PWR_IPMEMCTRL.FMAC_PGEN, to switch on the power of FMAC memory.
2. Poll the value of PWR_IPMEMSTS.FMAC_PRDY until it is '1', to make sure FMAC memory power is ready.

3.5.20.2 Power off FMAC memory

When the FMAC is not in use, follow the steps below to power off the FMAC memory to save power:

1. Write '1' to PWR_IPMEMCTRL.FMAC_PGEN, to switch off the power of FMAC memory.
2. Poll the value of PWR_IPMEMSTS.FMAC_PRDY until it is '0', to make sure FMAC memory power is off.

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3.5.21 Voltage scaling in RUN mode

The voltage of VDDD can be adjusted between 0.8V to 0.9V.

When operating in DCDC supply mode, the DCDC voltage can be set in the RUN mode by configuring the AFEC register DA_DCDC_VSEL.

For testing or suppling external to the chip (by setting DCDC_FON=1) purpose, DCDC can be set to output voltage above 1V. To ensure the DCDC safely outputs voltage above 1V, the OTP configuration DCDC_HIGH_VCORE_EN should be set to 1, and the register DCDC_VSELKEY must be configured to 0xF.

The mapping of DA_DCDC_VSEL to the output voltage of DCDC in locked and unlocked conditions is illustrated below.

Table 3-11 DCDC Output Voltage Configuration

AFEC_DCDC_VSEL (from AFEC)	**DCDC_VSELKEY!=0xF Or DCDC_HIGHT_VCORE_EN==0**	**DCDC_VSELKEY==0xF And DCDC_HIGHT_VCORE_EN==1**
0000	0.60V	0.60V
0001	0.60V	0.60V
0010	0.65V	0.65V
0011	0.70V	0.70V
0100	0.75V	0.75V
0101	0.80V	0.80V
0110	0.85V	0.85V
0111	0.90V	0.90V
1000	0.95V	0.95V
1001	1.00V	1.00V
1010	**1.00V**	**1.05V**
1011	**1.00V**	**1.10V**
1100	**1.00V**	**1.15V**
1101	**1.00V**	**1.20V**
1110	**1.00V**	**1.25V**
1111	**1.00V**	**1.30V**

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The DCDC has embedded Power-On-Reset (POR) and Brown-Out-Reset(BOR) circuits.The threshhold voltage of DCDC POR and BOR are set by AFEC registers AFEC_DCDC_VSEL_POR， AFEC_DCDC_VSEL_BOR respectively. The DCDC POR, BOR thresholds must be set according to the scaling output voltage of DCDC.

Table 3-12 DCDC VSEL_POR/VSEL_BOR Mapping

AFEC_DCDC_VSEL_POR/BOR[4:0]	$V_{MON,POR/BOR}$(V)	Equilvelant POR Threshold Voltage(V)	Equilvelant BOR Threshold Voltage(V)
00000	0.55	0.479	0.473
00001	0.60	0.522	0.516
00010	0.65	0.566	0.559
00011	0.70	0.609	0.602
00100	0.75	0.653	0.645
00101	0.80	0.696	0.688
00110	0.85	0.740	0.731
00111	0.90	0.783	0.774
01000	0.95	0.827	0.817
01001	1.00	0.871	0.86
01010	1.05	0.914	0.903
01011	1.10	0.957	0.946
01100	1.15	1.001	0.989
01101	1.20	1.044	1.032
01110	1.25	1.088	1.075
01111	1.30	1.131	1.118
Others(Not allowed)	>1.30	>=1.175	>=1.161

In Main LDO supply mode, PWR register MLDO_OVSEL is used to set the output voltage of Main LDO.

In External supply mode, voltage of VDDD is decided by user. It is not controllable with user software. Software should set the voltage of VDDDBK, PLL LDO the same level as soon as software boot to make sure no big leakage or malfunction caused by different voltage inside the chip.

It is essential to ensure proper voltage alignment among the BKP LDO, source of VDDD (Main LDO, DCDC or external supply), and PLLs' LDO.

VDDD POR monitors the voltage of VDDD to generate POR reset. The VDDD POR is controlled by the PWR register VDDD_POR_SEL. To ensure smooth voltage scaling without any power-related issues, it is essential to adhere to the following sequence when VDDD voltage is being scaled,

When scaling down the voltage, software must ensure that the VDDD POR threshhold voltage is lowered before making any changes to the VDDD voltage to prevent the triggering of VDDD POR. When scaling up the voltage, it is recommended to adjust the VDDD POR threshold after a specific delay following the adjustment of the VDDD voltage.

In the RUN mode, the VDDDBK power is supplied from the VDDD, and the output voltage configuration of BKPLDO does not impact the VDDDBK voltage.

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VDDDBK POR monitors the voltage of VDDDBK. The nominal threshold of VDDDBK POR is fixed at 0.7V. The nominal threshold of VDDDBK PDR is set at 0.65V. VDDDBK POR and PDR thresholds are set at a value which will not trigger POR or PDR evne when the supply is scaled down to 0.8V.

3.5.21.1 Scale-down DCDC from 0.9V to 0.8V

When operating in DCDC supply VDDD mode, follow the steps below to scale down DCDC from 0.9V to 0.8V

1. Set VDDD POR threshold by setting PWR register VDDD_POR_SEL to 2'b00(POR 0.70V; PDR 0.65V);
2. Set AFEC_DCDC_VSEL_POR to 5'b00101, which will set both VMON,BOR and VMON,POR to 0.8V.

   Note that in order to have valid behavior of the DCDC_POR, DCDC_BOR, it is mandatory that VMON,BOR not lager than VMON,POR.
3. Set the DCDC output voltage to 0.8V by configuring AFEC_DCDC_VSEL to 2'b0101.

3.5.21.2 Scale-up DCDC from 0.8V to 0.9V

When operating in DCDC supply VDDD mode, follow the steps below to scale up DCDC from 0.8V to 0.9V:

1. Set the DCDC output voltage to 0.9V by configuring AFEC_DCDC_VSEL to 'b0111.
2. Set AFEC_DCDC_VSEL_POR to 5'b00111, which will set both VMON,BOR and VMON,POR to 0.9V.
3. Note that in order to have valid behavior of the DCDC_POR, DCDC_BOR, it is mandatory that VMON,BOR not lager than VMON,POR.
4. Set VDDD POR threshold by setting PWR register VDDD_POR_SEL to 2'b11(POR 0.80V; PDR 0.75V);

3.5.21.3 Scale-down Main LDO from 0.9V to 0.8V

When operating in Main LDO supply VDDD mode, follow the steps below to scale down Main LDO from 0.9V to 0.8V:

1. Set VDDD POR threshold by setting PWR register VDDD_POR_SEL to 2'b00(POR 0.70V; PDR 0.65V);
2. Set the Main LDO output voltage to 0.8V by configuring MLDO_OVSEL to 2'b00（0.8V）.

3.5.21.4 Scale-up DCDC from 0.8V to 0.9V

When operating in Main LDO supply VDDD mode, follow the steps below to scale up Main LDO from 0.8V to 0.9V:

1. Set the Main LDO output voltage to 0.9V by configuring MLDO_OVSEL to 2'b10.
2. Set VDDD POR threshold by setting PWR register VDDD_POR_SEL to 2'b11(POR 0.80V; PDR 0.75V);

The software sequence above ensures VDDD POR threshold-voltage lowered before lowering VDDD voltage, so that no VDDD POR is triggered before when scaling down the voltage of VDDD.

3.5.21.5 Scale-down BKP LDO from 0.9V to 0.8V

The output voltage of BKP LDO (ALDO) is controlled by PWR registster BG_VREF_VSEL. To scale down BKP LDO output from 0.9V to 0.8V :

1. Set the BKP LDO output voltage to 0.8V by configuring BG_VREF VSEL=1(0.8v).

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3.5.21.6 Scale-up BKP LDO from 0.8V to 0.9V

The output voltage of BKP LDO (ALDO) is controlled by PWR registster BG_VREF_VSEL. To scale up BKP LDO output from 0.8V to 0.9V :

1. Set the BKP LDO output voltage to 0.9V by configuring BG_VREF VSEL=0(0.9v).

3.5.22 Voltage scaling in Low Power modes

When transitioning to sytem STOP2 mode or STANDBY mode, the power supply voltage of VDDD can be scaled down to 0.8V. The setting of PWR register MR_LPVSELEN determines whether the system will scale down the voltage of VDDD.

3.5.22.1 Scale-down DCDC from 0.9V to 0.8V

When operating in DCDC supply mode, follow the steps below to configure the DCDC output voltage scaling to 0.8V in system power modes STOP2/STANDBY(MR_STBY_OFF_EN = 0) :

1. In the system RUN mode, the DCDC voltage depends on the AFEC register DA_DCDC_VSEL; the DCDC POR threshold voltage depends on DCDC_VSEL_POR and the VDDD POR depends on the AFEC register VDDD_POR_MR_SEL.
2. Configure VDDD_LPPOR_VSEL=’b00(POR is 0.7V, PDR is 0.65V) to set the threshold voltage for VDDD POR in low power modes.
3. Set the target DCDC POR reference voltage by configuring DCDC_LPPORVSEL=’b00101(targe monitoring 0.8V).
4. Before entering Low Power modes, configure PWR register DCDC_LPVSEL=’b0101(0.8V) to set the target DCDC output voltage in STOP2/STANDBY mode.
5. Note that no need to configure DCDC_LPVSEL everytime before entering low power modes if it does not need to be adjusted. Just configure once in system initialization if it is fixed for all low power modes in a target application.
6. Enable voltage scaling in STOP2/STANDBY mode by configuring MR_LPVSELEN.
7. Start the system power mode transition to STOP2/STANDBY mode.

At wakeup of low power modes STOP2/STANDBY, the voltage of VDDD is adjusted according to setting of AFEC register DA_DCDC_VSEL first, followed by the VDDD POR threshold adjusted to AFEC register VDDD_POR_MR_SEL.

This PWR hardware controls the sequence of VDDD POR threshold adjustment and DCDC output voltage adjustment to make sure no POR is triggered during the voltage scaling.

DCDC can be forcibly enabled by setting DCDCFRCEN to 1. When this setting is enabled, the DCDC will operate regardless of the system power mode, and the output voltage of the DCDC will be determined by the value of DCDC_FVSEL. The Output voltage of DCDC is as depcited in Table .

Table 3-13 DCDC Output Voltage Configuration

DCDC_LPVSEL	DCDC_VSELKEY!=0xF Or	DCDC_VSELKEY==0xF And

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	DCDC_HIGHT_VCORE_EN==0	DCDC_HIGHT_VCORE_EN==1
0000	0.60V	0.60V
0001	0.60V	0.60V
0010	0.65V	0.65V
0011	0.70V	0.70V
0100	0.75V	0.75V
0101	0.80V	0.80V
0110	0.85V	0.85V
0111	0.90V	0.90V
1000	0.95V	0.95V
1001	1.00V	1.00V
1010	**1.00V**	**1.05V**
1011	**1.00V**	**1.10V**
1100	**1.00V**	**1.15V**
1101	**1.00V**	**1.20V**
1110	**1.00V**	**1.25V**
1111	**1.00V**	**1.30V**

3.5.22.2 Scale-down Main LDO from 0.9V to 0.8V

When operating in MAIN LDO supply mode, follow the steps below to configure the MAIN LDO output voltage scaling to 0.8V in system power modes STOP2/STANDBY(MR_STBY_OFF_EN = 0) :

1. In the system RUN mode, the MAIN LDO voltage depends on the PWR register MLDO_OVSEL and the VDDD POR depends on the AFEC register VDDD_POR_MR_SEL.
2. Configure PWR register VDDD_LPPOR_VSEL=’b00 (POR is 0.7V, PDR is 0.65V) to set the threshold voltage for VDDD POR in low power modes.
3. Before entering Low Power modes, configure PWR register MLDO_LPOVSEL=’b00(0.8V) to set the target MAIN LDO output voltage in STOP2/STANDBY mode.
4. Note that no need to configure MLDO_LPOVSEL everytime before entering low power modes if it does not need to be adjusted. Just configure once in system initialization if it is fixed for all low power modes in a target application.
5. Enable voltage scaling in STOP2/STANDBY mode by configuring MR_LPVSELEN=1.
6. Start the system power mode transition to STOP2/STANDBY mode.

At wakeup of low power modes STOP2/STANDBY, the voltage of VDDD is adjusted according to setting of PWR register MLDO_OVSELfirst, followed by the VDDD POR threshold adjusted to AFEC register VDDD_POR_MR_SEL.

This PWR hardware controls the sequence of VDDD POR threshold adjustment and MAIN LDO output voltage adjustment to make sure no POR is triggered during the voltage scaling.

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3.5.22.3 Scale-down BKP LDO from 0.9V to 0.8V

If MR_LPVSELEN is 1， the voltage of BKP LDO (ALDO) is controlled by BG_LPVREF_VSEL in low power modes STOP2 and STANDBY; otherwise, the voltage of BKP LDO is controlled by BG_VREF_VSEL as in RUN mode.

Follow the steps below to scale down the BKP LDO in low power modes:

1. Set the BKP LDO output voltage to 0.8V by configuring BG_LPVREF_VSEL=1(0.8v).
2. Configure MR_LPVSELEN=1, to enable the power scaling in low power modes.

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Email: sales@nsing.com.sg

3.6 Registers

3.6.1 PWR M7 Control register 1 (PWR_M7CTRL1)

This register allows controlling M7 core power.

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															CVBATF
															rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CSBF	CWKUPF	PDS	Reserved
												rc_w1	rc_w1	rw	

Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	CVBTF	Clear VBAT flags. Always read as 0. 0: Invalid 1: Clear PWR_M7CTRLSTS.SBF and PWR_M7CTRLSTS.VBATF flags.
15:4	Reserved	Reserved, the reset value must be maintained
3	CSBF	Clear STANDBY flags. Always read as 0. 0: Invalid 1: Clear PWR_M7CTRLSTS.SBF and PWR_M7CTRLSTS.VBATF flags.
2	CWKUPF	Clear the pin wakeup bit. Always read as 0. 0: Invalid 1: Clear the PWR_M7CTRLSTS.WKUPxF wakeup bit after 2 system clock cycles.
1	PDS	Power down deep sleep bit. Cooperates with the LPS bit. 0: When the M7 core outputs DEEPSLEEP as '1', the chip enters standby mode, and the voltage regulator status is controlled by the LPS bit. 1: When the M7 core outputs DEEPSLEEP as '1', the chip enters stop mode.
0	Reserved	Reserved, the reset value must be maintained

3.6.2 PWR M7 Control Status register (PWR_M7CTRLSTS)

This register allows controlling M7 core power.

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Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					WKUP6F	WKUP5F	WKUP4F	WKUP3F	WKUP2F	WKUP1F	WKUP0F	WKUP5 POL	WKUP4 POL	WKUP3 POL	WKUP2 POL
					r	r	r	r	r	r	r	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP1 POL	WKUP0 POL	WKUP5 EN	WKUP4 EN	WKUP3 EN	WKUP2 EN	WKUP1 EN	WKUP0 EN	Reserved					VBATF	SBF	Reserved
rw	rw	rw	rw	rw	rw	rw	rw						r	r	

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	WKUP6F	RTC wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the RTC alarm
25	WKUP5F	WKUP5 pin PC1 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
24	WKUP4F	WKUP4 pin PI11 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
23	WKUP3F	WKUP3 pin PI8 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
22	WKUP2F	WKUP2 pin PC13 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTRL1.CWKUPF bit.

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Bit field	Name	Description
		0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
21	WKUP1F	WKUP1 pin PA2 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTR1L.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
20	WKUP0F	WKUP0 pin PA0 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M7CTR1L.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
19	WKUP5POL	Wake-up polarity for the WKUP5 pin PC1. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
18	WKUP4POL	Wake-up polarity for the WKUP4 pin PI11. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
17	WKUP3POL	Wake-up polarity for the WKUP3 pin PI8. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
16	WKUP2POL	Wake-up polarity for the WKUP2 pin PC13. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
15	WKUP1POL	Wake-up polarity for the WKUP1 pin PA2. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up

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Bit field	Name	Description
		1: Low level wake-up
14	WKUP0POL	Wake-up polarity for the WKUP0 pin PA0. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
13	WKUP5EN	WKUP5 pin PC1 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
12	WKUP4EN	WKUP4 pin PI11 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
11	WKUP3EN	WKUP3 pin PI8 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
10	WKUP2EN	WKUP2 pin PC13 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
9	WKUP1EN	WKUP1 pin PA2 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
8	WKUP0EN	WKUP0 pin PA0 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*

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Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained
2	VBATF	VBAT flag. This bit is set by hardware and cleared by POR/PDR (power-on/power-down reset) or setting the PWR_M7CTRL1.CVBTF bit. 0: M7 core is not in VBAT mode 1: M7 core enters VBAT mode
1	SBF	STANDBY flag. This bit is set by hardware and cleared by POR/PDR (power-on/power-down reset) or by setting the PWR_M7CTRL1.CSBF bit. 0: M7 core is not in standby mode 1: M7 core enters standby mode
0	Reserved	Reserved, the reset value must be maintained.

3.6.3 PWR M7 Control register 2 (PWR_M7CTRL2)

This register allows controlling M7 core power.

Address offset: 0x08

Reset value: 0x7FFF E904

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	MEM_CNTVAL[5:0]						PWR_CNTVAL[7:0]								TCM_RDYMD[1]
	rw						rw								rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RDYMD[0]	PWR_RDYMD[1:0]		HCLK_ONINSLP	NRST_WUPEN	Reserved		RTC_ALMWUPEN	Reserved					BSRSTBRET	BSRVBRET	STOP2EN
rw	rw		rw	rw			rw						rw	rw	rw

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:25	MEM_CNTVAL[5:0]	counter value for memory power ready count down The value written to this field is stored in MEM_CNTVAL, with reset value 0. The value read back is MEM_CNTVAL + M7MEM_CNTVAL_OTP. MEM_CNTVAL_OTP is a 6 bit value loaded from OTP, default 6'b111111. The sum is read back is also used for memory power ready count down. At power-up, MEM_CNTVAL = M7MEM_CNTVAL_OTP. After CPU boot-up , user can change the value by writting to this field MEM_CNTVAL. If M7MEM_CNTVAL_OTP keeps default value 6'b111111: 6'b000001 6'b000000

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Bit field	Name	Description
		6'b000010 6'b000001 …… 6'b111111 6'b111110 If 6'b010000 is programmed to M7MEM_CNTVAL_OTP: 6'b000001 6'b010001 6'b000010 6'b010010 …… 6'b111111 6'b001111
24:17	PWR_CNTVAL[7:0]	counter value for CM7 logic power ready count down The value written to this field is stored in PWR_CNTVAL, with reset value 0. The value read back is PWR_CNTVAL + M7MEM_CNTVAL_OTP. M7MEM_CNTVAL_OTP is a 6 bit value loaded from OTP, default 8'b11111111. The sum is read back is also used for memory power ready count down. At power-up, PWR_CNTVAL = PWR_CNTVAL_OTP. After CPU boot-up , user can change the value by writting to this field PWR_CNTVAL. If M7MEM_CNTVAL_OTP keeps default value 8'b11111111: 8'b00000001 8'b00000000 8'b00000010 8'b00000001 …… 8'b11111111 8'b11111110 If M7MEM_CNTVAL_OTP keeps default value 8'b11111111: 8'b00000001 8'b00010001 8'b00000010 8'b00010001 …… 8'b11111111 8'b00001111
16:15	TCM_RDYMD[1:0]	Selected the way of check TCM power ready for CM7 domain 00: check only RDY signal from TCM power switch 01: check Delay after enabled TCM power switch of CM7 domain 10: Check delay and RDY signal from TCM power switch 11: check delay after RDY signal from TCM power switch
14:13	PWR_RDYMD[1:0]	Selected the way of check power ready for CM7 domain 00: check only RDY signal from power switch 01: check Delay after enabled power switch of CM7 domain 10: Check delay and RDY signal from power switch 11: check delay after RDY signal from power switch
12	HCLK_ONINSLP	1: HCLK is on when M7 core in sleep. 0: HCLK is off when M7 core is in sleep.
11	NRST_WUPEN	NRST wakeup event enable in standby mode for M7 core. 0: NRST event wakeup M7 core is disabled 1: NRST event wakeup M7 core is enabled
10:9	Reserved	Reserved, the reset value must be maintained.
8	RTC_ALMWUPEN	RTC_ALARM wakeup enable in standby mode for M7 core.

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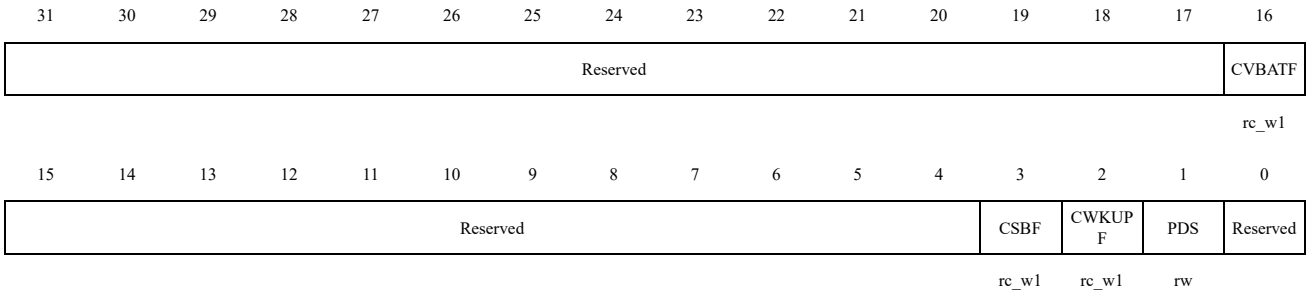
Bit field	Name	Description
		0: RTC_ALARM wakeup M7 core is disabled 1: RTC_ALARM wakeup M7 core is enabled
7:3	Reserved	Reserved, the reset value must be maintained.
2	BSRSTBRET	Backup SRAM retention enable in STANDBY mode. 0: Backup SRAM does not retain in STANDBY mode 1: Backup SRAM retains in STANDBY mode
1	BSRVBRET	Backup SRAM retention enable in VBAT mode. 0: Backup SRAM does not retain in VBAT mode 1: Backup SRAM retains in VBAT mode
0	STOP2EN	M7 core STOP2 mode enable. 0: M7 core enters STOP0 mode 1: M7 core enters STOP2 mode

3.6.4 PWR M4 Control register 1 (PWR_M4CTRL1)

This register allows controlling M4 core power.

Address offset: 0x20

Reset value: 0x0000 0000



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	CVBTF	Clear VBAT flags. Always read as 0. 0: Invalid 1: Clear PWR_M4CTRLSTS.SBF and PWR_M4CTRLSTS.VBATF flags.
15:4	Reserved	Reserved, the reset value must be maintained
3	CSBF	Clear STANDBY flags. Always read as 0. 0: Invalid 1: Clear PWR_M4CTRLSTS.SBF and PWR_M4CTRLSTS.VBATF flags.
2	CWKUPF	Clear the pin wakeup bit. Always read as 0.

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Bit field	Name	Description
		0: Invalid 1: Clear the PWR_M4CTRLSTS.WKUPxF wakeup bit after 2 system clock cycles.
1	PDS	Power down deep sleep bit. Cooperates with the LPS bit. 0: When the M4 core outputs DEEPSLEEP as '1', the chip enters standby mode, and the voltage regulator status is controlled by the LPS bit. 1: When the M4 core outputs DEEPSLEEP as '1', the chip enters stop mode.
0	Reserved	Reserved, the reset value must be maintained

3.6.5 PWR M4 Control Status register (PWR_M4CTRLSTS)

This register allows controlling M4 core power.

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					WKUP6F	WKUP5F	WKUP4F	WKUP3F	WKUP2F	WKUP1F	WKUP0F	WKUP5 POL	WKUP4 POL	WKUP3 POL	WKUP2 POL
					r	r	r	r	r	r	r	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP1 POL	WKUP0 POL	WKUP5 EN	WKUP4 EN	WKUP3 EN	WKUP2 EN	WKUP1 EN	WKUP0 EN	Reserved					VBATF	SBF	Reserved
rw	rw	rw	rw	rw	rw	rw	rw						r	r	

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	WKUP6F	RTC wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the RTC alarm
25	WKUP5F	WKUP5 pin PC1 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
24	WKUP4F	WKUP4 pin PI11 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the

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Bit field	Name	Description
		PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
23	WKUP3F	WKUP3 pin PI8 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
22	WKUP2F	WKUP2 pin PC13 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
21	WKUP1F	WKUP1 pin PA2 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
20	WKUP0F	WKUP0 pin PA0 wakeup flag. This bit is set to 1 by hardware and cleared by hardware, by system reset or setting the PWR_M4CTRL1.CWKUPF bit. 0: No wakeup event occurred 1: Wakeup event occurred on the WKUP pin *Note: When the WKUP pin is already at a high level, enabling the WKUP pin for wakeup will detect an additional wakeup event.*
19	WKUP5POL	Wake-up polarity for the WKUP5 pin PC1. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
18	WKUP4POL	Wake-up polarity for the WKUP4 pin PI11. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up

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Bit field	Name	Description
		1: Low level wake-up
17	WKUP3POL	Wake-up polarity for the WKUP3 pin PI8. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
16	WKUP2POL	Wake-up polarity for the WKUP2 pin PC13. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
15	WKUP1POL	Wake-up polarity for the WKUP1 pin PA2. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
14	WKUP0POL	Wake-up polarity for the WKUP0 pin PA0. Use a high level or low level to wake up from standby mode, make sure to disable wake-up enable when changing the wake-up method. 0: High level wake-up 1: Low level wake-up
13	WKUP5EN	WKUP5 pin PC1 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
12	WKUP4EN	WKUP4 pin PI11 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
11	WKUP3EN	WKUP3 pin PI8 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
10	WKUP2EN	WKUP2 pin PC13 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode

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Email: sales@nsing.com.sg

Bit field	Name	Description
		1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
9	WKUP1EN	WKUP1 pin PA2 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
8	WKUP0EN	WKUP0 pin PA0 wakeup enable 0: WKUP pin is a general I/O, events on the WKUP pin cannot wake up the chip from standby mode 1: WKUP pin is used for wakeup from Standby mode and forced in input pull down configuration (rising edge on WKUP pin wakes-up the system from standby mode). *Note: This bit is cleared during system reset.*
7:3	Reserved	Reserved, the reset value must be maintained
2	VBATF	VBAT flag. This bit is set by hardware and cleared by POR/PDR (power-on/power-down reset) or setting the PWR_M4CTRL1.CVBTF bit. 0: M4 core is not in VBAT mode 1: M4 core enters VBAT mode
1	SBF	STANDBY flag. This bit is set by hardware and cleared by POR/PDR (power-on/power-down reset) or by setting the PWR_M4CTRL1.CSBF bit. 0: M4 core is not in standby mode 1: M4 core enters standby mode
0	Reserved	Reserved, the reset value must be maintained.

3.6.6 PWR M4 Control register 2 (PWR_M4CTRL2)

This register allows controlling M4 core power.

Address offset: 0x28

Reset value: 0x7FFF E904

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	MEM_CNTVAL[5:0]						PWR_CNTVAL[7:0]								TCM_RDYMD[1]
	rw						rw								rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RDYMD[0]	PWR_RDYMD[1:0]		HCLK_ONINSLP	NRST_WUPEN	Reserved		RTC_ALMWUPEN	Reserved					BSRSTBRET	BSRVBRET	STOP2EN

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Email: sales@nsing.com.sg

rw rw rw rw rw rw rw rw

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:25	MEM_CNTVAL[5:0]	counter value for memory power ready count down The value written to this field is stored in M4MEM_CNTVAL_reg, with reset value 0. The value read back is M4MEM_CNTVAL + M4TCM_CNTVAL_OTP. M4TCM_CNTVAL_OTP is a 6 bit value loaded from OTP, default 6'b111111. The sum is read back is also used for memory power ready count down. At power-up, M4MEM_CNTVAL = M4TCM_CNTVAL_OTP. After CPU boot-up , user can change the value by writting to this field M4MEM_CNTVAL. If M4TCM_CNTVAL_OTP keeps default value 6'b111111: 6'b000001 6'b000000 6'b000010 6'b000001 …… 6'b111111 6'b111110 If 6'b010000 is programmed to M4TCM_CNTVAL_OTP**:** 6'b000001 6'b010001 6'b000010 6'b010010 …… 6'b111111 6'b001111
24:17	PWR_CNTVAL[7:0]	counter value for CM4 logic power ready count down The value written to this field is stored in PWR_CNTVA, with reset value 0. The value read back is PWR_CNTVAL + M4TCM_CNTVAL_OTP. M4TCM_CNTVAL_OTP is a 6 bit value loaded from OTP, default 8'b11111111. The sum is read back is also used for memory power ready count down. At power-up, PWR_CNTVAL = M4TCM_CNTVAL_OTP. After CPU boot-up , user can change the value by writting to this field PWR_CNTVAL If M4TCM_CNTVAL_OTP keeps default value 8'b11111111: 8'b00000001 8'b00000000 8'b00000010 8'b00000001 …… 8'b11111111 8'b11111110 If M4TCM_CNTVAL_OTP keeps default value 8'b11111111: 8'b00000001 8'b00010001 8'b00000010 8'b00010001 …… 8'b11111111 8'b00001111
16:15	TCM_RDYMD[1:0]	Selected the way of check TCM power ready for CM4 domain 00: check only RDY signal from TCM power switch 01: check Delay after enabled TCM power switch of CM4 domain

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Email: sales@nsing.com.sg

Bit field	Name	Description
		10: Check delay and RDY signal from TCM power switch 11: check delay after RDY signal from TCM power switch
14:13	PWR_RDYMD[1:0]	Selected the way of check power ready for CM4 domain 00: check only RDY signal from power switch 01: check Delay after enabled power switch of CM4 domain 10: Check delay and RDY signal from power switch 11: check delay after RDY signal from power switch
12	HCLK_ONINSLP	1: HCLK is on when M4 core in sleep. 0: HCLK is off when M4 core is in sleep.
11	NRST_WUPEN	NRST wakeup event enable in standby mode for M4 core. 0: NRST event wakeup M4 core is disabled 1: NRST event wakeup M4 core is enabled
10:9	Reserved	Reserved, the reset value must be maintained.
8	RTC_ALMWUPEN	RTC_ALARM wakeup enable in standby mode for M7 core. 0: RTC_ALARM wakeup M4 core is disabled 1: RTC_ALARM wakeup M4 core is enabled
7:3	Reserved	Reserved, the reset value must be maintained.
2	BSRSTBRET	Backup SRAM retention enable in STANDBY mode. 0: Backup SRAM does not retain in STANDBY mode 1: Backup SRAM retains in STANDBY mode
1	BSRVBRET	Backup SRAM retention enable in VBAT mode. 0: Backup SRAM does not retain in VBAT mode 1: Backup SRAM retains in VBAT mode
0	STOP2EN	M4 core STOP2 mode enable. 0: M4 core enters STOP0 mode 1: M4 core enters STOP2 mode

3.6.7 PWR System Control register 1 (PWR_SYSCTRL1)

Address offset: 0x40

Reset value: 0x0000 B801

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCDC_VSELKEY[3:0]				NRST_DGFCNT[11:0]											
rw				rw											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NRST_DGFBP	Reserved	AGF_STBWUPPBP	AGF_DTASGBP	AGF_ARSTOBP	Reserved		DBKP	Reserved			PVDEN	AVDEN	Reserved	SW3EN	BKPLDOEN
rw		rw	rw	rw			rw				rw	rw		rw	rw

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Bit field	Name	Description
31:28	DCDC_VSELKEY	DCDC_VSELKEY_UNLOCK key. If DCDC_VSELKEY = 4'hF, DCDC_VSELKEY_UNLOCK=1; else DCDC_VSELKEY_UNLOCK=0;
27:16	NRST_DGFCNT	Digtal Glitch Filter on NRST filtered pulse width configuration.
15	NRST_DGFBP	Bypass digital glitch Filter on NRST. 0: Enable digtal glitch Filter on NRST. 1: Bypass digital glitch Filter on NRST.
14	Reserved	Reserved, the reset value must be maintained.
13	AGF_STBWUPPBP	Bypass analog glitch filter on stanby wakeup pads 0: Enable analog glitch filter on stanby wakeup pads. 1: Bypass analog glitch filter on stanby wakeup pads.
12	AGF_DTASGBP	Bypass analog glitch filter on some (e.g Reset) Digtal to Analog Enable singnals 0: Enable analog glitch filter on someDigtal to Analog Enable singnals. 1: Bypass analog glitch filter on some Digtal to Analog Enable singnals.
11	AGF_ARSTOBP	Bypass analog glitch filter on Analog Reset outputs. 0: Enable analog glitch filter on Analog Reset outputs. 1: Bypass analog glitch filter on Analog Reset outputs.
10:9	Reserved	Reserved, the reset value must be maintained.
8	DBKP	Disable write protection for the backup domain. In the reset state, the RTC and backup domain registers are protected to prevent unauthorized writes. This bit must be set to enable write access to these registers. 0: Disable access to RTC and backup registers 1: Enable access to RTC and backup registers *Note: If the RTC clock is HSE/128, this bit must remain set to 1.*
7:5	Reserved	Reserved, the reset value must be maintained.
4	PVDEN	Power Voltage Detector (PVD) Enable. This bit is set and cleared by software. 0: Disable PVD 1: Enable PVD
3	AVDEN	Anolog Voltage Detector (AVD) Enable. This bit is set and cleared by software. 0: Disable AVD 1: Enable AVD
2	Reserved	Reserved, the reset value must be maintained.
1	SW3_SWEN	VDDD Backup from Backup LDO. 0: PWR hardware control SW3 1: force VDDDBK supply from BKP LDO. For debug
0	BKPLDOEN	Backup LDO enable: 0: Disable backup LDO 1: Enable backup LDO

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3.6.8 PWR System Control Status register (PWR_SYSCTRLSTS)

Address offset: 0x44

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											PWDO	AWDO	Reserved	OTP_ PWRRDY	DCDC_ BPF
											r	r		r	r

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	PVDO	PVD output. This bit is only valid when PVD is enabled by the PWR_SYSCTRL1.PVDEN bit. 0: VDD is higher than the PVD threshold selected by AFEC_PVD_CFG[3:0] 1: VDD is lower than the PVD threshold selected by AFEC_PVD_CFG[3:0] *Note: PVD is stopped in standby mode. Therefore, after standby mode or reset, this bit remains 0 until the PWR_SYSCTRL1.PVDEN bit is set.*
3	AVDO	AVD output. This bit is only valid when AVD is enabled by the PWR_SYSCTRL1.AVDEN bit. 0: VDDA is equal or higher than the AVD threshold selected with the AFEC_AVD_CFG[3:0] bits 1: VDDA is lower than the AVD threshold selected with the AFEC_AVD_CFG[3:0] bits *Note: PVD is stopped in standby mode. Therefore, after standby mode or reset, this bit remains 0 until the PWR_SYSCTRL1.AVDEN bit is set.*
2	Reserved	Reserved, the reset value must be maintained.
1	OTP_PWRRDY	OTP Power Ready This bit is set to 1 by hardware. 0: Not Ready; 1: Ready.
0	DCDC_BPF	Working mode is bypass or not for DCDC. This bit is set to 1 by hardware. 0: DCDC is not operating in bypass mode 1: DCDC is operating in bypass mode

3.6.9 PWR System Control register 2(PWR_SYSCTRL2)

Address offset: 0x48

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Reset value: 0x0001 07F2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					OTP_LPCLKDIV[2:0]			OTP_FRCSTB	OTP_FRCDSTB	OTP_STB_INSTP0	OTP_DSTB_INSTP0	OTP_STB_INSTP2	OTP_DSTB_INSTP2	EXTI_MASKRSTEN	VDDDM_RDYMD
						rw		rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				BKPLDO_CTRLEN	Reserved									MR_STBOFFEN	Reserved
				rw										rw	

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:24	OTP_LPCLKDIV	Clock dividor of pwr_sys_clk for OTP low power mode cotrol. 0: No division 1: divded by 2; 2: divided by 3; … 7: divided by 8. The divisor value must gurantee the divided clock frequcy not larger than 48MHz. E.g. when frequency of pwr_sys_clk is 300MHz, the divisor value should be 6 or 7.
23: 22	OTP_FRCSTB and OTP_FRCDSTB	OTP_FRCSTB and OTP_FRCDSTB decide the OTP power state in all system power modes. 00: OTP in normal mode (OTP power stated decided by OTP_STB_INSTP0, 01/11: OTP forced to DSTBY by software in RUN mode. 10: OTP forced to STBY by software in RUN mode. OTP_DSTB_INSTP0 or OTP_DSTB_INSTP2 or OTP_STB_INSTP2) After the OTP_FRCDSTB asserted, OTP stay in Deep Standby mode until OTP_FRCDSTB cleared to 0 by software.
21: 20	OTP_STB_INSTP0 and OTP_DSTB_INSTP0	OTP_STB_INSTP0 and OTP_DSTB_INSTP0 decide the OTP power state in system STOP0 mode. These bits will take effecte when {OTP_FRCSTB, OTP_FRCDSTB} = 2'b00; 00: OTP in normal mode 01/11: OTP keep in DSTBY mode in stop0 mode 10 : OTP enter STBY in stop0 mode. OTP Wakeup from Standby mode automatically after system wakeup from STP0 mode.
19:18	OTP_STB_INSTP2 and OTP_DSTB_INSTP2	OTP_STB_INSTP2 and OTP_DSTB_INSTP2 decide the OTP power state in system STOP2 mode. These bits will take effecte when {OTP_FRCSTB, OTP_DFRCSTB} = 2'b00; 00: OTP in normal mode 01/11: OTP keep in DSTBY mode in stop2 mode. 10: OTP enter STBY in stop2 mode.
17	EXTI_MASKRSTEN	0: When PWR start to power down CPUn to standby mode, EXTI can still issue

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Bit field	Name	Description
		interrupt to CPUn if system is still in RUN mode. 1: When PWR start to power down CPUn to standby mode, EXTI's IMRn/EMRn register will be reset and no interrupt/event will be send to CPU from EXTI
16	VDDDM_RDYMD	0: PWR use delay after dpts4 enable +2LSI cycle as main domain ready 1: PWR use dpts4 rdy(feedback from power switch chain) + 2cycle LSI delay as main domain ready
15:12	Reserved	Reserved, the reset value must be maintained.
11	BKPLDO_CTRLEN	This bit together with PWR_SYSCTRL1.BKPLDOEN and PWR_SYSCTRL2.MR_STBOFFEN determines the eanble/disable of BKLDO When PWR_SYSCTRL1.BKPLDOEN =1, it forces the ALDO on. When PWR_SYSCTRL1.BKPLDOEN =0: BKPLDO_CTRLEN =0: BKLDO is on in system RUN mode; BKPLDO_CTRLEN =1: BKLDO is off in system RUN mode; If PWR_SYSCTRL2.MR_STBOFFEN =0, BKPLDO_CTRLEN =0: BKLDO stays on in system Standby mode; BKPLDO_CTRLEN =1: BKLDO stays off in system Standby mode; If PWR_SYSCTRL2.MR_STBOFFEN =1, BKLDO is switched on and VDDDBK switch back to BKLDO before enter system Standby mode; Note: this bit should **not** be set if VBAT mode is requried in a certain application.
10:2	Reserved	Reserved, the reset value must be maintained.
1	MR_STBOFFEN	MR off enable or not when system enters into Standby mode 0: MR is on when system enters into Standby mode. 1: MR is off when system enters into Standby mode.
0	Reserved	Reserved, the reset value must be maintained.

3.6.10 PWR System Control register 3(PWR_SYSCTRL3)

Address offset: 0x4C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									HSC2_PSWACK1	HSC1_PSWACK1	GRC_PSWACK1	Reserved	HSC2_PWRRDY	HSC1_PWRRDY	GRC_PWRRDY
									rw	rw	rw		r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					HSC2_ISNEN	HSC1_ISNEN	GRC_ISNEN	Reserved	HSC2_FUCEN	HSC1_FUCEN	GRC_FUCEN	Reserved	HSC2_PGEN	HSC1_PGEN	GRC_PGEN
					rw	rw	rw		rw	rw	rw		rw	rw	rw

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
22	HSC2_PSWACK1	0: ACK1 delayed as ENA2; 1: HSC2 Domain power switch ACK1 used as ENA2 for dual-input-header;
21	HSC1_PSWACK1	0: ACK1 delayed as ENA2; 1: HSC1 Domain power switch ACK1 used as ENA2 for dual-input-header;
20	GRC_PSWACK1	0: ACK1 delayed as ENA2; 1: GRAPHIC Domain power switch ACK1 used as ENA2 for dual-input-header;
19	Reserved	Reserved, the reset value must be maintained.
18	HSC2_PWRRDY	HSC2 power domain ready flag. 0: HSC2 power domain is not ready; 1: HSC2 power domain is ready.
17	HSC1_PWRRDY	HSC1 power domain ready flag. 0: HSC1 power domain is not ready; 1: HSC1 power domain is ready.
16	GRC_PWRRDY	GRAPHIC power domain ready flag. 0: GRAPHIC power domain is not ready; 1: GRAPHIC power domain is ready.
15:11	Reserved	Reserved, the reset value must be maintained.
10	HSC2_ISNEN	HSC2 power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
9	HSC1_ISNEN	HSC1 power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
8	GRC_ISNEN	GRAPHIC power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
7	Reserved	Reserved, the reset value must be maintained.
6	HSC2_FUCEN	Function mode enable for HSC2 domain; 0: Disable 1: Enable
5	HSC1_FUCEN	Function mode enable for HSC1 domain; 0: Disable 1: Enable
4	GRC_FUCEN	Function mode enable for GRPAHIC; 0: Disable 1: Enable
3	Reserved	Reserved, the reset value must be maintained.
2	HSC2_PGEN	HSC2 domain power enable; 0: Disable 1: Enable
1	HSC1_PGEN	HSC1 domain power enable;

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Bit field	Name	Description
		0: Disable 1: Enable
0	GRC_PGEN	GRPAHIC domain power enable; 0: Disable 1: Enable

3.6.11 PWR System Control register 4(PWR_SYSCTRL4)

Address offset: 0x50

Reset value: 0x070E 0206

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		MR_LP VSELEN	Reserved	DCDC_LPVSEL[3:0]				VDDD_ LPPORSEL[1:0]		DCDC_LPPORVSEL[3:0]					BG_LPVR EFVSEL
		rw		rw				rw				rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BG_VREF VSEL	Reserved	VDDD_PORSEL[1:0]		MLDO_LPO VSEL[1:0]		MLDO_OVSEL[1:0]		Reserved				DCDC FRCEN	DCDCEN	MLDOEN	VCORE SRC
rw		rw		rw		rw						rw	rw	rw	rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	MR_LPVSELEN	Enable targeting MR voltage output in low power mode 0: Disable 1: Enable
28	Reserved	Reserved, the reset value must be maintained.
27:24	DCDC_LPVSEL[3:0]	Targeting dcdc voltage in low power mode, valid only when MR_LPVSELEN = 1 DCDC output voltage value in 0.05V per step 0101: 0.80V 0110: 0.85V 0111: 0.90V *Note:When DCDC_VSEL_LMT_UNLOCK=0, configures above 1.00V will be limited to 1.00V(VSEL=b1001).*
23:22	VDDD_LPPOR SEL[1:0]	VDDD POR config in low power mode. 00: POR is 0.7V, PDR is 0.65V 01: POR is 0.7V, PDR is 0.65V 10: POR is 0.75V, PDR is 0.7V 11: POR is 0.8V, PDR is 0.75V
21:17	DCDC_LPPOR VSEL[4:0]	DCDC POR voltage value 0.05V per step in low power mode, valid only when MR_LPVSELEN = 1 00101: 0.8V 00110: 0.85V

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Bit field	Name	Description
		00111: 0.9V
16	BG_LPVREF VSEL	targeting ALDO ref in low power mode, valid only when MR_LPVSELEN = 1 0: The voltage of BG is 0.9v 1: The voltage of BG is 0.8v
15	BG_VREF VSEL	0: The voltage of BG is 0.9v 1: The voltage of BG is 0.8v
14	Reserved	Reserved, the reset value must be maintained.
13:12	VDDD_POR SEL[1:0]	VDDD por config in low power mode. 00: POR is 0.7V, PDR is 0.65V 10: POR is 0.75V, PDR is 0.7V 11: POR is 0.8V, PDR is 0.75V
11:10	MLDO_LPO VSEL[1:0]	Output voltage of Main Regulator LDO option in SYS STOP2 and STANDBY mode: 00: 0.8V 01: 0.85V 10: 0.9V 11: 0.9V
9:8	MLDO_OVSEL[1:0]	Output voltage of Main Regulator LDO option in SYS RUN mode: 00: 0.8V 01: 0.85V 10:0.9V 11:0.9V
7:4	Reserved	Reserved, the reset value must be maintained.
3	DCDCFRCEN	0: DCDC in standard operational mode. 1: DCDC is forcibly activated, to supply external circuit. Independent of system power mode.
2	DCDCEN	0: DCDC is deactivated; 1: DCDC is activated;
1	MLDOEN	0: LDO is deactivated; 1: LDO is activated;
0	VCORESRC	1: VCORE/VDDD spupplied by external source 0: VCORE supplied by DCDC or LDO

3.6.12 PWR IP Memory Control register (PWR_IPMEMCTRL)

Address offset: 0x58

Reset value: 0x0000 1FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	ESC_PGEN	FMAC_PGEN	SDMMC1 PGEN	USB1_PGEN	EHT1_PGEN	SDMMC2 PGEN	USB2_PGEN	ETH2_PGEN	DVP_PGEN	DSI_PGEN	JPEG_PGEN	LCDC_PGEN	GPU_PGEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ESC_PGEN	ESC memory power gate enable 0: Power on 1: Power down
11	FMAC_PGEN	FMAC memory power gate enable 0: Power on 1: Power down
10	SDMMC1_PGEN	SDMMC1 memory power gate enable 0: Power on 1: Power down
9	USB1_PGEN	USB1 memory power gate enable 0: Power on 1: Power down
8	ETH1_PGEN	ETH1 memory power gate enable 0: Power on 1: Power down
7	SDMMC2_PGEN	SDMMC2 memory power gate enable 0: Power on 1: Power down
6	USB2_PGEN	USB2 memory power gate enable 0: Power on 1: Power down
5	ETH2_PGEN	EHT2 memory power gate enable 0: Power on 1: Power down
4	DVP_PGEN	DVP memory power gate enable 0: Power on 1: Power down
3	DSI_PGEN	DSI memory power gate enable 0: Power on 1: Power down
2	JPEG_PGEN	JPEG memory power gate enable 0: Power on 1: Power down
1	LCDC_PGEN	LCDC memory power gate enable 0: Power on 1: Power down

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Bit field	Name	Description
0	GPU_PGEN	GPU memory power gate enable 0: Power on 1: Power down

3.6.13 PWR IP Memory Status register (PWR_IPMEMSTS)

Address offset: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ESC_PRDY	FMAC_PRDY	SDMMC1_PRDY	USB1_PRDY	EHT1_PRDY	SDMMC2_PRDY	USB2_PRDY	ETH2_PRDY	DVP_PRDY	DSI_PRDY	JPEG_PRDY	LCDC_PRDY	GPU_PRDY
			r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31	ALLIP_PRDY	ALL IP memory power ready flag
30:13	Reserved	Reserved, the reset value must be maintained.
12	ESC_PRDY	ESC memory power ready flag
11	FMAC_PRDY	FMAC memory power ready flag
10	SDMMC1_PRDY	SDMMC1 memory power ready flag
9	USB1_PRDY	USB1 memory power ready flag
8	ETH1_PRDY	ETH1 memory power ready flag
7	SDMMC2_PRDY	SDMMC2 memory power ready flag
6	USB2_PRDY	USB2 memory power ready flag
5	ETH2_PRDY	EHT2 memory power ready flag
4	DVP_PRDY	DVP memory power ready flag
3	DSI_PRDY	DSI memory power ready flag
2	JPEG_PRDY	JPEG memory power ready flag
1	LCDC_PRDY	LCDC memory power ready flag
0	GPU_PRDY	GPU memory power ready flag

3.6.14 PWR CM7 Memory Low Power Control register (PWR_M7MEMLPCTRL)

Address offset: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MEM_PWGCFG[1:0]		MEM_RETSTP0EN	MEM_PGSTP0EN
												rw		rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:2	MEM_PGCFG	Memory power gate sequence control 00: all cm7 memories in one daisy chain 01: D-cache->I-cache->TCM daisy , parallel within dcache, icache, serial chain of TCM 10: D-cache + I-cache ->every 4 pieces of TCM memory(64 pieces in total) parallel. 11: all memory in one daisy chain
1:0	MEM_RETSTP0EN and MEM_PGSTP0EN	00: all cm7 memory in Chip disable mode. 01: all cm7 memory in Precharge mode. 10: Reserved 11: all cm7 memories in Retention 1 mode.

3.6.15 PWR CM7 Memory Low Power Status register (PWR_M7MEMLPSTS)

Address offset: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCMRDY	Reserved														
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31	TCMRDY	All enabled TCM memory power ready flag
30:0	Reserved	Reserved, the reset value must be maintained.

3.6.16 PWR CM7 TCM Part0 Program register (PWR_M7TCMPG0)

Address offset: 0x68

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_PG0[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_PG0[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	TCM_PG0[31:0]	Software control to power gate TCM Part0 memories. 0: PWR hardware controls TCM SRAM[i]; 1: TCM SRAM[i] is power gated. To Enalbe the SRAM again after it is power gated by sotware, Software should To Enalbe the SRAM again after it is power gated by sotware, Software should configure the corresponding bit to '0' again. If there are more than one pieces of SRAMS need to be enaled/disabled, the corresponding bits must be programmed once a bit. There should be only one bit change value within each write operation to this register. Bus address Map of TCM SRAMS: TCM_PG0[0]: 0x2000 0000 – 0x2000 3FFF TCM_PG0[1]: 0x2000 4000 – 0x2000 7FFF …. TCM_PG0[31]: 0x2007 FBFF – 0x2007 FFFF

3.6.17 PWR CM7 TCM Part1 Program register (PWR_M7TCMPG1)

Address offset: 0x6C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_PG1[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_PG1[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	TCM_PG1[31:0]	Software control to power gate TCM Part1 memories. 0: PWR hardware controls TCM SRAM[i+32]; 1: TCM SRAM[i+32] is power gated.

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Bit field	Name	Description
		To Enalbe the SRAM again after it is power gated by sotware, Software should To Enalbe the SRAM again after it is power gated by sotware, Software should configure the corresponding bit to '0' again. If there are more than one pieces of SRAMS need to be enaled/disabled, the corresponding bits must be programmed once a bit. There should be only one bit change value within each write operation to this register. Bus address Map of TCM SRAMS:TCM_PG1[0]: 0x2008 0000 – 0x2008 3FFF TCM_PG1[1]: 0x2008 4000 – 0x2008 7FFF …. TCM_PG1[31]: 0x200F FBFF – 0x200F FFFF

3.6.18 PWR CM7 TCM Part0 Rentain 1 register (PWR_M7TCMRET1N0)

Address offset: 0x70

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_RENT1N0[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RENT1N0[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	TCM_RENT1N0[31:0]	memory status depends on { TCM_RENT1Nx, TCM_RENT2Nx } 00: CM7 TCM memory enter Power Down mode when entering STOP2 01/11: CM7 TCM memory enter Retention mode 1 when entering STOP2 10: CM7 TCM memory enter Retention mode 2 when entering STOP2

3.6.19 PWR CM7 TCM Part1 Rentain 1 register (PWR_M7TCMRET1N1)

Address offset: 0x74

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_RENT1N1[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RENT1N1[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:0	TCM_RENT1 N1[31:0]	memory status depends on { TCM_RENT1Nx, TCM_RENT2Nx } 00: CM7 TCM memory enter Power Down mode when entering STOP2 01/11: CM7 TCM memory enter Retention mode 1 when entering STOP2 10: CM7 TCM memory enter Retention mode 2 when entering STOP2

3.6.20 PWR CM7 TCM Part0 Rentain 2 register (PWR_M7TCMRET2N0)

Address offset: 0x78

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_RENT2N0[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RENT2N0[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	TCM_RENT2 N0[31:0]	memory status depends on { TCM_RENT1Nx, TCM_RENT2Nx } 00: CM7 TCM memory enter Power Down mode when entering STOP2 01/11: CM7 TCM memory enter Retention mode 1 when entering STOP2 10: CM7 TCM memory enter Retention mode 2 when entering STOP2

3.6.21 PWR CM7 TCM Part1 Rentain 2 register (PWR_M7TCMRET2N1)

Address offset: 0x7C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_RENT2N1[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RENT2N1[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:0	TCM_RENT2N1[31:0]	memory status depends on { TCM_RENT1Nx, TCM_RENT2Nx } 00: CM7 TCM memory enter Power Down mode when entering STOP2 01/11: CM7 TCM memory enter Retention mode 1 when entering STOP2 10: CM7 TCM memory enter Retention mode 2 when entering STOP2

3.6.22 PWR CM7 TCM Part0 Power Ready register (PWR_M7TCMRDY0)

Address offset: 0x80

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_RDY[31:16]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RDY[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31:0	TCM_RDY[31:0]	0: TCM power is not ready; 1: TCM power is ready;

3.6.23 PWR CM7 TCM Part1 Power Ready register (PWR_M7TCMRDY1)

Address offset: 0x84

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCM_RDY[31:16]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCM_RDY[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31:0	TCM_RDY[31:0]	0: TCM power is not ready; 1: TCM power is ready;

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3.6.24 PWR CM4 Memory Low Power Control register (PWR_M4MEMLPCTRL)

Address offset: 0x90

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MEM_PWGCFG[1:0]		MEM_PGSTP0EN	MEM_RETSTP0EN
												rw		rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:2	MEM_PGCFG	Memory power gate sequence control 00: all cm4 memories in one daisy chain 01: all memory parallel 10: D-cache -> I-cache, parallel within each group. 11: all memory in one daisy chain
1:0	MEM_PGSTP0EN and MEM_RETSTP0EN	00: all cm4 memory in Chip disable mode. 01: all cm4 memory in Precharge mode. 10: Reserved 11: all cm4 memories in Retention 1 mode.

3.6.25 PWR System Memory Low Power Control register (PWR_SYSMEMLPCTRL)

Address offset: 0xA0

Reset value: 0x02AA A100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRDY	Reserved				AHBSRM5S2_RET2N	AHBSRM5S2_RET1N	AHBSRM5S1_RET2N	AHBSRM5S1_RET1N	AHBSRM4_RET2N	AHBSRM4_RET1N	AHBSRM3_RET2N	AHBSRM3_RET1N	AHBSRM2_RET2N	AHBSRM2_RET1N	AHBSRM1_RET2N
rw					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AHBSRM1_RET1N	AXISRM_RET2N	AXISRM_RET1N	Reserved			MEM_RETSTP0EN	MEM_PGSTP0EN	Reserved	AHBSRM5S2_PG	AHBSRM5S1_PG	AHBSRM4_PG	AHBSRM3_PG	AHBSRM2_PG	AHBSRM1_PG	AXISRM_PG
rw	rw	rw				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31	PRDY	All enabled system memory power ready flag.
30:27	Reserved	Reserved, the reset value must be maintained.
26:25	AHBSRM5S2_ RET2N and AHBSRM5S2_ RET1N	System SRAM5S2 memory status depends on { AHBSRM5S2_RET2N , AHBSRM5S2_RET1N } 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
24:23	AHBSRM5S1_ RET2N and AHBSRM5S1_ RET1N	System SRAM5S1 memory status depends on { AHBSRM5S1_RET2N , AHBSRM5S1_RET1N } 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
22:21	AHBSRM4_RET2N and AHBSRM4_RET1N	System SRAM4 memory status depends on { AHBSRM4_RET2N , AHBSRM4_RET1N } 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
20:19	AHBSRM3_RET2N and AHBSRM3_RET1N	System SRAM3 memory status depends on { AHBSRM3_RET2N , AHBSRM3_RET1N } 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
18:17	AHBSRM2_RET2N and AHBSRM2_RET1N	System SRAM2 memory status depends on { AHBSRM2_RET2N , AHBSRM2_RET1N } 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
16:15	AHBSRM1_RET2N and AHBSRM1_RET1N	System SRAM1 memory status depends on { AHBSRM1_RET2N , AHBSRM1_RET1N} 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
14:13	AXISRM_RET2N and AXISRM_RET1N	System memory status depends on { AXISRM_RET2N , AXISRM_RET1N } 00: System memory enter Power Down mode when entering STOP2 01/11: System memory enter Retention mode 1 when entering STOP2 10: System memory enter Retention mode 2 when entering STOP2
12:10	Reserved	Reserved, the reset value must be maintained.
9:8	MEM_RETSTP0EN and MEM_PGSTP0EN	00: all system memory in Chip disable mode. 01: Reserved. 10: all system memory in Precharge mode 11: all system memories in Retention 1 mode.

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Bit field	Name	Description
7	Reserved	Reserved, the reset value must be maintained.
6	AHBSRM5S2_PG	Software control to power gate AHB SRAM5S2 in SYS RUN mode 0: AHBSRAM5S2 power on 1: AHBSRAM5S2 power off
5	AHBSRM5S1_PG	Software control to power gate AHB SRAM5S1 in SYS RUN mode 0: AHBSRAM5S1 power on 1: AHBSRAM5S1 power off
4	AHBSRM4_PG	Software control to power gate AHB SRAM4 in SYS RUN mode 0: AHBSRAM4 power on 1: AHBSRAM4 power off
3	AHBSRM3_PG	Software control to power gate AHB SRAM3 in SYS RUN mode 0: AHBSRAM3 power on 1: AHBSRAM3 power off
2	AHBSRM2_PG	Software control to power gate AHB SRAM2 in SYS RUN mode 0: AHBSRAM2 power on 1: AHBSRAM2 power off
1	AHBSRM1_PG	Software control to power gate AHB SRAM1 in SYS RUN mode 0: AHBSRAM1 power on 1: AHBSRAM1 power off
0	AXISRM_PG	Software control to power gate AXI SRAM in SYS RUN mode 0: AXISRAM1 power on 1: AXISRAM1 power off

3.6.26 PWR System SHRTIM Power Control register (PWR_SHRTIMCTRL)

Address offset: 0xB0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											SHRA_PSWACK1	SHRA_PRDY	SHRA_ISNEN	SHRA_FUCEN	SHRA_PGEN
											rw	r	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			SHR2_PSWACK1	SHR2_PRDY	SHR2_ISNEN	SHR2_FUCEN	SHR2_PGEN	Reserved			SHR1_PSWACK1	SHR1_PRDY	SHR1_ISNEN	SHR1_FUCEN	SHR1_PGEN
			rw	r	rw	rw	rw				rw	r	rw	rw	rw

Bit field	Name	Description
30:21	Reserved	Reserved, the reset value must be maintained.
20	SHRA_PSWACK1	0: SHRTIM AFE delayed as ENA2; 1: SHRTIM AFE Domain power switch ACK1 used as ENA2 for dual-input-header;
19	SHRA_PWRRDY	SHRTIM AFE power domain ready flag.

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Bit field	Name	Description
		0: SHRTIM AFE power domain is not ready; 1: SHRTIM AFE power domain is ready.
18	SHRA_ISNEN	SHRTIM AFE power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
17	SHRA_FUCEN	Function mode enable for SHRTIM AFE; 0: Disable 1: Enable
16	SHRA_PGEN	SHRTIM AFE power gate enable 0: Power down 1: Power on
15:13	Reserved	Reserved, the reset value must be maintained.
12	SHR2_PSWACK1	0: SHRTIM2 delayed as ENA2; 1: SHRTIM2 Domain power switch ACK1 used as ENA2 for dual-input-header;
11	SHR2_PWRRDY	SHRTIM2 power domain ready flag. 0: SHRTIM2 power domain is not ready; 1: SHRTIM2 power domain is ready.
10	SHR2_ISNEN	SHRTIM2 power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
9	SHR2_FUCEN	Function mode enable for SHRTIM2; 0: Disable 1: Enable
8	SHR2_PGEN	SHRTIM2 power gate enable 0: Power down 1: Power on
7:5	Reserved	Reserved, the reset value must be maintained.
4	SHR1_PSWACK1	0: SHRTIM1 delayed as ENA2; 1: SHRTIM1 Domain power switch ACK1 used as ENA2 for dual-input-header;
3	SHR1_PWRRDY	SHRTIM1 power domain ready flag. 0: SHRTIM1 power domain is not ready; 1: SHRTIM1 power domain is ready.
2	SHR1_ISNEN	SHRTIM1 power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
1	SHR1_FUCEN	Function mode enable for SHRTIM1; 0: Disable 1: Enable
0	SHR1_PGEN	SHRTIM1 power gate enable 0: Power down 1: Power on

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3.6.27 PWR System MDMA Power Control register (PWR_MDMACTRL)

Address offset: 0xB4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											MDMA_PSWACK1	MDMA_PRDY	MDMA_ISNEN	MDMA_FUCEN	MDMA_PGEN
											rw	r	rw	rw	rw

Bit Field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	MDMA_PSWACK1	0: MDMA delayed as ENA2; 1: MDMA Domain power switch ACK1 used as ENA2 for dual-input-header;
3	MDMA_PWRRDY	MDMA power domain ready flag. 0: MDMA power domain is not ready; 1: MDMA power domain is ready.
2	MDMA_ISNEN	MDMA power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
1	MDMA_FUCEN	Function mode enable for MDMA; 0: Disable 1: Enable
0	MDMA_PGEN	MDMA power gate enable 0: Power down 1: Power on

3.6.28 PWR System ESC Power Control register (PWR_ESCCTRL)

Address offset: 0xB8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											ESC_PSWACK1	ESC_PRDY	ESC_ISNEN	ESC_FUCEN	ESC_PGEN

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		rw	r	rw	rw	rw

Bit Field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	ESC_PSWACK1	0: ESC delayed as ENA2; 1: ESC Domain power switch ACK1 used as ENA2 for dual-input-header;
3	ESC_PWRRDY	ESC power domain ready flag. 0: ESC power domain is not ready; 1: ESC power domain is ready.
2	ESC_ISNEN	ESC power domain isolation signal 0: Disable: Signal Isolated. 1: Enable: Signal pass through
1	ESC_FUCEN	Function mode enable for ESC; 0: Disable 1: Enable
0	ESC_PGEN	ESC power gate enable 0: Power down 1: Power on

3.6.29 PWR EMC RET Control Register 1 (PWR_EMCRETCTRL1)

Address offset: 0x100

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RETGB3 DET	RETGB2 DET	RETGB1 DET	RETGB0 DET	RETGBN3 DET	RETGBN2 DET	RETGBN1 DET	RETGBN0 DET	RETCLP3 DET	RETCLP2 DET	RETCLP1 DET	RETCLP0 DET
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	RETGB3DET	RET domain EMC GB3 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
10	RETGB2DET	RET domain EMC GB2 detection enable This bit is set and cleared by software. 0: Disable detection

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		1: Enable detection
9	RETGB1DET	RET domain EMC GB1 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
8	RETGB0DET	RET domain EMC GB0 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
7	RETGBN3DET	RET domain EMC GBN3 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
6	RETGBN2DET	RET domain EMC GBN2 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
5	RETGBN1DET	RET domain EMC GBN1 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
4	RETGBN0DET	RET domain EMC GBN0 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
3	RETCLP3DET	RET domain EMC Clamp3 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
2	RETCLP2DET	RET domain EMC Clamp2 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
1	RETCLP1DET	RET domain EMC Clamp1 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
0	RETCLP0DET	RET domain EMC Clamp0 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection

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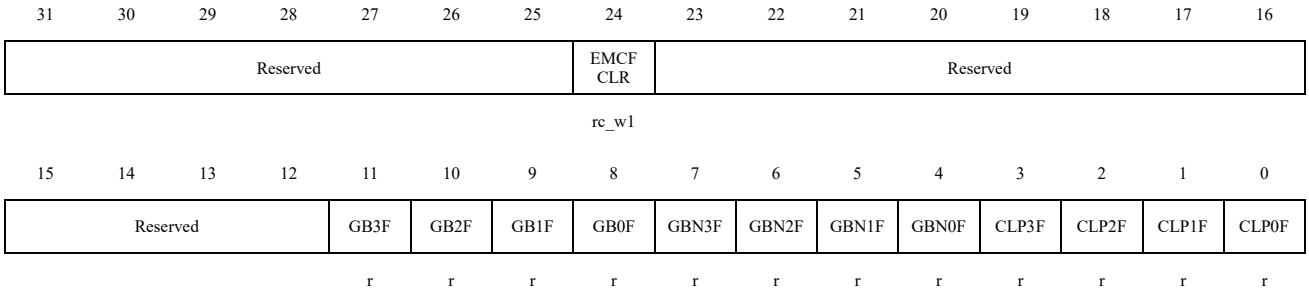
3.6.30 PWR EMC RET Status Register 1 (PWR_EMCRETSTS1)

Address offset: 0x104

Reset value: 0x0000 0000



Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	EMCFCLR	Clear EMC Flag: 0: No effect 1: Clear EMC flag
23:12	Reserved	Reserved, the reset value must be maintained.
11	GB3F	RET Domain EMC GB3 Flag: When the RET domain detects an EMC GB3 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB3 event 1: EMC GB3 event occurred
10	GB2F	RET Domain EMC GB2 Flag: When the RET domain detects an EMC GB2 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB2 event 1: EMC GB2 event occurred
9	GB1F	RET Domain EMC GB1 Flag: When the RET domain detects an EMC GB1 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB1 event 1: EMC GB1 event occurred
8	GB0F	RET Domain EMC GB0 Flag: When the RET domain detects an EMC GB0 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB0 event 1: EMC GB0 event occurred
7	GBN3F	RET Domain EMC GBN3 Flag: When the RET domain detects an EMC GBN3 event, this bit is set by the

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		hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN3 event 1: EMC GBN3 event occurred
6	GBN2F	RET Domain EMC GBN2 Flag: When the RET domain detects an EMC GBN2 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN2 event 1: EMC GBN2 event occurred
5	GBN1F	RET Domain EMC GBN1 Flag: When the RET domain detects an EMC GBN1 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN1 event 1: EMC GBN1 event occurred
4	GBN0F	RET Domain EMC GBN0 Flag: When the RET Domain detects an EMC GBN0 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN0 event 1: EMC GBN0 event occurred
3	CLP3F	RET Domain EMC Clamp3 Flag: When the RET domain detects an EMC Clamp3 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp3 event 1: EMC Clamp3 event occurred
2	CLP2F	RET Domain EMC Clamp2 Flag: When the RET domain detects an EMC Clamp2 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp2 event 1: EMC Clamp2 event occurred
1	CLP1F	RET Domain EMC Clamp1 Flag: When the RET domain detects an EMC Clamp1 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp1 event 1: EMC Clamp1 event occurred
0	CLP0F	RET Domain EMC Clamp0 Flag: When the RET domain detects an EMC Clamp0 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp0 event 1: EMC Clamp0 event occurred

3.6.31 PWR EMC RET Control Register 2 (PWR_EMCRETCTRL2)

Address offset: 0x108

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RETGB7DET	RETGB6DET	RETGB5DET	RETGB4DET	RETGBN7DET	RETGBN6DET	RETGBN5DET	RETGBN4DET	RETCLP7DET	RETCLP6DET	RETCLP5DET	RETCLP4DET
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	RETGB7DET	RET domain EMC GB7 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
10	RETGB6DET	RET domain EMC GB6 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
9	RETGB5DET	RET domain EMC GB5 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
8	RETGB4DET	RET domain EMC GB4 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
7	RETGBN7DET	RET domain EMC GBN7 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
6	RETGBN6DET	RET domain EMC GBN6 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
5	RETGBN5DET	RET domain EMC GBN5 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
4	RETGBN4DET	RET domain EMC GBN4 detection enable This bit is set and cleared by software. 0: Disable detection

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		1: Enable detection
3	RETCLP7DET	RET domain EMC Clamp7 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
2	RETCLP6DET	RET domain EMC Clamp6 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
1	RETCLP5DET	RET domain EMC Clamp5 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
0	RETCLP4DET	RET domain EMC Clamp4 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection

3.6.32 PWR EMC RET Status Register 2 (PWR_EMCRETSTS2)

Address offset: 0x10C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				GB7F	GB6F	GB5F	GB4F	GBN7F	GBN6F	GBN5F	GBN4F	CLP7F	CLP6F	CLP5F	CLP4F
				r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	GB7F	RET Domain EMC GB7 Flag: When the RET domain detects an EMC GB7 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB7 event 1: EMC GB7 event occurred
10	GB6F	RET Domain EMC GB6 Flag: When the RET domain detects an EMC GB6 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB6 event

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		1: EMC GB6 event occurred
9	GB5F	RET Domain EMC GB5 Flag: When the RET domain detects an EMC GB5 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB5 event 1: EMC GB5 event occurred
8	GB4F	RET Domain EMC GB4 Flag: When the RET domain detects an EMC GB4 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB4 event 1: EMC GB4 event occurred
7	GBN7F	RET Domain EMC GBN7 Flag: When the RET domain detects an EMC GBN7 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN7 event 1: EMC GBN7 event occurred
6	GBN6F	RET Domain EMC GBN6 Flag: When the RET domain detects an EMC GBN6 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN6 event 1: EMC GBN6 event occurred
5	GBN5F	RET Domain EMC GBN5 Flag: When the RET domain detects an EMC GBN5 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN5 event 1: EMC GBN5 event occurred
4	GBN4F	RET Domain EMC GBN4 Flag: When the RET Domain detects an EMC GBN4 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN4 event 1: EMC GBN4 event occurred
3	CLP7F	RET Domain EMC Clamp7 Flag: When the RET domain detects an EMC Clamp7 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp7 event 1: EMC Clamp7 event occurred
2	CLP6F	RET Domain EMC Clamp6 Flag: When the RET domain detects an EMC Clamp6 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp6 event 1: EMC Clamp6 event occurred
1	CLP5F	RET Domain EMC Clamp5 Flag: When the RET domain detects an EMC Clamp5 event, this bit is set by the

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		hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp5 event 1: EMC Clamp5 event occurred
0	CLP4F	RET Domain EMC Clamp4 Flag: When the RET domain detects an EMC Clamp4 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp4 event 1: EMC Clamp4 event occurred

3.6.33 PWR EMC RET Control Register 3 (PWR_EMCRETCTRL3)

Address offset: 0x110

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RETGB 11DET	RETGB 10DET	RETGB 9DET	RETGB 8DET	RETGBN 11DET	RETGBN 10DET	RETGBN 9DET	RETGBN 8DET	RETCLP 11DET	RETCLP 10DET	RETCLP 9DET	RETCLP 8DET
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	RETGB11DET	RET domain EMC GB11 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
10	RETGB10DET	RET domain EMC GB10 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
9	RETGB9DET	RET domain EMC GB9 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
8	RETGB8DET	RET domain EMC GB8 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
7	RETGBN11DET	RET domain EMC GBN11 detection enable This bit is set and cleared by software.

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		0: Disable detection 1: Enable detection
6	RETGBN10DET	RET domain EMC GBN10 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
5	RETGBN9DET	RET domain EMC GBN9 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
4	RETGBN8DET	RET domain EMC GBN8 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
3	RETCLP11DET	RET domain EMC Clamp11 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
2	RETCLP10DET	RET domain EMC Clamp10 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
1	RETCLP9DET	RET domain EMC Clamp9 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
0	RETCLP8DET	RET domain EMC Clamp8 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection

3.6.34 PWR EMC RET Status Register 3 (PWR_EMCRETSTS3)

Address offset: 0x114

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				GB11F	GB10F	GB9F	GB8F	GBN11F	GBN10F	GBN9F	GBN8F	CLP11F	CLP10F	CLP9F	CLP8F

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Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	GB11F	RET Domain EMC GB11 Flag: When the RET domain detects an EMC GB11 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB11 event 1: EMC GB11 event occurred
10	GB10F	RET Domain EMC GB10 Flag: When the RET domain detects an EMC GB10 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB10 event 1: EMC GB10 event occurred
9	GB9F	RET Domain EMC GB9 Flag: When the RET domain detects an EMC GB9 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB9 event 1: EMC GB9 event occurred
8	GB8F	RET Domain EMC GB8 Flag: When the RET domain detects an EMC GB8 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB8 event 1: EMC GB8 event occurred
7	GBN11F	RET Domain EMC GBN11 Flag: When the RET domain detects an EMC GBN11 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN11 event 1: EMC GBN11 event occurred
6	GBN10F	RET Domain EMC GBN10 Flag: When the RET domain detects an EMC GBN10 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN10 event 1: EMC GBN10 event occurred
5	GBN9F	RET Domain EMC GBN9 Flag: When the RET domain detects an EMC GBN9 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN9 event 1: EMC GBN9 event occurred
4	GBN8F	RET Domain EMC GBN8 Flag: When the RET Domain detects an EMC GBN8 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit.

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		0: No EMC GBN8 event 1: EMC GBN8 event occurred
3	CLP11F	RET Domain EMC Clamp11 Flag: When the RET domain detects an EMC Clamp11 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp11 event 1: EMC Clamp11 event occurred
2	CLP10F	RET Domain EMC Clamp10 Flag: When the RET domain detects an EMC Clamp10 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp10 event 1: EMC Clamp10 event occurred
1	CLP9F	RET Domain EMC Clamp9 Flag: When the RET domain detects an EMC Clamp9 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp9 event 1: EMC Clamp9 event occurred
0	CLP8F	RET Domain EMC Clamp8 Flag: When the RET domain detects an EMC Clamp8 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp8 event 1: EMC Clamp8 event occurred

3.6.35 PWR EMC RET Control Register 4 (PWR_EMCRETCTRL4)

Address offset: 0x118

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RETGB 14DET	RETGB 13DET	RETGB 12DET	Reserved	RETGBN 14DET	RETGBN 13DET	RETGBN 12DET	Reserved	RETCLP 14DET	RETCLP 13DET	RETCLP 12DET
					rw	rw	rw		rw	rw	rw		rw	rw	rw

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	RETGB14DET	RET domain EMC GB14 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection

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9	RETGB13DET	RET domain EMC GB13 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
8	RETGB12DET	RET domain EMC GB12 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
7	Reserved	Reserved, the reset value must be maintained.
6	RETGBN14DET	RET domain EMC GBN14 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
5	RETGBN13DET	RET domain EMC GBN13 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
4	RETGBN12DET	RET domain EMC GBN12 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
3	Reserved	Reserved, the reset value must be maintained.
2	RETCLP14DET	RET domain EMC Clamp14 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
1	RETCLP13DET	RET domain EMC Clamp13 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
0	RETCLP12DET	RET domain EMC Clamp12 detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection

3.6.36 PWR EMC RET Status Register 4 (PWR_EMCRETSTS4)

Address offset: 0x11C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					GB14F	GB13F	GB12F	Reserved	GBN14F	GBN13F	GBN12F	Reserved	CLP14F	CLP13F	CLP12F
					r	r	r		r	r	r		r	r	r

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	GB14F	RET Domain EMC GB14 Flag: When the RET domain detects an EMC GB14 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB14 event 1: EMC GB14 event occurred
9	GB13F	RET Domain EMC GB13 Flag: When the RET domain detects an EMC GB13 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB13 event 1: EMC GB13 event occurred
8	GB12F	RET Domain EMC GB12 Flag: When the RET domain detects an EMC GB12 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB12 event 1: EMC GB12 event occurred
7	Reserved	Reserved, the reset value must be maintained.
6	GBN14F	RET Domain EMC GBN14 Flag: When the RET domain detects an EMC GBN14 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN14 event 1: EMC GBN14 event occurred
5	GBN13F	RET Domain EMC GBN13 Flag: When the RET domain detects an EMC GBN13 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN13 event 1: EMC GBN13 event occurred
4	GBN12F	RET Domain EMC GBN12 Flag: When the RET Domain detects an EMC GBN12 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN12 event 1: EMC GBN12 event occurred
3	Reserved	Reserved, the reset value must be maintained.
2	CLP14F	RET Domain EMC Clamp14 Flag: When the RET domain detects an EMC Clamp14 event, this bit is set by the

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		hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp14 event 1: EMC Clamp14 event occurred
1	CLP13F	RET Domain EMC Clamp13 Flag: When the RET domain detects an EMC Clamp13 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp13 event 1: EMC Clamp13 event occurred
0	CLP12F	RET Domain EMC Clamp12 Flag: When the RET domain detects an EMC Clamp12 event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp12 event 1: EMC Clamp12 event occurred

3.6.37 PWR EMC BKP Control Register (PWR_EMCBKPCTRL)

Address offset: 0x120

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							BKPGB DET	Reserved			BKPGBN DET	Reserved			BKPCLP DET
							rw				rw				rw

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	BKPGBDET	Backup domain EMC GB detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
7	Reserved	Reserved, the reset value must be maintained.
4	BKPGBNDET	Backup domain EMC GBN detection enable This bit is set and cleared by software. 0: Disable detection 1: Enable detection
3:1	Reserved	Reserved, the reset value must be maintained.
0	BKPCLPDET	Backup domain EMC Clamp detection enable This bit is set and cleared by software. 0: Disable detection

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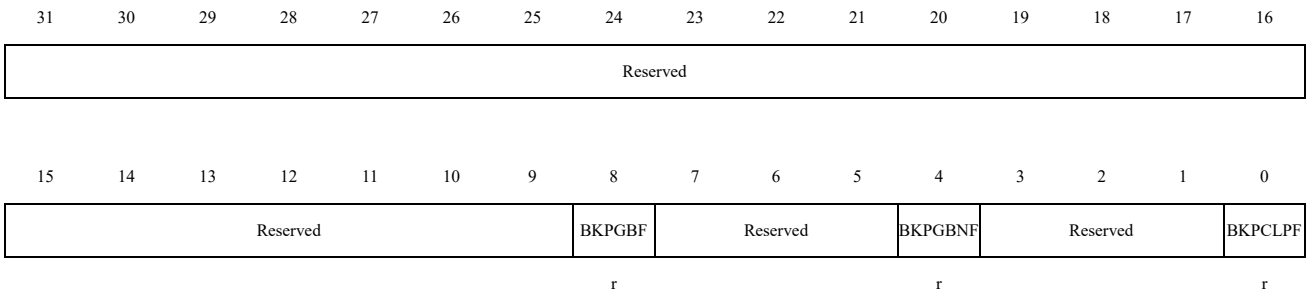
		1: Enable detection

3.6.38 PWR EMC BKP Status Register (PWR_EMCRETSTS)

Address offset: 0x124

Reset value: 0x0000 0000



Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	BKPGBF	Backup Domain EMC GB Flag: When the backup domain detects an EMC GB event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GB event 1: EMC GB event occurred
7:5	Reserved	Reserved, the reset value must be maintained.
4	BKPGBNF	Backup Domain EMC GBN Flag: When the RET Domain detects an EMC GBN event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC GBN event 1: EMC GBN event occurred
3:1	Reserved	Reserved, the reset value must be maintained.
0	BKPCLPF	Backup Domain EMC Clamp Flag: When the RET domain detects an EMC Clamp event, this bit is set by the hardware. Writing 1 to the EMCFCLR bit clears this bit. 0: No EMC Clamp event 1: EMC Clamp event occurred

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4 Reset and clock control (RCC)

The Reset and Clock Control (RCC) block is responsible for the generation of resets and clocks, which embeds two CPUs: an Arm® Cortex®-M7 and an Arm® Cortex®-M4, called CPU1(C1) and CPU2(C2), respectively.

4.1 Main features

The main features supported by RCC are as follows:

- Clock source control of different clock sources such as
  - HSI (High Speed Internal: 64 MHz).
  - HSE (High Speed External: 4 ~ 50 MHz).
  - MSI (Medium Speed Internal: 16 MHz).
  - PLL (Phase Locked Loop)
    - PLL1~3: 400MHz ~ 800MHz
    - SHRPLL: 400MHz ~ 1.25 GHz
  - LSE (Low Speed External: 32.768 KHz).
  - LSI (Low Speed Internal: 32 KHz).
- CPU (M7 and M4) clock selection.
- System bus clock selection.
- Peripheral clock selection.
- Clock source failure detection for HSE, LSE, LSI (primary) and PLL.
- Clock frequency offset detection for HSE and LSE.
- Reset generation for system, CPU and Peripherals.

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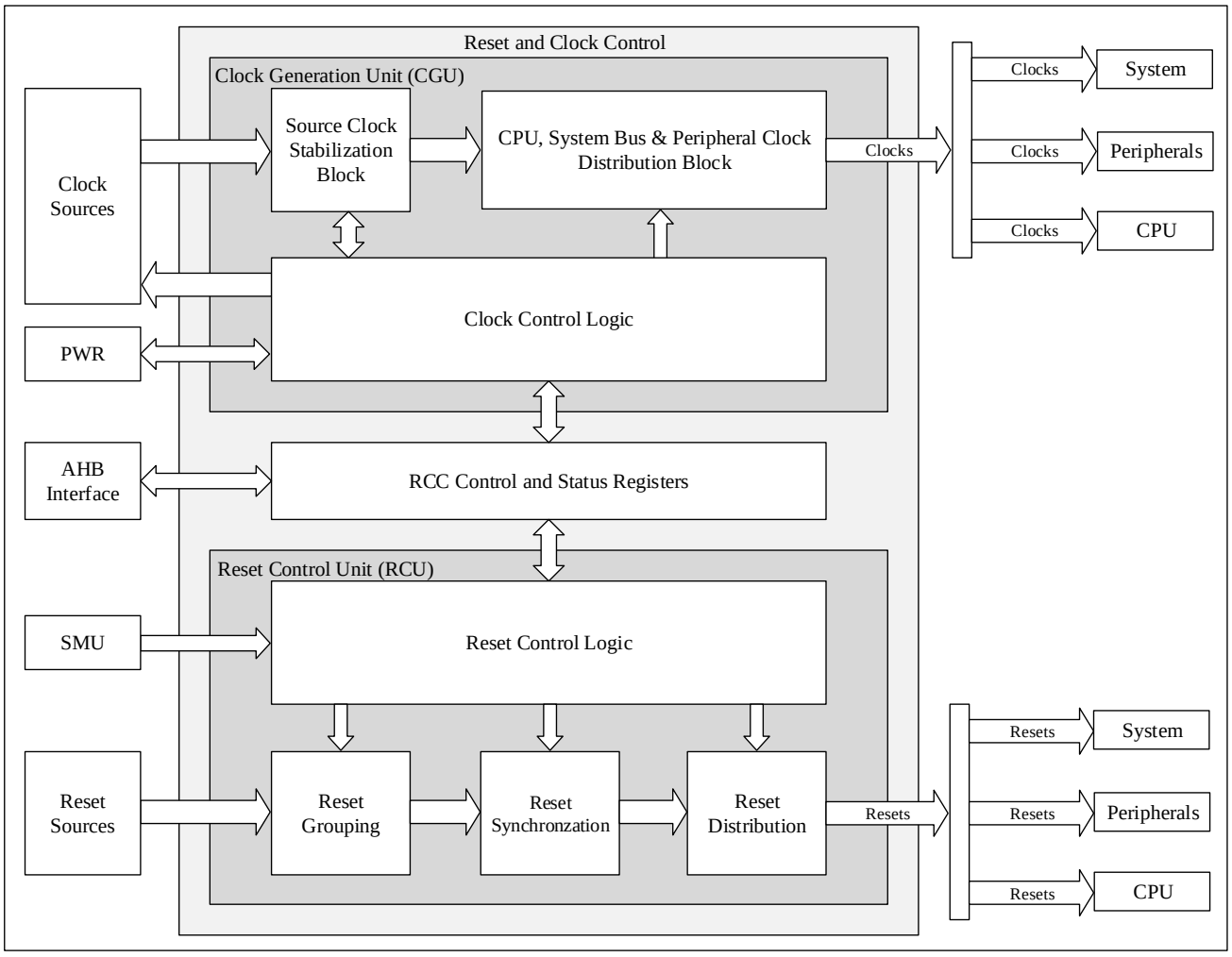
4.2 Block diagram

Figure 4-1 RCC Block Diagram



The RCC module is divided into:

- Clock Generation Unit (CGU)

  The CGU is responsible for clock source control and clock distribution to system, peripherals and CPU.

- Reset Control Unit (RCU)

  The RCU is responsible for reset control and distribution to system, peripherals and CPU.

- Register Interface

  This block consists of control and status registers which are accessed by CPU through AHB interface. The control registers are used by the CPU to provide clock and reset control information and the status registers are used to report the status of RCC module.

The RCC logic is divided into three parts based on the system power domains:

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- RCC main

  This module is placed in the Core power domain and is responsible for

  - System clock selection and system reset generation.
  - Providing clock and reset to M4 and M7 CPU.
  - Providing AXI, AHB and APB bus clocks and resets.
  - Providing clock and reset to peripherals in Core power domain and sub domains such as HSC, Ethercat, SHRTIM, CPU1 (M7), CPU2 (M4), MDMA and graphics sub system.
  - Providing clock gating control, clock division and clock source selection multiplexers for peripheral and system clocks.

- RCC retention

  This module is placed in the Retention power domain and is responsible for providing clock gating control, clock division, clock source selection multiplexers and reset control for peripherals in Retention power domain.

- RCC BKP

  This module is placed in the Backup power domain and is responsible for providing clock gating control, clock division, clock source selection multiplexers and reset control for peripherals in Backup power domain.

4.3 Reset Control Unit(RCU)

The Reset Control Unit takes inputs from reset sources such as Power On Reset (POR), NRST pad and reset request from certain peripherals and CPU to generate system reset, CPU reset (M7 and M4) and peripheral resets.

Register “RCC_CTRLSTS” contains status bits that correspond to each of the reset source. When a reset occurs, the source of reset generation can be ascertained by reading this register. After reading, the “RMRSTF” bit in this register should be set to 1’b1 to clear all the status bits.

4.3.1 Power On Reset (POR)

Each power domain has a POR and resets all the registers in that power domain. It has the following POR.

1. Main power domain POR from AFE and PWR.
2. Retention power domain POR from PWR.
3. Backup power domain POR from AFE.
4. C1(CM7) sub domain POR from PWR.
5. C2(CM4) sub domain POR from PWR.
6. HSC1 subsystem POR from PWR.
7. HSC2 subsystem POR from PWR.
8. SHRTIM sub domain POR from PWR.

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9. Graphic subsystem POR from PWR.
10. Ethercat sub domain POR from PWR.

4.3.2 System reset

A system reset resets all registers to their reset values except the reset flags in the reset status register(RCC_CTRLSTS) and certain registers in the Backup domain(these are reset only by programming the BDRST register and by Backup domain POR) .

System reset is asserted by following sources.

- NRST pin.
- POR reset (main domain) from PWR and AFE.
- IWDG & WWDG reset request.
- Reset request from CPU (M7 and M4).
- EMC reset request.
- Low Power Reset request from PWR.
- BOR reset.
- MMU reset request.

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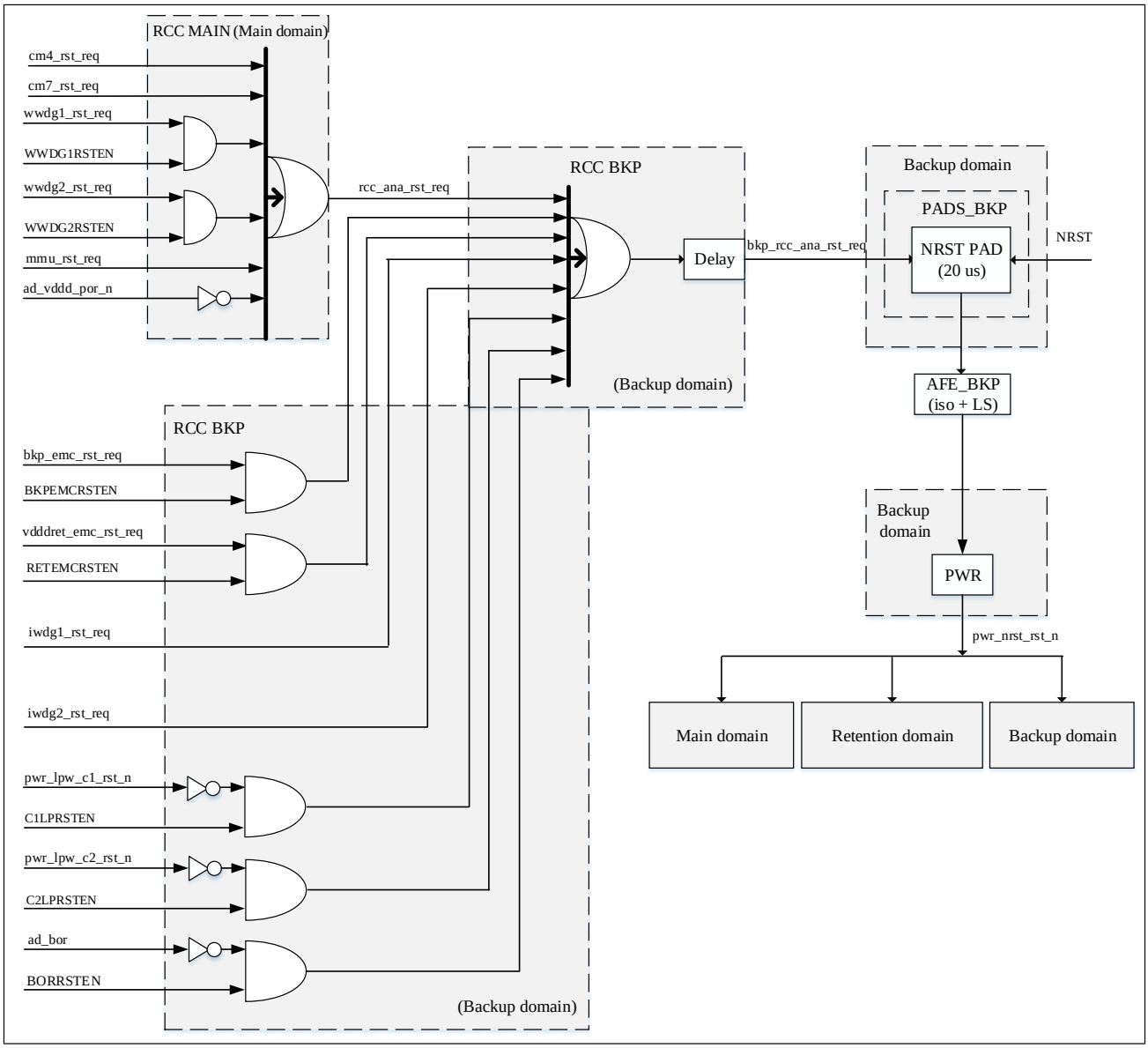
Figure 4-2 NRST reset generation



The NRST reset request signals from CPU (M7 & M4), MMU and IWDG cannot be masked (controlled) by software.

The remaining NRST reset request signals can be controlled by software.

- WWDG1:

RCC register bit RCC_CFG1.WWDG1RSTEN is used to control NRST reset assertion from WWDG1 reset source.

- WWDG2:

RCC register bit RCC_CFG1.WWDG2RSTEN is used to control NRST reset assertion from WWDG2 reset source.

- BKP_EMC:

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RCC register bit RCC_BDCTRL.BKPEMCRSTEN is used to control NRST reset assertion from stanby (Backup) domain EMC reset source.

- RET_EMC:

RCC register bit RCC_BDCTRL.RETEMCRSTEN is used to control NRST reset assertion from retention domain EMC reset source.

- M7 CPU sub domain low power NRST reset request:

RCC register bit RCC_BDCTRL.C1LPRSTEN is used to control this NRST reset source.

- M4 CPU sub domain low power NRST reset request:

RCC register bit RCC_BDCTRL.C2LPRSTEN is used to control this NRST reset source.

- BOR:

RCC register bit RCC_BDCTRL.BORRSTEN is used to control the NRST reset assertion due to BOR reset.

4.3.3 M7 CPU Reset

M7 CPU has Core reset and POR reset.
M7 Core reset has the following sources:

- Main power domain POR from PWR and AFE.
- CPU reset request from PWR.
- C1 domain low power reset from PWR.
- C1 domain POR reset from PWR.
- System Reset (NRST).
- WWDG1 reset request.
- System Boot complete signal from SMU.

M7 POR reset has the following sources:

- Main power domain POR from PWR and AFE.
- C1 domain POR reset from PWR.

4.3.4 M4 CPU Reset

M4 CPU has Core and POR reset.

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M4 Core reset has the following sources:

- Main power domain POR from PWR and AFE.
- CPU reset request from PWR.
- C2 domain low power reset from PWR.
- C2 domain POR reset from PWR.
- System Reset (NRST).
- WWDG2 reset request.
- System Boot complete signal from SMU.
- Soft Reset (AHB register) to hold the M4 CPU in reset till M7 CPU boot is completed.

M4 POR reset has the following sources:

- Main power domain POR from PWR and AFE.
- C2 domain POR reset from PWR.

4.3.5 Peripheral resets

Peripheral resets have the following sources:

- Power domain POR (main/ret/bkp) from AFE and PWR
- Sub-domain reset from PWR (Example: HSC subsystem reset, graphics subsystem reset).
- System Reset (NRST).
- Individual software programmable reset (RCC AHB register).

Configurable register bits can be used to reset the corresponding peripherals.for example, Set the register bit RCC_AHB1RST1.ADC1RST" to 1 to assert soft reset to ADC1 peripheral.

Table 4-1 Peripheral Resets

Domain	Sub Domain	Peripheral	Peripheral Resets	Domain POR	Sub Domain POR	System reset	SMU control	I/O pad reset	Soft Reset Register
Main	HSC1	Ethernet1	eth1_bus_rst_n	Y	Y	Y	Y	N	ETH1RST
			eth1_ptp_rst_n	Y	Y	Y	Y	N	ETH1RST
		USB1	usb1_bus_rst_n	Y	Y	Y	Y	N	USB1RST
			usb1_por_rst_n	Y	Y	N	N	N	USB1PORRST
			usb1_wrap_rst_n	Y	Y	Y	Y	N	USB1WRAPRST
	HSC2	Ethernet2	eth2_bus_rst_n	Y	Y	Y	Y	N	ETH2RST
			eth2_ptp_rst_n	Y	Y	Y	Y	N	ETH2RST
		USB2	usb2_bus_rst_n	Y	Y	Y	Y	N	USB2RST
			usb2_por_rst_n	Y	Y	N	N	N	USB2PORRST

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			usb2_wrap_rst_n	Y	Y	Y	Y	N	USB2WRAPRST
		SDMMC2	sdmmc2_bus_rst_n	Y	Y	Y	Y	N	SDHOST2RST
			sdmmc2_cfg_rst_n	Y	Y	Y	Y	N	SDMMC2RST
	Graphics	DVP{n=1,2}	dvp(n)_ahb_rst_n	Y	Y	Y	Y	N	DVP(n)RST
			dvp(n)_apb_rst_n	Y	Y	Y	Y	N	DVP(n)RST
		GPU	gpu_rst_n	Y	Y	Y	Y	N	GPURST
		DSI	dsi_esc_rst_n	Y	Y	Y	Y	N	DSIRST
			dsi_ulps_rst_n	Y	Y	Y	Y	N	DSIRST
			dsi_ker_rst_n	Y	Y	Y	Y	N	DSIRST
			dsi_cfg_rst_n	Y	Y	Y	Y	N	DSICFGRST
			dsi_bus_rst_n	Y	Y	Y	Y	N	DSIRST
			dsi_phy_rst_n	Y	Y	Y	Y	N	DSIRST
			dsi_vid_rst_n	Y	Y	Y	Y	N	DSIRST
		LCDC	lcdc_rst_n	Y	Y	Y	Y	N	LCDCRST
		JPEG	jpeg_dec_axi_bus_rst_n	Y	Y	Y	Y	N	JPEGDRST
			jpeg_enc_axi_bus_rst_n	Y	Y	Y	Y	N	JPEGERST
			jpeg_sgdma_h2p_rst_n	Y	Y	Y	Y	N	JPEGERST JPEGDRST
			jpeg_sgdma_p2h_rst_n	Y	Y	Y	Y	N	JPEGERST JPEGDRST
	Ethercat	Ethercat	ethercat_bus_rst_n	Y	Y	Y	Y	N	ESCRST
	SHRTIM1	SHRTIM1	shrtim1_ker_rst_n	Y	Y	Y	Y	N	SHRTIM1RST
			shrtim1_bus_rst_n	Y	Y	Y	Y	N	SHRTIM1RST
			shrtim1_sys_rst_n	Y	Y	Y	Y	N	N
			hrtim1_por_rst_n	Y	Y	N	N	N	N
	SHRTIM2	SHRTIM2	shrtim2_ker_rst_n	Y	Y	Y	Y	N	SHRTIM2RST
			shrtim2_bus_rst_n	Y	Y	Y	Y	N	SHRTIM2RST
			shrtim2_sys_rst_n	Y	Y	Y	Y	N	N
			hrtim2_por_rst_n	Y	Y	N	N	N	N
	SHRTIM_AFE	SHRTIM_AFE	shrtim_afe_por_rst_n	Y	Y	N	N	N	SHRTIMAFERST
	N	ADC(n){n=1,2,3}	adc(n)_async_rst_n	Y	N	Y	Y	N	ADC(n)RST
			adc(n)_bus_rst_n	Y	N	Y	Y	N	ADC(n)RST
	N	BTIM(n){n=1,2,3,4}	btimer(n)_rst_n	Y	N	Y	Y	N	BTIM(n)RST
	N	GTIMA(n){n=1,2,3,4,5,6,7}	gtimera(n)_rst_n	Y	N	Y	Y	N	GTIMA(n)RST
	N	GTIMB(n){n=1,2,3}	gtimerb(n)_rst_n	Y	N	Y	Y	N	GTIMB(n)RST
			gtimerb(n)_sys_rst_n	Y	N	Y	Y	N	N

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	N	USART(n){1,2,3,4,5,6,7,8}	usart(n)_rst_n	Y	N	Y	Y	N	USART(n)RST
	N	UART(n){n=9~15}	uart(n)_rst_n	Y	N	Y	Y	N	UART(n)RST
	N	SPI(n){n=1,2,3,4,5,6,7}	spi(n)_rst_n	Y	N	Y	Y	N	SPI(n)RST
	N	I2S(n){1,2,3,4}	i2s(n)_ker_rst_n	Y	N	Y	Y	N	N
			i2s(n)_rst_n	Y	N	Y	Y	N	I2S(n)RST
	N	I2C(n){n=1,2,3,4,5,6,7,8,9,10}	i2c(n)_bus_rst_n	Y	N	Y	Y	N	I2C(n)RST
			i2c(n)_ker_rst_n	Y	N	Y	Y	N	I2C(n)RST
	N	FDCAN(n){n=1,2,3,4,5,6,7,8}	fdcan(n)_ker_rst_n	Y	N	Y	Y	N	FDCAN(n)RST
			fdcan(n)_bus_rst_n	Y	N	Y	Y	N	FDCAN(n)RST
	N	DAC(n){n=12,34,56}	dacctrl(n)_rst_n	Y	N	Y	Y	N	DAC(n)RST
	N	WWDG1	wwdg1_rst_n	Y	N	Y	Y	N	WWDG1RST
	N	WWDG2	wwdg2_rst_n	Y	N	Y	Y	N	WWDG2RST
	N	ECCMON1	eccmon1_rst_n	Y	N	Y	Y	N	ECCM1RST
			eccmon1_m7_rst_n	Y	N	Y	Y	N	ECCM1RST
	N	ECCMON2	eccmon2_rst_n	Y	N	Y	Y	N	ECCM2RST
	N	ECCMON3	eccmon3_rst_n	Y	N	Y	Y	N	ECCM3RST
	N	ECCMON_AHBCACHE	eccmon_ahbcache_rst_n	Y	N	Y	Y	N	ECCMACRST
	N	SDPU	sdpu_bus_rst_n	Y	N	Y	Y	N	SDPURST
	N	CORDIC	cordic_rst_n	Y	N	Y	Y	N	CORDICRST
	N	FMAC	fmac_bus_rst_n	Y	N	Y	Y	N	FMACRST
	N	DSMU	dsmu_ker_rst_n	Y	N	Y	Y	N	DSMURST
			dsmu_ker_a_rst_n	Y	N	Y	Y	N	DSMURST
			dsmu_bus_rst_n	Y	N	Y	Y	N	DSMURST
	N	ATIM(n){n=1,2,3,4}	atimer(n)_rst_n	Y	N	Y	Y	N	ATIM(n)RST
			atimer(n)_sys_rst_n	Y	N	Y	Y	N	N
	N	CRC	crc_rst_n	Y	N	Y	Y	N	CRCRST
	N	SEMA4	sema4_rst_n	Y	N	Y	Y	N	SEMA4RST
	N	DMA_MUX1	dma_mux1_rst_n	Y	N	Y	Y	N	DMAMUX1RST
	N	DMA_MUX2	dma_mux2_rst_n	Y	N	Y	Y	N	DMAMUX2RST
	N	AFEC	afec_rst_n	Y	N	Y	N	N	N
			afec_por_rst_n	Y	N	N	N	N	N
	MDMA	MDMA	mdma_axi_bus_rst_n	Y	Y	Y	Y	N	MDMARST
			mdma_m7_bus_rst_n	Y	Y	Y	Y	N	MDMARST
	N	MMU	mmu_axi_rst_n	Y	N	Y	N	N	N
			mmu_hreset_n	Y	N	Y	Y	N	N

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			mmu_por_rst_n	Y	N	N	N	N	N
	N	SMU	smu_sys_rst_n	Y	N	Y	N	N	N
			smu_por_rst_n	Y	N	N	N	N	N
	N	OTPC	otpc_bus_rst_n	Y	N	Y	Y	N	OTPCRST
			otpc_sys_rst_n	Y	N	Y	N	N	N
	C1	TCM	tcm_core_rst_n	Y	Y	Y	Y	N	N
			tcm_axi_bus_rst_n	Y	Y	Y	Y	N	N
			tcm_apb_bus_rst_n	Y	Y	N	N	N	N
			tcm_axi_ramc(n)_rst_n	Y	Y	Y	Y	N	N
	N	AXI_ROMC	axi_romc_rst_n	Y	N	Y	Y	N	N
	N	AXI_RAMC	axi_ramc1_rst_n	Y	N	Y	Y	N	N
	N	AHB_RAMC(n){n=1,2,3,4,5}	ramc(n)_rst_n	Y	N	Y	Y	N	N
	N	AHB_RAMC_BKP	ramc_bkp_rst_n	Y	N	Y	Y	N	N
	N	XSPI(n){n=1,2}	xspi(n)_ker_rst_n	Y	N	Y	Y	N	XSPI(n)RST
			xspi(n)_bus_rst_n	Y	N	Y	Y	N	XSPI(n)RST
			xspi(n)_timer_rst_n	Y	N	Y	Y	N	XSPI(n)RST
	N	FEMC	femc_a_rst_n	Y	N	Y	Y	N	FEMCRST
			femc_m0_rst_n	Y	N	Y	Y	N	FEMCRST
			femc_m1_rst_n	Y	N	Y	Y	N	FEMCRST
			femc_cfg_rst_n	Y	N	Y	Y	N	FEMCCFGRST
	N	SDRAM	sdram_mem_rst_n	Y	N	Y	Y	N	SDRAMRST
			sdram_c_rst_n	Y	N	Y	Y	N	SDRAMRST
			sdram_m_rst_n	Y	N	Y	Y	N	SDRAMRST
			sdram_bus_rst_n	Y	N	Y	Y	N	N
	N	DMA(n){n=1,2,3}	dma(n)_rst_n	Y	N	Y	Y	N	DMA(n)RST
	C2	CM4 Cache D	cah_d_rst_n	Y	Y	Y	Y	N	CAHDRST
	C2	CM4 Cache I	cah_i_rst_n	Y	Y	Y	Y	N	CAHIRST
	N	DCMU	dcmu_m7_rst_n	Y	N	Y	Y	N	DCMURST
			dcmu_m4_rst_n	Y	N	Y	Y	N	DCMURST
	N	AXI Bus Matrix	axi_bus_matrix_gpv_rst_n	Y	N	Y	Y	N	N
			axi_bus_matrix_m7_sync_rst_n	Y	N	Y	Y	N	
			axi_bus_matrix_m7_gpv_rst_n	Y	N	Y	Y	N	
			axi_bus_matrix_m4_sync_rst_n	Y	N	Y	Y	N	
			axi_bus_matrix_m4_gpv_rst_n	Y	N	Y	Y	N	

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	N	AHB Bus Matrix(n) {n=1,2}	ahb_bus_matrix(n)_sync_rst_n	Y	N	Y	Y	N	N
	HSC2	AHB Bus Matrix3	ahb_bus_matrix3_sync_rst_n	Y	Y	Y	Y	N	N
	N	Debug	rcc_sys_ntrst	Y	N	N	N	Y	N
			sys_dap_rst_n	Y	N	N	N	N	N
			swd_por_rst_n	Y	N	N	N	N	N
			dualcore_debug_por_rst_n	Y	N	N	N	N	N
	C2		m4_dap_rst_n	Y	Y	N	N	N	N
	N	EST	est_rst_n	Y	N	Y	N	N	N
Retention	N	EXTI	exti_m4_rst_n	Y	N	Y	N	N	N
			exti_m7_rst_n	Y	N	Y	N	N	N
			exti_rst_n	Y	N	Y	N	N	N
	N	AFIO	afio_rst_n	Y	N	Y	N	N	AFIORST
	N	GPIO(n){n=A,B,C,D,E,F,G,H,I,J,K}	gpio(n)_rst_n	Y	N	Y	N	N	GPIO(n)RST
	N	LPTIM(n) {n=1,2,3,4,5}	lptim(n)_ker_rst_n	Y	N	Y	N	N	LPTIM(n)RST
			lptim(n)_prst_n	Y	N	Y	N	N	LPTIM(n)RST
	N	LPUART(n){n=1,2}	lpuart(n)_ker_rst_n	Y	N	Y	N	N	LPUART(n)RST
			lpuart(n)_prst_n	Y	N	Y	N	N	LPUART(n)RST
	N	COMP	compctrl_ker_rst_n	Y	N	Y	N	N	COMPRST
			compctrl_prst_n	Y	N	Y	N	N	COMPRST
Backup	N	PWR	rcc_bkp_pwr_rst_n	Y	N	Y	N	N	PWRRST
	N	RTC	rtc_core_rst_n	Y	N	Y	N	N	BDRST
			rtc_pclk_rst_n	Y	N	N	N	N	BDRST
			rtcclk_rst_n	Y	N	N	N	N	BDRST
	N	IWDG(n){n=1,2}	iwdg(n)_ker_rst_n	Y	N	Y	N	N	N
			iwdg(n)_bus_rst_n	Y	N	Y	N	N	N
	N	AFEC_BKP	afec_bkp_rst_n	Y	N	Y	N	N	N
	N	AFIO_BKP	afio_bkp_rst_n	Y	N	Y	N	N	AFIORST
	N	GPIOC_BKP	gpioc_bkp_rst_n	Y	N	Y	N	N	GPIOCRST

4.4 Clock Generation Unit (CGU)

The RCC provides a wide choice of clock generators:

- HSI (High-speed internal oscillator) clock: 64 MHz
- HSE (High-speed external oscillator) clock: 4 to 50 MHz
- MSI (Medium-speed internal oscillator) clock: 16 MHz

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- LSE (Low-speed external oscillator) clock: 32.768 kHz
- LSI (Low-speed internal oscillator) clock: 32 kHz

It offers a high flexibility for the application to select the appropriate clock for CPUs and peripherals, in particular for peripherals that require a specific clock such as Ethernet, USB, I2C and SDMMC.

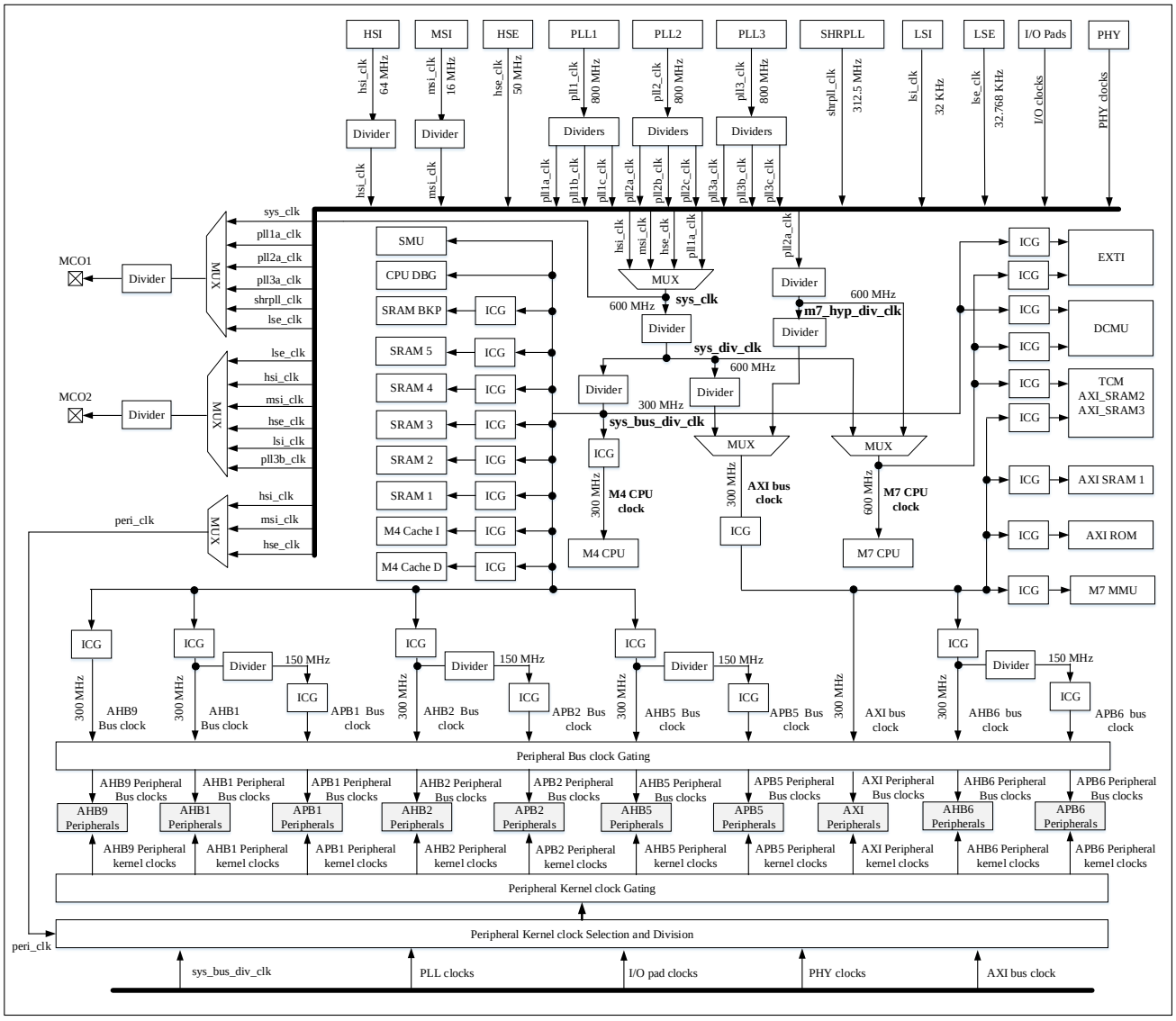
To optimize the power consumption, each clock source can be switched ON or OFF independently.

The RCC provides up to 3 PLLs; each of them can be configured with integer or fractional ratios. Additional dedicated SHRPLL clock for SHRTIM.

As shown in the Figure 4-3, the RCC offers 2 clock outputs (MCO1 and MCO2), with a great flexibility on the clock selection and frequency adjustment.

4.4.1 Clock tree

Figure 4-3 Clock Tree



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Note: The Maximum frequency of each clock line is represented in the diagram

The Clock Generation Unit (CGU) has the following functions.

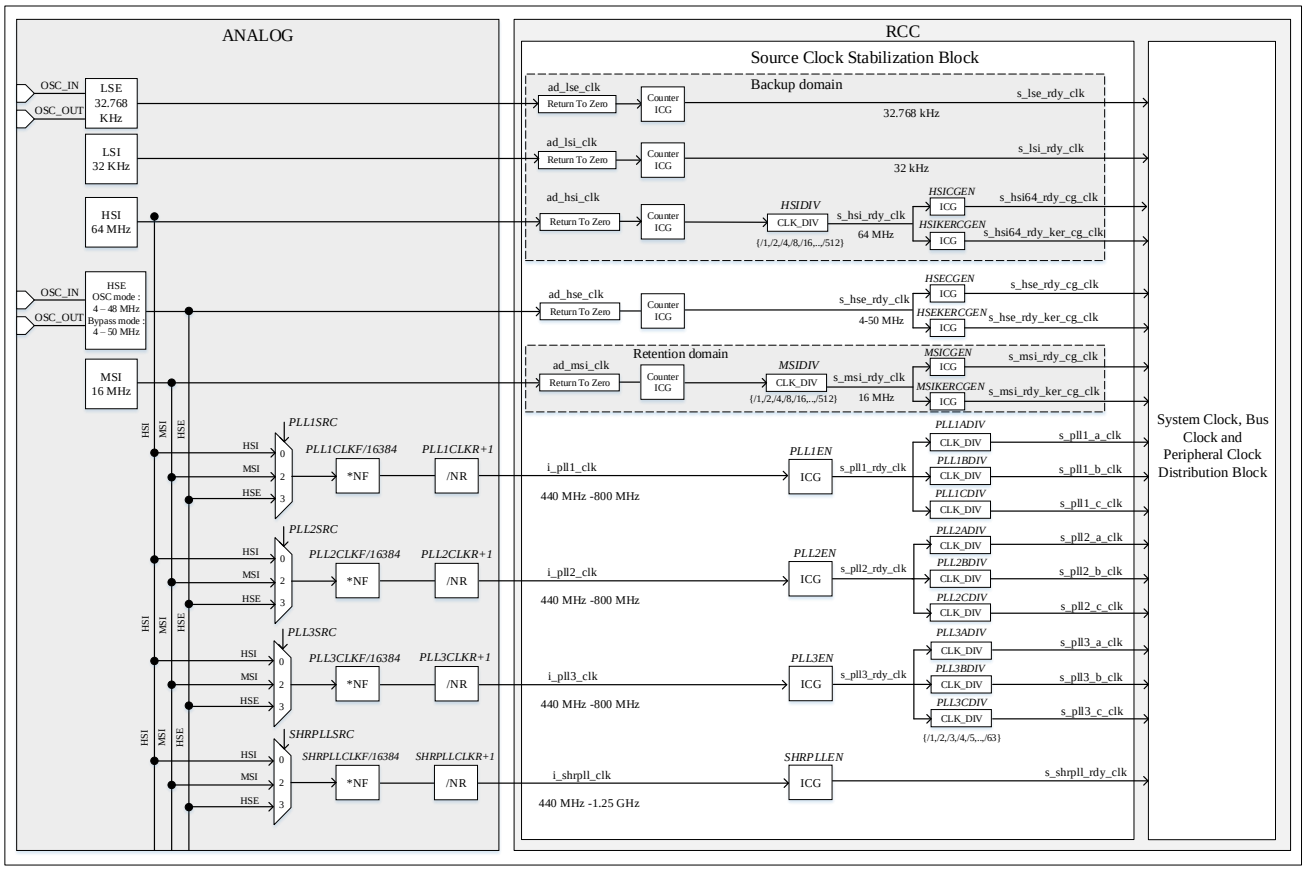
- Source Clock Stabilization: Filter out variations in duty cycle and amplitude of the source clocks.
- Distribute clocks to CPU, system bus and peripherals by utilizing clock gating, clock switching and clock division mechanisms.

Clock tree is divided into 3 clock domains

- Clock domain 1: This clock domain consists of clocks synchronous to M4 CPU and bus clock.
- Clock domain 2: This clock domain consists of clocks synchronous to M7 CPU clock.
- Clock domain 3: This clock domain consists of clocks synchronous to AXI clock.

4.4.2 Clock sources

Figure 4-4 Souce Clock Stabilization



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4.4.2.1 HSI clock

64 MHz Internal High Speed Oscillator.

The control logic of this oscillator is in the Backup power domain. This clock is used as default system clock after initial power-up and after wake up from system low power modes (stop0, stop2 and standby).

The HSI advantages are the following:

- Low-cost clock source since no external crystal is required
- Faster startup time than HSE

But the HSI frequency, even with frequency calibration, is less accurate than an external crystal oscillator or ceramic resonator.

The HSI Clock enable is controlled by the following sources:

- PWR control signal.
- RCC control register(RCC_SRCCTRL1.HSIEN)
- HSE CSS Logic.
- PLL source clock control.

The HSI can be switched ON and OFF using the RCC_SRCCTRL1.HSIEN bit. The following should be performed before turning off the HSI:

- If HSI clock is used as system clock, then switch system clock to MSI, HSE or PLL1 (Do not select HSI as the PLL1 clock source).
- If HSI clock is used by any peripheral as kernel clock, then switch the peripheral kernel clock to any other clock or gate the clock to the peripheral.
- If HSI clock is used as the source clock of a PLL, then disable the PLL clock and select the PLL source as either MSI or HSE.

Note: Turning off other clock sources should also be done before checking for the above conditions

The flag “HSIRDF” and “AFEHSIRDF” in “RCC_SRCCTRL1” register indicates if the HSI is stable or not. At startup, the HSI output clock is not released until this bit is set by hardware.

4.4.2.1.1 HSI Trim

RCC has the feature to perform fine adjustment of HSI Trim value by writing the increment/decrement factor in RCC_SRCCTRL3.HSITRIM.

An increment/decrement of HSI Trim value by a factor of 1 modifies the HSI clock frequency by a step size of 150 KHz.

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HSICAL = Internal trim value + HSITRIM, If the configured HSITRIM value puts HSICAL out of range, then the original HSI Trim value is set, and RCC_SRCCTRL2.HSICALEF flag bit will be set, an interrupt can also be generated if RCC_CLKINT2.HSICALEIE is enabled.

4.4.2.2 MSI clock

16 MHz Medium Speed Oscillator.

The control logic of this oscillator is in the Retention power domain. This clock is used as high speed clock by peripherals in the Retention power domain in stop2 system power mode. This clock can also be selected as system clock and kernel clock of certain peripherals.

The MSI Clock enable is controlled by the following sources:

- RCC control register(RCC_SRCCTRL1.MSIEN)
- PLL source clock control.

When the MSI clock is enabled, the MSI clock from analog module starts to toggle, however the initial few clock cycles are not reliable in terms of parameters such as duty cycle and frequency. To ensure that the duty cycle and frequency of the clock signal is stable, a delay is required, this delay value can be programmed in RCC_MSIRDDL.DELAY. After this wait period (typically around 1us) the MSI clock can be used for system operations.

The flag “MSIRDF” and “AFEMSIRDF” in “RCC_SRCCTRL1” register indicates if the MSI is stable or not.

4.4.2.2.1 MSI Trim

RCC has the feature to perform fine adjustment of MSI Trim value by writing the increment/decrement factor in RCC_SRCCTRL2.MSITRIM.

An increment/decrement of MSI Trim value by a factor of 1 modifies the MSI clock frequency by a step size of 33.2KHz.

MSICAL = Internal trim value + MSITRIM, If the configured MSITRIM value puts MSICAL out of range, then the original MSI Trim value is set, and RCC_SRCCTRL2.MSICALEF flag bit will be set, an interrupt can also be generated if RCC_CLKINT2.MSICALEIE is enabled.

4.4.2.3 HSE clock

4~48 MHz (Osc mode) & 4~50 MHz (Bypass mode) External High Speed Oscillator.

The control logic of this oscillator is in the Core power domain. This clock can be selected as system clock, kernel clock of certain peripherals and as reference clock of certain phy (USB, DSI...).

The HSE Clock enable is controlled by the following sources.

- PWR control signal.

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- RCC control registers(RCC_SRCCTRL1.HSEEN and RCC_SRCCTRL1.HSEBP)
- HSE CSS Logic.
- PLL source clock control.

When the HSE clock is enabled, the HSE clock from analog module starts to toggle, however the initial few clock cycles are not reliable in terms of parameters such as duty cycle and frequency. To ensure that the duty cycle and frequency of the clock signal is stable, a delay is required, this delay value can be programmed in RCC_HSERDDL.DELAY. After this wait period (typically around 1us) the HSE clock can be used for system operations.

The HSE enable procedure is as follows:

1. Set the bitfield RCC_HSERDDL.DELAY to a specified value.
2. Set the bit RCC_SRCCTRL1.HSERDCNTEN to 1'b0.
3. Set RCC_SRCCTRL1.HSEEN bit to 1'b1 when selecting crystal mode(Additional RCC_SRCCTRL1.HSEBP enable is required if bypass mode is selected.).
4. Wait for a predetermined time.
5. Set the bit RCC_SRCCTRL1.HSERDCNTEN to 1'b1.
6. Read the bit RCC_SRCCTRL1.HSERDF to check if it is set to 1'b1.

4.4.2.3.1 HSE Clock Security System (HSE CSS)

The clock security system can be enabled by software via the RCC_SRCCTRL1.HSECSSEN bit.

The clock offset detection can be enabled by software via the RCC_SRCCTRL1.HSECSSEN and RCC_HSEOS.HSEOSEN bit.

If a clock failure or offset is detected on the HSE clock, the system automatically switches to the HSI in order to provide a safe clock. The HSE is then automatically disabled, a clock failure event is sent to the break inputs of advanced-control timers, and an non maskable interrupt(NMI) is generated to inform the software about the failure, thus allowing the MCU to perform rescue operations. If the HSE output was used as clock source for PLLs when the failure occurred, the PLLs are also disabled.

Clock Offset Detection

The HSE clock offset detection is divided into two phases.

- HSE clock frequency calibration phase.
- HSE clock frequency offset detection phase.

HSE clock frequency calibration phase:

This phase is enabled by RCC_HSECAL.HSECALCNTEN. In this phase, the HSE clock of particular frequency is

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divided by 128 and a calibration counter is used to count the number of HSI clock pulses in half cycle of the HSE/128 clock. This calibration count value is stored in RCC_HSECAL.HSECALCNT, and write RCC_HSEOS.HSEOSTHR according to the HSE clock frequency.

For example, when the HSE is 48M, then the desired HSECALCNT = 64M/(48M/128)*0.5 = 85, HSEOSTHR configured as 3.

HSE clock frequency offset detection phase:

This phase is enabled by RCC_HSEOS.HSEOSEN. In this phase, offset counter is used to count the number of HSI clock pulses in half cycle of the HSE/128 clock. Compare the offset counter value with the calibration counter to determine if a 5% offset exists.

Programming Sequence to detect 5% offset in HSE clock.

1. If HSI clock is disabled then execute the sequence to enable HSI clock.
2. Execute the sequence to enable HSE clock.
3. Set the bit “HSECALCNTEN” in “RCC_HSECAL” register to 1’b1.
4. Read the bit “HSECALCNTF” in “RCC_HSECAL” register and check if it is set to 1’b1. Repeat this step till this bit is set to 1’b1.
5. Read the bit field “HSECALCNT” in “RCC_HSECAL” register. The value strored in this register can be used to verify the frequency of HSE clock.
6. Write the bit field “HSEOSTHR” in “RCC_HSEOS” register with threshold value corresponding to the HSE frequency. Refer to RCC register file for the threshold values.
7. Set the bit “HSEOSEN” in “RCC_HSEOS” register to 1’b1.
8. Set the bit “HSECSSEN” in “RCC_SRCCTRL1” register to 1’b1.
9. If an offset greater than or equal to 5% is detected on HSE clock frequency then HSE CSS interrupt will be asserted and the flag “HSECSSIF” will be set in the “RCC_CLKINT1” register.
10. Read the bit “HSEOSF” in “RCC_HSEOS” register. This bit will be set to 1’b1 if frequency offset is detected.
11. Set the bit “HSEEN” in “RCC_SRCCTRL1” register to 1’b0. Read the bit “HSERDF” in “RCC_SRCCTRL1” register and check if it is set to 1’b0. Repeat this step till the “HSERDF” bit is set to 1’b0.
12. Set the bit “HSECSSEN” in “RCC_SRCCTRL1” register to 1’b0.
13. Set the bit “HSECSSIC” in “RCC_CLKINT1” register to 1’b1. Read the bit “HSECSSIF” in “RCC_CLKINT1” register and check if it is set to 1’b0. Repeat this step till “HSECSSIF” bit is set to 1’b0.
14. Set the bit “HSEOSF” in “RCC_HSEOS” register to 1’b1.
15. Set the bit “HSEOSEN” in “RCC_HSEOS” register to 1’b0.
16. Set the bit “HSECALCNTEN” in “RCC_HSECAL” register to 1’b0.

4.4.2.4 LSI clock

32 KHz Low Speed Internal Oscillator.

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LSI clock consists of two clock sources.

- LSI Primary Clock Source.
- LSI Secondary Clock Source.

The control logic of this oscillator is in the Backup power domain. This is the first clock to toggle during system power-up and used by PWR in the Backup power domain to initiate system power-up and wake up from system low power modes like standby and stop2 . This clock is also used by peripherals in Backup and retention power domain.

LSI Primary Clock enable is controlled by the following sources.

- PWR control signal.
- RCC control register (RCC_BDCTRL.LSIEN and RCC_BDCTRL.LSIRDEN).
- LSI CSS Logic.
- IWDG control signal.

The flag “LSIRDF” and “AFELSIRDF” in “RCC_BDCTRL” register indicates if the Primary LSI is stable or not.

LSI Secondary Clock enable is controlled by the following sources.

- RCC control register (RCC_BDCTRL.LSISECEN).

The flag “LSISECRDF” in “RCC_BDCTRL” register indicates if the Secondary LSI is stable or not.

4.4.2.4.1 LSI Clock Security System (LSI CSS)

By default LSI clock is sourced from LSI primary source. If this source fails to generate LSI clock, then the LSI primary clock failure detection block detects this failure and switches the LSI clock to LSI secondary source, the failure event is recorded in the RCC status register and also generate interrupt, the control flow is shown in Figure 4-5, At this point RCC_BDCTRL.LSIOVREN is configured to 0, according to the RCC_BDCTRL.LSICSSEN to choose whether to turn on the CSS to switch the clock source via hardware.

In stop2 mode, if primary LSI failure is detected then the “RTC tamper” interrupt signal(When the corresponding EXTI is configured) wakes up the system to run mode. In standby mode, if primary LSI failure is detected then the “RTC PWR wakeup” event signal wakes up the system to run mode.

The primary LSI failure detection as follows:

1. Set the bit RCC_BDCTRL.LSICSSEN and RCC_CLKINT3.LSIFIE to 1’b1
2. If primary LSI failure is detected, then RCC interrupt is generated and the interrupt status flag “LSIFIF” bit in “RCC_CLKINT3” register is set to 1’b1
3. Read the register bit “LSIPFF” in “RCC_BDCTRL” register. If this bit is set to 1’b1, then it implies that primary

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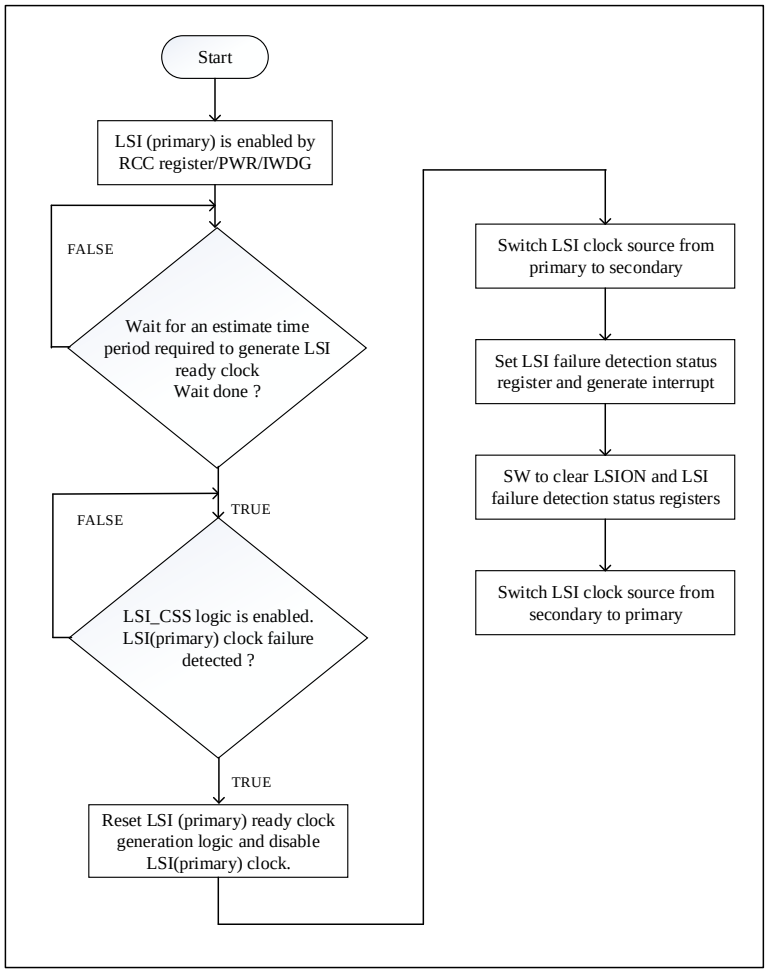
LSI has failed and the LSI clock is supplied by secondary LSI.

4. To restart the primary LSI, the following steps must be executed. If primary LSI restart is not required then system will continue to use the secondary LSI.
5. Set the bit “LSIFIE” in “RCC_CLKINT3” register to 1’b1.
6. Set the bit “LSIPFACK” bit in “RCC_BDCTRL” register to 1’b1.
7. Read the bit “LSIPFF” bit and check if the value is 1’b0. Repeat this step till the value of “LSIPFF” bit is 1’b0.
8. Set the bit “LSIPFACK” bit in “RCC_BDCTRL” register to 1’b0.
9. Set the “LSIEN” bit in “RCC_BDCTRL” register to 1’b1, reset primary LSI.

Figure 4-5 LSI CSS Control Flow



If the BDCTRL.LSIOVREN is configured as 1, the clock source can be switched via software according to the RCC_BDCTRL.LSICSSEN.

4.4.2.5 LSE clock

32.768 KHz Low Speed External Oscillator.

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The control logic of this oscillator is in the Backup power domain. This oscillator provides low power and accurate clock to peripherals in Backup and Retention power domain.

LSE Clock enable is controlled by the following sources.

- PWR control signal.
- RCC control registers(RCC_BDCTRL -> LSEEN and RCC_BDCTRL -> LSEBP).
- LSE CSS and offset detection Logic.

When the LSE clock is enabled, the LSE clock from analog module starts to toggle, however the initial few clock cycles are not reliable in terms of parameters such as duty cycle and frequency. To ensure that the duty cycle and frequency of the clock signal is stable, a delay is required, this delay value can be programmed in RCC_LSERDDL.DELAY. After this wait period (typically around 125ms) the LSE clock can be used for system operations.

The LSE enable procedure is as follows:

1. If you need to configure for bypass mode, set the bit “LSEBP” in “RCC_BDCTRL” register to 1’b1, otherwise set to 1’b0.
2. Set the bitfield “DELAY” in “RCC_LSERDDL” register to a pre-determined value.
3. Set the bit “LSERDCNTEN” in “RCC_BDCTRL” register to 1’b0.
4. Set the bit “LSELDOEN” in “RCC_BDCTRL” register to 1’b1.
5. Wait for 60us.
6. Set the bit “da_lse_agcopt” to 1’b1 (AFEC->TRIMR7 |=0x00400000; only for Oscillator Mode)
7. Set the bit “LSEEN” in “RCC_BDCTRL” register to 1’b1.
8. Set the bit “LSERDEN” in “RCC_BDCTRL” register to 1’b1.
9. Wait for pre-determined time (10us).
10. Set the bit “LSERDCNTEN” in “RCC_BDCTRL” register to 1’b1.
11. Read the bits “LSERDF” and “AFELSERDF” in “RCC_BDCTRL” register. Check if these bits are set to 1’b1. Repeat this step till these bits are set to 1’b1.

4.4.2.5.1 LSE Clock Security System (LSE CSS)

The clock security system can be enabled by software via the RCC_BDCTRL.LSECSSEN bit.

The clock offset detection can be enabled by software via the RCC_BDCTRL.LSECSSEN and RCC_LSEOS.LSEOSEN bit.

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The LSE Clock failure and offset detection events are stored in RCC status registers and also generate interrupts. This event is also used as a wake up source from system low power states such as Stop2 and Standby.

Clock Offset Detection

The LSE clock offset detection is divided into two phases.

- LSE clock frequency calibration phase.
- LSE clock frequency offset detection phase.

LSE clock frequency calibration phase:

This phase is enabled by RCC_LSEOS.LSECALCNTEN. In this phase, the LSE clock is divided by 128 and a calibration counter is used to count the number of LSI clock pulses in half cycle of the LSE/128 clock. This calibration count value is stored in RCC_HSEOS.LSECALCNT, and write RCC_LSEOS.LSEOSTHR according to the LSE clock frequency.

For example, when the LSE is 32.768K, then the desired LSECALCNT = 32K/(32.7368K/128)*0.5 = 62.5, LSEOSTHR configured as 5.

LSE clock frequency offset detection phase:

This phase is enabled by RCC_LSEOS.LSEOSEN. In this phase, offset counter is used to count the number of LSI clock pulses in half cycle of the LSE/128 clock. Compare the offset counter value with the calibration counter to determine if a 10% offset exists.

Programming Sequence to detect 10% offset in LSE clock.

1. If LSI clock is disabled then execute the sequence to enable LSI clock.
2. Execute the sequence to enable LSE clock.
3. Set the bit “LSECALCNTEN” in “RCC_LSEOS” register to 1’b1.
4. Read the bit “LSECALCNTF’ in “RCC_LSEOS” register and check if it is set to 1’b1. Repeat this step till this bit is set to 1’b1.
5. Read the bit field “LSECALCNT” in “RCC_LSEOS” register. The value strored in this register can be used to verify the frequency of LSE clock.
6. Write the bit field “LSEOSTHR” in “RCC_LSEOS” register with threshold value corresponding to the LSE frequency. Refer to RCC register file for the threshold values.
7. Set the bit “LSEOSEN” in “RCC_LSEOS” register to 1’b1.
8. Set the bit “LSECSSEN” in “RCC_BDCTRL” register to 1’b1.
9. Set the bit “LSECSSIE” in “RCC_CLKINT1” register to 1’b1.
10. If an offset greater than or equal to 10% is detected on LSE clock frequency then LSE CSS interrupt will be

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asserted and the flag “LSECSSIF” will be set in the “RCC_CLKINT1” register. The bit “LSECSSF” in “RCC_BDCTRL” register will be set to 1’b1. Read these two bits to confirm that LSE CSS is detected.

11. Read the bit “LSEOSF” in “RCC_LSEOS” register. This bit will be set to 1’b1 if frequency offset is detected.
12. Set the bits “LSELDOEN” and “LSEEN” in RCC_BDCTRL register to 1’b0.
13. Set the bit “LSECSSEN” in “RCC_BDCTRL” register to 1’b0.
14. Set the bit “LSECSSIC” in “RCC_CLKINT1” register to 1’b1.
15. Set the bit “LSEOSEN” in “RCC_LSEOS” register to 1’b0.
16. Set the bit “LSECALCNTEN” in “RCC_LSEOS” register to 1’b0.

4.4.2.6 PLL clock

400~800 MHz PLL(n)(n=1,2,3) & 400 MHz ~1.25GHz SHRPLL.

The control logic of this oscillator is in the Core power domain. HSI, MSI and HSE clocks can be configured as source clock to the plls. It has 4 plls.

- PLL1: Max frequency 800 MHz, this PLL is used as a system clock source and kernel clock source by certain peripherals.
- PLL2: Max frequency 800 MHz, this PLL is used as a system clock source and kernel clock source by certain peripherals.
- PLL3: Max frequency 800 MHz, this PLL is used as a kernel clock source by certain peripherals.
- SHRPLL: Max frequency 1.25 GHz, this PLL is used as a kernel clock source by SHRTIM peripheral.

PLL1, PLL2 and PLL3 clock outputs are further divided by configurable digital dividers andthen used as system clock or peripheral kernel clocks. SHRPLL clock output is divided by 4 inside AFE to generate 312.5 MHz clock for SHRTIM peripheral.

As shown in Figure 4-4, The PLL output frequency is generated with the following formula:

$$Fpllout = Fin * CLKF[25:0]/16384/(CLKR[5:0]+1)$$

In addition, BWAJ[11:0] = CLKF[25:0]/32768 – 1.

The CLKF, CLKR and BWAJ need to be configured with different parameters to ensure that the PLL achieves optimal performance, and the algorithmic code is given in the development kit driver.

PLL1, PLL2 and PLL3 typical configuration values are shown in the table below, or you can look up the table and configure the registers directly:

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Table 4-2 PLL Typical Parameters

Fin(MHz)	Fpllout(MHz)	CLKR[5:0]	CLKF[25:0]	BWADJ[11:0]
64	500	6'h00	26'h001F400	12'h002
64	720	6'h00	26'h002D000	12'h004
64	800	6'h00	26'h0032000	12'h005
64	624	6'h00	26'h0027000	12'h003
64	1250	6'h00	26'h004E200	12'h008
64	640	6'h00	26'h0028000	12'h004
64	532	6'h00	26'h0021400	12'h003
64	600	6'h00	26'h0025800	12'h003
64	400	6'h00	26'h0019000	12'h002
64	440	6'h00	26'h001B800	12'h002
64	528	6'h00	26'h0021000	12'h003
64	650	6'h00	26'h0028A00	12'h004
64	625	6'h00	26'h0027100	12'h003
64	480	6'h00	26'h001E000	12'h002
64	666	6'h00	26'h0029A00	12'h004
64	700	6'h00	26'h002BC00	12'h004
48	800	6'h02	26'h00C8000	12'h018
48	720	6'h00	26'h003C000	12'h006
48	640	6'h02	26'h00A0000	12'h013
48	624	6'h00	26'h0034000	12'h005
48	1250	6'h02	26'h0138800	12'h026
48	500	6'h02	26'h007D000	12'h00E
48	532	6'h02	26'h0085000	12'h00F
48	600	6'h00	26'h0032000	12'h005
48	440	6'h02	26'h006E000	12'h00C
48	528	6'h00	26'h002C000	12'h004
48	650	6'h02	26'h00A2800	12'h013
48	625	6'h02	26'h009C400	12'h012
48	480	6'h00	26'h0028000	12'h004
48	666	6'h00	26'h0037800	12'h005
48	700	6'h02	26'h00AF000	12'h014
48	400	6'h02	26'h0064000	12'h00B
48	450	6’h00	26'h0025800	12'h003
32	800	6’h00	26’h0064000	12’h00B
32	720	6’h00	26’h005A000	12’h00A
32	640	6’h00	26’h0050000	12’h009
32	624	6’h00	26’h004E000	12’h008
32	1250	6’h00	26’h009C400	12’h012

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32	500	6’h00	26’h003E800	12’h006
32	532	6’h00	26’h0042800	12’h007
32	600	6’h00	26’h004B000	12’h008
32	440	6’h00	26’h0037000	12’h005
32	528	6’h00	26’h0042000	12’h007
32	650	6’h00	26’h0051400	12’h009
32	625	6’h00	26’h004E200	12’h008
32	480	6’h00	26’h003C000	12’h006
32	666	6’h00	26’h0053400	12’h009
32	700	6’h00	26’h0057800	12’h009
32	400	6’h00	26’h0032000	12’h005
32	450	6’h00	26’h0038400	12’h006
25	800	6’h00	26’h0080000	12’h00F
25	720	6’h04	26’h0240000	12’h047
25	640	6’h04	26’h0200000	12’h03F
25	624	6’h018	26’h09C0000	12’h137
25	1250	6’h00	26’h00C8000	12’h018
25	500	6’h00	26’h0050000	12’h009
25	532	6’h018	26’h0850000	12’h109
25	600	6’h00	26’h0060000	12’h00B
25	440	6’h04	26’h0160000	12’h02B
25	528	6’h018	26’h0840000	12’h0107
25	650	6’h00	26’h0068000	12’h00C
25	625	6’h00	26’h0064000	12’h00B
25	480	6’h04	26’h0180000	12’h02F
25	666	6’h018	26’h0A68000	12’h14C
25	700	6’h00	26’h0070000	12’h00D
25	400	6’h00	26’h0040000	12’h007
25	450	6’h00	26’h0048000	12’h008
16	800	6'h00	26'h00C8000	12'h018
16	720	6'h00	26'h00B4000	12'h015
16	624	6'h00	26'h009C000	12'h012
16	1250	6'h00	26'h0138800	12'h026
16	500	6'h00	26'h007D000	12'h00E
16	640	6'h00	26'h00A0000	12'h013
16	532	6'h00	26'h0085000	12'h00F
16	600	6'h00	26'h0096000	12'h011
16	440	6'h00	26'h006E000	12'h00C
16	528	6'h00	26'h0084000	12'h00F
16	650	6'h00	26'h00A2800	12'h013
16	625	6'h00	26'h009C400	12'h012
16	480	6'h00	26'h0078000	12'h00E

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16	666	6'h00	26'h00A6800	12'h013
16	700	6'h00	26'h00AF000	12'h014
16	400	6'h00	26'h0064000	12'h00B
16	450	6'h00	26'h0070800	12'h00D
8	800	6'h00	26'h0190000	12'h031
8	500	6'h00	26'h00FA000	12'h01E

4.4.2.6.1 PLL failure detection

The PLL failure detection logic is enabled by RCC_PLLFD.PLL(n)FEN(n=1,2,3) or RCC_PLLFD.SHRPLLFEN.

If the bit RCC_CLKINT3.PLL(n)LKFIE set to 1'b1, The lock failure event is recorded in the RCC_CLKINT3 register and also used to generate non maskable interrupt(NMI).

Perform the following in the interrupt:

- Read the bit "RCC_CLKINT3.PLL(n)LKFIF". Check if the read value of this bit 1'b1
- Read the bit "RCC_PLLFD.PLL(n)FF". Check if the read value of this bit 1'b0
- Write 1'b1 to bit "RCC_CLKINT3.PLL(n)LKFIC" to clear the interrupt flag

If PLL1 was selected as system clock source, then upon lock failure the system clock is switched to HSI clock. This can be confirmed by reading the bits "SCLKSTS" in "RCC_SRCCTRL1" register.

If PLL2 was selected as M7 & AXI clock source in mode 1 & 2, then upon lock failure the M7 & AXI clocks are switched to system clock. This can be confirmed by reading the bits "M7HYPSEL" & "AXIHYPSEL" in "RCC_SRCCTRL2" register.

4.4.2.7 I/O clocks

Certain clocks of modules such as Ethernet, SDRAM, MIPI_DSI etc are provieded externally through the I/O interface.

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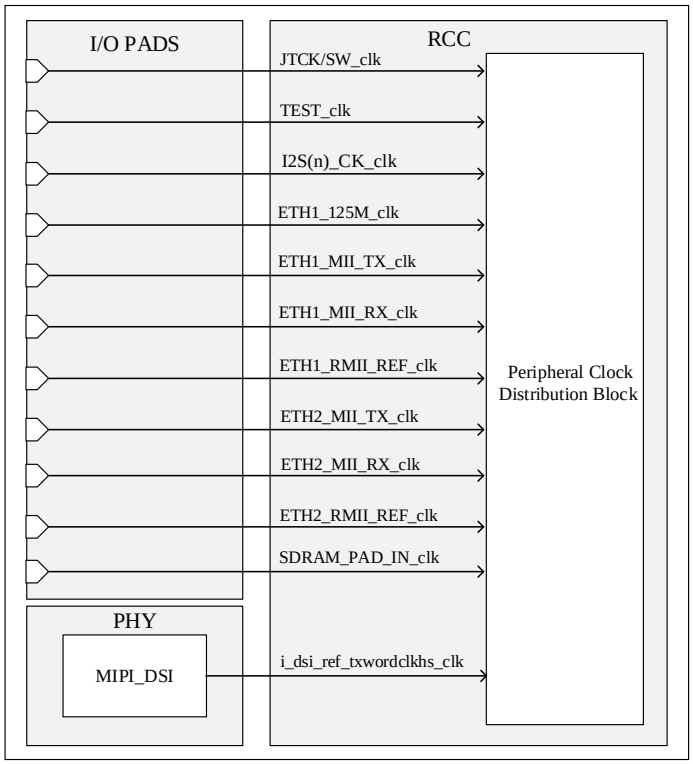
Figure 4-6 I/O Clocks



4.4.3 System bus and cpu clock configuration

After system power-up and system reset (NRST) events, the M4 CPU clock, M7 CPU clock and all bus (AHB/APB/AXI) clocks will be supplied by HSI clock source. Later software can program RCC registers to swtich system clock to PLL and there by allow system to function in the following clock modes. Software can also program the system clock (M4 CPU, M7 CPU and bus clocks) source to be HSE or MSI.

Table 4-3 System Clock Modes

Operation Modes	Processor and Bus Max frequencies (MHz)					Clock source for Max frequncies			Comments
	CM7	AXI & AHB6	CM4 & AHB(1,2,5)	APB6	APB(1,2,5)	CM7	AXI & AHB6	CM4 & AHB(1,2,5)	
Mode 2	600	300	300	150	150	PLL2A	PLL1A	PLL1A	AXI/AHB from same pll
Mode 1	600	300	300	150	150	PLL2A	PLL2A	PLL1A	AXI/CM7 from same pll
Mode 0	600	300	300	150	150	PLL1A	PLL1A	PLL1A	All from same pll

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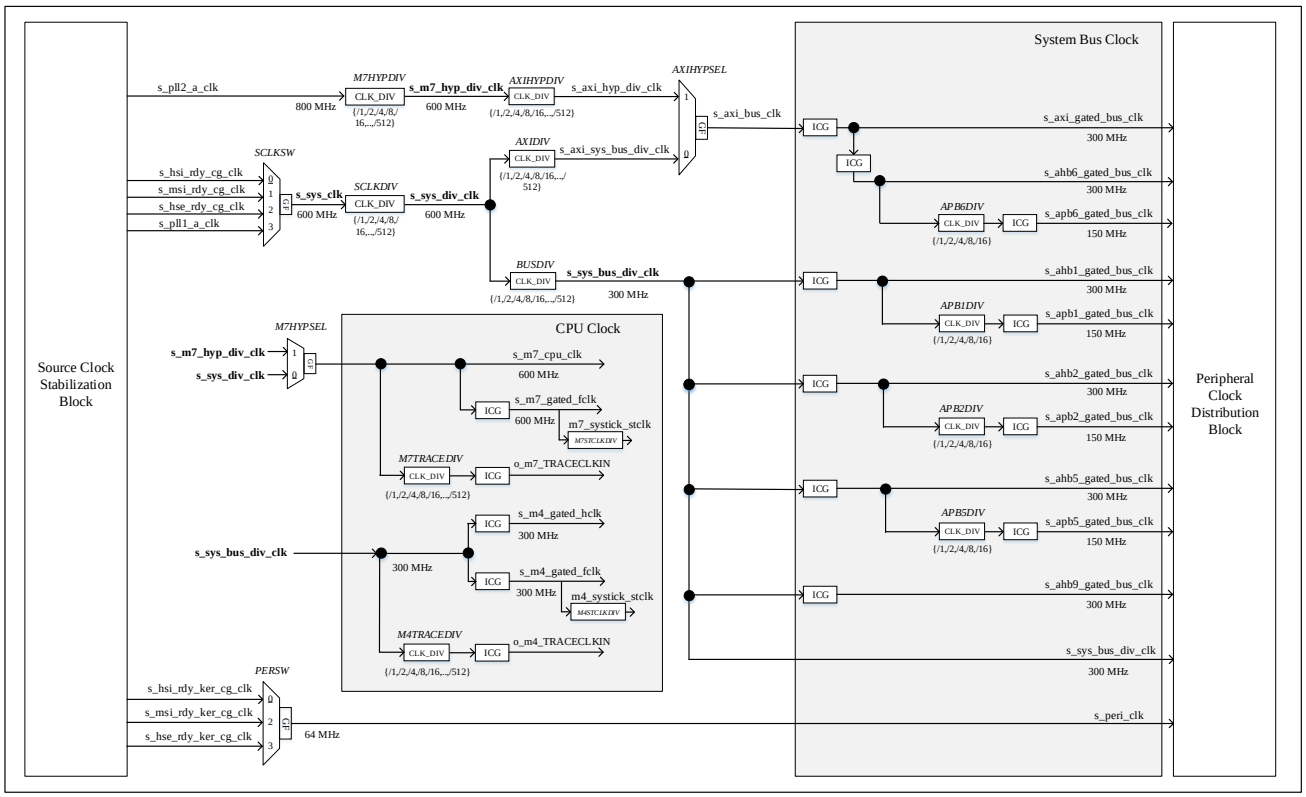
Figure 4-7 System bus and CPU Clocks



4.4.3.1 Set system clocks to Mode 0

Programming Sequence to set the system clocks to Mode 0 (0.9V) after power up or after NRST reset

1. Set the bit fields “AXIDIV[3:0]”, “AXIHYPDIV[3:0]” and “BUSDIV[3:0]” in RCC_SYSBUSDIV1 register to 4’b0001.
2. Wait for 1us.
3. Set the bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register to 3’b100.
4. Set the bit “PLL1LDOEN” to 1’b1 in “RCC_PLL1CTRL1” register.
5. Wait for 10us and set the bit “PLL1PD” to 1’b0 in “RCC_PLL1CTRL1” register.
6. Set the bit field “PLL1SRC[1:0]” to 2’b00 in “RCC_PLL1CTRL1” register.
7. Wait for 10us and set the bit “PLL1RST” to 1’b0 in “RCC_PLL1CTRL1” register.
8. Read the bit “PLL1PHLK” in “RCC_PLL1CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL1PHLK” bit is set to 1’b1.
9. Set the bit “PLL1EN” in “RCC_PLL1CTRL1” register to 1’b1.
10. Wait for 1us and set the bit field “PLL1ADIV[5:0]” in “RCC_PLL1DIV” register to 6’b000001”.
11. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b11.
12. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if this bit field is set to 2’b11.

Once the above steps are completed successfully, the CM4 system clock (s_sys_bus_div_clk), AHB(1,2,5), AXI and

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AHB6 clocks are all set to 300 MHz. APB(1,2,5,6) clocks are set to 150 MHz. CM7 clock is set to 600 MHz.The clock source of CM7, CM4 system clock and AXI clocks will be PLL1.

4.4.3.2 Set system clocks to Mode 1

Programming Sequence to set the system clocks to Mode 1 (0.9V) after power up or after NRST reset

1. Set the bit fields “AXIDIV[3:0]”, “AXIHYPDIV[3:0]” and “BUSDIV[3:0]” in “RCC_SYSBUSDIV1” register to 4’b0001.
2. Wait for 1us.
3. Set the bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register to 3’b100.
4. Set the bit “PLL1LDOEN” to 1’b1 in “RCC_PLL1CTRL1” register.
5. Wait for 10us and set the bit “PLL1PD” to 1’b0 in “RCC_PLL1CTRL1” register.
6. Set the bit field “PLL1SRC[1:0]” to 2’b00 in “RCC_PLL1CTRL1” register.
7. Wait for 10us and set the bit “PLL1RST” to 1’b0 in “RCC_PLL1CTRL1” register.
8. Read the bit “PLL1PHLK” in “RCC_PLL1CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL1PHLK” bit is set to 1’b1.
9. Set the bit “PLL1EN” in “RCC_PLL1CTRL1” register to 1’b1.
10. Set the bit field “PLL1ADIV[5:0]” in “RCC_PLL1DIV” register to 6’b000001”.
11. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b11.
12. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if this bit field is set to 2’b11.
13. Set the bit field “PLL2BWAJ[11:0]” to 12’h004 in “RCC_PLL2CTRL1” register.
14. Set the bit fields “PLL2CLKR[5:0]” to 6’h0 and “PLL2CLKF[25:0]” to 26’h0025800 in “RCC_PLL2_CR2” register.
15. Set the bit “PLL2LDOEN” to 1’b1 in “RCC_PLL2CTRL1” register.
16. Wait for 10us and set the bit “PLL2PD” to 1’b0 in “RCC_PLL2CTRL1” register.
17. Set the bit field “PLL2SRC[1:0]” to 2’b00 in “RCC_PLL2CTRL1” register.
18. Set the bit “PLL2RST” to 1’b0 in “RCC_PLL2CTRL1” register.
19. Read the bit “PLL2PHLK” in “RCC_PLL2CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL2PHLK” bit is set to 1’b1.
20. Set the bit “PLL2EN” in “RCC_PLL2CTRL1” register to 1’b1.
21. Wait for 1us and set the bit field “PLL2ADIV[5:0]” in “RCC_PLL2DIV” register to 6’b000001”.
22. Set the bits “M7HYPSEL” and “AXIHYPSEL” bits to 1’b1 in “RCC_SRCCTRL2” register.

Once the above steps are completed successfully, the CM4 system clock (s_sys_bus_div_clk) and AHB(1,2,5) clock is set to 300 MHz. CM7 clock is set to 600 MHz. AXI and AHB6 clocks are set to 300MHz. APB(1,2,5,6) clocks are set to 150 MHz. The clock source of CM7, AXI, AHB6 and APB6 clocks will be PLL2 and clock source of CM4 system clock (s_sys_bus_div_clk) and AHB(1,2,5) clock will be PLL1.

4.4.3.3 Set system clocks to Mode 2

Programming Sequence to set the system clocks to Mode 2 (0.9V) after power up or after NRST reset

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1. Set the bit fields “AXIDIV[3:0]”, “AXIHYPDIV[3:0]” and “BUSDIV[3:0]” in “RCC_SYSBUSDIV1” register to 4’b0001.
2. Wait for 1us.
3. Set the bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register to 3’b100.
4. Set the bit “PLL1LDOEN” to 1’b1 in “RCC_PLL1CTRL1” register.
5. Wait for 10us and set the bit “PLL1PD” to 1’b0 in “RCC_PLL1CTRL1” register.
6. Set the bit field “PLL1SRC[1:0]” to 2’b00 in “RCC_PLL1CTRL1” register.
7. Wait for 10us and set the bit “PLL1RST” to 1’b0 in “RCC_PLL1CTRL1” register.
8. Read the bit “PLL1PHLK” in “RCC_PLL1CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL1PHLK” bit is set to 1’b1.
9. Set the bit “PLL1EN” in “RCC_PLL1CTRL1” register to 1’b1.
10. Wait for 1us and set the bit field “PLL1ADIV[5:0]” in “RCC_PLL1DIV” register to 6’b000001”.
11. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b11.
12. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if this bit field is set to 2’b11.
13. Set the bit field “PLL2BWAJ[11:0]” to 12’h004 in “RCC_PLL2CTRL1” register.
14. Set the bit fields “PLL2CLKR[5:0]” to 6’h0 and “PLL2CLKF[25:0]” to 26’h0025800 in “RCC_PLL2CTRL2” register.
15. Set the bit “PLL2LDOEN” to 1’b1 in “RCC_PLL2CTRL1” register.
16. Wait for 10us and set the bit “PLL2PD” to 1’b0 in “RCC_PLL2CTRL1” register.
17. Set the bit field “PLL2SRC[1:0]” to 2’b00 in “RCC_PLL2CTRL1” register.
18. Wait for 10us and set the bit “PLL2RST” in “RCC_PLL2CTRL1” register to 1’b0.
19. Read the bit “PLL2PHLK” in “RCC_PLL2CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL2PHLK” bit is set to 1’b1.
20. Set the bit “PLL2EN” in “RCC_PLL2CTRL1” register to 1’b1.
21. Wait for 1us and set the bit field “PLL2ADIV[5:0]” to 6’b000001 in “RCC_PLL2DIV” register.
22. Set the bit “M7HYPSEL” to 1’b1 in “RCC_SRCCTRL2” register.

Once the above steps are completed successfully, the CM4 system clock (s_sys_bus_div_clk) and AHB(1,2,5) clock is set to 300 MHz. CM7 clock is set to 600 MHz. AXI and AHB6 clocks are set to 300 MHz. APB(1,2,5,6) clocks are set to 150 MHz. The clock source of CM7 will be PLL2 and clock source of CM4 system clock (s_sys_bus_div_clk) and AXI clock will be PLL1.

4.4.3.4 Switch on the PLL1/2/3 with HSI source

Programming Sequence to switch on the PLL1, PLL2 and PLL3 clock with HSI as the PLL source

1. Set the bit “HSIEN” in “RCC_SRCCTRL1” register to 1’b1.
2. Read the bit “HSIRDF” and “AFEHSIRDF” in “RCC_SRCCTRL1” register. Check if it is set to 1. Repeat this step till the bit “HSIRDF” is set to 1.
3. Steps 1 and 2 are performed by default after power up or after NRST reset.
4. Read “RCC_PLL1CTRL1” register and check if the “PLL1PHLK” bit is set to 1’b0, “PLL1EN” is set to 1’b0, “PLL1RST” bit is set to 1’b1 and “PLL1PD” bit is set to 1’b1 (default values). If this is not the case

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then set the bit “PLL1EN” to 1’b0, set the bit “PLL1RST” to 1’b1 and read the bit “PLL1PHLK” till it is set to 1’b0. Set the bit “PLL1PD” to 1’b1. (If PLL1 is selected as system clock then switch system clock to either HSI, MSI or HSE by following the respective sequence before executing this step).

5. Read “RCC_PLL1CTRL1” register and check if the “PLL1LDOEN” bit is set to 1’b1. If this is not the case then set the bit “PLL1LDOEN” to 1’b1.
6. Wait for 10us and set the bit “PLL1PD” to 1’b0 in “RCC_PLL1CTRL1” register.
7. Set the bit field “PLL1SRC[1:0]” in “RCC_PLL1CTRL1” register to 2’b00.
8. Set the bit field “PLL1BWAJ[11:0]” in “RCC_PLL1CTRL1” register to the required value.
9. Set the bit fields “PLL1CLKR[5:0]” and “PLL1CLKF[25:0]” in “RCC_PLL1CTRL2” register to the required value.
10. Wait for 10us and set the bit “PLL1RST” in “RCC_PLL1CTRL1” register to 1’b0.
11. Read the bit “PLL1PHLK” in “RCC_PLL1CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL1PHLK” bit is set to 1’b1.
12. Set the bit “PLL1EN” in “RCC_PLL1CTRL1” register to 1’b1.
13. Set the bit fields “PLL1ADIV[5:0]”, “PLL1B_DIV” and “PLL1C_DIV” in “RCC_PLL1DIV” register to appropriate clock division values.

Note 1: This sequence can also be applied to PLL2 and PLL3.

4.4.3.5 Switch on the PLL1/2/3 with MSI source

Programming Sequence to switch on the PLL1, PLL2 and PLL3 clock with MSI as the PLL source

1. Set the bit “MSIEN” in “RCC_SRCCTRL1” register to 1’b1.
2. Read the bit “MSIRDYF” and “AFEMSIRDF” in “RCC_SRCCTRL1” register. Check if it is set to 1. Repeat this step till the bit “MSIRDYF” is set to 1.
3. Read “RCC_PLL1CTRL1” register and check if the “PLL1PHLK” bit is set to 1’b0, “PLL1EN” is set to 1’b0, “PLL1RST” bit is set to 1’b1 and “PLL1PD” bit is set to 1’b1 (default values). If this is not the case then set the bit “PLL1EN” to 1’b0, set the bit “PLL1RST” to 1’b1 and read the bit “PLL1PHLK” till it is set to 1’b0. Set the bit “PLL1PD” to 1’b1. (If PLL1 is selected as system clock then switch system clock to either HSI, MSI or HSE by following the respective sequences before executing this step).
4. Read “RCC_PLL1CTRL1” register and check if the “PLL1LDOEN” bit is set to 1’b1. If this is not the case then set the bit “PLL1LDOEN” to 1’b1.
5. Wait for 10us and set the bit “PLL1PD” to 1’b0 in “RCC_PLL1CTRL1” register.
6. Set the bit field “PLL1SRC[1:0]” in “RCC_PLL1CTRL1” register to 2’b10.
7. Set the bit field “PLL1BWAJ[11:0]” in “RCC_PLL1CTRL1” register to the required value.
8. Set the bit fields “PLL1CLKR[5:0]” and “PLL1CLKF[25:0]” in “RCC_PLL1CTRL2” register to the required value.
9. Wait for 10us and set the bit “PLL1RST” in “RCC_PLL1CTRL1” register to 1’b0.
10. Read the bit “PLL1PHLK” in “RCC_PLL1CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL1PHLK” bit is set to 1’b1.
11. Set the bit “PLL1EN” in “RCC_PLL1CTRL1” register to 1’b1.

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12. Set the bit fields “PLL1ADIV[5:0]”, “PLL1BDIV[5:0]” and “PLL1CDIV[5:0]” in “RCC_PLL1DIV” register to appropriate clock division values.

Note 1: This sequence can also be applied to PLL2 and PLL3.

4.4.3.6 Switch on the PLL1/2/3 with HSE source

Programming Sequence to switch on the PLL1, PLL2 and PLL3 clock with HSE as the PLL source

1. Set the bit “HSEEN” in “RCC_SRCCTRL1” register to 1’b1.
2. Read the bit “HSERDF” in “RCC_SRCCTRL1” register. Check if it is set to 1. Repeat this step till the bit “HSERDF” is set to 1.
3. Read “RCC_PLL1CTRL1” register and check if the “PLL1PHLK” bit is set to 1’b0, “PLL1EN” is set to 1’b0, “PLL1RST” bit is set to 1’b1 and “PLL1PD” bit is set to 1’b1 (default values). If this is not the case then set the bit “PLL1EN” to 1’b0, set the bit “PLL1RST” to 1’b1 and read the bit “PLL1PHLK” till it is set to 1’b0. Set the bit “PLL1PD” to 1’b1. (If PLL1 is selected as system clock then switch system clock to either HSI, MSI or HSE by following the respective sequences before executing this step).
4. Read “RCC_PLL1CTRL1” register and check if the “PLL1LDOEN” bit is set to 1’b1. If this is not the case then set the bit “PLL1LDOEN” to 1’b1.
5. Wait for 10us and set the bit “PLL1PD” to 1’b0 in “RCC_PLL1CTRL1” register.
6. Set the bit field “PLL1SRC[1:0]” in “RCC_PLL1CTRL1” register to 2’b11.
7. Set the bit field “PLL1BWAJ[11:0]” in “RCC_PLL1CTRL1” register to the required value.
8. Set the bit fields “PLL1CLKR[5:0]” and “PLL1CLKF[25:0]” in “RCC_PLL1CTRL2” register to the required value.
9. Wait for 10us and set the bit “PLL1RST” in “RCC_PLL1CTRL1” register to 1’b0.
10. Read the bit “PLL1PHLK” in “RCC_PLL1CTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “PLL1PHLK” bit is set to 1’b1.
11. Set the bit “PLL1EN” in “RCC_PLL1CTRL1” register to 1’b1.
12. Set the bit fields “PLL1ADIV[5:0]”, “PLL1BDIV[5:0]” and “PLL1CDIV[5:0]” in “RCC_PLL1DIV” register to appropriate clock division values.

Note 1: This sequence can also be applied to PLL2 and PLL3.

4.4.3.7 Switch on the SHRPLL with HSI/MSI/HSE source

Programming Sequence to switch on the SHRPLL clock with HSI/MSI/HSE as the PLL source (after Power up or after NRST).

1. Execute the sequences to enable HSI/HSE/MSI clocks.
2. Set the bit “SHRPLLLDOEN” in “RCC_SHRPLLCTRL1” register to 1’b1.
3. Wait for 10us and set the bit “SHRPLLPD” in “RCC_SHRPLLCTRL1” register to 1’b0.
4. Set the bit field “SHRPLLSRC[1:0]” in “RCC_SHRPLLCTRL1” register to 2’b00/2’b10/2’b11 to select the SHRPLL clock source to HSI/MSI/HSE.

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5. Set the bit field “SHRPLLBWAJ[11:0]” in “RCC_SHRPLLCTRL1” register to the required value. Execute this step only if PLL output frequency requirement is different from default frequency (1.25GHz/4 = 312.5MHz), otherwise skip this step.
6. Set the bit fields “SHRPLLCLKR[5:0]” and “SHRPLLCLKF[25:0]” in “RCC_SHRPLLCTRL2” register to the required value. Execute this step only if PLL output frequency requirement is different from default frequency (1.25GHz/4 = 312.5MHz), otherwise skip this step.
7. Wait for 10us and set the bit “SHRPLLRST” in “RCC_PLL1CTRL1” register to 1’b0.
8. Read the bit “SHRPLLPHLK” in “RCC_SHRPLLCTRL1” register. Check if the bit is set to 1’b1. Repeat this step till the “SHRPLLPHLK” bit is set to 1’b1.
9. Set the bit “SHRPLLEN” in “RCC_SHRPLLCTRL1” register to 1’b1.

4.4.3.8 Switch system clock to HSI

Programming Sequence to switch system clock to HSI

1. Set the required prescalar values at “SCLKDIV[3:0]” and “BUSDIV[3:0]” bit fields in the “RCC_SYSBUSDIV1” register.
2. Set the required prescalar values at bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register.
3. Set the bit “HSIEN” in “RCC_SRCCTRL1” register to 1’b1.
4. Read the bit “HSIRDF” and “AFEHSIRDF” in “RCC_SRCCTRL1” register. Check if it is set to 1. Repeat this step till these two bits are set to 1.
5. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b00.
6. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if the read value of this bit field is 2’b00. Repeat this step till this bit field read value is 2’b00.
7. The above steps are performed by default after system power up or NRST reset.

4.4.3.9 Switch system clock to MSI

Programming Sequence to switch system clock to MSI

1. Set the required prescalar values at “SCLKDIV[3:0]” and “BUSDIV[3:0]” bit fields in the “RCC_SYSBUSDIV1” register.
2. Set the required prescalar values at bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register.
3. Set the bit “MSIEN” in “RCC_SRCCTRL1” register to 1’b1.
4. Read the bit “MSIRDYF” and “AFEMSIRDF” in “RCC_SRCCTRL1” register. Check if it is set to 1’b1. Repeat this step till these two bits are set to 1’b1.
5. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b01.
6. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if the read value of this bit field is 2’b01. Repeat this step till this bit field read value is 2’b01.

4.4.3.10 Switch system clock to HSE

Programming Sequence to switch system clock to HSE

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1. Set the required prescalar values at “SCLKDIV[3:0]” and “BUSDIV[3:0]” bit fields in the “RCC_SYSBUSDIV1” register.
2. Set the required prescalar values at bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register.
3. Set the bit “HSEEN” in “RCC_SRCCTRL1” register to 1’b1.
4. Read the bit “HSERDF” in “RCC_SRCCTRL1” register. Check if it is set to 1’b1. Repeat this step till the “HSERDF” bit is set to 1’b1.
5. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b10.
6. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if the read value of this bit field is 2’b10. Repeat this step till this bit field read value is 2’b10.

4.4.3.11 Switch system clock to PLL1

Programming Sequence to switch system clock to PLL1

1. Set the required prescalar values at “SCLKDIV[3:0]” and “BUSDIV[3:0]” bit fields in the “RCC_SYSBUSDIV1” register.
2. Set the required prescalar values at bit fields “APB1DIV[2:0]”, “APB2DIV[2:0]”, “APB5DIV[2:0]” and “APB6DIV[2:0]” in “RCC_SYSBUSDIV2” register.
3. Set the PLL1 source clock to either HSI, MSI or HSE by following the respective sequence.
4. Set the bit field “SCLKSW” in “RCC_SRCCTRL1” register to 2’b11.
5. Read the bit field “SCLKSTS” in “RCC_SRCCTRL1” register. Check if the read value of this bit field is 2’b11. Repeat this step till this bit field read value is 2’b11.

4.4.4 Peripheral clock configuration

In system, the peripheral clocks are divided into two categories.

Peripheral kernel clock: This clock can be sourced from system bus clocks, external clock or from system clock sources. This clock may not be synchronous to system bus clock. Programmable pre-scalars (dividers) and clock selection multiplexers are provided for kernel clock source selection and division.

Peripheral bus clock: This clock is derived from the system bus clocks, in order to access its registers. This clock is generally the AHB, APB or AXI clock depending on which bus the peripheral is connected to.

Each peripheral can be allocated to M4 or M7 CPU. The allocation information is programmed in RCC registers. A low power clock enable register is provided to each peripheral to enable/disable the kernel and bus clock in low power modes. The allocation register, low power clock enable register and M4/M7 CPU power modes are considered as inputs in the clock gating logic for each peripheral.

The clock gating control module has two integrated clock gates (ICG), one is used to gate the peripheral kernel clock and the other is used to gate the peripheral bus clock, Peripheral clock gating logic truth table

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Table 4-4 Peripheral clock gating logic truth table

Inputs			Outputs	
Cn_Perx_EN(1)	**Cn_Perx_LPEN**	**Cn_state**	**Perx_ker_clk_en**	**Perx_bus_clk_en**
0	X	X	0	0
1	X	Run	1	1
1	1	Sleep	1	1
1	0		0	0
1	0	Stop0/ Stop2/ Dgb_stop0/ Dbg_stop2	0	0
1	1		1	0
1	X	Standby/ Dbg_standby	0	0

Note: Perx indicates different peripherals, Cn indicates different cores (C1 is M7, C2 is M4)

Peripherals such as DMA(n), UART(n), GPIO(n), etc. do not need a specific kernel clock frequency, only needs to be configured for the peripherals bus clock(turn on the corresponding bus and enable bits).

Peripherals such as FDCAN(n), I2S(n), etc. require a clock fast enough to generate the correct communication rate, therefore a different kernel clock source needs to be selected. For that purpose the source can be selected among:

- PLL1 when the amount of active PLLs has to be reduced
- PLL2 or PLL3 if better flexibility is required. As an example, this solution allows changing the frequency bus via PLL1 without affecting the speed of some serial interfaces.
- HSI, MSI, HSE, LSI or LSE for low-power use-cases or when the peripheral has to quickly wake up from low power mode.

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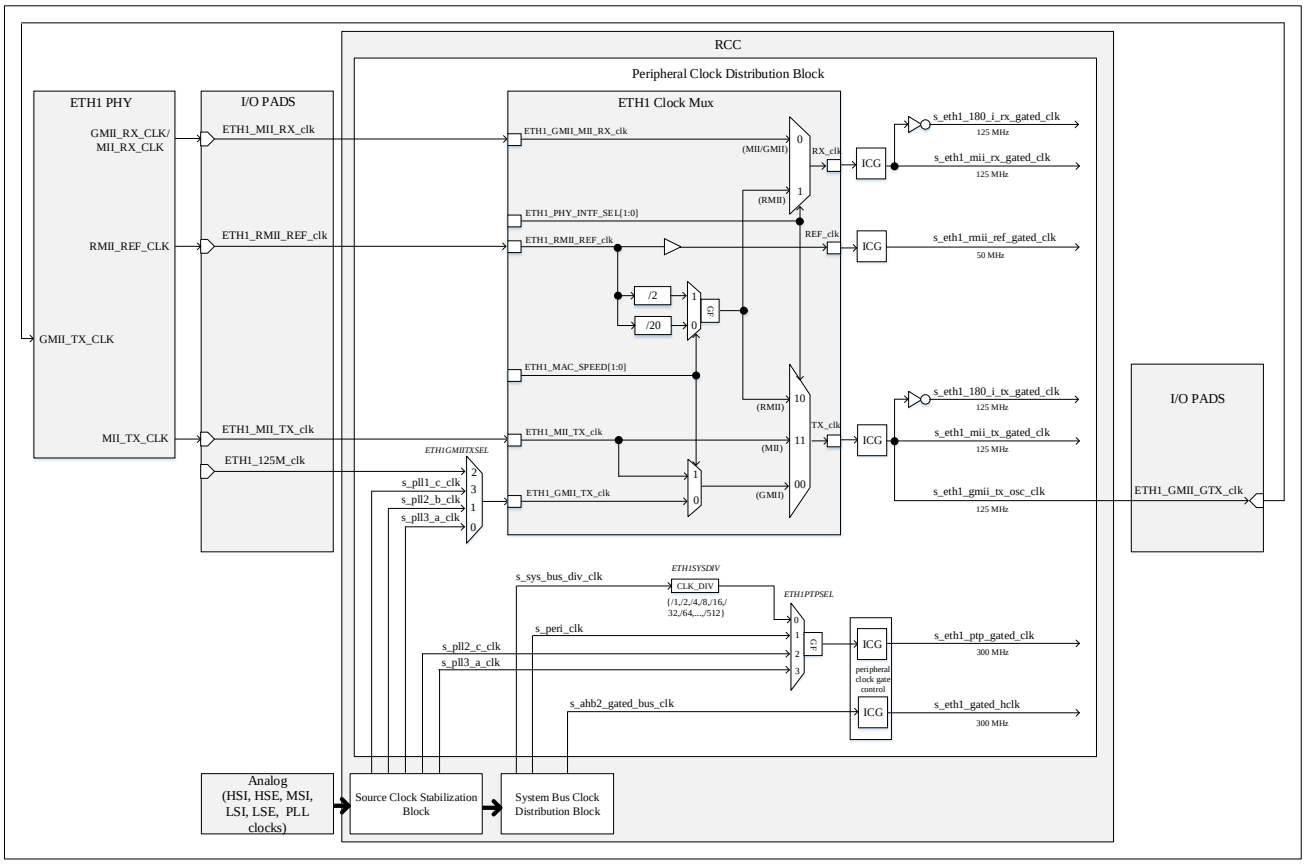
4.4.4.1 Ethernet

Figure 4-8 Ethernet1



Note: Enable module clock by configuring M7ETH2TXEN, M4ETH2TXEN, M7ETH2TXLPEN, M4ETH2TXLPEN, M7ETH2RXEN, M4ETH2RXEN, M7ETH2RXLPEN, M4ETH2RXLPEN, M7ETH2MACEN, M4ETH2MACEN, M7ETH2MACLPEN and M4ETH2MACLPEN

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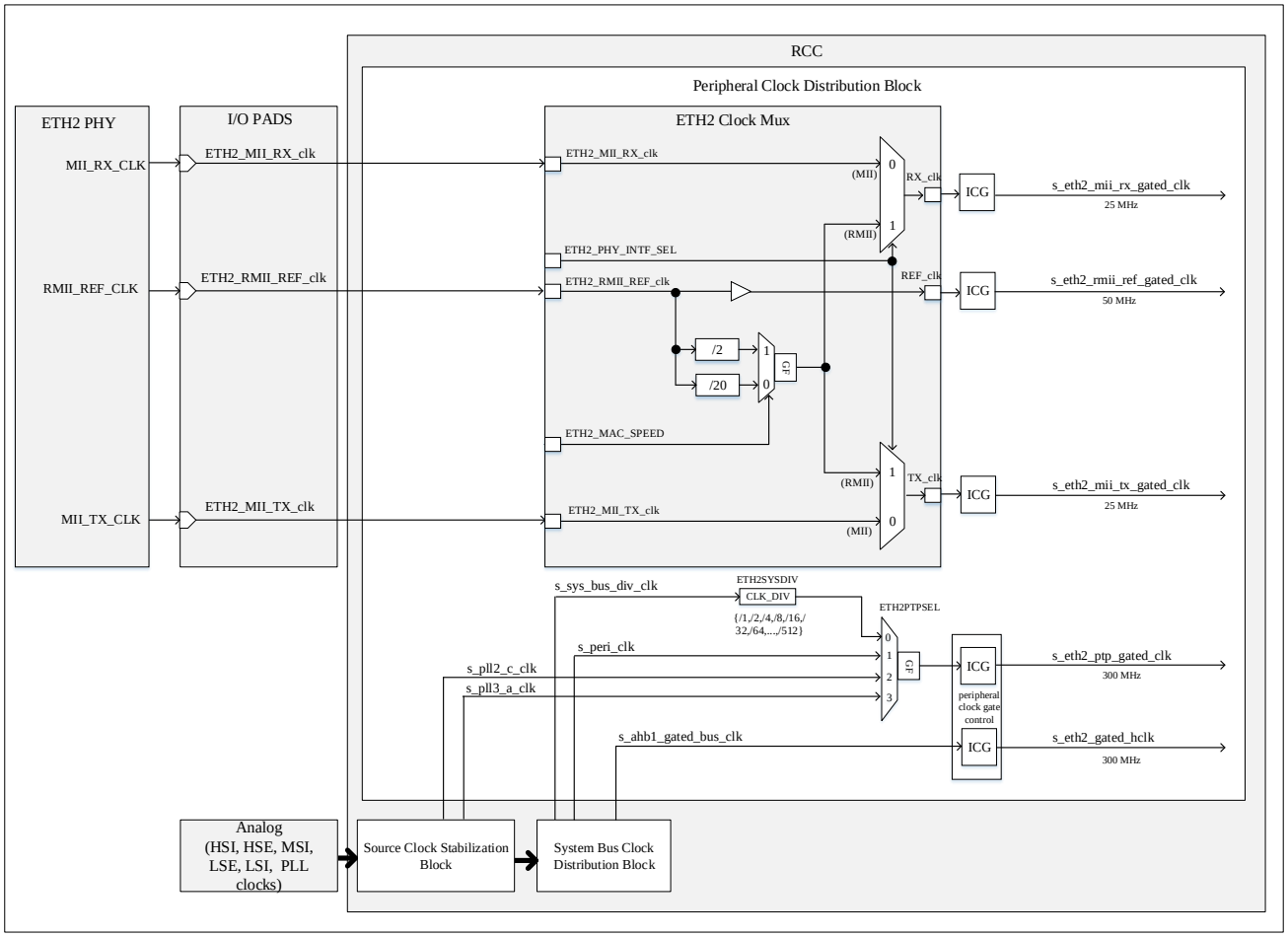
Figure 4-9 Ethernet2



Note: Enable module clock by configuring M7ETH1TXEN, M4ETH1TXEN, M7ETH1TXLPEN, M4ETH1TXLPEN, M7ETH1RXEN, M4ETH1RXEN, M7ETH1RXLPEN, M4ETH1RXLPEN, M7ETH1MACEN, M4ETH1MACEN, M7ETH1MACLPEN and M4ETH1MACLPEN

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4.4.4.2 SDMMC

Figure 4-10 SDMMC1

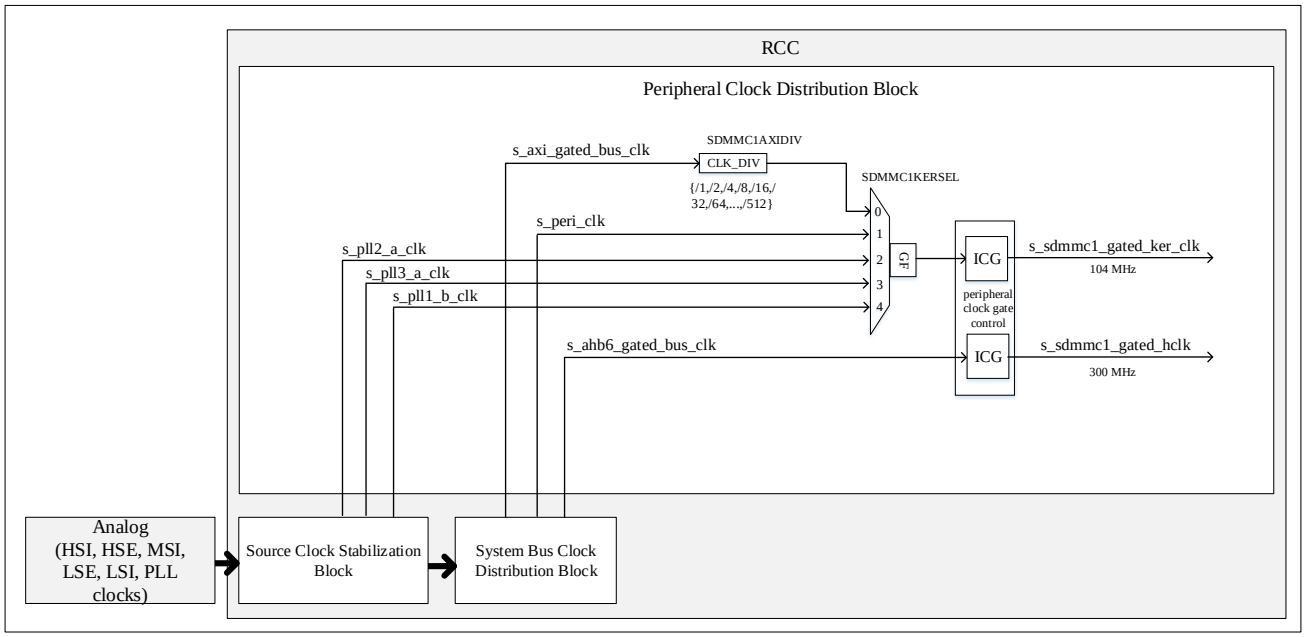
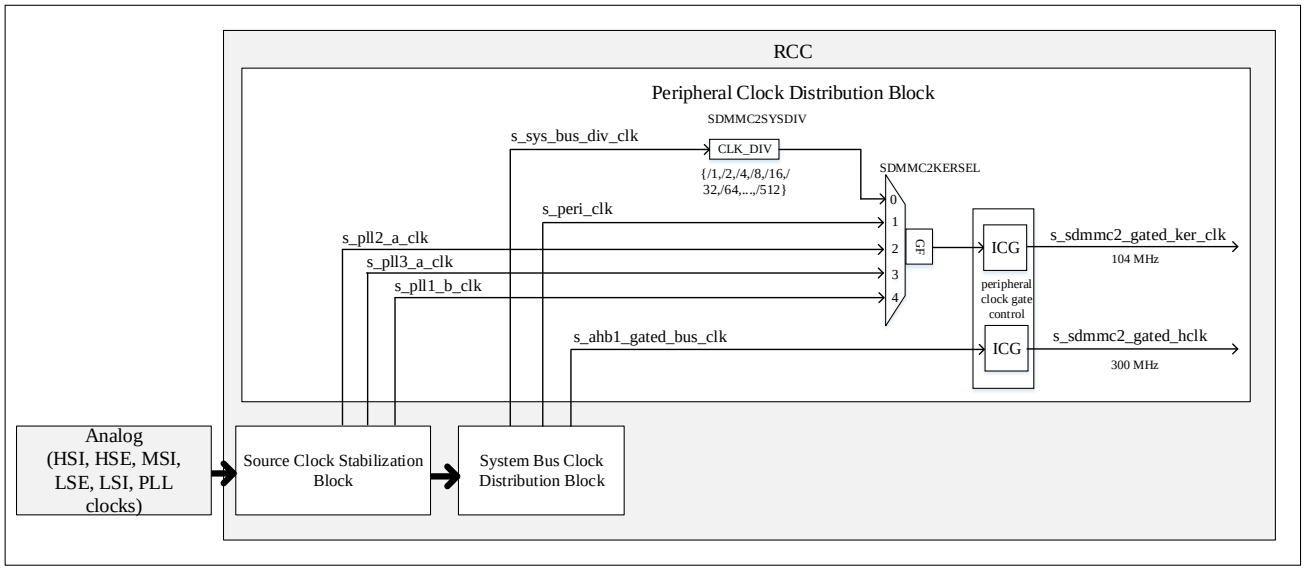


Figure 4-11 SDMMC2



4.4.4.3 USB

Note: ref_clk output to USB PHY

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Figure 4-12 USB1

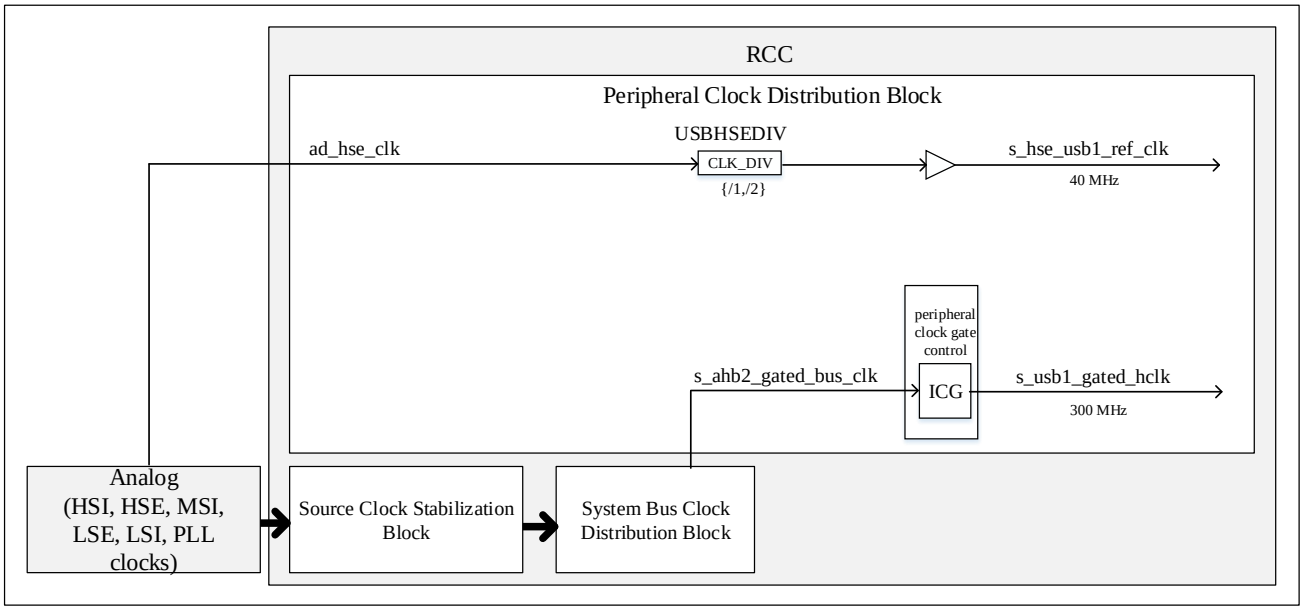
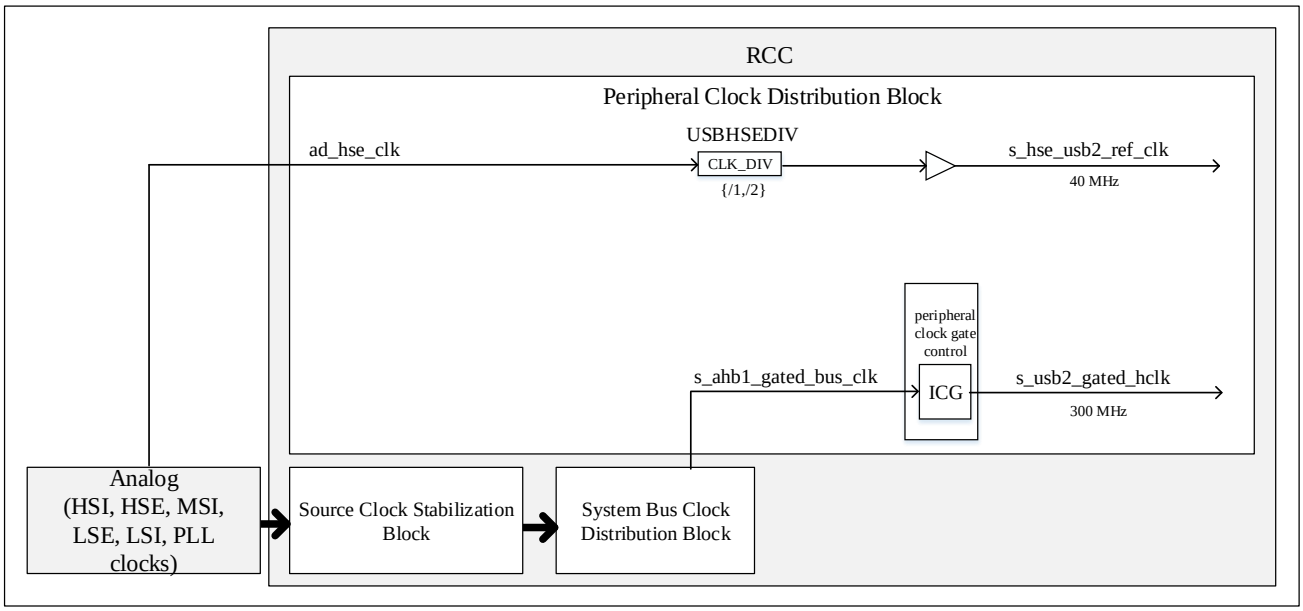


Figure 4-13 USB2



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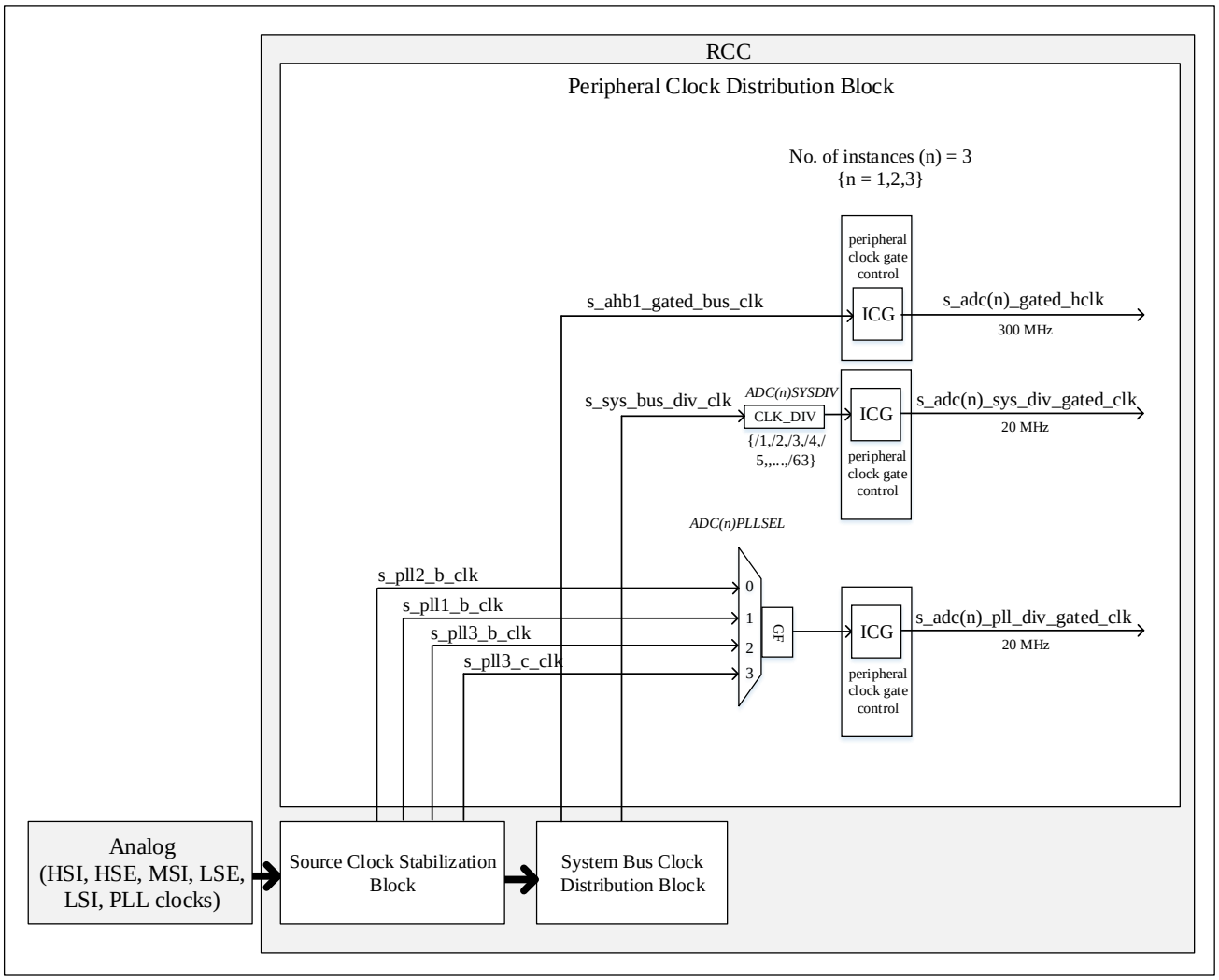
4.4.4.4 ADC

Figure 4-14 ADC(n) {n=1,2,3}



Note: Enable module clock by configuring M7ADC(n)PLLEN, M4ADC(n)PLLEN, M7ADC(n)PLLLPEN, M4ADC(n)PLLLPEN, M7ADC(n)SYSEN, M4ADC(n)SYSEN, M7ADC(n)SYSLPEN, M4ADC(n)SYSLPEN, M7ADC(n)BUSEN, M4ADC(n)BUSEN, M7ADC(n)BUSLPEN, M4ADC(n)BUSLPEN {n=1,2,3}.

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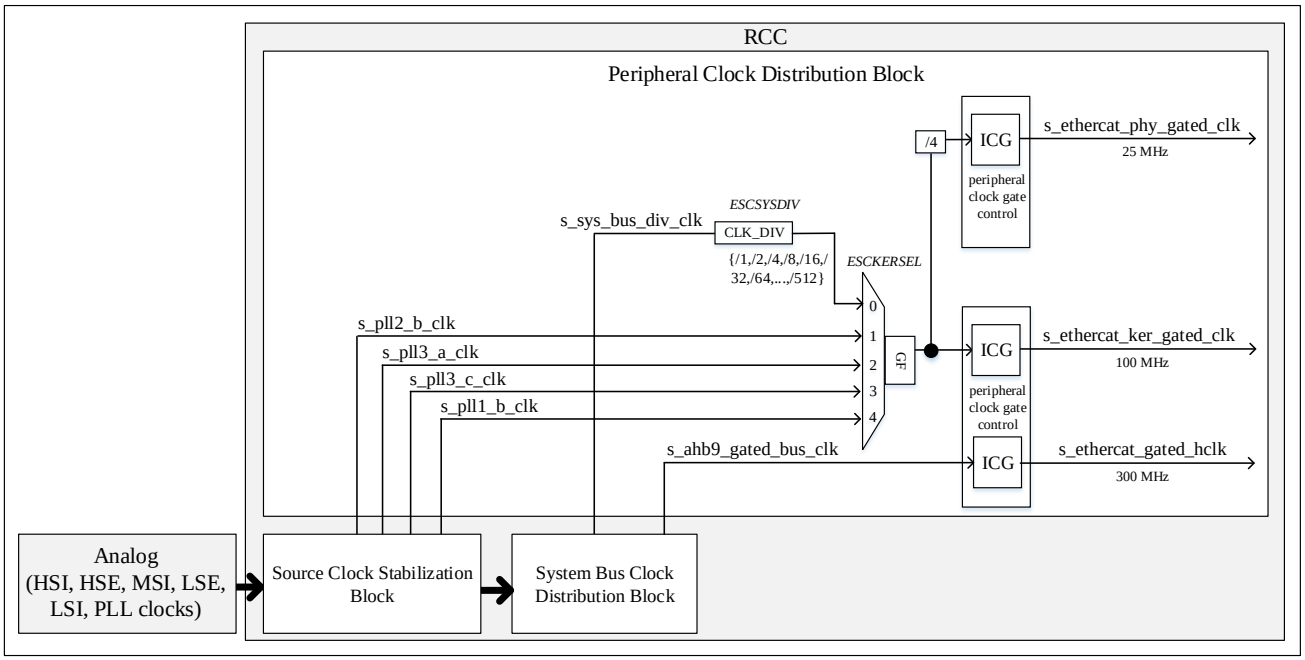
4.4.4.5 Ethercat

Figure 4-15 Ethercat



4.4.4.6 I2C

Figure 4-16 I2C(n) {n=1,2,3}

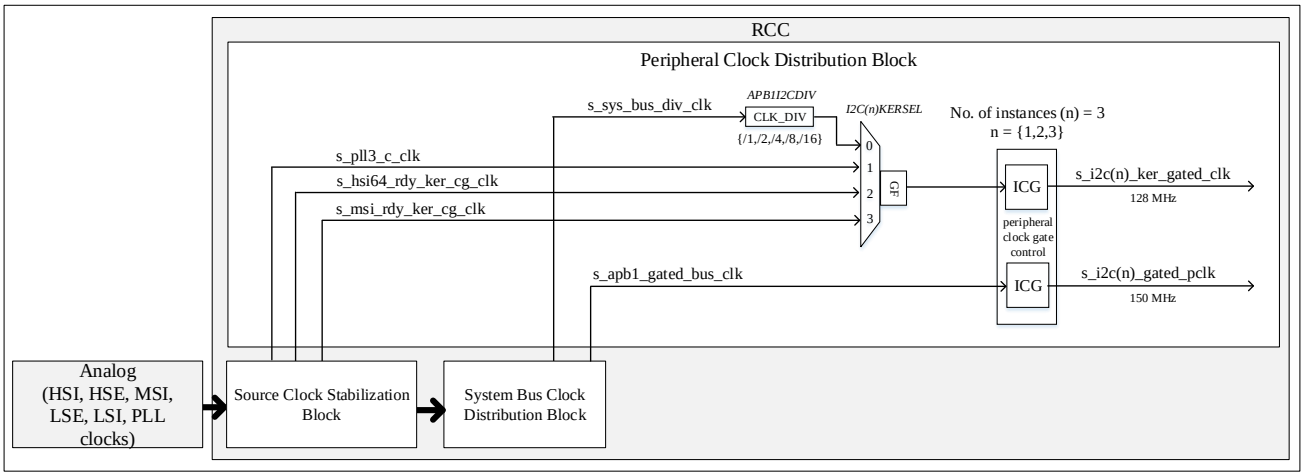


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Figure 4-17 I2C(n) {n=4,5,6}

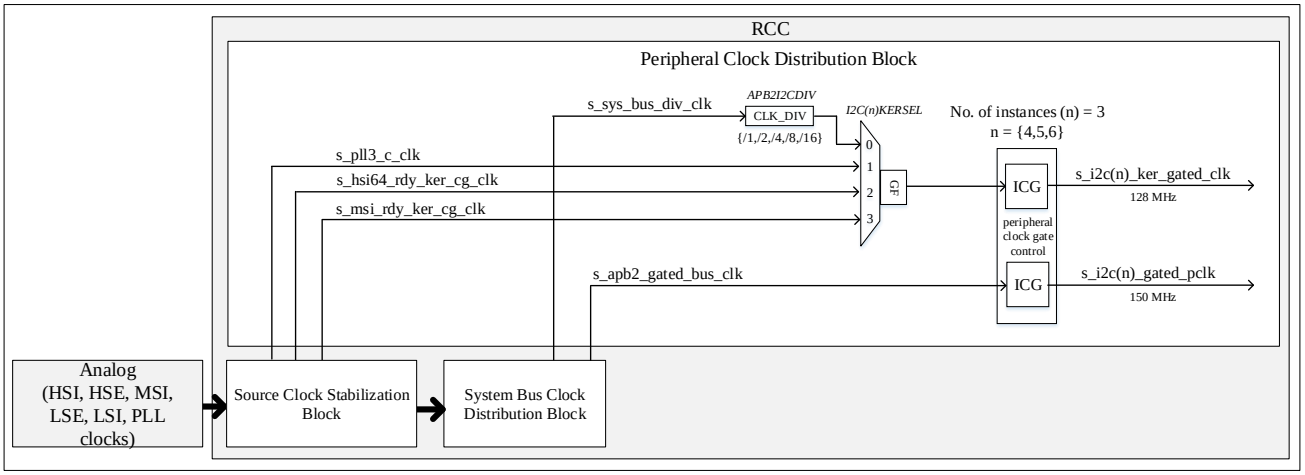
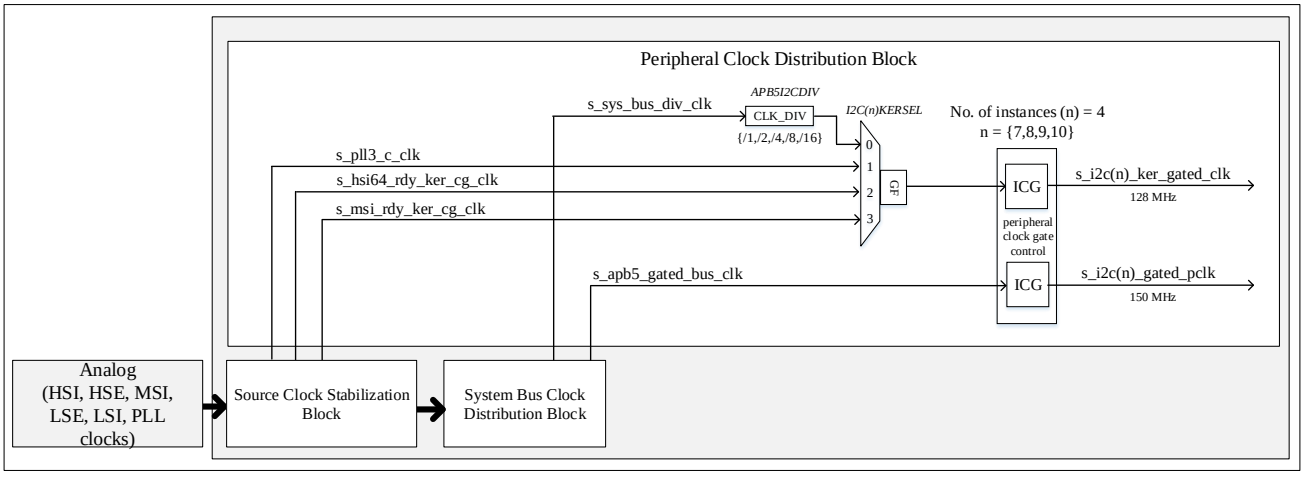


Figure 4-18 I2C(n) {n=7,8,9,10}



4.4.4.7 FDCAN

Note: The FDCAN kernel clock should be configured to the following frequencies: 20M, 40M, or 80M, and cannot be higher than the corresponding APBx clock frequency (x=1, 2)

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Figure 4-19 FDCANn) {n=1,2,5,6}

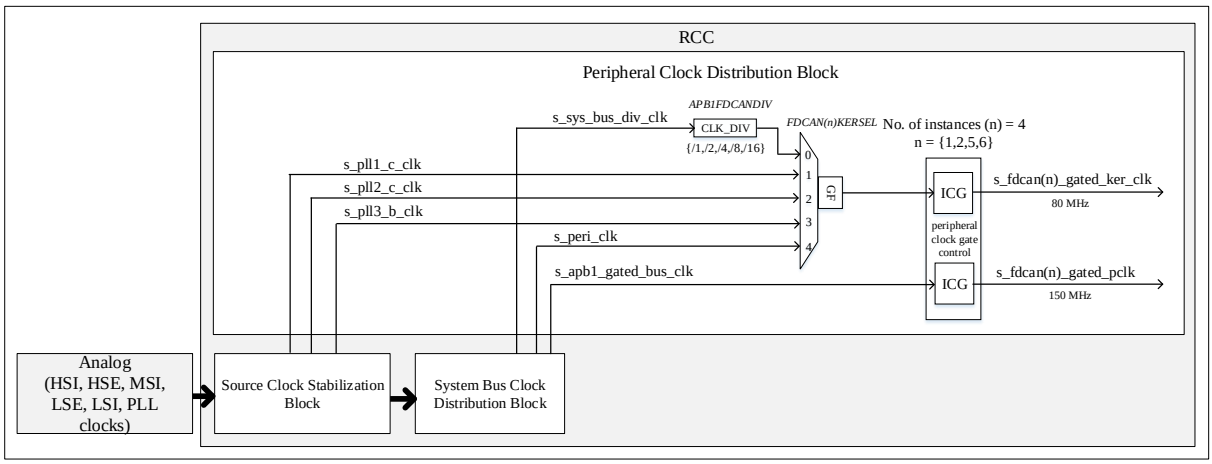
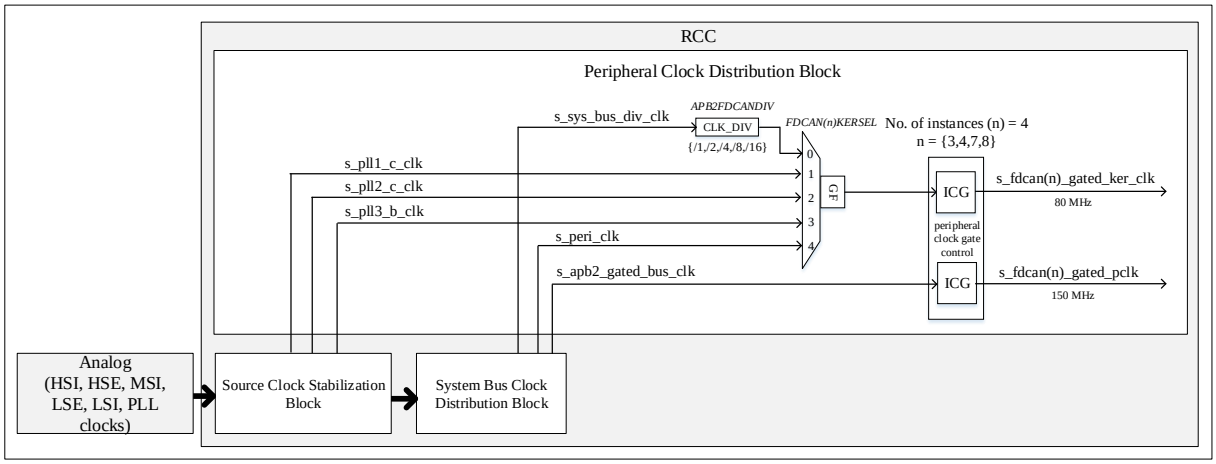


Figure 4-20 FDCAN(n) {n=3,4,7,8}



4.4.4.8 DSMU

Note: ker_a_clk is DSMU ACLK(audio clk), ker_clk is DSMU_CLK(filter_clk), See DSMU section for details.

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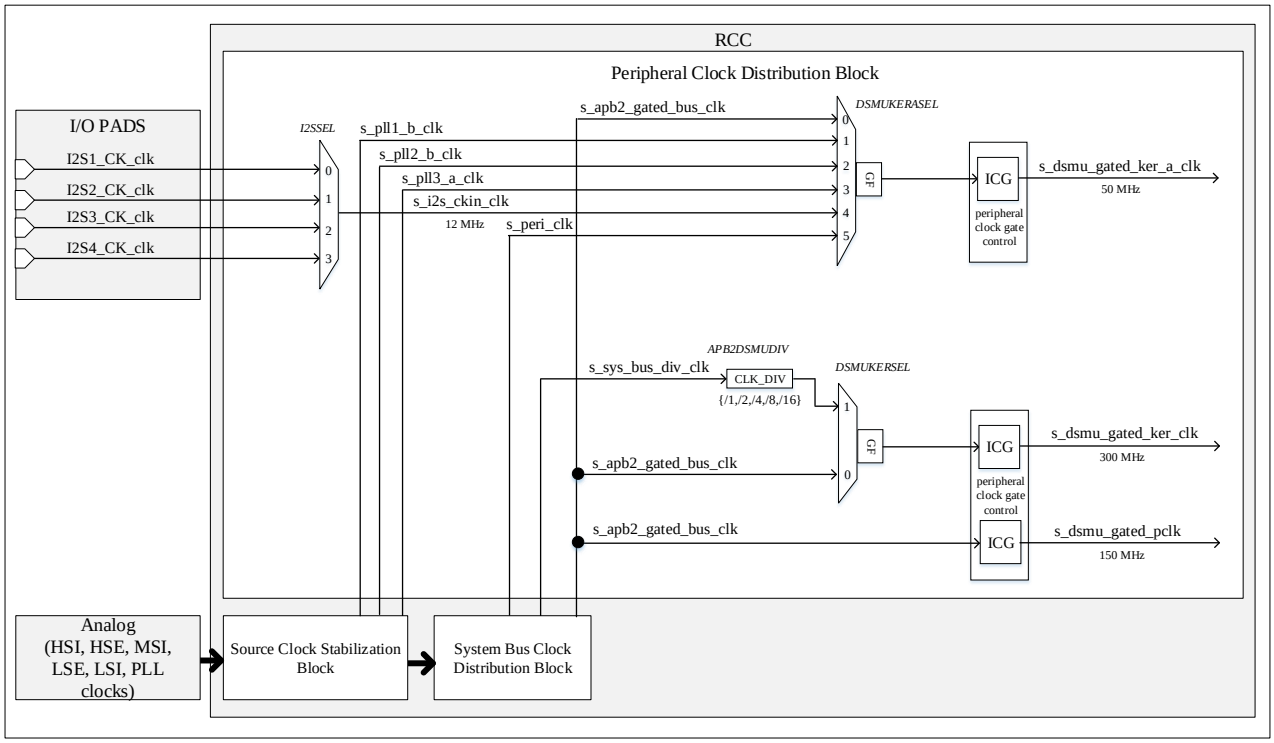
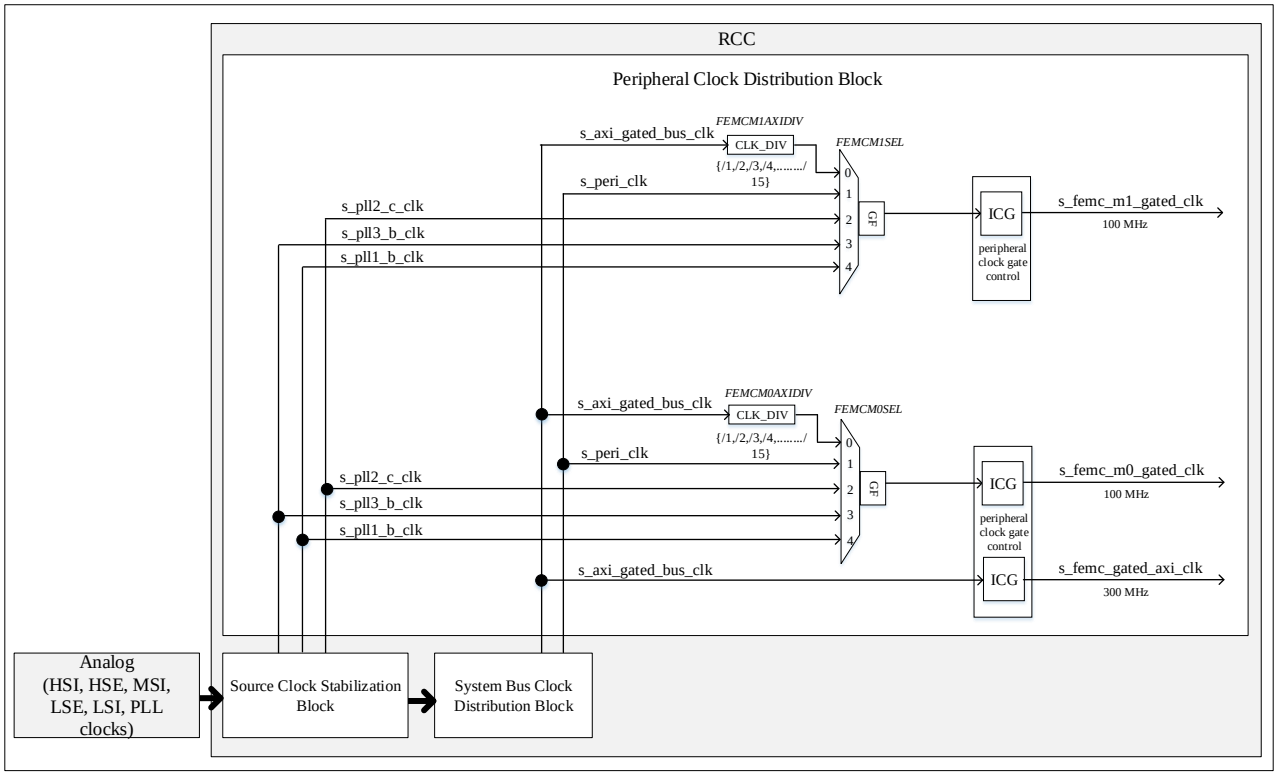
Figure 4-21 DSMU



4.4.4.9 FEMC

Figure 4-22 FEMC



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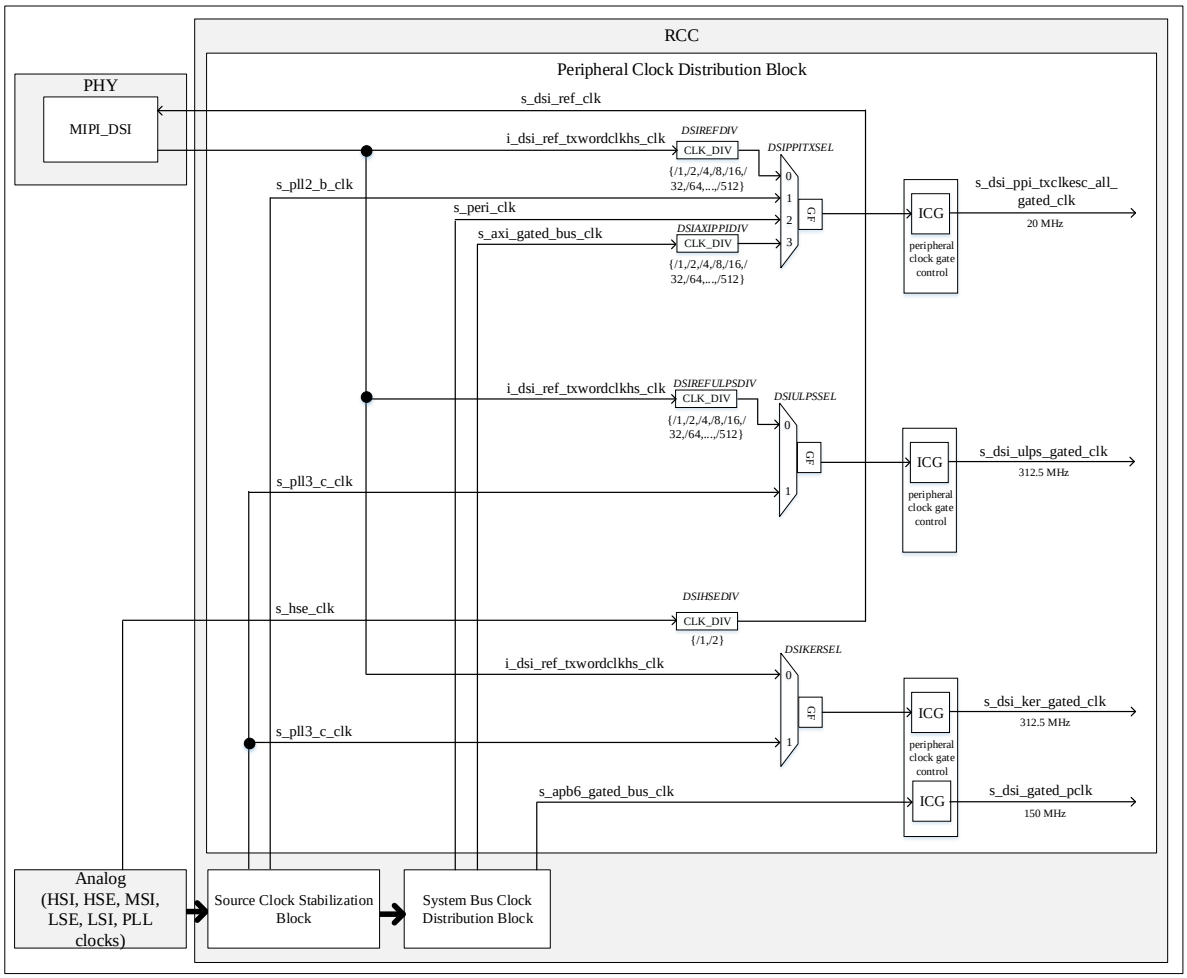
4.4.4.10 DSI

Note: ref_clk output to MIPI_DSI PHY

Figure 4-23 DSI



Note: Enable module clock by configuring M7DSIEN, M4DSIEN, M7DSILPEN, M4DSILPEN, M7DSIULPSEN, M4DSIULPSEN, M7DSIULPSLPEN, M4DSIULPSLPEN.

4.4.4.11 LCDC

Note: pclk for LCDC register configurations, axi_clk for LCDC memory accesses

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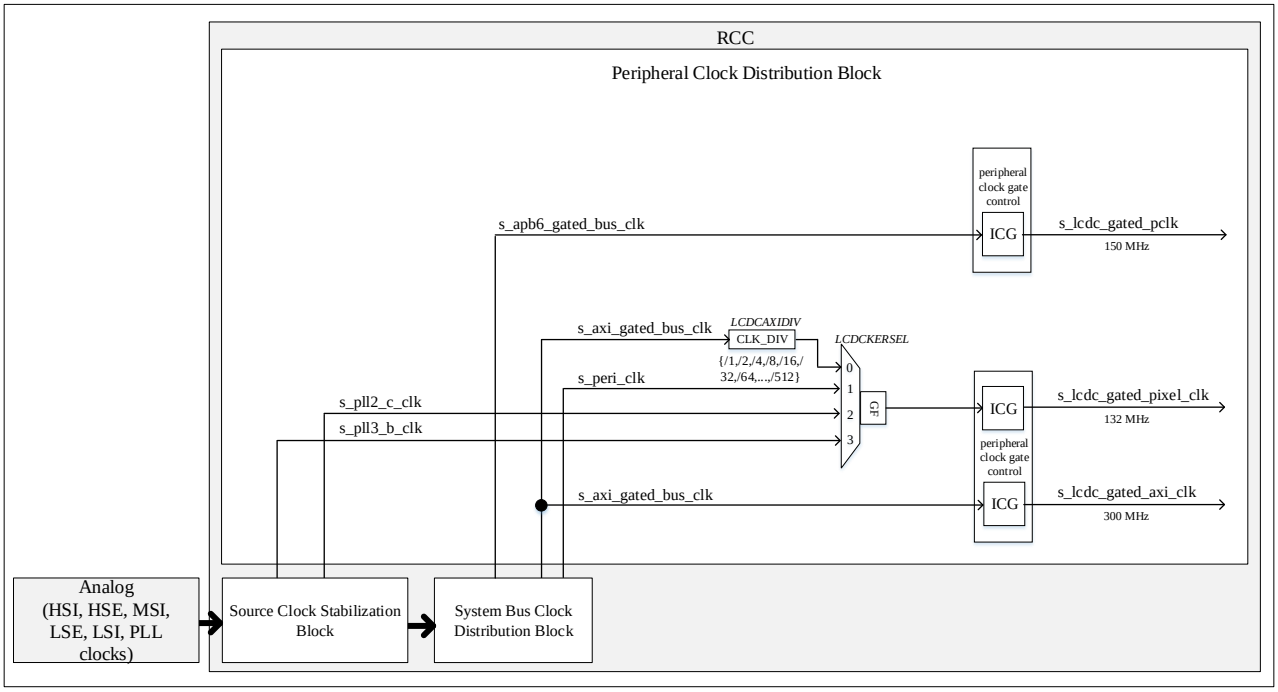
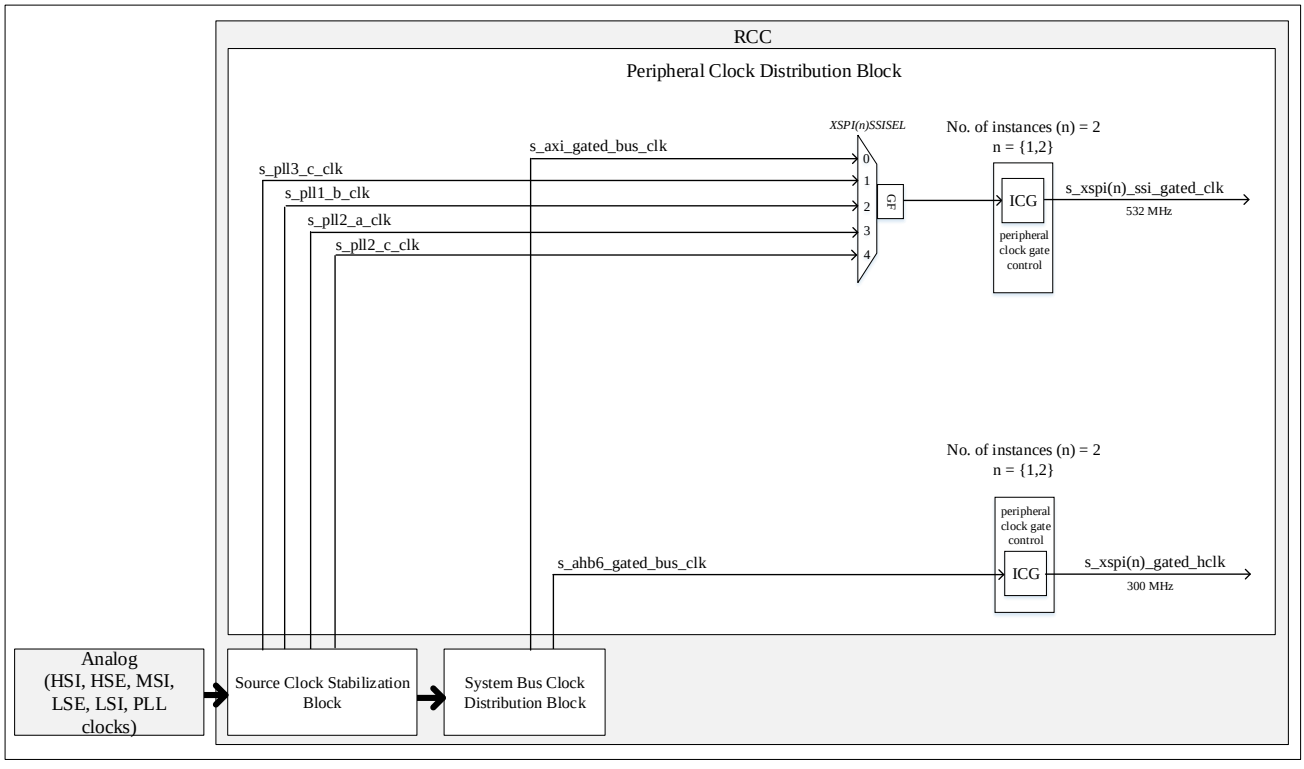
Figure 4-24 LCDC



Note: Enable module clock by configuring M7LCDCEN, M4LCDCEN, M7LCDCLPEN, M4LCDCLPEN, M7LCDCAPBEN, M4LCDCAPBEN, M7LCDCAPBLPEN, M4LCDCAPBLPEN.

4.4.4.12 XSPI

Figure 4-25 XSPI(n) {n=1,2}



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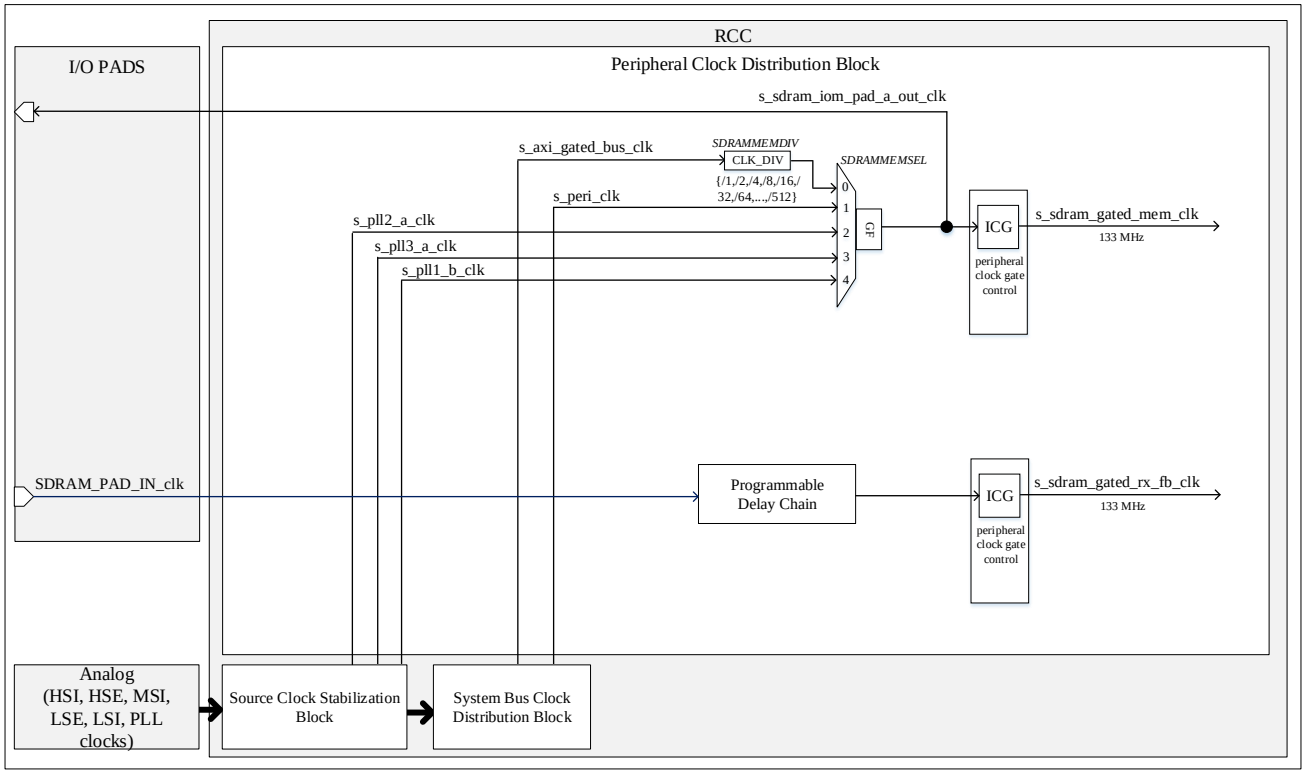
4.4.4.13 SDRAM

Figure 4-26 SDRAM



4.4.4.14 USART

Figure 4-27 USART(n) {n=1,2}

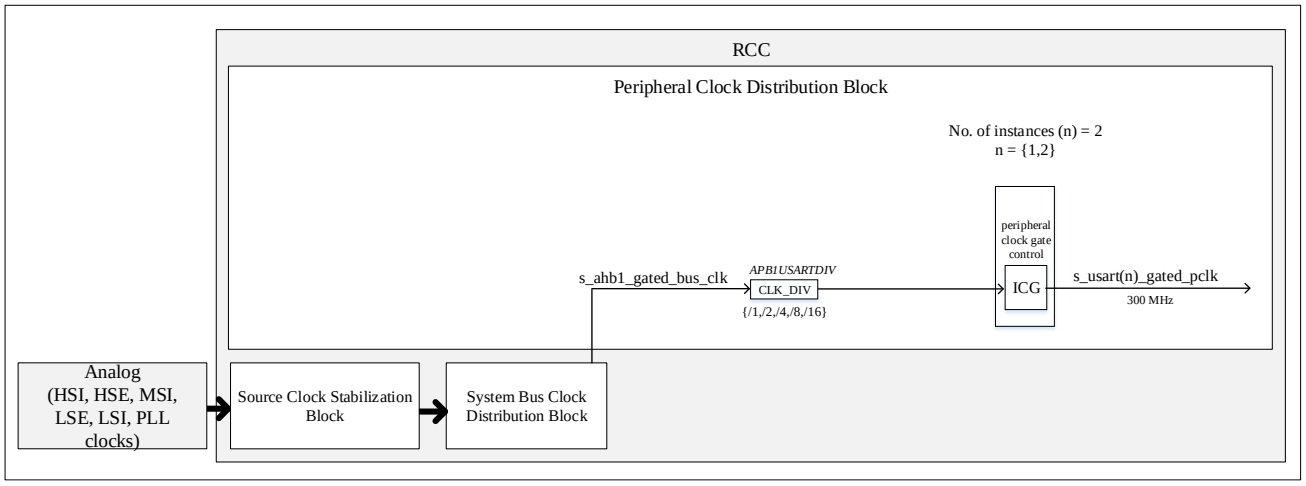


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Figure 4-28 USART(n) {n=3,4}

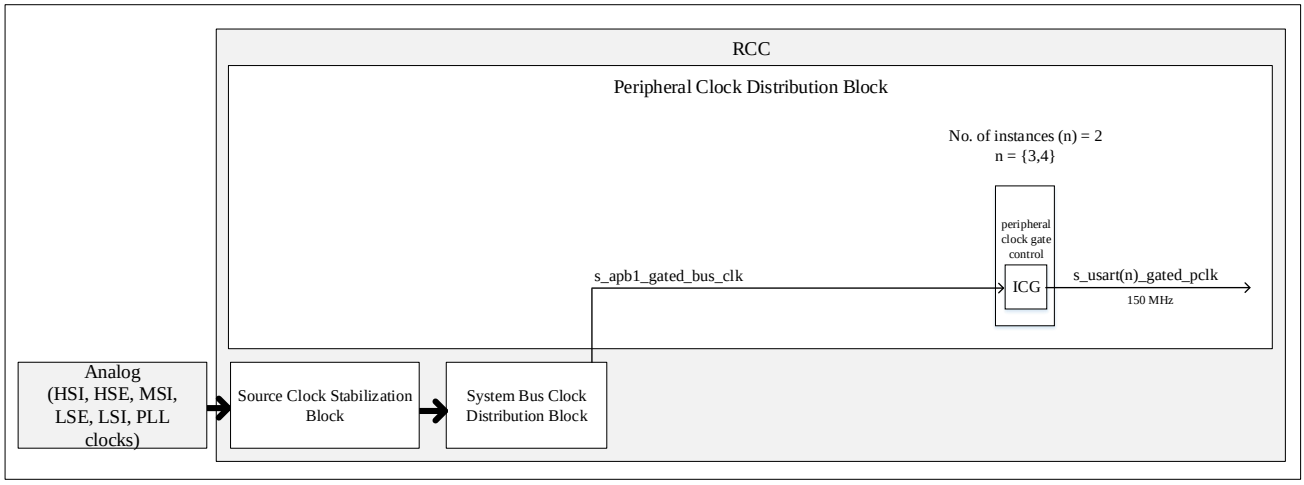
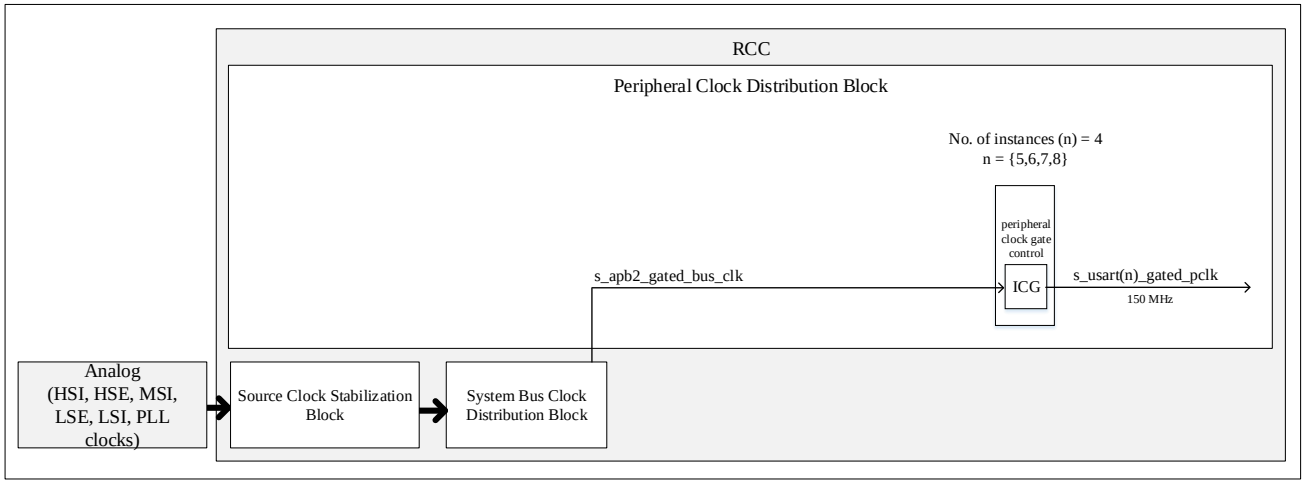


Figure 4-29 USART(n) {n=5,6,7,8}



4.4.4.15 UART

Figure 4-30 UART(n) {n=9,10,11,12}

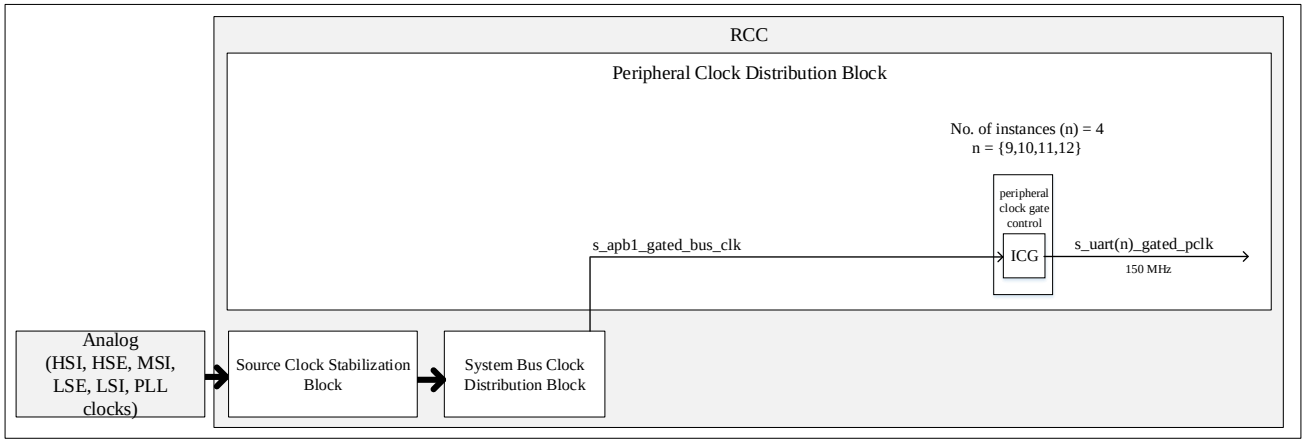


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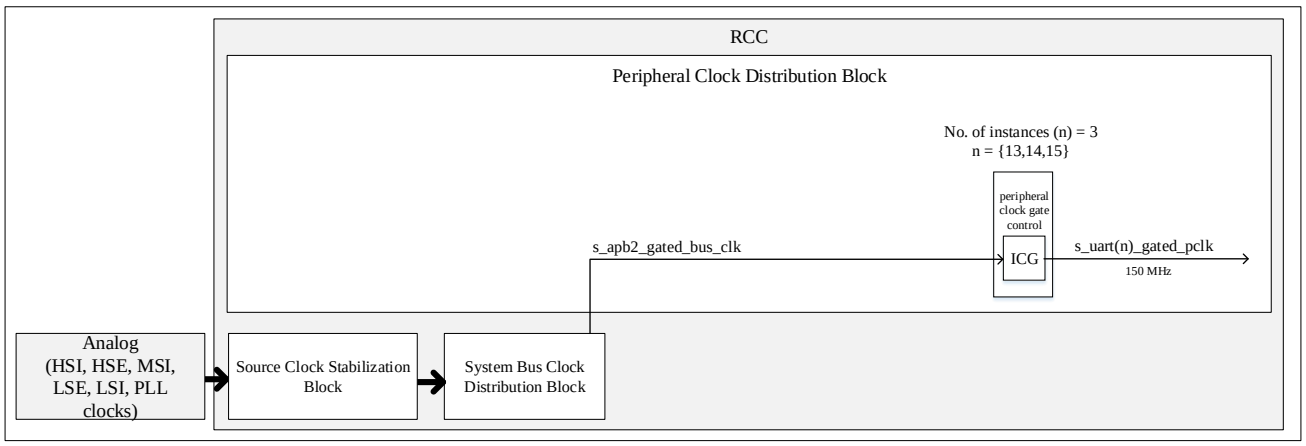
Figure 4-31 UART(n) {n=13,14,15}



4.4.4.16 SPI

Figure 4-32 SPI(n) {n=1,2}

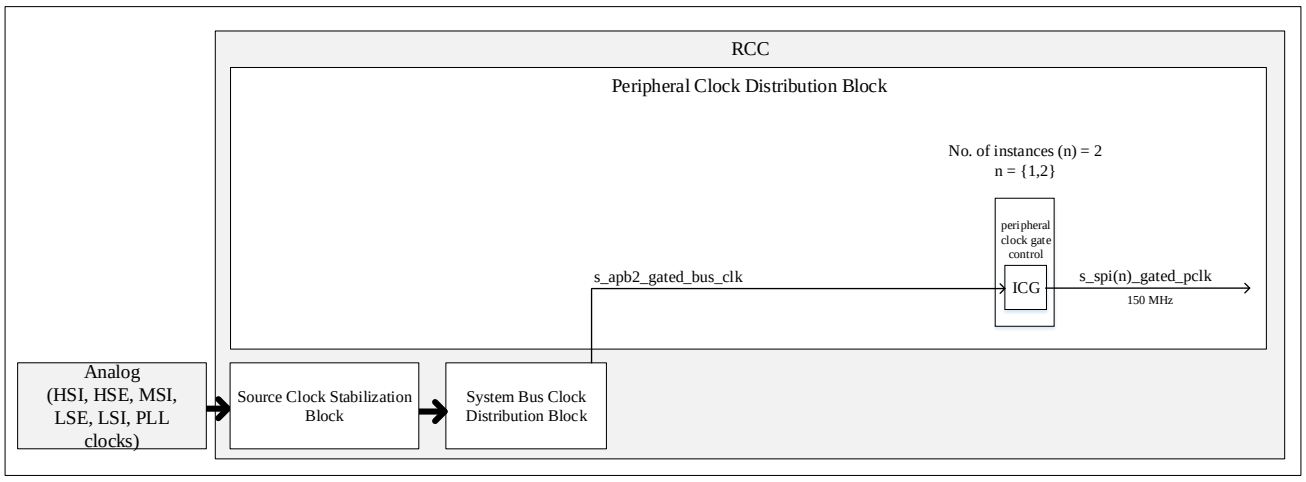


Figure 4-33 SPI(n) {n=3}

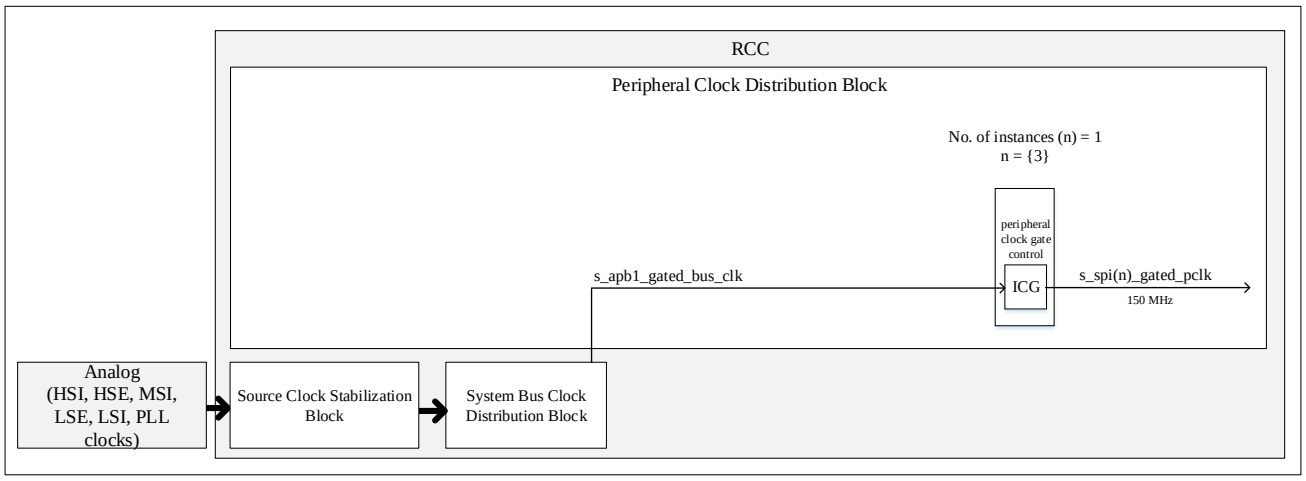


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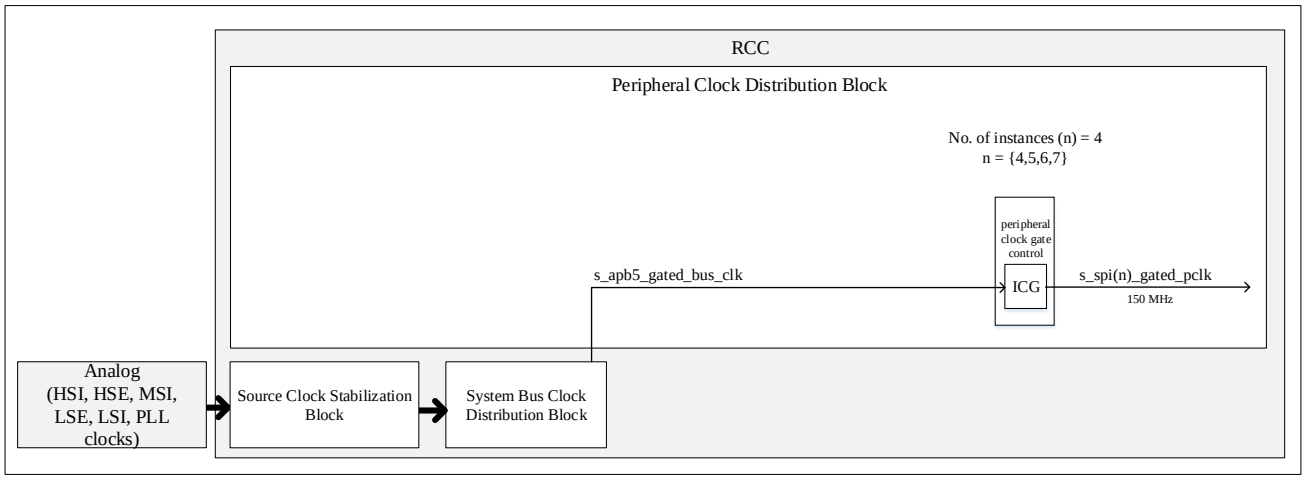
Figure 4-34 SPI(n) {n=4,5,6,7}



4.4.4.17 I2S

Figure 4-35 I2S(n) {n=1,2}

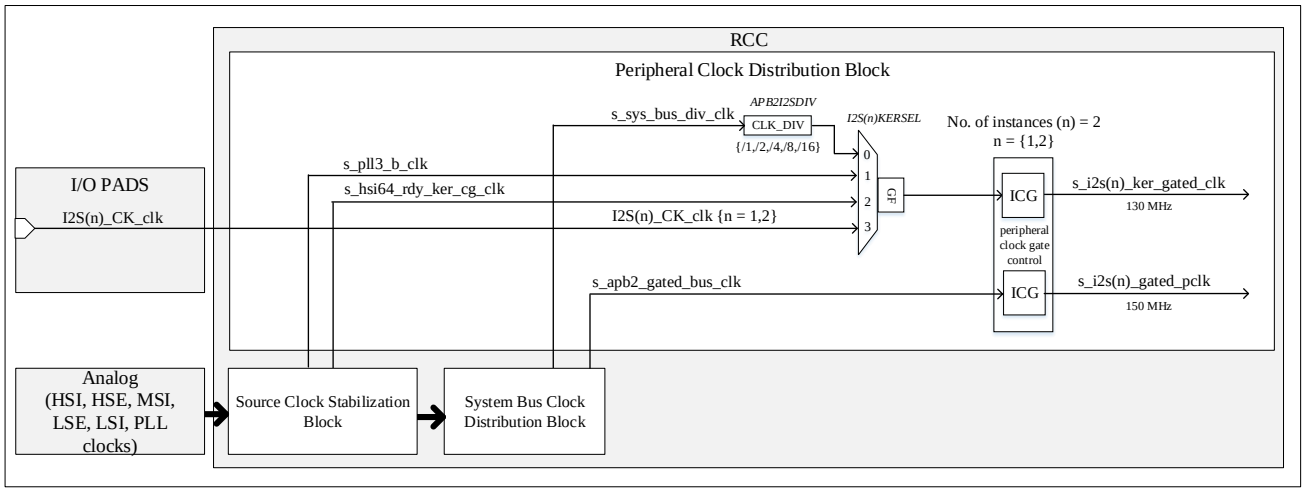
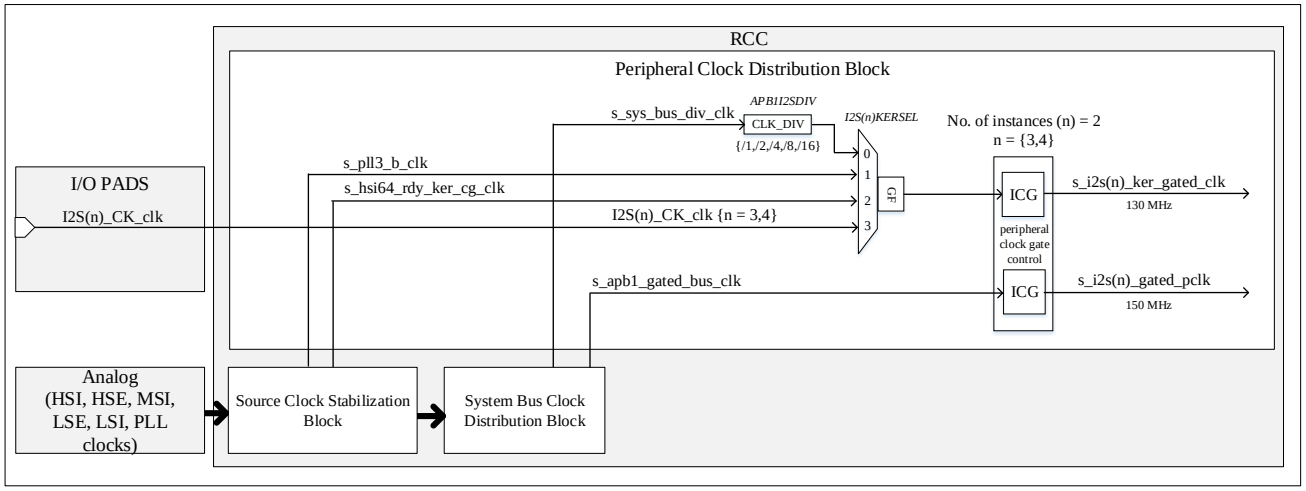


Figure 4-36 I2S(n) {n=3,4}



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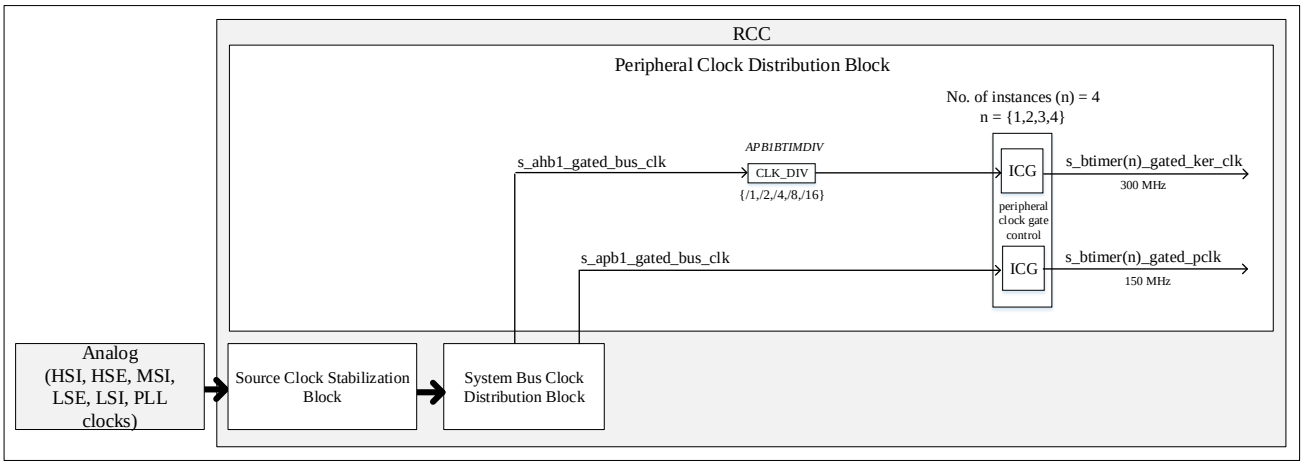
4.4.4.18 BTIM

Note: you need to make sure that gated_ker_clk is equal to gated_pclk or that gated_ker_clk is twice gated_pclk

Figure 4-37 BTIM(n) {n=1,2,3,4}



4.4.4.19 ATIM

Note: you need to make sure that gated_ker_clk is equal to gated_pclk or that gated_ker_clk is twice gated_pclk

Figure 4-38 ATIM(n) {n=1,2}

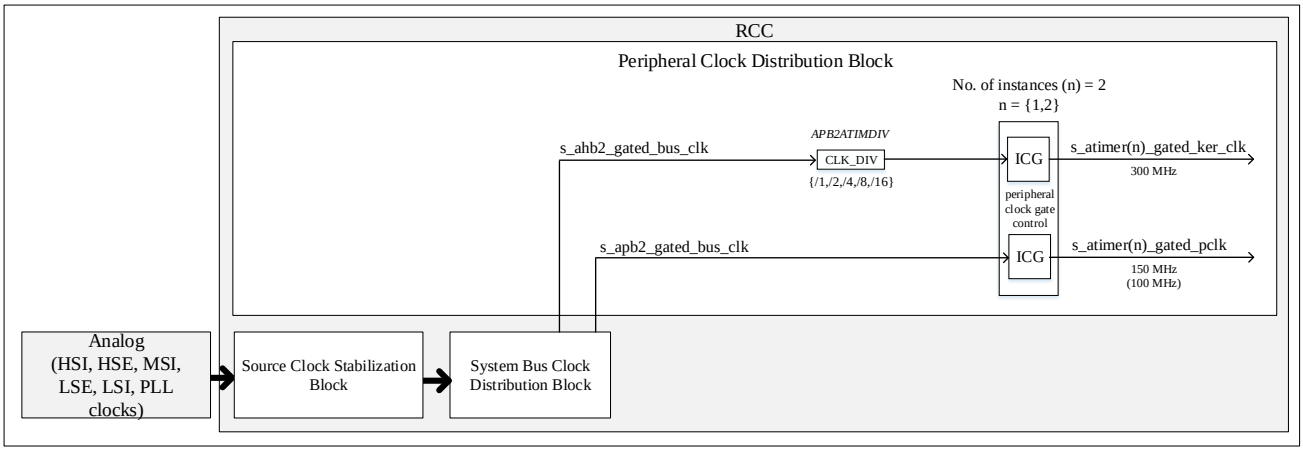


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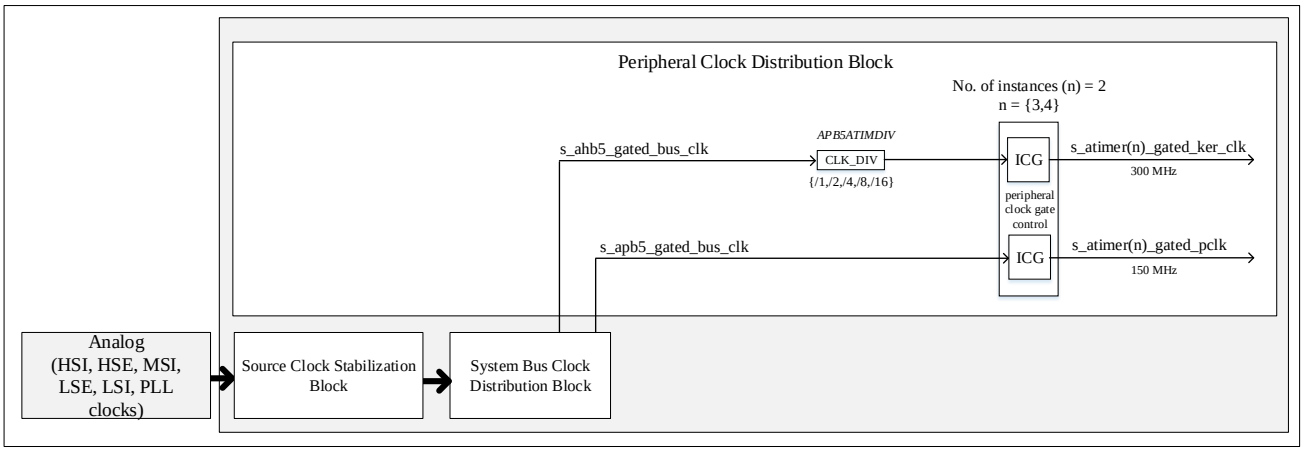
Figure 4-39 ATIM(n) {n=3,4}



4.4.4.20 GTIM

Note: you need to make sure that gated_ker_clk is equal to gated_pclk or that gated_ker_clk is twice gated_pclk

Figure 4-40 GTIMA(n) {n=1,2,3}

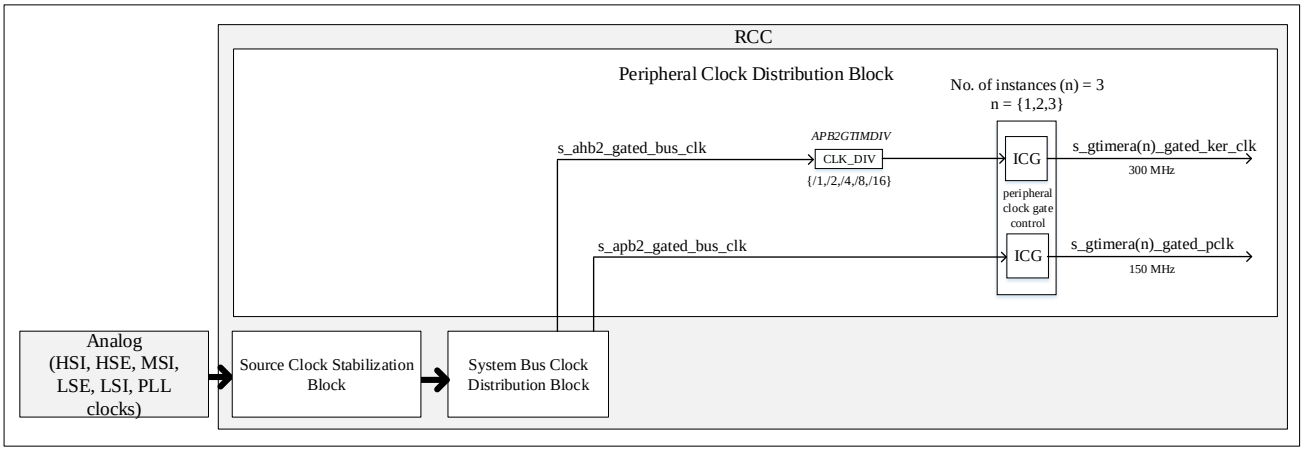


Figure 4-41 GTIMA(n) {n=4,5,6,7}

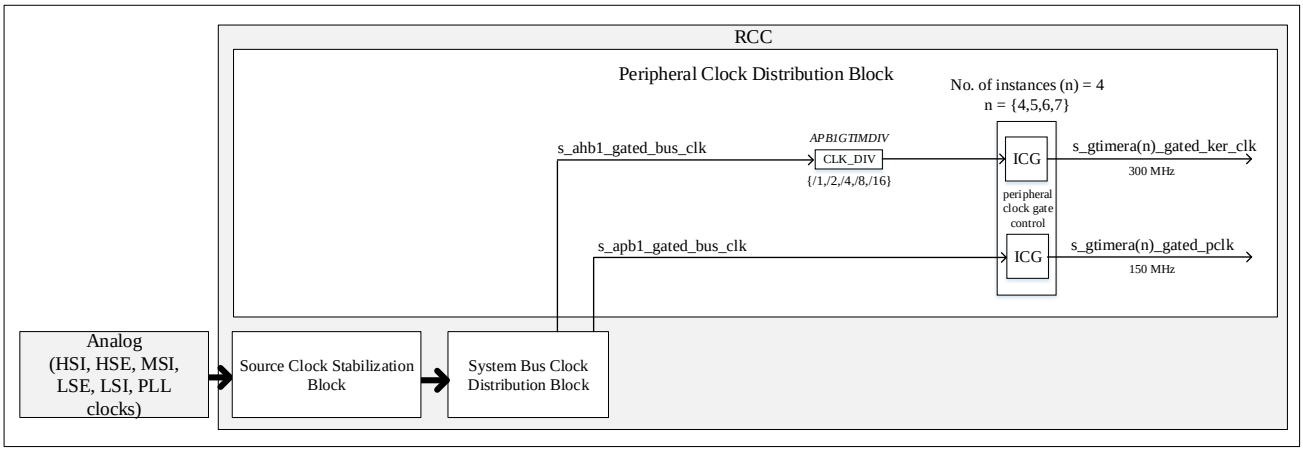


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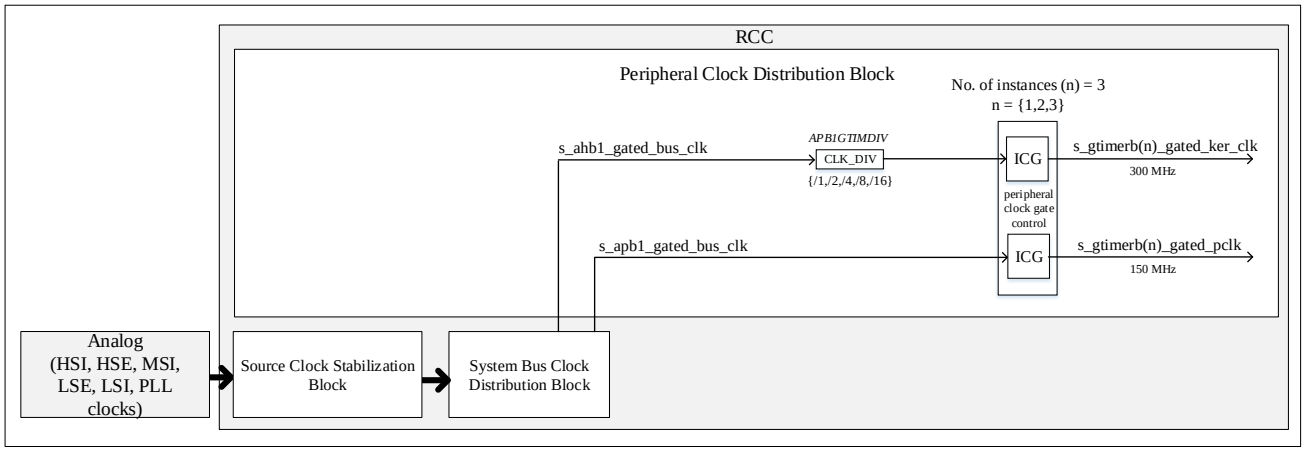
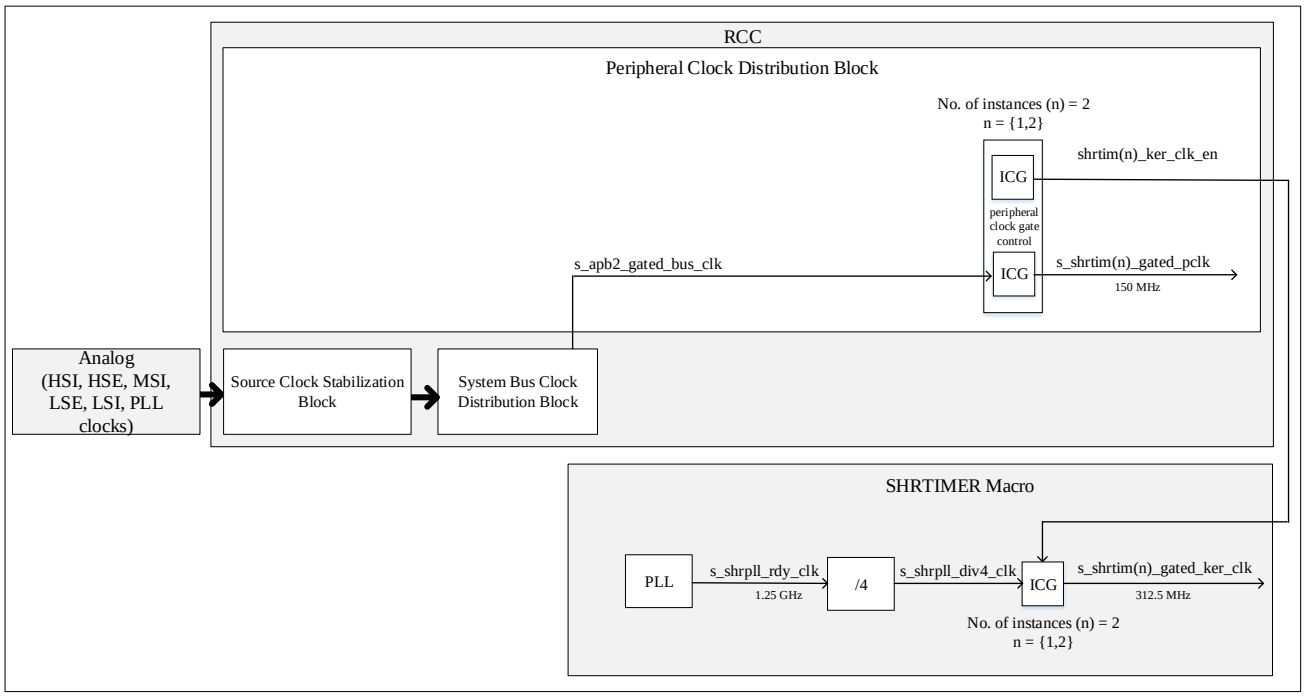
Figure 4-42 GTIMB(n) {n=1,2,3}



4.4.4.21 SHRTIM

Figure 4-43 SHRTIM(n) {n=1,2}



Note: The procedure for enabling the module clock is as follows(n=1,2):

1. *Assert SHRTIMER(n) soft reset by programming the bit "RCC_APB2RST1.SHRTIM(n)RST" to 1'b1.*
2. *Assert AFE reset by programming the bit "RCC_PLLSFTLK.SHRTIMAFERST" to 1'b0.*
3. *Program and enable the SHRPLL to the required frequency settings. (If the SHRPLL is enabled with default settings then its output clock frequency will be 312.5 MHz).*
4. *Wait for 1us.*
5. *De-assert SHRTIMER(n) soft reset by programming the bit "RCC_APB2RST1.SHRTIM(n)RST" to 1'b0.*
6. *De-assert AFE reset by programming the bit "RCC_PLLSFTLK.SHRTIMAFERST" to 1'b1.*

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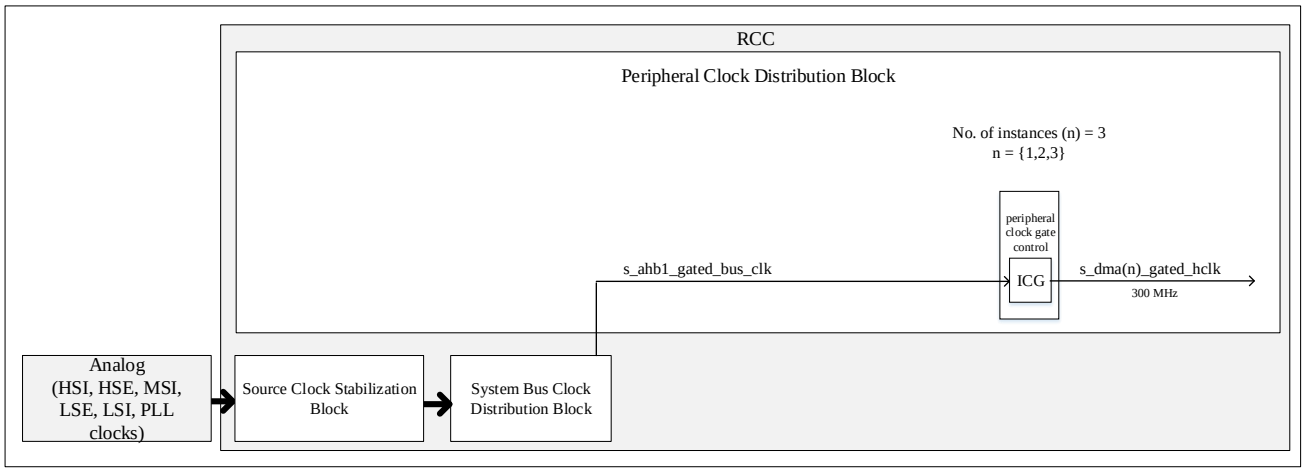
7. *Enable SHRTIMER(n) clocks by programming the bits "M7SHRTIM(n)EN", M4SHRTIM(n)EN", "M7SHRTIM(n)LPEN" and "M4SHRTIM(n)LPEN" to 1'b0 in "RCC_APB2EN1" register.*

4.4.4.22 DMA

Figure 4-44 DMA(n) {n=1,2,3}



4.4.4.23 DMAMUX

Figure 4-45 DMAMUX1

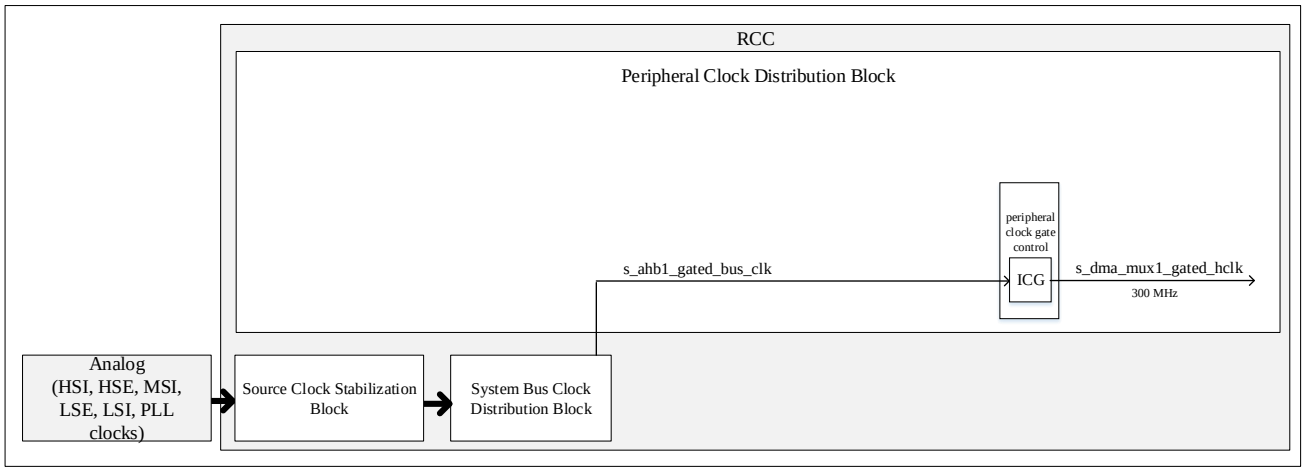


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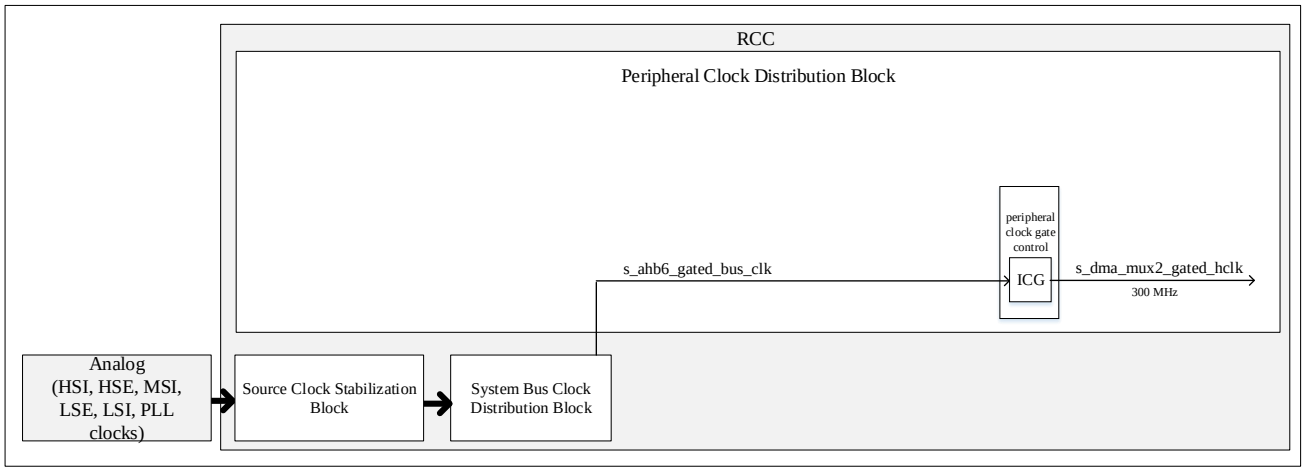
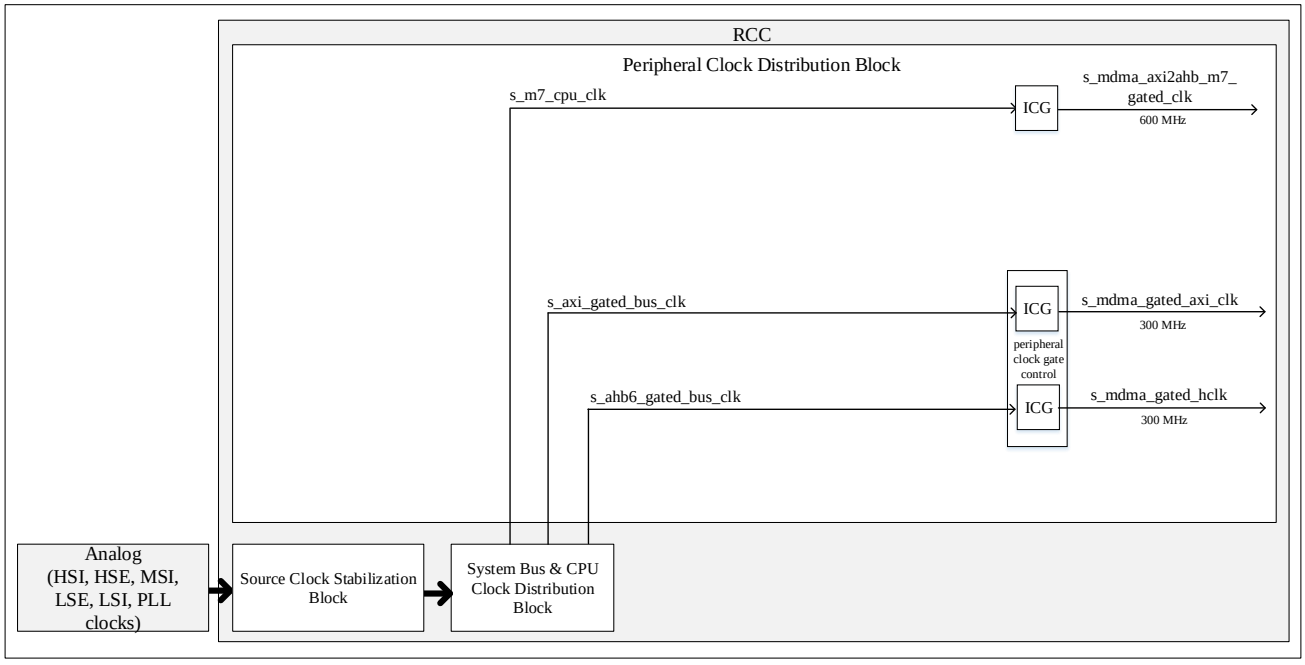
Figure 4-46 DMAMUX2



4.4.4.24 MDMA

Figure 4-47 MDMA



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4.4.4.25 ECCMON

Figure 4-48 ECCMON1

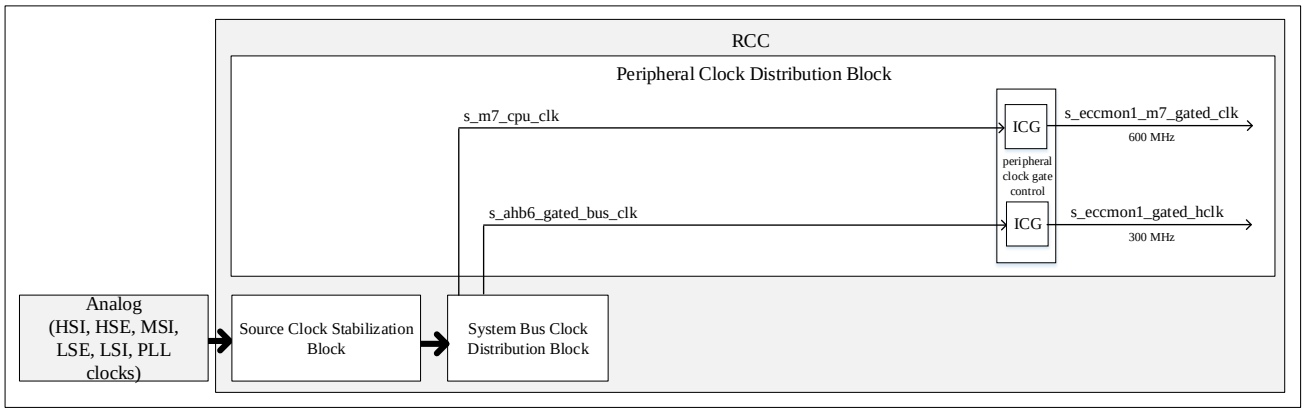

Figure 4-49 ECCMON2

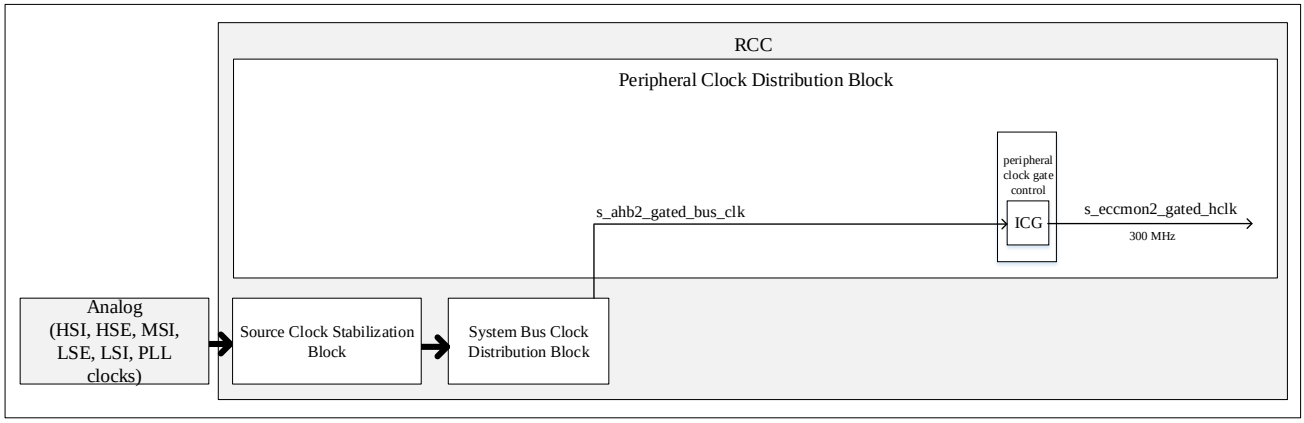

Figure 4-50 ECCMON3

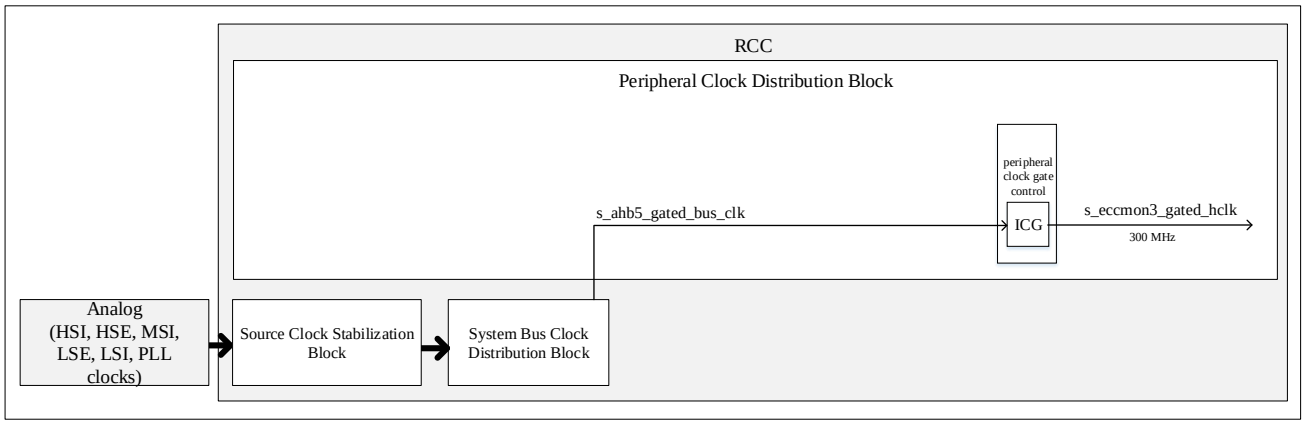

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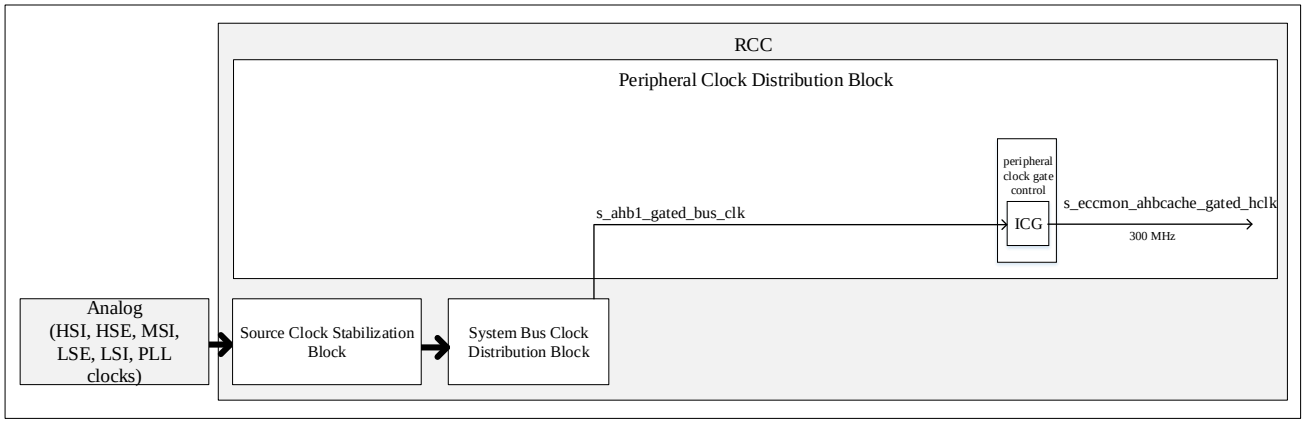
Figure 4-51 ECCMON_AHBCACHE



4.4.4.26 DAC

Figure 4-52 DAC(n) {n=12}

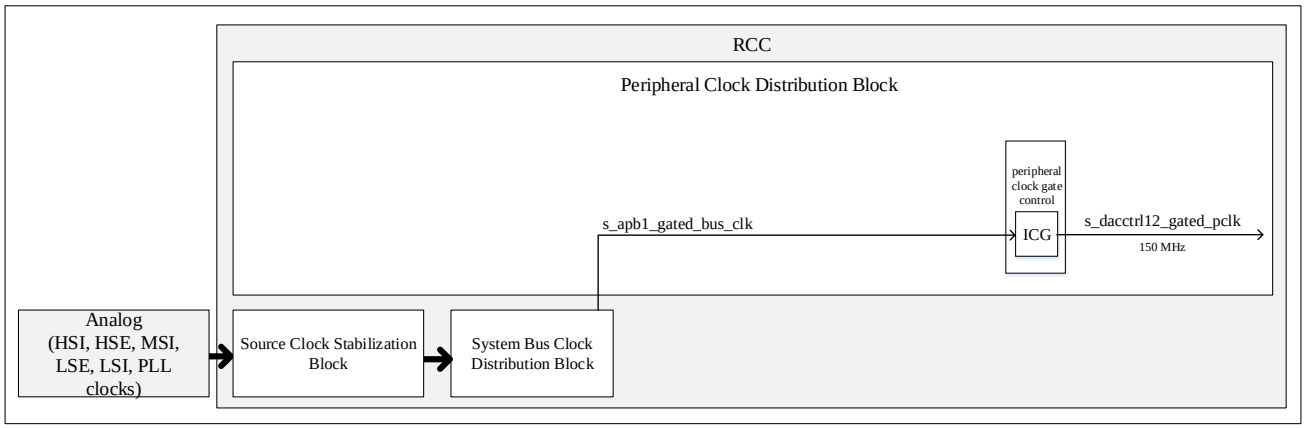
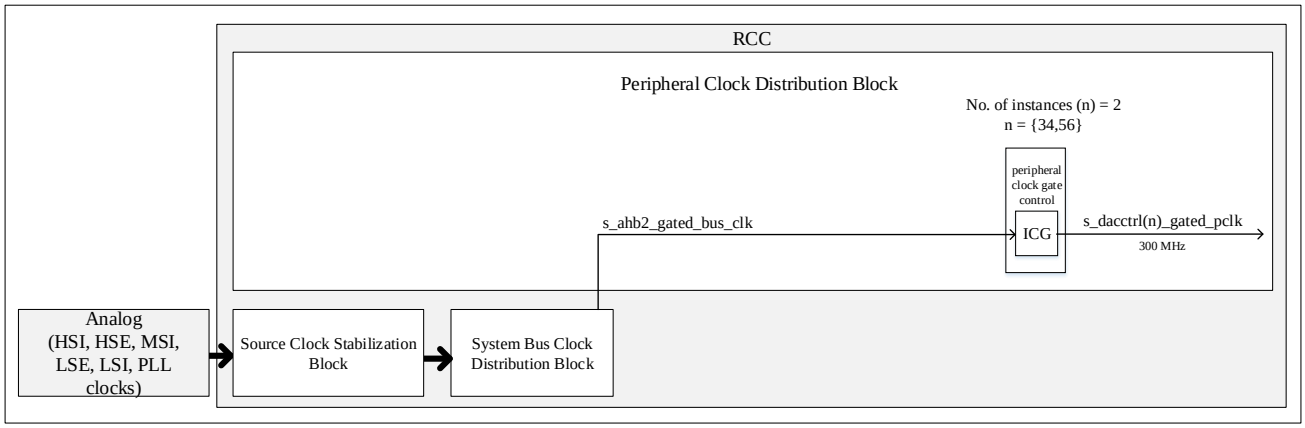


Figure 4-53 DAC(n) {n=34, 56}



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4.4.4.27 WWDG

Figure 4-54 WWDG1

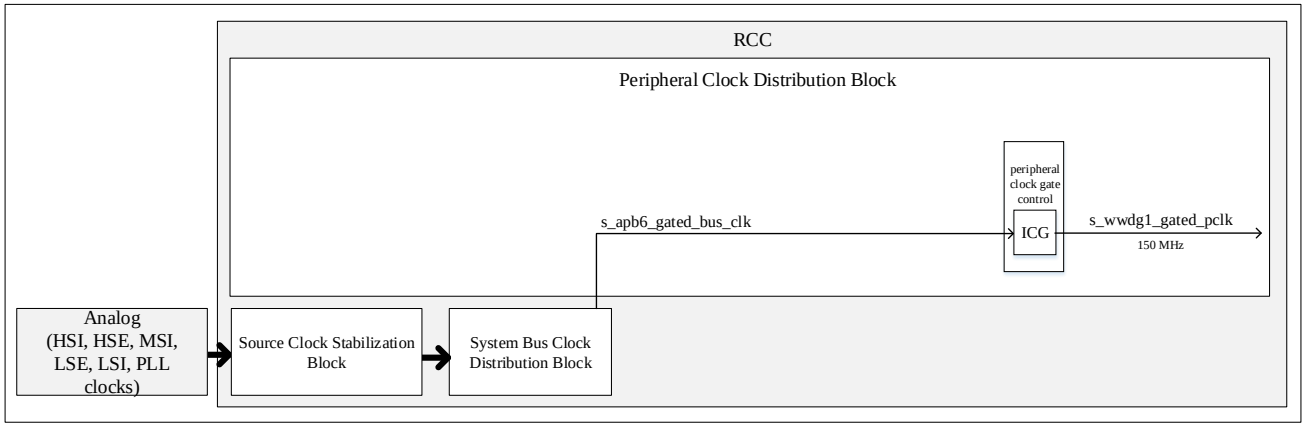
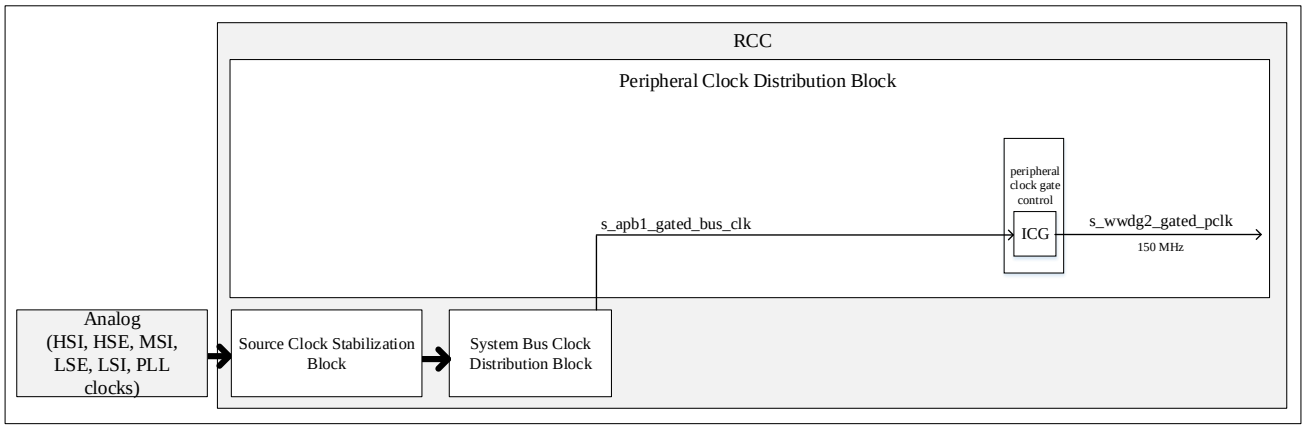
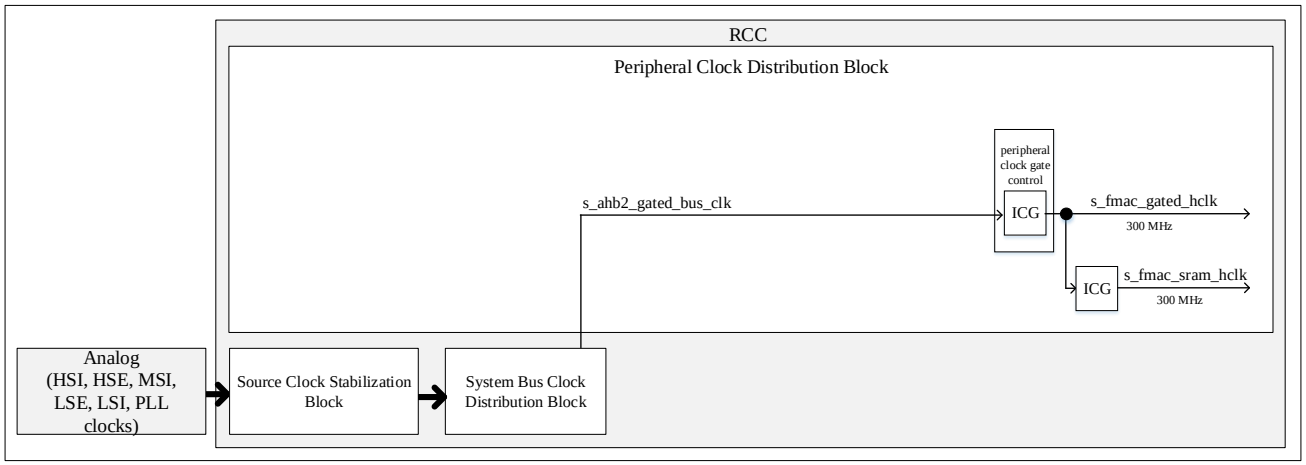


Figure 4-55 WWDG2



4.4.4.28 FMAC

Figure 4-56 FMAC



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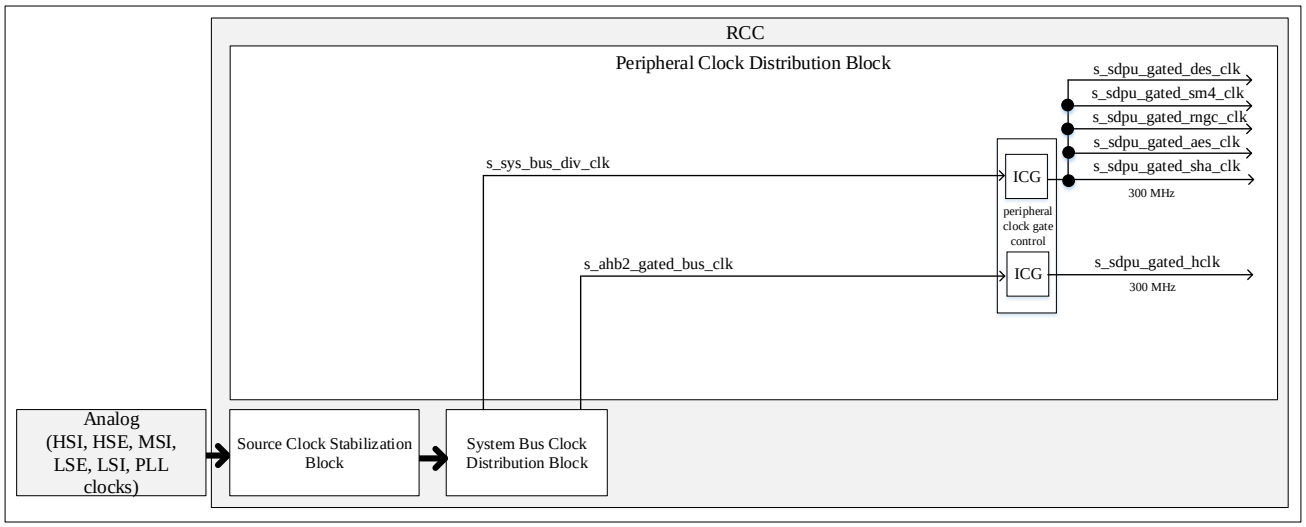
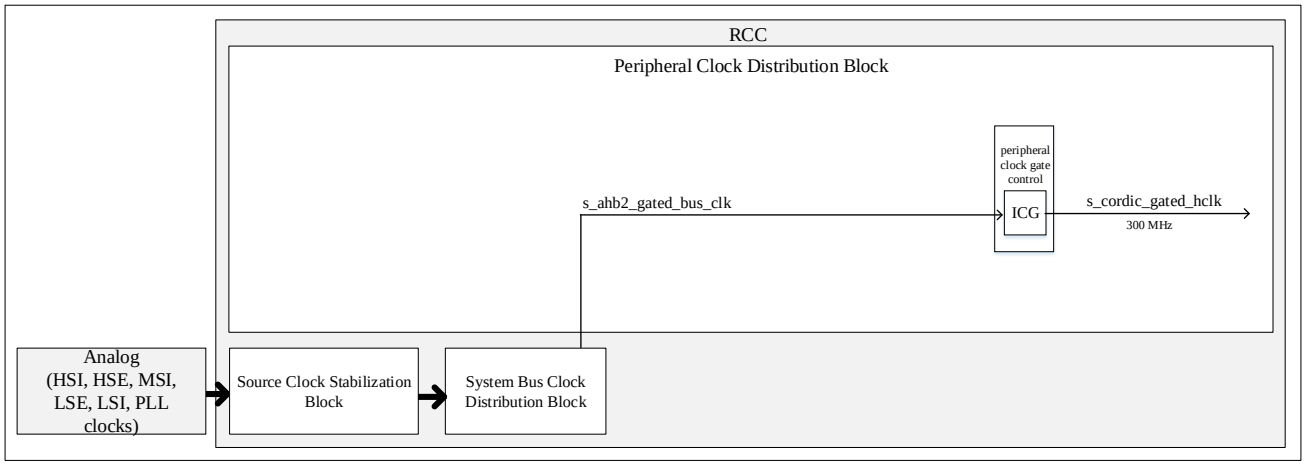
4.4.4.29 SDPU

Figure 4-57 SDPU



4.4.4.30 CORDIC

Figure 4-58 CORDIC



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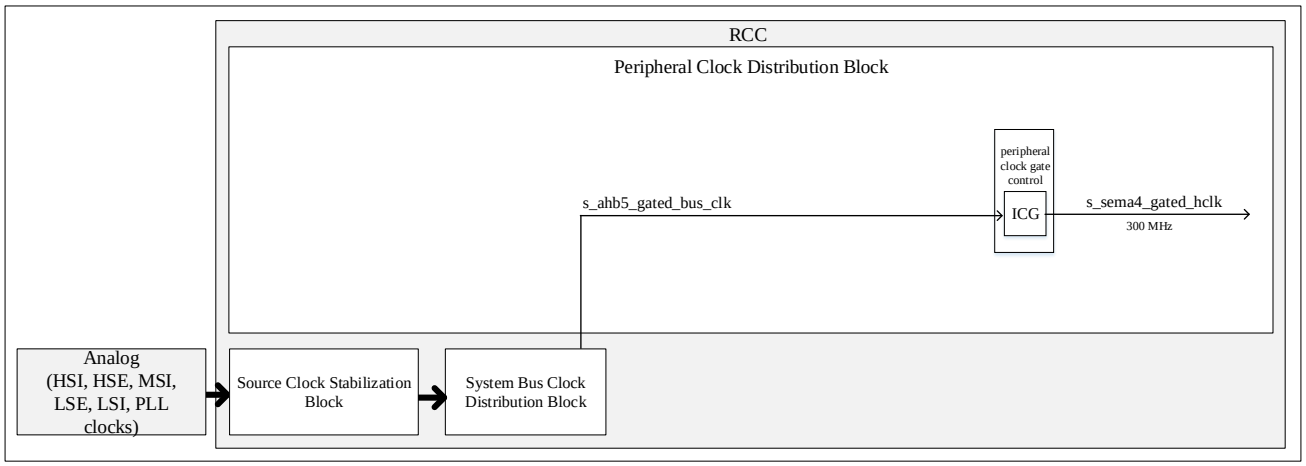
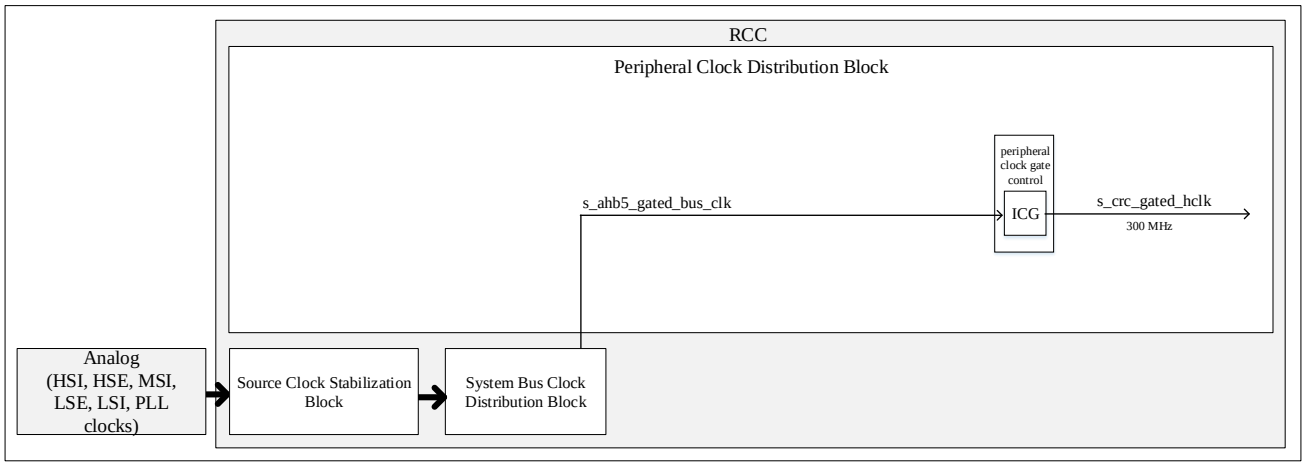
4.4.4.31 SEMA4

Figure 4-59 SEMA4



4.4.4.32 CRC

Figure 4-60 CRC



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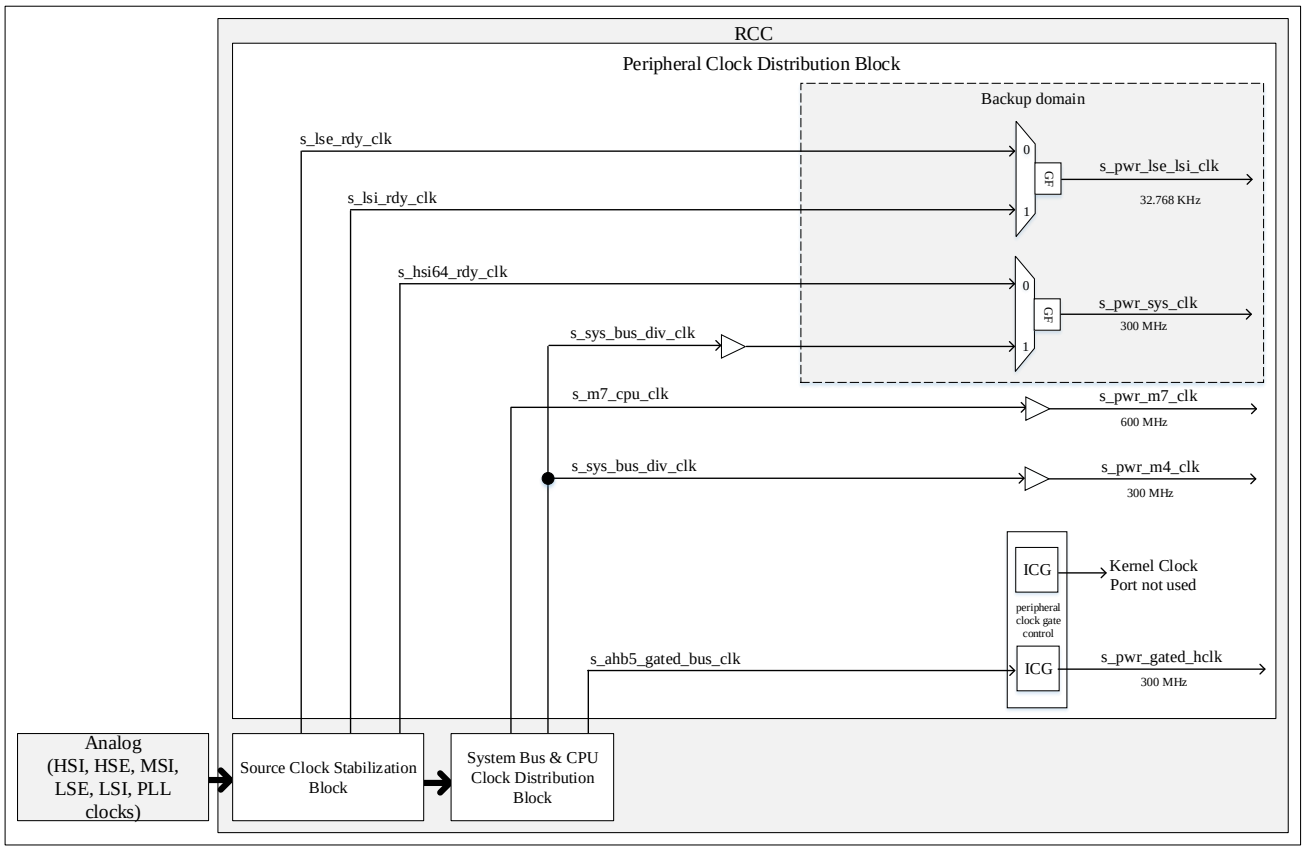
4.4.4.33 PWR

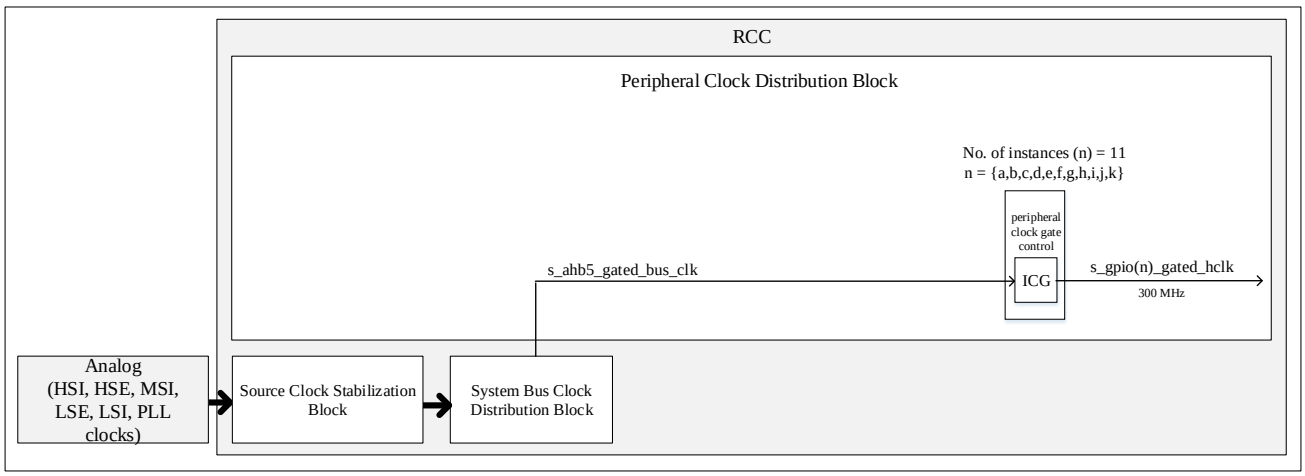
Figure 4-61 PWR



Note: Backup domain will automatically control LSE and LSI clock selection.

4.4.4.34 GPIO

Figure 4-62 GPIO



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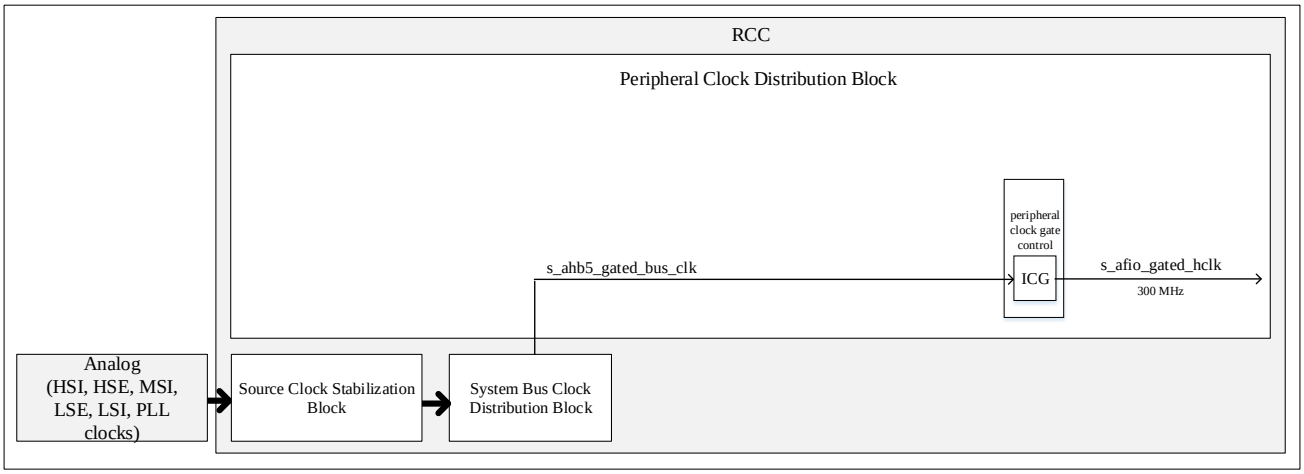
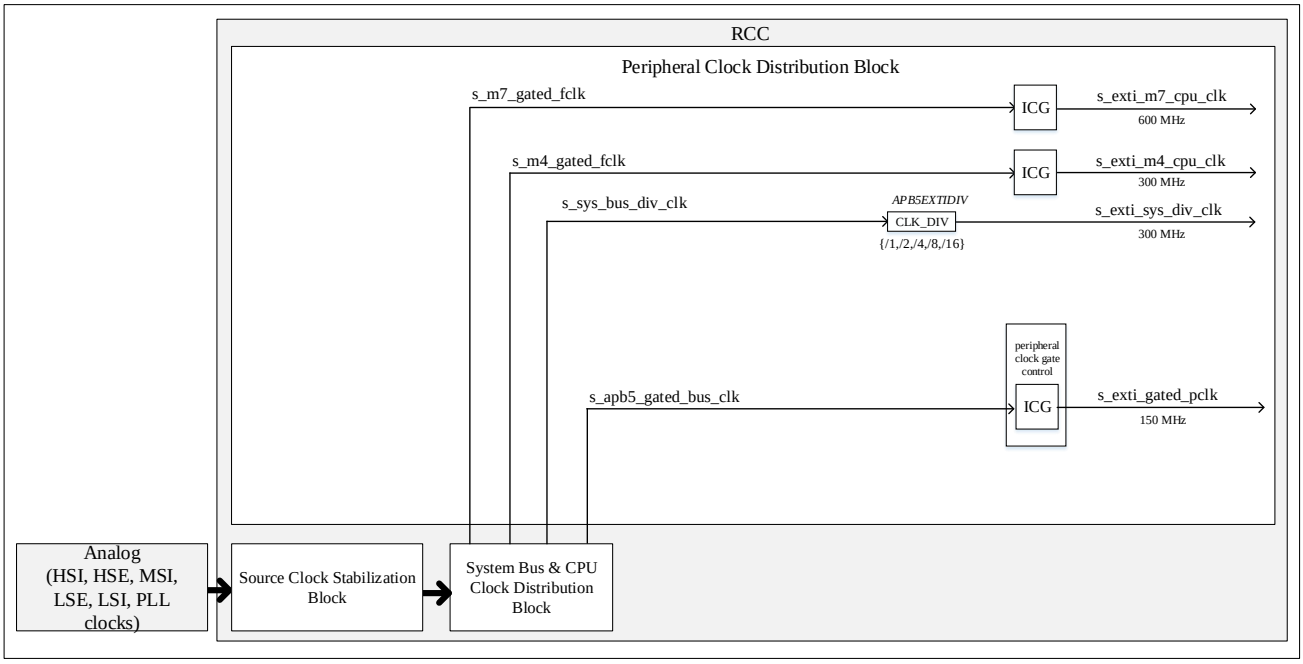
4.4.4.35 AFIO

Figure 4-63 AFIO



4.4.4.36 EXTI

Figure 4-64 EXTI



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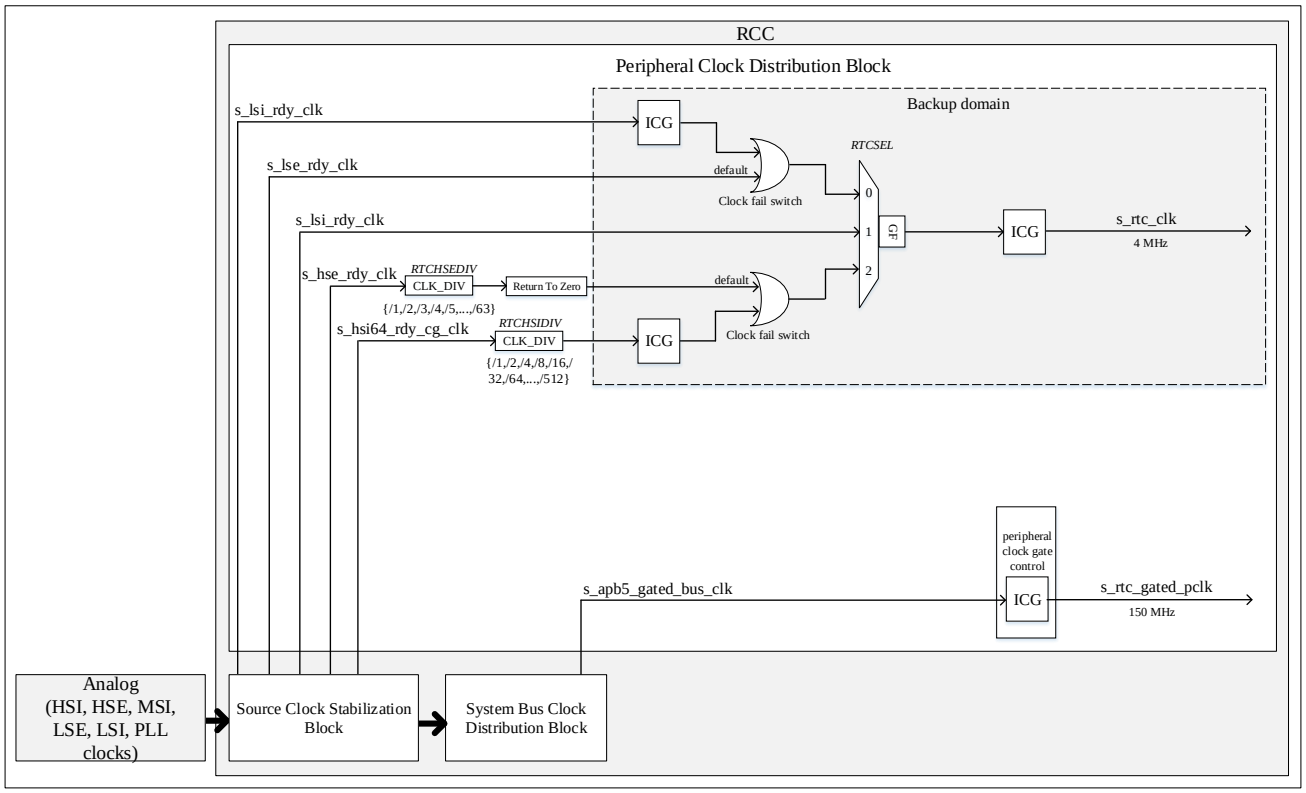
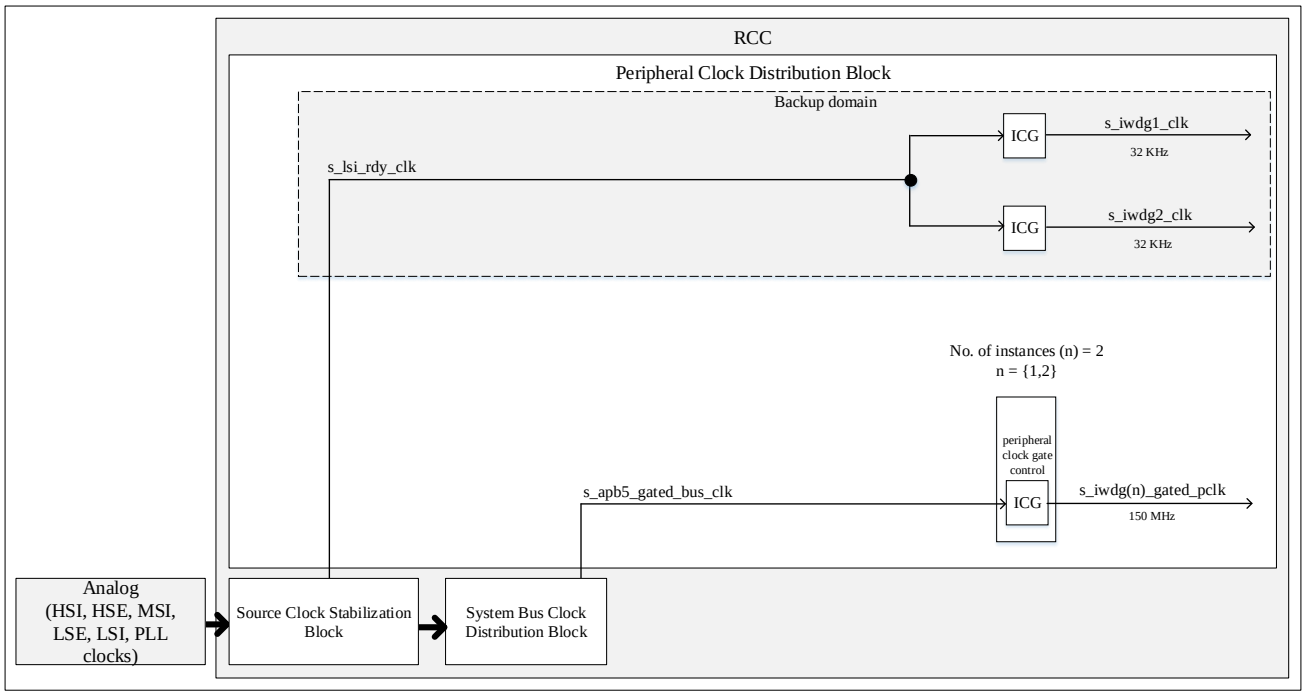
4.4.4.37 RTC

Figure 4-65 RTC



4.4.4.38 IWDG

Figure 4-66 IWDG(n) {n=1,2}



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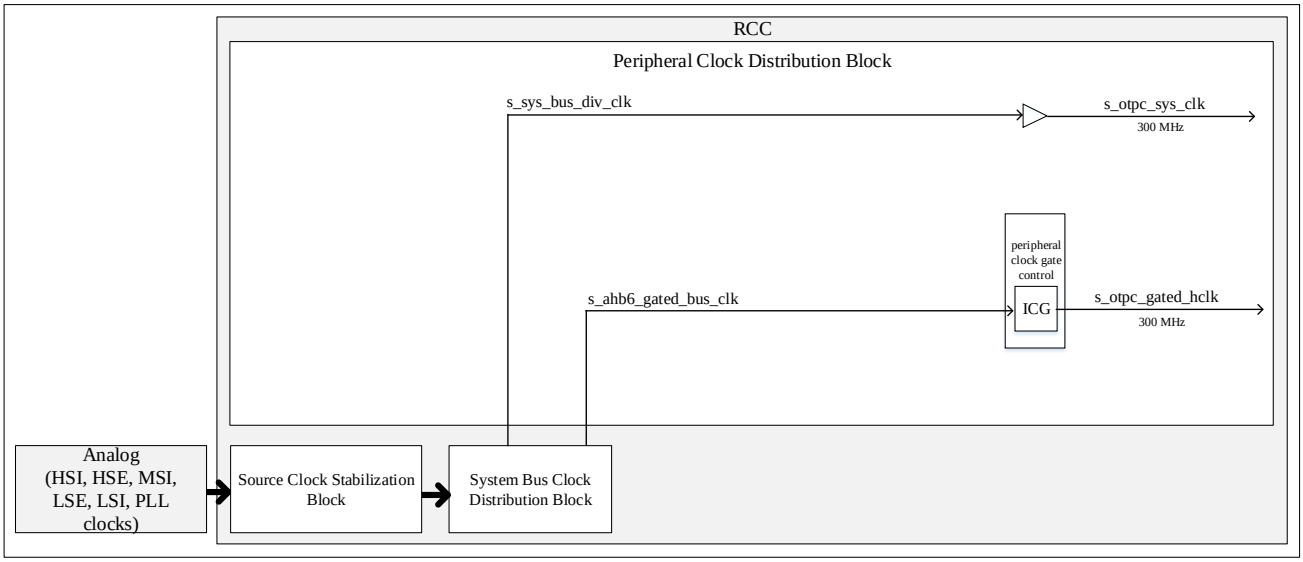
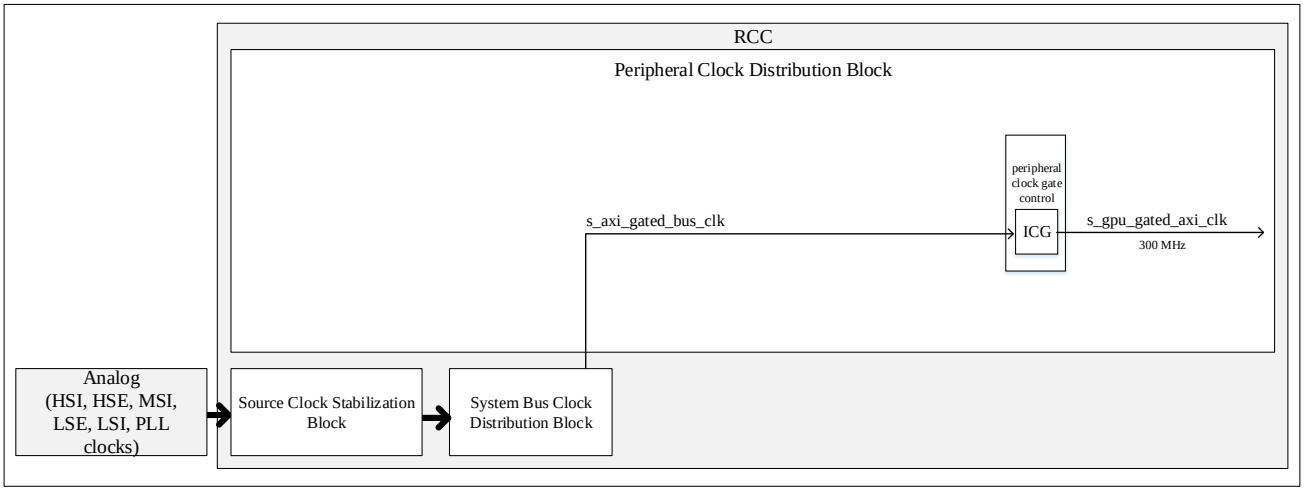
4.4.4.39 OTPC

Figure 4-67 OTPC



4.4.4.40 GPU

Figure 4-68 GPU



4.4.4.41 DVP

Note: pclk for DVP register configurations, hclk for DVP memory accesses

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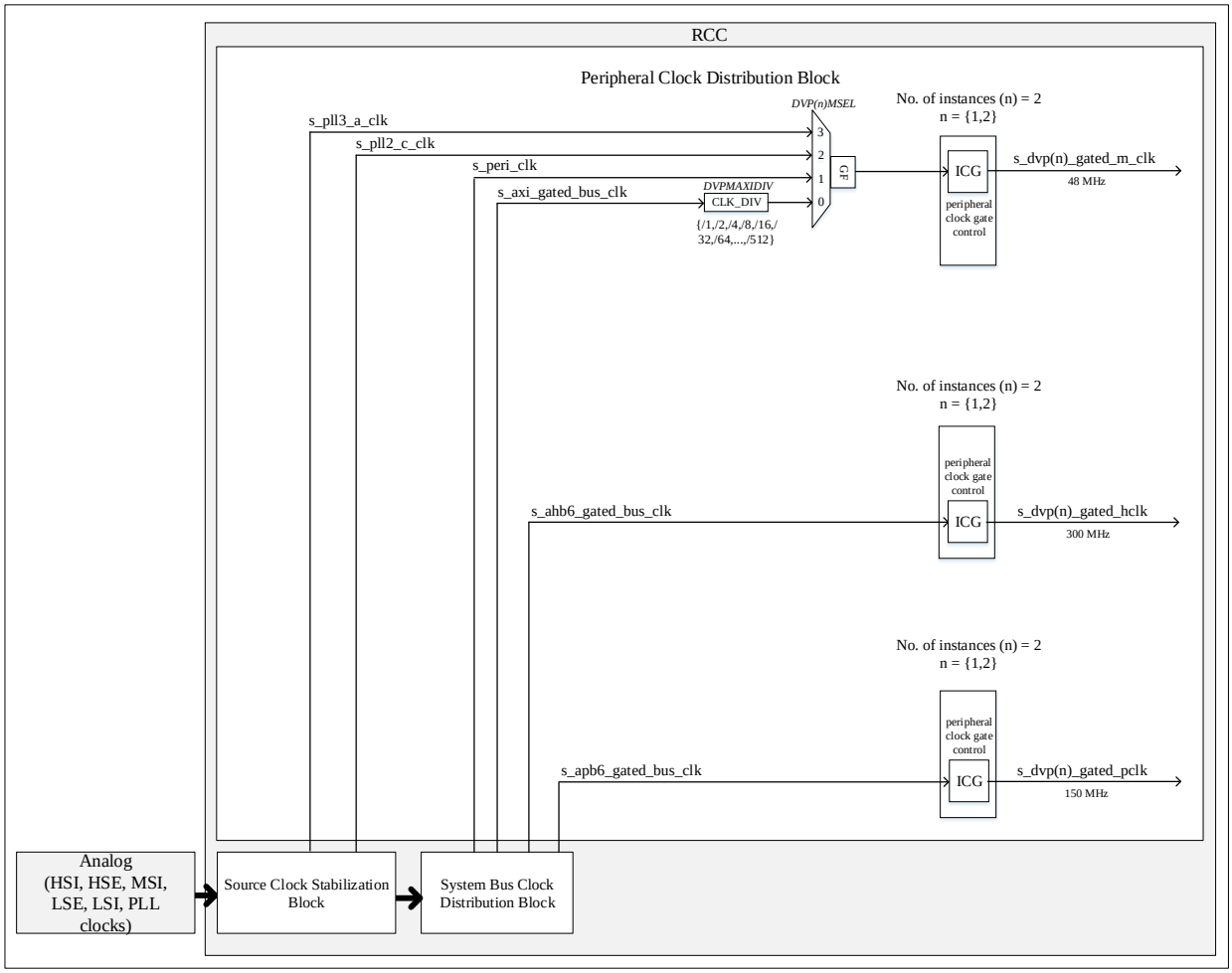
Figure 4-69 DVP(n) {n=1,2}



Note: Enable module clock by configuring M7DVP(n)EN, M4DVP(n)EN, M7DVP(n)LPEN, M4DVP(n)LPEN, M7DVP(n)APBEN, M4DVP(n)APBEN, M7DVP(n)APBLPEN, M4DVP(n)APBLPEN {n=1,2}.

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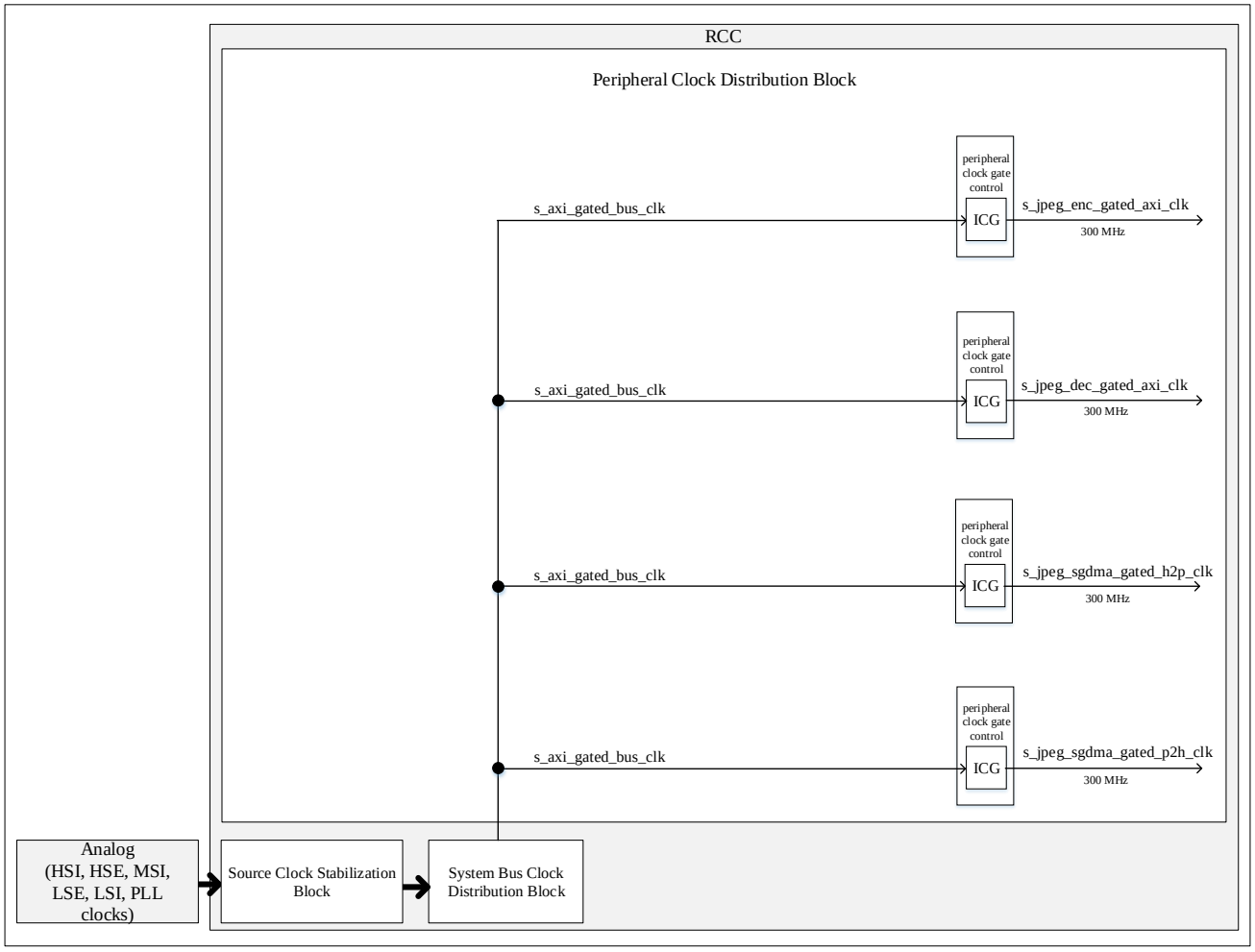
4.4.4.42 JPEG

Figure 4-70 JPEG



Note: Enable JPEG Decoder module clock by configuring M7JPEGDEN, M4JPEGDEN, M7JPEGDLPEN, M4JPEGDLPEN.

Note: Enable JPEG Encoder module clock by configuring M7JPEGEEN, M4JPEGEEN, M7JPEGELPEN, M4JPEGELPEN.

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4.4.4.43 SRAM

Figure 4-71 AHB_SRAM

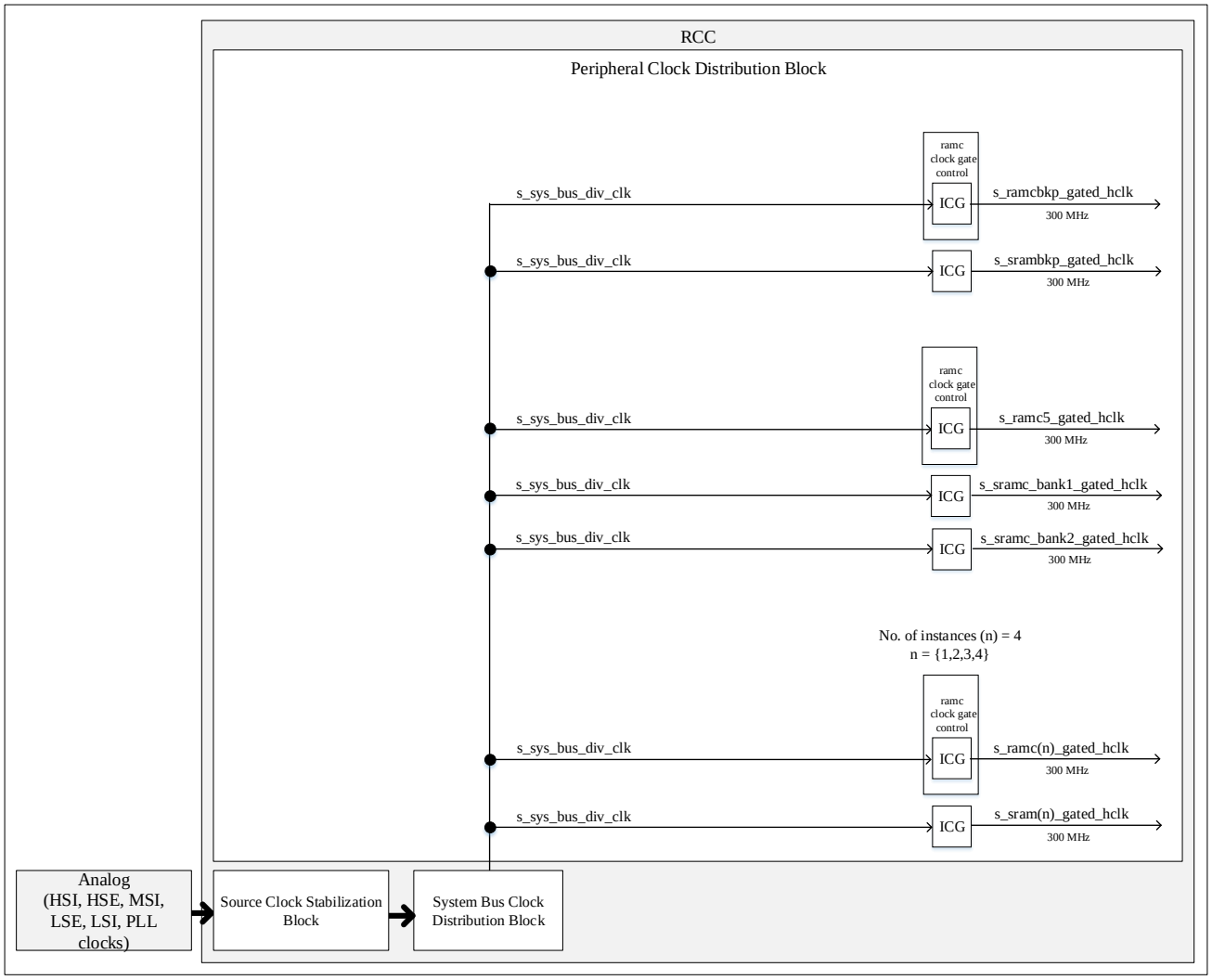
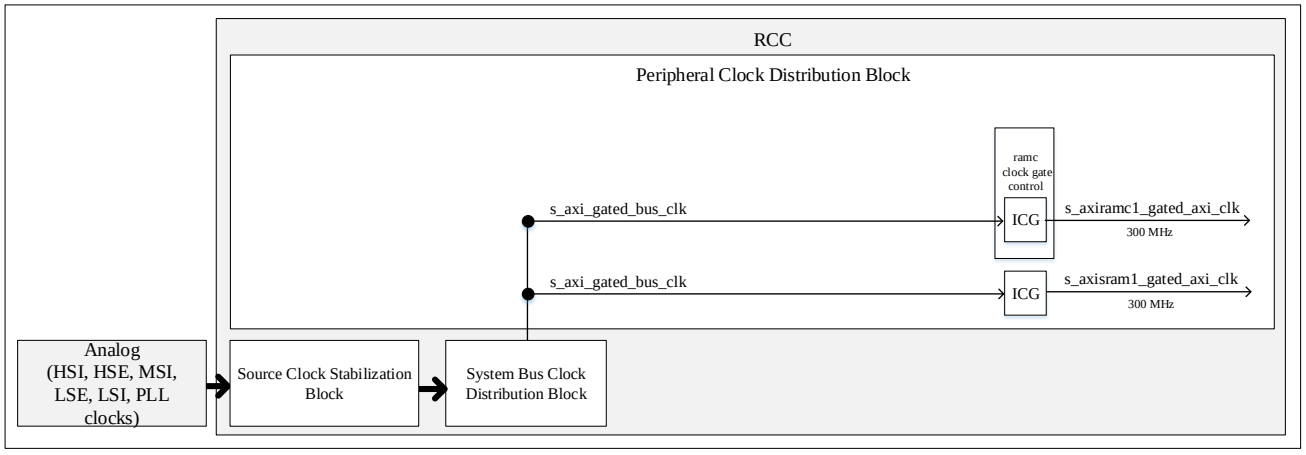


Figure 4-72 TCM_AXI_SRAM



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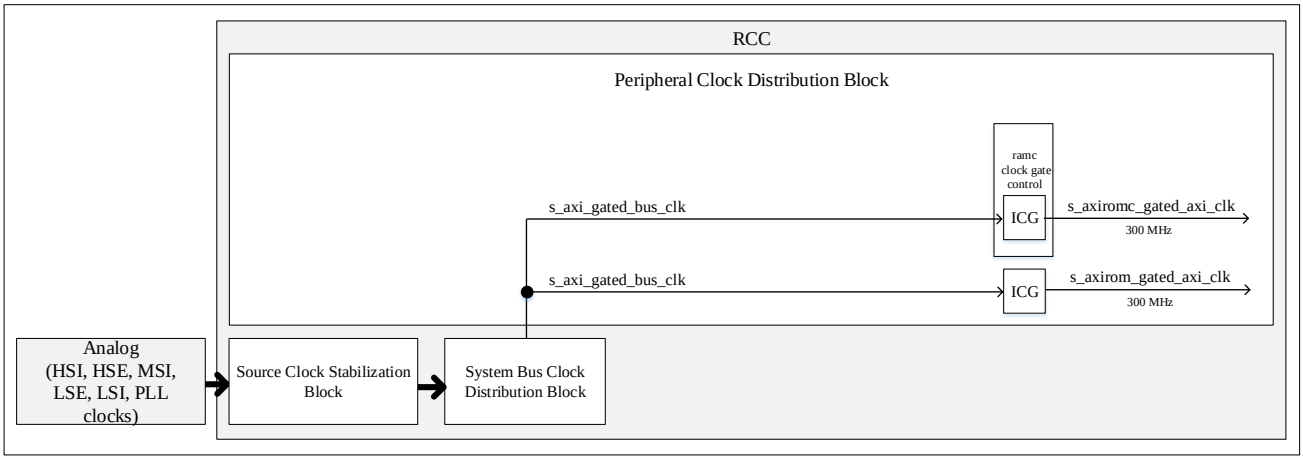
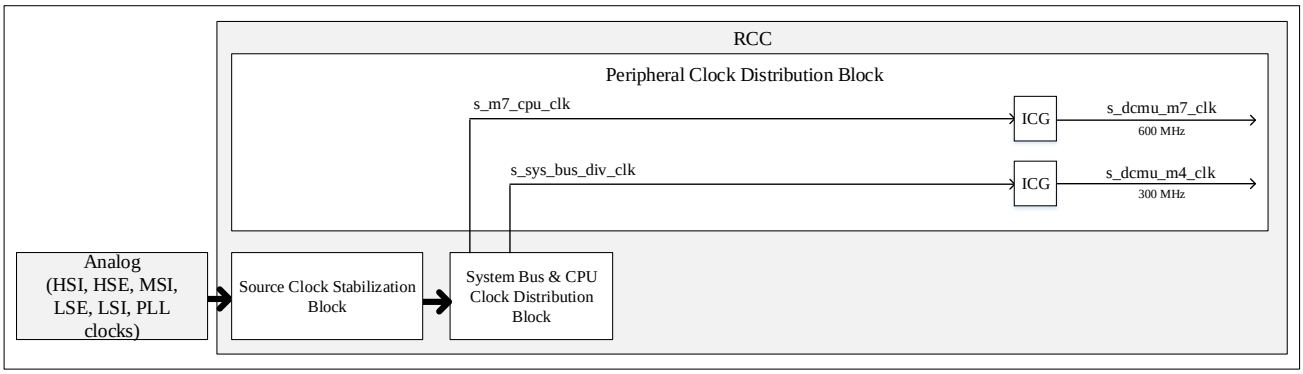
4.4.4.44 ROM

Figure 4-73 AXI_ROM



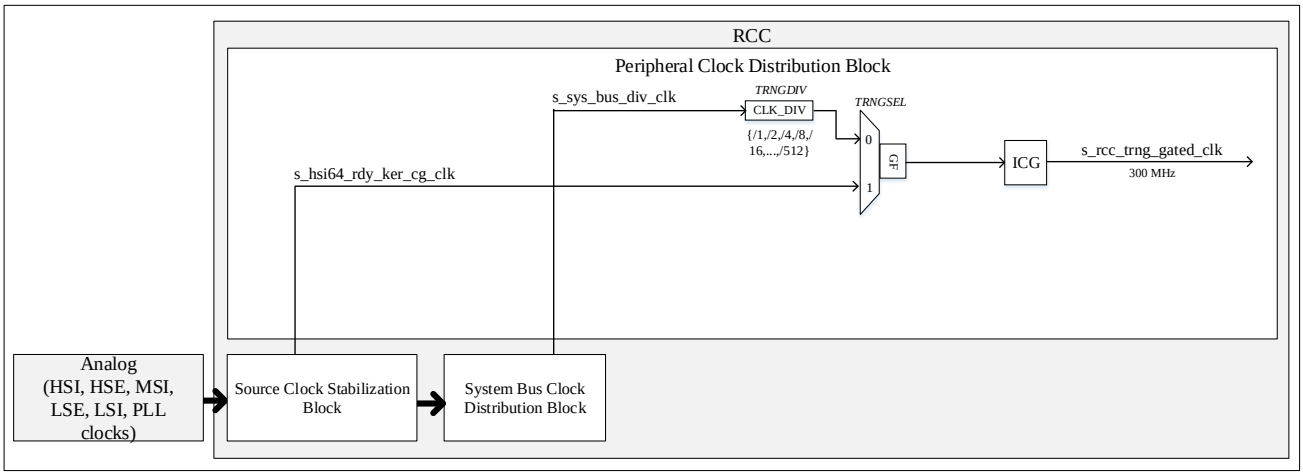
4.4.4.45 DCMU

Figure 4-74 DCMU



4.4.4.46 TRNG

Figure 4-75 TRNG



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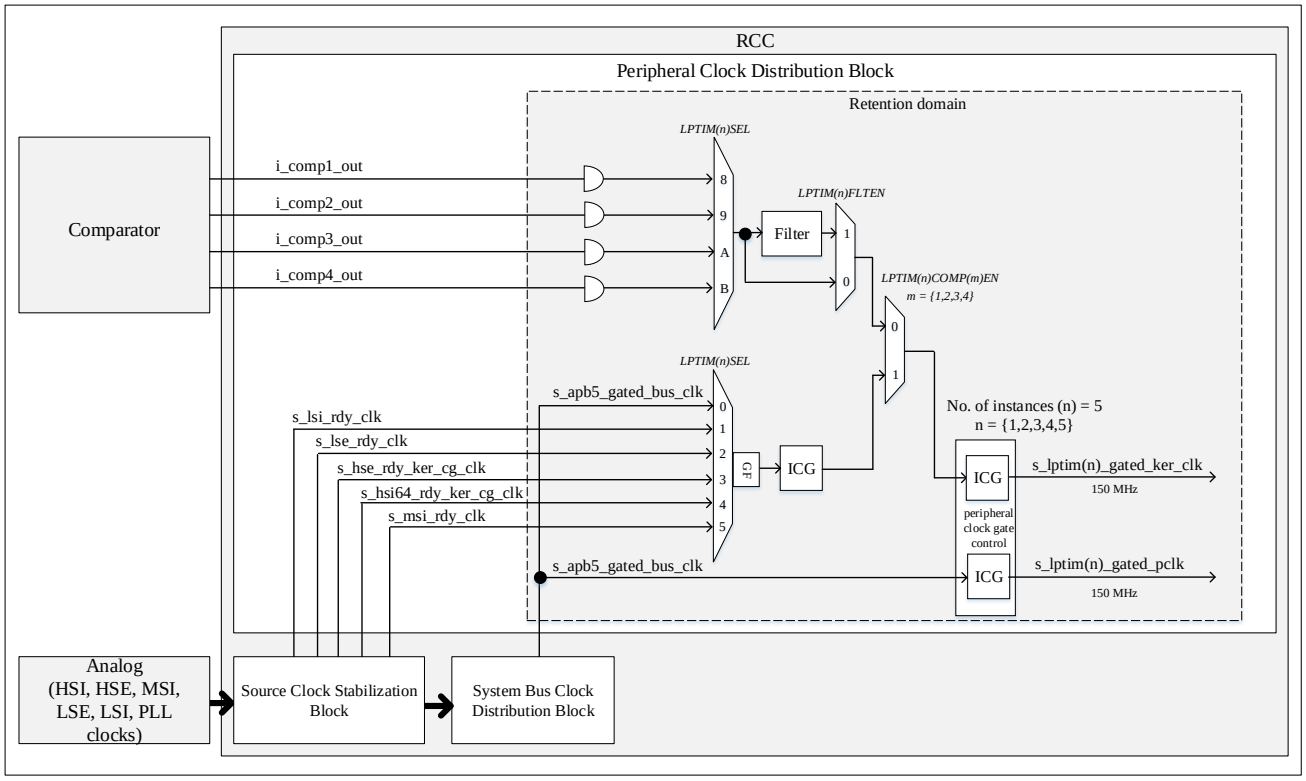
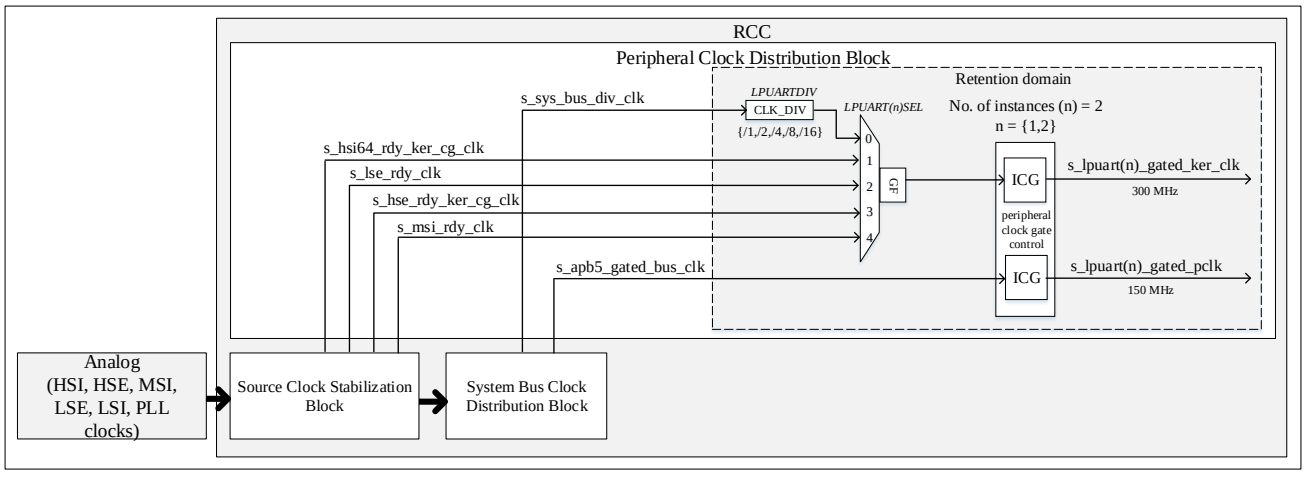
4.4.4.47 LPTIM

Figure 4-76 LPTIM(n) {n=1,2,3,4}



4.4.4.48 LPUART

Figure 4-77 LPUART(n) {n=1,2}



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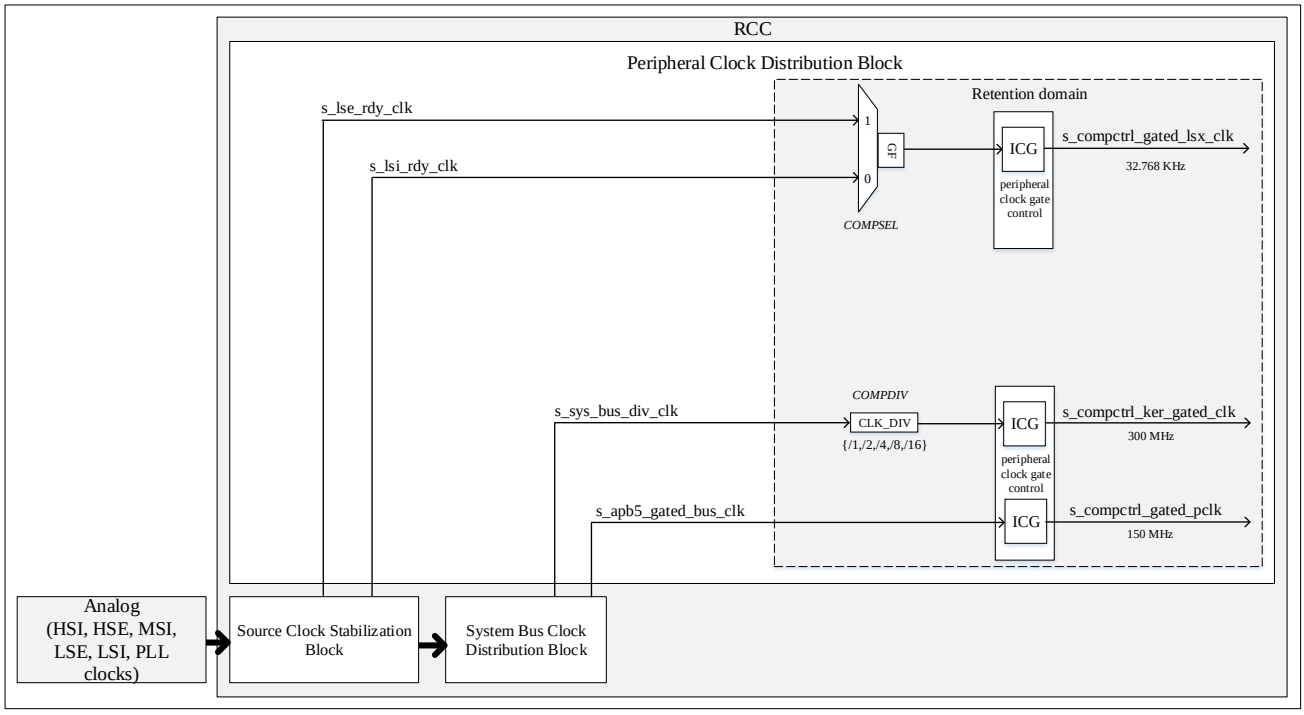
4.4.4.49 COMP

Figure 4-78 COMP



4.5 RCC Registers

4.5.1 PLL1 clock control register 1(RCC_PLL1CTRL1)

Address offset: 0x0000

Reset value: 0x19030004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		PLL1SRC[1:0]		Reserved							PLL1PHLK	PLL1LDOEN	PLL1EN	PLL1RST	PLL1PD
		rw									r	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PLL1BWAJ[11:0]											
				rw											

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:28	PLL1SRC[1:0]	PLL1 reference clock source selection 00: HSI Clock is the PLL source clock 01: No clock

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Bit field	Name	Description
		10: MSI Clock is the PLL source clock 11: HSE Clock is the PLL source clock
27:21	Reserved	Reserved, the reset value must be maintained.
20	PLL1PHLK	PLL1 phase Lock Set by hardware to indicate PLL phase lock. 0: PLL output clock is not phase locked to reference clock 1: PLL output clock is phase locked to reference clock.Use PLL output clock only after the lock bit is 1.
19	PLL1LDOEN	PLL1 LDO Enable Set and cleared by Software. 0: Disable PLL1 LDO 1: Enable PLL1 LDO
18	PLL1EN	PLL1 clock Enable Set and cleared by Software. 0: Disable PLL1 clock 1: Enable PLL1 clock *Note: PLL1 clock cannot be disable when used as system clock.*
17	PLL1RST	PLL1 Reset Set and cleared by software. 0: Clear reset 1: Reset PLL1
16	PLL1PD	PLL1 Power Down Set and cleared by software. 0: Enable power to analog circuitry in PLL 1: Disable power to analog circuitry in PLL
15:12	Reserved	Reserved, the reset value must be maintained.
11:0	PLL1BWAJ[11:0]	PLL1 Loop Bandwidth Adjustment The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 600 MHz.

4.5.2 PLL1 clock control register 2(RCC_PLL1CTRL2)

Address offset: 0x0004

Reset value: 0x00025800

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL1CLKR[5:0]						PLL1CLKF[25:0]									
rw						rw									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL1CLKF[25:0]															

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Bit field	Name	Description
31:26	PLL1CLKR[5:0]	PLL1 Reference Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 600 MHz.
25:0	PLL1CLKF[25:0]	PLL1 Feedback Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 600 MHz.

4.5.3 PLL2 clock control register 1(RCC_PLL2CTRL1)

Address offset: 0x0010

Reset value: 0x19030005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		PLL2SRC[1:0]		Reserved							PLL2PHLK	PLL2LDOEN	PLL2EN	PLL2RST	PLL2PD
		rw									r	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PLL2BWAJ[11:0]											
				rw											

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:28	PLL2SRC[1:0]	PLL2 reference clock source selection 00: HSI Clock is the PLL source clock 01: No clock 10: MSI Clock is the PLL source clock 11: HSE Clock is the PLL source clock
27:21	Reserved	Reserved, the reset value must be maintained.
20	PLL2PHLK	PLL2 phase Lock Set by hardware to indicate PLL phase lock. 0: PLL output clock is not phase locked to reference clock 1: PLL output clock is phase locked to reference clock.Use PLL output clock only after the lock bit is 1.
19	PLL2LDOEN	PLL2 LDO Enable Set and cleared by Software. 0: Disable PLL2 LDO

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Bit field	Name	Description
		1: Enable PLL2 LDO
18	PLL2EN	PLL2 clock Enable Set and cleared by Software. 0: Disable PLL2 clock 1: Enable PLL2 clock *Note: PLL2 clock cannot be disable when used as system clock.*
17	PLL2RST	PLL2 Reset Set and cleared by software. 0: Clear reset 1: Reset PLL2
16	PLL2PD	PLL2 Power Down Set and cleared by software. 0: Enable power to analog circuitry in PLL 1: Disable power to analog circuitry in PLL
15:12	Reserved	Reserved, the reset value must be maintained.
11:0	PLL2BWAJ[11:0]	PLL2 Loop Bandwidth Adjustment The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 800 MHz.

4.5.4 PLL2 clock control register 2(RCC_PLL2CTRL2)

Address offset: 0x0014

Reset value: 0x00032000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL2CLKR[5:0]						PLL2CLKF[25:0]									
rw						rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL2CLKF[25:0]															
rw															

Bit field	Name	Description
31:26	PLL2CLKR[5:0]	PLL2 Reference Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 800 MHz.
25:0	PLL2CLKF[25:0]	PLL2 Feedback Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 800 MHz.

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4.5.5 PLL3 clock control register 1(RCC_PLL3CTRL1)

Address offset: 0x0020

Reset value: 0x19030005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		PLL3SRC[1:0]		Reserved							PLL3PHLK	PLL3LDOEN	PLL3EN	PLL3RST	PLL3PD
		rw									r	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PLL3BWAJ[11:0]											
				rw											

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:28	PLL3SRC[1:0]	PLL3 reference clock source selection 00: HSI Clock is the PLL source clock 01: No clock 10: MSI Clock is the PLL source clock 11: HSE Clock is the PLL source clock
27:21	Reserved	Reserved, the reset value must be maintained.
20	PLL3PHLK	PLL3 phase Lock Set by hardware to indicate PLL phase lock. 0: PLL output clock is not phase locked to reference clock 1: PLL output clock is phase locked to reference clock.Use PLL output clock only after the lock bit is 1.
19	PLL3LDOEN	PLL3 LDO Enable Set and cleared by Software. 0: Disable PLL3 LDO 1: Enable PLL3 LDO
18	PLL3EN	PLL3 clock Enable Set and cleared by Software. 0: Disable PLL3 clock 1: Enable PLL3 clock *Note: PLL3 clock cannot be disable when used as system clock.*
17	PLL3RST	PLL3 Reset Set and cleared by software. 0: Clear reset 1: Reset PLL3
16	PLL3PD	PLL3 Power Down Set and cleared by software.

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Bit field	Name	Description
		0: Enable power to analog circuitry in PLL 1: Disable power to analog circuitry in PLL
15:12	Reserved	Reserved, the reset value must be maintained.
11:0	PLL3BWAJ[11:0]	PLL3 Loop Bandwidth Adjustment The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 800 MHz.

4.5.6 PLL3 clock control register 2(RCC_PLL3CTRL2)

Address offset: 0x0024

Reset value: 0x00032000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PLL3CLKR[5:0]						PLL3CLKF[25:0]									
rw						rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL3CLKF[25:0]															
rw															

Bit field	Name	Description
31:26	PLL3CLKR[5:0]	PLL3 Reference Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 800 MHz.
25:0	PLL3CLKF[25:0]	PLL3 Feedback Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 800 MHz.

4.5.7 SHRPLL clock control register 1(RCC_SHRPLLCTRL1)

Address offset: 0x018c

Reset value: 0x19030009

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SHRPLLSRC[1:0]		Reserved							SHRPLLPHLK	SHRPLLLDOEN	SHRPLLEN	SHRPLLRST	SHRPLLPD
		rw									r	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SHRPLLBWAJ[11:0]											

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Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:28	SHRPLLSRC[1:0]	SHRPLL reference clock source selection 00: HSI Clock is the PLL source clock 01: No clock 10: MSI Clock is the PLL source clock 11: HSE Clock is the PLL source clock
27:21	Reserved	Reserved, the reset value must be maintained.
20	SHRPLLPHLK	SHRPLL phase Lock Set by hardware to indicate PLL phase lock. 0: PLL output clock is not phase locked to reference clock 1: PLL output clock is phase locked to reference clock.Use PLL output clock only after the lock bit is 1.
19	SHRPLLLDOEN	SHRPLL LDO Enable Set and cleared by Software. 0: Disable SHRPLL LDO 1: Enable SHRPLL LDO
18	SHRPLLEN	SHRPLL clock Enable Set and cleared by Software. 0: Disable SHRPLL clock 1: Enable SHRPLL clock *Note: SHRPLL clock cannot be disable when used as system clock.*
17	SHRPLLRST	SHRPLL Reset Set and cleared by software. 0: Clear reset 1: Reset SHRPLL
16	SHRPLLPD	SHRPLL Power Down Set and cleared by software. 0: Enable power to analog circuitry in PLL 1: Disable power to analog circuitry in PLL
15:12	Reserved	Reserved, the reset value must be maintained.
11:0	SHRPLLBWAJ[11:0]	SHRPLL Loop Bandwidth Adjustment The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 312.5 MHz.

4.5.8 SHRPLL clock control register 2(RCC_SHRPLLCTRL2)

Address offset: 0x0190

Reset value: 0x0004e200

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHRPLLCLKR[5:0]						SHRPLLCLKF[25:0]									
rw						rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRPLLCLKF[25:0]															
rw															

Bit field	Name	Description
31:26	SHRPLLCLKR[5:0]	SHRPLL Reference Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 312.5 MHz.
25:0	SHRPLLCLKF[25:0]	SHRPLL Feedback Clock Divider The default value corresponds to PLL reference frequency of 64 MHz and output frequency of 312.5 MHz.

4.5.9 Clock source control register 1(RCC_SRCCTRL1)

Address offset: 0x0030

Reset value: 0x20000103

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFEMSIRDF	AFEHSIRDF	Reserved		SCLKSTS[1:0]		SCLKSW[1:0]		Reserved							
r	r			r		rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							HSERDCNTEN	MSIRDF	MSIEN	HSECSSEN	HSEBP	HSERDF	HSEEN	HSIRDF	HSIEN
							rw	r	rw	rw	rw	r	rw	r	rw

Bit field	Name	Description
31	AFEMSIRDF	AFE MSI Ready Flag 0: MSI is not ready 1: MSI is ready *Note: This bit switches to '0' when MSI trim value is changed. This bit is '1' does not indicate that MSI clock frequency is stable.*
30	AFEHSIRDF	AFE HSI Ready Flag 0: HSI is not ready 1: HSI is ready

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Bit field	Name	Description
		Note: This bit switches to '0' when HSI trim value is changed. This bit is '1' does not indicate that HSI clock frequency is stable.
29:28	Reserved	Reserved, the reset value must be maintained.
27:26	SCLKSTS[1:0]	System Clock Switch Selection Status 00: HSI is selected as the system clock 01: MSI is selected as the system clock 10: HSE is selected as the system clock 11: PLL1_A is selected as the system clock
25:24	SCLKSW[1:0]	System Clock Switch Selection. 00: HSI is selected as the system clock 01: MSI is selected as the system clock 10: HSE is selected as the system clock 11: PLL1_A is selected as the system clock
23:16	Reserved	Reserved, the reset value must be maintained.
15:9	Reserved	Reserved, the reset value must be maintained.
8	HSERDCNTEN	HSE ready generation counter enable Set and cleared by software. 0: Disable or Stop HSE ready counter 1: Enable or Start HSE ready counter
7	MSIRDF	MSI Ready Flag. Set by hardware to indicate that the MSI Clock is stable. 0: MSI clock is not stable. 1: MSI clock is stable.
6	MSIEN	MSI Clock Enable. Set and cleared by software. This bit cannot be cleared if the MSI clock is used directly or indirectly as the system clock. 0: Disable MSI clock. 1: Enable MSI clock.
5	HSECSSEN	HSE Clock Security System Enable. Set and cleared by software. 0: Disable HSE CSS. 1: Enable HSE CSS.
4	HSEBP	HSE clock bypass Set and cleared by software.This bit can be set only if the HSE oscillator is disabled. 0: HSE oscillator not bypassed. 1: HSE oscillator bypassed. *Note: Make sure HSEEN=0 before enabling HSEBP.*
3	HSERDF	HSE Ready Flag. Set by hardware to indicate that the HSE Clock is stable. 0: HSE clock is not stable. 1: HSE clock is stable.

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Bit field	Name	Description
2	HSEEN	HSE Clock Enable. Set and cleared by software. This bit cannot be cleared if the HSE clock is used directly or indirectly as the system clock. 0: Disable HSE clock 1: Enable HSE clock
1	HSIRDF	HSI Ready Flag Set by hardware to indicate that the HSI clock is stable. 0: HSI clock is not stable 1: HSI clock is stable
0	HSIEN	HSI Clock enable. Set and cleared by software. Set by hardware to enable HSI in case of failure of the HSE oscillator used directly or indirectly as system clock. This bit cannot be cleared if the HSI clock is used directly or indirectly as system clock. 0: Enable HSI clock. 1: Disable HSI clock.

4.5.10 Clock source control register 2(RCC_SRCCTRL2)

Address offset: 0x016c

Reset value: 0x00000f00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	BORF	HSICALEF	MSICALEF	Reserved										M7HYPSEL	AXIHYPSEL
	rc_w1	rc_w1	rc_w1											rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MSICAL[4:0]				Reserved			MSITRIM[4:0]				
				r							rw				

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	BORF	BOR status flag Set by hardware & cleared by software (write 1 to clear). 0 : BOR is not asserted 1 : BOR is asserted
29	HSICALEF	HSI calibration error status flag Set by hardware & cleared by software(write 1 to clear). 0 : No HSI calibration error

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Bit field	Name	Description
		1 : HSI calibration error occured
28	MSICALEF	MSI calibration error status flag Set by hardware & cleared by software(write 1 to clear). 0 : No MSI calibration error 1 : MSI calibration error occured
27:18	Reserved	Reserved, the reset value must be maintained.
17	M7HYPSEL	M7 hyper mode clock selection Set and cleared by software. 0: M7 CPU max clock frequency will be 600MHz which is supplied by PLL1A clock 1: M7 CPU max clock frequency will be 600MHz which is supplied by PLL2A clock
16	AXIHYPSEL	AXI hyper mode clock selection Set and cleared by software. 0: AXI bus max clock frequency will be 300MHz which is supplied by PLL1A clock 1: AXI bus max clock frequency will be 300MHz which is supplied by PLL2A clock
15:13	Reserved	Reserved, the reset value must be maintained.
12:8	MSICAL[4:0]	MSI clock calibration value. These bits represent the value after adding MSITRIM[4:0] to the internal calibration register value.
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	MSITRIM[4:0]	MSI clock trimming value. These bits can be programmed to adjust to variations in voltage and temperature that influence the frequency of the internal MSI RC. The overall trimming value of MSI is calculated by adding the MSI_TRIM[4:0] bits to internal calibration register value. The MSI_TRIM[4:0] bits are represented in 2's complement format. MSI_TRIM[4] = 1=> - trim value, MSI_TRIM[4] = 0 => + trim value, Every consecutive increment/decrement step will modify the MSI freqency by a step size of 33.2kHz.

4.5.11 Clock source control register 3(RCC_SRCCTRL3)

Address offset: 0x01dc

Reset value: 0x01600000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							HSICAL[8:0]								
							r								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							HSITRIM[8:0]								
							rw								

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Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:16	HSICAL[8:0]	HSI clock calibration value. These bits represent the value after adding HSITRIM[8:0] to the internal calibration register value.
15:9	Reserved	Reserved, the reset value must be maintained.
8:0	HSITRIM[8:0]	HSI clock trimming value. These bits can be programmed to adjust to variations in voltage and temperature that influence the frequency of the internal HSI RC. The overall trimming value of HSI is calculated by adding the HSITRIM[8:0] bits to internal calibration register value. The HSI_TRIM[8:0] bits are represented in 2's complement format. HSI_TRIM[8] = 1=> - trim value, HSI_TRIM[8] = 0 => + trim value, Every consecutive increment/decrement step will modify the HSI freqency by a step size of 150kHz.

4.5.12 PLL1 clock divider register(RCC_PLL1DIV)

Address offset: 0x0034

Reset value: 0x00020202

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										PLL1CDIV[5:0]					
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		PLL1BDIV[5:0]						Reserved		PLL1ADIV[5:0]					
		rw								rw					

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:22	Reserved	Reserved, the reset value must be maintained.
21:16	PLL1CDIV[5:0]	PLL1C divider values. Configure PLL1 divider value to PLL1C. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7

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Bit field	Name	Description
		001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
15:14	Reserved	Reserved, the reset value must be maintained.
13:8	PLL1BDIV[5:0]	PLL1B divider values. Configure PLL1 divider value to PLL1B. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	PLL1ADIV[5:0]	PLL1A divider values. Configure PLL1 divider value to PLL1A. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63

4.5.13 PLL2 clock divider register(RCC_PLL2DIV)

Address offset: 0x0038

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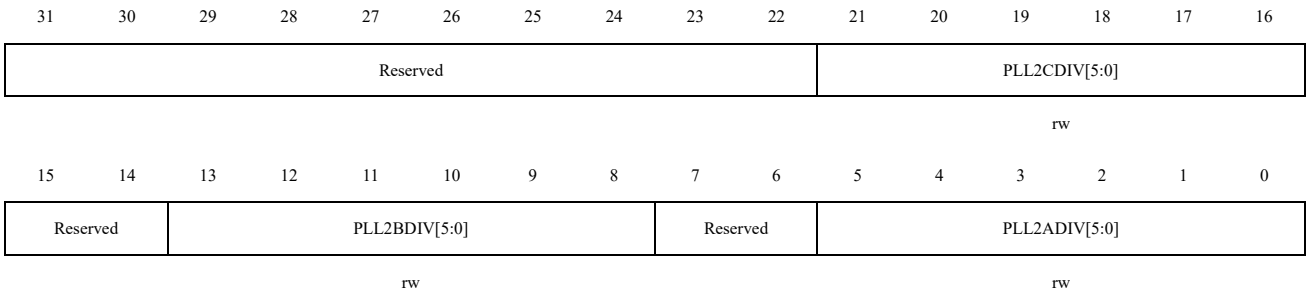
Reset value: 0x00020202



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:22	Reserved	Reserved, the reset value must be maintained.
21:16	PLL2CDIV[5:0]	PLL2C divider values. Configure PLL2 divider value to PLL2C. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
15:14	Reserved	Reserved, the reset value must be maintained.
13:8	PLL2BDIV[5:0]	PLL2B divider values. Configure PLL2 divider value to PLL2B. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 …

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Bit field	Name	Description
		111110: Divide by 62 111111: Divide by 63
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	PLL2ADIV[5:0]	PLL2A divider values. Configure PLL2 divider value to PLL2A. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63

4.5.14 PLL3 clock divider register(RCC_PLL3DIV)

Address offset: 0x003c

Reset value: 0x00020202

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										PLL3CDIV[5:0]					
										Rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		PLL3BDIV[5:0]						Reserved		PLL3ADIV[5:0]					
		rw								rw					

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:22	Reserved	Reserved, the reset value must be maintained.
21:16	PLL3CDIV[5:0]	PLL3C divider values. Configure PLL3 divider value to PLL3C. 000001: Divide by 1 (bypass) 000010: Divide by 2

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Bit field	Name	Description
		000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
15:14	Reserved	Reserved, the reset value must be maintained.
13:8	PLL3BDIV[5:0]	PLL3B divider values. Configure PLL3 divider value to PLL3B. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	PLL3ADIV[5:0]	PLL3A divider values. Configure PLL3 divider value to PLL3A. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62

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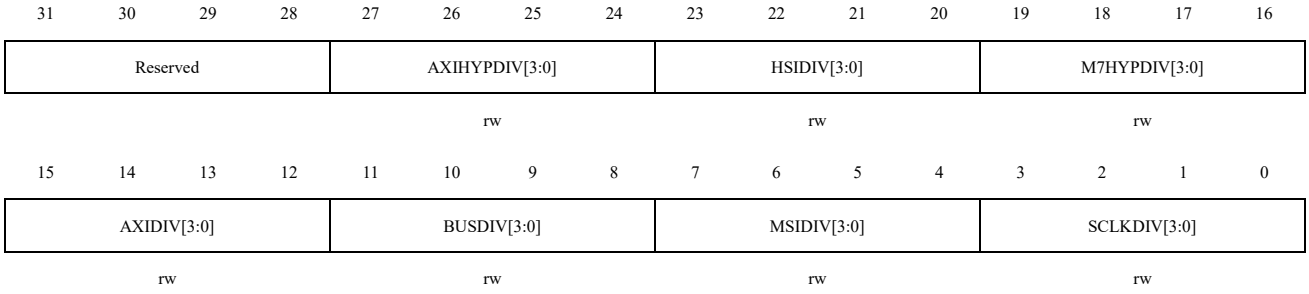
Bit field	Name	Description
		111111: Divide by 63

4.5.15 System bus divider register 1(RCC_SYSBUSDIV1)

Address offset: 0x0040

Reset value: 0x00000000



Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:24	AXIHYPDIV[3:0]	AXI Clock Hyper Mode divider values. Obtained by dividing the m7_hyp_div_clk. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
23:20	HSIDIV[3:0]	HSI Clock divider values. Obtained by dividing the HSI clock. *Note: All HSI are divided clocks except PLL clock sources* 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8

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Bit field	Name	Description
		0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
19:16	M7HYPDIV[3:0]	M7 Clock Hyper Mode divider values. Configure PLL2A divider value to m7_hyp_div_clk. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
15:12	AXIDIV[3:0]	AXI clock divider values. Obtained by dividing the sys_div_clk. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
11:8	BUSDIV[3:0]	System bus clock divider values. Configure sys_div_clk divider value to sys_bus_div_clk. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64

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Bit field	Name	Description
		1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
7:4	MSIDIV[3:0]	MSI clock divider values. Obtained by dividing the MSI clock. *Note: All MSI are divided clocks except PLL clock sources* 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
3:0	SCLKDIV[3:0]	System clock divider values. Configure sys_clk divider value to sys_div_clk. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed

4.5.16 System bus divider register 2(RCC_SYSBUSDIV2)

Address offset: 0x0044

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					APB6DIV[2:0]			Reserved					APB5DIV[2:0]		

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						rw									rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved					APB2DIV[2:0]			Reserved					APB1DIV[2:0]			
						rw									rw	

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:24	APB6DIV[2:0]	APB6 clock divider values. Configure AHB6 clock divider value to APB6 clock. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
23:19	Reserved	Reserved, the reset value must be maintained.
18:16	APB5DIV[2:0]	APB5 clock divider values. Configure AHB5 clock divider value to APB5 clock. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
15:11	Reserved	Reserved, the reset value must be maintained.
10:8	APB2DIV[2:0]	APB2 clock divider values. Configure AHB2 clock divider value to APB2 clock. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
7:3	Reserved	Reserved, the reset value must be maintained.
2:0	APB1DIV[2:0]	APB1 clock divider values. Configure AHB1 clock divider value to APB1 clock. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16

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4.5.17 BOOT mode register(RCC_BOOTMODE)

Address offset: 0x0048

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODE[31:0]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE[31:0]															
r															

Bit field	Name	Description
[31:0]	MODE[31:0]	The boot mode value from SMU(System Management Unit) is written into this register when "flow done" signal is high. 0: Internal Boot (Flash), Can be SIP(Silicon-In-Package) Flash or External Flash 1: Serial Downloader, Download program image from selected serial port into SRAM and execute it from SRAM

4.5.18 AHB1 peripherals clock divider register 1(RCC_AHB1DIV1)

Address offset: 0x004c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETH2SYSDIV[3:0]				SDMMC2SYSDIV[3:0]				Reserved							
rw				rw											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:28	ETH2SYSDIV[3:0]	Ethernet2 system clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8

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Bit field	Name	Description
		0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
27:24	SDMMC2SYSDIV[3:0]	SDMMC2 system clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
23:0	Reserved	Reserved, the reset value must be maintained.

4.5.19 AHB1 peripherals clock divider register 2(RCC_AHB1DIV2)

Address offset: 0x0194

Reset value: 0x00020202

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										ADC3SYSDIV[5:0]					
										rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		ADC2SYSDIV[5:0]						Reserved		ADC1SYSDIV[5:0]					
		rw								rw					

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21:16	ADC3SYSDIV[5:0]	ADC3 system clock prescalar values. 000001: Divide by 1 (bypass) 000010: Divide by 2

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Bit field	Name	Description
		000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
15:14	Reserved	Reserved, the reset value must be maintained.
13:8	ADC2SYSDIV[5:0]	ADC2 system clock prescalar values. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	ADC1SYSDIV[5:0]	ADC1 system clock prescalar values. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63

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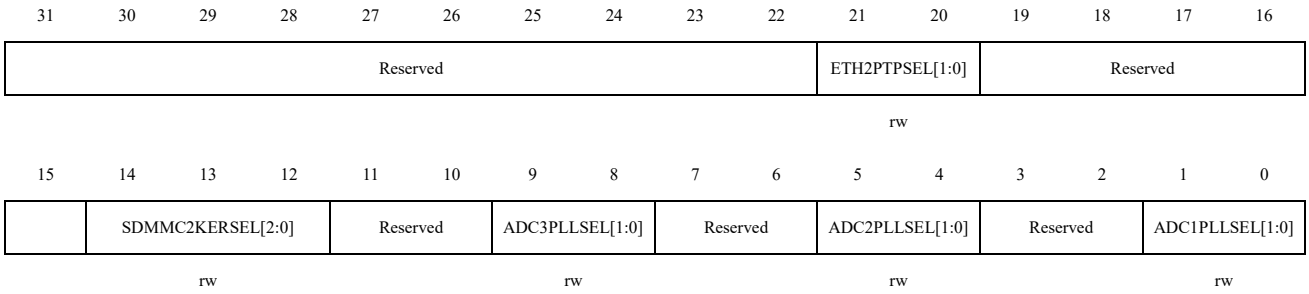
4.5.20 AHB1 peripherals clock source select register 1(RCC_AHB1SEL1)

Address offset: 0x0050

Reset value: 0x00000000



Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21:20	ETH2PTPSEL[1:0]	Ethernet2 PTP clock selection. 00: Divided system bus clock is selected as Ethernet2 PTP clock 01: Peripheral clock is selected as Ethernet2 PTP clock 10: PLL2_C clock is selected as Ethernet2 PTP clock 11: PLL3_A clock is selected as Ethernet2 PTP clock
19:15	Reserved	Reserved, the reset value must be maintained.
14:12	SDMMC2KERSEL[2:0]	SDMMC2 Kernel clock selection. 000: System bus clock is selected as SDMMC2 kernel clock 001: Peripheral clock is selected as SDMMC2 kernel clock 010: PLL2_A clock is selected as SDMMC2 kernel clock 011: PLL3_A clock is selected as SDMMC2 kernel clock 100: PLL1_B clock is selected as SDMMC2 kernel clock Other values: setting is not allowed
11:10	Reserved	Reserved, the reset value must be maintained.
9:8	ADC3PLLSEL[1:0]	ADC3 PLL clock selection 00: PLL2_B clock is selected as ADC3 PLL clock 01: PLL1_B clock is selected as ADC3 PLL clock 10: PLL3_B clock is selected as ADC3 PLL clock 11: PLL3_C clock is selected as ADC3 PLL clock
7:6	Reserved	Reserved, the reset value must be maintained.
5:4	ADC2PLLSEL[1:0]	ADC2 PLL clock selection 00: PLL2_B clock is selected as ADC2 PLL clock 01: PLL1_B clock is selected as ADC2 PLL clock 10: PLL3_B clock is selected as ADC2 PLL clock 11: PLL3_C clock is selected as ADC2 PLL clock

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Bit field	Name	Description
3:2	Reserved	Reserved, the reset value must be maintained.
1:0	ADC1PLLSEL[1:0]	ADC1 PLL clock selection 00: PLL2_B clock is selected as ADC1 PLL clock 01: PLL1_B clock is selected as ADC1 PLL clock 10: PLL3_B clock is selected as ADC1 PLL clock 11: PLL3_C clock is selected as ADC1 PLL clock

4.5.21 AHB1 peripherals clock enable register 1(RCC_AHB1EN1)

Address offset: 0x0054

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7SDMMC2EN	M4SDMMC2EN	M7SDMMC2LPEN	M4SDMMC2LPEN	Reserved				M7USB2EN	M4USB2EN	M7USB2LPEN	M4USB2LPEN	M7DMAMUX1EN	M4DMAMUX1EN	M7DMAMUX1LPEN	M4DMAMUX1LPEN
rw	rw	rw	rw					rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7ADC1PLLEN	M4ADC1PLLEN	M7ADC1PLLLPEN	M4ADC1PLLLPEN	M7ADC1SYSEN	M4ADC1SYSEN	M7ADC1SYSLPEN	M4ADC1SYSLPEN	Reserved				M7ADC1BUSEN	M4ADC1BUSEN	M7ADC1BUSLPEN	M4ADC1BUSLPEN
rw	rw	rw	rw	rw	rw	rw	rw					rw	rw	rw	rw

Bit field	Name	Description
31	M7SDMMC2EN	SDMMC2 M7 allocation and clock enable. Set and cleared by software. 0: SDMMC2 is not allocated to M7. The "sdmmc2_gated_ker_clk" and "sdmmc2_gated_hclk" are disabled in M7 RUN mode. 1: SDMMC2 is allocated to M7. The "sdmmc2_gated_ker_clk" and "sdmmc2_gated_hclk" are enabled in M7 RUN mode.
30	M4SDMMC2EN	SDMMC2 M4 allocation and clock enable. Set and cleared by software. 0: SDMMC2 is not allocated to M4. The "sdmmc2_gated_ker_clk" and "sdmmc2_gated_hclk" are disabled in M4 RUN mode. 1: SDMMC2 is allocated to M4. The "sdmmc2_gated_ker_clk" and "sdmmc2_gated_hclk" are enabled in M4 RUN mode.
29	M7SDMMC2LPEN	SDMMC2 M7 Low Power clock Enable. Set and cleared by software. 0: The "sdmmc2_gated_ker_clk" and "sdmmc2_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "sdmmc2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "sdmmc2_gated_hclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7SDMMC2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4SDMMC2LPEN	SDMMC2 M4 Low Power clock Enable. Set and cleared by software. 0: The "sdmmc2_gated_ker_clk" and "sdmmc2_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "sdmmc2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "sdmmc2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4SDMMC2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27:24	Reserved	Reserved, the reset value must be maintained.
23	M7USB2EN	USB2 M7 allocation and clock enable. Set and cleared by software. 0: USB2 is not allocated to M7. The "usb2_gated_hclk" is disabled in M7 RUN mode. 1: USB2 is allocated to M7. The "usb2_gated_hclk" is enabled in M7 RUN mode.
22	M4USB2EN	USB2 M4 allocation and clock enable. Set and cleared by software. 0: USB2 is not allocated to M4. The "usb2_gated_hclk" is disabled in M4 RUN mode. 1: USB2 is allocated to M4. The "usb2_gated_hclk" is enabled in M4 RUN mode.
21	M7USB2LPEN	USB2 M7 Low Power clock Enable. Set and cleared by software. 0: The "usb2_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usb2_gated_hclk" is enabled in M7 SLEEP mode. Note : M7USB2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4USB2LPEN	USB2 M4 Low Power clock Enable. Set and cleared by software. 0: The "usb2_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usb2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4USB2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7DMAMUX1EN	DMAMUX1 M7 allocation and clock enable. Set and cleared by software. 0: DMAMUX1 is not allocated to M7. The "dma_mux1_gated_hclk" is disabled in M7 RUN mode. 1: DMAMUX1 is allocated to M7. The "dma_mux1_gated_hclk" is enabled in M7 RUN mode.
18	M4DMAMUX1EN	DMAMUX1 M4 allocation and clock enable. Set and cleared by software. 0: DMAMUX1 is not allocated to M4. The "dma_mux1_gated_hclk" is disabled in M4 RUN mode.

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Bit field	Name	Description
		1: DMAMUX1 is allocated to M4. The "dma_mux1_gated_hclk" is enabled in M4 RUN mode.
17	M7DMAMUX1LPEN	DMAMUX1 M7 Low Power clock Enable. Set and cleared by software. 0: The "dma_mux1_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "dma_mux1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DMAMUX1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4DMAMUX1LPEN	DMAMUX1 M4 Low Power clock Enable. Set and cleared by software. 0: The "dma_mux1_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "dma_mux1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DMAMUX1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7ADC1PLLEN	ADC1PLL M7 allocation and clock enable. Set and cleared by software. 0: ADC1PLL is not allocated to M7. The "adc1_pll_div_gated_clk" is disabled in M7 RUN mode. 1: ADC1PLL is allocated to M7. The "adc1_pll_div_gated_clk" is enabled in M7 RUN mode.
14	M4ADC1PLLEN	ADC1PLL M4 allocation and clock enable. Set and cleared by software. 0: ADC1PLL is not allocated to M4. The "adc1_pll_div_gated_clk" is disabled in M4 RUN mode. 1: ADC1PLL is allocated to M4. The "adc1_pll_div_gated_clk" is enabled in M4 RUN mode.
13	M7ADC1PLLLPEN	ADC1PLL M7 Low Power clock Enable. Set and cleared by software. 0: The "adc1_pll_div_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc1_pll_div_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ADC1PLLEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4ADC1PLLLPEN	ADC1PLL M4 Low Power clock Enable. Set and cleared by software. 0: The "adc1_pll_div_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc1_pll_div_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ADC1PLLEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7ADC1SYSEN	ADC1SYS M7 allocation and clock enable. Set and cleared by software. 0: ADC1SYS is not allocated to M7. The "adc1_sys_div_gated_clk" is disabled in M7 RUN mode.

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Bit field	Name	Description
		1: ADC1SYS is allocated to M7. The "adc1_sys_div_gated_clk" is enabled in M7 RUN mode.
10	M4ADC1SYSEN	ADC1SYS M4 allocation and clock enable. Set and cleared by software. 0: ADC1SYS is not allocated to M4. The "adc1_sys_div_gated_clk" is disabled in M4 RUN mode. 1: ADC1SYS is allocated to M4. The "adc1_sys_div_gated_clk" is enabled in M4 RUN mode.
9	M7ADC1SYSLPEN	ADC1SYS M7 Low Power clock Enable. Set and cleared by software. 0: The "adc1_sys_div_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc1_sys_div_gated_clk" clock is enabled in M7 SLEEP and STOP mode. Note : M7ADC1SYSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4ADC1SYSLPEN	ADC1SYS M4 Low Power clock Enable. Set and cleared by software. 0: The "adc1_sys_div_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc1_sys_div_gated_clk" clock is enabled in M4 SLEEP and STOP mode. Note : M4ADC1SYSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7:4	Reserved	Reserved, the reset value must be maintained.
3	M7ADC1BUSEN	ADC1BUS M7 allocation and clock enable. Set and cleared by software. 0: ADC1BUS is not allocated to M7. The "adc1_gated_hclk" is disabled in M7 RUN mode. 1: ADC1BUS is allocated to M7. The "adc1_gated_hclk" is enabled in M7 RUN mode.
2	M4ADC1BUSEN	ADC1BUS M4 allocation and clock enable. Set and cleared by software. 0: ADC1BUS is not allocated to M4. The "adc1_gated_hclk" is disabled in M4 RUN mode. 1: ADC1BUS is allocated to M4. The "adc1_gated_hclk" is enabled in M4 RUN mode.
1	M7ADC1BUSLPEN	ADC1BUS M7 Low Power clock Enable. Set and cleared by software. 0: The "adc1_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7ADC1BUSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4ADC1BUSLPEN	ADC1BUS M4 Low Power clock Enable. Set and cleared by software. 0: The "adc1_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ADC1BUSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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4.5.22 AHB1 peripherals clock enable register 2(RCC_AHB1EN2)

Address offset: 0x0058

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				M7ETH2TXEN	M4ETH2TXEN	M7ETH2TXLPEN	M4ETH2TXLPEN	M7ETH2RXEN	M4ETH2RXEN	M7ETH2RXLPEN	M4ETH2RXLPEN	M7ETH2MACEN	M4ETH2MACEN	M7ETH2MACLPEN	M4ETH2MACLPEN
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	M7ETH2TXEN	ETH2TX M7 allocation and clock enable. Set and cleared by software. 0: ETH2TX is not allocated to M7. The "eth2_mii_tx_gated_clk" is disabled in M7 RUN mode. 1: ETH2TX is allocated to M7. The "eth2_mii_tx_gated_clk" is enabled in M7 RUN mode.
10	M4ETH2TXEN	ETH2TX M4 allocation and clock enable. Set and cleared by software. 0: ETH2TX is not allocated to M4. The "eth2_mii_tx_gated_clk" is disabled in M4 RUN mode. 1: ETH2TX is allocated to M4. The "eth2_mii_tx_gated_clk" is enabled in M4 RUN mode.
9	M7ETH2TXLPEN	ETH2TX M7 Low Power clock Enable. Set and cleared by software. 0: The "eth2_mii_tx_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "eth2_mii_tx_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ETH2TXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4ETH2TXLPEN	ETH2TX M4 Low Power clock Enable. Set and cleared by software. 0: The "eth2_mii_tx_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "eth2_mii_tx_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ETH2TXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7ETH2RXEN	ETH2RX M7 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: ETH2RX is not allocated to M7. The "eth2_mii_rx_gated_clk" is disabled in M7 RUN mode. 1: ETH2RX is allocated to M7. The "eth2_mii_rx_gated_clk" is enabled in M7 RUN mode.
6	M4ETH2RXEN	ETH2RX M4 allocation and clock enable. Set and cleared by software. 0: ETH2RX is not allocated to M4. The "eth2_mii_rx_gated_clk" is disabled in M4 RUN mode. 1: ETH2RX is allocated to M4. The "eth2_mii_rx_gated_clk" is enabled in M4 RUN mode.
5	M7ETH2RXLPEN	ETH2RX M7 Low Power clock Enable. Set and cleared by software. 0: The "eth2_mii_rx_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "eth2_mii_rx_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ETH2RXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4ETH2RXLPEN	ETH2RX M4 Low Power clock Enable. Set and cleared by software. 0: The "eth2_mii_rx_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "eth2_mii_rx_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ETH2RXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7ETH2MACEN	ETH2MAC M7 allocation and clock enable. Set and cleared by software. 0: ETH2MAC is not allocated to M7. The "eth2_gated_hclk" and "eth2_ptp_gated_clk" are disabled in M7 RUN mode. 1: ETH2MAC is allocated to M7. The "eth2_gated_hclk" and "eth2_ptp_gated_clk" are enabled in M7 RUN mode.
2	M4ETH2MACEN	ETH2MAC M4 allocation and clock enable. Set and cleared by software. 0: ETH2MAC is not allocated to M4. The "eth2_gated_hclk" and "eth2_ptp_gated_clk" are disabled in M4 RUN mode. 1: ETH2MAC is allocated to M4. The "eth2_gated_hclk" and "eth2_ptp_gated_clk" are enabled in M4 RUN mode.
1	M7ETH2MACLPEN	ETH2MAC M7 Low Power clock Enable. Set and cleared by software. 0: The "eth2_gated_hclk" and "eth2_ptp_gated_clk" clock are disabled in M7 SLEEP and STOP mode. 1: The "eth2_gated_hclk" is enabled in M7 SLEEP mode. The "eth2_ptp_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ETH2MACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4ETH2MACLPEN	ETH2MAC M4 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "eth2_gated_hclk" and "eth2_ptp_gated_clk" clock are disabled in M4 SLEEP and STOP mode. 1: The "eth2_gated_hclk" is enabled in M4 SLEEP mode. The "eth2_ptp_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ETH2MACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.23 AHB1 peripherals clock enable register 3(RCC_AHB1EN3)

Address offset: 0x005c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				M7ECCMACEN	M4ECCMACEN	M7ECCMACLPEN	M4ECCMACLPEN	Reserved				M7DMA1EN	M4DMA1EN	M7DMA1LPEN	M4DMA1LPEN
				rw	rw	rw	rw					rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				M7DMA2EN	M4DMA2EN	M7DMA2LPEN	M4DMA2LPEN	Reserved				M7DMA3EN	M4DMA3EN	M7DMA3LPEN	M4DMA3LPEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit field	Name	Description
31:28	Reserved	
27	M7ECCMACEN	ECCMON_AHBCACHE M7 allocation and clock enable. Set and cleared by software. 0: ECCMON_AHBCACHE is not allocated to M7. The "eccmon_ahbcache_gated_hclk" is disabled in M7 RUN mode. 1: ECCMON_AHBCACHE is allocated to M7. The "eccmon_ahbcache_gated_hclk" is enabled in M7 RUN mode.
26	M4ECCMACEN	ECCMON_AHBCACHE M4 allocation and clock enable. Set and cleared by software. 0: ECCMON_AHBCACHE is not allocated to M4. The "eccmon_ahbcache_gated_hclk" is disabled in M4 RUN mode. 1: ECCMON_AHBCACHE is allocated to M4. The "eccmon_ahbcache_gated_hclk" is enabled in M4 RUN mode.
25	M7ECCMACLPEN	ECCMON_AHBCACHE M7 Low Power clock Enable. Set and cleared by software. 0: The "eccmon_ahbcache_gated_hclk" is disabled in M7 SLEEP and STOP mode. 1: The "eccmon_ahbcache_gated_hclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7ECCMACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4ECCMACLPEN	ECCMON_AHBCACHE M4 Low Power clock Enable. Set and cleared by software. 0: The "eccmon_ahbcache_gated_hclk" is disabled in M4 SLEEP and STOP mode. 1: The "eccmon_ahbcache_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ECCMACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23:20	Reserved	Reserved, the reset value must be maintained.
19	M7DMA1EN	DMA1 M7 allocation and clock enable. Set and cleared by software. 0: DMA1 is not allocated to M7. The "dma1_gated_hclk" is disabled in M7 RUN mode. 1: DMA1 is allocated to M7. The "dma1_gated_hclk" is enabled in M7 RUN mode.
18	M4DMA1EN	DMA1 M4 allocation and clock enable. Set and cleared by software. 0: DMA1 is not allocated to M4. The "dma1_gated_hclk" is disabled in M4 RUN mode. 1: DMA1 is allocated to M4. The "dma1_gated_hclk" is enabled in M4 RUN mode.
17	M7DMA1LPEN	DMA1 M7 Low Power clock Enable. Set and cleared by software. 0: The "dma1_gated_hclk" is disabled in M7 SLEEP and STOP mode. 1: The "dma1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DMA1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4DMA1LPEN	DMA1 M4 Low Power clock Enable. Set and cleared by software. 0: The "dma1_gated_hclk" is disabled in M4 SLEEP and STOP mode. 1: The "dma1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DMA1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15:12	Reserved	Reserved, the reset value must be maintained.
11	M7DMA2EN	DMA2 M7 allocation and clock enable. Set and cleared by software. 0: DMA2 is not allocated to M7. The "dma2_gated_hclk" is disabled in M7 RUN mode. 1: DMA2 is allocated to M7. The "dma2_gated_hclk" is enabled in M7 RUN mode.
10	M4DMA2EN	DMA2 M4 allocation and clock enable. Set and cleared by software. 0: DMA2 is not allocated to M4. The "dma2_gated_hclk" is disabled in M4 RUN mode. 1: DMA2 is allocated to M4. The "dma2_gated_hclk" is enabled in M4 RUN mode.
9	M7DMA2LPEN	DMA2 M7 Low Power clock Enable. Set and cleared by software. 0: The "dma2_gated_hclk" is disabled in M7 SLEEP and STOP mode. 1: The "dma2_gated_hclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7DMA2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4DMA2LPEN	DMA2 M4 Low Power clock Enable. Set and cleared by software. 0: The "dma2_gated_hclk" is disabled in M4 SLEEP and STOP mode. 1: The "dma2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DMA2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7:4	Reserved	Reserved, the reset value must be maintained.
3	M7DMA3EN	DMA3 M7 allocation and clock enable. Set and cleared by software. 0: DMA3 is not allocated to M7. The "dma3_gated_hclk" is disabled in M7 RUN mode. 1: DMA3 is allocated to M7. The "dma3_gated_hclk" is enabled in M7 RUN mode.
2	M4DMA3EN	DMA3 M4 allocation and clock enable. Set and cleared by software. 0: DMA3 is not allocated to M4. The "dma3_gated_hclk" is disabled in M4 RUN mode. 1: DMA3 is allocated to M4. The "dma3_gated_hclk" is enabled in M4 RUN mode.
1	M7DMA3LPEN	DMA3 M7 Low Power clock Enable. Set and cleared by software. 0: The "dma3_gated_hclk" is disabled in M7 SLEEP and STOP mode. 1: The "dma3_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DMA3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4DMA3LPEN	DMA3 M4 Low Power clock Enable. Set and cleared by software. 0: The "dma3_gated_hclk" is disabled in M4 SLEEP and STOP mode. 1: The "dma3_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DMA3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.24 AHB1 peripherals clock enable register 4(RCC_AHB1EN4)

Address offset: 0x0060

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7ADC2PLLEN	M4ADC2PLLEN	M7ADC2PLLLPEN	M4ADC2PLLLPEN	M7ADC2SYSEN	M4ADC2SYSEN	M7ADC2SYSLPEN	M4ADC2SYSLPEN	Reserved				M7ADC2BUSEN	M4ADC2BUSEN	M7ADC2BUSLPEN	M4ADC2BUSLPEN
rw	rw	rw	rw	rw	rw	rw	rw					rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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M7ADC3PLLEN	M4ADC3PLLEN	M7ADC3PLLLPEN	M4ADC3PLLLPEN	M7ADC3SYSEN	M4ADC3SYSEN	M7ADC3SYSLPEN	M4ADC3SYSLPEN	Reserved	M7ADC3BUSEN	M4ADC3BUSEN	M7ADC3BUSLPEN	M4ADC3BUSLPEN
rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw

Bit field	Name	Description
31	M7ADC2PLLEN	ADC2PLL M7 allocation and clock enable. Set and cleared by software. 0: ADC2PLL is not allocated to M7. The "adc2_pll_div_gated_clk" is disabled in M7 RUN mode. 1: ADC2PLL is allocated to M7. The "adc2_pll_div_gated_clk" is enabled in M7 RUN mode.
30	M4ADC2PLLEN	ADC2PLL M4 allocation and clock enable. Set and cleared by software. 0: ADC2PLL is not allocated to M4. The "adc2_pll_div_gated_clk" is disabled in M4 RUN mode. 1: ADC2PLL is allocated to M4. The "adc2_pll_div_gated_clk" is enabled in M4 RUN mode.
29	M7ADC2PLLLPEN	ADC2PLL M7 Low Power clock Enable. Set and cleared by software. 0: The "adc2_pll_div_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc2_pll_div_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ADC2PLLEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4ADC2PLLLPEN	ADC2PLL M4 Low Power clock Enable. Set and cleared by software. 0: The "adc2_pll_div_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc2_pll_div_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ADC2PLLEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7ADC2SYSEN	ADC2SYS M7 allocation and clock enable. Set and cleared by software. 0: ADC2SYS is not allocated to M7. The "adc2_sys_div_gated_clk" is disabled in M7 RUN mode. 1: ADC2SYS is allocated to M7. The "adc2_sys_div_gated_clk" is enabled in M7 RUN mode.
26	M4ADC2SYSEN	ADC2SYS M4 allocation and clock enable. Set and cleared by software. 0: ADC2SYS is not allocated to M4. The "adc2_sys_div_gated_clk" is disabled in M4 RUN mode. 1: ADC2SYS is allocated to M4. The "adc2_sys_div_gated_clk" is enabled in M4 RUN mode.
25	M7ADC2SYSLPEN	ADC2SYS M7 Low Power clock Enable.

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Bit field	Name	Description
		Set and cleared by software. 0: The "adc2_sys_div_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc2_sys_div_gated_clk" clock is enabled in M7 SLEEP and STOP mode. Note : M7ADC2SYSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4ADC2SYSLPEN	ADC2SYS M4 Low Power clock Enable. Set and cleared by software. 0: The "adc2_sys_div_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc2_sys_div_gated_clk" clock is enabled in M4 SLEEP and STOP mode. Note : M4ADC2SYSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23:20	Reserved	Reserved, the reset value must be maintained.
19	M7ADC2BUSEN	ADC2BUS M7 allocation and clock enable. Set and cleared by software. 0: ADC2BUS is not allocated to M7. The "adc2_gated_hclk" is disabled in M7 RUN mode. 1: ADC2BUS is allocated to M7. The "adc2_gated_hclk" is enabled in M7 RUN mode.
18	M4ADC2BUSEN	ADC2BUS M4 allocation and clock enable. Set and cleared by software. 0: ADC2BUS is not allocated to M4. The "adc2_gated_hclk" is disabled in M4 RUN mode. 1: ADC2BUS is allocated to M4. The "adc2_gated_hclk" is enabled in M4 RUN mode.
17	M7ADC2BUSLPEN	ADC2BUS M7 Low Power clock Enable. Set and cleared by software. 0: The "adc2_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc2_gated_hclk" is enabled in M7 SLEEP mode. Note : M7ADC2BUSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4ADC2BUSLPEN	ADC2BUS M4 Low Power clock Enable. Set and cleared by software. 0: The "adc2_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ADC2BUSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7ADC3PLLEN	ADC3PLL M7 allocation and clock enable. Set and cleared by software. 0: ADC3PLL is not allocated to M7. The "adc3_pll_div_gated_clk" is disabled in M7 RUN mode. 1: ADC3PLL is allocated to M7. The "adc3_pll_div_gated_clk" is enabled in M7 RUN mode.
14	M4ADC3PLLEN	ADC3PLL M4 allocation and clock enable. Set and cleared by software. 0: ADC3PLL is not allocated to M4. The "adc3_pll_div_gated_clk" is disabled in M4 RUN mode.

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Bit field	Name	Description
		1: ADC3PLL is allocated to M4. The "adc3_pll_div_gated_clk" is enabled in M4 RUN mode.
13	M7ADC3PLLLPEN	ADC3PLL M7 Low Power clock Enable. Set and cleared by software. 0: The "adc3_pll_div_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc3_pll_div_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ADC3PLLEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4ADC3PLLLPEN	ADC3PLL M4 Low Power clock Enable. Set and cleared by software. 0: The "adc3_pll_div_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc3_pll_div_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ADC3PLLEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7ADC3SYSEN	ADC3SYS M7 allocation and clock enable. Set and cleared by software. 0: ADC3SYS is not allocated to M7. The "adc3_sys_div_gated_clk" is disabled in M7 RUN mode. 1: ADC3SYS is allocated to M7. The "adc3_sys_div_gated_clk" is enabled in M7 RUN mode.
10	M4ADC3SYSEN	ADC3SYS M4 allocation and clock enable. Set and cleared by software. 0: ADC3SYS is not allocated to M4. The "adc3_sys_div_gated_clk" is disabled in M4 RUN mode. 1: ADC3SYS is allocated to M4. The "adc3_sys_div_gated_clk" is enabled in M4 RUN mode.
9	M7ADC3SYSLPEN	ADC3SYS M7 Low Power clock Enable. Set and cleared by software. 0: The "adc3_sys_div_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc3_sys_div_gated_clk" clock is enabled in M7 SLEEP and STOP mode. Note : M7ADC3SYSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4ADC3SYSLPEN	ADC3SYS M4 Low Power clock Enable. Set and cleared by software. 0: The "adc3_sys_div_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc3_sys_div_gated_clk" clock is enabled in M4 SLEEP and STOP mode. Note : M4ADC3SYSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7:4	Reserved	Reserved, the reset value must be maintained.
3	M7ADC3BUSEN	ADC3BUS M7 allocation and clock enable. Set and cleared by software. 0: ADC3BUS is not allocated to M7. The "adc3_gated_hclk" is disabled in M7 RUN mode.

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Bit field	Name	Description
		1: ADC3BUS is allocated to M7. The "adc3_gated_hclk" is enabled in M7 RUN mode.
2	M4ADC3BUSEN	ADC3BUS M4 allocation and clock enable. Set and cleared by software. 0: ADC3BUS is not allocated to M4. The "adc3_gated_hclk" is disabled in M4 RUN mode. 1: ADC3BUS is allocated to M4. The "adc3_gated_hclk" is enabled in M4 RUN mode.
1	M7ADC3BUSLPEN	ADC3BUS M7 Low Power clock Enable. Set and cleared by software. 0: The "adc3_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "adc3_gated_hclk" is enabled in M7 SLEEP mode. Note : M7ADC3BUSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4ADC3BUSLPEN	ADC3BUS M4 Low Power clock Enable. Set and cleared by software. 0: The "adc3_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "adc3_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ADC3BUSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.25 AHB1 peripherals reset register 1(RCC_AHB1RST1)

Address offset: 0x0064

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SDMMC2RST	SDHOST2RST	Reserved					USB2WRAPRST	USB2PORRST	USB2RST	Reserved			DMAMUX1RST
		rw	rw						rw	rw	rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															ADC1RST
															rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	SDMMC2RST	SDMMC2 configuration soft reset 0: Clear reset 1: Reset SDMMC2
28	SDHOST2RST	SDHOST2 soft reset 0: Clear reset 1: Reset SDHOST2

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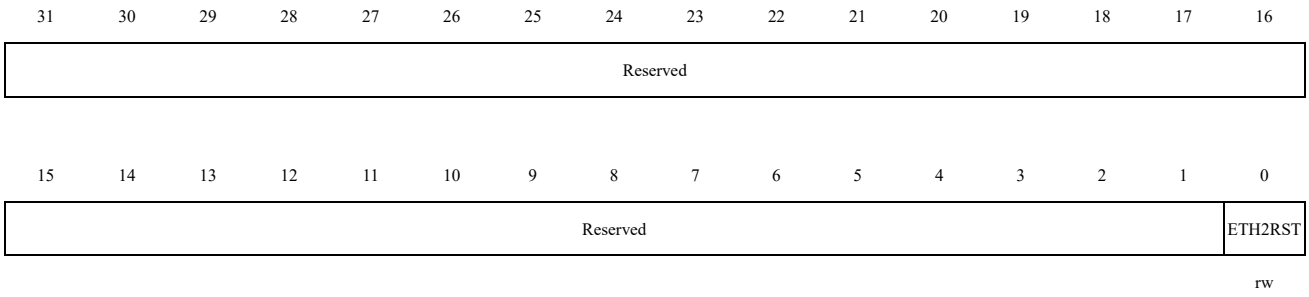
Bit field	Name	Description
27:23	Reserved	Reserved, the reset value must be maintained.
22	USB2WRAPRST	USB2 WRAPPER soft reset 0: Clear reset 1: Reset USB2 WRAPPER
21	USB2PORRST	USB2 POR soft reset 0: Clear reset 1: Reset USB2 POR
20	USB2RST	USB2 soft reset 0: Clear reset 1: Reset USB2
19:17	Reserved	Reserved, the reset value must be maintained.
16	DMAMUX1RST	DMA_MUX1 soft reset 0: Clear reset 1: Reset DMA_MUX1
15:1	Reserved	
0	ADC1RST	ADC1 soft reset 0: Clear reset 1: Reset ADC1

4.5.26 AHB1 peripherals reset register 2(RCC_AHB1RST2)

Address offset: 0x0068

Reset value: 0x00000000



Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	ETH2RST	ETH2 soft reset 0: Clear reset 1: Reset ETH2

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4.5.27 AHB1 peripherals reset register 3(RCC_AHB1RST3)

Address offset: 0x006c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							ECCMACRST	Reserved							DMA1RST
							rw								rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DMA2RST	Reserved							DMA3RST
							rw								rw

Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	ECCMACRST	ECCMON_AHBCACHE soft reset 0: Clear reset 1: Reset ECCMON_AHBCACHE
23:17	Reserved	Reserved, the reset value must be maintained.
16	DMA1RST	DMA1 soft reset 0: Clear reset 1: Reset DMA1
15:9	Reserved	Reserved, the reset value must be maintained.
8	DMA2RST	DMA2 soft reset 0: Clear reset 1: Reset DMA2
7:1	Reserved	Reserved, the reset value must be maintained.
0	DMA3RST	DMA3 soft reset 0: Clear reset 1: Reset DMA3

4.5.28 AHB1 peripherals reset register 4(RCC_AHB1RST4)

Address offset: 0x0070

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															ADC2RST
															rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															ADC3RST
															rw

Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	ADC2RST	ADC2 soft reset 0: Clear reset 1: Reset ADC2
15:1	Reserved	Reserved, the reset value must be maintained.
0	ADC3RST	ADC3 soft reset 0: Clear reset 1: Reset ADC3

4.5.29 APB1 peripherals clock divider register 1(RCC_APB1DIV1)

Address offset: 0x0074

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	APB1USARTDIV[2:0]			Reserved	APB1BTIMDIV[2:0]			Reserved					APB1GTIMDIV[2:0]		
	rw				rw								rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					APB1I2SDIV[2:0]			Reserved	APB1FDCANDIV[2:0]			Reserved	APB1I2CDIV[2:0]		
					rw				rw				rw		

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	APB1USARTDIV[2:0]	APB1 USART1 & USART2 clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
27	Reserved	Reserved, the reset value must be maintained.
26:24	APB1BTIMDIV[2:0]	APB1 Btimer clock prescalar values. 000: Divide by 1 100: Divide by 2

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Bit field	Name	Description
		101: Divide by 4 110: Divide by 8 111: Divide by 16
23:19	Reserved	Reserved, the reset value must be maintained.
18:16	APB1GTIMDIV[2:0]	APB1 Gtimer clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
15:11	Reserved	Reserved, the reset value must be maintained.
10:8	APB1I2SDIV[2:0]	APB1 I2S clock prescalar values Effective when "I2S(n)KERSEL" is selected as 2'b00. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
7	Reserved	Reserved, the reset value must be maintained.
6:4	APB1FDCANDIV[2:0]	APB1 FDCAND clock prescalar values Effective when "FDCAN(n)KERSEL" is selected as 3'b000 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
3	Reserved	Reserved, the reset value must be maintained.
2:0	APB1I2CDIV[2:0]	APB1 I2C clock prescalar values Effective when "I2C(n)KERSEL " is selected as 3'b000 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16

4.5.30 APB1 peripherals clock source select register 1(RCC_APB1SEL1)

Address offset: 0x0078

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	I2C1KERSEL[2:0]			Reserved	I2C2KERSEL[2:0]			Reserved	I2C3KERSEL[2:0]			Reserved	FDCAN1KERSEL[2:0]		
	rw				rw				rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					FDCAN2KERSEL[2:0]			Reserved				I2S4KERSEL[1:0]		I2S3KERSEL[1:0]	
					rw							rw		rw	

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	I2C1KERSEL[2:0]	I2C1 Kernel clock selection. 000: Divided system bus clock is selected as "i2c1_ker_gated_clk". 001: PLL3_C clock is selected as "i2c1_ker_gated_clk". 010: HSI clock is selected as "i2c1_ker_gated_clk". 011: MSI clock is selected as "i2c1_ker_gated_clk". Other values: setting is not allowed
27	Reserved	Reserved, the reset value must be maintained.
26:24	I2C2KERSEL[2:0]	I2C2 Kernel clock selection. 000: Divided system bus clock is selected as "i2c2_ker_gated_clk". 001: PLL3_C clock is selected as "i2c2_ker_gated_clk". 010: HSI clock is selected as "i2c2_ker_gated_clk". 011: MSI clock is selected as "i2c2_ker_gated_clk". Other values: setting is not allowed
23	Reserved	Reserved, the reset value must be maintained.
22:20	I2C3KERSEL[2:0]	I2C3 Kernel clock selection. 000: Divided system bus clock is selected as "i2c3_ker_gated_clk". 001: PLL3_C clock is selected as "i2c3_ker_gated_clk". 010: HSI clock is selected as "i2c3_ker_gated_clk". 011: MSI clock is selected as "i2c3_ker_gated_clk". Other values: setting is not allowed
19	Reserved	Reserved, the reset value must be maintained.
18:16	FDCAN1KERSEL[2:0]	FDCAN1 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan1_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan1_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan1_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan1_gated_ker_clk". 100: Peripheral clock is selected as "fdcan1_gated_ker_clk" Other values: setting is not allowed
15:11	Reserved	Reserved, the reset value must be maintained.
10:8	FDCAN2KERSEL[2:0]	FDCAN2 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan2_gated_ker_clk".

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Bit field	Name	Description
		001: PLL1_C clock is selected as "fdcan2_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan2_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan2_gated_ker_clk". 100: Peripheral clock is selected as "fdcan2_gated_ker_clk" Other values: setting is not allowed
7:4	Reserved	Reserved, the reset value must be maintained.
3:2	I2S4KERSEL[1:0]	I2S4 Kernel clock selection. 00: Divided system bus clock is selected as "i2s4_ker_gated_clk". 01: PLL3_B clock is selected as "i2s4_ker_gated_clk". 10: HSI clock is selected as "i2s4_ker_gated_clk". 11: i2s4_ckin_clk (from IOM) is selected as "i2s4_ker_gated_clk".
1:0	I2S3KERSEL[1:0]	I2S3 Kernel clock selection. 00: Divided system bus clock is selected as "i2s3_ker_gated_clk". 01: PLL3_B clock is selected as "i2s3_ker_gated_clk". 10: HSI clock is selected as "i2s3_ker_gated_clk". 11: i2s4_ckin_clk (from IOM) is selected as "i2s3_ker_gated_clk".

4.5.31 APB1 peripherals clock source select register 2(RCC_APB1SEL2)

Address offset: 0x007c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	FDCAN5KERSEL[2:0]			Reserved					FDCAN6KERSEL[2:0]			Reserved			
	rw									rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	FDCAN5KERSEL[2:0]	FDCAN5 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan5_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan5_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan5_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan5_gated_ker_clk". 100: Peripheral clock is selected as "fdcan5_gated_ker_clk" Other values: setting is not allowed

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Bit field	Name	Description
27:21	Reserved	Reserved, the reset value must be maintained.
22:20	FDCAN6KERSEL[2:0]	FDCAN6 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan6_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan6_gated_ker_clk". Other values: setting is not allowed 010: PLL2_C clock is selected as "fdcan6_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan6_gated_ker_clk". 100: Peripheral clock is selected as "fdcan6_gated_ker_clk" Other values: setting is not allowed
19:0	Reserved	Reserved, the reset value must be maintained.

4.5.32 APB1 peripherals clock enable register 1(RCC_APB1EN1)

Address offset: 0x0080

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7BTIM1EN	M4BTIM1EN	M7BTIM1LPEN	M4BTIM1LPEN	M7BTIM2EN	M4BTIM2EN	M7BTIM2LPEN	M4BTIM2LPEN	M7BTIM3EN	M4BTIM3EN	M7BTIM3LPEN	M4BTIM3LPEN	M7BTIM4EN	M4BTIM4EN	M7BTIM4LPEN	M4BTIM4LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7GTIMB1EN	M4GTIMB1EN	M7GTIMB1LPEN	M4GTIMB1LPEN	M7GTIMB2EN	M4GTIMB2EN	M7GTIMB2LPEN	M4GTIMB2LPEN	M7GTIMB3EN	M4GTIMB3EN	M7GTIMB3LPEN	M4GTIMB3LPEN	M7GTIMA4EN	M4GTIMA4EN	M7GTIMA4LPEN	M4GTIMA4LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7BTIM1EN	BTIMER1 M7 allocation and clock enable. Set and cleared by software. 0: BTIMER1 is not allocated to M7. The "btimer1_gated_ker_clk" and "btimer1_gated_pclk" are disabled in M7 RUN mode. 1: BTIMER1 is allocated to M7. The "btimer1_gated_ker_clk" and "btimer1_gated_pclk" are enabled in M7 RUN mode.
30	M4BTIM1EN	BTIMER1 M4 allocation and clock enable. Set and cleared by software. 0: BTIMER1 is not allocated to M4. The "btimer1_gated_ker_clk" and "btimer1_gated_pclk" are disabled in M4 RUN mode. 1: BTIMER1 is allocated to M4. The "btimer1_gated_ker_clk" and "btimer1_gated_pclk" are enabled in M4 RUN mode.
29	M7BTIM1LPEN	BTIMER1 M7 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "btimer1_gated_ker_clk" and "btimer1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "btimer1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "btimer1_gated_pclk" is enabled in M7 SLEEP mode. Note: M7BTIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4BTIM1LPEN	BTIMER1 M4 Low Power clock Enable. Set and cleared by software. 0: The "btimer1_gated_ker_clk" and "btimer1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "btimer1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "btimer1_gated_pclk" is enabled in M4 SEEP mode. Note: M4BTIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7BTIM2EN	BTIMER2 M7 allocation and clock enable. Set and cleared by software. 0: BTIMER2 is not allocated to M7. The "btimer2_gated_ker_clk" and "btimer2_gated_pclk" are disabled in M7 RUN mode. 1: BTIMER2 is allocated to M7. The "btimer2_gated_ker_clk" and "btimer2_gated_pclk" are enabled in M7 RUN mode.
26	M4BTIM2EN	BTIMER2 M4 allocation and clock enable. Set and cleared by software. 0: BTIMER2 is not allocated to M4. The "btimer2_gated_ker_clk" and "btimer2_gated_pclk" are disabled in M4 RUN mode. 1: BTIMER2 is allocated to M4. The "btimer2_gated_ker_clk" and "btimer2_gated_pclk" are enabled in M4 RUN mode.
25	M7BTIM2LPEN	BTIMER2 M7 Low Power clock Enable. Set and cleared by software. 0: The "btimer2_gated_ker_clk" and "btimer2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "btimer2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "btimer2_gated_pclk" is enabled in M7 SLEEP mode. Note: M7BTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4BTIM2LPEN	BTIMER2 M4 Low Power clock Enable. Set and cleared by software. 0: The "btimer2_gated_ker_clk" and "btimer2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "btimer2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "btimer2_gated_pclk" is enabled in M4 SEEP mode. Note: M4BTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Bit field	Name	Description
23	M7BTIM3EN	BTIMER3 M7 allocation and clock enable. Set and cleared by software. 0: BTIMER3 is not allocated to M7. The "btimer3_gated_ker_clk" and "btimer3_gated_pclk" are disabled in M7 RUN mode. 1: BTIMER3 is allocated to M7. The "btimer3_gated_ker_clk" and "btimer3_gated_pclk" are enabled in M7 RUN mode.
22	M4BTIM3EN	BTIMER3 M4 allocation and clock enable. Set and cleared by software. 0: BTIMER3 is not allocated to M4. The "btimer3_gated_ker_clk" and "btimer3_gated_pclk" are disabled in M4 RUN mode. 1: BTIMER3 is allocated to M4. The "btimer3_gated_ker_clk" and "btimer3_gated_pclk" are enabled in M4 RUN mode.
21	M7BTIM3LPEN	BTIMER3 M7 Low Power clock Enable. Set and cleared by software. 0: The "btimer3_gated_ker_clk" and "btimer3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "btimer3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "btimer3_gated_pclk" is enabled in M7 SLEEP mode. Note: M7BTIM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4BTIM3LPEN	BTIMER3 M4 Low Power clock Enable. Set and cleared by software. 0: The "btimer3_gated_ker_clk" and "btimer3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "btimer3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "btimer3_gated_pclk" is enabled in M4 SEEP mode. Note: M4BTIM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7BTIM4EN	BTIMER4 M7 allocation and clock enable. Set and cleared by software. 0: BTIMER4 is not allocated to M7. The "btimer4_gated_ker_clk" and "btimer4_gated_pclk" are disabled in M7 RUN mode. 1: BTIMER4 is allocated to M7. The "btimer4_gated_ker_clk" and "btimer4_gated_pclk" are enabled in M7 RUN mode.
18	M4BTIM4EN	BTIMER4 M4 allocation and clock enable. Set and cleared by software. 0: BTIMER4 is not allocated to M4. The "btimer4_gated_ker_clk" and "btimer4_gated_pclk" are disabled in M4 RUN mode. 1: BTIMER4 is allocated to M4. The "btimer4_gated_ker_clk" and "btimer4_gated_pclk" are enabled in M4 RUN mode.
17	M7BTIM4LPEN	BTIMER4 M7 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "btimer4_gated_ker_clk" and "btimer4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "btimer4_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "btimer4_gated_pclk" is enabled in M7 SLEEP mode. Note: M7BTIM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4BTIM4LPEN	BTIMER4 M4 Low Power clock Enable. Set and cleared by software. 0: The "btimer4_gated_ker_clk" and "btimer4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "btimer4_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "btimer4_gated_pclk" is enabled in M4 SEEP mode. Note: M4BTIM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7GTIMB1EN	GTIMERB1 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERB1 is not allocated to M7. The "gtimerb1_gated_ker_clk" and "gtimerb1_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERB1 is allocated to M7. The "gtimerb1_gated_ker_clk" and "gtimerb1_gated_pclk" are enabled in M7 RUN mode.
14	M4GTIMB1EN	GTIMERB1 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERB1 is not allocated to M4. The "gtimerb1_gated_ker_clk" and "gtimerb1_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERB1 is allocated to M4. The "gtimerb1_gated_ker_clk" and "gtimerb1_gated_pclk" are enabled in M4 RUN mode.
13	M7GTIMB1LPEN	GTIMERB1 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimerb1_gated_ker_clk" and "gtimerb1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimerb1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimerb1_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMB1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4GTIMB1LPEN	GTIMERB1 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimerb1_gated_ker_clk" and "gtimerb1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimerb1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimerb1_gated_pclk" is enabled in M4 SEEP mode. Note: M4GTIMB1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Bit field	Name	Description
11	M7GTIMB2EN	GTIMERB2 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERB2 is not allocated to M7. The "gtimerb2_gated_ker_clk" and "gtimerb2_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERB2 is allocated to M7. The "gtimerb2_gated_ker_clk" and "gtimerb2_gated_pclk" are enabled in M7 RUN mode.
10	M4GTIMB2EN	GTIMERB2 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERB2 is not allocated to M4. The "gtimerb2_gated_ker_clk" and "gtimerb2_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERB2 is allocated to M4. The "gtimerb2_gated_ker_clk" and "gtimerb2_gated_pclk" are enabled in M4 RUN mode.
9	M7GTIMB2LPEN	GTIMERB2 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimerb2_gated_ker_clk" and "gtimerb2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimerb2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimerb2_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMB2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4GTIMB2LPEN	GTIMERB2 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimerb2_gated_ker_clk" and "gtimerb2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimerb2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimerb2_gated_pclk" is enabled in M4 SEEP mode. Note: M4GTIMB2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7GTIMB3EN	GTIMERB3 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERB3 is not allocated to M7. The "gtimerb3_gated_ker_clk" and "gtimerb3_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERB3 is allocated to M7. The "gtimerb3_gated_ker_clk" and "gtimerb3_gated_pclk" are enabled in M7 RUN mode.
6	M4GTIMB3EN	GTIMERB3 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERB3 is not allocated to M4. The "gtimerb3_gated_ker_clk" and "gtimerb3_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERB3 is allocated to M4. The "gtimerb3_gated_ker_clk" and "gtimerb3_gated_pclk" are enabled in M4 RUN mode.
5	M7GTIMB3LPEN	GTIMERB3 M7 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "gtimerb3_gated_ker_clk" and "gtimerb3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimerb3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimerb3_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMB3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4GTIMB3LPEN	GTIMERB3 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimerb3_gated_ker_clk" and "gtimerb3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimerb3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimerb3_gated_pclk" is enabled in M4 SEEP mode. Note: M4GTIMB3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7GTIMA4EN	GTIMERA4 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA4 is not allocated to M7. The "gtimera4_gated_ker_clk" and "gtimera4_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA4 is allocated to M7. The "gtimera4_gated_ker_clk" and "gtimera4_gated_pclk" are enabled in M7 RUN mode.
2	M4GTIMA4EN	GTIMERA4 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA4 is not allocated to M4. The "gtimera4_gated_ker_clk" and "gtimera4_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA4 is allocated to M4. The "gtimera4_gated_ker_clk" and "gtimera4_gated_pclk" are enabled in M4 RUN mode.
1	M7GTIMA4LPEN	GTIMERA4 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera4_gated_ker_clk" and "gtimera4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera4_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera4_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMA4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4GTIMA4LPEN	GTIMERA4 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera4_gated_ker_clk" and "gtimera4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera4_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera4_gated_pclk" is enabled in M4 SEEP mode. Note: M4GTIMA4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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4.5.33 APB1 peripherals clock enable register 2(RCC_APB1EN2)

Address offset: 0x0084

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7GTIMA5EN	M4GTIMA5EN	M7GTIMA5LPEN	M4GTIMA5LPEN	M7GTIMA6EN	M4GTIMA6EN	M7GTIMA6LPEN	M4GTIMA6LPEN	M7GTIMA7EN	M4GTIMA7EN	M7GTIMA7LPEN	M4GTIMA7LPEN	M7SPI3EN	M4SPI3EN	M7SPI3LPEN	M4SPI3LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7DAC12EN	M4DAC12EN	M7DAC12LPEN	M4DAC12LPEN	Reserved				M7WWDG2EN	M4WWDG2EN	M7WWDG2LPEN	M4WWDG2LPEN	Reserved			
rw	rw	rw	rw					rw	rw	rw	rw				

Bit field	Name	Description
31	M7GTIMA5EN	GTIMERA5 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA5 is not allocated to M7. The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA5 is allocated to M7. The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" are enabled in M7 RUN mode.
30	M4GTIMA5EN	GTIMERA5 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA5 is not allocated to M4. The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA5 is allocated to M4. The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" are enabled in M4 RUN mode.
29	M7GTIMA5LPEN	GTIMERA5 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera5_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera5_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMA5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4GTIMA5LPEN	GTIMERA5 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera5_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera5_gated_pclk" is enabled in M4 SEEP mode.

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Bit field	Name	Description
		Note: M4GTIMA5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7GTIMA6EN	GTIMERA5 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA5 is not allocated to M7. The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA5 is allocated to M7. The "gtimera5_gated_ker_clk" and "gtimera5_gated_pclk" are enabled in M7 RUN mode.
26	M4GTIMA6EN	GTIMERA6 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA6 is not allocated to M4. The "gtimera6_gated_ker_clk" and "gtimera6_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA6 is allocated to M4. The "gtimera6_gated_ker_clk" and "gtimera6_gated_pclk" are enabled in M4 RUN mode.
25	M7GTIMA6LPEN	GTIMERA6 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera6_gated_ker_clk" and "gtimera6_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera6_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera6_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMA6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4GTIMA6LPEN	GTIMERA6 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera6_gated_ker_clk" and "gtimera6_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera6_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera6_gated_pclk" is enabled in M4 SEEP mode. Note: M4GTIMA6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7GTIMA7EN	GTIMERA7 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA7 is not allocated to M7. The "gtimera7_gated_ker_clk" and "gtimera7_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA7 is allocated to M7. The "gtimera7_gated_ker_clk" and "gtimera7_gated_pclk" are enabled in M7 RUN mode.
22	M4GTIMA7EN	GTIMERA7 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA7 is not allocated to M4. The "gtimera7_gated_ker_clk" and "gtimera7_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA7 is allocated to M4. The "gtimera7_gated_ker_clk" and "gtimera7_gated_pclk" are enabled in M4 RUN mode.

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Bit field	Name	Description
21	M7GTIMA7LPEN	GTIMERA7 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera7_gated_ker_clk" and "gtimera7_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera7_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera7_gated_pclk" is enabled in M7 SLEEP mode. Note: M7GTIMA7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4GTIMA7LPEN	GTIMERA7 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera7_gated_ker_clk" and "gtimera7_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera7_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera7_gated_pclk" is enabled in M4 SEEP mode. Note: M4GTIMA7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7SPI3EN	SPI3 M7 allocation and clock enable. Set and cleared by software. 0: SPI3 is not allocated to M7. The " spi3_gated_ker_clk" and "spi3_gated_pclk" are disabled in M7 RUN mode. 1: SPI3 is allocated to M7. The " spi3_gated_ker_clk" and "spi3_gated_pclk" are enabled in M7 RUN mode.
18	M4SPI3EN	SPI3 M4 allocation and clock enable. Set and cleared by software. 0: SPI3 is not allocated to M4. The " spi3_gated_ker_clk" and "spi3_gated_pclk" are disabled in M4 RUN mode. 1: SPI3 is allocated to M4. The " spi3_gated_ker_clk" and "spi3_gated_pclk" are enabled in M4 RUN mode.
17	M7SPI3LPEN	SPI3 M7 Low Power clock Enable. Set and cleared by software. 0: The " spi3_gated_ker_clk" and "spi3_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4SPI3LPEN	SPI3 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi3_gated_ker_clk" and "spi3_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi3_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4SPI3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7DAC12EN	DAC12 M7 allocation and clock enable. Set and cleared by software. 0: DAC12 is not allocated to M7. The "dac12_gated_pclk" is disabled in M7 RUN mode. 1: DAC12 is allocated to M7. The "dac12_gated_pclk" is enabled in M7 RUN mode.
14	M4DAC12EN	DAC12 M4 allocation and clock enable. Set and cleared by software. 0: DAC12 is not allocated to M4. The "dac12_gated_pclk" is disabled in M4 RUN mode. 1: DAC12 is allocated to M4. The "dac12_gated_pclk" is enabled in M4 RUN mode.
13	M7DAC12LPEN	DAC12 M7 Low Power clock Enable. Set and cleared by software. 0: The "dac12_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "dac12_gated_pclk" is enabled in M7 SLEEP mode. Note : M7DAC12EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4DAC12LPEN	DAC12 M4 Low Power clock Enable. Set and cleared by software. 0: The "dac12_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "dac12_gated_pclk" is enabled in M4 SLEEP mode. Note : M4DAC12EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11:8	Reserved	Reserved, the reset value must be maintained.
7	M7WWDG2EN	WWDG2 M7 allocation and clock enable. Set and cleared by software. 0: WWDG2 is not allocated to M7. The "wwdg2_gated_pclk" is disabled in M7 RUN mode. 1: WWDG2 is allocated to M7. The "wwdg2_gated_pclk" is enabled in M7 RUN mode.
6	M4WWDG2EN	WWDG2 M4 allocation and clock enable. Set and cleared by software. 0: WWDG2 is not allocated to M4. The "wwdg2_gated_pclk" is disabled in M4 RUN mode. 1: WWDG2 is allocated to M4. The "wwdg2_gated_pclk" is enabled in M4 RUN mode.
5	M7WWDG2LPEN	WWDG2 M7 Low Power clock Enable. Set and cleared by software. 0: The "wwdg2_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "wwdg2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7WWDG2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4WWDG2LPEN	WWDG2 M4 Low Power clock Enable. Set and cleared by software. 0: The "wwdg2_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "wwdg2_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4WWDG2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.34 APB1 peripherals clock enable register 3(RCC_APB1EN3)

Address offset: 0x0088

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7USART1EN	M4USART1EN	M7USART1LPEN	M4USART1LPEN	M7USART2EN	M4USART2EN	M7USART2LPEN	M4USART2LPEN	M7USART3EN	M4USART3EN	M7USART3LPEN	M4USART3LPEN	M7USART4EN	M4USART4EN	M7USART4LPEN	M4USART4LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7UART9EN	M4UART9EN	M7UART9LPEN	M4UART9LPEN	M7UART10EN	M4UART10EN	M7UART10LPEN	M4UART10LPEN	M7UART11EN	M4UART11EN	M7UART11LPEN	M4UART11LPEN	M7UART12EN	M4UART12EN	M7UART12LPEN	M4UART12LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7USART1EN	USART1 M7 allocation and clock enable. Set and cleared by software. 0: USART1 is not allocated to M7. The "usart1_gated_pclk" is disabled in M7 RUN mode. 1: USART1 is allocated to M7. The "usart1_gated_pclk" is enabled in M7 RUN mode.
30	M4USART1EN	USART1 M4 allocation and clock enable. Set and cleared by software. 0: USART1 is not allocated to M4. The "usart1_gated_pclk" is disabled in M4 RUN mode. 1: USART1 is allocated to M4. The "usart1_gated_pclk" is enabled in M4 RUN mode.
29	M7USART1LPEN	USART1 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart1_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4USART1LPEN	USART1 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart1_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7USART2EN	USART2 M7 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: USART2 is not allocated to M7. The "usart2_gated_pclk" is disabled in M7 RUN mode. 1: USART2 is allocated to M7. The "usart2_gated_pclk" is enabled in M7 RUN mode.
26	M4USART2EN	USART2 M4 allocation and clock enable. Set and cleared by software. 0: USART2 is not allocated to M4. The "usart2_gated_pclk" is disabled in M4 RUN mode. 1: USART2 is allocated to M4. The "usart2_gated_pclk" is enabled in M4 RUN mode.
25	M7USART2LPEN	USART2 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart2_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4USART2LPEN	USART2 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart2_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7USART3EN	USART3 M7 allocation and clock enable. Set and cleared by software. 0: USART3 is not allocated to M7. The "usart3_gated_pclk" is disabled in M7 RUN mode. 1: USART3 is allocated to M7. The "usart3_gated_pclk" is enabled in M7 RUN mode.
22	M4USART3EN	USART3 M4 allocation and clock enable. Set and cleared by software. 0: USART3 is not allocated to M4. The "usart3_gated_pclk" is disabled in M4 RUN mode. 1: USART3 is allocated to M4. The "usart3_gated_pclk" is enabled in M4 RUN mode.
21	M7USART3LPEN	USART3 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart3_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4USART3LPEN	USART3 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart3_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7USART4EN	USART4 M7 allocation and clock enable. Set and cleared by software. 0: USART4 is not allocated to M7. The "usart4_gated_pclk" is disabled in M7 RUN mode.

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Bit field	Name	Description
		1: USART4 is allocated to M7. The "usart4_gated_pclk" is enabled in M7 RUN mode.
18	M4USART4EN	USART4 M4 allocation and clock enable. Set and cleared by software. 0: USART4 is not allocated to M4. The "usart4_gated_pclk" is disabled in M4 RUN mode. 1: USART4 is allocated to M4. The "usart4_gated_pclk" is enabled in M4 RUN mode.
17	M7USART4LPEN	USART4 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart4_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4USART4LPEN	USART4 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart4_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart4_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7UART9EN	UART9 M7 allocation and clock enable. Set and cleared by software. 0: UART9 is not allocated to M7. The "uart9_gated_pclk" is disabled in M7 RUN mode. 1: UART9 is allocated to M7. The "uart9_gated_pclk" is enabled in M7 RUN mode.
14	M4UART9EN	UART9 M4 allocation and clock enable. Set and cleared by software. 0: UART9 is not allocated to M4. The "uart9_gated_pclk" is disabled in M4 RUN mode. 1: UART9 is allocated to M4. The "uart9_gated_pclk" is enabled in M4 RUN mode.
13	M7UART9LPEN	UART9 M7 Low Power clock Enable. Set and cleared by software. 0: The "uart9_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart9_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART9EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4UART9LPEN	UART9 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart9_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart9_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART9EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7UART10EN	UART10 M7 allocation and clock enable. Set and cleared by software. 0: UART10 is not allocated to M7. The "uart10_gated_pclk" is disabled in M7 RUN mode. 1: UART10 is allocated to M7. The "uart10_gated_pclk" is enabled in M7 RUN mode.
10	M4UART10EN	UART10 M4 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: UART10 is not allocated to M4. The "uart10_gated_pclk" is disabled in M4 RUN mode. 1: UART10 is allocated to M4. The "uart10_gated_pclk" is enabled in M4 RUN mode.
9	M7UART10LPEN	UART10 M7 Low Power clock Enable. Set and cleared by software. 0: The "uart10_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart10_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART10EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4UART10LPEN	UART10 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart10_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart10_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART10EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7UART11EN	UART11 M7 allocation and clock enable. Set and cleared by software. 0: UART11 is not allocated to M7. The "uart11_gated_pclk" is disabled in M7 RUN mode. 1: UART11 is allocated to M7. The "uart11_gated_pclk" is enabled in M7 RUN mode.
6	M4UART11EN	UART11 M4 allocation and clock enable. Set and cleared by software. 0: UART11 is not allocated to M4. The "uart11_gated_pclk" is disabled in M4 RUN mode. 1: UART11 is allocated to M4. The "uart11_gated_pclk" is enabled in M4 RUN mode.
5	M7UART11LPEN	UART11 M7 Low Power clock Enable. Set and cleared by software. 0: The "uart11_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart11_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART11EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4UART11LPEN	UART11 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart11_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart11_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART11EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7UART12EN	UART12 M7 allocation and clock enable. Set and cleared by software. 0: UART12 is not allocated to M7. The "uart12_gated_pclk" is disabled in M7 RUN mode. 1: UART12 is allocated to M7. The "uart12_gated_pclk" is enabled in M7 RUN mode.
2	M4UART12EN	UART12 M4 allocation and clock enable. Set and cleared by software. 0: UART12 is not allocated to M4. The "uart12_gated_pclk" is disabled in M4 RUN mode.

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Bit field	Name	Description
		1: UART12 is allocated to M4. The "uart12_gated_pclk" is enabled in M4 RUN mode.
1	M7UART12LPEN	UART12 M7 Low Power clock Enable. Set and cleared by software. 0: The "uart12_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart12_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART12EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4UART12LPEN	UART12 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart12_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart12_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART12EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.35 APB1 peripherals clock enable register 4(RCC_APB1EN4)

Address offset: 0x008c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7I2S3EN	M4I2S3EN	M7I2S3LPEN	M4I2S3LPEN	M7I2S4EN	M4I2S4EN	M7I2S4LPEN	M4I2S4LPEN	M7I2C1EN	M4I2C1EN	M7I2C1LPEN	M4I2C1LPEN	M7I2C2EN	M4I2C2EN	M7I2C2LPEN	M4I2C2LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7I2C3EN	M4I2C3EN	M7I2C3LPEN	M4I2C3LPEN	Reserved											
rw	rw	rw	rw												

Bit field	Name	Description
31	M7I2S3EN	I2S3 M7 allocation and clock enable. Set and cleared by software. 0: I2S3 is not allocated to M7. The "i2s3_ker_gated_clk" and "i2s3_gated_pclk" are disabled in M7 RUN mode. 1: I2S3 is allocated to M7. The "i2s3_ker_gated_clk" and "i2s3_gated_pclk" are enabled in M7 RUN mode.
30	M4I2S3EN	I2S3 M4 allocation and clock enable. Set and cleared by software. 0: I2S3 is not allocated to M4. The "i2s3_ker_gated_clk" and "i2s3_gated_pclk" are disabled in M4 RUN mode.

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Bit field	Name	Description
		1: I2S3 is allocated to M4. The "i2s3_ker_gated_clk" and "i2s3_gated_pclk" are enabled in M4 RUN mode.
29	M7I2S3LPEN	I2S3 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2s3_ker_gated_clk" and "i2s3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2s3_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2s3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2S3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4I2S3LPEN	I2S3 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2s3_ker_gated_clk" and "i2s3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2s3_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2s3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2S3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7I2S4EN	I2S4 M7 allocation and clock enable. Set and cleared by software. 0: I2S4 is not allocated to M7. The "i2s4_ker_gated_clk" and "i2s4_gated_pclk" are disabled in M7 RUN mode. 1: I2S4 is allocated to M7. The "i2s4_ker_gated_clk" and "i2s4_gated_pclk" are enabled in M7 RUN mode.
26	M4I2S4EN	I2S4 M4 allocation and clock enable. Set and cleared by software. 0: I2S4 is not allocated to M4. The "i2s4_ker_gated_clk" and "i2s4_gated_pclk" are disabled in M4 RUN mode. 1: I2S4 is allocated to M4. The "i2s4_ker_gated_clk" and "i2s4_gated_pclk" are enabled in M4 RUN mode.
25	M7I2S4LPEN	I2S4 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2s4_ker_gated_clk" and "i2s4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2s4_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2s4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2S4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4I2S4LPEN	I2S4 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2s4_ker_gated_clk" and "i2s4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode.

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Bit field	Name	Description
		1: The "i2s4_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2s4_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2S4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7I2C1EN	I2C1 M7 allocation and clock enable. Set and cleared by software. 0: I2C1 is not allocated to M7. The "i2c1_ker_gated_clk" and "i2c1_gated_pclk" are disabled in M7 RUN mode. 1: I2C1 is allocated to M7. The "i2c1_ker_gated_clk" and "i2c1_gated_pclk" are enabled in M7 RUN mode.
22	M4I2C1EN	I2C1 M4 allocation and clock enable. Set and cleared by software. 0: I2C1 is not allocated to M4. The "i2c1_ker_gated_clk" and "i2c1_gated_pclk" are disabled in M4 RUN mode. 1: I2C1 is allocated to M4. The "i2c1_ker_gated_clk" and "i2c1_gated_pclk" are enabled in M4 RUN mode.
21	M7I2C1LPEN	I2C1 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c1_ker_gated_clk" and "i2c1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c1_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4I2C1LPEN	I2C1 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c1_ker_gated_clk" and "i2c1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c1_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7I2C2EN	I2C2 M7 allocation and clock enable. Set and cleared by software. 0: I2C2 is not allocated to M7. The "i2c2_ker_gated_clk" and "i2c2_gated_pclk" are disabled in M7 RUN mode. 1: I2C2 is allocated to M7. The "i2c2_ker_gated_clk" and "i2c2_gated_pclk" are enabled in M7 RUN mode.
18	M4I2C2EN	I2C2 M4 allocation and clock enable. Set and cleared by software. 0: I2C2 is not allocated to M4. The "i2c2_ker_gated_clk" and "i2c2_gated_pclk" are disabled in M4 RUN mode.

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Bit field	Name	Description
		1: I2C2 is allocated to M4. The "i2c2_ker_gated_clk" and "i2c2_gated_pclk" are enabled in M4 RUN mode.
17	M7I2C2LPEN	I2C2 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c2_ker_gated_clk" and "i2c2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c2_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4I2C2LPEN	I2C2 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c2_ker_gated_clk" and "i2c2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c2_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7I2C3EN	I2C3 M7 allocation and clock enable. Set and cleared by software. 0: I2C3 is not allocated to M7. The "i2c3_ker_gated_clk" and "i2c3_gated_pclk" are disabled in M7 RUN mode. 1: I2C3 is allocated to M7. The "i2c3_ker_gated_clk" and "i2c3_gated_pclk" are enabled in M7 RUN mode.
14	M4I2C3EN	I2C3 M4 allocation and clock enable. Set and cleared by software. 0: I2C3 is not allocated to M4. The "i2c3_ker_gated_clk" and "i2c3_gated_pclk" are disabled in M4 RUN mode. 1: I2C3 is allocated to M4. The "i2c3_ker_gated_clk" and "i2c3_gated_pclk" are enabled in M4 RUN mode.
13	M7I2C3LPEN	I2C3 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c3_ker_gated_clk" and "i2c3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c3_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4I2C3LPEN	I2C3 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c3_ker_gated_clk" and "i2c3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode.

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Bit field	Name	Description
		1: The "i2c3_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11:0	Reserved	Reserved, the reset value must be maintained.

4.5.36 APB1 peripherals clock enable register 5(RCC_APB1EN5)

Address offset: 0x0090

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7FDCAN1EN	M4FDCAN1EN	M7FDCAN1LPEN	M4FDCAN1LPEN	M7FDCAN2EN	M4FDCAN2EN	M7FDCAN2LPEN	M4FDCAN2LPEN	M7FDCAN5EN	M4FDCAN5EN	M7FDCAN5LPEN	M4FDCAN5LPEN	M7FDCAN6EN	M4FDCAN6EN	M7FDCAN6LPEN	M4FDCAN6LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDCAN1STPREQ	FDCAN1STPACK	Reserved		FDCAN2STPREQ	FDCAN2STPACK	Reserved		FDCAN5STPREQ	FDCAN5STPACK	Reserved		FDCAN6STPREQ	FDCAN6STPACK	Reserved	
rw	r			rw	r			rw	r			rw	r		

Bit field	Name	Description
31	M7FDCAN1EN	FDCAN1 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN1 is not allocated to M7. The "fdcan1_gated_ker_clk" and "fdcan1_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN1 is allocated to M7. The "fdcan1_gated_ker_clk" and "fdcan1_gated_pclk" are enabled in M7 RUN mode.
30	M4FDCAN1EN	FDCAN1 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN1 is not allocated to M4. The "fdcan1_gated_ker_clk" and "fdcan1_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN1 is allocated to M4. The "fdcan1_gated_ker_clk" and "fdcan1_gated_pclk" are enabled in M4 RUN mode.
29	M7FDCAN1LPEN	FDCAN1 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan1_gated_ker_clk" and "fdcan1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan1_gated_pclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7FDCAN1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4FDCAN1LPEN	FDCAN1 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan1_gated_ker_clk" and "fdcan1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7FDCAN2EN	FDCAN2 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN2 is not allocated to M7. The "fdcan2_gated_ker_clk" and "fdcan2_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN2 is allocated to M7. The "fdcan2_gated_ker_clk" and "fdcan2_gated_pclk" are enabled in M7 RUN mode.
26	M4FDCAN2EN	FDCAN2 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN2 is not allocated to M4. The "fdcan2_gated_ker_clk" and "fdcan2_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN2 is allocated to M4. The "fdcan2_gated_ker_clk" and "fdcan2_gated_pclk" are enabled in M4 RUN mode.
25	M7FDCAN2LPEN	FDCAN2 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan2_gated_ker_clk" and "fdcan2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7FDCAN2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4FDCAN2LPEN	FDCAN2 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan2_gated_ker_clk" and "fdcan2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7FDCAN5EN	FDCAN5 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN5 is not allocated to M7. The "fdcan5_gated_ker_clk" and "fdcan5_gated_pclk" are disabled in M7 RUN mode.

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Bit field	Name	Description
		1: FDCAN5 is allocated to M7. The "fdcan5_gated_ker_clk" and "fdcan5_gated_pclk" are enabled in M7 RUN mode.
22	M4FDCAN5EN	FDCAN5 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN5 is not allocated to M4. The "fdcan5_gated_ker_clk" and "fdcan5_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN5 is allocated to M4. The "fdcan5_gated_ker_clk" and "fdcan5_gated_pclk" are enabled in M4 RUN mode.
21	M7FDCAN5LPEN	FDCAN5 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan5_gated_ker_clk" and "fdcan5_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan5_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan5_gated_pclk" is enabled in M7 SLEEP mode. Note : M7FDCAN5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4FDCAN5LPEN	FDCAN5 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan5_gated_ker_clk" and "fdcan5_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan5_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan5_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7FDCAN6EN	FDCAN6 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN6 is not allocated to M7. The "fdcan6_gated_ker_clk" and "fdcan6_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN6 is allocated to M7. The "fdcan6_gated_ker_clk" and "fdcan6_gated_pclk" are enabled in M7 RUN mode.
18	M4FDCAN6EN	FDCAN6 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN6 is not allocated to M4. The "fdcan6_gated_ker_clk" and "fdcan6_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN6 is allocated to M4. The "fdcan6_gated_ker_clk" and "fdcan6_gated_pclk" are enabled in M4 RUN mode.
17	M7FDCAN6LPEN	FDCAN6 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan6_gated_ker_clk" and "fdcan6_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan6_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan6_gated_pclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7FDCAN6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4FDCAN6LPEN	FDCAN6 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan6_gated_ker_clk" and "fdcan6_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan6_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan6_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	FDCAN1STPREQ	FDCAN1 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
14	FDCAN1STPACK	FDCAN1 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
13:12	Reserved	Reserved, the reset value must be maintained.
11	FDCAN2STPREQ	FDCAN2 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
10	FDCAN2STPACK	FDCAN2 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
9:8	Reserved	Reserved, the reset value must be maintained.
7	FDCAN5STPREQ	FDCAN5 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
6	FDCAN5STPACK	FDCAN5 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
5:4	Reserved	Reserved, the reset value must be maintained.
3	FDCAN6STPREQ	FDCAN6 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
2	FDCAN6STPACK	FDCAN6 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.

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4.5.37 APB1 peripherals reset register 1(RCC_APB1RST1)

Address offset: 0x0094

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			BTIM1RST	Reserved			BTIM2RST	Reserved			BTIM3RST	Reserved			BTIM4RST
			rw				rw				rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			GTIMB1RST	Reserved			GTIMB2RST	Reserved			GTIMB3RST	Reserved			GTIMA4RST
			rw				rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	BTIM1RST	BTIMER1 soft reset 0: Clear reset 1: Reset BTIMER1
27:25	Reserved	Reserved, the reset value must be maintained.
24	BTIM2RST	BTIMER2 soft reset 0: Clear reset 1: Reset BTIMER2
23:21	Reserved	Reserved, the reset value must be maintained.
20	BTIM3RST	BTIMER3 soft reset 0: Clear reset 1: Reset BTIMER3
19:17	Reserved	Reserved, the reset value must be maintained.
16	BTIM4RST	BTIMER4 soft reset 0: Clear reset 1: Reset BTIMER4
15:13	Reserved	Reserved, the reset value must be maintained.
12	GTIMB1RST	GTIMERB1 soft reset 0: Clear reset 1: Reset GTIMERB1
11:9	Reserved	Reserved, the reset value must be maintained.
8	GTIMB2RST	GTIMERB2 soft reset 0: Clear reset 1: Reset GTIMERB2
7:5	Reserved	Reserved, the reset value must be maintained.
4	GTIMB3RST	GTIMERB3 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset GTIMERB3
3:1	Reserved	Reserved, the reset value must be maintained.
0	GTIMA4RST	GTIMERA4 soft reset 0: Clear reset 1: Reset GTIMERA4

4.5.38 APB1 peripherals reset register 2(RCC_APB1RST2)

Address offset: 0x0098

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			GTIMA5RST	Reserved			GTIMA6RST	Reserved			GTIMA7RST	Reserved			SPI3RST
			rw				rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			DAC12RST	Reserved							WWDG2RST	Reserved			
			rw								rw				

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	GTIMA5RST	GTIMERA5 soft reset 0: Clear reset 1: Reset GTIMERA5
27:25	Reserved	Reserved, the reset value must be maintained.
24	GTIMA6RST	GTIMERA6 soft reset 0: Clear reset 1: Reset GTIMERA6
23:21	Reserved	Reserved, the reset value must be maintained.
20	GTIMA7RST	GTIMERA7 soft reset 0: Clear reset 1: Reset GTIMERA7
19:17	Reserved	Reserved, the reset value must be maintained.
16	SPI3RST	SPI3 soft reset 0: Clear reset 1: Reset SPI3
15:13	Reserved	Reserved, the reset value must be maintained.
12	DAC12RST	DAC12 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset DAC12
11:5	Reserved	Reserved, the reset value must be maintained.
4	WWDG2RST	WWDG2 soft reset 0: Clear reset 1: Reset WWDG2
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.39 APB1 peripherals reset register 3(RCC_APB1RST3)

Address offset: 0x009c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			USART1RST	Reserved			USART2RST	Reserved			USART3RST	Reserved			USART4RST
			rw				rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			UART9RST	Reserved			UART10RST	Reserved			UART11RST	Reserved			UART12RST
			rw				rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	USART1RST	USART1 soft reset 0: Clear reset 1: Reset USART1
27:25	Reserved	Reserved, the reset value must be maintained.
24	USART2RST	USART2 soft reset 0: Clear reset 1: Reset USART2
23:21	Reserved	Reserved, the reset value must be maintained.
20	USART3RST	USART3 soft reset 0: Clear reset 1: Reset USART3
19:17	Reserved	Reserved, the reset value must be maintained.
16	USART4RST	USART4 soft reset 0: Clear reset 1: Reset USART4
15:13	Reserved	Reserved, the reset value must be maintained.
12	UART9RST	UART9 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset UART9
11:9	Reserved	Reserved, the reset value must be maintained.
8	UART10RST	UART10 soft reset 0: Clear reset 1: Reset UART10
7:5	Reserved	Reserved, the reset value must be maintained.
4	UART11RST	UART11 soft reset 0: Clear reset 1: Reset UART11
3:1	Reserved	Reserved, the reset value must be maintained.
0	UART12RST	UART12 soft reset 0: Clear reset 1: Reset UART12

4.5.40 APB1 peripherals reset register 4(RCC_APB1RST4)

Address offset: 0x00a0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			I2S3RST	Reserved			I2S4RST	Reserved			I2C1RST	Reserved			I2C2RST
			rw				rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			I2C3RST	Reserved											
			rw												

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	I2S3RST	I2S3 soft reset 0: Clear reset 1: Reset I2S3
27:25	Reserved	Reserved, the reset value must be maintained.
24	I2S4RST	I2S4 soft reset 0: Clear reset 1: Reset I2S4
23:21	Reserved	Reserved, the reset value must be maintained.
20	I2C1RST	I2C1 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset I2C1
19:17	Reserved	Reserved, the reset value must be maintained.
16	I2C2RST	I2C2 soft reset 0: Clear reset 1: Reset I2C2
15:13	Reserved	Reserved, the reset value must be maintained.
12	I2C3RST	I2C3 soft reset 0: Clear reset 1: Reset I2C3
11:0	Reserved	Reserved, the reset value must be maintained.

4.5.41 APB1 peripherals reset register 5(RCC_APB1RST5)

Address offset: 0x00a4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			FDCAN1RST	Reserved			FDCAN2RST	Reserved			FDCAN5RST	Reserved			FDCAN6RST
			rw				rw				rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											CAHIRST	Reserved			CAHDRST
											rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	FDCAN1RST	FDCAN1 soft reset 0: Clear reset 1: Reset FDCAN1
27:25	Reserved	Reserved, the reset value must be maintained.
24	FDCAN2RST	FDCAN2 soft reset 0: Clear reset 1: Reset FDCAN2
23:21	Reserved	Reserved, the reset value must be maintained.
20	FDCAN5RST	FDCAN5 soft reset 0: Clear reset 1: Reset FDCAN5
19:17	Reserved	Reserved, the reset value must be maintained.

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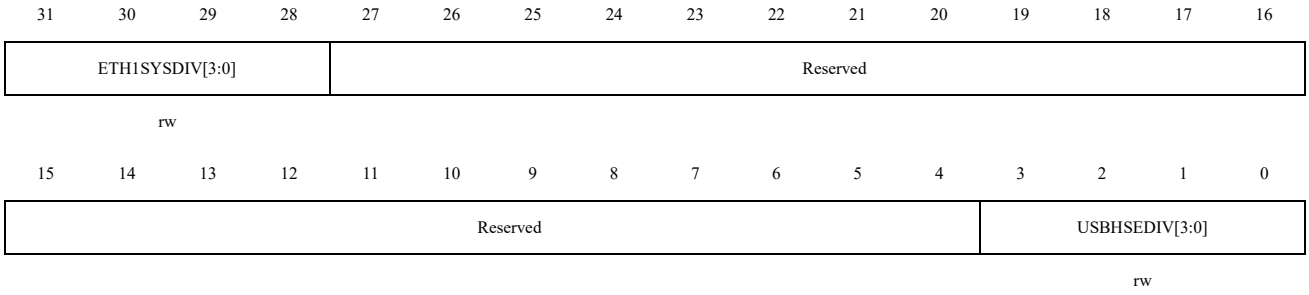
Bit field	Name	Description
16	FDCAN6RST	FDCAN6 soft reset 0: Clear reset 1: Reset FDCAN6
15:5	Reserved	Reserved, the reset value must be maintained.
4	CAHIRST	CAH_I soft reset 0: Clear reset 1: Reset CAH_I
3:1	Reserved	Reserved, the reset value must be maintained.
0	CAHDRST	CAH_D soft reset 0: Clear reset 1: Reset CAH_D

4.5.42 AHB2 peripherals clock divider register 1(RCC_AHB2DIV1)

Address offset: 0x00a8

Reset value: 0x00000000



Bit field	Name	Description
31:28	ETH1SYSDIV[3:0]	Ethernet1 system clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
27:4	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
3:0	USBHSEDIV[3:0]	USB HSE clock prescalar values. 0000: Divide by 1 0001: Divide by 2 Other values: setting is not allowed

4.5.43 AHB2 peripherals clock source select register 1(RCC_AHB2SEL1)

Address offset: 0x00ac

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
										ETH1PTPSEL[1:0]		ETH1GMIITXSEL[1:0]			
										rw		rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21:20	ETH1PTPSEL[1:0]	Ethernet1 PTP clock selection. 00: Divided system bus clock is selected as Ethernet1 PTP clock 01: Peripheral clock is selected as Ethernet1 PTP clock 10: PLL2_C clock is selected as Ethernet1 PTP clock 11: PLL3_A clock is selected as Ethernet1 PTP clock
19:18	ETH1GMIITXSEL[1:0]	Ethernet 1 clock mux 125 MHz clock source selection for "eth_gmii_tx_clk" port. 00: PLL3_A clock is selected as the 125 MHZ clock source for "eth_gmii_tx_clk". 01: PLL2_B clock is selected as the 125 MHz clock source for "eth_gmii_tx_clk". 10: Pad clock is selected as the 125 MHz clock source for "eth_gmii_tx_clk" 11: PLL1_C clock is selected as the 125 MHz clock source for "eth_gmii_tx_clk".
17:0	Reserved	Reserved, the reset value must be maintained.

4.5.44 AHB2 peripherals clock enable register 1(RCC_AHB2EN1)

Address offset: 0x00b0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved								M7USB1EN	M4USB1EN	M7USB1LPEN	M4USB1LPEN	Reserved			
								rw	rw	rw	rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7ECCM2EN	M4ECCM2EN	M7ECCM2LPEN	M4ECCM2LPEN	M7CORDICEN	M4CORDICEN	M7CORDICLPEN	M4CORDICLPEN	M7SDPUEN	M4SDPUEN	M7SDPULPEN	M4SDPULPEN	M7FMACEN	M4FMACEN	M7FMACLPEN	M4FMACLPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	M7USB1EN	USB1 M7 allocation and clock enable. Set and cleared by software. 0: USB1 is not allocated to M7. The "usb1_gated_hclk" is disabled in M7 RUN mode. 1: USB1 is allocated to M7. The "usb1_gated_hclk" is enabled in M7 RUN mode.
22	M4USB1EN	USB1 M4 allocation and clock enable. Set and cleared by software. 0: USB1 is not allocated to M4. The "usb1_gated_hclk" is disabled in M4 RUN mode. 1: USB1 is allocated to M4. The "usb1_gated_hclk" is enabled in M4 RUN mode.
21	M7USB1LPEN	USB1 M7 Low Power clock Enable. Set and cleared by software. 0: The "usb1_gated_hclk" is disabled in M7 SLEEP and STOP mode. 1: The "usb1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7USB1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4USB1LPEN	USB1 M4 Low Power clock Enable. Set and cleared by software. 0: The "usb1_gated_hclk" is disabled in M4 SLEEP and STOP mode. 1: The "usb1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4USB1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19:16	Reserved	Reserved, the reset value must be maintained.
15	M7ECCM2EN	ECCMON2 M7 allocation and clock enable. Set and cleared by software. 0: ECCMON2 is not allocated to M7. The "eccmon2_gated_hclk" is disabled in M7 RUN mode. 1: ECCMON2 is allocated to M7. The "eccmon2_gated_hclk" is enabled in M7 RUN mode.
14	M4ECCM2EN	ECCMON2 M4 allocation and clock enable. Set and cleared by software. 0: ECCMON2 is not allocated to M4. The "eccmon2_gated_hclk" is disabled in M4 RUN mode. 1: ECCMON2 is allocated to M4. The "eccmon2_gated_hclk" is enabled in M4 RUN mode.
13	M7ECCM2LPEN	ECCMON2 M7 Low Power clock Enable.

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Bit field	Name	Description
		Set and cleared by software. 0: The "eccmon2_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "eccmon2_gated_hclk" is enabled in M7 SLEEP mode. Note : M7ECCM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4ECCM2LPEN	ECCMON2 M4 Low Power clock Enable. Set and cleared by software. 0: The "eccmon2_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "eccmon2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ECCM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7CORDICEN	CORDIC M7 allocation and clock enable. Set and cleared by software. 0: CORDIC is not allocated to M7. The "cordic_gated_hclk" is disabled in M7 RUN mode. 1: CORDIC is allocated to M7. The "cordic_gated_hclk" is enabled in M7 RUN mode.
10	M4CORDICEN	CORDIC M4 allocation and clock enable. Set and cleared by software. 0: CORDIC is not allocated to M4. The "cordic_gated_hclk" is disabled in M4 RUN mode. 1: CORDIC is allocated to M4. The "cordic_gated_hclk" is enabled in M4 RUN mode.
9	M7CORDICLPEN	CORDIC M7 Low Power clock Enable. Set and cleared by software. 0: The "cordic_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "cordic_gated_hclk" is enabled in M7 SLEEP mode. Note : M7CORDICEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4CORDICLPEN	CORDIC M4 Low Power clock Enable. Set and cleared by software. 0: The "cordic_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "cordic_gated_hclk" is enabled in M4 SLEEP mode. Note : M4CORDICEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7SDPUEN	SDPU M7 allocation and clock enable. Set and cleared by software. 0: SDPU is not allocated to M7. The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" and "sdpu_gated_hclk" are disabled in M7 RUN mode. 1: SDPU is allocated to M7. The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" and "sdpu_gated_hclk" are enabled in M7 RUN mode.
6	M4SDPUEN	SDPU M4 allocation and clock enable. Set and cleared by software. 0: SDPU is not allocated to M4. The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" and "sdpu_gated_hclk" are disabled in M4 RUN mode.

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Bit field	Name	Description
		1: SDPU is allocated to M4. The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" and "sdpu_gated_hclk" are enabled in M4 RUN mode.
5	M7SDPULPEN	SDPU M7 Low Power clock Enable. Set and cleared by software. 0: The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" and "sdpu_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk"is enabled in M7 SLEEP and STOP mode. "sdpu_gated_hclk" is enabled in M7 SLEEP mode. Note : M7SDPUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4SDPULPEN	SDPU M4 Low Power clock Enable. Set and cleared by software. 0: The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" and "sdpu_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "sdpu_gated_(aes/des/sm4/rngc/sha)_clk" is enabled in M4 SLEEP and STOP mode. "sdpu_gated_hclk" is enabled in M4 SLEEP mode. Note : M4SDPUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7FMACEN	FMAC M7 allocation and clock enable. Set and cleared by software. 0: FMAC is not allocated to M7. The "fmac_gated_hclk" is disabled in M7 RUN mode. 1: FMAC is allocated to M7. The "fmac_gated_hclk" is enabled in M7 RUN mode.
2	M4FMACEN	FMAC M4 allocation and clock enable. Set and cleared by software. 0: FMAC is not allocated to M4. The "fmac_gated_hclk" is disabled in M4 RUN mode. 1: FMAC is allocated to M4. The "fmac_gated_hclk" are enabled in M4 RUN mode.
1	M7FMACLPEN	FMAC M7 Low Power clock Enable. Set and cleared by software. 0: The "fmac_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "fmac_gated_hclk" is enabled in M7 SLEEP mode. Note : M7FMACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4FMACLPEN	FMAC M4 Low Power clock Enable. Set and cleared by software. 0: The "fmac_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "fmac_gated_hclk" is enabled in M4 SLEEP mode. Note : M4FMACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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4.5.45 AHB2 peripherals clock enable register 2(RCC_AHB2EN2)

Address offset: 0x01b4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								M7DAC56EN	M4DAC56EN	M7DAC56LPEN	M4DAC56LPEN	M7DAC34EN	M4DAC34EN	M7DAC34LPEN	M4DAC34LPEN
								rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				M7ETH1TXEN	M4ETH1TXEN	M7ETH1TXLPEN	M4ETH1TXLPEN	M7ETH1RXEN	M4ETH1RXEN	M7ETH1RXLPEN	M4ETH1RXLPEN	M7ETH1MACEN	M4ETH1MACEN	M7ETH1MACLPEN	M4ETH1MACLPEN
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	M7DAC56EN	DAC56 M7 allocation and clock enable. Set and cleared by software. 0: DAC56 is not allocated to M7. The "dac56_gated_hclk" is disabled in M7 RUN mode. 1: DAC56 is allocated to M7. The "dac56_gated_hclk" is enabled in M7 RUN mode.
22	M4DAC56EN	DAC56 M4 allocation and clock enable. Set and cleared by software. 0: DAC56 is not allocated to M4. The "dac56_gated_hclk" is disabled in M4 RUN mode. 1: DAC56 is allocated to M4. The "dac56_gated_hclk" is enabled in M4 RUN mode.
21	M7DAC56LPEN	DAC56 M7 Low Power clock Enable. Set and cleared by software. 0: The "dac56_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "dac56_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DAC56EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4DAC56LPEN	DAC56 M4 Low Power clock Enable. Set and cleared by software. 0: The "dac56_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "dac56_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DAC56EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7DAC34EN	DAC34 M7 allocation and clock enable. Set and cleared by software. 0: DAC34 is not allocated to M7. The "dac34_gated_hclk" is disabled in M7 RUN mode. 1: DAC34 is allocated to M7. The "dac34_gated_hclk" is enabled in M7 RUN mode.
18	M4DAC34EN	DAC34 M4 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: DAC34 is not allocated to M4. The "dac34_gated_hclk" is disabled in M4 RUN mode. 1: DAC34 is allocated to M4. The "dac34_gated_hclk" is enabled in M4 RUN mode.
17	M7DAC34LPEN	DAC34 M7 Low Power clock Enable. Set and cleared by software. 0: The "dac34_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "dac34_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DAC34EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4DAC34LPEN	DAC34 M4 Low Power clock Enable. Set and cleared by software. 0: The "dac34_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "dac34_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DAC34EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15:12	Reserved	Reserved, the reset value must be maintained.
11	M7ETH1TXEN	ETH1TX M7 allocation and clock enable. Set and cleared by software. 0: ETH1TX is not allocated to M7. The "eth1_mii_tx_gated_clk" is disabled in M7 RUN mode. 1: ETH1TX is allocated to M7. The "eth1_mii_tx_gated_clk" is enabled in M7 RUN mode.
10	M4ETH1TXEN	ETH1TX M4 allocation and clock enable. Set and cleared by software. 0: ETH1TX is not allocated to M4. The "eth1_mii_tx_gated_clk" is disabled in M4 RUN mode. 1: ETH1TX is allocated to M4. The "eth1_mii_tx_gated_clk" is enabled in M4 RUN mode.
9	M7ETH1TXLPEN	ETH1TX M7 Low Power clock Enable. Set and cleared by software. 0: The "eth1_mii_tx_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "eth1_mii_tx_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ETH1TXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4ETH1TXLPEN	ETH1TX M4 Low Power clock Enable. Set and cleared by software. 0: The "eth1_mii_tx_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "eth1_mii_tx_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ETH1TXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7ETH1RXEN	ETH1RX M7 allocation and clock enable. Set and cleared by software. 0: ETH1RX is not allocated to M7. The "eth1_mii_rx_gated_clk" is disabled in M7 RUN mode. 1: ETH1RX is allocated to M7. The "eth1_mii_rx_gated_clk" is enabled in M7 RUN mode.

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Bit field	Name	Description
6	M4ETH1RXEN	ETH1RX M4 allocation and clock enable. Set and cleared by software. 0: ETH1RX is not allocated to M4. The "eth1_mii_rx_gated_clk" is disabled in M4 RUN mode. 1: ETH1RX is allocated to M4. The "eth1_mii_rx_gated_clk" is enabled in M4 RUN mode.
5	M7ETH1RXLPEN	ETH1RX M7 Low Power clock Enable. Set and cleared by software. 0: The "eth1_mii_rx_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "eth1_mii_rx_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ETH1RXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4ETH1RXLPEN	ETH1RX M4 Low Power clock Enable. Set and cleared by software. 0: The "eth1_mii_rx_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "eth1_mii_rx_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ETH1RXEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7ETH1MACEN	ETH1MAC M7 allocation and clock enable. Set and cleared by software. 0: ETH1MAC is not allocated to M7. The "eth1_gated_hclk" and "eth1_ptp_gated_clk are disabled in M7 RUN mode. 1: ETH1MAC is allocated to M7. The "eth1_gated_hclk" and "eth1_ptp_gated_clk" are enabled in M7 RUN mode.
2	M4ETH1MACEN	ETH1MAC M4 allocation and clock enable. Set and cleared by software. 0: ETH1MAC is not allocated to M4. The "eth1_gated_hclk" and "eth1_ptp_gated_clk" are disabled in M4 RUN mode. 1: ETH1MAC is allocated to M4. The "eth1_gated_hclk" and "eth1_ptp_gated_clk" is enabled in M4 RUN mode.
1	M7ETH1MACLPEN	ETH1MAC M7 Low Power clock Enable. Set and cleared by software. 0: The "eth1_gated_hclk" and "eth1_ptp_gated_clk" clock are disabled in M7 SLEEP and STOP mode. 1: The "eth1_gated_hclk" is enabled in M7 SLEEP mode.The "eth1_ptp_gated_clk" is enabled in M7 SLEEP and STOP0 mode. Note : M7ETH1MACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4ETH1MACLPEN	ETH1MAC M4 Low Power clock Enable. Set and cleared by software. 0: The "eth1_gated_hclk" and "eth1_ptp_gated_clk" clock are disabled in M4 SLEEP and STOP mode.

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Bit field	Name	Description
		1: The "eth1_gated_hclk" is enabled in M4 SLEEP mode. The "eth1_ptp_gated_clk" is enabled in M4 SLEEP and STOP0 mode. Note : M4ETH1MACEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.46 AHB2 peripherals reset register 1(RCC_AHB2RST1)

Address offset: 0x00b4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						DAC56RST	DAC34RST	Reserved	USB1WRAPRST	USB1PORRST	USB1RST	Reserved			ETH1RST
						rw	rw	rw	rw	rw	rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ECCM2RST	Reserved			CORDICRST	Reserved			SDPURST	Reserved			FMACRST
			rw				rw				rw				rw

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	DAC56RST	DAC56 soft reset 0: Clear reset 1: Reset DAC56
24	DAC34RST	DAC34 soft reset 0: Clear reset 1: Reset DAC34
23	Reserved	Reserved, the reset value must be maintained.
22	USB1WRAPRST	USB1 WRAPPER soft reset 0: Clear reset 1: Reset USB1 WRAPPER
21	USB1PORRST	USB1 POR soft reset 0: Clear reset 1: Reset USB1 POR
20	USB1RST	USB1 soft reset 0: Clear reset 1: Reset USB1
19:17	Reserved	Reserved, the reset value must be maintained.
16	ETH1RST	ETH1 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset ETH1
15:13	Reserved	Reserved, the reset value must be maintained.
12	ECCM2RST	ECCMON2 soft reset 0: Clear reset 1: Reset ECCMON2
11:9	Reserved	Reserved, the reset value must be maintained.
8	CORDICRST	CORDIC soft reset 0: Clear reset 1: Reset CORDIC
7:5	Reserved	Reserved, the reset value must be maintained.
4	SDPURST	SDPU soft reset 0: Clear reset 1: Reset SDPU
3:1	Reserved	Reserved, the reset value must be maintained.
0	FMACRST	FMAC soft reset 0: Clear reset 1: Reset FMAC

4.5.47 APB2 peripherals clock divider register 1(RCC_APB2DIV1)

Address offset: 0x00b8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	APB2ATIMDIV[2:0]			Reserved	APB2GTIMDIV[2:0]			Reserved					APB2I2SDIV[2:0]		
	rw				rw								rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	APB2DSMUDIV[2:0]			Reserved	APB2I2CDIV[2:0]			Reserved	APB2FDCANDIV[2:0]			Reserved			
	rw				rw				rw						

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	APB2ATIMDIV[2:0]	APB2 Atimer clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16

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Bit field	Name	Description
27	Reserved	Reserved, the reset value must be maintained.
26:24	APB2GTIMDIV[2:0]	APB2 Gtimer clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
23:19	Reserved	Reserved, the reset value must be maintained.
18:16	APB2I2SDIV[2:0]	APB2 I2S clock prescalar values Effective when "I2S(n)KERSEL" is selected as 2'b00. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
15	Reserved	Reserved, the reset value must be maintained.
14:12	APB2DSMUDIV[2:0]	DSMU system bus clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
11	Reserved	Reserved, the reset value must be maintained.
10:8	APB2I2CDIV[2:0]	APB2 I2C clock prescalar values Effective when "I2C(n)KERSEL" is selected as 3’b000. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
7	Reserved	Reserved, the reset value must be maintained.
6:4	APB2FDCANDIV[2:0]	APB2 FDCAN clock prescalar values Effective when "FDCAN(n)KERSEL" is selected as 3'b000. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
3:0	Reserved	Reserved, the reset value must be maintained.

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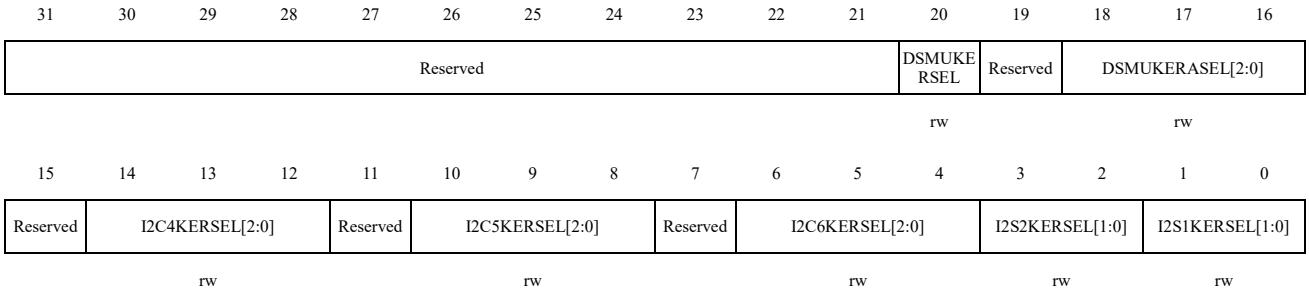
4.5.48 APB2 peripherals clock source select register 1(RCC_APB2SEL1)

Address offset: 0x00bc

Reset value: 0x00000000



Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20	DSMUKERSEL	DSMU Kernel clock selection. 0: APB2 bus clock is selected as "dsmu_gated_ker_clk". 1: Divided system bus clock is selected as "dsmu_gated_ker_clk".
19	Reserved	Reserved, the reset value must be maintained.
18:16	DSMUKERASEL[2:0]	DSMU Kernel A clock selection. 000: APB2 bus clock is selected as "dsmu_gated_ker_a_clk". 001: PLL1_B clock is selected as "dsmu_gated_ker_a_clk". 010: PLL2_B clock is selected as "dsmu_gated_ker_a_clk". 011: PLL3_A clock is selected as "dsmu_gated_ker_a_clk". 100: I2S_CKIN clock is selected as "dsmu_gated_ker_a_clk". 101: Peripheral clock is selected as "dsmu_gated_ker_a_clk". Other values: setting is not allowed
15	Reserved	Reserved, the reset value must be maintained.
14:12	I2C4KERSEL[2:0]	I2C4 Kernel clock selection. 000: Divided system bus clock is selected as "i2c4_ker_gated_clk". 001: PLL3_C clock is selected as "i2c4_ker_gated_clk". 010: HSI clock is selected as "i2c4_ker_gated_clk". 011: MSI clock is selected as "i2c4_ker_gated_clk". Other values: setting is not allowed
11	Reserved	Reserved, the reset value must be maintained.
10:8	I2C5KERSEL[2:0]	I2C5 Kernel clock selection. 000: Divided system bus clock is selected as "i2c5_ker_gated_clk". 001: PLL3_C clock is selected as "i2c5_ker_gated_clk". 010: HSI clock is selected as "i2c5_ker_gated_clk". 011: MSI clock is selected as "i2c5_ker_gated_clk". Other values: setting is not allowed

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Bit field	Name	Description
7	Reserved	Reserved, the reset value must be maintained.
6:4	I2C6KERSEL[2:0]	I2C6 Kernel clock selection. 000: Divided system bus clock is selected as "i2c6_ker_gated_clk". 001: PLL3_C clock is selected as "i2c6_ker_gated_clk". 010: HSI clock is selected as "i2c6_ker_gated_clk". 011: MSI clock is selected as "i2c6_ker_gated_clk". Other values: setting is not allowed
3:2	I2S2KERSEL[1:0]	I2S2 Kernel clock selection. 00: Divided system bus clock is selected as "i2s2_ker_gated_clk". 01: PLL3_B clock is selected as "i2s2_ker_gated_clk". 10: HSI clock is selected as "i2s2_ker_gated_clk". 11: i2s2_ckin_clk (from IOM) is selected as "i2s2_ker_gated_clk".
1:0	I2S1KERSEL[1:0]	I2S1 Kernel clock selection. 00: Divided system bus clock is selected as "i2s1_ker_gated_clk". 01: PLL3_B clock is selected as "i2s1_ker_gated_clk". 10: HSI clock is selected as "i2s1_ker_gated_clk". 11: i2s1_ckin_clk (from IOM) is selected as "i2s1_ker_gated_clk".

4.5.49 APB2 peripherals clock source select register 2(RCC_APB2SEL2)

Address offset: 0x00c0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	FDCAN3KERSEL[2:0]			Reserved					FDCAN4KERSEL[2:0]			Reserved			
	rw								rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	FDCAN7KERSEL[2:0]			Reserved					FDCAN8KERSEL[2:0]			Reserved			
	rw								rw						

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	FDCAN3KERSEL[2:0]	FDCAN3 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan3_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan3_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan3_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan3_gated_ker_clk". 100: Peripheral clock is selected as "fdcan3_gated_ker_clk".

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Bit field	Name	Description
		Other values: setting is not allowed
27:23	Reserved	Reserved, the reset value must be maintained.
22:20	FDCAN4KERSEL[2:0]	FDCAN4 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan4_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan4_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan4_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan4_gated_ker_clk". 100: Peripheral clock is selected as "fdcan4_gated_ker_clk". Other values: setting is not allowed
19:15	Reserved	Reserved, the reset value must be maintained.
14:12	FDCAN7KERSEL[2:0]	FDCAN7 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan7_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan7_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan7_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan7_gated_ker_clk". 100: Peripheral clock is selected as "fdcan7_gated_ker_clk". Other values: setting is not allowed
11:7	Reserved	Reserved, the reset value must be maintained.
6:4	FDCAN8KERSEL[2:0]	FDCAN8 Kernel clock selection. 000: Divided system bus clock is selected as "fdcan8_gated_ker_clk". 001: PLL1_C clock is selected as "fdcan8_gated_ker_clk". 010: PLL2_C clock is selected as "fdcan8_gated_ker_clk". 011: PLL3_B clock is selected as "fdcan8_gated_ker_clk". 100: Peripheral clock is selected as "fdcan8_gated_ker_clk". Other values: setting is not allowed
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.50 APB2 peripherals clock enable register 1(RCC_APB2EN1)

Address offset: 0x00c4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7ATIM1EN	M4ATIM1EN	M7ATIM1LPEN	M4ATIM1LPEN	M7ATIM2EN	M4ATIM2EN	M7ATIM2LPEN	M4ATIM2LPEN	M7GTIMA1EN	M4GTIMA1EN	M7GTIMA1LPEN	M4GTIMA1LPEN	M7GTIMA2EN	M4GTIMA2EN	M7GTIMA2LPEN	M4GTIMA2LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7GTIMA3EN	M4GTIMA3EN	M7GTIMA3LPEN	M4GTIMA3LPEN	M7SHRTIM1EN	M4SHRTIM1EN	M7SHRTIM1LPEN	M4SHRTIM1LPEN	M7SHRTIM2EN	M4SHRTIM2EN	M7SHRTIM2LPEN	M4SHRTIM2LPEN	Reserved			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				

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Bit field	Name	Description
31	M7ATIM1EN	ATIMER1 M7 allocation and clock enable. Set and cleared by software. 0: ATIMER1 is not allocated to M7. The "atimer1_gated_ker_clk" and "atimer1_gated_pclk" are disabled in M7 RUN mode. 1: ATIMER1 is allocated to M7. The "atimer1_gated_ker_clk" and "atimer1_gated_pclk" are enabled in M7 RUN mode.
30	M4ATIM1EN	ATIMER1 M4 allocation and clock enable. Set and cleared by software. 0: ATIMER1 is not allocated to M4. The "atimer1_gated_ker_clk" and "atimer1_gated_pclk" are disabled in M4 RUN mode. 1: ATIMER1 is allocated to M4. The "atimer1_gated_ker_clk" and "atimer1_gated_pclk" are enabled in M4 RUN mode.
29	M7ATIM1LPEN	ATIMER1 M7 Low Power clock Enable. Set and cleared by software. 0: The "atimer1_gated_ker_clk" and "atimer1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "atimer1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "atimer1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7ATIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4ATIM1LPEN	ATIMER1 M4 Low Power clock Enable. Set and cleared by software. 0: The "atimer1_gated_ker_clk" and "atimer1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "atimer1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "atimer1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4ATIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7ATIM2EN	ATIMER2 M7 allocation and clock enable. Set and cleared by software. 0: ATIMER2 is not allocated to M7. The "atimer2_gated_ker_clk" and "atimer2_gated_pclk" are disabled in M7 RUN mode. 1: ATIMER2 is allocated to M7. The "atimer2_gated_ker_clk" and "atimer2_gated_pclk" are enabled in M7 RUN mode.
26	M4ATIM2EN	ATIMER2 M4 allocation and clock enable. Set and cleared by software. 0: ATIMER2 is not allocated to M4. The "atimer2_gated_ker_clk" and "atimer2_gated_pclk" are disabled in M4 RUN mode. 1: ATIMER2 is allocated to M4. The "atimer2_gated_ker_clk" and "atimer2_gated_pclk" are enabled in M4 RUN mode.
25	M7ATIM2LPEN	ATIMER2 M7 Low Power clock Enable.

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Bit field	Name	Description
		Set and cleared by software. 0: The "atimer2_gated_ker_clk" and "atimer2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "atimer2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "atimer2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7ATIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4ATIM2LPEN	ATIMER2 M4 Low Power clock Enable. Set and cleared by software. 0: The "atimer2_gated_ker_clk" and "atimer2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "atimer2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "atimer2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4ATIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7GTIMA1EN	GTIMERA1 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA1 is not allocated to M7. The "gtimera1_gated_ker_clk" and "gtimera1_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA1 is allocated to M7. The "gtimera1_gated_ker_clk" and "gtimera1_gated_pclk" are enabled in M7 RUN mode.
22	M4GTIMA1EN	GTIMERA1 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA1 is not allocated to M4. The "gtimera1_gated_ker_clk" and "gtimera1_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA1 is allocated to M4. The "gtimera1_gated_ker_clk" and "gtimera1_gated_pclk" are enabled in M4 RUN mode.
21	M7GTIMA1LPEN	GTIMERA1 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera1_gated_ker_clk" and "gtimera1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7GTIMA1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4GTIMA1LPEN	GTIMERA1 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera1_gated_ker_clk" and "gtimera1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera1_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4GTIMA1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7GTIMA2EN	GTIMERA2 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA2 is not allocated to M7. The "gtimera2_gated_ker_clk" and "gtimera2_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA2 is allocated to M7. The "gtimera2_gated_ker_clk" and "gtimera2_gated_pclk" are enabled in M7 RUN mode.
18	M4GTIMA2EN	GTIMERA2 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA2 is not allocated to M4. The "gtimera2_gated_ker_clk" and "gtimera2_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA2 is allocated to M4. The "gtimera2_gated_ker_clk" and "gtimera2_gated_pclk" are enabled in M4 RUN mode.
17	M7GTIMA2LPEN	GTIMERA2 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera2_gated_ker_clk" and "gtimera2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7GTIMA2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4GTIMA2LPEN	GTIMERA2 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera2_gated_ker_clk" and "gtimera2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4GTIMA2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7GTIMA3EN	GTIMERA3 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA3 is not allocated to M7. The "gtimera3_gated_ker_clk" and "gtimera3_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA3 is allocated to M7. The "gtimera3_gated_ker_clk" and "gtimera3_gated_pclk" are enabled in M7 RUN mode.
14	M4GTIMA3EN	GTIMERA3 M4 allocation and clock enable. Set and cleared by software. 0: GTIMERA3 is not allocated to M4. The "gtimera3_gated_ker_clk" and "gtimera3_gated_pclk" are disabled in M4 RUN mode. 1: GTIMERA3 is allocated to M4. The "gtimera3_gated_ker_clk" and "gtimera3_gated_pclk" are enabled in M4 RUN mode.

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Bit field	Name	Description
13	M7GTIMA3LPEN	GTIMERA3 M7 Low Power clock Enable. Set and cleared by software. 0: The "gtimera3_gated_ker_clk" and "gtimera3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "gtimera3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "gtimera3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7GTIMA3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4GTIMA3LPEN	GTIMERA3 M4 Low Power clock Enable. Set and cleared by software. 0: The "gtimera3_gated_ker_clk" and "gtimera3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "gtimera3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "gtimera3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4GTIMA3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7SHRTIM1EN	GTIMERA3 M7 allocation and clock enable. Set and cleared by software. 0: GTIMERA3 is not allocated to M7. The "shrtimer1_gated_ker_clk" and "shrtimer1_gated_pclk" are disabled in M7 RUN mode. 1: GTIMERA3 is allocated to M7. The "shrtimer1_gated_ker_clk" and "shrtimer1_gated_pclk" are enabled in M7 RUN mode.
10	M4SHRTIM1EN	SHRTIMER1 M4 allocation and clock enable. Set and cleared by software. 0: SHRTIMER1 is not allocated to M4. The "shrtimer1_gated_ker_clk" and "shrtimer1_gated_pclk" are disabled in M4 RUN mode. 1: SHRTIMER1 is allocated to M4. The "shrtimer1_gated_ker_clk" and "shrtimer1_gated_pclk" are enabled in M4 RUN mode.
9	M7SHRTIM1LPEN	SHRTIMER1 M7 Low Power clock Enable. Set and cleared by software. 0: The "shrtimer1_gated_ker_clk" and "shrtimer1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "shrtimer1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "shrtimer1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SHRTIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4SHRTIM1LPEN	SHRTIMER1 M4 Low Power clock Enable. Set and cleared by software. 0: The "shrtimer1_gated_ker_clk" and "shrtimer1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "shrtimer1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "shrtimer1_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4SHRTIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7SHRTIM2EN	SHRTIMER2 M4 allocation and clock enable. Set and cleared by software. 0: SHRTIMER2 is not allocated to M4. The "shrtimer2_gated_ker_clk" and "shrtimer2_gated_pclk" are disabled in M4 RUN mode. 1: SHRTIMER2 is allocated to M4. The "shrtimer2_gated_ker_clk" and "shrtimer2_gated_pclk" are enabled in M4 RUN mode.
6	M4SHRTIM2EN	SHRTIMER2 M7 Low Power clock Enable. Set and cleared by software. 0: The "shrtimer2_gated_ker_clk" and "shrtimer2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "shrtimer2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "shrtimer2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SHRTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
5	M7SHRTIM2LPEN	SHRTIMER2 M4 Low Power clock Enable. Set and cleared by software. 0: The "shrtimer2_gated_ker_clk" and "shrtimer2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "shrtimer2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "shrtimer2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SHRTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4SHRTIM2LPEN	SHRTIMER2 M4 Low Power clock Enable. Set and cleared by software. 0: The "shrtimer2_gated_ker_clk" and "shrtimer2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "shrtimer2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "shrtimer2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SHRTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.51 APB2 peripherals clock enable register 2(RCC_APB2EN2)

Address offset: 0x00c8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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M7I2S1EN	M4I2S1EN	M7I2S1LPEN	M4I2S1LPEN	M7I2S2EN	M4I2S2EN	M7I2S2LPEN	M4I2S2LPEN	M7SPI1EN	M4SPI1EN	M7SPI1LPEN	M4SPI1LPEN	M7SPI2EN	M4SPI2EN	M7SPI2LPEN	M4SPI2LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7DSMUEN	M4DSMUEN	M7DSMULPEN	M4DSMULPEN	M7I2C4EN	M4I2C4EN	M7I2C4LPEN	M4I2C4LPEN	M7I2C5EN	M4I2C5EN	M7I2C5LPEN	M4I2C5LPEN	M7I2C6EN	M4I2C6EN	M7I2C6LPEN	M4I2C6LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7I2S1EN	I2S1 M7 allocation and clock enable. Set and cleared by software. 0: I2S1 is not allocated to M7. The "i2s1_ker_gated_clk" and "i2s1_gated_pclk" are disabled in M7 RUN mode. 1: I2S1 is allocated to M7. The "i2s1_ker_gated_clk" and "i2s1_gated_pclk" are enabled in M7 RUN mode.
30	M4I2S1EN	I2S1 M4 allocation and clock enable. Set and cleared by software. 0: I2S1 is not allocated to M4. The "i2s1_ker_gated_clk" and "i2s1_gated_pclk" are disabled in M4 RUN mode. 1: I2S1 is allocated to M4. The "i2s1_ker_gated_clk" and "i2s1_gated_pclk" are enabled in M4 RUN mode.
29	M7I2S1LPEN	I2S1 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2s1_ker_gated_clk" and "i2s1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2s1_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2s1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2S1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4I2S1LPEN	I2S1 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2s1_ker_gated_clk" and "i2s1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2s1_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2s1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2S1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7I2S2EN	I2S2 M7 allocation and clock enable. Set and cleared by software. 0: I2S2 is not allocated to M7. The "i2s2_ker_gated_clk" and "i2s2_gated_pclk" are disabled in M7 RUN mode. 1: I2S2 is allocated to M7. The "i2s2_ker_gated_clk" and "i2s2_gated_pclk" are enabled in M7 RUN mode.

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Bit field	Name	Description
26	M4I2S2EN	I2S2 M4 allocation and clock enable. Set and cleared by software. 0: I2S2 is not allocated to M4. The "i2s2_ker_gated_clk" and "i2s2_gated_pclk" are disabled in M4 RUN mode. 1: I2S2 is allocated to M4. The "i2s2_ker_gated_clk" and "i2s2_gated_pclk" are enabled in M4 RUN mode.
25	M7I2S2LPEN	I2S2 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2s2_ker_gated_clk" and "i2s2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2s2_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2s2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2S2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4I2S2LPEN	I2S2 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2s2_ker_gated_clk" and "i2s2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2s2_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2s2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2S2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7SPI1EN	SPI1 M7 allocation and clock enable. Set and cleared by software. 0: SPI1 is not allocated to M7. The " spi1_gated_ker_clk" and "spi1_gated_pclk" are disabled in M7 RUN mode. 1: SPI1 is allocated to M7. The " spi1_gated_ker_clk" and "spi1_gated_pclk" are enabled in M7 RUN mode.
22	M4SPI1EN	SPI1 M4 allocation and clock enable. Set and cleared by software. 0: SPI1 is not allocated to M4. The " spi1_gated_ker_clk" and "spi1_gated_pclk" are disabled in M4 RUN mode. 1: SPI1 is allocated to M4. The " spi1_gated_ker_clk" and "spi1_gated_pclk" are enabled in M4 RUN mode.
21	M7SPI1LPEN	SPI1 M7 Low Power clock Enable. Set and cleared by software. 0: The " spi1_gated_ker_clk" and "spi1_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Bit field	Name	Description
20	M4SPI1LPEN	SPI1 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi1_gated_ker_clk" and "spi1_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SPI1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7SPI2EN	SPI2 M7 allocation and clock enable. Set and cleared by software. 0: SPI2 is not allocated to M7. The " spi2_gated_ker_clk" and "spi2_gated_pclk" are disabled in M7 RUN mode. 1: SPI2 is allocated to M7. The " spi2_gated_ker_clk" and "spi2_gated_pclk" are enabled in M7 RUN mode.
18	M4SPI2EN	SPI2 M4 allocation and clock enable. Set and cleared by software. 0: SPI2 is not allocated to M4. The " spi2_gated_ker_clk" and "spi2_gated_pclk" are disabled in M4 RUN mode. 1: SPI2 is allocated to M4. The " spi2_gated_ker_clk" and "spi2_gated_pclk" are enabled in M4 RUN mode.
17	M7SPI2LPEN	SPI2 M7 Low Power clock Enable. Set and cleared by software. 0: The " spi2_gated_ker_clk" and "spi2_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4SPI2LPEN	SPI2 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi2_gated_ker_clk" and "spi2_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SPI2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7DSMUEN	DSMU M7 allocation and clock enable. Set and cleared by software. 0: DSMU is not allocated to M7. The "dsmu_gated_ker_clk", "dsmu_gated_ker_a_clk" and "dsmu_gated_pclk" are disabled in M7 RUN mode. 1: DSMU is allocated to M7. The "dsmu_gated_ker_clk", "dsmu_gated_ker_a_clk" and "dsmu_gated_pclk" are enabled in M7 RUN mode.

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Bit field	Name	Description
14	M4DSMUEN	DSMU M4 allocation and clock enable. Set and cleared by software. 0: DSMU is not allocated to M4. The "dsmu_gated_ker_clk", "dsmu_gated_ker_a_clk" and "dsmu_gated_pclk" are disabled in M4 RUN mode. 1: DSMU is allocated to M4. The "dsmu_gated_ker_clk", "dsmu_gated_ker_a_clk" and "dsmu_gated_pclk" are enabled in M4 RUN mode.
13	M7DSMULPEN	DSMU M7 Low Power clock Enable. Set and cleared by software. 0: The "dsmu_gated_ker_clk", "dsmu_gated_ker_a_clk" and "dsmu_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "dsmu_gated_ker_clk" and "dsmu_gated_ker_a_clk" are enabled in M7 SLEEP and STOP mode. "dsmu_gated_pclk" is enabled in M7 SLEEP mode. Note : M7DSMUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4DSMULPEN	DSMU M4 Low Power clock Enable. Set and cleared by software. 0: The "dsmu_gated_ker_clk", "dsmu_gated_ker_a_clk" and "dsmu_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "dsmu_gated_ker_clk" and "dsmu_gated_ker_a_clk" are enabled in M4 SLEEP and STOP mode. "dsmu_gated_pclk" is enabled in M4 SLEEP mode. Note : M4DSMUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7I2C4EN	I2C4 M7 allocation and clock enable. Set and cleared by software. 0: I2C4 is not allocated to M7. The "i2c4_ker_gated_clk" and "i2c4_gated_pclk" are disabled in M7 RUN mode. 1: I2C4 is allocated to M7. The "i2c4_ker_gated_clk" and "i2c4_gated_pclk" are enabled in M7 RUN mode.
10	M4I2C4EN	I2C4 M4 allocation and clock enable. Set and cleared by software. 0: I2C4 is not allocated to M4. The "i2c4_ker_gated_clk" and "i2c4_gated_pclk" are disabled in M4 RUN mode. 1: I2C4 is allocated to M4. The "i2c4_ker_gated_clk" and "i2c4_gated_pclk" are enabled in M4 RUN mode.
9	M7I2C4LPEN	I2C4 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c4_ker_gated_clk" and "i2c4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c4_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Email: sales@nsing.com.sg

Bit field	Name	Description
8	M4I2C4LPEN	I2C4 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c4_ker_gated_clk" and "i2c4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c4_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c4_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7I2C5EN	I2C5 M7 allocation and clock enable. Set and cleared by software. 0: I2C5 is not allocated to M7. The "i2c5_ker_gated_clk" and "i2c5_gated_pclk" are disabled in M7 RUN mode. 1: I2C5 is allocated to M7. The "i2c5_ker_gated_clk" and "i2c5_gated_pclk" are enabled in M7 RUN mode.
6	M4I2C5EN	I2C5 M4 allocation and clock enable. Set and cleared by software. 0: I2C5 is not allocated to M4. The "i2c5_ker_gated_clk" and "i2c5_gated_pclk" are disabled in M4 RUN mode. 1: I2C5 is allocated to M4. The "i2c5_ker_gated_clk" and "i2c5_gated_pclk" are enabled in M4 RUN mode.
5	M7I2C5LPEN	I2C5 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c5_ker_gated_clk" and "i2c5_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c5_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c5_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4I2C5LPEN	I2C5 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c5_ker_gated_clk" and "i2c5_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c5_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c5_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7I2C6EN	I2C6 M7 allocation and clock enable. Set and cleared by software. 0: I2C6 is not allocated to M7. The "i2c6_ker_gated_clk" and "i2c6_gated_pclk" are disabled in M7 RUN mode. 1: I2C6 is allocated to M7. The "i2c6_ker_gated_clk" and "i2c6_gated_pclk" are enabled in M7 RUN mode.

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Bit field	Name	Description
2	M4I2C6EN	I2C6 M4 allocation and clock enable. Set and cleared by software. 0: I2C6 is not allocated to M4. The "i2c6_ker_gated_clk" and "i2c6_gated_pclk" are disabled in M4 RUN mode. 1: I2C6 is allocated to M4. The "i2c6_ker_gated_clk" and "i2c6_gated_pclk" are enabled in M4 RUN mode.
1	M7I2C6LPEN	I2C6 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c6_ker_gated_clk" and "i2c6_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c6_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c6_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4I2C6LPEN	I2C6 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c6_ker_gated_clk" and "i2c6_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c6_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c6_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.52 APB2 peripherals clock enable register 3(RCC_APB2EN3)

Address offset: 0x00cc

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7USART5EN	M4USART5EN	M7USART5LPEN	M4USART5LPEN	M7USART6EN	M4USART6EN	M7USART6LPEN	M4USART6LPEN	M7USART7EN	M4USART7EN	M7USART7LPEN	M4USART7LPEN	M7USART8EN	M4USART8EN	M7USART8LPEN	M4USART8LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7UART13EN	M4UART13EN	M7UART13LPEN	M4UART13LPEN	M7UART14EN	M4UART14EN	M7UART14LPEN	M4UART14LPEN	M7UART15EN	M4UART15EN	M7UART15LPEN	M4UART15LPEN	Reserved			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				

Bit field	Name	Description
31	M7USART5EN	USART5 M7 allocation and clock enable. Set and cleared by software. 0: USART5 is not allocated to M7. The "usart5_gated_pclk" is disabled in M7 RUN mode. 1: USART5 is allocated to M7. The "usart5_gated_pclk" is enabled in M7 RUN mode.

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Bit field	Name	Description
30	M4USART5EN	USART5 M4 allocation and clock enable. Set and cleared by software. 0: USART5 is not allocated to M4. The "usart5_gated_pclk" is disabled in M4 RUN mode. 1: USART5 is allocated to M4. The "usart5_gated_pclk" is enabled in M4 RUN mode.
29	M7USART5LPEN	USART5 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart5_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart5_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4USART5LPEN	USART5 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart5_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart5_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7USART6EN	USART6 M7 allocation and clock enable. Set and cleared by software. 0: USART6 is not allocated to M7. The "usart6_gated_pclk" is disabled in M7 RUN mode. 1: USART6 is allocated to M7. The "usart6_gated_pclk" is enabled in M7 RUN mode.
26	M4USART6EN	USART6 M4 allocation and clock enable. Set and cleared by software. 0: USART6 is not allocated to M4. The "usart6_gated_pclk" is disabled in M4 RUN mode. 1: USART6 is allocated to M4. The "usart6_gated_pclk" is enabled in M4 RUN mode.
25	M7USART6LPEN	USART6 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart6_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart6_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4USART6LPEN	USART6 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart6_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart6_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7USART7EN	USART7 M7 allocation and clock enable. Set and cleared by software. 0: USART7 is not allocated to M7. The "usart7_gated_pclk" is disabled in M7 RUN mode. 1: USART7 is allocated to M7. The "usart7_gated_pclk" is enabled in M7 RUN mode.
22	M4USART7EN	USART7 M4 allocation and clock enable. Set and cleared by software.

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Email: sales@nsing.com.sg

Bit field	Name	Description
		0: USART7 is not allocated to M4. The "usart7_gated_pclk" is disabled in M4 RUN mode. 1: USART7 is allocated to M4. The "usart7_gated_pclk" is enabled in M4 RUN mode.
21	M7USART7LPEN	USART7 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart7_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart7_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4USART7LPEN	USART7 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart7_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart7_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7USART8EN	USART8 M7 allocation and clock enable. Set and cleared by software. 0: USART8 is not allocated to M7. The "usart8_gated_pclk" is disabled in M7 RUN mode. 1: USART8 is allocated to M7. The "usart8_gated_pclk" is enabled in M7 RUN mode.
18	M4USART8EN	USART8 M4 allocation and clock enable. Set and cleared by software. 0: USART8 is not allocated to M4. The "usart8_gated_pclk" is disabled in M4 RUN mode. 1: USART8 is allocated to M4. The "usart8_gated_pclk" is enabled in M4 RUN mode.
17	M7USART8LPEN	USART8 M7 Low Power clock Enable. Set and cleared by software. 0: The "usart8_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "usart8_gated_pclk" is enabled in M7 SLEEP mode. Note : M7USART8EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4USART8LPEN	USART8 M4 Low Power clock Enable. Set and cleared by software. 0: The "usart8_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "usart8_gated_pclk" is enabled in M4 SLEEP mode. Note : M4USART8EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7UART13EN	UART13 M7 allocation and clock enable. Set and cleared by software. 0: UART13 is not allocated to M7. The "uart13_gated_pclk" is disabled in M7 RUN mode. 1: UART13 is allocated to M7. The "uart13_gated_pclk" is enabled in M7 RUN mode.
14	M4UART13EN	UART13 M4 allocation and clock enable. Set and cleared by software. 0: UART13 is not allocated to M4. The "uart13_gated_pclk" is disabled in M4 RUN mode. 1: UART13 is allocated to M4. The "uart13_gated_pclk" is enabled in M4 RUN mode.

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Bit field	Name	Description
13	M7UART13LPEN	UART13 M7 Low Power clock Enable. Set and cleared by software. 0: The "uart13_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart13_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART13EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4UART13LPEN	UART13 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart13_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart13_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART13EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7UART14EN	UART14 M7 allocation and clock enable. Set and cleared by software. 0: UART14 is not allocated to M7. The "uart14_gated_pclk" is disabled in M7 RUN mode. 1: UART14 is allocated to M7. The "uart14_gated_pclk" is enabled in M7 RUN mode.
10	M4UART14EN	UART14 M4 allocation and clock enable. Set and cleared by software. 0: UART14 is not allocated to M4. The "uart14_gated_pclk" is disabled in M4 RUN mode. 1: UART14 is allocated to M4. The "uart14_gated_pclk" is enabled in M4 RUN mode.
9	M7UART14LPEN	UART14 M7 Low Power clock Enable. Set and cleared by software. 0: The "uart14_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart14_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART14EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4UART14LPEN	UART14 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart14_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart14_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART14EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7UART15EN	UART15 M7 allocation and clock enable. Set and cleared by software. 0: UART15 is not allocated to M7. The "uart15_gated_pclk" is disabled in M7 RUN mode. 1: UART15 is allocated to M7. The "uart15_gated_pclk" is enabled in M7 RUN mode.
6	M4UART15EN	UART15 M4 allocation and clock enable. Set and cleared by software. 0: UART15 is not allocated to M4. The "uart15_gated_pclk" is disabled in M4 RUN mode. 1: UART15 is allocated to M4. The "uart15_gated_pclk" is enabled in M4 RUN mode.
5	M7UART15LPEN	UART15 M7 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "uart15_gated_pclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "uart15_gated_pclk" is enabled in M7 SLEEP mode. Note : M7UART15EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4UART15LPEN	UART15 M4 Low Power clock Enable. Set and cleared by software. 0: The "uart15_gated_pclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "uart15_gated_pclk" is enabled in M4 SLEEP mode. Note : M4UART15EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.53 APB2 peripherals clock enable register 4(RCC_APB2EN4)

Address offset: 0x00d0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7FDCAN3EN	M4FDCAN3EN	M7FDCAN3LPEN	M4FDCAN3LPEN	M7FDCAN4EN	M4FDCAN4EN	M7FDCAN4LPEN	M4FDCAN4LPEN	M7FDCAN7EN	M4FDCAN7EN	M7FDCAN7LPEN	M4FDCAN7LPEN	M7FDCAN8EN	M4FDCAN8EN	M7FDCAN8LPEN	M4FDCAN8LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDCAN3STPREQ	FDCAN3STPACK	Reserved		FDCAN4STPREQ	FDCAN4STPACK	Reserved		FDCAN7STPREQ	FDCAN7STPACK	Reserved		FDCAN8STPREQ	FDCAN8STPACK	Reserved	
rw	r			rw	r			rw	r			rw	r		

Bit field	Name	Description
31	M7FDCAN3EN	FDCAN3 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN3 is not allocated to M7. The "fdcan3_gated_ker_clk" and "fdcan3_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN3 is allocated to M7. The "fdcan3_gated_ker_clk" and "fdcan3_gated_pclk" are enabled in M7 RUN mode.
30	M4FDCAN3EN	FDCAN3 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN3 is not allocated to M4. The "fdcan3_gated_ker_clk" and "fdcan3_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN3 is allocated to M4. The "fdcan3_gated_ker_clk" and "fdcan3_gated_pclk" are enabled in M4 RUN mode.

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Bit field	Name	Description
29	M7FDCAN3LPEN	FDCAN3 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan3_gated_ker_clk" and "fdcan3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7FDCAN3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4FDCAN3LPEN	FDCAN3 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan3_gated_ker_clk" and "fdcan3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7FDCAN4EN	FDCAN4 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN4 is not allocated to M7. The "fdcan4_gated_ker_clk" and "fdcan4_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN4 is allocated to M7. The "fdcan4_gated_ker_clk" and "fdcan4_gated_pclk" are enabled in M7 RUN mode.
26	M4FDCAN4EN	FDCAN4 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN4 is not allocated to M4. The "fdcan4_gated_ker_clk" and "fdcan4_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN4 is allocated to M4. The "fdcan4_gated_ker_clk" and "fdcan4_gated_pclk" are enabled in M4 RUN mode.
25	M7FDCAN4LPEN	FDCAN4 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan4_gated_ker_clk" and "fdcan4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan4_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7FDCAN4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4FDCAN4LPEN	FDCAN4 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan4_gated_ker_clk" and "fdcan4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan4_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan4_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4FDCAN4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7FDCAN7EN	FDCAN7 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN7 is not allocated to M7. The "fdcan7_gated_ker_clk" and "fdcan7_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN7 is allocated to M7. The "fdcan7_gated_ker_clk" and "fdcan7_gated_pclk" are enabled in M7 RUN mode.
22	M4FDCAN7EN	FDCAN7 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN7 is not allocated to M4. The "fdcan7_gated_ker_clk" and "fdcan7_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN7 is allocated to M4. The "fdcan7_gated_ker_clk" and "fdcan7_gated_pclk" are enabled in M4 RUN mode.
21	M7FDCAN7LPEN	FDCAN7 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan7_gated_ker_clk" and "fdcan7_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan7_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan7_gated_pclk" is enabled in M7 SLEEP mode. Note : M7FDCAN7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4FDCAN7LPEN	FDCAN7 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan7_gated_ker_clk" and "fdcan7_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan7_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan7_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7FDCAN8EN	FDCAN8 M7 allocation and clock enable. Set and cleared by software. 0: FDCAN8 is not allocated to M7. The "fdcan8_gated_ker_clk" and "fdcan8_gated_pclk" are disabled in M7 RUN mode. 1: FDCAN8 is allocated to M7. The "fdcan8_gated_ker_clk" and "fdcan8_gated_pclk" are enabled in M7 RUN mode.
18	M4FDCAN8EN	FDCAN8 M4 allocation and clock enable. Set and cleared by software. 0: FDCAN8 is not allocated to M4. The "fdcan8_gated_ker_clk" and "fdcan8_gated_pclk" are disabled in M4 RUN mode. 1: FDCAN8 is allocated to M4. The "fdcan8_gated_ker_clk" and "fdcan8_gated_pclk" are enabled in M4 RUN mode.

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Bit field	Name	Description
17	M7FDCAN8LPEN	FDCAN8 M7 Low Power clock Enable. Set and cleared by software. 0: The "fdcan8_gated_ker_clk" and "fdcan8_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "fdcan8_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "fdcan8_gated_pclk" is enabled in M7 SLEEP mode. Note : M7FDCAN8EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4FDCAN8LPEN	FDCAN8 M4 Low Power clock Enable. Set and cleared by software. 0: The "fdcan8_gated_ker_clk" and "fdcan8_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "fdcan8_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "fdcan8_gated_pclk" is enabled in M4 SLEEP mode. Note : M4FDCAN8EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	FDCAN3STPREQ	FDCAN3 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
14	FDCAN3STPACK	FDCAN3 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
13:12	Reserved	Reserved, the reset value must be maintained.
11	FDCAN4STPREQ	FDCAN4 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
10	FDCAN4STPACK	FDCAN4 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
9:8	Reserved	Reserved, the reset value must be maintained.
7	FDCAN7STPREQ	FDCAN7 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
6	FDCAN7STPACK	FDCAN7 Kernel and bus clock stop acknowledgement. 0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
5:4	Reserved	
3	FDCAN8STPREQ	FDCAN8 Kernel and bus clock stop request. 0: De-assert clock stop request. 1: Assert clock stop request.
2	FDCAN8STPACK	FDCAN8 Kernel and bus clock stop acknowledgement.

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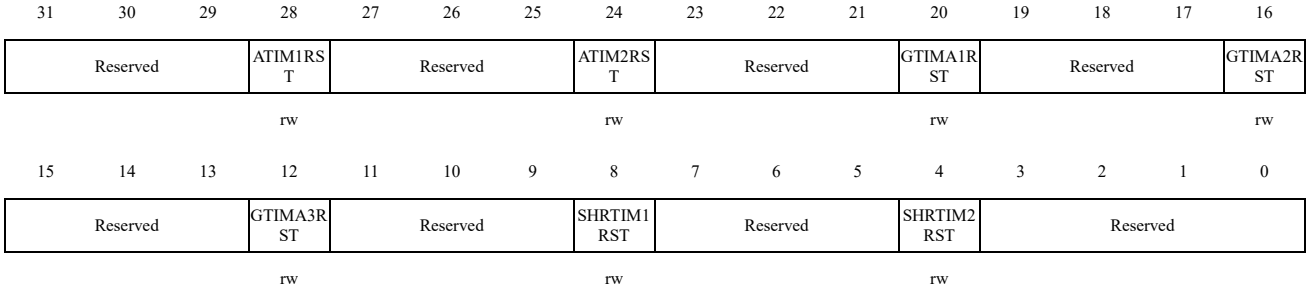
Bit field	Name	Description
		0: clock stop request is not acknowledged. 1: clock stop request is acknowledged.
1:0	Reserved	Reserved, the reset value must be maintained.

4.5.54 APB2 peripherals reset register 1(RCC_APB2RST1)

Address offset: 0x00d4

Reset value: 0x00000000



Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	ATIM1RST	ATIMER1 soft reset 0: Clear reset 1: Reset ATIMER1
27:25	Reserved	Reserved, the reset value must be maintained.
24	ATIM2RST	ATIMER2 soft reset 0: Clear reset 1: Reset ATIMER2
23:21	Reserved	Reserved, the reset value must be maintained.
20	GTIMA1RST	GTIMERA1 soft reset 0: Clear reset 1: Reset GTIMERA1
19:17	Reserved	Reserved, the reset value must be maintained.
16	GTIMA2RST	GTIMERA2 soft reset 0: Clear reset 1: Reset GTIMERA2
15:13	Reserved	Reserved, the reset value must be maintained.
12	GTIMA3RST	GTIMERA3 soft reset 0: Clear reset 1: Reset GTIMERA3
11:9	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
8	SHRTIM1RST	SHRTIMER1 soft reset 0: Clear reset 1: Reset SHRTIMER1
7:5	Reserved	Reserved, the reset value must be maintained.
4	SHRTIM2RST	SHRTIMER2 soft reset 0: Clear reset 1: Reset SHRTIMER2
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.55 APB2 peripherals reset register 2(RCC_APB2RST2)

Address offset: 0x00d8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			I2S1RST	Reserved			I2S2RST	Reserved			SPI1RST	Reserved			SPI2RST
			rw				rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			DSMURST	Reserved			I2C4RST	Reserved			I2C5RST	Reserved			I2C6RST
			rw				rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	I2S1RST	I2S1 soft reset 0: Clear reset 1: Reset I2S1
27:25	Reserved	Reserved, the reset value must be maintained.
24	I2S2RST	I2S2 soft reset 0: Clear reset 1: Reset I2S2
23:21	Reserved	Reserved, the reset value must be maintained.
20	SPI1RST	SPI1 soft reset 0: Clear reset 1: Reset SPI1
19:17	Reserved	Reserved, the reset value must be maintained.
16	SPI2RST	SPI2 soft reset 0: Clear reset 1: Reset SPI2

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Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained.
12	DSMURST	DSMU soft reset 0: Clear reset 1: Reset DSMU
11:9	Reserved	Reserved, the reset value must be maintained.
8	I2C4RST	I2C4 soft reset 0: Clear reset 1: Reset I2C4
7:5	Reserved	Reserved, the reset value must be maintained.
4	I2C5RST	I2C5 soft reset 0: Clear reset 1: Reset I2C5
3:1	Reserved	Reserved, the reset value must be maintained.
0	I2C6RST	I2C6 soft reset 0: Clear reset 1: Reset I2C6

4.5.56 APB2 peripherals reset register 3(RCC_APB2RST3)

Address offset: 0x00dc

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			USART5RST	Reserved			USART6RST	Reserved			USART7RST	Reserved			USART8RST
			rw				rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			UART13RST	Reserved			UART14RST	Reserved			UART15RST	Reserved			
			rw				rw				rw				

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	USART5RST	USART5 soft reset 0: Clear reset 1: Reset USART5
27:25	Reserved	Reserved, the reset value must be maintained.
24	USART6RST	USART6 soft reset 0: Clear reset 1: Reset USART6

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Bit field	Name	Description
23:21	Reserved	Reserved, the reset value must be maintained.
20	USART7RST	USART7 soft reset 0: Clear reset 1: Reset USART7
19:17	Reserved	Reserved, the reset value must be maintained.
16	USART8RST	USART8 soft reset 0: Clear reset 1: Reset USART8
15:13	Reserved	Reserved, the reset value must be maintained.
12	UART13RST	UART13 soft reset 0: Clear reset 1: Reset UART13
11:9	Reserved	Reserved, the reset value must be maintained.
8	UART14RST	UART14 soft reset 0: Clear reset 1: Reset UART14
7:5	Reserved	Reserved, the reset value must be maintained.
4	UART15RST	UART15 soft reset 0: Clear reset 1: Reset UART15
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.57 APB2 peripherals reset register 4(RCC_APB2RST4)

Address offset: 0x00e0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			FDCAN3RST	Reserved			FDCAN4RST	Reserved			FDCAN7RST	Reserved			FDCAN8RST
			rw				rw				rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	FDCAN3RST	FDCAN3 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset FDCAN3
27:25	Reserved	Reserved, the reset value must be maintained.
24	FDCAN4RST	FDCAN4 soft reset 0: Clear reset 1: Reset FDCAN4
23:21	Reserved	Reserved, the reset value must be maintained.
20	FDCAN7RST	FDCAN7 soft reset 0: Clear reset 1: Reset FDCAN7
19:17	Reserved	Reserved, the reset value must be maintained.
16	FDCAN8RST	FDCAN8 soft reset 0: Clear reset 1: Reset FDCAN8
15:0	Reserved	Reserved, the reset value must be maintained.

4.5.58 AHB5 peripherals clock enable register 1(RCC_AHB5EN1)

Address offset: 0x00e4

Reset value: 0x88880000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7GPIOAEN	M4GPIOAEN	M7GPIOALPEN	M4GPIOALPEN	M7GPIOBEN	M4GPIOBEN	M7GPIOBLPEN	M4GPIOBLPEN	M7GPIOCEN	M4GPIOCEN	M7GPIOCLPEN	M4GPIOCLPEN	M7GPIODEN	M4GPIODEN	M7GPIODLPEN	M4GPIODLPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7GPIOEEN	M4GPIOEEN	M7GPIOELPEN	M4GPIOELPEN	M7GPIOFEN	M4GPIOFEN	M7GPIOFLPEN	M4GPIOFLPEN	M7GPIOGEN	M4GPIOGEN	M7GPIOGLPEN	M4GPIOGLPEN	M7GPIOHEN	M4GPIOHEN	M7GPIOHLPEN	M4GPIOHLPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7GPIOAEN	GPIOA M7 allocation and clock enable. Set and cleared by software. 0: GPIOA is not allocated to M7. The "gpioa_gated_hclk" is disabled in M7 RUN mode. 1: GPIOA is allocated to M7. The "gpioa_gated_hclk" is enabled in M7 RUN mode.
30	M4GPIOAEN	GPIOA M4 allocation and clock enable. Set and cleared by software. 0: GPIOA is not allocated to M4. The "gpioa_gated_hclk" is disabled in M4 RUN mode. 1: GPIOA is allocated to M4. The "gpioa_gated_hclk" is enabled in M4 RUN mode.
29	M7GPIOALPEN	GPIOA M7 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "gpioa_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpioa_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOAEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4GPIOALPEN	GPIOA M4 Low Power clock Enable. Set and cleared by software. 0: The "gpioa_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpioa_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOAEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7GPIOBEN	GPIOB M7 allocation and clock enable. Set and cleared by software. 0: GPIOB is not allocated to M7. The "gpiob_gated_hclk" is disabled in M7 RUN mode. 1: GPIOB is allocated to M7. The "gpiob_gated_hclk" is enabled in M7 RUN mode.
26	M4GPIOBEN	GPIOB M4 allocation and clock enable. Set and cleared by software. 0: GPIOB is not allocated to M4. The "gpiob_gated_hclk" is disabled in M4 RUN mode. 1: GPIOB is allocated to M4. The "gpiob_gated_hclk" is enabled in M4 RUN mode.
25	M7GPIOBLPEN	GPIOB M7 Low Power clock Enable. Set and cleared by software. 0: The "gpiob_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpiob_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4GPIOBLPEN	GPIOB M4 Low Power clock Enable. Set and cleared by software. 0: The "gpiob_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpiob_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7GPIOCEN	GPIOC M7 allocation and clock enable. Set and cleared by software. 0: GPIOC is not allocated to M7. The "gpioc_gated_hclk" is disabled in M7 RUN mode. 1: GPIOC is allocated to M7. The "gpioc_gated_hclk" is enabled in M7 RUN mode.
22	M4GPIOCEN	GPIOC M4 allocation and clock enable. Set and cleared by software. 0: GPIOC is not allocated to M4. The "gpioc_gated_hclk" is disabled in M4 RUN mode. 1: GPIOC is allocated to M4. The "gpioc_gated_hclk" is enabled in M4 RUN mode.
21	M7GPIOCLPEN	GPIOC M7 Low Power clock Enable. Set and cleared by software. 0: The "gpioc_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpioc_gated_hclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7GPIOCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4GPIOCLPEN	GPIOC M4 Low Power clock Enable. Set and cleared by software. 0: The "gpioc_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpioc_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7GPIODEN	GPIOD M7 allocation and clock enable. Set and cleared by software. 0: GPIOD is not allocated to M7. The "gpiod_gated_hclk" is disabled in M7 RUN mode. 1: GPIOD is allocated to M7. The "gpiod_gated_hclk" is enabled in M7 RUN mode.
18	M4GPIODEN	GPIOD M4 allocation and clock enable. Set and cleared by software. 0: GPIOD is not allocated to M4. The "gpiod_gated_hclk" is disabled in M4 RUN mode. 1: GPIOD is allocated to M4. The "gpiod_gated_hclk" is enabled in M4 RUN mode.
17	M7GPIODLPEN	GPIOD M7 Low Power clock Enable. Set and cleared by software. 0: The "gpiod_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpiod_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIODEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4GPIODLPEN	GPIOD M4 Low Power clock Enable. Set and cleared by software. 0: The "gpiod_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpiod_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIODEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7GPIOEEN	GPIOE M7 allocation and clock enable. Set and cleared by software. 0: GPIOE is not allocated to M7. The "gpioe_gated_hclk" is disabled in M7 RUN mode. 1: GPIOE is allocated to M7. The "gpioe_gated_hclk" is enabled in M7 RUN mode.
14	M4GPIOEEN	GPIOE M4 allocation and clock enable. Set and cleared by software. 0: GPIOE is not allocated to M4. The "gpioe_gated_hclk" is disabled in M4 RUN mode. 1: GPIOE is allocated to M4. The "gpioe_gated_hclk" is enabled in M4 RUN mode.
13	M7GPIOELPEN	GPIOE M7 Low Power clock Enable. Set and cleared by software. 0: The "gpioe_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpioe_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOEEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Bit field	Name	Description
12	M4GPIOELPEN	GPIOE M4 Low Power clock Enable. Set and cleared by software. 0: The "gpioe_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpioe_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOEEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7GPIOFEN	GPIOF M7 allocation and clock enable. Set and cleared by software. 0: GPIOF is not allocated to M7. The "gpiof_gated_hclk" is disabled in M7 RUN mode. 1: GPIOF is allocated to M7. The "gpiof_gated_hclk" is enabled in M7 RUN mode.
10	M4GPIOFEN	GPIOF M4 allocation and clock enable. Set and cleared by software. 0: GPIOF is not allocated to M4. The "gpiof_gated_hclk" is disabled in M4 RUN mode. 1: GPIOF is allocated to M4. The "gpiof_gated_hclk" is enabled in M4 RUN mode.
9	M7GPIOFLPEN	GPIOF M7 Low Power clock Enable. Set and cleared by software. 0: The "gpiof_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpiof_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOFEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4GPIOFLPEN	GPIOF M4 Low Power clock Enable. Set and cleared by software. 0: The "gpiof_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpiof_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOFEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7GPIOGEN	GPIOG M7 allocation and clock enable. Set and cleared by software. 0: GPIOG is not allocated to M7. The "gpiog_gated_hclk" is disabled in M7 RUN mode. 1: GPIOG is allocated to M7. The "gpiog_gated_hclk" is enabled in M7 RUN mode.
6	M4GPIOGEN	GPIOG M4 allocation and clock enable. Set and cleared by software. 0: GPIOG is not allocated to M4. The "gpiog_gated_hclk" is disabled in M4 RUN mode. 1: GPIOG is allocated to M4. The "gpiog_gated_hclk" is enabled in M4 RUN mode.
5	M7GPIOGLPEN	GPIOG M7 Low Power clock Enable. Set and cleared by software. 0: The "gpiog_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpiog_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOGEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4GPIOGLPEN	GPIOG M4 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "gpiog_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpiog_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOGEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7GPIOHEN	GPIOH M7 allocation and clock enable. Set and cleared by software. 0: GPIOH is not allocated to M7. The "gpioh_gated_hclk" is disabled in M7 RUN mode. 1: GPIOH is allocated to M7. The "gpioh_gated_hclk" is enabled in M7 RUN mode.
2	M4GPIOHEN	GPIOH M4 allocation and clock enable. Set and cleared by software. 0: GPIOH is not allocated to M4. The "gpioh_gated_hclk" is disabled in M4 RUN mode. 1: GPIOH is allocated to M4. The "gpioh_gated_hclk" is enabled in M4 RUN mode.
1	M7GPIOHLPEN	GPIOH M7 Low Power clock Enable. Set and cleared by software. 0: The "gpioh_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpioh_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOHEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4GPIOHLPEN	GPIOH M4 Low Power clock Enable. Set and cleared by software. 0: The "gpioh_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpioh_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOHEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.59 AHB5 peripherals clock enable register 2(RCC_AHB5EN2)

Address offset: 0x00e8

Reset value: 0x00000008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7GPIOIEN	M4GPIOIEN	M7GPIOILPEN	M4GPIOILPEN	M7GPIOJEN	M4GPIOJEN	M7GPIOJLPEN	M4GPIOJLPEN	M7GPIOKEN	M4GPIOKEN	M7GPIOKLPEN	M4GPIOKLPEN	M7ECCM3EN	M4ECCM3EN	M7ECCM3LPEN	M4ECCM3LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWREN	Reserved	PWRLPEN	Reserved	M7CRCEN	M4CRCEN	M7CRCLPEN	M4CRCLPEN	M7SEMA4EN	M4SEMA4EN	M7SEMA4LPEN	M4SEMA4LPEN	M7AFIOEN	M4AFIOEN	M7AFIOLPEN	M4AFIOLPEN
rw		rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31	M7GPIOIEN	GPIOI M7 allocation and clock enable. Set and cleared by software. 0: GPIOI is not allocated to M7. The "gpioi_gated_hclk" is disabled in M7 RUN mode. 1: GPIOI is allocated to M7. The "gpioi_gated_hclk" is enabled in M7 RUN mode.
30	M4GPIOIEN	GPIOI M4 allocation and clock enable. Set and cleared by software. 0: GPIOI is not allocated to M4. The "gpioi_gated_hclk" is disabled in M4 RUN mode. 1: GPIOI is allocated to M4. The "gpioi_gated_hclk" is enabled in M4 RUN mode.
29	M7GPIOILPEN	GPIOI M7 Low Power clock Enable. Set and cleared by software. 0: The "gpioi_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpioi_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4GPIOILPEN	GPIOI M4 Low Power clock Enable. Set and cleared by software. 0: The "gpioi_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpioi_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7GPIOJEN	GPIOJ M7 allocation and clock enable. Set and cleared by software. 0: GPIOJ is not allocated to M7. The "gpioj_gated_hclk" is disabled in M7 RUN mode. 1: GPIOJ is allocated to M7. The "gpioj_gated_hclk" is enabled in M7 RUN mode.
26	M4GPIOJEN	GPIOJ M4 allocation and clock enable. Set and cleared by software. 0: GPIOJ is not allocated to M4. The "gpioj_gated_hclk" is disabled in M4 RUN mode. 1: GPIOJ is allocated to M4. The "gpioj_gated_hclk" is enabled in M4 RUN mode.
25	M7GPIOJLPEN	GPIOJ M7 Low Power clock Enable. Set and cleared by software. 0: The "gpioj_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpioj_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOJEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4GPIOJLPEN	GPIOJ M4 Low Power clock Enable. Set and cleared by software. 0: The "gpioj_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpioj_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOJEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7GPIOKEN	GPIOK M7 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: GPIOK is not allocated to M7. The "gpiok_gated_hclk" is disabled in M7 RUN mode. 1: GPIOK is allocated to M7. The "gpiok_gated_hclk" is enabled in M7 RUN mode.
22	M4GPIOKEN	GPIOK M4 allocation and clock enable. Set and cleared by software. 0: GPIOK is not allocated to M4. The "gpiok_gated_hclk" is disabled in M4 RUN mode. 1: GPIOK is allocated to M4. The "gpiok_gated_hclk" is enabled in M4 RUN mode.
21	M7GPIOKLPEN	GPIOK M7 Low Power clock Enable. Set and cleared by software. 0: The "gpiok_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "gpiok_gated_hclk" is enabled in M7 SLEEP mode. Note : M7GPIOKEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4GPIOKLPEN	GPIOK M4 Low Power clock Enable. Set and cleared by software. 0: The "gpiok_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "gpiok_gated_hclk" is enabled in M4 SLEEP mode. Note : M4GPIOKEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7ECCM3EN	ECCMON3 M7 allocation and clock enable. Set and cleared by software. 0: ECCMON3 is not allocated to M7. The "eccmon3_gated_hclk" is disabled in M7 RUN mode. 1: ECCMON3 is allocated to M7. The "eccmon3_gated_hclk" is enabled in M7 RUN mode.
18	M4ECCM3EN	ECCMON3 M4 allocation and clock enable. Set and cleared by software. 0: ECCMON3 is not allocated to M4. The "eccmon3_gated_hclk" is disabled in M4 RUN mode. 1: ECCMON3 is allocated to M4. The "eccmon3_gated_hclk" is enabled in M4 RUN mode.
17	M7ECCM3LPEN	ECCMON3 M7 Low Power clock Enable. Set and cleared by software. 0: The "eccmon3_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "eccmon3_gated_hclk" is enabled in M7 SLEEP mode. Note : M7ECCM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4ECCM3LPEN	ECCMON3 M4 Low Power clock Enable. Set and cleared by software. 0: The "eccmon3_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "eccmon3_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ECCM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	PWREN	PWR AHB clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "pwr_gated_hclk" is disabled. 1: The "pwr_gated_hclk" is enabled.
14	Reserved	Reserved, the reset value must be maintained.
13	PWRLPEN	PWR M7 Low Power clock Enable. Set and cleared by software. 0: The "pwr_gated_hclk" clocks is disabled in SLEEP. 1: The "pwr_gated_hclk" is enabled in SLEEP mode. Note : PWREN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	Reserved	Reserved, the reset value must be maintained.
11	M7CRCEN	CRC M7 allocation and clock enable. Set and cleared by software. 0: CRC is not allocated to M7. The "crc_gated_hclk" is disabled in M7 RUN mode. 1: CRC is allocated to M7. The "crc_gated_hclk" is enabled in M7 RUN mode.
10	M4CRCEN	CRC M4 allocation and clock enable. Set and cleared by software. 0: CRC is not allocated to M4. The "crc_gated_hclk" is disabled in M4 RUN mode. 1: CRC is allocated to M4. The "crc_gated_hclk" is enabled in M4 RUN mode.
9	M7CRCLPEN	CRC M7 Low Power clock Enable. Set and cleared by software. 0: The "crc_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "crc_gated_hclk" is enabled in M7 SLEEP mode. Note : M7CRCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4CRCLPEN	CRC M4 Low Power clock Enable. Set and cleared by software. 0: The "crc_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "crc_gated_hclk" is enabled in M4 SLEEP mode. Note : M4CRCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7SEMA4EN	SEMA4 M7 allocation and clock enable. Set and cleared by software. 0: SEMA4 is not allocated to M7. The "sema4_gated_hclk" is disabled in M7 RUN mode. 1: SEMA4 is allocated to M7. The "sema4_gated_hclk" is enabled in M7 RUN mode.
6	M4SEMA4EN	SEMA4 M4 allocation and clock enable. Set and cleared by software. 0: SEMA4 is not allocated to M4. The "sema4_gated_hclk" is disabled in M4 RUN mode. 1: SEMA4 is allocated to M4. The "sema4_gated_hclk" is enabled in M4 RUN mode.
5	M7SEMA4LPEN	SEMA4 M7 Low Power clock Enable. Set and cleared by software. 0: The "sema4_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "sema4_gated_hclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7SEMA4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4SEMA4LPEN	SEMA4 M4 Low Power clock Enable. Set and cleared by software. 0: The "sema4_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "sema4_gated_hclk" is enabled in M4 SLEEP mode. Note : M4SEMA4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7AFIOEN	AFIO M7 allocation and clock enable. Set and cleared by software. 0: AFIO is not allocated to M7. The "afio_gated_hclk" is disabled in M7 RUN mode. 1: AFIO is allocated to M7. The "afio_gated_hclk" is enabled in M7 RUN mode.
2	M4AFIOEN	AFIO M4 allocation and clock enable. Set and cleared by software. 0: AFIO is not allocated to M4. The "afio_gated_hclk" is disabled in M4 RUN mode. 1: AFIO is allocated to M4. The "afio_gated_hclk" is enabled in M4 RUN mode.
1	M7AFIOLPEN	AFIO M7 Low Power clock Enable. Set and cleared by software. 0: The "afio_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "afio_gated_hclk" is enabled in M7 SLEEP mode. Note : M7AFIOEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4AFIOLPEN	AFIO M4 Low Power clock Enable. Set and cleared by software. 0: The "afio_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "afio_gated_hclk" is enabled in M4 SLEEP mode. Note : M4AFIOEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.60 AHB5 peripherals reset register 1(RCC_AHB5RST1)

Address offset: 0x00ec

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			GPIOARST	Reserved			GPIOBRST	Reserved			GPIOCRST	Reserved			GPIODRST
			rw				rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			GPIOERST	Reserved			GPIOFRST	Reserved			GPIOGRST	Reserved			GPIOHRST

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rw rw rw rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	GPIOARST	GPIOA soft reset 0: Clear reset 1: Reset GPIOA
27:25	Reserved	Reserved, the reset value must be maintained.
24	GPIOBRST	GPIOB soft reset 0: Clear reset 1: Reset GPIOB
23:21	Reserved	Reserved, the reset value must be maintained.
20	GPIOCRST	GPIOC soft reset 0: Clear reset 1: Reset GPIOC
19:17	Reserved	Reserved, the reset value must be maintained.
16	GPIODRST	GPIOD soft reset 0: Clear reset 1: Reset GPIOD
15:13	Reserved	Reserved, the reset value must be maintained.
12	GPIOERST	GPIOE soft reset 0: Clear reset 1: Reset GPIOE
11:9	Reserved	Reserved, the reset value must be maintained.
8	GPIOFRST	GPIOF soft reset 0: Clear reset 1: Reset GPIOF
7:5	Reserved	Reserved, the reset value must be maintained.
4	GPIOGRST	GPIOG soft reset 0: Clear reset 1: Reset GPIOG
3:1	Reserved	Reserved, the reset value must be maintained.
0	GPIOHRST	GPIOH soft reset 0: Clear reset 1: Reset GPIOH

4.5.61 AHB5 peripherals reset register 2(RCC_AHB5RST2)

Address offset: 0x00f0

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			GPIOIRST	Reserved			GPIOJRST	Reserved			GPIOKRST	Reserved			ECCM3RST
			rw				rw				rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PWRRST	Reserved			CRCRST	Reserved			SEMA4RST	Reserved			AFIORST
			rw				rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	GPIOIRST	GPIOA soft reset 0: Clear reset 1: Reset GPIOA
27:25	Reserved	Reserved, the reset value must be maintained.
24	GPIOJRST	GPIOJ soft reset 0: Clear reset 1: Reset GPIOJ
23:21	Reserved	Reserved, the reset value must be maintained.
20	GPIOKRST	GPIOK soft reset 0: Clear reset 1: Reset GPIOK
19:17	Reserved	Reserved, the reset value must be maintained.
16	ECCM3RST	ECCMON3 soft reset 0: Clear reset 1: Reset ECCMON3
15:13	Reserved	Reserved, the reset value must be maintained.
12	PWRRST	PWR soft reset 0: Clear reset 1: Reset PWR
11:9	Reserved	Reserved, the reset value must be maintained.
8	CRCRST	CRC soft reset 0: Clear reset 1: Reset CRC
7:5	Reserved	Reserved, the reset value must be maintained.
4	SEMA4RST	SEMA4 soft reset 0: Clear reset 1: Reset SEMA4
3:1	Reserved	Reserved, the reset value must be maintained.
0	AFIORST	AFIO soft reset 0: Clear reset 1: Reset AFIO

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4.5.62 APB5 peripherals clock divider register 1(RCC_APB5DIV1)

Address offset: 0x00f4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	APB5ATIMDIV[2:0]			Reserved	APB5I2CDIV[2:0]			Reserved	APB5EXTIDIV[2:0]			Reserved			
	rw				rw				rw						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	APB5ATIMDIV[2:0]	APB5 Atimer clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
27	Reserved	Reserved, the reset value must be maintained.
26:24	APB5I2CDIV[2:0]	APB5 I2C clock prescalar values Effective when "I2C(n)KERSEL" is selected as 3’b000. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
23	Reserved	Reserved, the reset value must be maintained.
22:20	APB5EXTIDIV[2:0]	APB5 EXTI clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
19:0	Reserved	Reserved, the reset value must be maintained.

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4.5.63 APB5 peripherals clock source select register 1(RCC_APB5SEL1)

Address offset: 0x00f8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	I2C7KERSEL[2:0]			Reserved	I2C8KERSEL[2:0]			Reserved	I2C9KERSEL[2:0]			Reserved	I2C10KERSEL[2:0]		
	rw				rw				rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	I2C7KERSEL[2:0]	I2C7 Kernel clock selection. 000: Divided system bus clock is selected as "i2c7_ker_gated_clk". 001: PLL3_c clock is selected as "i2c7_ker_gated_clk". 010: HSI clock is selected as "i2c7_ker_gated_clk". 011: MSI clock is selected as "i2c7_ker_gated_clk". Other values: setting is not allowed
27	Reserved	Reserved, the reset value must be maintained.
26:24	I2C8KERSEL[2:0]	I2C8 Kernel clock selection. 000: Divided system bus clock is selected as "i2c8_ker_gated_clk". 001: PLL3_c clock is selected as "i2c8_ker_gated_clk". 010: HSI clock is selected as "i2c8_ker_gated_clk". 011: MSI clock is selected as "i2c8_ker_gated_clk". Other values: setting is not allowed
23	Reserved	Reserved, the reset value must be maintained.
22:20	I2C9KERSEL[2:0]	I2C9 Kernel clock selection. 000: Divided system bus clock is selected as "i2c9_ker_gated_clk". 001: PLL3_c clock is selected as "i2c9_ker_gated_clk". 010: HSI clock is selected as "i2c9_ker_gated_clk". 011: MSI clock is selected as "i2c9_ker_gated_clk". Other values: setting is not allowed
19	Reserved	Reserved, the reset value must be maintained.
18:16	I2C10KERSEL[2:0]	I2C10 Kernel clock selection. 000: Divided system bus clock is selected as "i2c10_ker_gated_clk". 001: PLL3_c clock is selected as "i2c10_ker_gated_clk". 010: HSI clock is selected as "i2c10_ker_gated_clk". 011: MSI clock is selected as "i2c10_ker_gated_clk".

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Bit field	Name	Description
		Other values: setting is not allowed
15:0	Reserved	Reserved, the reset value must be maintained.

4.5.64 APB5 peripherals clock enable register 1(RCC_APB5EN1)

Address offset: 0x00fc

Reset value: 0x00800000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7ATIM3EN	M4ATIM3EN	M7ATIM3LPEN	M4ATIM3LPEN	M7ATIM4EN	M4ATIM4EN	M7ATIM4LPEN	M4ATIM4LPEN	M7AFECEN	M4AFECEN	M7AFECLPEN	M4AFECLPEN	Reserved			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7SPI4EN	M4SPI4EN	M7SPI4LPEN	M4SPI4LPEN	M7SPI5EN	M4SPI5EN	M7SPI5LPEN	M4SPI5LPEN	M7SPI6EN	M4SPI6EN	M7SPI6LPEN	M4SPI6LPEN	M7SPI7EN	M4SPI7EN	M7SPI7LPEN	M4SPI7LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7ATIM3EN	ATIMER3 M7 allocation and clock enable. Set and cleared by software. 0: ATIMER3 is not allocated to M7. The "atimer3_gated_ker_clk" and "atimer3_gated_pclk" are disabled in M7 RUN mode. 1: ATIMER3 is allocated to M7. The "atimer3_gated_ker_clk" and "atimer3_gated_pclk" are enabled in M7 RUN mode.
30	M4ATIM3EN	ATIMER3 M4 allocation and clock enable. Set and cleared by software. 0: ATIMER3 is not allocated to M4. The "atimer3_gated_ker_clk" and "atimer3_gated_pclk" are disabled in M4 RUN mode. 1: ATIMER3 is allocated to M4. The "atimer3_gated_ker_clk" and "atimer3_gated_pclk" are enabled in M4 RUN mode.
29	M7ATIM3LPEN	ATIMER3 M7 Low Power clock Enable. Set and cleared by software. 0: The "atimer3_gated_ker_clk" and "atimer3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "atimer3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "atimer3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7ATIM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4ATIM3LPEN	ATIMER3 M4 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The "atimer3_gated_ker_clk" and "atimer3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "atimer3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "atimer3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4ATIM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7ATIM4EN	ATIMER4 M7 allocation and clock enable. Set and cleared by software. 0: ATIMER4 is not allocated to M7. The "atimer4_gated_ker_clk" and "atimer4_gated_pclk" are disabled in M7 RUN mode. 1: ATIMER4 is allocated to M7. The "atimer4_gated_ker_clk" and "atimer4_gated_pclk" are enabled in M7 RUN mode.
26	M4ATIM4EN	ATIMER4 M4 allocation and clock enable. Set and cleared by software. 0: ATIMER4 is not allocated to M4. The "atimer4_gated_ker_clk" and "atimer4_gated_pclk" are disabled in M4 RUN mode. 1: ATIMER4 is allocated to M4. The "atimer4_gated_ker_clk" and "atimer4_gated_pclk" are enabled in M4 RUN mode.
25	M7ATIM4LPEN	ATIMER4 M7 Low Power clock Enable. Set and cleared by software. 0: The "atimer4_gated_ker_clk" and "atimer4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "atimer4_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "atimer4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7ATIM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4ATIM4LPEN	ATIMER4 M4 Low Power clock Enable. Set and cleared by software. 0: The "atimer4_gated_ker_clk" and "atimer4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "atimer4_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "atimer4_gated_pclk" is enabled in M4 SLEEP mode. Note : M4ATIM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7AFECEN	AFEC M7 allocation and clock enable. Set and cleared by software. 0: AFEC is not allocated to M7. The "afec_gated_pclk" is disabled in M7 RUN mode. 1: AFEC is allocated to M7. The "afec_gated_pclk" is enabled in M7 RUN mode.
22	M4AFECEN	AFEC M4 allocation and clock enable. Set and cleared by software. 0: AFEC is not allocated to M4. The "afec_gated_pclk" is disabled in M4 RUN mode. 1: AFEC is allocated to M4. The "afec_gated_pclk" is enabled in M4 RUN mode.

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Bit field	Name	Description
21	M7AFECLPEN	AFEC M7 Low Power clock Enable. Set and cleared by software. 0: The "afec_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "afec_gated_pclk" is enabled in M7 SLEEP mode. Note : M7AFECEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4AFECLPEN	AFEC M4 Low Power clock Enable. Set and cleared by software. 0: The "afec_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "afec_gated_pclk" is enabled in M4 SLEEP mode. Note : M4AFECEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19:16	Reserved	Reserved, the reset value must be maintained.
15	M7SPI4EN	SPI4 M7 allocation and clock enable. Set and cleared by software. 0: SPI4 is not allocated to M7. The " spi4_gated_ker_clk" and "spi4_gated_pclk" are disabled in M7 RUN mode. 1: SPI4 is allocated to M7. The " spi4_gated_ker_clk" and "spi4_gated_pclk" are enabled in M7 RUN mode.
14	M4SPI4EN	SPI4 M4 allocation and clock enable. Set and cleared by software. 0: SPI4 is not allocated to M4. The " spi4_gated_ker_clk" and "spi4_gated_pclk" are disabled in M4 RUN mode. 1: SPI4 is allocated to M4. The " spi4_gated_ker_clk" and "spi4_gated_pclk" are enabled in M4 RUN mode.
13	M7SPI4LPEN	SPI4 M7 Low Power clock Enable. Set and cleared by software. 0: The " spi4_gated_ker_clk" and "spi4_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi4_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4SPI4LPEN	SPI4 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi4_gated_ker_clk" and "spi4_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi4_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi4_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SPI4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7SPI5EN	SPI5 M7 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: SPI5 is not allocated to M7. The " spi5_gated_ker_clk" and "spi5_gated_pclk" are disabled in M7 RUN mode. 1: SPI5 is allocated to M7. The " spi5_gated_ker_clk" and "spi5_gated_pclk" are enabled in M7 RUN mode.
10	M4SPI5EN	SPI5 M4 allocation and clock enable. Set and cleared by software. 0: SPI5 is not allocated to M4. The " spi5_gated_ker_clk" and "spi5_gated_pclk" are disabled in M4 RUN mode. 1: SPI5 is allocated to M4. The " spi5_gated_ker_clk" and "spi5_gated_pclk" are enabled in M4 RUN mode.
9	M7SPI5LPEN	SPI5 M7 Low Power clock Enable. Set and cleared by software. 0: The " spi5_gated_ker_clk" and "spi5_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi5_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi5_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4SPI5LPEN	SPI5 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi5_gated_ker_clk" and "spi5_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi5_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi5_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SPI5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7SPI6EN	SPI6 M7 allocation and clock enable. Set and cleared by software. 0: SPI6 is not allocated to M7. The " spi6_gated_ker_clk" and "spi6_gated_pclk" are disabled in M7 RUN mode. 1: SPI6 is allocated to M7. The " spi6_gated_ker_clk" and "spi6_gated_pclk" are enabled in M7 RUN mode.
6	M4SPI6EN	SPI6 M4 allocation and clock enable. Set and cleared by software. 0: SPI6 is not allocated to M4. The " spi6_gated_ker_clk" and "spi6_gated_pclk" are disabled in M4 RUN mode. 1: SPI6 is allocated to M4. The " spi6_gated_ker_clk" and "spi6_gated_pclk" are enabled in M4 RUN mode.
5	M7SPI6LPEN	SPI6 M7 Low Power clock Enable. Set and cleared by software.

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Bit field	Name	Description
		0: The " spi6_gated_ker_clk" and "spi6_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi6_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi6_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4SPI6LPEN	SPI6 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi6_gated_ker_clk" and "spi6_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi6_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi6_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SPI6EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7SPI7EN	SPI7 M7 allocation and clock enable. Set and cleared by software. 0: SPI7 is not allocated to M7. The " spi7_gated_ker_clk" and "spi7_gated_pclk" are disabled in M7 RUN mode. 1: SPI7 is allocated to M7. The " spi7_gated_ker_clk" and "spi7_gated_pclk" are enabled in M7 RUN mode.
2	M4SPI7EN	SPI7 M4 allocation and clock enable. Set and cleared by software. 0: SPI7 is not allocated to M4. The " spi7_gated_ker_clk" and "spi7_gated_pclk" are disabled in M4 RUN mode. 1: SPI7 is allocated to M4. The " spi7_gated_ker_clk" and "spi7_gated_pclk" are enabled in M4 RUN mode.
1	M7SPI7LPEN	SPI7 M7 Low Power clock Enable. Set and cleared by software. 0: The " spi7_gated_ker_clk" and "spi7_gated_pclk" are disabled in M7 SLEEP and STOP mode. 1: The "spi7_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "spi7_gated_pclk" is enabled in M7 SLEEP mode. Note : M7SPI7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4SPI7LPEN	SPI7 M4 Low Power clock Enable. Set and cleared by software. 0: The " spi7_gated_ker_clk" and "spi7_gated_pclk" are disabled in M4 SLEEP and STOP mode. 1: The "spi7_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "spi7_gated_pclk" is enabled in M4 SLEEP mode. Note : M4SPI7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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4.5.65 APB5 peripherals clock enable register 2(RCC_APB5EN2)

Address offset: 0x0100

Reset value: 0x00008000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7I2C7EN	M4I2C7EN	M7I2C7LPEN	M4I2C7LPEN	M7I2C8EN	M4I2C8EN	M7I2C8LPEN	M4I2C8LPEN	M7I2C9EN	M4I2C9EN	M7I2C9LPEN	M4I2C9LPEN	M7I2C10EN	M4I2C10EN	M7I2C10LPEN	M4I2C10LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTIEN	Reserved	EXTILPEN	Reserved	M7RTCPCLKEN	M4RTCPCLKEN	M7RTCPCLKLPEN	M4RTCPCLKLPEN	IWDG1PCLKEN	Reserved	IWDG1PCLKLPEN	Reserved	IWDG2PCLKEN	Reserved	IWDG2PCLKLPEN	Reserved
rw		rw		rw	rw	rw	rw	rw		rw		rw		rw	

Bit field	Name	Description
31	M7I2C7EN	I2C7 M7 allocation and clock enable. Set and cleared by software. 0: I2C7 is not allocated to M7. The "i2c7_ker_gated_clk" and "i2c7_gated_pclk" are disabled in M7 RUN mode. 1: I2C7 is allocated to M7. The "i2c7_ker_gated_clk" and "i2c7_gated_pclk" are enabled in M7 RUN mode.
30	M4I2C7EN	I2C7 M4 allocation and clock enable. Set and cleared by software. 0: I2C7 is not allocated to M4. The "i2c7_ker_gated_clk" and "i2c7_gated_pclk" are disabled in M4 RUN mode. 1: I2C7 is allocated to M4. The "i2c7_ker_gated_clk" and "i2c7_gated_pclk" are enabled in M4 RUN mode.
29	M7I2C7LPEN	I2C7 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c7_ker_gated_clk" and "i2c7_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c7_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c7_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4I2C7LPEN	I2C7 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c7_ker_gated_clk" and "i2c7_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c7_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c7_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4I2C7EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7I2C8EN	I2C8 M7 allocation and clock enable. Set and cleared by software. 0: I2C8 is not allocated to M7. The "i2c8_ker_gated_clk" and "i2c8_gated_pclk" are disabled in M7 RUN mode. 1: I2C8 is allocated to M7. The "i2c8_ker_gated_clk" and "i2c8_gated_pclk" are enabled in M7 RUN mode.
26	M4I2C8EN	I2C8 M4 allocation and clock enable. Set and cleared by software. 0: I2C8 is not allocated to M4. The "i2c8_ker_gated_clk" and "i2c8_gated_pclk" are disabled in M4 RUN mode. 1: I2C8 is allocated to M4. The "i2c8_ker_gated_clk" and "i2c8_gated_pclk" are enabled in M4 RUN mode.
25	M7I2C8LPEN	I2C8 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c8_ker_gated_clk" and "i2c8_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c8_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c8_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C8EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4I2C8LPEN	I2C8 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c8_ker_gated_clk" and "i2c8_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c8_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c8_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C8EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7I2C9EN	I2C9 M7 allocation and clock enable. Set and cleared by software. 0: I2C9 is not allocated to M7. The "i2c9_ker_gated_clk" and "i2c9_gated_pclk" are disabled in M7 RUN mode. 1: I2C9 is allocated to M7. The "i2c9_ker_gated_clk" and "i2c9_gated_pclk" are enabled in M7 RUN mode.
22	M4I2C9EN	I2C9 M4 allocation and clock enable. Set and cleared by software. 0: I2C9 is not allocated to M4. The "i2c9_ker_gated_clk" and "i2c9_gated_pclk" are disabled in M4 RUN mode. 1: I2C9 is allocated to M4. The "i2c9_ker_gated_clk" and "i2c9_gated_pclk" are enabled in M4 RUN mode.

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Bit field	Name	Description
21	M7I2C9LPEN	I2C9 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c9_ker_gated_clk" and "i2c9_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c9_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c9_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C9EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4I2C9LPEN	I2C9 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c9_ker_gated_clk" and "i2c9_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c9_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c9_gated_pclk" is enabled in M4 SLEEP mode. Note : M4I2C9EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7I2C10EN	I2C10 M7 allocation and clock enable. Set and cleared by software. 0: I2C10 is not allocated to M7. The "i2c10_ker_gated_clk" and "i2c9_gated_pclk" are disabled in M7 RUN mode. 1: I2C10 is allocated to M7. The "i2c10_ker_gated_clk" and "i2c9_gated_pclk" are enabled in M7 RUN mode.
18	M4I2C10EN	I2C10 M4 allocation and clock enable. Set and cleared by software. 0: I2C10 is not allocated to M4. The "i2c10_ker_gated_clk" and "i2c10_gated_pclk" are disabled in M4 RUN mode. 1: I2C10 is allocated to M4. The "i2c10_ker_gated_clk" and "i2c10_gated_pclk" are enabled in M4 RUN mode.
17	M7I2C10LPEN	I2C10 M7 Low Power clock Enable. Set and cleared by software. 0: The "i2c10_ker_gated_clk" and "i2c10_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "i2c10_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. "i2c10_gated_pclk" is enabled in M7 SLEEP mode. Note : M7I2C10EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4I2C10LPEN	I2C10 M4 Low Power clock Enable. Set and cleared by software. 0: The "i2c10_ker_gated_clk" and "i2c10_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "i2c10_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. "i2c10_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4I2C10EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	EXTIEN	EXTI clock enable. Set and cleared by software. 0: "exti_gated_pclk" is disabled. 1: "exti_gated_pclk" is enabled.
14	Reserved	Reserved, the reset value must be maintained.
13	EXTILPEN	EXTI Low Power clock Enable. Set and cleared by software. 0: The "exti_gated_pclk" clock is disabled insleep and STOP mode. 1: The "exti_gated_pclk" is enabled in M7/M4 SLEEP mode. Note : EXTIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	Reserved	Reserved, the reset value must be maintained.
11	M7RTCPCLKEN	RTCPCLK M7 allocation and clock enable. Set and cleared by software. 0: RTC APB clock is not allocated to M7. The "rtc_gated_pclk" is disabled in M7 RUN mode. 1: RTC APB clock is allocated to M7. The "rtc_gated_pclk" is enabled in M7 RUN mode.
10	M4RTCPCLKEN	RTCPCLK M4 allocation and clock enable. Set and cleared by software. 0: RTC APB clock is not allocated to M4. The "rtc_gated_pclk" is disabled in M4 RUN mode. 1: RTC APB clock is allocated to M4. The "rtc_gated_pclk" is enabled in M4 RUN mode.
9	M7RTCPCLKLPEN	RTCPCLK M7 Low Power clock Enable. Set and cleared by software. 0: The "rtc_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "rtc_gated_pclk" is enabled in M7 SLEEP mode. Note : M7RTCPCLKEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4RTCPCLKLPEN	RTCPCLK M4 Low Power clock Enable. Set and cleared by software. 0: The "rtc_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "rtc_gated_pclk" is enabled in M4 SLEEP mode. Note : M4RTCPCLKEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	IWDG1PCLKEN	IWDG1 APB clock enable. Set and cleared by software. 0: The "iwdg1_gated_pclk" is disabled. 1: The "iwdg1_gated_pclk" is enabled.
6	Reserved	Reserved, the reset value must be maintained.
5	IWDG1PCLKLPEN	IWDG1 Low Power APB clock Enable. Set and cleared by software. 0: The "iwdg1_gated_pclk" clock is disabled in SLEEP mode.

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Bit field	Name	Description
		1: The "iwdg1_gated_pclk" is enabled in SLEEP mode. Note : IWDG1PCLKEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	Reserved	Reserved, the reset value must be maintained.
3	IWDG2PCLKEN	IWDG2 APB clock enable. Set and cleared by software. 0: The "iwdg2_gated_pclk" is disabled. 1: The "iwdg2_gated_pclk" is enabled.
2	Reserved	Reserved, the reset value must be maintained.
1	IWDG2PCLKLPEN	IWDG2 Low Power APB clock Enable. Set and cleared by software. 0: The "iwdg2_gated_pclk" clock is disabled in SLEEP mode. 1: The "iwdg2_gated_pclk" is enabled in SLEEP mode. Note : IWDG2PCLKEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	Reserved	Reserved, the reset value must be maintained.

4.5.66 APB5 peripherals reset register 1(RCC_APB5RST1)

Address offset: 0x00104

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			ATIM3RST	Reserved			ATIM4RST	Reserved							
			rw				rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			SPI4RST	Reserved			SPI5RST	Reserved			SPI6RST	Reserved			SPI7RST
			rw				rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	ATIM3RST	ATIMER3 soft reset 0: Clear reset 1: Reset ATIMER3
27:25	Reserved	Reserved, the reset value must be maintained.
24	ATIM4RST	ATIMER4 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset ATIMER4
23:13	Reserved	Reserved, the reset value must be maintained.
12	SPI4RST	SPI4 soft reset 0: Clear reset 1: Reset SPI4
11:9	Reserved	Reserved, the reset value must be maintained.
8	SPI5RST	SPI5 soft reset 0: Clear reset 1: Reset SPI5
7:5	Reserved	Reserved, the reset value must be maintained.
4	SPI6RST	SPI6 soft reset 0: Clear reset 1: Reset SPI6
3:1	Reserved	Reserved, the reset value must be maintained.
0	SPI7RST	SPI7 soft reset 0: Clear reset 1: Reset SPI7

4.5.67 APB5 peripherals reset register 2(RCC_APB5RST2)

Address offset: 0x00108

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			I2C7RST	Reserved			I2C8RST	Reserved			I2C9RST	Reserved			I2C10RST
			rw				rw				rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	I2C7RST	I2C7 soft reset 0: Clear reset 1: Reset I2C7
27:25	Reserved	Reserved, the reset value must be maintained.
24	I2C8RST	I2C8 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset I2C8
23:21	Reserved	Reserved, the reset value must be maintained.
20	I2C9RST	I2C9 soft reset 0: Clear reset 1: Reset I2C9
19:17	Reserved	Reserved, the reset value must be maintained.
16	I2C10RST	I2C10 soft reset 0: Clear reset 1: Reset I2C10
15:0	Reserved	Reserved, the reset value must be maintained.

4.5.68 AHB9 peripherals clock divider register 1(RCC_AHB9DIV1)

Address offset: 0x01b8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												ESCSYSDIV[3:0]			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	ESCSYSDIV[3:0]	Ethercat system clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed

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4.5.69 AHB9 peripherals clock source select register 1(RCC_AHB9SEL1)

Address offset: 0x01bc

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													ESCKERSEL[2:0]		
													rw		

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2:0	ESCKERSEL[2:0]	Ethercat kernel clock selection. 000: Divided system bus clock is selected as Ethercat kernel clock 001: PLL2_B clock is selected as Ethercat kernel clock 010: PLL3_A clock is selected as Ethercat kernel clock 011: PLL3_C clock is selected as Ethercat kernel clock 100: PLL1_B clock is selected as Ethercat kernel clock Other values: setting is not allowed

4.5.70 AHB9 peripherals clock enable register 1(RCC_AHB9EN1)

Address offset: 0x01c0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												M7ESCEN	M4ESCEN	M7ESCLPEN	M4ESCLPEN
												rw	rw	rw	rw

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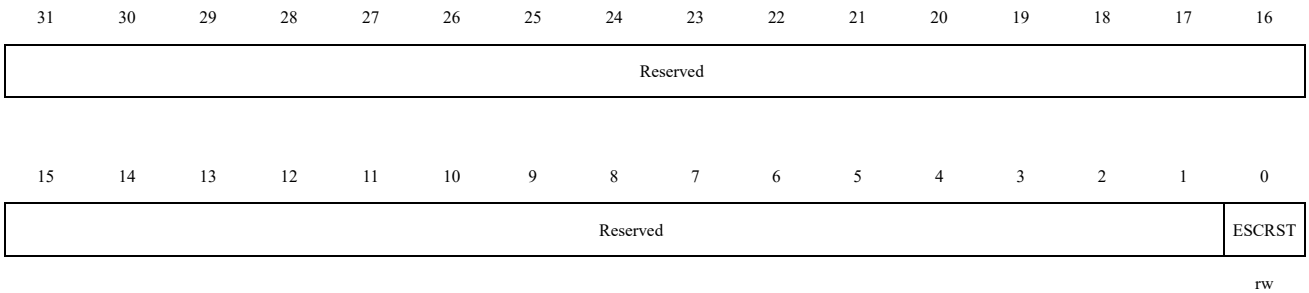
Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	M7ESCEN	ETHERCAT M7 allocation and clock enable. Set and cleared by software. 0: ETHERCAT is not allocated to M7. The "ethercat_ker_gated_clk" & "ethercat_phy_gated_clk" is disabled in M7 RUN mode. 1: ETHERCAT is allocated to M7. The "ethercat_ker_gated_clk" & "ethercat_phy_gated_clk" is enabled in M7 RUN mode.
2	M4ESCEN	ETHERCAT M4 allocation and clock enable. Set and cleared by software. 0: ETHERCAT is not allocated to M4. The "ethercat_ker_gated_clk" & "ethercat_phy_gated_clk" is disabled in M4 RUN mode. 1: ETHERCAT is allocated to M4. The "ethercat_ker_gated_clk" & "ethercat_phy_gated_clk" is enabled in M4 RUN mode.
1	M7ESCLPEN	ETHERCAT M7 Low Power clock Enable. Set and cleared by software. 0: The "ethercat_ker_gated_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "ethercat_ker_gated_clk" is enabled in M7 SLEEP and STOP mode. Note : M7ESCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4ESCLPEN	ETHERCAT M4 Low Power clock Enable. Set and cleared by software. 0: The "ethercat_ker_gated_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "ethercat_ker_gated_clk" is enabled in M4 SLEEP and STOP mode. Note : M4ESCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.71 AHB9 peripherals reset register 1(RCC_AHB9RST1)

Address offset: 0x01c4

Reset value: 0x00000000



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Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	ESCRST	Ethercat soft reset 0: Clear reset 1: Reset Ethercat

4.5.72 Retention domain clock divider register 1(RCC_RDDIV1)

Address offset: 0x010c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	COMPDIV[2:0]			Reserved	LPUARTDIV[2:0]			Reserved							
	rw				rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	COMPDIV[2:0]	APB5 COMP clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
27	Reserved	Reserved, the reset value must be maintained.
26:24	LPUARTDIV[2:0]	LPUART system clock prescalar values. 000: Divide by 1 100: Divide by 2 101: Divide by 4 110: Divide by 8 111: Divide by 16
23:0	Reserved	Reserved, the reset value must be maintained.

4.5.73 Retention domain clock source selection register 1(RCC_RDSEL1)

Address offset: 0x0110

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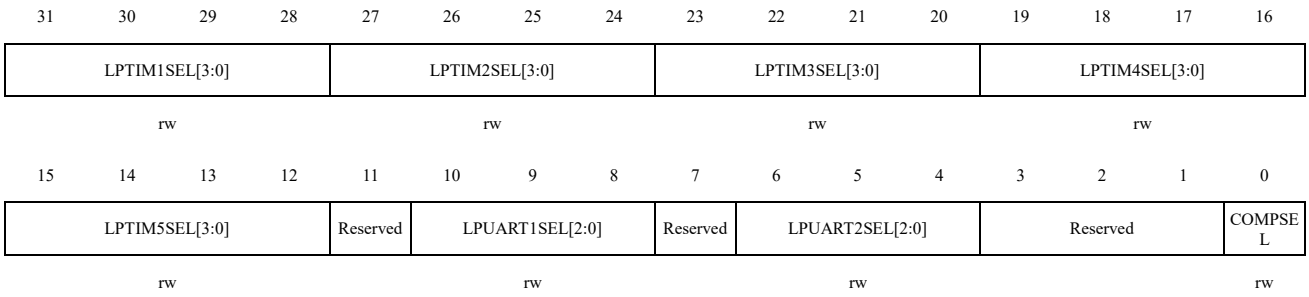
Reset value: 0x00000000



Bit field	Name	Description
31:28	LPTIM1SEL[3:0]	LPTIMER1 Kernel clock selection. 0000: APB5 bus clock is selected as "lptim1_gated_ker_clk". 0001: LSI clock is selected as "lptim1_gated_ker_clk". 0010: LSE clock is selected as "lptim1_gated_ker_clk". 0011: HSE clock is selected as "lptim1_gated_ker_clk". 0100: HIS clock is selected as "lptim1_gated_ker_clk". 0101: MSI clock is selected as "lptim1_gated_ker_clk". 1000: Comparator 1 output is selected as "lptim1_gated_ker_clk". 1001: Comparator 2 output is selected as "lptim1_gated_ker_clk". 1010: Comparator 3 output is selected as "lptim1_gated_ker_clk". 1011: Comparator 4 output is selected as "lptim1_gated_ker_clk". Other values: setting is not allowed
27:24	LPTIM2SEL[3:0]	LPTIMER2 Kernel clock selection. 0000: APB5 bus clock is selected as "lptim2_gated_ker_clk". 0001: LSI clock is selected as "lptim2_gated_ker_clk". 0010: LSE clock is selected as "lptim2_gated_ker_clk". 0011: HSE clock is selected as "lptim2_gated_ker_clk". 0100: HIS clock is selected as "lptim2_gated_ker_clk". 0101: MSI clock is selected as "lptim2_gated_ker_clk". 1000: Comparator 1 output is selected as "lptim2_gated_ker_clk". 1001: Comparator 2 output is selected as "lptim2_gated_ker_clk". 1010: Comparator 3 output is selected as "lptim2_gated_ker_clk". 1011: Comparator 4 output is selected as "lptim2_gated_ker_clk". Other values: setting is not allowed
23:20	LPTIM3SEL[3:0]	LPTIMER3 Kernel clock selection. 0000: APB5 bus clock is selected as "lptim3_gated_ker_clk". 0001: LSI clock is selected as "lptim3_gated_ker_clk". 0010: LSE clock is selected as "lptim3_gated_ker_clk". 0011: HSE clock is selected as "lptim3_gated_ker_clk". 0100: HIS clock is selected as "lptim3_gated_ker_clk". 0101: MSI clock is selected as "lptim3_gated_ker_clk".

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Bit field	Name	Description
		1000: Comparator 1 output is selected as "lptim3_gated_ker_clk". 1001: Comparator 2 output is selected as "lptim3_gated_ker_clk". 1010: Comparator 3 output is selected as "lptim3_gated_ker_clk". 1011: Comparator 4 output is selected as "lptim3_gated_ker_clk". Other values: setting is not allowed
19:16	LPTIM4SEL[3:0]	LPTIMER4 Kernel clock selection. 0000: APB5 bus clock is selected as "lptim4_gated_ker_clk". 0001: LSI clock is selected as "lptim4_gated_ker_clk". 0010: LSE clock is selected as "lptim4_gated_ker_clk". 0011: HSE clock is selected as "lptim4_gated_ker_clk". 0100: HIS clock is selected as "lptim4_gated_ker_clk". 0101: MSI clock is selected as "lptim4_gated_ker_clk". 1000: Comparator 1 output is selected as "lptim4_gated_ker_clk". 1001: Comparator 2 output is selected as "lptim4_gated_ker_clk". 1010: Comparator 3 output is selected as "lptim4_gated_ker_clk". 1011: Comparator 4 output is selected as "lptim4_gated_ker_clk". Other values: setting is not allowed
15:12	LPTIM5SEL[3:0]	LPTIMER5 Kernel clock selection. 0000: APB5 bus clock is selected as "lptim5_gated_ker_clk". 0001: LSI clock is selected as "lptim5_gated_ker_clk". 0010: LSE clock is selected as "lptim5_gated_ker_clk". 0011: HSE clock is selected as "lptim5_gated_ker_clk". 0100: HIS clock is selected as "lptim5_gated_ker_clk". 0101: MSI clock is selected as "lptim5_gated_ker_clk". 1000: Comparator 1 output is selected as "lptim5_gated_ker_clk". 1001: Comparator 2 output is selected as "lptim5_gated_ker_clk". 1010: Comparator 3 output is selected as "lptim5_gated_ker_clk". 1011: Comparator 4 output is selected as "lptim5_gated_ker_clk". Other values: setting is not allowed
11	Reserved	Reserved, the reset value must be maintained.
10:8	LPUART1SEL[2:0]	LPUART1 Kernel clock selection. 000: Divided system bus clock is selected as "lpuart1_gated_ker_clk". 001: HSI clock is selected as "lpuart1_gated_ker_clk". 010: LSE clock is selected as "lpuart1_gated_ker_clk". 011: HSE clock is selected as "lpuart1_gated_ker_clk". 100: MSI clock is selected as "lpuart1_gated_ker_clk". Other values: setting is not allowed
7	Reserved	Reserved, the reset value must be maintained.
6:4	LPUART2SEL[2:0]	LPUART2 Kernel clock selection. 000: Divided system bus clock is selected as "lpuart2_gated_ker_clk". 001: HSI clock is selected as "lpuart2_gated_ker_clk". 010: LSE clock is selected as "lpuart2_gated_ker_clk".

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Bit field	Name	Description
		011: HSE clock is selected as "lpuart2_gated_ker_clk". 100: MSI clock is selected as "lpuart2_gated_ker_clk". Other values: setting is not allowed
3:1	Reserved	Reserved, the reset value must be maintained.
0	COMPSEL	Comparator Controller clock selection 0: LSI clock is selected as "compctrl_gated_lsx_clk". 1: LSE clock is selected as "compctrl_gated_lsx_clk".

4.5.74 Retention domain control register 1(RCC_RDCTRL1)

Address offset: 0x01a8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		LPTIM2FLTEN	LPTIM2FLTSEL	LPTIM2COMP4EN	LPTIM2COMP3EN	LPTIM2COMP2EN	LPTIM2COMP1EN	Reserved			LPTIM2FLTDFC[4:0]				
		rw	rw	rw	rw	rw	rw				rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		LPTIM1FLTEN	LPTIM1FLTSEL	LPTIM1COMP4EN	LPTIM1COMP3EN	LPTIM1COMP2EN	LPTIM1COMP1EN	Reserved			LPTIM1FLTDFC[4:0]				
		rw	rw	rw	rw	rw	rw				rw				

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	LPTIM2FLTEN	Control signal to select filtered or non-filtered LPTIMER2 comparator clock source. 0: LPTIMER2 comparator clock source is not filtered. 1: LPTIMER2 comparator clock source is filtered
28	LPTIM2FLTSEL	Control signal to select the sample clock for the digital filter used at LPTIMER2 comparator clock source. 0: APB5 bus clock is used as sample clock of digital filter. 1: MSI clock is used as sample clock of digital filter.
27	LPTIM2COMP4EN	Enable signal for comparator 4 clock source to LPTIMER2. 0: Comparator 4 clock source to LPTIMER2 is disabled. 1: Comparator 4 clock source to LPTIMER2 is enabled.
26	LPTIM2COMP3EN	Enable signal for comparator 3 clock source to LPTIMER2. 0: Comparator 3 clock source to LPTIMER2 is disabled. 1: Comparator 3 clock source to LPTIMER2 is enabled.
25	LPTIM2COMP2EN	Enable signal for comparator 2 clock source to LPTIMER2. 0: Comparator 2 clock source to LPTIMER2 is disabled. 1: Comparator 2 clock source to LPTIMER2 is enabled.

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Bit field	Name	Description
24	LPTIM2COMP1EN	Enable signal for comparator 1 clock source to LPTIMER2. 0: Comparator 1 clock source to LPTIMER2 is disabled. 1: Comparator 1 clock source to LPTIMER2 is enabled.
23:21	Reserved	Reserved, the reset value must be maintained.
20:16	LPTIM2FLTDFC[4:0]	LPTIMER2 Glitch Filter stage control 00000: Filter bypass Others : counter value indicating minimum pulse width in terms of APB5 or MSI clock cycles.
15:14	Reserved	Reserved, the reset value must be maintained.
13	LPTIM1FLTEN	Control signal to select filtered or non-filtered LPTIMER1 comparator clock source. 0: LPTIMER1 comparator clock source is not filtered. 1: LPTIMER1 comparator clock source is filtered
12	LPTIM1FLTSEL	Control signal to select the sample clock for the digital filter used at LPTIMER1 comparator clock source. 0: APB5 bus clock is used as sample clock of digital filter. 1: MSI clock is used as sample clock of digital filter.
11	LPTIM1COMP4EN	Enable signal for comparator 4 clock source to LPTIMER1. 0: Comparator 4 clock source to LPTIMER1 is disabled. 1: Comparator 4 clock source to LPTIMER1 is enabled.
10	LPTIM1COMP3EN	Enable signal for comparator 3 clock source to LPTIMER1. 0: Comparator 3 clock source to LPTIMER1 is disabled. 1: Comparator 3 clock source to LPTIMER1 is enabled.
9	LPTIM1COMP2EN	Enable signal for comparator 2 clock source to LPTIMER1. 0: Comparator 2 clock source to LPTIMER1 is disabled. 1: Comparator 2 clock source to LPTIMER1 is enabled.
8	LPTIM1COMP1EN	Enable signal for comparator 1 clock source to LPTIMER1. 0: Comparator 1 clock source to LPTIMER1 is disabled. 1: Comparator 1 clock source to LPTIMER1 is enabled.
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	LPTIM1FLTDFC[4:0]	LPTIMER1 Glitch Filter stage control 00000: Filter bypass Others : counter value indicating minimum pulse width in terms of APB5 or MSI clock cycles.

4.5.75 Retention domain control register 2(RCC_RDCTRL2)

Address offset: 0x01ac

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		LPTIM4FLTEN	LPTIM4FLTSEL	LPTIM4COMP4EN	LPTIM4COMP3EN	LPTIM4COMP2EN	LPTIM4COMP1EN	Reserved			LPTIM4FLTDFC[4:0]				

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		rw	rw	rw	rw	rw	rw						rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		LPTIM3FLTEN	LPTIM3FLTSEL	LPTIM3COMP4EN	LPTIM3COMP3EN	LPTIM3COMP2EN	LPTIM3COMP1EN	Reserved			LPTIM3FLTDFC[4:0]				
		rw	rw	rw	rw	rw	rw						rw		

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	LPTIM4FLTEN	Control signal to select filtered or non-filtered LPTIMER4 comparator clock source. 0: LPTIMER4 comparator clock source is not filtered. 1: LPTIMER4 comparator clock source is filtered
28	LPTIM4FLTSEL	Control signal to select the sample clock for the digital filter used at LPTIMER4 comparator clock source. 0: APB5 bus clock is used as sample clock of digital filter. 1: MSI clock is used as sample clock of digital filter.
27	LPTIM4COMP4EN	Enable signal for comparator 4 clock source to LPTIMER4. 0: Comparator 4 clock source to LPTIMER4 is disabled. 1: Comparator 4 clock source to LPTIMER4 is enabled.
26	LPTIM4COMP3EN	Enable signal for comparator 3 clock source to LPTIMER4. 0: Comparator 3 clock source to LPTIMER4 is disabled. 1: Comparator 3 clock source to LPTIMER4 is enabled.
25	LPTIM4COMP2EN	Enable signal for comparator 2 clock source to LPTIMER4. 0: Comparator 2 clock source to LPTIMER4 is disabled. 1: Comparator 2 clock source to LPTIMER4 is enabled.
24	LPTIM4COMP1EN	Enable signal for comparator 1 clock source to LPTIMER4. 0: Comparator 1 clock source to LPTIMER4 is disabled. 1: Comparator 1 clock source to LPTIMER4 is enabled.
23:21	Reserved	Reserved, the reset value must be maintained.
20:16	LPTIM4FLTDFC[4:0]	LPTIMER4 Glitch Filter stage control 00000: Filter bypass Others : counter value indicating minimum pulse width in terms of APB5 or MSI clock cycles.
15:14	Reserved	Reserved, the reset value must be maintained.
13	LPTIM3FLTEN	Control signal to select filtered or non-filtered LPTIMER3 comparator clock source. 0: LPTIMER3 comparator clock source is not filtered. 1: LPTIMER3 comparator clock source is filtered
12	LPTIM3FLTSEL	Control signal to select the sample clock for the digital filter used at LPTIMER3 comparator clock source. 0: APB5 bus clock is used as sample clock of digital filter. 1: MSI clock is used as sample clock of digital filter.
11	LPTIM3COMP4EN	Enable signal for comparator 4 clock source to LPTIMER3. 0: Comparator 4 clock source to LPTIMER3 is disabled.

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Bit field	Name	Description
		1: Comparator 4 clock source to LPTIMER3 is enabled.
10	LPTIM3COMP3EN	Enable signal for comparator 3 clock source to LPTIMER3. 0: Comparator 3 clock source to LPTIMER3 is disabled. 1: Comparator 3 clock source to LPTIMER3 is enabled.
9	LPTIM3COMP2EN	Enable signal for comparator 2 clock source to LPTIMER3. 0: Comparator 2 clock source to LPTIMER3 is disabled. 1: Comparator 2 clock source to LPTIMER3 is enabled.
8	LPTIM3COMP1EN	Enable signal for comparator 1 clock source to LPTIMER3. 0: Comparator 1 clock source to LPTIMER3 is disabled. 1: Comparator 1 clock source to LPTIMER3 is enabled.
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	LPTIM3FLTDFC[4:0]	LPTIMER3 Glitch Filter stage control 00000: Filter bypass Others : counter value indicating minimum pulse width in terms of APB5 or MSI clock cycles.

4.5.76 Retention domain control register 3(RCC_RDCTRL3)

Address offset: 0x01b0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		LPTIM5FLTEN	LPTIM5FLTSEL	LPTIM5COMP4EN	LPTIM5COMP3EN	LPTIM5COMP2EN	LPTIM5COMP1EN	Reserved			LPTIM5FLTDFC[4:0]				
		rw	rw	rw	rw	rw	rw				rw				

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	LPTIM5FLTEN	Control signal to select filtered or non-filtered LPTIMER5 comparator clock source. 0: LPTIMER5 comparator clock source is not filtered. 1: LPTIMER5 comparator clock source is filtered
12	LPTIM5FLTSEL	Control signal to select the sample clock for the digital filter used at LPTIMER5 comparator clock source. 0: APB5 bus clock is used as sample clock of digital filter. 1: MSI clock is used as sample clock of digital filter.

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Bit field	Name	Description
11	LPTIM5COMP4EN	Enable signal for comparator 4 clock source to LPTIMER5. 0: Comparator 4 clock source to LPTIMER5 is disabled. 1: Comparator 4 clock source to LPTIMER5 is enabled.
10	LPTIM5COMP3EN	Enable signal for comparator 3 clock source to LPTIMER5. 0: Comparator 3 clock source to LPTIMER5 is disabled. 1: Comparator 3 clock source to LPTIMER5 is enabled.
9	LPTIM5COMP2EN	Enable signal for comparator 2 clock source to LPTIMER5. 0: Comparator 2 clock source to LPTIMER5 is disabled. 1: Comparator 2 clock source to LPTIMER5 is enabled.
8	LPTIM5COMP1EN	Enable signal for comparator 1 clock source to LPTIMER5. 0: Comparator 1 clock source to LPTIMER5 is disabled. 1: Comparator 1 clock source to LPTIMER5 is enabled.
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	LPTIM5FLTDFC[4:0]	LPTIMER5 Glitch Filter stage control 00000: Filter bypass Others : counter value indicating minimum pulse width in terms of APB5 or MSI clock cycles.

4.5.77 Retention domain clock enable register 1(RCC_RDEN1)

Address offset: 0x0114

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7LPTIM1EN	M4LPTIM1EN	M7LPTIM1LPEN	M4LPTIM1LPEN	M7LPTIM2EN	M4LPTIM2EN	M7LPTIM2LPEN	M4LPTIM2LPEN	M7LPTIM3EN	M4LPTIM3EN	M7LPTIM3LPEN	M4LPTIM3LPEN	M7LPTIM4EN	M4LPTIM4EN	M7LPTIM4LPEN	M4LPTIM4LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7LPTIM5EN	M4LPTIM5EN	M7LPTIM5LPEN	M4LPTIM5LPEN	M7LPUART1EN	M4LPUART1EN	M7LPUART1LPEN	M4LPUART1LPEN	M7LPUART2EN	M4LPUART2EN	M7LPUART2LPEN	M4LPUART2LPEN	Reserved			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				

Bit field	Name	Description
31	M7LPTIM1EN	LPTIMER1 M7 allocation and clock enable. Set and cleared by software. 0: LPTIMER1 is not allocated to M7. The "lptim1_gated_ker_clk" and "lptim1_gated_pclk" are disabled in M7 RUN mode. 1: LPTIMER1 is allocated to M7. The "lptim1_gated_ker_clk" and "lptim1_gated_pclk" are enabled in M7 RUN mode.
30	M4LPTIM1EN	LPTIMER1 M4 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: LPTIMER1 is not allocated to M4. The "lptim1_gated_ker_clk" and "lptim1_gated_pclk" are disabled in M4 RUN mode. 1: LPTIMER1 is allocated to M4. The "lptim1_gated_ker_clk" and "lptim1_gated_pclk" are enabled in M4 RUN mode.
29	M7LPTIM1LPEN	LPTIMER1 M7 Low Power clock Enable. Set and cleared by software. 0: The "lptim1_gated_ker_clk" and "lptim1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lptim1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lptim1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPTIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4LPTIM1LPEN	LPTIMER1 M4 Low Power clock Enable. Set and cleared by software. 0: The "lptim1_gated_ker_clk" and "lptim1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lptim1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lptim1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPTIM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7LPTIM2EN	LPTIMER2 M7 allocation and clock enable. Set and cleared by software. 0: LPTIMER2 is not allocated to M7. The "lptim2_gated_ker_clk" and "lptim2_gated_pclk" are disabled in M7 RUN mode. 1: LPTIMER2 is allocated to M7. The "lptim2_gated_ker_clk" and "lptim2_gated_pclk" are enabled in M7 RUN mode.
26	M4LPTIM2EN	LPTIMER2 M4 allocation and clock enable. Set and cleared by software. 0: LPTIMER2 is not allocated to M4. The "lptim2_gated_ker_clk" and "lptim2_gated_pclk" are disabled in M4 RUN mode. 1: LPTIMER2 is allocated to M4. The "lptim2_gated_ker_clk" and "lptim2_gated_pclk" are enabled in M4 RUN mode.
25	M7LPTIM2LPEN	LPTIMER2 M7 Low Power clock Enable. Set and cleared by software. 0: The "lptim2_gated_ker_clk" and "lptim2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lptim2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lptim2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4LPTIM2LPEN	LPTIMER2 M4 Low Power clock Enable.

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Bit field	Name	Description
		Set and cleared by software. 0: The "lptim2_gated_ker_clk" and "lptim2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lptim2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lptim2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPTIM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7LPTIM3EN	LPTIMER3 M7 allocation and clock enable. Set and cleared by software. 0: LPTIMER3 is not allocated to M7. The "lptim3_gated_ker_clk" and "lptim3_gated_pclk" are disabled in M7 RUN mode. 1: LPTIMER3 is allocated to M7. The "lptim3_gated_ker_clk" and "lptim3_gated_pclk" are enabled in M7 RUN mode.
22	M4LPTIM3EN	LPTIMER3 M4 allocation and clock enable. Set and cleared by software. 0: LPTIMER3 is not allocated to M4. The "lptim3_gated_ker_clk" and "lptim3_gated_pclk" are disabled in M4 RUN mode. 1: LPTIMER3 is allocated to M4. The "lptim3_gated_ker_clk" and "lptim3_gated_pclk" are enabled in M4 RUN mode.
21	M7LPTIM3LPEN	LPTIMER3 M7 Low Power clock Enable. Set and cleared by software. 0: The "lptim3_gated_ker_clk" and "lptim3_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lptim3_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lptim3_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPTIM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4LPTIM3LPEN	LPTIMER3 M4 Low Power clock Enable. Set and cleared by software. 0: The "lptim3_gated_ker_clk" and "lptim3_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lptim3_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lptim3_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPTIM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7LPTIM4EN	LPTIMER4 M7 allocation and clock enable. Set and cleared by software. 0: LPTIMER4 is not allocated to M7. The "lptim4_gated_ker_clk" and "lptim4_gated_pclk" are disabled in M7 RUN mode. 1: LPTIMER4 is allocated to M7. The "lptim4_gated_ker_clk" and "lptim4_gated_pclk" are enabled in M7 RUN mode.
18	M4LPTIM4EN	LPTIMER4 M4 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: LPTIMER4 is not allocated to M4. The "lptim4_gated_ker_clk" and "lptim4_gated_pclk" are disabled in M4 RUN mode. 1: LPTIMER4 is allocated to M4. The "lptim4_gated_ker_clk" and "lptim4_gated_pclk" are enabled in M4 RUN mode.
17	M7LPTIM4LPEN	LPTIMER4 M7 Low Power clock Enable. Set and cleared by software. 0: The "lptim4_gated_ker_clk" and "lptim4_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lptim4_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lptim4_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPTIM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4LPTIM4LPEN	LPTIMER4 M4 Low Power clock Enable. Set and cleared by software. 0: The "lptim4_gated_ker_clk" and "lptim4_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lptim4_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lptim4_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPTIM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7LPTIM5EN	LPTIMER5 M7 allocation and clock enable. Set and cleared by software. 0: LPTIMER5 is not allocated to M7. The "lptim5_gated_ker_clk" and "lptim5_gated_pclk" are disabled in M7 RUN mode. 1: LPTIMER5 is allocated to M7. The "lptim5_gated_ker_clk" and "lptim5_gated_pclk" are enabled in M7 RUN mode.
14	M4LPTIM5EN	LPTIMER5 M4 allocation and clock enable. Set and cleared by software. 0: LPTIMER5 is not allocated to M4. The "lptim5_gated_ker_clk" and "lptim5_gated_pclk" are disabled in M4 RUN mode. 1: LPTIMER5 is allocated to M4. The "lptim5_gated_ker_clk" and "lptim5_gated_pclk" are enabled in M4 RUN mode.
13	M7LPTIM5LPEN	LPTIMER5 M7 Low Power clock Enable. Set and cleared by software. 0: The "lptim5_gated_ker_clk" and "lptim5_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lptim5_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lptim5_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPTIM5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4LPTIM5LPEN	LPTIMER5 M4 Low Power clock Enable.

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Bit field	Name	Description
		Set and cleared by software. 0: The "lptim5_gated_ker_clk" and "lptim5_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lptim5_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lptim5_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPTIM5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7LPUART1EN	LPUART1 M7 allocation and clock enable. Set and cleared by software. 0: LPUART1 is not allocated to M7. The "lpuart1_gated_ker_clk" and "lpuart1_gated_pclk" are disabled in M7 RUN mode. 1: LPUART1 is allocated to M7. The "lpuart1_gated_ker_clk" and "lpuart1_gated_pclk" are enabled in M7 RUN mode.
10	M4LPUART1EN	LPUART1 M4 allocation and clock enable. Set and cleared by software. 0: LPUART1 is not allocated to M4. The "lpuart1_gated_ker_clk" and "lpuart1_gated_pclk" are disabled in M4 RUN mode. 1: LPUART1 is allocated to M4. The "lpuart1_gated_ker_clk" and "lpuart1_gated_pclk" are enabled in M4 RUN mode.
9	M7LPUART1LPEN	LPUART1 M7 Low Power clock Enable. Set and cleared by software. 0: The "lpuart1_gated_ker_clk" and "lpuart1_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lpuart1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lpuart1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPUART1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4LPUART1LPEN	LPUART1 M4 Low Power clock Enable. Set and cleared by software. 0: The "lpuart1_gated_ker_clk" and "lpuart1_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lpuart1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lpuart1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPUART1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7LPUART2EN	LPUART2 M7 allocation and clock enable. Set and cleared by software. 0: LPUART2 is not allocated to M7. The "lpuart2_gated_ker_clk" and "lpuart2_gated_pclk" are disabled in M7 RUN mode. 1: LPUART2 is allocated to M7. The "lpuart2_gated_ker_clk" and "lpuart2_gated_pclk" are enabled in M7 RUN mode.
6	M4LPUART2EN	LPUART2 M4 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: LPUART2 is not allocated to M4. The "lpuart2_gated_ker_clk" and "lpuart2_gated_pclk" are disabled in M4 RUN mode. 1: LPUART2 is allocated to M4. The "lpuart2_gated_ker_clk" and "lpuart2_gated_pclk" are enabled in M4 RUN mode.
5	M7LPUART2LPEN	LPUART2 M7 Low Power clock Enable. Set and cleared by software. 0: The "lpuart2_gated_ker_clk" and "lpuart2_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lpuart2_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "lpuart2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LPUART2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4LPUART2LPEN	LPUART2 M4 Low Power clock Enable. Set and cleared by software. 0: The "lpuart2_gated_ker_clk" and "lpuart2_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lpuart2_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "lpuart2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LPUART2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.78 Retention domain clock enable register 2(RCC_RDEN2)

Address offset: 0x0118

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7COMPEN	M4COMPEN	M7COMPLPEN	M4COMPLPEN	Reserved											
rw	rw	rw	rw												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31	M7COMPEN	COMP M7 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: COMP is not allocated to M7. The "comp_gated_ker_clk", "comp_gated_lsx_clk" and "comp_gated_pclk" are disabled in M7 RUN mode. 1: COMP is allocated to M7. The "comp_gated_ker_clk", "comp_gated_lsx_clk"and "comp_gated_pclk" are enabled in M7 RUN mode.
30	M4COMPEN	COMP M4 allocation and clock enable. Set and cleared by software. 0: COMP is not allocated to M4. The "comp_gated_ker_clk", "comp_gated_lsx_clk" and "comp_gated_pclk" are disabled in M4 RUN mode. 1: COMP is allocated to M4. The "comp_gated_ker_clk", "comp_gated_lsx_clk"and "comp_gated_pclk" are enabled in M4 RUN mode.
29	M7COMPLPEN	COMP M7 Low Power clock Enable. Set and cleared by software. 0: The "comp_gated_ker_clk", "comp_gated_lsx_clk" and "comp_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "comp_gated_ker_clk" and "comp_gated_lsx_clk" are enabled in M7 SLEEP and STOP mode. "comp_gated_pclk" is enabled in M7 SLEEP mode. Note : M7COMPEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
28	M4COMPLPEN	COMP M4 Low Power clock Enable. Set and cleared by software. 0: The "comp_gated_ker_clk", "comp_gated_lsx_clk" and "comp_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "comp_gated_ker_clk" and "comp_gated_lsx_clk" are enabled in M4 SLEEP and STOP mode. "comp_gated_pclk" is enabled in M4 SLEEP mode. Note : M4COMPEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
27:0	Reserved	Reserved, the reset value must be maintained.

4.5.79 Retention domain reset register 1(RCC_RDRST1)

Address offset: 0x011c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			LPTIM1RST	Reserved			LPTIM2RST	Reserved			LPTIM3RST	Reserved			LPTIM4RST
			rw				rw				rw				rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			LPTIM5RST	Reserved			LPUART1RST	Reserved			LPUART2RST	Reserved			
			rw				rw				rw				

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Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	LPTIM1RST	LPTIMER1 soft reset 0: Clear reset 1: Reset LPTIMER1
27:25	Reserved	Reserved, the reset value must be maintained.
24	LPTIM2RST	LPTIMER2 soft reset 0: Clear reset 1: Reset LPTIMER2
23:21	Reserved	Reserved, the reset value must be maintained.
20	LPTIM3RST	LPTIMER3 soft reset 0: Clear reset 1: Reset LPTIMER3
19:17	Reserved	Reserved, the reset value must be maintained.
16	LPTIM4RST	LPTIMER4 soft reset 0: Clear reset 1: Reset LPTIMER4
15:13	Reserved	Reserved, the reset value must be maintained.
12	LPTIM5RST	LPTIMER5 soft reset 0: Clear reset 1: Reset LPTIMER5
11:9	Reserved	Reserved, the reset value must be maintained.
8	LPUART1RST	LPUART1 soft reset 0: Clear reset 1: Reset LPUART1
7:5	Reserved	Reserved, the reset value must be maintained.
4	LPUART2RST	LPUART2 soft reset 0: Clear reset 1: Reset LPUART2
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.80 Retention domain reset register 2(RCC_RDRST2)

Address offset: 0x0120

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			COMPRST	Reserved											
			rw												

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	COMPRST	COMP soft reset 0: Clear reset 1: Reset COMP
27:0	Reserved	Reserved, the reset value must be maintained.

4.5.81 Backup domain control register(RCC_BDCTRL)

Address offset: 0x0124

Reset value: 0x0148ec0f

Note: BDCTRL is protected, you need to enable the PWR clock first, then configure PWR_SYSCTRL1.DBKP to 1 to change it.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFELSERDF	AFELSIRDF	Reserved	LSELDOEN	LSIOVREN	LSIPFACK	LSIPFF	LSICSSEN	Reserved	LSERDCNTEN	RTCLSFSW	RTCHSFSW	LSISECRDF	RTCEN	RTCSEL[1:0]	
r	r		rw	rw	rw	r	rw		rw	r	r	r	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BORRSTEN	C1LPRSTEN	C2LPRSTEN	BDRST	BKPEMCRSTEN	RETEMCRSTEN	LSECSSF	LSECSSEN	LSERDEN	LSEBP	LSERDF	LSEEN	LSIRDEN	LSISECEN	LSIRDF	LSIEN
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	r	rw	rw	rw	r	rw

Bit field	Name	Description
31	AFELSERDF	AFE LSE Ready 0: LSE is not ready. 1: LSE is ready. Note : This bit switching to '1' does not indicate that LSE clock frequency is stable. Note : This bit field is reset by BDRST
30	AFELSIRDF	AFE LSI Ready 0: LSI is not ready. 1: LSI is ready. Note : This bit switching to '1' does not indicate that LSI clock frequency is stable. Note : This bit field is reset by BDRST
29	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
28	LSELDOEN	LSE LDO Enable. Set and cleared by software. 0: LSE LDO is not enabled. 1: LSE LDO is enabled. Note : This bit field is reset by BDRST
27	LSIOVREN	Software override control bit for LSI clock switching between primary and secondary. 0: Software override is disabled, LSI clock source selected by hardware. 1: Software overrride is enabled, LSI clock source selected by LSICSSEN bit.
26	LSIPFACK	LSI primary failure acknowledgement. Set by software to acknowledge the failure of internal 32kHz LSI primary oscillator. 0: LSI primary clock failure is not acknowledged. 1: LSI primary clock failure is acknowleged.
25	LSIPFF	LSI primary failure status Set by hardware to indicate when a failure has been detected by the Clock Security System on the internal 32kHz LSI primary oscillator. 0: No failure detected on LSI primary. 1: Failure detected on LSI primary.
24	LSICSSEN	This is a dual purpose bit. When the bit LSIOVREN set to 0, this bit is used to enable LSI primary clock security system. 0: Disable LSI primary failure detection 1: Enable LSI primary failure detection When the bit LSIOVREN is set to 1, this bit is used to select the source of LSI clock. 0: LSI source is primary clock 1: LSI source is secondary clock Note : This bit field is reset by BDRST
23	Reserved	Reserved, the reset value must be maintained.
22	LSERDCNTEN	LSE ready generation counter enable. 0: Disable/stop LSE ready counter. 1: Enable/start LSE ready counter. Note : This bit field is reset by BDRST
21	RTCLSFSW	Status flag to indicate that when LSE source is selected as RTC clock, upon LSE failure the clock source is switched from LSE to LSI 0: LSE clock did not fail when RTC clock source is selected as LSE. 1: RTC clock source is selected as LSE and LSE clock failure event is detected. LSE clock source is switched to LSI clock.
20	RTCHSFSW	Status flag to indicate that when HSE source is selected as RTC clock, upon HSE failure the clock source is switched from HSE to HSI 0: HSE clock did not fail when RTC clock source is selected as HSE. 1: RTC clock source is selected as HSE and HSE clock failure event is detected. HSE clock source is switched to HSI clock.
19	LSISECRDF	Internal Secondary low-speed oscillator clock ready.

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Bit field	Name	Description
		Set and cleared by hardware to indicate when the internal RC 32 kHz oscillator clock is stable. 0: Internal Secondary RC 32 kHz oscillator clock is not stable 1: Internal Secondary RC 32 kHz oscillator clock is ready and stable
18	RTCEN	RTC Kernel clock enable. Set and cleared by software. 0: RTC kernel clock disabled 1: RTC kernel clock enabled Note : This bit field is reset by BDRST
17:16	RTCSEL[1:0]	RTC Kernel clock source selection. 00: No clock 01: LSE oscillator clock is selected as RTC kernel clock. 10: LSI oscillator clock is selected as RTC kernel clock. 11: Divided HSE oscillator clock is selected as RTC kernel clock. Note : This bit field is reset by BDRST
15	BORRSTEN	BOR Reset Request enable. Set and cleared by software. 0: BOR reset request will not cause NRST reset. 1: BOR reset request will cause NRST reset. Note : This bit field is reset by BDRST
14	C1LPRSTEN	C1 LPW Reset Request enable. Set and cleared by software. 0: C1 LPW reset request will not cause NRST reset. 1: C1 LPW reset request will cause NRST reset. Note : This bit field is reset by BDRST
13	C2LPRSTEN	C2 LPW Reset Request enable. Set and cleared by software. 0: C2 LPW reset request will not cause NRST reset. 1: C2 LPW reset request will cause NRST reset. Note : This bit field is reset by BDRST
12	BDRST	Backup domain software reset. Set and cleared by software. 0: Reset not activated 1: Resets the entire Backup domain
11	BKPEMCRSTEN	BKP EMC Reset Request enable. Set and cleared by software. 0: BKP EMC reset request will not cause NRST reset. 1: BKP EMC reset request will cause NRST reset. Note : This bit field is reset by BDRST
10	RETEMCRSTEN	VDDDRET EMC Reset Request enable. Set and cleared by software. 0: VDDDRET EMC reset request will not cause NRST reset.

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Bit field	Name	Description
		1: VDDDRET EMC reset request will cause NRST reset. Note : This bit field is reset by BDRST
9	LSECSSF	LSE failure Detection Set by hardware to indicate when a failure has been detected by the Clock Security System on the external 32kHz oscillator (LSE). 0: No failure detected on LSE 1: Failure detected on LSE Note : This bit field is reset by BDRST
8	LSECSSEN	LSECSS failure detection enable 0 : Disable LSE failure detection 1 : Enable LSE failure detection Note : This bit field is reset by BDRST
7	LSERDEN	LSE ready enable 0: External RC 32 kHz oscillator Ready logic is disabled 1: External RC 32 kHz oscillator Ready logic is enabled Note : This bit field is reset by BDRST
6	LSEBP	External low-speed oscillator bypass. This bit can be written only when the external 32 kHz oscillator is disabled. 0: LSE oscillator not bypassed 1: LSE oscillator bypassed *Note : This bit field is reset by BDRST* *Note: Make sure LSEEN=0 before enabling LSEBP.*
5	LSERDF	External low-speed oscillator clock ready. Set and cleared by hardware to indicate when the external 32 kHz oscillator clock is stable. After the LSEEN bit is cleared, LSERDF goes low after 6 external low-speed oscillator clock cycles. 0: External 32 kHz oscillator clock not stable 1: External 32 kHz oscillator clock is stable Note : This bit field is reset by BDRST
4	LSEEN	External low-speed oscillator enable Set and cleared by software. 0: External 32 kHz oscillator OFF 1: External 32 kHz oscillator ON Note : This bit field is reset by BDRST
3	LSIRDEN	LSI ready enable 0: Internal RC 32 kHz oscillator Ready logic is disabled 1: Internal RC 32 kHz oscillator Ready logic is enabled Note : This bit field is reset by BDRST
2	LSISECEN	LSI Secondary clock Oscillator enable 0: Internal RC 32 kHz oscillator OFF 1: Internal RC 32 kHz oscillator ON
1	LSIRDF	Internal low-speed oscillator clock ready.

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Bit field	Name	Description
		Set and cleared by hardware to indicate when the internal RC 32 kHz oscillator clock is stable. After the LSIEN bit is cleared, LSIRDF goes low after 3 internal RC 32 kHz oscillator clock cycles. 0: Internal RC 32 kHz oscillator clock is not stable 1: Internal RC 32 kHz oscillator clock is ready and stable
0	LSIEN	Internal low-speed oscillator enable 0: Internal RC 32 kHz oscillator OFF 1: Internal RC 32 kHz oscillator ON

4.5.82 LSI CSS delay register(RCC_LSICSSDL)

Address offset: 0x01e0

Reset value: 0x000000c8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DELAY[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAY[31:0]															
rw															

Bit field	Name	Description
[31:0]	DELAY[31:0]	This delay represents the estimated time required for the primary LSI clock to be stable during chip power up. Considering LSI frequency as 15.6 KHz (non trim value) and estimated LSI clock stabilization time to be 12.5ms, the default value of this counter will be approximately 200 (32'hC8) LSI clock cycles.

4.5.83 Control and status register(RCC_CTRLSTS)

Address offset: 0x0128

Reset value: 0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RMRSTF	Reserved														
rw															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1LPRSTF	C2LPRSTF	RETEMCRSTF	BKPEMCRSTF	BORRSTF	Reserved	MMURSTF	Reserved	WWDG1RSTF	WWDG2RSTF	IWDG1RSTF	IWDG2RSTF	CM4SFTRSTF	CM7SFTRSTF	PORRSTF	PINRSTF
r	r	r	r	r		r		r	r	r	r	r	r	r	r

Bit field	Name	Description
31	RMRSTF	Remove reset flag Set by software to clear all reset flags. 0: No effect 1: Clear all reset flags
30:16	Reserved	Reserved, the reset value must be maintained.
15	C1LPRSTF	C1 Low-power reset flag Set by hardware when a C1 domain Low-power management reset occurs.Cleared by writing to the RMRSTF bit. 0: No Low-power management reset occurred 1: C1 domain Low-power management reset occurred
14	C2LPRSTF	C2 Low-power reset flag Set by hardware when a C2 domain Low-power management reset occurs.Cleared by writing to the RMRSTF bit. 0: No Low-power management reset occurred 1: C2 domain Low-power management reset occurred
13	RETEMCRSTF	VDDDRET EMC reset flag Set by hardware when a VDDDRET emc reset occurs.Cleared by writing to the RMRSTF bit. 0: No VDDDRET emc reset occurred 1: VDDDRET emc reset occurred
12	BKPEMCRSTF	Backup EMC reset flag Set by hardware when a backup emc reset occurs.Cleared by writing to the RMRSTF bit. 0: No backup emc reset occurred 1: backup emc reset occurred
11	BORRSTF	BOR reset flag Set by hardware when a bor reset occurs.Cleared by writing to the RMRSTF bit. 0: No bor reset occurred 1: bor reset occurred
10	Reserved	Reserved, the reset value must be maintained.
9	MMURSTF	M7 MMU reset flag Set by hardware when a M7 MMU reset occurs. Cleared by writing to the RMRSTF bit. 0: No M7 MMU reset occurred 1: M7 MMU reset occurred
8	Reserved	Reserved, the reset value must be maintained.
7	WWDG1RSTF	Window watchdog 1 resetflag Set by hardware when a window watchdog 1 reset occurs.Cleared by writing to the RMRSTF bit.

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Bit field	Name	Description
		0: No window watchdog 1 reset occurred 1: Window watchdog 1 reset occurred
6	WWDG2RSTF	Window watchdog 2 resetflag Set by hardware when a window watchdog 2 reset occurs.Cleared by writing to the RMRSTF bit. 0: No window watchdog 2 reset occurred 1: Window watchdog 2 reset occurred
5	IWDG1RSTF	Independent watchdog 1 reset flag Set by hardware when an independent watchdog reset from VDD domain occurs. Cleared by writing to the RMRSTF bit. 0: No Independent Watchdog 1 reset occurred 1: Independent Watchdog 1 reset occurred
4	IWDG2RSTF	Independent watchdog 2 reset flag Set by hardware when an independent watchdog reset from VDD domain occurs. Cleared by writing to the RMRSTF bit. 0: No Independent Watchdog 2 reset occurred 1: Independent Watchdog 2 reset occurred
3	CM4SFTRSTF	M4 Software reset flag Set by hardware when a M4 software reset occurs.Cleared by writing to the RMRSTF bit. 0: No M4 software reset occurred 1: M4 Software reset occurred
2	CM7SFTRSTF	M7 Software reset flag Set by hardware when a M7 software reset occurs.Cleared by writing to the RMRSTF bit. 0: No M7 software reset occurred 1: M7 Software reset occurred
1	PORRSTF	POR/PDR reset flag Set by hardware when a POR/PDR reset occurs.Cleared by writing to the RMRSTF bit. 0: No POR/PDR reset occurred 1: POR/PDR reset occurred
0	PINRSTF	PIN reset flag Set by hardware when a reset from the NRST pin occurs. Cleared by writing to the RMRSTF bit. 0: No reset from NRST pin occurred 1: Reset from NRST pin occurred

4.5.84 Clock interrupt register 1(RCC_CLKINT1)

Address offset: 0x012c

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	LSECSSIE	LSECSSIF	LSECSSIC	Reserved		HSECSSIF	HSECSSIC	Reserved	BORIE	BORIF	BORIC	Reserved	PLL1RDIE	PLL1RDIF	PLL1RDIC
	rw	r	w			r	w		rw	r	w		rw	r	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PLL2RDIE	PLL2RDIF	PLL2RDIC	Reserved	PLL3RDIE	PLL3RDIF	PLL3RDIC	Reserved	SHRPLLRDIE	SHRPLLRDIF	SHRPLLRDIC	Reserved			
	rw	r	w		rw	r	w		rw	r	w				

Bit field	Name	Description
31	Reserved	
30	LSECSSIE	LSE CSS interrupt enable. Set and cleared by software to enable/disable interrupt caused by LSE CSS detection. 0: LSE CSS interrupt disabled 1: LSE CSS interrupt enabled
29	LSECSSIF	LSE CSS interrupt flag. Set by hardware when a failure is detected in the external 32 kHz oscillator and LSECSSIE is set. Cleared by software setting the LSECSSIC bit. 0: No clock security interrupt caused by LSE clock failure 1: Clock security interrupt caused by LSE clock failure
28	LSECSSIC	LSE CSS interrupt clear. This bit is set by software to clear the LSECSSIF flag. 0: No effect 1: Clear LSECSSIF flag
27:26	Reserved	Reserved, the reset value must be maintained.
25	HSECSSIF	HSE Clock security system interrupt flag. Set by hardware when a failure is detected in the HSE oscillator. Cleared by software setting the HSECSSIC bit. 0: No clock security interrupt caused by HSE clock failure 1: Clock security interrupt caused by HSE clock failure
24	HSECSSIC	HSE Clock security system interrupt clear. This bit is set by software to clear the HSECSSIF flag. 0: No effect 1: Clear HSECSSIF flag
23	Reserved	Reserved, the reset value must be maintained.
22	BORIE	BOR interrupt enable. Set and cleared by software to enable/disable interrupt caused by BOR. 0: BOR interrupt disabled 1: BOR interrupt enabled
21	BORIF	BOR interrupt flag. Set by hardware when a bor reset occurs and BORIE is set.Cleared by software setting the BORIC bit.

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Bit field	Name	Description
		0: No BOR reset interrupt 1: BOR reset interrupt
20	BORIC	BOR interrupt clear. This bit is set by software to clear the BORIF flag. 0: No effect 1: BORIF cleared
19	Reserved	Reserved, the reset value must be maintained.
18	PLL1RDIE	PLL1 ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by PLL1 lock. 0: PLL1 lock interrupt disabled 1: PLL1 lock interrupt enabled
17	PLL1RDIF	PLL1 ready interrupt flag. Set by hardware when the PLL1 lock and PLL1RDIE is set.Cleared by software setting the PLL1RDIC bit. 0: No clock ready interrupt caused by PLL1 lock 1: Clock ready interrupt caused by PLL1 lock
16	PLL1RDIC	PLL1 ready interrupt clear. This bit is set by software to clear the PLL1RDIF flag. 0: No effect 1: PLL1RDIF cleared
15	Reserved	Reserved, the reset value must be maintained.
14	PLL2RDIE	PLL2 ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by PLL2 lock. 0: PLL2 lock interrupt disabled 1: PLL2 lock interrupt enabled
13	PLL2RDIF	PLL2 ready interrupt flag. Set by hardware when the PLL2 lock and PLL2RDIE is set.Cleared by software setting the PLL2RDIC bit. 0: No clock ready interrupt caused by PLL2 lock 1: Clock ready interrupt caused by PLL2 lock
12	PLL2RDIC	PLL2 ready interrupt clear. This bit is set by software to clear the PLL2RDIF flag. 0: No effect 1: PLL2RDIF cleared
11	Reserved	Reserved, the reset value must be maintained.
10	PLL3RDIE	PLL3 ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by PLL3 lock. 0: PLL3 lock interrupt disabled 1: PLL3 lock interrupt enabled
9	PLL3RDIF	PLL3 ready interrupt flag. Set by hardware when the PLL3 lock and PLL3RDIE is set.Cleared by software setting the

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Bit field	Name	Description
		PLL3RDIC bit. 0: No clock ready interrupt caused by PLL3 lock 1: Clock ready interrupt caused by PLL3 lock
8	PLL3RDIC	PLL3 ready interrupt clear. This bit is set by software to clear the PLL3RDIF flag. 0: No effect 1: PLL3RDIF cleared
7	Reserved	Reserved, the reset value must be maintained.
6	SHRPLLRDIE	SHRPLL ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by SHRPLL lock. 0: SHRPLL lock interrupt disabled 1: SHRPLL lock interrupt enabled
5	SHRPLLRDIF	SHRPLL ready interrupt flag. Set by hardware when the SHRPLL lock and SHRPLLRDIE is set.Cleared by software setting the SHRPLLRDIC bit. 0: No clock ready interrupt caused by SHRPLL lock 1: Clock ready interrupt caused by SHRPLL lock
4	SHRPLLRDIC	SHRPLL ready interrupt clear. This bit is set by software to clear the SHRPLLRDIF flag. 0: No effect 1: SHRPLLRDIF cleared
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.85 Clock interrupt register 2(RCC_CLKINT2)

Address offset: 0x0130

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	HSERDIE	HSERDIF	HSERDIC	Reserved	HSIRDIE	HSIRDIF	HSIRDIC	Reserved	MSIRDIE	MSIRDIF	MSIRDIC	Reserved	LSERDIE	LSERDIF	LSERDIC
	rw	r	w		rw	r	w		rw	r	w		rw	r	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LSIRDIE	LSIRDIF	LSIRDIC	Reserved	HSICALEIE	HSICALEIF	HSICALEIC	Reserved	MSICALEIE	MSICALEIF	MSICALEIC	Reserved			
	rw	r	w		rw	r	w		rw	r	w				

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
30	HSERDIE	HSE ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by the external HSE oscillator stabilization. 0: HSE ready interrupt disabled 1: HSE ready interrupt enabled
29	HSERDIF	HSE ready interrupt flag. Set by hardware when HSE clock becomes stable and HSERDIE is set. Cleared by software setting the HSERDIC bit. 0: No clock ready interrupt caused by the external HSE oscillator 1: Clock ready interrupt caused by the external HSE oscillator
28	HSERDIC	HSE ready interrupt clear. This bit is set by software to clear the HSERDIF flag. 0: No effect 1: HSERDIF cleared
27	Reserved	Reserved, the reset value must be maintained.
26	HSIRDIE	HSI ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by the internal HSI oscillator stabilization. 0: HSI ready interrupt disabled 1: HSI ready interrupt enabled
25	HSIRDIF	HSI ready interrupt flag. Set by hardware when the Internal High Speed clock becomes stable and HSIRDIE is set. Cleared by software setting the HSIRDIC bit. 0: No clock ready interrupt caused by the internal HSI RC oscillator 1: Clock ready interrupt caused by the internal HSI RC oscillator
24	HSIRDIC	HSI ready interrupt clear. This bit is set software to clear the HSIRDIF flag. 0: No effect 1: HSIRDIF cleared
23	Reserved	Reserved, the reset value must be maintained.
22	MSIRDIE	MSI ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by the internal MSI oscillator stabilization. 0: MSI ready interrupt disabled 1: MSI ready interrupt enabled
21	MSIRDIF	MSI ready interrupt flag. Set by hardware when the Internal MSI clock becomes stable and MSIRDIE is set. Cleared by software setting the MSIRDIC bit. 0: No clock ready interrupt caused by the internal MSI oscillator 1: Clock ready interrupt caused by the internal MSI oscillator
20	MSIRDIC	MSI ready interrupt clear.

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Bit field	Name	Description
		This bit is set software to clear the MSIRDIF flag. 0: No effect 1: MSIRDIF cleared
19	Reserved	Reserved, the reset value must be maintained.
18	LSERDIE	LSE ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by the external LSE oscillator stabilization. 0: LSE ready interrupt disabled 1: LSE ready interrupt enabled
17	LSERDIF	LSE ready interrupt flag. Set by hardware when the External Low Speed clock becomes stable and LSERDIE is set.Cleared by software setting the LSERDIC bit. 0: No clock ready interrupt caused by the external LSE oscillator 1: Clock ready interrupt caused by the external LSE oscillator
16	LSERDIC	LSE ready interrupt clear. This bit is set by software to clear the LSERDIF flag. 0: No effect 1: LSERDIF cleared
15	Reserved	Reserved, the reset value must be maintained.
14	LSIRDIE	LSI ready interrupt enable. Set and cleared by software to enable/disable interrupt caused by internal LSI oscillator stabilization. 0: LSI ready interrupt disabled 1: LSI ready interrupt enabled
13	LSIRDIF	LSI ready interrupt flag. Set by hardware when the internal low speed clock becomes stable and LSIRDIE is set. Cleared by software setting the LSIRDIC bit. 0: No clock ready interrupt caused by the internal LSI oscillator 1: Clock ready interrupt caused by the internal LSI oscillator
12	LSIRDIC	LSI ready interrupt clear. This bit is set by software to clear the LSIRDIF flag. 0: No effect 1: LSIRDIF cleared
11	Reserved	Reserved, the reset value must be maintained.
10	HSICALEIE	HSI Trim Calibration Error Interrupt Enable. Set and cleared by software to enable/disable interrupt caused by internal HSI trim calibration error. 0: HSI Trim Calibration Error interrupt disabled 1: HSI Trim Calibration Error interrupt enabled
9	HSICALEIF	HSI Trim Calibration Error interrupt flag. Set by hardware when the internal low speed clock becomes stable and HSICALEIE is set.

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Bit field	Name	Description
		Cleared by software setting the HSICALEIC bit. 0: No HSI Trim calibration Error interrupt occured. 1: HSI Trim calibration interrupt Error occured.
8	HSICALEIC	HSI Trim Calibration Errorinterrupt clear. This bit is set by software to clear the HSICALEIF flag. 0: No effect 1: HSICALEIF cleared
7	Reserved	Reserved, the reset value must be maintained.
6	MSICALEIE	MSI Trim Calibration Error Interrupt Enable. Set and cleared by software to enable/disable interrupt caused by internal MSI trim calibration error. 0: MSI Trim Calibration Error interrupt disabled 1: MSI Trim Calibration Error interrupt enabled
5	MSICALEIF	MSI Trim Calibration Error interrupt flag. Set by hardware when the internal low speed clock becomes stable and MSICALEIE is set. Cleared by software setting the MSICALEIC bit. 0: No MSI Trim calibration Error interrupt occured. 1: MSI Trim calibration interrupt Error occured.
4	MSICALEIC	MSI Trim Calibration Errorinterrupt clear. This bit is set by software to clear the MSICALEIF flag. 0: No effect 1: MSICALEIF cleared
3:0	Reserved	Reserved, the reset value must be maintained.

4.5.86 Clock interrupt register 3(RCC_CLKINT3)

Address offset: 0x01d4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													PLL1LKFIE	PLL1LKFIF	PLL1LKFIC
													rw	r	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PLL2LKFIE	PLL2LKFIF	PLL2LKFIC	Reserved	PLL3LKFIE	PLL3LKFIF	PLL3LKFIC	Reserved	SHRPLLLKFIE	SHRPLLLKFIF	SHRPLLLKFIC	Reserved	LSIFIE	LSIFIF	LSIFIC
	rw	r	w		rw	r	w		rw	r	w		rw	r	w

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
18	PLL1LKFIE	PLL1 lock fail interrupt enable. Set and cleared by software to enable/disable interrupt caused by PLL1 lock failure. 0: PLL1 lock fail interrupt disabled 1: PLL1 lock fail interrupt enabled
17	PLL1LKFIF	PLL1 lock fail interrupt flag. Set by hardware when the PLL1 lock failure occurs and PLL1LKFIE is set.Cleared by software by setting the PLL1LKFIC bit. 0: No PLL lock fail interrupt 1: PLL lock fail interrupt
16	PLL1LKFIC	PLL1 lock fail interrupt clear. This bit is set by software to clear the PLL1LKFIF flag. 0: No effect 1: PLL1LKFIF cleared
15	Reserved	Reserved, the reset value must be maintained.
14	PLL2LKFIE	PLL2 lock fail interrupt enable. Set and cleared by software to enable/disable interrupt caused by PLL2 lock failure. 0: PLL2 lock fail interrupt disabled 1: PLL2 lock fail interrupt enabled
13	PLL2LKFIF	PLL2 lock fail interrupt flag. Set by hardware when the PLL2 lock failure occurs and PLL2LKFIE is set.Cleared by software by setting the PLL2LKFIC bit. 0: No PLL lock fail interrupt 1: PLL lock fail interrupt
12	PLL2LKFIC	PLL2 lock fail interrupt clear. This bit is set by software to clear the PLL2LKFIF flag. 0: No effect 1: PLL2LKFIF cleared
11	Reserved	Reserved, the reset value must be maintained.
10	PLL3LKFIE	PLL3 lock fail interrupt enable. Set and cleared by software to enable/disable interrupt caused by PLL3 lock failure. 0: PLL3 lock fail interrupt disabled 1: PLL3 lock fail interrupt enabled
9	PLL3LKFIF	PLL3 lock fail interrupt flag. Set by hardware when the PLL3 lock failure occurs and PLL3LKFIE is set.Cleared by software by setting the PLL3LKFIC bit. 0: No PLL lock fail interrupt 1: PLL lock fail interrupt
8	PLL3LKFIC	PLL3 lock fail interrupt clear. This bit is set by software to clear the PLL3LKFIF flag. 0: No effect 1: PLL3LKFIF cleared

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Bit field	Name	Description
7	Reserved	Reserved, the reset value must be maintained.
6	SHRPLLLKFIE	SHRPLL lock fail interrupt enable. Set and cleared by software to enable/disable interrupt caused by SHRPLL lock failure. 0: SHRPLL lock fail interrupt disabled 1: SHRPLL lock fail interrupt enabled
5	SHRPLLLKFIF	SHRPLL lock fail interrupt flag. Set by hardware when the SHRPLL lock failure occurs and SHRPLLLKFIE is set.Cleared by software by setting the SHRPLLLKFIC bit. 0: No PLL lock fail interrupt 1: PLL lock fail interrupt
4	SHRPLLLKFIC	SHRPLL lock fail interrupt clear. This bit is set by software to clear the SHRPLLLKFIF flag. 0: No effect 1: SHRPLLLKFIF cleared
3	Reserved	Reserved, the reset value must be maintained.
2	LSIFIE	LSI fail interrupt enable. Set and cleared by software to enable/disable interrupt caused by LSI fail detection. 0: LSI fail interrupt disabled 1: LSI fail interrupt enabled
1	LSIFIF	LSI fail interrupt flag. Set by hardware when a failure is detected in the internal 32 kHz oscillator and LSIFIE is set. Cleared by software setting the LSIFIC bit. 0: No interrupt caused by LSI clock failure 1: Interrupt caused by LSI clock failure
0	LSIFIC	LSI fail interrupt clear. This bit is set by software to clear the LSIFIF flag. 0: No effect 1: Clear LSIFIF flag

4.5.87 Clock configure register 1(RCC_CFG1)

Address offset: 0x0134

Reset value: 0x00aa0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								WWDG2RSTDLCNT[3:0]				WWDG1RSTDLCNT[3:0]			
									rw				rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						WWDG2RSTEN	WWDG1RSTEN	M7TRACEDIV[3:0]				M4TRACEDIV[3:0]			

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rw rw rw rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:20	WWDG2RSTDLCNT[3:0]	Counter threshold used to delay the assertion of WWDG2 reset when WWDG2 reset request event occurs.
19:16	WWDG1RSTDLCNT[3:0]	Counter threshold used to delay the assertion of WWDG1 reset when WWDG1 reset request event occurs.
15:10	Reserved	Reserved, the reset value must be maintained.
9	WWDG2RSTEN	WWDG2 Reset Request Enable. Set and cleared by software. 0: WWDG2 reset request will reset M4 CPU. 1: WWDG2 reset request will cause NRST reset.
8	WWDG1RSTEN	WWDG1 Reset Request Enable. Set and cleared by software. 0: WWDG1 reset request will reset M7 CPU. 1: WWDG1 reset request will cause NRST reset.
7:4	M7TRACEDIV[3:0]	M7 trace clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512
3:0	M4TRACEDIV[3:0]	M4 trace clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512

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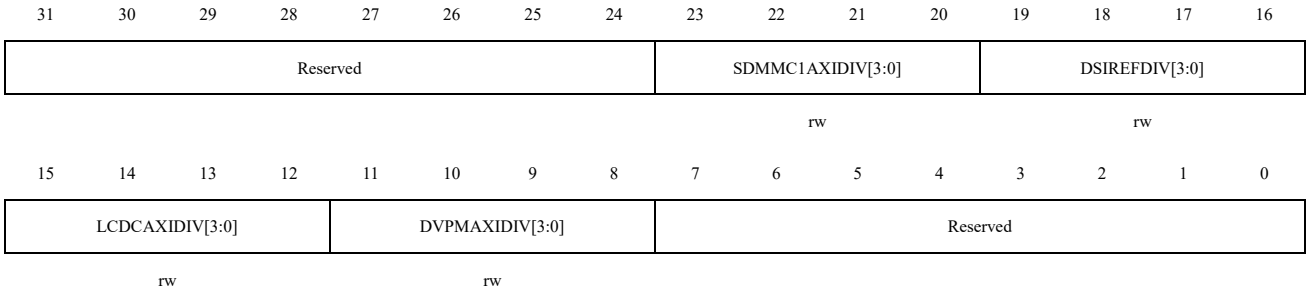
4.5.88 AXI peripherals clock divider register 1(RCC_AXIDIV1)

Address offset: 0x0138

Reset value: 0x00000000



Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
23:20	SDMMC1AXIDIV[3:0]	SDMMC1 AXI clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
19:16	DSIREFDIV[3:0]	DSI reference clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
15:12	LCDCAXIDIV[3:0]	LCDC AXI clock prescalar values. 0000: Divide by 1

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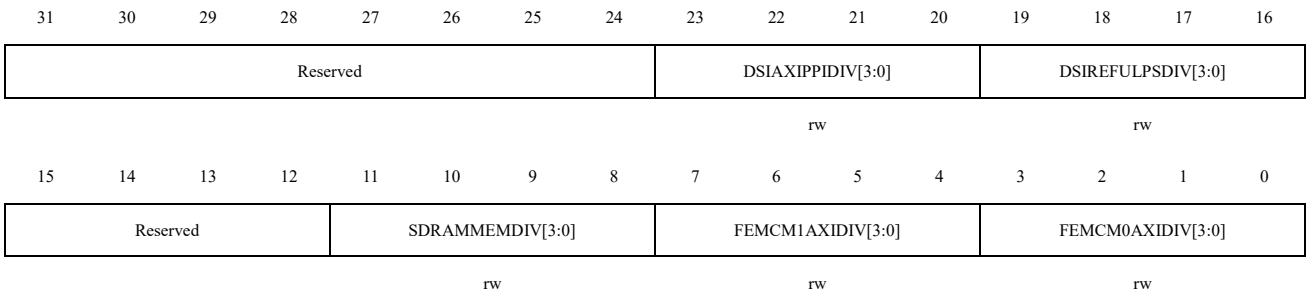
Bit field	Name	Description
		0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
11:8	DVPMAXIDIV[3:0]	DVP M clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
7:0	Reserved	Reserved, the reset value must be maintained.

4.5.89 AXI peripherals clock divider register 2(RCC_AXIDIV2)

Address offset: 0x0178

Reset value: 0x00000000



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
23:20	DSIAXIPPIDIV[3:0]	DSI AXI PPI clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
19:16	DSIREFULPSDIV[3:0]	DSI REF ULPS clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
15:12	Reserved	Reserved, the reset value must be maintained.
11:8	SDRAMMEMDIV[3:0]	SDRAM clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
7:4	FEMCM1AXIDIV[3:0]	FEMC M1 AXI clock prescalar values. 0001: Divide by 1 (bypass) 0010: Divide by 2 0011: Divide by 3 0100: Divide by 4

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Bit field	Name	Description
		0101: Divide by 5 0110: Divide by 6 0111: Divide by 7 1000: Divide by 8 1001: Divide by 9 1010: Divide by 10 1011: Divide by 11 1100: Divide by 12 1101: Divide by 13 1110: Divide by 14 1111: Divide by 15
3:0	FEMCM0AXIDIV[3:0]	FEMC M0 AXI clock prescalar values. 0001: Divide by 1 (bypass) 0010: Divide by 2 0011: Divide by 3 0100: Divide by 4 0101: Divide by 5 0110: Divide by 6 0111: Divide by 7 1000: Divide by 8 1001: Divide by 9 1010: Divide by 10 1011: Divide by 11 1100: Divide by 12 1101: Divide by 13 1110: Divide by 14 1111: Divide by 15

4.5.90 AXI peripherals clock source select register 1(RCC_AXISEL1)

Address offset: 0x013c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				DSIULPSSEL[1:0]		DSIKERSEL[1:0]		Reserved	SDMMC1KERSEL[2:0]			Reserved		DSIPPITXSEL[1:0]	
				rw		rw			rw					rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		LCDCKERSEL[1:0]		DVP1MSEL[1:0]		DVP2MSEL[1:0]		Reserved	XSPI1SSISEL[2:0]			Reserved	XSPI2SSISEL[2:0]		
		rw		rw		rw			rw				rw		

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Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:26	DSIULPSSEL[1:0]	DSI ULPS clock selection. 00: DSI reference clock is selected as DSI ULPS clock. 01: PLL3_C clock is selected as DSI ULPS clock. Other values: setting is not allowed
25:24	DSIKERSEL[1:0]	DSI Kernel clock selection. 00: DSI reference clock is selected as DSI kernel clock. 01: PLL3_C clock is selected as DSI kernel clock. Other values: setting is not allowed
23	Reserved	Reserved, the reset value must be maintained.
22:20	SDMMC1KERSEL[2:0]	SDMMC1 Kernel clock selection. 000: Divided AXI bus clock is selected as SDMMC1 kernel clock. 001: Peripheral clock is selected as SDMMC1 kernel clock. 010: PLL2_A clock is selected as SDMMC1 kernel clock. 011: PLL3_A clock is selected as SDMMC1 kernel clock. 100: PLL1_B clock is selected as SDMMC1 kernel clock. Other values: setting is not allowed
19:18	Reserved	Reserved, the reset value must be maintained.
17:16	DSIPPITXSEL[1:0]	DSI PPI clock selection. 00: Divided DSI reference clock clock is selected as DSI PPI clock . 01: PLL2_B clock is selected as DSI PPI clock . 10: Peripheral clock is selected as DSI PPI clock . 11: Divided AXI bus clock is selected as DSI PPI clock .
15:14	Reserved	Reserved, the reset value must be maintained.
13:12	LCDCKERSEL[1:0]	LCDC Kernel clock selection. 00: Divided AXI bus clock is selected as LCDC kernel clock. 01: Peripheral clock is selected as LCDC kernel clock. 10: PLL2_C clock is selected as LCDC kernel clock. 11: PLL3_B clock is selected as LCDC kernel clock.
11:10	DVP1MSEL[1:0]	DVP1 M clock selection. 00: Divided AXI bus clock is selected as DVP1 M clock. 01: Peripheral clock is selected as DVP1 M clock. 10: PLL2_C clock is selected as DVP1 M clock. 11: PLL3_A clock is selected as DVP1 M clock.
9:8	DVP2MSEL[1:0]	DVP2 M clock selection. 00: Divided AXI bus clock is selected as DVP2 M clock. 01: Peripheral clock is selected as DVP2 M clock. 10: PLL2_C clock is selected as DVP2 M clock. 11: PLL3_A clock is selected as DVP2 M clock.
7	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
6:4	XSPI1SSISEL[2:0]	XSPI1 SSI clock clock selection. 000: AXI bus clock is selected as XSPI1 SSI clock. 001: PLL3_C clock is selected as XSPI1 SSI clock. 010: PLL1_B clock is selected as XSPI1 SSI clock. 011: PLL2_A clock is selected as XSPI1 SSI clock. 100: PLL2_C clock is selected as XSPI1 SSI clock. Other values: setting is not allowed
3	Reserved	Reserved, the reset value must be maintained.
2:0	XSPI2SSISEL[2:0]	XSPI2 SSI clock clock selection. 000: AXI bus clock is selected as XSPI2 SSI clock. 001: PLL3_C clock is selected as XSPI2 SSI clock. 010: PLL1_B clock is selected as XSPI2 SSI clock. 011: PLL2_A clock is selected as XSPI2 SSI clock. 100: PLL2_C clock is selected as XSPI2 SSI clock. Other values: setting is not allowed

4.5.91 AXI peripherals clock source select register 2(RCC_AXISEL2)

Address offset: 0x017c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SDRAMMEMSEL[2:0]			Reserved	FEMCM1SEL[2:0]			Reserved	FEMCM0SEL[2:0]		
					rw				rw				rw		

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:8	SDRAMMEMSEL[2:0]	SDRAM clock selection. 000: Divided AXI bus clock is selected as SDRAM mem clock. 001: Peripheral clock is selected as SDRAM mem clock. 010: PLL2_A clock is selected as SDRAM mem clock. 011: PLL3_A clock is selected as SDRAM mem clock. 100: PLL1_B clock is selected as SDRAM mem clock. Other values: setting is not allowed
7	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
6:4	FEMCM1SEL[2:0]	FEMC M1 clock selection. 000: Divided AXI bus clock is selected as FEMC M1 clock. 001: Peripheral clock is selected as FEMC M1 clock. 010: PLL2_C clock is selected as FEMC M1 clock. 011: PLL3_B clock is selected as FEMC M1 clock. 100: PLL1_B clock is selected as FEMC M1 clock. Other values: setting is not allowed
3	Reserved	Reserved, the reset value must be maintained.
2:0	FEMCM0SEL[2:0]	FEMC M0 clock selection. 000: Divided AXI bus clock is selected as FEMC M0 clock. 001: Peripheral clock is selected as FEMC M0 clock. 010: PLL2_C clock is selected as FEMC M0 clock. 011: PLL3_B clock is selected as FEMC M0 clock. 100: PLL1_B clock is selected as FEMC M0 clock. Other values: setting is not allowed

4.5.92 AXI peripherals clock enable register 1(RCC_AXIEN1)

Address offset: 0x0140

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7JPEGDEN	M4JPEGDEN	M7JPEGDLPEN	M4JPEGDLPEN	Reserved				M7JPEGEEN	M4JPEGEEN	M7JPEGELPEN	M4JPEGELPEN	M7DMAMUX2EN	M4DMAMUX2EN	M7DMAMUX2LPEN	M4DMAMUX2LPEN
rw	rw	rw	rw					rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7MDMAEN	M4MDMAEN	M7MDMALPEN	M4MDMALPEN	M7SDMMC1EN	M4SDMMC1EN	M7SDMMC1LPEN	M4SDMMC1LPEN	M7ECCM1EN	M4ECCM1EN	M7ECCM1LPEN	M4ECCM1LPEN	M7OTPCEN	M4OTPCEN	M7OTPCLPEN	M4OTPCLPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7JPEGDEN	JPEG Decoder M7 allocation and clock enable. Set and cleared by software. 0: JPEG Decoder is not allocated to M7. The "jpeg_dec_gated_axi_clk" is disabled in M7 RUN mode. 1: JPEG Decoder is allocated to M7. The"jpeg_dec_gated_axi_clk" is enabled in M7 RUN mode.
30	M4JPEGDEN	JPEG Decoder M4 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: JPEG Decoder is not allocated to M4. The"jpeg_dec_gated_axi_clk" is disabled in M4 RUN mode. 1: JPEG Decoder is allocated to M4. The "jpeg_dec_gated_axi_clk" is enabled in M4 RUN mode.
29	M7JPEGDLPEN	JPEG Decoder M7 Low Power clock Enable. Set and cleared by software. 0: The "jpeg_dec_gated_axi_clk" clock is disabled in M7 SLEEP and STOP mode. 1:The "jpeg_dec_gated_axi_clk" is enabled in M7 SLEEP mode. Note : M7JPEGDEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
28	M4JPEGDLPEN	JPEG Decoder M4 Low Power clock Enable. Set and cleared by software. 0: The "jpeg_dec_gated_axi_clk" clock is disabled in M4 SLEEP and STOP mode. 1:The "jpeg_dec_gated_axi_clk" is enabled in M4 SLEEP mode. Note : M4JPEGDEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
27:24	Reserved	Reserved, the reset value must be maintained.
23	M7JPEGEEN	JPEG Encoder M7 allocation and clock enable. Set and cleared by software. 0: JPEG Encoder is not allocated to M7. The "jpeg_enc_gated_axi_clk" is disabled in M7 RUN mode. 1: JPEG Encoder is allocated to M7. The"jpeg_enc_gated_axi_clk" is enabled in M7 RUN mode.
22	M4JPEGEEN	JPEG Encoder M4 allocation and clock enable. Set and cleared by software. 0: JPEG Encoder is not allocated to M4. The "jpeg_enc_gated_axi_clk" is disabled in M4 RUN mode. 1: JPEG Encoder is allocated to M4. The"jpeg_enc_gated_axi_clk" is enabled in M4 RUN mode.
21	M7JPEGELPEN	JPEG Encoder M7 Low Power clock Enable. Set and cleared by software. 0: The "jpeg_enc_gated_axi_clk" clock is disabled in M7 SLEEP and STOP mode. 1:The "jpeg_enc_gated_axi_clk" is enabled in M7 SLEEP mode. Note : M7JPEGEEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
20	M4JPEGELPEN	JPEG Encoder M4 Low Power clock Enable. Set and cleared by software. 0: The "jpeg_enc_gated_axi_clk" clock is disabled in M4 SLEEP and STOP mode. 1:The "jpeg_enc_gated_axi_clk" is enabled in M4 SLEEP mode. Note : M4JPEGEEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
19	M7DMAMUX2EN	DMAMUX2 M7 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: DMAMUX2 is not allocated to M7. The "dma_mux2_gated_hclk" is disabled in M7 RUN mode. 1: DMAMUX2 is allocated to M7. The "dma_mux2_gated_hclk" is enabled in M7 RUN mode.
18	M4DMAMUX2EN	DMAMUX2 M4 allocation and clock enable. Set and cleared by software. 0: DMAMUX2 is not allocated to M4. The "dma_mux2_gated_hclk" is disabled in M4 RUN mode. 1: DMAMUX2 is allocated to M4. The "dma_mux2_gated_hclk" is enabled in M4 RUN mode.
17	M7DMAMUX2LPEN	DMAMUX2 M7 Low Power clock Enable. Set and cleared by software. 0: The "dma_mux2_gated_hclk" clock is disabled in M7 SLEEP and STOP mode. 1:The "dma_mux2_gated_hclk" is enabled in M7 SLEEP mode. Note : M7_DMAMUX2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4DMAMUX2LPEN	DMAMUX2 M4 Low Power clock Enable. Set and cleared by software. 0: The "dma_mux2_gated_hclk" clock is disabled in M4 SLEEP and STOP mode. 1:The "dma_mux2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4_DMAMUX2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7MDMAEN	MDMA M7 allocation and clock enable. Set and cleared by software. 0: MDMA is not allocated to M7. The "mdma_gated_axi_clk" and "mdma_gated_hclk" are disabled in M7 RUN mode. 1: MDMA is allocated to M7. The "mdma_gated_axi_clk" and "mdma_gated_hclk" are enabled in M7 RUN mode.
14	M4MDMAEN	MDMA M4 allocation and clock enable. Set and cleared by software. 0: MDMA is not allocated to M4. The "mdma_gated_axi_clk" and "mdma_gated_hclk" are disabled in M4 RUN mode. 1: MDMA is allocated to M4. The "mdma_gated_axi_clk" and "mdma_gated_hclk" are enabled in M4 RUN mode.
13	M7MDMALPEN	MDMA M7 Low Power clock Enable. Set and cleared by software. 0: The "mdma_gated_axi_clk" and "mdma_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1:The "mdma_gated_axi_clk" is enabled in M7 SLEEP and STOP mode. "mdma_gated_hclk" is enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7MDMAEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
12	M4MDMALPEN	MDMA M4 Low Power clock Enable. Set and cleared by software. 0: The "mdma_gated_axi_clk" and "mdma_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1:The "mdma_gated_axi_clk" is enabled in M4 SLEEP and STOP mode. "mdma_gated_hclk" is enabled in M4 SLEEP mode. Note : M4MDMAEN bitshould be enabled before enabling this bit, otherwise this bit has no effect.
11	M7SDMMC1EN	SDMMC1 M7 allocation and clock enable. Set and cleared by software. 0: SDMMC1 is not allocated to M7. The "sdmmc1_gated_ker_clk" and "sdmmc1_gated_hclk" are disabled in M7 RUN mode. 1: SDMMC1 is allocated to M7. The "sdmmc1_gated_ker_clk" and "sdmmc1_gated_hclk" are enabled in M7 RUN mode.
10	M4SDMMC1EN	SDMMC1 M4 allocation and clock enable. Set and cleared by software. 0: SDMMC1 is not allocated to M4. The "sdmmc1_gated_ker_clk" and "sdmmc1_gated_hclk" are disabled in M4 RUN mode. 1: SDMMC1 is allocated to M4. The "sdmmc1_gated_ker_clk" and "sdmmc1_gated_hclk" are enabled in M4 RUN mode.
9	M7SDMMC1LPEN	SDMMC1 M7 Low Power clock Enable. Set and cleared by software. 0: The "sdmmc1_gated_ker_clk" and "sdmmc1_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1:The "sdmmc1_gated_ker_clk" is enabled in M7 SLEEP and STOP mode. "sdmmc1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7SDMMC1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4SDMMC1LPEN	SDMMC1 M4 Low Power clock Enable. Set and cleared by software. 0: The "sdmmc1_gated_ker_clk" and "sdmmc1_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1:The "sdmmc1_gated_ker_clk" is enabled in M4 SLEEP and STOP mode. "sdmmc1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4SDMMC1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7ECCM1EN	ECCMON1 M7 allocation and clock enable. Set and cleared by software. 0: ECCMON1 is not allocated to M7. The "eccmon1_gated_hclk" is disabled in M7 RUN mode.

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Bit field	Name	Description
		1: ECCMON1 is allocated to M7. The "eccmon1_gated_hclk" is enabled in M7 RUN mode.
6	M4ECCM1EN	ECCMON1 M4 allocation and clock enable. Set and cleared by software. 0: ECCMON1 is not allocated to M4. The "eccmon1_gated_hclk" is disabled in M4 RUN mode. 1: ECCMON1 is allocated to M4. The "eccmon1_gated_hclk" is enabled in M4 RUN mode.
5	M7ECCM1LPEN	ECCMON1 M7 Low Power clock Enable. Set and cleared by software. 0: The "eccmon1_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1:The "eccmon1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7ECCM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4ECCM1LPEN	ECCMON1 M4 Low Power clock Enable. Set and cleared by software. 0: The "eccmon1_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1:The "eccmon1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4ECCM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7OTPCEN	OTPC M7 allocation and clock enable. Set and cleared by software. 0: OTPC is not allocated to M7. The "otpc_gated_hclk" is disabled in M7 RUN mode. 1: OTPC is allocated to M7. The "otpc_gated_hclk" is enabled in M7 RUN mode.
2	M4OTPCEN	OTPC M4 allocation and clock enable. Set and cleared by software. 0: OTPC is not allocated to M4. The "otpc_gated_hclk" is disabled in M4 RUN mode. 1: OTPC is allocated to M4. The "otpc_gated_hclk" is enabled in M4 RUN mode.
1	M7OTPCLPEN	M7 Low Power clock Enable. Set and cleared by software. 0: The "otpc_gated_hclk" clocks is disabled in M7 SLEEP and STOP mode. 1:The "otpc_gated_hclk" is enabled in M7 SLEEP mode. Note : M7OTPCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4OTPCLPEN	M4 Low Power clock Enable. Set and cleared by software. 0: The "otpc_gated_hclk" clocks is disabled in M4 SLEEP and STOP mode. 1:The "otpc_gated_hclk" is enabled in M4 SLEEP mode. Note : M4OTPCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.93 AXI peripherals clock enable register 2(RCC_AXIEN2)

Address offset: 0x0144

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Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7DSIEN	M4DSIEN	M7DSILPEN	M4DSILPEN	M7LCDCEN	M4LCDCEN	M7LCDCLPEN	M4LCDCLPEN	M7LCDCAPBEN	M4LCDCAPBEN	M7LCDCAPBLPEN	M4LCDAPBLPEN	M7DVP1EN	M4DVP1EN	M7DVP1LPEN	M4DVP1LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7DVP1APBEN	M4DVP1APBEN	M7DVP1APBLPEN	M4DVP1APBLPEN	M7DVP2EN	M4DVP2EN	M7DVP2LPEN	M4DVP2LPEN	M7DVP2APBEN	M4DVP2APBEN	M7DVP2APBLPEN	M4DVP2APBLPEN	M7WWDG1EN	M4WWDG1EN	M7WWDG1LPEN	M4WWDG1LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7DSIEN	DSI M7 allocation and clock enable. Set and cleared by software. 0: DSI is not allocated to M7. The "dsi_ppi_txclkesc_all_gated_clk" and "dsi_gated_pclk" are disabled in M7 RUN mode. 1: DSI is allocated to M7. The "dsi_ppi_txclkesc_all_gated_clk"and "dsi_gated_pclk" are enabled in M7 RUN mode.
30	M4DSIEN	DSI M4 allocation and clock enable. Set and cleared by software. 0: DSI is not allocated to M4. The "dsi_ppi_txclkesc_all_gated_clk"and "dsi_gated_pclk" are disabled in M4 RUN mode. 1: DSI is allocated to M4. The "dsi_ppi_txclkesc_all_gated_clk"and "dsi_gated_pclk" are enabled in M4 RUN mode.
29	M7DSILPEN	DSI M7 Low Power clock Enable. Set and cleared by software. 0: The "dsi_ppi_txclkesc_all_gated_clk"and "dsi_gated_pclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "dsi_ppi_txclkesc_all_gated_clk"is enabled in M7 SLEEP and STOP mode. "dsi_gated_pclk" is enabled in M7 SLEEP mode. Note : M7DSIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4DSILPEN	DSI M4 Low Power clock Enable. Set and cleared by software. 0: The "dsi_ppi_txclkesc_all_gated_clk"and "dsi_gated_pclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "dsi_ppi_txclkesc_all_gated_clk" is enabled in M4 SLEEP and STOP mode. "dsi_gated_pclk" is enabled in M4 SLEEP mode. Note : M4DSIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7LCDCEN	LCDC M7 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: LCDC is not allocated to M7. The "lcdc_gated_pixel_clk" and "lcdc_gated_axi_clk" are disabled in M7 RUN mode. 1: LCDC is allocated to M7. The "lcdc_gated_pixel_clk" and "lcdc_gated_axi_clk" are enabled in M7 RUN mode.
26	M4LCDCEN	LCDC M4 allocation and clock enable. Set and cleared by software. 0: LCDC is not allocated to M4. The "lcdc_gated_pixel_clk" and "lcdc_gated_axi_clk" are disabled in M4 RUN mode. 1: LCDC is allocated to M4. The "lcdc_gated_pixel_clk" and "lcdc_gated_axi_clk" are enabled in M4 RUN mode.
25	M7LCDCLPEN	LCDC M7 Low Power clock Enable. Set and cleared by software. 0: The "lcdc_gated_pixel_clk" and "lcdc_gated_axi_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "lcdc_gated_pixel_clk" is enabled in M7 SLEEP and STOP mode. "lcdc_gated_axi_clk" is enabled in M7 SLEEP mode. Note : M7LCDCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4LCDCLPEN	LCDC M4 Low Power clock Enable. Set and cleared by software. 0: The "lcdc_gated_pixel_clk" and "lcdc_gated_axi_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "lcdc_gated_pixel_clk" is enabled in M4 SLEEP and STOP mode. "lcdc_gated_axi_clk" is enabled in M4 SLEEP mode. Note : M4LCDCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7LCDCAPBEN	LCDC APB M7 allocation and clock enable. Set and cleared by software. 0: LCDC APB bus is not allocated to M7. The "lcdc_gated_pclk" is disabled in M7 RUN mode. 1: LCDC APB bus is allocated to M7. The "lcdc_gated_pclk" is enabled in M7 RUN mode.
22	M4LCDCAPBEN	LCDC APB M4 allocation and clock enable. Set and cleared by software. 0: LCDC APB bus is not allocated to M4. The "lcdc_gated_pclk" is disabled in M4 RUN mode. 1: LCDC APB bus is allocated to M4. The "lcdc_gated_pclk" is enabled in M4 RUN mode.
21	M7LCDCAPBLPEN	LCDC APB M7 Low Power clock Enable. Set and cleared by software. 0: The "lcdc_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "lcdc_gated_pclk" is enabled in M7 SLEEP mode. Note : M7LCDCAPBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Bit field	Name	Description
20	M4LCDCAPBLPEN	LCDC APB M4 Low Power clock Enable. Set and cleared by software. 0: The "lcdc_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "lcdc_gated_pclk" is enabled in M4 SLEEP mode. Note : M4LCDCAPBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7DVP1EN	DVP1 M7 allocation and clock enable. Set and cleared by software. 0: DVP1 is not allocated to M7. The "dvp1_gated_m_clk" and "dvp1_gated_hclk" are disabled in M7 RUN mode. 1: DVP1 is allocated to M7. The "dvp1_gated_m_clk" and "dvp1_gated_hclk" are enabled in M7 RUN mode.
18	M4DVP1EN	DVP1 M4 allocation and clock enable. Set and cleared by software. 0: DVP1 is not allocated to M4. The"dvp1_gated_m_clk" and "dvp1_gated_hclk" are disabled in M4 RUN mode. 1: DVP1 is allocated to M4. The "dvp1_gated_m_clk" and "dvp1_gated_hclk" are enabled in M4 RUN mode.
17	M7DVP1LPEN	DVP1 M7 Low Power clock Enable. Set and cleared by software. 0: The"dvp1_gated_m_clk" and "dvp1_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "dvp1_gated_m_clk" is enabled in M7 SLEEP and STOP mode. "dvp1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DVP1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4DVP1LPEN	DVP1 M4 Low Power clock Enable. Set and cleared by software. 0: The "dvp1_gated_m_clk" and "dvp1_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The"dvp1_gated_m_clk" is enabled in M4 SLEEP and STOP mode. "dvp1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4DVP1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7DVP1APBEN	DVP1 APB M7 allocation and clock enable. Set and cleared by software. 0: DVP1 APB bus is not allocated to M7. The "dvp1_gated_pclk" is disabled in M7 RUN mode. 1: DVP1 APB bus is allocated to M7. The "dvp1_gated_pclk" is enabled in M7 RUN mode.
14	M4DVP1APBEN	DVP1 APB M4 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: DVP1 APB bus is not allocated to M4. The "dvp1_gated_pclk" is disabled in M4 RUN mode. 1: DVP1 APB bus is allocated to M4. The "dvp1_gated_pclk" is enabled in M4 RUN mode.
13	M7DVP1APBLPEN	DVP1 APB M7 Low Power clock Enable. Set and cleared by software. 0: The "dvp1_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "dvp1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7DVP1APBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4DVP1APBLPEN	DVP1 APB M4 Low Power clock Enable. Set and cleared by software. 0: The "dvp1_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "dvp1_gated_pclk" is enabled in M4 SLEEP mode. Note : M4DVP1APBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7DVP2EN	DVP2 M7 allocation and clock enable. Set and cleared by software. 0: DVP2 is not allocated to M7. The"dvp2_gated_m_clk" and "dvp2_gated_hclk" are disabled in M7 RUN mode. 1: DVP2 is allocated to M7. The "dvp2_gated_m_clk" and "dvp2_gated_hclk" are enabled in M7 RUN mode.
10	M4DVP2EN	DVP2 M4 allocation and clock enable. Set and cleared by software. 0: DVP2 is not allocated to M4. The "dvp2_gated_m_clk" and "dvp2_gated_hclk" are disabled in M4 RUN mode. 1: DVP2 is allocated to M4. The "dvp2_gated_m_clk" and "dvp2_gated_hclk" are enabled in M4 RUN mode.
9	M7DVP2LPEN	DVP2 M7 Low Power clock Enable. Set and cleared by software. 0: The "dvp2_gated_m_clk" and "dvp2_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "dvp2_gated_m_clk" is enabled in M7 SLEEP and STOP mode. "dvp2_gated_hclk" is enabled in M7 SLEEP mode. Note : M7DVP2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4DVP2LPEN	DVP2 M4 Low Power clock Enable. Set and cleared by software. 0: The "dvp2_gated_m_clk" and "dvp2_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The"dvp2_gated_m_clk" is enabled in M4 SLEEP and STOP mode. "dvp2_gated_hclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4DVP2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7DVP2APBEN	DVP2 APB M7 allocation and clock enable. Set and cleared by software. 0: DVP2 APB bus is not allocated to M7. The "dvp2_gated_pclk" is disabled in M7 RUN mode. 1: DVP2 APB bus is allocated to M7. The "dvp2_gated_pclk" is enabled in M7 RUN mode.
6	M4DVP2APBEN	DVP2 APB M4 allocation and clock enable. Set and cleared by software. 0: DVP2 APB bus is not allocated to M4. The "dvp2_gated_pclk" is disabled in M4 RUN mode. 1: DVP2 APB bus is allocated to M4. The "dvp2_gated_pclk" is enabled in M4 RUN mode.
5	M7DVP2APBLPEN	DVP2 APB M7 Low Power clock Enable. Set and cleared by software. 0: The "dvp2_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "dvp2_gated_pclk" is enabled in M7 SLEEP mode. Note : M7DVP2APBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4DVP2APBLPEN	DVP2 APB M4 Low Power clock Enable. Set and cleared by software. 0: The "dvp2_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "dvp2_gated_pclk" is enabled in M4 SLEEP mode. Note : M4DVP2APBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7WWDG1EN	WWDG1 M7 allocation and clock enable. Set and cleared by software. 0: WWDG1 is not allocated to M7. The "wwdg1_gated_pclk" is disabled in M7 RUN mode. 1: WWDG1 is allocated to M7. The "wwdg1_gated_pclk" is enabled in M7 RUN mode.
2	M4WWDG1EN	WWDG1 M4 allocation and clock enable. Set and cleared by software. 0: WWDG1 is not allocated to M4. The "wwdg1_gated_pclk" is disabled in M4 RUN mode. 1: WWDG1 is allocated to M4. The "wwdg1_gated_pclk" is enabled in M4 RUN mode.
1	M7WWDG1LPEN	WWDG1 M7 Low Power clock Enable. Set and cleared by software. 0: The "wwdg1_gated_pclk" clock is disabled in M7 SLEEP and STOP mode. 1: The "wwdg1_gated_pclk" is enabled in M7 SLEEP mode. Note : M7WWDG1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4WWDG1LPEN	WWDG1 M4 Low Power clock Enable. Set and cleared by software. 0: The "wwdg1_gated_pclk" clock is disabled in M4 SLEEP and STOP mode. 1: The "wwdg1_gated_pclk" is enabled in M4 SLEEP mode.

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Bit field	Name	Description
		Note : M4WWDG1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.94 AXI peripherals clock enable register 3(RCC_AXIEN3)

Address offset: 0x0148

Reset value: 0x88888880

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7TASRAM2EN	M4TASRAM2EN	M7TASRAM2LPEN	M4TASRAM2LPEN	M7TASRAM3EN	M4TASRAM3EN	M7TASRAM3LPEN	M4TASRAM3LPEN	M7TCMEN	M4TCMEN	M7TCMLPEN	M4TCMLPEN	M7TCMAXIEN	M4TCMAXIEN	M7TCMAXILPEN	M4TCMAXILPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7TCMAPBEN	M4TCMAPBEN	M7TCMAPBLPEN	M4TCMAPBLPEN	M7ASRAM1EN	M4ASRAM1EN	M7ASRAM1LPEN	M4ASRAM1LPEN	M7AXIROMEN	M4AXIROMEN	M7AXIROMLPEN	M4AXIROMLPEN	M7GPUEN	M4GPUEN	M7GPULPEN	M4GPULPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	M7TASRAM2EN	TCM_AXISRAM2 M7 allocation and clock enable. Set and cleared by software. 0: TCM_AXISRAM2 is not allocated to M7. The "tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" are disabled in M7 RUN mode. 1: TCM_AXISRAM2 is allocated to M7. The "tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" are enabled in M7 RUN mode.
30	M4TASRAM2EN	TCM_AXISRAM2 M4 allocation and clock enable. Set and cleared by software. 0: TCM_AXISRAM2 is not allocated to M4. The "tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" are disabled in M4 RUN mode. 1: TCM_AXISRAM2 is allocated to M4. The "tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" are enabled in M4 RUN mode.
29	M7TASRAM2LPEN	TCM_AXISRAM2 M7 Low Power clock Enable. Set and cleared by software. 0: The "tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The"tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" are enabled in M7 SLEEP mode. Note : M7TASRAM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4TASRAM2LPEN	TCM_AXISRAM2 M4 Low Power clock Enable.

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Bit field	Name	Description
		Set and cleared by software. 0: The "tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The"tcm_axisram2_gated_axi_clk" and "tcm_axiramc2_gated_axi_clk" are enabled in M4 SLEEP mode. Note : M4TASRAM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7TASRAM3EN	TCM_AXISRAM3 M7 allocation and clock enable. Set and cleared by software. 0: TCM_AXISRAM3 is not allocated to M7. The "tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" are disabled in M7 RUN mode. 1: TCM_AXISRAM3 is allocated to M7. The "tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" are enabled in M7 RUN mode.
26	M4TASRAM3EN	TCM_AXISRAM3 M4 allocation and clock enable. Set and cleared by software. 0: TCM_AXISRAM3 is not allocated to M4. The "tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" are disabled in M4 RUN mode. 1: TCM_AXISRAM3 is allocated to M4. The "tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" are enabled in M4 RUN mode.
25	M7TASRAM3LPEN	TCM_AXISRAM3 M7 Low Power clock Enable. Set and cleared by software. 0: The "tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The"tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" are enabled in M7 SLEEP mode. Note : M7TASRAM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
24	M4TASRAM3LPEN	TCM_AXISRAM3 M4 Low Power clock Enable. Set and cleared by software. 0: The "tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The"tcm_axisram3_gated_axi_clk" and "tcm_axiramc3_gated_axi_clk" are enabled in M4 SLEEP mode. Note : M4TASRAM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7TCMEN	TCM Core M7 allocation and clock enable. Set and cleared by software. 0: TCM Core is not allocated to M7. "tcm_gated_core_clk" is disabled in M7 RUN mode. 1: TCM Core is allocated to M7. The "tcm_gated_core_clk" is enabled in M7 RUN mode.
22	M4TCMEN	TCM Core M4 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: TCM Core is not allocated to M4. "tcm_gated_core_clk" is disabled in M4 RUN mode. 1: TCM Core is allocated to M4. The "tcm_gated_core_clk" is enabled in M4 RUN mode.
21	M7TCMLPEN	TCM Core M7 Low Power clock Enable. Set and cleared by software. 0: The "tcm_gated_core_clk" is disabled in M7 SLEEP and STOP mode. 1: The "tcm_gated_core_clk" is enabled in M7 SLEEP and STOP mode. Note : M7TCMEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4TCMLPEN	TCM Core M4 Low Power clock Enable. Set and cleared by software. 0: The "tcm_gated_core_clk" is disabled in M4 SLEEP and STOP mode. 1: The "tcm_gated_core_clk" is enabled in M4 SLEEP and STOP mode. Note : M4TCMEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7TCMAXIEN	TCM AXI M7 allocation and clock enable. Set and cleared by software. 0: TCM AXI bus is not allocated to M7. "tcm_gated_axi_clk" is disabled in M7 RUN mode. 1: TCM AXI bus is allocated to M7. The "tcm_gated_axi_clk" is enabled in M7 RUN mode.
18	M4TCMAXIEN	TCM AXI M4 allocation and clock enable. Set and cleared by software. 0: TCM AXI bus is not allocated to M4. "tcm_gated_axi_clk" is disabled in M4 RUN mode. 1: TCM AXI bus is allocated to M4. The "tcm_gated_axi_clk" is enabled in M4 RUN mode.
17	M7TCMAXILPEN	TCM AXI M7 Low Power clock Enable. Set and cleared by software. 0: The "tcm_gated_axi_clk" is disabled in M7 SLEEP and STOP mode. 1: The "tcm_gated_axi_clk" is enabled in M7 SLEEP and STOP mode. Note : M7TCMAXIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4TCMAXILPEN	TCM AXI M4 Low Power clock Enable. Set and cleared by software. 0: The "tcm_gated_axi_clk" is disabled in M4 SLEEP and STOP mode. 1: The "tcm_gated_axi_clk" is enabled in M4 SLEEP and STOP mode. Note : M4TCMAXIEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7TCMAPBEN	TCM APB M7 allocation and clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: TCM APB bus is not allocated to M7. "tcm_gated_pclk" is disabled in M7 RUN mode. 1: TCM APB bus is allocated to M7. The "tcm_gated_pclk" is enabled in M7 RUN mode.
14	M4TCMAPBEN	TCM APB M4 allocation and clock enable. Set and cleared by software. 0: TCM APB bus is not allocated to M4. "tcm_gated_pclk" is disabled in M4 RUN mode. 1: TCM APB bus is allocated to M4. The "tcm_gated_pclk" is enabled in M4 RUN mode.
13	M7TCMAPBLPEN	TCM APB M7 Low Power clock Enable. Set and cleared by software. 0: The "tcm_gated_pclk" is disabled in M7 SLEEP and STOP mode. 1: The "tcm_gated_pclk" is enabled in M7 SLEEP and STOP mode. Note : M7TCMAPBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4TCMAPBLPEN	TCM APB M4 Low Power clock Enable. Set and cleared by software. 0: The "tcm_gated_pclk" is disabled in M4 SLEEP and STOP mode. 1: The "tcm_gated_pclk" is enabled in M4 SLEEP and STOP mode. Note : M4TCMAPBEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7ASRAM1EN	AXISRAM1 M7 allocation and clock enable. Set and cleared by software. 0: AXISRAM1 is not allocated to M7. The "axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" are disabled in M7 RUN mode. 1: AXISRAM1 is allocated to M7. The "axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" are enabled in M7 RUN mode.
10	M4ASRAM1EN	AXISRAM1 M4 allocation and clock enable. Set and cleared by software. 0: AXISRAM1 is not allocated to M4. The "axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" are disabled in M4 RUN mode. 1: AXISRAM1 is allocated to M4. The "axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" are enabled in M4 RUN mode.
9	M7ASRAM1LPEN	AXISRAM1 M7 Low Power clock Enable. Set and cleared by software. 0: The "axisram1_gated_axi_clk" and "tcm_axiramc1_gated_axi_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The"axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" are enabled in M7 SLEEP mode.

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Bit field	Name	Description
		Note : M7ASRAM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4ASRAM1LPEN	AXISRAM1 M4 Low Power clock Enable. Set and cleared by software. 0: The "axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The"axisram1_gated_axi_clk" and "axiramc1_gated_axi_clk" are enabled in M4 SLEEP mode. Note : M4ASRAM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7AXIROMEN	AXIROM M7 allocation and clock enable. Set and cleared by software. 0: AXIROM is not allocated to M7. The "axirom_gated_axi_clk" and "axiromc_gated_axi_clk" are disabled in M7 RUN mode. 1: AXIROM is allocated to M7. The "axirom_gated_axi_clk" and "axiromc_gated_axi_clk" are enabled in M7 RUN mode.
6	M4AXIROMEN	AXIROM M4 allocation and clock enable. Set and cleared by software. 0: AXIROM is not allocated to M4. The "axirom_gated_axi_clk" and "axiromc_gated_axi_clk" are disabled in M4 RUN mode. 1: AXIROM is allocated to M4. The "axirom_gated_axi_clk" and "axiromc_gated_axi_clk" are enabled in M4 RUN mode.
5	M7AXIROMLPEN	AXIROM M7 Low Power clock Enable. Set and cleared by software. 0: The "axirom_gated_axi_clk" and "axiromc_gated_axi_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The"axirom_gated_axi_clk" and "axiromc_gated_axi_clk" are enabled in M7 SLEEP mode. Note : M7AXIROMEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4AXIROMLPEN	AXIROM M4 Low Power clock Enable. Set and cleared by software. 0: The "axirom_gated_axi_clk" and "axiromc_gated_axi_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The"axirom_gated_axi_clk" and "axiromc_gated_axi_clk" are enabled in M4 SLEEP mode. Note : M4AXIROMEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7GPUEN	GPU M7 allocation and clock enable. Set and cleared by software. 0: GPU is not allocated to M7. The "gpu_gated_axi_clk" is disabled in M7 RUN mode.

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Bit field	Name	Description
		1: GPU is allocated to M7. The "gpu_gated_axi_clk" is enabled in M7 RUN mode.
2	M4GPUEN	GPU M4 allocation and clock enable. Set and cleared by software. 0: GPU is not allocated to M4. The "gpu_gated_axi_clk" is disabled in M4 RUN mode. 1: GPU is allocated to M4. The "gpu_gated_axi_clk" is enabled in M4 RUN mode.
1	M7GPULPEN	GPU M7 Low Power clock Enable. Set and cleared by software. 0: The "gpu_gated_axi_clk" clock is disabled in M7 SLEEP and STOP mode. 1: The "gpu_gated_axi_clk" is enabled in M7 SLEEP mode. Note : M7GPUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4GPULPEN	GPU M4 Low Power clock Enable. Set and cleared by software. 0: The "gpu_gated_axi_clk" clock is disabled in M4 SLEEP and STOP mode. 1: The "gpu_gated_axi_clk" is enabled in M4 SLEEP mode. Note : M4GPUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.95 AXI peripherals clock enable register 4(RCC_AXIEN4)

Address offset: 0x014c

Reset value: 0x00880000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7XSPI1EN	M4XSPI1EN	M7XSPI1LPEN	M4XSPI1LPEN	M7XSPI2EN	M4XSPI2EN	M7XSPI2LPEN	M4XSPI2LPEN	M7FEMCEN	M4FEMCEN	M7FEMCLPEN	M4FEMCLPEN	M7SDRAMEN	M4SDRAMEN	M7SDRAMLPEN	M4SDRAMLPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												M7DSIULPSEN	M4DSIULPSEN	M7DSIULPSLPEN	M4DSIULPSLPEN
												rw	rw	rw	rw

Bit field	Name	Description
31	M7XSPI1EN	XSPI1 M7 allocation and clock enable. Set and cleared by software. 0: XSPI1 is not allocated to M7. The "xspi1_ssi_gated_clk" and "xspi1_gated_hclk" are disabled in M7 RUN mode. 1: XSPI1 is allocated to M7. The "xspi1_ssi_gated_clk" and "xspi1_gated_hclk" are enabled in M7 RUN mode.

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Bit field	Name	Description
30	M4XSPI1EN	XSPI1 M4 allocation and clock enable. Set and cleared by software. 0: XSPI1 is not allocated to M4. The "xspi1_ssi_gated_clk" and "xspi1_gated_hclk" are disabled in M4 RUN mode. 1: XSPI1 is allocated to M4. The "xspi1_ssi_gated_clk" and "xspi1_gated_hclk" are enabled in M4 RUN mode.
29	M7XSPI1LPEN	XSPI1 M7 Low Power clock Enable. Set and cleared by software. 0: The "xspi1_ssi_gated_clk" and "xspi1_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "xspi1_ssi_gated_clk" is enabled in M7 SLEEP and STOP mode. "xspi1_gated_hclk" is enabled in M7 SLEEP mode. Note : M7XSPI1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
28	M4XSPI1LPEN	XSPI1 M4 Low Power clock Enable. Set and cleared by software. 0: The "xspi1_ssi_gated_clk" and "xspi1_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "xspi1_ssi_gated_clk" is enabled in M4 SLEEP and STOP mode. "xspi1_gated_hclk" is enabled in M4 SLEEP mode. Note : M4XSPI1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
27	M7XSPI2EN	XSPI2 M7 allocation and clock enable. Set and cleared by software. 0: XSPI2 is not allocated to M7. The "xspi2_ssi_gated_clk" and "xspi2_gated_hclk" are disabled in M7 RUN mode. 1: XSPI2 is allocated to M7. The "xspi2_ssi_gated_clk" and "xspi2_gated_hclk" are enabled in M7 RUN mode.
26	M4XSPI2EN	XSPI2 M4 allocation and clock enable. Set and cleared by software. 0: XSPI2 is not allocated to M4. The "xspi2_ssi_gated_clk" and "xspi2_gated_hclk" are disabled in M4 RUN mode. 1: XSPI2 is allocated to M4. The "xspi2_ssi_gated_clk" and "xspi2_gated_hclk" are enabled in M4 RUN mode.
25	M7XSPI2LPEN	XSPI2 M7 Low Power clock Enable. Set and cleared by software. 0: The "xspi2_ssi_gated_clk" and "xspi2_gated_hclk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "xspi2_ssi_gated_clk" is enabled in M7 SLEEP and STOP mode. "xspi2_gated_hclk" is enabled in M7 SLEEP mode. Note : M7XSPI2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

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Bit field	Name	Description
24	M4XSPI2LPEN	XSPI2 M4 Low Power clock Enable. Set and cleared by software. 0: The "xspi2_ssi_gated_clk" and "xspi2_gated_hclk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "xspi2_ssi_gated_clk" is enabled in M4 SLEEP and STOP mode. "xspi2_gated_hclk" is enabled in M4 SLEEP mode. Note : M4XSPI2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
23	M7FEMCEN	FEMC M7 allocation and clock enable. Set and cleared by software. 0: FEMC is not allocated to M7. The "femc_m0_gated_clk", "femc_m1_gated_clk" and "femc_gated_axi_clk" are disabled in M7 RUN mode. 1: FEMC is allocated to M7. The "femc_m0_gated_clk", "femc_m1_gated_clk" and "femc_gated_axi_clk" are enabled in M7 RUN mode.
22	M4FEMCEN	FEMC M4 allocation and clock enable. Set and cleared by software. 0: FEMC is not allocated to M4. The "femc_m0_gated_clk", "femc_m1_gated_clk" and "femc_gated_axi_clk" are disabled in M4 RUN mode. 1: FEMC is allocated to M4. The "femc_m0_gated_clk", "femc_m1_gated_clk" and "femc_gated_axi_clk" are enabled in M4 RUN mode.
21	M7FEMCLPEN	FEMC M7 Low Power clock Enable. Set and cleared by software. 0: The "femc_m0_gated_clk", "femc_m1_gated_clk" and "femc_gated_axi_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "femc_m0_gated_clk" and "femc_m1_gated_clk" are enabled in M7 SLEEP and STOP mode. "femc_gated_axi_clk" is enabled in M7 SLEEP mode. Note : M7FEMCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4FEMCLPEN	FEMC M4 Low Power clock Enable. Set and cleared by software. 0: The "femc_m0_gated_clk", "femc_m1_gated_clk" and "femc_gated_axi_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "femc_m0_gated_clk" and "femc_m1_gated_clk" are enabled in M4 SLEEP and STOP mode. "femc_gated_axi_clk" is enabled in M4 SLEEP mode. Note : M4FEMCEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7SDRAMEN	SDRAM M7 allocation and clock enable. Set and cleared by software. 0: SDRAM is not allocated to M7. The "sdram_gated_mem_clk", "sdram_gated_m_clk" and "sdram_gated_c_clk" are disabled in M7 RUN mode. 1: SDRAM is allocated to M7. The "sdram_gated_mem_clk", "sdram_gated_m_clk" and "sdram_gated_c_clk" are enabled in M7 RUN mode.

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Bit field	Name	Description
18	M4SDRAMEN	SDRAM M4 allocation and clock enable. Set and cleared by software. 0: SDRAM is not allocated to M4. The "sdram_gated_mem_clk", "sdram_gated_m_clk" and "sdram_gated_c_clk" are disabled in M4 RUN mode. 1: SDRAM is allocated to M4. The "sdram_gated_mem_clk", "sdram_gated_m_clk" and "sdram_gated_c_clk" are enabled in M4 RUN mode.
17	M7SDRAMLPEN	SDRAM M7 Low Power clock Enable. Set and cleared by software. 0: The "sdram_gated_mem_clk", "sdram_gated_m_clk" and "sdram_gated_c_clk" clocks are disabled in M7 SLEEP and STOP mode. 1: The "sdram_gated_mem_clk" is enabled in M7 SLEEP and STOP mode. "sdram_gated_m_clk" and "sdram_gated_c_clk" are enabled in M7 SLEEP mode. Note : M7SDRAMEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4SDRAMLPEN	SDRAM M4 Low Power clock Enable. Set and cleared by software. 0: The "sdram_gated_mem_clk", "sdram_gated_m_clk" and "sdram_gated_c_clk" clocks are disabled in M4 SLEEP and STOP mode. 1: The "sdram_gated_mem_clk" is enabled in M4 SLEEP and STOP mode. "sdram_gated_m_clk" and "sdram_gated_c_clk" are enabled in M4 SLEEP mode. Note : M4SDRAMEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15:4	Reserved	Reserved, the reset value must be maintained.
3	M7DSIULPSEN	DSI M7 allocation and clock enable. Set and cleared by software. 0: DSI ULPS is not allocated to M7. The "dsi_ulps_gated_clk" is disabled in M7 RUN mode. 1: DSI ULPS is allocated to M7. The "dsi_ulps_gated_clk"is enabled in M7 RUN mode.
2	M4DSIULPSEN	DSI M4 allocation and clock enable. Set and cleared by software. 0: DSI ULPS is not allocated to M4. The "dsi_ulps_gated_clk" is disabled in M4 RUN mode. 1: DSI ULPS is allocated to M4. The "dsi_ulps_gated_clk"is enabled in M4 RUN mode.
1	M7DSIULPSLPEN	DSI M7 Low Power clock Enable. Set and cleared by software. 0: The "dsi_ulps_gated_clk" clocks is disabled in M7 SLEEP and STOP mode. 1: The "dsi_ulps_gated_clk" clock is enabled in M7 SLEEP and STOP mode. Note : M7DSIULPSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4DSIULPSLPEN	DSI M4 Low Power clock Enable. Set and cleared by software. 0: The "dsi_ulps_gated_clk" clocks is disabled in M4 SLEEP and STOP mode. 1: The "dsi_ulps_gated_clk" clock is enabled in M4 SLEEP and STOP mode.

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Bit field	Name	Description
		Note : M4DSIULPSEN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.96 AXI peripherals reset register 1(RCC_AXIRST1)

Address offset: 0x0150

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			JPEGDRST	Reserved							JPEGERST	Reserved			DMAMUX2RST
			rw								rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			MDMARST	Reserved		SDMMC1RST	SDHOST1RST	Reserved			ECCM1RST	Reserved			OTPCRST
			rw			rw	rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	JPEGDRST	JPEG Decoder soft reset 0: Clear reset 1: Reset JPEG Decoder
27:21	Reserved	Reserved, the reset value must be maintained.
20	JPEGERST	JPEG Encoder soft reset 0: Clear reset 1: Reset JPEG Encoder
19:17	Reserved	Reserved, the reset value must be maintained.
16	DMAMUX2RST	DMA_MUX2 soft reset 0: Clear reset 1: Reset DMA_MUX2
15:13	Reserved	Reserved, the reset value must be maintained.
12	MDMARST	MDMA soft reset 0: Clear reset 1: Reset MDMA
11:10	Reserved	Reserved, the reset value must be maintained.
9	SDMMC1RST	SDMMC1 Configuration soft reset 0: Clear reset 1: Reset SDMMC1
8	SDHOST1RST	SDHOST1 soft reset 0: Clear reset

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Bit field	Name	Description
		1: Reset SDHOST1
7:5	Reserved	Reserved, the reset value must be maintained.
4	ECCM1RST	ECCMON1 soft reset 0: Clear reset 1: Reset ECCMON1
3:1	Reserved	Reserved, the reset value must be maintained.
0	OTPCRST	OTPC soft reset 0: Clear reset 1: Reset OTPC

4.5.97 AXI peripherals reset register 2(RCC_AXIRST2)

Address offset: 0x0154

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		DSICFGRST	DSIRST	Reserved			LCDCRST	Reserved							DVP1RST
		rw					rw								rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DVP2RST	Reserved							WWDG1RST
							rw								rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	DSICFGRST	DSI Configuration soft reset 0: Clear reset 1: Reset DSI Configuration
28	DSIRST	DSI soft reset 0: Clear reset 1: Reset DSI
27:25	Reserved	Reserved, the reset value must be maintained.
24	LCDCRST	LCDC soft reset 0: Clear reset 1: Reset LCDC
23:17	Reserved	Reserved, the reset value must be maintained.
16	DVP1RST	DVP1 soft reset 0: Clear reset 1: Reset DVP1

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Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained.
8	DVP2RST	DVP2 soft reset 0: Clear reset 1: Reset DVP2
7:1	Reserved	Reserved, the reset value must be maintained.
0	WWDG1RST	WWDG1 soft reset 0: Clear reset 1: Reset WWDG1

4.5.98 AXI peripherals reset register 3(RCC_AXIRST3)

Address offset: 0x0158

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															GPURST
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	GPURST	GPU soft reset 0: Clear reset 1: Reset GPU

4.5.99 AXI peripherals reset register 4(RCC_AXIRST4)

Address offset: 0x015c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			XSPI1RST	Reserved			XSPI2RST	Reserved		FEMCCFGRST	FEMCRST	Reserved			SDRAMRST
			rw				rw			rw	rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	XSPI1RST	XSPI1 soft reset 0: Clear reset 1: Reset XSPI1
27:25	Reserved	Reserved, the reset value must be maintained.
24	XSPI2RST	XSPI2 soft reset 0: Clear reset 1: Reset XSPI2
23:22	Reserved	Reserved, the reset value must be maintained.
21	FEMCCFGRST	FEMC configuration soft reset 0: Clear reset 1: Reset FEMC configuration
20	FEMCRST	FEMC soft reset 0: Clear reset 1: Reset FEMC
19:17	Reserved	Reserved, the reset value must be maintained.
16	SDRAMRST	SDRAM soft reset 0: Clear reset 1: Reset SDRAM
15:0	Reserved	Reserved, the reset value must be maintained.

4.5.100 Clock configure register 2(RCC_CFG2)

Address offset: 0x0160

Reset value: 0x55accccc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	M4CAHIEN	Reserved	M4CAHIPCLKEN	Reserved	M4CAHDEN	Reserved	M4CAHDPCLKEN	M7MMUEN	M7MMULPEN	M4MMUEN	M4MMULPEN	M7SRAMBKPEN	M4SRAMBKPEN	M7SRAMBKPLPEN	M4SRAMBKPLPEN
	rw		rw		rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7SRAM1EN	M4SRAM1EN	M7SRAM1LPEN	M4SRAM1LPEN	M7SRAM2EN	M4SRAM2EN	M7SRAM2LPEN	M4SRAM2LPEN	M7SRAM3EN	M4SRAM3EN	M7SRAM3LPEN	M4SRAM3LPEN	M7SRAM4EN	M4SRAM4EN	M7SRAM4LPEN	M4SRAM4LPEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	M4CAHIEN	M4 I Cache Clock Enable. Set and cleared by software. 0: M4 I Cache Clock "cah_i_cm4_gated_hclk" is disabled. 1: M4 I Cache Clock "cah_i_cm4_gated_hclk" is enabled.
29	Reserved	Reserved, the reset value must be maintained.
28	M4CAHIPCLKEN	M4 I Cache PCLKEN control. Set and cleared by software. 0: Disable M4 I Cache PCLKEN 1: Enable M4 I Cache PCLKEN
27	Reserved	Reserved, the reset value must be maintained.
26	M4CAHDEN	M4 D Cache Clock Enable. Set and cleared by software. 0: M4 D Cache Clock "cah_d_cm4_gated_hclk" is disabled. 1: M4 D Cache Clock "cah_d_cm4_gated_hclk" is enabled.
25	Reserved	Reserved, the reset value must be maintained.
24	M4CAHDPCLKEN	M4 D Cache PCLKEN control. Set and cleared by software. 0: Disable M4 D Cache PCLKEN 1: Enable M4 D Cache PCLKEN
23	M7MMUEN	MMU M7 allocation and clock enable. Set and cleared by software. 0: MMU is not allocated to M7. The MMU clocks are disabled. 1: MMU is allocated to M7. The MMU clocks are enabled in M7 RUN mode.
22	M7MMULPEN	MMU M7 Low Power clock enable. Set and cleared by software. 0: MMU clocks are disabled in M7 SLEEP and STOP mode. 1: MMU clocks are enabled in M7 SLEEP mode. Note : M7MMUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
21	M4MMUEN	MMU M4 allocation and clock enable. Set and cleared by software. 0: MMU is not allocated to M4. The MMU clocks are disabled. 1: MMU is allocated to M4. The MMU clocks are enabled in M4 RUN mode.
20	M4MMULPEN	MMU M4 Low Power clock enable. Set and cleared by software. 0: MMU clocks are disabled in M4 SLEEP and STOP mode. 1: MMU clocks are enabled in M4 SLEEP mode. Note : M4MMUEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19	M7SRAMBKPEN	BKP SRAM M7 allocation and clock enable. Set and cleared by software. 0: BKP SRAM is not allocated to M7. The BKP SRAM controller clock is disabled. 1: BKP SRAM is allocated to M7. The BKP SRAM controller clock is enabled in M7 RUN mode.
18	M4SRAMBKPEN	BKP SRAM M4 allocation and clock enable. Set and cleared by software.

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Bit field	Name	Description
		0: BKP SRAM is not allocated to M4. The BKP SRAM controller clock is disabled. 1: BKP SRAM is allocated to M4. The BKP SRAM controller clock is enabled in M4 RUN mode.
17	M7SRAMBKPLPEN	BKP SRAM M7 Low Power clock enable. Set and cleared by software. 0: BKP SRAM controller clock is disabled in M7 SLEEP and STOP mode. 1: BKP SRAM controller clock is enabled in M7 SLEEP mode. Note : M7SRAMBKPEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
16	M4SRAMBKPLPEN	BKP SRAM M4 Low Power clock enable. Set and cleared by software. 0: BKP SRAM controller clock is disabled in M4 SLEEP and STOP mode. 1: BKP SRAM controller clock is enabled in M4 SLEEP mode. Note : M4SRAMBKPEN bit should be enabled before enabling this bit, otherwise this bit has no effect.
15	M7SRAM1EN	SRAM1 M7 allocation and clock enable. Set and cleared by software. 0: SRAM1 is not allocated to M7. The SRAM1 controller clock is disabled. 1: SRAM1 is allocated to M7. The SRAM1 controller clock is enabled in M7 RUN mode.
14	M4SRAM1EN	SRAM1 M4 allocation and clock enable. Set and cleared by software. 0: SRAM1 is not allocated to M4. The SRAM1 controller clock is disabled. 1: SRAM1 is allocated to M4. The SRAM1 controller clock is enabled in M4 RUN mode.
13	M7SRAM1LPEN	SRAM1 M7 Low Power clock enable. Set and cleared by software. 0: SRAM1 controller clock is disabled in M7 SLEEP and STOP mode. 1: SRAM1 controller clock is enabled in M7 SLEEP mode. Note : M7SRAM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
12	M4SRAM1LPEN	SRAM1 M4 Low Power clock enable. Set and cleared by software. 0: SRAM1 controller clock is disabled in M4 SLEEP and STOP mode. 1: SRAM1 controller clock is enabled in M4 SLEEP mode. Note : M4SRAM1EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
11	M7SRAM2EN	SRAM2 M7 allocation and clock enable. Set and cleared by software. 0: SRAM2 is not allocated to M7. The SRAM2 controller clock is disabled. 1: SRAM2 is allocated to M7. The SRAM2 controller clock is enabled in M7 RUN mode.
10	M4SRAM2EN	SRAM2 M4 allocation and clock enable. Set and cleared by software. 0: SRAM2 is not allocated to M4. The SRAM2 controller clock is disabled. 1: SRAM2 is allocated to M4. The SRAM2 controller clock is enabled in M4 RUN mode.
9	M7SRAM2LPEN	SRAM2 M7 Low Power clock enable. Set and cleared by software. 0: SRAM2 controller clock is disabled in M7 SLEEP and STOP mode. 1: SRAM2 controller clock is enabled in M7 SLEEP mode. Note : M7SRAM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
8	M4SRAM2LPEN	SRAM2 M4 Low Power clock enable. Set and cleared by software. 0: SRAM2 controller clock is disabled in M4 SLEEP and STOP mode.

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Bit field	Name	Description
		1: SRAM2 controller clock is enabled in M4 SLEEP mode. Note : M4SRAM2EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
7	M7SRAM3EN	SRAM3 M7 allocation and clock enable. Set and cleared by software. 0: SRAM3 is not allocated to M7. The SRAM3 controller clock is disabled. 1: SRAM3 is allocated to M7. The SRAM3 controller clock is enabled in M7 RUN mode.
6	M4SRAM3EN	SRAM3 M4 allocation and clock enable. Set and cleared by software. 0: SRAM3 is not allocated to M4. The SRAM3 controller clock is disabled. 1: SRAM3 is allocated to M4. The SRAM3 controller clock is enabled in M4 RUN mode.
5	M7SRAM3LPEN	SRAM3 M7 Low Power clock enable. Set and cleared by software. 0: SRAM3 controller clock is disabled in M7 SLEEP and STOP mode. 1: SRAM3 controller clock is enabled in M7 SLEEP mode. Note : M7SRAM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
4	M4SRAM3LPEN	SRAM3 M4 Low Power clock enable. Set and cleared by software. 0: SRAM3 controller clock is disabled in M4 SLEEP and STOP mode. 1: SRAM3 controller clock is enabled in M4 SLEEP mode. Note : M4SRAM3EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
3	M7SRAM4EN	SRAM4 M7 allocation and clock enable. Set and cleared by software. 0: SRAM4 is not allocated to M7. The SRAM4 controller clock is disabled. 1: SRAM4 is allocated to M7. The SRAM4 controller clock is enabled in M7 RUN mode.
2	M4SRAM4EN	SRAM4 M4 allocation and clock enable. Set and cleared by software. 0: SRAM4 is not allocated to M4. The SRAM4 controller clock is disabled. 1: SRAM4 is allocated to M4. The SRAM4 controller clock is enabled in M4 RUN mode.
1	M7SRAM4LPEN	SRAM4 M7 Low Power clock enable. Set and cleared by software. 0: SRAM4 controller clock is disabled in M7 SLEEP and STOP mode. 1: SRAM4 controller clock is enabled in M7 SLEEP mode. Note : M7SRAM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
0	M4SRAM4LPEN	SRAM4 M4 Low Power clock enable. Set and cleared by software. 0: SRAM4 controller clock is disabled in M4 SLEEP and STOP mode. 1: SRAM4 controller clock is enabled in M4 SLEEP mode. Note : M4SRAM4EN bit should be enabled before enabling this bit, otherwise this bit has no effect.

4.5.101 Clock configure register 3(RCC_CFG3)

Address offset: 0x0164

Reset value: 0x00000044

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCO1SEL[3:0]				MCO1DIV[3:0]				MCO2SEL[3:0]				MCO2DIV[3:0]			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2SSEL[1:0]		PERSW[1:0]		Reserved				M7STCLKDIV[3:0]				M4STCLKDIV[3:0]			
rw		rw						rw				rw			

Bit field	Name	Description
31:28	MCO1SEL[3:0]	MCO1 clock selection register. 1000: LSI clock is selected as MCO1 clock. 1001: HSI clock is selected as MCO1 clock. 1010: MSI clock is selected as MCO1 clock. 1011: LSE clock is selected as MCO1 clock. 1100: HSE clock is selected as MCO1 clock. 1101: PLL3_B clock is selected as MCO1 clock. Other values: setting is not allowed
27:24	MCO1DIV[3:0]	MCO1 clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 Other values: setting is not allowed
23:20	MCO2SEL[3:0]	MCO2 clock selection register. 1000: sys_clk is selected as MCO2 clock. 1001: PLL1_A clock is selected as MCO2 clock. 1010: PLL2_A clock is selected as MCO2 clock. 1011: PLL3_A clock is selected as MCO2 clock. 1100: SHRPLL clock is selected as MCO2 clock 1101: LSE clock is selected as MCO2 clock Other values: setting is not allowed
19:16	MCO2DIV[3:0]	MCO2 clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16

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Bit field	Name	Description
		1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 Other values: setting is not allowed
15:14	I2SSEL[1:0]	DSMU I2S_CKIN clock selection register. 00: I2S1_ckin clock is selected 01: I2S2_ckin clock is selected 10: I2S3_ckin clock is selected. 11: I2S4_ckin clock is selected.
13:12	PERSW[1:0]	Peripheral clock selection register. 00: HSI clock is selected as peripheral clock. 10: MSI clock is selected as peripheral clock. 11: HSE clock is selected as peripheral clock.
11:8	Reserved	Reserved, the reset value must be maintained.
7:4	M7STCLKDIV[3:0]	M7 systick clock prescalar values from fclk. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed *Note: when the systick clock source is STCLK, the divider can be configured by this bit field*
3:0	M4STCLKDIV[3:0]	M4 systick clock prescalar values from fclk. 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed *Note: when the systick clock source is STCLK, the divider can be configured by this bit field*

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4.5.102 Clock configure register 4(RCC_CFG4)

Address offset: 0x0168

Reset value: 0xfffffdfe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AHB1CLKEN	AHB2CLKEN	AHB3CLKEN	Reserved	AHB5CLKEN	AHB6CLKEN	Reserved	Reserved	AXICLKEN	APB1CLKEN	APB2CLKEN	APB5CLKEN	APB6CLKEN	AHB9CLKEN	AXIMM7GCLKEN	AXIMM4GCLKEN
rw	rw	rw		rw	rw			rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSICGEN	HSIKERCGEN	HSECGEN	HSEKERCGEN	MSICGEN	MSIKERCGEN	Reserved	AXIMM7CLKEN	AXIGCLKEN	AXIMM4CLKEN	DCMUM7CLKEN	DCMUM4CLKEN	AHBM1CLKEN	AHBM2CLKEN	AHBM3CLKEN	DCMURST
rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	AHB1CLKEN	AHB1 bus clock enable. Set and cleared by software. 0: Disable AHB1 bus clock. 1: Enable AHB1 bus clock.
30	AHB2CLKEN	AHB2 bus clock enable. Set and cleared by software. 0: Disable AHB2 bus clock. 1: Enable AHB2 bus clock.
29	AHB3CLKEN	AHB3 bus clock enable. Set and cleared by software. 0: Disable AHB3 bus clock. 1: Enable AHB3 bus clock.
28	Reserved	Reserved, the reset value must be maintained.
27	AHB5CLKEN	AHB5 bus clock enable. Set and cleared by software. 0: Disable AHB5 bus clock. 1: Enable AHB5 bus clock.
26	AHB6CLKEN	AHB6 bus clock enable. Set and cleared by software. 0: Disable AHB6 bus clock. 1: Enable AHB6 bus clock.
25:24	Reserved	Reserved, the reset value must be maintained.
23	AXICLKEN	AHB8 bus clock enable. Set and cleared by software. 0: Disable AXI bus clock. 1: Enable AXI bus clock.
22	APB1CLKEN	APB1 bus clock enable.

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Bit field	Name	Description
		Set and cleared by software. 0: Disable APB1 bus clock. 1: Enable APB1 bus clock.
21	APB2CLKEN	APB2 bus clock enable. Set and cleared by software. 0: Disable APB2 bus clock. 1: Enable APB2 bus clock.
20	APB5CLKEN	APB5 bus clock enable. Set and cleared by software. 0: Disable APB5 bus clock. 1: Enable APB5 bus clock.
19	APB6CLKEN	APB6 bus clock enable. Set and cleared by software. 0: Disable APB6 bus clock. 1: Enable APB6 bus clock.
18	AHB9CLKEN	AHB9 bus clock enable. Set and cleared by software. 0: Disable AHB9 bus clock. 1: Enable AHB9 bus clock.
17	AXIMM7GCLKEN	AXI bus matrix M7 GPV clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
16	AXIMM4GCLKEN	AXI bus matrix M4 GPV clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
15	HSICGEN	HSI clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
14	HSIKERCGEN	HSI Kernel clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
13	HSECGEN	HSE clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
12	HSEKERCGEN	HSE Kernel clock enable. Set and cleared by software. 0: Disable clock.

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Bit field	Name	Description
		1: Enable clock.
11	MSICGEN	MSI clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
10	MSIKERCGEN	MSI Kernel clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
9	Reserved	Reserved, the reset value must be maintained.
8	AXIMM7CLKEN	AXI bus matrix M7 sub system clock enable. Set and cleared by Software 0: Disable clock. 1: Enable clock.
7	AXIGCLKEN	AXI bus matrix GPV clock enable. Set and cleared by software. 0: Disable clock. 1: Enable clock.
6	AXIMM4CLKEN	AXI bus matrix M4 sub system clock enable. Set and cleared by software 0: Disable clock. 1: Enable clock.
5	DCMUM7CLKEN	DCMU M7 clock enable. Set and cleared by software 0: Disable clock. 1: Enable clock.
4	DCMUM4CLKEN	DCMU M4 clock enable. Set and cleared by software 0: Disable clock. 1: Enable clock.
3	AHBM1CLKEN	AHB bus matrix 1 clock enable. Set and cleared by software 0: Disable clock. 1: Enable clock.
2	AHBM2CLKEN	AHB bus matrix 2 clock enable. Set and cleared by software 0: Disable clock. 1: Enable clock.
1	AHBM3CLKEN	AHB bus matrix 3 clock enable. Set and cleared by software 0: Disable clock.

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Bit field	Name	Description
		1: Enable clock.
0	DCMURST	DCMU soft reset 0: De-assert Soft Reset. 1: Assert Soft Reset.

4.5.103 Clock configure register 5(RCC_CFG5)

Address offset: 0x0170

Reset value: 0x02c10000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		RTCHSEDIV[5:0]						M7SRAM5EN	M4SRAM5EN	M7SRAM5LPEN	M4SRAM5LPEN	Reserved			DCDCLKEN
		rw						rw	rw	rw	rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		TRNGEN	TRNGSEL	TRNGDIV[3:0]				DSIHSEDIV[3:0]				RTCHSIDIV[3:0]			
		rw	rw	rw				rw				rw			

Bit field	Name	Description
31:30	Reserved	
29:24	RTCHSEDIV[5:0]	RTC HSE clockprescalar values. 000001: Divide by 1 (bypass) 000010: Divide by 2 000011: Divide by 3 000100: Divide by 4 000101: Divide by 5 000110: Divide by 6 000111: Divide by 7 001000: Divide by 8 001001: Divide by 9 001010: Divide by 10 … 111110: Divide by 62 111111: Divide by 63
23	M7SRAM5EN	SRAM5 M7 allocation and clock enable. Set and cleared by software. 0: SRAM5 is not allocated to M7. The SRAM5 controller clock is disabled. 1: SRAM5 is allocated to M7. The SRAM5 controller clock is enabled in M7 RUN mode.
22	M4SRAM5EN	SRAM5 M4 allocation and clock enable. Set and cleared by software. 0: SRAM5 is not allocated to M4. The SRAM5 controller clock is disabled.

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Bit field	Name	Description
		1: SRAM5 is allocated to M4. The SRAM5 controller clock is enabled in M4 RUN mode.
21	M7SRAM5LPEN	SRAM5 M7 Low Power clock enable. Set and cleared by software. 0: SRAM5 controller clock is disabled in M7 SLEEP and STOP mode. 1: SRAM5 controller clock is enabled in M7 SLEEP mode. Note : M7SRAM5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
20	M4SRAM5LPEN	SRAM5 M4 Low Power clock enable. Set and cleared by software. 0: SRAM5 controller clock is disabled in M4 SLEEP and STOP mode. 1: SRAM5 controller clock is enabled in M4 SLEEP mode. Note : M4SRAM5EN bit should be enabled before enabling this bit, otherwise this bit has no effect.
19:17	Reserved	Reserved, the reset value must be maintained.
16	DCDCLKEN	Dual core debug clock enable register. 0: Disable dual core debug clock. 1: Enable dual core debug clock.
15:14	Reserved	Reserved, the reset value must be maintained.
13	TRNGEN	TRNG clock enable register. 0: Disable TRNG clock. 1: Enable TRNG clock.
12	TRNGSEL	TRNG clock selection register. 0: Divided system bus clock is selected as TRNG clock. 1: HSI clock is selected as TRNG clock.
11:8	TRNGDIV[3:0]	TRNG sys clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed
7:4	DSIHSEDIV[3:0]	DSI HSE clock prescalar values. 0000: Divide by 1 0001: Divide by 2 Other values: setting is not allowed
3:0	RTCHSIDIV[3:0]	RTC HSI clock prescalar values. 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4

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Bit field	Name	Description
		0100: Divide by 8 0111: Divide by 16 1000: Divide by 32 1001: Divide by 64 1010: Divide by 128 1011: Divide by 256 1100: Divide by 512 Other values: setting is not allowed

4.5.104 M4 Reset Release register(RCC_M4RSTREL)

Address offset: 0x0174

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															EN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EN	CM4 Reset Release 0: CM4 is in reset state. 1: Release CM4 reset.

4.5.105 LSE ready delay(RCC_LSERDDL)

Address offset: 0x0198

Reset value: 0x00000fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DELAY[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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DELAY[31:0]

rw

Bit field	Name	Description
31:0	DELAY[31:0]	Counter delay of LSE clock ready signal . With LSE clock frequency of 32.768kHz and default delay value of 32'h00000fff, the LSE clock ready signal is delayed by 125ms

4.5.106 MSI ready delay(RCC_MSIRDDL)

Address offset: 0x019c

Reset value: 0x0000000f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DELAY[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAY[31:0]															
rw															

Bit field	Name	Description
31:0	DELAY[31:0]	Counter delay of MSI clock ready signal . With MSI clock frequency of 16MHz and default delay value of 32'h0000000f, the MSI clock ready signal is delayed by 1us

4.5.107 HSE ready delay(RCC_HSERDDL)

Address offset: 0x01a0

Reset value: 0x00023280

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DELAY[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAY[31:0]															
rw															

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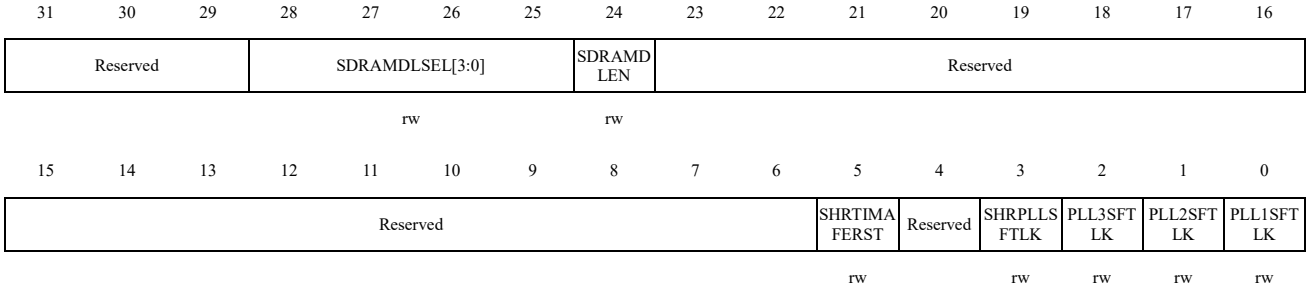
Bit field	Name	Description
31:0	DELAY[31:0]	Counter delay of HSE clock ready signal . With HSE clock frequency of 48MHz and default delay value of 32'h00023280, the HSE clock ready signal is delayed by 3ms

4.5.108 PLL software lock(RCC_PLLSFTLK)

Address offset: 0x01a4

Reset value: 0x00000020



Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28:25	SDRAMDLSEL[3:0]	SDRAM variable clock delay selection. 0000: Increase SDRAM clock latency by 0.2ns 0001: Increase SDRAM clock latency by 0.4ns 0010: Increase SDRAM clock latency by 0.6ns 0011: Increase SDRAM clock latency by 0.8ns 0100: Increase SDRAM clock latency by 1.0ns 0101: Increase SDRAM clock latency by 1.2ns 0110: Increase SDRAM clock latency by 1.4ns 0111: Increase SDRAM clock latency by 1.6ns 1000: Increase SDRAM clock latency by 1.8ns 1001: Increase SDRAM clock latency by 2.0ns 1010: Increase SDRAM clock latency by 2.2ns 1011: Increase SDRAM clock latency by 2.4ns 1100: Increase SDRAM clock latency by 2.6ns 1101: Increase SDRAM clock latency by 2.8ns 1110: Increase SDRAM clock latency by 3.0ns 1111: Increase SDRAM clock latency by 3.2ns
24	SDRAMDLEN	SDRAM Delay chain enable. 0: Bypass SDRAM clock delay chain.

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Bit field	Name	Description
		1: Enable SDRAM clock delay chain.
23:6	Reserved	Reserved, the reset value must be maintained.
5	SHRTIMAFERST	Soft reset register to assert POR reset to SHRTIM AFE. 0: Assert POR reset. 1: Deassert POR reset.
4	Reserved	Reserved, the reset value must be maintained.
3	SHRPLLSFTLK	SHRPLL Software Lock. Enable this bit if hardware PLL lock failed to get asserted. 0: Software PLL Lock is not enabled. 1: Software PLL Lock is enabled.
2	PLL3SFTLK	PLL3 Software Lock. Enable this bit if hardware PLL lock failed to get asserted. 0: Software PLL Lock is not enabled. 1: Software PLL Lock is enabled.
1	PLL2SFTLK	PLL2 Software Lock. Enable this bit if hardware PLL lock failed to get asserted. 0: Software PLL Lock is not enabled. 1: Software PLL Lock is enabled.
0	PLL1SFTLK	PLL1 Software Lock. Enable this bit if hardware PLL lock failed to get asserted. 0: Software PLL Lock is not enabled. 1: Software PLL Lock is enabled.

4.5.109 HSE offset detect register(RCC_HSEOS)

Address offset: 0x01c8

Reset value: 0x29400300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSEMAXPDTHR[7:0]								HSEMINNDTHR[7:0]							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSEOSTHR[7:0]								Reserved	HSEMAXPDF	HSEMINNDF	HSEOSF	Reserved	HSEMAXPDEN	HSEMINNDEN	HSEOSEN
rw									rc_w1	rc_w1	rc_w1		rw	rw	rw

Bit field	Name	Description
31:24	HSEMAXPDTHR[7:0]	Threshold value for detection of positive deviation in HSE clock at maximum frequency.

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Bit field	Name	Description
		This value indicates the number of HSI clock counts in half cycle of (HSE/64) clock when HSE clock frequency is 50MHz.
23:16	HSEMINNDTHR[7:0]	Threshold value for detection of negative deviation in HSE clock at minimum frequency. This value indicates the number of HSI clock counts in half cycle of (HSE/8) clock when HSE clock frequency is 4MHz.
15:8	HSEOSTHR[7:0]	Threshold value for detection of frequency offset greater than 5% in HSE clock. This value represents the offset HSI clock counts in half cycle of HSE/128 clock when HSE frequency is offset by 5%. This value differs based on HSE frequency, default value is for HSE = 48MHz. For other HSE frequencies, software should program the appropriate value. 4MHz -> 8'h20 5MHz -> 8'h1A 6MHz -> 8'h16 7MHz -> 8'h12 8MHz -> 8'h10 9MHz -> 8'h0E 10MHz -> 8'h0D 11MHz -> 8'h0C 12MHz -> 8'h0B 13MHz -> 8'h0A 14~15MHz -> 8'h09 16~17MHz -> 8'h08 18~19MHz -> 8'h07 20~24MHz -> 8'h06 25~30MHz -> 8'h05 31~39MHz -> 8'h04 40~50MHz -> 8'h03
7	Reserved	Reserved, the reset value must be maintained.
6	HSEMAXPDF	Status flag to indicate detection of positive deviation in HSE clock at maximum frequency. This flag indicates that the HSE frequency is greater than 50MHz. This bit is set by hardware and cleared by software by writing 1. 0 : HSE clock frequency is less than 50MHz. 1 : HSE clock frequency is greater than 50MHz.
5	HSEMINNDF	Status flag to indicate detection of negative deviation in HSE clock at minimum frequency. This flag indicates that the HSE frequency is less than 4MHz. This bit is set by hardware and cleared by software by writing 1. 0 : HSE clock frequency is not less than 4MHz. 1 : HSE clock frequency is less than 4MHz.
4	HSEOSF	Status flag to indicate an offset greater than or equal to 5% in HSE clock frequency. This bit is set by hardware and cleared by software by writing 1. 0 : HSE clcok frequency offset is not greater than 5%. 1 : HSE clock frequency offset is greater than or equal to 5%.

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Bit field	Name	Description
3	Reserved	Reserved, the reset value must be maintained.
2	HSEMAXPDEN	Control bit to enable detection of positive deviation in HSE clock at maximum frequency. This bit is set and cleared by software. 0 : Disable. 1 : Enable.
1	HSEMINNDEN	Control bit to enable detection of negative deviation in HSE clock at minimum frequency. This bit is set and cleared by software 0 : Disable. 1 : Enable.
0	HSEOSEN	Control bit to enable frequency offset detection in HSE clock. This bit is set and cleared by software. 0 : Disable. 1 : Enable.

4.5.110 HSE calibration register(RCC_HSECAL)

Address offset: 0x01d0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														HSECALCNTEN	HSECALCNTF
														rw	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSECALCNT[15:0]															
r															

Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	HSECALCNTEN	HSE calibration count enable. 0 : Enable Calibration Count. 1 : Disable Calibration Count.
16	HSECALCNTF	HSE calibration count status. 0 : HSE calibration count is not ready. 1 : HSE calibration count is ready.
15:0	HSECALCNT[15:0]	Number of HSI clock counts in half cycle of HSE/128 clock.

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4.5.111 LSE offset detect register(RCC_LSEOS)

Address offset: 0x01cc

Reset value: 0x00000005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						LSECALCNTEN	LSECALCNTF	LSECALCNT[7:0]							
						rw	r	r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						LSEOSF	LSEOSEN	LSEOSTHR[7:0]							
						r	rw	rw							

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	LSECALCNTEN	LSE calibration count enable. 0 : Enable Calibration Count. 1 : Disable Calibration Count.
24	LSECALCNTF	LSE calibration count status. 0 : LSE calibration count is not ready. 1 : LSE calibration count is ready.
23:16	LSECALCNT[7:0]	Number of LSI clock counts in half cycle of LSE/128 clock.
15:10	Reserved	Reserved, the reset value must be maintained.
9	LSEOSF	Status flag to indicate an offset greater than 10% in LSE clock frequency. This flag indicates that there is more than 10% offset in LSE clock frequency. 0 : LSE clock frequecny offset is not greater than 10%. 1 : LSE clock frequency offset is greater than 10%.
8	LSEOSEN	Contorl bit to enable frequency offset detection in LSE clock. This bit is set and cleared by software. 0 : Disable. 1 : Enable.
7:0	LSEOSTHR[7:0]	Threshold value for detection of frequency offset greater than 10% in LSE clock. This value represents the offset LSI clock counts in half cycle of LSE clcok when LSE frequency is offset by 10%.

4.5.112 PLL fail detect register(RCC_PLLFD)

Address offset: 0x01d8

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SHRPLLGF	PLL3GF	PLL2GF	PLL1GF	SHRPLLFF	PLL3FF	PLL2FF	PLL1FF	SHRPLLFEN	PLL3FEN	PLL2FEN	PLL1FEN
				r	r	r	r	r	r	r	r	rw	rw	rw	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	SHRPLLGF	This bit indicates the status of SHRPLL clock gate. 0: Clock gate is OFF. 1: Clock gate is ON.
10	PLL3GF	This bit indicates the status of PLL3 clock gate. 0: Clock gate is OFF. 1: Clock gate is ON.
9	PLL2GF	This bit indicates the status of PLL2 clock gate. 0: Clock gate is OFF. 1: Clock gate is ON.
8	PLL1GF	This bit indicates the status of PLL1 clock gate. 0: Clock gate is OFF. 1: Clock gate is ON.
7	SHRPLLFF	This bit indicates the status of SHRPLL fail state signal. 0: PLL fail state signal is de-asserted. 1: PLL fail state signal is asserted.
6	PLL3FF	This bit indicates the status of PLL3 fail state signal. 0: PLL fail state signal is de-asserted. 1: PLL fail state signal is asserted.
5	PLL2FF	This bit indicates the status of PLL2 fail state signal. 0: PLL fail state signal is de-asserted. 1: PLL fail state signal is asserted.
4	PLL1FF	This bit indicates the status of PLL1 fail state signal. 0: PLL fail state signal is de-asserted. 1: PLL fail state signal is asserted.
3	SHRPLLFEN	Control register to enable SHRPLL lock fail detection logic. 0: Disable SHRPLL lock fail detection logic. 1: Enable SHRPLL lock fail detection logic.
2	PLL3FEN	Control register to enable PLL3 lock fail detection logic. 0: Disable PLL3 lock fail detection logic. 1: enablepll3 lock fail detection logic.
1	PLL2FEN	Control register to enable PLL2 lock fail detection logic.

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Bit field	Name	Description
		0: Disable PLL2 lock fail detection logic. 1: Enable PLL2 lock fail detection logic.
0	PLL1FEN	Control register to enable PLL1 lock fail detection logic. 0: Disable PLL1 lock fail detection logic. 1: Enable PLL1 lock fail detection logic.

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5 Block Interconnect

5.1 Peripheral Interconnect

5.1.1 Introduction

This chapter shows the interconnect mapping between different peripherals. This allows direct communication and synchronization between peripherals, hence saving CPU resources and power consumption. This also avoids software intervention, allowing more predictable latency for certain applications.

5.1.2 Peripheral Mapping Details

5.1.2.1 Advanced/General Timers

Table 5-1 Timer Internal Trigger Inputs (part 1)

Signals	ATIM1	ATIM2	ATIM3	ATIM4	GTIMA1	GTIMA2	GTIMA3
itr0	-	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO
itr1	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	-	GTIMA1_TRGO	GTIMA1_TRGO
itr2	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	-	GTIMA2_TRGO
itr3	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	-
itr4	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO
itr5	ATIM2_TRGO	-	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO
itr6	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO
itr7	ATIM3_TRGO	ATIM3_TRGO	-	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO
itr8	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO
itr9	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO
itr10	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	-	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO
itr11	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO
itr12	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO
itr13	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO
itr14	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2
itr15	SHRTIM2_SYNC2	SHRTIM2_SYNC2	SHRTIM2_SYNC2	SHRTIM2_SYNC2	ETH2_PPS	ETH2_PPS	-

Table 5-2 Timer Internal Trigger Inputs (part 2)

Signals	GTIMA4	GTIMA5	GTIMA6	GTIMA7	GTIMB1	GTIMB2	GTIMB3
itr0	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO
itr1	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO
itr2	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO
itr3	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO
itr4	FDCAN1_SOC	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO

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itr5	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO
itr6	GTIMA5_TRGO	FDCAN2_SOC	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO
itr7	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO
itr8	GTIMA6_TRGO	GTIMA6_TRGO	FDCAN3_SOC	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO
itr9	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	FDCAN4_SOC	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO
itr10	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO
itr11	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	-	GTIMB1_TRGO	GTIMB1_TRGO
itr12	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	-	GTIMB2_TRGO
itr13	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	-
itr14	USB1_SOF	USB1_SOF	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2	SHRTIM1_SYNC2
itr15	USB2_SOF	USB2_SOF	SHRTIM2_SYNC2	SHRTIM2_SYNC2	ETH1_PPS	ETH1_PPS	-

Table 5-3 Timer External Trigger Inputs (part 1)

Signals	ATIM1	ATIM2	ATIM3	ATIM4	GTIMA1	GTIMA2	GTIMA3
etr0	ATIM1_ETR	ATIM2_ ETR	ATIM3_ ETR	ATIM4_ ETR	GTIMA1_ETR	GTIMA2_ETR	GTIMA3_ETR
etr1	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT
etr2	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT
etr3	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT
etr4	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT
etr5	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1
etr6	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2
etr7	ADC1_ AWD3	ADC1_ AWD3	ADC1_ AWD3	ADC1_ AWD3	GTIMA2_ETR	GTIMA1_ETR	GTIMA2_ETR
etr8	ADC2_ AWD1	LSE_CSS_OUT	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1
etr9	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2
etr10	ADC2_ AWD3	ADC2_ AWD3	ADC2_ AWD3	ADC2_ AWD3	GTIMB1_ETR	GTIMA3_ETR	GTIMA4_ETR
etr11	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1
etr12	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2
etr13	ADC3_ AWD3	ADC3_ AWD3	ADC3_ AWD3	ADC3_ AWD3	LSE	GTIMB2_ETR	GTIMB3_ETR

Table 5-4 Timer External Trigger Inputs (part 2)

Signals	GTIMA4	GTIMA5	GTIMA6	GTIMA7	GTIMB1	GTIMB2	GTIMB3
etr0	GTIMA4_ETR	GTIMA5_ETR	GTIMA6_ETR	GTIMA7_ETR	GTIMB1_ETR	GTIMB2_ETR	GTIMB3_ETR
etr1	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT
etr2	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT
etr3	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT
etr4	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT
etr5	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1
etr6	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2
etr7	GTIMA1_ETR	GTIMA6_ETR	GTIMA5_ETR	GTIMA5_ETR	GTIMB2_ETR	GTIMB1_ETR	GTIMB1_ETR

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etr8	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1
etr9	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2
etr10	GTIMA2_ETR	GTIMA7_ETR	GTIMA7_ETR	GTIMA6_ETR	GTIMB3_ETR	GTIMB3_ETR	GTIMB2_ETR
etr11	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1
etr12	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2
etr13	GTIMB1_ETR	GTIMB2_ETR	GTIMB3_ETR	GTIMB1_ETR	GTIMA1_ETR	GTIMA2_ETR	GTIMA3_ETR

Table 5-5 Timer OCREF Clear Inputs (part 1)

Signals	ATIM1	ATIM2	ATIM3	ATIM4	GTIMA1	GTIMA2	GTIMA3
ocref_clr0	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
ocref_clr1	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
ocref_clr2	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
ocref_clr3	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

Table 5-6 Timer OCREF Clear Inputs (part 2)

Signals	GTIMA4	GTIMA5	GTIMA6	GTIMA7	GTIMB1	GTIMB2	GTIMB3
ocref_clr0	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
ocref_clr1	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
ocref_clr2	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
ocref_clr3	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

Table 5-7 Timer TI1 Inputs (part 1)

Signals	ATIM1	ATIM2	ATIM3	ATIM4	GTIMA1	GTIMA2	GTIMA3
TI1_IN0	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1
TI1_IN1	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	LSE_ CSS_OUT	LSE	-
TI1_IN2	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP1_ OUT	MCO1	MCO2
TI1_IN3	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP2_ OUT	HSE_DIV32	HSE_DIV32
TI1_IN4	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP3_ OUT	RTC_ WAKEUP	RTC_ WAKEUP
TI1_IN5	-	-	-	-	COMP4_ OUT	LSE_ CSS_OUT	LSE_ CSS_OUT
TI1_IN6	-	-	-	-	-	LSI	LSI
TI1_IN7	-	-	-	-	-	-	-

Table 5-8 Timer TI1 Inputs (part 2)

Signals	GTIMA4	GTIMA5	GTIMA6	GTIMA7	GTIMB1	GTIMB2	GTIMB3
TI1_IN0	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1	EXTERNAL TI1
TI1_IN1	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	LSI	COMP1_ OUT
TI1_IN2	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	LSE_ CSS_OUT	COMP2_ OUT
TI1_IN3	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	RTC_WAKEUP	COMP3_ OUT

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TI1_IN4	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP1_ OUT	COMP4_ OUT
TI1_IN5	FDCAN1_TMP	FDCAN2_TMP	FDCAN3_TMP	FDCAN4_TMP	-	COMP2_ OUT	-
TI1_IN6	FDCAN1_RTP	FDCAN2_RTP	FDCAN3_RTP	FDCAN4_RTP	-	COMP3_ OUT	-
TI1_IN7	-	-	-	-	-	COMP4_ OUT	-

Table 5-9 Timer TI2 Inputs (part 1)

Signals	ATIM1	ATIM2	ATIM3	ATIM4	GTIMA1	GTIMA2	GTIMA3
TI2_IN0	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2
TI2_IN1	GTIMA7_CC1	GTIMA7_CC2	GTIMA7_CC3	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
TI2_IN2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
TI2_IN3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
TI2_IN4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	GTIMA6_CC1	GTIMA6_CC2	GTIMA6_CC3

Table 5-10 Timer TI2 Inputs (part 2)

Signals	GTIMA4	GTIMA5	GTIMA6	GTIMA7	GTIMB1	GTIMB2	GTIMB3
TI2_IN0	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2	EXTERNAL TI2
TI2_IN1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
TI2_IN2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
TI2_IN3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
TI2_IN4	GTIMA6_CC4	COMP4_OUT	COMP4_OUT	COMP4_OUT	GTIMA7_CC3	GTIMA7_CC4	GTIMA7_CC3

Table 5-11 Timer TI3 Inputs (part 1)

Signals	ATIM1	ATIM2	ATIM3	ATIM4	GTIMA1	GTIMA2	GTIMA3
TI3_IN0	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3
TI3_IN1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
TI3_IN2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
TI3_IN3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
TI3_IN4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

Table 5-12 Timer TI3 Inputs (part 2)

Signals	GTIMA4	GTIMA5	GTIMA6	GTIMA7	GTIMB1	GTIMB2	GTIMB3
TI3_IN0	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3	EXTERNAL TI3
TI3_IN1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT

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TI3_IN2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
TI3_IN3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
TI3_IN4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

Table 5-13 Timer TI4 Inputs (part 1)

Signals	**ATIM1**	**ATIM2**	**ATIM3**	**ATIM4**	**GTIMA1**	**GTIMA2**	**GTIMA3**
TI4_IN0	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4
TI4_IN1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
TI4_IN2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
TI4_IN3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
TI4_IN4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

Table 5-14 Timer TI4 Inputs (part 2)

Signals	**GTIMA4**	**GTIMA5**	**GTIMA6**	**GTIMA7**	**GTIMB1**	**GTIMB2**	**GTIMB3**
TI4_IN0	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4	EXTERNAL TI4
TI4_IN1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
TI4_IN2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
TI4_IN3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
TI4_IN4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

Table 5-15 Advanced Timer Break 2 Inputs

Signals	**ATIM1**	**ATIM2**	**ATIM3**	**ATIM4**
Brk2in0	BKIN2 PIN	BKIN2 PIN	BKIN2 PIN	BKIN2 PIN
Brk2in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
Brk2in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
Brk2in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
Brk2in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
Brk2in5	-	-	-	-
Brk2in6	DSMU_BRK[1]	DSMU_BRK[1]	DSMU_BRK[1]	-
Brk2in7	-	-	-	-
Brk2in8	DSMU_BRK[3]	-	DSMU_BRK[3]	DSMU_BRK[3]

Table 5-16 Advanced Timer Break Inputs

Signals	**ATIM1**	**ATIM2**	**ATIM3**	**ATIM4**	**GTIMB1**	**GTIMB2**	**GTIMB3**
brkin0	BKIN PIN	BKIN PIN	BKIN PIN	BKIN PIN	BKIN PIN	BKIN PIN	BKIN PIN
brkin1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
brkin2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT

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brkin3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
brkin4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
brkin5	DSMU_BRK[0]	DSMU_BRK[0]	DSMU_BRK[0]	-	DSMU_BRK[0]	-	-
brkin6	-	-	-	-	-	DSMU_BRK[1]	-
brkin7	DSMU_BRK[2]	-	DSMU_BRK[2]	DSMU_BRK[2]	-	-	DSMU_BRK[2]
brkin8	-	-	-	-	-	-	-

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Table 5-17 SHRTIM Burst Trigger Events and Clocks

Destination	Source
SHRTIM1_BM_TRG	BTIM1_TRGO
SHRTIM1_BM_CK1	GTIMB1_OC1
SHRTIM1_BM_CK2	GTIMB2_OC1
SHRTIM1_BM_CK3	GTIMB3_OC1
SHRTIM1_BM_CK4	BTIM1_TRGO
SHRTIM2_BM_TRG	BTIM2_TRGO
SHRTIM2_BM_CK1	GTIMB1_OC2
SHRTIM2_BM_CK2	GTIMB2_OC2
SHRTIM2_BM_CK3	GTIMB3_OC2
SHRTIM2_BM_CK4	GTIMA2_TRGO

Table 5-18 SHRTIM Update Events

Destination	Source
SHRTIM1_UPD_EN1	GTIMB1_OC1
SHRTIM1_UPD_EN2	GTIMB2_OC1
SHRTIM1_UPD_EN3	GTIMB3_OC1
SHRTIM2_UPD_EN1	GTIMB1_OC2
SHRTIM2_UPD_EN2	GTIMB2_OC2
SHRTIM2_UPD_EN3	GTIMB3_OC2
SHRTIM1_UPD_EN1	GTIMB1_OC1
SHRTIM1_UPD_EN2	GTIMB2_OC1

Table 5-19 SHRTIM Synchronization Inputs

Destination	Source
SHRTIM1_IN_SYNC1	ATIM1_TRGO
SHRTIM1_IN_SYNC2	ATIM2_TRGO
SHRTIM1_IN_SYNC3	ATIM3_TRGO
SHRTIM1_IN_SYNC4	SHRTIM1_SCIN (IO)
SHRTIM1_IN_SYNC5	SHRTIM2_OUT_SYNC2

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SHRTIM2_IN_SYNC1	ATIM1_TRGO
SHRTIM2_IN_SYNC2	ATIM2_TRGO
SHRTIM2_IN_SYNC3	ATIM3_TRGO
SHRTIM2_IN_SYNC4	SHRTIM2_SCIN (IO)
SHRTIM2_IN_SYNC5	SHRTIM1_OUT_SYNC2

Table 5-20 SHRTIM External Event Inputs

Destination	**EExSRC[1:0]=0 (from GPIO pin)**	**EExSRC[1:0]=1(1)**	**EExSRC[1:0]=2**	**EExSRC[1:0]=3**	**EExSRC[1:0]=4**
SHRTIM1_EEV1[4:1]	SHRTIM1_EEV1	COMPX_OUT	ATIM1_TRGO	ADC1_AWD1	-
SHRTIM1_EEV2[4:1]	SHRTIM1_EEV2	COMPX_OUT	GTIMA1_TRGO	ADC1_AWD2	-
SHRTIM1_EEV3[4:1]	SHRTIM1_EEV3	COMPX_OUT	GTIMA2_TRGO	ADC1_AWD3	-
SHRTIM1_EEV4[4:1]	SHRTIM1_EEV4	COMPX_OUT	ATIM2_TRGO	ADC2_AWD1	-
SHRTIM1_EEV5[4:1]	SHRTIM1_EEV5	COMPX_OUT	ATIM3_TRGO	ADC2_AWD2	FDCAN2_RTP
SHRTIM1_EEV6[4:1]	SHRTIM1_EEV6	COMPX_OUT	ATIM4_TRGO	ADC2_AWD3	FDCAN2_TMP
SHRTIM1_EEV7[4:1]	SHRTIM1_EEV7	COMPX_OUT	GTIMA6_TRGO	ADC3_AWD1	FDCAN2_SOC
SHRTIM1_EEV8[4:1]	SHRTIM1_EEV8	COMPX_OUT	GTIMA4_TRGO	ADC3_AWD2	FDCAN1_RTP
SHRTIM1_EEV9[4:1]	SHRTIM1_EEV9	COMPX_OUT	GTIMA7_TRGO	GTIMA3_TRGO	FDCAN1_TMP
SHRTIM1_EEV10[4:1]	SHRTIM1_EEV10	COMPX_OUT	GTIMA5_TRGO	ADC3_AWD3	FDCAN1_SOC
SHRTIM2_EEV1[4:1]	SHRTIM2_EEV1	COMPX_OUT	ATIM1_TRGO	ADC1_AWD1	-
SHRTIM2_EEV2[4:1]	SHRTIM2_EEV2	COMPX_OUT	GTIMA1_TRGO	ADC1_AWD2	-
SHRTIM2_EEV3[4:1]	SHRTIM2_EEV3	COMPX_OUT	GTIMA2_TRGO	ADC1_AWD3	-
SHRTIM2_EEV4[4:1]	SHRTIM2_EEV4	COMPX_OUT	ATIM2_TRGO	ADC2_AWD1	-
SHRTIM2_EEV5[4:1]	SHRTIM2_EEV5	COMPX_OUT	ATIM3_TRGO	ADC2_AWD2	FDCAN4_RTP
SHRTIM2_EEV6[4:1]	SHRTIM2_EEV6	COMPX_OUT	ATIM4_TRGO	ADC2_AWD3	FDCAN4_TMP
SHRTIM2_EEV7[4:1]	SHRTIM2_EEV7	COMPX_OUT	GTIMA6_TRGO	ADC3_AWD1	FDCAN4_SOC
SHRTIM2_EEV8[4:1]	SHRTIM2_EEV8	COMPX_OUT	GTIMA4_TRGO	ADC3_AWD2	FDCAN3_RTP
SHRTIM2_EEV9[4:1]	SHRTIM2_EEV9	COMPX_OUT	GTIMA7_TRGO	GTIMA3_TRGO	FDCAN3_TMP
SHRTIM2_EEV10[4:1]	SHRTIM2_EEV10	COMPX_OUT	GTIMA5_TRGO	ADC3_AWD3	FDCAN3_SOC

(1): comparator output selection is software programmable (comp1-4). Refer to SHRTIM chapter for more details.

Table 5-21 SHRTIM Fault Inputs

Signals	**External Input (x=1/2) FLTxSRC[1:0] = 00**	**On-chip source(1) FLTxSRC[1:0] = 01**	**External Input(2) FLTxSRC[1:0] = 10**	**On-chip source FLTxSRC[1:0] = 11**
SHRTIMX_FLT1[4:1]	SHRTIMX_FLT1	COMPX_OUT	EEV1_MUXOUT	DSMU_BRK[0]
SHRTIMX_FLT2[4:1]	SHRTIMX_FLT2	COMPX_OUT	EEV2_MUXOUT	DSMU_BRK[1]
SHRTIMX_FLT3[4:1]	SHRTIMX_FLT3	COMPX_OUT	EEV3_MUXOUT	DSMU_BRK[2]
SHRTIMX_FLT4[4:1]	SHRTIMX_FLT4	COMPX_OUT	EEV4_MUXOUT	DSMU_BRK[3]
SHRTIMX_FLT5[4:1]	SHRTIMX_FLT5	COMPX_OUT	EEV5_MUXOUT	DSMU_BRK[0]

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SHRTIMX_FLT6[4:1]	SHRTIMX_FLT6	COMPX_OUT	EEV6_MUXOUT	DSMU_BRK[1]
SHRTIMX_FLT7[4:1]	SHRTIMX_FLT7	COMPX_OUT	EEV7_MUXOUT	-
SHRTIMX_FLT8[4:1]	SHRTIMX_FLT8	COMPX_OUT	EEV8_MUXOUT	-

(1) Comparator output selection is software programmable. Refer to SHRTIM chapter for more details.

(2) External event selection is software programmable. Refer to SHRTIM chapter for more details.

5.1.2.3 ADCs

Table 5-22 ADC1/2/3 Trigger inputs

Signals	**ADC1/2/3**	
	Regular triggers	**Injected triggers**
trig0	ATIM1_CC1	ATIM1_CC1
trig1	ATIM1_CC2	ATIM1_CC2
trig2	ATIM1_CC3	ATIM1_CC3
trig3	ATIM1_CC4	ATIM1_CC4
trig4	ATIM1_TRGO	ATIM1_TRGO
trig5	ATIM2_CC1	ATIM2_CC1
trig6	ATIM2_CC2	ATIM2_CC2
trig7	ATIM2_CC3	ATIM2_CC3
trig8	ATIM1_TRGO2	ATIM1_TRGO2
trig9	ATIM2_TRGO	ATIM2_TRGO
trig10	ATIM3_CC1	ATIM3_CC1
trig11	ATIM3_CC2	ATIM3_CC2
trig12	ATIM3_CC3	ATIM3_CC3
trig13	ATIM3_CC4	ATIM3_CC4
trig14	ATIM2_TRGO2	ATIM2_TRGO2
trig15	ATIM3_TRGO	ATIM3_TRGO
trig16	ATIM4_TRGO2	ATIM4_TRGO2
trig17	ATIM3_TRGO2	ATIM3_TRGO2
trig18	ATIM4_TRGO	ATIM4_TRGO
trig19	GTIMB1_TRGO	GTIMB1_TRGO
trig20	GTIMB2_TRGO	GTIMB2_TRGO
trig21	GTIMB3_TRGO	GTIMB3_TRGO
trig22	GTIMA1_TRGO	GTIMA1_TRGO
trig23	GTIMB1_CC2	GTIMB1_CC2
trig24	GTIMB2_CC4	GTIMB2_CC4
trig25	GTIMB3_CC2	GTIMB3_CC2
trig26	GTIMA1_CC4	GTIMA1_CC4
trig27	SHRTIM1_ADC_TRG1	SHRTIM1_ADC_TRG2
trig28	SHRTIM1_ADC_TRG3	SHRTIM1_ADC_TRG4
trig29	SHRTIM2_ADC_TRG1	SHRTIM2_ADC_TRG2
trig30	SHRTIM2_ADC_TRG3	SHRTIM2_ADC_TRG4

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trig31	EXTI0~15	EXTI0~15

5.1.2.4 DACs

Table 5-23 DAC1/2 Trigger Mapping

	DAC1		**DAC2**	
	Update/reset	**Inc/Dec**	**Update/reset**	**Inc/Dec**
0	SW	SW	SW	SW
1	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO
2	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO
3	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO
4	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO
5	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO
6	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO
7	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO
8	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO
9	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO
10	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO
11	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO
12	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO
13	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO
14	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO
15	EXTI5	EXTI6	EXTI5	EXTI6
16	EXTI7	EXTI8	EXTI7	EXTI8
17	EXTI9	EXTI10	EXTI9	EXTI10
18	SHRTIM1_DAC_RESET_TRG1	SHRTIM1_STEP_TRIG1	SHRTIM1_DAC_ RESET_TRG1	SHRTIM1_STEP_TRIG1
19	SHRTIM1_DAC_ RESET_TRG2	SHRTIM1_STEP_TRIG2	SHRTIM1_DAC_ RESET_TRG2	SHRTIM1_STEP_TRIG2
20	SHRTIM1_DAC_ RESET_TRG3	SHRTIM1_STEP_TRIG3	SHRTIM1_DAC_ RESET_TRG3	SHRTIM1_STEP_TRIG3
21	SHRTIM1_DAC_ RESET_TRG4	SHRTIM1_STEP_TRIG4	SHRTIM1_DAC_ RESET_TRG4	SHRTIM1_STEP_TRIG4
22	SHRTIM1_DAC_ RESET_TRG5	SHRTIM1_STEP_TRIG5	SHRTIM1_DAC_ RESET_TRG5	SHRTIM1_STEP_TRIG5
23	SHRTIM1_DAC_ RESET_TRG6	SHRTIM1_STEP_TRIG6	SHRTIM1_DAC_ RESET_TRG6	SHRTIM1_STEP_TRIG6
24	SHRTIM1_DAC_TRG1	-	SHRTIM1_DAC_TRG1	-
25	SHRTIM2_DAC_ RESET_TRG1	SHRTIM2_STEP_TRIG1	SHRTIM2_DAC_ RESET_TRG1	SHRTIM2_STEP_TRIG1
26	SHRTIM2_DAC_ RESET_TRG2	SHRTIM2_STEP_TRIG2	SHRTIM2_DAC_ RESET_TRG2	SHRTIM2_STEP_TRIG2
27	SHRTIM2_DAC_ RESET_TRG3	SHRTIM2_STEP_TRIG3	SHRTIM2_DAC_ RESET_TRG3	SHRTIM2_STEP_TRIG3
28	SHRTIM2_DAC_ RESET_TRG4	SHRTIM2_STEP_TRIG4	SHRTIM2_DAC_ RESET_TRG4	SHRTIM2_STEP_TRIG4
29	SHRTIM2_DAC_ RESET_TRG5	SHRTIM2_STEP_TRIG5	SHRTIM2_DAC_ RESET_TRG5	SHRTIM2_STEP_TRIG5

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30	SHRTIM2_DAC_ RESET_TRG6	SHRTIM2_STEP_TRIG6	SHRTIM2_DAC_ RESET_TRG6	SHRTIM2_STEP_TRIG6
31	SHRTIM2_DAC_TRG1	-	SHRTIM2_DAC_TRG1	-

Table 5-24 DAC3/4 Trigger Mapping

	DAC3		**DAC4**	
	Update/reset	**Inc/Dec**	**Update/reset**	**Inc/Dec**
0	SW	SW	SW	SW
1	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO
2	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO
3	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO
4	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO
5	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO
6	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO
7	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO
8	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO
9	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO
10	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO
11	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO
12	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO
13	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO
14	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO
15	EXTI5	EXTI6	EXTI5	EXTI6
16	EXTI7	EXTI8	EXTI7	EXTI8
17	EXTI9	EXTI10	EXTI9	EXTI10
18	SHRTIM1_DAC_RESET_TRG1	SHRTIM1_STEP_TRIG1	SHRTIM1_DAC_ RESET_TRG1	SHRTIM1_STEP_TRIG1
19	SHRTIM1_DAC_ RESET_TRG2	SHRTIM1_STEP_TRIG2	SHRTIM1_DAC_ RESET_TRG2	SHRTIM1_STEP_TRIG2
20	SHRTIM1_DAC_ RESET_TRG3	SHRTIM1_STEP_TRIG3	SHRTIM1_DAC_ RESET_TRG3	SHRTIM1_STEP_TRIG3
21	SHRTIM1_DAC_ RESET_TRG4	SHRTIM1_STEP_TRIG4	SHRTIM1_DAC_ RESET_TRG4	SHRTIM1_STEP_TRIG4
22	SHRTIM1_DAC_ RESET_TRG5	SHRTIM1_STEP_TRIG5	SHRTIM1_DAC_ RESET_TRG5	SHRTIM1_STEP_TRIG5
23	SHRTIM1_DAC_ RESET_TRG6	SHRTIM1_STEP_TRIG6	SHRTIM1_DAC_ RESET_TRG6	SHRTIM1_STEP_TRIG6
24	SHRTIM1_DAC_TRG2	-	SHRTIM1_DAC_TRG2	-
25	SHRTIM2_DAC_ RESET_TRG1	SHRTIM2_STEP_TRIG1	SHRTIM2_DAC_ RESET_TRG1	SHRTIM2_STEP_TRIG1
26	SHRTIM2_DAC_ RESET_TRG2	SHRTIM2_STEP_TRIG2	SHRTIM2_DAC_ RESET_TRG2	SHRTIM2_STEP_TRIG2
27	SHRTIM2_DAC_ RESET_TRG3	SHRTIM2_STEP_TRIG3	SHRTIM2_DAC_ RESET_TRG3	SHRTIM2_STEP_TRIG3
28	SHRTIM2_DAC_ RESET_TRG4	SHRTIM2_STEP_TRIG4	SHRTIM2_DAC_ RESET_TRG4	SHRTIM2_STEP_TRIG4
29	SHRTIM2_DAC_ RESET_TRG5	SHRTIM2_STEP_TRIG5	SHRTIM2_DAC_ RESET_TRG5	SHRTIM2_STEP_TRIG5

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30	SHRTIM2_DAC_ RESET_TRG6	SHRTIM2_STEP_TRIG6	SHRTIM2_DAC_ RESET_TRG6	SHRTIM2_STEP_TRIG6
31	SHRTIM2_DAC_TRG2	-	SHRTIM2_DAC_TRG2	-

Table 5-25 DAC5/6 Trigger Mapping

	DAC5		**DAC6**	
	Update/reset	**Inc/Dec**	**Update/reset**	**Inc/Dec**
0	SW	SW	SW	SW
1	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO
2	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO	ATIM2_TRGO
3	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO	ATIM3_TRGO
4	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO
5	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO
6	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO
7	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO
8	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO
9	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO
10	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO
11	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO
12	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO
13	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO
14	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO
15	EXTI5	EXTI6	EXTI5	EXTI6
16	EXTI7	EXTI8	EXTI7	EXTI8
17	EXTI9	EXTI10	EXTI9	EXTI10
18	SHRTIM1_DAC_RESET_TRG1	SHRTIM1_STEP_TRIG1	SHRTIM1_DAC_RESET_TRG1	SHRTIM1_STEP_TRIG1
19	SHRTIM1_DAC_ RESET_TRG2	SHRTIM1_STEP_TRIG2	SHRTIM1_DAC_ RESET_TRG2	SHRTIM1_STEP_TRIG2
20	SHRTIM1_DAC_ RESET_TRG3	SHRTIM1_STEP_TRIG3	SHRTIM1_DAC_ RESET_TRG3	SHRTIM1_STEP_TRIG3
21	SHRTIM1_DAC_ RESET_TRG4	SHRTIM1_STEP_TRIG4	SHRTIM1_DAC_ RESET_TRG4	SHRTIM1_STEP_TRIG4
22	SHRTIM1_DAC_ RESET_TRG5	SHRTIM1_STEP_TRIG5	SHRTIM1_DAC_ RESET_TRG5	SHRTIM1_STEP_TRIG5
23	SHRTIM1_DAC_ RESET_TRG6	SHRTIM1_STEP_TRIG6	SHRTIM1_DAC_ RESET_TRG6	SHRTIM1_STEP_TRIG6
24	SHRTIM1_DAC_TRG1	-	SHRTIM1_DAC_TRG3	-
25	SHRTIM2_DAC_ RESET_TRG1	SHRTIM2_STEP_TRIG1	SHRTIM2_DAC_ RESET_TRG1	SHRTIM2_STEP_TRIG1
26	SHRTIM2_DAC_ RESET_TRG2	SHRTIM2_STEP_TRIG2	SHRTIM2_DAC_ RESET_TRG2	SHRTIM2_STEP_TRIG2
27	SHRTIM2_DAC_ RESET_TRG3	SHRTIM2_STEP_TRIG3	SHRTIM2_DAC_ RESET_TRG3	SHRTIM2_STEP_TRIG3
28	SHRTIM2_DAC_ RESET_TRG4	SHRTIM2_STEP_TRIG4	SHRTIM2_DAC_ RESET_TRG4	SHRTIM2_STEP_TRIG4

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29	SHRTIM2_DAC_ RESET_TRG5	SHRTIM2_STEP_TRIG5	SHRTIM2_DAC_ RESET_TRG5	SHRTIM2_STEP_TRIG5
30	SHRTIM2_DAC_ RESET_TRG6	SHRTIM2_STEP_TRIG6	SHRTIM2_DAC_ RESET_TRG6	SHRTIM2_STEP_TRIG6
31	SHRTIM2_DAC_TRG1	-	SHRTIM2_DAC_TRG3	-

5.1.2.5 DSMU

Table 5-26 DSMU Trigger Inputs

Signals	Trigger sources
DSMU_JTRG0	ATIM1_TRGO
DSMU_JTRG1	ATIM2_TRGO
DSMU_JTRG2	ATM3_TRGO
DSMU_JTRG3	ATIM4_TRGO
DSMU_JTRG4	GTIMB1_TRGO
DSMU_JTRG5	GTIMB2_TRGO
DSMU_JTRG6	GTIMB3_TRGO
DSMU_JTRG7	GTIMA1_TRGO
DSMU_JTRG8	GTIMA2_TRGO
DSMU_JTRG9	GTIMA3_TRGO
DSMU_JTRG10	GTIMA4_TRGO
DSMU_JTRG11	GTIMA5_TRGO
DSMU_JTRG12	ATIM1_TRGO2
DSMU_JTRG13	ATIM3_TRGO2
DSMU_JTRG14	SHRTIM1_ADC_TRG1
DSMU_JTRG15	SHRTIM1_ADC_TRG2
DSMU_JTRG16	SHRTIM1_ADC_TRG3
DSMU_JTRG17	SHRTIM1_ADC_TRG4
DSMU_JTRG18	SHRTIM2_ADC_TRG1
DSMU_JTRG19	SHRTIM2_ADC_TRG2
DSMU_JTRG20	SHRTIM2_ADC_TRG3
DSMU_JTRG21	SHRTIM2_ADC_TRG4
DSMU_JTRG22	EXTI6
DSMU_JTRG23	EXTI7
DSMU_JTRG24	EXTI8
DSMU_JTRG25	EXTI9
DSMU_JTRG26	EXTI10
DSMU_JTRG27	EXTI11
DSMU_JTRG28	EXTI12

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DSMU_JTRG29	EXTI13
DSMU_JTRG30	EXTI14
DSMU_JTRG31	EXTI15

5.1.2.6 ETHs

Table 5-27 ETH Trigger Inputs

Trigger source	Destination
GTIMB1_TRGO	ETH1_PTP0
GTIMB2_TRGO	ETH1_PTP1
FDCAN1_TMP	ETH1_PTP2
FDCAN 2_TMP	
shrtim1_dac_trg2	ETH1_PTP3
GTIMA1_TRGO	ETH2_PTP0
GTIMA2_TRGO	ETH2_PTP1
FDCAN 3_TMP	ETH2_PTP2
FDCAN 4_TMP	
shrtim2_dac_trg2	ETH2_PTP3

5.1.2.7 FDCAN

Table 5-28 FDCAN Event Inputs

Source Peripheral	Source Signal	Destination Signal	Destination Peripheral
GPTIM1	TRGO	SWT0	FDCAN1
		EVT0	
GPTIM2	TRGO	SWT1	
		EVT1	
ETH_1	PPS	SWT2	
		EVT2	
SHRTIM_1	SHRTIM1_DAC_TRG1	SWT3	
		EVT3	
GPTIM2	TRGO	SWT0	FDCAN 2
		EVT0	
GPTIM3	TRGO	SWT1	
		EVT1	

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ETH_1	PPS	SWT2	
		EVT2	
SHRTIM_1	SHRTIM1_DAC_TRG2	SWT3	
		EVT3	
GPTIM8	TRGO	SWT0	FDCAN 3
		EVT0	
GPTIM9	TRGO	SWT1	
		EVT1	
ETH_2	PPS	SWT2	
		EVT2	
SHRTIM_2	SHRTIM2_DAC_TRG1	SWT3	
		EVT3	
GPTIM9	TRGO	SWT0	FDCAN 4
		EVT0	
GPTIM10	TRGO	SWT1	
		EVT1	
ETH_2	PPS	SWT2	
		EVT2	
SHRTIM_2	SHRTIM2_DAC_TRG2	SWT3	

5.1.2.8 LPTIMER

Table 5-29 LPTIMER Trigger Inputs

Signals	Source
LPTIM_EXT_TRIG0	LPTIMX_ETR
LPTIM_EXT_TRIG1	RTC_ALRA_TRG
LPTIM_EXT_TRIG2	RTC_ALRB_TRG
LPTIM_EXT_TRIG3	RTC_TAMP1
LPTIM_EXT_TRIG4	RTC_TAMP2
LPTIM_EXT_TRIG5	RTC_TAMP3
LPTIM_EXT_TRIG6	COMP1_OUT
LPTIM_EXT_TRIG7	COMP2_OUT
LPTIM_EXT_TRIG8	COMP3_OUT
LPTIM_EXT_TRIG9	COMP4_OUT

5.1.2.9 COMP Blanking

Table 5-30 COMP Blanking Inputs

Blanking Signal	Source			
	COMP1	**COMP2**	**COMP3**	**COMP4**
1	ATIM1_OC5	ATIM1_OC5	ATIM1_OC5	GTIMB2_OC4
2	GTIMB1_OC5	GTIMB1_OC5	GTIMB2_OC5	ATIM2_OC5

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3	GTIMB2_OC5	GTIMB2_OC5	GTIMB1_OC4	GTIMB1_OC4
4	ATIM2_OC5	ATIM2_OC5	ATIM2_OC5	ATIM1_OC5
5	ATIM3_OC5	ATIM3_OC5	ATIM3_OC5	ATIM3_OC5
6	GTIMA4_OC1	GTIMA4_OC1	GTIMA4_OC1	GTIMA4_OC1
7	GTIMB3_OC5	GTIMB3_OC5	GTIMB3_OC5	GTIMB3_OC5
8	ATIM4_OC5	ATIM4_OC5	ATIM4_OC5	GTIMB2_OC3
9	GTIMA2_OC3	GTIMA2_OC3	GTIMA4_OC2	ATIM4_OC5
10	GTIMA1_OC3	GTIMA1_OC3	GTIMA1_OC3	GTIMA1_OC3
11	GTIMA3_OC3	GTIMA3_OC3	GTIMA3_OC3	GTIMA3_OC3
12	GTIMA5_OC3	GTIMA5_OC3	GTIMA5_OC3	GTIMA5_OC3
13	GTIMA6_OC3	GTIMA6_OC3	GTIMA6_OC3	GTIMA6_OC3
14	GTIMA7_OC3	GTIMA7_OC3	GTIMA7_OC3	GTIMA7_OC3

5.2 DMA

5.2.1 Introduction

N32H7xxx has one MDMA and 3 DMAs. The MDMA enables data transfer between memories as well as peripherals in the AXI bus domain. The DMA1/2/3 enables memory transfer in the AHB domains. DMA transfers can be triggered by software or hardware.

DMA_MUX1 is used to map any peripheral DMA requests to any DMA1/2/3. In addition, DMAMUX1 enables synchronization of a DMA request with a timer or external GPIO or a DMA transfer complete. DMA requests itself can be generated from trigger events such as timers/GPIO/the completion of another DMA transfers.

DMAMUX2 has the same function, except synchronization, but it is dedicated for MDMA.

5.2.2 DMA Mapping Details

Table 5-31 DMAMUX2 DMA request inputs

DMAMUX2 Request Inputs	Source Signal	Source Peripherals
DMAMUX2_REQ_IN1	DMAMUX_REQ_GEN0	DMAMUX2 (Internal request generator)
DMAMUX2_REQ_IN2	DMAMUX_REQ_GEN1	
DMAMUX2_REQ_IN3	DMAMUX_REQ_GEN2	
DMAMUX2_REQ_IN4	DMAMUX_REQ_GEN3	
DMAMUX2_REQ_IN5	DMAMUX_REQ_GEN4	
DMAMUX2_REQ_IN6	DMAMUX_REQ_GEN5	
DMAMUX2_REQ_IN7	DMAMUX_REQ_GEN6	
DMAMUX2_REQ_IN8	DMAMUX_REQ_GEN7	
DMAMUX2_REQ_IN9	DMAMUX_REQ_GEN8	
DMAMUX2_REQ_IN10	DMAMUX_REQ_GEN9	
DMAMUX2_REQ_IN11	DMAMUX_REQ_GEN10	

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DMAMUX2_REQ_IN12	DMAMUX_REQ_GEN11	
DMAMUX2_REQ_IN13	DMAMUX_REQ_GEN12	
DMAMUX2_REQ_IN14	DMAMUX_REQ_GEN13	
DMAMUX2_REQ_IN15	DMAMUX_REQ_GEN14	
DMAMUX2_REQ_IN16	DMAMUX_REQ_GEN15	
DMAMUX2_REQ_IN17	NC	
DMAMUX2_REQ_IN18	NC	
DMAMUX2_REQ_IN19	NC	
DMAMUX2_REQ_IN20	NC	
DMAMUX2_REQ_IN21	NC	
DMAMUX2_REQ_IN22	NC	
DMAMUX2_REQ_IN23	NC	
DMAMUX2_REQ_IN24	NC	
DMAMUX2_REQ_IN25	DMA_REQ_TX	xSPI1
DMAMUX2_REQ_IN26	DMA_REQ_RX	xSPI1
DMAMUX2_REQ_IN27	DMA_REQ_TX	xSPI2
DMAMUX2_REQ_IN28	DMA_REQ_RX	xSPI2

Table 5-32 DMAMUX2 DMA Trigger Inputs

DMAMUX2 Trigger Inputs	Source Signal	Source Peripheral
DMAMUX2_TRG_IN1	DMA1_INT_TFR0 (TRANSFER COMPLETE)	DMA1
DMAMUX2_TRG_IN2	DMA1_INT_TFR1 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN3	DMA1_INT_TFR2 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN4	DMA1_INT_TFR3 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN5	DMA1_INT_TFR4 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN6	DMA1_INT_TFR5 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN7	DMA1_INT_TFR6 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN8	DMA1_INT_TFR7 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN9	DMA2_ INT_TRF0 (TRANSFER COMPLETE)	DMA2
DMAMUX2_TRG_IN10	DMA2_ INT_TRF1 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN11	DMA2_ INT_TRF2 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN12	DMA2_ INT_TRF3 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN13	DMA2_ INT_TRF4 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN14	DMA2_ INT_TRF5 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN15	DMA2_ INT_TRF6 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN16	DMA2_ INT_TRF7 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN17	DMA3_ INT_TRF0 (TRANSFER COMPLETE)	DMA3
DMAMUX2_TRG_IN18	DMA3_ INT_TRF1 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN19	DMA3_ INT_TRF2 (TRANSFER COMPLETE)	

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DMAMUX2_TRG_IN20	DMA3_ INT_TRF3 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN21	DMA3_ INT_TRF4 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN22	DMA3_ INT_TRF5 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN23	DMA3_ INT_TRF6 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN24	DMA3_ INT_TRF7 (TRANSFER COMPLETE)	
DMAMUX2_TRG_IN25	LCDC_LI_IT	LCDC
DMAMUX2_TRG_IN26	GPU_SPEC_INT	GPU
DMAMUX2_TRG_IN27	JPEG_SGDMA_H2P_INT	JPEG CODEC
DMAMUX2_TRG_IN28	JPEG_SGDMA_P2H_INT	JPEG CODEC
DMAMUX2_TRG_IN29	MIPI DSI INT	DSIHOST
DMAMUX2_TRG_IN30	USB1 INT	USBCTRL1
DMAMUX2_TRG_IN31	USB2 INT	USBCTRL2
DMAMUX2_TRG_IN32	SDMMC1 INT	SDMMC1
DMAMUX2_TRG_IN33	SDMMC2 INT	SDMMC2
DMAMUX2_TRG_IN34	DVP1 INT	DVP1
DMAMUX2_TRG_IN35	DVP2 INT	DVP2
DMAMUX2_TRG_IN36	ETH1 INT	ETH1
DMAMUX2_TRG_IN37	ETH2 INT	ETH2
DMAMUX2_TRG_IN38	SDPU INT	SDPU

Table 5-33 DMAMUX1 DMA Request Inputs

DMAMUX1 Request Inputs	**Source Signal**	**Source Peripherals**
DMAMUX1_REQ_IN1	DMAMUX_REQ_GEN0	DMAMUX1 (Internal request generator)
DMAMUX1_REQ_IN2	DMAMUX_REQ_GEN1	
DMAMUX1_REQ_IN3	DMAMUX_REQ_GEN2	
DMAMUX1_REQ_IN4	DMAMUX_REQ_GEN3	
DMAMUX1_REQ_IN5	DMAMUX_REQ_GEN4	
DMAMUX1_REQ_IN6	DMAMUX_REQ_GEN5	
DMAMUX1_REQ_IN7	DMAMUX_REQ_GEN6	
DMAMUX1_REQ_IN8	DMAMUX_REQ_GEN7	
DMAMUX1_REQ_IN9	ADC1_DMA	ADC1
DMAMUX1_REQ_IN10	ADC2_DMA	ADC2
DMAMUX1_REQ_IN11	ADC3_DMA	ADC3
DMAMUX1_REQ_IN12	SHRTIM_DMA0	SHRTIM1
DMAMUX1_REQ_IN13	SHRTIM_DMA1	
DMAMUX1_REQ_IN14	SHRTIM_DMA2	
DMAMUX1_REQ_IN15	SHRTIM_DMA3	
DMAMUX1_REQ_IN16	SHRTIM_DMA4	
DMAMUX1_REQ_IN17	SHRTIM_DMA5	

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DMAMUX1_REQ_IN18	SHRTIM_DMA6	
DMAMUX1_REQ_IN19	SHRTIM_DMA0	SHRTIM2
DMAMUX1_REQ_IN20	SHRTIM_DMA1	
DMAMUX1_REQ_IN21	SHRTIM_DMA2	
DMAMUX1_REQ_IN22	SHRTIM_DMA3	
DMAMUX1_REQ_IN23	SHRTIM_DMA4	
DMAMUX1_REQ_IN24	SHRTIM_DMA5	
DMAMUX1_REQ_IN25	SHRTIM_DMA6	
DMAMUX1_REQ_IN26	ATIM_UP_DMA	ATIM1
DMAMUX1_REQ_IN27	ATIM_CH1_DMA	
DMAMUX1_REQ_IN28	ATIM_CH2_DMA	
DMAMUX1_REQ_IN29	ATIM_CH3_DMA	
DMAMUX1_REQ_IN30	ATIM_CH4_DMA	
DMAMUX1_REQ_IN31	ATIM_COM_DMA	
DMAMUX1_REQ_IN32	ATIM_TRG_DMA	
DMAMUX1_REQ_IN33	ATIM_UP_DMA	ATIM2
DMAMUX1_REQ_IN34	ATIM_CH1_DMA	
DMAMUX1_REQ_IN35	ATIM_CH2_DMA	
DMAMUX1_REQ_IN36	ATIM_CH3_DMA	
DMAMUX1_REQ_IN37	ATIM_CH4_DMA	
DMAMUX1_REQ_IN38	ATIM_COM_DMA	
DMAMUX1_REQ_IN39	ATIM_TRG_DMA	
DMAMUX1_REQ_IN40	ATIM_UP_DMA	ATIM3
DMAMUX1_REQ_IN41	ATIM_CH1_DMA	
DMAMUX1_REQ_IN42	ATIM_CH2_DMA	
DMAMUX1_REQ_IN43	ATIM_CH3_DMA	
DMAMUX1_REQ_IN44	ATIM_CH4_DMA	
DMAMUX1_REQ_IN45	ATIM_COM_DMA	
DMAMUX1_REQ_IN46	ATIM_TRG_DMA	
DMAMUX1_REQ_IN47	ATIM_UP_DMA	ATIM4
DMAMUX1_REQ_IN48	ATIM_CH1_DMA	
DMAMUX1_REQ_IN49	ATIM_CH2_DMA	
DMAMUX1_REQ_IN50	ATIM_CH3_DMA	
DMAMUX1_REQ_IN51	ATIM_CH4_DMA	
DMAMUX1_REQ_IN52	ATIM_COM_DMA	
DMAMUX1_REQ_IN53	ATIM_TRG_DMA	
DMAMUX1_REQ_IN54	GTIMA_CH1_DMA	GTIMA1
DMAMUX1_REQ_IN55	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN56	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN57	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN58	GTIMA_TRG_DMA	

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DMAMUX1_REQ_IN59	GTIMA_UP	
DMAMUX1_REQ_IN60	GTIMA_CH1_DMA	GTIMA2
DMAMUX1_REQ_IN61	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN62	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN63	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN64	GTIMA_TRG_DMA	
DMAMUX1_REQ_IN65	GTIMA_UP	
DMAMUX1_REQ_IN66	GTIMA_CH1_DMA	GTIMA3
DMAMUX1_REQ_IN67	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN68	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN69	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN70	GTIMA_TRG_DMA	
DMAMUX1_REQ_IN71	GTIMA_UP	
DMAMUX1_REQ_IN72	GTIMA_CH1_DMA	GTIMA4
DMAMUX1_REQ_IN73	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN74	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN75	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN76	GTIMA_TRG_DMA	
DMAMUX1_REQ_IN77	GTIMA_UP	
DMAMUX1_REQ_IN78	GTIMA_CH1_DMA	GTIMA5
DMAMUX1_REQ_IN79	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN80	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN81	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN82	GTIMA_TRG_DMA	
DMAMUX1_REQ_IN83	GTIMA_UP	
DMAMUX1_REQ_IN84	GTIMA_CH1_DMA	GTIMA6
DMAMUX1_REQ_IN85	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN86	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN87	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN88	GTIMA_TRG_DMA	
DMAMUX1_REQ_IN89	GTIMA_UP	
DMAMUX1_REQ_IN90	GTIMA_CH1_DMA	GTIMA7
DMAMUX1_REQ_IN91	GTIMA_CH2_DMA	
DMAMUX1_REQ_IN92	GTIMA_CH3_DMA	
DMAMUX1_REQ_IN93	GTIMA_CH4_DMA	
DMAMUX1_REQ_IN94	GTIMA_TRG_DMA	
DMAMUX1_REQ_IN95	GTIMA_UP	
DMAMUX1_REQ_IN96	GTIMB_CH1_DMA	GTIMB1
DMAMUX1_REQ_IN97	GTIMB_CH2_DMA	
DMAMUX1_REQ_IN98	GTIMB_CH3_DMA	
DMAMUX1_REQ_IN99	GTIMB_CH4_DMA	

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DMAMUX1_REQ_IN100	GTIMB_TRG_DMA	
DMAMUX1_REQ_IN101	GTIMB_UP	
DMAMUX1_REQ_IN102	GTIMB_CH1_DMA	GTIMB2
DMAMUX1_REQ_IN103	GTIMB_CH2_DMA	
DMAMUX1_REQ_IN104	GTIMB_CH3_DMA	
DMAMUX1_REQ_IN105	GTIMB_CH4_DMA	
DMAMUX1_REQ_IN106	GTIMB_TRG_DMA	
DMAMUX1_REQ_IN107	GTIMB_UP	
DMAMUX1_REQ_IN108	GTIMB_CH1_DMA	GTIMB3
DMAMUX1_REQ_IN109	GTIMB_CH2_DMA	
DMAMUX1_REQ_IN110	GTIMB_CH3_DMA	
DMAMUX1_REQ_IN111	GTIMB_CH4_DMA	
DMAMUX1_REQ_IN112	GTIMB_TRG_DMA	
DMAMUX1_REQ_IN113	GTIMB_UP	
DMAMUX1_REQ_IN114	I2C_DMA_RX	I2C1
DMAMUX1_REQ_IN115	I2C_DMA_TX	
DMAMUX1_REQ_IN116	I2C_DMA_RX	I2C2
DMAMUX1_REQ_IN117	I2C_DMA_TX	
DMAMUX1_REQ_IN118	I2C_DMA_RX	I2C3
DMAMUX1_REQ_IN119	I2C_DMA_TX	
DMAMUX1_REQ_IN120	I2C_DMA_RX	I2C4
DMAMUX1_REQ_IN121	I2C_DMA_TX	
DMAMUX1_REQ_IN122	I2C_DMA_RX	I2C5
DMAMUX1_REQ_IN123	I2C_DMA_TX	
DMAMUX1_REQ_IN124	I2C_DMA_RX	I2C6
DMAMUX1_REQ_IN125	I2C_DMA_TX	
DMAMUX1_REQ_IN126	I2C_DMA_RX	I2C7
DMAMUX1_REQ_IN127	I2C_DMA_TX	
DMAMUX1_REQ_IN128	I2C_DMA_RX	I2C8
DMAMUX1_REQ_IN129	I2C_DMA_TX	
DMAMUX1_REQ_IN130	I2C_DMA_RX	I2C9
DMAMUX1_REQ_IN131	I2C_DMA_TX	
DMAMUX1_REQ_IN132	I2C_DMA_RX	I2C10
DMAMUX1_REQ_IN133	I2C_DMA_TX	
DMAMUX1_REQ_IN134	USART_RX_DMA	USART1
DMAMUX1_REQ_IN135	USART_TX_DMA	
DMAMUX1_REQ_IN136	USART_RX_DMA	USART2
DMAMUX1_REQ_IN137	USART_TX_DMA	
DMAMUX1_REQ_IN138	USART_RX_DMA	USART3
DMAMUX1_REQ_IN139	USART_TX_DMA	
DMAMUX1_REQ_IN140	USART_RX_DMA	USART4

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DMAMUX1_REQ_IN141	USART_TX_DMA	
DMAMUX1_REQ_IN142	USART_RX_DMA	USART5
DMAMUX1_REQ_IN143	USART_TX_DMA	
DMAMUX1_REQ_IN144	USART_RX_DMA	USART6
DMAMUX1_REQ_IN145	USART_TX_DMA	
DMAMUX1_REQ_IN146	USART_RX_DMA	USART7
DMAMUX1_REQ_IN147	USART_TX_DMA	
DMAMUX1_REQ_IN148	USART_RX_DMA	USART8
DMAMUX1_REQ_IN149	USART_TX_DMA	
DMAMUX1_REQ_IN150	UART_RX_DMA,	UART9
DMAMUX1_REQ_IN151	UART_TX_DMA	
DMAMUX1_REQ_IN152	UART_RX_DMA	UART10
DMAMUX1_REQ_IN153	UART_TX_DMA	
DMAMUX1_REQ_IN154	UART_RX_DMA	UART11
DMAMUX1_REQ_IN155	UART_TX_DMA	
DMAMUX1_REQ_IN156	UART_RX_DMA	UART12
DMAMUX1_REQ_IN157	UART_TX_DMA	
DMAMUX1_REQ_IN158	UART_RX_DMA	UART13
DMAMUX1_REQ_IN159	UART_TX_DMA	
DMAMUX1_REQ_IN160	UART_RX_DMA	UART14
DMAMUX1_REQ_IN161	UART_TX_DMA	
DMAMUX1_REQ_IN162	UART_RX_DMA	UART15
DMAMUX1_REQ_IN163	UART_TX_DMA	
DMAMUX1_REQ_IN164	SPI1_RX_DMA	SPI1
DMAMUX1_REQ_IN165	I2S1_TX_DMA	I2S1
DMAMUX1_REQ_IN166	SPI2_RX_DMA	SPI2
DMAMUX1_REQ_IN167	I2S2_TX_DMA	I2S2
DMAMUX1_REQ_IN168	SPI3_RX_DMA	SPI3
DMAMUX1_REQ_IN169	I2S3_TX_DMA	I2S3
DMAMUX1_REQ_IN170	SPI4_RX_DMA	SPI4
DMAMUX1_REQ_IN171	I2S4_TX_DMA	I2S4
DMAMUX1_REQ_IN172	SPI5_RX_DMA	SPI5
DMAMUX1_REQ_IN173	SPI1_TX_DMA	SPI1
DMAMUX1_REQ_IN174	SPI6_RX_DMA	SPI6
DMAMUX1_REQ_IN175	SPI2_TX_DMA	SPI2
DMAMUX1_REQ_IN176	SPI7_RX_DMA	SPI7
DMAMUX1_REQ_IN177	SPI3_TX_DMA	SPI3
DMAMUX1_REQ_IN178	I2S1_RX_DMA	I2S1
DMAMUX1_REQ_IN179	SPI4_TX_DMA	SPI4
DMAMUX1_REQ_IN180	I2S2_RX_DMA	I2S2

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DMAMUX1_REQ_IN181	SPI5_TX_DMA	SPI5
DMAMUX1_REQ_IN182	I2S3_RX_DMA	I2S3
DMAMUX1_REQ_IN183	SPI6_TX_DMA	SPI6
DMAMUX1_REQ_IN184	I2S4_RX_DMA	I2S4
DMAMUX1_REQ_IN185	SPI7_TX_DMA	SPI7
DMAMUX1_REQ_IN186	LPUART_DMA_RX	LPUART1
DMAMUX1_REQ_IN187	LPUART_DMA_TX	
DMAMUX1_REQ_IN188	LPUART_DMA_RX	LPUART2
DMAMUX1_REQ_IN189	LPUART_DMA_TX	
DMAMUX1_REQ_IN190	DAC1_DMA_REQ	DAC12
DMAMUX1_REQ_IN191	DAC2_DMA_REQ	
DMAMUX1_REQ_IN192	DMA_REQ0	DSMU
DMAMUX1_REQ_IN193	DMA_REQ1	
DMAMUX1_REQ_IN194	DMA_REQ2	
DMAMUX1_REQ_IN195	DMA_REQ3	
DMAMUX1_REQ_IN196	FDCAN_DMA_REQ	FDCAN 1
DMAMUX1_REQ_IN197	FDCAN _DMA_REQ	FDCAN 2
DMAMUX1_REQ_IN198	FDCAN _DMA_REQ	FDCAN 3
DMAMUX1_REQ_IN199	FDCAN _DMA_REQ	FDCAN 4
DMAMUX1_REQ_IN200	FDCAN _DMA_REQ	FDCAN 5
DMAMUX1_REQ_IN201	FDCAN _DMA_REQ	FDCAN 6
DMAMUX1_REQ_IN202	FDCAN _DMA_REQ	FDCAN 7
DMAMUX1_REQ_IN203	FDCAN _DMA_REQ	FDCAN 8
DMAMUX1_REQ_IN204	CORDIC_DMA_RD	CORDIC
DMAMUX1_REQ_IN205	CORDIC_DMA_WR	
DMAMUX1_REQ_IN206	FMAU_DMA_RD	FMAU
DMAMUX1_REQ_IN207	FMAU_DMA_WR	
DMAMUX1_REQ_IN208	BTIM_DMA_REQ	BTIM1
DMAMUX1_REQ_IN209	BTIM_DMA_REQ	BTIM2
DMAMUX1_REQ_IN210	BTIM_DMA_REQ	BTIM3
DMAMUX1_REQ_IN211	BTIM_DMA_REQ	BTIM4
DMAMUX1_REQ_IN212	GTIMB _COM_DMA	GTIMB1
DMAMUX1_REQ_IN213	GTIMB _COM_DMA	GTIMB2
DMAMUX1_REQ_IN214	GTIMB _COM_DMA	GTIMB3
DMAMUX1_REQ_IN215	DAC3_DMA_REQ	DAC34
DMAMUX1_REQ_IN216	DAC4_DMA_REQ	DAC34
DMAMUX1_REQ_IN217	DAC5_DMA_REQ	DAC56
DMAMUX1_REQ_IN218	DAC6_DMA_REQ	DAC56

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Table 5-34 DMAMUX1 DMA Trigger Inputs

DMAMUX1 Trigger inputs	Source
DMAMUX1_TRG_IN1	Any of dmamux_evt0-7
DMAMUX1_TRG_IN2	Any of dmamux_evt8-15
DMAMUX1_TRG_IN3	Any of dmamux_evt16-23
DMAMUX1_TRG_IN4	LPTIMER4_OUT
DMAMUX1_TRG_IN5	LPTIMER3_OUT
DMAMUX1_TRG_IN6	LPTIMER2_OUT
DMAMUX1_TRG_IN7	LPTIMER1_OUT
DMAMUX1_TRG_IN8	IOM_EXTI0
DMAMUX1_TRG_IN9	FDCAN1 IRQ0
DMAMUX1_TRG_IN10	FDCAN2 IRQ0
DMAMUX1_TRG_IN11	FDCAN3 IRQ0
DMAMUX1_TRG_IN12	FDCAN4 IRQ0
DMAMUX1_TRG_IN13	FDCAN5 IRQ0
DMAMUX1_TRG_IN14	FDCAN6 IRQ0
DMAMUX1_TRG_IN15	FDCAN7 IRQ0
DMAMUX1_TRG_IN16	FDCAN8 IRQ0
DMAMUX1_TRG_IN17	LPTIMER5_OUT
DMAMUX1_TRG_IN18	ESC_IRQ
DMAMUX1_TRG_IN19	FDCAN1 IRQ1
DMAMUX1_TRG_IN20	FDCAN2 IRQ1
DMAMUX1_TRG_IN21	FDCAN3 IRQ1
DMAMUX1_TRG_IN22	FDCAN4 IRQ1
DMAMUX1_TRG_IN23	FDCAN5 IRQ1
DMAMUX1_TRG_IN24	FDCAN6 IRQ1
DMAMUX1_TRG_IN25	FDCAN7 IRQ1
DMAMUX1_TRG_IN26	FDCAN8 IRQ1

Table 5-35 DMAMUX1 DMA Synchronization Inputs

DMAMUX1 Synchronization inputs	Source
DMAMUX1_SYNC_IN1	Any of dmamux_evt0-7
DMAMUX1_SYNC_IN2	Any of dmamux_evt8-15
DMAMUX1_SYNC_IN3	Any of dmamux_evt16-23
DMAMUX1_SYNC_IN4	LPTIMER5_OUT
DMAMUX1_SYNC_IN5	LPTIMER4_OUT
DMAMUX1_SYNC_IN6	LPTIMER3_OUT
DMAMUX1_SYNC_IN7	LPTIMER2_OUT
DMAMUX1_SYNC_IN8	LPTIMER1_OUT

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DMAMUX1_SYNC_IN9	IOM_EXTI0

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6 SDRAM Controller

6.1 Introduction

There is one SDRAM controller connected to the AHB bus. It provides access up to two external SDRAM/LPSDRAM memory devices.

6.2 Main Features

The main features supported by SDRAM are shown below:

- Two SDRAM devices with independent configuration
- 8-bit, 16-bit, 32-bit data bus width
- 13-bits Address Row, 11-bits Address Column, 4 internal banks: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)
- Row address configurable as 11,12, 13 bit, Column address configurable as 8,9,10,11 bit
- Word, half-word, byte access
- Automatic row and bank boundary management
- Support for burst mode
- Write access protection
- Programmable timing parameters
- Support Software reset
- SDRAM power-up initialization by software
- CAS latency of 1,2,3
- Automatic Refresh operation with programmable Refresh rate
- SDRAM suspend and wakeup by software

6.3 Block Diagram

The block diagram of SDRAM controller with a wrapper is shown below:

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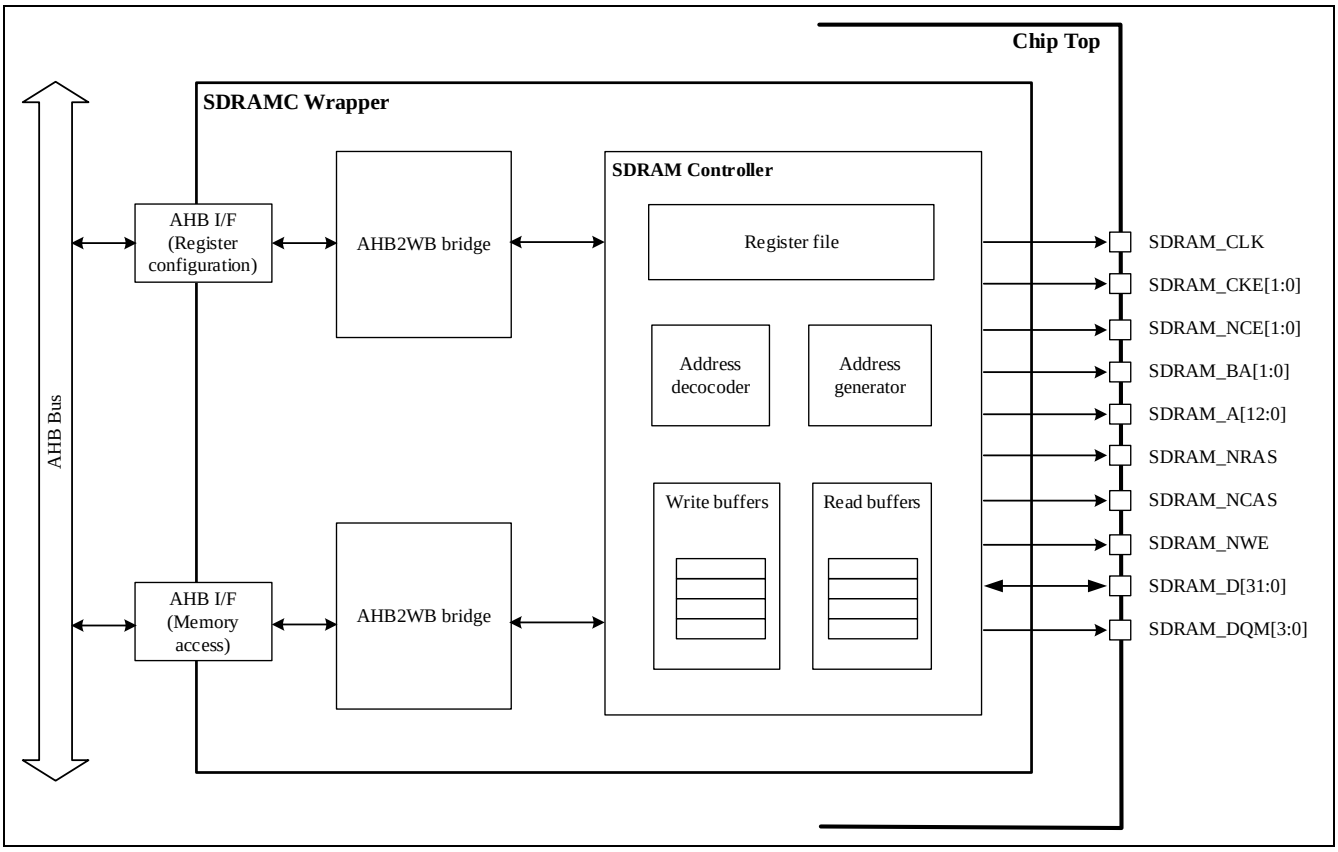
Figure 6-1 SRAM Controller Block Diagram



6.4 Pin Definitions

Table 39-1 shows the pins used by SDRAMC and their corresponding functions.

Table 6-1 SDRAMC Pin Definitions

Pin Name	IO type	Description
SDRAM_CLK	Output	SDRAM clock
SDRAM_CKE[1:0]	Output	SDRAM_CKE0: SDRAM Device 1 Clock Enable SDRAM_CKE1: SDRAM Device 2 Clock Enable
SDRAM_NCE[1:0]	Output	SDRAM_NCE0: SDRAM Device 1 Chip Enable SDRAM_NCE1: SDRAM Device 2 Chip Enable
SDRAM_BA[1:0]	Output	Bank Address
SDRAM_A[12:0]	Output	Address (Column address, Row address)
SDRAM_NRAS	Output	Row Address Strobe
SDRAM_NCAS	Output	Column Address Strobe
SDRAM_NWE	Output	Write Enable
SDRAM_D[31:0]	Inout	Bidirectional data bus
SDRAM_DQM[3:0]	Output	Output Byte Mask for write accesses

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6.5 Function Description

6.5.1 Clock and Reset

There are 2 clock domains with SDRAM controller:

- AHB Bus domain: It is used for both register configuration and memory access. Maximum clock frequency is 300Mhz.
- Memory clock domain: It is used for external memory device. Maximum clock frequency is 133Mhz.

Note: There is a delay version of memory clock input to SDRAM controller. This clock is used for sampling the read data from external memory with the delay compensation on pad. The delay value is configurable, see RCC_PLLSFTLK.SDRAMDLSEL and RCC_PLLSFTLK.SDRAMDLEN registers for more detail.

6.5.2 SDRAM GPIO configuration

Each pin of SDRAM controllers can be connected to SDRAM device pin throughout several GPIO ports. It is configurable to select which port is used for each pin. Table 6-2 summarize the basic GPIO registers configuration for cases of external SDRAM and SiP SDRAM, respectively.

Note-1: There are some GPIO port options configured to connect to one SDRAM pin (e.g. SDRAM_CKE0 can be selected to connect to PC3, PH2, or PC5), however, user must only connect one GPIO port to one SDRAM pin at one time.

Note-2: There are some other GPIO registers and AFIO registers related to SDRAM (e.g. GPIOx_DS, AFIO_SDRAM_HSMOD_CFGn, AFIO_SDRAM_VREF_ENn, AFIO_SDRAMDSN_CFGn or AFIO_SDRAMDSP_CFGn), refer to chapter of GPIO and AFIO for more detail in case user wants to change their default setting.

Table 6-2 SDRAM GIPO configuration

SDRAM pin	External SDRAM		SiP SDRAM	
	GPIO port	Remap	GPIO Registers Setting	
SDRAM_A0	PF0	AF0	PE8	AF1
SDRAM_A1	PF1	AF0	PE9	AF1
SDRAM_A2	PF2	AF0	PE10	AF1
SDRAM_A3	PF3	AF0	PE11	AF7
SDRAM_A4	PF4	AF0	PH6	AF1
SDRAM_A5	PF5	AF0	PH7	AF10
SDRAM_A6	PF12	AF0	PH8	AF1
SDRAM_A7	PF13	AF0	PH9	AF11
SDRAM_A8	PF14	AF0	PH10	AF1
SDRAM_A9	PF15	AF0	PH11	AF9
SDRAM_A10	PG0	AF0	PG1	AF1
SDRAM_A11	PG1	AF0	PH12	AF1

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SDRAM pin	External SDRAM		SiP SDRAM	
	GPIO port	Remap	GPIO Registers Setting	
SDRAM_A12	PG2	AF0	-	-
SDRAM_BA0	PG4	AF0	PF15	AF1
SDRAM_BA1	PG5	AF0	PG0	AF1
SDRAM_CKE0	PC3	AF0	PD14	AF1
	PH2	AF0		
	PC5	AF0		
SDRAM_CKE1	PH7	AF0	-	-
	PB5	AF0		
SDRAM_CLK	PG8	AF0	PG8	AF0
SDRAM_D0	PD14	AF0	PI4	AF10
SDRAM_D1	PD15	AF0	PI5	AF1
SDRAM_D2	PD0	AF0	PI6	AF10
SDRAM_D3	PD1	AF0	PI7	AF1
SDRAM_D4	PE7	AF0	PF4	AF1
SDRAM_D5	PE8	AF0	PF1	AF1
SDRAM_D6	PE9	AF0	PI9	AF10
	PC12	AF0		
SDRAM_D7	PE10	AF0	PI10	AF1
	PD2	AF0		
SDRAM_D8	PA4	AF0	PI1	AF1
	PE11	AF0		
SDRAM_D9	PA5	AF0	PI2	AF11
	PE12	AF0		
SDRAM_D10	PE13	AF0	PI3	AF1
	PB14	AF0		
SDRAM_D11	PE14	AF0	PD0	AF1
	PB15	AF0		
SDRAM_D12	PC0	AF1	PD1	AF1
	PE15	AF0		
SDRAM_D13	PD8	AF0	PD2	AF1
SDRAM_D14	PD9	AF0	PG15	AF7
SDRAM_D15	PD10	AF0	PE1	AF9
SDRAM_D16	PH8	AF0	-	-
SDRAM_D17	PH9	AF0		
SDRAM_D18	PH10	AF0		
SDRAM_D19	PH11	AF0		
SDRAM_D20	PH12	AF0		
SDRAM_D21	PH13	AF0		
SDRAM_D22	PH14	AF0		

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SDRAM pin	External SDRAM		SiP SDRAM	
	GPIO port	Remap	GPIO Registers Setting	
SDRAM_D23	PH15	AF0		
SDRAM_D24	PI0	AF0		
SDRAM_D25	PI1	AF0		
SDRAM_D26	PI2	AF0		
SDRAM_D27	PI3	AF0		
SDRAM_D28	PI6	AF0		
SDRAM_D29	PI7	AF0		
SDRAM_D30	PI9	AF0		
SDRAM_D31	PI10	AF0		
SDRAM_DQM0	PE0	AF0	PA5	AF1
SDRAM_DQM1	PE1	AF0	PG2	AF1
SDRAM_DQM2	PI4	AF0	-	-
SDRAM_DQM3	PI5	AF0		
SDRAM_NRAS	PF11	AF0	PF11	AF0
SDRAM_NCAS	PG15	AF0	PC5	AF7
SDRAM_NCE0	PC2	AF0	PF13	AF1
	PH3	AF0		
	PC4	AF0		
SDRAM_NCE1	PH6	AF0	-	-
	PB6	AF0		
SDRAM_NWE	PC0	AF0	PA7	AF0
	PH5	AF0		
	PA7	AF0		

6.5.3 SDRAM Initialization

Software must configure SDRAM controller's registers after power up and GPIO configuration, to gain access to all connected memory devices. SDRAMC configuration registers are accessed through the AHB configuration register interface.

6.5.3.1 SDRAM device's initialization sequence

Software must perform the initialization sequence for SDRAM type of memory devices in the order described below. Failing to do so may result in an undefined behavior.

1. Calculate burst length for each synchronous device connected to the SDRAM controller:

   Burst Length = 64 / Memory Bus Width (in bit).

2. Perform the SDRAM initialization sequence for every connected SDRAM device using the SDRAM Operation Setup Register and the SDRAM Operation Request Register. The initialization requirements are described in the SDRAM device's datasheet.

3. Configure Base Address and Address Mask registers

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4. Configure Refresh Interval Register
5. Configure all SDRAM Timing Registers
6. Configure all Chip Select Configuration Registers

See chapter 6.5.3.2 for an example of SDRAM initialization.

6.5.3.2 SDRAM initialization example

SDRAM Device models' information:

Table 6-3 SDRAM device model's size

Model name	Vendor	Connected to	Memory Size	Number of Rows	Number of Columns
M12L64164A(2C)	ESMT	SDRAM 1	1M x 16-Bit x 4 Banks	4096(12bits row address)	256 (8bits column address)
M12L128168A	ESMT	SDRAM 2	2M x 16-Bit x 4 Banks	4096(12bits row address)	512 (9bits column address)

Table 6-4 SDRAM device model's mode register

Model name	Mode register							
	BA0-BA1	A13-A10/AP	A9	A8-A7	A6-A4	A3	A2-A0	
	RFU	RFU	W.B.L	TM	CAS Latency	Burst Type	Burst Length	
M12L64164A(2C)	RFU	RFU	0: Burst 1: Single	00: Mode Register test Others: Reserved	010: 2 011: 3 Others: Reserved	0: Sequential 1: Interleave	* BT=0: 000:1 001:2 010:4 011:8 111: 256 Others: Reserved	* BT=1: 000:1 001:2 010:4 011:8 Others: Reserved
M12L128168A	RFU	RFU	0: Burst 1: Single	00: Mode Register test Others: Reserved	010: 2 011: 3 Others: Reserved	0: Sequential 1: Interleave	* BT=0: 000:1 001:2 010:4 011:8 111: 512 Others: Reserved	* BT=1: 000:1 001:2 010:4 011:8 Others: Reserved

Table 6-5 SDRAM device mode's timing requirement

SDRAM Manual Parameters	Symbol	M12L64164A(2C)	M12L128168A	Timing register
Row active to row active delay	$t_{RRD(min)}$	10ns	10ns	SDRAM_RRDLY
RAS to CAS delay	$t_{RCD(min)}$	15ns	15ns	SDRAM_RCDLY
Row Precharge time	$t_{RP(min)}$	15ns	15ns	SDRAM_PT

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Row active time	$t_{RAS(min\sim max)}$	38ns~100us	38ns~100us	SDRAM_RAT
Row cycle time (Operating)	$t_{RC(min)}$	53ns	53ns	SDRAM_RCT
Row cycle time (Auto refresh)	$t_{RFC(min)}$	55ns	55ns	SDRAM_RFCT
Last data in to row precharge	$t_{RDL(min)}$	2 cycles	2 cycles	SDRAM_WRT
Refresh period(1)	-	64ms(4096 rows)	64ms(4096 rows)	SDRAM_RI

Note(1): Calculation formula reference Table 6-6 step-4.

Below table shows the necessary configuration clock is steps:

Table 6-6 SDRAM initialization flow example

Step No.	Detail description	Remark
1.	**Calculate burst length** For these SDRAM models, memory data bit widths both are 16-bit, hence: ● SDRAM1: Burst length = 64 / 16 = 4 ● SDRAM2: Burst length = 64 / 16 = 4	Burst length should be set same for the controller register and device mode registers in step 2.4
2.	**SDRAM Initialization**	
2.1.	Power on stable By default, after reset CKE=High, DQM=High, and other pins in inactive state(Note: check it if the status is not like that). Ensure this state is kept at least 200μs before next steps.	-
2.2.	Precharge all banks 1. Configure SDRAM_OS register ● CKEN: 1'b1 ● OPCODE[1:0]: 2'b01 (Precharge All Banks) ● CS[1:0]: 2'b00 (SDRAM 1 and SDRAM 2 are selected) ● BANKADD[1:0]: 2'b00 (don't care) ● ADD[13:0]: 14'h0000 (don't care) => SDRAM_OS: 32'h5000_0000 2. Read (or Write) SDRAM_OR register *Note: This is a dummy access to activate previous SDRAM_OS register configuration, hence the read/write data is "don't care".*	-
2.3.	Auto-refresh 1. Configure SDRAM_OS register ● CKEN: 1'b1 (allow Auto-refresh) ● OPCODE[1:0]: 2'b10 (Auto-refresh) ● CS[1:0]: 2'b00 (SDRAM 1 and SDRAM 2 are selected) ● BANKADD[1:0]: 2'b00 (don't care) ● ADD[13:0]: 14'h0000 (don't care) => SDRAM_OS: 32'h6000_0000 2. Read (or Write) SDRAM_OR register	-

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	3. Repeat 1 and 2 above once more at least	
2.4.	Load Mode Register 1. Configure SDRAM_OS register ● CKEN: 1'b1 ● OPCODE[1:0]: 2'b11 (Load Mode Register) ● CS[1:0]: 2'b00 (SDRAM 1 and SDRAM 2 are selected) *Note: Both models use same Mode register scheme hence it can use one command. In case of different mode registers, separate the command for each device* ● BANKADD[1:0]: 2'b00 (don't care since the models do not use) ● ADD[13:0]: 14'h0032 A13-A10: not used by the models A9: 1'b0 (Write Burst Length mode = Burst) A8-A7: 2'b00 (Mode Register Set) A6-A4: 3'b011 (CAS Latency=3) A3: 1'b0 (Burst Type=Sequential) A2-A0: 3'b010 (Burst Length=4) => SDRAM_OS: 32'h7000_0032 2. Read (or Write) SDRAM_OR register	The bit definitions of ADD[13:0] are consistent with Table 6-4
3.	**Configure SDRAM_BADDx and SDRAM_ADDMASKx**	
3.1.	Configure SDRAM1 (M12L64164A) This device is total 1M x 16bit x 4banks = 8Mbytes. Therefore, the address range used: 0xC000_0000-0xC07F_FFFF Based on this, configure registers as following: => SDRAM_BADD1: 32'hC000_0000 => SDRAM_ADDMASK1: 32'hFF80_0000	Address map assigned for SDRAM1 is 0xC000_0000-0xCFFF_FFFF. However, this device model uses a smaller range of it.
3.2.	Configure SDRAM2 (M12L128168A) This device is total 2M x 16bit x 4banks = 16Mbytes. Therefore, the address range used: 0xD000_0000-0xD0FF_FFFF Based on this, configure registers as following: => SDRAM_BADD2: 32'hD000_0000 => SDRAM_ADDMASK2: 32'hFF00_0000	SDRAM2 is 0xD000_0000-0xDFFF_FFFF. However, this device model uses a smaller range of it.
4.	**Configure SDRAM_RI register** Value set for this register is calculated as below: Refresh Interval = (Refresh Period / Number of Rows / Mem clock Period) For these devices test: ● Refresh period = 64ms = 64000000 ns ● Number of rows = 4096 (both devices) ● Mem clock period = 10ns (100MHz) Refresh Interval = 64000000/4096/10 ≈ 1562. For a reliable refresh interval, it should bet set to smaller number, hence:	If two devices have different requirement on Refresh period, calculate and use the smaller value.

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	=> SDRAM_RI: 32'h0000_05DC (1500)	
5.	**Configure all SDRAM Timing Registers** Based on device datasheet, configure necessary timing parameters. For these devices, under memory clock = 100Mhz (10ns), it can be configured as following: => Row Active Time Register (SDRAM_RAT): 4 => Row Cycle Time Register (SDRAM_RCT): 6 => Row Active to Row Active Delay Register (SDRAM_RRDLY): 2 => Precharge Time Register (SDRAM_PT): 2 => Write Recovery Time Register (SDRAM_WRT): 3 => Refresh Cycle Time Register (SDRAM_RFCT): 6 => RAS to CAS Delay Time Register (SDRAM_RCDLY): 2	The values setting in this example are typical values. Can change them as long as they satisfy device's timing requirement. If two devices have different requirement on Refresh period, calculate and use the smaller or higher values, which can satisfy all devices.
6.	**Configure SDRAM_CFGx**	
6.1.	Configure SDRAM1 (M12L64164A) ● SDRAM Enable (bit[31]): 1'b1 ● Refresh Enable (bit[30]): 1'b1 ● Auto Precharge Enable (bit[23]): 1'b1 ● Mem bus width (bit[22:21]): 2'b01 (16-bit) ● Burst length (bit[20:18]): 3'b011 (length=4) ● CAS Latency (bit[17:16]): 2'b11 ● Prefetch Enable (bit[9]): 1'b1 ● SOM Enable (bit[8]): 1'b1 ● Bank Interleave Enable (bit[4]): 1'b1 ● Address configuration (bit[3:0]): 4'b0000 (4 banks, 4096 rows, 256 columns) => SDRAM_CFG1: 32'hC0AF_0310	CAS Latency setting must be same with the value set for device mode register
6.2.	Configure SDRAM2 (M12L128168A) ● SDRAM Enable (bit[31]): 1'b1 ● Refresh Enable (bit[30]): 1'b1 ● Auto Precharge Enable (bit[23]): 1'b1 ● Mem bus width (bit[22:21]): 2'b01 (16-bit) ● Burst length (bit[20:18]): 3'b011 (length=4) ● CAS Latency (bit[17:16]): 2'b11 ● Prefetch Enable (bit[9]): 1'b1 ● SOM Enable (bit[8]): 1'b1 ● Bank Interleave Enable (bit[4]): 1'b1 ● Address configuration (bit[3:0]): 4'b0001 (4 banks, 4096 rows, 512 columns) => SDRAM_CFG2: 32'hC0AF_0311	CAS Latency setting must be same with the value set for device mode register

Note-1: Memory clock assumed operated at 100Mhz (clock cycle=10ns)

Note-2: Need to calculate correctly the maximum burst length. If set to smaller number than needed, the data can be lost. If set to larger, it affects to access performance.

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Note-3: The value can be changed depended on device features or user intention

6.5.3.3 SDRAM Mode Register value requirements

There are a few requirements for the SDRAM device Mode Register value that have to be met to assure proper operation:

- The Burst Length field must be set to the value that corresponds to the Burst Length value calculated in step 1 of the SDRAM initialization sequence.
- Burst Type must be sequential.
- CAS Latency field must be set to the value that corresponds to the CAS Latency programmed into the Chip SDRAM Configuration Registers. CAS Latency depends on the speed of the device. SDRAMC supports CAS Latencies of 1, 2 and 3.
- Write Burst Mode must be set to Programmed Burst Length.
- Make sure that the settings in the SDRAM Configuration Register represent the values written to the Mode Register for each connected device.

6.5.4 SDRAM device's Address Range

Each SDRAM device can occupy from 64KB to 256MB of address space. Values written to **Base Address Register** and **Address Mask Register** (see chapter 6.6) define the address range that device occupies. SDRAM device is considered enabled and will be used in address decoding, when bit SDRAMEN in the **SDRAM Configuration Register** is set to 1. SDRAM device chip select is selected, when the memory access address (from system) and the value of the **Base Address Register**, both masked with the value of **Address Mask Register**, are equal:

Chip select = (Memory access address[31:0] & Address Mask [31:0]) = = (Base Address[31:0] & Address Mask[31:0])

*Note: Error is generated in case the memory access address decodes to the address range not covered by any of the enabled chip selects. Do not program **Base Address Register** and **Address Mask Register** to values that would result in chip select's address range overlapping with other SDRAM device chip selects' address ranges. Overlapping address region access will lead to wrong operation.*

According to system address map, the base address of SDRAM 1 is 0xC00000000 and SDRAM 2 is 0xD0000000. Table 6-7 shows the detail of SDRAM device address range and size, which this SDRAMC supports.

Base Address Register value is 0xC00000000(SDRAM1 value) or 0xD00000000(SDRAM2 value)

Address Mask Register value is (0xFFFFFFFF-(SDRAM device size-1))

Table 6-7 SDRAM device address range supported

Device	Base Address Register Value	Address Mask Register Value	Address Range	SDRAM Size(byte)
SDRAM 1	0xC0000000	0xFFFF0000	0xC0000000 – 0xC000FFFF	64KB

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	0xC0000000	0xFFFE0000	0xC0000000 – 0xC001FFFF	128KB
	0xC0000000	0xFFFC0000	0xC0000000 – 0xC003FFFF	256KB
	0xC0000000	0xFFF80000	0xC0000000 – 0xC007FFFF	512KB
	0xC0000000	0xFFF00000	0xC0000000 – 0xC00FFFFF	1MB
	0xC0000000	0xFFE00000	0xC0000000 – 0xC01FFFFF	2MB
	0xC0000000	0xFFC00000	0xC0000000 – 0xC03FFFFF	4MB
	0xC0000000	0xFF800000	0xC0000000 – 0xC07FFFFF	8MB
	0xC0000000	0xFF000000	0xC0000000 – 0xC0FFFFFF	16MB
	0xC0000000	0xFE000000	0xC0000000 – 0xC1FFFFFF	32MB
	0xC0000000	0xFC000000	0xC0000000 – 0xC3FFFFFF	64MB
	0xC0000000	0xF8000000	0xC0000000 – 0xC7FFFFFF	128MB
	0xC0000000	0xF0000000	0xC0000000 – 0xCFFFFFFF	256MB
SDRAM 2	0xD0000000	0xFFFF0000	0xD0000000 – 0xD000FFFF	64KB
	0xD0000000	0xFFFE0000	0xD0000000 – 0xD001FFFF	128KB
	0xD0000000	0xFFFC0000	0xD0000000 – 0xD003FFFF	256KB
	0xD0000000	0xFFF80000	0xD0000000 – 0xD007FFFF	512KB
	0xD0000000	0xFFF00000	0xD0000000 – 0xD00FFFFF	1MB
	0xD0000000	0xFFE00000	0xD0000000 – 0xD01FFFFF	2MB
	0xD0000000	0xFFC00000	0xD0000000 – 0xD03FFFFF	4MB
	0xD0000000	0xFF800000	0xD0000000 – 0xD07FFFFF	8MB
	0xD0000000	0xFF000000	0xD0000000 – 0xD0FFFFFF	16MB
	0xD0000000	0xFE000000	0xD0000000 – 0xD1FFFFFF	32MB
	0xD0000000	0xFC000000	0xD0000000 – 0xD3FFFFFF	64MB
	0xD0000000	0xF8000000	0xD0000000 – 0xD7FFFFFF	128MB
	0xD0000000	0xF0000000	0xD0000000 – 0xDFFFFFFF	256MB

Note: The remap function doesn't affect to base address and address map value calculated in this table, i.e. user must always use the base address 0xC00000000 for the calculation even the base address of SDRAM 1 is switched to 0x60000000 when remap enabled.

6.5.5 Accessing SDRAM devices timing diagrams

Access to SDRAM memory device is initiated when:

- There is a read or write access through the SDRAM controller's AHB Memory Access Interface.
- The read or write cycle's address is located within one of the enabled SDRAM device's address range.

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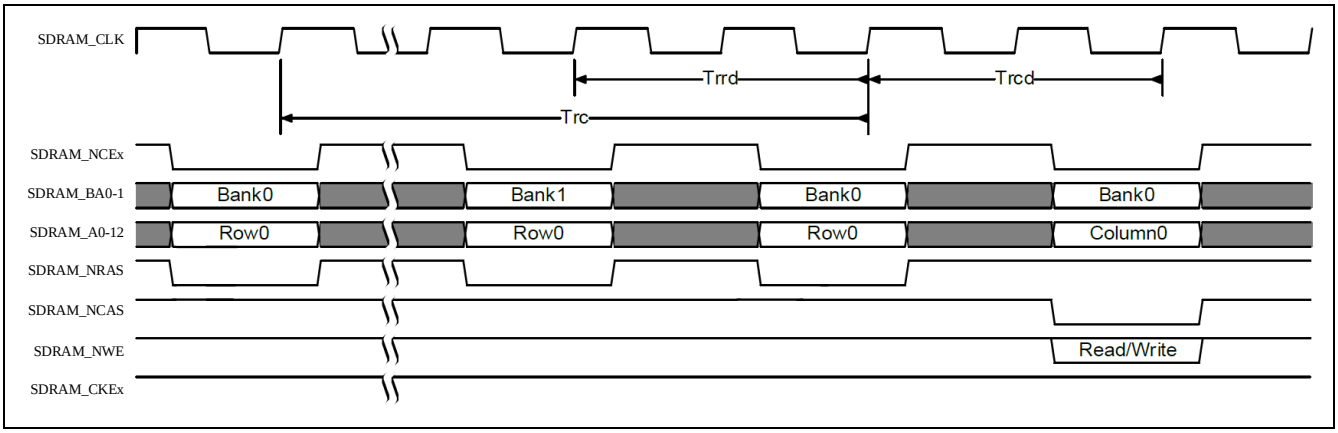
- The SDRAM Operation is requested using the access to SDRAM Operation Request Register.
- The SDRAM Write Operation is necessary to flush the write buffers, requested using the write access to Synchronous Memory Buffer Operations Register.

6.5.5.1 Row Activation

Before the core can write to or read from any SDRAM device, the row hit by the access address must be activated.

Figure 6-2 SDRAM Row activation



SDRAM Row is activated when:

- Current SDRAM read or write operation hits currently closed row.
- Current SDRAM read or write operation hits currently precharged bank.
- **Row Cycle Time** is not violated.
- **Row Active To Row Active** delay is not violated.
- **Precharge Time** is not violated.
- **Refresh Cycle Time** is not violated.

Description of timing parameters:

- **T_{rc} – Row Cycle Time** – also RAS Cycle Time. This parameter is set in the Row Cycle Time Register.
- **T_{rrd} – Row Active to Row Active Delay** – Defines the minimum delay between two Active commands to different banks on the same SDRAM device. The parameter is set in the Row Active to Row Active Delay Register.
- **T_{rcd} – RAS to CAS Delay** – Defines minimum delay between Row Active command and Read or Write command to the same bank in the same SDRAM device. The parameter is set in the RAS to CAS Delay Register.

6.5.5.2 Single Write Transfer without Auto Precharge

Figure 6-3 Single SDRAM Write without Auto Precharge

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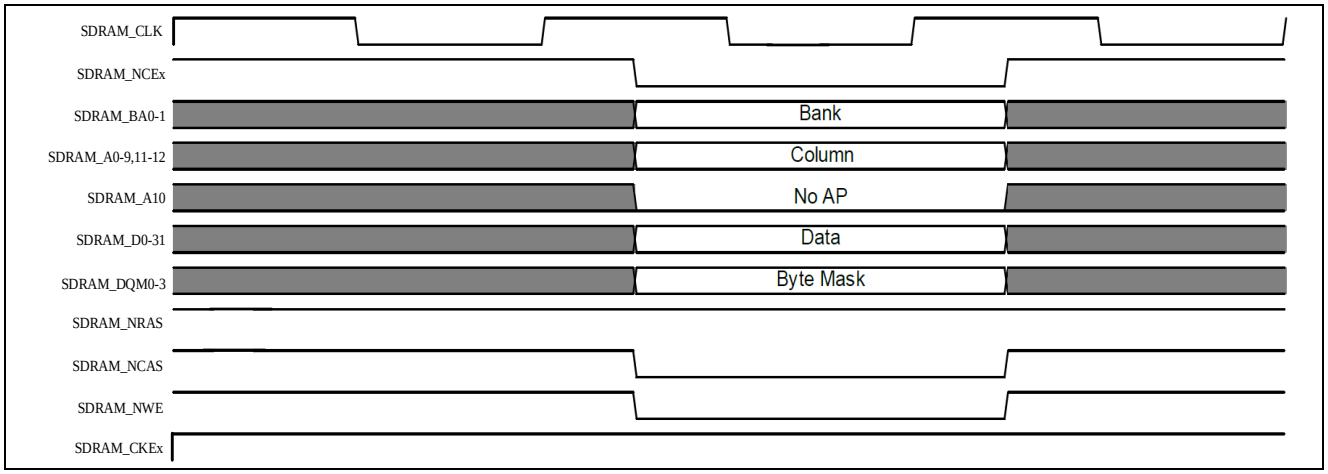
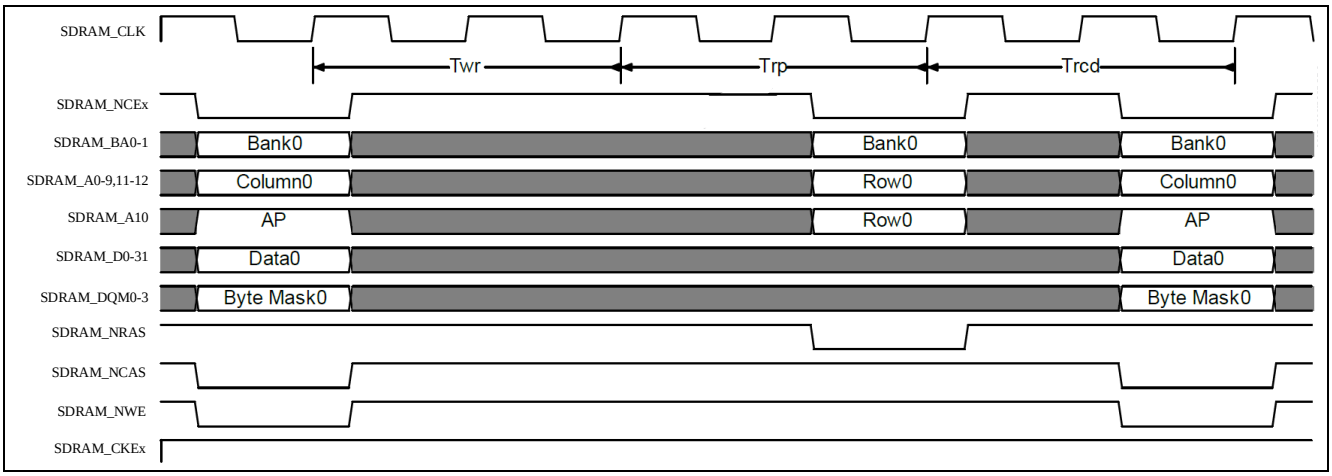


Single SDRAM Write without Auto Precharge is initiated when:

- Current SDRAM write operation hits already open row.
- The **Burst Length** field, a part of the SDRAM Configuration Register, is set to length 1. The software must program the **Burst Length** field to the value that corresponds to the mode register value written to the SDRAM memory device.
- RAS to CAS Delay is not violated.
- The **Auto** Precharge **Enable** bit, a part of the SDRAM Configuration Register, is set to 0 (disabled).

6.5.5.3 Single Write Transfer with Auto Precharge

Figure 6-4 Single SDRAM Write with Auto Precharge



Single SDRAM Write with Auto Precharge is initiated under the same conditions as Single SDRAM Write without Auto Precharge, except:

- The **Auto Precharge** Enable bit, a part of the SDRAM Configuration Register, is set to 1 (enabled).

Description of timing parameters:

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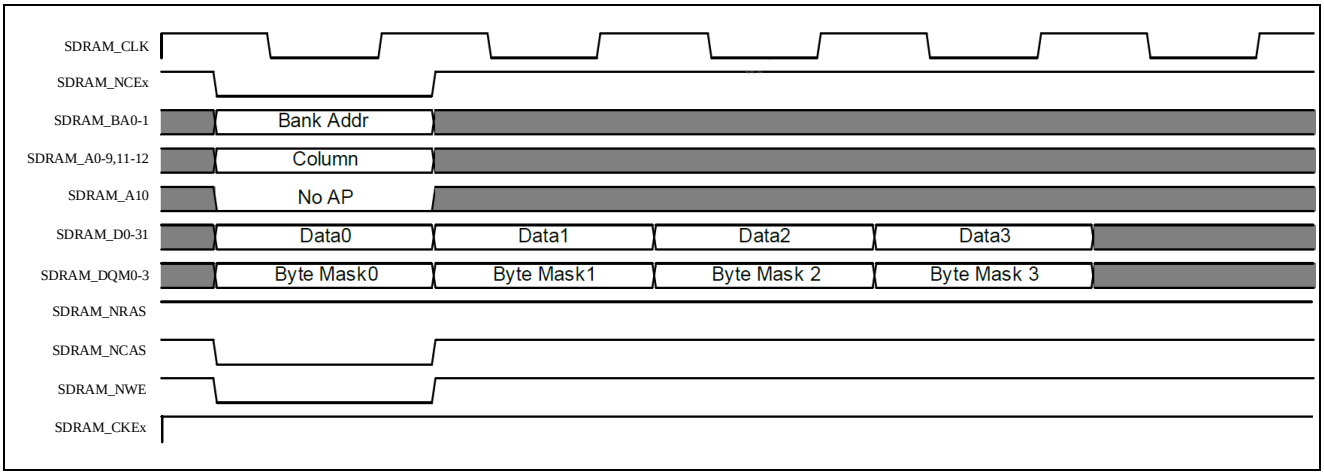
- **T_{wr} – Write Recovery Time** – This parameter is set in the Write Recovery Time Register. The SDRAM memory device issues internal precharge command **Write Recovery Time** after the write command was issued.
- **T_{rp} – Precharge Time** – This parameter is set in the Precharge Time Register. The controller must not access a specific row in a bank for **Precharge Time** after internal or external precharge command was issued.
- **T_{rcd}** – See chapter 6.5.5.1 Row Activation.

6.5.5.4 Burst Write Transfer without Auto Precharge

Figure 6-5 Burst SDRAM Write without Auto Precharge



Burst SDRAM Write without Auto Precharge is initiated when:

- Current SDRAM write operation hits already open row.
- The **Burst Length** field, a part of the SDRAM Configuration Register, is set to length greater than 1. The software must program the **Burst Length** field to the value that corresponds to the mode register value written to the SDRAM memory device. The controller terminates Write Burst without Auto Precharge when all valid bytes from the write buffer have been written to the memory.
- RAS to CAS Delay is not violated.
- The **Auto Precharge Enable** bit, a part of the SDRAM Configuration Register, is set to 0 (disabled).

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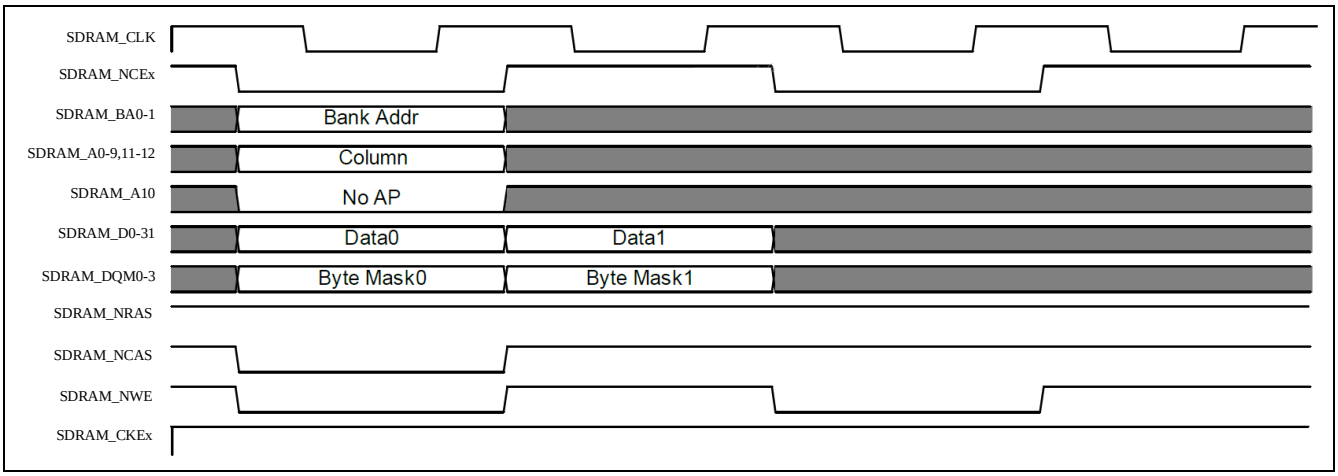
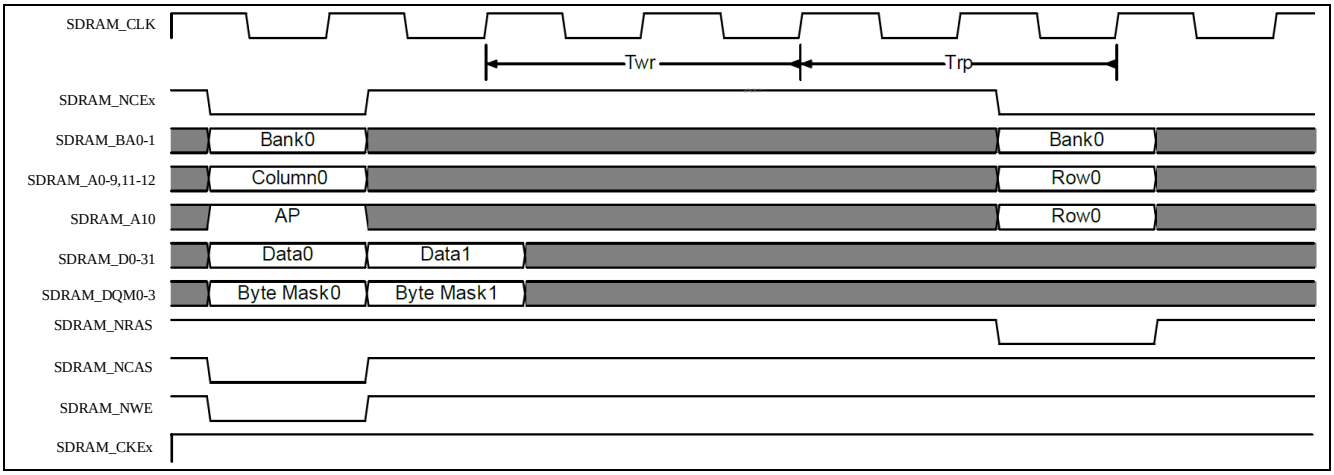
Figure 6-6 Write Burst Terminate



Write bursts with Auto Precharge disabled are terminated on the clock cycle following the clock cycle the last valid byte from the write buffer was written to the memory. The Error: Reference source not found shows a write burst of length 4 or 8 terminated after the second write transfer.

6.5.5.5 Burst Write Transfer with Auto Precharge

Figure 6-7 Burst SDRAM write with Auto Precharge



Burst SDRAM write with Auto Precharge is initiated under the same conditions as burst SDRAM write without Auto Precharge, except:

- The Auto **Precharge** Enable bit, a part of the SDRAM Configuration Register, is set to 1 (enabled).
- The Memory Controller does not terminate Write with Auto Precharge bursts. It always performs full-programmed burst length write, regardless of the number of valid bytes stored in the write buffer. It masks invalid bytes using DQM signals. For description of timing parameters, see Single Write Transfer with Auto Precharge.

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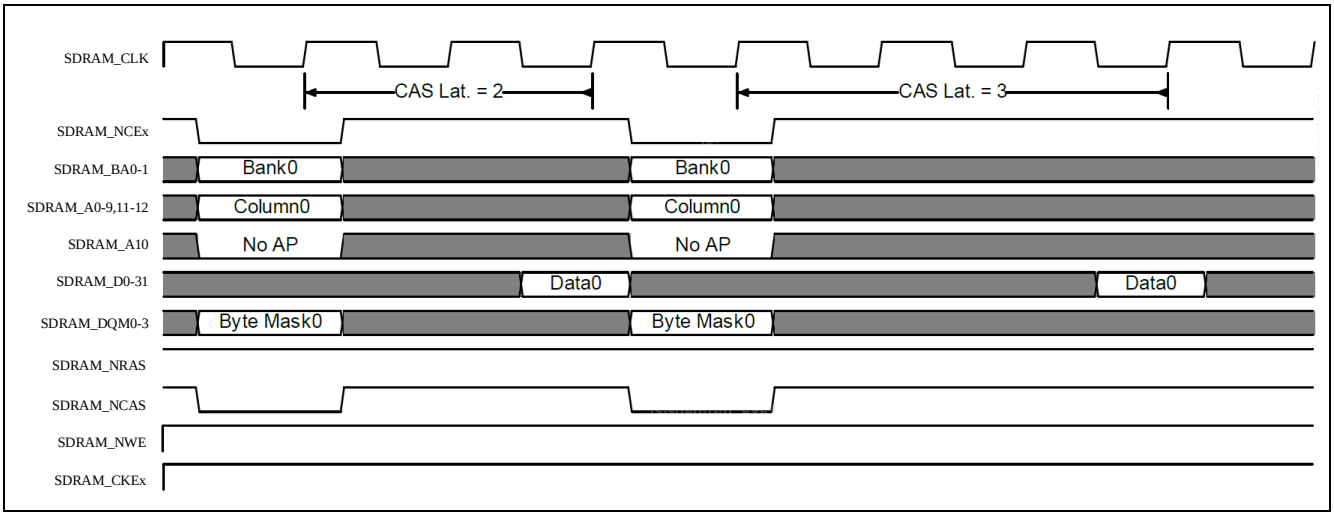
6.5.5.6 Single Read Transfer without Auto Precharge

Figure 6-8 Single SDRAM read without Auto Precharge



Single SDRAM read without Auto Precharge is initiated when:

- Current SDRAM read operation address hits already open row.
- The **Burst Length** field, a part of the SDRAM Configuration Register, is set to length 1. The software must set the **Burst Length** field to the value that corresponds to mode register value written to the SDRAM memory device.
- RAS to CAS Delay is not violated.
- The **Auto Precharge Enable** bit, a part of the SDRAM Configuration Register, is set to 0 (disabled).

Description of timing parameter:

- **CAS Latency** – Set for each chip select separately in the **CAS Latency** field, a part of the SDRAM Configuration Register. Software must set this field to a value corresponding to the CAS Latency value written to the SDRAM device's mode register.

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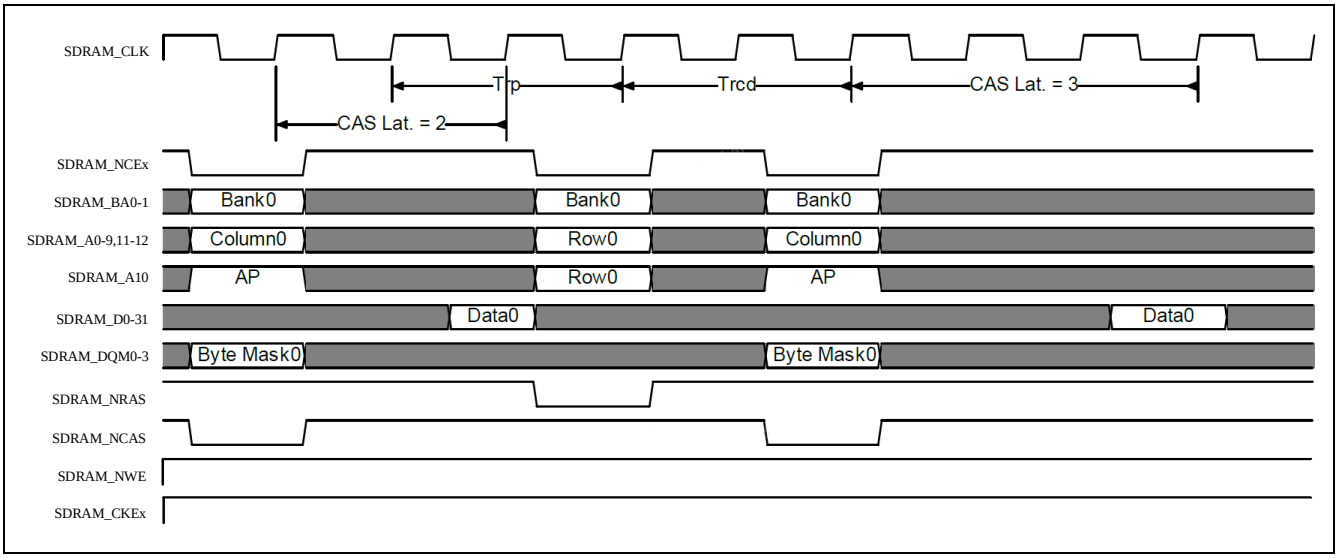
6.5.5.7 Single Read Transfer with Auto Precharge

Figure 6-9 Single SDRAM read with Auto Precharge



Single SDRAM read with auto precharge is initiated under the same conditions as single SDRAM read without auto precharge, except:

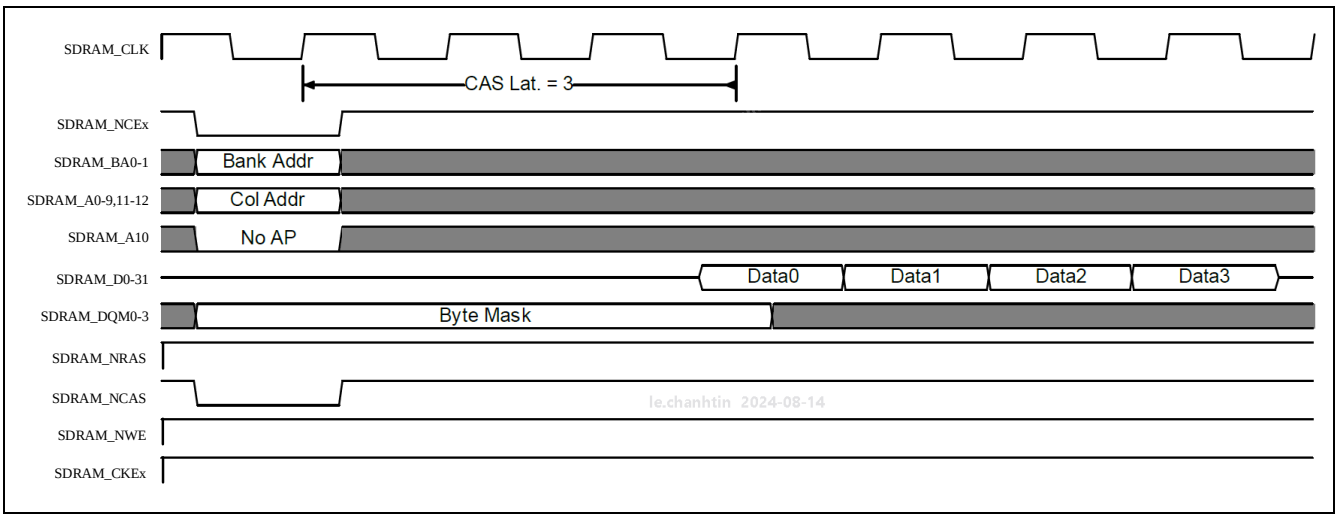
- The **Auto Precharge Enable** bit, a part of the Chip Select Configuration Register, is set to 1 (enabled).

Description of timing parameters:

- **CAS Latency** – See chapter 6.5.5.6 Single Read Transfer without Auto Precharge.
- **T_{rp} – Precharge Time** – parameter is set in the Precharge Time Register**.** Subsequent access to the same row is not allowed for **Precharge Time** after internal precharge command was executed.
- **T_{rcd} – RAS to CAS Delay** – See chapter 6.5.5.1 Row Activation.

6.5.5.8 Burst Read Transfer without Auto Precharge

Figure 6-10 Burst SDRAM read without Auto Precharge



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Burst SDRAM read without Auto Precharge is initiated when:

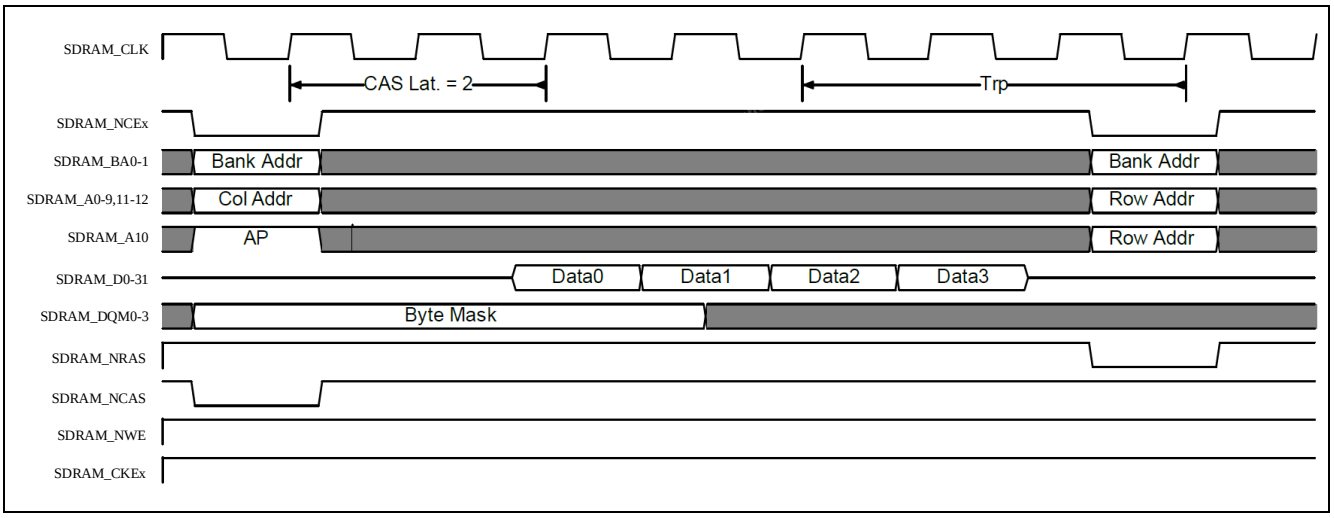
- The current SDRAM Read operation address hits already open row.
- The **Burst Length** field, a part of the SDRAM Configuration Register, is set to length larger than 1. The software must set the **Burst Length** field to the value that corresponds to the mode register value written to the SDRAM memory device. Complete burst is executed every time the Read operation is initiated.
- RAS to CAS Delay is not violated – See chapter 6.5.5.1 Row Activation.
- The **Auto Precharge Enable** bit, a part of the SDRAM Configuration Register is set to 0 (disabled).

Description of timing parameters:

- **CAS Latency** – See chapter 6.5.5.6 Single Read Transfer without Auto Precharge.

6.5.5.9 Burst Read Transfer with Auto Precharge

Figure 6-11 Burst SDRAM read with Auto Precharge



Burst SDRAM read with auto precharge is initiated under the same conditions as burst SDRAM read without auto precharge, except:

- The **Auto Precharge Enable** bit, a part of the SDRAM Configuration Register, is set to 1 (enabled).

Description of timing parameters:

- **CAS Latency** – See chapter 6.5.5.6 Single Read Transfer without Auto Precharge.
- $\mathbf{T_{rp}}$ – See chapter 6.5.5.7 Single Read Transfer with Auto Precharge.

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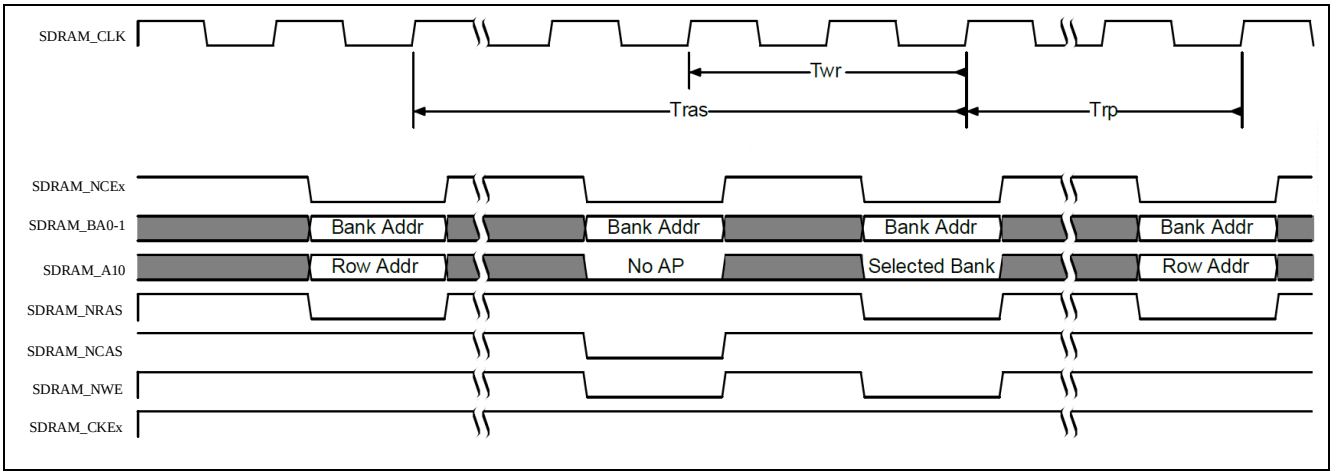
6.5.5.10 Precharge Selected Bank

Figure 6-12 Precharge Selected SDRAM Bank



Precharge of the specific bank in the SDRAM device is initiated when:

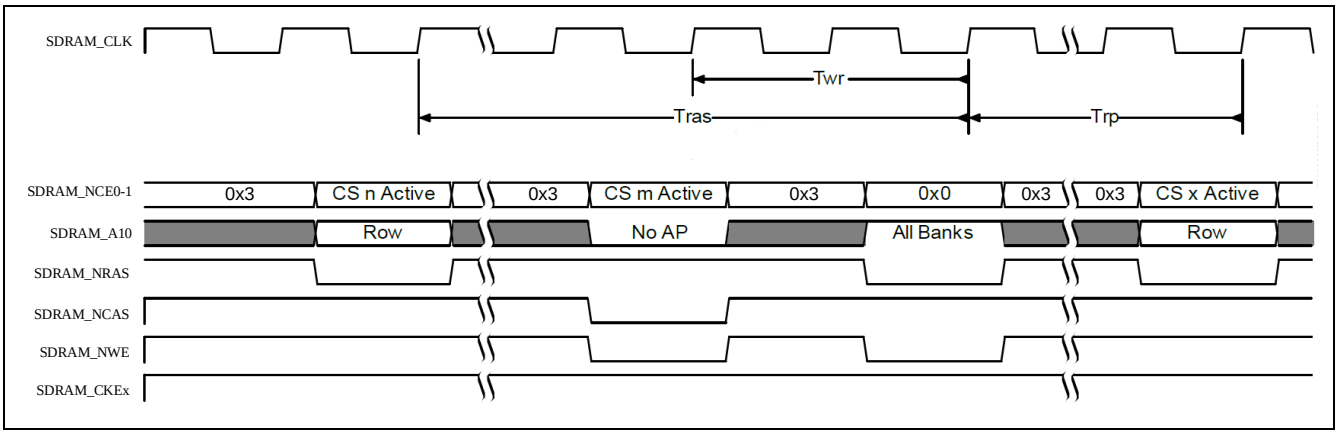
- Current Read or Write operation's address hits a closed row and some other row in the same bank is already open.

Description of the Error: Reference source not found timing parameters:

- **T_{ras} – Row Active Time** – After the row in a specific bank is activated, it must not be precharged (closed) until the **Minimum Row Active Time** expires. **Minimum Row Active Time** parameter is set in the Row Active Time Register.
- **T_{wr} – Write Recovery Time** – After the last data is written to the specified bank, it must not be pracharged until **Write Recovery Time** expires. This timing parameter is set in the Write Recovery Time Register.
- **T_{rp} – Precharge Time** – After the Precharge Command is issued to a specified bank, it must not be accessed (refreshed, activated or precharged) until **Precharge Time** expires. This parameter is set in the Precharge Time Register.

6.5.5.11 Precharge All Banks

Figure 6-13 Precharge All SDRAM Banks



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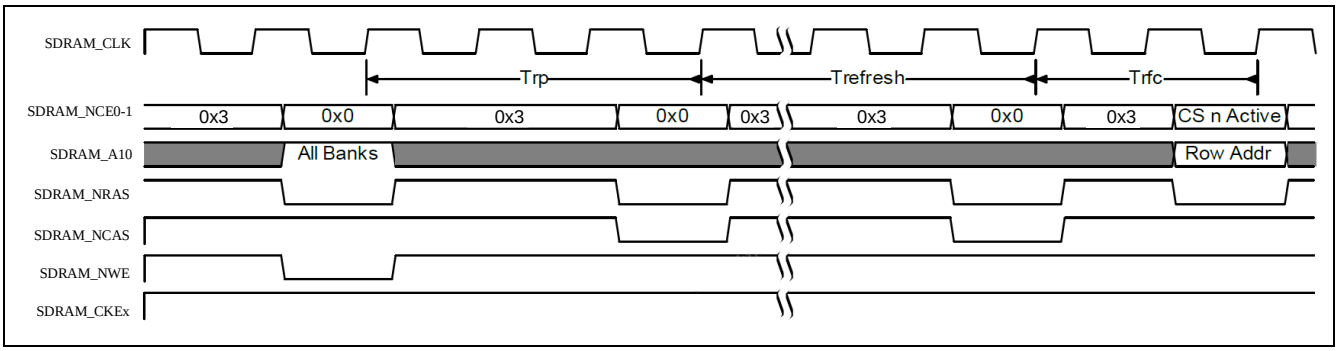
Precharge All SDRAM Banks in all devices is initiated when:

- Refresh Timer Expires and there is at least one open row in one of the connected devices.
- Precharge All Command is configured in the SDRAM Operation Setup Register and read or write access is issued to the SDRAM Operation Request Register.

The timing parameters in the Figure 6-13 are the same as in the Figure 6-12, except they must be met in every connected device, since all banks in all devices are precharged issuing this command.

6.5.5.12 Auto Refresh

Figure 6-14 Auto Refresh



SDRAM Auto Refresh command is initiated when:

- When Refresh Timer expires, all rows in all devices are inactive (were precharged) and T_{rp} is not violated.
- When Refresh Command is configured in the SDRAM Operation Setup Register and read or write access is issued to the SDRAM Operation Request Register.

Description of Error: Reference source not found timing parameters:

- **T_{rp} – Precharge Recovery Time** – See Precharge Selected Bank.
- **$T_{refresh}$ – Refresh Interval** – set in the Refresh Interval Register. Most of the SDRAM devices' datasheets provide information about the refresh period in ms.
- You must divide this value with the number of rows in a device and divide that with the memory clock period to obtain the value for this register. It is recommended to set the register to a few percent lower value, to allow some margin between two refresh cycles.
- **T_{rfc} – Refresh Cycle Time** – No commands can be issued to any of the SDRAM devices, until the **Refresh Cycle Time** is met. This timing parameter is set in the Refresh Cycle Time Register.

6.5.6 SDRAM device's suspend and wakeup sequences

6.5.6.1 Suspend sequence

Suspend sequence for synchronous dynamic devices is usually more complicated than suspend sequence for static devices. Every synchronous dynamic device's datasheet provides information on the special sequence used to suspend the device. In general, suspend sequence for synchronous dynamic devices should follow the following steps:

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1. The software must disable all synchronous dynamic device chip selects. It does that by writing a value of 0 to all **SDRAMEN** bits, part of SDRAM_CFGx Register. **Do not disable the SDRAM device while it is being accessed.**
2. Wait for at least 32 memory clock cycles to allow any read or write operations to finish on the memory bus.
3. When all dynamic device chip selects are disabled and after the appropriate delay, the software must perform a write operation to the SDRAM_CBO Register, to flush any write data present in the write buffers to the external memory.
4. After flush of the write buffers, the software must perform a read operation from the SDRAM_CBO Register, to invalidate all data present in the read buffers.
5. When all chip selects are disabled, write buffers flushed and read buffers invalidated, the software must write a value of 0 to all **REFRESHEN** bits, part of SDRAM_CFGx Register. Software must now wait long enough, to satisfy a few (5-10) times the **Refresh Cycle Time**, to allow any pending refresh cycles to finish.
6. The software issues appropriate sequence of commands to external SDRAM devices using the SDRAM_OS Register and SDRAM_OR Register. It should issue Precharge All command first, to make sure no rows are open when entering suspend mode. After issuing the Precharge All command, it must wait enough time, so that the **Precharge Time** will not be violated.
7. The software will have to issue the Refresh command to the connected SDRAM devices with **CKEN** value of 0 using the SDRAM_OS Register and SDRAM_OR Register, in order to make them enter Self Refresh Mode. If the device's datasheet specifies different or additional operations, they should be followed, to assure proper operation.

6.5.6.2 Wakeup sequence

Every synchronous dynamic device's datasheet specifies the proper wakeup sequence. The system software should follow that sequence which, in general, requires the following steps:

1. Devices can have a minimum self refresh time timing parameter specified. The core does not time this parameter, so the software must be sure not to start the wakeup procedure before this timing parameter is met.
2. The software must now follow any procedure specified in the device's datasheet, using the SDRAM_OS Register and SDRAM_OR Register. This procedure usually comprises of a few NOP operations followed by a few Auto Refresh Commands, all issued with the CKE value of 1. If the device does not require any special command sequence to exit the Self Refresh mode, you should issue at least one NOP command with **CKEN** value of 1 to enable the external memory clock. Then issue at least one Auto Refresh command to all connected devices with **CKEN** value of 1, since there is no way of knowing when the last internal refresh command executed.
3. The software can than enable synchronous dynamic device refresh operation as appropriate. This is done by writing a value of 1 to **REFRESHEN** bit located in the SDRAM_CFGx Register.
4. The software can enable synchronous chip selects as appropriate. This is done by writing a value of 1 to **SDRAMEN** bit located in the SDRAM_CFGx Register.

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6.5.7 Memory Data Buffering

The SDRAM controller has implemented read and write buffers in order to support faster accesses to external SDRAM devices.

6.5.7.1 Write Data Buffering

The data is stored in the write data buffer when there is a write access issued and:

- One of the implemented write buffers is empty or
- Address of the write cycle is within one of the implemented write buffer's address range or
- Data in at least one of the implemented write buffers was already stored to the external memory device.

The data from the internal write buffer is stored to the external memory device when there is a write access issued and:

- All implemented write buffers are non-empty and the address of the write transfer is not within any of the implemented write buffers' address ranges or
- At least one write buffer is not empty and has not been stored to the external memory device and address of the write transfer is not in its address range and currently accessed chip select has *Store On Miss (*SOMEN) bit set in its SDRAM Configuration Register. This means that valid write data from one buffer will be stored to the external memory device while the second buffer accepts the next write data simultaneously. This can increase speed of write transfers for some applications.
- There is a write to the Synchronous Memory Buffer Operations Register and at least one of the write buffers contains valid data not written to the external memory device yet.

Note that least recently accessed write buffer is always stored first.

6.5.7.2 Read Data Buffering

The read data is provided from the synchronous memory data buffers (read or write) when there is a read access requested and:

- All bytes requested are present in write or read buffers. Valid bytes present in one of the write buffers take precedence before the bytes stored in the read buffers.

The data is read from the external memory device and stored into the read buffer when there is a read access requested and:

- No or not all bytes requested on the read bus are present in write or read buffers or
- The current read burst type is increment type and the currently accessed chip select has *Prefetch Enable* (PREFCHRDEN) bit set in its SDRAM Configuration Register and the prefetch data is not present in any of the read buffers. This effectively means that while read data is provided from one buffer to the AHB read data bus, the second read buffer is filled from the external memories simultaneously. This can boost performance of read transfers in certain applications (like large DMA transfers).

Note that the least recently accessed read buffer is filled from the external memory first.

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6.5.8 Write protection

The SDRAM controller supports the write protection function. When the bit WP[n] of SDRAM Write Protection Register is set to 1, it doesn't allow any write access to SDRAM device. A write access to SDRAM device this time will cause an error response on AHB Memory access interface and the SDRAM memory is not updated.

This function can be enabled for each individual SDRAM device.

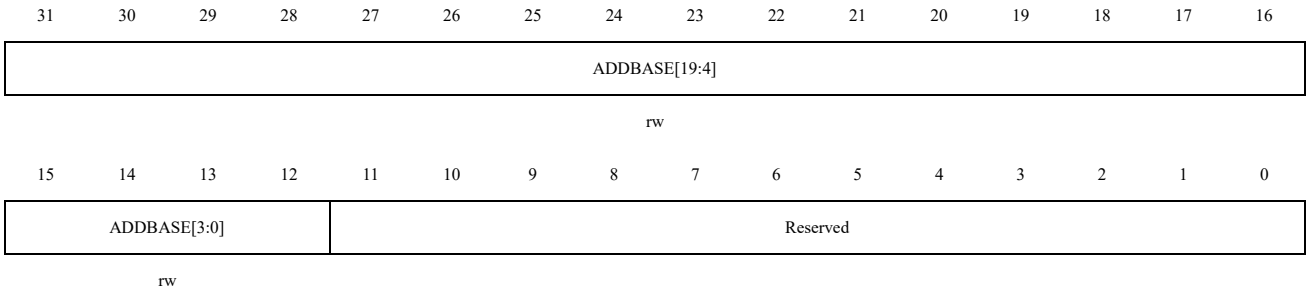
The read access is not impacted by this function.

6.6 Registers

6.6.1 SDRAM Base Address for SDRAM1 Register (SDRAM_BADD1)

Address offset: 0x0080

Reset value: 0x0000 0000

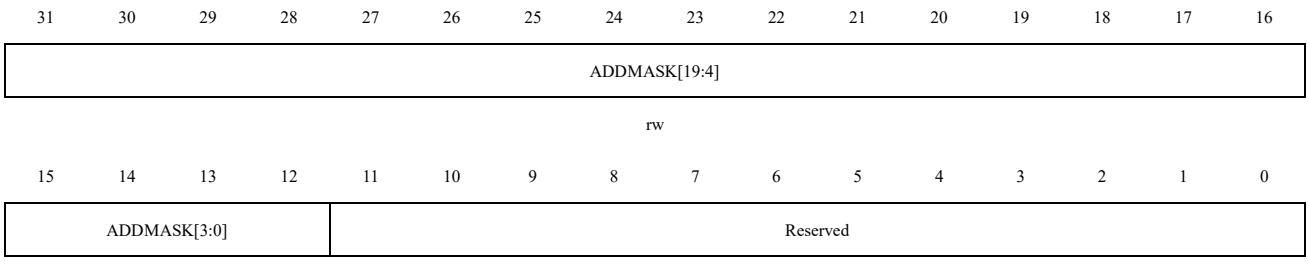


Bit field	Name	Description
31:12	ADDBASE[19:0]	Base address value for SDRAM1. It uses the values written to the pair of corresponding Base Address and Address Mask registers to decode the SDRAM1's address range.
11:0	Reserved	Reserved, the reset value must be maintained.

6.6.2 SDRAM Address Mask for SDRAM1 Register (SDRAM_ADDMASK1)

Address offset: 0x0084

Reset value: 0x0000 0000



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rw

Bit field	Name	Description
31:12	ADDMASK[19:0]	Address mask value for SDRAM1. It uses the values written to the pair of corresponding Base Address and Address Mask registers to decode the SDRAM1's address range.
11:0	Reserved	Reserved, the reset value must be maintained.

6.6.3 SDRAM Base Address for SDRAM2 Register (SDRAM_BADD2)

Address offset: 0x0088

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDBASE[19:4]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDBASE[3:0]				Reserved											
rw															

Bit field	Name	Description
31:12	ADDBASE[19:0]	Base address value for SDRAM2. It uses the values written to the pair of corresponding Base Address and Address Mask registers to decode the SDRAM2's address range.
11:0	Reserved	Reserved, the reset value must be maintained.

6.6.4 SDRAM Address Mask for SDRAM2 Register (SDRAM_ADDMASK2)

Address offset: 0x008C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDMASK[19:4]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDMASK[3:0]				Reserved											
rw															

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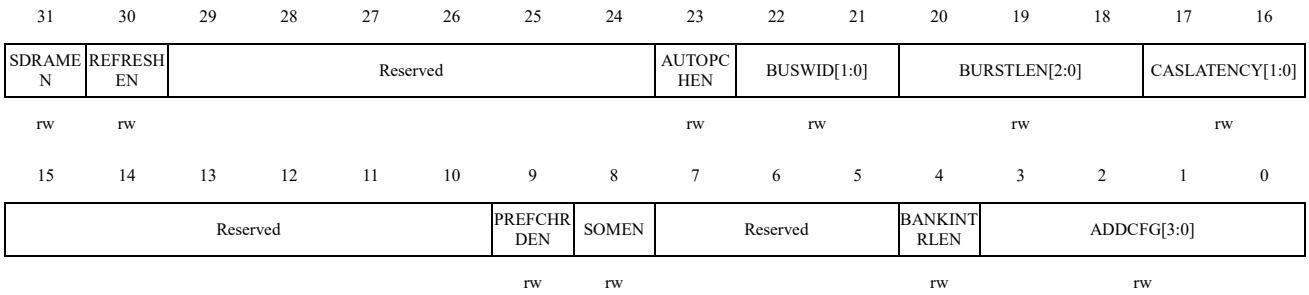
Bit field	Name	Description
31:12	ADDMASK[19:0]	Address mask value for SDRAM2. It uses the values written to the pair of corresponding Base Address and Address Mask registers to decode the SDRAM2's address range.
11:0	Reserved	Reserved, the reset value must be maintained.

6.6.5 SDRAM Configuration for SDRAM1 Register (SDRAM_CFG1)

Address offset: 0x00A0

Reset value: 0x0001 0000



Bit field	Name	Description
31	SDRAMEN	SDRAM1 enable. 0: SDRAM1 is disabled 1: SDRAM1 is enabled
30	REFRESHEN	Refresh commands enable. 0: Refresh is disabled 1: Refresh is enabled
29:24	Reserved	Reserved, the reset value must be maintained.
23	AUTOPCHEN	Auto Precharge enable. 0: Auto precharge is disabled 1: Auto precharge is enabled
22:21	BUSWID[1:0]	Bus width. 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved
20:18	BURSTLEN[2:0]	Burst length. 000: Burst length 1 001: Burst length 2 011: Burst length 4 111: Burst length 8 Other values are invalid
17:16	CASLATENCY[1:0]	CAS latency.

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Bit field	Name	Description
		These bits set the SDRAM1 CAS latency in number of memory clock cycles. 00: Reserved 01: 1 cycle 10: 2 cycles 11: 3 cycles
15:10	Reserved	Reserved, the reset value must be maintained.
9	PREFCHRDEN	Prefetch read enable. 0: Prefetch read is disabled 1: Prefetch read is enabled
8	SOMEN	Store On Miss(SOM) enable. 0: Write buffer store on miss is disabled 1: Write buffer store on miss is enabled
7:5	Reserved	Reserved, the reset value must be maintained.
4	BANKINTRLEN	Bank interleaving enable during SDRAM1 address generation. 0: Bank interleaving is disabled 1: Bank interleaving is enabled
3:0	ADDCFG[3:0]	Address configuration defines the organization of the SDRAM1. 0000: 4 Banks, 4096 Rows, 256 Columns 0001: 4 Banks, 4096 Rows, 512 Columns 0010: 4 Banks, 4096 Rows, 1024 Columns 0011: 4 Banks, 4096 Rows, 2048 Columns 0100: 4 Banks, 8192 Rows, 256 Columns 0101: 4 Banks, 8192 Rows, 512 Columns 0110: 4 Banks, 8192 Rows, 1024 Columns 0111: 4 Banks, 8192 Rows, 2048 Columns 1000: 4 Banks, 2048 Rows, 256 Columns 1001: 4 Banks, 2048 Rows, 512 Columns 1010: 4 Banks, 2048 Rows, 1024 Columns 1011: 4 Banks, 2048 Rows, 2048 Columns Other values: Reserved

6.6.6 SDRAM Configuration for SDRAM2 Register (SDRAM_CFG2)

Address offset: 0x00A4

Reset value: 0x0001 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SDRAMEN	REFRESHEN	Reserved						AUTOPCHEN	BUSWID[1:0]		BURSTLEN[2:0]			CASLATENCY[1:0]	
rw	rw							rw	rw		rw			rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PREFCHRDEN	SOMEN	Reserved			BANKINTRLEN	ADDCFG[3:0]			

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rw rw rw rw

Bit field	Name	Description
31	SDRAMEN	SDRAM2 enable. 0: SDRAM2 is disabled 1: SDRAM2 is enabled
30	REFRESHEN	Refresh commands enable. 0: Refresh is disabled 1: Refresh is enabled
29:24	Reserved	Reserved, the reset value must be maintained.
23	AUTOPCHEN	Auto Precharge enable. 0: Auto precharge is disabled 1: Auto precharge is enabled
22:21	BUSWID[1:0]	Bus width. 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved
20:18	BURSTLEN[2:0]	Burst length. 000: Burst length 1 001: Burst length 2 011: Burst length 4 111: Burst length 8 Other values are invalid
17:16	CASLATENCY[1:0]	CAS latency. These bits set the SDRAM2 CAS latency in number of memory clock cycles. 00: Reserved 01: 1 cycle 10: 2 cycles 11: 3 cycles
15:10	Reserved	Reserved, the reset value must be maintained.
9	PREFCHRDEN	Prefetch read enable. 0: Prefetch read is disabled 1: Prefetch read is enabled
8	SOMEN	Store On Miss(SOM) enable. 0: Write buffer store on miss is disabled 1: Write buffer store on miss is enabled
7:5	Reserved	Reserved, the reset value must be maintained.
4	BANKINTRLEN	Bank interleaving enable during SDRAM2 address generation. 0: Bank interleaving is disabled 1: Bank interleaving is enabled

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Bit field	Name	Description
3:0	ADDCFG[3:0]	Address configuration defines the organization of the SDRAM2. 0000: 4 Banks, 4096 Rows, 256 Columns 0001: 4 Banks, 4096 Rows, 512 Columns 0010: 4 Banks, 4096 Rows, 1024 Columns 0011: 4 Banks, 4096 Rows, 2048 Columns 0100: 4 Banks, 8192 Rows, 256 Columns 0101: 4 Banks, 8192 Rows, 512 Columns 0110: 4 Banks, 8192 Rows, 1024 Columns 0111: 4 Banks, 8192 Rows, 2048 Columns 1000: 4 Banks, 2048 Rows, 256 Columns 1001: 4 Banks, 2048 Rows, 512 Columns 1010: 4 Banks, 2048 Rows, 1024 Columns 1011: 4 Banks, 2048 Rows, 2048 Columns Other values: Reserved

6.6.7 SDRAM Row Active Time Register (SDRAM_RAT)

Address offset: 0x00B0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TRAS[5:0]					
										rw					

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	TRAS[5:0]	Row active time These bits define the minimum self refresh period in number of memory clock cycles. 000000: 1 cycle 000001: 2 cycles 000002: 3 cycles … … 111111: 64 cycles

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6.6.8 SDRAM Row Cycle Time Register (SDRAM_RCT)

Address offset: 0x00B4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TRC[5:0]					
										rw					

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	TRC[5:0]	Row cycle time These bits define the delay between the refresh command and the activate command, as well as the delay between two consecutive refresh commands. It is expressed in number of memory clock cycles. 000000: 1 cycle 000001: 2 cycles 000002: 3 cycles … … 111111: 64 cycles

6.6.9 SDRAM Row Active to Row Active Delay Register (SDRAM_RRDLY)

Address offset: 0x00B8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TRRD[5:0]					
										rw					

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.

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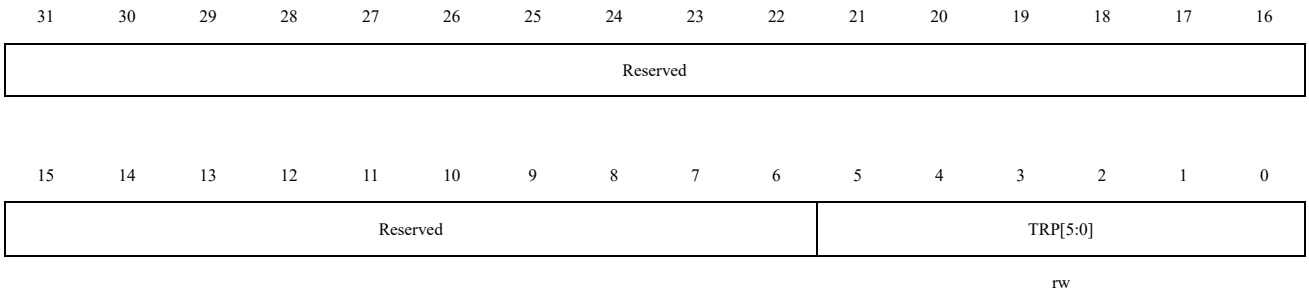
Bit field	Name	Description
5:0	TRRD[5:0]	Row active to row active delay time These bits define the minimum delay between two active commands to different banks on the same SDRAM chip. 000000: 1 cycle 000001: 2 cycles 000002: 3 cycles … … 111111: 64 cycles

6.6.10 SDRAM Precharge Time Register (SDRAM_PT)

Address offset: 0x00BC

Reset value: 0x0000 0000



Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	TRP[5:0]	Precharge time These bits define the delay between an internal or external precharge command and another command in number of memory clock cycles. 000000: 1 cycle 000001: 2 cycles 000002: 3 cycles … … 111111: 64 cycles

6.6.11 SDRAM Write Recovery Time Register (SDRAM_WRT)

Address offset: 0x00C0

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TWR[5:0]					
										rw					

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	TWR[5:0]	Write recovery time These bits define the delay between a write and an internal precharge command in number of memory clock cycles. 000000: 1 cycle 000001: 2 cycles 000002: 3 cycles … … 111111: 64 cycles

6.6.12 SDRAM Refresh Cycle Time Register (SDRAM_RFCT)

Address offset: 0x00C4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TRFC[5:0]					
										rw					

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	TRFC[5:0]	Refresh cycle time These bits define the delay between any two consecutive commands in number of memory clock cycles. 000000: 1 cycle 000001: 2 cycles

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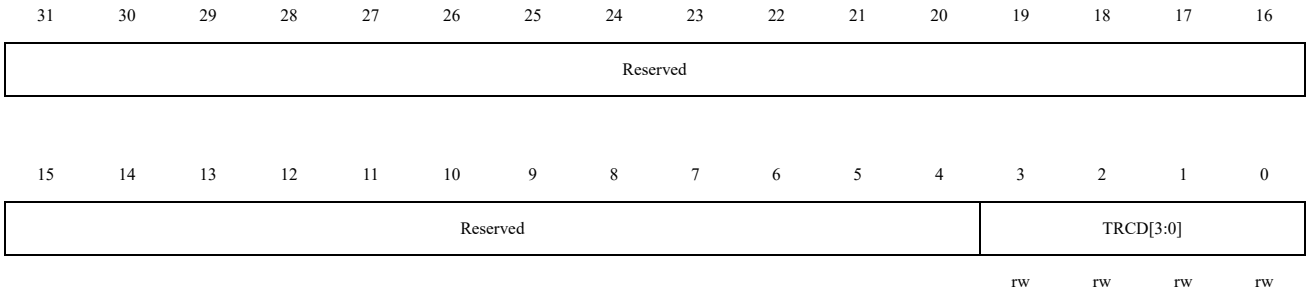
Bit field	Name	Description
		000002: 3 cycles … … 111111: 64 cycles

6.6.13 SDRAM RAS to CAS Delay Register (SDRAM_RCDLY)

Address offset: 0x00C8

Reset value: 0x0000 0000



Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	TRCD[3:0]	RAS to CAS delay time These bits define minimum delay between row active commands and read or write command to the same bank in the same SDRAM chip. 0000: 1 cycle 0001: 2 cycles 0002: 3 cycles … … 1111: 16 cycles

6.6.14 SDRAM Refresh Interval Register (SDRAM_RI)

Address offset: 0x00CC

Reset value: 0x0000 0000

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rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:0	TRI[23:0]	Refresh Interval Time These bits define delay between two auto refresh commands in number of memory clock cycles. 000000h: 1 cycle 000001h: 2 cycles 000002h: 3 cycles …… FFFFFFh: 16,777,216 cycles

6.6.15 SDRAM Controller Buffer Operation Register (SDRAM_CBO)

Address offset: 0x00E0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DUMMY[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMMY[15:0]															
rw															

Bit field	Name	Description
31:0	DUMMY[31:0]	Dummy data An access to this register starts an operation on controller buffer: Write: release all current data in controller's write buffer to external memory device Read: from this register: erase all current data in controller's read buffer. These bits are dummy, the data (any value) written to this register is discarded, and read returns all 0s.

6.6.16 SDRAM Operation Request Register (SDRAM_OR)

Address offset: 0x00E4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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DUMMY[31:16]
rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMMY[15:0]															
rw															

Bit field	Name	Description
31:0	DUMMY[31:0]	Dummy data An access (write or read) to this register starts to send the command, which is set up in SDRAM_OS, to external memory bus. These bits are dummy, the data (any value) written to this register is discarded, and read returns all 0s.

6.6.17 SDRAM Operation Setup Register (SDRAM_OS)

Address offset: 0x00E8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	CKEN	OPCODE[1:0]		Reserved		CS[1:0]		Reserved						BANKADD[1:0]	
	rw	rw				rw								rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		ADD[13:0]													
		rw													

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	CKEN	Clock enable This bit defines whether the clock will be enable or not while issuing the command. After current command is executed, the clock retains its status until the next command is issued. 0: clock is disable 1: clock is enable
29:28	OPCODE[1:0]	Operation Code. These bits define the command types: 00: No Operation 01: Precharge SDRAM1 and SDRAM2 external memory bank

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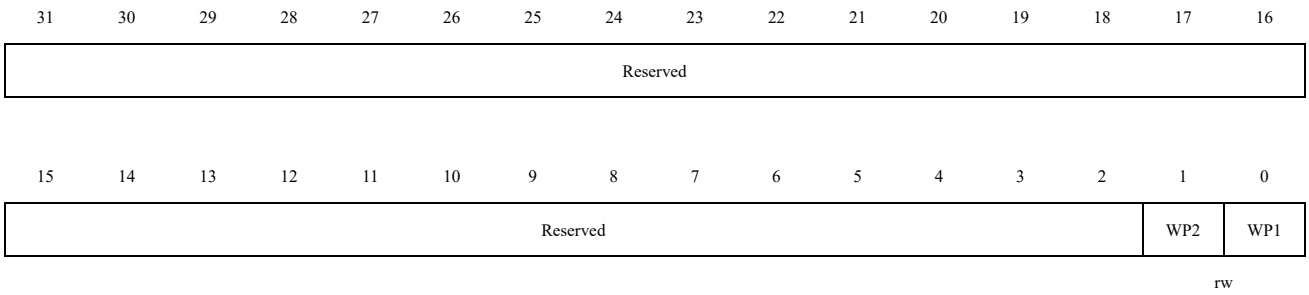
Bit field	Name	Description
		10: Auto Refresh (CKEN=1) or Self Refresh (CKEN=0) 11: Load Mode Register
27:26	Reserved	Reserved, the reset value must be maintained.
25:24	CS[1:0]	Chip Select. These bits define the selection of SDRAM1, SDRAM2 or both 00: SDRAM1 and SDRAM2 are selected 01: SDRAM1 is de-selected, SDRAM2 is selected 10: SDRAM1 is selected, SDRAM2 is de-selected 11: SDRAM1 and SDRAM2 are de-selected
23:18	Reserved	Reserved, the reset value must be maintained.
17:16	BANKADD[1:0]	Bank Address These bits define the bank address issued to external memory bus. 00: Bank 1 01: Bank 2 10: Bank 3 11: Bank 4
15:14	Reserved	Reserved, the reset value must be maintained.
13:0	ADD[13:0]	Address These bits define the address (mux of column and row address) issued to external memory bus.

6.6.18 SDRAM Write Protection Register (SDRAM_WP)

Address offset: 0x0100

Reset value: 0x0000 0000



Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	WP2	SRAM2 Write protection These bits enable write mode access to the SDRAM chip. 0: write accesses allowed of SDRAM2 1: write accesses ignored of SDRAM2
0	WP1	SRAM1 Write protection

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Bit field	Name	Description
		These bits enable write mode access to the SDRAM chip. 0: write accesses allowed of SDRAM1 1: write accesses ignored of SDRAM1

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7 SEMA4

7.1 Introduction

The hardware semaphore block provides 32 (32-bit) register based semaphores.The semaphores can be used to ensure synchronization between different processes running between different cores. The SEMA4 provides a non-blocking mechanism to lock semaphores in an atomic way. The following functions are provided:

• Locking a semaphore can be done in two ways:

– 2-step lock: by writing COREID and PROCID to the semaphore, followed by a read check

– 1-step lock: by reading the COREID from the semaphore

• Interrupt generation when a semaphore is freed

– Each semaphore may generate an interrupt on one of the interrupt lines

• Semaphore clear protection

– A semaphore is only cleared when COREID and PROCID match

• Global semaphore clear per COREID

7.2 Main Features

The main features supported by SEMA4 are shown below:

• 32 (32-bit) semaphores

• 8-bit PROCID

• 4-bit COREID

• 2 interrupt lines

• Lock indication

7.3 Block Diagram

As illustrated in Figure 7-1, The SEMA4 is divided into three sub-blocks:

- The semaphore block, which holds the semaphore status and IDs.
- The semaphore interface block, which provides AHB access to the semaphores through the SEMA4_Rx and SEMA4_RLRx registers.
- The interrupt interface block, which controls interrupts using the SEMA4_CnISR, SEMA4_CnIER, SEMA4_CnMISR, and SEMA4_CnICR registers.

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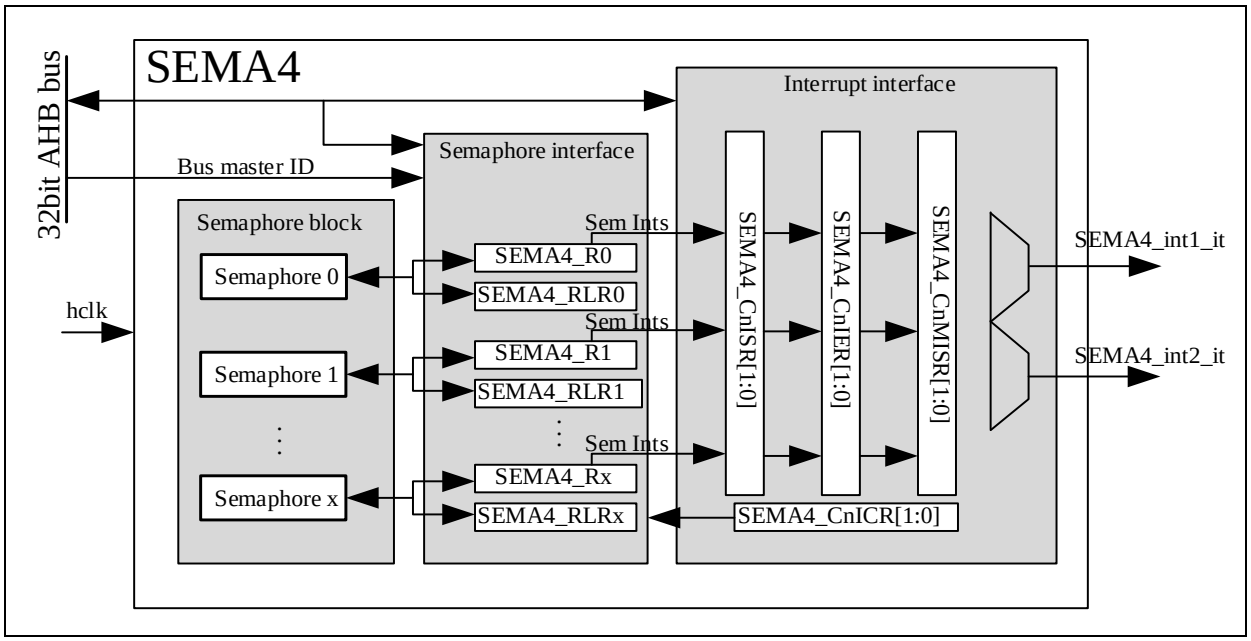
Figure 7-1 SEMA4 top level block diagram



7.4 1.4 Function Description

In the SEMA4 top-level block diagram shown in Figure 1 1, the AHB bus master can lock semaphore X using either the two-step (write) lock or the one-step (read) lock method. Once the process is complete, a locked semaphore can be cleared through a protected procedure, and all locked semaphores can be cleared at once. An interrupt may be generated for any semaphore that is released. SEMA4 restricts the locking and unlocking of semaphores to authorized AHB bus master IDs only.

7.4.1 SEMA4 lock procedures

There are two lock procedures:

- 2-step (write) lock
- 1-step (read) lock

When the LOCK bit is 0, the semaphore is considered free, with both the COREID and PROCID set to 0. When the LOCK bit is set to 1, the semaphore is locked, with the COREID representing the AHB bus master responsible for the lock, and the PROCID identifying the specific process within that AHB bus master.

For write locking, the COREID is derived from the master ID, while the PROCID is taken from the write data. In read locking, the COREID is sourced from the AHB bus master ID, and the PROCID is set to zero.

The 1-step (read) lock does not use the PROCID, while the 2-step (write) lock involves the COREID from the AHB bus master ID and the PROCID, which is managed by the software of that AHB bus master. Each process under a given AHB bus master must have a unique PROCID, and PROCID is only relevant in the 2-step lock process.

Both the 1-step and 2-step lock procedures can be used concurrently.

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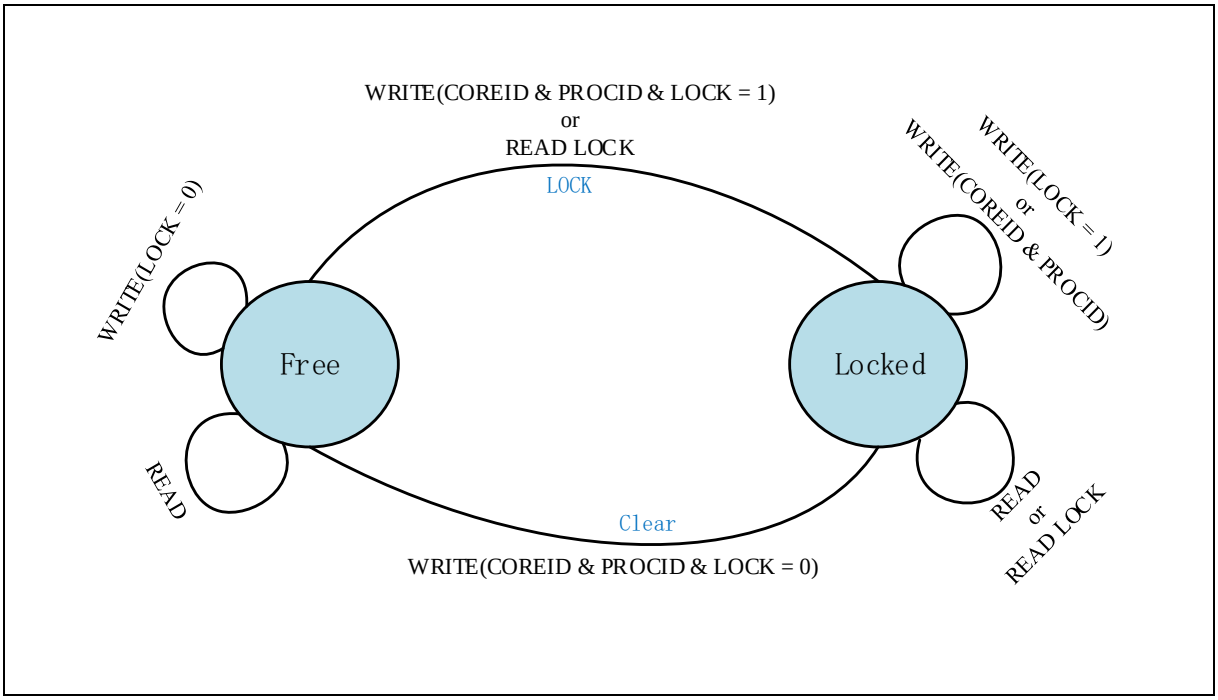
Figure 7-2 AHB single read write timing protocol



7.4.1.1 2-step (write) lock procedure

The 2-step lock procedure involves a write operation to lock the semaphore, followed by a read operation to verify the lock's success via the SEMA4_Rx register.

- Write operation: The semaphore is written with the PROCID and COREID, and the LOCK bit is set to 1. The lock is established if the semaphore is free at the time of writing.
- Read-back operation: The software reads the semaphore to check the lock status. If the PROCID and COREID match, the lock is confirmed.
- If the values do not match, a retry is needed, as another AHB bus master or process may have already locked the semaphore.

Semaphores can only be locked when they are free, and locking is permitted when PROCID is 0. Any subsequent write attempts with LOCK set to 1 on an already locked semaphore will be ignored.

7.4.1.2 1-step (read) lock procedure

The 1-step procedure involves a single read operation to both lock and verify the semaphore directly from the SEMA4_RLRx register.

- Read Lock: Lock the semaphore using the COREID.
- If the read COREID matches and PROCID is 0, the lock is successfully established. If the COREID matches but PROCID is not 0, it indicates that another process from the same COREID has locked the semaphore using the 2-step (write) procedure.
- If the COREID does not match, retry is needed as the semaphore might be locked by another AHB bus master or process.

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A semaphore can only be locked when it is free. When performing a read lock on a free semaphore, the PROCID is set to 0. If the semaphore is already locked, the read operation will return the COREID and PROCID of the entity that currently holds or previously held the lock. Every read lock operation, including the initial one that secures the semaphore, will reveal the COREID of the entity managing the semaphore.

If multiple processes from the same AHB bus master use the 1-step procedure, they will all observe the same semaphore status. However, if only one process locks the semaphore, each process from that AHB bus master will perceive the semaphore as being locked by itself, showing the associated COREID.

7.4.2 SEMA4 clear procedures

7.4.2.1 Clear through SEMA4_Rx registers

Clearing a semaphore is a protected process designed to prevent accidental clearing by unauthorized AHB bus masters or processes without the proper semaphore lock privilege. To clear a semaphore, write to it with the correct COREID and PROCID, and set the LOCK bit to 0. After successful clearing, the semaphore's LOCK, COREID, and PROCID values are all reset to 0.

Following the clearance, an interrupt may be triggered to signal the event, provided the semaphore interrupt feature is enabled.

The clearing process involves writing to the SEMA4_Rx registers for the semaphore:

- Write operation: Set the semaphore with the PROCID and COREID, and set LOCK to 0.
- If the PROCID and COREID match, the semaphore is released, and an interrupt may be triggered if the interrupt feature is enabled.
- If the PROCID and COREID do not match, the write operation is ignored, the semaphore remains locked, and no interrupt is generated (indicating that the semaphore is locked by another AHB bus master or process).

When multiple processes from the same AHB bus master use the 1-step lock procedure (PROCID = 0), clearing the semaphore will also affect all processes from that AHB bus master that are using the same semaphore.

7.4.2.2 Clear through SEMA4_CLR register.

All semaphores locked by an AHB bus master can be cleared simultaneously using the SEMA4_CLR register. The procedure for clearing all semaphores locked by an AHB bus master is as follows:

- Write operation: Enter the COREID and the correct KEY value. This action clears (frees) all semaphores locked by the matching COREID, and may generate an interrupt if the interrupt feature is enabled.

This procedure can be used to address issues with a malfunctioning AHB bus master. In such cases, another AHB bus master can clear the locked semaphores by writing the malfunctioning COREID into the SEMA4_CLR register with the correct KEY value, thereby releasing all semaphores with the matching COREID.

An interrupt may be triggered for the semaphores that are released. To enable this functionality, the semaphore interrupt must be activated in the SEMA4_CnIER registers.

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7.4.3 SEMA4 interrupts

There are two interrupt lines, SEMA4_int1_it (for interrupt 1) and SEMA4_int2_it (for interrupt 2), which allow each semaphore to generate an interrupt. Each of these interrupt lines offers the following features:

- Interrupt enable per semaphore
- Interrupt clear per semaphore
- Interrupt status per semaphore
- Masked interrupt status per semaphore

The interrupt clear (SEMA4_CnICR) clears both the interrupt status and the masked interrupt status for the associated semaphore on the interrupt line.

The interrupt status (SEMA4_CnISR) reflects the semaphore interrupt status on the interrupt line before it is enabled.

The masked interrupt status (SEMA4_CnMISR) shows the semaphore interrupt status for only the enabled semaphore interrupts on the interrupt line. To clear the interrupt line, all masked interrupt statuses for the enabled semaphores must be cleared.

The procedure for generating an interrupt when a semaphore becomes free is described as Figure 7-3.

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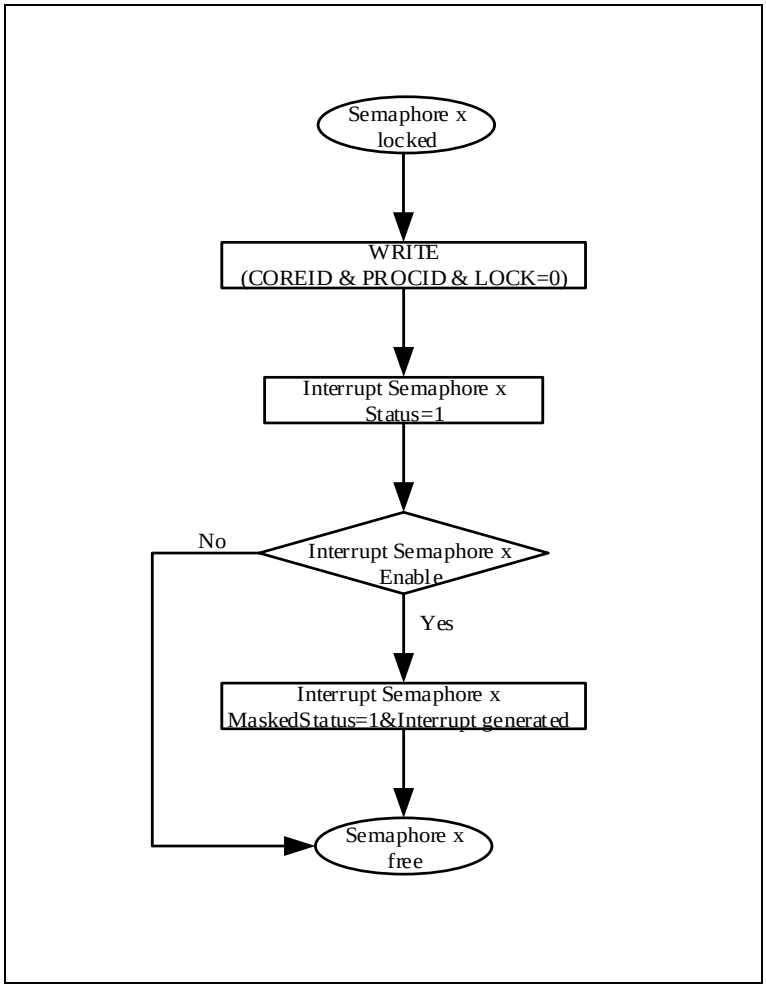
Figure 7-3 The procedure to get an interrupt when a semaphore becomes free



7.4.3.1 Attempt to lock the semaphore x

If the semaphore lock is successful, no interrupt is required.

If the semaphore lock fails:

Clear any pending interrupt status for semaphore x on the interrupt line SEMA4_intn_it using the SEMA4_CnICR register.

Retry locking semaphore x:

- If the lock is successful on retry, no interrupt is needed (this indicates that the semaphore was freed between the initial attempt and the clearing of the semaphore interrupt status).
- If the lock is still unsuccessful, enable the semaphore x interrupt for the interrupt line SEMA4_intn_it using the SEMA4_CnIER register.

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7.4.3.2 Upon receiving the semaphore x free interrupt, attempt to lock semaphore

- If the semaphore lock is successfully obtained:

Disable the semaphore x interrupt for the interrupt line SEMA4_intn_it using the SEMA4_CnIER register.

Clear any pending interrupt status for semaphore x on the interrupt line SEMA4_intn_it using the SEMA4_CnICR register.

- If the semaphore x lock fails:

Clear any pending interrupt status for semaphore x on the interrupt line SEMA4_intn_it using the SEMA4_CnICR register.

Retry locking semaphore x:

- If the lock is successfully obtained (indicating that the semaphore was freed between the initial attempt and the clearing of the interrupt status), disable the semaphore x interrupt for the interrupt line SEMA4_intn_it using the SEMA4_CnIER register.
- If the lock is still unsuccessful, wait for the semaphore free interrupt.

Note: An interrupt alone does not lock the semaphore. After an interrupt, either the AHB bus master or the process must execute the lock procedure to secure the semaphore. Multiple AHB bus masters can be alerted by the semaphore free interrupts. Each AHB bus master receives its interrupt, and the first one to respond will lock the semaphore.

7.4.4 AHB bus master ID verification

The SEMA4 system allows only authorized AHB bus master IDs to lock and unlock semaphores:

- For the 2-step lock procedure, during the AHB bus master's write access to the semaphore via the SEMA4_Rx register, validation is conducted against valid bus master IDs.
  - Attempts from unauthorized AHB bus master IDs are rejected, and the semaphore will not be locked.

- For the 1-step lock procedure, during the AHB bus master's read access from the SEMA4_RLRx register, validation is performed against authorized bus master IDs.
  - If an unauthorized AHB bus master ID reads from SEMA4_RLRx, the read data will vary based on the semaphore status:
    - If the semaphore is free, the read data will be all 0s.
    - If the semaphore was previously locked, the read data will reflect the SEMA4_RLRx data.
- For clearing a semaphore, write access to the SEMA4_CLR register is validated against valid bus master IDs. Only authorized bus master IDs can write to the SEMA4_CLR register to clear COREID semaphores.

Attempts from unauthorized AHB bus master IDs are discarded and will not clear the COREID semaphore.

Details on the relationship between bus master/CPU and COREID are provided in Table 7-1

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Table 7-1 Authorized AHB bus master IDs

Bus master 0(CPU1)	Bus master 1(CPU2)
COREID = 3	COREID = 1

Note: Accesses from unauthorized AHB bus master IDs to other registers are granted.

7.4.5 Design implementation Details

7.4.5.1 Lock procedure

When an AHB bus master intends to lock a semaphore, the procedure is as follows:

Using the 2-step method:

(1) Read the SEMA4_Rx register: If SEMA4_Rx[31] = 1'b1, it indicates that the semaphore is currently locked, and the 2-step operation will be ignored. If SEMA4_Rx[31] = 1'b0, the semaphore is free.

(2) If the semaphore is locked (SEMA4_Rx[31] = 1'b1): Wait until the semaphore becomes free (check if SEMA4_Rx[31] = 1'b0), then retry by writing to SEMA4_Rx with the PROCID, COREID, and LOCK = 1.

(3) Write to SEMA4_Rx: Set the PROCID, COREID, and LOCK = 1. Read back the SEMA4_Rx register. If the PROCID and COREID match, the lock is confirmed.

Using the 1-step method:

(1) Read the SEMA4_RLRx register: If the read COREID matches and PROCID is not 0, it indicates that the semaphore is locked by another process from the same COREID using the 2-step procedure (since a 1-step lock would have PROCID set to 0). If the read COREID matches and PROCID is 0, the lock is successfully established.

The COREID is derived from the AHB bus master ID, while the PROCID is assigned by the software of that specific AHB bus master. Each process within an AHB bus master must have a unique PROCID. PROCID is used exclusively in the 2-step lock procedure.

7.4.5.2 Clear procedure

The first clearing procedure involves writing to the SEMA4_Rx registers:

Write to the semaphore: Set the PROCID and COREID, and set LOCK to 0.

If the PROCID and COREID match: The semaphore is freed, and an interrupt may be generated if enabled by configuring the SEMA4_CnICR register.

The second clearing procedure allows for clearing all locked semaphores simultaneously using the SEMA4_CLR register:

Write to the SEMA4_CLR register: Enter the COREID and the correct KEY value. This action clears (frees) all semaphores with a matching COREID, and an interrupt may be triggered.

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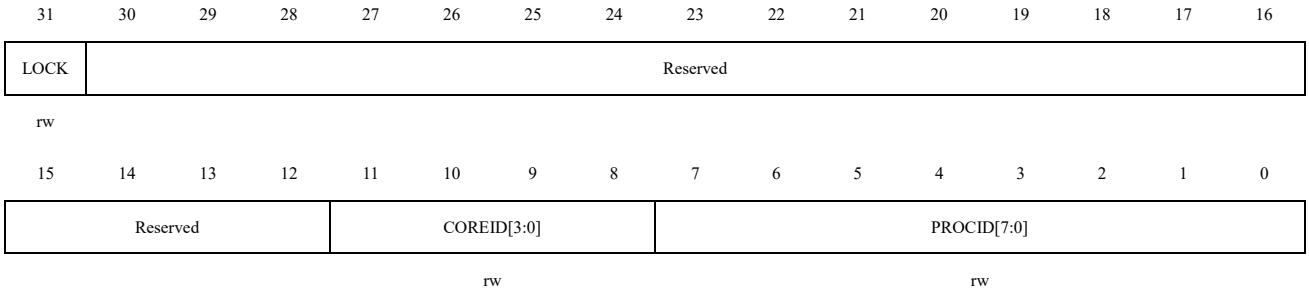
7.5 Registers

7.5.1 SEMA4 Register Semaphore x(x = 0 to 31) (SEMA4_Rx)

Address offset: 0x000 + 0x4 * x

Reset value: 0x0000 0000



Bit field	Name	Description
31	LOCK	Lock indication. This bit can be written and read by software. 0: On write free semaphore (only when COREID and PROCID match), on read semaphore is free. 1: On write try to lock semaphore, on read semaphore is locked.
30:12	Reserved	Reserved, the reset value must be maintained.
11:8	COREID[3:0]	Semaphore COREID. Written by software, when the semaphore is free and the LOCK bit is at the same time written to 1, the COREID is written only when the bus ID of the AHB bus master writing the semaphore matches. When the semaphore is cleared (LOCK bit written to 0 and AHB bus master ID matched COREID), the COREID is cleared to 0. When the semaphore is cleared (LOCK bit written to 0 and AHB bus master ID does not match COREID), the COREID is not be affected. Write when LOCK bit is already 1 (semaphore locked), the COREID is not affected. A read returns the stored COREID value.
7:0	PROCID[7:0]	Semaphore PROCID. Written by software, when the semaphore is free and the lock bit is written to 1, the PROCID is set to the written data. When the semaphore is cleared, (LOCK bit written to 0), the PROCID is cleared to 0. Write when LOCK bit is already 1 (semaphore locked), the PROCID is not affected. A read returns the programmed PROCID value.

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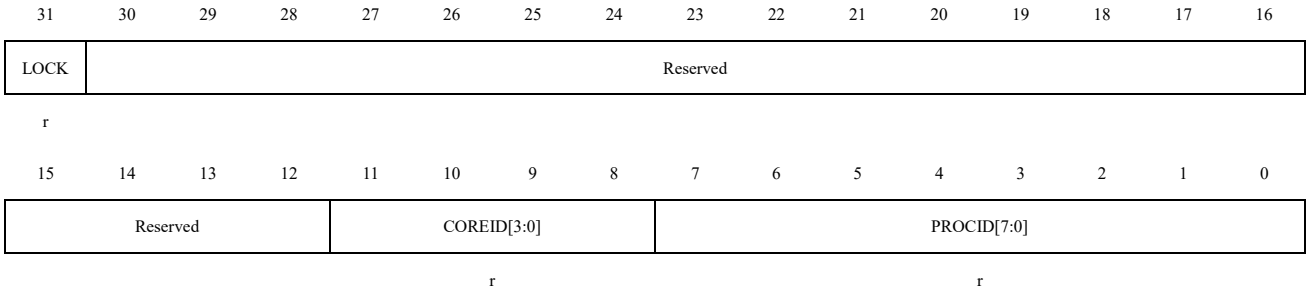
7.5.2 SEMA4 Read Lock Register Semaphore x(x = 0 to 31) (SEMA4_RLx)

Address offset: 0x080 + 0x004 * x

Reset value: 0x0000 0000



Bit field	Name	Description
31	LOCK	Lock indication This bit is read only by software at this address. A read with a valid bus master ID always returns 1. When the semaphore is free and the software performs a read, the hardware sets the semaphore to locked. When the semaphore is locked and the software performs a read, the LOCK bit is not effected. 0: Semaphore free 1: Semaphore locked
30:12	Reserved	Reserved, the reset value must be maintained.
11:8	COREID[3:0]	Semaphore COREID. This field is read only by software at this address. On a read, when the semaphore is free, the hardware sets the COREID to the AHB bus master ID reading the semaphore. The COREID of the AHB bus master locking the semaphore, is read. On a read when the semaphore is locked, this field returns the COREID of the AHB bus master that has locked the semaphore.
7:0	PROCID[7:0]	Semaphore PROCID This field is read only by software at this address. On a read when the semaphore is free, this filed returns 0. On a read when the semaphore is locked, this field returns the processor ID of the process that locked the semaphore.

7.5.3 SEMA4 Interrupt Enable Register (n=1 to 2) (SEMA4_CnIEN)

Address offset: 0x100 + 0x010 * (n-1)

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ISE[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISE[15:0]															
rw															

Bit field	Name	Description
31:0	ISE[31:0]	Freed Interrupt semaphore x enable bit This bit is read and written by software. 0: Freed Interrupt generation for semaphore x disabled (masked) 1: Freed Interrupt generation for semaphore x enabled (not masked)

7.5.4 SEMA4 Interrupt Clear Register (SEMA4_CnICLR) (n=1 to 2)

Address offset: 0x104 + 0x010 * (n-1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ISC[31:16]															
rc_w1															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISC[15:0]															
rc_w1															

Bit field	Name	Description
31:0	ISC[31:0]	Interrupt semaphore x clear bit This bit is read and written by software, and is always read 0. 0: Interrupt semaphore x status and masked status not affected 1: Interrupt semaphore x status and masked status cleared

7.5.5 SEMA4 Interrupt Status Register (SEMA4_CnISTS) (n=1 to 2)

Address offset: 0x108 + 0x010 * (n-1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ISF[31:16]															
r															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISF[15:0]															
r															

Bit field	Name	Description
31:0	ISF[31:0]	Freed Interrupt semaphore x status bit before enable (mask) This bit is set by hardware, and reset only by software. This bit is cleared by software writing the corresponding SEMA4_CnICR bit. 0: Freed Interrupt semaphore x status, no Freed interrupt pending 1: Freed Interrupt semaphore x status, Freed interrupt pending

7.5.6 SEMA4 Mask Interrupt Status Register (SEMA4_CnMISTS) (n=1 to 2)

Address offset: 0x10C + 0x010 * (n-1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MISF[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISF[15:0]															

Bit field	Name	Description
31:0	MISF[31:0]	Masked Freed interrupt semaphore x status bit after enable (mask) This bit is set by hardware and read only by software. This bit is cleared by software writing the corresponding SEMA4_CnICR bit. 0: Freed Interrupt semaphore x status after masking not pending 1: Freed Interrupt semaphore x status after masking pending

7.5.7 SEMA4 LockFail Interrupt Status Register (SEMA4_CnILFSTS) (n=1 to 2)

Address offset: 0x120 + 0x004 * (n-1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ISF[31:16]															
r															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISF[15:0]															
r															

Bit field	Name	Description
31:0	ISF[31:0]	LockFail Interrupt semaphore x status bit before enable (mask) This bit is set by hardware, and reset only by software. This bit is cleared by software writing the corresponding SEMA4_CnICR bit. 0: LockFail Interrupt semaphore x status, no lock fail interrupt pending 1: LockFail Interrupt semaphore x status, lock fail interrupt pending

7.5.8 SEMA4 LockFail Interrupt Enable Register (SEMA4_CnLFIEN) (n=1 to 2)

Address offset: 0x130 + 0x010 * (n-1)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ISE[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISE[15:0]															
rw															

Bit field	Name	Description
31:0	ISE[31:0]	LockFail Interrupt semaphore x enable bit This bit is read and written by software. 0: LockFail Interrupt generation for semaphore x disabled (masked) 1: LockFail Interrupt generation for semaphore x enabled (not masked)

7.5.9 SEMA4 Clear Register (SEMA4_CLR)

Address offset: 0x140

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[31:16]															
w															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	COREID[3:0]	Reserved

w

Bit field	Name	Description
31:16	KEY[15:0]	Semaphore clear key This field can be written by software and is always read 0. If this key value does not match SEMA4_KEYR.KEY, semaphores are not effected. If this key value matches SEMA4_KEYR.KEY, all semaphores matching the COREID are cleared to the free state.
15:12	Reserved	Reserved, the reset value must be maintained.
11:8	COREID[3:0]	COREID of semaphores to be cleared This field can be written by software and is always read 0. This field indicates the COREID for which the semaphores are cleared when writing the SEMA4_CLR.
7:0	Reserved	Reserved, the reset value must be maintained.

7.5.10 SEMA4 Interrupt Clear Register (SEMA4_KEYCLR)

Address offset: 0x144

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:16	KEY[15:0]	Semaphore clear key This field can be written and read by software. Key value to match when clearing semaphores.
15:0	Reserved	Reserved, the reset value must be maintained.

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8 Dual Core Messaging Unit (DCMU)

8.1 Introduction

The Dual Core Messaging Unit (DCMU) module facilitates communication and coordination between two processors within the SoC by exchanging messages (such as data, status, and control) through the DCMU interface. Additionally, the DCMU allows one processor to notify the other processor using interrupts.

Because the DCMU manages the messaging between processors, it operates with distinct clocks from each side of the various peripheral buses. As a result, the DCMU must synchronize accesses from one side to the other. This synchronization is achieved by using two sets of corresponding registers: one set facing Processor A and the other facing Processor B.

8.2 Main Features

The DCMU includes the following features:

- Messaging control through interrupts or polling mechanisms
- Symmetrical processor interfaces with each side offering support for:
  - Four general-purpose interrupt requests that are reflected to the opposite side
  - Three general-purpose flags reflected to the opposite side
  - Four receive registers with maskable interrupt capability
  - Four transmit registers with maskable interrupt capability
- The mentioned interrupts can also serve to wake up the other processor from low-power modes.

The Major Features of the DCMU described as Table 8-1 :

Table 8-1 Main Features of the DCMU

Major Feature	Description
Inter processor Interrupts	▪ The DCMU has 12 interrupt sources on each side (Processor A Side and Processor B Side) that are used for signaling the other processor. The interrupts can be used for notification of RX/TX events and general-purpose signaling between the processors.
DCMU Reset	▪ Processor A can issue a reset to the entire DCMU by setting a control bit (MURST) in the Processor A Control Register (DCMU_CTRL). ▪ The MURST bit is a self-clearing bit automatically clears itself after the reset operation.
Status and Control Communications between Core Complexes	▪ The DCMU facilitates communication between the two core complexes through the status and control registers located on both the Processor B and Processor A side of the DCMU. ▪ The status register of one DCMU side reflects the status of the other DCMU side. ▪ The control register is used for control operations, including enabling an interrupt and sending an interrupt to the opposite processor.

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Synchronized Message Transfers between Core Complexes	▪ Data messages are transferred between core complexes using transmit empty and receive full flags available on both sides of the DCMU. ▪ The synchronization of these transmit and receive flags is achieved through a specific mechanism. There exists inherent latency between updating the flag on one side and reflecting its status on the other side. For further information on latency, refer to the section on Event Update Timing.
Accessing Shared Memory Directly and Avoiding Collisions	▪ To transmit data or messages from one side of the DCMU to the other, the DCMU offers 4 transmit registers and 4 receive registers on each side of the DCMU ▪ Processor A or Processor B can directly access the shared memory resources of the SoC. However, to prevent simultaneous access to shared memory by both core complexes, the DCMU offers a method, utilizing interrupts and transmit-receive registers for both processors. For further details, refer to the Messaging Examples section.
Support for Different Clocks in the Two Core Complexes	▪ At the core of the DCMU module lies the event control mechanism, responsible for synchronizing the access of one DCMU side to the other DCMU side, as these two sides of the DCMU can operate using different clocks. ▪ Formulated event update latency.
Memory-Mapped Registers	▪ The DCMU is connected as a peripheral under the Peripheral bus on both sides. On the Processor A Side , it is connected to the Processor A Peripheral Bus, and on the Processor B side, it is connected to the Processor B Peripheral Bus.

8.3 Functional Description

8.3.1 Block Diagram

The DCMU provides 32-bit status and control registers to both the Processor A and Processor B sides for control functions such as interrupts and resets, as well as for monitoring the status of the opposite side.

For messaging, the DCMU features four 32-bit write-only transmit registers and four 32-bit read-only receive registers on each side. These registers are used to send messages between the processors. Additionally, these messages can be managed using three general-purpose flags included in the control and status registers on either side of the DCMU.

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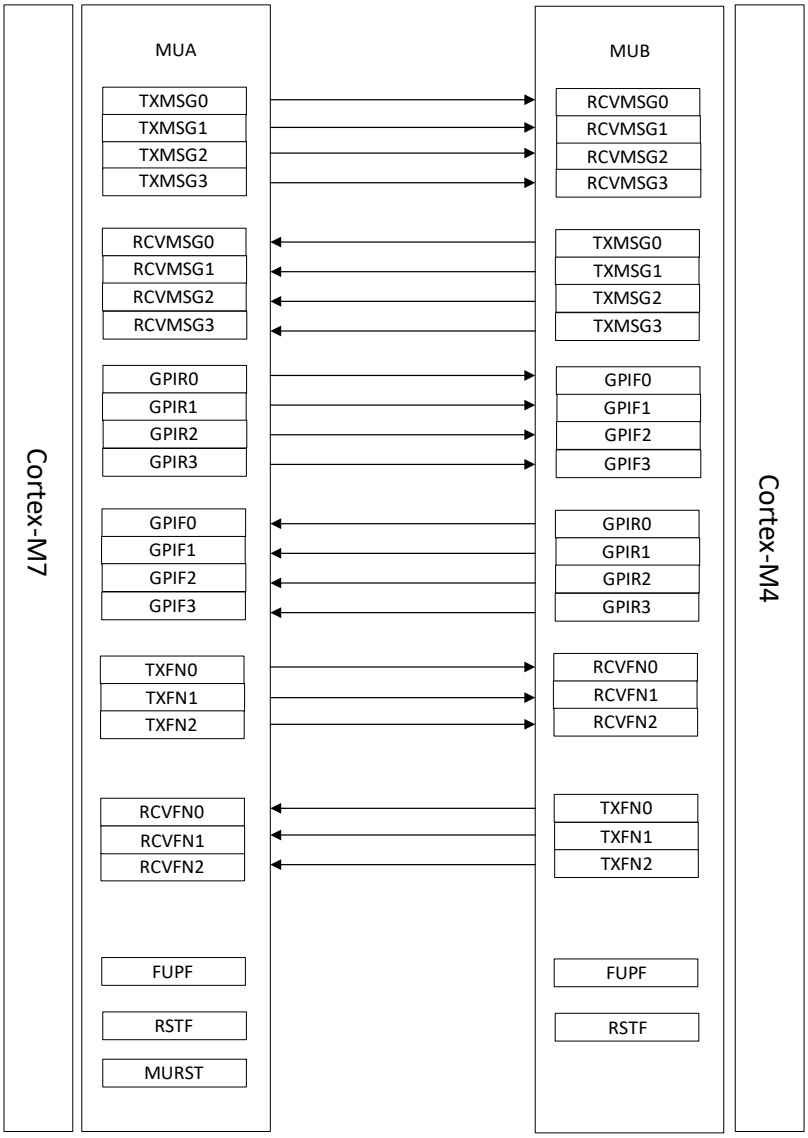
Figure 8-1 DCMU Block Diagram



8.3.2 Messaging Examples

The DCMU module consists of MUA and MUB, each with its own set of registers to control interrupts and transmit data.

Based on message classification, the DCMU features the following transmission processes.

- Passing short messages

The transmit registers can be used to send short messages ranging from one to four words in length. For example, when transmitting a four-word message, only one of the registers needs its corresponding interrupt enable bit set on the receiver's end. The first three words are written to registers with interrupts masked, while the fourth word is written to another register, triggering an interrupt on the receiver's side.

- Passing frame information

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Transmit registers can be used to pass frame information for long messages stored in shared system memory. This frame information typically includes details such as the start address, the number of words, and possibly a message type code.

- Passing event notices and requests

Processor A and Processor B can signal events and requests that do not include data words by using general interrupts. For example, they can acknowledge that a long message has been read from shared system memory.

- Passing fixed length data.

Fixed-length data with a specific format can be stored in predefined locations within the shared memory. A processor can use a general interrupt—from either Processor A or Processor B—to notify the other processor that the data is prepared and ready for processing.

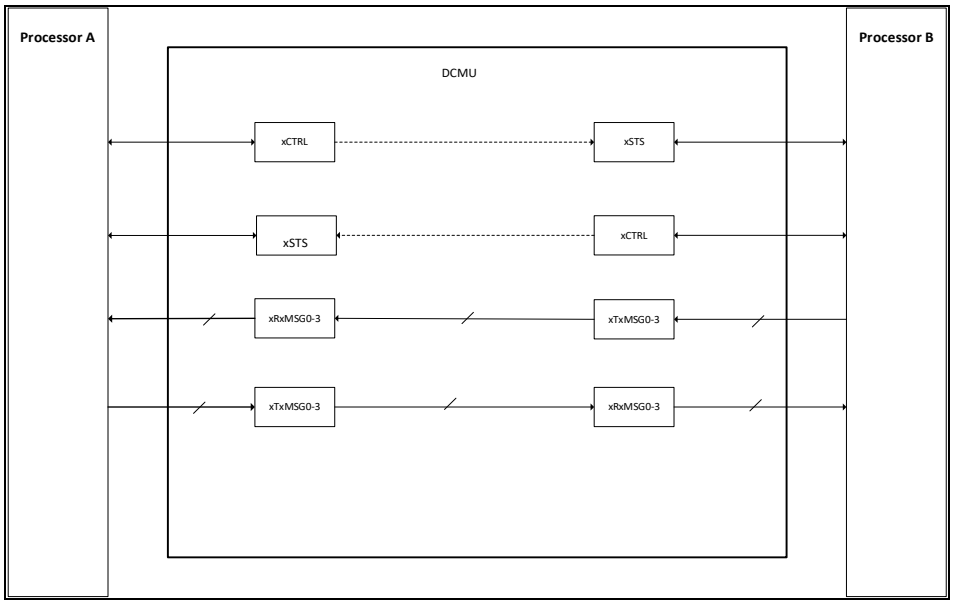
- Passing announcements

The three flags can be used by a processor to announce its current program state or other status messages to the other processor.

All the message type mentioned above transmission through the following structure.

The message transmits use the registers include CTRL, STS, RCVMSG0-RCVMSG3 and TXMSG0-TXMSG3.

Figure 8-2 DCMU Messaging Transmission



8.3.2.1 Reset

The DCMU has two sources of reset, each with a different function from either the DCMU's perspective or the system's perspective.

- An asynchronous system reset is connected to both sides of the DCMU interface.
- One programmable hardware reset (MURST bit) in the DCMUA_CTRL register (on the Processor A side).

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Table 8-2 DCMU Programmable Reset

Reset	Description
Processor A DCMU reset	● Processor A DCMU Reset bit (MURST) of the DCMUA_CTRL register ● The MURST reset impacts the messaging sections on both Processor A and Processor B sides. It causes all control and status registers to revert to their default values and clears all internal states. ● It is up to the Processor A software to decide whether to use the MURST reset or not. ● After asserting the MURST bit, the instruction immediately following should not write to DCMU registers. Such a write may be overwritten by the reset sequence, causing the register to remain at its reset value. It is recommended to wait at least one instruction after asserting the MURST bit before attempting to write to DCMU registers.

After initiating reset events using the MURST bit, the program running on Processor A can confirm the completion of the reset sequence on the Processor B side by examining the RSTF bit in the DCMUA_STS register.

8.3.2.2 Interrupts

The DCMU handles interrupt requests between Processor A and Processor B, managing interrupts from Processor B to Processor A and vice versa. This section details all the interrupts generated by the module.

8.3.2.2.1 Interrupts to the Processors

There are 12 interrupt sources from the DCMU to the Processors:

- Four receive interrupts for each of the receive registers: Asserted when the Processor receive full bits (xSTS[RFFn]) are set and the xCTRL[RFIEn] bits enabled
- Four transmit interrupts for each of the transmit registers: Asserted when the Processor transmit empty bits (xSTS[TEFn]) are set and the xCTRL[TEIEn] bits enabled
- Four general purpose interrupts: Asserted when the xSTS[GPIFn] bits are set and the xCTRL[GPIEn] bits enabled

All interrupts can be masked using the Processor Control Register (xCTRL). The DCMU does not assign any internal priority to these interrupts. Consequently, multiple interrupts—such as Receive 0 and Receive 1 interrupts, or any combination of transmit and general-purpose interrupts—can be triggered simultaneously. The prioritization of these interrupts should be managed by the interrupt controller at the chip level.

To deactivate the request to the interrupt controller, the software should clear the General Purpose Interrupt Pending bits (GPIF0, GPIF1, GPIF2, and GPIF3), typically as part of the interrupt service routine.

8.3.2.2.2 General Purpose Interrupt Clearing Sequence

When one processor writes to the General Purpose Interrupt Request (GPIR) bit, this write operation is synchronized with the clock of the other processor to set the General Purpose Interrupt Pending (GPIF) bit on that side. Once the GPIF bit is set, and if the General Purpose Interrupt Enable (GPIE) bit is also set on the receiving processor's side, the transmitting processor issues a general-purpose interrupt to the receiving processor. The receiving processor can clear this interrupt by writing a "1" to its GPIF bit, which deactivates the interrupt immediately upon writing. This

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write operation is also synchronized with the clock of the other processor, resulting in the clearing of the GPIR bit on the transmitting side. It is recommended that software refrains from writing to the GPIR bit again until it has been cleared to prevent any synchronization issues.

8.3.2.3 Interrupt Messaging Protocols

8.3.2.3.1 Messaging Protocols Using Interrupts

The following example illustrates a four-word messaging sequence sent from one processor to the other.

In this example, the receive interrupts for the first, second, and third messages are disabled, while the receive interrupt for the fourth message is enabled. The registers are written sequentially for $n = 0, 1, 2, 3$. For $n = 0, 1,$ and 2 , the interrupts are disabled; therefore, no interrupt is sent to the other core complex, even though interrupt conditions occur. For $n = 3$, the interrupt is enabled, and the final Receive Interrupt request is generated.

1. Write Sequence

- The Processor writes the message information sequentially to its Transmit Registers 0, 1, 2.
- When Transmit Register 3 is written to, the RFF3 bit in the xSTS register is set after synchronization, and it immediately triggers the Receive 3 interrupt on the other processor.

2. Read Sequence

- Upon acknowledging the Receive 3 interrupt, the other processor proceeds to read the message transmitted from the receive registers.
- After completing the read from Receive Register 3, the interrupt bit is cleared.

Figure 8-3 shows the programmer's model of a messaging protocol using transmit and receive registers. Refer to Table 1 3 and Figure 8-3 for a comprehensive understanding of the generalized protocol sequence.

Figure 8-3 Messaging Model Using Transmit and Receive Registers

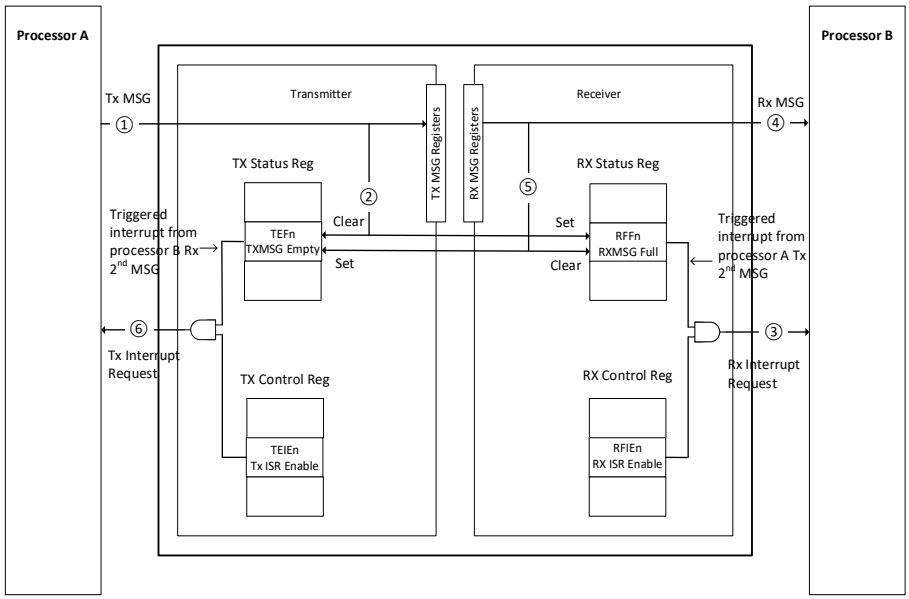

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Table 8-3 Messaging Protocol Using Transmit and Receive Registers.

Sequence	Action	Description
1	Processor A Data write	When Processor A writes data to the DCMUA_TXMSGn register, it is immediately reflected in Processor B's DCMUB_RCVMSGn register.
2	Clear Tx Empty bit and Set Rx Full bit	-The data write to the DCMUA_TXMSGn register Clears the transmitter empty bit (TEFn) in the Processor A Transmit Status Register - Sets the receiver full bit (RFFn) in the Processor B Receive Status Register
3	Generate Receive Interrupt request	When the receiver full bit (RFFn) in the Receive Status Register is set, it generates a Receive Interrupt request to Processor B.
4	Processor B Data read	Upon receiving the Receive Interrupt request, Processor B reads data from the DCMUB_RCVMSGn register.
5	Clear Rx Full bit and Set Tx Empty bit	- Reading the data out of the DCMUB_RCVMSGn register - Clears the receiver full bit (RFFn) in the Processor B Receive Status Register Sets the transmitter empty bit (TEFn) in the Processor A Transmit Status Register
6	Generate Transmit Interrupt request	When the transmitter empty bit (TEFn) in the Transmit Status Register is set, it generates a Transmit Interrupt request to Processor A.

Note:

Transmit registers are utilized to convey frame information for long messages stored in shared memory. This frame information typically includes the starting address, the word count, and potentially a message type code.

Software can leverage the messaging hardware to establish protocols for various message types. Comprehensive support is provided for both interrupt-driven and polling-based management approaches.

The software procedure as follow:

(1) Set the DCMUB_CTRL.RFIE3 to 1, and set DCMUA_CTRL.TFIE3 to 1.

(2) Processor A Write 3 data to DCMUA_TXMSG0, DCMUA_TXMSG1, DCMUA_TXMSG2 register.

(3) generate a Receive Interrupt request to Processor B.

(4) Upon receiving the Receive Interrupt request, Processor B reads DCMUB_RCVMSG0, DCMUB_RCVMSG1, and DCMUB_RCVMSG2 register.

(5) Reading DCMUB_RCVMSG0, DCMUB_RCVMSG1, and DCMUB_RCVMSG2 registers will clear the DCMUB_CTRL.RFFn and set the DCMUA_CTRL.TEFn.

(6) The set of DCMUA_CTRL.TEFn generate an Interrupt request to Processor A.

(7) Repeat (2) ~ (7) to send another 4 data.

8.3.2.3.2 Messaging Protocols Using Event Interrupts

Events and requests that do not include data words can be communicated from Processor B to Processor A using the two general-purpose interrupts. Fixed-length formatted data can be stored in predefined locations within shared memory. A processor can use a general-purpose interrupt to notify the other processor that the data is ready. The three flags can be used by a processor to indicate its current program state or convey similar information to the other processor.

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Table 8-4 and Figure 8-4 describe the event sequence when the Processor triggers an interrupt.

Figure 8-4 Messaging Model Using a General Purpose Interrupt

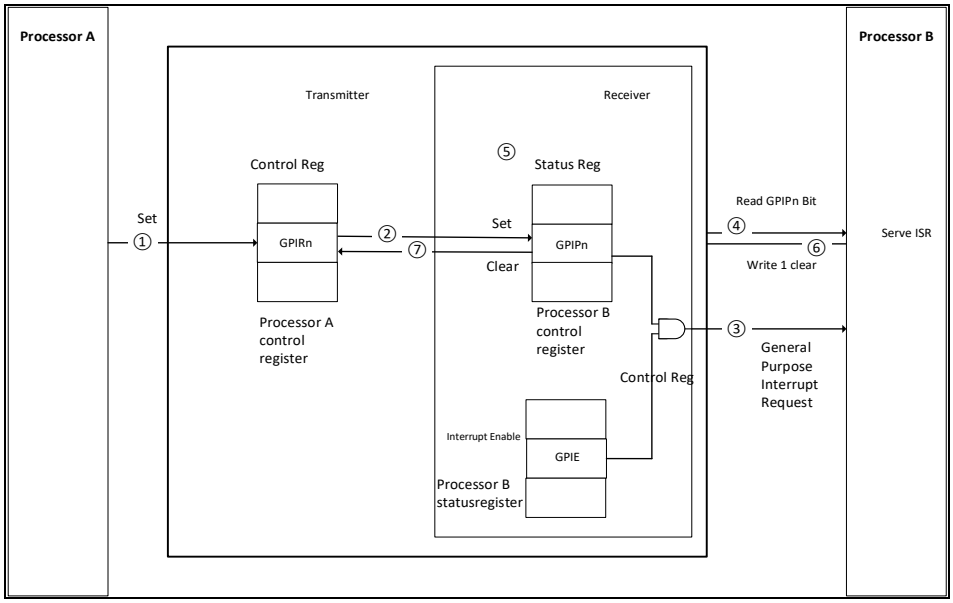

Table 8-4 Interrupt Messaging Protocol (Generalized)

Sequence	Action	Description
1	Processor A sets General Interrupt request bit	Processor A sets its corresponding General Interrupt Request bit (GPIRn = 1) in the control register (DCMUA_CTRL).
2	General Interrupt Request Pending status bit is set	The General Interrupt Request Pending status bit (GPIFn) in the status register DCMUB_STS is set to “1”.
3	General Interrupt request to Processor B is generated	Setting the GPIFn bit generates a General Interrupt request to Processor B. However, the Interrupt Request Enable bit (GPIEn) must be set on Processor B for the interrupt to be received
4	Processor B reads status register	The Processor B reads the GPIFn bit in the DCMUB_STS register.
5	Processor B services the interrupt	-
6	Processor B sets GPIFn bit to clear interrupt	Processor B clears the interrupt by writing a “1” to the corresponding GPIFn bit.
7	GPIRn bit is cleared	By setting the GPIFn bit to “1”, the General Interrupt Request bit (GPIRn) in Processor A’s control register (DCMUA_CTRL) is cleared.

The software procedure as follow:

1 Set DCMUB_CTRL.GPIEn to 1.

2 Set the associates DCMUA_CTRL.GPIRn,

3 Set DCMUB_STS.GPIFnto 1

4 Processor B read the GPIFn in DCMUB_STS.

5 Processor read data from predefined locations in the shared memory.

6 The Processor B write 1 to the GPIFn to clear the interrupt.

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7 Set GPIFn to 1 to clear DCMUA_CTRL.GPIRn.

8.3.2.4 Exclusive Access to Shared Memory

The DCMU can be used to notify one processor that the other is currently accessing shared memory, thereby preventing potential data overwriting during periods of exclusive memory access.

The tables below detail the signaling protocol used by Processor A to indicate to Processor B that it is currently writing to shared memory. It is assumed that specific bits and registers—including the GPIR0 bit, DCMUB_RCVMSG0 register, DCMUB_TXMSG0 register, DCMUA_RCVMSG0 register, and DCMUA_TXMSG0 register—are allocated to facilitate exclusive access within the shared memory protocol.

Table 8-5 Processor A Performs an Exclusive Access to Shared Memory

Sequence	Action	Description
1	Processor A sends GPIRn request to Processor B using Processor A control register	When Processor A wants to perform exclusive access to the shared memory, it sends a GPIR0 request to Processor B.
2	Processor A sends an exclusive access request using a transmit data register (DCMUA_TXMSGn)	Processor A sends an exclusive-access request including the command, target location, and length of the access to Processor B using a selected transmit data register (DCMUA_TXMSG0)
3	Processor A waits for a dedicated interrupt from Processor B	The Processor A waits for a dedicated interrupt (as an acknowledgement) triggered by the Processor B before proceeding.
4	Processor A accesses shared memory	After receiving a dedicated interrupt from the Processor B, Processor A proceeds.

Table 8-6 Processor B Scans for Transaction Information

Sequence	Action	Description
1	Processor B receives an interrupt from a receive data register (DCMUB_RCVMSGn)	-
2	Processor B reads the receive data register (DCMUB_RCVMSGn)	-
3	Processor B scans the receive data register contents	For transaction information (whether Processor A has requested an exclusive-access)

Table 8-7 Processor B Accepts Exclusive Access by Processor A

Sequence	Action	Description
1	Processor B triggers a dedicated interrupt	Processor B acknowledges Processor A’s request by triggering a dedicated acknowledgment interrupt to Processor A.
2	Processor B sends a code message to Processor A	In addition to the acknowledgment interrupt, Processor B sends a code message to Processor A through the designated transmit register (DCMUB_TXMSGn). This message notifies Processor A that it can now exclusively access the shared memory.

Table 8-8 Processor B Rejects Exclusive Access by Processor A

Sequence	Action	Description
1	Processor B ignores Processor A	If Processor B does not grant permission to Processor A, it will ignore the

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	request for exclusive access	exclusive access request.

The software procedure is as follows:

1 If Processor A intends to perform an exclusive access to the shared memory, it sets the GPIRn bit to 1 in the DCMUA_CTRL register. Concurrently, Processor B enables the corresponding interrupt by setting the GPIEn bit to 1 in its DCMUB_CTRL register.

2 Processor A send write data to DCMUA_TXMSGn.

3 Processor B Check the DCMUB_STS.RFFn, and Read DCMUB_RCVMSGn.

4 Processor B scans the received data.

5 If Processor B accepts the exclusive access requested by Processor A, Processor B sets DCMUB_CTRL.GPIRn to 1, generates DCMUA_STS.GPIFn to inform Processor A of acceptance, and writes a code message to DCMUB_TXMSGn.

6 Upon receiving a dedicated interrupt from Processor B, Processor A proceeds with the exclusive access procedure.

8.3.2.5 Packet Data Transfers

The following example illustrates the packet transfer sequence between the Processor B and Processor A subsystems:

Table 8-9 Packet Data Transfer Sequence

Sequence	Action	Description
1	Processor B requests DMA	The Processor B sends a DMA request to initiate the packet data transfer.
2	DMA data transfer	DMA acknowledges.
3		DMA starts transferring data from the specified Processor B location to the specified shared memory.
4		DMA interrupts the Processor B to signal that the packet transfer has finished.
5	Processor B informs Processor A that data is in shared memory	Processor B uses the DCMU's transmit register on its side to send a packet information message to Processor A, notifying it of newly arrived packet data stored in shared memory. This message includes the command, the data location, and the length of the packet information
6	Processor A receives interrupt	Processor A receives an interrupt (assuming its corresponding DCMU-side receive interrupt is enabled), which activates the pending processing task to handle and process the packet data from memory.
7	Processor A reads data, writes data	The Processor A reads or processes packet data from shared memory.
8		The Processor A writes the result of packet processing to a separate buffer.
9	Processor A informs Processor B that transfer is finished	After Processor A completes processing the packet data, it notifies Processor B by using the DCMU Processor A Side transmit register (DCMUA_TXMSGn).
10	Processor A sends interrupt to Processor B (request for more data)	Processor B receives a subsequent interrupt from Processor A, indicating that Processor A is requesting additional packet data.

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8.4 Application Information

This section describes certain software restrictions when accessing the DCMU.

8.4.1 General Restrictions

This section lists the restrictions that are applicable to both sides (Processor A, Processor B) of the DCMU.

8.4.1.1 Write-After-Write to a Transmit Register

A write to a transmit register indicates to the receiver side that data is prpared for retrieval.

- Writing to the transmit register again without first confirming that the data has been retrieved is prohibited, since the transmitter cannot accurately determine when the receiver will attempt to access the data.
- Before attempting to write to the transmit register again, the transmitter side should wait for a “Transmitter Empty” interrupt or poll the “Transmitter Empty” bit in the Status Register.
- Failing to adhere to this restriction could result in incorrect data being read on the receiver side of the DCMU.

8.4.1.2 Read-After-Read from a Receive Register

Reading a receive register notifies the transmitter side that data can be written to that register. Similarly, the receiver processor should refrain from reading a receive register until it has received a “Receiver Full” interrupt or has polled the “Receiver Full” bit in the Status Register.

- Reading a receive register again without first confirming that the data has been written is prohibited, because the receiver cannot accurately determine when the transmitter will attempt to write the data.
- Before attempting to read the receive register again, the receiver side should wait for a “Receiver Full” interrupt or poll the “Receiver Full” bit in the Status Register.
- Failing to adhere to this restriction may cause incorrect data to be written on the transmitter side of the DCMU.

8.4.2 Processor Restrictions

This section outlines the restrictions that apply to each processor side within the DCMU.

8.4.2.1 Before Entering Low Power Mode

Before entering Low Power mode, the processor must ensure that the Processor Event Pending (EP) bit in the Status Register is cleared.

- If the Event Pending bit (EPF) remains set to “1,” the processor must wait and continuously poll the EPF bit until it is cleared before executing the low power mode instruction.
- Please note that if the other processor is in Low Power mode, the EPF bit may remain set to “1.” In this situation, the other processor’s clock must be turned on to clear the EPF bit before the processor can enter Low Power mode.

8.4.2.2 Before Setting a General Interrupt Request Bit (GIR0–3)

Before setting a General Interrupt Request bit (GPIR0–3), ensure that the corresponding GPIRn bit is cleared,

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indicating that no general interrupt is currently pending. Typically, attempting to set the GPIRn bit when it is already set to “1” will be ignored. However, in some cases, this action may trigger a second interrupt. This restriction is implemented to prevent unpredictable behavior.

8.4.2.3 Reset Bit Restrictions

The reset bit (MURST) restrictions are:

- Before asserting the MURST bit in the DCMUA_CTRL register, ensure that Processor B is not currently engaged in any DCMU-related activities.
- Avoid writing to an DCMU register in the instruction immediately following the assertion of the MURST bit in the DCMUA_CTRL register, as the written data may be overwritten by the reset value.

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8.5 Registers

The DCMU registers contains two sides:

- DCMU registers on Processor A-Side (CM7);
- DCMU registers on Processor B-Side (CM4);

8.5.1 DCMU Processor A-Side Registers

8.5.1.1 DCMU Processor A Transmit Message Register 0 (DCMUA_TXMSG0)

Address Offset: 0x0000

Reset Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
w															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Transmit Message Register 0 Data write in TXMSG0 is reflected in the Processor B RCVMSG0 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF0) in the Processor A Status Register (DCMUA.STS) on the transmitter side, and sets a “receive full flag” bit (RFF0) in the Processor B side.

8.5.1.2 DCMU Processor A Transmit Message Register 1 (DCMUA_TXMSG1)

Address Offset: 0x0004

Reset Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
w															

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Bit field	Name	Description
31:0	DATA[31:0]	Processor A Transmit Message Register 1 Data write in TXMSG1 is reflected in the Processor B RCVMSG1 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF1) in the Processor A Status Register (DCMUA.STS) on the transmitter side, and sets a “receive full flag” bit (RFF1) in the Processor B side.

8.5.1.3 DCMU Processor A Transmit Message Register 2 (DCMUA_TXMSG2)

Address offset: 0x0008

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
w															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Transmit Message Register 2 Data write in TXMSG2 is reflected in the Processor B RCVMSG2 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF2) in the Processor A Status Register (DCMUA.STS) on the transmitter side, and sets a “receive full flag” bit (RFF2) in the Processor B side.

8.5.1.4 DCMU Processor A Transmit Message Register 3 (DCMUA_TXMSG3)

Address offset: 0x000C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
w															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Transmit Message Register 3 Data write in TXMSG3 is reflected in the Processor B RCVMSG3 register.

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Bit field	Name	Description
		A Write to the transmit register clears a “transmit empty flag” bit (TEF3) in the Processor A Status Register (DCMUA.STS) on the transmitter side, and sets a “receive full flag” bit (RFF3) in the Processor B side.

8.5.1.5 DCMU Processor A Receive Message Register 0 (DCMUA_RCVMSG0)

Address offset: 0x0010

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Receive Message Register 0 Data reflects the data written to Processor B Transmit Register 1 (DCMUB.TXMSG0) Reading the RCVMSG0 register clears the “receive full flag” bit (RFF0) in the Processor A Status Register (DCMUA.STS) on the receive side, and sets the “transmit empty flag” (TEF0) in the Processor B Status Register on the transmit side.

8.5.1.6 DCMU Processor A Receive Message Register 1 (DCMUA_RCVMSG1)

Address offset: 0x0014

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Receive Message Register 1 Data reflects the data written to Processor B Transmit Register 1 (DCMUB.TXMSG1) Reading the RCVMSG1 register clears the “receive full flag” bit (RFF1) in the Processor A Status Register (DCMUA.STS) on the receive side, and sets the “transmit

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Bit field	Name	Description
		empty flag" (TEF1) in the Processor B Status Register on the transmit side.

8.5.1.7 DCMU Processor A Receive Message Register 2 (DCMUA_RCVMSG2)

Address offset: 0x0018

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Receive Message Register 2 Data reflects the data written to Processor B Transmit Register 1 (DCMUB.TXMSG2) Reading the RCVMSG2 register clears the "receive full flag" bit (RFF2) in the Processor A Status Register (DCMUA.STS) on the receive side, and sets the "transmit empty flag" (TEF2) in the Processor B Status Register on the transmit side.

8.5.1.8 DCMU Processor A Receive Message Register 3 (DCMUA_RCVMSG3)

Address offset: 0x001C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r															

Bit field	Name	Description
31:0	DATA[31:0]	Processor A Receive Message Register 3 Data reflects the data written to Processor B Transmit Register 1 (DCMUB.TXMSG3) Reading the RCVMSG3 register clears the "receive full flag" bit (RFF3) in the Processor A Status Register (DCMUA.STS) on the receive side, and sets the "transmit

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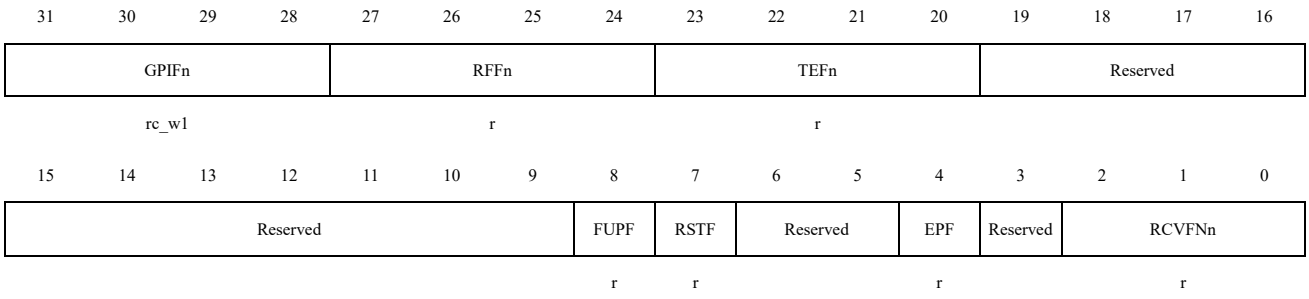
Bit field	Name	Description
		empty flag" (TEF3) in the Processor B Status Register on the transmit side.

8.5.1.9 DCMUA Processor A Status Register (DCMUA_STS)

Address offset: 0x0020

Reset value: 0x00F0 0080



Bit field	Name	Description
31:28	GPIFn[0:3]	For n = {0, 1, 2, 3} Processor A General Interrupt Request n Pending Flag. (Read-Write) GIPn bit signals the Processor A that the GPIRn bit in the DCMUB.CTRL register on the Processor B-side was set from "0" to "1". If the GPIEn bit in the DCMUA.CTRL register is set to "1", a General Purpose Interrupt n request is issued. The GPIFn bit is cleared by writing it back as "1". Writing "0", or writing "1" when the GPIFn bit is cleared is ignored. Use this feature in the interrupt routine, where the GPIFn bit is cleared in order to de-assert the interrupt request source at the interrupt controller. The proper bit clearing sequence is: clear a Processor A register, set the desired bit in it (Processor A register), and write it to the DCMUA.STS register, thus clearing the GPIFn bit.
27:24	RFFn[0:3]	For n = {0, 1, 2, 3} Processor A Receive Message Register n Full Flag. (Read-Only) 0: DCMUA.RCVMSG is not full (default) 1: DCMUA.RCVMSG is full
23:20	TEFn[0:3]	For n = {0, 1, 2, 3} Processor A Transmit Message Register n Full Flag. (Read-Only) 0: DCMUA.TXMSG is not empty 1: DCMUA.TXMSG is empty(default)
19:9	Reserved	Reserved, the reset value must be maintained.
8	FUPF	Processor A Flags Update Pending Flag 0: No flags updated, initiated by the Processor A, in progress (default) 1: Processor A initiated flags update, processing
7	RSTF	Processor B reset state
6:5	Reserved	Reserved, the reset value must be maintained.
4	EPF	Processor A-side Event Pending Flag

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Bit field	Name	Description
		0: The Processor A-side event is not pending (default) 1: The Processor A-side event is pending
3	Reserved	Reserved, the reset value must be maintained.
2:0	RCVFNn[2:0]	For n = {0,1,2} Processor A-side Receive Flag Number n. (Read-only) 0: TXFNn bit in DCMUB.CTRL register is written 0 (default) 1: TXFNn bit in DCMUB.CTRL register is written 1

8.5.1.10 DCMUA Processor A Control Register (DCMUA_CTRL)

Address offset: 0x0024

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIEn				RFIEn				TEIEn				GPIRn			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										MURST	Reserved		TXFNn		
										rw			rw		

Bit field	Name	Description
31:28	GPIEn[0:3]	For n= {0,1,2,3} Processor A General Purpose Interrupt Request Enable Register (Read-Write) 0000 – Disables Processor A General Purpose Interrupt n. (default) 0001 – Enables Processor A General Purpose Interrupt n.
27:24	RFIEn[0:3]	For n= {0,1,2,3} Processor A Receive Full Interrupt Enable Register (Read-Write) 0000 - Disables Processor A Receive Full Interrupt n. (default) 0001 - Enables Processor A Receive Full Interrupt n.
23:20	TEIEn[0:3]	For n= {0,1,2,3} Processor A Transmit Empty Interrupt Enable Register (Read-Write) 0000 - Disables Processor A Transmit Empty Interrupt n. (default) 0001 – Enables Processor A Transmit Empty Interrupt n.
19:16	GPIRn[0:3]	For n= {0,1,2,3} Processor A General Purpose Interrupt Request n (Read-Write) 0000 - Processor A General Interrupt n is not requested to the Processor B (default). 0001 - Processor A General Interrupt n is requested to the Processor B.
15:6	Reserved	Reserved, the reset value must be maintained.
5	MURST	Processor A DCMU Reset. • Setting MURST bit to "1" resets both the Processor B and the Processor A sides of the DCMU module, forcing all control and status registers to return to their default values and all internal states to be cleared. • Before setting the MURST bit to "1", it is advisable to interrupt the Processor B, because setting the MURST bit may affect the ongoing Processor B program. • After setting the MURST bit, monitor the value of the RSTF bit in the DCMUA_STS

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Bit field	Name	Description
		register to know when the reset sequence on the Processor B-side has ended. • MURST bit can only be written as "1". • MURST bit is always read as "0". • MURST bit is cleared during the DCMU reset sequence. 0 - N/A. Self -clearing bit (default). 1 - Asserts the Processor A DCMU reset.
2:0	TXFNn[2:0]	For n= {0,1,2,3} Processor A to Processor B Transmit Flag Number n (Read-Write) 000 - Clears the RCVFNn bit in the DCMUB.STS register 001 - Sets the RCVFNn bit in the DCMUB.STS register

8.5.2 DCMU Processor B-Side Registers

8.5.2.1 DCMU Processor B Transmit Message Register 0 (DCMUB_TXMSG0)

Address offset: 0x0000

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
w															

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Transmit Message Register 0 Data write in TXMSG0 is reflected in the Processor A RCVMSG0 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF0) in the Processor B Status Register (DCMUB.STS) on the transmitter side, and sets a “receive full flag” bit (RFF0) in the Processor A side.

8.5.2.2 DCMU Processor B Transmit Message Register 1 (DCMUB_TXMSG1)

Address offset: 0x0004

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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DATA[15:0]

w

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Transmit Message Register 1 Data write in TXMSG1 is reflected in the Processor A RCVMSG1 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF1) in the Processor B Status Register (DCMUB.STS) on the transmitter side, and sets a “receive full flag” bit (RFF1) in the Processor A side.

8.5.2.3 DCMU Processor B Transmit Message Register 2 (DCMUB_TXMSG2)

Address offset: 0x0008

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
w															

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Transmit Message Register 2 Data write in TXMSG2 is reflected in the Processor A RCVMSG2 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF2) in the Processor B Status Register (DCMUB.STS) on the transmitter side, and sets a “receive full flag” bit (RFF2) in the Processor A side.

8.5.2.4 DCMU Processor B Transmit Message Register 3 (DCMUB_TXMSG3)

Address offset: 0x000C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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DATA[15:0]

w

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Transmit Message Register 3 Data write in TXMSG3 is reflected in the Processor A RCVMSG3 register. A Write to the transmit register clears a “transmit empty flag” bit (TEF3) in the Processor B Status Register (DCMUB.STS) on the transmitter side, and sets a “receive full flag” bit (RFF3) in the Processor A side.

8.5.2.5 DCMU Processor B Receive Message Register 0 (DCMUB_RCVMSG0)

Address offset: 0x0010

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r															

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Receive Message Register 0 Data reflects the data written to Processor A Transmit Register 1 (DCMUA.TXMSG0) Reading the RCVMSG0 register clears the “receive full flag” bit (RFF0) in the Processor B Status Register (DCMUB.STS) on the receive side, and sets the “transmit empty flag” (TEF0) in the Processor A Status Register on the transmit side.

8.5.2.6 DCMU Processor B Receive Message Register 1 (DCMUB_RCVMSG1)

Address offset: 0x0014

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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DATA[15:0]

r

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Receive Message Register 1 Data reflects the data written to Processor A Transmit Register 1 (DCMUA.TXMSG1) Reading the RCVMSG1 register clears the “receive full flag” bit (RFF1) in the Processor B Status Register (DCMUB.STS) on the receive side, and sets the “transmit empty flag” (TEF1) in the Processor A Status Register on the transmit side.

8.5.2.7 DCMU Processor B Receive Message Register 2 (DCMUB_RCVMSG2)

Address Offset: 0x0018

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															

r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															

r

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Receive Message Register 2 Data reflects the data written to Processor A Transmit Register 1 (DCMUA.TXMSG2) Reading the RCVMSG2 register clears the “receive full flag” bit (RFF2) in the Processor B Status Register (DCMUB.STS) on the receive side, and sets the “transmit empty flag” (TEF2) in the Processor A Status Register on the transmit side.

8.5.2.8 DCMU Processor B Receive Message Register 3 (DCMUB_RCVMSG3)

Address offset: 0x001C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA[31:16]															

r

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r															

Bit field	Name	Description
31:0	DATA[31:0]	Processor B Receive Message Register 3 Data reflects the data written to Processor A Transmit Register 1 (DCMUA.TXMSG3) Reading the RCVMSG3 register clears the “receive full flag” bit (RFF3) in the Processor B Status Register (DCMUB.STS) on the receive side, and sets the “transmit empty flag” (TEF3) in the Processor A Status Register on the transmit side.

8.5.2.9 DCMUB Processor B Status Register (DCMUB_STS)

Address offset: 0x0020

Reset value: 0x00F0 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPIFn				RFFn				TEFn				Reserved			
rc_w1				r				r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							FUPF	RSTF	Reserved		EPF	Reserved	RCVFNn		
							r	r			r		r		

Bit field	Name	Description
31:28	GPIFn[0:3]	For n = {0, 1, 2, 3} Processor B General Interrupt Request n Pending Flag. (Read-Write) GIPn bit signals the Processor B that the GPIRn bit in the DCMUA.CTRL register on the Processor A-side was set from "0" to "1". If the GPIEn bit in the DCMUB.CTRL register is set to "1", a General Purpose Interrupt n request is issued. The GPIFn bit is cleared by writing it back as "1". Writing "0", or writing "1" when the GPIFn bit is cleared is ignored. Use this feature in the interrupt routine, where the GPIFn bit is cleared in order to de-assert the interrupt request source at the interrupt controller. The proper bit clearing sequence is: clear a Processor B register, set the desired bit in it (Processor B register), and write it to the DCMUB.STS register, thus clearing the GPIFn bit.
27:24	RFFn[0:3]	For n = {0, 1, 2, 3} Processor B Receive Message Register n Full Flag. (Read-Only) 0: DCMUB.RCVMSG is not full (default)

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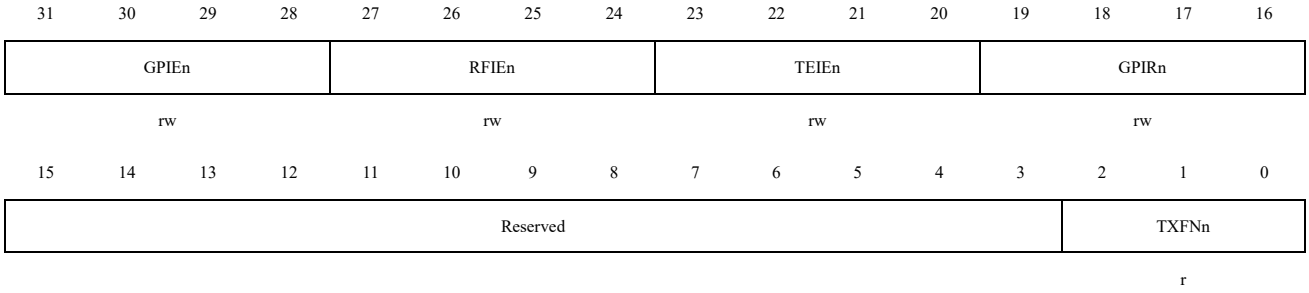
Bit field	Name	Description
		1: DCMUB.RCVMSG is full
23:20	TEFn[0:3]	For n = {0, 1, 2, 3} Processor B Transmit Message Register n Full Flag. (Read-Only) 0: DCMUB.TXMSG is not empty 1: DCMUB.TXMSG is empty(default)
19:9	Reserved	Reserved, the reset value must be maintained.
8	FUPF	Processor A Flags Update Pending Flag 0: No flags updated, initiated by the Processor B, in progress (default) 1: Processor A initiated flags update, processing
7	RSTF	Processor A reset state
6:5	Reserved	Reserved, the reset value must be maintained.
4	EPF	Processor B-side Event Pending Flag 0: The Processor B-side event is not pending (default) 1: The Processor B-side event is pending
3	Reserved	Reserved, the reset value must be maintained.
2:0	RCVFNn[2:0]	For n = {0,1,2} Processor B-side Receive Flag Number n. (Read-only) 0- TXFNn bit in DCMUA.CTRL register is written 0 (default) 1- TXFNn bit in DCMUA.CTRL register is written 1

8.5.2.10 DCMUB Processor B Control Register (DCMUB_CTRL)

Address offset: 0x0024

Reset value: 0x0000 0000



Bit field	Name	Description
31:28	GPIEn[0:3]	For n= {0,1,2,3} Processor B General Purpose Interrupt Request Enable Register (Read-Write) 0000 – Disables Processor B General Purpose Interrupt n. (default) 0001 – Enables Processor B General Purpose Interrupt n.
27:24	RFIEn[0:3]	For n= {0,1,2,3} Processor B Receive Full Interrupt Enable Register (Read-Write) 0000 - Disables Processor B Receive Full Interrupt n. (default) 0001 - Enables Processor B Receive Full Interrupt n.
23:20	TEIEn[0:3]	For n= {0,1,2,3} Processor B Transmit Empty Interrupt Enable Register (Read-Write) 0000 - Disables Processor B Transmit Empty Interrupt n. (default)

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Bit field	Name	Description
		0001 – Enables Processor B Transmit Empty Interrupt n.
19:16	GPIRn[0:3]	For n= {0,1,2,3} Processor B General Purpose Interrupt Request n (Read-Write) 0000 - Processor B General Interrupt n is not requested to the Processor B (default). 0001 - Processor B General Interrupt n is requested to the Processor B.
15:3	Reserved	Reserved, the reset value must be maintained.
2:0	TXFNn[2:0]	For n= {0,1,2,3} Processor B to Processor A Transmit Flag Number n (Read-Write) 000 - Clears the RCVFNn bit in the DCMUA.STS register 001 - Sets the RCVFNn bit in the DCMUA.STS register

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9 One-time Programmable Controller (OTPC)

9.1 Introduction

One-time programmable (OTP) memory are fuse type of memory device that can allow one time program from one value to the opposite. Some fuse memory default value is 1 and can program to 0, some are native 0 can program to 1. This OTP controller is design for EMEMORY EG002K32TJ022LZ01 anti-fuse IP with size 2K words (8 Kbytes). Initial value of this memory is 1 and can be programmed to 0. It has built-in redundancy and repair function. It supports bit program. Using OTP as storage for Analog trim values and system configurations. When system boot up, OTP controller (OTPC) should read out trim values and system configurations and provide to other IPs.

9.2 Main Features

OTPC controller module is design to provide a secure system setting storage and automatic setting loading when boot up. Each address corresponds to a data length of 32 bits. The main features of OTPC are shown in below Table 9-1:

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Table 9-1 OTPC feature Description

Features	Sub Feature	Scenario
Clock	sys_clk	System clock, only used during boot up. When system is booting up, clock Maximum frequency is around 64 MHz
	apb_clk	APB clock used to access OTPC register for issue read/write operation under Normal condition. (External conncetion AHB Bus)Maximum frequency is 300 MHz
Reset	sys_rst_n	Reset signal for system clock domain signals.
	prst_n	Reset signal for AHB clock domain signals.
Register	Lock	When OTPC_CTRL.LOCK is Locked, OTPC_CTRL register can't be change. User needs to program correct key in correct order to unlock OTPC_CTRL register access. If OTPC_CTRL is Locked, user can only do read operation.
	Program	OTPC_CTRL.PRMD bit indicates next operation is read or write. Operation is issued by OTPC_ADDR register.
	Read	When OTPC_CTRL.PRMD is 0 or OTPC_CTRL.LOCK is 1, User write to OTPC_ADDR register will trigger read operation to corresponding address.
	Error	There are seven error types. KEY error, program error, write error, read error, OOR error, busy error.
	Valid tags	Valid tag of system configures multi-copy area. Each valid tag standards for 16 copies of certain area.
	Unused	Unused tag for User memory and system configuration reserve area
Boot Up (Power Up)	Valid tags read	Once the system boots up, SMU will request OTP starts to read analog trim value and system configurations. First OTPC will read valid tag and unused information in order to locate correct copy of system information or configuration.
	Key read	OTPC key is encrypted with Fixed key and protected by complement.
	System info read	System info region contains analog trim values and peripheral enable information. This region will be decrypted with read out OTP key.
	System config read	System configuration region contains some system details. This region will be decrypted with read out OTP key.
Normal Mode	OTPC read	After booting up, user can issue a read operation by program read address with OTPC_CTRL.PRMD is 0. Check error bits to ensure read operation is not in protection region. Then check OTPC_STS.BUSY bit to make sure read process is finished. After OTPC_STS.BUSY bit become 0, user can read data from OTPC_RDATA register.
	OTPC write	After booting up, user can issue a write operation by unlock OTPC_CTRL register and change OTPC_CTRL.PRMD to 1. Then write program data to OTPC_WDATA register and issue the write access by write program address to OTPC_ADDR register. Check error bits to ensure write operation is not in protection region. Then check OTPC_STS.BUSY bit to make sure write process is finished.

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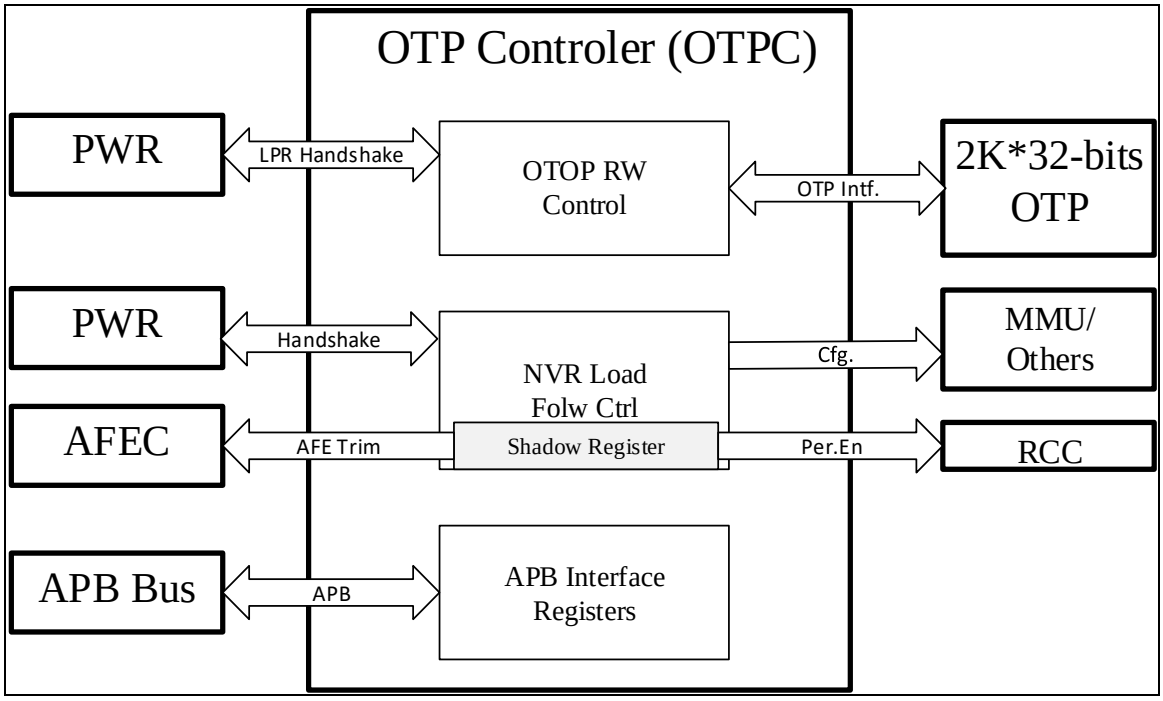
9.3 Functional Description

Block diagram of OTPC in system level is shown in Figure 9-1. OTPC interacts with Power manage module (PWR) for low power mode request. PWR module also in charge of OTP power switch and low power control. OTPC handshakes with SMU module during system boot up for boot up flow control.

Figure 9-1 OTPC System level diagram



OTPC provides read out trim values from OTP to AFEC for Analog modules trimming. MMU and other peripheral gets system configuration from OTPC after booting up. OTPC also stores peripheral enable controls and provides to RCC module for peripheral enable/disable. APB interface is used for register read/write operation.

Main framework of OTPC is shown in Figure 9-2. There are two sets of control paths and state machines in OTPC. One for system boot up flow and the other for read/program operation when system is ready. Only one state machine controls OTP at a time. After boot up the boot up flow control circuit will be clock gated and reduce power consumption.

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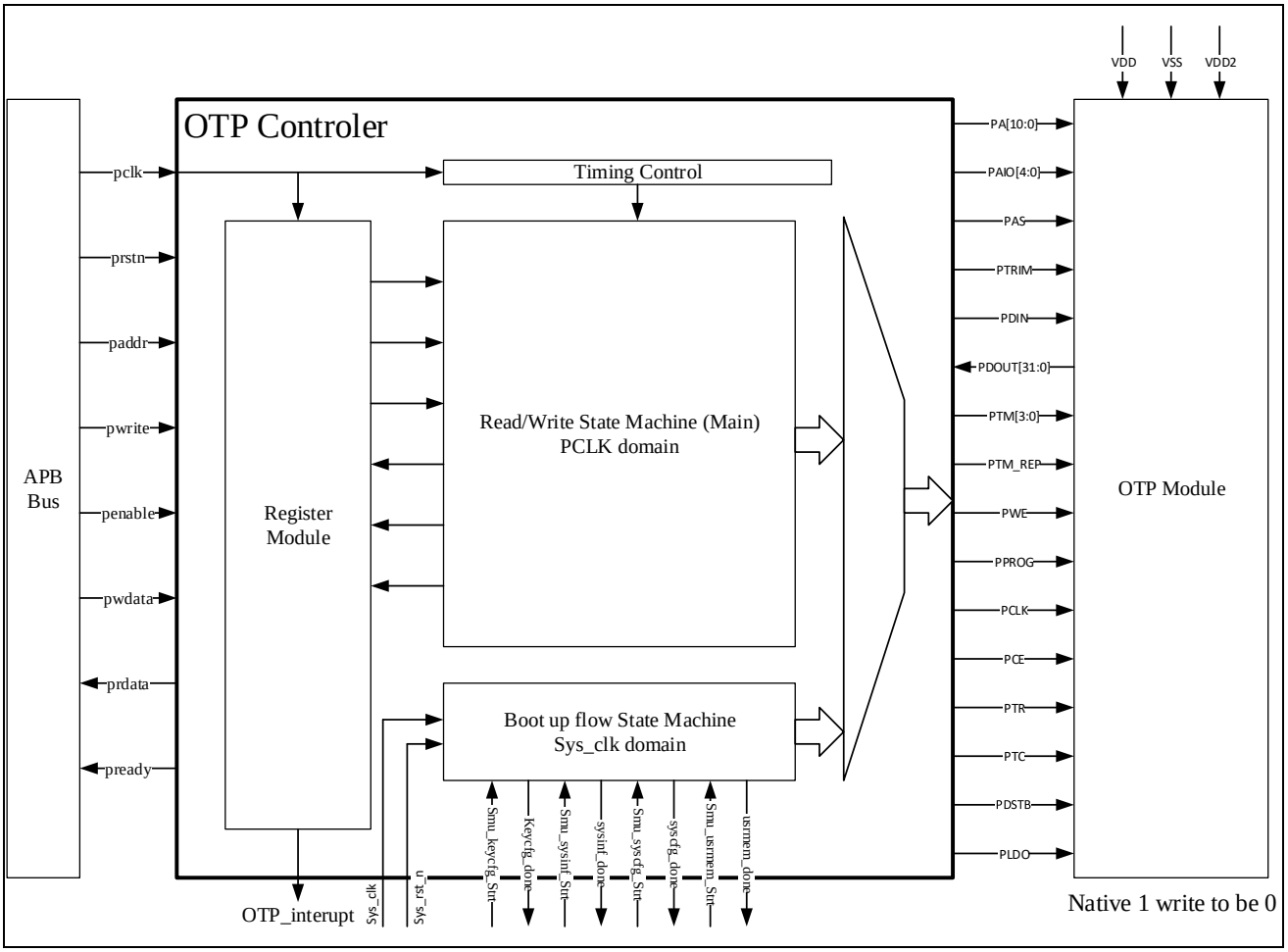
Figure 9-2 OTPC Block level control diagram



When system boot up, OTPC mainly use system clock (up to 64 MHz) to conduct reading. For read/program operation issued by program APB register, the operation is running at APB clock (up to 300 MHz). These two parts of circuit generates PCLK for OTP module by build in pre-scalar. Following parts of this manual introduce details of OTPC circuit.

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9.3.1 Application Information

This section describes certain software restrictions when accessing the MU.

9.3.1.1 OTPC Clock Division

There are two clock input to OTPC module, sys_clk and pclk. For OTP, the maximum read frequency is 20 MHz and some control signal setup time is up to microsecond level. Sys_clk only be used when system booting up and the frequency is around 64 MHz during boot up. APB clock is up to 300 MHz and can be adjustable. Clock pre-scaling method is different for sys_clk and APB clock.

9.3.1.1.1 Normal Operation Clock Division

For read/write operation under APB clock domain have two clock dividers. Those clock dividers are related to OTPC_USC register configurations. The pre-scalar diagram is shown in Figure 9-3. The four MSB of OTPC_USC register will be used as read clock generation and according to equation below, the generated clock won't have frequency higher than 16 MHz.

$$OTPC_USC[7:0] = OTPC_USC[7:4] * 16 + Y = X * 16 + Y$$

$$\frac{f_{pclk}}{OTPC_USC[7:0]} = 1\ MHz\ (1\ us) = \frac{f_{pclk}}{X * 16 + Y}$$

$$f_{pclk} = (X * 16 + Y)\ MHz$$

$$\frac{f_{pclk} - Y}{X} = 16\ MHz$$

$$\frac{f_{pclk}}{X} = \left(16 + \frac{Y}{X}\right)\ MHz\ (\text{worst case: X = 1（X != 0）, Y = 15（max）, 31 MHz})$$

$$f_{rclk} = \frac{f_{pclk}}{2(USC[7:4] + 1)} = \frac{f_{pclk}}{2(X + 1)} < \left(8 + \frac{Y}{2X}\right)\ MHz\ (\max 15.5\ MHz) < 20\ MHz$$

Clock pre-scalar generates microsecond signal based on OTPC_USC register and use it to decide transactions of state machine. The timing can be change alter the value in OTPC_USC register. Since OTPC_USC register value is the same as clock frequency, the counter just simply counts from 0 to OTPC_USC value to get 1 us frequency signal.

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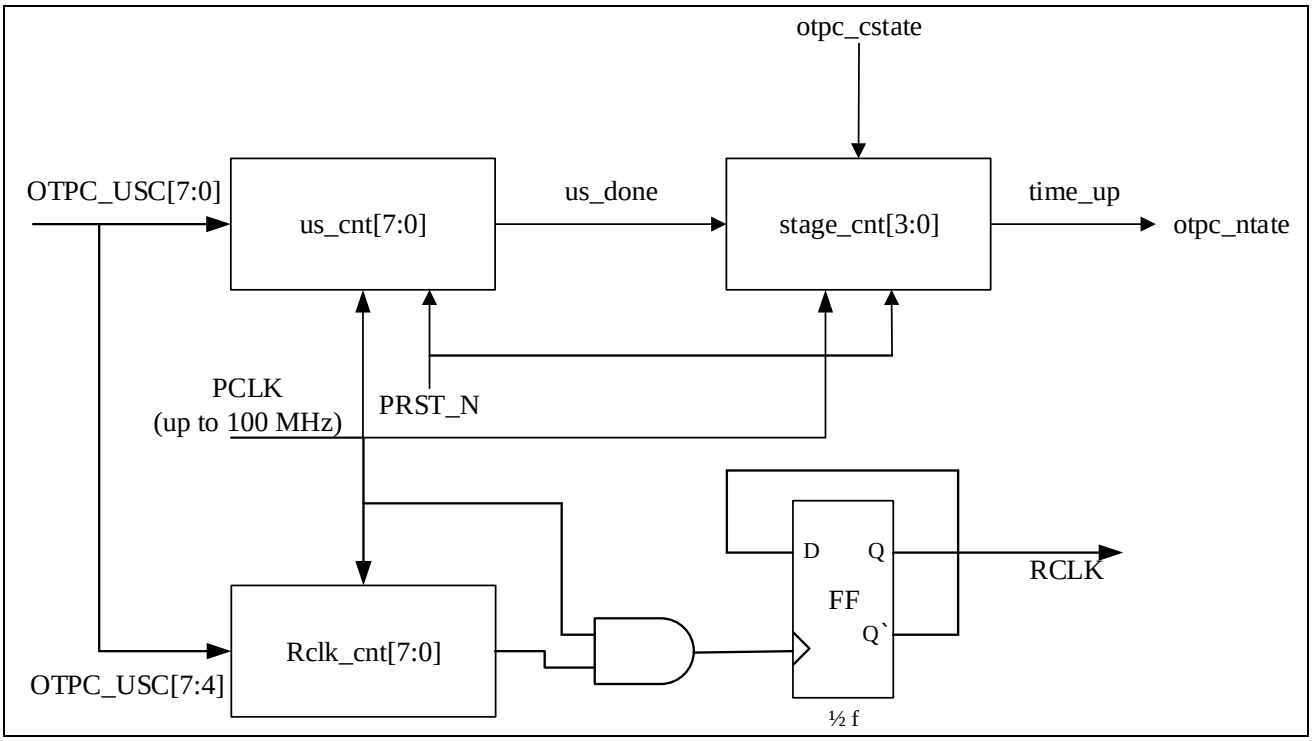
Figure 9-3 Clock pre-scalar block diagram in APB clock domain



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9.3.1.1.2 Valid Tag and Unused Tag

The first part of data OTPC will read is the valid tag for multi-copy system configuration region and unused tags for single copy system configuration region and reserved region. This is because we need the valid information for system configuration region to retrieve correct copy of data. This region is not encrypted. This is because encryption will make information lost and protection make this valid tag unable to program for a second time.

There are eight configurations in system configuration region which has 16 copies. Hence, each of those configurations can be program for 16 times. Each valid tag has 16 bits ([15:0]) and one bit represents one copy for this configuration. Examples for Valid tag and corresponding program and read address are shown as Table 9-2. When OTPC reading this part of system configuration (address range from *refer to NVR table file*), OTPC only gets the valid copy value according to the Valid tag for the configuration.

Table 9-2 Examples of valid tag and read/program address

Valid tag	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NO.1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Valid tag is all 1, no valid copy，Read Address = Config Base Address，Program Address = Config Base Address															
NO.2	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
	5 copies have been program to this configuration.Read Address = Config Base Address + 0x4.Program Address = Config Base Address + 0x5.															
NO.3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	All copies have been program to this configuration.Read Address = Config Base Address + 0xf.Program Reject.															

Unused tag only represents if corresponding word has been programmed or not. One-bit unused tag covers one word in the rest of 256 words in user memory region. Unused tags are store in word base. Example of unused tag is shown in Table 9-3. This unused tag only prevent user to do second program to the same word. Second program will trigger OTPC_STS.PGE.

Table 9-3 Example of unused tag protection

	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Unused tag	1	0	0	1	0	0	0	1	1	0	1	0	1	1	1	1
Address	0x30f	0x30e	0x30d	0x30c	0x30b	0x30a	0x309	0x308	0x307	0x306	0x305	0x304	0x303	0x302	0x301	0x300
Access	RW	RO	RO	RW	RO	RO	RO	RW	RW	RO	RW	RO	RW	RW	RW	RW

After system boot up, these valid tags and unused tags information will be store in registers under APB clock domain. When user issues read operation, OTPC reads to the valid copy. When user program address covered by unused tag or valid tag, it will also program the unused tag/valid tag. User don't have access to the valid tag region. They can check the valid tag/unused tag register to make sure the next program is legal.

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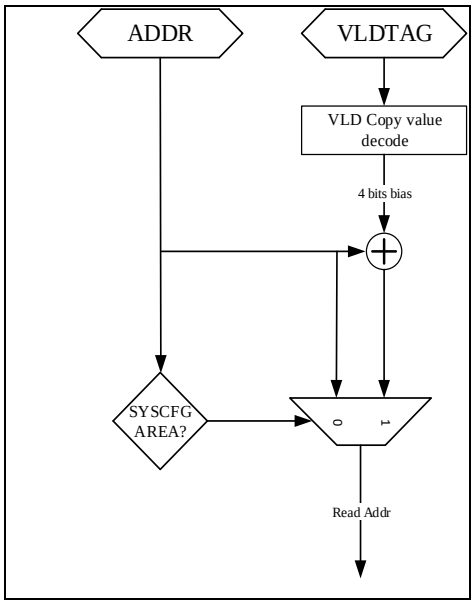
9.3.2 OTPC Read Control

User can issue a read request by setting OTPC_CTRL.PRMD to 0 then program OTPC_ADDR. After that OTPC checks if current mode has access to this particular address. OTPC USER mode is load from system configuration region and store in APB clock domain.

If the read address is in multi-copy system configuration region, OTPC decode the valid address for this configuration and pass to OTPC read address to read address register (shown in Figure 9-4).

Figure 9-4 Read address calculation logic



OTPC state machine and OTPC conducts two read operations are shown in Figure 9-5.

Figure 9-5 OTPC read state machine and timing 1

OTPC pass the data to register file and give a read done signal. OTPC decryption logic uses OTPC key to decrypt read out data and store inside OTPC_RDATA register. If this region is not encrypted (valid tag/unused tag). It will store the original read out value in the register.

For multi replica system configuration areas, OTPC only reads the latest valid replica address and decodes using the valid replica address. For example, OTPC_SCJVLD.USR_NVR-VLD[15:0]=0x0000FFF0, indicating that the SEC_JTAG user configuration has already written 4 valid data, regardless of whether the read address is 0x310 or 0x31F, currently only data at address 0x313 will be read.

9.3.2.1 Read UCID

The UCID is 128 bits and follows the definition of national technology chip serial numbers. It contains information related to chip production and version. The information it contains is written at the factory and guaranteed to be unique to any MCU microcontroller in any situation. User applications or external devices can read it through the OTPC interface and cannot be modified.

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UCID Address: 0x0238, occupying 16 bytes

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9.3.3 OTPC Program Control

To issue a program request, user needs to unlock OTPC_CTRL register by program correct keys in correct order to OTPC_KEY register and write OTPC_CTRLPRMD bit to 1. Then program the OTPC_WDATA register for the program value and issue program request by writing the program address to OTPC_ADDR register. OTPC register module gives program information to OTPC module after request has been accepted. This includes program address and program data after encode.

In OTPC register module, it checks if the program address is valid or not. In USER mode, user can program system config and user memory area only. Program to area outside this range will trigger WRPE in OTPC_STS register. If user program address that is protected by valid tag or unused tag but all valid copies have been programmed then it will trigger PGE in OTPC_STS register. Depending on which region the program address is located at, there are three program scenarios:

- Unused area of user memory:

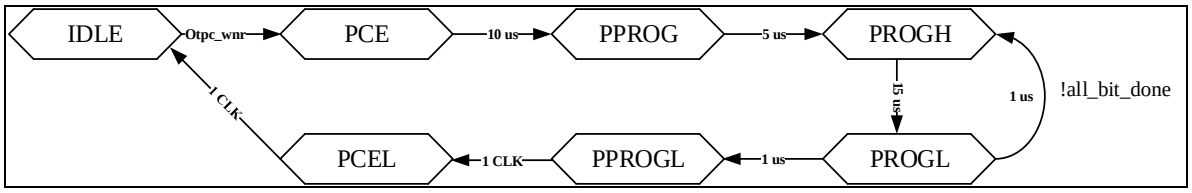
- Addresses from 0x500 to 0x5ff only store data and have no specific meaning. Each address can only be written once, and whether the corresponding address can be written can be checked through the OTPC_UMUUx register.

- NVR User Configuration Area:

- The addresses range from 0x300 to 0x3CF, and each user configuration corresponds to 16 replicas, occupying 0x10 addresses, and can only be programmed by calling the BOOT API. The current valid tag value and the remaining number of writable copies can be viewed through the OTPC-xxVLD register. For detailed descriptions of the meaning of each address, please refer to section 10.4.1.2.

OTPC receives program request, address and data from register module, then it will start the program sequence. State machine of OTPC program procedure is shown in Figure 9-6. For each bit program in OTP, OTPC needs to program twice, with PAS = 0 and 1 (for redundant program). Valid tag/unused tag program only programs one bit.

Figure 9-6 OTPC program state machine



OTPC register module provides data program address, program data, valid tag/unused tag address, program position. Figure 9-7 illustrates address provide to OTPC module.

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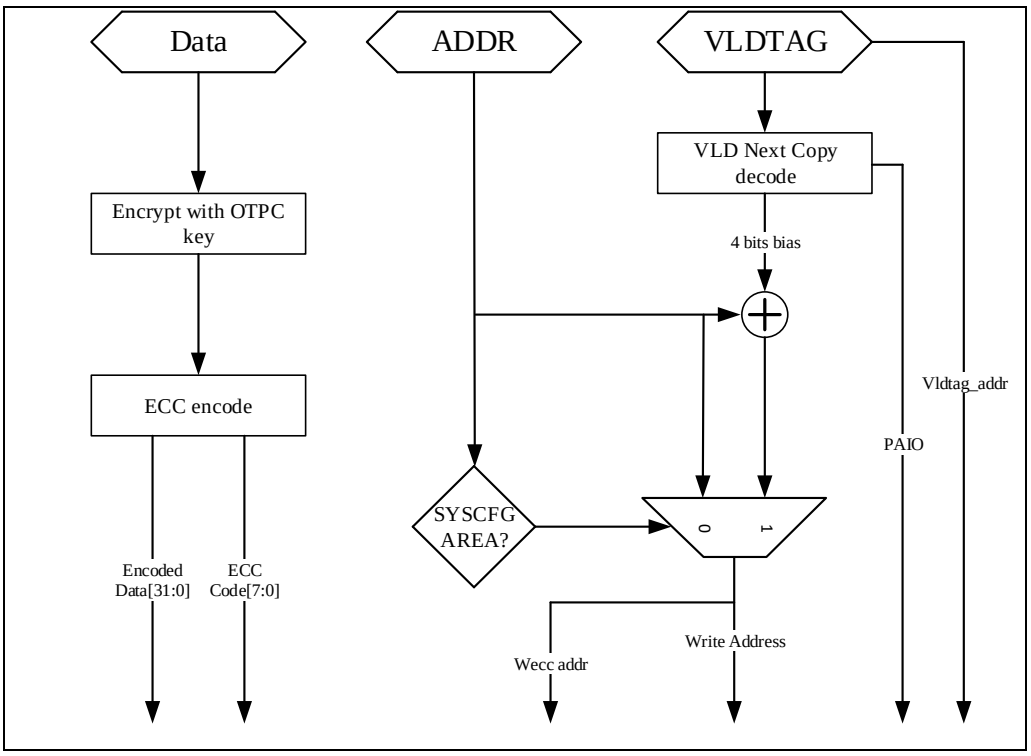
Figure 9-7 Program signals provided to OTPC by OTPC register module



After receiving program related data, OTPC will starts program OTP. When OTPC programmed valid tag/unused tag, OTPC handshakes with OTP register module and update shadow register for valid tag and unused tag. This can make sure even if OTPC stops when data is half program, this word will be marked as programmed and won't be able to program again.

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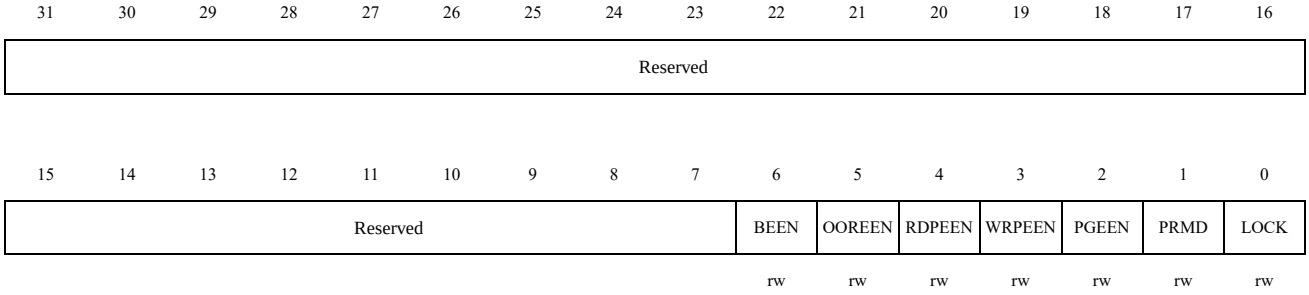
9.4 OTPC Registers

9.4.1 OTPC Control Register (OTPC_CTRL)

Address offset: 0x00

Reset value: 0x0000 0001



Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	BEEN	BUSYERR output interrupt Enable 0: Disable 1: Enable
5	OOREEN	OORERR output interrupt Enable 0: Disable 1: Enable
4	RDPEEN	RDPRTERR output interrupt Enable 0: Disable 1: Enable
3	WRPEEN	WRPRTERR output interrupt Enable 0: Disable 1: Enable
2	PGEEN	PGERR output interrupt Enable 0: Disable 1: Enable
1	PRMD	Program mode switch Software can set or clear this bit 0: OTP next address operation is read 1: OTP next address operation is write
0	LOCK	OTP control regsiter lock. Software can only set this bit. Hareware resets this bit when software unlock with correct sequence. Any unsuccessful unlock operation will lead to this bit remains set until the next reset 0: OTPC_CTRL register is unlock

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Bit Field	Name	Description
		1: OTPC_CTRL register is locked, can't be write

9.4.2 OTPC Status Register (OTPC_STS)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									BE	OORE	RDPE	WRPE	PGE	KEYE	BUSY
									rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	r	r

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	BE	Busy request error This bit is set by hardware when user issued a request when OTPC is busy with last operation. Software can clear this bit by writing 1
5	OORE	Read/write out of access range error This bit indicates last operation is out of access range of OTP, hardware sets this bit when user issued a out of range request. Software can clear this bit by writing 1 to this bit
4	RDPE	Read protection error This bit is set by hardware when user try to read read protected region like key or reaserved area. Software clears this bit by writing 1
3	WRPE	Write protection error This bit will be set when User try to write to protected region (in user mode, region like system information, reserved area can't be program). Software writes 1 to clear this bit
2	PGE	Program error This bit indicates therer is a program error Program unused bit protected region for second time. Or program multicopy configuration more than 16 times Software writes 1 to clear this bit
1	KEYE	Key error This bit inidcates error key has been provided to OTPC when unlocking CR register. User can only retry unlock process after reset
0	BUSY	Busy current operation is on going, any write opeartaion to related register will be

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Bit Field	Name	Description
		ignore. User should issue new operation after BUSY bit become 0

9.4.3 OTPC KEY Register (OTPC_KEY)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY[15:0]															
w															

Bit Field	Name	Description
31:0	KEY[31:0]	Key Value register User can write keys in correct order to unlock OTPC KEY 1: 0x45670123 KEY 2: 0xCDEF89AB

9.4.4 OTPC Microsecond Control Register (OTPC_USC)

Address offset: 0x0c

Reset value: 0x0000 012f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							VAL[8:0]								
							rw								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	VAL[8:0]	1us count number AHB clock frequency scale to 1 us, AHB clock maximum is 300 MHz. defalut is 300 to make sure even without change this value user can still do read or write correctly

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9.4.5 OTPC Operate Address Register (OTPC_ADDR)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR[31:0]	Address for operation. Writing to this regsiter will trigger operation according to OTPC_CTRL.PRMD bit value. Hence this register should be program last

9.4.6 OTPC Read Data Register (OTPC_RDATA)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAT[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
r															

Bit Field	Name	Description
31:0	DAT[31:0]	Read data value will be store in this register. After issue a read operation, user needs to wait until BUSY bit in OTPC_STS regsiter clear then read this register, otherwise this register value corresponds to last read operation

9.4.7 OTPC Write Data Register (OTPC_WDATA)

Address offset: 0x18

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAT[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
rw															

Bit Field	Name	Description
31:0	DAT[31:0]	Write data value indicates data that user wants to program into OTP. This data should be write before address.

9.4.8 OTPC User Config Valid of SEC_JTAG Register (OTPC_SECJVLD)

Address offset: 0x20

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.9 OTPC User Config Valid of SEC_MODE Register (OTPC_SECMDVLD)

Address offset: 0x28

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.10 OTPC User Config Valid of RDP2 Register (OTPC_RDP2VLD)

Address offset: 0x30

Reset value: 0x0001 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.11 OTPC User Config Valid of BTM Register (OTPC_BTMVLD)

Address offset: 0x38

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.12 OTPC User Config Valid of BOR Register (OTPC_BORVLD)

Address offset: 0x3C

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.13 OTPC User Config Valid of IWDG Register (OTPC_IWDGVLD)

Address offset: 0x40

Reset value: 0x0000 ffff

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.14 OTPC User Config Valid of TCM Size Register (OTPC_TCMSZVLD)

Address offset: 0x44

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.15 OTPC User Config Valid of JTAG Key Register (OTPC_JTAGKVLD)

Address offset: 0x50

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Reset value: 0x0001 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.16 OTPC User Config Valid of REK Unitx Register (OTPC_REKUxVLD，x = 1~4)

Address offset: 0x54+4*(x-1)

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

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9.4.17 OTPC User Config Valid of IDK Unitx Register (OTPC_IDKUxVLD，x = 1~4)

Address offset: 0x64+4*(x-1)

Reset value: 0x0000 ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USR_NVR_VLD[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	USR_NVR_VLD[15:0]	Multi-Copy valid tag value. Number of 1 represents how many times of program left for this area. Maximum program time is 16 times. OTPC after boot up flow it will load from OTP. This tag changes from LSB to MSB with each times of program All 1 means no valid copy. MSB 0 indicates valid copy position. All 0 means no longer programable

9.4.18 OTPC USER Memory unused flag Register (OTPC_UMUUx, x=0~7)

Address offset: 0x74+ 4*x，form 0x74 to 0x90

Reset value: 0xffff ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UU[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UU[15:0]															
r															

Bit Field	Name	Description
31:0	UU[31:0]	USER Memory region unused tage: region 0~31 words 1: unused, can programe 0: used, write protect

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Bit Field	Name	Description
		Note: Each ***x*** represents 32 words. Total 256-words

9.4.19 OTPC Debug Port 1 Register (OTPC_CRLD1)

Address offset: 0xb8

Reset value: 0x3fff 00ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		NRIWDG[13:0]													
		r													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	BOR[2:0]			Reserved								SJTAG[3:0]			
	r											r			

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:16	NRIWDG[13:0]	Valid SYS_CFG_NRST_IWDG_OTP payload data. OTPC Only after boot up flow it will load from OTP.
15	Reserved	Reserved, the reset value must be maintained.
14:12	BOR[2:0]	Valid SYS_CFG_BOR_OTP payload data OTPC Only after boot up flow it will load from OTP
11:4	Reserved	Reserved, the reset value must be maintained
3:0	SJTAG[3:0]	Valid SEC_JTAG_CFG_OTP payload data OTPC Only after boot up flow it will load from OTP

9.4.20 OTPC Debug Port 2 Register (OTPC_CRLD2)

Address offset: 0xbc

Reset value: 0xffff 913f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			L2MD	L1MD	L0MD	ROOTMD	INITMD	Reserved		TCMSZ[5:0]					
			r	r	r	r	r	r		r					

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Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	L2MD	Chip mode state OTPC Only after boot up flow it will load from OTP
11	L1MD	Chip mode state OTPC Only after boot up flow it will load from OTP
10	L0MD	Chip mode state OTPC Only after boot up flow it will load from OTP
9	ROOTMD	Chip mode state OTPC Only after boot up flow it will load from OTP
8	INITMD	Chip mode state OTPC Only after boot up flow it will load from OTP
7:6	Reserved	Reserved, the reset value must be maintained
5:0	TCMSZ[5:0]	Valid TCM_SZ_CFG_OTP payload data

10 System Security

10.1 Introduction

As security requirements generally vary from application to application, N32Hxxx incorporates a range of security features that help to protect their secure resources such as firmware, keys, security certificates, etc.

Different set of features can be used to protect against different kinds of attack. They are designed to be configured for different security levels depending on protection needs in different stages in the product lifecycle.

In addition, N32Hxxx provide a general-purpose accelerator that improves the performance of selected cryptographic algorithms.

This section explains different security features available on the N32Hxxx devices.

10.2 Main Security Features

The main security features are shown below:

- Secure boot with encrypted Boot ROM
- Secure firmware download
- Flexible secure region partitioning
  - Flash secure region
  - RTAD custom-secure region
  - Program Firmware Only Execution Region (PFOER) for execute-only firmware protection

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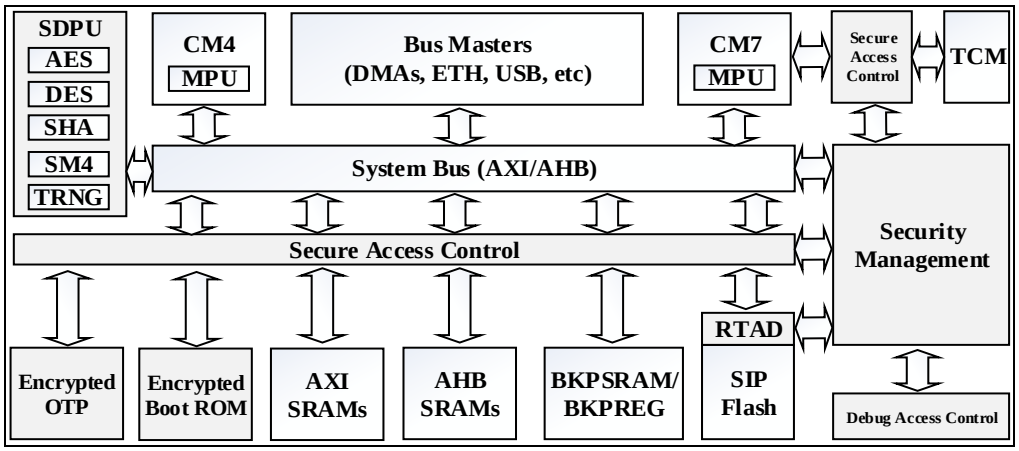
- TCM user secure regions
- SRAM user secure regions

- Flexible lifecycle security scheme with Global Read Protection (RDP)
- SIP Flash Write Protection (WRP)
- Real Time AES Decryption (RTAD) for SIP Flash
- Secure On-chip One-Time Programmable Controller (OTPC) with on-chip OTP array
- Secure debug control for JTAG/SWD
- Cryptographic Accelerators (AES, DES, SM4, SHA)
- Random Number Generator (TRNG)
- Tamper protection against voltage, temperature and clock attacks

10.3 System Security Architecture

Figure 10-1shows a simplified diagram of the security architecture:

Figure 10-1 N32Hxxx System Security Architecture



On top of the ARMv7-M security mechanisms in Cortex-M7 and Cortex-M4 using respective core's MPU, N32Hxxx devices come with an extensive range of security features that gives software developers more flexibility to secure their code and assets in many memories against different kinds of attack across the product lifecycle.

This is enabled by a security management unit that employs different security mechanisms (RDP/WRP/PFOER) to protect memories (ROM/RAM/OTP) and backup registers against unauthorized transactions coming from other masters than the two CPUs. Security configurations can be programmable by secure code using option bytes.

Additionally, encryption and decryption are employed to protect secure regions such as BOOT ROM, SIP Flash, and OTP. Security keys are stored and protected in OTP. RTAD keys can be programmable by user code.

Nevertheless, a Security Data Processing Unit provides several industry-standard cryptographic hardware

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accelerators including AES/DES/SHA/SM4.

N32Hxxx also supports secure boot with encrypted Boot ROM and secure firmware installation and update.

10.4 Security Feature Description

10.4.1 Option Bytes

10.4.1.1 Flash Option Bytes

The SIP Flash memory includes a set of non-volatile option bytes that defines the security configuration of the chip. They are loaded at power-on reset or system reset. They can be read and modified only through call BOOT API.

These option bytes are configured by the end-user depending on the application requirements. Some option bytes might have been initialized during manufacturing stage.

Flash Option Byte Organization

Table 10-1 shows the Flash option byte organization. The following describes the use of the option bytes.

Table 10-1 Flash Option Byte Organization

Offset	Name	Bit Field	Field Name
0x0000	RDP	[7:0]	RDP1
		[15:8]	nRDP1
		[23:16]	Reserved
		[31:24]	Reserved
0x0004	WRP	[0]	Reserved
		[31:1]	WRP
0x0008	nWRP	[0]	Reserved
		[31:1]	nWRP
0x000C	M7_BOOTADDR	[31:0]	M7_BOOTADDR
0x0010	M4_BOOTADDR	[31:0]	M4_BOOTADDR
0x0014	ENCRYPTION	[15:0]	CRYPTION_LVL
0x0016	SEC_MODE	[15:0]	SEC_MODE
0x0018	SEC_CFG1	[31]	DMES1
		[30:29]	Reserved
		[28:16]	SEC_END1
		[15:13]	Reserved
		[12:0]	SEC_BEGIN1
0x001C	Reserved	[31:0]	Reserved
0x0020	PFOER_CFG1	[31]	DMEP1
		[30:29]	Reserved
		[28:16]	PFOER_END1
		[15:13]	Reserved
		[12:0]	PFOER_BEGIN1

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0x0024	Reserved	[31:0]	Reserved
0x0028	Reserved	[31:0]	Reserved
0x002C	CRC	[31:0]	CRC

Flash Option Byte Description

- RDP: used to define the RDP protection level. Refer to Section 10.4.5.2 for more details.
- WRP/nWRP: write protection option for Flash. Refer to Section 10.4.6 for more details.
- M7_BOOTADDR: defines the executing or storing address of Cortex-M7 user code depending on CRYPTION_LVL. If encryption is not enabled, this is the executing address as well as storing address of Cortex M7 user code. However, when encryption is enabled, this is only the storing address and the executing address must be defined in the Flash user configuration table (EXE_ADDR_M7).
- M4_BOOTADDR: defines the executing address of Cortex-M4 user code.
- CRYPTION_LVL: Encryption level definition
  - 0xFFFF: No Encryption (Default)
  - 0xE00B: Encryption + No Binding
  - 0xEBEB: Encryption + Binding
  - Others: No Encryption
- SEC_MODE: this non-volatile option can be used by the application to manage secure access mode, as described in Section 10.4.2.
- SEC_CFG1: Flash secure region definition (Refer to Section 10.4.4.1 for more details)
  - SEC_BEGIN1: Flash secure region start address
  - SEC_END1: Flash secure region end address
  - DMES1: when set to 1, the secure region can be erased during a RDP protection level regression or an approved mass erase
- PFOER_CFG1: Flash PFOER region definition (Refer to Section 10.4.4.2 for more details)
  - PFOER_BEGIN1: PFOER region start address
  - PFOER_END1: PFOER region end address
  - DMEP1: when set to 1, the PFOER region can be erased during a RDP protection level regression or an approved mass erase
- CRC: this is CRC calculation for Option byte region, used for verification purposes.

10.4.1.2 OTP Option Bytes

Table 10-2 shows the OTP option byte organization. Only 16 modifications are allowed for OTP option bytes. The following describes the use of the option bytes.

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Table 10-2 OTP Option Byte Organization

OTP Region	Option Bytes	Bit Alignment	OTP address
OB1_OTP_INFO	RESERVED	RESERVED	0x0300
	SEC_JTAG _CFG_OTP	{12'hfff, SEC_JTAG _CFG_OTP_bakn[3:0], 12'h0, SEC_JTAG _CFG_OTP[3:0]}	0x0310
	RESERVED	RESERVED	0x0320
	SEC_MODE_OTP	{SEC_MODE_OTP_bakn[15:0], SEC_MODE_OTP[15:0]}	0x0330
OB2_OTP_INFO	RESERVED	RESERVED	0x0340
	RDP2_OTP	{nRDP2_OTP_bakn[7:0], RDP2_OTP_bakn[7:0], nRDP2_OTP[7:0], RDP2_OTP[7:0]}	0x0350
	RESERVED	RESERVED	0x0360
OB3_OTP_INFO	SYS_CFG_BTM_OTP	{SYS_CFG_BTM_OTP_bakn[15:0], SYS_CFG_BTM_OTP[15:0]}	0x0370
	SYS_CFG_BOR_OTP	{13'h1fff, SYS_CFG_BOR_OTP_bakn[2:0], 13'h0, SYS_CFG_BOR_OTP[2:0]}	0x0380
	SYS_CFG_NRST_IWDG_OTP	{2'b11, SYS_CFG_NRST_IWDG_OTP_bakn[13:0], 2'b0, SYS_CFG_NRST_IWDG_OTP[13:0]}	0x0390
	TCM_SZ_CFG_OTP	{10'h3ff, TCM_SZ_CFG_OTP_bakn[5:0], 10'h0, TCM_SZ_CFG_OTP[5:0]}	0x03a0
	RESERVED	RESERVED	0x03b0
	RESERVED	RESERVED	0x03c0

OTP Option Byte Description

- SEC_JTAG _CFG_OTP: JTAG Configuration
  - 1111/1001: JTAG/SWD allowed
  - others: JTAG/SWD disabled
- SEC_MODE_OTP: this non-volatile option can be used by the application to manage secure access mode, as described in Section 10.4.2.
  - 0xE5CE: Enable
  - others: Disabled
- RDP2_OTP: used to define the RDP protection level. Refer to Section 10.4.5.2 for more details.
- SYS_CFG_BTM_OTP: Boot mode configuration
  - 16'h5AA5: Boot from Flash
  - 16'h4884: Boot from serial interface
  - Others: boot mode determined by BOOT0
- SYS_CFG_BOR_OTP: brownout voltage level option, refer to PWR section for more details.
- SYS_CFG_NRST_IWDG_OTP: NRST and watchdog management option
  - nRST_STOP_C_M7(bit13)/nRST_STOP_C_M4(bit12): active low, system reset is generated when entering respective Cortex-M7 and Cortex-M4 stop0/stop2 modes; Automatic reset (0), non automatic reset (1).

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- nRST_STDBY_C_M7(bit11)/nRST_STDBY_C_M4(bit10): active low, system reset is generated when entering respective Cortex-M7 and Cortex-M4 standby modes; Automatic reset (0), non automatic reset (1).
- IWDG_SW_M7(bit9)/IWDG_SW_M4(bit8): Hardware (0) or software (1) watchdog control selection
- IWDG_STOP0_M7(bit7)/IWDG_STOP0_M4(bit6): IWDG1 (Cortex-M7) and IWDG2 (Cortex-M4) active in respective CPU STOP0 mode if 1, freeze if 0.
- IWDG_STOP2_M7(bit5)/IWDG_STOP2_M4(bit4): IWDG1 (Cortex-M7) and IWDG2 (Cortex-M4) active in respective CPU STOP2 mode if 1, freeze if 0.
- IWDG_STANDBY_M7(bit3)/IWDG_STANDBY_M4(bit2): IWDG1 (Cortex-M7) and IWDG2 (Cortex-M4) active in respective CPU standby mode if 1, freeze if 0.
- IWDG_SLEEP_M7(bit1)/IWDG_SLEEP_M4(bit0): IWDG1 (Cortex-M7) and IWDG2 (Cortex-M4) active in respective CPU sleep mode if 1, freeze if 0.

■ TCM_SZ_CFG_OTP: TCM Size configuration.

- There is 1M SRAM available for TCM allocation, please refer to Table 10-3 Embedded SRAM for details.

Table 10-3 TCM Size Configuration Table

TCM_SZ_CFG_OTP	ITCM Size(KB)	DTCM Size(KB)	SRAM Size(KB)
0	1024	0	0
1	896	128	0
2	768	256	0
3	640	384	0
4	512	512	0
5	384	640	0
6	256	768	0
7	128	896	0
8	0	1024	0
9	896	0	128
10	768	128	128
11	640	256	128
12	512	384	128
13	384	512	128
14	256	640	128
15	128	768	128
16	0	896	128
17	768	0	256
18	640	128	256
19	512	256	256
20	384	384	256
21	256	512	256
22	128	640	256

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23	0	768	256
24	640	0	384
25	512	128	384
26	384	256	384
27	256	384	384
28	128	512	384
29	0	640	384
30	512	0	512
31	384	128	512
32	256	256	512
33	128	384	512
34	0	512	512
35	384	0	640
36	256	128	640
37	128	256	640
38	0	384	640
39	256	0	768
40	128	128	768
41	0	256	768
42	128	0	896
43	0	128	896
44~63	0	0	1024

10.4.1.3 Option Byte Modification

Option bytes can only be modified by secure library code. An option byte change operation can be used to modify the configuration and the protection settings saved in the non-volatile option byte area of SIP Flash or OTP.

The secure management module features two sets of option byte registers:

- The first register set contains the current values of the option bytes. Their values are loaded by secure library code from Flash or OTP after power on reset, system reset or wakeup from system standby mode.
- The second register set allows the modification of the option bytes.

Users are required to call secure library for modification.The user application needs to check the outcome of the operation through the return value from the operation. If it is not successful, the user application can check what was wrong in their configuration.

Unlocking the Flash option byte modification

After reset, the MMU_STS.OBL bit is set to 1 and the Flash option byte is locked. As a result, the application software must call BOOT API to unlock the option configuration register before attempting to change the option bytes. MMMU_STS.OBL bit is now cleared and Flash Option byte is unlocked.

Any wrong sequence locks up the corresponding register/bit until the next system reset, and generates a bus error.

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Unlocking OTPC_CTRL register

Similarly, an unlocking sequence is required before users can program OTP option byte. Refer to OTPC chapter.

Option byte modification sequence

To modify user option bytes, follow the sequence below:

- Unlock sequence
  - For Flash option byte modification: Unlock Flash option byte modification using BOOT API, unless the register is already unlocked.
  - For OTP option byte modification: Unlock OTPC_CTRL by writing correct key sequence to OTPC_KEY register, unless the register is already unlocked.
- Call secure library to modify the Flash/OTP option bytes accordingly
- Wait until the API is done and check the status

10.4.2 Secure Boot

Secure boot in BOOT ROM is a protected code that is always executed after a system reset. As a root of trust, this code checks the chip security configurations and activates respective run-time protections, reducing the risk of malwares that can run on the chip. Secure boot also authenticates the next level firmware before executing it.

10.4.3 Secure Firmware Install

Secure firmware install is an immutable secure service embedded in SECURE BOOT ROM. It allows secure installation of OEM firmware in untrusted production environment (such as OEM contract manufacturer).

The confidentiality of the installed images written either in internal SIP Flash memory or encrypted in external Flash memory is also protected, using AES.

Note that secure firmware update is not supported and required to be done by customer application code.

10.4.4 Flexible Secure Region Partitioning

N32Hxxx allows the configuration of multiple secure regions as follows:

- Flash secure region
- Flash PFOER (Program Firmware Only Execute Region)
- Four user RTAD regions with configurable access levels (execute only, data access only, or normal access)
  - Each region can be encrypted and decrypted with different keys
- User secure region in TCM (for Cortex-M7 only)
- User secure region in SRAM (for Cortex-M4 only)

10.4.4.1 Flash secure region (Cortex-M7 Only)

N32Hxxx allows the definition of a secure-only region in the user area of Flash memory. This region can be accessed

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only while the Cortex-M7 CPU executes secure application code with the SEC_MODE option byte setting to enable. Secure-only regions help isolating secure user code from application non-secure code as shown in Figure 10-2. As an example, they can be used to protect a customer secure firmware upgrade code, a custom secure boot library or a third party secure library.

Flash secure region programming

One secure-only region can be defined in Flash by setting the SEC_END1 and SEC_BEGIN1 in the SEC_CFG1 option byte so that the END address is strictly higher than the BEGIN address. SEC_BEGIN1 and SEC_END1 are defined with a granularity of 4096 bytes.

As an example, to set a secure-only region on the first 32 Kbytes of user bank 1 (i.e. from address 0x1500 0000 to address 0x1500 7FFF, both included), the SEC_CFG1 register must be configured as follows:

- SEC_BEGIN1[12:0] = 0x000
- SEC_END1[12:0] = 0x007

The secure-only region size defined above is equal to:

[(SEC_END1 - SEC_BEGIN1) + 1] x 4096 = 8 x 4096 bytes = 32 Kbytes.

These option bytes can be modified only by the CPU running BOOTROM secure library.

The minimum secure-only area that can be set is 8KB.

Flash secure region properties

- Arm Cortex-M7 debug events are ignored while executing code in this area.
- Only the Arm Cortex-M7 core executing secure library or user secure application can access it (Master ID filtering). In all other cases, accessing the secure-only area is illegal.
- Flash secure region is protected by RDP. Refer to chapter 10.4.5 for more details.
- Illegal transactions to a secure-only region are managed as follows:
    - Data read transactions return all 1s. Data write transactions are ignored. No bus error is generated but an error flag is raised.
- A valid secure-only region can be erase-protected depending on DMES1 option byte configuration. When it's erased-protected, the behavior is as follows:
    - No erase operations to a sector located in this area are possible (including the sector containing the area start address and the end address).
    - No mass erase can be performed if a single valid secure-only region is defined including erase due to RDP level regression

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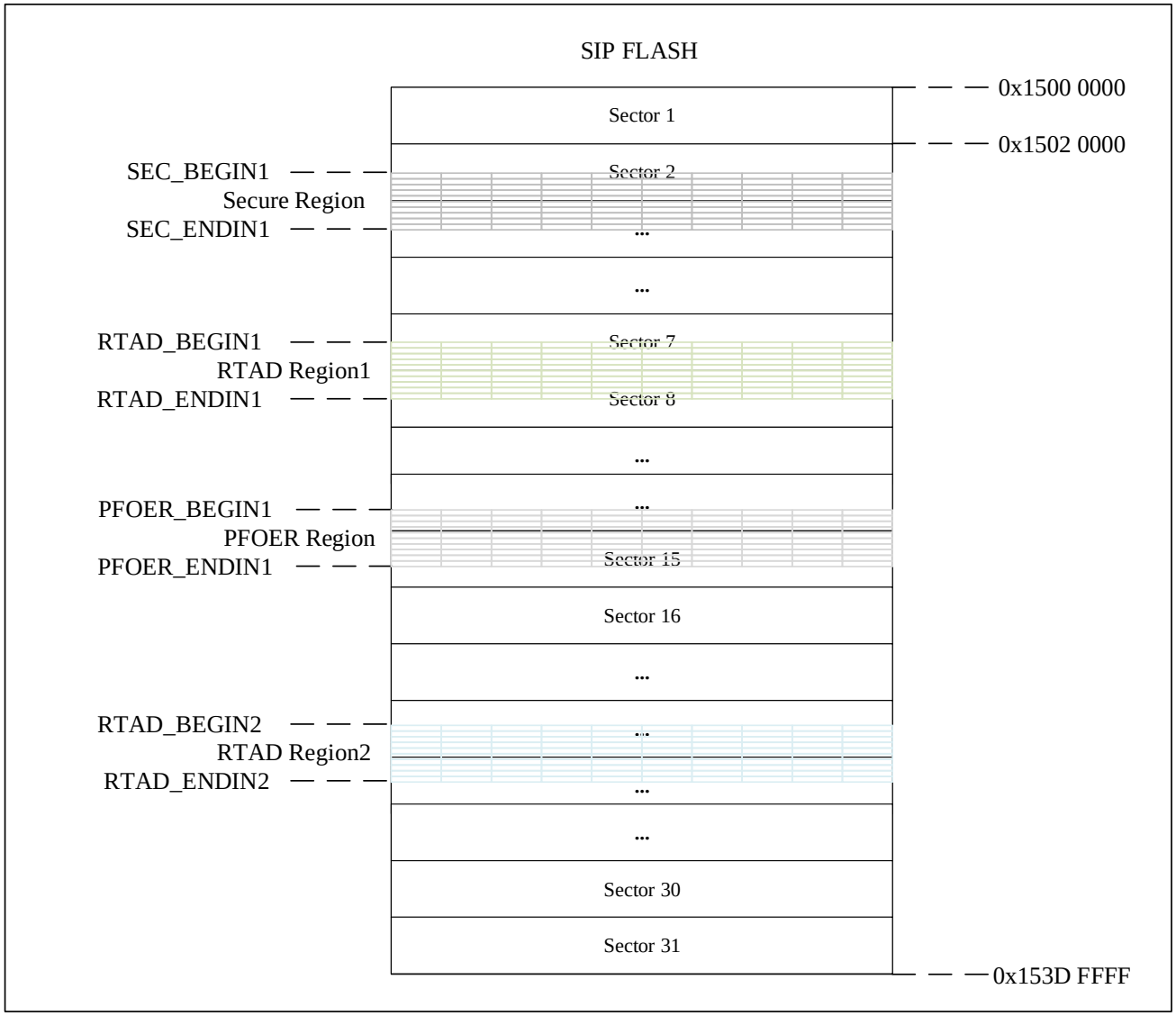
Figure 10-2 Flash secure region partitioning



10.4.4.2 Program Firmware Only Execution Region (PFOER)

N32Hxxx allows the definition of an “executable-only” area in the user area of each Flash memory bank as shown in Figure 10-2. In this area, only instruction fetch transactions from the system are allowed. Even literal load is not allowed. This protection is particularly efficient to protect third party software intellectual property.

Note that Executable-only area usage requires the customer code to be compiled accordingly using “execute-only” option.

PFOER region programming

One PFOER region can be defined in Flash by setting the PFOER_END1 and PFOER_BEGIN1 in the PFOER_CFG1 option byte so that the END address is strictly higher than the BEGIN address. PFOER_BEGIN1 and PFOER_END1 are defined with a granularity of 4096 bytes.

As an example, to set a PFOER region on the first 16 Kbytes of user bank 1 (i.e. from address 0x1500 0000 to address

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0x1500 7FFF, both included), the PFOER_CFG1 register must be configured as follows:

- PFOER_BEGIN1[12:0] = 0x000
- PFOER_END1[12:0] = 0x003

The PFOER region size defined above is equal to:

[(PFOER_END1 - PFOER_BEGIN1) + 1] x 4096 = 4 x 4096 bytes = 16 Kbytes.

These option bytes can be modified only by the CPU running BOOT ROM secure library.

The minimum PFOER area that can be set is 8KB.

Flash PFOER region properties

- Arm Cortex-M7 debug events are ignored while executing code in this area.
- Only the Arm Cortex-M7 core can execute from this region.
- PFOER secure region is protected by RDP. Refer to chapter 10.4.5 for more details.
- Illegal transactions to a PFOER region are managed as follows:
  - Data read transactions return all 1s. Data write transactions are ignored. No bus error is generated but an error flag is raised.
- A valid PFOER region can be erase-protected depending on DMEP1 option byte configuration. When it's erased-protected, the behavior is as follows:
  - No erase operations to a sector located in this area are possible (including the sector containing the area start address and the end address).
  - No mass erase can be performed if a single valid PFOER region is defined including erase due to RDP level regression

10.4.4.3 Flash RTAD Custom Secure Regions

N32Hxxx allows the definition of four RTAD custom-secure regions in the user area of Flash memory as shown in Figure 10-2. Non-secure Flash region is recommended to be defined as RTAD custom secure regions especially when the Flash is external.

RTAD regions are encrypted by 128-bit AES. Decryption is done by RTAD module with software programmable keys (RTAD_KEY1/2/3/4). RTAD_CRC can be used for key verification. Refer to chapter 10.4.7 for more details on RTAD operations.

RTAD Region programming

RTAD custom secure region can be defined in Flash memory by setting RBEG[12:0] and REND[12:0] in MMU_RTR1/2/3/4 registers. User code is required to activate these regions via REN in the MMU_RTADC1/2/3/4 registers.

A nonce is shared for all 4 RTAD regions. It is programmable in the AFIO_XSPI1_DEC_NONCE0/1/2 registers of the AFIO module.

RTAD custom-secure region properties

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The security level of the four RTAD regions can also be set via MMU_RTADC registers involving RPROPERTY and RMOD as follows:

RPROPERTY[1:0]: Region Property. Even when REN=0, RPROPERTY can still be active for this Region.

00: Only instruction fetch is allowed in this Region. Data access is blocked.

01: Only data/literal load is allowed in this region. Instruction fetch is blocked.

1x: both instruction and data accesses are allowed.

RMOD [1:0]: RTAD mode for RTAD Region

00: Only enable decryption for instruction fetch

01: Only enable decryption for data/literal load

1x: do decryption for both instruction fetch and data/literal load

10.4.4.4 TCM Secure Region (Cortex-M7 only)

N32Hxxx allows the definition of a secure-only region in the user area of ITCM memory as shown in Figure 10-3. This region can be executed only by the Cortex-M7 CPU. Note that this is only implemented when encryption is enabled through the option byte CRYPTION_LVL for FLASH and Flash User Configuration Table as shown in Table 10-4 is embedded in the M7_BOOT_ADDR address's Flash content for secure region configuration by secure code.

Table 10-4 Flash User Configuration Table

Offset	Name	Field	Description
0x0000	Header[127:0]	[31:0]:"NSSF" [63:32]:Version [95:64]: Header Size [127:96]:Reserved	NSSF: Identification Tag Version: Version Header Size: 0x100 Reserved
	Nonce_encry[127:0]	NONCE cipher text: [31:0]: always 0 [127:32]:nonce	The low 4 bytes of the NONCE plaintext always remain as 0, the upper 12 bytes are effective.
	rek_encry[127:0]	Encrypted REK	REK key is used to decrypt the encrypted Application.
	app_hash[255:0]	Application Digest	Plaintext application SHA256 digest is encrypted with a public key.
	EXE_ADDR_M7[31:0]	M7 Executing address	Location to execute M7 code
	App_size_M7[31:0]	M7 firmware program size	In bytes
	SaveAddr_M4[31:0]	M4 firmware storing address	Location to execute M4 code
	App_size_M4[31:0]	M4 firmware program size	In bytes
	Reserved	Reserved	Reserved
0x0100	M7 code		Encrypted user code
	M4 code		

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TCM secure region programming

The TCM security zone can be defined in the ITCM by setting EXE-ADDR_M7 to the ITCM memory area in the Flash user configuration table. Configure App_Size_S7 to determine the size of the safe zone, with a maximum of 1MB and a granularity of 4KB. The option byte M7_BOOT_ADDR can be used to specify the location of the secure TCM code in Flash that needs to be copied to ITCM for execution.

These option bytes can be modified only by the CPU running BOOTROM secure library.

TCM Secure region properties

- TCM secure region is protected by RDP. Refer to chapter 10.4.5 for more details.
- Illegal transactions to a secure-only region are managed as follows:
  - Data read transactions return all 1s. Data write transactions are ignored. No bus error is generated but an error flag is raised.

10.4.4.5 SRAM Secure Region (Cortex-M4 only)

N32Hxxx allows the definition of a secure-only region in the user area of SRAM memory as shown in Figure 10-3. Only Arm Cortex-M4 code executing from this region is considered as secure code. Note that this is only implemented when encryption is enabled through the option byte CRYPTION_LVL for FLASH and Flash User Configuration Table as shown in Table 10-4 is embedded in the Flash content for secure region configuration by secure code.

SRAM secure region programming

SRAM safe areas can be defined in AHB SRAM1-5 or AXI SRAM 1-3 by setting SaveAddr_M4 [31:0] in the flash option byte to these SRAM storage areas. Configure App_Size_S4 to determine the size of the safe zone, with a maximum of 1MB and a granularity of 4KB.The M4_BOOTADDR in the Flash user configuration table can be used to specify the location of the secure code in Flash that needs to be copied to SRAM for execution.

These option bytes can be modified only by the CPU running BOOTROM secure library.

SRAM Secure region properties

- SRAM secure region is protected by RDP. Refer to chapter 10.4.5 for more details.
- This is only for Cortex-M4 protected SRAM code. Cortex-M7 CPU running code from this region is considered as non-secure code. Thus, in RDP protection level L1 and L2, Cortex-M7 cannot execute code properly in region as literal load is blocked due to the access from non-secure code to Cortex-M4 secure region.
- Illegal transactions to a secure-only region are managed as follows:
  - Data read transactions return all 1s. Data write transactions are ignored. No bus error is generated but an error flag is raised.

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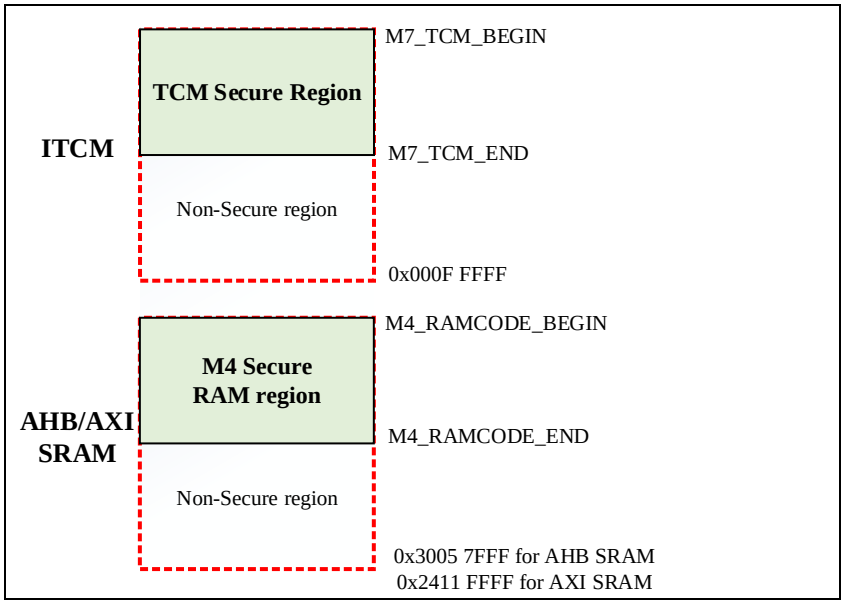
Figure 10-3 Flash secure region partitioning



10.4.4.6 Flexible secure TCM size configuration

For flexibility, software can adjust the sizing and mapping of ITCM, DTCM, AXI SRAM 2 and AXISRAM 3 accordingly. Refer to TCM chapter for more details.

Volatile programming using BOOT API interface

To prevent illegal users from utilizing it for stealing secure code and data, the TCM size configuration is securely checked by SECURE_BOOTROM. TCM_CR register can only be programmable by SECURE_BOOTROM.

Users can program TCM size configuration by calling the BOOT API interface.

Secure code in TCM or AXI SRAM 2 and 3 are erased if TCM size configuration update.

Users can read the status from the TCMC_CTR register to confirm if the size has been updated. Otherwise, users need to check if their configuration is wrong.

Non-Volatile programming using TCM_SZ_CFG_OTP in the OTP

TCM_SZ_CFG_OTP in the OTP can be changed by “Nations MCU Download Tool” when BOOT PIN=1(Serial Download mode). This OTP configuration will be loaded automatically into TCMC_CTR register during power up or system reset.

10.4.5 Lifecycle Security Scheme with RDP

10.4.5.1 Introduction

The global readout protection (RDP) mechanism (full hardware feature) controls the access to the chip debug, test

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and firmware development throughout the product lifecycle, as summarized on Table 10-5. The supported transitions, summarized on Figure 10-4, can be requested (when available) through the debug interface or via the secure code and user applications.

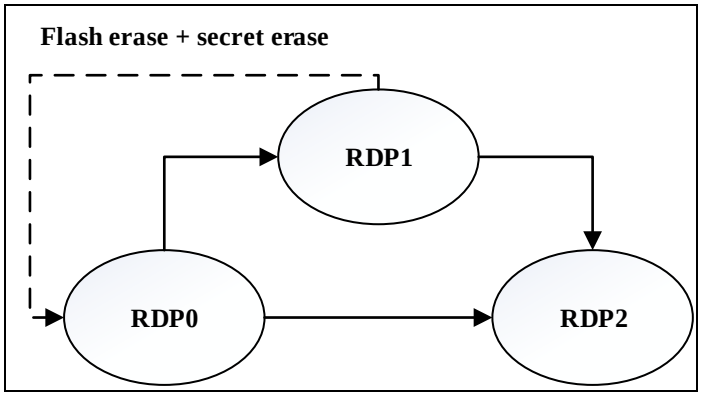
Table 10-5 Product lifecycle security management

RDP Protection Level		Debug	Description
Level 0	Device is open, except protected regions	All regions, except secure regions	Unprotected, except BOOTROM/ BOOTPATCH/OTP/Flash Secure/PFOER code Used for debug, test and development
Level 1	Device memories are protected	Only non-secure SRAM/TCM region	Accesses to Flash memory, secure SRAM/TCM, BKPSRAM and backup registers is not allowed from non-secure downloaded code or debuggers
Level 2	Chip is protected	Disabled	User Level 2 mode is mainly designed for chip protection. Debugger such as JTAG/SWD is disabled. Option byte modification is not allowed. Only option byte read is possible. Hence, downgrading from Level 2 to lower levels is not possible.

According to the RDP protection level, the secure management module restricts unauthorized accesses from illegal users to protected memories (AHBSRAM1-5, BOOTROM, TCM, AXISRAM1-3, BKPRAM, Flash secure code, BOOTPATCH and Flash protected user code) and RTC backup registers. Refer to chapter 10.4.5.2 for more details.

As shown on Figure 10-4, the Flash memory is automatically erased, either partially or in totality, during a RDP regression.

Figure 10-4 RDP transition



10.4.5.2 Global Readout Protection (RDP)

The readout protection (RDP) is global as it does not only apply to the SIP Flash but also to other secure regions such as SRAM, TCM, BOOTROM, OTP and backup registers.

The RDP level is set by writing the values given in Table 10-6 into the RDP option bytes (see Section 10.4.1.3).

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Table 10-6 RDP values for different RDP levels

RDP Level	RDP1	nRDP1	RDP2	nRDP2
L0	0xA5	0x5A	!0xCC	!0x33
L1	!0xA5	!0x5A	!0xCC	!0x33
L2	Don't care	Don't care	0xCC	0x33

Definitions of RDP protection level for each memory

Flash RDP protection definition

Table 10-7 shows the RDP access protection for SIP Flash.

Flash RDP Level 0

Majority of the accesses to the Flash memory are open, except protected regions such as BOOTPATCH, Flash Secure Code, and Flash FPOER region.

- BOOTPATCH
  - Only secure BOOTROM code has the full access to BOOTPATCH.
  - BOOTPATCH user itself can only read/jump into BOOTPATCH and erasing/ programming is not allowed.
  - Other users can call BOOTPATCH API, but cannot directly read data in BOOTPATCH.
- Option Byte
  - All users can read data in these regions in RDP level 0, but they are not executable
  - Only SECURE_BOOTROM/BOOTROM_API users can erase these regions
  - Programming and erasing are allowed, however, only BOOTROM users have access to the Flash configuration interface, hence, other users rather than BOOTROM required to call BOOTROM API to perform programming and erasing operations.
- Flash secure region
  - Read/Jump to this secure region is only allowed for SECURE_BOOTROM/BOOTROM_API/ BOOTPATCH and Flash secure code itself.
  - Only SECURE BOOTROM can program this region
  - Only SECURE_BOOTROM/BOOTROM_API can directly erase Flash SECURE region. Other users can only indirectly erase Flash secure region by using BOOTROM_API. Whether it can be erased or not depends on Flash WRP/DMES1 configuration of secure regions.
- Flash PFOER
  - Reading/programming is not allowed, only jump is allowed.
  - Only SECURE_BOOTROM/BOOTROM_API can directly erase Flash PFOER region. Other user IDs can only indirectly erase Flash SECURE region by using BOOTROM API. Whether it can be

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erased or not depends on Flash WRP/DMEP configuration of PFOER regions.

- Flash non-secure regions
  - Read/Write to this region is not allowed, only jump is allowed. Users shall partition their code and literals accordingly.
  - Only SECURE_BOOTROM/BOOTROM_API can directly erase Flash PFOER region. Other users can only indirectly erase Flash SECURE region by using BOOTROM_API. Whether it can be erased or not depends on Flash WRP configuration of Flash Non Secure regions.

Flash RDP Level 1

RDP Level 1 is mainly designed for memory protection against illegal codes, downloaded into SRAM/TCM/SDRAM or other external memories, from accessing Flash non-secure region. Debuggers and other users than BOOTROM/BOOTPATCH/ FLASH are not allowed to read/program/erase Flash non-secure region. The rest of access permission to Flash is the same as in RDP level 0.

Flash RDP Level 2

Debuggers such as JTAG/SWD is disabled, thus, cannot access Flash. Other users than BOOTROM/Flash/SRAM/ TCM accessing to Flash is also disabled.

Flash Option byte modification is not allowed. Only option byte read is possible. Hence, downgrading from RDP level 2 to lower levels is not possible.

The rest of the access permission to the Flash in RDP level 2 is the same as in RDP level 1.

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Table 10-7 RDP protection for SIP Flash

RDP Protection Level	Access Area		Access Type	SECURE BOOTROM	BOOTROM_API NS_BOOTPATCH	SIP Flash			TCM/SRAM		Debug Or Other Code Location
						SECURE	PFOER	non-SECURE	Secure TCM/SRAM	Non-Secure TCM/SRAM	
Level 0	SIP Flash	NS_BOOTPATCH	Read	Yes	Yes	No	No	No	No	No	No
			PE	Yes	No	No	No	No	No	No	No
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		OB_FLASH	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			PE	Yes	Yes	IPO	IPO	IPO	IPO	IPO	IPO
			Jump	No	No	No	No	No	No	No	No
		Secure Area	Read	Yes	Yes	Yes	No	No	No	No	No
			PE	Yes	ME	IME	IME	IME	IME	IME	IME
			Jump	Yes	Yes	Yes	No	No	No	No	No
		PFOER	Read	No	No	No	No	No	No	No	No
			PE	ME	ME	IME	IME	IME	IME	IME	IME
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		Non-Secure	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			PE	Yes	Yes	IPIE	IPIE	IPIE	IPIE	IPIE	IPIE
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Level 1	SIP Flash	NS_BOOTPATCH	Read	Yes	Yes	No	No	No	No	No	No
			PE	Yes	No	No	No	No	No	No	No
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		OB_FLASH	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			PE	Yes	Yes	IPO	IPO	IPO	IPO	IPO	IPO
			Jump	No	No	No	No	No	No	No	No
		Secure Area	Read	Yes	Yes	Yes	No	No	No	No	No
			PE	Yes	ME	IME	IME	IME	IME	IME	IME
			Jump	Yes	Yes	Yes	No	No	No	No	No
		PFOER	Read	No	No	No	No	No	No	No	No
			PE	ME	ME	IME	IME	IME	IME	IME	IME
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		Non-Secure	Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
			PE	Yes	Yes	IPIE	IPIE	IPIE	IPIE	IME	IME
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Level 2	SIP Flash	NS_BOOTPATCH	Read	Yes	Yes	No	No	No	No	No	No
			PE	Yes	No	No	No	No	No	No	No
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

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		OB_FLASH	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
			PE	No	No	No	No	No	No	No	No
			Jump	No	No	No	No	No	No	No	No
		Secure Area	Read	Yes	Yes	Yes	No	No	No	No	No
			PE	Yes	ME	IME	IME	IME	IME	IME	No
			Jump	Yes	Yes	Yes	No	No	No	No	No
		PFOER	Read	No	No	No	No	No	No	No	No
			PE	ME	ME	IME	IME	IME	IME	IME	IME
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
		Non-Secure	Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
			PE	Yes	Yes	IPIE	IPIE	IPIE	IPIE	IME	No
			Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No

IPO: Indirect Program Only using BOOTROM API; IME: Indirect Mass Erase Only using BOOTROM API; PE: Both Direct Program and Erase Allowed; IPIE: Indirect Program Indirect Erase

BOOTROM RDP protection definition

Table 10-8 shows the RDP access protection for BOOTROM.

Only SECURE BOOTROM and BOOTROM_API/BOOTPATCH users are allowed to access SECURE BOOTROM, regardless of RDP protection level.

BOOTROM_API read access is only open for SECURE BOOTROM and BOOTROM_API/ BOOTPATCH users. Jump access is only allowed for users from BOOTROM/FLASH/TCM/SRAM in all RDP levels. Other users than BOOTROM/FLASH/TCM/SRAM can call BOOTROM_API in RDP level 0 and level 1 only.

Table 10-8 RDP protection for BOOTROM

RDP Protection Level	Access Area	Access Type	SECURE_BOOTROM	BOOTROM_API NS_BOOTPATCH	SIP Flash			TCM/SRAM		Debug or code from other regions
					SECURE	PFOER	Non-Secure	secure TCM/SRAM	Non-secure TCM/SRAM	
Level 0	SECURE_BOOTROM	Read	Yes	Yes	No	No	No	No	No	No
		Jump	Yes	Yes	No	No	No	No	No	No
	BOOTROM_API	Read	Yes	Yes	No	No	No	No	No	No
		Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Level 1	SECURE_BOOTROM	Read	Yes	Yes	No	No	No	No	No	No
		Jump	Yes	Yes	No	No	No	No	No	No
	BOOTROM_API	Read	Yes	Yes	No	No	No	No	No	No

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		Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Level 2	SECURE_BOOTROM	Read	Yes	Yes	No	No	No	No	No	No
		Jump	Yes	Yes	No	No	No	No	No	No
	BOOTROM_API	Read	Yes	Yes	No	No	No	No	No	No
		Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No

RDP protection definition for RAM/TCM/RTC Backup Registers

Table 10-9 shows the details of RDP protection for RAM/TCM/RTC Backup Registers.

RDP level 0

Accesses to TCM/SRAM/BKPSRAM/Backup registers are open to all users.

RDP level 1

In this mode, the protection against other users than BOOTROM/FLASH/secure SRAM/TCM are enabled. Their read/write accesses to protected TCM/SRAM and backup regions are disabled. Jump to BKPSRAM is also disabled.

The rest of access permission is the same as in RDP level 0.

RDP level 2

Debugger is disabled, thus cannot access SRAM/TCM/backup registers. Other users than FLASH/BOOTROM/ TCM/ SRAM accessing to TCM/SRAM/BKPSRAM/backup registers is disabled. The rest of the access permission is the same as in RDP level 1.

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Table 10-9 RDP protection for RAM/TCM/RTC Backup Registers

RDP Protection Level	Access Area			Access Type	SECURE_BOOTROM	BOOTROM_API NS_BOOTPATCH	SIP Flash			TCM/SRAM		Debug or code from other regions
							SECURE	PFOER	Non-Secure	secure TCM/SRAM	Non-secure TCM/SRAM	
Level L0	TCM/SRAM	Secure	TCM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			SRAM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		Non-Secure	TCM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			SRAM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Backup SRAM			Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Backup Register			Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Level L1	TCM/SRAM	Secure	TCM	Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			SRAM	Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
		Non-Secure	TCM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
			SRAM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Backup SRAM			Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	No	No

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	Backup Register			Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Level L2	TCM/SRAM	Secure	TCM	Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
			SRAM	Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
		Non-Secure	TCM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
			SRAM	Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
	Backup SRAM			Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Jump	Yes	Yes	Yes	Yes	Yes	Yes	No	No
	Backup Register			Read	Yes	Yes	Yes	Yes	Yes	Yes	No	No
				Write	Yes	Yes	Yes	Yes	Yes	Yes	No	No

OTP RDP protection definition

Table 10-10 shows the details of RDP protection for OTP.

Analog trimming and key information (Key_Info1 and Key_Info2) are not open for reading, except SECURE_BOOTROM in all RDP levels. Modification is not possible, except Key_Info2 region in RDP level 0 and level 1 by SECURE_BOOTROM.

System information modification is not allowed for all users. Only read access is allowed in all RDP levels for all users, except debug and other users than FLASH/BOOTROM/SRAM/TCM in RDP level 2.

OTP option byte modification is only possible with SECURE_BOOTROM or BOOTROM_API/ BOOTPATCH in the RDP protection level 0 and level 1. In the RDP level 1, OB1_OTP and OB2_OTP can only be modified with SECURE_BOOTROM.

User Information and Reserved areas are open for all users, except:

- Debugger and other users than FLASH/BOOTROM/SRAM/TCM in RDP level 1 and level 2

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Table 10-10 RDP protection for OTP

OTP Area	RDP Protection Level	Access Type	SECURE_BOOTROM	BOOTROM_API BOOTPATCH	SIP FLASH	Secure TCM/SRAM Code	Non-Secure TCM/SRAM Code	Debug or code in other regions
OB1_OTP	Level L0(1)	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes	No	No	No	No	No
	Level L1(1)	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes	No	No	No	No	No
	Level L2	Read	Yes	Yes	Yes	Yes	Yes	No
		Write	No(3)	No	No	No	No	No
OB2_OTP	Level L0(1)	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes(4)	No	No	No	No	No
	Level L1(1)	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes(4)	No	No	No	No	No
	Level L2	Read	Yes	Yes	Yes	Yes	Yes	No
		Write	No	No	No	No	No	No
OB3_OTP	Level L0(1)	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes	Yes(2)	No	No	No	No
	Level L1(1)	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes	Yes(2)	No	No	No	No
	Level L2	Read	Yes	Yes	Yes	Yes	Yes	No
		Write	No	No	No	No	No	No
User Info	Level 0	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes	Yes	Yes	Yes	Yes	Yes
	Level 1	Read	Yes	Yes	Yes	Yes	Yes	Yes
		Write	Yes	Yes	Yes	Yes	No	No
	Level 2	Read	Yes	Yes	Yes	Yes	No	No
		Write	Yes	Yes	Yes	Yes	No	No

(1) In RDP level 0 and 1, when users write data into these regions, the OTPC will automatically write its VLD address bit. If users directly write its VLD address, it will be rejected and the program error flag will be asserted.

(2) In RDP level 0 and 1, OB3_OTP can be written by SECURE_BOOTROM and BOOTROM_API, except TCM_SZ_CFG_OTP. Only SECURE_BOOTROM can modify TCM_SZ_CFG_OTP.

(3) Only 'SM_CFG_OTP' can be written by SECURE_BOOTROM in RDP level 2.

(4) In RDP level 0 and 1, only one modification is allowed for OB2_OTP.

RDP for Non-CPU masters

For other non-CPU masters (such as MDMA, DMAs, GPU, USB, etc.) to be able to access secure memories,

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respective software is required to activate their memory access in MMU_xxx_ME registers. Otherwise, its access to secure memories are not guaranteed. Their access permissions are the same as the software code that enables their memory access in MMU_xxx_ME.

RDP protection errors

The corresponding error flag is raised when an illegal read or write access is detected. There is no bus error generated. Refer to MMU_STS register for more details. Optionally, users can choose to generate an interrupt or reset when there is an illegal access detected.

10.4.6 Flash Write Protection (WRP)

The Flash memory write protection (WRP) prevents illegals or unwanted write/erase to special sections of the Flash memory user area.

Any 128KB Flash sector can be independently write-protected or unprotected by clearing/setting the corresponding WRP bit in the FLASH option byte WRP configuration. Total of 31 sectors can be protected, starting from 0x15000 0000.

A write-protected sector can neither be erased nor programmed. As a result, a sector erase cannot be performed if one sector is write-protected, unless a sector erase is executed during an RDP level 1 to 0 regression.

The embedded Flash memory write-protection user option bits can be modified without any restriction when the RDP level is set to level 0 or level 1. When it is set to level 2, the write protection bit field can no more be changed in the option bytes.

Note: PFOER or Flash secure areas are erase protected when it's enabled via DMES1 or DMEP1.

10.4.7 Real Time AES Decryption (RTAD) for SIP Flash

Real-Time AES Decryption (RTAD) engine is a module that sits in between the AXI Bus Matrix and the xSPI1 controller. It performs real-time AES 128-bit decryption of the data from SIP Flash when it is operating in XIP mode.

- It performs real-time decryption of the data from SIP Flash when it is operating in XIP mode.
- It uses AES-128 counter mode to perform decryption.
- 128 bits block is memory aligned to the memory mapped address aligned to lower 4 bits of address, i.e. the lower 4 bits of address is used to address the 128 bits (16 bytes) within the block.
- Performs decryption only as encryption required to be done off-line and written into the SPI flash through non-XIP mode.
- Supports all AHB3 transfer types including INCR and all WRAP burst types.
- Sufficient buffer to handle AHB wrapping burst to minimize re-fetching of data from SPI flash.

Refer to RTAD Chapter for more details on RTAD function.

10.4.8 Secure On-chip OTP Controller (OTPC) with on-chip OTP array

The OTPC provides the primary user-visible mechanism for interfacing with the on-chip OTP. These OTP's uses

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include:

- Unique chip identifiers
- Mask revision numbers
- Cryptographic keys
- Security configuration
- Boot characteristics
- Various control signals requiring permanent non-volatility

The OTP provides:

- Ability to read the fuses directly
- Ability to write (program) the fuses by software or JTAG/SWD
- OTP read-protect and write-protect
- Lock OTP for selected OTP fields

Refer to OTPC chapter for more details.

10.4.9 Secure debug control for JTAG/SWD

The device restricts access to embedded debug features, in order to guarantee the confidentiality of customer assets against unauthorized usage of debug & trace features.

On top of the RDP debug protection shown in Table 10-5, additional debug restriction mechanisms are as follows:

- Respective debug access port is totally disabled during the execution of SECURE_BOOTROM, secure FLASH code and Flash PFOER code. For example, if CM7 is executing from SECURE BOOTROM, CM7 debug access port is completely disabled.
- DAP Secure Mode: By default, all DAPs are disabled, once secure code in BOOTROM and FLASH execution are complete, DAP will be released.

10.4.10 Cryptographic Accelerators (AES, DES, SM4, SHA, TRNG)

N32Hxxx employs several cryptographic accelerator features as shown in Table 10-11:

Table 10-11 N32Hxxx Cryptographic Accelerator Features

Main Feature	Sub Feature	Description
Algorithm	AES	Support128,192 & 256 bits Key
		Support CBC,ECB Mode
	DES	Support DES,TDES
		Support 2 KEY and 3KEY in TDES
	SM4	Support CBC,ECB Mode
	SHA	Support SHA1,SHA224,SHA256,SHA384,SHA512
	RNG	Support TRNG & PRNG mode

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		Support LSFR129 for post process
		Support XOR combine all the source
		Support FIPS-140 CAVP
	Other	Support RNG and other algorithms running at the meantime
System	FIFO configure	Support algorithm data configured through FIFO
SDMA	Data Transport	Support auto transport data as a master from/to SRAM through AHB interface
		Support base address of SRAM transport through parameter
		Support data transport max size = 4KB (1024words)
		Support data transport data size check
		Support data transport CRC16 calculation
		Support SRAM max size = 2MB (512Kwords)
		Support Data rejoin in the case of source/destination address offset = 1/2/3

10.4.11 Tamper protection against voltage, temperature and clock attacks

N32Hxxx devices include active protection of critical security assets against temperature, voltage and frequency attacks. More specifically, it features:

- erasure of device secrets upon tamper detection including backup SRAM and backup registers
- improved guarantee of safe execution for the CPU and its associated security peripherals, including:
  - out-of-range voltage (example: VBAT), temperature and clocking (LSE/HSE) detection
  - security watchdog IWDG clocked by the internal oscillator LSI
  - possible selection of internal oscillator HSI as system clock
  - power supply protection
  - RTC/TAMP domain powered automatically with VBAT

10.5 Security Management Registers

10.5.1 MMU Control Register (MMU_CTRL)

Address offset: 0x00

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														RSTE	INTE

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Bit Field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	RSTE	Reset enable When oversteps its MMU authority, does this setting generate a reset. 0: Diable 1: Enable
0	INTE	Interrupt Enable When oversteps its MMU authority, does this setting generate a interrupt. 0: Diable 1: Enable

10.5.2 MMU Status Register (MMU_STS)

Address offset: 0x04

Reset value: 0x04000030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					XSPIL	ITRDE	ITWRE	BKRDE	BKWRE	H5RDE	H5WRE	H4RDE	H4WRE	H3RDE	H3WRE
					rs	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H2RDE	H2WRE	H1RDE	H1WRE	X3RDE	X3WRE	X2RDE	X2WRE	X1RDE	X1WRE	OBL	FLASHL	XSPIRDE	Reserved		
rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rs	rs	rc_w0			

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained
26	XSPIL	XSPI configure lock Write to 1 only. When it is set, it indicates that access to Flash configuration interface is locked. This bit is reset by hardware after detecting the unlock sequence. In the event of unsuccessful unlock operation, this bit remains set until the next reset.
25	ITRDE	ITCM Read error cleared by writing 0 0: not detected 1: detected
24	ITWRE	ITCM Write error cleared by writing 0 0: not detected 1: detected
23	BKRDE	BKP SRAM register Read error

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		cleared by writing 0 0: not detected 1: detected
22	BKWRE	BKP SRAM register Write error cleared by writing 0 0: not detected 1: detected
21	H5RDE	AHBSRAM5 Read error cleared by writing 0 0: not detected 1: detected
20	H5WRE	AHBSRAM5 Write error cleared by writing 0 0: not detected 1: detected
19	H4RDE	AHBSRAM4 Read error cleared by writing 0 0: not detected 1: detected
18	H4WRE	AHBSRAM4 Write error cleared by writing 0 0: not detected 1: detected
17	H3RDE	AHBSRAM3 Read error cleared by writing 0 0: not detected 1: detected
16	H3WRE	AHBSRAM3 Write error cleared by writing 0 0: not detected 1: detected
15	H2RDE	AHBSRAM2 Read error cleared by writing 0 0: not detected 1: detected
14	H2WRE	AHBSRAM2 Write error cleared by writing 0 0: not detected 1: detected
13	H1RDE	AHBSRAM1 Read error cleared by writing 0 0: not detected 1: detected

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12	H1WRE	AHBSRAM1 Write error cleared by writing 0 0: not detected 1: detected
11	X3RDE	AXISRAM3 Read error cleared by writing 0 0: not detected 1: detected
10	X3WRE	AXISRAM3 Write error cleared by writing 0 0: not detected 1: detected
9	X2RDE	AXISRAM2 Read error cleared by writing 0 0: not detected 1: detected
8	X2WRE	AXISRAM2 Write error cleared by writing 0 0: not detected 1: detected
7	X1RDE	AXISRAM1 Read error cleared by writing 0 0: not detected 1: detected
6	X1WRE	AXISRAM1 Write error cleared by writing 0 0: not detected 1: detected
5	OBL	Option byte lock Write to 1 only. When it is set, it indicates that access to Option Byte is locked. This bit is reset by hardware after detecting the unlock sequence. In the event of unsuccessful unlock operation, this bit remains set until the next reset. (BOOTROM handles access restriction via configuration interface, HW handles via XIP interface)
4	FLASHL	Flash lock Write to 1 only. When it is set, it indicates that access to Flash main is locked. This bit is reset by hardware after detecting the unlock sequence. In the event of unsuccessful unlock operation, this bit remains set until the next reset. (BOOTROM handles access restriction via configuration interface, HW handles via XIP interface)
3	XSPIRDE	XSPI Read error cleared by writing 0 0: not detected 1: detected
2:0	Reserved	Reserved,the reset value must be maintained

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10.5.3 MMU RTADx Config Register(MMU_RTADCx, x = 1~4)

Address offset: 0x34 + (x-1) * 4

Reset value: 0x000000f0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RPROPERTY		RMOD		Reserved	RKEYL	RCFGL	REN
								rw		rw			rw	rw	rw

Bit Field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:6	RPROPERTY	Region x Property. When SET to "01", The Region setting by RREGION1(RBEG/REND) Can be treated as a Data Flash Region. Even though REN=0, RPROPERTY can still be active for this Regionx. 00: Only instruction fetch is allowed in this Region. Data access is blocked. 01: Only data/literal load is allowed in this region. Instruction fetch is blocked. 1x: both instruction and data accesses are allowed..
5:4	RMOD	RTAD mode for RTAD Region x 00: Only do decryption for instruction, 01: Only do decryption for data/literal, 1x: do decryption for both instruction and data/literal(all of this Region).
3	Reserved	Reserved,the reset value must be maintained
2	RKEYL	RTAD key lock for RTAD Region x 0: Unlock, Can be modified freely. 1: Lock, Can not be modified. Once it is locked, kept until next reset.
1	RCFGL	RTAD configuration lock for RTAD Region x RPROPERTY /RMOD/REN/KEY/RREGION1(RBEG/REND) Lock or Unlock. 0: Unlock, Can be modified freely.

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		1: Lock, Can not be modified. Once it is locked, kept until next reset. writing RCFGL =1 -> RKEYL=1 by HW
0	REN	RTAD Region x Enable. RTAD is Automatically Enable by Hardware for BOOTPATCH, And is Automatically Disable by Hardware for OB_FLASH. 0: RTAD is Disable for RTAD Region1 of FLASHMain. 1: RTAD is Enable for RTAD Region1 of FLASHMain.

10.5.4 MMU RTAD Kye1 Partx Register (MMU_RTK1Px, x = 0~3)

Address offset: 0x44 + x * 4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY[15:0]															
rw															

Bit Field	Name	Description
31:0	KEY	Random Key For RTAD Region part, Can be Written Only by using BOOTROM_API

10.5.5 MMU RTAD Kye2 Partx Register (MMU_RTK2Px, x = 0~3)

Address offset: 0x54 + x * 4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY[15:0]															
rw															

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Bit Field	Name	Description
31:0	KEY	Random Key For RTAD Region part, Can be Written Only by using BOOTROM_API

10.5.6 MMU RTAD Kye3 Partx Register (MMU_RTK3Px, x = 0~3)

Address offset: 0x64 + x * 4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY[15:0]															
rw															

Bit Field	Name	Description
31:0	KEY	Random Key For RTAD Region part, Can be Written Only by using BOOTROM_API

10.5.7 MMU RTAD Kye4 Partx Register (MMU_RTK4Px, x = 0~3)

Address offset: 0x74 + x * 4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY[15:0]															
rw															

Bit Field	Name	Description
31:0	KEY	Random Key For RTAD Region part, Can be Written Only by using BOOTROM_API

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10.5.8 MMU RTAD Regionx Register (MMU_RTRx, x = 1~4)

Address offset: 0x84 + (x - 1) * 4

Reset value: 0x00001FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			REND[12:0]												
			rw												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RBEG[12:0]												
			rw												

Bit Field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28:16	REND[12:0]	RTAD Region x END for RTAD Region x Addr={REND[12:0],12'hFFF} If RBEGx<RENDx & RENx=1, Then the corresponding RTAD Regionx is Active. RTAD Region x BEGIN/END, The granulity is 4KB.
15:13	Reserved	Reserved,the reset value must be maintained
12:0	RBEG[12:0]	RTAD Region x BEGIN for RTAD Region x Addr={RBEG[12:0],12'h000} If (RBEGx<RENDx) & (RENx=1), Then the corresponding RTAD Regionx is Active. RTAD Region x BEGIN/END, The granulity is 4KB.

10.5.9 MMU RTAD CRC32 Polynomial Register (MMU_RTCRC)

Address offset: 0xb8

Reset value: 0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRC[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC[15:0]															
r															

Bit Field	Name	Description
31:0	CRC	CRC32 Polynomial 0x04C11DB7(Ethernet): X32 + X26 + X23 + X22 + X16 + X12

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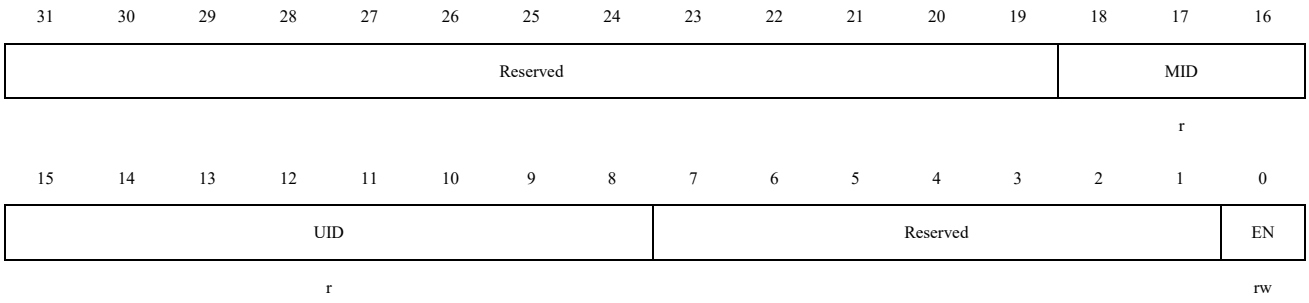
		+ X11 + X10 + X8 + X7 + X5 +X4 + X2 + X + 1, The CRC Initial Value is 32'hFFFF_FFFF. CRC calculation Only Need One Clcok Cycle. RTAD_CRC is sharing for all the 4 RTAD_KEY1/2/3/4. UserCode should read it back to verify after each RTAD_KEYx[127:0] has been written, It will be updated when the next RTAD_KEYy is written.

10.5.10 MMU ETH1 Memery Access Enable Register (MMU_ETH1ME)

Address offset: 0x012c

Reset value: 0x00000000



Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.11 MMU ETH2 Memery Access Enable Register (MMU_ETH2ME)

Address offset: 0x0130

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.12 MMU USB1 Memery Access Enable Register (MMU_USB1ME)

Address offset: 0x0134

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable

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		[0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.13 MMU USB2 Memery Access Enable Register (MMU_USB2ME)

Address offset: 0x0138

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

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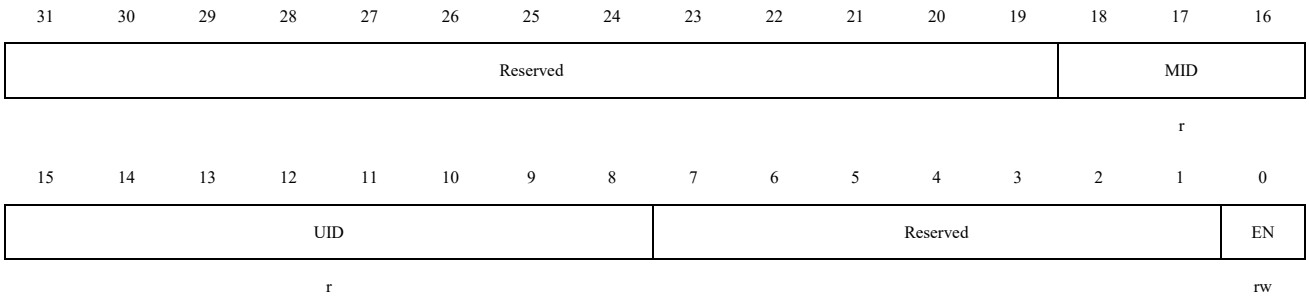
10.5.14 MMU SDMMC1 Memery Access Enable Register (MMU_SD1ME)

Address offset: 0x013c

Reset value: 0x00000000

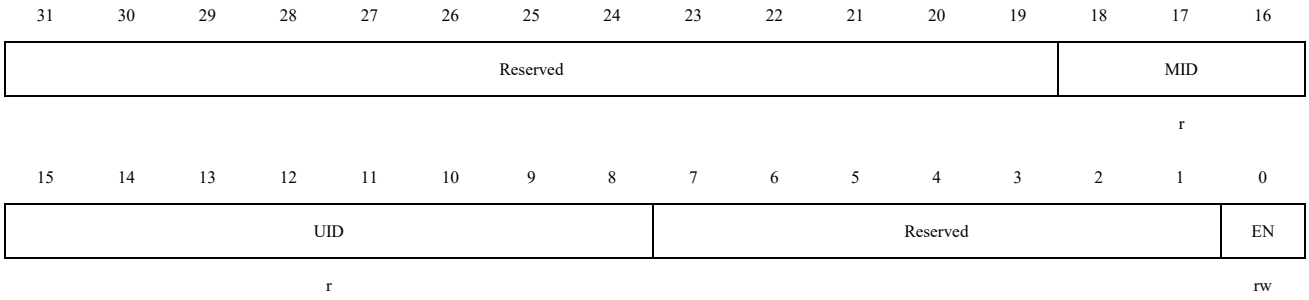


Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.15 MMU SDMMC2 Memery Access Enable Register (MMU_SD2ME)

Address offset: 0x0140

Reset value: 0x00000000



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Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.16 MMU DVP1 Memery Access Enable Register (MMU_DVP1ME)

Address offset: 0x0144

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable

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7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.17 MMU DVP2 Memery Access Enable Register (MMU_DVP2ME)

Address offset: 0x0148

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.18 MMU DMA1 Memery Access Enable Register (MMU_DMA1ME)

Address offset: 0x014c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		

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														r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.19 MMU DMA2 Memery Access Enable Register (MMU_DMA2ME)

Address offset: 0x0150

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable

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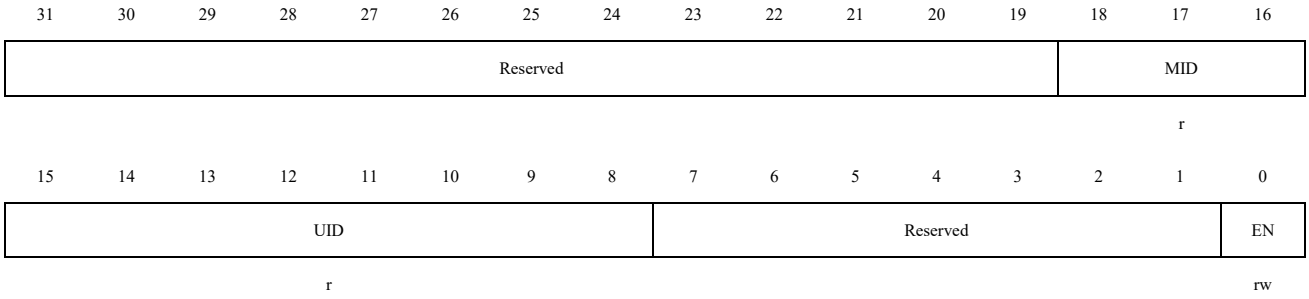
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.20 MMU DMA3 Memery Access Enable Register (MMU_DMA3ME)

Address offset: 0x0154

Reset value: 0x00000000



Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.21 MMU MDMA Memery Access Enable Register (MMU_MDMAME)

Address offset: 0x0158

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Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.22 MMU JPEG Memery Access Enable Register (MMU_JPEGME)

Address offset: 0x015c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained

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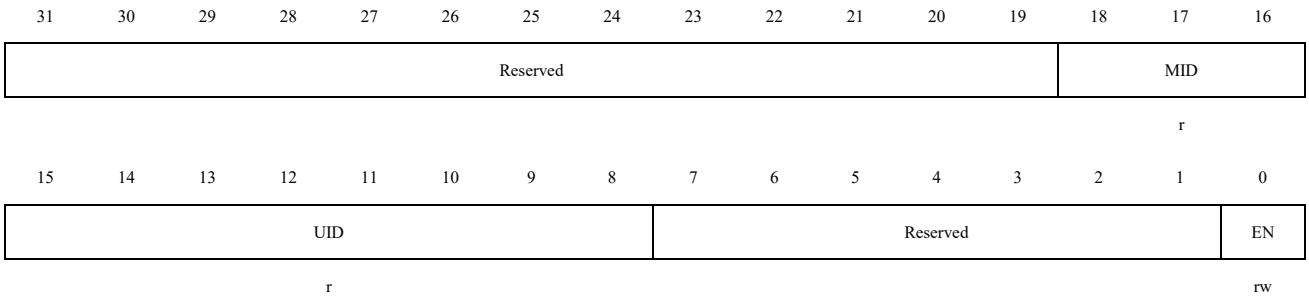
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.23 MMU LCD Memery Access Enable Register (MMU_LCDME)

Address offset: 0x0160

Reset value: 0x00000000



Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable

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		1:Enable

10.5.24 MMU GPU Memery Access Enable Register (MMU_GPUME)

Address offset: 0x0164

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN
r															rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.25 MMU SDPU Memery Access Enable Register (MMU_SDPUME)

Address offset: 0x0168

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MID		
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UID								Reserved							EN

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r rw

Bit Field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained
18:16	MID	Master enable [0]: CM7, [1]: CM4, [2]: DEBUG 0:Disable 1:Enable
15:8	UID	user ID that enable [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0:Disable 1:Enable
7:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable memory access for this master 0:Disable 1:Enable

10.5.26 MMU XSPI Read Error Debug Register (MMU_XRD)

Address offset: 0x0170

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							

r r

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master reads error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user reads error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram,

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		[3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.27 MMU XSPI Read Error Address Register (MMU_XRAD)

Address offset: 0x0178

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.XSPIRDE detected and kept until SW clears the MMU_STS.XSPIRDE FLAG)

10.5.28 MMU AXI SRAMn Write Error Debug Register (MMU_XnWD, n = 1~3)

Address offset: 0x017c + (n - 1) *16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
				r				r							

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master writes error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred

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7:0	UID	user writes error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.29 MMU AXI SRAMn Read Error Debug Register (MMU_XnRD, n = 1~3)

Address offset: 0x0180 + (n - 1) * 16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
				r				r							

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master reads error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user reads error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.30 MMU AXI SRAMn Write Error Address Register (MMU_XnWAD, n = 1~3)

Address offset: 0x0184 + (n - 1) * 16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.XnWRE detected and kept until SW clears the MMU_STS.XnWRE FLAG)

10.5.31 MMU AXI SRAMn Read Error Address Register (MMU_XnRAD, n = 1~3)

Address offset: 0x0188 + (n - 1) * 16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.XnRDE detected and kept until SW clears the MMU_STS.XnRDE FLAG)

10.5.32 MMU AHB SRAMn Write Error Debug Register (MMU_HnWD, n = 1~5)

Address offset: 0x0210 + (n - 1) * 16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
r				r											

Bit Field	Name	Description

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31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master writes error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user writes error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.33 MMU AHB SRAMn Read Error Debug Register (MMU_HnRD, n = 1~5)

Address offset: 0x0214 + (n - 1) * 16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
				r				r							

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master reads error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user reads error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.34 MMU AHB SRAMn Write Error Address Register (MMU_HnWAD, n = 1~5)

Address offset: 0x0218 + (n - 1) * 16

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.HnWRE detected and kept until SW clears the MMU_STS.HnWRE FLAG)

10.5.35 MMU AHB SRAMn Read Error Address Register (MMU_HnRAD, n = 1~5)

Address offset: 0x021c + (n - 1) * 16

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.HnRDE detected and kept until SW clears the MMU_STS.HnRDE FLAG)

10.5.36 MMU Backup SRAM Write Error Debug Register (MMU_BKWD)

Address offset: 0x0260

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
				r				r							

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master writes error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user writes error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.37 MMU Backup SRAM Read Error Debug Register (MMU_BKRD)

Address offset: 0x0264

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
				r				r							

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master reads error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user reads error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

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10.5.38 MMU Backup SRAM Write Error Address Register (MMU_BKWAD)

Address offset: 0x0268

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.BKWRE detected and kept until SW clears the MMU_STS.BKWRE FLAG)

10.5.39 MMU Backup SRAM Read Error Address Register (MMU_BKRAD)

Address offset: 0x026c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.BKRDE detected and kept until SW clears the MMU_STS.BKRDE FLAG)

10.5.40 MMU ITCM SRAM Write Error Debug Register (MMU_ITWD)

Address offset: 0x0270

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
r				r											

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master writes error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user writes error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram, [3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.41 MMU ITCM SRAM Read Error Debug Register (MMU_ITRD)

Address offset: 0x0274

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MID				UID							
r				r											

Bit Field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	MID	Master reads error ID [0]: DEBUG,[1]: other non-cpu master(ETH/USB/etc),[2]: CM7,[3]: CM4 0: No errors 1: An error occurred
7:0	UID	user reads error ID [0]:other_id(SDRAM,external SRAM,etc), [1]: nonsec_tcm/sram, [2]: sec_tcm/sram,

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		[3]:non_sec_flash, [4] pfoer_flash, [5]: sec_flash, [6]: bootrom_api, [7]:sec_bootrom 0: No errors 1: An error occurred

10.5.42 MMU ITCM SRAM Write Error Address Register (MMU_ITWAD)

Address offset: 0x0278

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.ITWRE detected and kept until SW clears the MMU_STS.ITWRE FLAG)

10.5.43 MMU ITCM SRAM Read Error Address Register (MMU_ITRAD)

Address offset: 0x027c

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDR	MMU Debug Register (captured once MMU_STS.ITRDE detected and kept until SW clears the MMU_STS.ITRDE FLAG)

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11 Real Time AES Decryption (RTAD)

11.1 Introduction

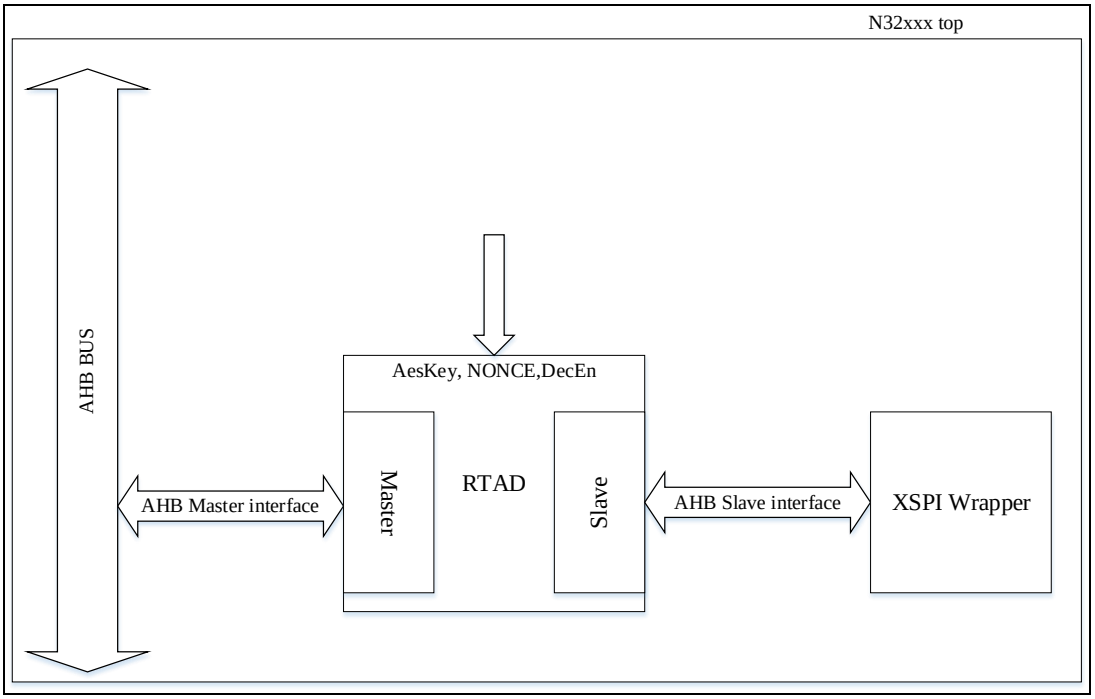
The Real-Time AES Decryption (RTAD) engine is a module that sits in between the AHB Bus Matrix (NIC-400 portion) and the xSPI controller (only XSPI1, not supported for XSPI2). It performs real-time AES 128-bit decryption of the data from xSPI IP when it is operating in XIP mode.

11.2 Main Features

- It performs real-time decryption of the data from xSPI IP when it is operating in XIP mode.
- It uses AES-128 counter mode to perform decryption.
- 128 bits block is memory aligned to the memory mapped address aligned to lower 4 bits of address. i.e the lower 4 bits of address is used to address the 128 bits (16 bytes) within the block.
- Performs decryption only as encryption is done off-line and written into the SPI flash through non-XIP mode.
- Supports AHB-32 slave on the side facing NIC-400 and AHB-32 on the master side facing the xSPI controller.
- Supports all AHB3 transfer types including INCR and all WRAP burst types.
- Sufficient buffer to handle AHB wrapping burst to minimize re-fetching of data from SPI flash.

11.3 Block diagram

Figure 11-1 RTAD block diagram



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11.4 Function description

RTAD performs real-time AES 128-bit decryption of the data from xSPI IP (only XSPI1) when it is operating in XIP READ mode (only as encryption is done off-line and written into the SPI flash through non-XIP mode).

11.4.1 Programming guide

The operation flow is as below:

1) If RTAD is enable, Unlock RTAD_KEY and RTAD_CFG by configuring MMU_RTADCx (x= 1~4), and then start configuring for RTAD function.

2) Configure NONCE.

The NONCE 96-bit is used for RTAD algorithm and is configured by AFIO registers (Refers them in AFIO User Manual-Register overview for more details) as followings:

- AFIO_XSPI1_DEC_NONCE2.
- AFIO_XSPI1_DEC_NONCE1.
- AFIO_XSPI1_DEC_NONCE0.

3) Configure RTAD Work Mode and Enable RTAD

- Set MMU_RTADCx. RTAD_ENABLE1 to Enable RTAD.
- Configure the Flash region now is data/literal fetch or instruction fetch by RTAD_MODE field and RTAD_PROPERTY field of MMU_RTAD**Cx** (x = 1~4) registers.
- Configure Decode Regions in MMU_RTRx RTAD_BEGINx and RTAD_ENDx field (x = 1~4).

4) Configure AesKey to MMU_RTKxPx

- AesKey is used for AES 128-bit decryption algorithm and it is selected by which region you access.
- When access Flash main, if Flash main is divided into Regions determined by MMU_RTRx register (XIP read address in range of RTAD_BEGINx field and RTAD_ENDx field of MMU_RTRx), then AesKey is determined by MMU_RTKxPx.

5) AesKey verify

- After write key to MMU_RTKxPy(x = 1~4, y = 0~3)**,** hardware will calculate RTAD_CRC from MMU_RTKxPy, then read RTAD_CRC back to verify.
- CRC poly 0x04C11DB7, initial value 0xFFFF_FFFF.

After these steps above, the RTAD will decrypted the data from xSPI Flash (The xSPI must work on XIP mode).The operation is described in details as below steps and diagram.

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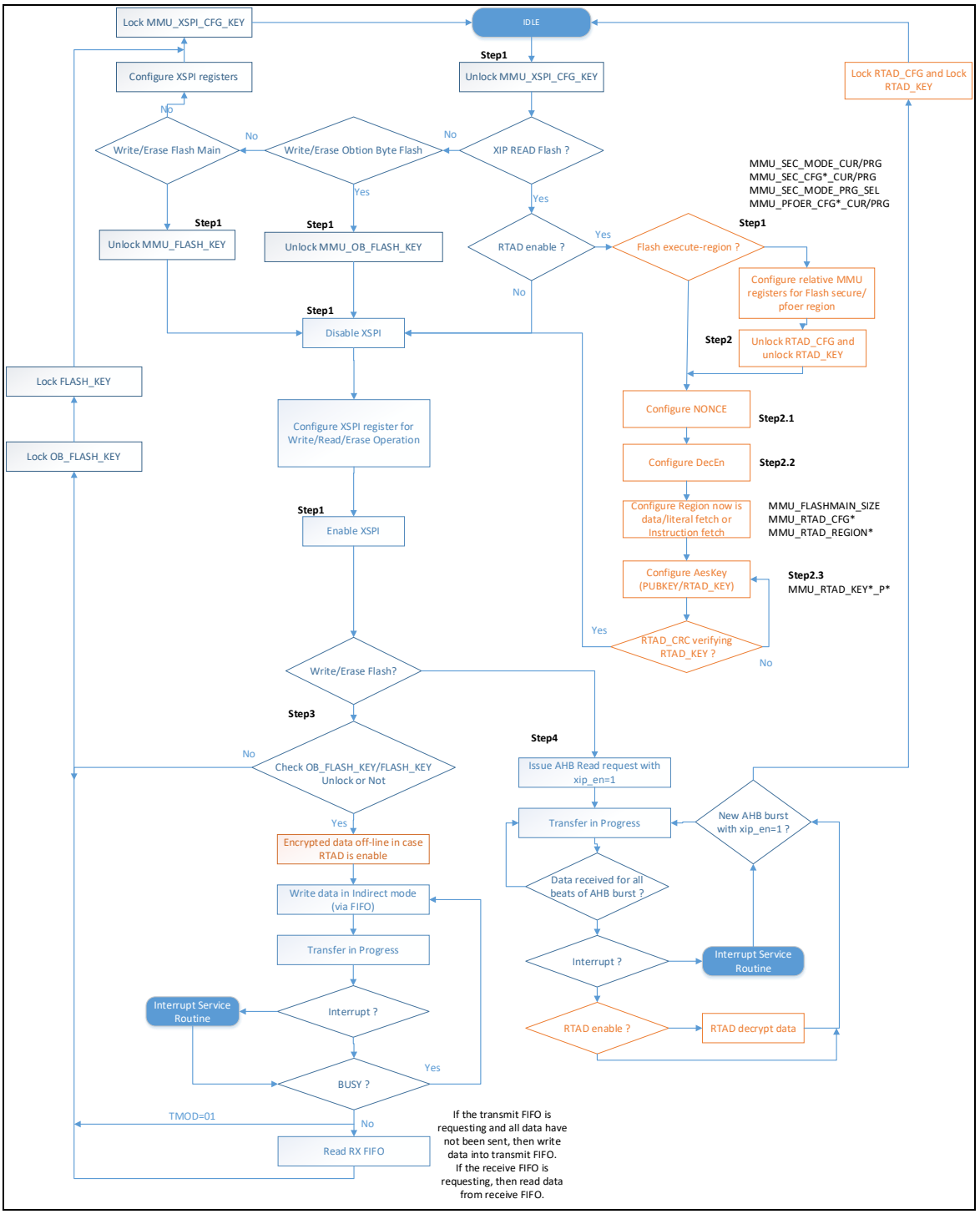
Figure 11-2 RTAD work flow



11.4.2 Register Overview

Refers registers from AFIO and MMU for details.

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12 GPIO And AFIO

12.1 Introduction

GPIO refers to general-purpose I/O, and AFIO refers to alternate function I/O. The chip supports up to 168 GPIOs, which are divided into 11 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE/GPIOF/GPIOG/GPIOH/GPIOI/GPIOJ/GPIOK). Each group has 16 ports (Group K has a total of 8 ports). GPIO ports share pins with other multiplexed peripherals, allowing users to configure them flexibly according to requirements. Each GPIO pin can be independently configured as an output (push-pull or open-drain), input (floating, pull-up, or pull-down) or alternate peripheral function port. Except for the analog pins, other GPIO pins have high current capacity.

12.2 Main features

GPIO ports have the following characteristics:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up
  - Input pull down
  - Analog function
  - Open drain output, pull-up and pull-down configurable
  - Push-pull output, pull-up and pull-down configurable
  - Push-pull alternate function, pull-up and pull-down configurable
  - Open drain alternate function, pull-up and pull-down configurable
- Separate bit setting or bit clearing functions
- All IOs have external interrupt capability
- All I/O support low-power mode wake-up, with configurable rising or falling edge
  - 16 EXTI can be used for SLEEP mode, STOP0 mode and STOP2 mode wake-up, all I/O can be alternated as EXTI
  - PA0/PA2/PC1/PC13/PI8/PI11 can be used for STANDBY mode wake-up
- Support software remapping of IO alternate function
- Support GPIO lock mechanism, which can only be cleared by reset after being locked

Each I/O port bit can be programmed arbitrarily, but the I/O port registers can be accessed as 32-bit word, half-word or byte since it is an AHB interface (except AFIO registers which supports only 32 bit word access).

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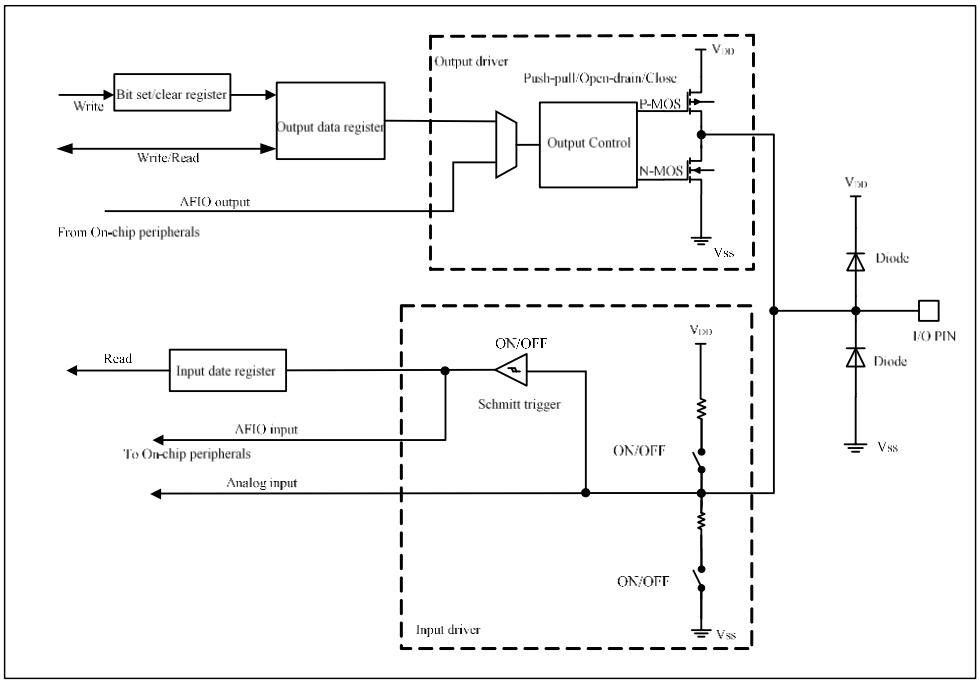
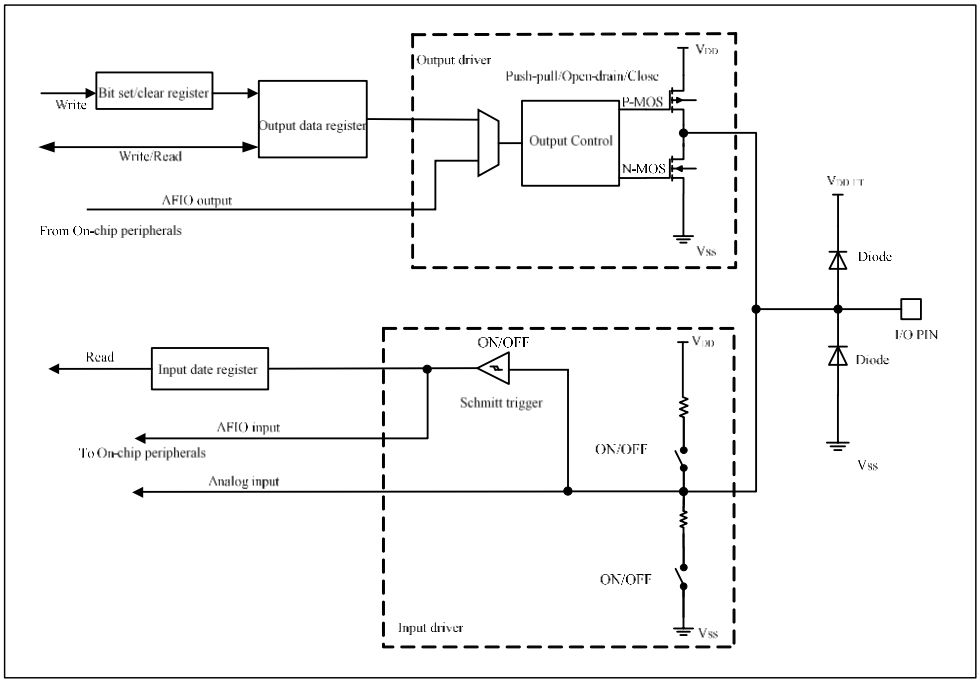
The figure below shows the basic structure of an I/O port.

Figure 12-1 Basic Structure of I/O Port



Most I/O ports can be configured to be compatible with 5V. The following diagram shows the structure of 5V-compatible I/O ports:

Figure 12-2 Basic Structure of I/O Port



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12.3 I/O function description

12.3.1 I/O mode configuration

The IO port mode can be configured through the registers GPIOx_PMODE, GPIOx_POTYPE and GPIOx_PUPD (x= A,B,C,D,E,F,G,H,I,J,K). The I/O configurations in different operation modes are shown in the following table:

Table 12-1 I/O Port Configuration Table

PMODE[1:0]	POT	PUPD[1:0]		I/O configuration
01	0	0	0	General-purpose output push-pull
	0	0	1	General-purpose output push-pull + pull-up
	0	1	0	General-purpose output push-pull + pull-down
	0	1	1	Reserved
	1	0	0	General-purpose output open-drain
	1	0	1	General-purpose output open-drain + pull-up
	1	1	0	General-purpose output open-drain + pull-down
	1	1	1	Reserved
10	0	0	0	Alternate function push-pull
	0	0	1	Alternate function push-pull + pull-up
	0	1	0	Alternate function push-pull + pull-down
	0	1	1	Reserved
	1	0	0	Alternate function open-drain
	1	0	1	Alternate function open-drain + pull-up
	1	1	0	Alternate function open-drain + pull-down
	1	1	1	Reserved
00	x	0	0	Input floating
	x	0	1	Input pull-up
	x	1	0	Input pull-down
	x	1	1	Reserved
11	x	0	0	Analog
	x	0	1	Reserved
	x	1	0	
	x	1	1	

The input and output characteristics of I/O under different configurations are shown in the following table：

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Table 12-2 Input and Output Characteristics of Different Configurations

Feature	GPIO Input	GPIO Output	Analog	Alternate function
Output buffer	Disabled	Enabled	Disabled	Configure according to peripheral functions
Schmitt trigger	Enabled	Enabled	Disabled Output is forced to 0	Enabled
Pull-up/pull-down/float	Configurable	Configurable	Disabled	Configurable
Open drain	Disabled	Configurable, GPIO outputs 0 when the output data is "0", and GPIO high impedance when "1"	Disabled	Configurable, GPIO outputs 0 when the output data is "0", and GPIO high impedance when "1"
Push pull	Disabled	Configurable, when the output data is "0", the GPIO outputs 0, and when the output data is "1", the GPIO outputs 1	Disabled	Configurable, GPIO outputs 0 when the output data is "0", and GPIO high impedance when "1"
Input data register (I/O status)	Readable	Readable	Read out 0	Readable
Output data register(Output value)	Invalid	Readable and writable	Invalid	Readable

12.3.1.1 Input mode

When I/O port is configured in input mode:

- Output buffer is disabled
- Schmitt trigger input is activated
- Whether pull-up and pull-down resistors are enabled depends on the configuration of the GPIOx_PUPD register
- The data appearing on the I/O pin is sampled into the input data register
- Read access to the input data register provides the I/O status

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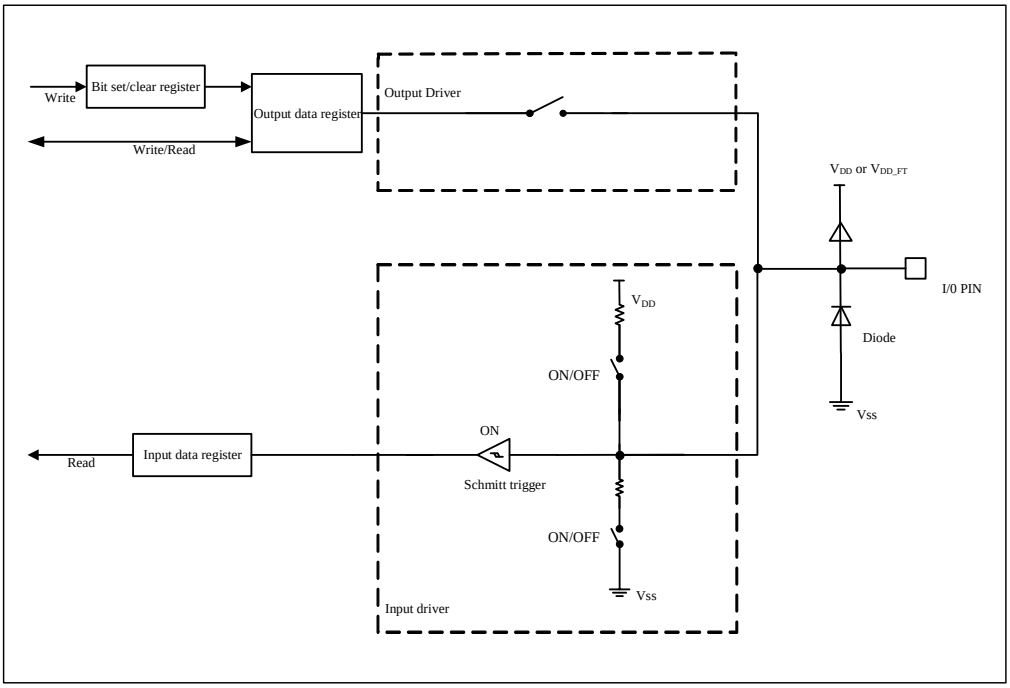
Figure 12-3 Input Floating/Pull-up/Pull-Down Configuration



12.3.1.2 Output mode

When I/O port is configured as output mode:

- Output buffer is activated
  - Open-drain mode: '0' on the output data register activates N-MOS, and the pin outputs low level.

    The '1' port on the output data register is placed in a high impedance state (P-MOS is never activated)
  - Push-pull mode: '0' on the output data register activates N-MOS, and the pin outputs low level.

    '1' on the output data register activates P-MOS, and the pin outputs high level.
- Schmidt trigger input is activated
- Whether the weak pull-up and pull-down resistors are enabled depends on the configuration of the GPIOx_PUPD register
- The data appearing on the I/O pin is sampled into the input data register
- Read access to input data register for I/O status
- Read access to the output data register gets the last written value

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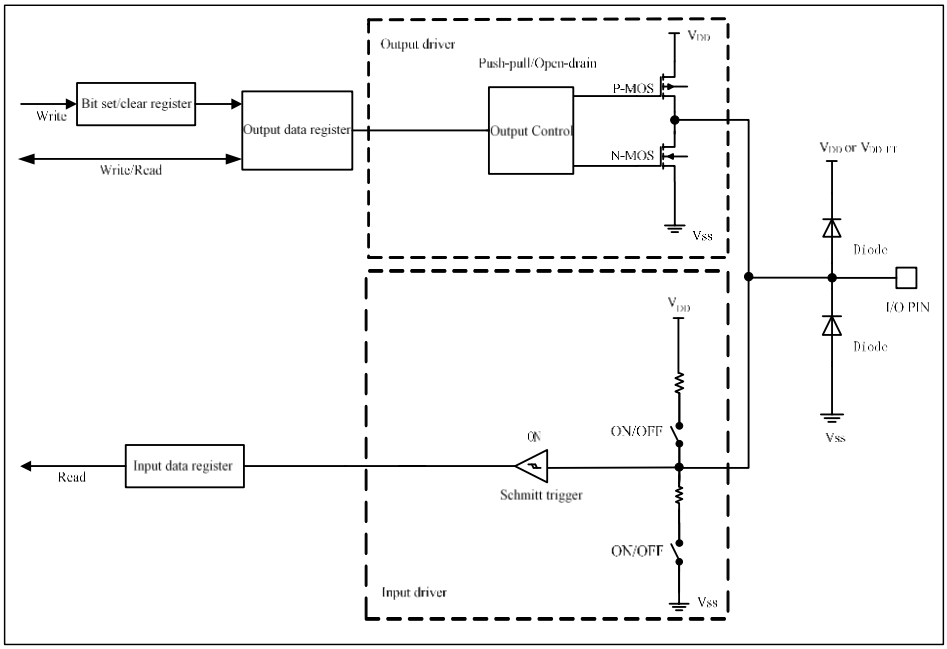
Figure 12-4 Output Mode Configuration



12.3.1.3 Alternate function mode

When the I/O port is configured as alternate function mode:

- In open-drain or push-pull configuration, the output buffer is controlled by the peripheral
- Schmidt trigger input is activated
- Whether the weak pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- Signal-driven output buffer with built-in peripherals
- The data appearing on the I/O pin is sampled into the input data register
- Read access to input data register for I/O status

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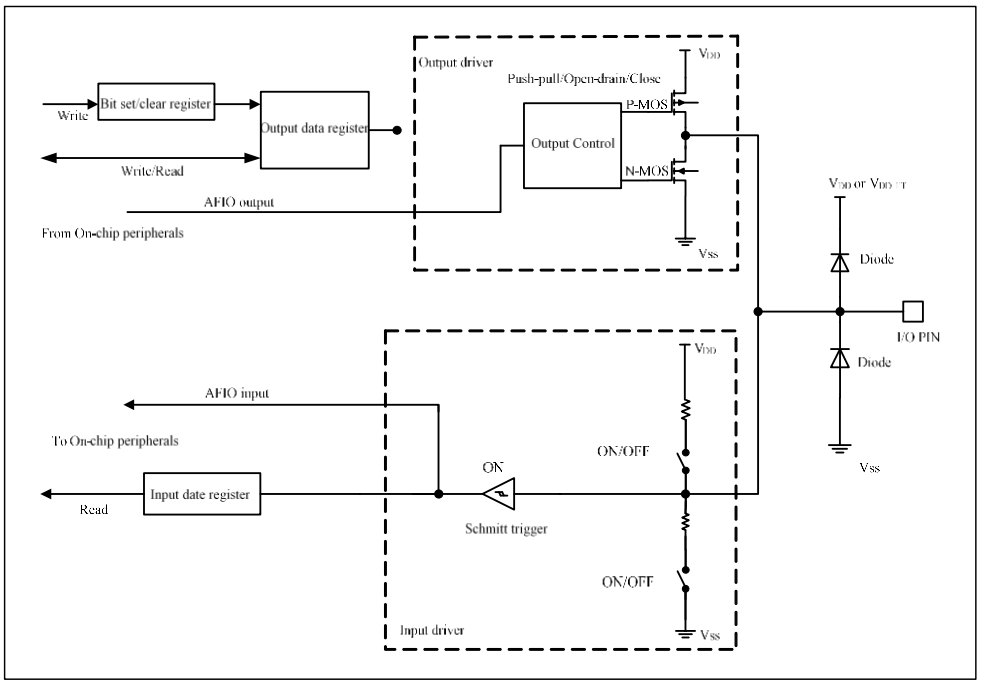
Figure 12-5 Alternate Function Configuration

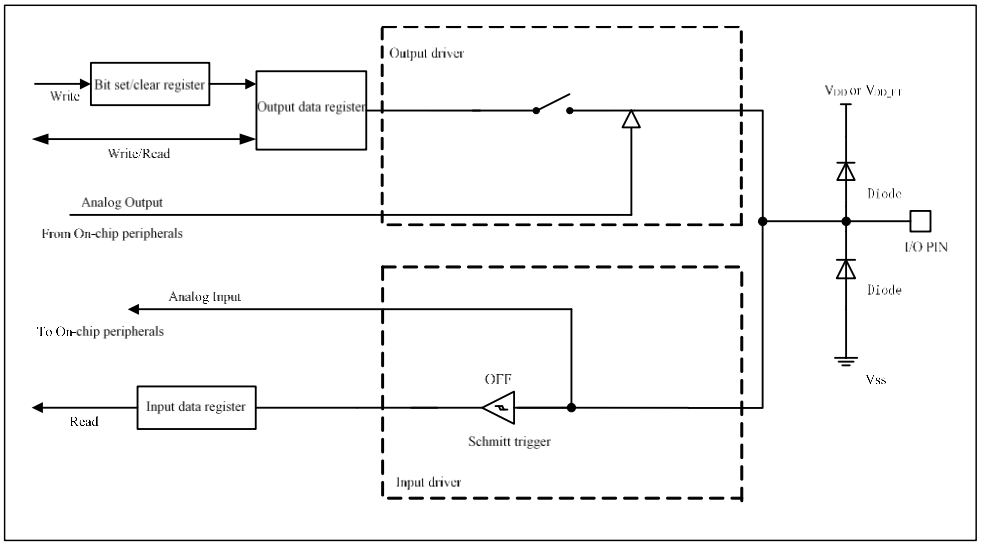


12.3.1.4 Analog mode

When the I/O Port is programmed as analog mode：

- Output buffer is disabled
- Schmitt trigger input is disabled and output value is forced to '0' (achieving zero consumption on each analog I/O pin)
- Weak pull-up and pull-down resistors are disabled
- When reading the input data register, the value is '0'

Figure 12-6 High Impedance Analog Mode Configuration



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12.3.2 Status after reset

During and after reset, the alternate function is not turned on, and the I/O port is configured to analog function mode (GPIOx_PMODE.PMODEy[1:0]=11b). But there are several exceptional signals:

- PH0-OSC_IN, PH1-OSC_OUT pins are default as OSC_IN, OSC_OUT pins, placed in analog mode

- After reset, the SWD_JTAG pins related to the debugging system are enabled by default, and put JTAG pin into input pull-up or pull-down mode
  - PA15: JTDI in input pull-up mode
  - PA14: JTCK in input pull-down mode
  - PA13: JTMS in input pull-up mode
  - PB4: NJTRST in input pull-up mode
  - PB3: JTD0 is placed in input floating mode
- PC13、PC14、PC15：
  - PC13~15 are three pins in the Backup domain, and the default is analog mode when powered on for the first time
- BOOT0:
  - The default mode is input pull-down when powered on. After the startup judgment is completed, it is in analog mode.

12.3.3 Individual bit setting and bit clearing

By writing '1' to the bit in the "set register (GPIOx_PBSC) and reset register (GPIOx_PBC)", the individual bit operation of the data register (GPIOx_POD) can be realized, and one or more bits can be set. The bit written with '1' is set or cleared accordingly, and the bit not written with '1' will not be changed. The software does not need interrupt disable, and is completed in a single AHB write operation.

12.3.4 External interrupt/wake-up line

All ports have external interrupt capability, which can be configured in the EXTI module:

- The port must be configured in input mode
- All ports can be configured for SLEEP/STOP0/STOP2 mode wake-up, supporting configurable rising or falling edges
- PA0/PA2/PC1/PC13/PI8/PI11 can be used for waking up from STANDBY mode
- All I/O ports can be connected to any of the 16 external interrupt/event lines, configured by the AFIO_EXTI_CFGx register

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12.3.5 Alternate function

When the I/O port is configured in alternate function mode. The port mode register (GPIOx_PMODE), output type register (GPIOx_POTYPE configuration push-pull or open-drain) and alternate function configuration register must be programmed before using, specifically as follows:

- Alternate input function: The port must be configured in input mode (floating, pull-up, or pull-down) and the input pin must be driven externally.
- Alternate output function: The port must be configured as a multiplexed output mode (push-pull or open-drain).
- Bidirectional alternate function: The port must be configured as a multiplexed output mode (push-pull or open-drain). In this case, the input driver is automatically configured as a floating input mode.
- Ports must be programmed to configure the desired multiplexed function.

In alternate output mode, the port is disconnected from the pin and output data register, and is connected to the output signal of the on-chip peripheral. If software configures a GPIO pin as an alternate output function but the peripheral is not activated, its output will be undefined.

12.3.5.1 Clock output MCO

The microcontroller allows the output of clock signals to external MCO pins, with two MCO outputs (MCO1/MCO2), which can be output through PC9/PA8 pins. The MCO pins must be configured as alternate push-pull output mode. The selection of the clock signal for MCO1 clock can be made from the following 6 clock signals, controlled by the clock configuration register RCC_CFG3.MCO1SEL[3:0]:

- MSI
- HSI
- HSE
- PLL3_B
- LSI
- LSE

The selection of the clock signal for MCO2 clock can be made from the following 6 clock signals, controlled by the clock configuration register RCC_CFG3.MCO2SEL[3:0]:

- SYS_CLK
- PLL1_A
- PLL2_A
- PLL3_A
- SHRPLL
- LSE

The alternate relationship of MCO1 and MCO2 signals is shown in the table below:

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Table 12-3 MCO Alternate Function Remap

Alternate function	GPIO port	Remap
MCO1	PA8	AF15
MCO2	PC9	AF15

12.3.5.2 Backup domain PC13/PC14/PC15 function remapping

The mode of PC14/PC15 is determined according to the following priority order:

- When LSE is enabled (RCC_BDCTRL.LSEEN is set), PC14/PC15 pins will be forced to analog mode. If LSE is configured in external clock mode (RCC_BDCTRL.LSEBP is set), PC14 is forced to analog mode, OSC32_OUT (PC15) can also be used for other purposes
- If LSE is not enabled and the backup domain is powered by VDD, PC14/PC15 can be used as GPIO.

The mode of PC13 is determined according to the following priority order:

- When RTC-OUT is enabled (alarm output, calibration clock output, automatic wake-up output, or tamper event output enabled), PC13 is used as the RTC output pin.
- When RTC-OUT is disabled, and RTC-TAMP1 is enabled, PC13 is used as the tamper detection input pin.
- If none of the above functions are enabled, and the backup domain is powered by VDD, PC13 can be used as GPIO.

The configuration conditions for different modes of PC13 to PC15 are shown in the table below:

PC14 and PC15	Conditions	PAD Mode Configuration	Priority
LSE	LSE enable	Analog mode	high
GPIO	LSE is turned off, the backup domain is powered by VDD, and does not enter low power mode (STANDBY, STOP0).	The mode of GPIO is determined by the application.	low
PC13	**Conditions**	**PAD Mode Configuration**	**Priority**
RTC-OUT	alarm output, calibration clock output, automatic wake-up output, or intrusion event output enabled.	Alternate push-pull output	high
RTC-TAMP1	RTC-OUT1 disabled, RTC-TAMP1 enable	Input floating	medium
GPIO	RTC-TAMP1 disabled, RTC-OUT disabled, backup domain powered by VDD, and not entering low power mode (STANDBY, STOP0)	The mode of GPIO is determined by the application.	low

When PC13~PC15 are used as GPIO, they can be configured as timestamp trigger input pins, as detailed in the table below:

Table 12-4 Timestamp Alternate Function Remap

Alternate function	GPIO port	Remap
Timestamp trigger input	PC13	AF9
	PC14	AF9

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	PC15	AF9

12.3.5.3 HSE/LSE pins used as GPIO ports

OSC_IN and OSC_OUT of HSE are mapped to PH0 and PH1 respectively, and OSC32_IN and OSC32_OUT of LSE are mapped to PC14 and PC15 respectively. If HSE or LSE is off, the corresponding pin can be used as GPIO. If HSE or LSE is on, the corresponding pin goes into analog mode and bypasses the GPIO configuration.

When HSE or LSE is configured in bypass mode, the pins remain as external clock inputs, and OSC_OUT or OSC32_OUT can still be used as GPIO.

12.3.5.4 JTAG/SWD alternate function remapping

The SWD-JTAG debug interface is enabled by default when the chip is powered on, and the debug interface is mapped to the GPIO port, as shown in the following table.

Alternate function	GPIO port	Remap
JTMS/SWDIO	PA13	AF15
JTCK/SWCLK	PA14	AF15
JTDI	PA15	AF15
JTDO	PB3	AF15
NJTRST	PB4	AF15

If you need to use its GPIO function during debugging, the above remapping configuration can be changed by setting the debugging IO alternate function configuration register (GPIOx_AFL or GPIOx_AFH).

12.3.5.5 Pull-Up/Pull-Down configuration

Since the JTAG pin is directly connected to the internal debug register (JTCK/SWCLK is directly connected to the clock terminal), it must be ensured that the JTAG input pin cannot be in a floating state. In order to avoid any uncontrolled IO levels, the input pins of JTAG are fixed with internal pull-up/pull-down:

- NJTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- JTCK/SWCLK: internal pull-down

Note: Once the JTAG interface is released by user software, the GPIO controller regains control, and it is necessary to ensure that the reset state of GPIO registers is consistent with the above.

12.3.5.6 SHRTIMx alternate function remapping

12.3.5.6.1 SHRTIM1 alternate function remapping

The external event input SHRTIM1_EXEVx (x=1~10) and SHRTIM1_FILTx (x= 1~6) can be mapped to some pins, configured in the AFIO_SHRT1_EXEV_CFGx (x=1,2) and AFIO_SHRT1_FLT_SEL registers (pin names are listed in the Register bit descriptions). For other signal mapping relationships, refer to the table below.

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Table 12-5 SHRTIM1 Alternate Function Remapping

Alternate function	GPIO port	Remap
SHRTIM1_CHA1	PC6	AF7
SHRTIM1_CHA2	PC7	AF7
SHRTIM1_CHB1	PC8	AF4
SHRTIM1_CHB2	PA8	AF3
SHRTIM1_CHC1	PA9	AF5
SHRTIM1_CHC2	PA10	AF3
SHRTIM1_CHD1	PA11	AF4
SHRTIM1_CHD2	PA12	AF3
SHRTIM1_CHE1	PG6	AF5
SHRTIM1_CHE2	PG7	AF5
SHRTIM1_CHF1	PG4	AF6
SHRTIM1_CHF2	PG5	AF7
SHRTIM1_SCIN	PB11	AF3
	PE0	AF5
SHRTIM1_SCOUT	PB10	AF6
	PE1	AF5

12.3.5.6.2 SHRTIM2 alternate function remapping

The external event input SHRTIM2_EXEVx (x=1~10) and SHRTIM2_FILTx (x= 1~6) can be mapped to some pins, configured in the AFIO_SHRT2_EXEV_CFGx(x=1,2) and AFIO_SHRT2_FLT_SEL registers (pin names are listed in the Register bit descriptions). For other signal mapping relationships, refer to the table below.

Table 12-6 SHRTIM2 Alternate Function Remapping

Alternate function	GPIO port	Remap
SHRTIM2_CHA1	PF0	AF5
SHRTIM2_CHA2	PF1	AF6
SHRTIM2_CHB1	PF2	AF6
SHRTIM2_CHB2	PF3	AF6
SHRTIM2_CHC1	PF4	AF7
SHRTIM2_CHC2	PF5	AF6
SHRTIM2_CHD1	PH2	AF6
SHRTIM2_CHD2	PH3	AF5
SHRTIM2_CHE1	PH4	AF4
SHRTIM2_CHE2	PH5	AF4
SHRTIM2_CHF1	PF14	AF4
SHRTIM2_CHF2	PF15	AF5
SHRTIM2_SCIN	PD8	AF4
	PG2	AF5
SHRTIM2_SCOUT	PD9	AF3
	PG3	AF3

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12.3.5.7 ATIMx alternate function remapping

12.3.5.7.1 ATIM1 alternate function remapping

Table 12-7ATIM1 Alternate Function Remapping

Alternate function	GPIO port	Remap
ATIM1_ETR	PA12	AF5
	PG5	AF8
	PE7	AF6
ATIM1_CH1	PA8	AF4
	PK1	AF4
	PE9	AF6
ATIM1_CH2	PA9	AF6
	PJ11	AF4
	PE11	AF5
ATIM1_CH3	PA10	AF4
	PJ9	AF3
	PE13	AF5
ATIM1_CH4	PA11	AF5
	PE14	AF6
ATIM1_BKIN1	PA6	AF8
	PE15	AF4
	PB12	AF6
	PK2	AF3
ATIM1_BKIN2	PE6	AF4
	PG4	AF7
	PA12	AF4
ATIM1_CH1N	PA7	AF9
	PB13	AF6
	PE8	AF6
	PK0	AF4
ATIM1_CH2N	PJ10	AF4
	PB0	AF5
	PB14	AF6
	PE10	AF5
ATIM1_CH3N	PB1	AF7
	PB15	AF6
	PJ8	AF3
	PE12	AF6
ATIM1_CH4N	PB2	AF8
	PD10	AF5

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Alternate function	GPIO port	Remap
	PH6	AF6

12.3.5.7.2 ATIM2 alternate function remapping

Table 12-8 ATIM2 Alternate Function Remapping

Alternate function	GPIO port	Remap
ATIM2_ETR	PA0	AF5
	PG8	AF6
	PI3	AF7
ATIM2_CH1	PJ8	AF4
	PC6	AF8
	PI5	AF8
ATIM2_CH2	PJ6	AF3
	PJ10	AF5
	PI6	AF7
	PC7	AF8
ATIM2_CH3	PK0	AF5
	PC8	AF5
	PI7	AF8
ATIM2_CH4	PC9	AF9
	PI2	AF7
ATIM2_BKIN1	PA6	AF9
	PK2	AF4
	PG2	AF6
	PI4	AF7
ATIM2_BKIN2	PG3	AF4
	PA8	AF5
	PI1	AF8
ATIM2_CH1N	PA5	AF8
	PA7	AF10
	PJ9	AF4
	PH13	AF5
ATIM2_CH2N	PB0	AF6
	PB14	AF7
	PJ7	AF3
	PJ11	AF5
	PH14	AF6
ATIM2_CH3N	PB1	AF8
	PB15	AF7
	PK1	AF5
	PH15	AF7

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Alternate function	GPIO port	Remap
ATIM2_CH4N	PB2	AF9
	PI0	AF6

12.3.5.7.3 ATIM3 alternate function remapping

Table 12-9 ATIM3 Alternate Function Remapping

Alternate function	GPIO port	Remap
ATIM3_ETR	PF6	AF6
	PH12	AF7
ATIM3_CH1	PF8	AF6
	PA6	AF10
	PH8	AF6
ATIM3_CH2	PF9	AF7
	PH10	AF6
ATIM3_CH3	PF10	AF5
	PD8	AF5
ATIM3_CH4	PF7	AF5
	PD14	AF5
ATIM3_BKIN1	PF5	AF7
	PH7	AF5
ATIM3_BKIN2	PI14	AF5
	PI15	AF4
ATIM3_CH1N	PH9	AF5
ATIM3_CH2N	PH11	AF5
ATIM3_CH3N	PD9	AF4
ATIM3_CH4N	PD15	AF5

12.3.5.7.4 ATIM4 alternate function remapping

Table 12-10 ATIM4 Alternate Function Remapping

Alternate function	GPIO port	Remap
ATIM4_ETR	PF6	AF7
	PJ0	AF4
ATIM4_CH1	PF9	AF8
	PA7	AF11
	PJ1	AF5
ATIM4_CH2	PF10	AF6
	PJ3	AF4

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Alternate function	GPIO port	Remap
ATIM4_CH3	PF7	AF6
	PJ12	AF5
ATIM4_CH4	PF8	AF7
	PJ14	AF3
ATIM4_BKIN1	PG0	AF7
	PD7	AF6
ATIM4_BKIN2	PJ5	AF4
	PK3	AF4
ATIM4_CH1N	PJ2	AF4
ATIM4_CH2N	PJ4	AF4
ATIM4_CH3N	PJ13	AF5
ATIM4_CH4N	PJ15	AF3

12.3.5.8 GTIMx alternate function remapping

12.3.5.8.1 GTIMA1 alternate function remapping

Table 12-11 GTIMA1 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA1_ETR	PA0	AF7
	PA5	AF10
	PA15	AF10
	PF4	AF8
GTIMA1_CH1	PF0	AF6
	PA0	AF6
	PA5	AF9
	PA15	AF9
GTIMA1_CH2	PF1	AF7
	PA1	AF4
	PB3	AF8
GTIMA1_CH3	PF2	AF7
	PA2	AF3
	PB10	AF7
GTIMA1_CH4	PF3	AF7
	PA3	AF7
	PB11	AF4

12.3.5.8.2 GTIMA2 alternate function remapping

Table 12-12 GTIMA2 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA2_ETR	PD2	AF7

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Alternate function	GPIO port	Remap
	PB8	AF6
GTIMA2_CH1	PA6	AF11
	PC6	AF9
	PB4	AF10
GTIMA2_CH2	PA7	AF12
	PC7	AF9
	PB5	AF8
GTIMA2_CH3	PB0	AF7
	PC8	AF6
	PB6	AF4
GTIMA2_CH4	PB1	AF9
	PC9	AF10
	PB7	AF5

12.3.5.8.3 GTIMA3 alternate function remapping

Table 12-13 GTIMA3 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA3_ETR	PD11	AF3
	PE0	AF6
GTIMA3_CH1	PD12	AF3
	PB6	AF5
GTIMA3_CH2	PD13	AF3
	PB7	AF6
GTIMA3_CH3	PD14	AF6
	PB8	AF7
GTIMA3_CH4	PD15	AF6
	PB9	AF6

12.3.5.8.4 GTIMA4 alternate function remapping

Table 12-14 GTIMA4 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA4_ETR	PA4	AF10
	PH8	AF7
GTIMA4_CH1	PA0	AF8
	PH10	AF7
GTIMA4_CH2	PA1	AF5
	PH11	AF6

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Alternate function	GPIO port	Remap
GTIMA4_CH3	PA2	AF4
	PH12	AF8
GTIMA4_CH4	PA3	AF8
	PI0	AF7

12.3.5.8.5 GTIMA5 alternate function remapping

Table 12-15 GTIMA5 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA5_ETR	PB2	AF10
	PG3	AF5
GTIMA5_CH1	PF0	AF7
	PF6	AF8
	PG12	AF9
GTIMA5_CH2	PF1	AF8
	PF7	AF7
	PG13	AF7
GTIMA5_CH3	PF2	AF8
	PF8	AF8
	PG14	AF8
GTIMA5_CH4	PF3	AF8
	PF9	AF9

12.3.5.8.6 GTIMA6 alternate function remapping

Table 12-16 GTIMA6 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA6_ETR	PG2	AF7
	PB3	AF9
GTIMA6_CH1	PF11	AF4
	PK4	AF4
GTIMA6_CH2	PF12	AF5
	PK5	AF4
GTIMA6_CH3	PF13	AF6
	PK6	AF4
GTIMA6_CH4	PF14	AF5
	PK7	AF4

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12.3.5.8.7 GTIMA7 alternate function remapping

Table 12-17 GTIMA7 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMA7_ETR	PI11	AF5
	PI14	AF6
GTIMA7_CH1	PH6	AF7
	PB14	AF8
GTIMA7_CH2	PH9	AF6
	PB15	AF8
GTIMA7_CH3	PI9	AF5
	PI12	AF5
GTIM7_CH4	PI10	AF6
	PI13	AF5

12.3.5.8.8 GTIMB1 alternate function remapping

Table 12-18 GTIMB1Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMB1_ETR	PE2	AF5
	PG1	AF8
GTIMB1_CH1N	PE4	AF5
	PA1	AF6
GTIMB1_CH1P	PE5	AF5
	PA2	AF5
	PC12	AF9
GTIMB1_CH2	PE6	AF5
	PA3	AF9
GTIMB1_CH3	PE0	AF7
GTIMB1_CH4	PE1	AF6
GTIMB1_BRK	PE3	AF3
	PA0	AF9
	PD2	AF8

12.3.5.8.9 GTIMB2 alternate function remapping

Table 12-19 GTIMB2 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMB2_ETR	PF2	AF9
	PD5	AF5
GTIMB2_CH1N	PF8	AF9
	PD0	AF5

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Alternate function	GPIO port	Remap
	PB6	AF6
GTIMB2_CH1P	PF6	AF9
	PD1	AF4
	PB8	AF8
GTIMB2_CH2	PF5	AF8
	PD2	AF9
GTIMB2_CH3	PF4	AF9
	PD3	AF6
GTIMB2_CH4	PF3	AF9
	PD4	AF6
GTIMB2_BRK	PF10	AF7
	PB4	AF11

12.3.5.8.10 GTIMB3 alternate function remapping

Table 12-20 GTIMB3 Alternate Function Remapping

Alternate function	GPIO port	Remap
GTIMB3_ETR	PH5	AF5
	PI15	AF5
GTIMB3_CH1N	PF9	AF10
	PJ0	AF5
	PB7	AF7
GTIMB3_CH1P	PF7	AF8
	PJ1	AF6
	PB9	AF7
GTIMB3_CH2	PH2	AF7
	PJ2	AF5
GTIMB3_CH3	PH3	AF6
	PJ3	AF5
GTIMB3_CH4	PH4	AF5
	PJ4	AF5
GTIMB3_BRK	PG6	AF6
	PB5	AF9

12.3.5.9 LPTIMx alternate function remapping

12.3.5.9.1 LPTIM1 alternate function remapping

Table 12-21 LPTIM1 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPTIM1_ETR	PG14	AF9
	PE0	AF8

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Alternate function	GPIO port	Remap
LPTIM1_IN1	PD12	AF4
	PG12	AF10
LPTIM1_IN2	PH2	AF8
	PG11	AF8
	PE1	AF7
LPTIM1_OUT	PD13	AF4
	PG13	AF8

12.3.5.9.2 LPTIM2 alternate function remapping

Table 12-22 LPTIM2 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPTIM2_ETR	PB11	AF5
	PE0	AF9
LPTIM2_IN1	PB10	AF8
	PD12	AF5
LPTIM2_IN2	PB12	AF7
	PD11	AF4
LPTIM2_OUT	PB13	AF7
	PD10	AF6

12.3.5.9.3 LPTIM3 alternate function remapping

Table 12-23 LPTIM3 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPTIM3_ETR	PI10	AF7
LPTIM3_IN1	PI8	AF4
LPTIM3_IN2	PI9	AF6
LPTIM3_OUT	PA1	AF7

12.3.5.9.4 LPTIM4 alternate function remapping

Table 12-24 LPTIM4 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPTIM4_ETR	PF15	AF6
LPTIM4_IN1	PG0	AF8
LPTIM4_IN2	PG1	AF9
LPTIM4_OUT	PA2	AF6

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12.3.5.9.5 LPTIM5 alternate function remapping

Table 12-25 LPTIM5 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPTIM5_ETR	PJ5	AF5
LPTIM5_IN1	PH6	AF8
LPTIM5_IN2	PH7	AF6
LPTIM5_OUT	PA3	AF10

12.3.5.10 FDCANx alternate function remapping

12.3.5.10.1 FDCAN1 alternate function remapping

Table 12-26 FDCAN1 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN1_TX	PI8	AF5
	PA12	AF9
	PH13	AF7
	PD1	AF6
	PB9	AF9
FDCAN1_RX	PI9	AF8
	PA11	AF9
	PH14	AF9
	PD0	AF8
	PB8	AF10

12.3.5.10.2 FDCAN2 alternate function remapping

Table 12-27 FDCAN2 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN2_TX	PH9	AF9
	PB13	AF10
	PB6	AF10
FDCAN2_RX	PH8	AF10
	PB12	AF10
	PB5	AF11

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12.3.5.10.3 FDCAN3 alternate function remapping

Table 12-28 FDCAN3 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN3_TX	PF7	AF10
	PF15	AF8
	PD13	AF7
	PG9	AF8
FDCAN3_RX	PF6	AF11
	PF14	AF7
	PD12	AF9
	PG10	AF11

12.3.5.10.4 FDCAN4 alternate function remapping

Table 12-29 FDCAN4 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN4_TX	PE2	AF7
	PI10	AF8
	PF0	AF9
FDCAN4_RX	PE3	AF5
	PI11	AF6
	PF1	AF10

12.3.5.10.5 FDCAN5 alternate function remapping

Table 12-30 FDCAN5 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN5_TX	PF4	AF11
	PH4	AF8
	PE8	AF8
FDCAN5_RX	PF5	AF9
	PH5	AF8
	PE9	AF8

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12.3.5.10.6 FDCAN6 alternate function remapping

Table 12-31 FDCAN6 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN6_TX	PI12	AF6
	PF12	AF6
	PE13	AF7
FDCAN6_RX	PI13	AF6
	PF13	AF8
	PE14	AF9

12.3.5.10.7 FDCAN7 alternate function remapping

Table 12-32 FDCAN7 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN7_TX	PJ3	AF8
	PH6	AF10
	PJ6	AF4
	PG7	AF7
FDCAN7_RX	PJ4	AF7
	PH7	AF8
	PJ7	AF4
	PG8	AF8

12.3.5.10.8 FDCAN8 alternate function remapping

Table 12-33 FDCAN8 Alternate Function Remapping

Alternate function	GPIO port	Remap
FDCAN8_TX	PJ0	AF7
	PJ8	AF8
	PG2	AF9
FDCAN8_RX	PJ1	AF8
	PJ9	AF8
	PG3	AF7

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12.3.5.11 DVPx alternate function remapping

12.3.5.11.1 DVP1 alternate function remapping

Table 12-34 DVP1 Alternate Function Remapping

Alternate function	GPIO port	Remap
DVP1_PIXCLK	PF6	AF3
	PA6	AF3
DVP1_HSYNC	PA4	AF3
	PB2	AF4
	PH8	AF5
DVP1_VSYNC	PG9	AF4
	PB7	AF3
	PI5	AF6
DVP1_D0	PH9	AF4
	PC6	AF5
	PA9	AF2
DVP1_D1	PH10	AF5
	PC7	AF5
	PA10	AF2
DVP1_D2	PH11	AF4
	PB13	AF3
	PC8	AF3
	PG10	AF7
	PE0	AF4
DVP1_D3	PH12	AF5
	PC9	AF4
	PG11	AF5
	PE1	AF4
DVP1_D4	PE4	AF3
	PH14	AF4
	PC11	AF3
DVP1_D5	PD3	AF3
	PB6	AF3
	PI4	AF5
DVP1_D6	PE5	AF3
	PB8	AF5
	PI6	AF5
DVP1_D7	PE6	AF2
	PB9	AF4
	PI7	AF6
DVP1_D8	PH6	AF4

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Alternate function	GPIO port	Remap
	PI1	AF5
	PC10	AF4
DVP1_D9	PJ5	AF2
	PH7	AF3
	PI2	AF4
	PC12	AF4
DVP1_D10	PI3	AF4
	PD6	AF4
	PB5	AF4
DVP1_D11	PF10	AF4
	PH15	AF5
	PD2	AF6
DVP1_D12	PF11	AF2
	PD12	AF2
	PG6	AF4
DVP1_D13	PJ4	AF2
	PD13	AF2
	PG7	AF4
	PI0	AF3
	PG15	AF4
DVP1_D14	PJ3	AF2
	PD4	AF3
DVP1_D15	PJ2	AF2
	PD5	AF3
DVP1_MCLK	PB1	AF5

12.3.5.11.2 DVP2 alternate function remapping

Table 12-35 DVP2 Alternate Function Remapping

Alternate function	GPIO port	Remap
DVP2_PIXCLK	PF7	AF3
	PH5	AF2
DVP2_HSYNC	PF8	AF4
	PH4	AF3
	PD8	AF3
DVP2_VSYNC	PF9	AF4
	PJ1	AF3
	PD9	AF2
DVP2_D0	PE2	AF3
	PF0	AF4

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Alternate function	GPIO port	Remap
	PK3	AF3
DVP2_D1	PE3	AF2
	PF1	AF5
	PK4	AF3
DVP2_D2	PF2	AF4
	PI12	AF3
	PK5	AF3
DVP2_D3	PI13	AF3
	PF3	AF4
	PK6	AF3
DVP2_D4	PI14	AF3
	PF4	AF5
	PK7	AF3
DVP2_D5	PF5	AF4
	PF6	AF4
	PK2	AF2
DVP2_D6	PC2	AF5
	PF12	AF4
	PK1	AF2
DVP2_D7	PC3	AF5
	PF13	AF4
	PK0	AF2
DVP2_D8	PF14	AF3
	PJ6	AF2
	PI4	AF6
DVP2_D9	PF15	AF4
	PJ7	AF2
	PI5	AF7
DVP2_D10	PG0	AF6
	PJ8	AF2
	PI6	AF6
DVP2_D11	PG1	AF6
	PJ9	AF2
	PI7	AF7
DVP2_D12	PB2	AF5
	PJ10	AF2
	PG2	AF4
	PJ15	AF2
DVP2_D13	PI15	AF3
	PJ11	AF2

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Alternate function	GPIO port	Remap
	PG3	AF2
	PJ14	AF2
DVP2_D14	PB12	AF4
	PG4	AF5
	PJ13	AF4
DVP2_D15	PD11	AF2
	PG5	AF6
	PJ12	AF4
DVP2_MCLK	PG12	AF6

12.3.5.12 FEMC alternate function remapping

Table 12-36 FEMC Alternate Function Remapping

Alternate function	GPIO port	Remap
FEMC_A0	PF0	AF3
FEMC_A1	PF1	AF4
	PC5	AF3
FEMC_A2	PF2	AF3
FEMC_A3	PF3	AF3
	PF10	AF8
FEMC_A4	PF4	AF4
	PI12	AF1
FEMC_A5	PF5	AF3
FEMC_A6	PF12	AF3
FEMC_A7	PF13	AF3
	PI13	AF1
FEMC_A8	PF14	AF2
FEMC_A9	PF15	AF3
	PI14	AF1
FEMC_A10	PG0	AF5
	PA3	AF3
FEMC_A11	PG1	AF5
	PK2	AF0
FEMC_A12	PG2	AF3
	PK6	AF1
FEMC_A13	PG3	AF1

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Alternate function	GPIO port	Remap
FEMC_A14	PG4	AF4
FEMC_A15	PG5	AF5
	PK7	AF1
FEMC_A16/FEMC_CLE	PD11	AF1
FEMC_A17/FEMC_ALE	PD12	AF1
FEMC_A18	PD13	AF1
FEMC_A19	PE3	AF1
	PA0	AF2
FEMC_A20	PE4	AF1
FEMC_A21	PE5	AF1
FEMC_A22	PE6	AF0
	PC4	AF3
FEMC_A23	PE2	AF2
FEMC_A24	PG13	AF3
FEMC_A25	PC0	AF3
	PG14	AF4
FEMC_D0/FEMC_DA0	PC1	AF8
	PD14	AF4
	PI11	AF3
FEMC_D1/FEMC_DA1	PD15	AF4
FEMC_D2/FEMC_DA2	PD0	AF3
	PJ6	AF0
FEMC_D3/FEMC_DA3	PD1	AF3
	PJ7	AF0
FEMC_D4/FEMC_DA4	PE7	AF5
FEMC_D5/FEMC_DA5	PE8	AF5
	PJ10	AF0
FEMC_D6/FEMC_DA6	PE9	AF5
	PC12	AF2
	PJ11	AF0
FEMC_D7/FEMC_DA7	PE10	AF4
	PD2	AF3
	PK3	AF1
FEMC_D8/FEMC_DA8	PA4	AF1
	PE11	AF2

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Alternate function	GPIO port	Remap
FEMC_D9/FEMC_DA9	PA5	AF2
	PE12	AF3
	PK4	AF1
FEMC_D10/FEMC_DA10	PE13	AF2
	PB14	AF2
FEMC_D11/FEMC_DA11	PE14	AF3
	PB15	AF2
	PK5	AF1
FEMC_D12/FEMC_DA12	PC0	AF4
	PE15	AF2
FEMC_D13/FEMC_DA13	PD8	AF2
	PB10	AF2
FEMC_D14/FEMC_DA14	PD9	AF1
FEMC_D15/FEMC_DA15	PD10	AF3
	PB11	AF1
FEMC_D16	PH8	AF3
FEMC_D17	PH9	AF2
FEMC_D18	PH10	AF3
FEMC_D19	PH11	AF2
FEMC_D20	PH12	AF3
FEMC_D21	PH13	AF2
FEMC_D22	PH14	AF2
FEMC_D23	PH15	AF3
FEMC_D24	PI0	AF1
FEMC_D25	PI1	AF3
FEMC_D26	PI2	AF2
FEMC_D27	PI3	AF3
FEMC_D28	PI6	AF3
FEMC_D29	PI7	AF4

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Alternate function	GPIO port	Remap
FEMC_D30	PI9	AF2
FEMC_D31	PI10	AF4
FEMC_NE1/FEMC_NCE1	PC7	AF3
	PD7	AF2
FEMC_NE2/FEMC_NCE2	PC8	AF1
	PG9	AF3
FEMC_NE3	PG6	AF2
	PG10	AF4
FEMC_NE4	PG12	AF3
FEMC_NOE	PD4	AF2
FEMC_NWE	PD5	AF2
FEMC_NADV/FEMC_NL	PB7	AF2
FEMC_NWAIT	PC6	AF3
	PD6	AF2
FEMC_NBL0	PE0	AF2
	PJ13	AF1
FDMC_NBL1	PE1	AF2
FDMC_NBL2	PI4	AF3
FDMC_NBL3	PI5	AF4
FEMC_CLK	PD3	AF1
FEMC_INT/FEMC_BUSY	PC8	AF2
	PG7	AF2
FEMC_BAA	PH6	AF3
	PJ15	AF0
	PJ12	AF1
FEMC_CRE	PH7	AF2
	PJ14	AF0

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12.3.5.13 USARTx alternate function remapping

12.3.5.13.1 USART1 alternate function remapping

Table 12-37 USART1 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART1_TX	PF0	AF8
	PB14	AF9
	PA9	AF7
	PB6	AF7
USART1_RX	PF1	AF9
	PB15	AF9
	PA10	AF5
	PB7	AF8
USART1_CK	PF2	AF10
	PA8	AF6
USART1_CTS	PF3	AF10
	PA11	AF6
USART1_RTS_DE	PF4	AF10
	PA12	AF6

12.3.5.13.2 USART2 alternate function remapping

Table 12-38 USART2 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART2_TX	PA2	AF7
	PD5	AF6
USART2_RX	PA3	AF11
	PD6	AF7
USART2_CK	PA4	AF11
	PD7	AF7
USART2_CTS	PA0	AF10
	PD3	AF7
USART2_RTS_DE	PA1	AF8
	PD4	AF7

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12.3.5.13.3 USART3 alternate function remapping

Table 12-39 USART3 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART3_TX	PB10	AF9
	PD8	AF6
	PC10	AF7
USART3_RX	PB11	AF6
	PD9	AF5
	PC11	AF7
USART3_CK	PB12	AF8
	PD10	AF7
	PC12	AF10
USART3_CTS	PB13	AF8
	PD11	AF5
USART3_RTS_DE	PB14	AF10
	PD12	AF6

12.3.5.13.4 USART4 alternate function remapping

Table 12-40 USART4 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART4_TX	PC6	AF10
	PG14	AF10
USART4_RX	PC7	AF10
	PG9	AF7
USART4_CK	PG7	AF6
	PC8	AF7
USART4_CTS	PG13	AF9
	PG15	AF5
USART4_RTS_DE	PG8	AF7
	PG12	AF11

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12.3.5.13.5 USART5 alternate function remapping

Table 12-41 USART5 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART5_TX	PE3	AF4
	PG12	AF12
USART5_RX	PE2	AF6
	PG11	AF9
USART5_CK	PE15	AF5
	PG15	AF6
USART5_CTS	PG13	AF10
USART5_RTS_DE	PG14	AF11

12.3.5.13.6 USART6 alternate function remapping

Table 12-42 USART6 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART6_TX	PE5	AF6
	PH15	AF8
USART6_RX	PE4	AF6
	PH14	AF7
USART6_CK	PE14	AF7
USART6_CTS	PG4	AF8
USART6_RTS_DE	PG5	AF9

12.3.5.13.7 USART7 alternate function remapping

Table 12-43 USART7 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART7_TX	PH5	AF6
	PF15	AF7
USART7_RX	PH4	AF6
	PF14	AF6
USART7_CK	PH3	AF7
	PF13	AF7
USART7_CTS	PG2	AF8

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Alternate function	GPIO port	Remap
USART7_RTS_DE	PG3	AF6

12.3.5.13.8 USART8 alternate function remapping

Table 12-44 USART8 Alternate Function Remapping

Alternate function	GPIO port	Remap
USART8_TX	PI3	AF8
	PI5	AF9
USART8_RX	PI2	AF8
	PI4	AF8
USART8_CK	PI1	AF9
	PI6	AF8
USART8_CTS	PJ8	AF5
USART8_RTS_DE	PJ9	AF5

12.3.5.14 UARTx alternate function remapping

12.3.5.14.1 UART9 alternate function remapping

Table 12-45 UART9 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART9_TX	PA0	AF11
	PA12	AF7
	PH13	AF6
	PC10	AF8
	PD1	AF5
	PB9	AF8
UART9_RX	PI9	AF7
	PA1	AF9
	PA11	AF7
	PH14	AF8
	PC11	AF8
	PD0	AF6
	PB8	AF9
UART9_CTS	PB0	AF8
	PB15	AF10

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Alternate function	GPIO port	Remap
UART9_RTS_DE	PB14	AF11
	PA15	AF11

12.3.5.14.2 UART10 alternate function remapping

Table 12-46 UART10 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART10_TX	PH12	AF9
	PB13	AF9
	PC12	AF11
	PB6	AF8
UART10_RX	PH11	AF7
	PB12	AF9
	PD2	AF10
	PB5	AF10
UART10_CTS	PH9	AF7
	PC9	AF11
UART10_RTS_DE	PH8	AF8
	PC8	AF8

12.3.5.14.3 UART11 alternate function remapping

Table 12-47 UART11 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART11_TX	PF7	AF9
	PE8	AF7
	PA15	AF12
	PB4	AF12
UART11_RX	PF6	AF10
	PE7	AF7
	PA8	AF7
	PB3	AF10
UART11_CTS	PF9	AF11
	PE10	AF6
UART11_RTS_DE	PF8	AF10
	PE9	AF7

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12.3.5.14.4 UART12 alternate function remapping

Table 12-48 UART12 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART12_TX	PD12	AF7
	PJ8	AF6
	PE1	AF8
UART12_RX	PD13	AF5
	PJ9	AF6
	PE0	AF10
UART12_CTS	PD14	AF7
	PJ10	AF6
UART12_RTS_DE	PD15	AF7
	PJ11	AF6

12.3.5.14.5 UART13 alternate function remapping

Table 12-49 UART13 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART13_TX	PG1	AF10
	PE13	AF6
	PD15	AF8
UART13_RX	PG0	AF9
	PE12	AF7
	PD14	AF8
UART13_CTS	PJ4	AF6
	PE14	AF8
	PD12	AF8
	PD0	AF7
UART13_RTS_DE	PJ3	AF6
	PE15	AF6
	PD13	AF6

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12.3.5.14.6 UART14 alternate function remapping

Table 12-50 UART14 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART14_TX	PH7	AF7
	PJ11	AF7
UART14_RX	PH6	AF9
	PJ10	AF7
UART14_CTS	PH9	AF8
	PJ9	AF7
UART14_RTS_DE	PH8	AF9
	PJ8	AF7

12.3.5.14.7 UART15 alternate function remapping

Table 12-51 UART15 Alternate Function Remapping

Alternate function	GPIO port	Remap
UART15_TX	PH3	AF8
	PJ1	AF7
UART15_RX	PH2	AF9
	PJ0	AF6
UART15_CTS	PH5	AF7
	PJ3	AF7
UART15_RTS_DE	PH4	AF7
	PJ2	AF6

12.3.5.15 LPUARTx alternate function remapping

12.3.5.15.1 LPUART1 alternate function remapping

Table 12-52 LPUART1 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPUART1_CTS	PA11	AF8
LPUART1_DE/LPUART1_RTS	PA12	AF8
LPUART1_RX	PA10	AF6
	PB7	AF9
LPUART1_TX	PA9	AF8
	PB6	AF9

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12.3.5.15.2 LPUART2 alternate function remapping

Table 12-53 LPUART2 Alternate Function Remapping

Alternate function	GPIO port	Remap
LPUART2_CTS	PD2	AF11
LPUART2_DE/LPUART2_RTS	PD3	AF8
LPUART2_RX	PI3	AF9
	PD5	AF7
LPUART2_TX	PI2	AF9
	PD4	AF8

12.3.5.16 I2C alternate function remapping

12.3.5.16.1 I2C1 alternate function remapping

Table 12-54 I2C1 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C1_SCL	PG5	AF10
	PD4	AF9
	PB6	AF11
	PB8	AF11
I2C1_SDA	PG4	AF9
	PD5	AF8
	PB7	AF10
	PB9	AF10
I2C1_SMBA	PG6	AF7
	PD1	AF7
	PB5	AF12

12.3.5.16.2 I2C2 alternate function remapping

Table 12-55 I2C2 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C2_SCL	PF1	AF11
	PH4	AF9
	PB10	AF10
I2C2_SDA	PF0	AF10
	PH5	AF9
	PB11	AF7
I2C2_SMBA	PF2	AF11
	PH6	AF11
	PB12	AF12

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12.3.5.16.3 I2C3 alternate function remapping

Table 12-56 I2C3 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C3_SCL	PH7	AF9
	PK0	AF6
	PA8	AF9
I2C3_SDA	PH8	AF11
	PK1	AF6
	PC9	AF12
I2C3_SMBA	PH9	AF10
	PK2	AF5
	PA9	AF10

12.3.5.16.4 I2C4 alternate function remapping

Table 12-57 I2C4 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C4_SCL	PF14	AF8
	PH11	AF8
	PD12	AF10
	PB8	AF12
	PB6	AF12
I2C4_SDA	PF15	AF9
	PH12	AF10
	PD13	AF8
	PB7	AF11
	PB9	AF11
I2C4_SMBA	PF13	AF9
	PH10	AF8
	PD11	AF6
	PB5	AF13
	PB9	AF12

12.3.5.16.5 I2C5 alternate function remapping

Table 12-58 I2C5 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C5_SCL	PF1	AF12
	PA8	AF10
	PC11	AF9
I2C5_SDA	PF0	AF11
	PC9	AF13
	PC10	AF9
I2C5_SMBA	PF2	AF12
	PA9	AF11

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Alternate function	GPIO port	Remap
	PC12	AF12

12.3.5.16.6 I2C6 alternate function remapping

Table 12-59 I2C6 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C6_SCL	PF4	AF12
	PF12	AF7
	PE14	AF10
I2C6_SDA	PF3	AF11
	PF11	AF5
	PE13	AF8
I2C6_SMBA	PF5	AF10
	PF13	AF10
	PE15	AF7

12.3.5.16.7 I2C7 alternate function remapping

Table 12-60 I2C7 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C7_SCL	PI13	AF7
	PE8	AF9
	PD9	AF6
I2C7_SDA	PI12	AF7
	PE7	AF8
	PD8	AF7
I2C7_SMBA	PI14	AF7
	PE9	AF9
	PD10	AF8

12.3.5.16.8 I2C8 alternate function remapping

Table 12-61 I2C8 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C8_SCL	PD15	AF9
	PJ9	AF9
	PG5	AF11
	PI3	AF10
I2C8_SDA	PD14	AF9
	PJ8	AF9
	PG4	AF10
	PI2	AF10

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Alternate function	GPIO port	Remap
I2C8_SMBA	PD13	AF9
	PJ10	AF8
	PG6	AF8
	PI1	AF10

12.3.5.16.9 I2C9 alternate function remapping

Table 12-62 I2C9 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C9_SCL	PI11	AF7
	PJ1	AF9
	PJ4	AF8
	PH15	AF9
I2C9_SDA	PI10	AF9
	PJ0	AF8
	PJ3	AF9
	PH14	AF10
I2C9_SMBA	PI9	AF9
	PJ2	AF7
	PH13	AF8

12.3.5.16.10 I2C10 alternate function remapping

Table 12-63 I2C10 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2C10_SCL	PI1	AF11
	PJ14	AF4
	PK4	AF5
	PK7	AF5
	PI6	AF9
I2C10_SDA	PI0	AF8
	PJ13	AF6
	PK3	AF5
	PK6	AF5
	PI5	AF10
I2C10_SMBA	PI3	AF11
	PJ12	AF6
	PK5	AF5
	PI4	AF9

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12.3.5.17 SPIx/I2Sx alternate function remapping

12.3.5.17.1 SPI1 alternate function remapping

Table 12-64 SPI1 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI1_NSS	PA4	AF4
	PA15	AF2
	PG10	AF8
SPI1_SCK	PA5	AF4
	PG11	AF6
	PB3	AF1
SPI1_MISO	PA6	AF4
	PG9	AF5
	PB4	AF2
SPI1_MOSI	PA7	AF5
	PD7	AF3

12.3.5.17.2 SPI2 alternate function remapping

Table 12-65 SPI2 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI2_NSS	PA11	AF2
	PI0	AF4
	PB4	AF3
SPI2_SCK	PB10	AF4
	PB13	AF4
	PA9	AF3
	PA12	AF1
	PI1	AF6
	PD3	AF4
SPI2_MISO	PC2	AF6
	PB14	AF4
	PI2	AF5
SPI2_MOSI	PC1	AF4
	PC3	AF6
	PB15	AF4
	PI3	AF5

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12.3.5.17.3 SPI3 alternate function remapping

Table 12-66 SPI3 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI3_NSS	PA4	AF5
	PA15	AF3
	PD4	AF4
SPI3_SCK	PC10	AF5
	PD7	AF4
	PB3	AF2
SPI3_MISO	PB1	AF6
	PC11	AF4
	PD5	AF4
	PB4	AF4
SPI3_MOSI	PB2	AF6
	PC12	AF5
	PD6	AF5

12.3.5.17.4 SPI4 alternate function remapping

Table 12-67 SPI4 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI4_NSS	PA0	AF3
	PA4	AF6
	PG8	AF4
	PA15	AF4
SPI4_SCK	PA5	AF5
	PC12	AF6
	PG13	AF5
	PB3	AF3
SPI4_MISO	PA6	AF5
	PG12	AF7
	PB4	AF5
SPI4_MOSI	PA7	AF6
	PB5	AF7
	PG14	AF6

12.3.5.17.5 SPI5 alternate function remapping

Table 12-68 SPI5 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI5_NSS	PF6	AF5

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Alternate function	GPIO port	Remap
	PH5	AF3
	PK1	AF3
SPI5_SCK	PF7	AF4
	PH6	AF5
	PK0	AF3
SPI5_MISO	PF8	AF5
	PH7	AF4
	PJ11	AF3
SPI5_MOSI	PF9	AF5
	PF11	AF3
	PJ10	AF3

12.3.5.17.6 SPI6 alternate function remapping

Table 12-69 SPI6 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI6_NSS	PE4	AF4
	PF2	AF5
	PE11	AF4
SPI6_SCK	PE2	AF4
	PF3	AF5
	PE12	AF5
SPI6_MISO	PE5	AF4
	PF4	AF6
	PE13	AF4
SPI6_MOSI	PE6	AF3
	PF5	AF5
	PE14	AF5

12.3.5.17.7 SPI7 alternate function remapping

Table 12-70 SPI7 Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI7_NSS	PI12	AF4
	PJ2	AF3
	PH12	AF6
	PH13	AF4
SPI7_SCK	PI8	AF3
	PJ1	AF4
SPI7_MISO	PI13	AF4
	PJ3	AF3
	PH14	AF5

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Alternate function	GPIO port	Remap
SPI7_MOSI	PI14	AF4
	PJ4	AF3
	PH15	AF6

12.3.5.17.8 I2S1 alternate function remapping

Table 12-71 I2S1 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2S1_CK	PA5	AF6
	PG11	AF7
	PB3	AF4
I2S1_CKIN	PC9	AF5
I2S1_MCK	PC4	AF5
I2S1_SDI	PA6	AF6
	PG9	AF6
	PB4	AF6
I2S1_SDO	PA7	AF7
	PD7	AF5
I2S1_WS	PA4	AF7
	PA15	AF5
	PG10	AF9

12.3.5.17.9 I2S2 alternate function remapping

Table 12-72 I2S2 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2S2_CK	PB10	AF5
	PB13	AF5
	PA9	AF4
	PA12	AF2
	PI1	AF7
	PD3	AF5
I2S2_CKIN	PC9	AF6
I2S2_MCK	PC6	AF6
I2S2_SDI	PC2	AF7
	PB14	AF5
	PI2	AF6
I2S2_SDO	PC1	AF5
	PC3	AF7
	PB15	AF5
	PI3	AF6
I2S2_WS	PA11	AF3

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Alternate function	GPIO port	Remap
	PI0	AF5
	PB4	AF7

12.3.5.17.10 I2S3 alternate function remapping

Table 12-73 I2S3 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2S3_CK	PC10	AF6
	PB3	AF5
I2S3_CKIN	PC9	AF7
I2S3_MCK	PC7	AF6
I2S3_SDI	PC11	AF5
	PB4	AF8
I2S3_SDO	PB2	AF7
	PC12	AF7
	PD6	AF6
I2S3_WS	PA4	AF8
	PA15	AF6

12.3.5.17.11 I2S4 alternate function remapping

Table 12-74 I2S4 Alternate Function Remapping

Alternate function	GPIO port	Remap
I2S4_CK	PA5	AF7
	PC12	AF8
	PG13	AF6
	PB3	AF6
I2S4_CKIN	PC9	AF8
I2S4_MCK	PA3	AF6
I2S4_SDI	PA6	AF7
	PG12	AF8
	PB4	AF9
I2S4_SDO	PA7	AF8
	PG14	AF7
I2S4_WS	PA0	AF4
	PA4	AF9
	PG8	AF5
	PA15	AF7

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12.3.5.17.12 SPI/I2S alternate function remapping

Table 12-75 SPI/I2S Alternate Function Remapping

Alternate function	GPIO port	Remap
SPI1_MOSI/I2S1_SDO	PB5	AF5
SPI3_MOSI/I2S3_SDO	PB5	AF6
SPI4_MOSI/I2S4_SDO	PB5	AF7
SPI2_NSS/I2S2_WS	PB9	AF5
	PB12	AF5

12.3.5.18 XSPIx alternate function remapping

12.3.5.18.1 XSPI1 alternate function remapping

Table 12-76 XSPI1 Alternate Function Remapping

Alternate function	GPIO port	Remap
XSPI_CLK	PF10	AF0
	PB2	AF0
	PA3	AF0
XSPI_IO0	PF8	AF0
	PA2	AF0
	PB1	AF0
	PD11	AF0
	PC9	AF0
	PC3	AF2
	PB12	AF0
XSPI_IO1	PF9	AF0
	PB0	AF0
	PD12	AF0
	PC10	AF0
XSPI_IO2	PA3	AF1
	PE2	AF0
	PF7	AF0
	PA7	AF1
	PB13	AF0
	PC2	AF2
XSPI_IO3	PA1	AF1
	PF6	AF0
	PA6	AF0
	PD13	AF0
XSPI_IO4	PC1	AF0
	PH2	AF2

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Alternate function	GPIO port	Remap
	PD4	AF0
	PE7	AF1
XSPI_IO5	PC2	AF3
	PH3	AF1
	PE8	AF2
	PD5	AF0
XSPI_IO6	PC3	AF3
	PD6	AF0
	PE9	AF2
	PG9	AF0
XSPI_IO7	PD7	AF0
	PE10	AF2
	PG14	AF0
XSPI_DQS	PB2	AF1
	PC5	AF1
	PA1	AF0
xSPI1_NCLK	PB12	AF1
	PI15	AF6
	PF11	AF1
xSPI1_NCS1	PB10	AF0
	PK7	AF0
	PB6	AF1
xSPI1_NCS2	PE7	AF2
	PC11	AF0
xSPI1_NCS3	PE8	AF3
	PE11	AF1
xSPI1_NCS4	PE9	AF3
	PG6	AF0
xSPI1_NCSIN	PE10	AF3
	PE1	AF1

12.3.5.18.2 XSPI2 alternate function remapping

Table 12-77 XSPI2 Alternate Function Remapping

Alternate function	GPIO port	Remap
XSPI2_CLK	PI13	AF0
	PF4	AF2
	PF10	AF1
	PB2	AF2
XSPI2_IO0	PI9	AF1

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Alternate function	GPIO port	Remap
	PF0	AF1
	PF8	AF1
	PB1	AF1
XSPI2_IO1	PI10	AF2
	PF1	AF2
	PF9	AF1
	PB0	AF1
XSPI2_IO2	PI11	AF0
	PF2	AF1
	PF7	AF1
	PA7	AF2
XSPI2_IO3	PI12	AF0
	PF3	AF1
	PF6	AF1
	PA6	AF1
XSPI2_IO4	PH2	AF3
	PJ1	AF0
	PG0	AF2
XSPI2_IO5	PH3	AF2
	PJ2	AF0
	PG1	AF2
XSPI2_IO6	PK3	AF0
	PG10	AF0
XSPI2_IO7	PK4	AF0
	PG11	AF0
XSPI2_DQS	PF12	AF1
	PG7	AF0
	PK6	AF0
	PG15	AF1
XSPI2_NCLK	PI14	AF0
	PF5	AF1
XSPI2_NCS1	PE5	AF0
	PG12	AF0
	PK5	AF0
XSPI2_NCS2	PG0	AF3
	PE7	AF3
	PI4	AF1
XSPI2_NCS3	PG1	AF3
	PI5	AF2
XSPI2_NCS4	PG10	AF1

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Alternate function	GPIO port	Remap
	PI6	AF1
XSPI2_NCSIN	PG11	AF1
	PI7	AF2

12.3.5.19 ETHx alternate function remapping

12.3.5.19.1 ETH1 alternate function remapping

Table 12-78 ETH1 Alternate Function Remapping

Alternate function	GPIO port	Remap
ETH1_CLK125	PD10	AF1
ETH1_GMII_GTX_CLK	PF5	AF2
ETH1_MII_RXD0/ETH1_RMII_RXD0/ETH1_GMII_RXD0	PC4	AF1
ETH1_MII_RXD1/ETH1_RMII_RXD1/ETH1_GMII_RXD1	PC5	AF2
ETH1_MII_RXD2/ETH1_GMII_RXD2	PB0	AF2
	PH6	AF2
ETH1_MII_RXD3/ETH1_GMII_RXD3	PB1	AF2
	PH7	AF1
ETH1_GMII_RXD4	PE12	AF2
	PH8	AF2
ETH1_GMII_RXD5	PE13	AF1
	PH9	AF1
ETH1_GMII_RXD6	PE14	AF2
	PH10	AF2
ETH1_GMII_RXD7	PE15	AF1
	PH11	AF1
ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_GMII_TXD0	PB12	AF2
	PG13	AF0
ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1	PB13	AF1
	PG12	AF1
	PG14	AF1
ETH1_MII_TXD2/ETH1_GMII_TXD2	PE3	AF0
	PC2	AF4
	PB7	AF0
ETH1_MII_TXD3/ETH1_GMII_TXD3	PE2	AF1
	PB8	AF0
ETH1_GMII_TXD4	PF0	AF2
	PI4	AF2
ETH1_GMII_TXD5	PF1	AF3
	PI5	AF3
ETH1_GMII_TXD6	PF2	AF2

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Alternate function	GPIO port	Remap
	PI6	AF2
ETH1_GMII_TXD7	PF3	AF2
	PI7	AF3
ETH1_ MDC	PC1	AF1
ETH1_MDIO	PA2	AF1
ETH1_MII_COL/ETH1_GMII_COL	PH3	AF3
	PA3	AF2
ETH1_MII_CRS/ETH1_GMII_CRS	PA0	AF0
	PH2	AF4
ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK/ETH1_GMII_RX_CLK	PA1	AF2
ETH1_MII_RX_DV/ETH1_RMII_CRS_DV/ETH1_GMII_RX_DV	PA7	AF3
ETH1_MII_RX_ER/ETH1_GMII_RX_ER	PI10	AF3
	PB10	AF1
ETH1_MII_TX_CLK/ETH1_GMII_TX_CLK	PC3	AF4
ETH1_MII_TX_EN/ETH1_RMII_TX_EN/ETH1_GMII_TX_EN	PB11	AF0
	PG11	AF2
ETH1_MII_TX_ER/ETH1_GMII_TX_ER	PB2	AF3
	PA9	AF0
ETH1_PHY_INTN	PD15	AF1
	PG7	AF1
	PG15	AF2
	PB4	AF0
ETH1_PPS_OUT	PD14	AF2
	PG8	AF2
	PB5	AF2

12.3.5.19.2 ETH2 alternate function remapping

Table 12-79 ETH2 Alternate Function Remapping

Alternate function	GPIO port	Remap
ETH2_MII_RXD0/ETH2_RMII_RXD0	PG2	AF2
	PI1	AF2
	PG9	AF1
ETH2_MII_RXD1/ETH2_RMII_RXD1	PG3	AF0
	PI2	AF1
	PG10	AF2
ETH2_MII_RXD2	PJ8	AF0
	PG4	AF1
ETH2_MII_RXD3	PJ9	AF0
	PG5	AF2

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Alternate function	GPIO port	Remap
ETH2_MII_TX_CLK	PI8	AF0
	PG0	AF4
ETH2_MII_TX_EN/ETH2_RMII_TX_EN	PF11	AF6
	PH13	AF1
ETH2_MII_TX_ER	PG1	AF4
	PJ5	AF0
ETH2_MII_TXD0/ETH2_RMII_TXD0	PH4	AF0
	PF12	AF2
	PH14	AF1
ETH2_MII_TXD1/ETH2_RMII_TXD1	PH5	AF1
	PF13	AF2
	PH15	AF2
ETH2_MII_TXD2	PJ0	AF0
	PF14	AF1
ETH2_MII_TXD3	PJ1	AF1
	PF15	AF2
ETH2_PHY_INTN	PE4	AF0
	PE7	AF4
	PD15	AF2
ETH2_PPS_OUT	PF10	AF2
	PI15	AF0
	PD10	AF2
ETH2_MDC	PF7	AF2
ETH2_MDIO	PF6	AF2
ETH2_MII_COL	PF8	AF2
	PK0	AF0
ETH2_MII_CRS	PF9	AF2
	PK1	AF0
ETH2_MII_RX_CLK/ETH2_RMII_REF_CLK	PF4	AF3
	PJ4	AF0
	PA8	AF0
ETH2_MII_RX_DV/ETH2_RMII_CRS_DV	PC0	AF2
	PJ3	AF0
	PH12	AF2
ETH2_MII_RX_ER	PG6	AF1
	PI3	AF2

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12.3.5.20 ESC alternate function remapping

Table 12-80 ESC Alternate Function Remapping

Alternate function	GPIO port	Remap
ESC_EEPROM_CLK	PE5	AF8
	PE8	AF12
	PJ10	AF9
ESC_EEPROM_DATA	PE6	AF6
	PE9	AF11
	PJ11	AF8
ESC_IRQ	PJ5	AF6
	PC8	AF9
	PD3	AF10
	PI6	AF11
ESC_LATCH0	PI9	AF11
	PC0	AF10
	PD11	AF7
	PK7	AF6
ESC_LATCH1	PD6	AF10
	PK4	AF6
	PI5	AF11
ESC_LED_ERR	PB2	AF12
	PD8	AF9
	PK0	AF7
	PG15	AF9
	PD0	AF10
ESC_LED_RUN	PA4	AF13
	PE15	AF8
	PK1	AF7
ESC_LED_STATE_RUN	PE4	AF8
	PA5	AF11
	PE10	AF8
	PJ15	AF4
ESC_LINK_ACT0	PD12	AF11
	PC12	AF13
	PG15	AF8
	PH2	AF10
ESC_P1_MII_TX_EN	PH2	AF11
ESC_LINK_ACT1	PA11	AF11
	PD7	AF10
	PI7	AF9
ESC_MDC	PF7	AF11
	PC1	AF9
	PE12	AF10
	PC7	AF12
ESC_MDIO	PF6	AF12

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Alternate function	GPIO port	Remap
	PE13	AF11
	PA2	AF8
	PC6	AF13
ESC_P1_LINK	PA2	AF9
ESC_P0_LINK	PE11	AF8
	PK2	AF6
	PE0	AF11
ESC_P0_MII_RX_CLK	PF5	AF11
	PA1	AF10
ESC_P0_MII_RX_DV	PA0	AF12
	PA7	AF13
ESC_P0_MII_RX_ER	PI10	AF10
	PH3	AF9
	PB10	AF12
ESC_P0_MII_RXD0	PF8	AF11
	PC4	AF7
ESC_P0_MII_RXD1	PF9	AF12
	PC5	AF9
ESC_P0_MII_RXD2	PB0	AF10
	PH6	AF12
	PH10	AF9
ESC_P0_MII_RXD3	PB1	AF11
	PH7	AF11
	PH11	AF10
ESC_P0_MII_TX_CLK	PC3	AF9
ESC_P0_MII_TX_EN	PB11	AF9
	PG11	AF10
ESC_P0_MII_TXD0	PB12	AF3
	PG13	AF11
ESC_P0_MII_TXD1	PB13	AF13
	PG12	AF13
	PG14	AF12
ESC_P0_MII_TXD2	PE3	AF6
	PC2	AF10
	PC10	AF11
	PJ12	AF7
	PB7	AF13
ESC_P0_MII_TXD3	PE2	AF8
	PC11	AF11
	PJ13	AF7
ESC_P1_LINK	PA6	AF12
	PG8	AF9
	PA10	AF8
ESC_P1_MII_RX_CLK	PF4	AF13
	PJ4	AF9

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Alternate function	GPIO port	Remap
	PA8	AF11
ESC_P1_MII_RX_DV	PJ3	AF10
	PH12	AF12
	PC0	AF9
ESC_P1_MII_RX_ER	PG6	AF9
	PI3	AF12
ESC_P1_MII_RXD0	PG2	AF10
	PI1	AF12
	PG9	AF9
ESC_P1_MII_RXD1	PG3	AF8
	PI2	AF12
	PG10	AF12
ESC_P1_MII_RXD2	PJ8	AF10
	PG4	AF11
ESC_P1_MII_RXD3	PJ9	AF10
	PG5	AF12
ESC_P1_MII_TX_CLK	PI8	AF6
	PG0	AF10
ESC_P1_MII_TX_EN	PF10	AF9
	PF11	AF7
	PH13	AF9
ESC_P1_MII_TXD0	PH4	AF10
	PF12	AF8
	PH14	AF11
ESC_P1_MII_TXD1	PH5	AF10
	PF13	AF13
	PH15	AF10
ESC_P1_MII_TXD2	PJ0	AF9
	PF14	AF10
ESC_P1_MII_TXD3	PJ1	AF10
	PF15	AF10
ESC_RESET_IN	PI11	AF8
	PI0	AF9
	PE1	AF10
ESC_RESET_OUT	PD13	AF10
	PC6	AF13
	PD1	AF9
ESC_SYNC0	PD9	AF8
	PA9	AF12
	PI4	AF11
ESC_SYNC1	PJ2	AF8
	PA12	AF11
	PD5	AF9

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12.3.5.21 SDRAM alternate function remapping

12.3.5.21.1 SDRAM alternate function remapping

Table 12-81 SDRAM Alternate Function Remapping

Alternate function	GPIO port	Remap
SDRAM_A0	PF0	AF0
	PE8	AF1
SDRAM_A1	PF1	AF0
	PE9	AF1
SDRAM_A2	PF2	AF0
	PE10	AF1
SDRAM_A3	PF3	AF0
	PE11	AF7
SDRAM_A4	PF4	AF0
	PH6	AF1
SDRAM_A5	PF5	AF0
	PH7	AF10
SDRAM_A6	PF12	AF0
	PH8	AF1
SDRAM_A7	PF13	AF0
	PH9	AF11
SDRAM_A8	PF14	AF0
	PH10	AF1
SDRAM_A9	PF15	AF0
	PH11	AF9
SDRAM_A10	PG0	AF0
	PG1	AF1
SDRAM_A11	PG1	AF0
	PH12	AF1
SDRAM_A12	PG2	AF0
SDRAM_BA0	PG4	AF0
	PF15	AF1
SDRAM_BA1	PG5	AF0
	PG0	AF1
SDRAM_CKE0	PC3	AF0
	PH2	AF0
	PC5	AF0
	PD14	AF1
SDRAM_CKE1	PH7	AF0
	PB5	AF0

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SDRAM_CLK	PG8	AF0
SDRAM_D0	PD14	AF0
	PI4	AF10
SDRAM_D1	PD15	AF0
	PI5	AF1
SDRAM_D2	PD0	AF0
	PI6	AF10
SDRAM_D3	PD1	AF0
	PI7	AF1
SDRAM_D4	PE7	AF0
	PF4	AF1
SDRAM_D5	PE8	AF0
	PF1	AF1
SDRAM_D6	PE9	AF0
	PC12	AF0
	PI9	AF10
SDRAM_D7	PE10	AF0
	PD2	AF0
	PI10	AF1
SDRAM_D8	PA4	AF0
	PE11	AF0
	PI1	AF1
SDRAM_D9	PA5	AF0
	PE12	AF0
	PI2	AF11
SDRAM_D10	PE13	AF0
	PB14	AF0
	PI3	AF1
SDRAM_D11	PE14	AF0
	PB15	AF0
	PD0	AF1
SDRAM_D12	PC0	AF1
	PE15	AF0
	PD1	AF1
SDRAM_D13	PD8	AF0
	PD2	AF1
SDRAM_D14	PD9	AF0
	PG15	AF7
SDRAM_D15	PD10	AF0
	PE1	AF9

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SDRAM_D16	PH8	AF0
SDRAM_D17	PH9	AF0
SDRAM_D18	PH10	AF0
SDRAM_D19	PH11	AF0
SDRAM_D20	PH12	AF0
SDRAM_D21	PH13	AF0
SDRAM_D22	PH14	AF0
SDRAM_D23	PH15	AF0
SDRAM_D24	PI0	AF0
SDRAM_D25	PI1	AF0
SDRAM_D26	PI2	AF0
SDRAM_D27	PI3	AF0
SDRAM_D28	PI6	AF0
SDRAM_D29	PI7	AF0
SDRAM_D30	PI9	AF0
SDRAM_D31	PI10	AF0
SDRAM_DQM0	PE0	AF0
	PA5	AF1
SDRAM_DQM1	PE1	AF0
	PG2	AF1
SDRAM_DQM2	PI4	AF0
SDRAM_DQM3	PI5	AF0
SDRAM_NRAS	PF11	AF0
SDRAM_NCAS	PG15	AF0
	PC5	AF7
SDRAM_NCE0	PC2	AF0
	PH3	AF0
	PC4	AF0
	PF13	AF1
SDRAM_NCE1	PH6	AF0
	PB6	AF0
SDRAM_NWE	PC0	AF0
	PH5	AF0
	PA7	AF0

12.3.5.22 LCD alternate function remapping

Table 12-82 LCD Alternate Function Remapping

Alternate function	GPIO port	Remap
	PE4	AF2

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Alternate function	GPIO port	Remap
LCD_B0	PJ12	AF2
	PG14	AF5
LCD_B1	PA10	AF0
	PD0	AF4
	PJ13	AF2
	PG12	AF4
	PC10	AF3
LCD_B2	PA3	AF4
	PC9	AF2
	PD2	AF4
	PD6	AF3
	PJ14	AF1
	PG10	AF5
LCD_B3	PD10	AF4
	PA8	AF1
	PJ15	AF1
	PG11	AF4
LCD_B4	PA10	AF1
	PJ13	AF3
	PG12	AF5
	PE12	AF4
	PC11	AF2
	PK3	AF2
	PI4	AF4
LCD_B5	PA3	AF5
	PK4	AF2
	PB5	AF3
	PI5	AF5
LCD_B6	PA15	AF0
	PK5	AF2
	PB8	AF4
	PI6	AF4
LCD_B7	PD2	AF5
	PK6	AF2
	PB9	AF3
	PI7	AF5
LCD_G0	PE5	AF2
	PB1	AF3
	PJ7	AF1
LCD_G1	PE6	AF1
	PB0	AF3
	PJ8	AF1

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Alternate function	GPIO port	Remap
LCD_G2	PC0	AF5
	PA6	AF2
	PI15	AF1
	PJ9	AF1
	PH13	AF3
LCD_G3	PJ12	AF3
	PG10	AF6
	PC9	AF3
	PE11	AF3
	PJ10	AF1
	PH14	AF3
LCD_G4	PH4	AF1
	PB10	AF3
	PJ11	AF1
	PH15	AF4
LCD_G5	PH4	AF2
	PC1	AF3
	PB11	AF2
	PK0	AF1
	PI0	AF2
LCD_G6	PI11	AF4
	PK1	AF1
	PC7	AF4
	PI1	AF4
LCD_G7	PB15	AF3
	PK2	AF1
	PG8	AF3
	PI2	AF3
	PD3	AF2
LCD_R0	PI15	AF2
	PH2	AF5
	PG13	AF4
	PE0	AF3
LCD_R1	PA2	AF2
	PH3	AF4
	PJ0	AF1
LCD_R2	PA1	AF3
	PJ1	AF2
	PH8	AF4
	PC10	AF2
LCD_R3	PA15	AF1
	PB0	AF4

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Alternate function	GPIO port	Remap
	PJ2	AF1
	PH9	AF3
LCD_R4	PA5	AF3
	PJ3	AF1
	PH10	AF4
	PA11	AF1
LCD_R5	PC0	AF6
	PJ4	AF1
	PH11	AF3
	PA9	AF1
	PA12	AF0
LCD_R6	PA8	AF2
	PB1	AF4
	PJ5	AF1
	PH12	AF4
	PC12	AF3
	PE1	AF3
LCD_R7	PJ0	AF2
	PC4	AF4
	PE15	AF3
	PJ6	AF1
	PG6	AF3
LCD_CLK	PI14	AF2
	PE14	AF4
	PB14	AF3
	PG7	AF3
LCD_DE	PF10	AF3
	PC5	AF4
	PE13	AF3
	PK7	AF2
LCD_HSYNC	PI10	AF5
	PI12	AF2
	PC6	AF4
LCD_VSYNC	PI9	AF3
	PI13	AF2
	PA4	AF2
	PA7	AF4

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12.3.5.23 SDMMCx alternate function remapping

12.3.5.23.1 SDMMC1 alternate function remapping

Table 12-83 SDMMC1 Alternate Function Remapping

Alternate function	GPIO port	Remap
SDMMC1_CD	PD1	AF2
SDMMC1_CDIR	PB9	AF0
SDMMC1_D0	PB13	AF2
	PC8	AF0
SDMMC1_D0DIR	PC6	AF0
SDMMC1_D1	PC9	AF1
SDMMC1_D2	PC10	AF1
SDMMC1_D3	PC11	AF1
SDMMC1_D4	PB8	AF2
	PD14	AF3
SDMMC1_D5	PB9	AF1
	PD15	AF3
SDMMC1_D6	PC6	AF1
	PB6	AF2
SDMMC1_D7	PC7	AF1
	PB7	AF1
SDMMC1_CK	PC12	AF1
SDMMC1_CKIN	PB8	AF1
SDMMC1_CMD	PD2	AF2
SDMMC1_D123DIR	PC7	AF0
SDMMC1_LEDCTRL	PI11	AF1
	PF9	AF3
	PE8	AF4
SDMMC1_RST	PD3	AF0
SDMMC1_SEL	PI8	AF1
	PA11	AF0
	PJ12	AF0
SDMMC1_WP	PD0	AF2

12.3.5.23.2 SDMMC2 alternate function remapping

Table 12-84 SDMMC2 Alternate Function Remapping

Alternate function	GPIO port	Remap
SDMMC2_CD	PD5	AF1
SDMMC2_CDIR	PG5	AF3
SDMMC2_D0	PB14	AF1
	PG9	AF2
SDMMC2_D0DIR	PG13	AF1
SDMMC2_D1	PB15	AF1
	PG10	AF3
SDMMC2_D2	PG11	AF3

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Alternate function	GPIO port	Remap
	PB3	AF0
SDMMC2_D3	PG12	AF2
	PB4	AF1
SDMMC2_D4	PG4	AF3
	PB8	AF3
SDMMC2_D5	PG5	AF4
	PB9	AF2
SDMMC2_D6	PG13	AF2
	PC6	AF2
SDMMC2_D7	PG14	AF3
	PC7	AF2
SDMMC2_CK	PC1	AF2
	PD6	AF1
SDMMC2_CKIN	PC4	AF2
	PG4	AF2
SDMMC2_CMD	PA0	AF1
	PD7	AF1
SDMMC2_D123DIR	PG14	AF2
SDMMC2_LEDCTRL	PI11	AF2
	PF8	AF3
	PE9	AF4
SDMMC2_RST	PG15	AF3
SDMMC2_SEL	PI8	AF2
	PC5	AF8
	PJ13	AF0
SDMMC2_WP	PD4	AF1

12.3.5.24 USBx_HS alternate function remapping

12.3.5.24.1 USB1_HS alternate function remapping

Table 12-85 USB1_HS Alternate Function Remapping

Alternate function	GPIO port	Remap
USB1_SOF	PA8	AF8
USB1_VBUS	PA9	AF9
USB1_ID	PA10	AF7
USB1_DM	PA11	AF10
USB1_DP	PA12	AF10

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12.3.5.24.2 USB2_HS alternate function remapping

Table 12-86 USB2_HS Alternate Function Remapping

Alternate function	GPIO port	Remap
USB2_SOF	PA4	AF12
USB2_ID	PB12	AF11
USB2_VBUS	PB13	AF11
USB2_DM	PB14	AF12
USB2_DP	PB15	AF11

12.3.5.25 DSMU alternate function remapping

Table 12-87 DSMU Alternate Function Remapping

Alternate function	GPIO port	Remap
DSMU_CKIN0	PC0	AF7
DSMU_CKIN1	PB2	AF11
	PB13	AF12
	PC2	AF8
	PD7	AF8
DSMU_CKIN2	PC4	AF6
	PE8	AF10
	PB15	AF12
DSMU_CKIN3	PE5	AF7
	PD8	AF8
	PC6	AF11
DSMU_CKIN4	PE11	AF6
	PC1	AF6
	PD6	AF8
DSMU_CKIN5	PE13	AF9
	PC10	AF10
	PB7	AF12
DSMU_CKIN6	PF14	AF9
	PD0	AF9
DSMU_CKIN7	PB11	AF8
	PB8	AF13
DSMU_DATIN0	PC1	AF7
DSMU_DATIN1	PD6	AF9
	PC3	AF8
	PB1	AF10
	PB12	AF13
DSMU_DATIN2	PC5	AF5

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Alternate function	GPIO port	Remap
	PE7	AF9
	PB14	AF13
DSMU_DATIN3	PE4	AF7
	PD9	AF7
	PC7	AF11
DSMU_DATIN4	PE10	AF7
	PC0	AF8
	PD7	AF9
DSMU_DATIN5	PE12	AF8
	PC11	AF10
	PB6	AF13
DSMU_DATIN6	PF13	AF11
	PD1	AF8
DSMU_DATIN7	PB10	AF11
	PB9	AF13
DSMU_CKOUT	PC2	AF9
	PB0	AF9
	PE9	AF10
	PD10	AF9
	PD3	AF9

12.3.5.26 EVENT alternate function remapping

EVENT supports full pin mapping, as detailed in the table below.

Table 12-88 EVENT Alternate Function Remapping

Alternate function	GPIO port	Remap
EVENT_OUT	PAx（x=0~15）	AF14
	PBx（x=0~15）	AF14
	PCx（x=0~15）	AF14
	PDx（x=0~15）	AF14
	PEx（x=0~15）	AF14
	PFx（x=0~15）	AF14
	PGx（x=0~15）	AF14
	PHx（x=0~15）	AF14
	PIx（x=0~15）	AF14
	PJx（x=0~15）	AF14
	PKx（x=0~7）	AF14

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12.3.5.27 COMP alternate function remapping

12.3.5.27.1 COMP1 alternate function remapping

Table 12-89 COMP1 Alternate Function Remapping

Alternate function	GPIO port	Remap
COMP1_OUT	PC5	AF6
	PE12	AF9

12.3.5.27.2 COMP2 alternate function remapping

Table 12-90 COMP2 Alternate Function Remapping

Alternate function	GPIO port	Remap
COMP2_OUT	PE8	AF11
	PE13	AF10

12.3.5.27.3 COMP3 alternate function remapping

Table 12-91 COMP3 Alternate Function Remapping

Alternate function	GPIO port	Remap
COMP3_OUT	PF0	AF12
	PF13	AF12

12.3.5.27.4 COMP4 alternate function remapping

Table 12-92 COMP4 Alternate Function Remapping

Alternate function	GPIO port	Remap
COMP4_OUT	PH8	AF12
	PH12	AF11

12.3.5.28 RTC alternate function remapping

Table 12-93 RTC alternate function remapping

Alternate function	GPIO port	Remap
RTC_REFIN	PB15	AF15
RTC_OUT2	PB2	AF15

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Alternate function	GPIO port	Remap
RTC_OUT2	PI8	AF15

12.3.6 IO Configuration of Peripherals

Table 12-94 ADC/DAC

ADC/DAC Pin	GPIO Configuration
ADC	Analog mode
DAC	Analog mode

Table 12-95 SHRTIM

SHRTIM Pin	Configuration	GPIO Configuration
SHRTIM1/2_CHx1(x=A~F)	Output compare channel x	Push-pull alternate output
SHRTIM1/2_CHx2(x=A~F)	Complementary output channel x	Push-pull alternate output
SHRTIM1/2_FLTx(x=1~6)	Fault input x	Alternate input mode
SHRTIM1/2_SCIN	Synchronous signal input	Alternate input mode
SHRTIM1/2_SCOUT	Synchronous signal output	Push-pull alternate output
SHRTIM1/2_EXEVx(x=1~10)	External event input x	Alternate input mode

Table 12-96 ATIM1/2/3/4

ATIM Pin	Configuration	GPIO Configuration
ATIM1/2/3/4_CHx(x=1~4)	Input capture channel x	Alternate input mode
	Output compare channel x	Push-pull alternate output
ATIM1/2/3/4_CHxN(x=1~4)	Complementary output channel x	Push-pull alternate output
ATIM1/2/3/4_BKIN1	break input	Alternate input mode
ATIM1/2/3/4_BKIN2	Bidirectional break	Open-drain alternate output
ATIM1/2/3/4_ETR	External trigger clock input	Alternate input mode

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Table 12-97 GTIMA1~7

GTIM pin	Configuration	GPIO Configuration
GTIMA1~7_CHx(x=1~4)	Input capture channel x	Alternate input mode
	Output compare channel x	Push-pull alternate output
GTIMA1~7_ETR	External trigger clock input	Alternate input mode

Table 12-98 GTIMB1/2/3

GTIM pin	Configuration	GPIO Configuration
GTIMB1/2/3_CHx(x=1P,2,34)	Input capture channel x	Alternate input mode
	Output compare channel x	Push-pull alternate output
GTIMB1/2/3_CH1N	Complementary output channel 1	Push-pull alternate output
GTIMB1/2/3_BKIN	Break input	Alternate input mode
	Bidirectional break	Open-drain alternate output
GTIMB1/2/3_ETR	External trigger clock input	Alternate input mode

Table 12-99 LPTIM1/2/3/4/5

LPTIM Pin	Configuration	GPIO Configuration
LPTIM1/2/3/4/5_INx(x=1，2)	Input channel x	Alternate input mode
LPTIM1/2/3/4/5_OUT	PWM output	Push-pull alternate output
LPTIM1/2/3/4/5_ETR	External trigger input	Alternate input mode

Table 12-100 FDCAN1/2/3/4/5/6/7/8

FDCAN Pin	GPIO Configuration
FDCAN1/2/3/4/5/6/7/8_TX	Push-pull alternate output
FDCAN1/2/3/4/5/6/7/8_RX	Alternate input mode

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Table 12-101 DVP1/2

DVP Pin	GPIO Configuration
DVP1/2_HSYNC	Alternate input mode
DVP1/2_VSYNC	Alternate input mode
DVP1/2_PCLK	Alternate input mode
DVP1/2_Dx（x=0~7）	Alternate input mode

Table 12-102 FEMC

FEMC Pin	GPIO Configuration
FEMC_Ax（x=0~25）	Push-pull alternate output
FEMC_Dx（x=0~31） FEMC_DAx (x=0~15）	Push-pull alternate output
FEMC_CLK	Push-pull alternate output
FEMC_NOE	Push-pull alternate output
FEMC_NWE	Push-pull alternate output
FEMC_NE（x=1~4）	Push-pull alternate output
FEMC_NCE（x=1,2）	Push-pull alternate output
FEMC_ALE	Push-pull alternate output
FEMC_CLE	Push-pull alternate output
FEMC_NBLx（x=0~3）	Push-pull alternate output
FEMC_NADV/NL	Push-pull alternate output
FEMC_NWAIT	Alternate input mode
FEMC_INT/BUSY	Alternate input mode
FEMC_BAA	Push-pull alternate output
FEMC_CRE	Push-pull alternate output

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Table 12-103 U(S)ARTx (USART : x = {1..8}, UART : x ={1..7})

U(S)ART Pin	Configuration	GPIO Configuration
U(S)ARTx_TX	Full duplex transmissions	Push-pull alternate output
	Half duplex synchronous mode	Push-pull alternate output + Pull-up
	Single-wire mode	Alternate input mode
U(S)ARTx_RX	Full duplex transmissions	Alternate input mode
	Half duplex synchronous mode	Unused, can be used as general I/O.
USARTx_CK	Synchronous mode	Push-pull alternate output
U(S)ARTx_RTS_DE	Hardware flow control	Push-pull alternate output
U(S)ARTx_CTS	Hardware flow control	Alternate input mode

Table 12-104 LPUART1/2

LPUART Pin	Configuration	GPIO Configuration
LPUARTx_TX	Full duplex transmissions	Push-pull alternate output
	Half duplex synchronous mode	Push-pull alternate output + Pull-up
	Single-wire mode	Alternate input mode
LPUARTx_RX	Full duplex transmissions	Alternate input mode
	Half duplex synchronous mode	Unused, can be used as general I/O.
LPUARTx_RTS_DE	Hardware flow control	Push-pull alternate output
LPUARTx_CTS	Hardware flow control	Alternate input mode

Table 12-105 I2C (x= {1…10})

I2C Pin	Configuration	GPIO Configuration
I2Cx_SCL	I2C clock	Open-drain alternate output
I2Cx_SDA	I2C data	Open-drain alternate output
I2Cx_SMBA	SMBA data	Push-pull alternate output

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Table 12-106 SPI(x={1..7})

SPI Pin	Configuration	GPIO Configuration
SPIx_SCK	Master mode	Push-pull alternate output
	Slave mode	Alternate input mode
SPIx_MOSI	Full-duplex mode / Master mode	Push-pull alternate output
	Full-duplex mode / Slave mode	Alternate input mode
	Simplex bidirectional data line /	Push-pull alternate output
	Simplex bidirectional data line /	Unused, can be used as general I/O.
SPIx_MISO	Full-duplex mode / Master mode	Push-pull alternate output
	Full-duplex mode / Slave mode	Alternate input mode
	Simplex bidirectional data line /	Push-pull alternate output
	Simplex bidirectional data line /	Unused, can be used as general I/O.
SPIx_NSS	Hardware slave mode	Alternate input mode
	Hardware master mode / NSS output	Push-pull alternate output
	Software mode	Unused, can be used as general I/O.

Table 12-107 I2S (x={1..4})

I2S Pin	Configuration	GPIO Configuration
I2Sx_WS	Master mode	Push-pull alternate output
	Slave mode	Alternate input mode
I2Sx_CK	Master mode	Push-pull alternate output
	Slave mode	Alternate input mode
I2Sx_SDI	Transmitter	Push-pull alternate output
	Receiver	Alternate input mode
I2Sx_SDO	Transmitter	Alternate input mode
	Receiver	Push-pull alternate output
I2Sx_MCK	Master mode	Push-pull alternate output
	Slave mode	Unused, can be used as general I/O.

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I2S Pin	Configuration	GPIO Configuration
I2S_CKIN	-	Alternate input mode

Table 12-108 DSMU

DSMU Pin	Configuration	GPIO Configuration
DSMU_CKINx(0~7)	Synchronous signal input	Input mode
DSMU_CKOUT	Synchronous signal inout (in & out)	Inout mode
DSMU_DATINx（x=0~7）	Synchronous signal input	Input mode

Table 12-109 XSPI1/2

XSPI Pin	Configuration	GPIO Configuration
XSPI1/2_IO x（x=0~7）	Master /Slave mode	Push-pull alternate output
XSPI1/2_CLK	Chip select output signals	Alternate function mode
XSPI1/2_NCLK	Negative clock output signals	Alternate function mode
XSPI1/2_DQS	Data strobe input signals	Alternate function mode
XSPI1/2_NCSIN	Slave select inputs	Alternate function mode
XSPI1/2_NCSx (x=1..4)	Chip select output signals	Alternate function mode

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Table 12-110 ETH1/2

ETH Pin	GPIO Configuration
ETH1/2_MDC	Push-pull alternate output + fast toggle
ETH1/2_MDIO	Push-pull alternate output + fast toggle
ETH1/2_PPS_OUT	Push-pull alternate output
ETH1/2_PHY_INTN	Alternate input mode
ETH1/2_MII_CRS/ETH1_GMII_CRS	Alternate input mode
ETH1/2_MII_COL/ETH1_GMII_COL	Alternate input mode
ETH1/2_MII_RX_ER/ETH1_GMII_RX_ER	Alternate input mode
ETH1/2_MII_RX_DV/ETH1_GMII_RX_DV/	Alternate input mode
ETH1/2_MII_RXD3/ ETH1_GMII_RXD3	Alternate input mode
ETH1/2_MII_RXD2/ ETH1_GMII_RXD2	Alternate input mode
ETH1/2_MII_RXD1/ ETH1_GMII_RXD1/	Alternate input mode
ETH1/2_MII_RXD0/ETH1_GMII_RXD0/	Alternate input mode
ETH1_GMII_RXDx (x=4..7)	Alternate input mode
ETH1/2_MII_RX_CLK/ETH1_GMII_RX_CLK/	Alternate input mode
ETH1/2_MII_TX_EN/ETH1_GMII_TX_EN/	Push-pull alternate output + fast toggle
ETH1/2_MII_TX_ER/ETH1_GMII_TX_ER	Push-pull alternate output
ETH1/2_MII_TX_CLK/ ETH1_GMII_TX_CLK	Alternate input mode
ETH1/2_MII_TXD3/ ETH1_GMII_TXD3	Push-pull alternate output + fast toggle
ETH1/2_MII_TXD2/ ETH1_GMII_TXD2	Push-pull alternate output + fast toggle
ETH1/2_MII_TXD1/ ETH1_GMII_TXD1/	Push-pull alternate output + fast toggle
ETH1/2_MII_TXD0/ ETH1_GMII_TX_EN/	Push-pull alternate output + fast toggle
ETH1_GMII_TXDx (x=4..7)	Push-pull alternate output + fast toggle
ETH1_CLK125	Alternate input mode
ETH1_GMII_GTX_CLK	Push-pull alternate output

Table 12-111 USBHS Dualrole

USB Pin	GPIO Configuration
USB_HS_DM	Push-pull alternate output
USB_HS_ID	Alternate input mode
USB_HS_SOF	Push-pull alternate output
USB_VBUS	Alternate input mode

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Table 12-112 ESC

ESC Pin	GPIO Configuration
ESC_EEPROM_CLK	Alternate function mode
ESC_EEPROM_DATA	Alternate function mode
ESC_IRQ	Alternate function mode
ESC_LATCH[1:0]	Alternate input mode
ESC_LED_ERR	Alternate function mode
ESC_LED_RUN	Alternate function mode
ESC_LED_STATE_RUN	Alternate function mode
ESC_LINK_ACT[1:0]	Alternate function mode
ESC_MDC	Alternate function mode
ESC_MDIO	Alternate function mode
ESC_RESET_OUT	Alternate function mode
ESC_RESET_IN	Alternate input mode
ESC_P0_LINK	Alternate input mode
ESC_P0_MII_RX_CLK	Alternate input mode
ESC_P0_MII_RX_DV	Alternate input mode
ESC_P0_MII_RX_ER	Alternate input mode
ESC_P0_MII_RXD[3:0]	Alternate function mode
ESC_P0_MII_TX_CLK	Alternate function mode
ESC_P0_MII_TX_EN	Alternate function mode
ESC_P0_MII_TXD[3:0]	Alternate function mode
ESC_P1_MII_RX_CLK	Alternate input mode
ESC_P1_MII_RX_DV	Alternate input mode
ESC_P1_MII_RX_ER	Alternate input mode
ESC_P1_MII_RXD[3:0]	Alternate function mode
ESC_P1_MII_TX_CLK	Alternate function mode
ESC_P1_MII_TX_EN	Alternate function mode
ESC_P1_MII_TXD[3:0]	Alternate function mode
ESC_P1_LINK	Alternate input mode
ESC_SYNC[1:0]	Alternate function mode

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Table 12-113 SDRAM

SDRAM Pin	Configuration	GPIO Configuration
SDRAM_A[12:0]	Output address signals	Alternate function mode
SDRAM_BA[1:0]	Output bank address signals	Alternate function mode
SDRAM_NCAS	Output column address signal	Alternate function mode
SDRAM_NCE[1:0]	Output chip enable signal	Alternate function mode
SDRAM_CKE[1:0]	Output clock enable signal	Alternate function mode
SDRAM_CLK	Output clock signal	Alternate function mode
SDRAM_D[31:0]	Bidirectional data signals	Alternate function mode
SDRAM_DMQ[3:0]	Output data mask signal	Alternate function mode
SDRAM_NRAS	Output row address strobe signal	Alternate function mode
SDRAM_NWE	Output write enable signal	Alternate function mode

Table 12-114 LCD

LCD Pin	Configuration	GPIO Configuration
LCD_B[7:0]	Blue output signal	Alternate function mode
LCD_G[7:0]	Green output signal	Alternate function mode
LCD_R[7:0]	Red output signal	Alternate function mode
LCD_CLK	Clock output signal	Alternate function mode
LCD_DE	Data Enable output signal	Alternate function mode
LCD_HSYNC	Horizontal Synchronization output signal	Alternate function mode
LCD_VSYNC	Vertical Synchronization output signal	Alternate function mode

Table 12-115 SDMMC1/2

SDMMC Pin	Configuration	GPIO Configuration
SDMMC_D[7:0]	Bidirectional Data Lines	Push-pull alternate function mode
SDMMC_WP	Write Protection Input	Alternate function mode
SDMMC_CD	Card Detection Input	Alternate function mode
SDMMC_CMD	Bidirectional Command Line	Push-pull alternate function mode
SDMMC_CK	Clock Output to Card	Push-pull alternalte function mode
SDMMC_CKIN	Feedback Clock Input From Card	Alternate function mode
SDMMC_RST	EMMC Hardware Reset Output	Push-pull alternate function mode
SDMMC_CDIR	Command Direction Output	Push-pull alternate function mode
SDMMC_D0DIR	Data0 Direction Output	Push-pull alternate function mode
SDMMC_D123DIR	Data1/2/3 Direction Output	Push-pull alternate function mode
SDMMC_LEDCTRL	LED CTRL Output	Push-pull alternate function mode
SDMMC_SEL	1.8V Switching Enable Output	Push-pull alternate function mode

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Table 12-116 Other

Pin	Alternate function	GPIO configuration
RTC_REFIN	RTC reference clock input	Alternate input mode
RTC_OUT2	RTC out2 pin	Push-pull alternate output
Timestamp	Timestamp trigger input	Alternate input mode
MCO1/2	Clock output	Push-pull alternate output
EXTI Input Line	External interrupt input	Input mode
COMPx_OUT	COMP output	Push-pull alternate output
EVENT_OUT	Event output	Push-pull alternate output

12.3.7 GPIO locking mechanism

The locking mechanism is used to freeze the IO configuration to prevent accidental changes. When a lock (LOCK) procedure is performed on a port bit, the configuration of the port cannot be changed until the next reset, refer to the port configuration lock register GPIOx_PLOCK.

- PLOCKK, that is, GPIOx_PLOCK [16], becomes 1 only after the correct sequence w1-> w0-> w1-> r0 (r0 here is also a must). After that, it becomes 0 only if the system reset is performed.
- PLOCKy can only be modified at PLOCKK=0.
- The lock sequence to set PLOCKK bit, w1-> w0-> w1-> r0 will be valid only if the value (1 or 0) in GPIOx_PLOCK.PLOCK[15:0] does not change during this sequence. The GPIOx_PLOCK.PLOCKK bit will not be set if the value in GPIOx_PLOCK.PLOCK[15:0] changes during this sequence.
- As long as GPIOx_PLOCK.PLOCKK=0 and GPIOx_PLOCK.PLOCKy=0 or 1, all configuration and alternate function bits can be modified. When GPIOx_PLOCK.PLOCKK=1 but GPIOx_LOCK.PLOCK[x] = 0, the corresponding configuration and alternate function bits corresponding to GPIOx_PLOCK.PLOCK[x] = 0 can be modified.
- Only when GPIOx_PLOCK.PLOCKK=1 and GPIOx_PLOCK.PLOCK[x] = 1, the configurations corresponding to GPIOx_PLOCK.PLOCK[x] = 1 are locked and cannot be modified.

If the lock sequence operation is wrong, then it must be redone (w1-> w0-> w1-> r0) to initiate the lock operation again.

12.3.8 GPIO PAD Types

There are 3 types of GPIO in the chip; 5V Tolerant, 3.3 V Tolerant and 3.3V Tolerant (SDRAM). Each type of pads will have different drive strength capabilities. See 12.4.13 for more details.

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Table 12-117 GPIO PAD Types

5V Tolerant	BOOT0, PA8, PA10, PA11, PA12, PA13, PA14, PA15 PB3, PB4, PB9 PC6, PC7, PC8, PC13, PC14, PC15 PD3 PE4, PE6 PG3 PH0, PH1, PH4 PI8, PI15 PJ0, PJ3, PJJ4, PJ5, PJ6, PJ7, PJ8, PJ9, PJ10, PJ11, PJ12, PJ13, PJ14,PJ15 PK0, PK1, PK2
3.3V Tolerant	PA0, PA1, PA2, PA3, PA6, PA9 PB0, PB1, PB2, PB7, PB8, PB10, PB11, PB12, PB13 PC1, PC9, PC10, PC11 PD4, PD5, PD6, PD7, PD11, PD12, PD13 PE2,PE3, PE5 PF6, PF7, PF8, PF9, PF10 PG6, PG7, PG9, PG10, PG11, PG12, PG13, PG14 PI11, PI12, PI13, PI14 PJ1, PJ2, PK3, PK4, PK5, PK6, PK7
3.3V Tolerant (SDRAM)	PI10,PI9,PI7,PI6,PI5,PI4,PI3,PI2,PI1,PI0 PH15,PH14,PH13,PH12,PH11,PH10,PH9,PH8,PH7,PH6,PH5,PH3,PH2 PG15,PG8,PG5,PG4,PG2,PG1,PG0 PF15,PF14,PF13,PF12,PF11,PF5,PF4,PF3,PF2,PF1,PF0 PE15,PE14,PE13,PE12,PE11,PE10,PE9,PE8,PE7,PE1,PE0 PD15,PD14,PD10,PD9,PD8,PD2,PD1,PD0 PC12,PC5,PC4,PC3,PC2,PC0 PB15,PB14,PB6,PB5,PA7,PA5,PA4

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12.4 GPIO Registers

These peripheral registers are 32-bit words.

12.4.1 GPIO Registers Overview

GPIOA base address：0x58032800

GPIOB base address：0x58032C00

GPIOC base address：0x58033000

GPIOD base address：0x58033400

GPIOE base address：0x58033800

GPIOF base address：0x58033C00

GPIOG base address：0x58034000

GPIOH base address：0x58034400

GPIOI base address：0x58034800

GPIOJ base address：0x58034C00

GPIOK base address：0x58035000

12.4.2 GPIO Mode Description Register (GPIOx_PMODE)

Address offset: 0x00

Reset value: 0xABFF FFFF（x=A）；0xFFFF FEBF（x=B）；0xFFFFFFFF（x=C,D,E,F,G,H,I,J），0x0000 FFFF（x=K）

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
PMODE15	PMODE14 [1:0]	PMODE13 [1:0]	PMODE12 [1:0]	PMODE11 [1:0]	PMODE10 [1:0]	PMODE9 [1:0]	PMODE8 [1:0]
rw	rw	rw	rw	rw	rw	rw	rw
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PMODE7[1:0]	PMODE6 [1:0]	PMODE5 [1:0]	PMODE4[1:0]	PMODE3 [1:0]	PMODE2 [1:0]	PMODE1 [1:0]	PMODE0 [1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18	PMODEy[1:0]	Mode bits for port y (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) 00: Input mode 01: General output mode 10: Alternate function mode 11: Analog function mode (state after reset)

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Bit Field	Name	Description
17:16		
15:14		
13:12		
11:10		
9:8		
7:6		
5:4		
3:2		
1:0		

12.4.3 GPIO Output Type Definition(GPIOx_POTYPE)

Address offset: 0x04

Reset value: 0x0000 0000(x = A,B,C,D,E,F,G,H,I,J)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	POTy[15:0]	Output mode bits for port y (y = 0…15 for and y = 0….7 for x=K) 0: Output push-pull mode (state after reset) 1: Output open-drain mode

12.4.4 GPIO Port Slew Rate Configuration Register(GPIOx_SR)

Address offset: 0x08

Reset value: 0x0000 FFFF（x= A,B,C,D,E,F,G,H,I,J）；0x0000 00FF（x=K）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	SRy[15:0]	Toggle rate configuration for port y (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) These bits can only be read or written as 16-bit words. 0：Fast slew rate 1：Slow slew rate

12.4.5 GPIO Pull-Up/Pull-Down Description Register(GPIOx_PUPD)

Address offset: 0x0C

Reset value: 0x6400 0000（x=A）；0x0000 0100（x=B）；0x0000 0000（x=C,D,E,F,G,H,I,J,K）

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
PUPD15[1:0]	PUPD14[1:0]	PUPD13[1:0]	PUPD12[1:0]	PUPD11[1:0]	PUPD10[1:0]	PUPD9[1:0]	PUPD8[1:0]
rw rw	rw rw	rw rw	rw rw	rw rw	rw rw	rw rw	rw rw
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PUPD7[1:0]	PUPD6[1:0]	PUPD5[1:0]	PUPD4[1:0]	PUPD3[1:0]	PUPD2[1:0]	PUPD1[1:0]	PUPD0[1:0]
rw rw	rw rw	rw rw	rw rw	rw rw	rw rw	rw rw	rw rw

Bit Field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	PUPDy[1:0]	Mode bits for port y (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) 00: No pull-up, pull-down 01: Pull-up 10: Pull-down 11: Reserved

12.4.6 GPIO Input Data Register(GPIOx_PID)

Address offset: 0x10

Reset value: 0x0000 0000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
Reserved

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PIDy[15:0]	Port output data (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) These bits are read-only and can only be read in the form of 16-bit words, and the read value is the state of the corresponding I/O port.

12.4.7 GPIO Output Data Register(GPIOx_POD)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PODy[15:0]	Port output data (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) These bits can only be read or written as 16-bit words. For GPIOx_PBSC (x = A…D), the corresponding POD bits can be independently set/cleared.

12.4.8 GPIO Bit Set/Clear Register (GPIOx_PBSC)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	PBCy	Clear bit y of port GPIOx (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K)

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Bit Field	Name	Description
		These bits can only be written and operated as words (16 bits). 0: Does not affect the corresponding ODRy bit 1: Clear the corresponding ODRy bit to 0 *Note: if the corresponding bits of BSy and BRy are set at the same time, the BSy bit works.*
15:0	PBSy	Set bit y of port GPIOx (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) These bits can only be written and operated as words (16 bits). 0: Does not affect the corresponding ODRy bit 1: Set the corresponding ODRy bit to 1

12.4.9 GPIO Configuration Lock Register(GPIOx_PLOCK)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															PLOCKK
															rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	PLOCKK	Lock key. This bit can be read at any time, and it can only be modified by the key lock write sequence. 0: Port configuration lock key is activated 1: The port configuration lock key is activated, and the GPIOx_LCKR register is locked before the next system reset. The write sequence of the lock key: Write 1 -> write 0 -> write 1 -> read 0 -> read 1 The last reading can be omitted, but it can be used to confirm that the lock key has been activated. *Note: the value of Lck [15:0] cannot be changed when the writing sequence of lock key is operated. Any error in the operation key writing sequence will not activate the key.* *For x= K, LCKK is GPIOK_LCKR[8]*
15:0	PLOCKy	Configuration lock bit y of port GPIOx (y = 0…15 for x = A,B,C,D,E,F,G,H,I,J and y = 0….7 for x=K) These bits are readable and writable but can only be written when the LCKK bit is 0. 0: Do not lock the configuration of the port 1: Lock the configuration of the port

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12.4.10 GPIO Alternate Function Low Register(GPIOx_AFL)

Address offset: 0x20

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL7[3:0]				AFSEL6[3:0]				AFSEL5[3:0]				AFSEL4[3:0]			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL3[3:0]				AFSEL2[3:0]				AFSEL1[3:0]				AFSEL0[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:0	AFSELy[3:0]	Alternate function configuration for port y (y = 0…7) 0000：AF0 0001：AF1 0010：AF2 0011：AF3 0100：AF4 0101：AF5 0110：AF6 0111：AF7 1000：AF8 1001：AF9 1010：AF10 1011：AF11 1100：AF12 1101：AF13 1110：AF14 1111：AF15

12.4.11 GPIO Alternate Function High Register(GPIOx_AFH)

Address offset: 0x24

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
rw				rw				rw				rw			

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Bit Field	Name	Description
31:0	AFSELy[3:0]	Alternate function configuration for port y (y = 8….15) 0000：AF0 0001：AF1 0010：AF2 0011：AF3 0100：AF4 0101：AF5 0110：AF6 0111：AF7 1000：AF8 1001：AF9 1010：AF10 1011：AF11 1100：AF12 1101：AF13 1110：AF14 1111：AF15

12.4.12 GPIO Bit Clear Register(GPIOx_PBC)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PBCy[15:0]	Clear bit y of port GPIOx (y = 0...15) These bits can only be written and operated as words (16 bits). 0: Does not affect the corresponding PODy bit 1: Clear the corresponding PODy bit to 0

12.4.13 GPIO Driver Strength Configuration Register(GPIOx_DS)

Address offset: 0x1C

Reset value: 0xAAAA AAAA（x = A,B,C,D,E,F,G,H,I,J）；0x0000 AAAA（x=K）

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31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
DS15[1:0]	DS14[1:0]	DS13[1:0]	DS12[1:0]	DS11[1:0]	DS10[1:0]	DS9[1:0]	DS8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
DS7[1:0]	DS6[1:0]	DS5[1:0]	DS4[1:0]	DS3[1:0]	DS2[1:0]	DS1[1:0]	DS0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	DSy[1:0]	Port y drive capability configuration (y = 0…15) 3.3V Tolerant PADs DSy[1] / DSy[0] / Drive Strength 0 / 0 / 2mA 0 / 1 / 8mA 1 / 0 / 4mA 1 / 1 / 12mA 5V Tolerant PADs DSy[1] / DSy[0] / Drive Strength 0 / 0 / 1mA 0 / 1 / 4mA 1 / 0 / 2mA 1 / 1 / 6mA DSNz, DSPz (z=0..2). See AFIO_SDRAMDSN_CFGx and AFIO_SDRAMDSP_CFGx 3.3V Tolerant PADs (SDRAM) DSy[1] / DSy[0] / DSNz / DSPz / Drive Strength 0 / 0 / 0 / 0 / 1mA 0 / 0 / 1 / 1 / 2mA 0 / 1 / 0 / 0 / 8mA 1 / 0 / 0 / 0 / 4mA 1 / 0 / 1 / 1 / 5mA 1 / 1 / 0 / 0 / 12mA

12.5 AFIO Registers

12.5.1 AFIO Register Overview

AFIO base address: 0x58032400

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12.5.2 AFIO Mapping Configuration Register(AFIO_RMP_CFG)

Address offset: 0x00

Reset value: 0x0000 0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	EXTI_AFLTBYPS	SIP_SDRAM_SEL	SPI4_SEL	SPI3_SEL	SPI2_SEL	SPI1_SEL	SDMMC1_CLKFB	SDMMC2_CLKFB	I2S_FULL_DUPLEX		Reserved	XSPI2_EDN	XSPI1_EDN	FEMC_SEL	FEMC_NOBYTE
	rw	rw	rw	rw	rw	rw	rw	rw	rw			rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETH2_PHY	ETH1_PHY[1:0]		SPI7_NSS	SPI6_NSS	SPI5_NSS	SPI4_NSS	SPI3_NSS	SPI2_NSS	SPI1_NSS	Reserved			SIP_FLASH SEL[2:0]		
rw	rw		rw	rw	rw	rw	rw	rw	rw	rw			rw		

Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	EXTI_AFLTBYPS	Bypass analog filter for EXTI 0: Filtered 1: Unfiltered
29	SIP_SDRAM_SEL	Set SIP SDRAM PAD priority. 0: No set priority. 1: Prioritise the AFSEL of the PAD to SIP SDRAM over than the other module's AF selection.
28	SPI4SEL	Select SPI4 or I2S4 function. 0: I2S4 ENABLE (only for IOs sharing SPI/I2S) 1: SPI4 ENABLE
27	SPI3SEL	Select SPI3 or I2S3 function. 0: I2S3 ENABLE (only for IOs sharing SPI/I2S) 1: SPI3 ENABLE
26	SPI2SEL	Select SPI2 or I2S2 function. 0: I2S2 ENABLE (only for IOs sharing SPI/I2S) 1: SPI2 ENABLE
25	SPI1SEL	Select SPI1 or I2S1 function. 0: I2S1 ENABLE (only for IOs sharing SPI/I2S) 1: SPI1 ENABLE
24	SDMMC1_CLKFB	To select between external or feedback clock input 0: External clock input 1: Feedback clock input
23	SDMMC2_CLKFB	To select between external or feedback clock input 0: External clock input

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Bit Field	Name	Description
		1: Feedback clock input
22:21	I2S_FDUP[1:0]	To enable I2S full duplex mode 00: I2S1 full duplex mode enable 01: I2S2 full duplex mode enable 10: I2S3 full duplex mode enable 11: I2S4 full duplex mode enable
20	Reserved	Reserved, the reset value must be maintained.
19	XSPI2_EDN	XSPI2 endian selection 0: Little endian 1: Big endian
18	XSPI1_EDN	XSPI1 endian selection 0: Little endian 1: Big endian
17	FEMCSEL	Select FEMC work mode 0: SRAM/PSRAM/NOR device 1: NAND device
16	FEMC_NOBYTE	Enable WE_N = ANDed of NBLs for Flashes do not support byte strobes 0: Support byte strobes 1: Not support byte strobes
15	ETH2_PHY	For the ETH2 PHY selection 0: MII 1: RMII
14:13	ETH1_PHY[1:0]	For the ETH1 PHY selection 00: GMII 01: RGMII 10: RMII 11: MII
12	SPI7_NSS	NSS mode of SPI7(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle
11	SPI6_NSS	NSS mode of SPI6(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle
10	SPI5_NSS	NSS mode of SPI5(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle
9	SPI4_NSS	NSS mode of SPI4(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle

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Bit Field	Name	Description
8	SPI3_NSS	NSS mode of SPI3(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle
7	SPI2_NSS	NSS mode of SPI2(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle
6	SPI1_NSS	NSS mode of SPI1(when NSS is configured as AFIO push-pull): 0: NSS will be high-z when idle 1: NSS will be 1 when idle
5:3	Reserved	Reserved, the reset value must be maintained.
2:0	SIP_FLASHSEL [2:0]	000: IS25WJ032F 001: IS25LP016D/IS25WP016D 010: XM25LU32CK 011: GT25Q16A 100: GT25Q32A 111: Disable SIP segment (switch to Main IOM) –Default

12.5.3 AFIO IOM Filter Control Register (AFIO_FILTER_CFG)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									IOFLITCFG [6:0]						
									rw						

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6:0	IOFLITCFG[6:0]	Glitch Filter stage control 0000000: Filter bypass others : counter value indicating minimum pulse width in terms of hclk cycles

12.5.4 AFIO XSPI1 Nonce Register0(AFIO_XSPI1_NON0)

Address offset: 0x08

Reset value: 0xA54B 885C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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XSPI1_DEC_NONCE0[31:16]

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XSPI1_DEC_NONCE0[15:0]															

rw

Bit Field	Name	Description
31:0	XSPI1_DEC_NONCE[31:0]	XSPI decryption Nonce[31:0] [96 bit in total] The RTAD uses AES128-CTR to run decryption base on the give key, nonce value and read address bit, and get DataFilter result

12.5.5 AFIO XSPI1 Nonce Register1(AFIO_XSPI1_ NON1)

Address offset: 0x0C

Reset value: 0x0000 0DC0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
XSPI1_DEC_NONCE1[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XSPI1_DEC_NONCE1[15:0]															

rw

Bit Field	Name	Description
31:0	XSPI1_DEC_NONCE[31:0]	XSPI decryption Nonce [63:32] [96 bit in total] The RTAD uses AES128-CTR to run decryption base on the give key, nonce value and read address bit, and get DataFilter result

12.5.6 AFIO XSPI1 Nonce Register2(AFIO_XSPI1_ NON2)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
XSPI1_DEC_NONCE2[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XSPI1_DEC_NONCE2[15:0]															

rw

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Bit Field	Name	Description
31:0	XSPI1_DEC_NONCE[31:0]	XSPI decryption Nonce [95:64] [96 bit in total] The RTAD uses AES128-CTR to run decryption base on the give key, nonce value and read address bit, and get DataFilter result

12.5.7 AFIO ADC Remap Configure Register(AFIO_ADCRMP_CFG)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								ADC1_EXTIRISEL[3:0]				ADC1_EXTIRRSEL[3:0]			
								rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC2_EXTIRISEL[3:0]				ADC2_EXTIRRSEL[3:0]				ADC3_EXTIRISEL[3:0]				ADC3_EXTIRRSEL[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:20	ADC1_EXTIETRI[3:0]	Select the interrupt line as the external trigger signal source for ADC1 injection channel 0000: EXTI Line0 0001: EXTI Line1 0010: EXTI Line2 0011: EXTI Line3 0100: EXTI Line4 0101: EXTI Line5 0110: EXTI Line6 0111: EXTI Line7 1000: EXTI Line8 1001: EXTI Line9 1010: EXTI Line10 1011: EXTI Line11 1100: EXTI Line12 1101: EXTI Line13 1110: EXTI Line14 1111: EXTI Line 15
19:16	ADC1_EXTIETRR[3:0]	Select the interrupt line as the external trigger signal source of ADC1regular channel

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		0000: EXTI Line0 0001: EXTI Line1 0010: EXTI Line2 0011: EXTI Line3 0100: EXTI Line4 0101: EXTI Line5 0110: EXTI Line6 0111: EXTI Line7 1000: EXTI Line8 1001: EXTI Line9 1010: EXTI Line10 1011: EXTI Line11 1100: EXTI Line12 1101: EXTI Line13 1110: EXTI Line14 1111: EXTI Line 15
15:12	ADC2_EXTIETRI[3:0]	Select the interrupt line as the external trigger signal source for ADC2 injection channel 0000: EXTI Line0 0001: EXTI Line1 0010: EXTI Line2 0011: EXTI Line3 0100: EXTI Line4 0101: EXTI Line5 0110: EXTI Line6 0111: EXTI Line7 1000: EXTI Line8 1001: EXTI Line9 1010: EXTI Line10 1011: EXTI Line11 1100: EXTI Line12 1101: EXTI Line13 1110: EXTI Line14 1111: EXTI Line 15
11:8	ADC2_EXTIETRR[3:0]	Select the interrupt line as the external trigger signal source of ADC2 regular channel 0000: EXTI Line0 0001: EXTI Line1 0010: EXTI Line2 0011: EXTI Line3 0100: EXTI Line4 0101: EXTI Line5 0110: EXTI Line6

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		0111: EXTI Line7 1000: EXTI Line8 1001: EXTI Line9 1010: EXTI Line10 1011: EXTI Line11 1100: EXTI Line12 1101: EXTI Line13 1110: EXTI Line14 1111: EXTI Line 15
7:4	ADC3_ EXTIETRI[3:0]	Select the interrupt line as the external trigger signal source for ADC3 injection channel 0000: EXTI Line0 0001: EXTI Line1 0010: EXTI Line2 0011: EXTI Line3 0100: EXTI Line4 0101: EXTI Line5 0110: EXTI Line6 0111: EXTI Line7 1000: EXTI Line8 1001: EXTI Line9 1010: EXTI Line10 1011: EXTI Line11 1100: EXTI Line12 1101: EXTI Line13 1110: EXTI Line14 1111: EXTI Line 15
3:0	ADC3_EXTIETRR[3:0]	Select the interrupt line as the external trigger signal source of ADC3 regular channel 0000: EXTI Line0 0001: EXTI Line1 0010: EXTI Line2 0011: EXTI Line3 0100: EXTI Line4 0101: EXTI Line5 0110: EXTI Line6 0111: EXTI Line7 1000: EXTI Line8 1001: EXTI Line9 1010: EXTI Line10 1011: EXTI Line11 1100: EXTI Line12 1101: EXTI Line13

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		1110: EXTI Line14 1111: EXTI Line 15

12.5.8 AFIO External Interrupt Configuration Register 0 (AFIO_EXTI_CFG0)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXTI3[7:0]								EXTI2[7:0]							
rw								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI1[7:0]								EXTI0[7:0]							
rw								rw							

Bit Field	Name	Description
31:24 23:16 15:8 7:0	EXTIx[7:0]	EXTIx configuration（x = 0 … 3） These bits can be read and written by software to select the input source for the EXTIx external interrupt. 8'h0 : PA[0] pin 8'h1 : PB[0] pin 8'h2 : PC[0] pin 8'h3 : PD[0] pin 8'h4 : PE[0] pin 8'h5 : PF[0] pin 8'h6 : PG[0] pin 8'h7 : PH[0] pin 8'h8 : PI[0] pin 8'h9 : PJ[0] pin 8'hA : PK[0]pin 8'hB : PA[1] pin 8'hC : PB[1] pin 8'hD : PC[1] pin 8'hE : PD[1] pin 8'hF : PE[1] pin 8'h10 : PF[1 pin 8'h11 : PG[1] pin 8'h12 : PH[1] pin 8'h13 : PI[1] pin 8'h14 : PJ[1] pin 8'h15 : PK[1] pin

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Bit Field	Name	Description
		8'h16 : PA[2] pin 8'h17 : PB[2] pin 8'h18 : PC[2] pin 8'h19 : PD[2] pin 8'h1A : PE[2] pin 8'h1B : PF[2] pin 8'h1C : PG[2] pin 8'h1D : PH[2] pin 8'h1E : PI[2] pin 8'h1F : PJ[2] pin 8'h20 : PK[2] pin 8'h21 : PA[3] pin 8'h22 : PB[3] pin 8'h23 : PC[3] pin 8'h24 : PD[3] pin 8'h25 : PE[3] pin 8'h26 : PF[3] pin 8'h27 : PG[3] pin 8'h28 : PH[3] pin 8'h29 : PI[3] pin 8'h2A : PJ[3] pin 8'h2B : PK[3] pin 8'h2C : PA[4] pin 8'h2D : PB[4] pin 8'h2E : PC[4] pin 8'h2F : PD[4] pin 8'h30 : PE[4] pin 8'h31 : PF[4] pin 8'h32 : PG[4] pin 8'h33 : PH[4] pin 8'h34 : PI[4] pin 8'h35 : PJ[4] pin 8'h36 : PK[4] pin 8'h37 : PA[5] pin 8'h38 : PB[5] pin 8'h39 : PC[5] pin 8'h3A : PD[5] pin 8'h3B : PE[5] pin

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Bit Field	Name	Description
		8'h3C : PF[5] pin 8'h3D : PG[5] pin 8'h3E : PH[5] pin 8'h3F : PI[5] pin 8'h40 : PJ[5] pin 8'h41 : PK[5] pin 8'h42 : PA[6] pin 8'h43 : PB[6] pin 8'h44 : PC[6] pin 8'h45 : PD[6] pin 8'h46 : PE[6] pin 8'h47 : PF[6] pin 8'h48 : PG[6] pin 8'h49 : PH[6] pin 8'h4A: PI[6] pin 8'h4B: PJ[6] pin 8'h4C: PK[6] pin 8'h4D : PA[7] pin 8'h4E : PB[7] pin 8'h4F : PC[7] pin 8'h50 : PD[7] pin 8'h51 : PE[7] pin 8'h52 : PF[7] pin 8'h53 : PG[7] pin 8'h54 : PH[7] pin 8'h55 : PI[7] pin 8'h56 : PJ[7] pin 8'h57 : PK[7] pin 8'h58 : PA[8] pin 8'h59 : PB[8] pin 8'h5A : PC[8] pin 8'h5B : PD[8] pin 8'h5C : PE[8] pin 8'h5D : PF[8] pin 8'h5E : PG[8] pin 8'h5F : PH[8] pin 8'h60 : PI[8] pin 8'h61 : PJ[8] pin 8'h62 : 0

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Bit Field	Name	Description
		8'h63 : PA[9] pin 8'h64 : PB[9] pin 8'h65 : PC[9] pin 8'h66 : PD[9] pin 8'h67 : PE[9] pin 8'h68: PF[9] pin 8'h69 : PG[9] pin 8'h6A : PH[9] pin 8'h6B : PI[9] pin 8'h6C : PJ[9] pin 8'h6D : 0 8'h6E : PA[10] pin 8'h6F : PB[10] pin 8'h70 : PC[10] pin 8'h71 : PD[10] pin 8'h72 : PE[10] pin 8'h73 : PF[10] pin 8'h74 : PG[10] pin 8'h75 : PH[10] pin 8'h76 : PI[10] pin 8'h77 : PJ[10] pin 8'h78 : 0 8'h79 : PA[11] pin 8'h7A : PB[11] pin 8'h7B : PC[11] pin 8'h7C : PD[11] pin 8'h7D : PE[11] pin 8'h7E : PF[11] pin 8'h7F: PG[11] pin 8'h80 : PH[11] pin 8'h81 : PI[11] pin 8'h82 : PJ[11] pin 8'h83 : 0 8'h84 : PA[12] pin 8'h85 : PB[12] pin 8'h86 : PC[12] pin 8'h87 : PD[12] pin 8'h88 : PE[12] pin

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Bit Field	Name	Description
		8'h89 : PF[12] pin 8'h8A : PG[12] pin 8'h8B : PH[12] pin 8'h8C : PI[12] pin 8'h8D : PJ[12] pin 8'h8E : 0 8'h8F : PA[13] pin 8'h90 : PB[13] pin 8'h91 : PC[13] pin 8'h92 : PD[13] pin 8'h93 : PE[13] pin 8'h94 : PF[13] pin 8'h95 : PG[13] pin 8'h96 : PH[13] pin 8'h97 : PI[13] pin 8'h98 : PJ[13] pin 8'h99 : 0 8'h9A : PA[14] pin 8'h9B : PB[14] pin 8'h9C: PC[14] pin 8'h9D : PD[14] pin 8'h9E : PE[14] pin 8'h9F : PF[14] pin 8'hA0 : PG[14] pin 8'hA1 : PH[14] pin 8'hA2 : PI[14] pin 8'hA3 : PJ[14] pin 8'hA4 : 0 8'hA5 : PA[15] pin 8'hA6 : PB[15] pin 8'hA7 : PC[15] pin 8'hA8 : PD[15] pin 8'hA9 : PE[15] pin 8'hAA : PF[15] pin 8'hAB : PG[15] pin 8'hAC : PH[15] pin 8'hAD : PI[15] pin 8'hAE : PJ[15] pin 8'hAF : 0

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Bit Field	Name	Description
		Others: reserved

12.5.9 AFIO External Interrupt Configuration Register 1 (AFIO_EXTI_CFG1)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXTI7[7:0]								EXTI6[7:0]							
rw								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI5[7:0]								EXTI4[7:0]							
rw								rw							

Bit Field	Name	Description
31:24 23:16 15:8 7:0	EXTIx[7:0]	EXTIx configuration（x = 4 … 7） These bits can be read and written by software to select the input source for the EXTIx external interrupt. 8'h0 : PA[0] pin 8'h1 : PB[0] pin 8'h2 : PC[0] pin 8'h3 : PD[0] pin 8'h4 : PE[0] pin 8'h5 : PF[0] pin 8'h6 : PG[0] pin 8'h7 : PH[0] pin 8'h8 : PI[0] pin 8'h9 : PJ[0] pin 8'hA : PK[0]pin 8'hB : PA[1] pin 8'hC : PB[1] pin 8'hD : PC[1] pin 8'hE : PD[1] pin 8'hF : PE[1] pin 8'h10 : PF[1 pin 8'h11 : PG[1] pin 8'h12 : PH[1] pin 8'h13 : PI[1] pin 8'h14 : PJ[1] pin 8'h15 : PK[1] pin

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		8'h16 : PA[2] pin 8'h17 : PB[2] pin 8'h18 : PC[2] pin 8'h19 : PD[2] pin 8'h1A : PE[2] pin 8'h1B : PF[2] pin 8'h1C : PG[2] pin 8'h1D : PH[2] pin 8'h1E : PI[2] pin 8'h1F : PJ[2] pin 8'h20 : PK[2] pin 8'h21 : PA[3] pin 8'h22 : PB[3] pin 8'h23 : PC[3] pin 8'h24 : PD[3] pin 8'h25 : PE[3] pin 8'h26 : PF[3] pin 8'h27 : PG[3] pin 8'h28 : PH[3] pin 8'h29 : PI[3] pin 8'h2A : PJ[3] pin 8'h2B : PK[3] pin 8'h2C : PA[4] pin 8'h2D : PB[4] pin 8'h2E : PC[4] pin 8'h2F : PD[4] pin 8'h30 : PE[4] pin 8'h31 : PF[4] pin 8'h32 : PG[4] pin 8'h33 : PH[4] pin 8'h34 : PI[4] pin 8'h35 : PJ[4] pin 8'h36 : PK[4] pin 8'h37 : PA[5] pin 8'h38 : PB[5] pin 8'h39 : PC[5] pin 8'h3A : PD[5] pin 8'h3B : PE[5] pin 8'h3C : PF[5] pin 8'h3D : PG[5] pin

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		8'h3E : PH[5] pin 8'h3F : PI[5] pin 8'h40 : PJ[5] pin 8'h41 : PK[5] pin 8'h42 : PA[6] pin 8'h43 : PB[6] pin 8'h44 : PC[6] pin 8'h45 : PD[6] pin 8'h46 : PE[6] pin 8'h47 : PF[6] pin 8'h48 : PG[6] pin 8'h49 : PH[6] pin 8'h4A: PI[6] pin 8'h4B: PJ[6] pin 8'h4C: PK[6] pin 8'h4D : PA[7] pin 8'h4E : PB[7] pin 8'h4F : PC[7] pin 8'h50 : PD[7] pin 8'h51 : PE[7] pin 8'h52 : PF[7] pin 8'h53 : PG[7] pin 8'h54 : PH[7] pin 8'h55 : PI[7] pin 8'h56 : PJ[7] pin 8'h57 : PK[7] pin 8'h58 : PA[8] pin 8'h59 : PB[8] pin 8'h5A : PC[8] pin 8'h5B : PD[8] pin 8'h5C : PE[8] pin 8'h5D : PF[8] pin 8'h5E : PG[8] pin 8'h5F : PH[8] pin 8'h60 : PI[8] pin 8'h61 : PJ[8] pin 8'h62 : 0 8'h63 : PA[9] pin 8'h64 : PB[9] pin

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		8'h65 : PC[9] pin 8'h66 : PD[9] pin 8'h67 : PE[9] pin 8'h68: PF[9] pin 8'h69 : PG[9] pin 8'h6A : PH[9] pin 8'h6B : PI[9] pin 8'h6C : PJ[9] pin 8'h6D : 0 8'h6E : PA[10] pin 8'h6F : PB[10] pin 8'h70 : PC[10] pin 8'h71 : PD[10] pin 8'h72 : PE[10] pin 8'h73 : PF[10] pin 8'h74 : PG[10] pin 8'h75 : PH[10] pin 8'h76 : PI[10] pin 8'h77 : PJ[10] pin 8'h78 : 0 8'h79 : PA[11] pin 8'h7A : PB[11] pin 8'h7B : PC[11] pin 8'h7C : PD[11] pin 8'h7D : PE[11] pin 8'h7E : PF[11] pin 8'h7F: PG[11] pin 8'h80 : PH[11] pin 8'h81 : PI[11] pin 8'h82 : PJ[11] pin 8'h83 : 0 8'h84 : PA[12] pin 8'h85 : PB[12] pin 8'h86 : PC[12] pin 8'h87 : PD[12] pin 8'h88 : PE[12] pin 8'h89 : PF[12] pin 8'h8A : PG[12] pin 8'h8B : PH[12] pin 8'h8C : PI[12] pin

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		8'h8D : PJ[12] pin 8'h8E : 0 8'h8F : PA[13] pin 8'h90 : PB[13] pin 8'h91 : PC[13] pin 8'h92 : PD[13] pin 8'h93 : PE[13] pin 8'h94 : PF[13] pin 8'h95 : PG[13] pin 8'h96 : PH[13] pin 8'h97 : PI[13] pin 8'h98 : PJ[13] pin 8'h99 : 0 8'h9A : PA[14] pin 8'h9B : PB[14] pin 8'h9C: PC[14] pin 8'h9D : PD[14] pin 8'h9E : PE[14] pin 8'h9F : PF[14] pin 8'hA0 : PG[14] pin 8'hA1 : PH[14] pin 8'hA2 : PI[14] pin 8'hA3 : PJ[14] pin 8'hA4 : 0 8'hA5 : PA[15] pin 8'hA6 : PB[15] pin 8'hA7 : PC[15] pin 8'hA8 : PD[15] pin 8'hA9 : PE[15] pin 8'hAA : PF[15] pin 8'hAB : PG[15] pin 8'hAC : PH[15] pin 8'hAD : PI[15] pin 8'hAE : PJ[15] pin 8'hAF : 0 Others: reserved

12.5.10 AFIO External Interrupt Configuration Register 2 (AFIO_EXTI_CFG2)

Address offset: 0x20

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXTI11[7:0]								EXTI10[7:0]							
rw								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI9[7:0]								EXTI8[7:0]							
rw								rw							

Bit Field	Name	Description
31:24 23:16 15:8 7:0	EXTIx[7:0]	EXTIx configuration（x = 8 … 11） These bits can be read and written by software to select the input source for the EXTIx external interrupt. 8'h0 : PA[0] pin 8'h1 : PB[0] pin 8'h2 : PC[0] pin 8'h3 : PD[0] pin 8'h4 : PE[0] pin 8'h5 : PF[0] pin 8'h6 : PG[0] pin 8'h7 : PH[0] pin 8'h8 : PI[0] pin 8'h9 : PJ[0] pin 8'hA : PK[0]pin 8'hB : PA[1] pin 8'hC : PB[1] pin 8'hD : PC[1] pin 8'hE : PD[1] pin 8'hF : PE[1] pin 8'h10 : PF[1 pin 8'h11 : PG[1] pin 8'h12 : PH[1] pin 8'h13 : PI[1] pin 8'h14 : PJ[1] pin 8'h15 : PK[1] pin 8'h16 : PA[2] pin 8'h17 : PB[2] pin 8'h18 : PC[2] pin 8'h19 : PD[2] pin 8'h1A : PE[2] pin 8'h1B : PF[2] pin

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		8'h1C : PG[2] pin 8'h1D : PH[2] pin 8'h1E : PI[2] pin 8'h1F : PJ[2] pin 8'h20 : PK[2] pin 8'h21 : PA[3] pin 8'h22 : PB[3] pin 8'h23 : PC[3] pin 8'h24 : PD[3] pin 8'h25 : PE[3] pin 8'h26 : PF[3] pin 8'h27 : PG[3] pin 8'h28 : PH[3] pin 8'h29 : PI[3] pin 8'h2A : PJ[3] pin 8'h2B : PK[3] pin 8'h2C : PA[4] pin 8'h2D : PB[4] pin 8'h2E : PC[4] pin 8'h2F : PD[4] pin 8'h30 : PE[4] pin 8'h31 : PF[4] pin 8'h32 : PG[4] pin 8'h33 : PH[4] pin 8'h34 : PI[4] pin 8'h35 : PJ[4] pin 8'h36 : PK[4] pin 8'h37 : PA[5] pin 8'h38 : PB[5] pin 8'h39 : PC[5] pin 8'h3A : PD[5] pin 8'h3B : PE[5] pin 8'h3C : PF[5] pin 8'h3D : PG[5] pin 8'h3E : PH[5] pin 8'h3F : PI[5] pin 8'h40 : PJ[5] pin 8'h41 : PK[5] pin 8'h42 : PA[6] pin

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		8'h43 : PB[6] pin 8'h44 : PC[6] pin 8'h45 : PD[6] pin 8'h46 : PE[6] pin 8'h47 : PF[6] pin 8'h48 : PG[6] pin 8'h49 : PH[6] pin 8'h4A: PI[6] pin 8'h4B: PJ[6] pin 8'h4C: PK[6] pin 8'h4D : PA[7] pin 8'h4E : PB[7] pin 8'h4F : PC[7] pin 8'h50 : PD[7] pin 8'h51 : PE[7] pin 8'h52 : PF[7] pin 8'h53 : PG[7] pin 8'h54 : PH[7] pin 8'h55 : PI[7] pin 8'h56 : PJ[7] pin 8'h57 : PK[7] pin 8'h58 : PA[8] pin 8'h59 : PB[8] pin 8'h5A : PC[8] pin 8'h5B : PD[8] pin 8'h5C : PE[8] pin 8'h5D : PF[8] pin 8'h5E : PG[8] pin 8'h5F : PH[8] pin 8'h60 : PI[8] pin 8'h61 : PJ[8] pin 8'h62 : 0 8'h63 : PA[9] pin 8'h64 : PB[9] pin 8'h65 : PC[9] pin 8'h66 : PD[9] pin 8'h67 : PE[9] pin 8'h68: PF[9] pin 8'h69 : PG[9] pin 8'h6A : PH[9] pin

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		8'h6B : PI[9] pin 8'h6C : PJ[9] pin 8'h6D : 0 8'h6E : PA[10] pin 8'h6F : PB[10] pin 8'h70 : PC[10] pin 8'h71 : PD[10] pin 8'h72 : PE[10] pin 8'h73 : PF[10] pin 8'h74 : PG[10] pin 8'h75 : PH[10] pin 8'h76 : PI[10] pin 8'h77 : PJ[10] pin 8'h78 : 0 8'h79 : PA[11] pin 8'h7A : PB[11] pin 8'h7B : PC[11] pin 8'h7C : PD[11] pin 8'h7D : PE[11] pin 8'h7E : PF[11] pin 8'h7F: PG[11] pin 8'h80 : PH[11] pin 8'h81 : PI[11] pin 8'h82 : PJ[11] pin 8'h83 : 0 8'h84 : PA[12] pin 8'h85 : PB[12] pin 8'h86 : PC[12] pin 8'h87 : PD[12] pin 8'h88 : PE[12] pin 8'h89 : PF[12] pin 8'h8A : PG[12] pin 8'h8B : PH[12] pin 8'h8C : PI[12] pin 8'h8D : PJ[12] pin 8'h8E : 0 8'h8F : PA[13] pin 8'h90 : PB[13] pin 8'h91 : PC[13] pin

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		8'h92 : PD[13] pin 8'h93 : PE[13] pin 8'h94 : PF[13] pin 8'h95 : PG[13] pin 8'h96 : PH[13] pin 8'h97 : PI[13] pin 8'h98 : PJ[13] pin 8'h99 : 0 8'h9A : PA[14] pin 8'h9B : PB[14] pin 8'h9C: PC[14] pin 8'h9D : PD[14] pin 8'h9E : PE[14] pin 8'h9F : PF[14] pin 8'hA0 : PG[14] pin 8'hA1 : PH[14] pin 8'hA2 : PI[14] pin 8'hA3 : PJ[14] pin 8'hA4 : 0 8'hA5 : PA[15] pin 8'hA6 : PB[15] pin 8'hA7 : PC[15] pin 8'hA8 : PD[15] pin 8'hA9 : PE[15] pin 8'hAA : PF[15] pin 8'hAB : PG[15] pin 8'hAC : PH[15] pin 8'hAD : PI[15] pin 8'hAE : PJ[15] pin 8'hAF : 0 Others: reserved

12.5.11 AFIO External Interrupt Configuration Register 3 (AFIO_EXTI_CFG3)

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXTI15[7:0]								EXTI14[7:0]							
rw								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI13[7:0]								EXTI12[7:0]							

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rw rw

Bit Field	Name	Description
31:24 23:16 15:8 7:0	EXTIx[7:0]	EXTIx configuration（x = 12 … 15） These bits can be read and written by software to select the input source for the EXTIx external interrupt. 8'h0 : PA[0] pin 8'h1 : PB[0] pin 8'h2 : PC[0] pin 8'h3 : PD[0] pin 8'h4 : PE[0] pin 8'h5 : PF[0] pin 8'h6 : PG[0] pin 8'h7 : PH[0] pin 8'h8 : PI[0] pin 8'h9 : PJ[0] pin 8'hA : PK[0]pin 8'hB : PA[1] pin 8'hC : PB[1] pin 8'hD : PC[1] pin 8'hE : PD[1] pin 8'hF : PE[1] pin 8'h10 : PF[1 pin 8'h11 : PG[1] pin 8'h12 : PH[1] pin 8'h13 : PI[1] pin 8'h14 : PJ[1] pin 8'h15 : PK[1] pin 8'h16 : PA[2] pin 8'h17 : PB[2] pin 8'h18 : PC[2] pin 8'h19 : PD[2] pin 8'h1A : PE[2] pin 8'h1B : PF[2] pin 8'h1C : PG[2] pin 8'h1D : PH[2] pin 8'h1E : PI[2] pin 8'h1F : PJ[2] pin 8'h20 : PK[2] pin

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		8'h21 : PA[3] pin 8'h22 : PB[3] pin 8'h23 : PC[3] pin 8'h24 : PD[3] pin 8'h25 : PE[3] pin 8'h26 : PF[3] pin 8'h27 : PG[3] pin 8'h28 : PH[3] pin 8'h29 : PI[3] pin 8'h2A : PJ[3] pin 8'h2B : PK[3] pin 8'h2C : PA[4] pin 8'h2D : PB[4] pin 8'h2E : PC[4] pin 8'h2F : PD[4] pin 8'h30 : PE[4] pin 8'h31 : PF[4] pin 8'h32 : PG[4] pin 8'h33 : PH[4] pin 8'h34 : PI[4] pin 8'h35 : PJ[4] pin 8'h36 : PK[4] pin 8'h37 : PA[5] pin 8'h38 : PB[5] pin 8'h39 : PC[5] pin 8'h3A : PD[5] pin 8'h3B : PE[5] pin 8'h3C : PF[5] pin 8'h3D : PG[5] pin 8'h3E : PH[5] pin 8'h3F : PI[5] pin 8'h40 : PJ[5] pin 8'h41 : PK[5] pin 8'h42 : PA[6] pin 8'h43 : PB[6] pin 8'h44 : PC[6] pin 8'h45 : PD[6] pin 8'h46 : PE[6] pin 8'h47 : PF[6] pin 8'h48 : PG[6] pin

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		8'h49 : PH[6] pin 8'h4A: PI[6] pin 8'h4B: PJ[6] pin 8'h4C: PK[6] pin 8'h4D : PA[7] pin 8'h4E : PB[7] pin 8'h4F : PC[7] pin 8'h50 : PD[7] pin 8'h51 : PE[7] pin 8'h52 : PF[7] pin 8'h53 : PG[7] pin 8'h54 : PH[7] pin 8'h55 : PI[7] pin 8'h56 : PJ[7] pin 8'h57 : PK[7] pin 8'h58 : PA[8] pin 8'h59 : PB[8] pin 8'h5A : PC[8] pin 8'h5B : PD[8] pin 8'h5C : PE[8] pin 8'h5D : PF[8] pin 8'h5E : PG[8] pin 8'h5F : PH[8] pin 8'h60 : PI[8] pin 8'h61 : PJ[8] pin 8'h62 : 0 8'h63 : PA[9] pin 8'h64 : PB[9] pin 8'h65 : PC[9] pin 8'h66 : PD[9] pin 8'h67 : PE[9] pin 8'h68: PF[9] pin 8'h69 : PG[9] pin 8'h6A : PH[9] pin 8'h6B : PI[9] pin 8'h6C : PJ[9] pin 8'h6D : 0 8'h6E : PA[10] pin 8'h6F : PB[10] pin

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		8'h70 : PC[10] pin 8'h71 : PD[10] pin 8'h72 : PE[10] pin 8'h73 : PF[10] pin 8'h74 : PG[10] pin 8'h75 : PH[10] pin 8'h76 : PI[10] pin 8'h77 : PJ[10] pin 8'h78 : 0 8'h79 : PA[11] pin 8'h7A : PB[11] pin 8'h7B : PC[11] pin 8'h7C : PD[11] pin 8'h7D : PE[11] pin 8'h7E : PF[11] pin 8'h7F: PG[11] pin 8'h80 : PH[11] pin 8'h81 : PI[11] pin 8'h82 : PJ[11] pin 8'h83 : 0 8'h84 : PA[12] pin 8'h85 : PB[12] pin 8'h86 : PC[12] pin 8'h87 : PD[12] pin 8'h88 : PE[12] pin 8'h89 : PF[12] pin 8'h8A : PG[12] pin 8'h8B : PH[12] pin 8'h8C : PI[12] pin 8'h8D : PJ[12] pin 8'h8E : 0 8'h8F : PA[13] pin 8'h90 : PB[13] pin 8'h91 : PC[13] pin 8'h92 : PD[13] pin 8'h93 : PE[13] pin 8'h94 : PF[13] pin 8'h95 : PG[13] pin 8'h96 : PH[13] pin 8'h97 : PI[13] pin

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		8'h98 : PJ[13] pin 8'h99 : 0 8'h9A : PA[14] pin 8'h9B : PB[14] pin 8'h9C: PC[14] pin 8'h9D : PD[14] pin 8'h9E : PE[14] pin 8'h9F : PF[14] pin 8'hA0 : PG[14] pin 8'hA1 : PH[14] pin 8'hA2 : PI[14] pin 8'hA3 : PJ[14] pin 8'hA4 : 0 8'hA5 : PA[15] pin 8'hA6 : PB[15] pin 8'hA7 : PC[15] pin 8'hA8 : PD[15] pin 8'hA9 : PE[15] pin 8'hAA : PF[15] pin 8'hAB : PG[15] pin 8'hAC : PH[15] pin 8'hAD : PI[15] pin 8'hAE : PJ[15] pin 8'hAF : 0 Others: reserved

12.5.12 AFIO IO Port 5V Tolerance Configuration Register 0 (AFIO_TOL5V_CFG0)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PA7 TOLENN	PA6 TOLENN	PA5 TOLENN	PA4 TOLENN	PA3 TOLENN	PA2 TOLENN	PA1_C TOLENN	PA1 TOLENN	PA0_C TOLENN	PA0 TOLENN
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	PA7TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
8	PA6TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
7	PA5TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
6	PA4TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
5	PA3TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
4	PA2TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
3	PA1_CTOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
2	PA1TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
1	PA0_CTOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
0	PA0TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

12.5.13 AFIO IO Port 5V Tolerance Configuration Register 1 (AFIO_TOL5V_CFG1)

Address offset: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														PB1 TOLENN	PB0 TOLENN
														rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	PB1TOLENN	0: Disable 5V tolerance

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		1: Enable 5V tolerance
0	PB0TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

12.5.14 AFIO IO Port 5V Tolerance Configuration Register 2 (AFIO_TOL5V_CFG2)

Address offset: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					PC13 TOLENN	PC8 TOLENN	PC6 TOLENN	PC5 TOLENN	P4 TOLENN	PC3_C TOLENN	PC3 TOLENN	PC2_C TOLENN	PC2 TOLENN	PC1 TOLENN	PC0 TOLENN
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	PC13TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
9	PC8TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
8	PC6TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
7	PC5TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
6	PC4TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
5	PC3_CTOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
4	PC3TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
3	PC2_CTOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
2	PC2TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
1	PC1TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
0	PC0TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

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12.5.15 AFIO SHRTIM1 Fault Configuration Register (AFIO_SHRT1_FALT_CFG)

Address offset: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								SHRT_FALT6[3:0]				SHRT_FALT5[3:0]			
									rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRT_FALT4[3:0]				SHRT_FALT3[3:0]				SHRT_FALT2[3:0]				SHRT_FALT1[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:20 19:16 15:12 11:8 7:4 3:0	SHRT_FALTx[3:0]	SHRTIM1_FALTx configure fault channel (x=1…6): 0001: PA15 0010: PB3 0011: PC11 0100: PD4 0101: PE4 0110: PG9 0111: PG10 1000: PI6 1001: PI15 1010 : PK2 Others: Reserved

12.5.16 AFIO SHRTIM2 Fault Configuration Register (AFIO_SHRT2_FALT_CFG)

Address offset: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								SHRT_FALT6[3:0]				SHRT_FALT5[3:0]			
									rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRT_FALT4[3:0]				SHRT_FALT3[3:0]				SHRT_FALT2[3:0]				SHRT_FALT1[3:0]			

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rw rw rw rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:20 19:16 15:12 11:8 7:4 3:0	SHRT_FALTx[3:0]	SHRTIM2_FALTx configure fault channel (x=1…6): 0001: PC5 0010: PD1 0011: PD15 0100: PF9 0101: PF13 0110: PG1 0111: PI0 1000: PI9 1001: PI13 1010 : PJ0 1011 : PK1 1100 : PK6 Others : Reserved

12.5.17 AFIO IO Port 5V Tolerance Configuration Register 3 (AFIO_TOL5V_CFG3)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PF14 TOLENN	PF13 TOLENN	PF12 TOLENN	PF11 TOLENN	PF10 TOLENN	PF9 TOLENN	PF8 TOLENN	PF7 TOLENN	PF6 TOLENN	PF5 TOLENN	PF4 TOLENN	PF3 TOLENN
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	PF14TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
10	PF13TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
9	PF12TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

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8	PF11TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
7	PF10TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
6	PF9TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
5	PF8TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
4	PF7TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
3	PF6TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
2	PF5TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
1	PF4TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
0	PF3TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

12.5.18 AFIO IO Port 5V Tolerance Configuration Register 4 (AFIO_TOL5V_CFG4)

Address offset: 0x44

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PH5 TOLENN	PH4 TOLENN	PH3 TOLENN	PH2 TOLENN
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	PH5TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
2	PH4TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
1	PH3TOLENN	0: Disable 5V tolerance

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		1: Enable 5V tolerance
0	PH2TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

12.5.19 AFIO IO Port 5V Tolerance Configuration Register 5 (AFIO_TOL5V_CFG5)

Address offset: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														PI15 TOLENN	PI8 TOLENN
														rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	PI15TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
0	PI8TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

12.5.20 AFIO IO Port 5V Tolerance Configuration Register 6 (AFIO_TOL5V_CFG6)

Address offset: 0x4C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										PJ7 TOLENN	PJ6 TOLENN	PJ5 TOLENN	PJ4 TOLENN	PJ3 TOLENN	PJ0 TOLENN
										rw	rw	rw	rw	rw	rw

Bit Field	Name	Description

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31:6	Reserved	Reserved, the reset value must be maintained.
5	PJ7TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
4	PJ6TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
3	PJ5TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
2	PJ4TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
1	PJ3TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance
0	PJ0TOLENN	0: Disable 5V tolerance 1: Enable 5V tolerance

12.5.21 AFIO IO Port Analog Filtering Configuration Register 0 (AFIO_EFT_CFG0)

Address offset: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PB_EFTEN[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA_EFTEN[15:0]															
rw															

Bit Field	Name	Description
31:16	PB_EFTEN [15:0]	PBx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PB3,PB4,PB9 (Rest are unconnected)
15:0	PA_EFTEN [15:0]	PAx EFT enable (x = 0 … 15) 0: Disable EFT 1: Enable EFT Supported IOs: PA8,PA10,PA11,PA12,PA13,PA14,PA15 (Rest are unconnected)

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12.5.22 AFIO IO Port Analog Filtering Configuration Register 1 (AFIO_EFT_CFG1)

Address offset: 0x58

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD_EFTEN[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC_EFTEN15:0]															
rw															

Bit Field	Name	Description
31:16	PD_EFTEN [15:0]	PDx EFT enable (x = 0 … 15) 0:Disable EFT IE 1: Enable EFT IE Supported IOs: PD3 (Rest are unconnected)
15:0	PC_EFTEN [15:0]	PCx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PC6,PC7,PC8,PC13,PC14,PC15 (Rest are unconnected)

12.5.23 AFIO IO Port Analog Filtering Configuration Register 2 (AFIO_EFT_CFG2)

Address offset: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PF_EFTEN[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PE_EFTEN15:0]															
rw															

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Bit Field	Name	Description
31:16	PF_EFTEN [15:0]	PFx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: No pads supported
15:0	PE_EFTEN [15:0]	PEx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PE4,PE6 (Rest are unconnected)

12.5.24 AFIO IO Port Analog Filtering Configuration Register 3 (AFIO_EFT_CFG3)

Address offset: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PH_EFTEN[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PG_EFTEN15:0]															
rw															

Bit Field	Name	Description
31:16	PH_EFTEN [15:0]	PHx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PH0,PH1,PH4(Rest are unconnected)
15:0	PG_EFTEN [15:0]	PGx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PG3 (Rest are unconnected)

12.5.25 AFIO IO Port Analog Filtering Configuration Register 4 (AFIO_EFT_CFG4)

Address offset: 0x64

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_EFTEN[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PJ_EFTEN15:0]															
rw															

Bit Field	Name	Description
31:16	PI_EFTEN [15:0]	PJx EFT enable(x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PI8,PI15 (Rest are unconnected)
15:0	PJ_EFTEN [15:0]	PIx EFT enable (x = 0 … 15) 0: Disable EFT IE 1: Enable EFT IE Supported IOs:PJ0,PJ3,PJ4,P5,PJ6,PJ7,PJ8,PJ9,PJ10,PJ11,PJ12,PJ14,PJ15 (Rest are unconnected)

12.5.26 AFIO IO Port Analog Filtering Configuration Register 5 (AFIO_EFT_CFG5)

Address offset: 0x68

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						JRST_EFTBYPS	BOOT_EFTEN	PK_EFTEN[7:0]							
						rw	rw	rw							

Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	JRST_EFTBYPS	BYPASS 0: Filtered output 1: Unfiltered output for JTAG RST
8	BOOT_EFTEN	BOOT pin EFT enable

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Bit Field	Name	Description
		0: Disable EFT IE 1: Enable EFT IE
7:0	PK_EFTEN[7:0]	PKx EFT enable (x = 0 … 7) 0: Disable EFT IE 1: Enable EFT IE Supported IOs: PK0,PK1,PK2 (Rest are unconnected)

12.5.27 AFIO IO Port Digital Filtering Configuration Register 0 (AFIO_DIGEFT_CFG0)

Address offset: 0x6C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PB_DIGEFTEN[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA_DIGEFTEN [15:0]															
rw															

Bit Field	Name	Description
31:16	PB_DIGEFTEN[15:0]	PBx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PBx 1: Enable digital filtering for port PBx
15:0	PA_DIGEFTEN[15:0]	PAx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PAx 1: Enable digital filtering for port PAx

12.5.28 AFIO IO Port Digital Filtering Configuration Register 1 (AFIO_DIGEFT_CFG1)

Address offset: 0x70

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD_DIGEFTEN[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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PC_DIGEFTEN[15:0]

rw

Bit Field	Name	Description
31:16	PD_DIGEFTEN [15:0]	PDx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PDx 1: Enable digital filtering for port PDx
15:0	PC_DIGEFTEN[15:0]	PCx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PCx 1: Enable digital filtering for port PCx

12.5.29 AFIO IO Port Digital Filtering Configuration Register 2 (AFIO_DIGEFT_CFG2)

Address offset: 0x74

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PF_DIGEFTEN[15:0]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PE_DIGEFTEN[15:0]															

rw

Bit Field	Name	Description
31:16	PF_DIGEFTEN[15:0]	PFx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PFx 1: Enable digital filtering for port PFx
15:0	PE_DIGEFTEN[15:0]	PEx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PEx 1: Enable digital filtering for port PEx

12.5.30 AFIO IO Port Digital Filtering Configuration Register 3 (AFIO_DIGEFT_CFG3)

Address offset: 0x78

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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PH_DIGEFTEN[15:0]

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PG_DIGEFTEN[15:0]															

rw

Bit Field	Name	Description
31:16	PH_DIGEFTEN[15:0]	PHx port digital filtering enable bit (x = 0 …15) 0: Disable digital filtering for port PHx 1: Enable digital filtering for port PHx
15:0	PG_DIGEFTEN[15:0]	PGx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PGx 1: Enable digital filtering for port PGx

12.5.31 AFIO IO Port Digital Filtering Configuration Register 4 (AFIO_DIGEFT_CFG4)

Address offset: 0x7C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_DIGEFTEN[15:0]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PJ_DIGEFTEN[15:0]															

rw

Bit Field	Name	Description
31:16	PI_DIGEFTEN[6:0]	PIx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PIx 1: Enable digital filtering for port PIx
15:0	PJ_DIGEFTEN[15:0]	PJx port digital filtering enable bit (x = 0 … 15) 0: Disable digital filtering for port PJx 1: Enable digital filtering for port PJx

12.5.32 AFIO IO Port Digital Filtering Configuration Register 5 (AFIO_DIGEFT_CFG5)

Address offset: 0x80

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PK_DIGEFTEN[7:0]							
								rw							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	PK_DIGEFTEN[7:0]	PKx port digital filtering enable bit (x = 0 … 7) 0: Disable digital filtering for port PKx 1: Enable digital filtering for port PKx

12.5.33 AFIO SHRTIM1 External Event Configuration Register 0 (AFIO_SHRT1_EXEV_CFG0)

Address offset: 0x84

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							SHRT_EXEV5[4:0]					SHRT_EXEV4[4:1]			
							rw					rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRT_EVEX4[0]	SHRT_EXEV3[4:0]						SHRT_EXEV2[4:0]					SHRT_EXEV1[4:0]			
rw	rw						rw					rw			

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:20 19:15 14:10 9:5 4:0	SHRT_EXEVx[4:0]	SHRTIM1_EXEVx configure external event input channel (x=1…5): 00001: PB4 00010: PB5 00011: PB6 00100: PB7 00101: PC10 00110: PC12 00111: PD5

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		01000: PD8 01001: PD9 01010: PE6 01011: PG0 01100: PG11 01101: PG12 01110: PG13 01111: PI14 10000: PJ5 10001: PK3 10010: PK4 Others: Reserved

12.5.34 AFIO SHRTIM1 External Event Configuration Register 1 (AFIO_SHRT1_EXEV_CFG1)

Address offset: 0x88

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							SHRT_EXEV10 [4:0]					SHRT_EXEV9 [4:1]			
									rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRT_EXEV9[0]	SHRT_EXEV8 [4:0]						SHRT_EXEV7[4:0]					SHRT_EXEV6[4:0]			
	rw						rw					rw			

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:20 19:15 14:10 9:5 4:0	SHRT_EXEVx[4:0]	SHRTIM1_EXEVx configure external event input channel (x=6…10): 00001: PB4 00010: PB5 00011: PB6 00100: PB7 00101: PC10 00110: PC12 00111: PD5 01000: PD8 01001: PD9 01010: PE6 01011: PG0

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		01100: PG11 01101: PG12 01110: PG13 01111: PI14 10000: PJ5 10001: PK3 10010: PK4 Others: Reserved

12.5.35 AFIO SHRTIM2 External Event Configuration Register 0 (AFIO_SHRT2_EXEV_CFG0)

Address offset: 0x8C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							SHRT_EXEV5[4:0]					SHRT_EXEV4[4:1]			
									rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRT_EVEX4[0]	SHRT_EXEV3[4:0]					SHRT_EXEV2[4:0]					SHRT_EXEV1[4:0]				
rw						rw					rw				

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:20 19:15 14:10 9:5 4:0	SHRT_EXEVx[4:0]	SHRTIM2_EXEVx configure external event input channel (x=1…5): 00001: PA2 00010: PC4 00011: PD0 00100: PD11 00101: PE3 00110: PE14 00111: PF10 01000: PG8 01001: PG15 01010: PH7 01011: PH8 01100: PH10 01101: PH11 01110: PH12 01111: PI11 10000: PJ2

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		10001: PJ14 10010: PK0 Others: Reserved

12.5.36 AFIO SHRTIM2 External Event Configuration Register 1 (AFIO_SHRT2_EXEV_CFG1)

Address offset: 0x90

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							SHRT_EXEV10 [4:0]					SHRT_EXEV9 [4:1]			
									rw				rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHRT_EXEV9[0]	SHRT_EXEV8 [4:0]					SHRT_EXEV7[4:0]					SHRT_EXEV6[4:0]				
	rw					rw					rw				

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:20 19:15 14:10 9:5 4:0	SHRT_EXEVx[4:0]	SHRTIM2_EXEVx configure external event input channel (x=6…10): 00001: PA2 00010: PC4 00011: PD0 00100: PD11 00101: PE3 00110: PE14 00111: PF10 01000: PG8 01001: PG15 01010: PH7 01011: PH8 01100: PH10 01101: PH11 01110: PH12 01111: PI11 10000: PJ2 10001: PJ14 10010: PK0

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		Others: Reserved

12.5.37 AFIO SIP Pull-up/Pull-down Configuration Register (AFIO_SIP_PUPD)

Address offset: 0x94

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUPD7		PUPD6		PUPD5		PUPD4		PUPD3		PUPD2		PUPD1		PUPD0	
rw		rw		rw		rw		rw		rw		rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	PUPDx	x= 0…7 SIP XSPI data pads pull up - pull down configuration 00: No pull-up, pull-down 01: Pull-up 10: Pull-down 11: Reserved

12.5.38 AFIO SDRAM HS MODE Configuration Register (AFIO_SDRAM_HSMOD_CFG0)

Address offset: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSA15	HSA14	HSA13	HSA12	HSA11	HSA10	HSA9	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSB15	HSB14	HSB13	HSB12	HSB11	HSB10	HSB9	HSB8	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	HSA[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM Only PA4,PA5,PA7 are functional
15:0	HSB[15:0]	HS_EN pad interface connection for SDRAM PAD model

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Bit Field	Name	Description
		0: Disable 1: Enable – SDRAM Only PB5,PB6,PB14,PB15 are functional HSMODE_B[0] = PB0 HSMODE_B[1] = PB1 …. HSMODE_[15] = PB15

12.5.39 AFIO SDRAM HS MODE Configuration Register (AFIO_SDRAM_HSMOD_CFG1)

Address offset: 0x9C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSC15	HSC14	HSC13	HSC12	HSC11	HSC10	HSC9	HSC8	HSC7	HSC6	HSC5	HSC4	HSC3	HSC2	HSC1	HSC0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSD15	HSD14	HSD13	HSD12	HSD11	HSD10	HSD9	HSD8	HSD7	HSD6	HSD5	HSD4	HSD3	HSD2	HSD1	HSD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	HSC[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM (HSMODE_C[15:13] will be used as MODE configuration bit for pad PC[15:13] in BKP)- SDRAM PC0,PC2,PC3,PC4,PC5,PC12
15:0	HSD[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM PD0,PD1,PD2,PD8,PD9,PD10,PD14,PD15

12.5.40 AFIO SDRAM HS MODE Configuration Register (AFIO_SDRAM_HSMOD_CFG2)

Address offset: 0xA0

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSE15	HSE14	HSE13	HSE12	HSE11	HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSF15	HSF14	HSF13	HSF12	HSF11	HSF10	HSF9	HSF8	HSF7	HSF6	HSF5	HSF4	HSF3	HSF2	HSF1	HSF0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	HSE[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM PE0,PE1,PE7,PE8,PE9,PE10,PE11,PE12,PE13,PE14,PE15
15:0	HSF[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM PF0,PF1,PF2,PF3,PF4,PF5,PF11,PF12,PF13,PF14,PF15

12.5.41 AFIO SDRAM HS MODE Configuration Register (AFIO_SDRAM_HSMOD_CFG3)

Address offset: 0xA4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSG15	HSG14	HSG13	HSG12	HSG11	HSG10	HSG9	HSG8	HSG7	HSG6	HSG5	HSG4	HSG3	HSG2	HSG1	HSG0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSH15	HSH14	HSH13	HSH12	HSH11	HSH10	HSH9	HSH8	HSH7	HSH6	HSH5	HSH4	HSH3	HSH2	HSH1	HSH0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	HSG[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM PG0,PG1,PG2,PG4,PG5,PG15
15:0	HSH[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM PH2,PH3,PH5,PH6,PH7,PH8,PH9,PH10,PH11,PH12,PH13,PH14,PH15

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12.5.42 AFIO SDRAM HS MODE Configuration Register (AFIO_SDRAM_HSMOD_CFG4)

Address offset: 0xA8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSI15	HSI14	HSI13	HSI12	HSI11	HSI10	HSI9	HSI8	HSI7	HSI6	HSI5	HSI4	HSI3	HSI2	HSI1	HSI0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:16	HSI[15:0]	HS_EN pad interface connection for SDRAM PAD model 0: Disable 1: Enable - SDRAM PI0,PI1,PI2,PI3,PI4,PI5,PI6,PI7,PI9,PI10
15:0	Reserved	Reserved, the reset value must be maintained.

12.5.43 AFIO SIP SR Configuration Register (AFIO_SIP_SR)

Address offset: 0xB0

Reset value: 0x0000 00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	SRy	SIP XSPI data pads slew rate configuration(y=0…7) 0: fast slew rate 1: slow slew rate

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12.5.44 AFIO SIP DS Configuration Register (AFIO_SIP_DS)

Address offset: 0xB4

Reset value: 0x0000 5555

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS7[1:0]		DS6[1:0]		DS5[1:0]		DS4[1:0]		DS3[1:0]		DS2[1:0]		DS1[1:0]		DS0[1:0]	
rw		rw		rw		rw		rw		rw		rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	DSy	SIP XSPI data pads driver strength configuration(y= 0…7) 00：2mA driver strength 10：4mA driver strength 01：8mA driver strength 11：12mA driver strength

12.5.45 AFIO ADC Switch Configuration Register (AFIO_ADCSW_CFG)

Address offset: 0xD0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			VREF	SWPJ7	SWPJ6	DAC135_SEL[2:0]			SWPJ5	SWPJ4	TEMP	SWPJ3	SWPJ0	DAC246_SEL[2:1]	
			rw	rw	rw	rw			rw	rw	rw	rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC246_SEL[0]	VBAT	SWPI15[1:0]		SWPA1_C[1:0]		SWPC3_C[1:0]		SWPC2_C[1:0]				SWPA0_C[3:0]			
rw	rw	rw		rw		rw		rw				rw			

Bit Field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	VREF	Vrefint monitor enable in ADC3_INP19 0: Disable.

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		1: Enable
27	SWPJ7	PJ7 switch open 0: PJ7 analog switch closed 1: PJ7 analog switch open for ADC3_INP19
26	SWPJ6	PJ6 switch open 0: PJ6 analog switch closed 1: PJ6 analog switch open for ADC3_INP18
25:23	DAC135_SEL[2:0]	DAC135 monitor enable in ADC2_INP16(x=1,2,3) 000: Disable. 001: DAC1 monitor enable in ADC2_INP16 010: DAC3 monitor enable in ADC2_INP16 100: DAC5 monitor enable in ADC2_INP16 Others: Reserved
22	SWPJ5	PJ5 switch open 0: PJ5 analog switch closed 1: PJ5 analog switch open for ADC2_INP16
21	SWPJ4	PJ4 switch open 0: PJ4 analog switch closed 1: PJ4 analog switch open for ADC3_INP19
20	TEMP	Temperature monitor enable in ADC3_INP18 0: Disable. 1: Enable
19	SWPJ3	PJ3 switch open 0: PJ3 analog switch closed 1: PJ3 analog switch open for ADC3_INP18
18	SWPJ0	PJ0 switch open 0: PJ0 analog switch closed 1: PJ0 analog switch open for ADC2_INP16
17:15	DAC246_SEL[2:0]	DAC246 monitor enable in ADC2_INP17 000: Disable. 001: DAC2 monitor enable in ADC2_INP17 010: DAC4 monitor enable in ADC2_INP17 100: DAC6 monitor enable in ADC2_INP17 Others: Reserved
14	VBAT	VABT monitor enable in ADC3_INP17 0: Disable. 1: Enable
13:12	SWPI15[1:0]	PI15 switch open 00: Analog switch closed. 01: Analog switch open PI15 for ADC2_INP17 10: Analog switch open PI15 for ADC3_INP17 Other: Reserved

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11:10	SWPA1_C[1:0]	PA1_C switch open 00: Analog switch closed. 01: Analog switch open PA1_C for ADC2_INP1. 10: Analog switch open PA1_C for ADC1_INP1. Other: Reserved
9:8	SWPC3_C[1:0]	PC3_C switch open 00: Analog switch closed. 01: Analog switch open PC3_C for ADC2_INP1 10: Analog switch open PC3_C for ADC3_INP2 Other: Reserved
7:4	SWPC2_C[3:0]	PC2_C switch open 0000: Analog switch closed. 0001: Analog switch open PC2_C for ADC2_INP0 0010: Analog switch open PC2_C for ADC2_INN1 0100: Analog switch open PC2_C for ADC3_INP0 1000: Analog switch open PC2_C for ADC3_INN1 Other: Reserved
3:0	SWPA0_C[3:0]	PA0_C switch open. 0000: Analog switch closed. 0001: Analog switch open PA0_C for ADC2_INP0 0010: Analog switch open PA0_C for ADC2_INN1 0100: Analog switch open PA0_C for ADC1_INP0 1000: Analog switch open PA0_C for ADC1_INN1 Other: Reserved

12.5.46 AFIO SDRAM VREF Enable 0 Configuration Register (AFIO_SDRAM_VREF_EN0)

Address offset: 0xD8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VREF_EN0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VREF_EN0[15:0]															
rw															

Bit Field	Name	Description
31:0	VREF_EN0[31:0]	VREF_EN PAD signal connection for SDRAM PAD Model

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		SDRAM_VREF_EN [72:0] = { VREF_EN2 , VREF_EN1, VREF_EN0 }; SDRAM_VREF_EN [72:0] refer to Table 12-118.

Table 12-118 SDRAM PAD

80	79	78	76	75	74	73	72	71	70	69	68	67	66	65	64
Reserved							PI10	PI9	PI7	PI6	PI5	PI4	PI3	PI2	PI1
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
PI0	PH15	PH14	PH13	PH12	PH11	PH10	PH9	PH8	PH7	PH6	PH5	PH3	PH2	PG15	PG8
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
PG5	PG4	PG2	PG1	PG0	PF15	PF14	PF13	PF12	PF11	PF5	PF4	PF3	PF2	PF1	PF0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE1	PE0	PD15	PD14	PD10	PD9	PD8
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD2	PD1	PD0	PC12	PC5	PC4	PC3	PC2	PC0	PB15	PB14	PB6	PB5	PA7	PA5	PA4

12.5.47 AFIO SDRAM VREF Enable 1 Configuration Register (AFIO_SDRAM_VREF_EN1)

Address offset: 0xDC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VREF_EN1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VREF_EN1[15:0]															
rw															

Bit Field	Name	Description
31:0	VREF_EN1[31:0]	VREF_EN PAD signal connection for SDRAM PAD Model SDRAM_VREF_EN[72:0] = { VREF_EN2 ,VREF_EN1, VREF_EN0 }; SDRAM_VREF_EN [72:0] refer to Table 12-118.

12.5.48 AFIO SDRAM VREF Enable 2 Configuration Register (AFIO_SDRAM_VREF_EN2)

Address offset: 0xE0

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							VREF_EN2[8:0]								
							rw								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8:0	VREF_EN2[8:0]	VREF_EN PAD signal connection for SDRAM PAD Model SDRAM_VREF_EN [72:0] = {VREF_EN2 ,VREF_EN1, VREF_EN0 } SDRAM_VREF_EN [72:0] refer to Table 12-118.

12.5.49 AFIO SDRAM DSN 0 Configuration Register (AFIO_SDRAMDSN_CFG0)

Address offset: 0xE4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSN0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSN0[15:0]															
rw															

Bit Field	Name	Description
31:0	DSN0[31:0]	DSN PAD signal connection for SDRAM PAD Model SDRAM_DSN [74:0] = {DSN2 , DSN1, DSN0 } SDRAM_DSN [74:0] refer to Table 12-118.

12.5.50 AFIO SDRAM DSN 1 Configuration Register (AFIO_SDRAMDSN_CFG1)

Address offset: 0xE8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSN1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSN1[15:0]															

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rw

Bit Field	Name	Description
31:0	DSN1[31:0]	DSN PAD signal connection for SDRAM PAD Model SDRAM_DSN [72:0]= {DSN2 , DSN1, DSN0 } SDRAM_DSN [72:0] refer to Table 12-118.

12.5.51 AFIO SDRAM DSN 2 Configuration Register (AFIO_SDRAMDSN_CFG2)

Address offset: 0xEC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DSN2[8:0]								

rw

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8:0	DSN2[8:0]	DSN PAD signal connection for SDRAM PAD Model SDRAM_DSN [72:0]= {DSN2 , DSN1, DSN0 } SDRAM_DSN [72:0] = refer to Table 12-118.

12.5.52 AFIO SDRAM DSP 0 Configuration Register (AFIO_SDRAMDSP_CFG0)

Address offset: 0xF0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSP0[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSP1[15:0]															

rw

Bit Field	Name	Description
31:0	DSP0[31:0]	DSP PAD signal connection for SDRAM PAD Model SDRAM_DSP [72:0]= {DSN2 , DSN1, DSN0 }

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		SDRAM_DSP [72:0] refer to Table 12-118.

12.5.53 AFIO SDRAM DSP 1 Configuration Register (AFIO_SDRAMDSP_CFG1)

Address offset: 0xF4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSP1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSP1[15:0]															
rw															

Bit Field	Name	Description
31:0	DSP1[31:0]	DSP PAD signal connection for SDRAM PAD Model SDRAM_DSP [72:0]= {DSN2 , DSN1, DSN0 } SDRAM_DSP [72:0] refer to Table 12-118.

12.5.54 AFIO SDRAM DSP 2 Configuration Register (AFIO_SDRAMDSP_CFG2)

Address offset: 0xF8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DSP2[8:0]								
							rw								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8:0	DSP2[8:0]	DSP PAD signal connection for SDRAM PAD Model SDRAM_DSP [72:0]= {DSN2 , DSN1, DSN0 } SDRAM_DSP [72:0] refer to Table 12-118.

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13 Interrupts and Events

13.1 Nested Vector Interrupt Controller

13.1.1 NVIC features

Both CPU1 (Cortex-M7) and CPU2 (Cortex-M4) cores contains their own Nested Vector Interrupt Controller (respectively NVIC1 and NVIC2). N32Hxxx supports the following interrupt configuration:

- 234 maskable interrupt channels
- 16 programmable priority levels

The NVIC handles the management of interrupt and exceptions.

For more information on NVIC, refer to PM0253 and PM0214 programming manuals for Cortex-M7 and for Cortex-M4, respectively

13.1.2 SysTick calibration value register

The SysTick calibration value (SYST_CALIB) is set to constant 0x3E8.

It provides a reference time-base of 1 ms with respect to the SysTick frequency of 1MHz.

The SysTick reload value must be programmed in the SYST_RVR register based on the frequency employed in the application:

For instance, the reloading value = (100 × SYST_CALIB) - 1 = 0x1869F when the SysTick frequency is 100MHz.

13.1.3 Interrupt and exception vectors

Reset, NMI, HardFault, MemManage, Bus Fault, UsageFault, SVCall, DebugMonitor, PendSV, and SysTick are CPU's internal exceptions connected to its NVIC.

CPU's Floating Point Unit (FPU) interrupt connected to its NVIC, in position 55.

SEMA4 interrupt line 1 is connected to the NVIC1 position 172, while SEMA4 interrupt line 2 is connected to the NVIC2 position 173.

DCMUA interrupt is connected to the NVIC1 position 177, while DCMUB interrupt line is connected to the NVIC2 on the same position.

CM4 AHB ICache and DCache interrupts are only connected to NVIC2, position 53 and 54 accordingly.

WWDG1 interrupt is connected to NVIC1 position 0, whereas WWDG2 interrupt is connected to the NVIC2 position 0.

WWDG1 reset is connected to the NVIC2 position 174 via the EXTI whereas WWDG2 reset is connected to the NVIC1 position 174 via EXTI.

Remaining interrupt lines are routed in a symmetrical way on both NVIC1 and NVIC2.

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Table 13-1 NVIC1 and NVIC2 mapping

NVIC1 (CM7)	NVIC2 (CM4)	Priority	Acronym	Description	Address offset
-	-	-	MSP	Main Stack pointer	0x00000000
-	-	-3	Reset	Reset	0x00000004
-	-	-2	NMI	Non-Maskable Interrupt (RCC CSS)	0x00000008
-	-	-1	HardFault	All faults	0x0000000C
-	-	0	MemManage	Memory Management	0x00000010
-	-	1	BusFault	Prefetch fault, memory access fault	0x00000014
-	-	2	UsageFault	Undefined instruction or illegal state	0x00000018
-	-	-	-	Reserved	0x0000001C
-	-	-	-	Reserved	0x00000020
-	-	-	-	Reserved	0x00000024
-	-	-	-	Reserved	0x00000028
-	-	3	SVCall	System Service Call via SWI instruction	0x0000002C
-	-	4	DebugMonitor	Debug Monitor	0x00000030
-	-	-	-	-	0x00000034
-	-	5	PendSV	Pendable request for system service	0x00000038
-	-	6	Systick	System tick timer	0x0000003C
0	-	7	WWDG1	WWDG1 interrupt	0x00000040
-	0	7	WWDG2	WWDG2 interrupt	0x00000040
1	1	8	PVD	PVD through EXTI line 16	0x00000044
2	2	9	RTC_TAMPER	RTC tamper, timestamp or CSS LSE or RTC OVERFLOW or LSICSS through EXTI line 18	0x00000048
3	3	10	RTC_WKUP	RTC Wakeup interrupt through EXTI line 19	0x0000004C
4	4	11	RCC	RCC global interrupt	0x00000050
5	5	12	EXTI0	EXTI Line 0 interrupt	0x00000054
6	6	13	EXTI1	EXTI Line 1 interrupt	0x00000058
7	7	14	EXTI2	EXTI Line 2 interrupt	0x0000005C
8	8	15	EXTI3	EXTI Line 3 interrupt	0x00000060
9	9	16	EXTI4	EXTI Line 4 interrupt	0x00000064
10	10	17	EXTI9_5	EXTI Line[9:5] interrupt	0x00000068
11	11	18	EXTI15_10	EXTI Line[15:10] interrupt	0x0000006C
12	12	19	DMA1_channel_0	DMA1 channel 0 global interrupt	0x00000070
13	13	20	DMA1_channel_1	DMA1 channel 1 global interrupt	0x00000074
14	14	21	DMA1_channel_2	DMA1 channel 2 global interrupt	0x00000078

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15	15	22	DMA1_channel_3	DMA1 channel 3 global interrupt	0x0000007C
16	16	23	DMA1_channel_4	DMA1 channel 4 global interrupt	0x00000080
17	17	24	DMA1_channel_5	DMA1 channel 5 global interrupt	0x00000084
18	18	25	DMA1_channel_6	DMA1 channel 6 global interrupt	0x00000088
19	19	26	DMA1_channel_7	DMA1 channel 7 global interrupt	0x0000008C
20	20	27	DMA2_channel_0	DMA2 channel 0 global interrupt	0x00000090
21	21	28	DMA2_channel_1	DMA2 channel 1 global interrupt	0x00000094
22	22	29	DMA2_channel_2	DMA2 channel 2 global interrupt	0x00000098
23	23	30	DMA2_channel_3	DMA2 channel 3 global interrupt	0x0000009C
24	24	31	DMA2_channel_4	DMA2 channel 4 global interrupt	0x000000A0
25	25	32	DMA2_channel_5	DMA2 channel 5 global interrupt	0x000000A4
26	26	33	DMA2_channel_6	DMA2 channel 6 global interrupt	0x000000A8
27	27	34	DMA2_channel_7	DMA2 channel 7 global interrupt	0x000000AC
28	28	35	DMA3_channel_0	DMA3 channel 0 global interrupt	0x000000B0
29	29	36	DMA3_channel_1	DMA3 channel 1 global interrupt	0x000000B4
30	30	37	DMA3_channel_2	DMA3 channel 2 global interrupt	0x000000B8
31	31	38	DMA3_channel_3	DMA3 channel 3 global interrupt	0x000000BC
32	32	39	DMA3_channel_4	DMA3 channel 4 global interrupt	0x000000C0
33	33	40	DMA3_channel_5	DMA3 channel 5 global interrupt	0x000000C4
34	34	41	DMA3_channel_6	DMA3 channel 6 global interrupt	0x000000C8
35	35	42	DMA3_channel_7	DMA3 channel 7 global interrupt	0x000000CC
36	36	43	MDMA_channel_0	MDMA channel 0 global interrupt	0x000000D0
37	37	44	MDMA_channel_1	MDMA channel 1 global interrupt	0x000000D4
38	38	45	MDMA_channel_2	MDMA channel 2 global interrupt	0x000000D8
39	39	46	MDMA_channel_3	MDMA channel 3 global interrupt	0x000000DC
40	40	47	MDMA_channel_4	MDMA channel 4 global interrupt	0x000000E0
41	41	48	MDMA_channel_5	MDMA channel 5 global interrupt	0x000000E4
42	42	49	MDMA_channel_6	MDMA channel 6 global interrupt	0x000000E8
43	43	50	MDMA_channel_7	MDMA channel 7 global interrupt	0x000000EC
44	44	51	MDMA_channel_8	MDMA channel 8 global interrupt	0x000000F0
45	45	52	MDMA_channel_9	MDMA channel 9 global interrupt	0x000000F4
46	46	53	MDMA_channel_10	MDMA channel 10 global interrupt	0x000000F8
47	47	54	MDMA_channel_11	MDMA channel 11 global interrupt	0x000000FC
48	48	55	MDMA_channel_12	MDMA channel 12 global interrupt	0x00000100
49	49	56	MDMA_channel_13	MDMA channel 13 global interrupt	0x00000104
50	50	57	MDMA_channel_14	MDMA channel 14 global interrupt	0x00000108
51	51	58	MDMA_channel_15	MDMA channel 15 global interrupt	0x0000010C
52	52	59	SDPU	SDPU global interrupt	0x00000110

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53	-	60	-	Reserved	0x00000114
-	53		AHB CM4 iCache	CM4 AHB iCache interrupt	
54	-	61	-	Reserved	0x00000118
-	54		AHB CM4 dCache	CM4 AHB dCache interrupt	
55	-	62	FPU_CPU1	FPU_CM7 global interrupt	0x0000011C
-	55		FPU_CPU2	FPU_CM4 global interrupt	
56	56	63	ECCMON	ECCMON global interrupt	0x00000120
57	57	64	RTC ALARM	RTC Alarm through EXTI line 17	0x00000124
58	58	65	I2C1_EVENT	I2C1 Event interrupt	0x00000128
59	59	66	I2C1_ERR	I2C1 error interrupt	0x0000012C
60	60	67	I2C2_EVENT	I2C2 Event interrupt	0x00000130
61	61	68	I2C2_ERR	I2C2 error interrupt	0x00000134
62	62	69	I2C3_EVENT	I2C3 Event interrupt	0x00000138
63	63	70	I2C3_ERR	I2C3 error interrupt	0x0000013C
64	64	71	I2C4_EVENT	I2C4 Event interrupt	0x00000140
65	65	72	I2C4_ERR	I2C4 error interrupt	0x00000144
66	66	73	I2C5_EVENT	I2C5 Event interrupt	0x00000148
67	67	74	I2C5_ERR	I2C5 error interrupt	0x0000014C
68	68	75	I2C6_EVENT	I2C6 Event interrupt	0x00000150
69	69	76	I2C6_ERR	I2C6 error interrupt	0x00000154
70	70	77	I2C7_EVENT	I2C7 Event interrupt	0x00000158
71	71	78	I2C7_ERR	I2C7 error interrupt	0x0000015C
72	72	79	I2C8_EVENT	I2C8 Event interrupt	0x00000160
73	73	80	I2C8_ERR	I2C8 error interrupt	0x00000164
74	74	81	I2C9_EVENT	I2C9 Event interrupt	0x00000168
75	75	82	I2C9_ERR	I2C9 error interrupt	0x0000016C
76	76	83	I2C10_EVENT	I2C10 Event interrupt	0x00000170
77	77	84	I2C10_ERR	I2C10 error interrupt	0x00000174
78	78	85	I2S1	I2S1 global interrupt	0x00000178
79	79	86	I2S2	I2S1 global interrupt	0x0000017C
80	80	87	I2S3	I2S1 global interrupt	0x00000180
81	81	88	I2S4	I2S1 global interrupt	0x00000184
82	82	89	xSPI1_IRQ	xSPI1 global interrupt	0x00000188
83	83	90	xSPI2_IRQ	xSPI1 global interrupt	0x0000018C
84	84	91	SPI1	SPI1 global interrupt	0x00000190
85	85	92	SPI2	SPI2 global interrupt	0x00000194
86	86	93	SPI3	SPI3 global interrupt	0x00000198
87	87	94	SPI4	SPI4 global interrupt	0x0000019C

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88	88	95	SPI5	SPI5 global interrupt	0x000001A0
89	89	96	SPI6	SPI6 global interrupt	0x000001A4
90	90	97	SPI7	SPI7 global interrupt	0x000001A8
91	91	98	LCD_EVENT	TFT LCD Controller event interrupt	0x000001AC
92	92	99	LCD_ERR	TFT LCD Controller error interrupt	0x000001B0
93	93	100	DVP1	DVP1 global interrupt	0x000001B4
94	94	101	DVP2	DVP1 global interrupt	0x000001B8
95	95	102	DMAMUX2	DMAMUX2 (MDMA MUX) global interrupt	0x000001BC
96	96	103	USBHS1_HS_EPx_OUT	USBHS1_HS endpoint out global interrupt	0x000001C0
97	97	104	USBHS1_HS_EPx_IN	USBHS1_HS endpoint in global interrupt	0x000001C4
98	98	105	USBHS1_HS_WKUP	USBHS1_HS WKUP interrupt through EXTI line 62	0x000001C8
99	99	106	USBHS1_HS	USBHS1_HS global interrupt	0x000001CC
100	100	107	USBHS2_HS_EPx_OUT	USBHS2_HS endpoint out global interrupt	0x000001D0
101	101	108	USBHS2_HS_EPx_IN	USBHS2_HS endpoint in global interrupt	0x000001D4
102	102	109	USBHS2_HS_WKUP	USBHS2_HS WKUP interrupt through EXTI line 63	0x000001D8
103	103	110	USBHS2_HS	USBHS2_HS global interrupt	0x000001DC
104	104	111	ETH1	Ethernet 1 global interrupt	0x000001E0
105	105	112	ETH1_PMT_LPI	Ethernet 1 PMT wakeup interrupt and LPI interrupt through EXTI line 83	0x000001E4
106	106	113	ETH2	Ethernet 2 global interrupt	0x000001E8
107	107	114	ETH2_PMT_LPI	Ethernet 2 PMT wakeup interrupt and LPI interrupt through EXTI line 84	0x000001EC
108	108	115	FDCAN1_INT0	FDCAN1 global interrupt line 0	0x000001F0
109	109	116	FDCAN2_INT0	FDCAN2 global interrupt line 0	0x000001F4
110	110	117	FDCAN3_INT0	FDCAN3 global interrupt line 0	0x000001F8
111	111	118	FDCAN4_INT0	FDCAN4 global interrupt line 0	0x000001FC
112	112	119	FDCAN1_INT1	FDCAN1 global interrupt line 1	0x00000200
113	113	120	FDCAN2_INT1	FDCAN2 global interrupt line 1	0x00000204
114	114	121	FDCAN3_INT1	FDCAN3 global interrupt line 1	0x00000208
115	115	122	FDCAN4_INT1	FDCAN4 global interrupt line 1	0x0000020C
116	116	123	USART1	USART1 global interrupt	0x00000210
117	117	124	USART2	USART2 global interrupt	0x00000214
118	118	125	USART3	USART3 global interrupt	0x00000218
119	119	126	USART4	USART4 global interrupt	0x0000021C
120	120	127	USART5	USART5 global interrupt	0x00000220
121	121	128	USART6	USART6 global interrupt	0x00000224
122	122	129	USART7	USART7 global interrupt	0x00000228

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123	123	130	USART8	USART8 global interrupt	0x0000022C
124	124	131	UART9	UART9 global interrupt	0x00000230
125	125	132	UART10	UART10 global interrupt	0x00000234
126	126	133	UART11	UART11 global interrupt	0x00000238
127	127	134	UART12	UART12 global interrupt	0x0000023C
128	128	135	UART13	UART13 global interrupt	0x00000240
129	129	136	UART14	UART14 global interrupt	0x00000244
130	130	137	UART15	UART15 global interrupt	0x00000248
131	131	138	LPUART1	LPUART1 global interrupt + wakeup through EXTI line 49	0x0000024C
132	132	139	LPUART2	LPUART2 global interrupt + wakeup through EXTI line 52	0x00000250
133	133	140	GPU	GPU global interrupt	0x00000254
134	134	141	-	Reserved	0x00000258
135	135	142	SDMMC1	SDMMC1_IRQ + WKUP through EXTI line 24	0x0000025C
136	136	143	SDMMC2	SDMMC2_IRQ + WKUP through EXTI line 25	0x00000260
137	137	144	ADC1	ADC1 global interrupt	0x00000264
138	138	145	ADC2	ADC2 global interrupt	0x00000268
139	139	146	ADC3	ADC3 global interrupt	0x0000026C
140	140	147	COMP12	COMP1 and COMP2 through EXTI line 20 and 21	0x00000270
141	141	148	COMP34	COMP3 and COMP4 through EXTI line 22 and 23	0x00000274
142	142	149	SHRTIM1_INT1	High Resolution timer 1 interrupt 1	0x00000278
143	143	150	SHRTIM1_INT2	High Resolution timer 1 interrupt 2	0x0000027C
144	144	151	SHRTIM1_INT3	High Resolution timer 1 interrupt 3	0x00000280
145	145	152	SHRTIM1_INT4	High Resolution timer 1 interrupt 4	0x00000284
146	146	153	SHRTIM1_INT5	High Resolution timer 1 interrupt 5	0x00000288
147	147	154	SHRTIM1_INT6	High Resolution timer 1 interrupt 6	0x0000028C
148	148	155	SHRTIM1_INT7	High Resolution timer 1 interrupt 7	0x00000290
149	149	156	SHRTIM1_INT8	High Resolution timer 1 interrupt 8	0x00000294
150	150	157	SHRTIM2_INT1	High Resolution timer 1 interrupt 1	0x00000298
151	151	158	SHRTIM2_INT2	High Resolution timer 1 interrupt 2	0x0000029C
152	152	159	SHRTIM2_INT3	High Resolution timer 1 interrupt 3	0x000002A0
153	153	160	SHRTIM2_INT4	High Resolution timer 1 interrupt 4	0x000002A4
154	154	161	SHRTIM2_INT5	High Resolution timer 1 interrupt 5	0x000002A8
155	155	162	SHRTIM2_INT6	High Resolution timer 1 interrupt 6	0x000002AC
156	156	163	SHRTIM2_INT7	High Resolution timer 1 interrupt 7	0x000002B0
157	157	164	SHRTIM2_INT8	High Resolution timer 1 interrupt 8	0x000002B4
158	158	165	FDCAN5_INT0	FDCAN5 global interrupt line 0	0x000002B8

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159	159	166	FDCAN6_INT0	FDCAN6 global interrupt line 0	0x000002BC
160	160	167	FDCAN7_INT0	FDCAN7 global interrupt line 0	0x000002C0
161	161	168	FDCAN8_INT0	FDCAN8 global interrupt line 0	0x000002C4
162	162	169	FDCAN5_INT1	FDCAN5 global interrupt line 1	0x000002C8
163	163	170	FDCAN6_INT1	FDCAN6 global interrupt line 1	0x000002CC
164	164	171	FDCAN7_INT1	FDCAN7 global interrupt line 1	0x000002D0
165	165	172	FDCAN8_INT1	FDCAN8 global interrupt line 1	0x000002D4
166	166	173	DSI	MIPI DSI Interrupt through EXTI line 87	0x000002D8
167	-		-	Reserved	
-	167	174	AHB_CACHE_PARMON	AHB i/dCACHE parity error interrupt	0x000002DC
168	168	175	LPTIM5_WKUP	LPTIM5 wakeup through EXTI 86	0x000002E0
169	169	176	JPEG SGDMA H2P	JPEG SGDMA Host to Peripheral Interrupt	0x000002E4
170	170	177	JPEG SGDMA P2H	JPEG SGDMA Peripheral to Host Interrupt	0x000002E8
171	171	178	WAKEUP_IO	6 WAKEUP IOs through EXTI line 70-75	0x000002EC
172	-	179	SEMA4_INT1	SEMA4 interrupt 1	0x000002F0
-	173	180	SEMA4_INT2	SEMA4 interrupt 2	0x000002F4
174	-	181	WWDG2_RST	WWDG2 reset interrupt through EXTI line 82	0x000002F8
-	174	181	WWDG1_RST	WWDG1 reset interrupt through EXTI line 81	
175	175	182	OTPC	OTPC IRQ	0x000002FC
176	176	183	FEMC	FEMC interrupt	0x00000300
177	-	184	DCMUB	DCMUB interrupt	0x00000304
-	177		DCMUA	DCMUA interrupt	
178	178	185	DAC1	DAC1 IRQ	0x00000308
179	179	186	DAC2	DAC2 IRQ	0x0000030C
180	180	187	MDMA AHBS ERROR	MDMA AHBS ERROR through EXTI line 55-56	0x00000310
181	181	188	CM7 Error on Cache Read	CM7 Error on Cache Read through EXTI line 64-65	0x00000314
182	182	189	DAC3	DAC3 interrupt	0x00000318
183	183	190	DAC4	DAC4 interrupt	0x0000031C
184	184	191	EMC	EMC event interrupt through EXTI line 88-89	0x00000320
185	185	192	DAC5	DAC5 interrupt	0x00000324
186	186	193	DAC6	DAC6 interrupt	0x00000328
187	187	194	ESC_OPB	ETHERCAT Slave Control OPB Interrupt	0x0000032C
188	188	195	ESC_SYNC0	ETHERCAT Slave Control SYNC0 Interrupt	0x00000330
189	189	196	ESC_SYNC1	ETHERCAT Slave Control SYNC1 Interrupt	0x00000334
190	190	197	ESC_WRP	ETHERCAT Slave Control WRAPPER Interrupt	0x00000338
191	191	198	-	Reserved	0x0000033C
192	192	199	ATIM1_BRK	Advanced timer 1 break interrupt	0x00000340

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193	193	200	ATIM1_TRG_COM	Advanced timer 1 trigger and commutation interrupts	0x00000344
194	194	201	ATIM1_CC	Advanced timer 1 capture/compare interrupt	0x00000348
195	195	202	ATIM1_UP	Advanced timer 1 update interrupt	0x0000034C
196	196	203	ATIM2_BRK	Advanced timer 2 break interrupt	0x00000350
197	197	204	ATIM2_TRG_COM	advanced timer 2 trigger and commutation interrupts	0x00000354
198	198	205	ATIM2_CC	Advanced timer 2 capture/compare interrupt	0x00000358
199	199	206	ATIM2_UP	Advanced timer 2 update interrupt	0x0000035C
200	200	207	ATIM3_BRK	Advanced timer 3 break interrupt	0x00000360
201	201	208	ATIM3_TRG_COM	Advanced timer 3 trigger and commutation interrupts	0x00000364
202	202	209	ATIM3_CC	Advanced timer 3 capture/compare interrupt	0x00000368
203	203	210	ATIM3_UP	Advanced timer 3 update interrupt	0x0000036C
204	204	211	ATIM4_BRK	Advanced timer 4 break interrupt	0x00000370
205	205	212	ATIM4_TRG_COM	Advanced timer 4 trigger and commutation interrupts	0x00000374
206	206	213	ATIM4_CC	Advanced timer 4 capture/compare interrupt	0x00000378
207	207	214	ATIM4_UP	Advanced timer 4 update interrupt	0x0000037C
208	208	215	GTIMA1	General timer A1 global interrupt	0x00000380
209	209	216	GTIMA2	General timer A2 global interrupt	0x00000384
210	210	217	GIIMA3	General timer A3 global interrupt	0x00000388
211	211	218	GTIMA4	General timer A4 global interrupt	0x0000038C
212	212	219	GTIMA5	General timer A5 global interrupt	0x00000390
213	213	220	GTIMA6	General timer 6 global interrupt	0x00000394
214	214	221	GTIMA7	General timer A7 global interrupt	0x00000398
215	215	222	GTIMB1	General timer B1 global interrupt	0x0000039C
216	216	223	GTIMB2	General timer B2 global interrupt	0x000003A0
217	217	224	GTIMB3	General timer B3 global interrupt	0x000003A4
218	218	225	BTIM1	Base timer 1 global interrupt	0x000003A8
219	219	226	BTIM2	Base timer 2 global interrupt	0x000003AC
220	220	227	BTIM3	Base timer 3 global interrupt	0x000003B0
221	221	228	BTIM4	Base timer 4 global interrupt	0x000003B4
222	222	229	LPTIM1_WKUP	LPTIM1 wakeup through EXTI 66	0x000003B8
223	223	230	LPTIM2_WKUP	LPTIM2 wakeup through EXTI 67	0x000003BC
224	224	231	LPTIM3_WKUP	LPTIM3 wakeup through EXTI 68	0x000003C0
225	225	232	LPTIM4_WKUP	LPTIM4 wakeup through EXTI 69	0x000003C4
226	226	233	DSMU_FLT0	DSMU Filter Interrupt 0	0x000003C8
227	227	234	DSMU_FLT1	DSMU Filter Interrupt 1	0x000003CC

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228	228	235	DSMU_FLT2	DSMU Filter Interrupt 2	0x000003D0
229	229	236	DSMU_FLT3	DSMU Filter Interrupt 3	0x000003D4
230	230	237	FMAC	FMAC global interrupt	0x000003D8
231	231	238	CORDIC	Cordic global interrupt	0x000003DC
232	232	239	DMAMUX1	DMAMUX1 interrupt	0x000003E0
233	233	240	MMU	MMU interrupt	0x000003E4

13.2 Extended Interrupt/Event Controller (EXTI)

13.2.1 Introduction

The Extended Interrupt and Event Controller (EXTI) handles wake-up functionality through configurable and direct event inputs from on-chip peripherals and external inputs. It sends wake-up events to PWR, transfers interrupt and events signals to the two CPU.

The EXTI wakeup events can be used to wake up the system from STOP0 and STOP2 mode. They can also wake up CPUs from SLEEP, STOP0 and STOP2 modes. They can also be used to generate interrupts and events in run modes.

13.2.2 EXTI main features

EXTI Main features are as follows:

- Wake up system from STOP0/STOP2 mode
- Generate interrupts and events to CPUs

These requests can be generated from the following event inputs:

- Direct event (from on-chip peripherals, where event flags are present and cleared at the source peripherals, not in EXTI) with the following functions:
  - Only rising edge trigger is allowed
  - Masking capability
- Configurable events (from external devices or on-chip peripherals that only generate pulse events) with the following functions:
  - Software trigger
  - Both rising and falling edge triggers are allowed and programmable
  - Masking capability

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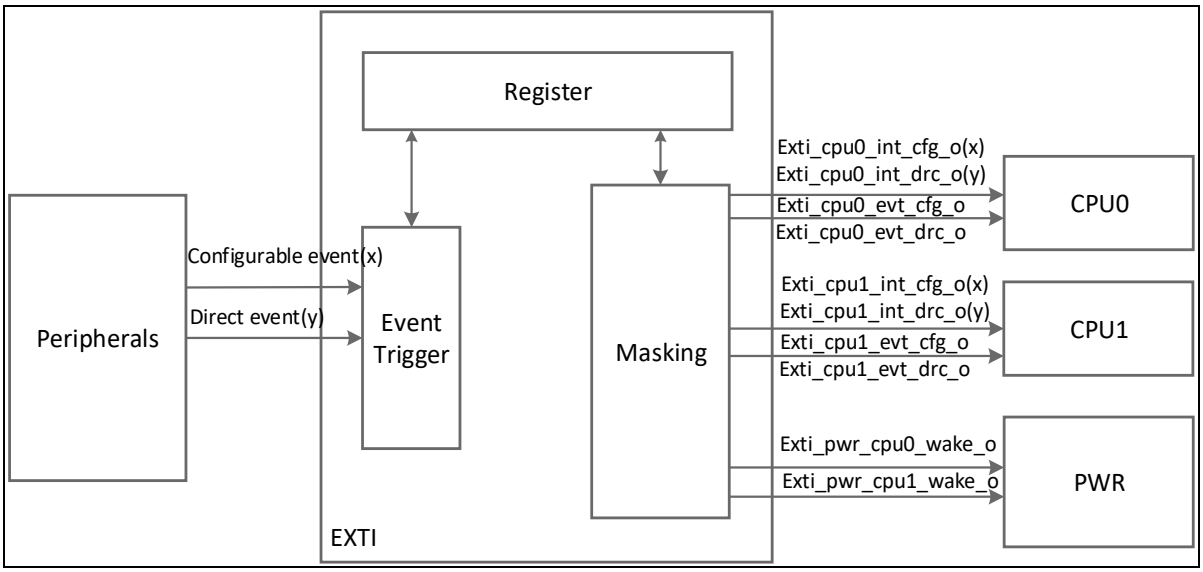
13.2.3 EXTI block diagram

Figure 13-1 EXTI Block Diagram



As shown in Figure 13-1, on-chip/off-chip peripherals send the events to EXTI and trigger the following:

- Interrupts and events to CPUx NVIC and rxev inputs respectively for wakeup in CSLEEP mode
- Wakeup events to PWR for system or CPU wakeup in system STOP0/STOP2 or CSTOP0/CSTOP2

13.2.4 EXTI functional description

Table 13-2 shows the available registers that are used for configurable and direct event inputs. Only Masking registers are available for direct events, whereas all 5 registers are available for configurable events as their triggers can be programmable as rising/falling and software triggered.

Table 13-2 EXTI Event input configurations and register control

Event Input type	EXTI_RT_CFG	EXTI_FT_CFG	EXTI_SWIE	EXTI_M4IMASK EXTI_M7IMASK	EXTI_M4EMASK EXTI_M7EMASK
Configurable	X	X	X	X	X
Direct	-	-	-	X	X

13.2.4.1 EXTI configurable event input

Figure 13-2 shows the configurable event triggering logic.

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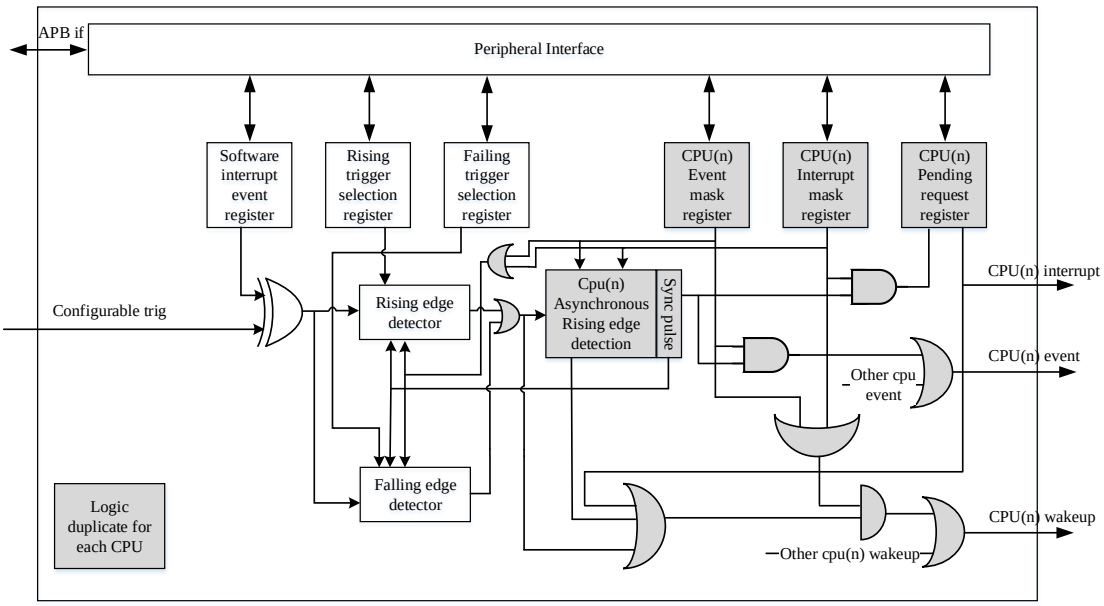
Figure 13-2 Configurable event triggering logic



Rising/Falling Edge Selection Register (EXTI_RT_CFGx/EXTI_FT_CFGx)

These registers are used to configure the edge for triggering. It can be rising edge, falling edge or both edges.

Software Interrupt Event Register (EXTI_SWIEx)

There registers are to generate events by software.

Interrupt/Event Mask Registers (EXTI_CM4/CM7IMASKx or EXTI_CM4/CM7EMASKx)

These two registers are dedicatedly allocated for each CPU (CPU0/1). They are used to mask the interrupts and events from inputs to respective CPUs.

CPU Pending Register (EXTI_CM4/CM7PENDx)

Detected un-masked interrupts will set respective CPU pending registers. These will be used as interrupt events to respective NVIC. Un-masked events will not be able to set CPU pending registers.

13.2.4.2 EXTI direct event input

Figure 13-3 shows the direct event triggering logic.

Only interrupt/event mask registers are available for direct interrupt/event masking. For trigger detection, it is always fixed as rising edge.

There is no pending registers for direct events as it is expected that the pending flag is present and cleared at the source peripheral. In addition, there is no software trigger available for direct event.

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Figure 13-3 Direct event triggering logic

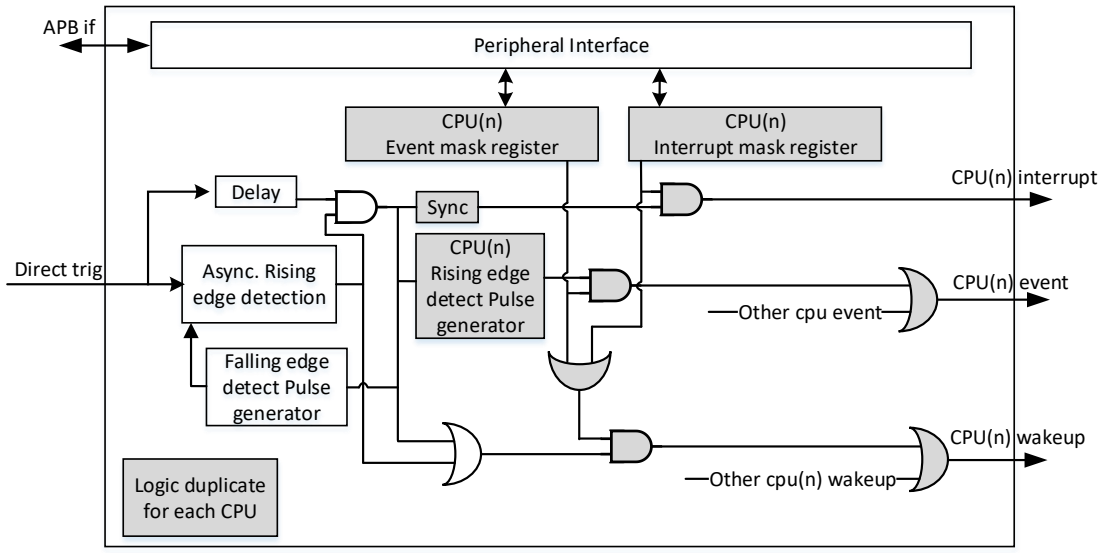

Table 13-3 shows the line number of configurable and direct events for software configuration.

Table 13-3 EXTI mapping for configurable and direct events

RT_CFGx FT_CFGx SWIEx M7IMASKx M4IMASKx M7EMASKx M4EMASKx	Configurable Events	EXTI Line	M7IMASKx_DRC M4IMASKx_DRC M7EMASKx_DRC M4EMASKx_DRC	Direct Events	EXTI Line
0	EXTI0	EXTI Line0	0	SDMMC1_wkup	EXTI Line24
1	EXTI1	EXTI Line1	1	SDMMC2_wkup	EXTI Line25
2	EXTI2	EXTI Line2	2	ETH1_wkup	EXTI Line83
3	EXTI3	EXTI Line3	3	ETH2_wkup	EXTI Line84
4	EXTI4	EXTI Line4	4	Reserved	Reserved
1	EXTI5	EXTI Line5	1	Reserved	Reserved
6	EXTI6	EXTI Line6	6	Reserved	Reserved
7	EXTI7	EXTI Line7	7	Reserved	Reserved
8	EXTI8	EXTI Line8	8	Reserved	Reserved
9	EXTI9	EXTI Line9	9	Reserved	Reserved
10	EXTI10	EXTI Line10	10	Reserved	Reserved
11	EXTI11	EXTI Line11	11	Reserved	Reserved
12	EXTI12	EXTI Line12	12	Reserved	Reserved
13	EXTI13	EXTI Line13	13	Reserved	Reserved
14	EXTI14	EXTI Line14	14	Reserved	Reserved
15	EXTI15	EXTI Line15	15	Reserved	Reserved

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RT_CFGx FT_CFGx SWIEx M7IMASKx M4IMASKx M7EMASKx M4EMASKx	Configurable Events	EXTI Line	M7IMASKx_DRC M4IMASKx_DRC M7EMASKx_DRC M4EMASKx_DRC	Direct Events	EXTI Line
16	PVD and AVD	EXTI Line16	16	Reserved	Reserved
17	RTC alarms	EXTI Line17	17	Reserved	Reserved
18	RTC tamper	EXTI Line18	18	Reserved	Reserved
19	RTC wakeup	EXTI Line19	19	Reserved	Reserved
20	COMP1	EXTI Line20	20	Reserved	Reserved
21	COMP2	EXTI Line21	21	Reserved	Reserved
22	COMP3	EXTI Line22	22	Reserved	Reserved
23	COMP4	EXTI Line23	23	Reserved	Reserved
24	WWDG1 reset	EXTI Line81	24	Reserved	Reserved
25	WWDG2 reset	EXTI Line82	25	Reserved	Reserved
26	Reserved	Reserved	26	Reserved	Reserved
27	Reserved	Reserved	27	DCMUA Interrupt	EXTI Line51
28	DSI video error	EXTI Line87	28	Reserved	Reserved
29	Reserved	Reserved	29	Reserved	Reserved
30	Reserved	Reserved	30	DCMUB Interrupt	EXTI Line54
31	WKUP1	EXTI Line70	31	Reserved	Reserved
32	WKUP2	EXTI Line71	32	Reserved	Reserved
33	WKUP3	EXTI Line72	33	Reserved	Reserved
34	WKUP4	EXTI Line73	34	Reserved	Reserved
35	WKUP5	EXTI Line74	35	Reserved	Reserved
36	WKUP6	EXTI Line75	36	Reserved	Reserved
37	LPTIM1 wakeup	EXTI Line66	37	Reserved	Reserved
38	LPTIM2 wakeup	EXTI Line67	38	CM7_AHBSRDY_ERROR	EXTI Line56
39	LPTIM3 wakeup	EXTI Line68	39	CM7 AHBS_ABORT	EXTI Line55
40	LPTIM4 wakeup	EXTI Line69	40	Reserved	Reserved
41	LPTIM5 wakeup	EXTI Line86	41	Reserved	Reserved
42	LPUART1 wakeup	EXTI Line49	42	Reserved	Reserved
43	LPUART2 wakeup	EXTI Line52	43	Reserved	Reserved
44	CM7 Correctable Error on Cache Read Event	EXTI Line64	44	Reserved	Reserved
45	CM7 Fatal Error on Cache Read Event	EXTI Line65	45	Reserved	Reserved

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RT_CFGx FT_CFGx SWIEx M7IMASKx M4IMASKx M7EMASKx M4EMASKx	Configurable Events	EXTI Line	M7IMASKx_DRC M4IMASKx_DRC M7EMASKx_DRC M4EMASKx_DRC	Direct Events	EXTI Line
46	Reserved	Reserved	46	Reserved	Reserved
47	Reserved	Reserved	47	Reserved	Reserved
48	USB1 Wakeup	EXTI Line62	48	Reserved	Reserved
49	USB2 Wakeup	EXTI Line63	49	Reserved	Reserved
50	VDDD EMC event	EXTI Line89	50	Reserved	Reserved
51	BKP EMC event	EXTI Line88	51	Reserved	Reserved
52	Reserved	Reserved	52	RCC interrupt	EXTI Line76
53	Reserved	Reserved	53	SEMA1 interrupt	EXTI Line77
54	Reserved	Reserved	54	SEMA2 interrupt	EXTI Line78
55	Reserved	Reserved	55	CortexM4 SEV interrupt	EXTI Line79
56	Reserved	Reserved	56	CortexM7 SEV interrupt	EXTI Line80
57	Reserved	Reserved	57	HSECSS interrupt	EXTI Line85
58	Reserved	Reserved	58	Reserved	

13.2.5 EXTI event input mapping

Table 13-4 shows the EXTI event input mapping and their respective capabilities. An Event input can either wake up CPU1, CPU2, and in the case of “Any” can wake up any CPU.

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Table 13-4 EXTI Event Input Mapping

EXTI Event Line	Source	Type	Wakeup targets(1)	Connection to NVIC
0-15	EXTI[15:0]	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
16	PVD and AVD	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
17	RTC alarms	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
18	RTC tamper, RTC timestamp, LSECSS, RTC calendar overflow, LSICSS	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
19	RTC wakeup timer	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
20	COMP1	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
21	COMP2	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
22	COMP3	Configurable	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
23	COMP4	Configurable	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
24	SDMMC1 wakeup event	Direct	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
25	SDMMC2 wakeup event	Direct	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
26-48	Reserved	-	-	-
49	LPUART1 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes

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EXTI Event Line	Source	Type	Wakeup targets(1)	Connection to NVIC
50	Reserved	-	-	-
51	DCMUA Interrupt	Direct	CM7 (CPU Cn_STP0 /Cn_STP2)	No(2)
52	LPUART2 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
53	Reserved	-	-	-
54	DCMUB Interrupt	Direct	CM4 (CPU Cn_STP0 /Cn_STP2)	No(2)
55	CM7 AHBS_ABORT	Direct	Any (CM7/CM4 Cn_SLP OR CM4 Cn_STP0 /Cn_STP2)	Yes
56	CM7_AHBSRDY_ERROR	Direct	Any (CPU Cn_SLP/Cn_STP0 /Cn_STP2)	Yes
57	Reserved	-	-	-
58	Reserved	-	-	-
59	Reserved	-	-	-
60	Reserved	-	-	-
61	Reserved	-	-	-
62	USB1_HS wakeup	Configurable	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
63	USB2_HS wakeup	Configurable	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
64	CM7 Correctable Error on Cache Read	Configurable	CM4 (Cn_SLP/Cn_STP0 /Cn_STP2)	Yes
65	CM7 Fatal Error on Cache Read	Configurable	CM4 (Cn_SLP/Cn_STP0 /Cn_STP2))	Yes
66	LPTIM1 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
67	LPTIM2 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
68	LPTIM3 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU	Yes

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EXTI Event Line	Source	Type	Wakeup targets(1)	Connection to NVIC
			Cn_SLP/Cn_STP0/Cn_STP2)	
69	LPTIM4 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
70	WKUP1	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
71	WKUP2	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
72	WKUP3	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
73	WKUP4	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
74	WKUP5	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
75	WKUP6	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
76	RCC interrupt	Direct	Any (CPU Cn_SLP/ Cn_STP0/Cn_STP2)	No(2)
77	SEMA1 interrupt	Direct	CM7 (Cn_SLP/Cn_STP0/Cn_STP2)	No(2)
78	SEMA2 interrupt	Direct	CM4 (Cn_SLP/Cn_STP0/Cn_STP2)	No(2)
79	CortexM4 SEV interrupt	Direct	CM7 (Cn_SLP)	No(3)
80	CortexM7 SEV interrupt	Direct	CM4 (Cn_SLP)	No(3)
81	WWDG1 reset	Configurable	CM4 (Cn_SLP/Cn_STP0/Cn_STP2)	Yes
82	WWDG2 reset	Configurable	CM7 (Cn_SLP/Cn_STP0/Cn_STP2)	Yes
83	ETHERNET1 wakeup (LPI+PMT)	Direct	Any (SYSTEM STOP0 OR CPU	Yes

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EXTI Event Line	Source	Type	Wakeup targets(1)	Connection to NVIC
			Cn_SLP/Cn_STP0/Cn_STP2)	
84	ETHERNET2 wakeup (LPI+PMT)	Direct	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
85	HSECSS interrupt	Direct	Any (CPU Cn_SLP/ Cn_STP0/Cn_STP2)	No(2)
86	LPTIMER5 wakeup	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
87	DSI Error Event (Video Error + Overflow + Underflow)	Configurable	Any (SYSTEM STOP0 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
88	BKP EMC	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
89	VDDD EMC	Configurable	Any (SYSTEM STOP0/2 OR CPU Cn_SLP/Cn_STP0/Cn_STP2)	Yes
90	Reserved	-	-	-

(1) This is for wakeup in low power modes. For interrupts, as long as connection to NVIC is available, it can interrupt any CPU in run mode.

(2) Available on CPU NVIC directly from peripheral, used for system power/clk wakeup via PWR so that CPU power/clock is available to sample interrupt for wakeup. This is useful for CPU low power wakeup where the system is at higher power mode (.e.g. system at run mode, CM4 at STOP0 or CM7 STwP2)

(3) Not available on CPU NVIC, to be used for system wakeup via PWR or CPU event input (rxev)

13.2.6 EXTI programming guide

13.2.6.1 Common guide

Configurable Events

The Configurable events need to be activated by programming the selected edge in the respective EXTI_RT_CFGx/EXTI_FT_CFGx registers. The respective interrupt/event and pending PRx bit in the EXTI_M4/M7PENDx are set when an enabled and unmasked events are detected. The pending PRx bit shall be checked and cleared by software. This will also clear the respective interrupt to CPU. There is no CPU Event pending bit.

The interrupts/events can be also created by software by writing 1 into the EXTI_SWIEx.

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Direct Events

The Direct event inputs are required to be activated in the source peripherals.

A direct even trigger is detected on the rising edge only. There are no respective interrupt pending bit and software trigger for the direct events. Software is required to unmask the detected triggers so that interrupts/events can be generated to CPUs.

13.2.6.2 EXTI interrupt programming guide

- Program the selected edge in the EXTI_RT_CFGx/FT_CFGx registers to activate the event inputs if they are configurable events.
- Unmask the event interrupt by write 1 into the respective mask bits in the EXTI_CM4/CM7IMASKx register.
- Program the respective NVICs to enable the corresponding interrupt line or use the SEVONPEND so that CPU can detect the interrupt after a WFI/WFE instruction. Note that the respective EXTI pending bit is required to be cleared by software if the event is configurable.

13.2.6.3 EXTI event programming guide

- Program the selected edge in the EXTI_RT_CFGx/FT_CFGx registers to activate the event inputs if they are configurable events.
- Unmask the event inputs by write 1 into the respective mask bits in the EXTI_CM4/CM7EMASKx register.
- CPU can detect event inputs after a WFE instruction. No NVIC programming needed. There is no EXTI pending bit to clear for events.

13.2.6.4 EXTI CPU wakeup procedure

- Program the selected edge in the EXTI_RT_CFGx/FT_CFGx registers to activate the event inputs if they are configurable events.
- Program the EXTI_CM4/CM7IMASKx or EXTI_CM4/CM7EMASKx to unmask the event inputs so that the wakeup events can be generated.

13.2.6.5 EXTI software interrupt/event trigger programming guide

- Program the selected edge in the EXTI_RT_CFGx/FT_CFGx registers to activate the event inputs if they are configurable events.
- Program the EXTI_CM4/CM7IMASKx or EXTI_CM4/CM7EMASKx to unmask the event inputs so that the wakeup events can be generated.
- Program “1” to the respective interrupt enable bit in the EXTI_SWIEx register to generate software trigger interrupt/events.

13.3 EXTI Registers

Every register can only be accessed with 32-bit (word). x is the line number for each event input as shown in Table 13-3 EXTI mapping for configurable and direct events

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13.3.1.1 Rising Edge Trigger Selection Register (EXTI_RT_CFG0)

Address offset: 0x00

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RT_CFG[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT_CFG[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	RTx	RTx: Rising trigger event configuration bit of Configurable Event input x(x=0…31). 0: Rising trigger disabled (for Event and Interrupt) for input line 1: Rising trigger enabled (for Event and Interrupt) for input line

13.3.1.2 Rising Edge Trigger Selection Register (EXTI_RT_CFG1)

Address offset: 0x04

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												RT_CFG[19:16]			
												rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT_CFG[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	RT_CFGx[19:0]	RTx: Rising trigger event configuration bit of Configurable Event input x+32 x(x=0…19). 0: Rising trigger disabled (for Event and Interrupt) for input line 1: Rising trigger enabled (for Event and Interrupt) for input line

13.3.1.3 Falling Edge Trigger Selection Register (EXTI_FT_CFG0)

Address offset: 0x20

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FT_CFG[31:16]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT_CFG[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	FT_CFGx	FTx: Falling trigger event configuration bit of Configurable Event input x(x=0…31). 0: Falling trigger disabled (for Event and Interrupt) for input line 1: Falling trigger enabled (for Event and Interrupt) for input line

13.3.1.4 Falling Edge Trigger Selection Register (EXTI_FT_CFG1)

Address offset: 0x24

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												FT_CFG[19:16]			
												rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT_CFG[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	FT_CFGx	FTx: Falling trigger event configuration bit of Configurable Event input x+32 x(x=0…19). 0: Falling trigger disabled (for Event and Interrupt) for input line 1: Falling trigger enabled (for Event and Interrupt) for input line

13.3.1.5 Software Interrupt Enable Register (EXTI_SWIE0)

Address offset: 0x40

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SWIE0x[31:16]															
t															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWIE0x[15:0]															
t															

Bit field	Name	Description

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31:0	SWIE0x[31:0]	SWIE0x: Software interrupt on line x 0: Writing 0 has no effect. 1: Writing a 1 to this bit will trigger an event on line x. This bit is auto cleared by hardware.

13.3.1.6 5Software Interrupt Enable Register (EXTI_SWIE1)

Address offset: 0x44

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												SWIE1x[19:16]			
												t			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWIE1x[15:0]															
t															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	SWIE1x[19:0]	SWIE1x: Software interrupt on line x+32. 0: Writing 0 has no effect. 1: Writing a 1 to this bit will trigger an event on line x. This bit is auto cleared by hardware.

13.3.1.7 EXTI to CPU1 interrupt mask register (EXTI_M7IMASK0)

Address offset: 0x60

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7IMSK0x[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7IMSK0x[15:0]															
rw															

Bit field	Name	Description
31:0	M7IMSK0x	Interrupt mask on line x 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

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13.3.1.8 EXTI to CPU1 interrupt mask register (EXTI_M7IMASK1)

Address offset: 0x64

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M7IMSK1x[19:16]			
												rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7IMSK1x[15:0]															
rw															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	M7IMSK1x[19:0]	Interrupt mask on line x+32. 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

13.3.1.9 EXTI to CPU2 interrupt mask register (EXTI_M4IMASK0)

Address offset: 0x80

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M4IMSK0x[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4IMSK0x[15:0]															
rw															

Bit field	Name	Description
31:0	M4IMSK0x[31:0]	Interrupt mask on line x 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

13.3.1.10 EXTI to CPU2 interrupt mask register (EXTI_M4IMASK1)

Address offset: 0x84

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M4IMSK1x[19:16]			
												rw			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4IMSK1x[15:0]															
rw															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	M4IMSK1x[19:0]	Interrupt mask on line x+32. 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

13.3.1.11 EXTI to CPU1 event mask register (EXTI_M7EMASK0)

Address offset: 0xA0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7EMASK0x[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7EMASK0x[15:0]															
rw															

Bit field	Name	Description
31:0	M7EMASK0x[31:0]	Event mask on line x 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.12 EXTI to CPU1 event mask register (EXTI_M7EMASK1)

Address offset: 0xA4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M7EMASK1x[19:16]			
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7EMASK1x[15:0]															
rw															

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Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	M7EMASK1x[19:0]	Event mask on line x+32. 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.13 EXTI to CPU2 event mask register (EXTI_M4EMASK0)

Address offset: 0xC0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M4EMASK0x[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4EMASK0x[15:0]															
rw															

Bit field	Name	Description
31:0	M4EMASK0x[31:0]	Event mask on line x 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.14 EXTI to CPU2 event mask register (EXTI_M4EMASK1)

Address offset: 0xC4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M4EMASK1x[19:16]			
													rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4EMASK1x[15:0]															
rw															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	M4EMASK1x[19:0]	Event mask on line x+32. 0: Event request from Line x is masked 1: Event request from Line x is unmasked

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13.3.1.15 EXTI CPU1 Pending Register (EXTI_M7PEND0)

Address offset: 0xE0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7PEND0x[31:16]															
rc_w1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7PEND0x[15:0]															
rc_w1															

Bit field	Name	Description
31:0	M7PEND0x[31:0]	Pending bit for line x 0: No trigger request occurred 1: selected trigger request occurred This bit is set when the selected edge event arrives on the external interrupt l

13.3.1.16 EXTI CPU1 Pending Register (EXTI_M7PEND1)

Address offset: 0xE4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M7PEND1x[19:16]			
												rc_w1			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7PEND1x[15:0]															
rc_w1															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	M7PEND1x[19:0]	Pending bit for line x+32. 0: No trigger request occurred 1: selected trigger request occurred This bit is set when the selected edge event arrives on the external interrupt l

13.3.1.17 EXTI CPU2 Pending Register (EXTI_M4PEND0)

Address offset: 0x100

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M4PEND0x[31:16]															
rc_w1															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4PEND0x[15:0]															
rc_w1															

Bit field	Name	Description
31:0	M4PEND0x[31:0]	CPU1 Pending bit for line x 0: No trigger request occurred 1: selected trigger request occurred This bit is set when the selected edge event arrives on the external interrupt l

13.3.1.18 EXTI CPU2 Pending Register (EXTI_M4PEND1)

Address offset: 0x104

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M4PEND1x[19:16]			
												rc_w1			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4PEND1x[15:0]															
rc_w1															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:0	M4PEND1x[19:0]	CPU1 Pending bit for line x+32. 0: No trigger request occurred 1: selected trigger request occurred This bit is set when the selected edge event arrives on the external interrupt l

13.3.1.19 EXTI to CPU1 interrupt mask register (EXTI_M7IMASK0_DRC)

Address offset: 0x120

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7IMASK0_DRCx[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7IMASK0_DRCx[15:0]															
rw															

Bit field	Name	Description

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31:0	M7IMASK0_DRCx[31:0]	Interrupt mask on line x 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

13.3.1.20 EXTI to CPU1 interrupt mask register (EXTI_M7IMASK1_DRC)

Address offset: 0x124

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					M7IMASK1_DRC[26:16]										
					rw										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7IMASK1_DRC[15:0]															
rw															

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:0	M7IMASK1_DRCx[26:0]	Interrupt mask on line x+32. 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

13.3.1.21 EXTI to CPU2 interrupt mask register (EXTI_M4IMASK0_DRC)

Address offset: 0x140

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M4IMASK0_DRC[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4IMASK0_DRC[15:0]															
rw															

Bit field	Name	Description
31:0	M4IMASK0_DRCx[31:0]	Interrupt mask on line x 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

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13.3.1.22 EXTI to CPU2 interrupt mask register (EXTI_M4IMASK1_DRC)

Address offset: 0x144

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					M4IMASK1_DRCx[26:16]										
					rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4IMASK1_DRCx[15:0]															
rw															

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:0	M4IMASK1_DRCx[26:0]	Interrupt mask on line x+32. 0: Interrupt request from Line x is masked 1: Interrupt request from Line x is unmasked

13.3.1.23 EXTI to CPU1 event mask register (EXTI_M7EMASK0_DRC)

Address offset: 0x160

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M7EMASK0_DRCx[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7EMASK0_DRCx[15:0]															
rw															

Bit field	Name	Description
31:0	M7EMASK0_DRCx[31:0]	Event mask on line x 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.24 EXTI to CPU1 event mask register (EXTI_M7EMASK1_DRC)

Address offset: 0x164

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					M7EMASK1_DRCx[26:16]										
					rw										

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M7EMASK1_DRCx[15:0]															
rw															

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:0	M7EMASK1_DRCx[26:0]	Event mask on line x+32. 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.25 EXTI to CPU2 event mask register (EXTI_M4EMASK0_DRC)

Address offset: 0x180

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M4EMASK0_DRCx[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4EMASK0_DRCx[15:0]															
rw															

Bit field	Name	Description
31:0	M4EMASK0_DRCx[31:0]	Event mask on line x 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.26 EXTI to CPU2 event mask register (EXTI_M4EMASK1_DRC)

Address offset: 0x184

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					M4EMASK1_DRCx[26:16]										
					rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M4EMASK1_DRCx[15:0]															
rw															

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.

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26:0	M4EMASK1_DRCx[26:0]	Event mask on line x+32. 0: Event request from Line x is masked 1: Event request from Line x is unmasked

13.3.1.27 EXTI Timestamp select register (EXTI_TSSEL)

Address offset: 0x1C0

Reset value: 0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TSSEL[3:0]				Reserved							
				rw											

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:8	TSSEL[3:0]	Select the external interrupt input as the trigger source for the timestamp event 0000: Select EXTI0 as the trigger source of the timestamp event; 0001: Select EXTI1 as the trigger source of the timestamp event. ... 1111: Select EXTI15 as the trigger source for the timestamp event.
7:0	Reserved[7:0]	Reserved, the reset value must be maintained.

14 DMA request multiplexer (DMAMUX)

14.1 Introduction

A peripheral initiates a DMA transfer request by activating its DMA request signal. This request remains pending until the DMA controller processes it by issuing a DMA acknowledge signal, which then deactivates the original DMA request signal.

The DMAMUX allows DMA request lines to be routed between the device's peripherals and its DMA controllers. This routing is managed by a programmable, multi-channel DMA request line multiplexer. Each channel can select a distinct DMA request line either unconditionally or in response to events from its DMAMUX synchronization inputs. Additionally, the DMAMUX can generate DMA requests based on programmable events triggered by its input signals.

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14.2 Main features

The DMAMUX includes the following features:

- Each DMA request generator channel:
  - DMA request trigger input selector
  - DMA request counter
  - Event overrun flag for selected DMA request trigger input
- Each DMA request line multiplexer channel output:
  - Up to 210 input DMA request lines from peripherals
  - Up to 3 DMA request line output
  - Synchronization input selector
  - DMA request counter
  - Event overrun flag for selected synchronization input
  - One event output, for DMA request chaining
- AHB slave interface, no burst supported, 32-bit access only
- DMAMUX overrun interrupt

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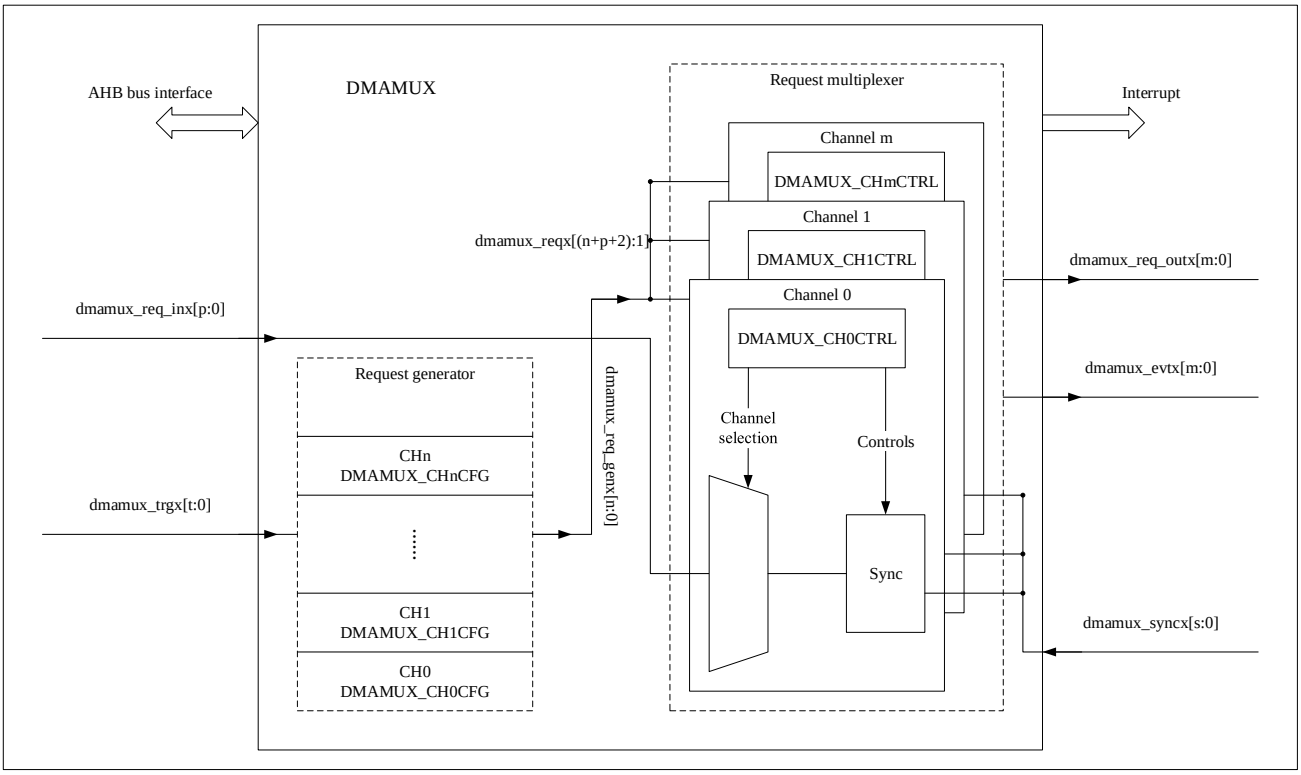
14.3 Block Diagram

Figure 14-1 DMAMUX Diagram



DMAMUX includes two main sub-blocks: the request line multiplexer and the request line generator.

The implementation assigns:

- Inputs to the DMAMUX request multiplexer sub-block (dmamux_reqx) originate from peripherals (dmamux_req_inx) and from the channels of the DMAMUX request generator sub-block (dmamux_req_genx)
- The DMAMUX sends request outputs (dmamux_req_outx) to the DMA controllers' channels
- Internal or external signals to DMA request trigger inputs (dmamux_trgx)
- Internal and external signals are supplied to the synchronization inputs (dmamux_syncx)

14.4 Function Description

This chip integrates two instances of DMAMUX, the hardware configuration features of DMAMUX1 and DMAMUX2 are shown in the table below.

Table 14-1 DMAMUX Inputs and Outputs

Features	DMAMUX1	DMAMUX2
Number of sync. Inputs	9	1 (internal used or unused)
Number of peripheral requests	210	4
Number of request trigger inputs	26	38

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Features	DMAMUX1	DMAMUX2
Number of request generator channels	8	16
Number of output request channels	24	16

14.4.1 DMAMUX channels

A DMAMUX channel refers to a DMAMUX request multiplexer channel that can incorporate an additional DMAMUX request generator channel based on the input selected by the request multiplexer.

Each DMAMUX request multiplexer channel is linked and exclusively assigned to a single DMA controller channel.

14.4.1.1 Channel configuration procedure

To configure both a DMAMUX x channel and the corresponding DMA y channel, follow these steps:

1. Fully set up and configure DMA channel y, ensuring all settings are complete except for enabling the channel.
2. Fully set up and configure the related DMAMUX y channel.
3. Enable DMA channel y by setting the EN bit in the DMA y channel register.

14.4.2 DMAMUX request line multiplexer

The DMAMUX request multiplexer, equipped with multiple channels, manages the routing of DMA request and acknowledge control signals, referred to as DMA request lines.

Each DMA request line is simultaneously connected to all channels of the DMAMUX request line multiplexer.

DMA requests originate either from the peripherals or from the DMAMUX request generator.

Specifically, each DMAMUX request line multiplexer channel x selects the corresponding DMA request line number as defined by the DMAMUX_CHxCTRL.REQID [7:0] register.

Note: The null value in the field REQID means no DMA request line selected.

A non-zero REQID may be assigned to multiple channels only if the application ensures that these channels are not activated simultaneously. In other words, if two different channels receive the same asserted hardware request at the same time, it can lead to unpredictable behavior in the DMA hardware.

Additionally, beyond selecting DMA requests, synchronization modes and/or event generation can be configured and enabled as needed.

14.4.2.1 Synchronization mode and channel event generation

Each DMAMUX request line multiplexer channel x can be individually synchronized by enabling the DMAMUX_CHxCTRL.SYEN bit.

DMAMUX features multiple synchronization inputs, which are connected in parallel to all the request multiplexer channels.

The synchronization input for a specific channel x is selected using the DMAMUX_CHxCTRL.SYID [2:0] register.

When a channel operates in synchronization mode, the selected input DMA request line is forwarded to the multiplexer channel output upon detecting a programmable rising or falling edge on the chosen synchronization

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signal, as configured by DMAMUX_CHxCTRL.SYPOL [1:0].

Additionally, there is a programmable DMA request counter within the DMAMUX request multiplexer. This counter can be utilized for generating channel request outputs and potentially for event generation. Event generation for channel x is enabled by setting the DMAMUX_CHxCTRL.EVEGEN bit.

When a synchronization edge is detected, the pending selected input DMA request line is connected to the DMAMUX multiplexer channel x output.

Note: If a synchronization event occurs without a pending selected input DMA request line, it is ignored. Subsequent asserted input request lines will not be connected to the DMAMUX multiplexer channel output until another synchronization event takes place.

From this point forward, each time the connected DMAMUX request is handled by the DMA controller (i.e., the request is deasserted), the DMAMUX request counter is decremented.

Upon underflow, the DMA request counter is automatically reloaded with the value from the DMAMUX_CHxCTRL.NUMREQ [4:0] field, and the input DMA request line is disconnected from the multiplexer channel x output.

Therefore, the number of DMA requests sent to the multiplexer channel x output following a detected synchronization event is equal to the value specified in the DMAMUX_CHxCTRL.NUMREQ [4:0] field plus one.

Note: The DMAMUX_CHxCTRL.NUMREQ [4:0] field value should only be modified by software when both the synchronization enable bit and the event generation enable (EVEGEN) bit of the corresponding multiplexer channel x are disabled.

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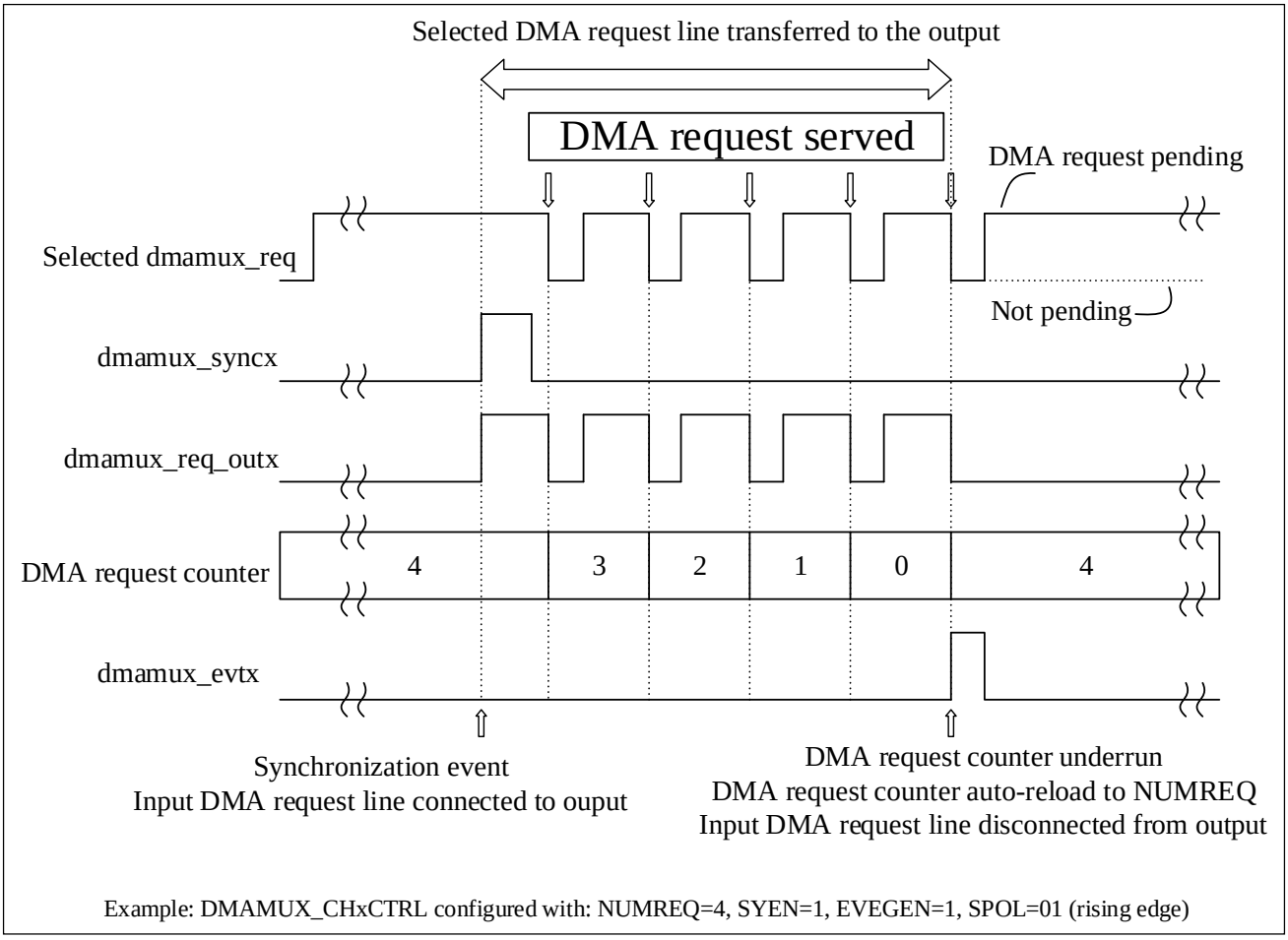
Figure 14-2 DMAMUX Sync Event Generation Example 1



Example: DMAMUX_CHxCTRL configured with: NUMREQ=4, SYEN=1, EVEGEN=1, SPOL=01 (rising edge)

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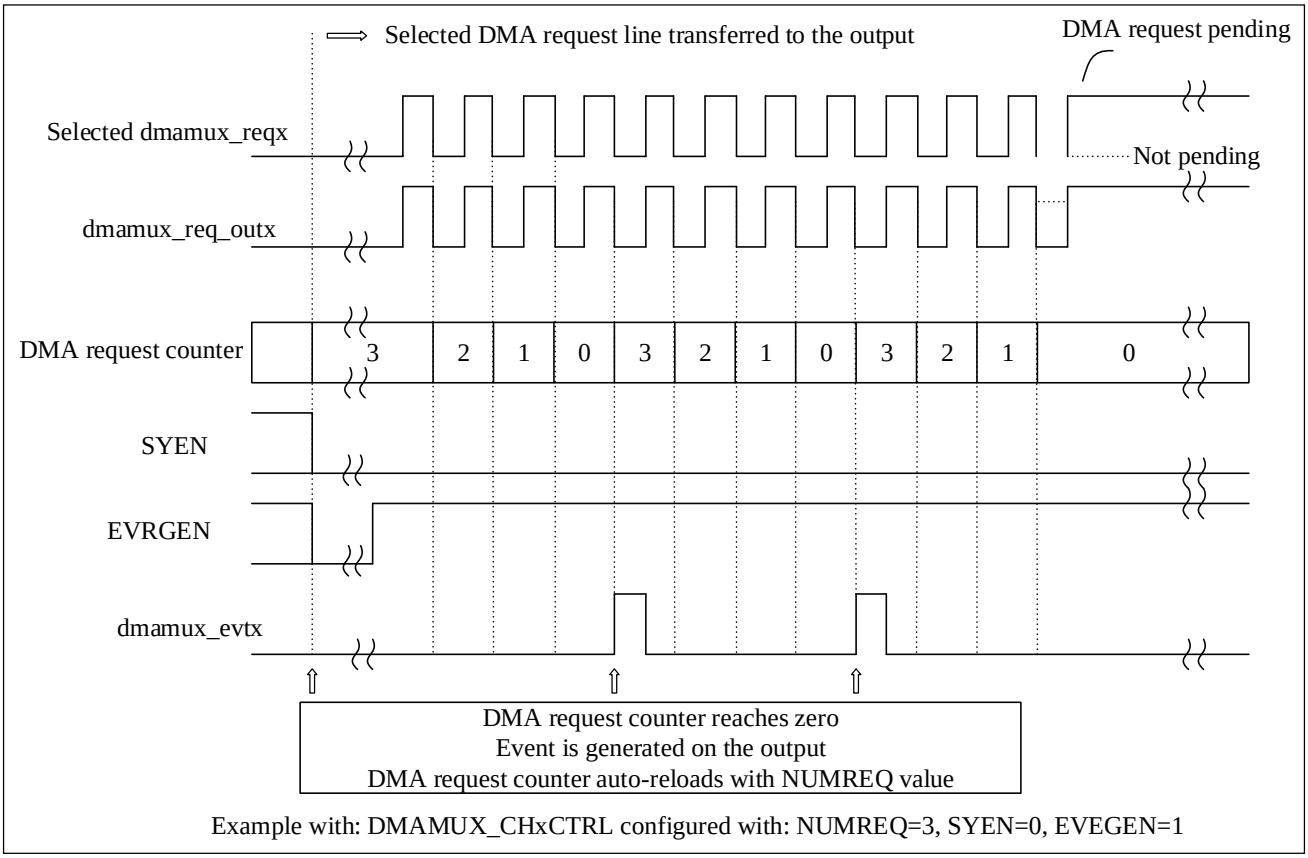
Figure 14-3 DMAMUX Sync Event Generation Example 2



If the DMAMUX_CHXCTRL.EVEGEN bit is enabled, the multiplexer channel generates a channel event as a one AHB clock cycle pulse when its DMA request counter is automatically reloaded with the value from the programmed NUMREQ field, as depicted in the waveform above.

Note: If DMAMUX_CHXCTRL.EVEGEN is enabled and DMAMUX_CHxCTRL.NUMREQ [4:0] is set to 0, an event is generated after each DMA request is served.

Note: A synchronization event (edge) is detected if the state following the edge remains stable for more than two AHB clock cycles.

When writing to the DMAMUX_CHxCTRL register, synchronization events are masked for three AHB clock cycles.

14.4.2.2 Synchronization overrun and interrupt

If a new synchronization event occurs before the request counter underruns (the internal request counter programmed via the DMAMUX_CHxCTRL.NUMREQ [4:0]), the synchronization overrun flag DMAMUX_STS.SOFx is activated.

Note: Synchronization for the request multiplexer channel x must be disabled (DMAMUX_CHxCTRL.SYEN = 0) once the related DMA controller channel is no longer in use. Otherwise, a new synchronization event detection will result in a synchronization overrun due to the absence of a DMA acknowledge (i.e., no served request) from the DMA controller.

The overrun flag DMAMUX_STS.SOFx can be cleared by setting the corresponding clear synchronization overrun flag DMAMUX_CLR.CSOFx.

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Enabling the synchronization overrun flag generates an interrupt if the synchronization overrun interrupt enable bit DMAMUX_CHxCTRL.SOIE is set.

14.4.3 DMAMUX request generator

The DMAMUX request generator issues DMA requests in response to trigger events on its DMA request trigger inputs. It consists of multiple channels, with DMA request trigger inputs connected in parallel to all these channels. The outputs from the DMAMUX request generator channels serve as inputs to the DMAMUX request line multiplexer.

Each DMAMUX request generator channel x includes an enable bit, DMAMUX_RGCFG.GEN (generator enable). The DMA request trigger input for channel x is selected via the DMAMUX_RGCFG.SIGID (trigger signal ID) field. Trigger events on a DMA request trigger input can be configured as rising edge, falling edge, or either edge, with the active edge determined by the DMAMUX_RGCFG.GPOL (generator polarity) field.

When a trigger event occurs, the corresponding generator channel begins producing DMA requests on its output. Each time a DMA request generated by the DMAMUX is serviced by the connected DMA controller (i.e., the request is deasserted), an internal DMA request counter within the DMAMUX request generator is decremented. If the counter underruns, the request generator channel ceases to produce DMA requests, and the DMA request counter is automatically reloaded with its programmed value upon the next trigger event.

Therefore, the total number of DMA requests generated following a trigger event is GNUMREQ [4:0] + 1.

Note: The DMAMUX_CHxCFG.GNUMREQ [4:0] field value should only be modified by software when the DMAMUX_CHxCFG.GEN bit of the corresponding generator channel x is disabled.

A trigger event (edge) is recognized if the state after the edge remains stable for more than two AHB clock cycles. Additionally, when writing to the DMAMUX_RGxCFG register, trigger events are masked for three AHB clock cycles.

14.4.3.1 Trigger overrun and interrupt

If a new DMA request trigger event occurs before the DMAMUX request generator counter underruns (the internal counter programmed via the DMAMUX_CHxCFG.GNUMREQ [4:0] field), and if the request generator channel x is enabled via DMAMUX_CHxCFG.GEN, the hardware asserts the request trigger event overrun flag bit DMAMUX_RGSTS.OFx.

Note: The request generator channel x must be disabled (DMAMUX_RGCFG.GEN = 0) once the related DMA controller channel is no longer in use. Otherwise, a new detected trigger event will cause a trigger overrun due to the absence of an acknowledgment (i.e., no served request) from the DMA.

The overrun flag DMAMUX_RGCFG.OFx is cleared by setting the corresponding clear overrun flag bit DMAMUX_RGCFG.COFx.

Enabling the DMAMUX request trigger overrun flag generates an interrupt if the DMA request trigger event overrun interrupt enable bit DMAMUX_RGCFG.TOVIEN is set.

14.4.4 DMAMUX interrupt

An interrupt can be generated by:

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- a synchronization event overrun in each DMA request line multiplexer channel
- a trigger event overrun in each DMA request generator channel

For each scenario, individual per-channel interrupt enable, status and clear flag register bits are available.

Table 14-2 Interrupt Signal

Interrupt Signal	Interrupt Event	Event Flag	Clear Bit	Enable Bit
dmamuxovr_it	Synchronization event overrun on channel x of the DMAMUX request line multiplexer	SOFx	CSOFx	SOIEN
	Trigger event overrun on channel x of the DMAMUX request generator	OFx	COFx	TOVIEN

14.4.5 DMAMUX programming guide

DMAMUX channel need to be disable first before Program the registers. Both DMAMUX_CHxCTRL.SYEN and DMAMUX_CHXCTRL.EVEGEN should be both 0 before config the DMAMUX_CHxCTRL.SYEN and EGE to other value.

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14.5 Registers

14.5.1 DMAMUX1 registers

DMAMUX1 Base Address: 0x4004_6400

14.5.1.1 DMAMUX1 request line multiplexer channel x control register (DMAMUX1_CHxCTRL)

Address offset: 0x00 + 0x04 * x (x = 0 to 23)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				SYID[3:0]				NUMREQ[4:0]					SYPOL[1:0]		SYEN
				rw				rw					rw		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						EVEGEN	SOIEN	REQID[7:0]							
						rw	rw	rw							

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:24	SYID	Synchronization identification Selects the synchronization input. See Table 5-35.
23:19	NUMREQ	Number of DMA requests minus 1 to forward Specifies the quantity of DMA requests to send to the DMA controller after a synchronization event and/or the number of DMA requests required before generating an output event. *Note: This field should only be modified when both the SOIEN and EVEGEN bits are set to low.*
18:17	SYPOL	Synchronization polarity Defines the edge polarity of the selected synchronization input: 00: no event 01: rising edge 10: failing edge 11: both edge
16	SYEN	Synchronization enable 0: synchronization disable 1: synchronization enable
15:10	Reserved	Reserved, the reset value must be maintained.
9	EVEGEN	Event generation enable 0: event generation disabled

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		1: event generation enable
8	SOIEN	Synchronization overrun interrupt enable 0: interrupt disabled 1: interrupt enabled
7:0	REQID	DMA request identification Selects the input DMA request. See Table 5-33 about assignments of multiplexer inputs to resources.

14.5.1.2 DMAMUX1 request line multiplexer interrupt channel status register (DMAMUX1_STS)

Address offset: 0x80

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								SOF23	SOF22	SOF21	SOF20	SOF19	SOF18	SOF17	SOF16
								r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOF15	SOF14	SOF13	SOF12	SOF11	SOF10	SOF9	SOF8	SOF7	SOF6	SOF5	SOF4	SOF3	SOF2	SOF1	SOF0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:0	SOFx	Synchronization overrun event flag The flag is set when a synchronization event occurs on DMA request line multiplexer channel x while the DMA request counter value is below NUMREQ [4:0]. The flag is cleared by writing a 1 to the corresponding CSOFx bit in DMAMUX1_CLR register.

14.5.1.3 DMAMUX1 request line multiplexer interrupt clear flag register (DMAMUX1_CLR)

Address offset: 0x84

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CSOF23	CSOF22	CSOF21	CSOF20	CSOF19	CSOF18	CSOF17	CSOF16
								w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSOF15	CSOF14	CSOF13	CSOF12	CSOF11	CSOF10	CSOF9	CSOF8	CSOF7	CSOF6	CSOF5	CSOF4	CSOF3	CSOF2	CSOF1	CSOF0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

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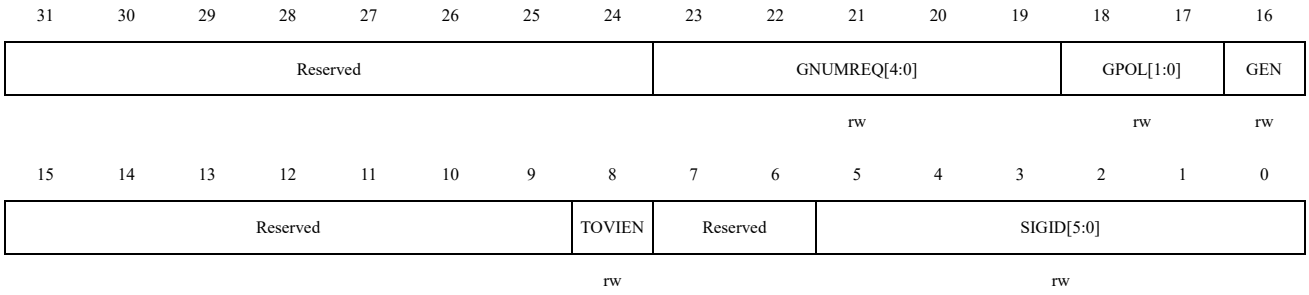
Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:0	CSOFx	Clear synchronization overrun event flag Wirte 1 in each bit clears the corresponding overrun flag SOFx in the DMAMUX1_STS register.

14.5.1.4 DMAMUX1 request generator channel x configuration register (DMAMUX1_CHxCFG)

Address offset: 0x100 + 0x04 * x (x = 0 to 7)

Reset value: 0x0000 0000



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:19	GNUMREQ	Number of DMA request to be generated (minus 1) The actual number generated is GNUBREQ [4:0] + 1 This filed shall only be written when GE bit is disabled.
18:17	GPOL	DMA request generator trigger polarity 00: no event 01: rising edge 10: failing edge 11: both edge
16	GEN	DMA request generator channel x enable 0: DMA request generator channel x disabled 1: DMA request generator channel x enabled
15:9	Reserved	Reserved, the reset value must be maintained.
8	TOVIEN	Trigger overrun interrupt enable 0: Interrupt on a trigger overrun event occurrence is disabled 1: Interrupt on a trigger overrun event occurrence is enabled
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	SIGID	Signal identification Selects the DMA request trigger input used for the channel x of the DMA request generator. See Table 5-34.

14.5.1.5 DMAMUX1 request generator interrupt status register (DMAMUX1_RGSTS)

Address offset: 0x180

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
								r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	OFx	Trigger overrun event flag The flag is set when a new trigger event occurs on DMA request generator channel x. The flag is cleared by writing 1 to the corresponding COFx bit in the DMAMUX1_RGCLR register

14.5.1.6 DMAMUX1 request generator interrupt clear flag register (DMAMUX1_RGCLR)

Address offset: 0x184

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								COF7	COF6	COF5	COF4	COF3	COF2	COF1	COF0
								w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	COFx	Clear trigger overrun event flag Writing a 1 in each bit clears the corresponding overrun flag OFx in the DMAMUX1_RGSTS register

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14.5.2 DMAMUX2 registers

DMAMUX2 Base Address: 0x5112_0000

14.5.2.1 DMAMUX2 request line multiplexer channel x control register (DMAMUX2_CHxCTRL)

Address offset: 0x00 + 0x04 * x (x = 0 to 15)

Reset value: 0x0000 0000

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:24	SYID	Synchronization identification Selects the synchronization input. *Note: DMAMUX2 has only one synchronous input, so this bit field can only be set to 0, other values are invalid.*
23:19	NUMREQ	Number of DMA requests minus 1 to forward Specifies the number of DMA requests to send to the DMA controller after a synchronization event and/or the number of DMA requests required before an output event is generated. *Note: This field should only be modified when both the SOIEN and EVEGEN bits are set to low.*
18:17	SYPOL	Synchronization polarity Defines the edge polarity of the selected synchronization input: 00: no event 01: rising edge 10: failing edge 11: both edge
16	SYEN	Synchronization enable 0: synchronization disable 1: synchronization enable
15:10	Reserved	Reserved, the reset value must be maintained.
9	EVEGEN	Event generation enable 0: event generation disabled

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		1: event generation enable
8	SOIEN	Synchronization overrun interrupt enable 0: interrupt disabled 1: interrupt enabled
7:0	REQID	DMA request identification Selects the input DMA request. See Table 5-31 about assignments of multiplexer inputs to resources.

14.5.2.2 DMAMUX2 request line multiplexer interrupt channel status register (DMAMUX2_STS)

Address offset: 0x80

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOF15	SOF14	SOF13	SOF12	SOF11	SOF10	SOF9	SOF8	SOF7	SOF6	SOF5	SOF4	SOF3	SOF2	SOF1	SOF0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	SOFx	Synchronization overrun event flag The flag is set when a synchronization event occurs on DMA request line multiplexer channel x while the DMA request counter value is below NUMREQ [4:0]. The flag is cleared by writing a 1 to the corresponding CSOFx bit in DMAMUX2_CLR register.

14.5.2.3 DMAMUX2 request line multiplexer interrupt clear flag register (DMAMUX2_CLR)

Address offset: 0x84

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSOF15	CSOF14	CSOF13	CSOF12	CSOF11	CSOF10	CSOF9	CSOF8	CSOF7	CSOF6	CSOF5	CSOF4	CSOF3	CSOF2	CSOF1	CSOF0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

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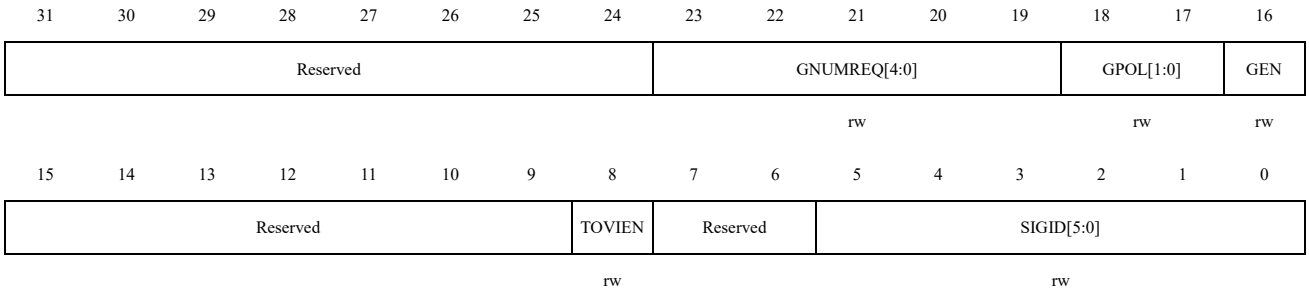
Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CSOFx	Clear synchronization overrun event flag Wirte a 1 in each bit clears the corresponding overrun flag SOFx in the DMAMUX2_STS register.

14.5.2.4 DMAMUX2 request generator channel x configuration register (DMAMUX2_CHxCFG)

Address offset: 0x100 + 0x04 * x (x = 0 to 15)

Reset value: 0x0000 0000



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:19	GNUMREQ	Number of DMA request to be generated (minus 1) The actual number generated is GNUBREQ[4:0] + 1 Note: this filed shall be written when GE bit is disabled.
18:17	GPOL	DMA request generator trigger polarity 00: no event 01: rising edge 10: failing edge 11: both edge
16	GEN	DMA request generator channel x enable 0: DMA request generator channel x disabled 1: DMA request generator channel x enabled
15:9	Reserved	Reserved, the reset value must be maintained.
8	TOVIEN	Trigger overrun interrupt enable 0: Interrupt on a trigger overrun event occurrence is disabled 1: Interrupt on a trigger overrun event occurrence is enabled
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	SIGID	Signal identification Selects the DMA request trigger input used for the channel x of the DMA request generator. See Table 5-32.

14.5.2.5 DMAMUX2 request generator interrupt status register (DMAMUX2_RGSTS)

Address offset: 0x180

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OF15	OF14	OF13	OF12	OF11	OF10	OF9	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	OFx	Trigger overrun event flag The flag is set when a new trigger event occurs on DMA request generator channel x. The flag is cleared by writing a 1 to the corresponding COFx bit in the DMAMUX2_RGCLR register

14.5.2.6 DMAMUX2 request generator interrupt clear flag register (DMAMUX2_RGCLR)

Address offset: 0x184

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COF15	COF14	COF13	COF12	COF11	COF10	COF9	COF8	COF7	COF6	COF5	COF4	COF3	COF2	COF1	COF0
								w	w	w	w	w	w	w	w

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	COFx	Clear trigger overrun event flag Writing a 1 in each bit clears the corresponding overrun flag OFx in the DMAMUX2_RGSTS register

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15 DMA Controller

15.1 Introduction

DMA Controller is controlled by CPU to perform fast data transfer from source to destination. After configuration, data can be transferred without CPU intervention. Thus, CPU can be released for other computation/control tasks or save overall system power consumption.

The chip has three DMA controllers (DMA1, DMA2, DMA3), each with 8 logical channels. Each logical channel is used to serve memory access requests from one or multiple peripherals. An internal arbiter controls the priority of different DMA channels.

15.2 Main Features

The DMA includes the following features:

General

- AMBA 2.0-compliant
- AHB slave interface – used to program the DMA
- Channels
  - 8 channels per DMA, one per source and destination pair
  - Unidirectional channels – data transfers in one direction only
  - Programmable channel priority
- AHB master interfaces that allows simultaneous DMA transfers
  - Support 2 master buses: 1 for Memory Access, 1 for Peripheral Access
- Managers that can be on different AHB layers (multi-layer support)
- Source and destination that can be on different AHB layers (pseudo fly-by performance)
- 32 Bit Data bus for each AHB manager interface
- Transfers
  - Support for memory to memory, memory to peripheral, peripheral to memory, and peripheral to peripheral DMA transfers
  - DMA burst indication on the last beat
- Arbitration scheme to decide which of the request lines is granted access to a particular master bus interface

Address Generation

- Programmable source and destination addresses (on AHB bus)
- Address increment, decrement, or no change

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- Multi-block transfers achieved through:
  - Linked Lists (block chaining)
  - Auto-reloading of channel registers
  - Contiguous address between blocks
- Independent source and destination selection of multi-block transfer type
- Scatter/Gather

Channel Buffering

- Single FIFO per channel for source and destination
- D flip-flop-based FIFO
- Automatic data packing or unpacking to fit FIFO width

Channel Control

- Programmable source and destination for each channel
- Programmable transfer type for each channel (memory to memory, memory to peripheral, peripheral to memory, and peripheral to peripheral)
- Programmable burst transaction size for each channel
- Programmable enable and disable of DMA channel
- Support for disabling channel without data loss
- Support for suspension of DMA operation
- Programmable maximum burst transfer size per channel
- Channel locking – can be programmed to be over the transaction, block, or DMA transfer level

Transfer Initiation

- Handshaking interfaces for source and destination peripherals
  - Hardware handshaking interface
  - Software handshaking interface
  - Peripheral interrupt handshaking interface
- Handshaking interface supports single or burst DMA transactions
- Polarity control for hardware handshaking interface
- Enabling and disabling of individual DMA handshaking interfaces

Flow Control

- Programmable flow control at block transfer level (source, destination, or DMA controller)
- Software control of source data pre-fetch when destination is flow controller

Interrupts

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- Combined and separate interrupt requests
- Interrupt generation on:
  - DMA transfer (multi-block) completion
  - Block transfer completion
  - Single and burst transaction completion
  - Error condition
- Support of interrupt enabling and masking

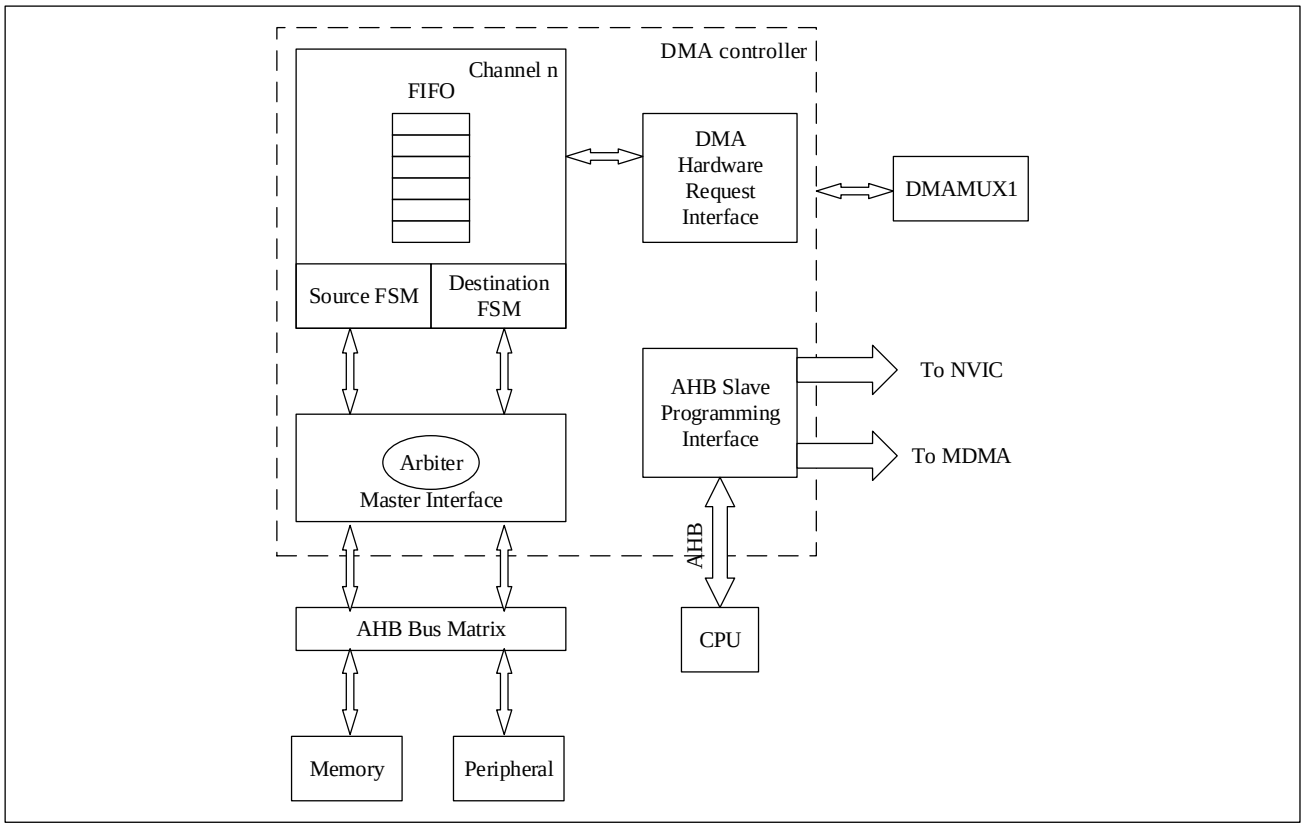
Low Power Mode

- Global Clock Gating
- Channel-Specific Clock Gating

15.3 Block Diagram

The below figure shows the following functional groupings of the main interfaces to the DMA block:

Figure 15-1 DMA Block Diagram



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15.4 Function Description

15.4.1 Basic Definitions

The following terms are concise definitions of the DMA concepts used throughout this section:

Source peripheral – Device on an AHB layer from which the DMA controller reads data; the DMA controller then stores the data in the channel FIFO. The source peripheral teams up with a destination peripheral to form a channel. The source peripheral is either an AHB or APB slave. If the source is an APB slave, it is accessed through the AHB-APB bridge.

Destination peripheral – Device to which the DMA controller writes the stored data from the FIFO (previously read from the source peripheral). The destination peripheral is either an AHB or APB slave. If the destination is an APB slave, it is accessed through the AHB-APB bridge.

Memory – Source or destination that is always "ready" for a DMA transfer and does not require a handshaking interface to interact with the DMA controller. A peripheral should be assigned as memory only if it does not insert more than 16 wait states. If more than 16 wait states are required, then the peripheral must use a handshaking interface – the default if the peripheral is not programmed to be memory – in order to signal when the peripheral is ready to accept or supply data.

A memory peripheral can also generate SPLIT/RETRY responses.

Channel – Read/write data path between a source peripheral on one configured AHB layer and a destination peripheral on the same or different AHB layer that occurs through the channel FIFO. If the source peripheral is not memory, then a source handshaking interface is assigned to the channel.

If the destination peripheral is not memory, then a destination handshaking interface is assigned to the channel. Source and destination handshaking interfaces can be assigned dynamically by programming the channel registers.

Master interface – DMA controller is a master on the AHB bus, reading data from the source and writing it to the destination over the AHB bus. It is possible to have up to 2 master interfaces, which means that up to four independent source and destination channels can operate simultaneously. Each channel has to arbitrate for the master interface. You need to have more than one master interface if the source and destination peripherals reside on different AHB layers.

Slave interface – The AHB interface over which the DMA controller is programmed. The slave interface in practice can be on the same layer as any of the master interfaces, or it can be on a separate layer.

Handshaking interface – A set of signals or software registers that conform to a protocol and handshake between the DMA controller and source or destination peripheral in order to control transferring a single or burst transaction between them. This interface is used to request, acknowledge, and control a DMA transaction. A channel can receive a request through one of three types of handshaking interface: hardware, software, or peripheral interrupt.

- **Hardware handshaking interface** – Uses hardware signals to control transferring a single or burst transaction between the DMA controller and the source or destination peripheral. For more information about this interface, see 15.4.6.3 and 15.4.7.1.
- **Software handshaking interface** – Uses software registers to control transferring a single or burst transaction

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between the DMA controller and the source or destination peripheral. No special DMA handshaking signals are needed on the I/O of the peripheral. This mode is useful for interfacing an existing peripheral to the DMA controller without modifying it. For more information about this interface, see 15.4.10.

- **Peripheral interrupt handshaking interface** – Simple use of the hardware handshaking interface. In this mode, the interrupt line from the peripheral is tied to the dma_req input of the hardware handshaking interface; other interface signals are ignored. For more information about this interface, see 15.4.8.

Flow controller – Device (either the DMA controller, or source/destination peripheral) that determines the length of a DMA block transfer and terminates it.

- If you know the length of a block before enabling the channel, then you should program the DMA controller as the flow controller.
- If the length of a block is not known prior to enabling the channel, the source or destination peripheral needs to terminate a block transfer. In this mode, the peripheral is the flow controller.

Flow control mode (DMA_CHnCFG.FCM) – Special mode that only applies when the destination peripheral is the flow controller. It controls the data pre-fetching from the source peripheral.

Transfer hierarchy – Figure 15-2 illustrates the hierarchy between DMA transfers, block transfers, transactions (single or burst), and AHB transfers (single or burst) for non-memory peripherals. Figure 15-3 shows the transfer hierarchy for memory.

Note: For memory peripherals, there is no DMA Transaction Level.

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Figure 15-2 Transfer Hierarchy for Non-Memory Peripherals

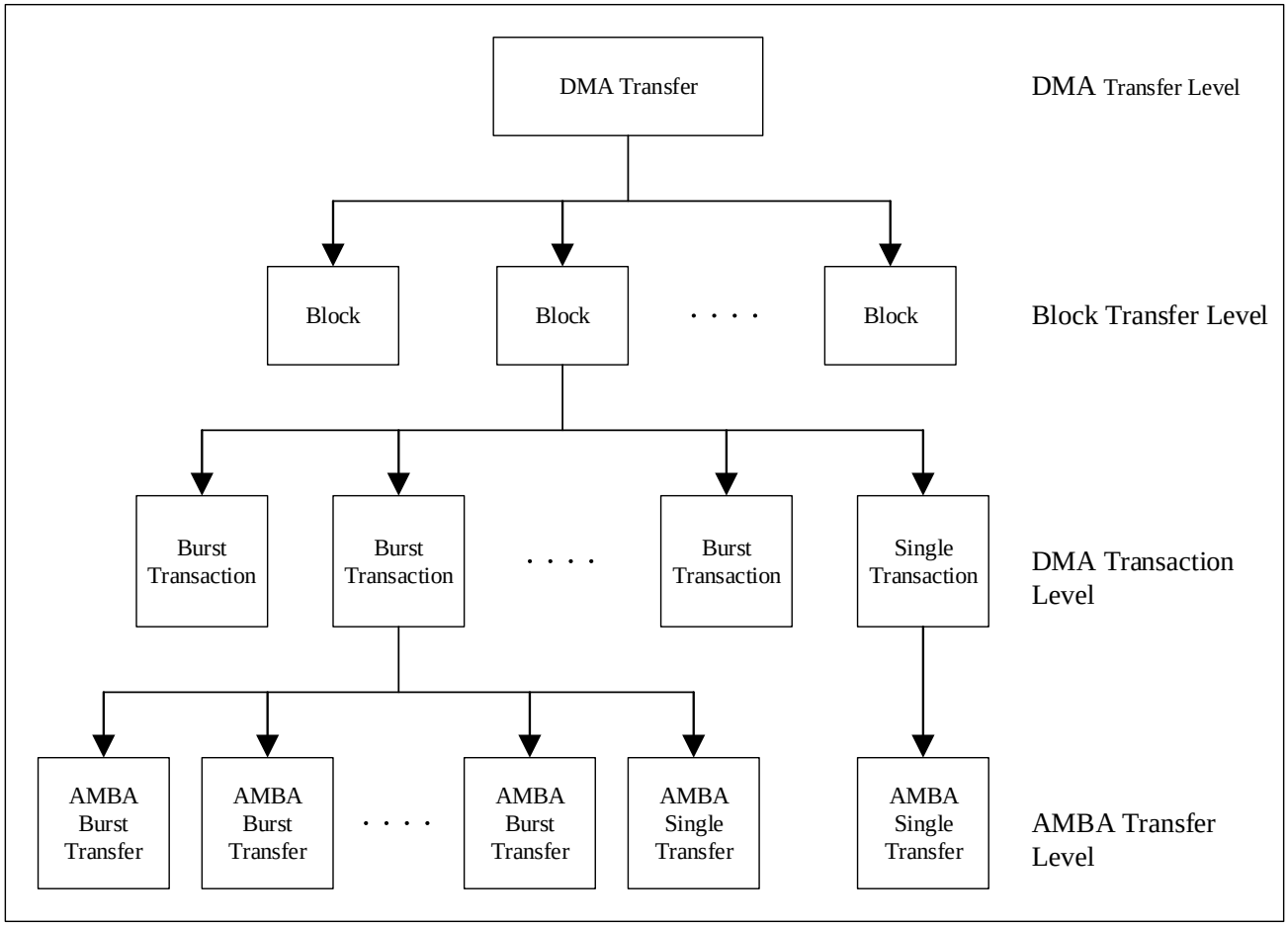

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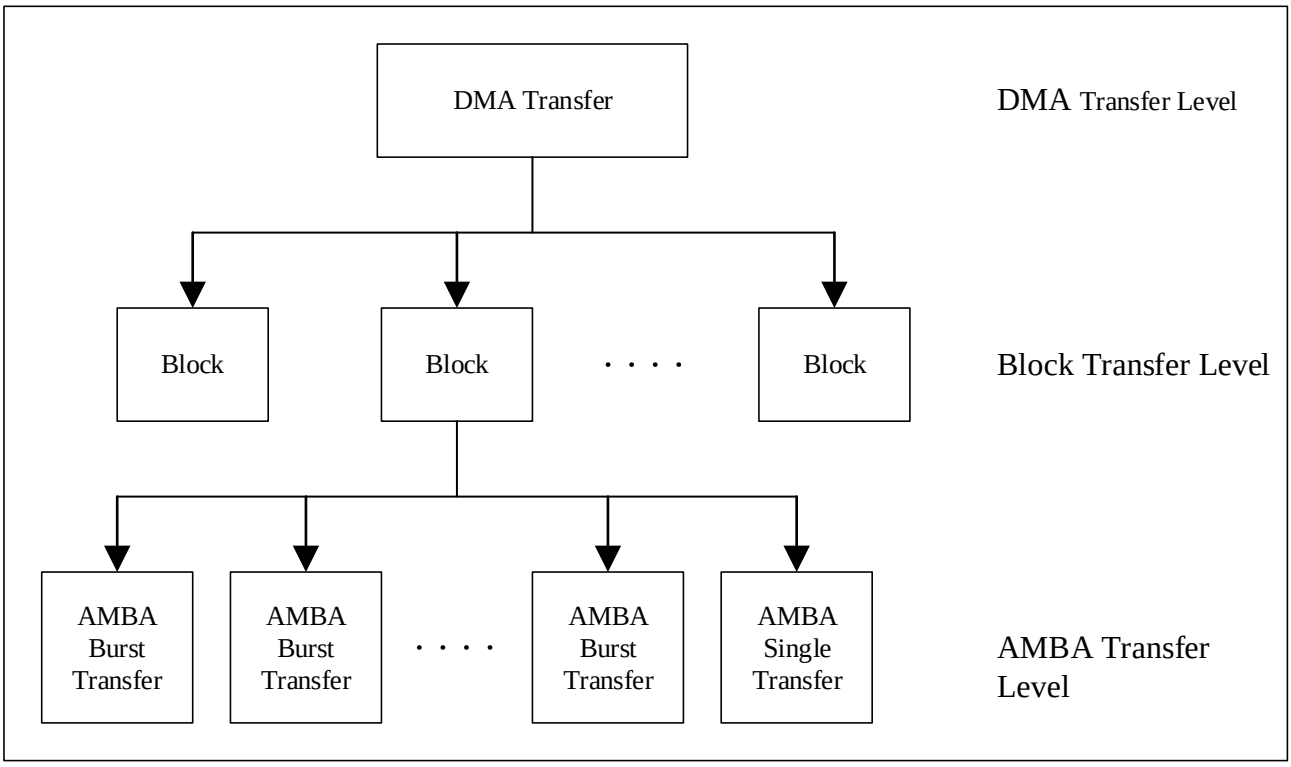
Figure 15-3 Transfer Hierarchy for Memory



Block – Block of DMA data, the amount of which is the block length and is determined by the flow controller. For transfers between the DMA and memory, a block is broken directly into a sequence of bursts and single transfers. For transfers between the DMA and a non-memory peripheral, a block is broken into a sequence of DMA transactions (single and bursts). These are in turn broken into a sequence of AHB transfers.

Transaction – Basic unit of a DMA transfer, as determined by either the hardware or software handshaking interface. A transaction is relevant only for transfers between the DMA controller and a source or destination peripheral if the peripheral is a non-memory device.

There are two types of transactions:

- **Single transaction** – Length of a single transaction is always 1 and is converted to a single AHB transfer.
- **Burst transaction** – Length of a burst transaction is programmed into the DMA. The burst transaction is converted into a sequence of bursts and AHB single transfers. The burst transaction length is under program control and normally bears some relationship to the FIFO sizes in the DMA and in the source and destination peripherals.

DMA transfer – Software controls the number of blocks in a DMA transfer. After the DMA transfer is complete, the hardware within the DMA controller disables the channel and generates an interrupt to signal the DMA transfer completion. You can then reprogram the channel for a new DMA transfer.

- **Single-block DMA transfer** – Consists of a single block.
- **Multi-block DMA transfer** – DMA transfer may consist of multiple DMA blocks. Multi-block DMA transfers are supported through block chaining (linked list pointers), auto-reloading channel registers, and contiguous blocks. The source and destination can independently select which method to use.

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- **Linked lists (block chaining)** – Linked list pointer (LLP) points to the location in system memory where the next linked list item (LLI) exists. The LLI is a set of registers that describes the next block (block descriptor) and an LLP register. The DMA controller fetches the LLI at the beginning of every block when block chaining is enabled. For more information about linked lists and block chaining, see 15.4.9.1.

  LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit, even if the AHB master interface of the LLI supports more than a 32-bit data width.

- **Auto-reloading** – DMA controller automatically reloads the channel registers at the end of each block to the value when the channel was first enabled. For more information about this function, see 15.4.9.2.

- **Contiguous blocks** – Address between successive blocks is selected to be a continuation from the end of the previous block. For more information, see 15.4.9.3.

Scatter – Relevant to destination transfers within a block. The destination address is incremented or decremented by a programmed amount when a scatter boundary is reached. The number of AHB transfers between successive scatter boundaries is under software control.

Gather – Relevant to source transfers within a block. The source address is incremented or decremented by a programmed amount when a gather boundary is reached. The number of AHB transfers between successive gather boundaries is under software control.

For more information about scatter and gather, see 15.4.14.

Channel locking – Software can program a channel to keep the AHB master interface by locking arbitration of the master bus interface for the duration of a DMA transfer, block, or transaction (single or burst). For more information on channel locking, see 15.4.12.2.

Bus locking – Software can program a channel to maintain control of the AHB bus by asserting hlock for the duration of a DMA transfer, block, or transaction (single or burst). At minimum, channel locking is asserted during bus locking. For more information, see 15.4.12.1.

FIFO mode – Special mode to improve bandwidth. When enabled, the channel waits until the FIFO is less than half full to fetch the data from the source peripheral, and waits until the FIFO is greater than or equal to half full in order to send data to the destination peripheral. Because of this, the channel can transfer the data using bursts, which eliminates the need to arbitrate for the AHB master interface in each single AHB transfer. When this mode is not enabled, the channel waits only until the FIFO can transmit or accept a single AHB transfer before it requests the master bus interface.

Pseudo fly-by operation – Typically, it takes two AHB bus cycles to complete a transfer—one for reading the source and one for writing to the destination. However, when the source and destination peripherals of a DMA transfer are on different AHB layers, it is possible for the DMA controller to fetch data from the source and store it in the channel FIFO at the same time that the DMA controller extracts data from the channel FIFO and writes it to the destination peripheral. This activity is known as pseudo fly-by operation. In order for this to occur in appropriate sequential order, the source and destination logic in the DMA controller should first win their respective master interfaces, and then the master interface for both source and destination layers must win arbitration of their AHB layer.

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15.4.2 Block Flow Controller and Transfer Type

The device that controls the length of a block is known as the flow controller. Either the DMA controller, the source peripheral, or the destination peripheral must be assigned as the flow controller.

- If the block size is known prior to when the channel is enabled, then the DMA controller should be programmed as the flow controller. The block size should be programmed into the DMA_CHnCTRL.BTS field.
- If the block size is unknown when the DMA channel is enabled, either the source or destination peripheral must be the flow controller.

The DMA_CHnCTRL.TTFC field indicates the transfer type and flow controller for that channel. Table 15-1 lists valid transfer types and flow controller combinations.

Table 15-1 Transfer Types and Flow Controller Combinations

DMA_CHnCTRL.TTFC	Transfer Type	Flow Controller
000	Memory to Memory	DMA controller
001	Memory to Peripheral	DMA controller
010	Peripheral to Memory	DMA controller
011	Peripheral to Peripheral	DMA controller
100	Peripheral to Memory	Peripheral
101	Peripheral to Peripheral	Source Peripheral
110	Memory to Peripheral	Peripheral
111	Peripheral to Peripheral	Destination Peripheral

15.4.3 Handshaking Interface

Handshaking interfaces are used at the transaction level to control the flow of single or burst transactions. The operation of the handshaking interface is different and depends on whether the peripheral or the DMA controller is the flow controller.

The peripheral uses the handshaking interface to indicate to the DMA controller that it is ready to transfer or accept data over the AHB bus.

A non-memory peripheral can request a DMA transfer through the DMA controller using one of two types of handshaking interfaces:

- Hardware
- Software

Software selects between the hardware or software handshaking interface on a per-channel basis. Software handshaking is accomplished through memory-mapped registers, while hardware handshaking is accomplished using a dedicated handshaking interface.

Note: Throughout the remainder of this section, references to both source and destination hardware handshaking interfaces assume an active-high interface (refer to SRCHSPOL and DSTHSPOL bits in the DMA_CHnCFG register). When active-low handshaking interfaces are used, then the active level and edge are reversed from that of an active-

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high interface.

The type of handshaking interface depends on whether the peripheral is a flow controller or not.

Note: Source and destination peripherals can independently select the handshaking interface type; that is, hardware or software handshaking. For more information, refer to the HSSELSRC and HSSELDST bits in the DMA_CHnCFG register.

15.4.4 Memory Peripherals

Figure 15-3 shows the DMA transfer hierarchy of the DMA for a memory peripheral. There is no handshaking interface with the DMA controller, and therefore the memory peripheral can never be a flow controller. Once the channel is enabled, the transfer proceeds immediately without waiting for a transaction request.

The alternative to not having a transaction-level handshaking interface is to allow the DMA controller to attempt AHB transfers to the peripheral once the channel is enabled. If the peripheral slave cannot accept these AHB transfers, it inserts wait states onto the bus (by de-asserting hready) until it is ready; it is not recommended that more than 16 wait states be inserted onto the bus. By using the handshaking interface, the peripheral can signal to the DMA controller that it is ready to transmit or receive data, and then the DMA controller can access the peripheral without the peripheral inserting wait states onto the bus.

Note: If a channel is used exclusively for memory-to-memory DMA transfers – that is, no transaction-level handshaking on the source or destination side – then set SRCMSIZE and DSTMSIZE fields (in the DMA_CHnCTRL register) to 4 in order to achieve logic optimization.

The SRCMSIZE and DSTMSIZE are properties valid only for peripherals with a handshaking interface; they cannot be used for defining the burst length for memory peripherals.

When the peripherals are memory, the DMA controller is always the flow controller and uses DMA transfers to move blocks; thus the SRCMSIZE and DSTMSIZE values are not used for memory peripherals. The SRCMSIZE and DSTMSIZE limitations are used to accommodate devices that have limited resources, such as a FIFO. Memory does not normally have limitations similar to the FIFOs.

Therefore:

- Length of burst transfers to memory is always equal to the number of data items available in a channel FIFO or data items required to complete the block transfer, whichever is smaller.
- Length of burst transfers from memory is always equal to the space available in a channel FIFO or number of data items required to complete the block transfer, whichever is smaller.

Note: The length of burst transfers to or from memory can be limited by software by programming the MAMBABL field in the DMA_CHnCFG register.

15.4.5 Software Handshaking

When the slave peripheral requires the DMA controller to perform a DMA transaction, it communicates this request by sending an interrupt to the CPU or interrupt controller. The interrupt service routine then uses the software registers detailed in section 15.5.3 to initiate and control a DMA transaction. This group of software registers is used to implement the software handshaking interface.

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The HSSELSRC/HSSELDST bit in the DMA_CHnCFG register must be set to enable software handshaking.

For details on how the software handshaking flow works, refer to 15.4.6.4 and 15.4.7.2.

15.4.6 Handshaking Interface – Peripheral Is Not Flow Controller

When the peripheral is not the flow controller, the DMA controller tries to efficiently transfer the data using as little of the bus bandwidth as possible. Generally, the DMA controller tries to transfer the data using burst transactions and, where possible, fill or empty the channel FIFO in single bursts – provided that the software has not limited the burst length. The DMA controller can also lock the arbitration for the master bus interface so that a channel is permanently granted the master bus interface. Additionally, the DMA controller can assert the AMBA hlock signal to lock the DW_ahb system arbiter. For more information, refer to 15.4.12.

Before describing the handshaking interface operation when the peripheral is not the flow controller, the following sections define the terms "**Single Transaction Region**" and "**Early-Terminated Burst Transaction**".

15.4.6.1 Single Transaction Region

There are cases where a DMA block transfer cannot complete using only burst transactions. Typically this occurs when the block size is not a multiple of the burst transaction length. In these cases, the block transfer uses burst transactions up to the point where the amount of data left to complete the block is less than the amount of data in a burst transaction. At this point, the DMA controller samples the "single" status flag and completes the block transfer using single transactions.

The peripheral asserts a single status flag to indicate to the DMA controller that there is enough data or space to complete a single transaction from or to the source/destination peripheral.

Note: For hardware handshaking, the single status flag is a signal on the hardware handshaking interface; refer to 15.4.6.3. For software handshaking, the single status flag is one of the software handshaking interface registers; refer to 15.4.6.4.

The Single Transaction Region is the time interval where the DMA controller uses single transactions to complete the block transfer; burst transactions are exclusively used outside this region.

Note: Burst transactions can also be used in this region; for more information, refer to section 15.4.6.2.

The Single Transaction Region applies to only a peripheral that is not the flow controller. The precise definition of when this region is entered is dependent on what acts as the flow controller:

- The DMA controller is the flow controller – The source peripheral enters the Single Transaction Region when the number of bytes left to complete in the source block transfer is less than *src_burst_size_bytes*. If: *blk_size_bytes / src_burst_size_bytes = integer*, then the source never enters this region, and the source block uses only burst transactions.

  The destination peripheral enters the Single Transaction Region when the number of bytes left to complete in the destination block transfer is less than dst_burst_size_bytes. If: *blk_size_bytes / dst_burst_size_bytes = integer*, then the destination never enters this region, and the destination block uses only burst transactions.

- Either the source or destination peripheral is the flow controller – The destination or source peripheral enters the Single Transaction Region when the flow control peripheral – that is, the source or destination – signals the last transaction in the block and when the amount of data left to be transferred in the destination/source block is

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less than that which is specified by *dst_burst_size_bytes* or *src_burst_size_bytes*.

15.4.6.2 Early-Terminated Burst Transaction

When a source or destination peripheral is in the Single Transaction Region, a burst transaction can still be requested. However, *src_burst_size_bytes* or *dst_burst_size_bytes* is greater than the number of bytes left to complete in the source/destination block transfer at the time that the burst transaction is triggered. In this case, the burst transaction is started and "early-terminated" at block completion without transferring the programmed amount of data – that is, *src_burst_size_bytes* or *dst_burst_size_bytes* – but only the amount required to complete the block transfer. An Early-Terminated Burst Transaction occurs between the DMA controller and the peripheral only when the peripheral is not the flow controller.

The DMA controller never terminates defined-length bursts early. The DMA controller detects a burst when in the Single Transaction Region, the DMA controller issues an undefined length burst (INCR) of length only large enough to complete the block transfer. It does not transfer all programmed *src_burst_size_bytes* or *dst_burst_size_bytes*.

15.4.6.3 Hardware Handshaking – Peripheral Is Not Flow Controller

Figure 15-4 illustrates the hardware handshaking interface between a peripheral (whether a destination or source) and the DMA controller when the peripheral is not the flow controller.

Figure 15-4 Hardware Handshaking Interface – Peripheral Is Not Flow Controller

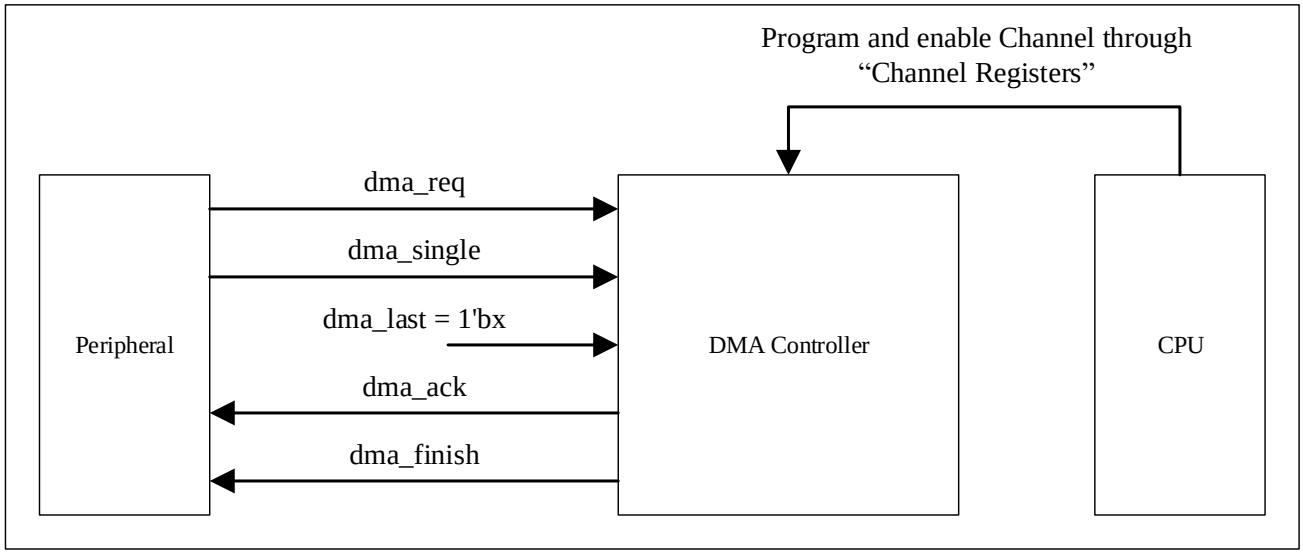

Table 15-2 describes the hardware handshaking signals in the case where the peripheral is not the flow controller; that is, where either the DMA controller or the other peripheral is the flow controller. Signal polarity can be programmed using the SRCHSPOL and DSTHSPOL fields in the DMA_CHnCFG register.

Table 15-2 Hardware Handshaking Interface

Signal	I/O Type	Description
dma_ack	O	DMA controller acknowledge signal to peripheral. The dma_ack signal is asserted after the data phase of the last AHB transfer in the current transaction – single or burst – to the peripheral that has completed. For a single transaction, dma_ack remains asserted until the peripheral de-asserts dma_single; dma_ack is de-asserted one hclk cycle later. For a burst transaction, dma_ack remains

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Signal	I/O Type	Description
		asserted until the peripheral de-asserts dma_req; dma_ack is de-asserted one hclk cycle later.
dma_finish	O	DMA controller asserts dma_finish to signal block completion. This has the same timing as dma_ack and forms a handshaking loop with dma_req if the last transaction in the block is a burst transaction, or with dma_single if the last transaction in the block is a single transaction. There is an exception to the timing definition mentioned earlier when dma_finish interfaces with a source peripheral when the destination peripheral is the flow controller.
dma_last	I	Since the peripheral is not the flow controller, dma_last is not sampled by the DMA controller and this signal is ignored.
dma_req	I	Burst transaction request from peripheral. The DMA controller always interprets the dma_req signal as a burst transaction request, regardless of the level of dma_single. This is a level-sensitive signal; once asserted by the peripheral, dma_req must remain asserted until the DMA controller asserts dma_ack. Upon receiving the dma_ack signal from the DMA controller to indicate the burst transaction is complete, the peripheral should de-assert the burst request signal, dma_req. Once dma_req is de-asserted by the peripheral, the DMA controller de-asserts dma_ack. If an active level on dma_req is detected in the Single Transaction Region (see 15.4.6.1), then the block is completed using an Early-Terminated Burst Transaction (see 15.4.6.2).
dma_single	I	Single transfer status. The dma_single signal is a status signal that is asserted by a destination peripheral when it can accept at least one destination data item; otherwise it is cleared. For a source peripheral, the dma_single signal is again a status signal and is asserted by a source peripheral when it can transmit at least one source data item; otherwise it is cleared. Once asserted, dma_single must remain asserted until dma_ack is asserted, at which time the peripheral should de-assert dma_single. This signal is sampled by the DMA controller only in the Single Transaction Region of the block transfer (see 15.4.6.1). Outside of this region, dma_single is ignored and all transactions are burst transactions.

Note: When the dma_req or dma_single signal is asserted, it must remain asserted until dma_ack is asserted; otherwise, the behavior of DMA controller is not defined and data integrity is not guaranteed. In such scenarios, the corresponding channel can be reused by disabling the channel and then by re-enabling the channel with appropriate programming required for subsequent DMA transfers.

15.4.6.4 Software Handshaking – Peripheral Is Not Flow Controller

When the peripheral is not the flow controller, then the last transaction registers are not used (the DMA_SRCLTREQ register and the DMA_DSTLTREQ register), and the values in these registers are ignored.

Operation – Peripheral Not In Single Transaction Region

Writing a 1 to the DMA_SRCSWTREQ or DMA_DSTSWTREQ register is always interpreted as a burst transaction request. However, in order for a burst transaction request to start, software must write a 1 to the DMA_SRCSGTREQ or DMA_DSTSGTREQ register.

You can write a 1 to the DMA_SRCSGTREQ or DMA_DSTSGTREQ and DMA_SRCSWTREQ or DMA_DSTSWTREQ registers in any order, but both registers must be asserted in order to initiate a burst transaction. Upon completion of the burst transaction, the hardware clears the DMA_SRCSGTREQ or DMA_DSTSGTREQ and DMA_SRCSWTREQ or DMA_DSTSWTREQ registers.

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Email: sales@nsing.com.sg

Operation – Peripheral In Single Transaction Region

Writing a 1 to the DMA_SRCSGTREQ or DMA_DSTSGTREQ initiates a single transaction. Upon completion of the single transaction, both the DMA_SRCSGTREQ or DMA_DSTSGTREQ and DMA_SRCSWTREQ or DMA_DSTSWTREQ bits are cleared by hardware. Therefore, writing a 1 to the DMA_SRCSWTREQ or DMA_DSTSWTREQ is ignored while a single transaction has been initiated, and the requested burst transaction is not serviced.

Again, writing a 1 to the DMA_SRCSWTREQ or DMA_DSTSWTREQ register is always a burst transaction request. However, in order for a burst transaction request to start, the corresponding channel bit in the DMA_SRCSGTREQ or DMA_DSTSGTREQ must be asserted. Therefore, to ensure that a burst transaction is serviced in this region, you must write a 1 to the DMA_SRCSWTREQ or DMA_DSTSWTREQ before writing a 1 to the DMA_SRCSGTREQ or DMA_DSTSGTREQ register. If the programming order is reversed, a single transaction is started instead of a burst transaction. The hardware clears both the DMA_SRCSWTREQ or DMA_DSTSWTREQ and the DMA_SRCSGTREQ or DMA_DSTSGTREQ registers after the burst transaction request completes. When a burst transaction is initiated in the Single Transaction Region (see 15.4.6.1), then the block completes using an Early-Terminated Burst Transaction (see 15.4.6.2).

Software can poll the relevant channel bit in the DMA_SRCSGTREQ or DMA_DSTSGTREQ and DMA_SRCSWTREQ or DMA_DSTSWTREQ registers. When both are 0, then either the requested burst or the single transaction is complete. Alternatively, enable and unmask the IntSrcTran or IntDstTran interrupts to generate an interrupt when the requested source or destination transaction has completed.

Note: The transaction-complete interrupts are triggered when both single and burst transactions are complete. The same transaction-complete interrupt is used for both single and burst transactions.

15.4.6.5 Single Transactions – Peripheral Is Not Flow Controller

When the source peripheral is not the flow controller, the source peripheral can hardcode dma_single to an inactive level (hardware handshaking), or software will never need to initiate single transactions from the source (software handshaking). This can happen if either of the following is true:

- Block size is a multiple of the burst transaction length.
  - If DMA controller is the flow controller, and *blk_size_bytes_dma / src_burst_size_bytes = integer*
  - If the destination peripheral is the flow controller, and *blk_size_bytes_dst / src_burst_size_bytes = integer*
- Block size is not a multiple of the burst transaction length, but the peripheral can dynamically adjust the watermark level that triggers a burst request in order to enable block completion.

When the destination peripheral is not a flow controller, then the destination peripheral may hardcode dma_single to an inactive level (hardware handshaking), or software will never need to initiate single transactions to the destination (software handshaking). This can happen when any of the following are true:

- Block size is a multiple of the burst transaction length.
  - If DMA controller is the flow controller, and *blk_size_bytes_dma / dst_burst_size_bytes = integer*
  - If the source peripheral is flow controller, and *blk_size_bytes_src / dst_burst_size_bytes = integer*
- The destination peripheral can dynamically adjust the watermark level upwards so that a burst request is

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triggered in order to enable a destination block completion.

- It is guaranteed that data at some point will be extracted from the destination FIFO in the "Single transaction region" in order to trigger a burst transaction.

If none of the above are true, then a series of burst transactions followed by single transactions are needed to complete the source/destination block transfer.

15.4.7 Handshaking Interface – Peripheral Is Flow Controller

When the peripheral is the flow controller, it controls the length of the block and must communicate to the DMA controller when the block transfer is complete. The peripheral does this by telling the DMA controller that the current transaction (burst or single) is the last transaction in the block. When the peripheral is the flow controller and the block size is not a multiple of the SRCMSIZE/DESTMSIZE fields (in the DMA_CHnCTRL register), then the peripheral must use single transactions to complete a block transfer.

Note: Since the peripheral can terminate the block on a single transaction, there is no notion of a Single Transaction Region such as there is when the peripheral is not the flow controller.

When the peripheral is the flow controller, it indicates directly to DMA controller which type of transaction (single or burst) to perform. Where possible, the DMA controller uses the maximum possible burst length. It can also lock the arbitration for the master bus so that a channel is permanently granted the master bus interface. The DMA controller can also assert the hlock signal to lock the DW_ahb system arbiter. For more information, refer to 15.4.12.

15.4.7.1 Hardware Handshaking – Peripheral Is Flow Controller

Figure 15-5 shows the hardware handshaking interface between a destination or source peripheral and the DMA controller when the peripheral is the flow controller.

Figure 15-5 Hardware Handshaking Interface – Peripheral Is Flow Controller

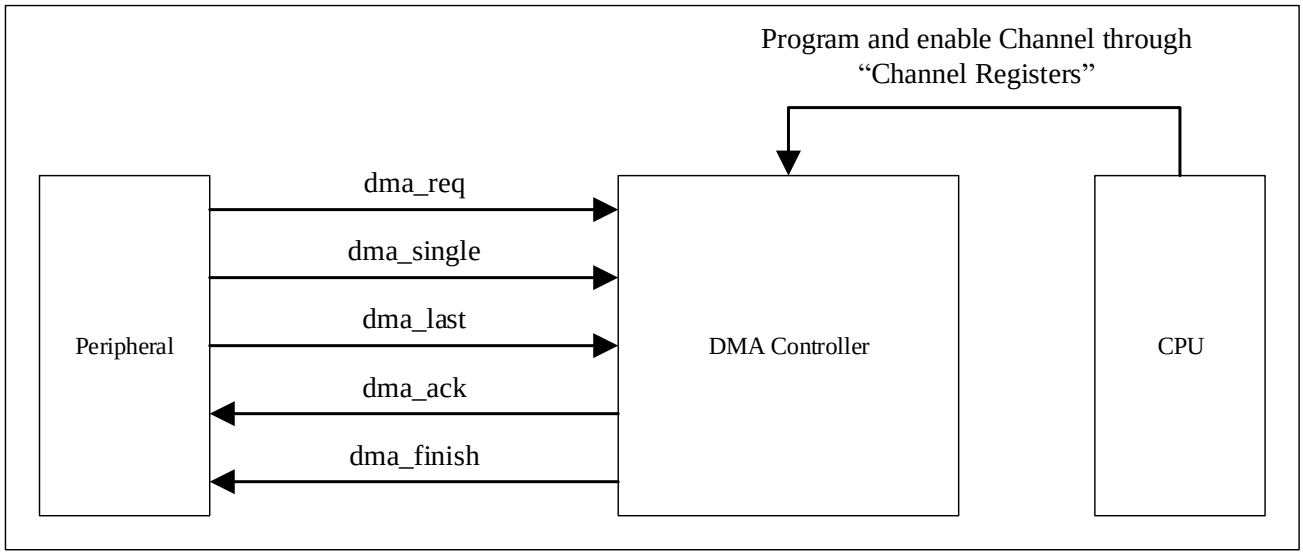

Table 15-3 describes the operation of the hardware handshaking interface signals when the peripheral is the flow controller.

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Table 15-3 Hardware Handshaking Interface

Signal	I/O Type	Description
dma_ack	O	DMA controller acknowledge signal to the peripheral. This is asserted after the data phase of the last AHB transfer in the current transaction (single or burst) to the peripheral has completed. It forms a handshaking loop with dma_req and remains asserted until the peripheral de-asserts dma_req (de-asserted one hclk cycle later).
dma_finish	O	DMA controller block transfer complete signal. The DMA controller asserts dma_finish in order to signal block completion. This uses the same timing as dma_ack and forms a handshaking loop with dma_req.
dma_last	I	Last transaction in block. When the peripheral is the flow controller, it asserts dma_last on the same cycle as dma_req is asserted in order to signal that this transaction request is the last in the block; the block transfer is complete after this transaction is complete. If dma_single is high in the same cycle, then the last transaction is a single transaction. If dma_single is low in the same cycle, then the last transaction is a burst transaction.
dma_req	I	Transaction request from peripheral. An active level on dma_req initiates a transaction request. The type of transaction – single or burst – is qualified by dma_single. Once dma_req is asserted, it must remain asserted until dma_ack is asserted. When the peripheral that is driving dma_req determines that dma_ack is asserted, it must de-assert dma_req.
dma_single	I	Single or burst transaction request. If dma_single is de-asserted in the same clock cycle as a rising edge on dma_req, a burst transaction is requested by the peripheral. If asserted, the peripheral requests a single transaction.

Note: When the dma_req or dma_single signal is asserted, they must remain asserted until dma_ack is asserted; otherwise, the behavior of DMA controller is not defined and data integrity is not guaranteed. In such scenarios, the corresponding channel can be reused by disabling the channel and then by re-enabling the channel with appropriate programming required for subsequent DMA transfers.

15.4.7.2 Software Handshaking – Peripheral is Flow Controller

Writing a 1 to the Source/Destination Software Transaction Request initiates a transaction; see DMA_SRCSWTREQ or DMA_DSTSWTREQ, respectively. The type of transaction (single or burst) depends on the state of the corresponding channel bit in the Single Source/Destination Transaction Request register; see DMA_SRCSGTREQ or DMA_DSTSGTREQ, respectively.

If DMA_SRCSGTREQ[n] or DMA_DSTSGTREQ[n] = 1 when a 1 is written to the DMA_SRCSWTREQ[n] or DMA_DSTSWTREQ[n] register, it means that software is requesting a single transaction on channel n, or a burst transaction otherwise.

The request is the last in the block if the corresponding channel bit in the Last Source/Destination Request register is asserted; refer to DMA_SRCLTREQ or DMA_DSTLTREQ, respectively.

If DMA_SRCLTREQ[n] or DMA_DSTLTREQ[n] = 1 when a 1 is written to the DMA_SRCSWTREQ[n] or DMA_DSTSWTREQ[n] register, this means that software is indicating that this transaction is the last transaction in the block. The DMA_SRCSGTREQ or DMA_DSTSGTREQ and DMA_SRCLTREQ or DMA_DSTLTREQ registers must be written to before the DMA_SRCSWTREQ or DMA_DSTSWTREQ registers.

On completion of the transaction (single or burst) the relevant channel bit in the DMA_SRCSWTREQ or

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DMA_DSTSWTREQ register is cleared by hardware. Software can therefore poll this bit in order to determine when the requested transaction has completed. Alternatively, the IntSrcTran or IntDstTran interrupts can be enabled and unmasked in order to generate an interrupt when the requested transaction (single or burst) is complete.

When the peripheral is the flow controller and the block size is not a multiple of the SRCMSIZE/DESTMSIZE fields (in the DMA_CHnCTRL register), then software must use single transactions to complete the block transfer.

15.4.7.3 Single Transactions – Peripheral is Flow Controller

When the source peripheral is the flow controller, then it can hardcode dma_single to an inactive level (hardware handshaking), or software will never need to initiate single transactions from the source (software handshaking). This occurs when: *blk_size_bytes_src / src_burst_size_bytes = integer*.

When the destination peripheral is the flow controller, then the destination peripheral can hardcode dma_single to an inactive level (hardware handshaking), or software will never need to initiate single transactions to the destination (software handshaking) when: *blk_size_bytes_dst / dst_burst_size_bytes = integer*.

15.4.8 Peripheral Interrupt Request Interface

The interface illustrated in Figure 15-6 is a simplified version of the hardware handshaking interface. In this mode:

- The interrupt line from the peripheral is tied to the dma_req input.
- The dma_single input is tied low.
- All other interface signals are ignored.

This interface can be used where the slave peripheral does not have hardware handshaking signals. To the DMA controller, this is the same 15.4.6.3.

The peripheral can never be the flow controller, since it cannot connect to the dma_last signal. The interrupt line from the peripheral is tied to the dma_req line, as shown in Figure 15-6. The timing of the interrupt line from the peripheral must be the same as the dma_req line, as discussed in 15.4.6.3.

Since the dma_ack line is not sampled by the peripheral, the handshaking loop is as follows:

1 Peripheral generates an interrupt that asserts dma_req.

2 DMA controller completes the burst transaction and generates an end-of-burst transaction interrupt, IntSrcTran or IntDstTran. Interrupts must be enabled and the transaction complete interrupt unmasked.

3 The interrupt service routine clears the interrupt in the peripheral so that the dma_req is de-asserted.

Notice that dma_single is hardcoded to an inactive level. For conditions where the source/destination peripheral can tie dma_single to an inactive level, refer to 15.4.6.5.

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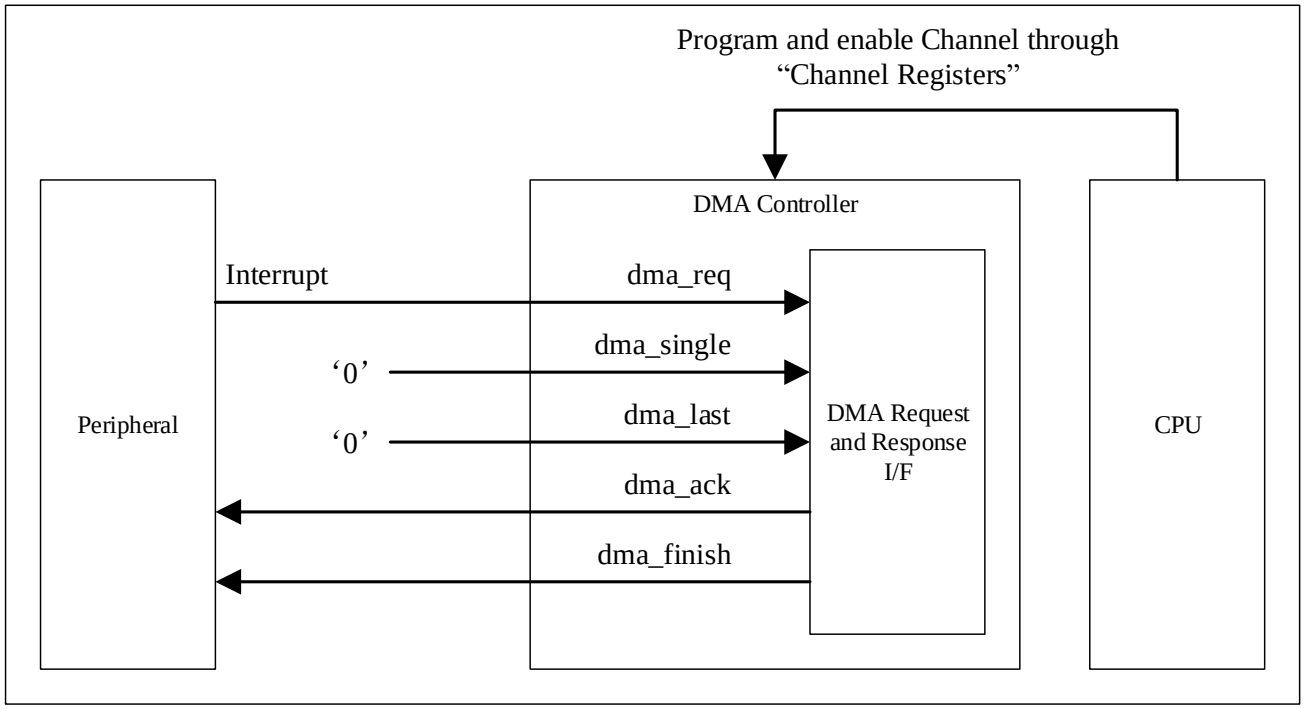
Figure 15-6 Transaction Request Through Peripheral Interrupt



15.4.9 Transfer Types

A DMA transfer may consist of single or multi-block transfers. On successive blocks of a multi-block transfer, the DMA_CHnSA/DMA_CHnDA register in the DMA is reprogrammed using either of the following methods:

- Block chaining using linked lists
- Auto-reloading
- Contiguous address between blocks

On successive blocks of a multi-block transfer, the DMA_CHnCTRL register in the DMA is reprogrammed using either of the following methods:

- Block chaining using linked lists
- Auto-reloading

When block chaining, using Linked Lists is the multi-block method of choice. On successive blocks, the DMA_CHnLLP register in the DMA is reprogrammed using block chaining with linked lists.

A block descriptor consists of 4 registers: DMA_CHnSA, DMA_CHnDA, DMA_CHnLLP and DMA_CHnCTRL. This four registers, along with the DMA_CHnCFG register, are used by the DMA controller to set up and describe the block transfer.

Note: The term Link List Item (LLI) and block descriptor are synonymous.

15.4.9.1 Multi-Block Transfers – Block Chaining Using Linked Lists

Note: Multi-block transfers in which the source and destination are swapped during the transfer are not supported. In a multi-block transfer, the direction must not change for the duration of the transfer.

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In this case, the DMA controller reprograms the channel registers prior to the start of each block by fetching the block descriptor for that block from system memory. This is known as an LLI update.

DMA block chaining uses a Linked List Pointer register (DMA_CHnLLP) that stores the address in memory of the next linked list item. Each LLI contains the corresponding block descriptors:

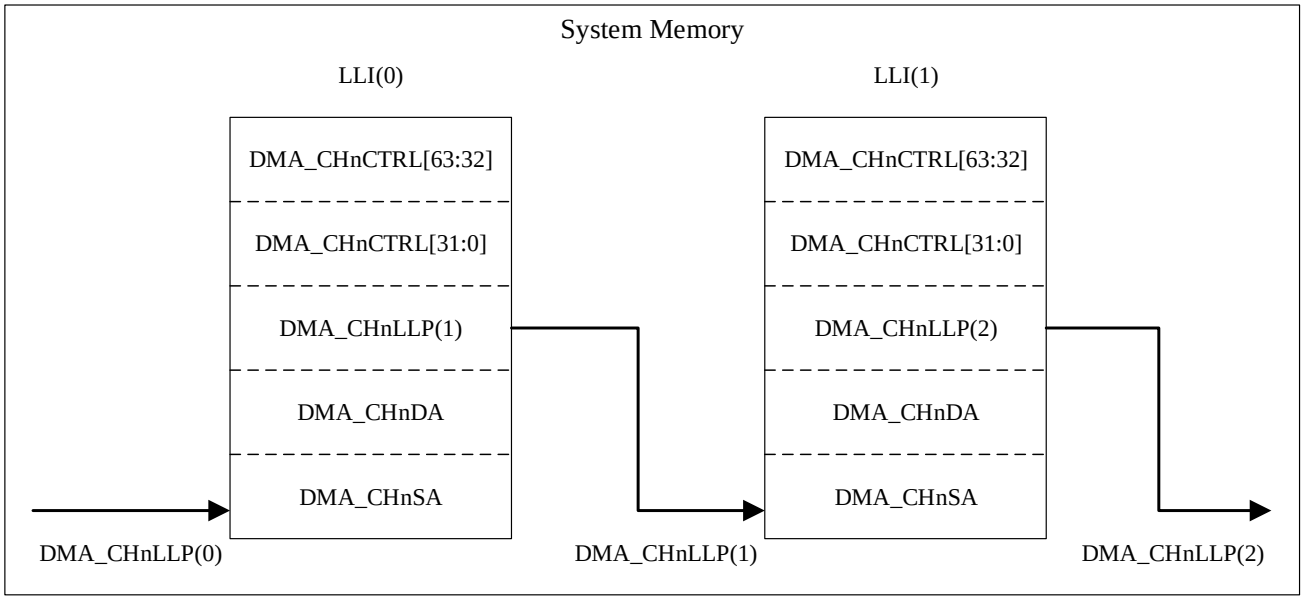
- DMA_CHnSA
- DMA_CHnDA
- DMA_CHnLLP
- DMA_CHnCTRL

To set up block chaining, you program a sequence of Linked Lists in memory.

LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit.

The DMA_CHnSA, DMA_CHnDA, DMA_CHnLLP, and DMA_CHnCTRL registers are fetched from system memory on an LLI update. The updated contents of the DMA_CHnCTRL register are written back to memory on block completion. Figure 15-7 show how you use chained linked lists in memory to define multi-block transfers using block chaining.

Figure 15-7 Multi-Block Transfer Using Linked Lists



15.4.9.2 Auto-Reloading of Channel Registers

During auto-reloading, the channel registers are reloaded with their initial values at the completion of each block and the new values used for the new block.

15.4.9.3 Contiguous Address between Blocks

In this case, the address between successive blocks is selected as a continuation from the end of the previous block.

Enabling the source or destination address to be contiguous between blocks is a function of the LLPSRCEN field (in

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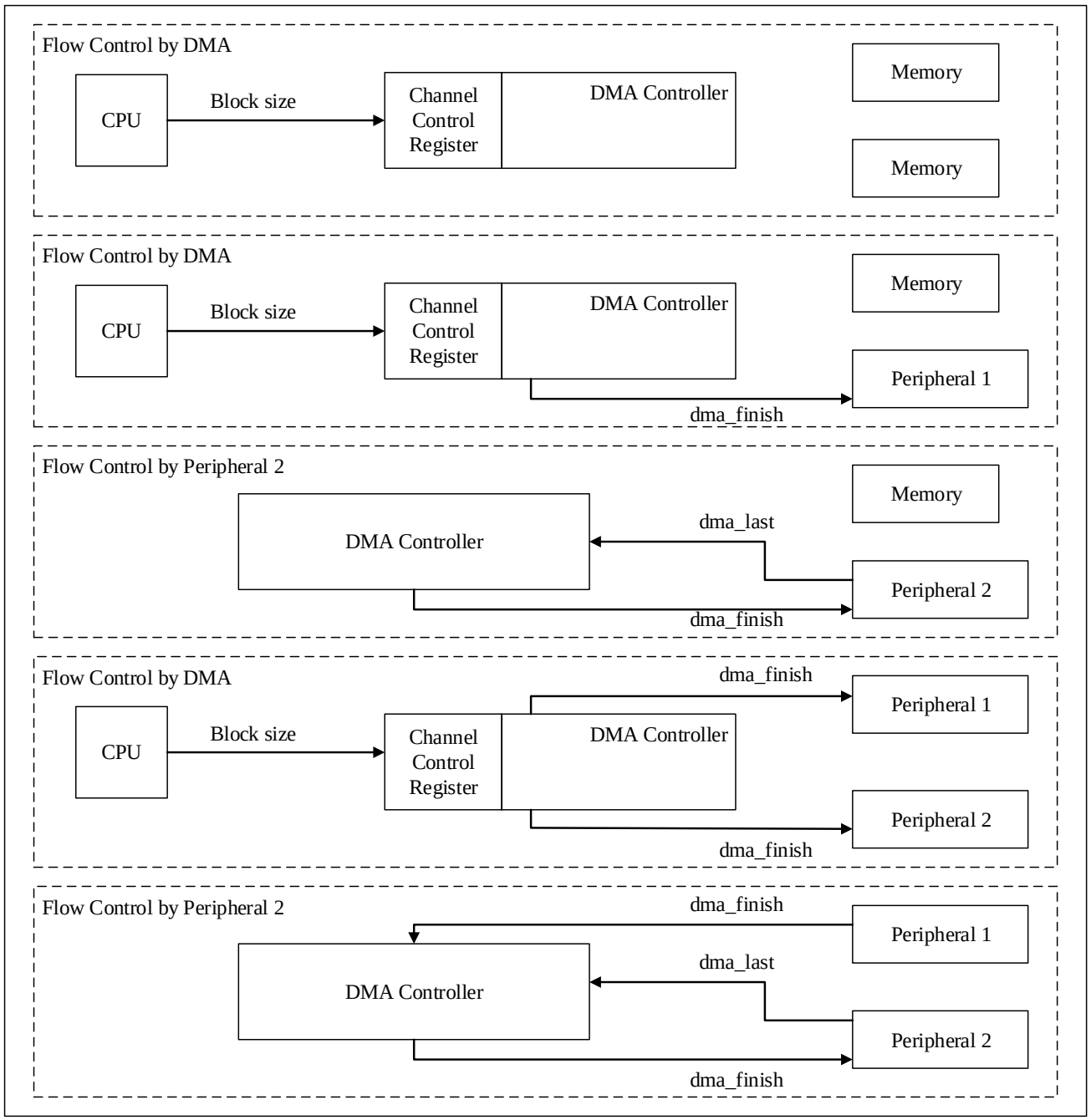
the DMA_CHnCTRL register), ASR field (in the DMA_CHnCFG register), LLPDSTEN field, and ADR field.

15.4.10 Flow Control Configurations

Figure 15-8 indicates five different flow control configurations using hardware handshaking interfaces – a simplified version of the interface is shown. These scenarios can also be used for software handshaking, which uses software registers instead of signals.

Figure 15-8 Flow Control Configurations



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15.4.11 Generating Requests for the AHB Master Bus Interface

Each channel has a source state machine and destination state machine running in parallel. These state machines generate the request inputs to the arbiter, which arbitrates for the master bus interface (one arbiter per master bus interface).

When the source/destination state machine is granted control of the master bus interface, and when the master bus interface is granted control of the external AHB bus, then AHB transfers between the peripheral and the DMA controller (on behalf of the granted state machine) can take place.

AHB transfers from the source peripheral or to the destination peripheral cannot proceed until the channel FIFO is ready. For burst transaction requests and for transfers involving memory peripherals, the criterion for "FIFO readiness" is controlled by the FIFOMS field of the DMA_CHnCFG register.

The definition of FIFO readiness is the same for:

- Single transactions
- Burst transactions, where FIFOMS = 0
- Transfers involving memory peripherals, where FIFOMS = 0

The channel FIFO is deemed ready when the space/data available is sufficient to complete a single AHB transfer of the specified transfer width. FIFO readiness for source transfers occurs when the channel FIFO contains enough room to accept at least a single transfer of source transfer width (the STW field of the DMA_CHnCTRL register). FIFO readiness for destination transfers occurs when the channel FIFO contains data to form at least a single transfer of destination transfer width (the DTW field of the DMA_CHnCTRL register).

When FIFOMS = 1, then the criteria for FIFO readiness for burst transaction requests and transfers involving memory peripherals are as follows:

- A FIFO is ready for a source burst transfer when the FIFO is less than half empty.
- A FIFO is ready for a destination burst transfer when the FIFO is greater than or equal to half full.

Exceptions to this "readiness" occur. During these exceptions, a value of FIFOMS =0 is assumed. The following are the exceptions:

- Near the end of a burst transaction or block transfer – The channel source state machine does not wait for the channel FIFO to be less than half empty if the number of source data items left to complete the source burst transaction or source block transfer is less than CHn_FIFO_DEPTH/2.
- Similarly, the channel destination state machine does not wait for the channel FIFO to be greater than or equal to half full, if the number of destination data items left to complete the destination burst transaction or destination block transfer is less than CHn_FIFO_DEPTH/2.
- When a channel is suspended – The destination state machine does not wait for the FIFO to become half empty to flush the FIFO, regardless of the value of the FIFOMS field.
- After receipt of a split/retry response from a source or destination – The AMBA protocol requires that after an AHB master receives a split/retry response, it must re-issue the transfer that received the split/retry before attempting any other transfer. Therefore, a transfer is re-issued to the same address that returned the split/retry,

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regardless of FIFOMS, when the DMA controller is next granted the AHB bus. This is repeated until an OKAY response is received on the AHB hresp bus.

Note: The FIFO depth of channels 0 to 1 is 64 bytes, and the FIFO depth of channels 2 to 7 is 16 bytes.

When the source or destination peripheral is not memory, the source or destination state machine waits for a single or burst transaction request. Upon receipt of a transaction request and only if the channel FIFO is "ready" for source or destination AHB transfers, a request for the master bus interface is made by the source or destination state machine.

Note: There is one exception to this, which occurs when the destination peripheral is the flow controller and FCM = 1 (data pre-fetching is disabled, in the DMA_CHnCFG register). Then the source state machine does not generate a request for the master bus interface (even if the FIFO is "ready" for source transfers and has received a source transaction request) until the destination requests new data.

When the source/destination peripheral is memory, the source/destination state machine must wait until the channel FIFO is "ready". A request is then made for the master bus interface. There is no handshaking mechanism employed between a memory peripheral and the DMA controller.

15.4.12 Locked DMA Transfers

It is possible to program the DMA for:

- Bus locking – Asserts the AHB hlock signal.
- Channel locking – Locks the arbitration for the AHB master interface, which grants ownership of the master bus interface to one of the requesting channel state machines (source or destination).

Bus and channel locking can proceed for the duration of a DMA transfer, a block transfer, or a single or burst transaction.

15.4.12.1 Bus Locking

If the LOCKB bit in the Channel Configuration register is set, then the AHB hlock signal is asserted for the duration specified in the LOCKBL field.

15.4.12.2 Channel Locking

If the LOCKCH field is set, then the arbitration for the master bus interface is exclusively reserved for the source and destination peripherals of that channel for the duration specified in the LOCKCHL field.

If bus locking is activated for a certain duration, then it follows that the channel is also automatically locked for that duration. Three cases arise:

- LOCKB = 0 – Programmed values of LOCKCH and LOCKCHL are used.
- LOCKB = 1 and LOCKCH = 0 – DMA transfer proceeds as if LOCKCH = 1 and LOCKCHL = LOCKBL. The programmed values of LOCKCH and LOCKCHL are ignored.
- LOCKB = 1 and LOCKCH = 1 – Two cases arise:
  - LOCKBL <= LOCKCHL – In this case, the DMA transfer proceeds as if LOCKCHL = LOCKBL and the programmed value of LOCKCHL is ignored. Thus, if bus locking is enabled over the DMA transfer level, then channel locking is enabled over the DMA transfer level, regardless of the programmed value of

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LOCKCHL.

- LOCKBL > LOCKCHL – The programmed value of LOCKCHL is used. Thus, if bus locking is enabled over the DMA block transfer level and channel locking is enabled over the DMA transfer level, then channel locking is performed over the DMA transfer level.

15.4.12.3 Locking Levels

If locking is enabled for a channel, then locking of the AHB master bus interface at a programmed locking transfer level is activated when the channel is first granted the AHB master bus interface at the start of that locking transfer level. It continues until the locking transfer level has completed; that is, if channel 0 has enabled channel level locking at the block transfer level, then this channel locks the master bus interface when it is first granted the master bus interface at the start of the block transfer, and continues to lock the master bus interface until the block transfer has completed.

Source and destination block transfers occur successively in time, and a new source block cannot commence until the previous destination block has completed. When both source and destination are on the same AHB layer, then block level locking is terminated on completion of the block to the destination. If they are on separate layers, then block-level locking is terminated on completion of the block on that layer – when the source block on the source AHB layer completes, and when the destination block on the destination AHB layer completes. The same is true for DMA transfer-level locking.

Transaction-level locking is different due to the fact that source and destination transactions occur independently in time, and the number of source and destination transactions in a DMA block or DMA transfer do not have to match. When the source and destination are on the same AHB layer, then transaction-level locking is cleared at the end of a source or destination transaction only if the opposing peripheral is not currently in the middle of a transaction.

For example, if locking is enabled at the transaction level and an end-of-source transaction is signaled, then this disables locking only if one of the following is true:

- The destination is on a different AHB layer
- The destination is on the same AHB layer, but the channel is not currently in the middle of a transaction to the destination peripheral.

The same rules apply when an end-of-destination transaction is signalled.

If channel-level or bus-level locking is enabled for a channel at the transaction level, and either the source or destination of the channel is a memory device, then the locking is ignored and the channel proceeds as if locking (bus or channel) is disabled.

Note: Since there is no notion of a transaction level for a memory peripheral, then transaction-level locking is not allowed when either source or destination is memory.

15.4.13 Arbitration for AHB Master Interface

Each DMA channel has two request lines that request ownership of a particular master bus interface: channel source and channel destination request lines.

Source and destination arbitrate separately for the bus. Once a source/destination state machine gains ownership of the master bus interface and the master bus interface has ownership of the AHB bus, then AHB transfers can proceed

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Email: sales@nsing.com.sg

between the peripheral and DMA controller. Figure 15-9 illustrates the arbitration flow of the master bus interface.

An arbitration scheme decides which of the request lines is granted the particular master bus interface. Each channel has a programmable priority. A request for the master bus interface can be made at any time, but is granted only after the current AHB transfer (burst or single) has completed. Therefore, if the master interface is transferring data for a lower priority channel and a higher priority channel requests service, then the master interface will complete the current burst for the lower priority channel before switching to transfer data for the higher priority channel.

To prevent a channel from saturating the master bus interface, it can be given a maximum AMBA burst length (MAMBABL field in the DMA_CHnCFG register) at channel setup time. This also prevents the master bus interface from saturating the AHB bus where the system arbiter cannot change the grant lines until the end of an undefined length burst.

The following is the interface arbitration scheme employed when no channel has locked (see 15.4.12.2) the arbitration for the master bus interface:

- If only one request line is active at the highest priority level, then the request with the highest priority wins ownership of the AHB master bus interface; it is not necessary for the priority levels to be unique.

  If more than one request is active at the highest requesting priority, then these competing requests proceed to a second tier of arbitration.

- If equal priority requests occur, then the lower-numbered channel is granted.

  In other words, if a peripheral request attached to Channel 0 and a peripheral request attached to Channel 7 have the same priority, then the peripheral attached to Channel 0 is granted first.

Note: A channel source is granted before the destination if both have their request lines asserted when a grant decision is made. A channel source and channel destination inherit their channel priority and therefore always have the same priority.

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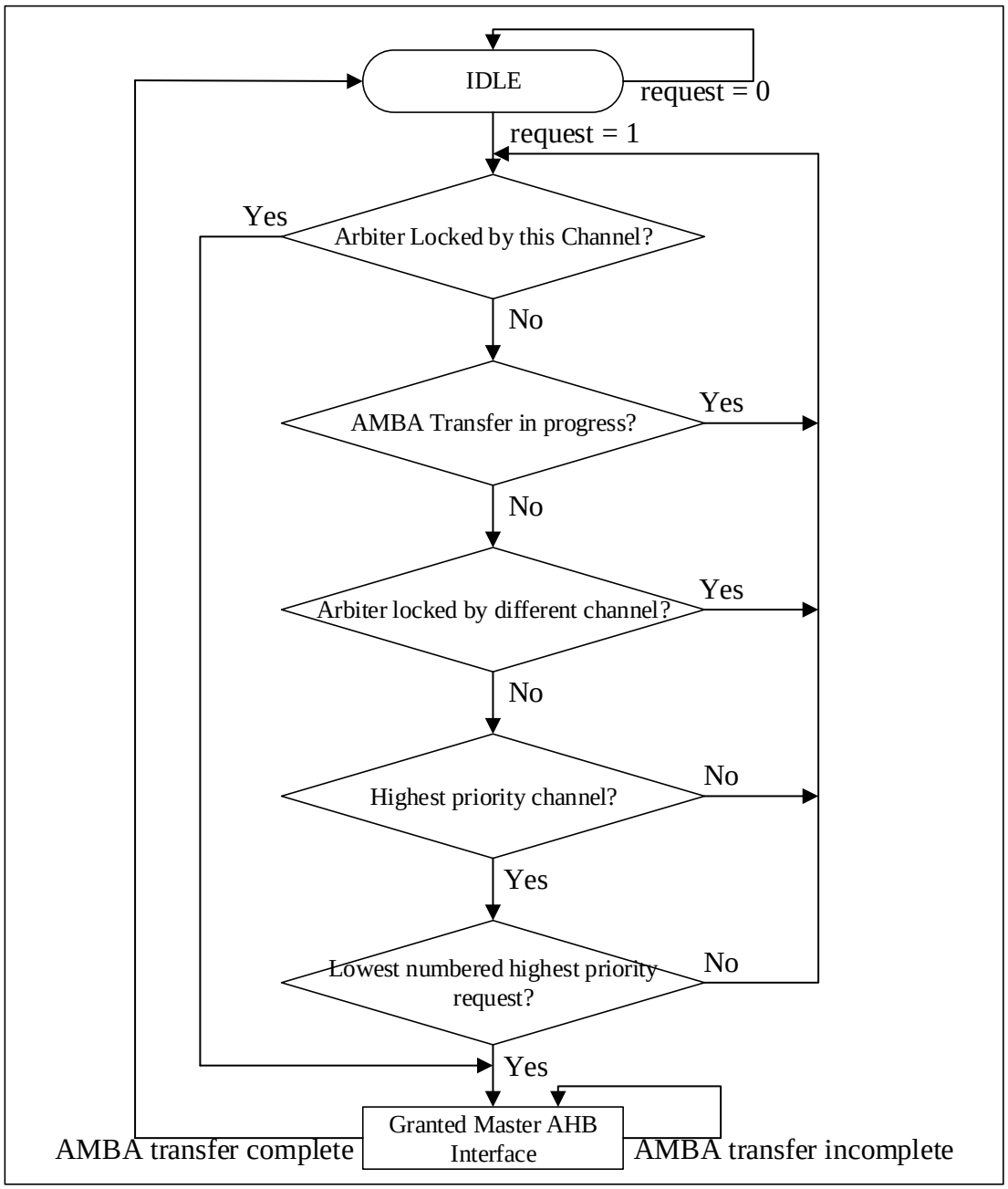
Figure 15-9 Arbitration Flow for Master Bus Interface



15.4.14 Scatter or Gather

Scatter is relevant to a destination transfer. The destination address is incremented or decremented by a programmed amount (the scatter increment) when a scatter boundary is reached. The destination address is incremented or decremented by the value stored in the destination scatter increment (DSI) field of the DMA_CHnDS register, multiplied by the number of bytes in a single AHB transfer to the destination ((decoded value of DTW field of the DMA_CHnCTRL register) / 8) – when a scatter boundary is reached. The number of destination transfers between successive scatter boundaries is programmed into the destination scatter count (DSC) field of the DMA_CHnDS register.

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Scatter is enabled by writing a 1 to the DSTSCAEN field of the DMA_CHnCTRL register. The DINC field determines if the address is incremented, decremented, or remains fixed when a scatter boundary is reached. If the DINC field indicates a fixed-address control throughout a DMA transfer, then the DSTSCAEN field is ignored, and the scatter feature is automatically disabled.

Gather is relevant to a source transfer. The source address is incremented or decremented by a programmed amount when a gather boundary is reached. The number of source transfers between successive gather boundaries is programmed into the source gather count (SGC) field of the DMA_CHnSG register. The source address is incremented or decremented by the value stored in the source gather increment (SGI) field, multiplied by the number of bytes in a single AHB transfer from the source ((decoded value of STW field of the DMA_CHnCTRL register) / 8) – when a gather boundary is reached.

Gather is enabled by writing a 1 to the SRCGATEN field of the DMA_CHnCTRL register. The SINC field determines if the address is incremented, decremented, or remains fixed when a gather boundary is reached. If the SINC field indicates a fixed-address control throughout a DMA transfer, then the SRCGATEN field is ignored, and the gather feature is automatically disabled.

Note: For multi-block transfers, the counters that keep track of the number of transfers left to reach a gather/scatter boundary are re-initialized to the source gather count (SGC) and destination scatter count (DSC), respectively, at the start of each block transfer.

Figure 15-10 shows an example of a destination scatter transfer:

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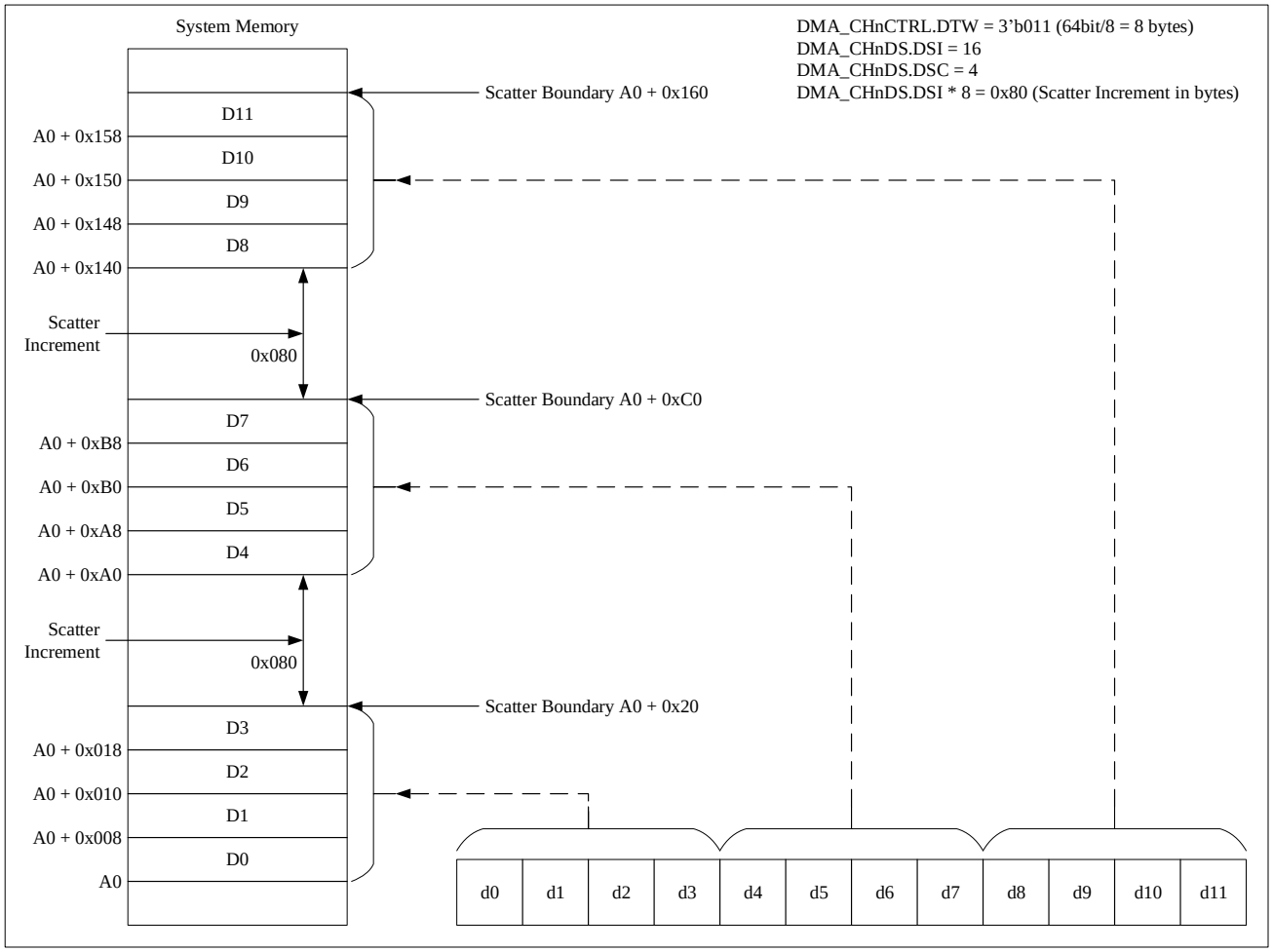
Figure 15-10 Destination Scatter Transfer



As an example of gather increment, consider the following:

- DMA_CHnCTRL.STW = 3'b 010 (32 bits)
- DMA_CHnSG.SGC = 0x04 (source gather count)
- DMA_CHnCTRL.SRCGATEN = 1 (source gather enabled)
- DMA_CHnSA = A0 (starting source address)

Figure 15-11 shows a source gather when SGI = 0x01.

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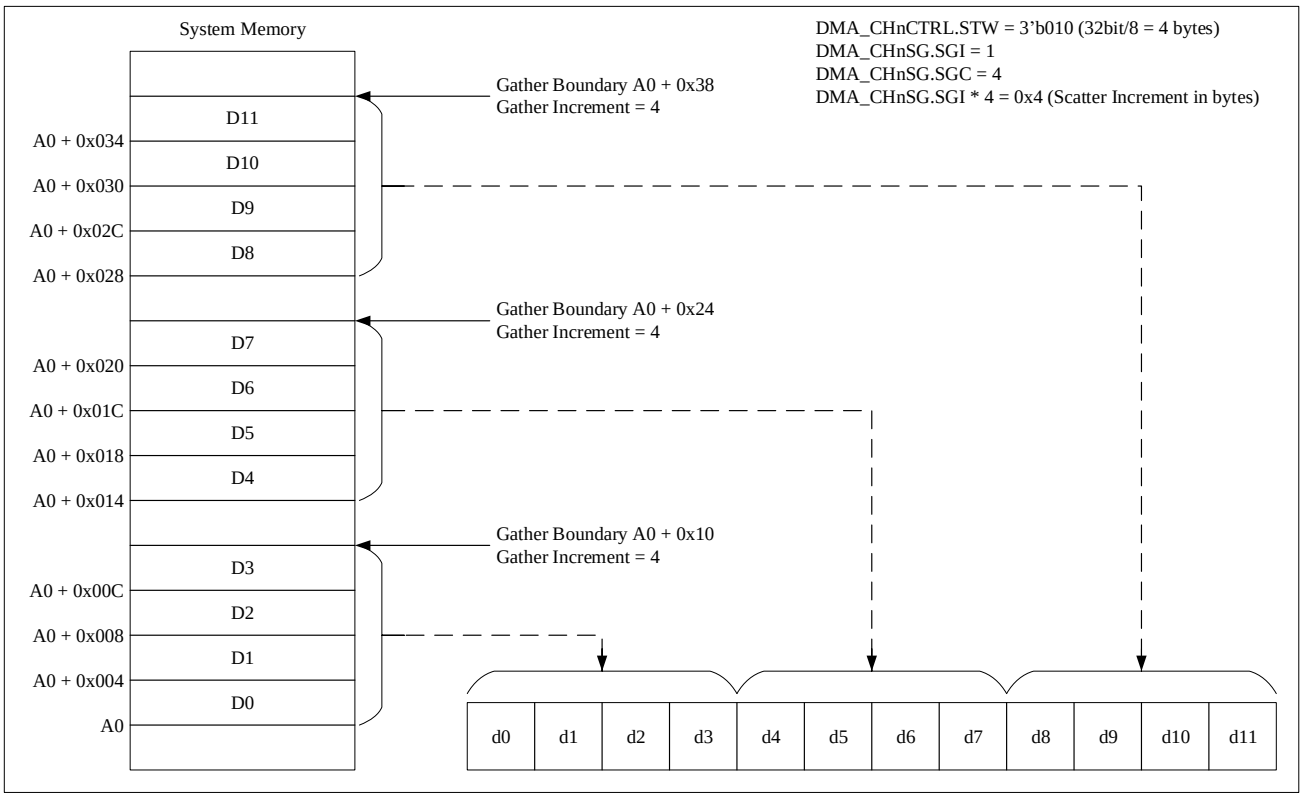
Figure 15-11 Source Gather Transfer



15.4.15 AHB Transfer Error Handling

Upon occurrence of an error in an AHB transfer, the following occurs:

1 DMA transfer in progress stops immediately,

2 Relevant channel is disabled,

3 An interrupt is issued (if not masked).

If multiple channels are enabled, only the one where the AHB error is detected is disabled.

The contents of the FIFO are not cleared, but they become inaccessible and are overwritten once the channel is re-enabled to start a new sequence.

There is no support for automatically resuming the transfer from the point where the error occurred, and the full block transfer has to be re-initiated in order to be successfully completed.

The DMA does not use the hardware handshaking interface to signal the error occurrence in any way, nor does it signal the end of a transfer. In practice, this means that if a request from a peripheral is active when the error occurs – dma_req is high if peripheral is the flow controller; dma_req or dma_single are high if peripheral is not the flow controller – the channel is disabled without the DMA ever asserting dma_ack (or dma_finish).

The hardware handshake interface on the peripheral side has to be re-initiated by the CPU upon detection of the error interrupt. The dma_req signal needs to be brought low before the channel is re-enabled and then brought high when the channel has been enabled.

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15.4.16 Illegal Register Access

An illegal access can be any of the following:

- An AHB transfer of hsize greater than 64 is attempted.
- The hsel signal is asserted, but the address does not decode to a valid address.
- A write to the DMA_CHnSA, DMA_CHnDA, DMA_CHnLLP, DMA_CHnCTRL, DMA_CHnSG, or DMA_CHnDS registers occurs when the channel is enabled.
- A read from the DMA_TCINTCLR, DMA_BTCINTCLR, DMA_STCINTCLR, DMA_DTCINTCLR, DMA_ERRINTCLR is attempted.
- A write to the DMA_TCINTSTS, DMA_BTCINTSTS, DMA_STCINTSTS, DMA_DTCINTSTS, DMA_ERRINTSTS is attempted.
- A write to the DMA_INTCBESTS register is attempted.
- A write to either the DMA ID register or DMA Component ID register is attempted.

An illegal access (read/write) returns an error response.

15.4.17 Interrupt

The following sections describe the registers pertaining to interrupts, their status, and how to clear them. For each channel, there are five types of interrupt sources:

- **IntBlock** – Block Transfer Complete Interrupt

  This interrupt is generated on DMA block transfer completion to the destination peripheral.

- **IntDstTran** – Destination Transaction Complete Interrupt

  This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the destination side.

  Note: If the destination for a channel is memory, then that channel will never generate the IntDstTran interrupt. Because of this, the corresponding bit in this field will not be set.

- **IntErr** – Error Interrupt

  This interrupt is generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled.

- **IntSrcTran** – Source Transaction Complete Interrupt

  This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side.

  Note: If the source or destination is memory, then IntSrcTran/IntDstTran interrupts should be ignored, as there is no concept of a "DMA transaction level" for memory.

- **IntTfr** – DMA Transfer Complete Interrupt

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This interrupt is generated on DMA transfer completion to the destination peripheral.

When a channel has been enabled to generate interrupts, the following is true:

- Interrupt events are stored in the Raw Status registers.
- The contents of the Raw Status registers are masked with the contents of the Mask registers.
- The masked interrupts are stored in the Status registers.
- The contents of the Status registers are used to drive the int_* port signals.
- Writing to the appropriate bit in the Clear registers clears an interrupt in the Raw Status registers and the Status registers on the same clock cycle.

The contents of each of the five Status registers is ORed to produce a single bit for each interrupt type in the Combined Status register; that is, DMA_INTCBESTS register.

For interrupts to propagate past the Raw interrupt register stage, INTEN must be set to 1'b1 (in the DMA_CHnCTRL register), and the relevant interrupt must be unmasked in the interrupt mask register.

15.4.18 Programming Guide

15.4.18.1 Single-block Transfer

This section describes the programming steps for a single-block transfer.

1 Read the Channel Enable register to choose a free (disabled) channel; refer to DMA_CHEN register.

2 Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.

3 Program the following channel registers:

a) Write the starting source address in the DMA_CHnSA register for channel n.

b) Write the starting destination address in the DMA_CHnDA register for channel n.

c) Program LLPSRCEN, LLPDSTEN with 0 (in the DMA_CHnCTRL register) and ASR, ADR with 0 (in the DMA_CHnCFG register). Program the DMA_CHnLLP register with 0.

d) Write the control information for the DMA transfer in the DMA_CHnCTRL register for channel n. For example, in the register, you can program the following:

1) Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TTFC of the DMA_CHnCTRL register.

2) Set up the transfer characteristics, such as:

- Transfer width for the source in the STW field.
- Transfer width for the destination in the DTW field.
- Source master layer in the SMS field where the source resides.
- Destination master layer in the DMS field where the destination resides.

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- Incrementing/decrementing or fixed address for the source in the SINC field.
- Incrementing/decrementing or fixed address for the destination in the DINC field.

e) Write the channel configuration information into the DMA_CHnCFG register for channel n.

1) Designate the handshaking interface type (hardware or software) for the source and destination peripherals; this is not required for memory.

This step requires programming the HSSELSRC/HSSELDST bits, respectively. Writing a 0 activates the hardware handshaking interface to handle source/destination requests. Writing a 1 activates the software handshaking interface to handle source and destination requests.

2) If the hardware handshaking interface is activated for the source or destination peripheral, assign a handshaking interface to the source and destination peripheral; this requires programming the SRCPER and DSTPER bits, respectively.

f) If gather is enabled (the SRCGATEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnSG register for channel n.

g) If scatter is enabled (the DSTSCAEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnDS register for channel n.

4 Ensure that bit 0 of the DMA_CFG register is enabled before writing to DMA_CHEN.

5 Source and destination request single and burst DMA transactions in order to transfer the block of data (assuming non-memory peripherals). The DMA controller acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.

6 Once the transfer completes, hardware sets the interrupts and disables the channel. At this time, you can respond to either the Block Complete or Transfer Complete interrupts, or poll for the transfer complete raw interrupt status register (DMA_RAWTCINTSTS[n], n = channel number) until it is set by hardware, in order to detect when the transfer is complete. Note that if this polling is used, the software must ensure that the transfer complete interrupt is cleared by writing to the Interrupt Clear register (DMA_TCINTCLR[n], n = channel number), before the channel is enabled.

15.4.18.2 Multi-Block Transfer with Linked List

This section describes the programming steps for a multi-block transfer for source and destination Linked List Address.

1 Read the Channel Enable register (see DMA_CHEN) to choose a free (disabled) channel.

2 Set up the chain of Linked List Items (otherwise known as block descriptors) in memory. Write the control information in the LLI.CTRL register location of the block descriptor for each LLI in memory (see Figure 15-7) for channel n. For example, in the register, you can program the following:

a) Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TTFC of the DMA_CHnCTRL register.

b) Set up the transfer characteristics, such as:

1) Transfer width for the source in the STW field.

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2) Transfer width for the destination in the DTW field.

3) Source master layer in the SMS field where the source resides.

4) Destination master layer in the DMS field where the destination resides.

5) Incrementing/decrementing or fixed address for the source in the SINC field.

6) Incrementing/decrementing or fixed address for the destination in the DINC field.

3 Write the channel configuration information into the DMA_CHnCFG register for channel n.

a) Designate the handshaking interface type (hardware or software) for the source and destination peripherals; this is not required for memory.

This step requires programming the HSSELSRC/HSSELDST bits, respectively. Writing a 0 activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a 1 activates the software handshaking interface to handle source/destination requests.

b) If the hardware handshaking interface is activated for the source or destination peripheral, assign the handshaking interface to the source and destination peripheral. This requires programming the SRCPER and DSTPER bits, respectively.

4 Make sure that the LLI.CTRL register locations's LLPSRCEN and LLPDSTEN fields of all LLI entries in memory (except the last) are set to 1. The LLI.CTRL register locations's LLPSRCEN and LLPDSTEN fields of the last Linked List Item must be set to 0. Figure 15-7 shows a Linked List example with two list items.

5 Make sure that the LLI.LLP register locations of all LLI entries in memory (except the last) are non-zero and point to the base address of the next Linked List Item.

6 Make sure that the LLI.SA/LLI.DA register locations of all LLI entries in memory point to the start source/destination block address preceding that LLI fetch.

7 Make that the DONE field of the LLI.CTRL register locations of all LLI entries in memory is cleared.

8 If gather is enabled (the SRCGATEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnSG register for channel n.

9 If scatter is enabled (the DSTSCAEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnDS register for channel n.

10 Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.

11 Program LLPSRCEN, LLPDSTEN with 1 (in the DMA_CHnCTRL register) and ASR, ADR with 0 (in the DMA_CHnCFG register).

12 Program the DMA_CHnLLP register with LLP(0), the pointer to the first linked list item.

13 Finally, enable the channel by writing a 1 to the DMA_CHEN.CHn bit; the transfer is performed.

14 The DMA controller fetches the first LLI from the location pointed to by DMA_CHnLLP.

15 Source and destination request single and burst DMA transactions to transfer the block of data (assuming non-

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memory peripheral). The DMA controller acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.

16 The DMA_CHnCTRL [63:32] register is written out to system memory.

The DMA_CHnCTRL [63:32] register is written out to the same location on the same layer (the LMS field in the DMA_CHnLLP register) where it was originally fetched; that is, the location of the DMA_CHnCTRL register of the linked list item fetched prior to the start of the block transfer. Only the second word of the DMA_CHnCTRL register is written out (bits [63:32]) because only the BTS and DONE fields have been updated by the DMA hardware. Additionally, the DONE bit is asserted to indicate block completion.

Therefore, software can poll the DONE bit of the CTRL register in the LLI to ascertain when a block transfer has completed.

Note: Do not poll the DONE bit in the DMA memory map (that is DMA_CHnCTRL register); instead, poll the DONE bit in the LLI for that block. If the polled DONE bit in the LLI is asserted, then this block transfer has completed. This DONE bit in the LLI is cleared at the start of the transfer (Step 7).

17 The end-of-block interrupt, int_block, is generated after the write-back of the control register has completed.

18 The DMA does not wait for the block interrupt to be cleared, but continues fetching the next LLI from the memory location pointed to by the current DMA_CHnLLP register and automatically reprograms the DMA_CHnSA, DMA_CHnDA, DMA_CHnLLP, and DMA_CHnCTRL channel registers.

The DMA transfer continues until the DMA controller determines that the LLPSRCEN and LLPDSTEN fields of the DMA_CHnCTRL register at the end of the block transfer are 0 and the LOC field of the DMA_CHnLLP register is 0 (as discussed earlier). The DMA controller then knows that the previously transferred block was the last block in the DMA transfer.

15.4.18.3 Multi-Block Transfer with Auto-Reloaded

This section describes the programming steps for a multi-block transfer for source and destination Auto-Reloaded Address.

1 Read the Channel Enable register (see DMA_CHEN) to choose an available (disabled) channel.

2 Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.

3 Program the following channel registers:

a) Write the starting source address in the DMA_CHnSA register for channel n.

b) Write the starting destination address in the DMA_CHnDA register for channel n.

c) Program LLPSRCEN, LLPDSTEN with 0 (in the DMA_CHnCTRL register) and ASR, ADR with 1 (in the DMA_CHnCFG register). Program the DMA_CHnLLP register with 0.

d) Write the control information for the DMA transfer in the DMA_CHnCTRL register for channel n. For example, in the register, you can program the following:

1) Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TTFC of the DMA_CHnCTRL register.

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2) Set up the transfer characteristics, such as:

- Transfer width for the source in the STW field.
- Transfer width for the destination in the DTW field.
- Source master layer in the SMS field where the source resides.
- Destination master layer in the DMS field where the destination resides.
- Incrementing/decrementing or fixed address for the source in the SINC field.
- Incrementing/decrementing or fixed address for the destination in the DINC field.

e) If gather is enabled (the SRCGATEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnSG register for channel n.

f) If scatter is enabled (the DSTSCAEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnDS register for channel n.

g) Write the channel configuration information into the DMA_CHnCFG register for channel n. Ensure that the reload bits, ASR and ADR, are enabled.

1) Designate the handshaking interface type (hardware or software) for the source and destination peripherals; this is not required for memory.

This step requires programming the HSSELSRC/HSSELDST bits, respectively. Writing a 0 activates the hardware handshaking interface to handle source/destination requests. Writing a 1 activates the software handshaking interface to handle source and destination requests.

2) If the hardware handshaking interface is activated for the source or destination peripheral, assign the handshaking interface to the source and destination peripheral. This requires programming the SRCPER and DSTPER bits, respectively.

4 Ensure that bit 0 of the DMA_CFG register is enabled before writing to DMA_CHEN.

5 Source and destination request single and burst DMA transactions to transfer the block of data (assuming non-memory peripherals). The DMA controller acknowledges on completion of each burst/single transaction and carries out the block transfer.

6 When the block transfer has completed, the DMA controller reloads the DMA_CHnSA, DMA_CHnDA, and DMA_CHnCTRL registers. Hardware sets the block-complete interrupt. If the DMA controller samples to the LLPSRCEN, LLPDSTEN is 0 (in the DMA_CHnCTRL register) and ASR, ADR is 0 (in the DMA_CHnCFG register), then the DMA transfer has completed. Hardware sets the transfer complete interrupt and disables the channel. You can either respond to the Block Complete or Transfer Complete interrupts, or poll for the transfer complete raw interrupt status register (DMA_RAWTCINTSTS[n], n = channel number) until it is set by hardware, in order to detect when the transfer is complete. Note that if this polling is used, software must ensure that the transfer complete interrupt is cleared by writing to the Interrupt Clear register (DMA_TCINTCLR[n], n = channel number), before the channel is enabled. If the DMA controller samples to the LLPSRCEN, LLPDSTEN is not 0 (in the DMA_CHnCTRL register) and ASR, ADR is not 0 (in the DMA_CHnCFG register), the next step is performed.

7 The DMA transfer proceeds as follows:

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a) If interrupts are enabled (INTEN = 1, in the DMA_CHnCTRL register) and the block-complete interrupt is unmasked (DMA_BTCINTMSK[x] = 1'b1, where x is the channel number), hardware sets the block-complete interrupt when the block transfer has completed. It then stalls until the block-complete interrupt is cleared by software. If the next block is to be the last block in the DMA transfer, then the block-complete ISR (interrupt service routine) should clear the reload bits (ASR/ADR in the DMA_CHnCFG register). If the next block is not the last block in the DMA transfer, then the reload bits should remain enabled.

b) If interrupts are disabled (INTEN = 0, in the DMA_CHnCTRL register) or the block-complete interrupt is masked (DMA_BTCINTMSK[x] = 1'b0, where x is the channel number), then hardware does not stall until it detects a write to the block-complete interrupt clear register; instead, it immediately starts the next block transfer. In this case, software must clear the reload bits (ASR/ADR in the DMA_CHnCFG register) to indicate that the next transfer is the last block of the DMA transfer.

15.4.18.4 Multi-Block Transfer with SA Auto-Reloaded and DA Linked List

This section describes the programming steps for a multi-block transfer for Source Address Auto-Reloaded and Destination Address Linked List.

1 Read the Channel Enable register (see DMA_CHEN) to choose a free (disabled) channel.

2 Set up the chain of Linked List Items (otherwise known as block descriptors) in memory. Write the control information in the LLI.CTRL register location of the block descriptor for each LLI in memory (see Figure 15-7) for channel n. For example, in the register, you can program the following:

a) Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TTFC of the DMA_CHnCTRL register.

b) Set up the transfer characteristics, such as:

1) Transfer width for the source in the STW field.

2) Transfer width for the destination in the DTW field.

3) Source master layer in the SMS field where the source resides.

4) Destination master layer in the DMS field where the destination resides.

5) Incrementing/decrementing or fixed address for the source in the SINC field.

6) Incrementing/decrementing or fixed address for the destination in the DINC field.

3 Write the starting source address in the DMA_CHnSA register for channel n.

Note: The values in the LLI.SA register locations of each of the Linked List Items (LLIs) set up in memory, although fetched during an LLI fetch, are not used.

4 Write the channel configuration information into the DMA_CHnCFG register for channel n.

a) Designate the handshaking interface type (hardware or software) for the source and destination peripherals; this is not required for memory.

This step requires programming the HSSELSRC/HSSELDST bits, respectively. Writing a 0 activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a 1 activates the software handshaking interface to handle source/destination requests.

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b) If the hardware handshaking interface is activated for the source or destination peripheral, assign the handshaking interface to the source and destination peripheral. This requires programming the SRCPER and DSTPER bits, respectively.

5 Make sure that the LLPSRCEN field is set to 0 and LLPDSTEN field is set to 1 for the LLI.CTRL register locations of all LLI entries in memory (except the last). The LLI.CTRL register locations's LLPSRCEN and LLPDSTEN fields of the last Linked List Item must be set to 0. Figure 15-7 shows a Linked List example with two list items.

6 Make sure that the LLI.LLP register locations of all LLI entries in memory (except the last) are non-zero and point to the base address of the next Linked List Item.

7 Make sure that the LLI.DA register locations of all LLI entries in memory point to the start destination block address preceding that LLI fetch.

8 Make that the DONE field of the LLI.CTRL register locations of all LLI entries in memory is cleared.

9 If gather is enabled (the SRCGATEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnSG register for channel n.

10 If scatter is enabled (the DSTSCAEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnDS register for channel n.

11 Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.

12 Program LLPSRCEN with 0, LLPDSTEN with 1 (in the DMA_CHnCTRL register) and ASR with 1, ADR with 0 (in the DMA_CHnCFG register).

13 Program the DMA_CHnLLP register with LLP(0), the pointer to the first linked list item.

14 Ensure that bit 0 of the DMA_CFG register is enabled before writing to DMA_CHEN register.

15 The DMA controller fetches the first LLI from the location pointed to by DMA_CHnLLP.

Note: The LLI.SA, LLI.DA, LLI.LLP, and LLI.CTRL registers are fetched. The LLI.SA register (although fetched) is not used.

16 Source and destination request single and burst DMA transactions in order to transfer the block of data (assuming non-memory peripheral). The DMA controller acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.

17 The DMA_CHnCTRL [63:32] register is written out to system memory.

The DMA_CHnCTRL [63:32] register is written out to the same location on the same layer (the LMS field in the DMA_CHnLLP register) where it was originally fetched; that is, the location of the DMA_CHnCTRL register of the linked list item fetched prior to the start of the block transfer. Only the second word of the DMA_CHnCTRL register is written out (bits [63:32]) because only the BTS and DONE fields have been updated by the DMA hardware. Additionally, the DONE bit is asserted to indicate block completion.

Therefore, software can poll the DONE bit of the CTRL register in the LLI to ascertain when a block transfer has completed.

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Note: Do not poll the DONE bit in the DMA memory map (that is DMA_CHnCTRL register); instead, poll the DONE bit in the LLI for that block. If the polled DONE bit in the LLI is asserted, then this block transfer has completed. This DONE bit in the LLI is cleared at the start of the transfer (Step 8).

18 The end-of-block interrupt, int_block, is generated after the write-back of the control register has completed.

19 The DMA controller reloads the DMA_CHnSA register from the initial value. Hardware sets the block-complete interrupt. If the DMA controller samples to the LLPSRCEN, LLPDSTEN is 0 (in the DMA_CHnCTRL register) and ASR, ADR is 0 (in the DMA_CHnCFG register), then the DMA transfer has completed. Hardware sets the transfer complete interrupt and disables the channel. You can either respond to the Block Complete or Transfer Complete interrupts, or poll for the transfer complete raw interrupt status register (DMA_RAWTCINTSTS[n], n = channel number) until it is set by hardware, in order to detect when the transfer is complete. Note that if this polling is used, software must ensure that the transfer complete interrupt is cleared by writing to the Interrupt Clear register (DMA_TCINTCLR[n], n = channel number), before the channel is enabled. If the DMA controller samples to the LLPSRCEN, LLPDSTEN is not 0 (in the DMA_CHnCTRL register) and ASR, ADR is not 0 (in the DMA_CHnCFG register), the following steps are performed.

20 The DMA transfer proceeds as follows:

a) If interrupts are enabled (INTEN = 1, in the DMA_CHnCTRL register) and the block-complete interrupt is unmasked (DMA_BTCINTMSK[x] = 1'b1, where x is the channel number), hardware sets the block-complete interrupt when the block transfer has completed. It then stalls until the block-complete interrupt is cleared by software. If the next block is to be the last block in the DMA transfer, then the block-complete ISR (interrupt service routine) should clear the reload bit (ASR in the DMA_CHnCFG register). If the next block is not the last block in the DMA transfer, then the ASR bit should remain enabled.

b) If interrupts are disabled (INTEN = 0, in the DMA_CHnCTRL register) or the block-complete interrupt is masked (DMA_BTCINTMSK[x] = 1'b0, where x is the channel number), then hardware does not stall until it detects a write to the block-complete interrupt clear register; instead, it immediately starts the next block transfer. In this case, software must clear the reload bit (ASR in the DMA_CHnCFG register) to indicate that the next transfer is the last block of the DMA transfer.

21 The DMA controller fetches the next LLI from memory location pointed to by the current DMA_CHnLLP register and automatically reprograms the DMA_CHnDA, DMA_CHnCTRL, and DMA_CHnLLP registers. Note that the DMA_CHnSA is not reprogrammed, since the reloaded value is used for the next DMA block transfer. If the next block is the last block of the DMA transfer, then the DMA_CHnCTRL and DMA_CHnLLP registers just fetched from the LLI should match last Linked List Item (as discussed earlier).

15.4.18.5 Multi-Block Transfer with SA Auto-Reloaded and DA Contiguous

This section describes the programming steps for a multi-block transfer for Source Address Auto-Reloaded and Destination Address Contiguous.

1 Read the Channel Enable register (see DMA_CHEN) to choose a free (disabled) channel.

2 Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.

3 Program the following channel registers:

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a) Write the starting source address in the DMA_CHnSA register for channel n.

b) Write the starting destination address in the DMA_CHnDA register for channel n.

c) Program LLPSRCEN, LLPDSTEN with 0 (in the DMA_CHnCTRL register) and ASR with 1, ADR with 0 (in the DMA_CHnCFG register). Program the DMA_CHnLLP register with 0.

d) Write the control information for the DMA transfer in the DMA_CHnCTRL register for channel n. For example, in the register, you can program the following:

   1) Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TTFC of the DMA_CHnCTRL register.

   2) Set up the transfer characteristics, such as:

      - Transfer width for the source in the STW field.
      - Transfer width for the destination in the DTW field.
      - Source master layer in the SMS field where the source resides.
      - Destination master layer in the DMS field where the destination resides.
      - Incrementing/decrementing or fixed address for the source in the SINC field.
      - Incrementing/decrementing or fixed address for the destination in the DINC field.

e) If gather is enabled (the SRCGATEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnSG register for channel n.

f) If scatter is enabled (the DSTSCAEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnDS register for channel n.

g) Write the channel configuration information into the DMA_CHnCFG register for channel n.

   1) Designate the handshaking interface type (hardware or software) for the source and destination peripherals; this is not required for memory.

      This step requires programming the HSSELSRC/HSSELDST bits, respectively. Writing a 0 activates the hardware handshaking interface to handle source/destination requests. Writing a 1 activates the software handshaking interface to handle source and destination requests.

   2) If the hardware handshaking interface is activated for the source or destination peripheral, assign the handshaking interface to the source and destination peripheral. This requires programming the SRCPER and DSTPER bits, respectively.

4 Ensure that bit 0 of the DMA_CFG register is enabled before writing to DMA_CHEN.

5 Source and destination request single and burst DMA transactions to transfer the block of data (assuming non-memory peripherals). The DMA controller acknowledges on completion of each burst/single transaction and carries out the block transfer.

6 When the block transfer has completed, the DMA controller reloads the DMA_CHnSA register, and the DMA_CHnDA register remains unchanged. Hardware sets the block-complete interrupt. If the DMA controller samples to the LLPSRCEN, LLPDSTEN is 0 (in the DMA_CHnCTRL register) and ASR, ADR is 0 (in the

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DMA_CHnCFG register), then the DMA transfer has completed. Hardware sets the transfer complete interrupt and disables the channel. You can either respond to the Block Complete or Transfer Complete interrupts, or poll for the transfer complete raw interrupt status register (DMA_RAWTCINTSTS[n], n = channel number) until it is set by hardware, in order to detect when the transfer is complete. Note that if this polling is used, software must ensure that the transfer complete interrupt is cleared by writing to the Interrupt Clear register (DMA_TCINTCLR[n], n = channel number), before the channel is enabled. If the DMA controller samples to the LLPSRCEN, LLPDSTEN is not 0 (in the DMA_CHnCTRL register) and ASR, ADR is not 0 (in the DMA_CHnCFG register), the next step is performed.

7 The DMA transfer proceeds as follows:

a) If interrupts are enabled (INTEN = 1, in the DMA_CHnCTRL register) and the block-complete interrupt is unmasked (DMA_BTCINTMSK[x] = 1'b1, where x is the channel number), hardware sets the block-complete interrupt when the block transfer has completed. It then stalls until the block-complete interrupt is cleared by software. If the next block is to be the last block in the DMA transfer, then the block-complete ISR (interrupt service routine) should clear the reload bit (ASR in the DMA_CHnCFG register). If the next block is not the last block in the DMA transfer, then the reload bit should remain enabled.

b) If interrupts are disabled (INTEN = 0, in the DMA_CHnCTRL register) or the block-complete interrupt is masked (DMA_BTCINTMSK[x] = 1'b0, where x is the channel number), then hardware does not stall until it detects a write to the block-complete interrupt clear register; instead, it immediately starts the next block transfer. In this case, software must clear the reload bit (ASR in the DMA_CHnCFG register) to indicate that the next transfer is the last block of the DMA transfer.

15.4.18.6 Multi-Block Transfer with SA Linked List and DA Contiguous

This section describes the programming steps for a multi-block transfer for Source Address Linked List and Destination Address Contiguous.

1 Read the Channel Enable register (see DMA_CHEN) to choose a free (disabled) channel.

2 Set up the linked list (otherwise known as block descriptors) in memory. Write the control information in the LLI.CTRL register location of the block descriptor for each LLI in memory (see Figure 15-7) for channel n. For example, in the register, you can program the following:

a) Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TTFC of the DMA_CHnCTRL register.

b) Set up the transfer characteristics, such as:

1) Transfer width for the source in the STW field.

2) Transfer width for the destination in the DTW field.

3) Source master layer in the SMS field where the source resides.

4) Destination master layer in the DMS field where the destination resides.

5) Incrementing/decrementing or fixed address for the source in the SINC field.

6) Incrementing/decrementing or fixed address for the destination in the DINC field.

3 Write the starting source address in the DMA_CHnDA register for channel n.

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Note: The values in the LLI.DA register locations of each of the Linked List Items (LLIs) set up in memory, although fetched during an LLI fetch, are not used.

4 Write the channel configuration information into the DMA_CHnCFG register for channel n.

a) Designate the handshaking interface type (hardware or software) for the source and destination peripherals; this is not required for memory.

This step requires programming the HSSELSRC/HSSELDST bits, respectively. Writing a 0 activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a 1 activates the software handshaking interface to handle source/destination requests.

b) If the hardware handshaking interface is activated for the source or destination peripheral, assign the handshaking interface to the source and destination peripheral. This requires programming the SRCPER and DSTPER bits, respectively.

5 Make sure that the LLPSRCEN field is set to 1 and LLPDSTEN field is set to 0 for the LLI.CTRL register locations of all LLI entries in memory (except the last). The LLI.CTRL register locations's LLPSRCEN and LLPDSTEN fields of the last Linked List Item must be set to 0. Figure 15-7 shows a Linked List example with two list items.

6 Make sure that the LLI.LLP register locations of all LLI entries in memory (except the last) are non-zero and point to the base address of the next Linked List Item.

7 Make sure that the LLI.SA register locations of all LLI entries in memory point to the start source block address preceding that LLI fetch.

8 Make that the DONE field of the LLI.CTRL register locations of all LLI entries in memory is cleared.

9 If gather is enabled (the SRCGATEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnSG register for channel n.

10 If scatter is enabled (the DSTSCAEN field in the DMA_CHnCTRL register is enabled), program the DMA_CHnDS register for channel n.

11 Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.

12 Program LLPSRCEN with 1, LLPDSTEN with 0 (in the DMA_CHnCTRL register) and ASR, ADR with 0 (in the DMA_CHnCFG register).

13 Program the DMA_CHnLLP register with LLP(0), the pointer to the first linked list item.

14 Ensure that bit 0 of the DMA_CFG register is enabled before writing to DMA_CHEN register.

15 The DMA controller fetches the first LLI from the location pointed to by DMA_CHnLLP.

Note: The LLI.SA, LLI.DA, LLI.LLP, and LLI.CTRL registers are fetched. The LLI.DA register location of the LLI (although fetched) is not used. The DMA_CHnDA register in the DMA remains unchanged.

16 Source and destination request single and burst DMA transactions to transfer the block of data (assuming non-memory peripheral). The DMA controller acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.

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17 The DMA_CHnCTRL [63:32] register is written out to system memory.

The DMA_CHnCTRL [63:32] register is written out to the same location on the same layer (the LMS field in the DMA_CHnLLP register) where it was originally fetched; that is, the location of the DMA_CHnCTRL register of the linked list item fetched prior to the start of the block transfer. Only the second word of the DMA_CHnCTRL register is written out (bits [63:32]) because only the BTS and DONE fields have been updated by the DMA hardware. Additionally, the DONE bit is asserted to indicate block completion.

Therefore, software can poll the DONE bit of the CTRL register in the LLI to ascertain when a block transfer has completed.

Note: Do not poll the DONE bit in the DMA memory map (that is DMA_CHnCTRL register); instead, poll the DONE bit in the LLI for that block. If the polled DONE bit in the LLI is asserted, then this block transfer has completed. This DONE bit in the LLI is cleared at the start of the transfer (Step 8).

18 The end-of-block interrupt, int_block, is generated after the write-back of the control register has completed.

19 The DMA controller does not wait for the block interrupt to be cleared, but continues and fetches the next LLI from the memory location pointed to by the current DMA_CHnLLP register and automatically reprograms the DMA_CHnSA, DMA_CHnLLP, and DMA_CHnCTRL registers. The DMA_CHnDA register is left unchanged. The DMA transfer continues until the DMA controller determines that the LLPSRCEN and LLPDSTEN fields of the DMA_CHnCTRL register at the end of the block transfer are 0 and the LOC field of the DMA_CHnLLP register is 0 (as discussed earlier). The DMA controller then knows that the previously transferred block was the last block in the DMA transfer.

15.4.18.7 Disabling a Channel Prior to Transfer Completion

Under normal operation, software enables a channel by writing a 1 to the CHn bit (in the DMA_CHEN register), and hardware disables a channel on transfer completion by clearing the CHn bit.

The recommended way for software to disable a channel without losing data is to use the CHSUSP bit in conjunction with the FIFOEMPTY bit in the Channel Configuration register (DMA_CHnCFG).

1 If software wishes to disable a channel prior to the DMA transfer completion, then it can set the CHSUSP bit to tell the DMA controller to halt all transfers from the source peripheral. Therefore, the channel FIFO receives no new data.

2 Software can now poll the FIFOEMPTY bit until it indicates that the channel FIFO is empty.

3 The CHn bit can then be cleared by software once the channel FIFO is empty.

When STW < DTW (in the DMA_CHnCTRL register) and the CHSUSP bit is high, the FIFOEMPTY is asserted once the contents of the FIFO do not permit a single word of DTW to be formed. However, there may still be data in the channel FIFO, but not enough to form a single transfer of DTW. In this scenario, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral.

It is permissible to remove the channel from the suspension state by writing a 0 to the CHSUSP register. The DMA transfer completes in the normal manner.

Note: If a channel is disabled by software, an active single or burst transaction is not guaranteed to receive an acknowledgment.

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

15.5 Registers

The N32H7xx supports 3 DMA controllers:

- The DMA1 module register starts at address 0x4004 6800
- The DMA2 module register starts at address 0x4004 6C00
- The DMA3 module register starts at address 0x4004 7000

15.5.1 DMA Channel n Registers

15.5.1.1 DMA Channel n Source Address register (DMA_CHnSA)

Address offset: 0x0000 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0000

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current AHB transfer.

Note: You must program the DMA_CHnSA address to be aligned to DMA_CHnCTRL.STW.

For information on how the DMA_CHnSA is updated at the start of each DMA block for multi-block transfers, refer 15.4.18.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit field	Name	Description
31:0	ADDR	Current Source Address of DMA transfer: Updated after each source transfer. The SINC field in the DMA_CHnCTRL register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

15.5.1.2 DMA Channel n Destination Address register (DMA_CHnDA)

Address offset: 0x0008 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0000

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the

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destination address of the current AHB transfer.

Note: You must program the DMA_CHnDA address to be aligned to DMA_CHnCTRL.DTW.

For information on how the DMA_CHnDA is updated at the start of each DMA block for multi-block transfers, refer 15.4.18.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit field	Name	Description
31:0	ADDR	Current Destination Address of DMA transfer: Updated after each destination transfer. The DINC field in the DMA_CHnCTRL register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

15.5.1.3 DMA Channel n Linked List Pointer register (DMA_CHnLLP)

Address offset: 0x0010 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0000

The LLP register has two functions:

- The logical result of the equation LOC != 0 is used to set up the type of DMA transfer - single or multi-block. If LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type.
- LOC != 0 contains the pointer to the next LLI for block chaining using linked lists; refer to 15.4.9.1. The LLPx register can also point to the address where writeback of the control and source/destination status information occur after block completion.

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOC[30:14]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOC[13:0]														LMS[1:0]	
rw														rw	

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Bit field	Name	Description
31:2	LOC	Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses (Hsize=2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit.
1:0	LMS	List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides. 0x0: The memory device stores the next linked list item on AHB master 1 0x1: The memory device stores the next linked list item on AHB master 2

15.5.1.4 DMA Channel n Control register (DMA_CHnCTRL)

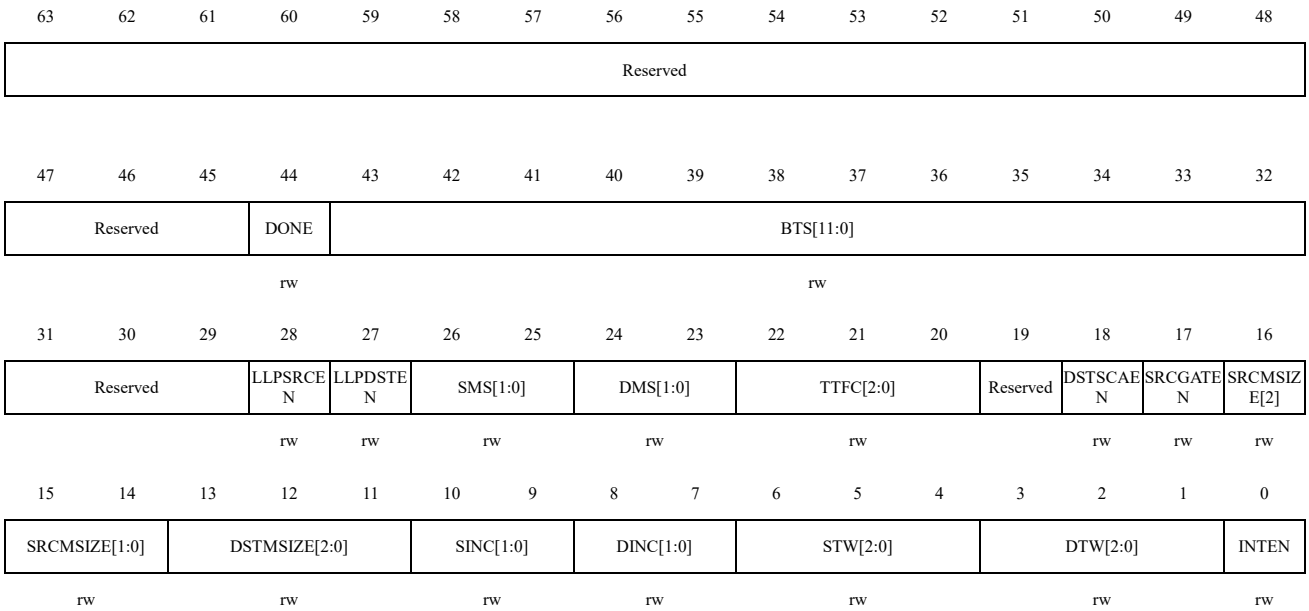
Address offset: 0x0018 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0002 0030 4801

This registers contain fields that control the DMA transfer. The DMA_CHnCTRL register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. For information about the behavior of this register between blocks, refer to 15.4.9.

If status write-back is enabled, the upper word of the control register, bits [63:32], is written to the control register location of the LLI in system memory at the end of the block transfer.

Note: You need to program these registers prior to enabling the channel.



Bit field	Name	Description
63:45	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
44	DONE	Done bit. If status write-back is enabled, the upper word of the control register, bits [63:32], is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI DONE bit to see when a block transfer is complete. The LLI DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. LLI accesses are always 32-bit accesses (Hsize=2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit. For more information, refer to 15.4.9. 0x0: DONE bit is deasserted at the end of block transfer 0x1: Set the DONE bit at the end of block transfer
43:32	BTS	Block Transfer Size. When the DMA controller is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size. The number programmed into BTS indicates the total number of single transactions to perform for every block transfer; a single transaction is mapped to a single AMBA beat. The width of single transaction is determined by STW field. Once the transfer starts, the read-back value is the total number of data items already read from the source peripheral, regardless of what is the flow controller. When the source or destination peripheral is assigned as the flow controller, then the maximum block size that can be read back saturates at 4095, but the actual block size can be greater.
31:29	Reserved	Reserved, the reset value must be maintained.
28	LLPSRCEN	Linked List Pointer for Source Enable. Block chaining is enabled on the source side only if this field is high and LOC is non-zero in DMA_CHnLLP register. For more information, see 15.4.9.1. 0x0: Block chaining using Linked List is disabled on the Source side 0x1: Block chaining using Linked List is enabled on the Source side
27	LLPDSTEN	Linked List Pointer for Destination Enable. Block chaining is enabled on the destination side only if field field is high and LOC is non-zero in DMA_CHnLLP register. For more information, see 15.4.9.1. 0x0: Block chaining using Linked List is disabled on the Destination side 0x1: Block chaining using Linked List is enabled on the Destination side
26:25	SMS	Source Master Select. Identifies the Master Interface layer where the source device (peripheral or memory) resides. 0x0: Source device (peripheral or memory) is accessed from AHB master 1 0x1: Source device (peripheral or memory) is accessed from AHB master 2
24:23	DMS	Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides. 0x0: Destination device (peripheral or memory) is accessed from AHB master 1

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Bit field	Name	Description
		0x1: Destination device (peripheral or memory) is accessed from AHB master 2
22:20	TTFC	Transfer Type and Flow Control. Flow control can be assigned to the DMA controller, the source peripheral, or the destination peripheral. For multi-block transfers using linked list operation, TTFC must be constant for all blocks of this multi-block transfer. 0x0: Transfer type is Memory to Memory and Flow Controller is DMA controller 0x1: Transfer type is Memory to Peripheral and Flow Controller is DMA controller 0x2: Transfer type is Peripheral to Memory and Flow Controller is DMA controller 0x3: Transfer type is Peripheral to Peripheral and Flow Controller is DMA controller 0x4: Transfer type is Peripheral to Memory and Flow Controller is Peripheral 0x5: Transfer type is Peripheral to Peripheral and Flow Controller is Source Peripheral 0x6: Transfer type is Memory to Peripheral and Flow Controller is Peripheral 0x7: Transfer type is Peripheral to Peripheral and Flow Controller is Destination Peripheral
19	Reserved	Reserved, the reset value must be maintained.
18	DSTSCAEN	Destination scatter enable. Scatter on the destination side is applicable only when the DINC bit indicates an incrementing or decrementing address control. 0x0: Destination Scatter is disabled 0x1: Destination Scatter is enabled
17	SRCGATEN	Source gather enable. Gather on the source side is applicable only when the SINC bit indicates an incrementing or decrementing address control. 0x0: Source gather is disabled 0x1: Source gather is enabled
16:14	SRCMSIZE	Source Burst Transaction Length. Number of data items, each of width STW, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface. 0x0: Number of data items to be transferred is 1 0x1: Number of data items to be transferred is 4 0x2: Number of data items to be transferred is 8 0x3: Number of data items to be transferred is 16 0x4: Number of data items to be transferred is 32 0x5: Number of data items to be transferred is 64 0x6: Number of data items to be transferred is 128 0x7: Number of data items to be transferred is 256 *Note: This value is not related to the AHB bus master HBURST bus.*
13:11	DSTMSIZE	Destination Burst Transaction Length. Number of data items, each of width DTW, to be read from the destination every time a destination burst transaction request is made from either the corresponding hardware or

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Email: sales@nsing.com.sg

Bit field	Name	Description
		software handshaking interface. 0x0: Number of data items to be transferred is 1 0x1: Number of data items to be transferred is 4 0x2: Number of data items to be transferred is 8 0x3: Number of data items to be transferred is 16 0x4: Number of data items to be transferred is 32 0x5: Number of data items to be transferred is 64 0x6: Number of data items to be transferred is 128 0x7: Number of data items to be transferred is 256 *Note: This value is not related to the AHB bus master HBURST bus.*
10:9	SINC	Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to "No change". 0x0: Increments the source address 0x1: Decrements the source address 0x2: No change in the source address 0x3: No change in the source address
8:7	DINC	Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to "No change". 0x0: Increments the destination address 0x1: Decrements the destination address 0x2: No change in the destination address 0x3: No change in the destination address
6:4	STW	Source Transfer Width. Mapped to AHB bus hsize. For a non-memory peripheral, typically the peripheral (source) FIFO width. 0x0: Source transfer width is 8 bits 0x1: Source transfer width is 16 bits 0x2: Source transfer width is 32 bits Others: Reserved
3:1	DTW	Destination Transfer Width. Mapped to AHB bus hsize. For a non-memory peripheral, typically the peripheral (destination) FIFO width. 0x0: Destination transfer width is 8 bits 0x1: Destination transfer width is 16 bits 0x2: Destination transfer width is 32 bits Others: Reserved
0	INTEN	Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled. Functions as a global mask bit

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Email: sales@nsing.com.sg

Bit field	Name	Description
		for all interrupts for the channel; Raw* interrupt registers still assert if INTEN = 0. 0x0: Interrupt is disabled 0x1: Interrupt is enabled

15.5.1.5 DMA Channel n Configuration register (DMA_CHnCFG)

Address offset: 0x0040 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0004 0000 0E00

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.

Note: You need to program this register prior to enabling the channel.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reserved															

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reserved		DSTPER[2:0]			Reserved	SRCPER[2:0]			Reserved		PROTCTL[2:0]			FIFOMS	FCM
		rw				rw						rw		rw	rw

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADR	SDR	MAMBABL[9:0]										SRCHSPOL	DSTHSPOL	LOCKB	LOCKCH
rw	rw	rw										rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKBL[1:0]		LOCKCHL[1:0]		HSSELSRC	HSSELDST	FIFOEMPTY	CHSUSP	CHPRIOR[2:0]			Reserved				
rw		rw		rw	rw	r	rw	rw							

Bit field	Name	Description
63:46	Reserved	Reserved, the reset value must be maintained.
45:43	DSTPER	Destination Peripheral hardware interface: Assigns a hardware handshaking interface to the destination of channel x if the HSSELDST field is 0; otherwise, this field is ignored. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. 0x0: Assigns hardware handshaking interface 0 0x1: Assigns hardware handshaking interface 1 0x2: Assigns hardware handshaking interface 2 0x3: Assigns hardware handshaking interface 3 0x4: Assigns hardware handshaking interface 4 0x5: Assigns hardware handshaking interface 5

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Bit field	Name	Description
		0x6: Assigns hardware handshaking interface 6 0x7: Assigns hardware handshaking interface 7 *Note: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.*
42	Reserved	Reserved, the reset value must be maintained.
41:39	SRCPER	Source Peripheral hardware interface: Assigns a hardware handshaking interface to the source of channel x if the HSSELSRC field is 0; otherwise, this field is ignored. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. 0x0: Assigns hardware handshaking interface 0 0x1: Assigns hardware handshaking interface 1 0x2: Assigns hardware handshaking interface 2 0x3: Assigns hardware handshaking interface 3 0x4: Assigns hardware handshaking interface 4 0x5: Assigns hardware handshaking interface 5 0x6: Assigns hardware handshaking interface 6 0x7: Assigns hardware handshaking interface 7 *Note: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.*
38:37	Reserved	Reserved, the reset value must be maintained.
36:34	PROTCTL	Protection Control. Used to drive the AHB HPROT [3:1] bus. The AMBA Specification recommends that the default value of HPROT indicates a non-cached, non-buffered, privileged data access. The reset value is used to indicate such an access. HPROT [0] is tied high because all transfers are data accesses, as there are no opcode fetches. There is a one-to-one mapping of these register bits to the HPROT [3:1] master interface signals. Mapping of HPROT bus is as follows: ■ 1'b1 to HPROT[0] ■ PROTCTL[0] to HPROT[1] ■ PROTCTL[1] to HPROT[2] ■ PROTCTL[2] to HPROT[3]
33	FIFOMS	FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0x0: Space/data available for single AHB transfer of the specified transfer width. 0x1: Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the FIFO depth for source transfers. The exceptions are at the end of a burst transaction request or at the end of a block transfer.
32	FCM	Flow Control Mode. Determines when source transaction requests are serviced when the Destination

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Bit field	Name	Description
		Peripheral is the flow controller. 0x0: Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 0x1: Source transaction requests are not serviced until a destination transaction request occurs. In this mode, the amount of data transferred from the source is limited so that it is guaranteed to be transferred to the destination prior to block termination by the destination. Data pre-fetching is disabled.
31	ADR	Automatic Destination Reload. The DMA_CHnDA register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated. 0x0: Destination Reload disabled 0x1: Destination Reload enabled
30	ASR	Automatic Source Reload. The DMA_CHnSA register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated. 0x0: Source Reload disabled 0x1: Source Reload enabled
29:20	MAMBABL	Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	SRCHSPOL	Source Handshaking Interface Polarity. 0x0: Active high 0x1: Active low *Note: When all peripherals use the hardware handshake interface, the polarity of this interface must be configured as high active.*
18	DSTHSPOL	Destination Handshaking Interface Polarity. 0x0: Active high 0x1: Active low *Note: When all peripherals use the hardware handshake interface, the polarity of this interface must be configured as high active.*
17	LOCKB	Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in LOCKBL. For more information, refer to 15.4.12. 0x0: Bus lock bit is not enabled 0x1: Bus lock bit is enabled
16	LOCKCH	Channel Lock Bit. When the channel is granted control of the master bus interface and if this bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in LOCKCHL. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in LOCKCHL.

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Bit field	Name	Description
		0x0: Channel lock bit is not enabled 0x1: Channel lock bit is enabled
15:14	LOCKBL	Bus lock level. Indicates the duration over which LOCKB bit applies. 0x0: Over complete DMA transfer 0x1: Over complete DMA block transfer 0x2: Over complete DMA transaction 0x3: Over complete DMA transaction
13:12	LOCKCHL	Channel lock level. Indicates the duration over which LOCKCH bit applies. 0x0: Over complete DMA transfer 0x1: Over complete DMA block transfer 0x2: Over complete DMA transaction 0x3: Over complete DMA transaction
11	HSSELSRC	Source Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces - hardware or software - is active for source requests on this channel. If the source peripheral is memory, then this bit is ignored. 0x0: Hardware handshaking interface. Software initiated transaction requests are ignored. 0x1: Software handshaking interface. Hardware initiated transaction requests are ignored.
10	HSSELDST	Destination Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces - hardware or software - is active for destination requests on this channel. If the destination peripheral is memory, then this bit is ignored. 0x0: Hardware handshaking interface. Software initiated transaction requests are ignored. 0x1: Software handshaking interface. Hardware initiated transaction requests are ignored.
9	FIFOEMPTY	Channel FIFO status. Indicates if there is data left in the channel FIFO. Can be used in conjunction with CHSUSP to cleanly disable a channel. For more information, refer to 15.4.18.7. 0x0: Channel FIFO is not empty 0x1: Channel FIFO is empty
8	CHSUSP	Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with FIFOEMPTY to cleanly disable a channel without losing any data. For more information, refer to 15.4.18.7. 0x0: DMA transfer from the source is not suspended 0x1: Suspend DMA transfer from the source

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Bit field	Name	Description
7:5	CHPRIOR	Channel Priority. A priority of 7 is the highest priority, and 0 is the lowest. 0x0: Channel priority is 0 0x1: Channel priority is 1 0x2: Channel priority is 2 0x3: Channel priority is 3 0x4: Channel priority is 4 0x5: Channel priority is 5 0x6: Channel priority is 6 0x7: Channel priority is 7 *Note: For configuration registers with different channels, the reset value for this bit field is the same as the logical channel number.*
4:0	Reserved	Reserved, the reset value must be maintained.

15.5.1.6 DMA Channel n Source Gather register (DMA_CHnSG)

Address offset: 0x0048 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0000

The Source Gather register contains two fields:

- Source gather count field (SGC): Specifies the number of contiguous source transfers of STW between successive gather intervals. This is defined as a gather boundary.
- Source gather interval field (SGI): Specifies the source address increment/decrement in multiples of STW on a gather boundary when gather mode is enabled for the source transfer.

Note: The DMA returns an ERROR response to an illegal register access, which includes accessing registers that have been removed during DMA configuration.

The SINC field controls whether the address increments or decrements. When the SINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DMA_CHnSG register is ignored. For more information, see 15.4.14.

Bit field	Name	Description
31:20	SGC	Source Gather Count. Source contiguous transfer count between successive gather boundaries.

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Bit field	Name	Description
19:0	SGI	Source Gather Interval.

15.5.1.7 DMA Channel n Destination Scatter register (DMA_CHnDS)

Address offset: 0x0050 + 0x58 × n (n = 0 to 7)

Reset value: 0x0000 0000

The Destination Scatter register contains two fields:

- Destination scatter count field (DSC): Specifies the number of contiguous destination transfers of DTW between successive scatter intervals.
- Destination scatter interval field (DSI): Specifies the destination address increment/decrement in multiples of DTW on a scatter boundary when scatter mode is enabled for the destination transfer.

Note: The DMA returns an ERROR response to an illegal register access, which includes accessing registers that have been removed during DMA configuration.

The DINC field controls whether the address increments or decrements. When the DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DMA_CHnDS register is ignored. For more information, see 15.4.14.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSC[11:0]												DSI[19:16]			
rw												rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSI[15:0]															
rw															

Bit field	Name	Description
31:20	DSC	Destination Scatter Count. Destination contiguous transfer count between successive scatter boundaries.
19:0	DSI	Destination Scatter Interval.

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15.5.2 DMA Interrupt Registers

15.5.2.1 DMA IntTfr Interrupt Raw Status register (DMA_RAWTCINTSTS)

Address offset: 0x02C0

Reset value: 0x0000 0000

This register indicates the Raw status for DMA Transfer Complete interrupt.

Interrupt events are stored in this Raw Interrupt Status register before masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 raw transfer complete interrupt.

Each bit in this register is cleared by writing a 1 to the corresponding location in the DMA IntTfr Interrupt Clear register.

Note: Write access is available to this register or software testing purposes only. Under normal operation, writes to this register are not recommend.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Raw Status for IntTfr Interrupt. 0x0: Inactive Raw Interrupt Status 0x1: Active Raw Interrupt Status

15.5.2.2 DMA IntBlock Interrupt Raw Status register (DMA_RAWBTCINTSTS)

Address offset: 0x02C8

Reset value: 0x0000 0000

This register indicates the Raw status for DMA Block Transfer Complete interrupt.

Interrupt events are stored in this Raw Interrupt Status register before masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 raw block transfer complete interrupt.

Each bit in this register is cleared by writing a 1 to the corresponding location in the DMA IntBlock Interrupt Clear register.

Note: Write access is available to this register or software testing purposes only. Under normal operation, writes to this register are not recommend.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Raw Status for IntBlock Interrupt. 0x0: Inactive Raw Interrupt Status 0x1: Active Raw Interrupt Status

15.5.2.3 DMA IntSrcTran Interrupt Raw Status register (DMA_RAWSTCINTSTS)

Address offset: 0x02D0

Reset value: 0x0000 0000

This register indicates the Raw status for DMA Source Transaction Complete interrupt.

Interrupt events are stored in this Raw Interrupt Status register before masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 raw source transaction complete interrupt.

Each bit in this register is cleared by writing a 1 to the corresponding location in the DMA IntSrcTran Interrupt Clear register.

Note: Write access is available to this register or software testing purposes only. Under normal operation, writes to this register are not recommend.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Raw Status for IntSrcTran Interrupt. 0x0: Inactive Raw Interrupt Status

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Bit field	Name	Description
		0x1: Active Raw Interrupt Status

15.5.2.4 DMA IntDstTran Interrupt Raw Status register (DMA_RAWDTCINTSTS)

Address offset: 0x02D8

Reset value: 0x0000 0000

This register indicates the Raw status for DMA Destination Transaction Complete interrupt.

Interrupt events are stored in this Raw Interrupt Status register before masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 raw destination transaction complete interrupt.

Each bit in this register is cleared by writing a 1 to the corresponding location in the DMA IntDstTran Interrupt Clear register.

Note: Write access is available to this register or software testing purposes only. Under normal operation, writes to this register are not recommend.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Raw Status for IntDstTran Interrupt. 0x0: Inactive Raw Interrupt Status 0x1: Active Raw Interrupt Status

15.5.2.5 DMA IntErr Interrupt Raw Status register (DMA_RAWERRINTSTS)

Address offset: 0x02E0

Reset value: 0x0000 0000

This register indicates the Raw status for DMA Error interrupt.

Interrupt events are stored in this Raw Interrupt Status register before masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 raw error interrupt.

Each bit in this register is cleared by writing a 1 to the corresponding location in the DMA IntErr Interrupt Clear register.

Note: Write access is available to this register or software testing purposes only. Under normal operation, writes to this register are not recommend.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Raw Status for IntErr Interrupt. 0x0: Inactive Raw Interrupt Status 0x1: Active Raw Interrupt Status

15.5.2.6 DMA IntTfr Interrupt Status register (DMA_TCINTSTS)

Address offset: 0x02E8

Reset value: 0x0000 0000

Channel DMA Transfer complete interrupt event from all channels is stored in this Interrupt Status register after masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 transfer complete interrupt.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								r	r	r	r	r	r	r	r

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Status for IntTfr Interrupt. 0x0: Inactive Interrupt Status 0x1: Active Interrupt Status

15.5.2.7 DMA IntBlock Interrupt Status register (DMA_BTCINTSTS)

Address offset: 0x02F0

Reset value: 0x0000 0000

Channel Block complete interrupt event from all channels is stored in this Interrupt Status register after masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 block transfer complete interrupt.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								r	r	r	r	r	r	r	r

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Status for IntBlock Interrupt. 0x0: Inactive Interrupt Status 0x1: Active Interrupt Status

15.5.2.8 DMA IntSrcTran Interrupt Status register (DMA_STCINTSTS)

Address offset: 0x02F8

Reset value: 0x0000 0000

Channel Source Transaction complete interrupt event from all channels is stored in this Interrupt Status register after masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 status source transaction complete interrupt.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								r	r	r	r	r	r	r	r

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Status for IntSrcTran Interrupt. 0x0: Inactive Interrupt Status 0x1: Active Interrupt Status

15.5.2.9 DMA IntDstTran Interrupt Status register (DMA_DTCINTSTS)

Address offset: 0x0300

Reset value: 0x0000 0000

Channel destination transaction complete interrupt event from all channels is stored in this Interrupt Status register after masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 status destination

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transaction complete interrupt.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								r	r	r	r	r	r	r	r

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Status for IntDstTran Interrupt. 0x0: Inactive Interrupt Status 0x1: Active Interrupt Status

15.5.2.10 DMA IntErr Interrupt Status register (DMA_ERRINTSTS)

Address offset: 0x0308

Reset value: 0x0000 0000

Channel Error interrupt event from all channels is stored in this Interrupt Status register after masking. This register has a bit allocated per channel; for example, bit 2 is the Channel 2 status error interrupt.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								r	r	r	r	r	r	r	r

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Status for IntErr Interrupt. 0x0: Inactive Interrupt Status 0x1: Active Interrupt Status

15.5.2.11 DMA IntTfr Interrupt Mask register (DMA_TCINTMSK)

Address offset: 0x0310

Reset value: 0x0000 0000

The contents of the DMA IntTfr Interrupt Raw Status register is masked with the contents of this Mask register. Each

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Email: sales@nsing.com.sg

bit of register is allocated per channel; for example, bit 2 is the mask bit for the Channel 2 transfer complete interrupt.

A channel CHn bit will be written only if the corresponding mask write enable bit in the CHnWEN field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to this Mask register writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged.

Writing a 1 to any bit in this register unmasks the corresponding interrupt, thus allowing the DMA controller to set the appropriate bit in the Status registers and int_* port signals (Internal interrupt signals).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Interrupt Mask Write Enable. 0x0: Interrupt mask write disable 0x1: Interrupt mask write enable
n	CHn	Channel n IntTfr Interrupt Mask. 0x0: Mask the interrupts 0x1: Unmask the interrupts

15.5.2.12 DMA IntBlock Interrupt Mask register (DMA_BTCINTMSK)

Address offset: 0x0318

Reset value: 0x0000 0000

The contents of the DMA IntBlock Interrupt Raw Status register is masked with the contents of this Mask register. Each bit of register is allocated per channel; for example, bit 2 is the mask bit for the Channel 2 block complete interrupt.

A channel CHn bit will be written only if the corresponding mask write enable bit in the CHnWEN field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to this Mask register writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged.

Writing a 1 to any bit in this register unmasks the corresponding interrupt, thus allowing the DMA controller to set the appropriate bit in the Status registers and int_* port signals (Internal interrupt signals).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Interrupt Mask Write Enable. 0x0: Interrupt mask write disable 0x1: Interrupt mask write enable
n	CHn	Channel n IntBlock Interrupt Mask. 0x0: Mask the interrupts 0x1: Unmask the interrupts

15.5.2.13 DMA IntSrcTran Interrupt Mask register (DMA_STCINTMSK)

Address offset: 0x0320

Reset value: 0x0000 0000

The contents of the DMA IntSrcTran Interrupt Raw Status register is masked with the contents of this Mask register. Each bit of register is allocated per channel; for example, bit 2 is the mask bit for the Channel 2 source transaction complete interrupt.

A channel CHn bit will be written only if the corresponding mask write enable bit in the CHnWEN field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to this Mask register writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged.

Writing a 1 to any bit in this register unmasks the corresponding interrupt, thus allowing the DMA controller to set the appropriate bit in the Status registers and int_* port signals (Internal interrupt signals).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Interrupt Mask Write Enable. 0x0: Interrupt mask write disable

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Bit field	Name	Description
		0x1: Interrupt mask write enable
n	CHn	Channel n IntSrcTran Interrupt Mask. 0x0: Mask the interrupts 0x1: Unmask the interrupts

15.5.2.14 DMA IntDstTran Interrupt Mask register (DMA_DTCINTMSK)

Address offset: 0x0328

Reset value: 0x0000 0000

The contents of the DMA IntDstTran Interrupt Raw Status register is masked with the contents of this Mask register. Each bit of register is allocated per channel; for example, bit 2 is the mask bit for the Channel 2 destination transaction complete interrupt.

A channel CHn bit will be written only if the corresponding mask write enable bit in the CHnWEN field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to this Mask register writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged.

Writing a 1 to any bit in this register unmasks the corresponding interrupt, thus allowing the DMA controller to set the appropriate bit in the Status registers and int_* port signals (Internal interrupt signals).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Interrupt Mask Write Enable. 0x0: Interrupt mask write disable 0x1: Interrupt mask write enable
n	CHn	Channel n IntDstTran Interrupt Mask. 0x0: Mask the interrupts 0x1: Unmask the interrupts

15.5.2.15 DMA IntErr Interrupt Mask register (DMA_ERRINTMSK)

Address offset: 0x0330

Reset value: 0x0000 0000

The contents of the DMA IntErr Interrupt Raw Status register is masked with the contents of this Mask register. Each

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bit of register is allocated per channel; for example, bit 2 is the mask bit for the Channel 2 error interrupt.

A channel CHn bit will be written only if the corresponding mask write enable bit in the CHnWEN field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to this Mask register writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged.

Writing a 1 to any bit in this register unmasks the corresponding interrupt, thus allowing the DMA controller to set the appropriate bit in the Status registers and int_* port signals (Internal interrupt signals).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Interrupt Mask Write Enable. 0x0: Interrupt mask write disable 0x1: Interrupt mask write enable
n	CHn	Channel n IntErr Interrupt Mask. 0x0: Mask the interrupts 0x1: Unmask the interrupts

15.5.2.16 DMA IntTfr Interrupt Clear register (DMA_TCINTCLR)

Address offset: 0x0338

Reset value: 0x0000 0000

Each bit in the DMA IntTfr Interrupt Raw Status register and DMA IntTfr Interrupt Status register is cleared on the same cycle by writing a 1 to the corresponding location in this register. Each bit is allocated per channel; for example, bit 2 is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. This registers are not readable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								w	w	w	w	w	w	w	w

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Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Clear for IntTfr Interrupt. 0x0: No effect 0x1: Clears interrupts

15.5.2.17 DMA IntBlock Interrupt Clear register (DMA_BTCINTCLR)

Address offset: 0x0340

Reset value: 0x0000 0000

Each bit in the DMA IntBlock Interrupt Raw Status register and DMA IntBlock Interrupt Status register is cleared on the same cycle by writing a 1 to the corresponding location in this register. Each bit is allocated per channel; for example, bit 2 is the clear bit for the Channel 2 block done interrupt. Writing a 0 has no effect. This registers are not readable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								w	w	w	w	w	w	w	w

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Clear for IntBlock Interrupt. 0x0: No effect 0x1: Clears interrupts

15.5.2.18 DMA IntSrcTran Interrupt Clear register (DMA_STCINTCLR)

Address offset: 0x0348

Reset value: 0x0000 0000

Each bit in the DMA IntSrcTran Interrupt Raw Status register and DMA IntSrcTran Interrupt Status register is cleared on the same cycle by writing a 1 to the corresponding location in this register. Each bit is allocated per channel; for example, bit 2 is the clear bit for the Channel 2 source transaction complete interrupt. Writing a 0 has no effect. This registers are not readable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								w	w	w	w	w	w	w	w

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Clear for IntSrcTran Interrupt. 0x0: No effect 0x1: Clears interrupts

15.5.2.19 DMA IntDstTran Interrupt Clear register (DMA_DTCINTCLR)

Address offset: 0x0350

Reset value: 0x0000 0000

Each bit in the DMA IntDstTran Interrupt Raw Status register and DMA IntDstTran Interrupt Status register is cleared on the same cycle by writing a 1 to the corresponding location in this register. Each bit is allocated per channel; for example, bit 2 is the clear bit for the Channel 2 destination transaction complete interrupt. Writing a 0 has no effect. This registers are not readable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								w	w	w	w	w	w	w	w

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Clear for IntDstTran Interrupt. 0x0: No effect 0x1: Clears interrupts

15.5.2.20 DMA IntErr Interrupt Clear register (DMA_ERRINTCLR)

Address offset: 0x0358

Reset value: 0x0000 0000

Each bit in the DMA IntErr Interrupt Raw Status register and DMA IntErr Interrupt Status register is cleared on the same cycle by writing a 1 to the corresponding location in this register. Each bit is allocated per channel; for example, bit 2 is the clear bit for the Channel 2 error interrupt. Writing a 0 has no effect. This registers are not readable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
								w	w	w	w	w	w	w	w

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Clear for IntErr Interrupt. 0x0: No effect 0x1: Clears interrupts

15.5.2.21 DMA Interrupt Combined Status register (DMA_INTCBESTS)

Address offset: 0x0360

Reset value: 0x0000 0000

The contents of each of the five Status registers DMA_TCINTSTS, DMA_BTCINTSTS, DMA_STCINTSTS, DMA_DTCINTSTS, DMA_ERRINTSTS is ORed to produce a single bit for each interrupt type in this Combined Status register. This register is read-only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											ERR	DSTT	SRCT	BLOCK	TFR
											r	r	r	r	r

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	ERR	OR of the contents of DMA_ERRINTSTS register. 0x0: OR of the contents of DMA_ERRINTSTS register is 0 0x1: OR of the contents of DMA_ERRINTSTS register is 1
3	DSTT	OR of the contents of DMA_DTCINTSTS register. 0x0: OR of the contents of DMA_DTCINTSTS register is 0 0x1: OR of the contents of DMA_DTCINTSTS register is 1
2	SRCT	OR of the contents of DMA_STCINTSTS register. 0x0: OR of the contents of DMA_STCINTSTS register is 0 0x1: OR of the contents of DMA_STCINTSTS register is 1
1	BLOCK	OR of the contents of DMA_BTCINTSTS register.

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Bit field	Name	Description
		0x0: OR of the contents of DMA_BTCINTSTS register is 0 0x1: OR of the contents of DMA_BTCINTSTS register is 1
0	TFR	OR of the contents of DMA_TCINTSTS register. 0x0: OR of the contents of DMA_TCINTSTS register is 0 0x1: OR of the contents of DMA_TCINTSTS register is 1

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15.5.3 DMA Software Handshake Registers

15.5.3.1 DMA Source Software Transaction Request register (DMA_SRCSWTREQ)

Address offset: 0x0368

Reset value: 0x0000 0000

A bit is assigned for each channel in this register. Bit n is ignored when software handshaking is not enabled for the source of channel n.

A channel CHn bit will be written only if the corresponding channel write enable bit in the CHnWEN field is asserted on the same AHB write transfer, and if the channel is enabled in the DMA Channel Enable register. For example, writing hex 0101 writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged. This allows software to set a bit in this register without performing a read-modified write operation.

The functionality of this register depends on whether the source is a flow control peripheral or not. For a description of when the source is not a flow controller, refer to 15.4.6.4. For a description of when the source is a flow controller, refer to 15.4.7.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Source Software Transaction Request write enable. 0x0: Source request write disable 0x1: Source request write enable
n	CHn	Channel n Source Software Transaction Request. 0x0: Source request is not active 0x1: Source request is active

15.5.3.2 DMA Destination Software Transaction Request register (DMA_DSTSWTREQ)

Address offset: 0x0370

Reset value: 0x0000 0000

A bit is assigned for each channel in this register. Bit n is ignored when software handshaking is not enabled for the destination of channel n.

A channel CHn bit will be written only if the corresponding channel write enable bit in the CHnWEN field is asserted on the same AHB write transfer, and if the channel is enabled in the DMA Channel Enable register.

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The functionality of this register depends on whether the destination is a flow control peripheral or not. For a description of when the destination is not a flow controller, refer to 15.4.6.4. For a description of when the source is a flow controller, refer to 15.4.7.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Destination Software Transaction Request write enable. 0x0: Destination request write disable 0x1: Destination request write enable
n	CHn	Channel n Destination Software Transaction Request. 0x0: Destination request is not active 0x1: Destination request is active

15.5.3.3 DMA Source Single Transaction Request register (DMA_SRCSGTREQ)

Address offset: 0x0378

Reset value: 0x0000 0000

A bit is assigned for each channel in this register. Bit n is ignored when software handshaking is not enabled for the source of channel n.

A channel CHn bit will be written only if the corresponding channel write enable bit in the CHnWEN field is asserted on the same AHB write transfer, and if the channel is enabled in the DMA Channel Enable register.

The functionality of this register depends on whether the source is a flow control peripheral or not. For a description of when the source is not a flow controller, refer to 15.4.6.4. For a description of when the source is a flow controller, refer to 15.4.7.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Source Single Transaction Request write enable. 0x0: Single write disable 0x1: Single write enable
n	CHn	Channel n Source Single Transaction Request. 0x0: Source request is not active 0x1: Source request is active

15.5.3.4 DMA Destination Single Transaction Request register (DMA_DSTSGTREQ)

Address offset: 0x0380

Reset value: 0x0000 0000

A bit is assigned for each channel in this register. Bit n is ignored when software handshaking is not enabled for the destination of channel n.

A channel CHn bit will be written only if the corresponding channel write enable bit in the CHnWEN field is asserted on the same AHB write transfer, and if the channel is enabled in the DMA Channel Enable register.

The functionality of this register depends on whether the destination is a flow control peripheral or not. For a description of when the destination is not a flow controller, refer to 15.4.6.4. For a description of when the source is a flow controller, refer to 15.4.7.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Destination Single Transaction Request write enable. 0x0: Single write disable 0x1: Single write enable
n	CHn	Channel n Destination Single Transaction Request. 0x0: Destination Single or burst request is not active 0x1: Destination Single or burst request is active

15.5.3.5 DMA Source Last Transaction Request register (DMA_SRCLTREQ)

Address offset: 0x0388

Reset value: 0x0000 0000

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A bit is assigned for each channel in this register. Bit n is ignored when software handshaking is not enabled for the source of channel n, or when the source of channel n is not a flow controller.

A channel CHn bit will be written only if the corresponding channel write enable bit in the CHnWEN field is asserted on the same AHB write transfer, and if the channel is enabled in the DMA Channel Enable register.

For a description of this register, refer to 15.4.7.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Source Last Transaction Request write enable. 0x0: Source last transaction request write disable 0x1: Source last transaction request write enable
n	CHn	Channel n Source Last Transaction Request. 0x0: Not last transaction in current block 0x1: Last transaction in current block

15.5.3.6 DMA Destination Last Transaction Request register (DMA_DSTLTREQ)

Address offset: 0x0390

Reset value: 0x0000 0000

A bit is assigned for each channel in this register. Bit n is ignored when software handshaking is not enabled for the destination of channel n, or when the destination of channel n is not a flow controller.

A channel CHn bit will be written only if the corresponding channel write enable bit in the CHnWEN field is asserted on the same AHB write transfer, and if the channel is enabled in the DMA Channel Enable register.

For a description of this register, refer to 15.4.7.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Destination Last Transaction Request write enable. 0x0: Destination last transaction request write disable 0x1: Destination last transaction request write enable
n	CHn	Channel n Destination Last Transaction Request. 0x0: Not last transaction in current block 0x1: Last transaction in current block

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15.5.4 DMA Miscellaneous Registers

15.5.4.1 DMA Configuration register (DMA_CFG)

Address offset: 0x0398

Reset value: 0x0000 0000

This register is used to enable the DMA, which must be done before any channel activity can begin.

If the global channel enable bit is cleared while any channel is still active, then EN field still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the EN bit returns 0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EN	DMA Enable bit. 0x0: DMA Disabled 0x1: DMA Enabled

15.5.4.2 DMA Channel Enable register (DMA_CHEN)

Address offset: 0x03A0

Reset value: 0x0000 0000

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive; it can then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the global DMA channel enable bit, DMA Configuration register's bit 0, is 0. When the global channel enable bit is 0, then a write to this register is ignored and a read will always read back 0.

The channel enable bit, CHn, is written only if the corresponding channel write enable bit, CHnWEN, is asserted on the same AHB write transfer. For example, writing hex 01x1 writes a 1 into bit 0, while bits [7:1] remains unchanged. Writing hex 00xx leaves bits [7:0] unchanged. Note that a read-modified write is not required.

For information on software disabling a channel by writing 0 to CHn field, see 15.4.18.7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
w	w	w	w	w	w	w	w	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
n + 8	CHnWEN	Channel n Enable bit write enable. 0x0: Channel Enable bit write disable 0x1: Channel Enable bit write enable
n	CHn	Channel n Enable. This bit is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. 0x0: Not last transaction in current block 0x1: Last transaction in current block

15.5.4.3 DMA ID register (DMA_ID)

Address offset: 0x03A8

Reset value: 0x0000 0000

This is the DMA ID register, which is a read-only register that reads back the hardcoded module ID number.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VALUE[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE[15:0]															
r															

Bit field	Name	Description
31:0	VALUE	Hardcoded DMA peripheral ID.

15.5.4.4 DMA Test register (DMA_TEST)

Address offset: 0x03B0

Reset value: 0x0000 0000

This register is used to put the AHB slave interface into test mode, during which the readback value of the writable registers match the value written, assuming the DMA configuration has not optimized the same registers. In normal

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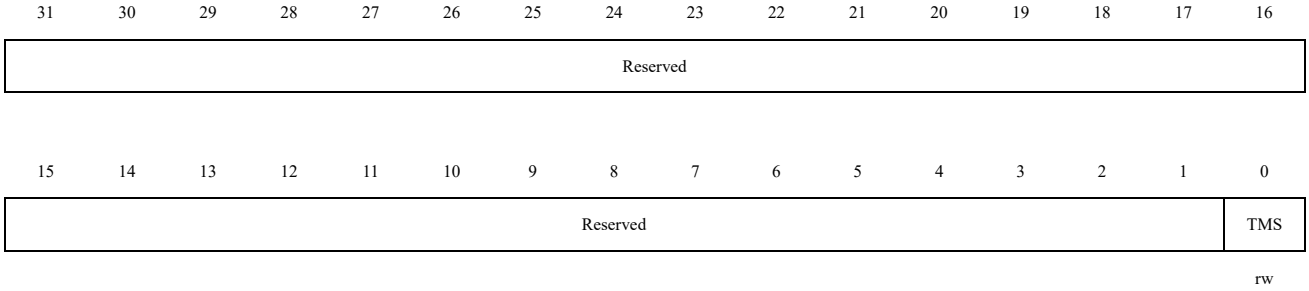
operation, the readback value of some registers is a function of the DMA state and does not match the value written.



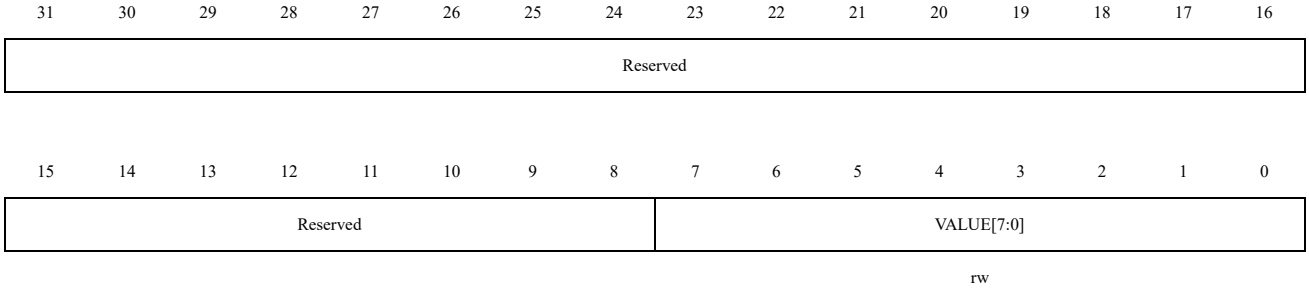
Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	TMS	Test Mode Select. 0x0: Puts the AHB slave interface into Normal mode. 0x1: Puts the AHB slave interface into Test mode. In this mode, the readback value of the writable registers always matches the values written.

15.5.4.5 DMA Low Power Timeout register (DMA_LPTIMEOUT)

Address offset: 0x03B8

Reset value: 0x0000 0008

This register holds the timeout value of Low Power Counter. The final programmed value (or the default reset value if not programmed) determines what is the timeout value the of low power counter.



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	VALUE	This field holds timeout value of low power counter register.

15.5.4.6 DMA Component ID register (DMA_COMPID)

Address offset: 0x03F8

Reset value: 0x3232 332A 4457 1110

This is the DMA Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

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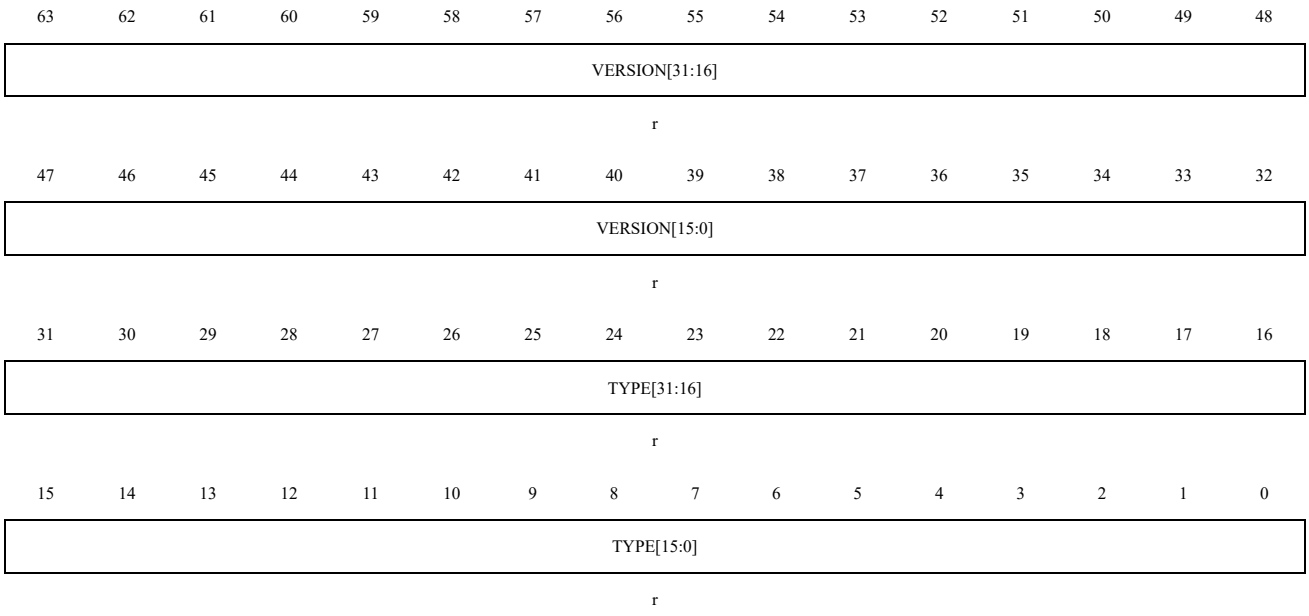

Bit field	Name	Description
63:32	VERSION	DMA Component Version.
31:0	TYPE	DMA Component Type.

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16 MDMA Controller

16.1 Introduction

This chapter provides a basic overview of the MDMA, which is a highly configurable, highly programmable, high performance, multi-master multi-channel DMA Controller with AXI as the bus interface for data transfer.

16.2 Main Features

The MDMA includes the following features:

General Features

- Independent core, slave interface and master interface clocks
- 16 channels, one per source and destination pair
- Data transfers in one direction only (each channel is unidirectional)
- 2 AXI master interfaces: 1 for Accessing TCM, 1 for Accessing other Memory
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- AMBA 4 AXI-compliant master interface
- AHB slave interface for programming the DMA controller
  - AHB slave interface supports only SINGLE transfers (hburst= 3'b000)
- 64 bits AXI master data bus width
- Multiple levels of DMA transfer hierarchy

  DMA transfer split into transaction, block, and complete DMA transfer levels
- Support for AXI unaligned transfers

Channel Buffering

- Single FIFO per channel
- Automatic packing/unpacking of data to fit FIFO width

Channel Control

- Programmable transfer type for each channel (memory-to-memory, memory-to-peripheral, peripheral-to-memory and peripheral-to-peripheral)
- Single or multiple DMA transactions
- Programmable multiple transaction size for each channel
- Programmable maximum AMBA burst transfer size for each channel
- Channel disabling without data loss
- Channel suspend and resume

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- Programmable channel priority
- Programmable multi-block transfer using linked list, contiguous address, and auto reload methods
- Dynamic extension of linked list
- Independent configuration of SRC/DST multi-block transfer type
- Multiple state machines, one for each channel SRC and DST
- Separate state machines for data and LLI access
- Control signals, such as cache and protection, programmable per DMA block
- Programmable transfer length (block length)
- Error status register to ease debugging during error events

Flow Control

- Programmable flow control at DMA transfer level
  - If the size of the block transfer is known prior to DMA initialization, the DMA controller is a flow controller at the DMA block transfer level
  - If the size of the DMA block transfer is unknown prior to the DMA initialization, either source or destination peripheral is the flow controller for undefined length (demand mode) DMA block transfers

Trigger from DMA1~3

- The MDMA can be configured to do transactions based on triggers from DMA1~3 interrupt through DMAMUX. Please refer to the DMAMUX section

Handshaking Interface

- Programmable software and hardware handshaking interfaces for non-memory peripherals
- 16 hardware handshaking interfaces/peripherals
- Enabling/disabling of individual handshake interfaces Programmable mapping between peripherals and channels; many-to-one mapping with only one peripheral active at a time
- Memory mapped registers to control DMA transfer in software handshaking mode

Interrupt Outputs

- Combined and separate interrupt outputs
- Interrupt generation on
  - DMA transfer completion
  - Block transfer completion
  - Single or multiple transaction completion
  - Error condition
  - Channel suspend or disable

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- Interrupt enabling and masking

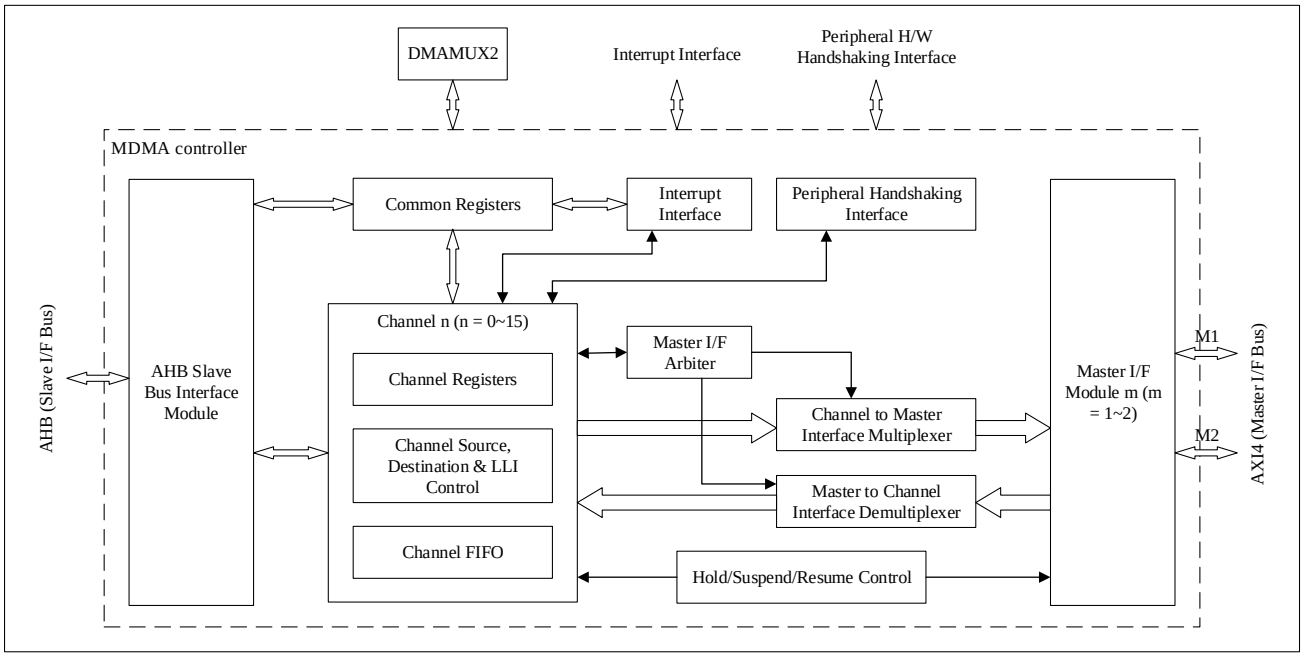
Bus Interface

- AMBA 4 AXI protocols for master interface and AHB protocols for slave interface
- Data bus width 64 bits for master interface
- Outstanding transactions on master interface
- Setting outstanding transaction limit per channel on the master interface
- Out-of-order transaction support for different channels connected on same master interface Transactions of a particular channel are always initiated in order
- Increment and fixed address transfers on master interface
- Source and destination data transfer addresses; must be aligned to respective transfer widths
- Data bus width of 32 bits for slave interface
- Transfer size (width) used for slave interface; must be same as data bus width

16.3 Block Diagram

The below figure shows the following functional groupings of the main interfaces to the MDMA block:

Figure 16-1 MDMA Block Diagram



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16.4 Function Description

16.4.1 Basic Definitions

The following terms are concise definitions of the MDMA concepts used throughout this section:

Source peripheral – Device on an AXI layer from which the MDMA controller reads data. The MDMA controller then stores the data in the channel FIFO. The source peripheral teams up with a destination peripheral to form a channel.

Destination peripheral – Device to which the MDMA controller writes the stored data from the FIFO (data is previously read from the source peripheral).

Memory – Source or destination that is always ready for a DMA transfer and does not require a handshaking interface to interact with the MDMA controller.

Channel – Read/write data path between a source peripheral on one configured AXI layer and a destination peripheral on the same or a different AXI layer that occurs through the channel FIFO. If the source peripheral is not memory, then a source handshaking interface is assigned to the channel. If the destination peripheral is not memory, then a destination handshaking interface is assigned to the channel. Source and destination handshaking interfaces can be assigned dynamically by programming the channel registers.

Master interface – MDMA controller is a master on the AXI bus, reading data from the source and writing it to the destination over the AXI bus. It is possible to have up to two master interfaces, so that up to two independent source and destination channels can operate simultaneously. Each channel has to arbitrate for the master interface. If the source and destination peripherals reside on different AXI layers, there must be multiple master interfaces.

Slave interface – The AHB interface over which the MDMA controller is programmed. The slave interface can be on the same layer as any of the master interfaces, or it can be on a separate layer.

Handshaking interface – A set of signals or software registers that conform to a protocol to perform a handshake between the MDMA controller and the source or destination peripheral. A handshake helps to control the transfer of a single or burst transaction between the MDMA controller and the peripheral. This interface is used to request, acknowledge, and control a MDMA transaction. A channel can receive a request through one of two types of handshaking interface: hardware or software.

- **Hardware handshaking interface** – Uses hardware signals to control the transfer of a single or burst transaction between the MDMA controller and the source or destination peripheral. The simple use of the hardware handshaking interface is when the interrupt line from the peripheral is tied to the “dma_req” input of the hardware handshaking interface; other interface signals are ignored.
- **Software handshaking interface** – Uses software registers to control transferring a single or burst transaction between the MDMA controller and the source or destination peripheral. In this mode, no special MDMA handshaking signals are needed on the I/O of the peripheral. This mode is useful for interfacing an existing peripheral to the MDMA controller without modifying it.

Flow controller – Device (either the MDMA controller, or a source or destination peripheral) that determines the length of a DMA block transfer and terminates it. If the length of a block is known before enabling the channel, then

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the MDMA controller should be programmed as the flow controller. If the length of a block is not known prior to enabling the channel, the source or destination peripheral should terminate the block transfer. In this mode, the peripheral (source/destination) is the flow controller.

Transfer hierarchy – Transfers are split into a maximum of four levels: DMA transfer level, block transfer level, transaction level, and AXI transfer level. This is done to minimize the effect of the scenario where the channel is granted to a particular set of peripherals, but a peripheral does not have enough data to transfer continuously. In such a scenario, the channel can not be given to any other peripheral, which reduces the performance.

Figure 16-2 illustrates the hierarchy between DMA transfers, block transfers, transactions (single or burst), and AMBA AXI transfers (single or burst) for non-memory peripherals.

Figure 16-3 illustrates the hierarchy between DMA transfers, block transfers, and AMBA AXI transfers (single or burst) for memory peripherals.

Note: There is no transaction level for memory peripherals, as a memory is assumed to be always ready for data transfer.

Figure 16-2 Transfer Hierarchy for Non-Memory Peripherals

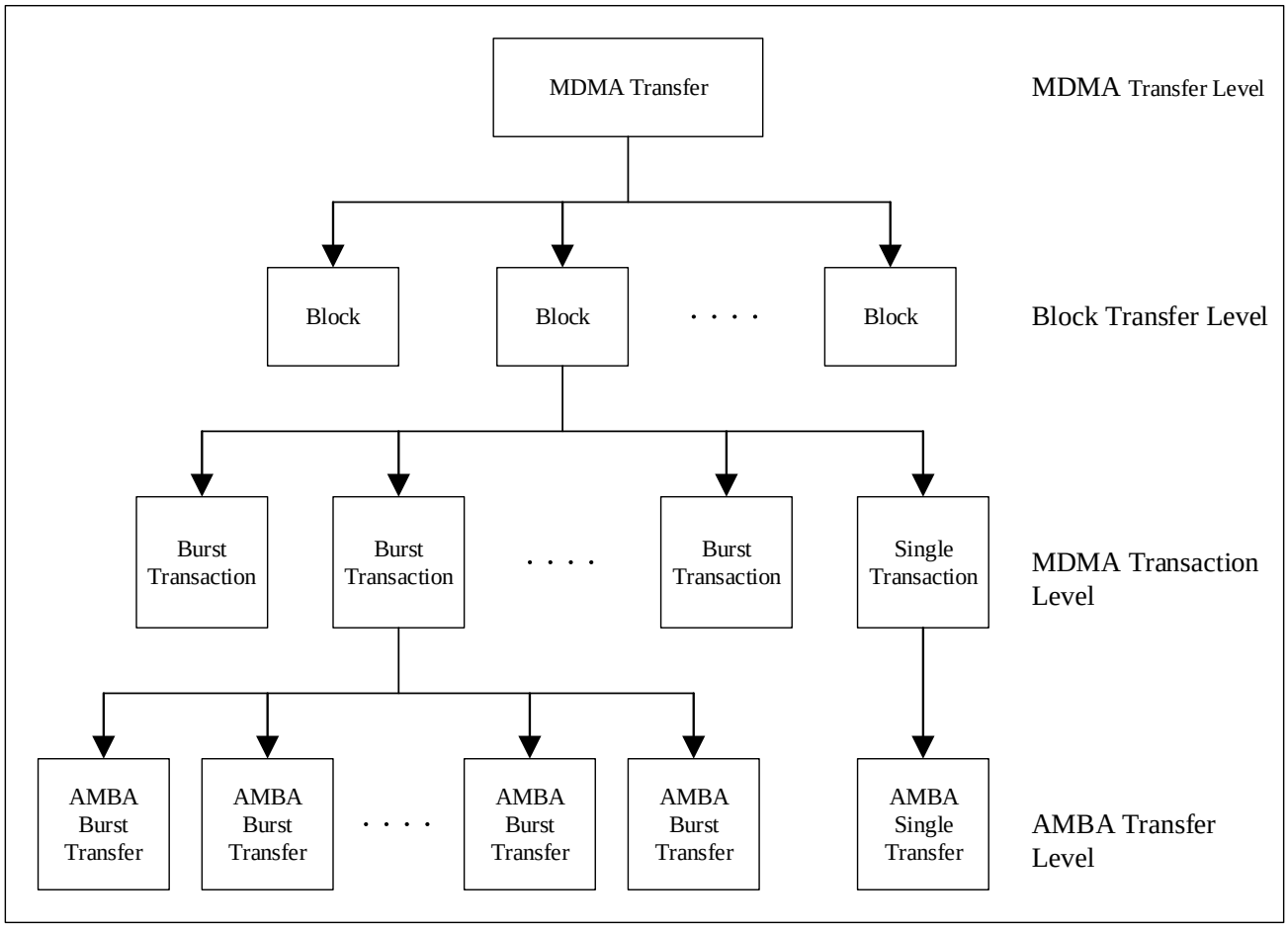

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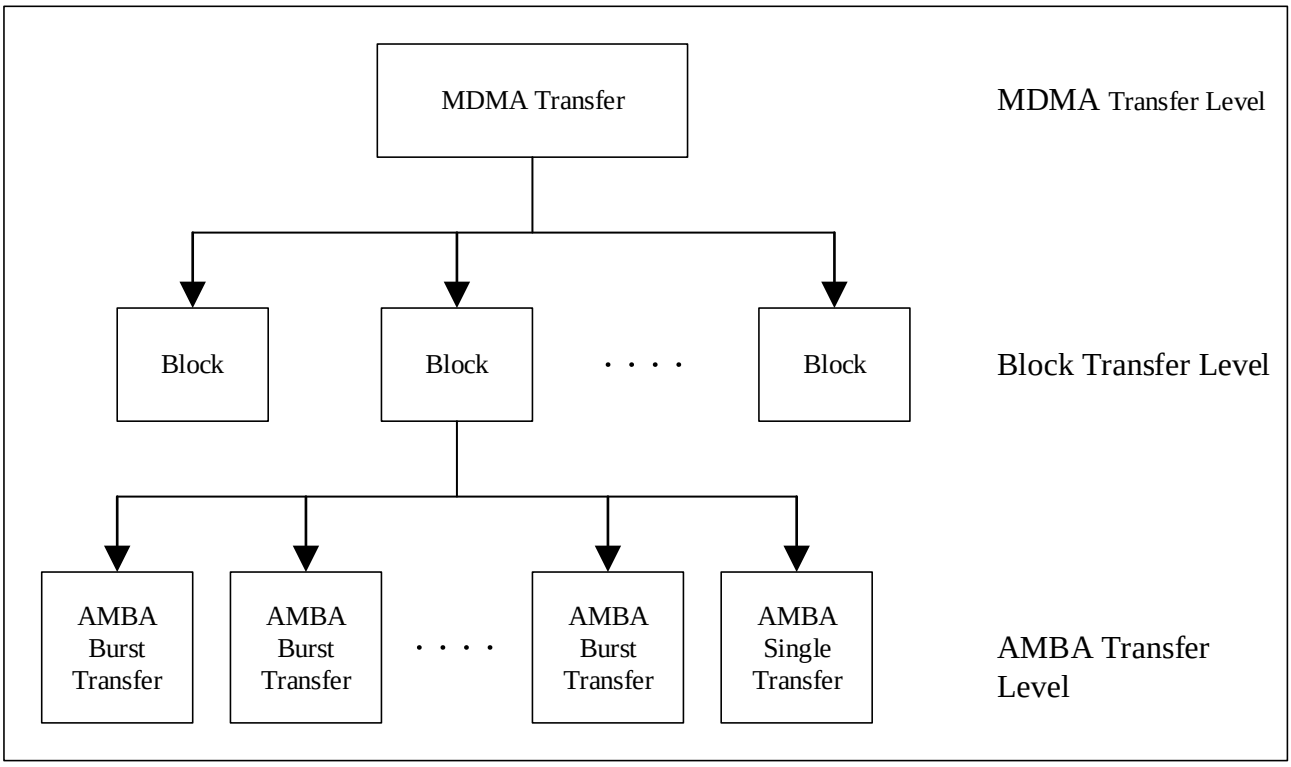
Figure 16-3 Transfer Hierarchy for Memory



Transaction – Basic unit of a MDMA transfer, as determined by either the hardware or the software handshaking interface. A transaction is relevant only for transfers between the MDMA controller and a source or destination peripheral if the peripheral is a non-memory device. There are two types of transactions:

- **Single transaction** – Length of a single transaction is always 1 and it is converted to an INCR AXI transfer of burst length 1.
- **Burst transaction** – Length of a burst transaction is programmed into the MDMA controller. A burst transaction is converted into a sequence of AXI burst transfers. The burst transaction length is under program control and normally bears some relationship to the FIFO sizes in the MDMA controller and in the source and destination peripherals.

Block – A block of MDMA data, the amount of which is the block length and is determined by the flow controller. For transfers between the MDMA controller and memory, a block is broken directly into a sequence of burst transfers. For transfers between the MDMA controller and a non-memory peripheral, a block is broken into a sequence of MDMA transactions. These are in turn broken into a sequence of AXI transfers.

DMA transfer – Software controls the number of blocks in a MDMA transfer. Once the DMA transfer has completed, the hardware within the MDMA controller disables the channel and can generate an interrupt to signal the DMA transfer completion. The channel can then be reprogrammed for a new DMA transfer.

- **Single-block DMA transfer** – Consists of a single block.
- **Multi-block DMA transfer** – A DMA transfer may consist of multiple DMA blocks. Multi-block DMA transfers are supported through block chaining (linked list pointers), auto-reloading of channel registers, and contiguous blocks. The source and destination can independently select which method to use.

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- **Linked lists (block chaining)** – A linked list pointer (LLP) points to the location in system memory where the next linked list item (LLI) exists. The LLI is a set of registers that describes the next block (block descriptor) and an LLP register. The MDMA controller fetches the LLI at the beginning of every block when block chaining is enabled. LLI access always uses the burst size (arsize/awsize) that is the same as the data bus width and cannot be changed or programmed to anything other than this. Burst length (awlen/arlen) is chosen based on the data bus width so that the access does not cross one complete LLI structure of 64 bytes.

  MDMA controller fetches the entire LLI (40 bytes) in one AXI burst, if the burst length is not limited by other settings.

- **Auto-reloading** – MDMA controller automatically reloads the channel registers at the end of each block to the value that was set when the channel was first enabled.

- **Contiguous blocks** – Address between successive blocks is selected to be a continuation from the end of the previous block.

Channel locking – Software can program a channel to keep the AXI master interface by locking arbitration of the master bus interface for the duration of a DMA transfer, block transfer, or transaction (single or burst).

16.4.2 Clocks and Resets

MDMA main reset is from RCC module. Please refer to RCC documentation for more details.

MDMA also supports a soft reset, which is set using the RSTREQ field in the MDMA_SWRST register. The soft reset procedure is as follows.

1 Software writes 1 to the RSTREQ bit to reset the MDMA. Software polls the RSTREQ bit until it is seen as 0, which confirms the reset.

  MDMA resets all the modules in different clock domains except for the slave bus interface module.

2 The Slave bus interface module is not reset because software is polling the RSTREQ field.

3 MDMA clears the RSTREQ bit to 0.

Note: Software is not allowed to write 0 to the RSTREQ field. A reset does not guarantee the completion of the data transfer for ongoing or posted requests. If a reset is asserted in between transfers, it might result in AXI protocol violations.

16.4.3 Slave Bus Interface

Slave Bus Interface Module implements the logic to access the internal registers of MDMA by an external AHB Master. This module support only the little-endian scheme for data transfer.

The AHB Slave Bus Interface can be used to perform the read or write operations to the Common Register (see 16.5.1) and Channel Register (see 16.5.2) space. While performing the read or write transfers, the Slave Bus Interface might provide the slave interface access errors and read/write transactions might fail because of any of the following reasons:

- Decode Access Errors
- Write to Read-Only Register Access Error

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- Read to Write-Only Register Error
- Write-on-Hold Error
- Undefined Address Access Error

The AHB Slave bus interface supports a 32-bit data bus width. This Slave bus interface supports only single AHB transfer.

16.4.4 Master Bus Interface

The master interface implements the transfer of data on the AXI bus. The AXI protocol is AXI4. MDMA supports a maximum of two master interfaces, which operate independently to transfer data between peripherals and memories. Both master interfaces use the same AXI protocol. Address and Data bus widths of master interfaces are 32-bit and 64-bit respectively, but both master interfaces use the same configuration.

The master interface implements all five channels specified in the AXI protocol:

- Write address
- Write data
- Write response
- Read address
- Read data

The master interface implements different FIFOs for temporary storage of data transferred between external memories or peripherals through different channels in MDMA controller.

MDMA supports a maximum of 16 channels, which can be assigned to either of the master interfaces, based on a well-defined, programmable arbitration scheme for accessing the master interface.

Apart from channel source and destination peripherals, LLI fetch and LLI write-back operations also need access to the master interface. MDMA controller implements a programmable arbitration scheme which is explained in the following section.

16.4.5 Arbitration Scheme

DMA transfers can be split into the following transfer hierarchy levels:

- Transaction level (only applicable for non-memory peripherals)
- Block level
- Complete DMA transfer level
- AXI transfer level

MDMA controller implements a dynamic priority and fair-among-equals arbitration scheme, with options for channel locking at different DMA transfer hierarchy levels.

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The number of priority levels available is the same as the number of enabled channels and the priority value is programmable for each channel in the Channel Configuration register. Multiple channels can be given the same priority level, however, some priority levels remain unused. A priority of 15 is the highest priority, and 0 is the lowest.

Dynamic priority and fair-among-equals arbitration is a two-tier arbitration scheme which works as follows:

- The first-tier arbitration uses the priority inputs of the requests and decides which one of the requesting clients is issued the grant signal. The request with the highest priority is granted access to the AXI channel on the master interface.
- If two or more requests to the arbiter have the same programmed priority value, the second-tier arbitration, based on the fair-among-equals scheme, is used. In this scheme, the grant is issued fairly among actively requesting clients with the same priority level.

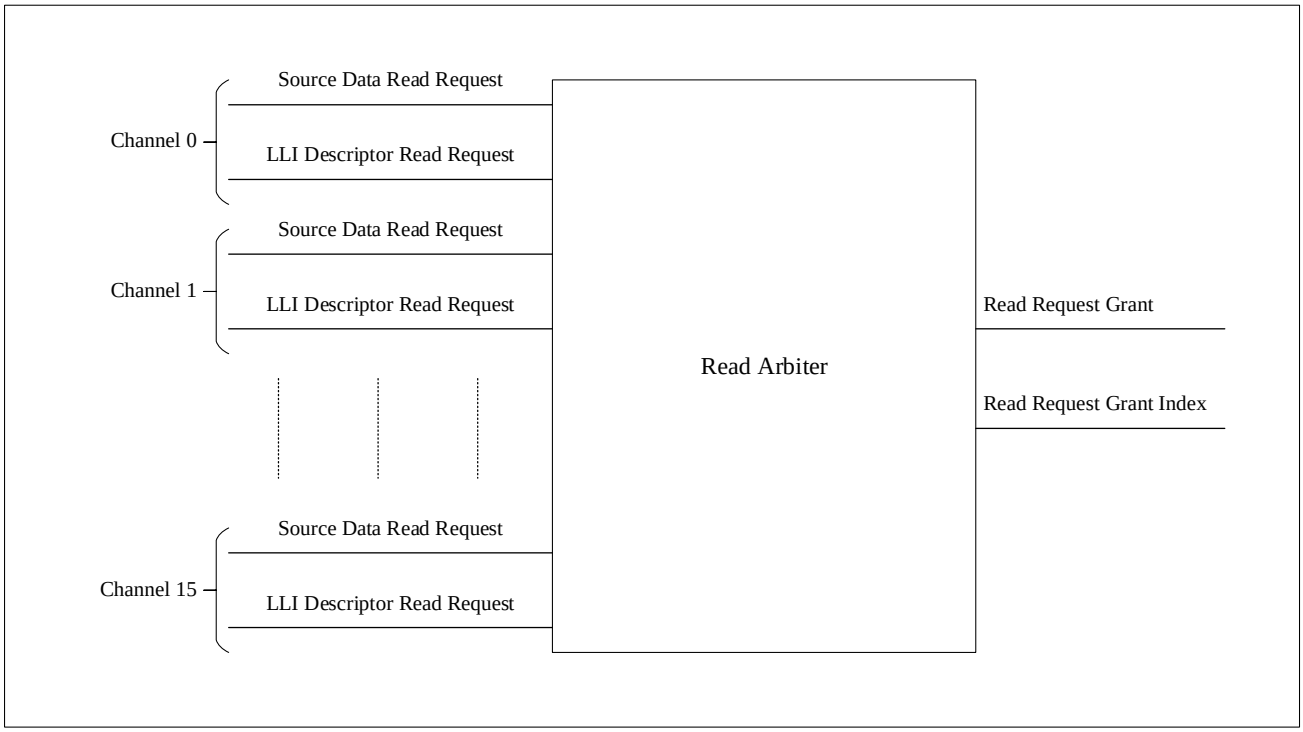
16.4.5.1 Single Arbiter Scheme

In Single Arbiter scheme, the arbitration of the read requests from source, destination, and LLI state machine is performed by using the Single Arbiter. The read requests from a channel to the arbiter consists of the following requests:

- Source Data Read Request
- LLI Descriptor Read Request

The Single arbiter scheme performs the arbitration between these read requests from all channels based on the Dynamic priority (first-tier arbitration) and fair-among-equals (second-tier arbitration) scheme described in 16.4.5. The granted read request gets the access to the AXI Master Interface. The block diagram of the Single Arbiter Scheme - Read Arbiter is as shown in Figure 16-4.

Figure 16-4 Single Arbiter Scheme - Read Arbiter



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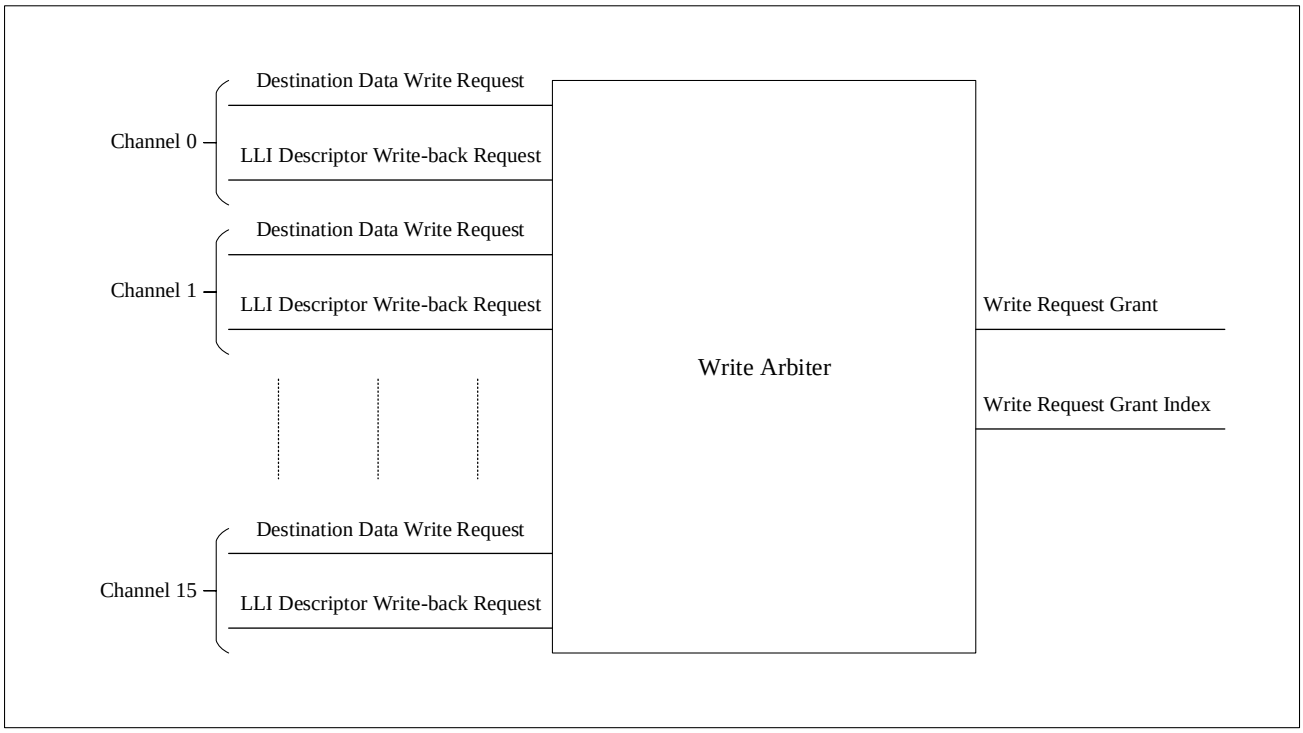
Similarly, the arbitration of write requests from destination and LLI state machine is performed using the Single Arbiter. The write requests from a channel to arbiter consists of the following:

- Destination Data Write Request
- LLI Descriptor Write-Back Request

The Single arbiter scheme performs the arbitration between these write requests from all channels based on the Dynamic priority (first-tier arbitration) and fair-among-equals (second-tier arbitration) scheme. The granted write request gets the access to the AXI Master Interface. The block diagram of the Single Arbiter Scheme – Write Arbiter is as shown in Figure 16-5.

Figure 16-5 Single Arbiter Scheme - Write Arbiter



16.4.5.2 Multi-Arbiter Scheme

To meet higher QoR (timing) requirement (if required) - the Multi-Arbiter Scheme is introduced. This Multi-Arbiter scheme uses the two-stage arbitration architecture.

The first-stage has multiple arbiters with each having up to eight Channels related to read or write requests with registered grant outputs. For the definition of read or write requests for a channel, see 16.4.5.1. The second-stage has single arbiter with grant outputs from each of the first-stage arbiter as request input to the second-stage arbiter. The grant output of the second-stage arbiter is not registered. The Multi-Arbiter scheme splits the single arbiter into multiple smaller arbiters as shown in Figure 16-6 and Figure 16-7. This helps in improving the overall QoR of the MDMA.

The block diagram of Multi-Arbiter Scheme - Read Arbiter is as shown in Figure 16-6. Each of the Read Arbiter arbitrates using Dynamic priority (first-tier arbitration) and fair-among-equals (second-tier arbitration) scheme at the individual arbiter level.

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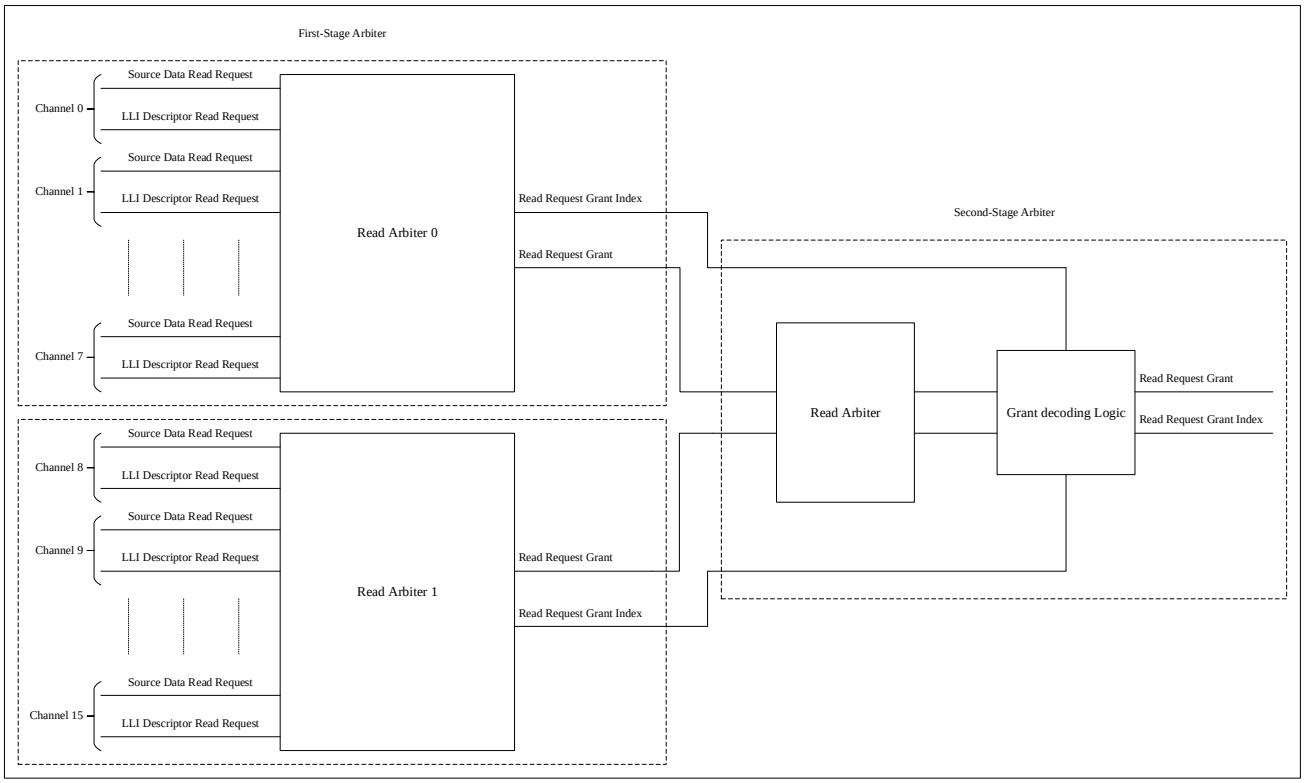
Figure 16-6 Multi-Arbiter Scheme - Read Arbiter



The block diagram of Multi-Arbiter Scheme – Write Arbiter is as shown in Figure 16-7. Each of the Write Arbiter arbitrates using Dynamic priority (first-tier arbitration) and fair-among-equals (second-tier arbitration) scheme at the individual arbiter level.

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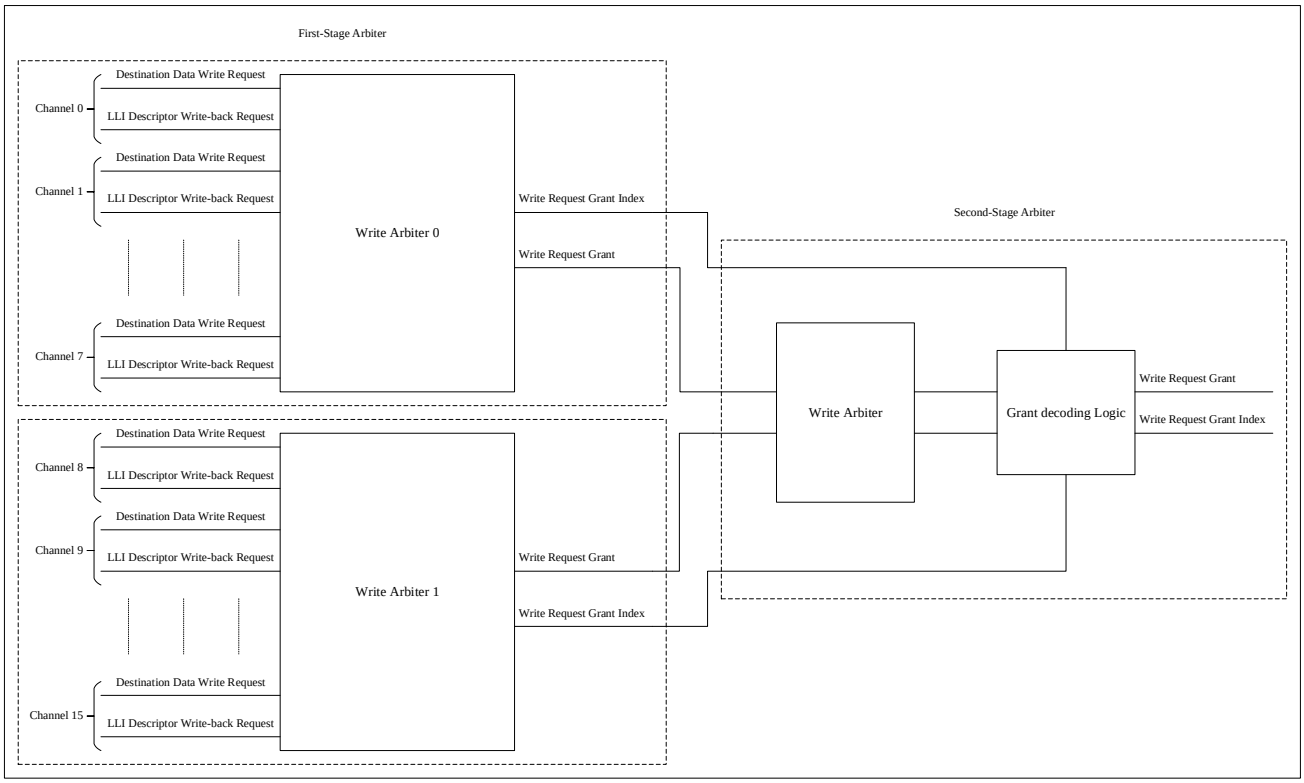
Figure 16-7 Multi-Arbiter Scheme - Write Arbiter



16.4.5.3 Locks and Grants

The lock input of the arbiter enables a request, despite other requests, to be given an exclusive grant for the duration of the corresponding lock input. After a client receives the grant, it can lock out other clients from the arbitration process by setting the corresponding lock input.

MDMA design allows a channel to be locked to the arbiter at the transaction (only applicable for non-memory peripherals), block, or complete DMA transfer level. By default, MDMA controller locks the arbiter for one complete AXI transfer. If channel locking is enabled at a higher level – for a transaction, block, or complete DMA transfer – the channel that locked the arbiter gets access to the master interface until the end of locking period, and requests from other channels during this time are ignored.

16.4.5.4 Priority for Different Accesses

If the source, destination, and linked list peripherals of different channels with the same priority value are connected on the same master interface, the priority for different accesses are as follows:

- For AXI Read Channel

  Linked List fetch > Source Data Transfer

- For AXI Write Channel

  Destination Data Transfer > Linked List Write-back

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16.4.5.5 Same Channel Transfer, Fetch and Access

Source data transfer, destination data transfer, linked list fetch, and linked list status write back access for a particular channel generally happens sequentially as follows:

Linked list fetch > Source data transfer and destination data transfer > linked list write back.

There is no need for arbitration between different accesses in this case.

16.4.6 Single Transaction Region

In certain cases, a DMA block transfer cannot complete using only burst transactions. Typically this occurs when the block size is not a multiple of the burst transaction length. In these cases, the block transfer uses burst transactions up to the point where the amount of data left to complete the block is less than the amount of data in a burst transaction. At this point, the MDMA controller samples the dma_single status flag and completes the block transfer using single transactions. The peripheral asserts a single status flag to indicate to the MDMA controller that there is enough data or space to complete a single transaction from or to the source or destination peripheral.

For hardware handshaking, the single status flag is a signal on the hardware handshaking interface. For software handshaking, the single status flag is one bit in the software handshaking interface register.

The single transaction region is the time interval where the MDMA controller uses single transactions to complete the block transfer; burst transactions are used only outside this region.

The following terms are used for explaining single transaction region.

- Source single transaction size in bytes:

  src_single_size_bytes = MDMA_CHnCTRL.STW / 8

- Source burst transaction size in bytes:

  src_burst_size_bytes = MDMA_CHnCTRL.SRCMSIZE * *src_single_size_bytes*

- Destination single transaction size in bytes:

  dst_single_size_bytes = MDMA_CHnCTRL.DTW / 8

- Destination burst transaction size in bytes:

  dst_burst_size_bytes = MDMA_CHnCTRL.DSTMSIZE * *dst_single_size_bytes*

- Block size in bytes:

  - If MDMA is flow controller

    With the MDMA as the flow controller, the processor programs the MDMA with the number of data items (block size) of source transfer width (MDMA_CHnCTRL.STW) to be transferred by the MDMA in a block transfer; this is programmed into the MDMA_CHnBTS.NUM field. Therefore, the total number of bytes to be transferred in a block is:

    blk_size_bytes_dma = MDMA_CHnBTS.NUM * *src_single_size_bytes*

  - If source peripheral is flow controller

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blk_size_bytes_src = (Number of source burst transactions in block * *src_burst_size_bytes*) + (Number of source single transactions in block * *src_single_size_bytes*)

- If destination peripheral is block flow controller

  blk_size_bytes_dst = (Number of destination burst transactions in block * *dst_burst_size_bytes*) + (Number of destination single transactions in block * *dst_single_size_bytes*)

The single transaction region applies only to a peripheral that is not the flow controller. The precise definition of when this region is entered depends on what acts as the flow controller.

- If the MDMA controller is the flow controller:
  - The source peripheral enters the single transaction region when the number of bytes left to complete in the source block transfer is less than *src_burst_size_bytes*.

    If *blk_size_bytes_dma* / *src_burst_size_bytes* is an integer, then the source peripheral never enters this region, and the source block transfer uses only burst transactions.
  - The destination peripheral enters the single transaction region when the number of bytes left to complete in the destination block transfer is less than *dst_burst_size_bytes*.

    If *blk_size_bytes_dma* / *dst_burst_size_bytes* is an integer, then the destination peripheral never enters this region, and the destination block transfer uses only burst transactions.
- If either the source or the destination peripheral is the flow controller:
  - Single transaction region is not applicable for the flow controller peripheral.
  - If the source peripheral is the flow controller, the destination peripheral enters the single transaction region when the flow control peripheral (that is, the source peripheral) signals the last transaction in the block and when the amount of data left to be transferred in the destination block is less than the value specified by *dst_burst_size_bytes*.
  - If the destination peripheral is the flow controller, the source peripheral enters the single transaction region when the flow control peripheral (that is, the destination peripheral) signals the last transaction in the block and when the amount of data left to be transferred in the source block is less than the value specified by *src_burst_size_bytes*.

Note: If a peripheral is not the flow controller, MDMA controller ignores dma_single input outside the single transaction region.

16.4.7 Handshaking Interface

Handshaking interfaces are used at the transaction level to control the flow of single or burst transactions. The operation of the handshaking interface depends on whether the peripheral or the MDMA controller is the flow controller. The peripheral uses the handshaking interface to indicate to the MDMA controller that it is ready to transfer or accept data over the AXI bus.

MDMA supports a maximum of 16 hardware handshaking interfaces. The type of handshaking interface used (software or hardware) is independently programmable for each channel source and destination in the Channel

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Configuration register. Software handshaking is accomplished through memory-mapped registers, while hardware handshaking is accomplished using a dedicated handshaking interface.

16.4.7.1 Hardware Handshaking

The following set of I/O signals are used for hardware handshaking.

dma_req – Burst transaction request input from peripheral. The functionality of this signal depends on whether the peripheral is the flow controller or not.

- **If peripheral is not flow controller** – The MDMA controller always interprets the dma_req signal as a burst transaction request, regardless of the level of dma_single. Once dma_req is asserted, it must remain asserted until dma_ack is asserted. When the peripheral that is driving dma_req determines that dma_ack is asserted, it must de-assert dma_req. If an active level on dma_req is detected in the single transaction region, then the block transfer is completed using an early terminated burst transaction.
- **If peripheral is flow controller** – An active level on dma_req initiates a transaction request. The type of transaction (whether single or burst) is qualified by the dma_single input. Once dma_req is asserted, it must remain asserted until dma_ack is asserted. When the peripheral that is driving dma_req determines that "dma_ack" is asserted, it must de-assert dma_req.

dma_single – Single transaction request input from peripheral. The functionality of this signal depends on whether the peripheral is the flow controller or not.

- **If peripheral is not flow controller** – The dma_single signal is a status signal that is asserted by a source or destination peripheral when it can transmit or accept at least one source or destination data item; otherwise it is cleared. This signal is sampled by the MDMA controller only in the single transaction region of the block transfer. Outside this region, dma_single is ignored and all transactions are burst transactions, which means MDMA controller waits for dma_req to be asserted. Once dma_single is asserted, it must remain asserted until dma_ack is asserted. When the peripheral that is driving dma_single determines that dma_ack is asserted, it must de-assert dma_single.
- **If peripheral is flow controller** – The dma_single signal is asserted by a source or destination peripheral to request a single transaction. If dma_single is asserted in the same clock cycle as dma_req is asserted, a single transaction is requested by the peripheral. If dma_single is deasserted, the peripheral is requesting a burst transaction. Once dma_single is asserted, it must remain asserted until dma_ack is asserted. When the peripheral that is driving dma_single determines that dma_ack is asserted, it must de-assert dma_single.

dma_last – The last transaction in a block request from a peripheral. The functionality of this signal depends on whether the peripheral is the flow controller or not.

- **If peripheral is not flow controller** – The dma_last signal is not relevant and it is ignored.
- **If peripheral is flow controller** – The peripheral asserts dma_last on the same cycle as dma_req is asserted in order to signal that this transaction request is the last in the block and the block transfer is complete after this transaction is complete. If dma_single is high in the same cycle as dma_last (and dma_req) is asserted, the last transaction is a single transaction. If dma_single is low in the same cycle as dma_last (and dma_req) is asserted, the last transaction is a burst transaction. Once dma_last is asserted, it must remain asserted until dma_ack is asserted. When the peripheral that is driving dma_last determines that dma_ack is asserted, it must de-assert dma_last.

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dma_ack – MDMA acknowledges signal output to the peripheral. The functionality of this signal depends on whether the peripheral is the flow controller or not.

- **If peripheral is not flow controller** – The dma_ack signal is asserted after the last AXI data transfer in the current transaction (single or burst) to the peripheral has completed. For a single transaction, dma_ack remains asserted until the peripheral de-asserts dma_single (that is, dma_ack is de-asserted one dmac_core_clock cycle after the de-assertion of dma_single). For a burst transaction, dma_ack remains asserted until the peripheral de-asserts dma_req (that is, dma_ack is de-asserted one dmac_core_clock cycle after the de-assertion of dma_req).
- **If peripheral is flow controller** – The dma_ack signal is asserted after the last AXI data transfer in the current transaction (single or burst) to the peripheral has completed. It forms a handshaking loop with dma_req and remains asserted until the peripheral de-asserts dma_req (that is, dma_ack is de-asserted one dmac_core_clock cycle after the de-assertion of dma_req).

dma_finish – This is the MDMA block transfer complete indication signal output to the peripheral. The dma_finish signal is asserted to signal block completion. This uses the same timing as dma_ack and forms a handshaking loop with dma_req and/or dma_single.

Figure 16-8 shows the hardware handshaking interface between a destination or source peripheral and MDMA controller.

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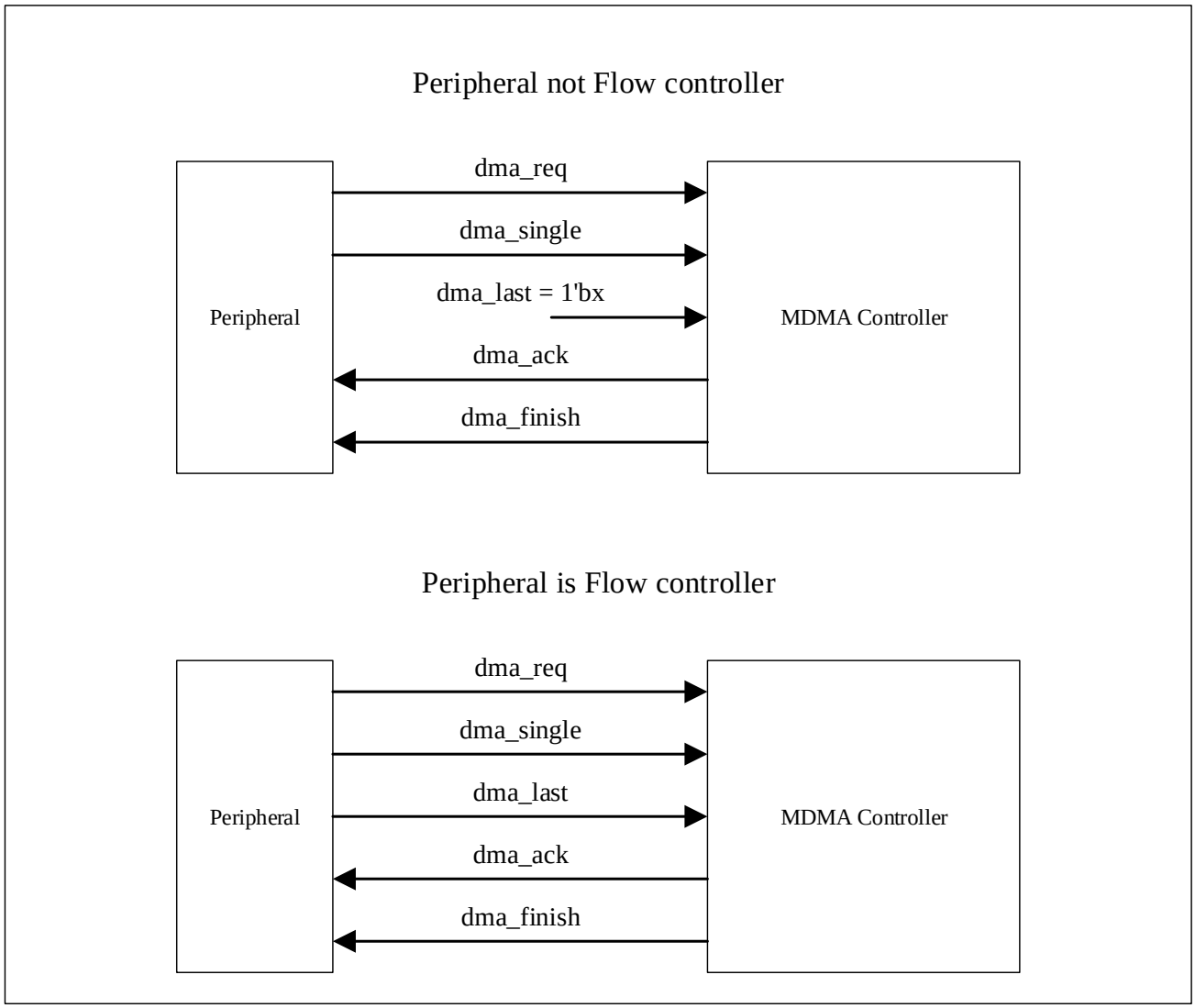
Figure 16-8 Hardware Handshaking Interface



Note: Once a peripheral asserts dma_req, dma_single, or dma_last, de-asserting the signal before the MDMA controller asserts dma_ack is not allowed. Doing so might result in unpredictable behavior. Irrespective of who is the flow controller and whether the peripheral is in Single Transaction Region, dma_req, dma_single, and dma_last signals must be de-asserted once MDMA controller asserts dma_ack. It is recommended that you follow this requirement, otherwise, unpredictable behavior may occur.

Table 16-1 shows all possible combinations of Flow Controller and Hardware Handshaking Interface signal values.

Table 16-1 Flow Controller and Hardware Handshaking Interface

Peripheral Is Flow Controller?	Peripheral in Single Transaction Region?	dma_req	dma_single	dma_last	MDMA Controller Action
No	No	0	0	x	Not a valid transaction request.
		0	1	x	Not a valid transaction request. If peripheral is not Flow Controller, “dma_single” is not sampled by MDMA

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Peripheral Is Flow Controller?	Peripheral in Single Transaction Region?	dma_req	dma_single	dma_last	MDMA Controller Action
					controller outside Single Transaction Region.
		1	x	x	Burst transaction request. If peripheral is not Flow Controller, "dma_single" is not sampled by MDMA controller outside Single Transaction Region. If peripheral is not the flow controller, "dma_last" does not have any relevance and it is ignored.
	Yes	0	0	x	Not a valid transaction request.
		0	1	x	Single Transaction request. MDMA controller initiates AXI burst of burst length 1. If peripheral is not the flow controller, "dma_last" does not have any relevance and it is ignored.
		1	0	x	Burst Transaction request. MDMA controller initiates AXI burst of burst length needed to complete the transaction (AXI burst length <= transaction size). This is called Early Burst Termination. If peripheral is not the flow controller, "dma_last" does not have any relevance and it is ignored.
		1	1	x	Burst Transaction request. MDMA controller initiates AXI burst of burst length needed to complete the transaction (AXI burst length <= transaction size). This is called Early Burst Termination. If peripheral is not the flow controller, "dma_last" does not have any relevance and it is ignored.
Yes	-(1)	0	0	x	Not a valid transaction request.
		0	1	x	Not a valid transaction request. If peripheral is flow controller, "dma_req" MUST be asserted to in it ate a transaction. MDMA controller waits till "dma_req" is asserted. The type of transaction (single or burst) is qualified by "dma_single" input.

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Peripheral Is Flow Controller?	Peripheral in Single Transaction Region?	dma_req	dma_single	dma_last	MDMA Controller Action
		1	0	0	Burst transaction request (not the last transaction).
		1	0	1	Last Burst transaction request.
		1	1	0	Single transaction request (not the last transaction).
		1	1	1	Last single transaction request.

1 Single Transaction Region is not applicable to Flow Control Peripheral, see 16.4.6.

16.4.7.2 Software Handshaking

When the slave peripheral requires the MDMA controller to perform a MDMA transaction, it communicates this request by sending an interrupt to the CPU or interrupt controller. The interrupt service routine then uses the software handshaking registers to initiate and control a MDMA transaction. A group of software registers is used to implement the software handshaking interface. The HSSELSRC/HSSELDST bit in the Channel Configuration register must be set to enable software handshaking.

The following registers are used for software handshaking:

- MDMA_CHnHSSRC – Software Handshake Register for Source of Channel n, see **错误!未找到引用源。**.
- MDMA_CHnHSDST – Software Handshake Register for Destination of Channel n, see **错误!未找到引用源。**.

MDMA controller clears the active request bits in MDMA_CHnHSSRC to 0 when the corresponding source transaction is completed. Similarly, active request bits in MDMA_CHnHSDST are cleared to 0 when the destination transaction is completed.

Note: The functionality of the software handshaking register bits are same as that of the corresponding hardware handshaking signals except that there are no register fields corresponding to dma_ack and dma_finish signals.

If software handshaking is used for a source and/or destination peripheral, the MDMA transfer automatically stalls after completion of the requested source and/or destination transaction. The MDMA controller does not proceed with the transfer until the hardware detects that software has set SHSR (in MDMA_CHnHSSRC and/or MDMA_CHnHSDST register) bit to 1.

16.4.8 Peripheral Interrupt Request Interface

This is a simplified version of the hardware handshaking interface. In this mode:

- The interrupt line from the peripheral is tied to the dma_req input.
- The dma_single input is tied low.
- The dma_last input is tied low.
- The dma_ack and dma_finish outputs are ignored (unconnected).

This interface can be used when the slave peripheral does not have hardware handshaking signals. To the MDMA controller, this is the same situation as the case of the Hardware Handshaking Interface when the peripheral is not the flow contoller.

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The peripheral can never be the flow controller because it cannot connect to the dma_last signal. The interrupt line from the peripheral is tied to the dma_req line and the timing of the interrupt line from the peripheral must be the same as the dma_req line as the case of the Hardware Handshaking Interface when the peripheral is not the flow controller.

Because the peripheral does not sample the dma_ack line, the handshaking loop is as follows:

1 Peripheral generates an interrupt that asserts “dma_req”.

2 MDMA controller completes the burst transaction and generates an end-of-burst transaction interrupt (Source\Destination Transaction Completed interrupt). Global Interrupt must be enabled in MDMA Configuration register and the corresponding channel's transaction completion indication interrupt must be enabled in CHn Interrupt Status Enable register and CHn Interrupt Signal Enable register.

3 The interrupt service routine clears the interrupt in the peripheral so that the “dma_req” is deasserted.

16.4.9 Flow Control Configurations

The transfer type and flow control configurations are decided by the value of the TTFC field in the MDMA Channel n Configuration register, which is programmable for a particular MDMA transfer.

Figure 16-9 indicates different flow control configurations using hardware handshaking interfaces (a simplified version of the interface is shown). These scenarios can also be used for software handshaking, which uses software registers instead of hardware signals.

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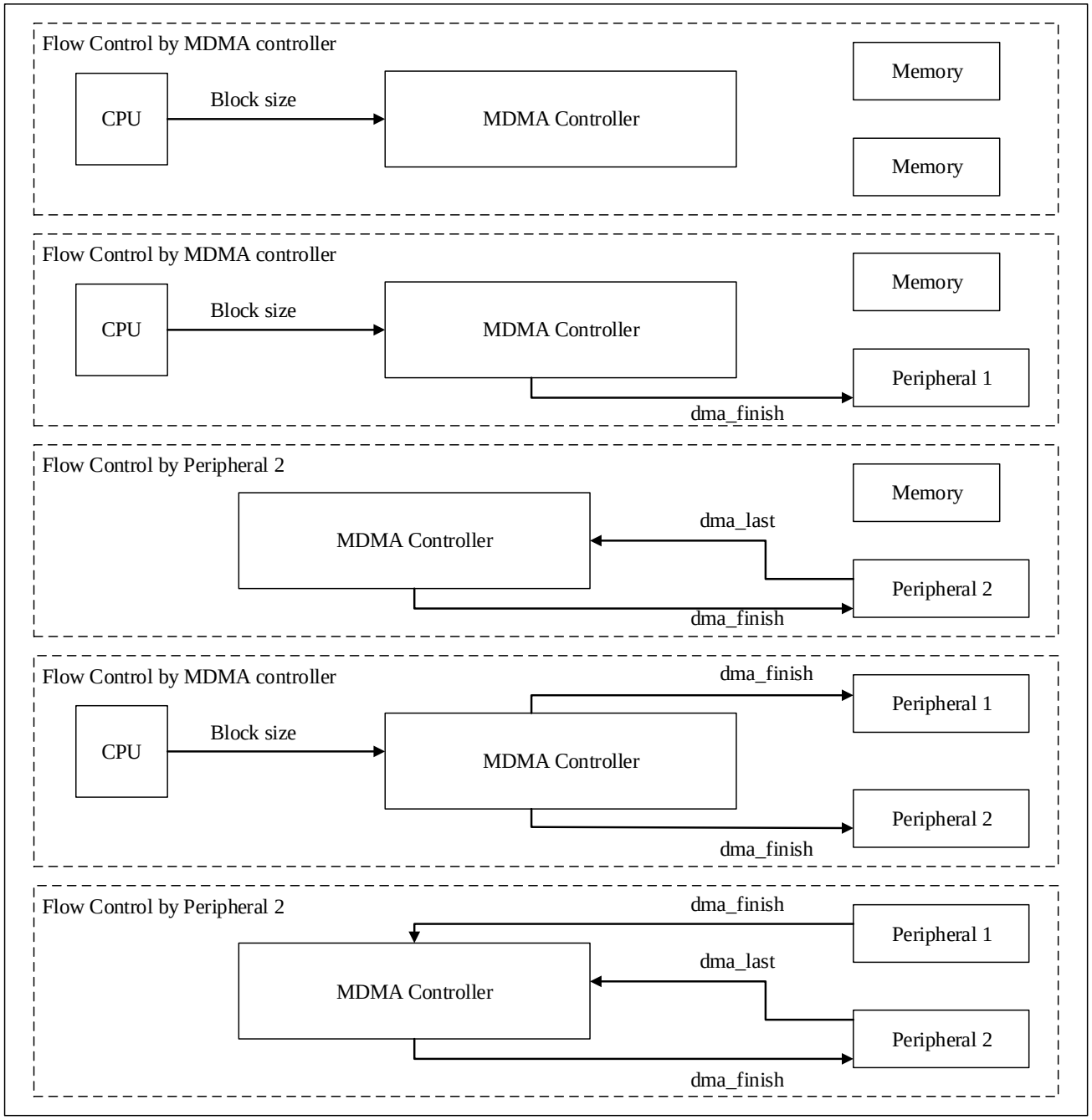
Figure 16-9 Flow Control Configurations (1)



1 All hardware handshake signals are not shown for clarity.

16.4.10 Early Terminated Burst Transaction

When a source or destination peripheral is in the single transaction region, a burst transaction can still be requested. However, in this case, *src_burst_size_bytes* or *dst_burst_size_bytes* is greater than the number of bytes left to complete the source or destination block transfer at the time the burst transaction is triggered. In this case, the burst transaction is started and "early-terminated" at block completion without transferring the programmed amount of data. Only the amount of data required to complete the block transfer is transferred.

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An early terminated burst transaction occurs only when the peripheral is not the flow controller.

- If the source peripheral is the flow controller and it does not have enough data for a burst transfer towards the end of a transaction, it asserts dma_single until it signals the last transaction by asserting dma_last along with dma_single. (The destination peripheral might enter the single transaction region at this point).
- If the destination peripheral is in the single transaction region and the destination peripheral still requests a burst transaction by asserting dma_req, then MDMA controller starts a burst transaction and early terminates it at block completion without transferring the programmed amount (MDMA_CHnCTRL.DSTMSIZE) of data.
- If the destination peripheral is the flow controller and it does not have enough data for a burst transfer towards the end of transaction, it asserts dma_single until it signals the last transaction by asserting dma_last along with dma_single. (The source peripheral might enter the single transaction region at this point).
- If the source peripheral is in the single transaction region and the source peripheral still requests a burst transaction by asserting dma_req, then MDMA controller starts a burst transaction and early terminates it at block completion without transferring the programmed amount (MDMA_CHnCTRL.SRCMSIZE) of data.

Note: When the destination peripheral is the flow controller, there can be data loss if the following conditions are met:

- *MDMA_CHnCTRL.STW > MDMA_CHnCTRL.DTW*
- *blk_size_bytes_dst / src_single_size_bytes != integer*

The amount of data lost is: src_single_size_bytes – dst_single_size_bytes

16.4.11 Transfer Control

Transfer control logic facilitates the data transfer from a source peripheral of the channel to the destination peripheral. It interacts with multiple other modules, such as the channel source and destination state machine, linked list control logic, channel registers, channel FIFO control logic and so on.

Data from the source peripheral is temporarily stored in the channel FIFO before being sent to the destination peripheral. MDMA controller implements the logic needed to pack and unpack data to fit the FIFO configuration, if source and destination peripherals use different transfer size (arsize, awsize) for data transfer.

16.4.11.1 Single Block Transfer

If a DMA transfer consists of a single block, the software sets the multi-block type bits (SMBTT and DMBTT) of both source and destination peripherals in the MDMA_CHnCFG register to 2’b00. In this case, the MDMA controller disables the channel once the block transfer corresponding to the block length programmed in MDMA_CHnBTS register is completed.

The MDMA_CHnINTSTS register is updated with the status corresponding to the completed block transfer. The MDMA_CHnINTSTS register is updated based on the settings of the MDMA_CHnINTSTSEN register and interrupts are generated based on the settings of the MDMA_CHnINTSTSEN, MDMA_CRINTSTS, and MDMA_CFG registers.

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16.4.11.2 Multi-block Transfer

If MDMA is programmed for multi-block transfers, the MDMA_CHnSA and MDMA_CHnDA registers are reprogrammed using either of the following methods on successive blocks of a multi-block transfer:

- Contiguous Address
- Auto Reloading
- Linked List

The MDMA_CHnCTRL and MDMA_CHnBTS registers are reprogrammed using either of the following methods on successive blocks of a multi-block transfer:

- Auto Reloading
- Linked List

The MDMA_CHnINTSTS register is updated with the status corresponding to the completed block transfer. The MDMA_CHnINTSTS register is updated based on the settings of the MDMA_CHnINTSTSEN and interrupts are generated based on the settings of the MDMA_CHnINTSTSEN, MDMA_CRINTSTS, and MDMA_CFG registers.

Note: If a multi-block transfer is enabled, there must be at least two blocks in the complete DMA transfer for Contiguous Address and Auto-Reloading-based multi-block transfers. Otherwise, it will result in unpredictable behavior.

The register update method for multi-block transfers depends on the value of the multi-block type bits (SMBTT and DMBTT) in the MDMA_CHnCFG register. All possible combinations of the multi-block register update methods are captured in the following table.

Table 16-2 Register Update Methods for Multi-block Transfer

SMBTT(1)	DMBTT(1)	Register Update Method				Remarks
		MDMA_CHnSA	MDMA_CHnDA	MDMA_CHnCTRL	MDMA_CHnBTS	
00	00	No update	No update	No update	No update	Single block or last block of multiblock
00	01	Contiguous	Reloaded from initial value	Reloaded from initial value	Reloaded from initial value	-
00	10	-	-	-	-	-
01	00	Reloaded from initial value	Contiguous	Reloaded from initial value	Reloaded from initial value	-
01	01	Reloaded from initial value	Reloaded from initial value	Reloaded from initial value	Reloaded from initial value	-
01	10	-	-	-	-	-
10	00	-	-	-	-	-
10	01	-	-	-	-	-
10	10	-	-	-	-	-
00	11	Contiguous	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	-
01	11	Reloaded from	Loaded from next	Loaded from next	Loaded from next	-

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SMBTT[1]	DMBTT[1]	Register Update Method				Remarks
		MDMA_CHnSA	MDMA_CHnDA	MDMA_CHnCTRL	MDMA_CHnBTS	
		initial value	LLI	LLI	LLI	
11	00	Loaded from next LLI	Contiguous	Loaded from next LLI	Loaded from next LLI	-
11	01	Loaded from next LLI	Reloaded from initial value	Loaded from next LLI	Loaded from next LLI	-
11	11	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	-
10	11	-	-	-	-	Invalid programming. SIMBTE[2] interrupt is generated
11	10	-	-	-	-	Invalid programming. SIMBTE[2] interrupt is generated

1 Are the bit [1:0] and bit [3:2] fields of the MDMA_CHnCFG register, respectively.

2 Slave Interface Multi Block Type Error.

16.4.11.2.1 Contiguous Address

In this case, the address between successive blocks is selected as a continuation from the end of the previous block. Enabling the source or destination address to be contiguous between blocks is a function of SMBTT and DMBTT fields.

MDMA_CHnSA and MDMA_CHnDA updates cannot be selected to be contiguous at the same time. If required, this functionality can be achieved indirectly, by using linked lists. To do this, set up the LLI.CHnSA address of the next block descriptor to be one greater than the end address of the previous block. Similarly, set up the LLI.CHnDA address of the next block descriptor to be one greater than the end address of the previous block.

Note: If a Contiguous-Address-based multi-block transfer is enabled, there must be at least two blocks in the complete DMA transfer. Otherwise, it will result in unpredictable behavior.

16.4.11.2.2 Auto Reloading

In this case, the channel transfer control registers are reloaded with their initial values at the completion of each block and these values are used for the new block. Some or all of the MDMA_CHnSA, MDMA_CHnDA, MDMA_CHnBTS, and MDMA_CHnCTRL channel registers are reloaded from their initial value at the start of a new block transfer, depending on the multi-block transfer type selected for source and destination peripherals.

The MDMA controller does not proceed to the next block transfer until software clears the corresponding channel's block transfer complete interrupt by writing 1 to the corresponding bit in the MDMA_CHnINTCLR register if this interrupt is not masked off.

Note: If Auto-Reloading-based multi-block transfer is enabled, there should be at least two blocks in the complete DMA transfer. Otherwise, it will result in unpredictable behavior.

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16.4.11.2.3 Linked List

In this case, the MDMA controller reprograms the channel transfer control registers prior to the start of each block, by fetching the block descriptor for that block from system memory. This is known as an LLI update.

MDMA block chaining uses a linked list pointer register (MDMA_CHnLLP) to store the address in memory of the next linked list item. Each LLI contains the following block descriptors:

- MDMA_CHnSA
- MDMA_CHnDA
- MDMA_CHnBTS
- MDMA_CHnCTRL
- MDMA_CHnLLP

To set up block chaining, a sequence of linked lists should be programmed in memory. MDMA controller allows dynamic extension of linked lists, which eliminates the need for creating the entire linked list in the system memory in advance. The SRLLI and LSRLLI fields (in the MDMA_CHnCTRL register) of the LLI are used to achieve this functionality.

For linked-list-based multi-block transfers, the SRLLI bit of the LLI.CHnCTRL register indicates whether the linked list item fetched from the memory is valid or not. If this bit is set to 0, it indicates the LLI is invalid, while 1 indicates the LLI is valid. If the LLI is invalid, MDMA controller discards the LLI and generates an LLI Error interrupt (if the corresponding channel error interrupt mask bit is set to 0). This error condition causes the MDMA controller to halt the corresponding channel gracefully. MDMA controller waits till software writes any value to the MDMA_CHnBTRR register to indicate the availability of a valid LLI, before attempting another LLI read operation.

LLI access always uses a burst size (arsize or awsize) that is the same as the data bus width and cannot be changed or programmed to anything other than this. Burst length (awlen or arlen) is chosen based on the data bus width so that the access does not cross one complete LLI structure of 64 bytes. MDMA controller fetches the LLI (40 bytes) in one AXI burst, if the burst length is not limited by other setting.

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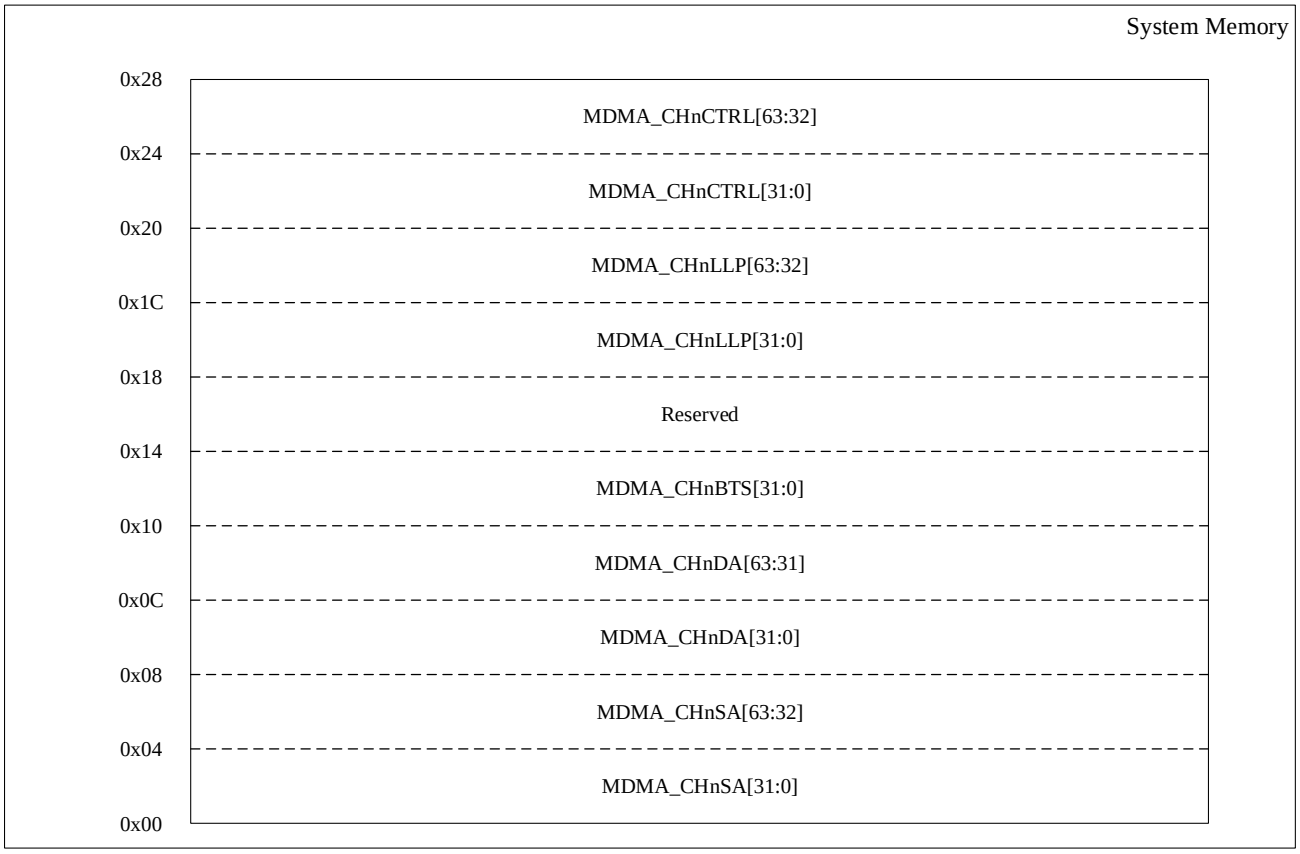
Figure 16-10 MDMA Linked List Item (Descriptor)



For more information about programming linked-list-based multi-block transfers, see 16.4.15.2.

16.4.11.2.4 Suspension of Transfers between Blocks

At the end of every block transfer, a Block Transfer Done Interrupt is asserted if:

- Global Interrupt is enabled (MDMA_CFG.GLBINTEN = 1)
- The channel block transfer completion interrupt is enabled (MDMA_CHnINTSTSEN.BLKTD = 1 AND MDMA_CHnINTSGLEN.BLKTD = 1 AND MDMA_CHnCTRL.BTIOC = 1)

For Contiguous Address and Auto-Reloading-based multi-block transfers (if neither source nor destination peripheral uses Linked-List-based multi-block transfers), the DMA transfer automatically stalls after the Block Transfer Done Interrupt is asserted, if the Block Transfer Done Interrupt is enabled and unmasked. The MDMA controller does not proceed to the next block transfer until a write to the appropriate field in MDMA_CHnINTCLR register, done by software to clear the channel Block Transfer Done Interrupt, is detected by hardware.

Channel suspension between blocks is used to ensure that the Block Transfer Done ISR (Interrupt Service Routine) of the next-to-last block is serviced before the start of the final block commences. This ensures that the ISR has cleared the MDMA_CHnCFG.SMBTT and/or MDMA_CHnCFG.DMBTT bits before completion of the final block. The MDMA_CHnCFG.SMBTT and/or MDMA_CHnCFG.DMBTT bits should be cleared in the Block Transfer Done ISR for the next-to-last block transfer.

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16.4.11.2.5 End of Multi-Block Transfers

If either source or destination peripheral uses Linked-List-based multi-block transfers, the corresponding last block indication bit, LSRLLI, in the LLI.CHnCTRL register indicates whether the current block is the last block in the transfer or not. If this bit is set to 1 for the current block, the MDMA controller understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of current block transfer.

For Contiguous Address and Auto-Reloading-based multi-block transfers (if neither source nor destination peripheral uses Linked-List-based multi-block transfers), if the corresponding multiblock type selection bits namely MDMA_CHnCFG.SMBTT and/or MDMA_CHnCFG.DMBTT bits are 2'b00 at the end of a block transfer, the MDMA controller understands that the previous block was the final block in the transfer and completes the DMA transfer operation.

16.4.12 AXI Unaligned Transfers

The unaligned memory accesses are common in the AXI-based systems, where the memory access address it not aligned to the natural boundary of the transfer width. The MDMA supports the generation of the unaligned memory DMA transfers on the AXI master interface. This feature support eliminates the following restrictions for the memory accesses:

- Source AXI data transfers – MDMA_CHnSA addresses must align to the source transfer width that is MDMA_CHnCTRL.STW (AXI bus arsize)
- Destination AXI data transfers – MDMA_CHnDA addresses must align to the destination transfer width that is MDMA_CHnCTRL.DTW (AXI bus awsize)

Thus, you can program MDMA_CHnSA and MDMA_CHnDA registers with any address, and it can be unaligned or aligned to the source or destination transfer width for memory accesses. The unaligned access is supported for combinations of MDMA_CHnCFG.TTFC where the memory access is involved (TTFC = 0x1, TTFC = 0x2, TTFC = 0x4, TTFC = 0x6).

MDMA controller handles the packing and the unpacking of the data considering the unaligned offset at both source and destination transfers. The data received from the unaligned source transaction is packed to align with FIFO width, and then it is stored in the FIFO. At the destination end, the data is read from the FIFO and unpacked based on the MDMA_CHnDA register and destination transfer width. The invalid bytes of the destination transfer are invalidated by driving the respective write strobes to 0. The following section provides more details about unaligned transfer based on MDMA, source, or destination as a flow controller.

16.4.12.1 MDMA Controller as a Flow Controller

The definition of the MDMA_CHnBTS register remains the same that is the number programmed into NUM field indicates the total number of data width MDMA_CHnCTRL.STW to be transferred in a DMA block transfer. If the source address is unaligned, then the unaligned bytes in the source are considered to derive at the total bytes transferred in a DMA block transfer.

The equation to calculate the total number of valid bytes transferred in a block for an unaligned transfer is as follows:

blk_size_bytes_dma_u = (MDMA_CHnBTS.NUM * *src_single_size_bytes*) - Source Unaligned bytes

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- The MDMA controller fetches the *blk_size_bytes_dma_u* bytes of data from the source and transfers all bytes to the destination based on the MDMA_CHnDA register.
- The destination unaligned bytes does not increase or decrease the valid number of bytes transferred in a DMA block. Only the source unaligned bytes affect the total number of bytes transferred in a DMA block.
- The unaligned transfer is supported for combinations of Transfer Type and Flow Controller wherever memory is involved (TTFC = 0x0, TTFC = 0x1, TTFC = 0x2).
- When Multi-Block Type is contiguous for either source or destination, initial address of the subsequent block is computed as following (Unaligned nature of the MDMA_CHnSA/MDMA_CHnDA also result in subsequent block initial address to be unaligned):
  - Source Contiguous: Next MDMA_CHnSA = Current MDMA_CHnSA + *blk_size_bytes_dma_u*
  - Destination Contiguous: Next MDMA_CHnDA = Current MDMA_CHnDA + *blk_size_bytes_dma_u* + Destination Unaligned bytes

16.4.12.2 Source is the Flow Controller

The equation to calculate the total number of valid bytes transferred in a block transfer for an unaligned transfer is as follows:

blk_size_bytes_src_u = (Number of source burst transactions in block * *src_burst_size_bytes*) + (Number of source single transactions in block * *src_single_size_bytes*) - Source Unaligned bytes

- The MDMA controller fetches the *blk_size_bytes_src_u* bytes of data from the source and transfers all bytes to the destination based on the MDMA_CHnDA register.
- The destination unaligned bytes does not increase or decrease the valid number of bytes transferred in DMA block. Only the source unaligned bytes affect the total number of bytes transferred in a DMA block.
- The unaligned transfer is supported for combinations of Transfer Type and Flow Controller wherever a memory is involved (TTFC = 0x4), when the source is the Flow Controller.
- When Multi-Block Type is Contiguous for either source or destination, initial address the subsequent block is computed as following (Unaligned nature of the MDMA_CHnSA/MDMA_CHnDA also results in sub-sequent block initial address to be unaligned):
  - Source Contiguous: Next MDMA_CHnSA = Current MDMA_CHnSA + *blk_size_bytes_src_u*
  - Destination Contiguous: Next MDMA_CHnDA = Current MDMA_CHnDA + *blk_size_bytes_src_u* + Destination Unaligned bytes

16.4.12.3 Destination is the Flow Controller

The equation to calculate the total number of valid bytes transferred in a block transfer for an unaligned transfer is as follows:

blk_size_bytes_dst_u = (Number of destination burst transactions in block * d*st_burst_size_bytes*) + (Number of destination single transactions in block * *dst_single_size_bytes*) - Destination Unaligned bytes

- The MDMA controller always provides the *blk_size_bytes_dst_u* bytes of data to the destination.

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- If source address is unaligned, then MDMA controller fetches an additional *src_single_size_bytes* to compensate the source unaligned bytes and to provide *blk_size_bytes_dst_u* bytes to the destination for a block.
  - Along with that, in few scenarios when destination is unaligned, then MDMA controller fetches ceil (Destination Unaligned bytes / *src_single_size_bytes*) amount of additional data from the source.
  - For example, if STW = 64 bit, DTW = 64 bit, TTFC = 0x6, DSTMSIZE = 16 data items, MDMA_CHnSA = 0x1007 (source is unaligned), and MDMA_CHnDA = 0xF008 (destination is aligned).
    - Number of bytes to be fetched from Source for a destination request (DST_REQ_DATA)

      = DSTMSIZE * DTW

      = 16 * 8

      = 128 bytes
    - Data can be fetched from the source for the first destination request

      = (DST_REQ_DATA/STW) * STW - source unaligned bytes

      = (128/8) * 8 - 7

      = 121 bytes

  From the previous example, source needs to fetch 7 more bytes of data for the first destination request (because of the unaligned source transfer). Hence, MDMA controller fetches an additional *src_single_size_bytes* of data to compensate unaligned bytes.
- The unaligned transfer is supported for combinations of Transfer Type and Flow Controller wherever a memory is involved (TTFC = 0x6), when Destination is the Flow Controller.
- When Multi-Block Type is Contiguous for either source or destination, initial address the subsequent block is computed based on the following formula (Unaligned nature of the MDMA_CHnSA/MDMA_CHnDA also result in sub-sequent block initial address to be unaligned):
  - Source Contiguous: Next MDMA_CHnSA = Current MDMA_CHnSA (Aligned) + *blk_size_bytes_dst_u* + Source Unaligned bytes
  - Destination Contiguous: Next MDMA_CHnDA = Current MDMA_CHnDA + *blk_size_bytes_dst_u*

16.4.13 Channel Suspend and Disable

Under normal operation, software enables a channel by writing a 1 to the channel enable register (MDMA_CHEN register), and hardware disables a channel on transfer completion by clearing the MDMA_CHEN register.

Software can suspend or disable a channel before a transfer completes. The suspend and disable procedures are explained in the following sections.

16.4.13.1 Channel Suspend

To suspend a channel during DMA transfer:

1 Software writes a 1 to the channel suspend bit CHn in the channel suspend register (MDMA_CHSUSP).

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2 MDMA controller gracefully halts all transfers from the source peripheral, after completing all AXI transfers initiated on the source peripheral.

3 MDMA controller sets CHSS bit (in the MDMA_CHnINTSTS register) to 1 to indicate that source data transfer is suspended and generates the interrupt if it is not masked off.

Note: If the channel FIFO is full and the destination peripheral is not requesting data transfer, MDMA controller cannot receive any more data on the corresponding master interface, which could lead to a deadlock.

The requests initiated by source/destination/LLI state machines and present in the Master Interface Read Address Channel and Write Address Channel FIFOs to be sent on the AXI Master Interface will be sent on the AXI Master Interface even if the Channel Suspend request is initiated. Based on the Master Interface Read Address and Write Address Channel FIFO depth configuration, maximum 8 read/write requests may be initiated and MDMA controller waits for the data/response for these requests also before suspending the channel.

4 MDMA controller transfers all the data in channel FIFO to destination peripheral.

When STW < DTW and the MDMA_CHSUSP.CHn bit is high, there may still be data in the channel FIFO, but not enough to form a single transfer of DTW. The data remaining in the channel FIFO is transferred to destination if channel is resumed later which results in filling of more data in channel FIFO.

5 MDMA controller clears channel locking and resets the channel locking settings in the MDMA_CHnCFG register.

6 MDMA controller sets the CHLC bit (in the MDMA_CHnINTSTS register) to 1 to indicate that channel locking is cleared.

7 MDMA controller sets the CHS bit (in the MDMA_CHnINTSTS register) to 1 to indicate that the channel is suspended.

8 MDMA controller generates a CHS interrupt (if it is not masked off).

After a channel suspend, software may either resume the channel after some time, or disable the channel.

16.4.13.2 Channel Suspend and Resume

To suspend and resume a channel:

1 Follow steps 1 to 4 in 16.4.13.1.

2 Software writes a 0 to the channel suspend bit CHn in the channel suspend register (MDMA_CHSUSP).

3 MDMA controller resumes the DMA transfer from the point where it got suspended.

Note: Once software initiates the channel suspend procedure by writing a 1 to the channel suspend bit (CHn in the MDMA_CHSUSP register), writing 0 to CHn bit to resume the channel before MDMA controller asserts CHS bit (in the MDMA_CHnINTSTS register) is not allowed. MDMA controller ignores this write operation.

16.4.13.3 Channel Suspend and Disable Prior to Transfer Completion

To suspend and disable a channel:

1 Follow steps 1 to 4 in 16.4.13.1.

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2 To disable the suspended channel using software, write a 0 to the channel enable bit (CHn) in the channel enable register (MDMA_CHEN) after MDMA controller asserts the CHS bit (in the MDMA_CHnINTSTS register) to 1 to indicate that channel is suspended.

When STW < DTW and the MDMA_CHSUSP.CHn bit is high, there may still be data in the channel FIFO, but not enough to form a single transfer of DTW.

In this scenario, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral and is lost.

3 MDMA controller sets the CHD bit (in the MDMA_CHnINTSTS register) to 1 to indicate that the channel is disabled.

4 MDMA controller generates a CHD interrupt (if it is not masked off).

5 MDMA controller clears the MDMA_CHEN.CHn bit to 0.

16.4.13.4 Channel Disable Prior to Transfer Completion without Suspend

To disable a channel without suspending:

1 Software writes a 0 to the channel enable bit CHn in the channel enable register (MDMA_CHEN).

2 MDMA controller gracefully halts all transfers from the source peripheral, after completing all AXI transfers initiated on the source peripheral.

3 MDMA controller transfers all the data in the channel FIFO to the destination peripheral.

If STW < DTW and the MDMA_CHEN.CHn bit is low, there may still be data in the channel FIFO, but not enough to form a single transfer of DTW.

In this scenario, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral and is lost.

4 MDMA controller clears channel locking and resets the channel locking settings in the MDMA_CHnCFG register.

5 MDMA controller sets the CHLC bit (in the MDMA_CHnINTSTS register) to 1 to indicate that channel locking is cleared.

6 MDMA controller sets the CHD bit (in the MDMA_CHnINTSTS register) to 1 to indicate that the channel is disabled.

7 MDMA controller generates a CHD interrupt (if it is not masked off).

8 MDMA controller clears the MDMA_CHEN.CHn bit to 0.

Note: Once software initiates the channel disable procedure by writing a 0 to the channel enable bit (CHn in the MDMA_CHEN register), writing a 1 to CHn bit to re-enable the channel before MDMA controller asserts CHD bit (in the MDMA_CHnINTSTS register) is not allowed. MDMA controller ignores this write operation.

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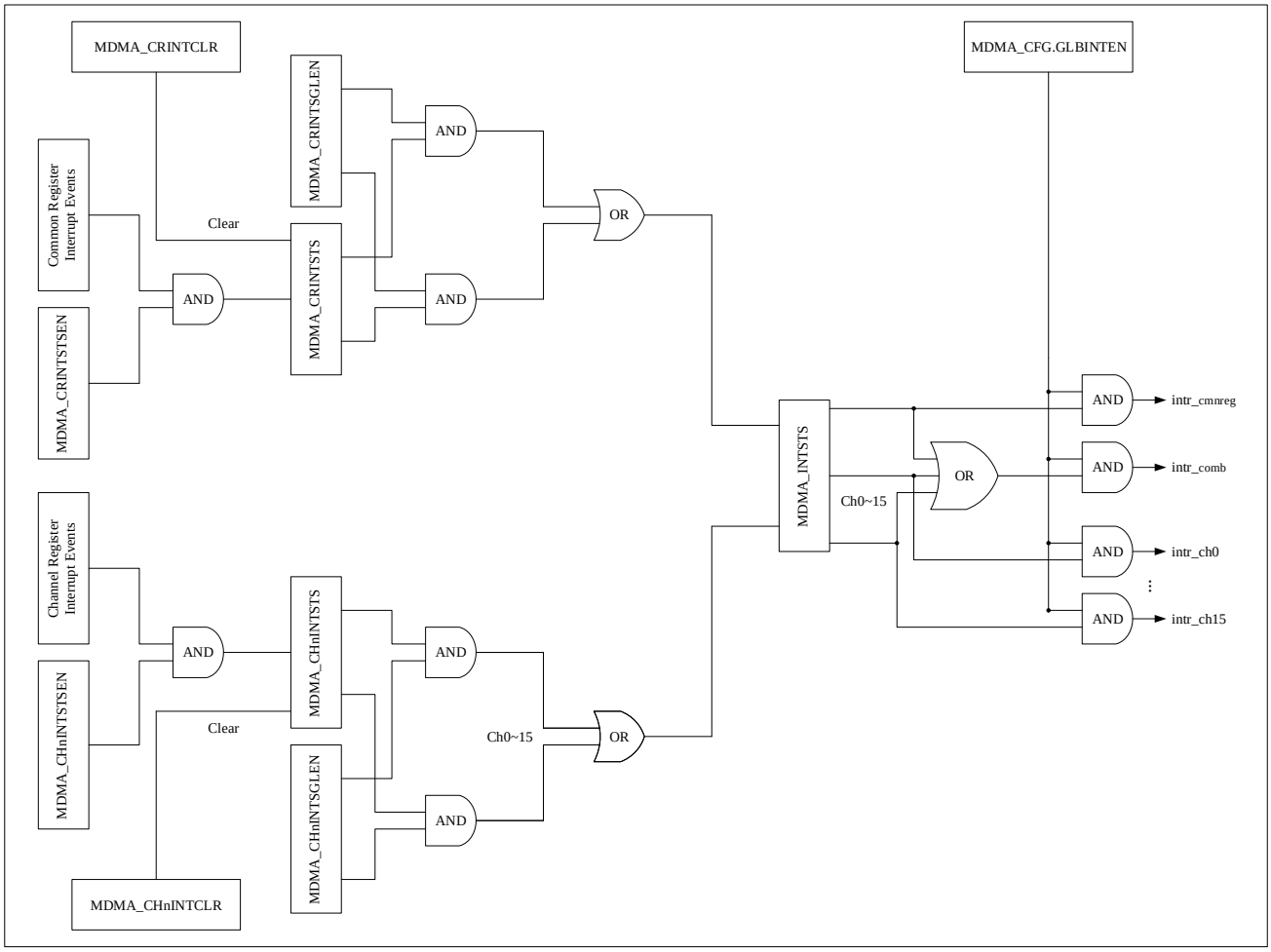
16.4.14 Interrupt

MDMA supports combined and individual interrupt outputs. MDMA has different registers to support the interrupt interface. Software can read these registers to understand the source of the interrupt and take appropriate actions. For more information, refer to the relevant interrupt registers in section 16.5.1 and section 16.5.2.

Figure 16-11 shows the interrupt generation mechanism in MDMA.

Figure 16-11 MDMA Interrupt Generation (1) (2) (3)



1 The intr_comb in the figure indicates a combination of interrupts by MDMA common register interrupt and MDMA channel n interrupts.

2 The intr_cmnreg in the figure indicates an individual MDMA common register interrupt.

3 The intr_chn (n = 0 to 15) in the figure indicates an individual MDMA channel n interrupt.

16.4.15 Programming Guide

16.4.15.1 Single-Block Transfer

This section describes the programming steps for a single-block transfer.

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1 Software reads the MDMA Channel Enable register to select an available (unused) channel.

2 Software programs MDMA_CHnCFG register with multi-block type value of both source and destination peripheral to be 2'b00 (SMBTT and/or DMBTT bits).

3 Software programs MDMA_CHnSA and/or MDMA_CHnDA, MDMA_CHnBTS, and MDMA_CHnCTRL registers with appropriate values for the block.

4 Software enables the channel by writing 1 to the appropriate bit location in MDMA_CHEN register.

5 Source and destination requests single or burst DMA transactions to transfer the block of data (assuming non-memory peripherals). The MDMA controller acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.

6 Software waits for the block transfer completion interrupt/polls the block transfer completion indication bit (BLKTD) in MDMA_CHnINTSTS register till the bit is 1.

16.4.15.2 Linked-List-Based Multi-Bock Transfer

This section describes the programming steps for a linked-list-based multi-block transfer.

1 Software reads the MDMA Channel Enable register to select an available (unused) channel.

2 Software programs the MDMA_CHnCFG register with appropriate values for the DMA transfer.

The SMBTT and/or DMBTT bits must be set to 2’b11.

3 Software programs the base address of the first linked list item and the master interface on which the linked list item is available in the MDMA_CHnLLP register.

4 Software creates one or more linked list items in system memory. Software can create the entire linked list item in advance or dynamically extend the linked list using the SRLLI and LSRLLI fields (in the MDMA_CHnCTRL register) of the LLI.

5 Software enables the channel by writing 1 to the appropriate bit location in MDMA_CHEN register.

Note: It is possible to swap the sequence of step 4 and step 5. However, if step 5 is performed before step 4, or if the linked list item for the next block transfer is not available in system memory at any time during the multi-block transfer, as indicated by SRLLI bit of the fetched LLI being set to 0, MDMA controller might generate a LLI Invalid Error interrupt.

6 MDMA controller initiates the DMA block transfer operation based on the settings for the block transfer.

7 The block transfer might start immediately or after the hardware or software handshaking request, depending on the settings of the TTFC field in the MDMA_CHnCFG register.

8 MDMA controller copies the linked list contents to the registers used for executing the MDMA block transfer (that is, the MDMA_CHnSA and/or MDMA_CHnDA, MDMA_CHnBTS, and MDMA_CHnCTRL registers) and initiates the MDMA block transfer.

9 During the linked list fetch phase:

a) If MDMA controller sees MDMA_CHnCTRL.LSRLLI bit of the fetched LLI as 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of current block transfer.

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b) If MDMA controller sees MDMA_CHnCTRL.LSRLLI bit of the fetched LLI as 0, it understands that there are one or more blocks to be transferred and goes to step 6.

c) If MDMA controller sees MDMA_CHnCTRL.LSRLLI bit of the fetched LLI as 0, MDMA controller might generate LLI Invalid Error Interrupt. MDMA controller waits till software writes (any value) to MDMA_CHnBTRR to indicate valid LLI availability, before attempting another LLI read operation.

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16.5 Registers

16.5.1 MDMA Common Registers

16.5.1.1 MDMA ID register (MDMA_ID)

Address offset: 0x0000

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NBR[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NBR[15:0]															
r															

Bit field	Name	Description
31:0	NBR	MDMA Component ID Number.

16.5.1.2 MDMA Version register (MDMA_VERSION)

Address offset: 0x0008

Reset value: 0x3230 302A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NBR[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NBR[15:0]															
r															

Bit field	Name	Description
31:0	NBR	MDMA Component Version Number.

16.5.1.3 MDMA Configuration register (MDMA_CFG)

Address offset: 0x0010

Reset value: 0x0000 0000

This register is used to enable the MDMA, which must be done before any channel activity can begin. This register also contains global interrupt enable bit.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														GLBINTEN	EN
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	GLBINTEN	This bit is used to globally enable the interrupt generation. 0x0: MDMA Interrupts are disabled 0x1: MDMA Interrupts are enabled
0	EN	This bit is used to enable the MDMA. 0x0: MDMA is disabled 0x1: MDMA is enabled *NOTE: If this bit is cleared while any channel is still active, then this bit still returns 1 to indicate that there are channels still active until MDMA hardware has terminated all activity on all channels, at which point this bit returns zero (0).*

16.5.1.4 MDMA Channel Enable register (MDMA_CHEN)

Address offset: 0x0018

Reset value: 0x0000 0000

This is MDMA Channel Enable Register. If software wants to set up a new channel, it can read this register to find out which channels are currently inactive and then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the MDMA Global Enable bit (bit 0 of MDMA Configuration register) is 0. When Global Enable bit is 0, a write to the MDMA Configuration register is ignored and a read always reads back 0.

The channel enable bit, CHn, is written only if the corresponding channel write enable bit, CHnWEN, is asserted on the same slave interface write transfer. For example, writing hex 0001_XXX1 writes a 1 into bit 0, while bits [15:1] remains unchanged. Writing hex 0000_XXXX leaves bits [15:0] unchanged.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CH15WEN	CH14WEN	CH13WEN	CH12WEN	CH11WEN	CH10WEN	CH9WEN	CH8WEN	CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
n + 16	CHnWEN	Channel n Enable bit write enable (n = 0, 1, … 15). Read back value of this register bit is always '0'. 0x0: Channel n Enable bit write disable 0x1: Channel n Enable bit write enable
n	CHn	Channel n Enable (n = 0, 1, … 15). This bit is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. 0x0: Channel n is disabled 0x1: Channel n is enabled

16.5.1.5 MDMA Channel Suspend register (MDMA_CHSUSP)

Address offset: 0x0020

Reset value: 0x0000 0000

This is MDMA Channel Suspend Register. The channel suspend bit, CHn, is written only if the corresponding channel write enable bit, CHnWEN, is asserted on the same slave interface write transfer. For example, writing hex 0001_XXX1 writes a 1 into bit 0, while bits [15:1] remains unchanged. Writing hex 0000_XXXX leaves bits [15:0] unchanged.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CH15WEN	CH14WEN	CH13WEN	CH12WEN	CH11WEN	CH10WEN	CH9WEN	CH8WEN	CH7WEN	CH6WEN	CH5WEN	CH4WEN	CH3WEN	CH2WEN	CH1WEN	CH0WEN
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
n + 16	CHnWEN	Channel n Suspend bit write enable (n = 0, 1, … 15). Read back value of this register bit is always '0'. 0x0: Channel n Suspend bit write disable 0x1: Channel n Suspend bit write enable
n	CHn	Channel n Suspend Request (n = 0, 1, … 15). Software sets this bit to 1 to request channel suspend. If this bit is set to 1, MDMA suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with Channel n Interrupt Status register's bit 29 (Channel Suspended) to cleanly disable the channel without losing any data. In this case, software first sets this bit to 1 and polls Channel n Interrupt Status register's bit 29 till it is set to 1. Software can then clear Channel n Enable bit to 0 to disable the channel (in Channel

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Bit field	Name	Description
		Enable register). Software can clear this bit to 0, after MDMA sets Channel n Interrupt Status register's bit 29 to 1, to exit the channel suspend mode. 0x0: No Channel Suspend Request 0x1: Request for Channel Suspend *NOTE: This bit is cleared when channel is disabled.*

16.5.1.6 MDMA Interrupt Status register (MDMA_INTSTS)

Address offset: 0x0030

Reset value: 0x0000 0000 0000 0000

MDMA Interrupt Status Register captures the combined channel interrupt for each channel and combined common register block interrupt.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reserved															

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reserved															COMREG
															r

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
63:33	Reserved	Reserved, the reset value must be maintained.
32	COMREG	Common Register Interrupt Status Bit. 0x0: Common Register Interrupt is Inactive 0x1: Common Register Interrupt is Active
31:16	Reserved	Reserved, the reset value must be maintained.
n	CHn	Channel n Interrupt Status Bit (n = 0, 1, … 15). 0x0: Channel n Interrupt is Inactive 0x1: Channel n Interrupt is Active

16.5.1.7 MDMA Common Register Interrupt Clear register (MDMA_CRINTCLR)

Address offset: 0x0038

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Reset value: 0x0000 0000

Writing 1 to specific field clears the corresponding field in MDMA Common Register Interrupt Status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SIURDEIC	Reserved				SICRWOHEIC	SICRR2WOEIC	SICRW2ROEIC	SICRDEIC
							w					w	w	w	w

Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	SIURDEIC	Slave Interface Undefined Register Decode Error Interrupt Clear bit. 0x0: Inactive signal. No action taken. 0x1: Clear the SIURDEIS interrupt in the MDMA Common Register Interrupt Status register.
7:4	Reserved	Reserved, the reset value must be maintained.
3	SICRWOHEIC	Slave Interface Common Register Write On Hold Error Interrupt Clear bit. 0x0: Inactive signal. No action taken. 0x1: Clear the SICRWOHEIS interrupt in the MDMA Common Register Interrupt Status register.
2	SICRR2WOEIC	Slave Interface Common Register Read to Write Only Error Interrupt Clear bit. 0x0: Inactive signal. No action taken. 0x1: Clear the SICRR2WOEIS interrupt in the MDMA Common Register Interrupt Status register.
1	SICRW2ROEIC	Slave Interface Common Register Write to Read Only Error Interrupt Clear bit. 0x0: Inactive signal. No action taken. 0x1: Clear the SICRW2ROEIS interrupt in the MDMA Common Register Interrupt Status register.
0	SICRDEIC	Slave Interface Common Register Decode Error Interrupt Clear bit. 0x0: Inactive signal. No action taken. 0x1: Clear the SICRDEIS interrupt in the MDMA Common Register Interrupt Status register.

16.5.1.8 MDMA Common Register Interrupt Status Enable register (MDMA_CRINTSTSEN)

Address offset: 0x0040

Reset value: 0xFFFF FFFF

Writing 1 to specific field enables the corresponding interrupt status generation in MDMA Common Register Interrupt Status register.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SIURDEIS	Reserved				SICRWOHEIS	SICRR2WOEIS	SICRW2ROEIS	SICRDEIS
							rw					rw	rw	rw	rw

Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	SIURDEIS	Slave Interface Undefined Register Decode Error Interrupt Status Enable bit. This bit is used to enable the corresponding channel interrupt status bit. 0x0: SIURDEIS bit in the MDMA Common Register Interrupt Status register is Disabled. 0x1: SIURDEIS bit in the MDMA Common Register Interrupt Status register is Enabled.
7:4	Reserved	Reserved, the reset value must be maintained.
3	SICRWOHEIS	Slave Interface Common Register Write On Hold Error Interrupt Status Enable bit. This bit is used to enable the corresponding channel interrupt status bit. 0x0: SICRWOHEIS bit in the MDMA Common Register Interrupt Status register is Disabled. 0x1: SICRWOHEIS bit in the MDMA Common Register Interrupt Status register is Enabled.
2	SICRR2WOEIS	Slave Interface Common Register Read to Write Only Error Interrupt Status Enable bit. This bit is used to enable the corresponding channel interrupt status bit. 0x0: SICRR2WOEIS bit in the MDMA Common Register Interrupt Status register is Disabled. 0x1: SICRR2WOEIS bit in the MDMA Common Register Interrupt Status register is Enabled.
1	SICRW2ROEIS	Slave Interface Common Register Write to Read Only Error Interrupt Status Enable bit. This bit is used to enable the corresponding channel interrupt status bit. 0x0: SICRW2ROEIS bit in the MDMA Common Register Interrupt Status register is Disabled. 0x1: SICRW2ROEIS bit in the MDMA Common Register Interrupt Status register is Enabled.
0	SICRDEIS	Slave Interface Common Register Decode Error Interrupt Status Enable bit. This bit is used to enable the corresponding channel interrupt status bit. 0x0: SICRDEIS bit in the MDMA Common Register Interrupt Status register is Disabled. 0x1: SICRDEIS bit in the MDMA Common Register Interrupt Status register is Enabled.

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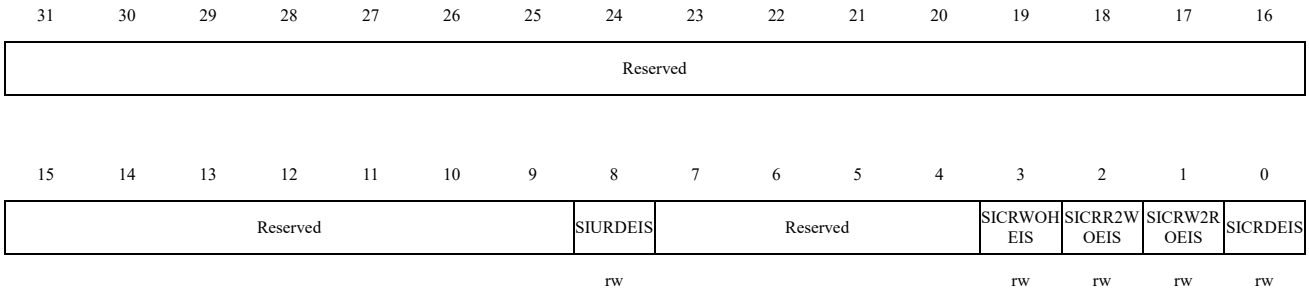
16.5.1.9 MDMA Common Register Interrupt Signal Enable register (MDMA_CRINTSGLEN)

Address offset: 0x0048

Reset value: 0xFFFF FFFF

Writing 1 to specific field will propagate the corresponding interrupt status in MDMA Common Register Interrupt Status Register to generate a port evel interrupt.



Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	SIURDEIS	Slave Interface Undefined Register Decode Error Interrupt Signal Enable bit. This bit is used to enable the corresponding channel interrupt status bit to generate a port level interrupt. 0x0: SIURDEIS bit in the MDMA Common Register Interrupt Status register is Disabled at port level. 0x1: SIURDEIS bit in the MDMA Common Register Interrupt Status register is Enabled at port level.
7:4	Reserved	Reserved, the reset value must be maintained.
3	SICRWOHEIS	Slave Interface Common Register Write On Hold Error Interrupt Signal Enable bit. This bit is used to enable the corresponding channel interrupt status bit to generate a port level interrupt. 0x0: SICRWOHEIS bit in the MDMA Common Register Interrupt Status register is Disabled at port level. 0x1: SICRWOHEIS bit in the MDMA Common Register Interrupt Status register is Enabled at port level.
2	SICRR2WOEIS	Slave Interface Common Register Read to Write Only Error Interrupt Signal Enable bit. This bit is used to enable the corresponding channel interrupt status bit to generate a port level interrupt. 0x0: SICRR2WOEIS bit in the MDMA Common Register Interrupt Status register is Disabled at port level. 0x1: SICRR2WOEIS bit in the MDMA Common Register Interrupt Status register is Enabled at port level.
1	SICRW2ROEIS	Slave Interface Common Register Write to Read Only Error Interrupt Signal Enable bit. This bit is used to enable the corresponding channel interrupt status bit to generate a port level interrupt.

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Bit field	Name	Description
		0x0: SICRW2ROEIS bit in the MDMA Common Register Interrupt Status register is Disabled at port level. 0x1: SICRW2ROEIS bit in the MDMA Common Register Interrupt Status register is Enabled at port level.
0	SICRDEIS	Slave Interface Common Register Decode Error Interrupt Signal Enable bit. This bit is used to enable the corresponding channel interrupt status bit to generate a port level interrupt. 0x0: SICRDEIS bit in the MDMA Common Register Interrupt Status register is Disabled at port level. 0x1: SICRDEIS bit in the MDMA Common Register Interrupt Status register is Enabled at port level.

16.5.1.10 MDMA Common Register Interrupt Status register (MDMA_CRINTSTS)

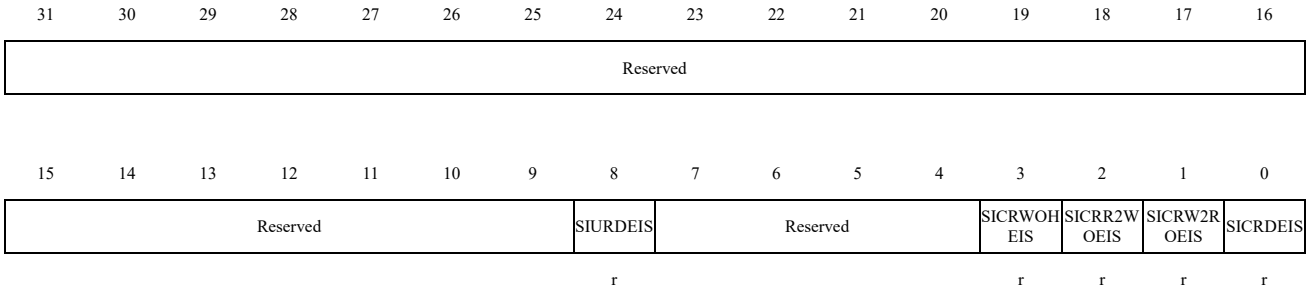
Address offset: 0x0050

Reset value: 0x0000 0000

This Register captures Slave interface access errors:

- Decode Error
- Write to read only register
- Read to write only register
- Write on hold
- Undefined address

Error Interrupt status is generated if the corresponding Status Enable bit in MDMA_CRINTSTSEN register is set to 1. Error Interrupt status bit is cleared to 0 on writing 1 to the corresponding interrupt clear bit in MDMA_CRINTCLR register.



Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	SIURDEIS	Slave Interface Undefined Register Decode Error Interrupt Status bit. Decode Error generated by MDMA during register access. This error occurs if the register access is to undefined address range (>0x8FF if 8 channels are

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Bit field	Name	Description
		configured, >0x4FF if 4 channels are configured etc.) resulting in error response by MDMA slave interface. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CRINTCLR on enabling the channel (required when the interrupt is not enabled). 0x0: Slave Interface Decode Error not detected. 0x1: Slave Interface Decode Error detected.
7:4	Reserved	Reserved, the reset value must be maintained.
3	SICRWOHEIS	Slave Interface Common Register Write On Hold Error Interrupt Status bit. This error occurs if an illegal write operation is performed on a common register; this happens if a write operation is performed on a common register except MDMA_SWRST with RSTREQ field set to 1 when MDMA is in Hold mode. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CRINTCLR on enabling the channel (required when the interrupt is not enabled). 0x0: Slave Interface Common Register Write On Hold Error not detected. 0x1: Slave Interface Common Register Write On Hold Error detected.
2	SICRR2WOEIS	Slave Interface Common Register Read to Write Only Error Interrupt Status bit. This error occurs if Read operation is performed to a Write Only register in the common register space (0x000 to 0x0FF). This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CRINTCLR on enabling the channel (required when the interrupt is not enabled). 0x0: Slave Interface Read to Write Only Error not detected. 0x1: Slave Interface Read to Write Only Error detected.
1	SICRW2ROEIS	Slave Interface Common Register Write to Read Only Error Interrupt Status bit. This error occurs if Write operation is performed to a Read Only register in the common register space (0x000 to 0x0FF). This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CRINTCLR on enabling the channel (required when the interrupt is not enabled). 0x0: Slave Interface Write to Read Only Error not detected. 0x1: Slave Interface Write to Read Only Error detected.
0	SICRDEIS	Slave Interface Common Register Decode Error Interrupt Status bit. Decode Error generated by MDMA during register access. This error occurs if the register access is to an invalid address in the common register space (0x000 to 0x0FF) resulting in error response by MDMA slave interface. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CRINTCLR on enabling the channel (required when the interrupt is not enabled). 0x0: Slave Interface Decode Error not detected. 0x1: Slave Interface Decode Error detected.

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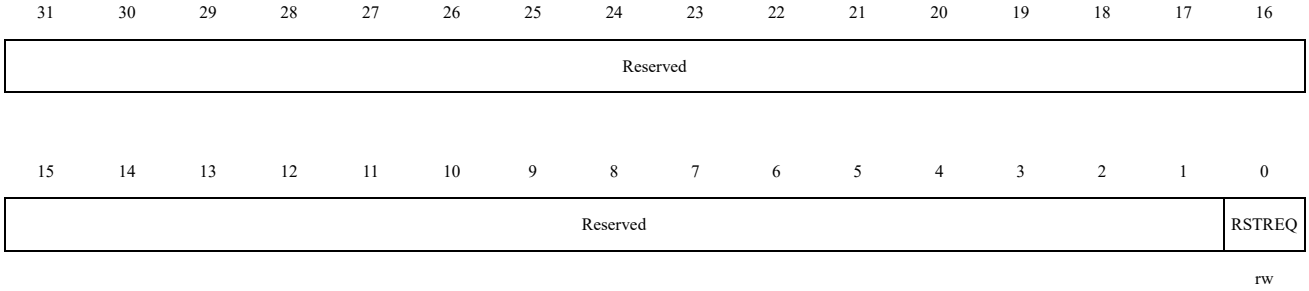
16.5.1.11 MDMA Software Reset register (MDMA_SWRST)

Address offset: 0x0058

Reset value: 0x0000 0000

This register is used to initiate the Software Reset to MDMA.



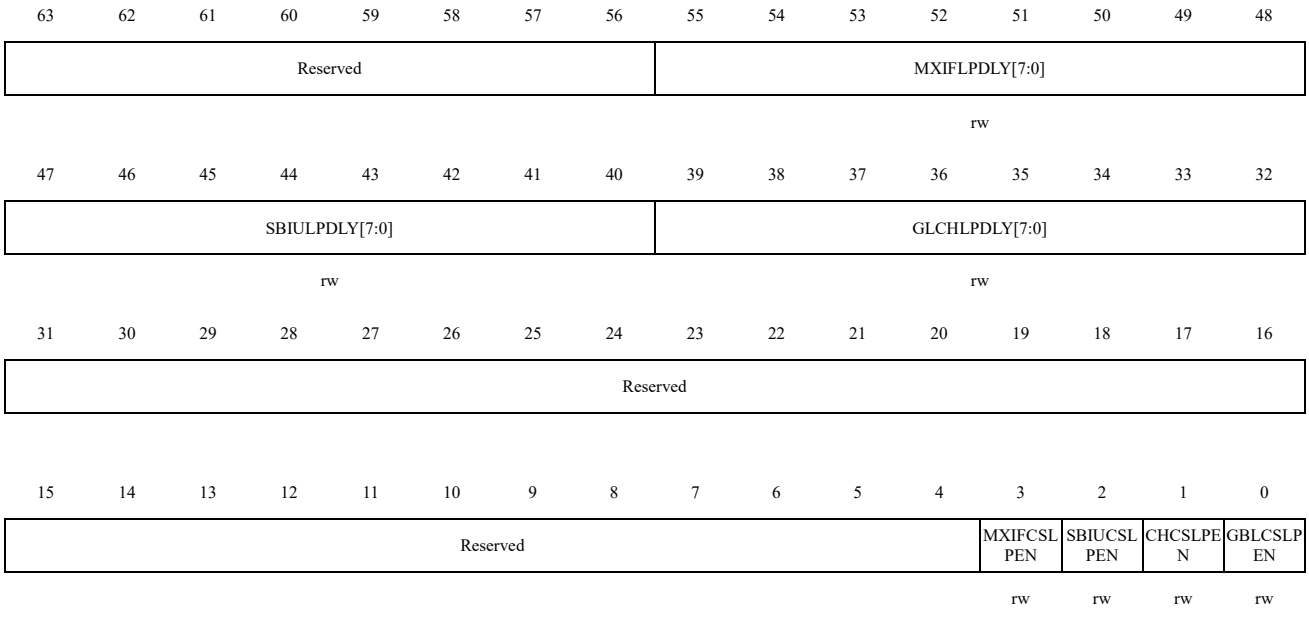
Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	RSTREQ	MDMA Reset Request bit. Software writes 1 to this bit to reset the MDMA and polls this bit to see it as 0. MDMA resets all the modules except the slave bus interface module and clears this bit to 0. *NOTE: Software is not allowed to write 0 to this bit.*

16.5.1.12 MDMA Low Power Configuration register (MDMA_LPCFG)

Address offset: 0x0060

Reset value: 0x0000 0000 0000 0000

This register should be programmed prior to enabling the channel.



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Bit field	Name	Description
63:56	Reserved	Reserved, the reset value must be maintained.
55:48	MXIFLPDLY	Defines the load value to be programmed into the AXI Master Interface low power delay counter. The programmed value must be greater than or equal to 0x4. If value programmed is less than 0x4, then the register value is reset to 4. The maximum value programmed into this register field is limited to 7, otherwise the upper bits of this field is reset to 0x0.
47:40	SBIULPDLY	Defines the load value to be programmed into the SBIU low power delay counter. The programmed value must be greater than or equal to 0x4. If value programmed is less than 0x4, then the register value is reset to 4. The maximum value programmed into this register field is limited to 7, otherwise the upper bits of this field is reset to 0x0.
39:32	GLCHLPDLY	Defines the load value to be programmed into the Global and MDMA Channel low power delay counter. The programmed value must be greater than or equal to 0x4. If value programmed is less than 0x4, then the register value is reset to 4. The maximum value programmed into this register field is limited to 7, otherwise the upper bits of this field is reset to 0x0.
31:4	Reserved	Reserved, the reset value must be maintained.
3	MXIFCSLPEN	AXI Master Interface Context Sensitive Low Power feature enable. 0x0: The feature is disabled 0x1: The feature is enabled
2	SBIUCSLPEN	SBIU Context Sensitive Low Power feature enable. 0x0: The feature is disabled 0x1: The feature is enabled
1	CHCSLPEN	MDMA Channel Context Sensitive Low Power feature enable. 0x0: The feature is disabled 0x1: The feature is enabled
0	GBLCSLPEN	Global Context Sensitive Low Power feature enable. 0x0: The feature is disabled 0x1: The feature is enabled

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16.5.2 MDMA Channel n Registers

16.5.2.1 MDMA Channel n Source Address register (MDMA_CHnSA)

Address offset: 0x0100 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000 0000 0000

The starting source address is programmed by software before the MDMA channel is enabled, or by an LLI update before the start of the MDMA transfer. While the MDMA transfer is in progress, this register is updated to reflect the source address of the current AXI transfer.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR[63:48]															
rw															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR[47:32]															
rw															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit field	Name	Description
63:0	ADDR	Current Source Address of MDMA transfer: Updated after each source transfer. The SINC field in the MDMA_CHnCTRL register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer.

16.5.2.2 MDMA Channel n Destination Address register (MDMA_CHnDA)

Address offset: 0x0108 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000 0000 0000

The starting destination address is programmed by software before the MDMA channel is enabled, or by an LLI update before the start of the MDMA transfer. While the MDMA transfer is in progress, this register is updated to reflect the destination address of the current AXI transfer.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR[63:48]															

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rw

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR[47:32]															

rw

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															

rw

Bit field	Name	Description
63:0	ADDR	Current Destination Address of MDMA transfer: Updated after each destination transfer. The DINC field in the MDMA_CHnCTRL register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer.

16.5.2.3 MDMA Channel n Block Transfer Size register (MDMA_CHnBTS)

Address offset: 0x0110 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000

When MDMA is the flow controller, the MDMA uses this register before the channel is enabled for block-size.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										NUM[21:16]					

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUM[15:0]															

rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21:0	NUM	Block Transfer Size. The number programmed into NUM field indicates the total number of data of width MDMA_CHnCTRL.STW to be transferred in a MDMA block transfer. Block Transfer Size = NUM + 1. When the transfer starts, the read-back value is the total number of data items already read from the source peripheral, regardless of who is the flow controller. When the

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Bit field	Name	Description
		source or destination peripheral is assigned as the flow controller, the value before the transfer starts saturates at 8191, but the actual block size can be greater.

16.5.2.4 MDMA Channel n Control register (MDMA_CHnCTRL)

Address offset: 0x0118 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000 0000 1200

This register contains fields that control the MDMA transfer. This register should be programmed prior to enabling the channel except for LLI-based multi-block transfer. When LLI-based multi-block transfer is enabled, this register is loaded from the corresponding location of the LLI and it can be varied on a block-by-block basis within a MDMA transfer. The software is not allowed to directly update this register through MDMA slave interface. Any write to this register during LLI based multi-block transfer is ignored.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
SRLLI	LSRLLI	Reserved			BTIOC	Reserved		DBL[7:0]							
rw	rw				rw			rw							
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DBLEN	SBL[7:0]								SBLEN	Reserved					
rw	rw								rw						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	NPLWEN	Reserved								DSTMSIZE[3:0]				SRCMSIZE[3:2]	
	rw									rw				rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRCMSIZE[1:0]		DTW[2:0]			STW[2:0]			Reserved	DINC	Reserved	SINC	Reserved	DMS	Reserved	SMS
rw		rw			rw				rw		rw		rw		rw

Bit field	Name	Description
63	SRLLI	Linked List Item (LLI) valid. Indicates whether the linked list item fetched from the memory is valid. **LLI based multi-block transfer:** This register is loaded from the LLI. Hence, the software is not allowed to directly update this register through the MDMA slave interface. This field can be used to dynamically extend the LLI by the software. On noticing this bit as 0, MDMA discards the LLI and generates the LLI Invalid Error Interrupt if the corresponding channel error interrupt mask bit is set to 0. In the case of LLI pre-fetching, the LLI Invalid Error interrupt is not generated even if this bit is seen to be 0 for the pre-fetched LLI. In this case, MDMA attempts the LLI fetch operation again after completing the current block transfer and generates the LLI Invalid Error interrupt only if this bit is still seen to be 0.

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Bit field	Name	Description
		This error condition causes the MDMA to halt the corresponding channel gracefully. MDMA waits until software writes (any value) to MDMA Channel n Block Transfer Resume Request register to indicate valid LLI availability before attempting another LLI read operation. This bit is cleared to 0 and written back to the corresponding LLI location after block transfer completion when LLI writeback option is enabled. Hence, for LLI-based multi-block transfers, the software might manipulate/redefine any descriptor with this bit set to 0 if LLI write-back option is enabled. 0x0: Indicates LLI content is Invalid 0x1: Indicates LLI content is Valid
62	LSRLLI	Last Linked List Item (LLI). Indicates whether the linked list item fetched from the memory is the last one or not. **LLI based multi-block transfer:** MDMA uses this bit to decide if another LLI fetch is needed in the current DMA transfer. ■ If this bit is 0, MDMA fetches the next LLI from the address pointed out by LLP field in the current LLI. ■ If this bit is 1, MDMA understands that current block is the final block in the dma transfer and ends the dma transfer once the AMBA transfer corresponding to the current block completes. 0x0: Indicates LLI content is not the last one 0x1: Indicates LLI content is the last one
61:59	Reserved	Reserved, the reset value must be maintained.
58	BTIOC	Interrupt On Completion of Block Transfer. This bit is used to control the block transfer completion interrupt generation on a block by block basis for linked list based multi-block transfers. Writing 1 to this register field enables MDMA_CHnINTSTS register Block Transfer Done field (bit 0) if this interrupt generation is enabled in MDMA_CHnINTEN register and the external interrupt output is is asserted if this interrupt generation is enabled in MDMA_CHnINTEN register. 0x0: Disables MDMA_CHnINTSTS register Block Transfer Done field 0x1: Enables MDMA_CHnINTSTS register Block Transfer Done field *Note: If a linked-list-based multi-block transfer is not used for both source and destination (for instance if source and destination use contiguous address or auto-reload-based multi-block transfer), the value of this field cannot be modified per block. Additionally, the value programmed before the channel is enabled is used for all the blocks in the DMA transfer.*
57:56	Reserved	Reserved, the reset value must be maintained.
55:48	DBL	Destination Burst Length. AXI Burst length used for destination data transfer. The specified burst length is used for destination data transfer till the extent possible; remaining transfers use maximum possible value that is less than or equal to 128. The maximum value of DBL is limited by 128.

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Bit field	Name	Description
		Note: The DBL setting may not be honored towards endto-block transfers, the end of a transaction (only applicable to non-memory peripharals), and during 4K boundary crossings.
47	DBLEN	Destination Burst Length Enable. If this bit is set to 1, MDMA uses the value of DBL as AXI Burst length for destination data transfer till the extent possible; remaining transfers use maximum possible burst length. If this bit is set to 0, MDMA uses any possible value which is less than or equal to 128 as AXI Burst length for destination data transfer.
46:39	SBL	Source Burst Length. AXI Burst length used for source data transfer. The specified burst length is used for source data transfer till the extent possible; remaining transfers use maximum possible value that is less than or equal to 128. The maximum value of SBL is limited by 128.
38	SBLEN	Source Burst Length Enable. If this bit is set to 1, MDMA uses the value of SBL as AXI Burst length for source data transfer till the extent possible; remaining transfers use maximum possible burst length. If this bit is set to 0, MDMA uses any possible value which is less than or equal to 128 as AXI Burst length for source data transfer.
37:31	Reserved	Reserved, the reset value must be maintained.
30	NPLWEN	Non Posted Last Write Enable. This bit decides whether posted writes can be used throughout the block transfer. 0x0: Posted writes may be used throughout the block transfer. 0x1: Posted writes may be used till the end of the block (inside a block) and the last write in the block must be non-posted. This is to synchronize block completion interrupt generation to the last write data reaching the end memory/peripheral.
29:22	Reserved	Reserved, the reset value must be maintained.
21:18	DSTMSIZE	Destination Burst Transaction Length. Number of data items, each of width MDMA_CHnCTRL.DTW, to be written to the destination every time a destination burst transaction request is made from the corresponding hardware or software handshaking interface. 0x0: 1 Data Item read from Destination in the burst transaction 0x1: 4 Data Item read from Destination in the burst transaction 0x2: 8 Data Item read from Destination in the burst transaction 0x3: 16 Data Item read from Destination in the burst transaction 0x4: 32 Data Item read from Destination in the burst transaction 0x5: 64 Data Item read from Destination in the burst transaction 0x6: 128 Data Item read from Destination in the burst transaction Others: Reserved *Note: This Value is not related to the AXI awlen signal.*
17:14	SRCMSIZE	Source Burst Transaction Length. Number of data items, each of width MDMA_CHnCTRL.STW, to be read from the source every time a source burst transaction request is made from the corresponding

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Bit field	Name	Description
		hardware or software handshaking interface. 0x0: 1 Data Item read from Source in the burst transaction 0x1: 4 Data Item read from Source in the burst transaction 0x2: 8 Data Item read from Source in the burst transaction 0x3: 16 Data Item read from Source in the burst transaction 0x4: 32 Data Item read from Source in the burst transaction 0x5: 64 Data Item read from Source in the burst transaction 0x6: 128 Data Item read from Source in the burst transaction Others: Reserved *Note: This Value is not related to the AXI arlen signal.*
13:11	DTW	Destination Transfer Width. Mapped to AXI bus awsize, this value must be less than or equal to 64. 0x0: Destination transfer width is 8 bits 0x1: Destination transfer width is 16 bits 0x2: Destination transfer width is 32 bits 0x3: Destination transfer width is 64 bits Others: Reserved
10:8	STW	Source Transfer Width. Mapped to AXI bus arsize, this value must be less than or equal to 64. 0x0: Source transfer width is 8 bits 0x1: Source transfer width is 16 bits 0x2: Source transfer width is 32 bits 0x3: Source transfer width is 64 bits Others: Reserved
7	Reserved	Reserved, the reset value must be maintained.
6	DINC	Destination Address Increment. Indicates whether to increment the destination address on every destination transfer. If the device is writing data from a destination peripheral FIFO with a fixed address, then set this field to 'No change'. 0x0: Increment 0x1: No Change *Note: Increment aligns the address to the next MDMA_CHnCTRL.DTW boundary.*
5	Reserved	Reserved, the reset value must be maintained.
4	SINC	Source Address Increment. Indicates whether to increment the source address on every destination transfer. If the device is writing data from a source peripheral FIFO with a fixed address, then set this field to 'No change'. 0x0: Increment 0x1: No Change *Note: Increment aligns the address to the next MDMA_CHnCTRL.STW boundary.*
3	Reserved	Reserved, the reset value must be maintained.
2	DMS	Destination Master Select.

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Bit field	Name	Description
		Identifies the Master Interface layer from which the destination device (peripheral or memory) is accessed. 0x0: Destination device on Master-1 interface layer 0x1: Destination device on Master-2 interface layer
1	Reserved	Reserved, the reset value must be maintained.
0	SMS	Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed. 0x0: Source device on Master-1 interface layer 0x1: Source device on Master-2 interface layer

16.5.2.5 MDMA Channel n Configuration register (MDMA_CHnCFG)

Address offset: 0x0120 + 0x100 × n (n = 0 to 15)

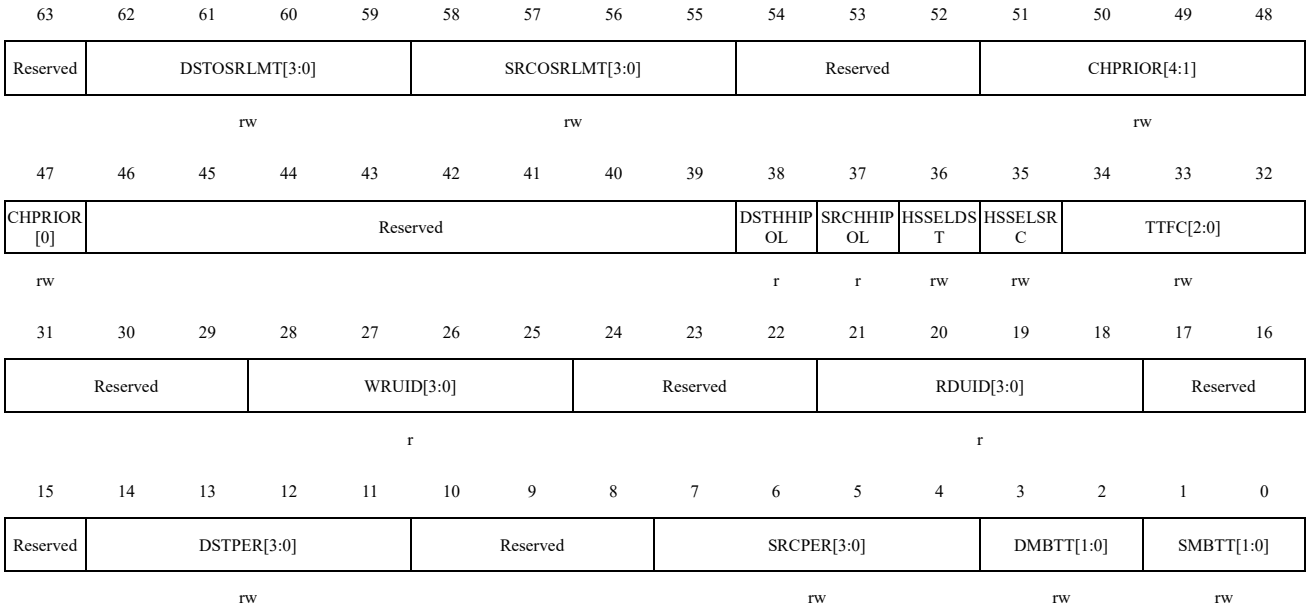
Reset value: 0x0007 801B 0000 0000

This register contains fields that configure the DMA transfer. This register should be programmed prior to enabling the channel.

Bits [63:32] of the channel configuration register remains fixed for all blocks of a multi-block transfer and can be programmed only when channel is disabled.

Bits [3:0] of the channel configuration register can be programmed even when channel is enabled.

Software clears these bits to end the multi-block transfers. For Contiguous-Address and Auto-Reloading-based multi-block transfers (if neither source nor destination peripheral uses Linked-List-based multi-block transfers), if the corresponding multi-block type selection bits namely SMBTT and/or DMBTT bits are seen to be 2'b00 at the end of a block transfer, the MDMA understands that the previous block was the final block in the transfer and completes the DMA transfer operation.



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Bit field	Name	Description
63	Reserved	Reserved, the reset value must be maintained.
62:59	DSTOSRLMT	Destination Outstanding Request Limit. ■ Maximum outstanding request supported is 16 ■ Destination Outstanding Request Limit = DSTOSRLMT + 1
58:55	SRCOSRLMT	Source Outstanding Request Limit. ■ Maximum outstanding request supported is 16 ■ Source Outstanding Request Limit = SRCOSRLMT + 1
54:52	Reserved	Reserved, the reset value must be maintained.
51:47	CHPRIOR	Channel Priority. A priority of 15 is the highest priority, and 0 is the lowest. This field must be programmed within the following range: 0 to 15. A programmed value outside this range will cause erroneous behavior.
46:39	Reserved	Reserved, the reset value must be maintained.
38	DSTHHIPOL	Destination Hardware Handshaking Interface Polarity. 0x0: Active HIGH 0x1: Active LOW *Note: When all peripherals use the hardware handshake interface, the polarity of this interface must be configured as high active.*
37	SRCHHIPOL	Source Hardware Handshaking Interface Polarity. 0x0: Active HIGH 0x1: Active LOW *Note: When all peripherals use the hardware handshake interface, the polarity of this interface must be configured as high active.*
36	HSSELDST	Destination Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces (hardware or software) is active for destination requests on this channel. If the destination peripheral is memory, then this bit is ignored. 0x0: Hardware Handshaking Interface is used for the Destination peripheral 0x1: Software Handshaking Interface is used for the Destination peripheral
35	HSSELSRC	Source Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces (hardware or software) is active for source requests on this channel. If the source peripheral is memory, then this bit is ignored. 0x0: Hardware Handshaking Interface is used for the Source peripheral 0x1: Software Handshaking Interface is used for the Source peripheral
34:32	TTFC	Transfer Type and Flow Control. The following transfer types are supported. ■ Memory to Memory ■ Memory to Peripheral ■ Peripheral to Memory

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Bit field	Name	Description
		■ Peripheral to Peripheral Flow Control can be assigned to the MDMA, the source peripheral, or hte destination peripheral. 0x0: Transfer type is Memory to Memory and Flow Controller is MDMA 0x1: Transfer type is Memory to Peripheral and Flow Controller is MDMA 0x2: Transfer type is Peripheral to Memory and Flow Controller is MDMA 0x3: Transfer type is Peripheral to Peripheral and Flow Controller is MDMA 0x4: Transfer type is Peripheral to Memory and Flow Controller is Source Peripheral 0x5: Transfer type is Peripheral to Peripheral and Flow Controller is Source Peripheral 0x6: Transfer type is Memory to Peripheral and Flow Controller is Destination Peripheral 0x7: Transfer type is Peripheral to Peripheral and Flow Controller is Destination Peripheral
31:29	Reserved	Reserved, the reset value must be maintained.
28:25	WRUID	Defines the number of AXI Unique ID's supported for the AXI Write Channel. The value programmed must be less than or equal to 2. Otherwise, it is limited by the value 2.
24:22	Reserved	Reserved, the reset value must be maintained.
21:18	RDUID	Defines the number of AXI Unique ID's supported for the AXI Read Channel. The value programmed must be less than or equal to 2. Otherwise, it is limited by the value 2.
17:15	Reserved	Reserved, the reset value must be maintained.
14:11	DSTPER	Assigns a hardware handshaking interface (0 to 15) to the destination of Channel x if the HSSELDST field is 0; otherwise, this field is ignored. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. *Note: For correct MDMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.*
10:8	Reserved	Reserved, the reset value must be maintained.
7:4	SRCPER	Assigns a hardware handshaking interface (0 to 15) to the source of Channel x if the HSSELSRC field is 0; otherwise, this field is ignored. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. *Note: For correct MDMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.*
3:2	DMBTT	Destination Multi Block Transfer Type. These bits define the type of multi-block transfer used for destination peripheral. If the type selected is Contiguous, the MDMA_CHnDA register is loaded with the value of the end source address of previous block + 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Reload, the MDMA_CHnDA register is reloaded from the initial value of ADDR at the end of every block for multi-block transfers. A new block transfer

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Bit field	Name	Description
		is then initiated. If the type selected is Linked List, the MDMA_CHnDA register is loaded from the Linked List if MDMA_CHnCTRL.SRLLI bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. MDMA_CHnCTRL and MDMA_CHnBTS registers are loaded from their initial values or from the linked list (if MDMA_CHnCTRL.SRLLI bit is set to 1) at the end of every block for multi-block transfers based on the multi-block transfer type programmed for source and destination peripherals. Contiguous transfer on both source and destination peripheral is not a valid multi-block transfer configuration. 0x0: Contiguous Multiblock Type used for Destination Transfer 0x1: Reload Multiblock Type used for Destination Transfer 0x2: Reserved 0x3: Linked List based Multiblock Type used for Destination Transfer
1:0	SMBTT	Source Multi Block Transfer Type. These bits define the type of multi-block transfer used for source peripheral. If the type selected is Contiguous, the MDMA_CHnSA register is loaded with the value of the end source address of previous block + 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Reload, the MDMA_CHnSA register is reloaded from the initial value of ADDR at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Linked List, the MDMA_CHnSA register is loaded from the Linked List if MDMA_CHnCTRL.SRLLI bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. MDMA_CHnCTRL and MDMA_CHnBTS registers are loaded from their initial values or from the linked list (if MDMA_CHnCTRL.SRLLI bit is set to 1) at the end of every block for multi-block transfers based on the multi-block transfer type programmed for source and destination peripherals. Contiguous transfer on both source and destination peripheral is not a valid multi-block transfer configuration. 0x0: Contiguous Multiblock Type used for Source Transfer 0x1: Reload Multiblock Type used for Source Transfer 0x2: Reserved 0x3: Linked List based Multiblock Type used for Source Transfer

16.5.2.6 MDMA Channel n Linked List Pointer register (MDMA_CHnLLP)

Address offset: 0x0128 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000 0000 0000

This is the Linked List Pointer register. This register must be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if linked-list-based block chaining is enabled. This register is updated with

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new value of linked list pointer during the LLI update stage of dma transfer.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR[63:48]															
rw															

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR[47:32]															
rw															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:6]										Reserved					LMS
rw															r

Bit field	Name	Description
63:6	ADDR	Starting Address Memory of LLI block. Starting Address In Memory of next LLI if block chaining is enabled. The six LSBs of the starting address are not stored because the address is assumed to be aligned to a 64-byte boundary. LLI access always uses the burst size (arsize/awsize) that is same as the data bus width and cannot be changed or programmed to anything other than this. Burst length (awlen/arlen) is chosen based on the data bus width so that the access does not cross one complete LLI structure of 64 bytes. MDMA will fetch the entire LLI (40 bytes) in one AXI burst if the burst length is not limited by other settings.
5:1	Reserved	Reserved, the reset value must be maintained.
0	LMS	LLI master Select. This bit identifies the AXI layer/interface where the memory device that stores the next linked list item resides. 0x0: next Linked List item resides on AXI Master1 interface 0x1: next Linked List item resides on AXI Master2 interface

16.5.2.7 MDMA Channel n Status register (MDMA_CHnSTS)

Address offset: 0x0130 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000 0000 0000

Channel n Status Register contains fields that indicate the status of DMA transfers for Channel n.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reserved															

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47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reserved	LEFTDATA[14:0]														
r															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										CBTSIZE[21:16]					
										r					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CBTSIZE[15:0]															
r															

Bit field	Name	Description
63:47	Reserved	Reserved, the reset value must be maintained.
46:32	LEFTDATA	Data Left in FIFO. This bit indicates the total number of data left in MDMA channel FIFO after completing the current block transfer. The width of the data in channel FIFO is equal to MDMA_CHnCTRL.STW. For normal block transfer completion without errors, LEFTDATA = 0. If any error occurs during the dma transfer, the block transfer might be terminated early and in such a case, LEFTDATA indicates the data remaining in channel FIFO which could not be transferred to destination peripheral. This field is cleared to zero on enabling the channel. *Note: If MDMA_CHnCTRL.DTW > MDMA_CHnCTRL.STW, there may be residual data left in the FIFO which is not enough to form one MDMA_CHnCTRL.STW of data and LEFTDATA will return 0 in this case.*
31:22	Reserved	Reserved, the reset value must be maintained.
21:0	CBTSIZE	Completed Block Transfer Size. This bit indicates the total number of data of width MDMA_CHnCTRL.STW transferred for the previous block transfer. For normal block transfer completion without any errors, this value will be equal to the value programmed in NUM field of MDMA_CHnBTS register. If any error occurs during the dma transfer, the block transfer might be terminated early and in such a case, this value indicates the actual data transferred without error in the current block. This field is cleared to zero on enabling the channel.

16.5.2.8 MDMA Channel n Software Handshake Source register (MDMA_CHnSHSRC)

Address offset: 0x0138 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SHLRWE	SHLR	SHSRWE	SHSR	SHRWE	SHR
										w	rw	w	rw	w	rw

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	SHLRWE	Write Enable bit for Software Handshake Last Request for Channel Source. 0x0: Disables write to the SHLR bit 0x1: Enables write to the SHLR bit
4	SHLR	Software Handshake Last Request for Channel Source. This bit is used to request LAST dma source data transfer if software handshaking method is selected for the source of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channel n or if the source of Channel n is not the flow controller. SHR bit must be set to 1 for MDMA to treat it as a valid software handshaking request. If SHSR bit is set to 1, the LAST request is for SINGLE dma transaction (AXI burst length = 1), else the request is treated as a BURST transaction request. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only MDMA can clear this bit. 0x0: Source peripheral indication that the curent transfer is not the last transfer 0x1: Source peripheral indication to dmac that the current transfer is the last transfer *Note: SHLR bit is written only if the corresponding write enable bit, SHLRWE is asserted on the same register write operation and if the Channel n is enabled in the MDMA_CHEN register. This allows software to set a bit in this register without performing a read-modified write operation.*
3	SHSRWE	Write Enable bit for Software Handshake Single Request for Channel Source. 0x0: Disables write to the SHSR bit 0x1: Enables write to the SHSR bit
2	SHSR	Software Handshake Single Request for Channel Source. This bit is used to request SINGLE (AXI burst length = 1) dma source data transfer if software handshaking method is selected for the source of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channel n. The functionality of this field depends on whether the peripheral is the flow controller. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only MDMA can clear this bit. 0x0: Source peripheral is not requesting for a single transfe

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Bit field	Name	Description
		0x1: Source peripheral request for a single dma transfer *Note: SHSR bit is written only if the corresponding write enable bit, SHSRWE is asserted on the same register write operation and if the Channel n is enabled in the MDMA_CHEN register. This allows software to set a bit in this register without performing a read-modified write operation.*
1	SHRWE	Write Enable bit for Software Handshake Request for Channel Source. 0x0: Disables write to the SHR bit 0x1: Enables write to the SHR bit *Note: This bit always returns 0 on a read back.*
0	SHR	Software Handshake Request for Channel Source. This bit is used to request dma source data transfer if software handshaking method is selected for the source of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channel n. The functionality of this field depends on whether the peripheral is the flow controller or not. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only MDMA can clear this bit. 0x0: Source peripheral is not requesting for a burst transfer 0x1: Source peripheral request for a burst dma transfer *Note: SHR bit is written only if the corresponding write enable bit, SHRWE is asserted on the same register write operation and if the Channel n is enabled in the MDMA_CHEN register. This allows software to set a bit in this register without performing a read-modified write operation.*

16.5.2.9 MDMA Channel n Software Handshake Destination register (MDMA_CHnSHDST)

Address offset: 0x0140 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SHLRWE	SHLR	SHSRWE	SHSR	SHRWE	SHR
										w	rw	w	rw	w	rw

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	SHLRWE	Write Enable bit for Software Handshake Last Request for Channel Destination. 0x0: Disables write to the SHLR bit 0x1: Enables write to the SHLR bit

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Bit field	Name	Description
		Note: This bit always returns 0 on a read back.
4	SHLR	Software Handshake Last Request for Channel Destination. This bit is used to request LAST dma destination data transfer if software handshaking method is selected for the destination of the corresponding channel. This bit is ignored if software handshaking is not enabled for the destination of the Channel n or if the destination of Channel n is not the flow controller. SHR bit must be set to 1 for MDMA to treat it as a valid software handshaking request. If SHSR bit is set to 1, the LAST request is for SINGLE dma transaction (AXI burst length = 1), else the request is treated as a BURST transaction request. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only MDMA can clear this bit. 0x0: Destination peripheral indication that the curent transfer is not the last transfer 0x1: Destination peripheral indication to dmac that the current transfer is the last transfer *Note: SHLR bit is written only if the corresponding write enable bit, SHLRWE is asserted on the same register write operation and if the Channel n is enabled in the MDMA_CHEN register. This allows software to set a bit in this register without performing a read-modified write operation.*
3	SHSRWE	Write Enable bit for Software Handshake Single Request for Channel Destination. 0x0: Disables write to the SHSR bit 0x1: Enables write to the SHSR bit *Note: This bit always returns 0 on a read back.*
2	SHSR	Software Handshake Single Request for Channel Destination. This bit is used to request SINGLE (AXI burst length = 1) dma destination data transfer if software handshaking method is selected for the destination of the corresponding channel. This bit is ignored if software handshaking is not enabled for the destination of the Channel n. The functionality of this field depends on whether the peripheral is the flow controller. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only MDMA can clear this bit. 0x0: Destination peripheral is not requesting for a single transfe 0x1: Destination peripheral request for a single dma transfer *Note: SHSR bit is written only if the corresponding write enable bit, SHSRWE is asserted on the same register write operation and if the Channel n is enabled in the MDMA_CHEN register. This allows software to set a bit in this register without performing a read-modified write operation.*
1	SHRWE	Write Enable bit for Software Handshake Request for Channel Destination. 0x0: Disables write to the SHR bit 0x1: Enables write to the SHR bit *Note: This bit always returns 0 on a read back.*
0	SHR	Software Handshake Request for Channel Destination.

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Bit field	Name	Description
		This bit is used to request dma destination data transfer if software handshaking method is selected for the destination of the corresponding channel. This bit is ignored if software handshaking is not enabled for the destination of the Channel n. The functionality of this field depends on whether the peripheral is the flow controller. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only MDMA can clear this bit. 0x0: Destination peripheral is not requesting for a burst transfer 0x1: Destination peripheral request for a burst dma transfer *Note: SHR bit is written only if the corresponding write enable bit, SHRWE is asserted on the same register write operation and if the Channel n is enabled in the MDMA_CHEN register. This allows software to set a bit in this register without performing a read-modified write operation.*

16.5.2.10 MDMA Channel n Block Transfer Resume Request register (MDMA_CHnBTRR)

Address offset: 0x0148 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000

This register is used during Linked List based multi-block transfer.

For Linked-List-based multi-block transfer, SRLLI bit in MDMA_CHnCTRL register indicates whether the linked list item fetched from the memory is valid (0: LLI is invalid, 1: LLI is valid). On noticing this bit as 0, MDMA discards the LLI and generates LLI Invalid Error Interrupt if the corresponding channel error interrupt mask bit is set to 0. This error condition causes the MDMA to halt the corresponding channel gracefully. MDMA waits till software writes (any value) to this register to indicate valid LLI availability, before attempting another LLI read operation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															RESREQ
															w

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	RESREQ	Block Transfer Resume Request during Linked-List-based multi-block transfer. 0x0: No request to resume the block transfer 0x1: Request for resuming the block transfer

16.5.2.11 MDMA Channel n AXI QoS register (MDMA_CHnAXIQOS)

Address offset: 0x0158 + 0x100 × n (n = 0 to 15)

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Reset value: 0x0000 0000

This register is allowed to be updated only when the channel is disabled, which means that it remains fixed for the entire DMA transfer.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ARQOS[3:0]				AWQOS[3:0]			
									r				r		

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:4	ARQOS	AXI ARQOS. These bits form the arqos output of AXI4 master interface.
3:0	AWQOS	AXI AWQOS. These bits form the awqos output of AXI4 master interface.

16.5.2.12 MDMA Channel n Interrupt Status Enable register (MDMA_CHnINTSTSEN)

Address offset: 0x0180 + 0x100 × n (n = 0 to 15)

Reset value: 0xFFFF FFFF

Writing 1 to specific field enables the corresponding interrupt status generation in Channel n Interrupt Status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHA	CHD	CHS	CHSS	CHLC	Reserved					SIWOHE	Reserved	SIWOCEE	SIRTWOE	SIWTROE	SIDE
rw	rw	rw	rw	rw						rw		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SIMBTE	SLIE	LWSE	LRSE	LWDE	LRDE	DSTSE	SRCSE	DSTDE	SRCDE	DSTTC	SRCTC	Reserved	DMATD	BLKTD
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

Bit field	Name	Description
31	CHA	Channel Aborted. 0x0: Disable the generation of Channel Aborted Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Channel Aborted Interrupt in MDMA_CHnINTSTS
30	CHD	Channel Disabled. 0x0: Disable the generation of Channel Disabled Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Channel Disabled Interrupt in MDMA_CHnINTSTS
29	CHS	Channel Suspended.

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Bit field	Name	Description
		0x0: Disable the generation of Channel Suspended Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Channel Suspended Interrupt in MDMA_CHnINTSTS
28	CHSS	Channel Source Suspended. 0x0: Disable the generation of Channel Source Suspended Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Channel Source Suspended Interrupt in MDMA_CHnINTSTS
27	CHLC	Channel Lock Cleared. 0x0: Disable the generation of Channel Lock Cleared Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Channel Lock Cleared Interrupt in MDMA_CHnINTSTS
26:22	Reserved	Reserved, the reset value must be maintained.
21	SIWOHE	Slave Interface Write On Hold Error. 0x0: Disable the generation of Slave Interface Write On Hold Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Slave Interface Write On Hold Error Interrupt in MDMA_CHnINTSTS
20	Reserved	Reserved, the reset value must be maintained.
19	SIWOCEE	Slave Interface Write On Channel Enabled Error. 0x0: Disable the generation of Slave Interface Write On Channel enabled Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Slave Interface Write On Channel enabled Error Interrupt in MDMA_CHnINTSTS
18	SIRTWOE	Slave Interface Read to Write Only Error. 0x0: Disable the generation of Slave Interface Read to write Only Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Slave Interface Read to write Only Error Interrupt in MDMA_CHnINTSTS
17	SIWTROE	Slave Interface Write to Read Only Error. 0x0: Disable the generation of Slave Interface Write to Read Only Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Slave Interface Write to Read Only Error Interrupt in MDMA_CHnINTSTS
16	SIDE	Slave Interface Decode Error. 0x0: Disable the generation of Slave Interface Decode Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Slave Interface Decode Error Interrupt in MDMA_CHnINTSTS
15	Reserved	Reserved, the reset value must be maintained.
14	SIMBTE	Slave Interface Multi Block Type Error. 0x0: Disable the generation of Slave Interface Multi Block type Error Interrupt in MDMA_CHnINTSTS

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Bit field	Name	Description
		0x1: Enable the generation of Slave Interface Multi Block type Error Interrupt in MDMA_CHnINTSTS
13	SLIE	LLI Invalid Error. 0x0: Disable the generation of LLI Invalid Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of LLI Invalid Error Interrupt in MDMA_CHnINTSTS
12	LWSE	LLI Write Slave Error. 0x0: Disable the generation of LLI Write Slave Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of LLI Write Slave Error Interrupt in MDMA_CHnINTSTS
11	LRSE	LLI Read Slave Error. 0x0: Disable the generation of LLI Read Slave Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of LLI Read Slave Error Interrupt in MDMA_CHnINTSTS
10	LWDE	LLI Write Decode Error. 0x0: Disable the generation of LLI Write Decode Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of LLI Write Decode Error Interrupt in MDMA_CHnINTSTS
9	LRDE	LLI Read Decode Error. 0x0: Disable the generation of LLI Read Decode Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of LLI Read Decode Error Interrupt in MDMA_CHnINTSTS
8	DSTSE	Destination Slave Error. 0x0: Disable the generation of Destination Slave Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Destination Slave Error Interrupt in MDMA_CHnINTSTS
7	SRCSE	Source Slave Error. 0x0: Disable the generation of Source Slave Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Source Slave Error Interrupt in MDMA_CHnINTSTS
6	DSTDE	Destination Decode Error. 0x0: Disable the generation of Destination Decode Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Destination Decode Error Interrupt in MDMA_CHnINTSTS
5	SRCDE	Source Decode Error. 0x0: Disable the generation of Source Decode Error Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Source Decode Error Interrupt in MDMA_CHnINTSTS
4	DSTTC	Destination Transaction Completed. 0x0: Disable the generation of Destination Transaction Completed Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Destination Transaction Completed Interrupt in MDMA_CHnINTSTS

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Bit field	Name	Description
3	SRCTC	Source Transaction Completed. 0x0: Disable the generation of Source Transaction Completed Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Source Transaction Completed Interrupt in MDMA_CHnINTSTS
2	Reserved	Reserved, the reset value must be maintained.
1	DMATD	DMA Transfer Done. 0x0: Disable the generation of DMA Transfer Done Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of DMA Transfer Done Interrupt in MDMA_CHnINTSTS
0	BLKTD	Block Transfer Done. 0x0: Disable the generation of Block Transfer Done Interrupt in MDMA_CHnINTSTS 0x1: Enable the generation of Block Transfer Done Interrupt in MDMA_CHnINTSTS

16.5.2.13 MDMA Channel n Interrupt Status register (MDMA_CHnINTSTS)

Address offset: 0x0188 + 0x100 × n (n = 0 to 15)

Reset value: 0x0000 0000

Channel n Interrupt Status Register captures the Channel n specific interrupts.

Error Interrupt status is generated if the corresponding Status Enable bit in MDMA_CHnINTSTSEN register is set to 1. Status bit is cleared to 0 on writing 1 to the corresponding interrupt clear bit in MDMA_CHnINTCLR.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHA	CHD	CHS	CHSS	CHLC	Reserved					SIWOHE	Reserved	SIWOCEE	SIRTWOE	SIWTROE	SIDE
r	r	r	r	r						r		r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SIMBTE	SLIE	LWSE	LRSE	LWDE	LRDE	DSTSE	SRCSE	DSTDE	SRCDE	DSTTC	SRCTC	Reserved	DMATD	BLKTD
	r	r	r	r	r	r	r	r	r	r	r	r		r	r

Bit field	Name	Description
31	CHA	Channel Aborted. This indicates to the software that the corresponding channel in MDMA is aborted. 0x0: Channel is not aborted 0x1: Channel is aborted
30	CHD	Channel Disabled. This indicates to the software that the corresponding channel in MDMA is disabled. 0x0: Channel is not disabled 0x1: Channel is disabled
29	CHS	Channel Suspended. This indicates to the software that the corresponding channel in MDMA is suspended. 0x0: Channel is not suspended

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Bit field	Name	Description
		0x1: Channel is suspended
28	CHSS	Channel Source Suspended. This indicates to the software that the corresponding channel source data transfer in MDMA is suspended. 0x0: Channel Source is not suspended 0x1: Channel Source is suspended
27	CHLC	Channel Lock Cleared. This indicates to the software that the locking of the corresponding channel in MDMA is cleared. 0x0: Channel Locking is not cleared 0x1: Channel Locking is cleared
26:22	Reserved	Reserved, the reset value must be maintained.
21	SIWOHE	Slave Interface Write On Hold Error. This error occurs if an illegal write operation is performed on a register; this happens if a write operation is performed on a channel register when MDMA is in Hold mode. 0x0: Slave Interface Write On Hold Error not detected 0x1: Slave Interface Write On Hold Error detected
20	Reserved	Reserved, the reset value must be maintained.
19	SIWOCEE	Slave Interface Write On Channel Enabled Error. This error occurs if an illegal write operation is performed on a register; this happens if a write operation is performed on a register when the channel is enabled and if it is not allowed for the corresponding register as per the MDMA specification. 0x0: Slave Interface Write On Channel Enabled Error not detected 0x1: Slave Interface Write On Channel Enabled Error detected
18	SIRTWOE	Slave Interface Read to Write Only Error. This error occurs if read operation is performed to a Write Only register. 0x0: Slave Interface Read to Write Only Error not detected 0x1: Slave Interface Read to Write Only Error detected
17	SIWTROE	Slave Interface Write to Read Only Error. This error occurs if write operation is performed to a Read Only register. 0x0: Slave Interface Write to Read Only Error not detected 0x1: Slave Interface Write to Read Only Error detected
16	SIDE	Slave Interface Decode Error. Decode Error generated by MDMA during register access. This error occurs if the register access is to invalid address in Channel n register space resulting in error response by MDMA slave interface. 0x0: Slave Interface Decode Error not detected 0x1: Slave Interface Decode Error detected
15	Reserved	Reserved, the reset value must be maintained.
14	SIMBTE	Slave Interface Multi Block Type Error. This error occurs if multi-block transfer type programmed in MDMA_CHnCFG register

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Bit field	Name	Description
		(SMBTT and DMBTT) is invalid. This error condition causes the MDMA to halt the corresponding channel gracefully; Error Interrupt is generated if the corresponding channel error interrupt mask bit is set to 0 and the channel waits till software writes (any value) to MDMA_CHnBTRR to indicate valid multiblock transfer type availability. 0x0: Slave Interface Multi-block transfer type Error not detected 0x1: Slave Interface Multi-block transfer type Error detected
13	SLIE	LLI Invalid Error. This error occurs if MDMA_CHnCTRL.SRLLI bit is seen to be 0 during MDMA LLI fetch phase. This error condition causes the MDMA to halt the corresponding channel gracefully; Error Interrupt is generated if the corresponding channel error interrupt mask bit is set to 0 and the channel waits till software writes (any value) to MDMA_CHnBTRR to indicate valid LLI availability. In the case of LLI pre-fetching, LLI Invalid Error Interrupt is not generated even if MDMA_CHnCTRL.SRLLI bit is seen to be 0 for the pre-fetched LLI. In this case, MDMA controller re-attempts the LLI fetch operation after completing the current block transfer and generates LLI Invalid Error Interrupt only if MDMA_CHnCTRL.SRLLI bit is still seen to be 0. 0x0: LLI Invalid Error not detected 0x1: LLI Invalid type Error detected
12	LWSE	LLI Write Slave Error. Slave Error detected by Master Interface during LLI writeback operation. This error occurs if the slave interface on which LLI resides issues a Slave Error. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: LLI Write Slave Error not detected 0x1: LLI Write Slave Error detected
11	LRSE	LLI Read Slave Error. Slave Error detected by Master Interface during LLI read operation. This error occurs if the slave interface on which LLI resides issues a Slave Error. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: LLI Read Slave Error not detected 0x1: LLI Read Slave Error detected
10	LWDE	LLI Write Decode Error. Decode Error detected by Master Interface during LLI writeback operation. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: LLI Write Decode Error not detected 0x1: LLI Write Decode Error detected
9	LRDE	LLI Read Decode Error. Decode Error detected by Master Interface during LLI read operation. This error occurs

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Bit field	Name	Description
		if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: LLI Read Decode Error not detected 0x1: LLI Read Decode Error detected
8	DSTSE	Destination Slave Error. Slave Error detected by Master Interface during destination data transfer. This error occurs if the slave interface to which the data is written issues a Slave Error. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: Destination Slave Error not detected 0x1: Destination Slave Error detected
7	SRCSE	Source Slave Error. Slave Error detected by Master Interface during source data transfer. This error occurs if the slave interface to which the data is written issues a Slave Error. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: Source Slave Error not detected 0x1: Source Slave Error detected
6	DSTDE	Destination Decode Error. Decode Error detected by Master Interface during destination data transfer. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: Destination Decode Error not detected 0x1: Destination Decode Error detected
5	SRCDE	Source Decode Error. Decode Error detected by Master Interface during source data transfer. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the MDMA to disable the corresponding channel gracefully; the MDMA_CHEN.CHn bit which received the error is set to 0. 0x0: Source Decode Error not detected 0x1: Source Decode Error detected
4	DSTTC	Destination Transaction Completed. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CHnINTCLR register or on enabling the channel (needed when interrupt is not enabled.) 0x0: Destination Transaction Completed not detected 0x1: Destination Transaction Completed detected
3	SRCTC	Source Transaction Completed. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in MDMA_CHnINTCLR register or on enabling the channel (needed when interrupt is not

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Bit field	Name	Description
		enabled.) 0x0: Source Transaction Completed not detected 0x1: Source Transaction Completed detected
2	Reserved	Reserved, the reset value must be maintained.
1	DMATD	DMA Transfer Done. This indicates to the software that the MDMA has completed the requested DMA transfer. The MDMA sets this bit to 1 along with setting BLKTD bit to 1 when the last block transfer is completed. 0x0: DMA Transfer not completed 0x1: DMA Transfer Completed
0	BLKTD	Block Transfer Done. This indicates to the software that the MDMA has completed the requested block transfer. The MDMA sets this bit to 1 when the transfer is successfully completed. 0x0: Block Transfer not completed 0x1: Block Transfer completed

16.5.2.14 MDMA Channel n Interrupt Signal Enable register (MDMA_CHnINTSGLEN)

Address offset: 0x0190 + 0x100 × n (n = 0 to 15)

Reset value: 0xFFFF FFFF

This register contains fields that are used to enable the generation of port level interrupt at the channel level.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHA	CHD	CHS	CHSS	CHLC	Reserved					SIWOHE	Reserved	SIWOCEE	SIRTWOE	SIWTROE	SIDE
rw	rw	rw	rw	rw						rw		rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SIMBTE	SLIE	LWSE	LRSE	LWDE	LRDE	DSTSE	SRCSE	DSTDE	SRCDE	DSTTC	SRCTC	Reserved	DMATD	BLKTD
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

Bit field	Name	Description
31	CHA	Channel Aborted. 0x0: Disable the generation of Channel Aborted Interrupt to generate a port level interrupt 0x1: Enable the generation of Channel Aborted Interrupt to generate a port level interrupt
30	CHD	Channel Disabled. 0x0: Disable the generation of Channel Disabled Interrupt to generate a port level interrupt

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Bit field	Name	Description
		0x1: Enable the generation of Channel Disabled Interrupt to generate a port level interrupt
29	CHS	Channel Suspended. 0x0: Disable the generation of Channel Suspended Interrupt to generate a port level interrupt 0x1: Enable the generation of Channel Suspended Interrupt to generate a port level interrupt
28	CHSS	Channel Source Suspended. 0x0: Disable the generation of Channel Source Suspended Interrupt to generate a port level interrupt 0x1: Enable the generation of Channel Source Suspended Interrupt to generate a port level interrupt
27	CHLC	Channel Lock Cleared. 0x0: Disable the generation of Channel Lock Cleared Interrupt to generate a port level interrupt 0x1: Enable the generation of Channel Lock Cleared Interrupt to generate a port level interrupt
26:22	Reserved	Reserved, the reset value must be maintained.
21	SIWOHE	Slave Interface Write On Hold Error. 0x0: Disable the generation of Slave Interface Write On Hold Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Slave Interface Write On Hold Error Interrupt to generate a port level interrupt
20	Reserved	Reserved, the reset value must be maintained.
19	SIWOCEE	Slave Interface Write On Channel Enabled Error. 0x0: Disable the generation of Slave Interface Write On Channel enabled Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Slave Interface Write On Channel enabled Error Interrupt to generate a port level interrupt
18	SIRTWOE	Slave Interface Read to Write Only Error. 0x0: Disable the generation of Slave Interface Read to write Only Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Slave Interface Read to write Only Error Interrupt to generate a port level interrupt
17	SIWTROE	Slave Interface Write to Read Only Error. 0x0: Disable the generation of Slave Interface Write to Read Only Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Slave Interface Write to Read Only Error Interrupt to generate a port level interrupt
16	SIDE	Slave Interface Decode Error. 0x0: Disable the generation of Slave Interface Decode Error Interrupt to generate a port level interrupt

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Bit field	Name	Description
		0x1: Enable the generation of Slave Interface Decode Error Interrupt to generate a port level interrupt
15	Reserved	Reserved, the reset value must be maintained.
14	SIMBTE	Slave Interface Multi Block Type Error. 0x0: Disable the generation of Slave Interface Multi Block type Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Slave Interface Multi Block type Error Interrupt to generate a port level interrupt
13	SLIE	LLI Invalid Error. 0x0: Disable the generation of LLI Invalid Error Interrupt to generate a port level interrupt 0x1: Enable the generation of LLI Invalid Error Interrupt to generate a port level interrupt
12	LWSE	LLI Write Slave Error. 0x0: Disable the generation of LLI Write Slave Error Interrupt to generate a port level interrupt 0x1: Enable the generation of LLI Write Slave Error Interrupt to generate a port level interrupt
11	LRSE	LLI Read Slave Error. 0x0: Disable the generation of LLI Read Slave Error Interrupt to generate a port level interrupt 0x1: Enable the generation of LLI Read Slave Error Interrupt to generate a port level interrupt
10	LWDE	LLI Write Decode Error. 0x0: Disable the generation of LLI Write Decode Error Interrupt to generate a port level interrupt 0x1: Enable the generation of LLI Write Decode Error Interrupt to generate a port level interrupt
9	LRDE	LLI Read Decode Error. 0x0: Disable the generation of LLI Read Decode Error Interrupt to generate a port level interrupt 0x1: Enable the generation of LLI Read Decode Error Interrupt to generate a port level interrupt
8	DSTSE	Destination Slave Error. 0x0: Disable the generation of Destination Slave Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Destination Slave Error Interrupt to generate a port level interrupt
7	SRCSE	Source Slave Error. 0x0: Disable the generation of Source Slave Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Source Slave Error Interrupt to generate a port level

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Bit field	Name	Description
		interrupt
6	DSTDE	Destination Decode Error. 0x0: Disable the generation of Destination Decode Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Destination Decode Error Interrupt to generate a port level interrupt
5	SRCDE	Source Decode Error. 0x0: Disable the generation of Source Decode Error Interrupt to generate a port level interrupt 0x1: Enable the generation of Source Decode Error Interrupt to generate a port level interrupt
4	DSTTC	Destination Transaction Completed. 0x0: Disable the generation of Destination Transaction Completed Interrupt to generate a port level interrupt 0x1: Enable the generation of Destination Transaction Completed Interrupt to generate a port level interrupt
3	SRCTC	Source Transaction Completed. 0x0: Disable the generation of Source Transaction Completed Interrupt to generate a port level interrupt 0x1: Enable the generation of Source Transaction Completed Interrupt to generate a port level interrupt
2	Reserved	Reserved, the reset value must be maintained.
1	DMATD	DMA Transfer Done. 0x0: Disable the generation of DMA Transfer Done Interrupt to generate a port level interrupt 0x1: Enable the generation of DMA Transfer Done Interrupt to generate a port level interrupt
0	BLKTD	Block Transfer Done. 0x0: Disable the generation of Block Transfer Done Interrupt to generate a port level interrupt 0x1: Enable the generation of Block Transfer Done Interrupt to generate a port level interrupt

16.5.2.15 MDMA Channel n Interrupt Clear register (MDMA_CHnINTCLR)

Address offset: 0x0198 + 0x100 × n (n = 0 to 15)

Reset value: 0xFFFF FFFF

Writing 1 to specific field will clear the corresponding field in Channel n Interrupt Status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHA	CHD	CHS	CHSS	CHLC	Reserved					SIWOHE	Reserved	SIWOCEE	SIRTWOE	SIWTROE	SIDE
w	w	w	w	w						w		w	w	w	w

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SIMBTE	SLIE	LWSE	LRSE	LWDE	LRDE	DSTSE	SRCSE	DSTDE	SRCDE	DSTTC	SRCTC	Reserved	DMATD	BLKTD
	w	w	w	w	w	w	w	w	w	w	w	w		w	w

Bit field	Name	Description
31	CHA	Channel Aborted. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Channel Aborted Interrupt in MDMA_CHnINTSTS.
30	CHD	Channel Disabled. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Channel Disabled Interrupt in MDMA_CHnINTSTS.
29	CHS	Channel Suspended. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Channel Suspended Interrupt in MDMA_CHnINTSTS.
28	CHSS	Channel Source Suspended. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Channel Source Suspended Interrupt in MDMA_CHnINTSTS.
27	CHLC	Channel Lock Cleared. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Channel Lock Cleared Interrupt in MDMA_CHnINTSTS.
26:22	Reserved	Reserved, the reset value must be maintained.
21	SIWOHE	Slave Interface Write On Hold Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Slave Interface Write On Hold Error Interrupt in MDMA_CHnINTSTS.
20	Reserved	Reserved, the reset value must be maintained.
19	SIWOCEE	Slave Interface Write On Channel Enabled Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Slave Interface Write On Channel enabled Error Interrupt in MDMA_CHnINTSTS.
18	SIRTWOE	Slave Interface Read to Write Only Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Slave Interface Read to write Only Error Interrupt in MDMA_CHnINTSTS.
17	SIWTROE	Slave Interface Write to Read Only Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Slave Interface Write to Read Only Error Interrupt in MDMA_CHnINTSTS.
16	SIDE	Slave Interface Decode Error. 0x0: Inactive signal. No action taken.

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Bit field	Name	Description
		0x1: Clear the generation of Slave Interface Decode Error Interrupt in MDMA_CHnINTSTS.
15	Reserved	Reserved, the reset value must be maintained.
14	SIMBTE	Slave Interface Multi Block Type Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Slave Interface Multi Block type Error Interrupt in MDMA_CHnINTSTS.
13	SLIE	LLI Invalid Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of LLI Invalid Error Interrupt in MDMA_CHnINTSTS.
12	LWSE	LLI Write Slave Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of LLI Write Slave Error Interrupt in MDMA_CHnINTSTS.
11	LRSE	LLI Read Slave Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of LLI Read Slave Error Interrupt in MDMA_CHnINTSTS.
10	LWDE	LLI Write Decode Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of LLI Write Decode Error Interrupt in MDMA_CHnINTSTS.
9	LRDE	LLI Read Decode Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of LLI Read Decode Error Interrupt in MDMA_CHnINTSTS.
8	DSTSE	Destination Slave Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Destination Slave Error Interrupt in MDMA_CHnINTSTS.
7	SRCSE	Source Slave Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Source Slave Error Interrupt in MDMA_CHnINTSTS.
6	DSTDE	Destination Decode Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Destination Decode Error Interrupt in MDMA_CHnINTSTS.
5	SRCDE	Source Decode Error. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Source Decode Error Interrupt in MDMA_CHnINTSTS.
4	DSTTC	Destination Transaction Completed. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Destination Transaction Completed Interrupt in MDMA_CHnINTSTS.
3	SRCTC	Source Transaction Completed.

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Bit field	Name	Description
		0x0: Inactive signal. No action taken. 0x1: Clear the generation of Source Transaction Completed Interrupt in MDMA_CHnINTSTS.
2	Reserved	Reserved, the reset value must be maintained.
1	DMATD	DMA Transfer Done. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of DMA Transfer Done Interrupt in MDMA_CHnINTSTS.
0	BLKTD	Block Transfer Done. 0x0: Inactive signal. No action taken. 0x1: Clear the generation of Block Transfer Done Interrupt in MDMA_CHnINTSTS.

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Email: sales@nsing.com.sg

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

17 Super High-resolution Timer (SHRTIM1/SHRTIM2)

17.1 Introduction

The supper high-resolution timer can generate up to 12 channels of highly precise digital signals, mainly used for driving power conversion systems such as switch-mode power supplies or lighting systems, but can also be used for applications with extremely high time resolution requirements.

This timer adopts a modular architecture that can generate independent waveforms or coupled waveforms. The waveform is determined by independent timing signals (using counters and comparator units) as well as various external events (such as analog or digital feedback and synchronous signals), thus enabling the generation of a wide range of control signals (PWM, phase shift, constant Ton, etc.), meeting the requirements of most conversion topologies.

For control and monitoring purposes, the timer also has timing measurement functions and is connected to built-in ADC and DAC converters. Additionally, the timer features a light-load management mode and can handle various fault mechanisms to achieve safe shut-down.

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17.2 Main Features

- Multiple super high-resolution timing units
  - 100ps resolution, all outputs support full resolution, possibility to adjust duty cycle, frequency, and pulse width in triggered one-pulse mode
  - 6 16-bit timing units (each timing unit contains 1 independent counter and 5 compare units, compare unit 5 dedicated to ADC triggering)
  - 12 channels of output can be controlled by any timing unit, with up to 32 set/reset sources for each channel
  - Modular structure can meet the requirements of multiple independent converters equipped with 1 or 2 switches, as well as the requirements of a few large multi-switch topologies
- Up to 10 external events can be used for any timing unit
  - Programmable polarity and edge effectiveness
  - 10 events with a fast asynchronous mode
  - 10 events with a programmable digital filters
  - Spurious events filtering with blanking and windowing modes
  - All 10 external events fully mapped to any GPIO or any analog comparator
- Multiple channels connect to built-in analog peripherals
  - 10 trigger signals for ADC converters, ADC trigger signals can be fully mapped to any compare unit
  - 3 trigger signals for DAC converters
  - 7 comparators for analog signal conditioning
- Rich protection mechanisms
  - 6 fault inputs can be combined and associated with any timing unit
  - 6 fault inputs can be fully mapped to any analog comparator
  - Programmable polarity and edge effectiveness, digital filters
  - Resonant converters equipped with dedicated delay protection
- Multiple SHRTIM instances can be synchronized with external synchronization input/output
- Multi-functional output stage
  - Full resolution deadtime time insertion
  - Programmable output polarity
  - Chopping mode
- Burst mode controller, capable of handling light-load operations on multiple converters simultaneously, supporting 32-bit burst mode counting
- 8 interrupt vectors, each vector with up to 14 sources

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- 7 DMA requests, with up to 14 sources, with a burst mode for multiple registers update

17.3 SHRTIM Register

17.3.1 SHRTIM Master Timer Control Register（SHRTIM_MCTRL）

Address offset: 0x00

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BRSTDMA		MREPTUE	Reserved	PLEN	DACTRIG		Reserved		TFCNTE	TECNTE	TDCNTE	TCCNTE	TBCNTE	TACNTE	MCNTE
rw		rw	r	rw	rw		r		rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCOSRC		SYNCSTR	SYNCRS	Reserve	SYNCIN				ILV	HLF	RTG	CONT	CKPSC		
rw		rw	rw	r	rw				rw	rw	rw	rw	rw		

Bit Field	Name	Description
[31:30]	BRSTDMA	Burst DMA Update These bits define during a burst DMA transaction how the update of registers happen 00: Update done independently from the DMA burst transfer completion 01: Update done when the DMA burst transfer is completed 10: Update done on master timer roll-over following a DMA burst transfer completion. This mode only works in continuous mode. 11: Reserved
[29]	MREPTUEN	Master Timer Repetition update This bit defines whether an update occurs when the master timer repetition period is completed (either due to roll-over or reset events). MREPTUEN can be set only if BRSTDMA[1:0] = 00 or 01. 0: Repetition event does not cause register update 1: Repetition event cause register update
[28]	Reserved	Reserved, the reset value must be maintained
[27]	PLEN	Preload enable This bit enables the registers preload mechanism and defines whether the write accesses to the memory mapped registers are done into SHRTIM's active or preload registers. 0: Preload disabled: the write access is directly done into the active register 1: Preload enabled: the write access is done into the preload register
[26:25]	DACTRIG	DAC Synchronization A DAC synchronization event can be enabled and generated when the master

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		timer update occurs. These bits are defining on which output the DAC synchronization is sent (refer to Section DAC triggers for connections details). 00: No DAC trigger generated 01: Trigger generated on shrtim_dac_trg1 10: Trigger generated on shrtim_dac_trg2 11: Trigger generated on shrtim_dac_trg3
[24:23]	Reserved	Reserved, the reset value must be maintained
[22]	TFCNTEN	Timer F counter enable 0: Timer F counter disabled 1: Timer F counter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[21]	TECNTEN	Timer E counter enable 0: Timer E counter disabled 1: Timer E counter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[20]	TDCNTEN	Timer D counter enable 0: Timer D counter disabled 1: Timer D counter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[19]	TCCNTEN	Timer C counter enable 0: Timer C counter disabled 1: Timer Ccounter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[18]	TBCNTEN	Timer B counter enable 0: Timer B counter disabled 1: Timer B counter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[17]	TACNTEN	Timer A counter enable 0: Timer A counter disabled 1: Timer A counter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[16]	MCNTEN	Master timer counter enable 0: Master timer counter disabled 1: Master timer counter enabled *Note: This bit must not be changed within 8 cycles of f_{SHRTIM} clock*
[15:14]	SYNCOSRC	Synchronization source These bits define the source and event that will be sent on the synchronous outputs SYNCOUT2 and SYNCOUT1. 00 : Master timer start 01: Master timer compare 1 event 10: Timer A start/reset 11: Timer A compare 1 event
[13]	SYNCSTRT	Synchronization Starts Master

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		This bit enables the master timer start when receiving a synchronization input event: 0: No effect on the master timer 1: A synchronization input event starts the master timer
[12]	SYNCRST	Synchronization Resets Master This bit enables the master timer reset when receiving a synchronization input event: 0: No effect on the master timer 1: A synchronization input event resets the master timer
[11]	Reserved	Reserved, the reset value must be maintained
[10:8]	SYNCIN	Synchronization input These bits are defining the synchronization input source. 000：SHRTIM runs in standalone mode because synchronization input have been disabled. 001: The shrtim_in_sync[0] input is driven by the TRGO of an on-chip timer 010: The shrtim_in_sync[1] input is driven by the TRGO of an on-chip timer 011: The shrtim_in_sync[2] input is driven by the TRGO of an on-chip timer 100: The shrtim_in_sync[3] input is driven by an external source via SHRTIM_SCIN(IOM) 101: Reserved 110: Reserved 111: Reserved For the cascading of shrtim_in_sync, please refer to section Synchronous Inputs. *Note: This parameter cannot be changed once the impacted timers are enabled.*
[7:6]	ILV	Master interleaved mode 00: Interleaved mode disabled 01: Triple interleaved mode: this mode uses SHRTIM_MCMP1DAT and SHRTIM_MCMP2DAT, as well as SHRTIM_MPRD . When SHRTIM_MPRD register is written, the SHRTIM_MCMP1DAT active register is automatically updated with SHRTIM_MPRD/3 value，and the SHRTIM_MCMP2DAT active register is automatically updated with SHRTIM_MPRD*2/3 value. 10: Quad interleaved mode: this mode uses SHRTIM_MCMP1DAT, SHRTIM_MCMP2DAT and SHRTIM_MCMP3DAT, as well as SHRTIM_MPRD. When SHRTIM_MPRD register is written, the SHRTIM_MCMP1DAT active register is automatically updated with MPRD/4 value，the SHRTIM_MCMP2DAT active register is automatically updated with SHRTIM_MPRD/2 value, and the SHRTIM_MCMP3DAT active register is automatically updated with SHRTIM_MPRD*3/4 value. 11: Interleaved mode disabled *Note: ILV[1:0] enables the interleaved mode and this bitfield is significant only when the HLF bit is reset.*
[5]	HLF	Half mode This bit enables half-mode, the SHRTIM_MCMP1DAT active register is

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		automatically updated with SHRTIM_MPRD/2 value when SHRTIM_MPRD register is written. 0: Half mode disabled 1: Half mode enabled
[4]	RTG	Re-triggerable mode This bit defines the behavior of the master timer counter in single-shot mode. 0: The timer is not re-triggerable: a counter reset can be done only if the counter is stopped (period elapsed) 1: The timer is re-triggerable: a counter reset is done whatever the counter state (running or stopped)
[3]	CONT	Continuous mode 0: The timer operates in single-shot mode and stops when it reaches the SHRTIM_MPRD value 1: The timer operates in continuous (free-running) mode and rolls over to zero when it reaches the SHRTIM_MPRD value
[2:0]	CKPSC	Master clock prescaler These 3 bits define the 8 possible clock prescaling ratio for the master timer. The counter clock equivalent frequency ($f_{COUNTER}$) is equal to $f_{HRCK} / 2^{CKPSC[2:0]}$. *Note: The prescaling ratio cannot be modified once the timer is enabled.*

17.3.2 SHRTIM Master Timer Interrupt Status Register（SHRTIM_MINTSTS）

Address offset: 0x04

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									MUPDITF	SYNCINITF	MREPTITF	MCMP4ITF	MCMP3ITF	MCMP2ITF	MCMP1ITF
									r	r	r	r	r	r	r

Bit Field	Name	Description
[31:7]	Reserved	Reserved, the reset value must be maintained
[6]	MUPDITF	Master Update Interrupt Flag This interrupt line is asserted each time master timer registers are updated. 0: No update register request received. 1: Update register was received. This bit is set by hardware only. This bit is only set by hardware and can be cleared by software by writing 0 to the register.

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[5]	SYNCINITF	Sync Input Interrupt Flag This interrupt line is asserted each time a synchronization input is received by the SHRTIM if interrupt is enabled. 0: No synchronization input was received. 1: Synchronization input was received. This bit is set by hardware only. This bit is only set by hardware and can be cleared by software by writing 0 to the register
[4]	MREPTITF	Master Repetition Interrupt Flag This interrupt line is asserted when enabled and when the zero value for Repetition counter is reached everytime. 0: Repetition counter has not reached the zero value. 1: Repetition counter has reached the zero value causing an interrupt. This bit is only set by hardware and can be cleared by software by writing 0 to the register
[3]	MCMP4ITF	Master Compare 4 Interrupt Flag This interrupt line is asserted when enabled and when the master timer count matches compare 4 register value. 0: No match between master timer counter and compare 4 event. 1: Master timer counter matched with compare 4 event. This bit is only set by hardware and can be cleared by software by writing 0 to the register
[2]	MCMP3ITF	Master Compare 3 Interrupt Flag This interrupt line is asserted when enabled and when the master timer count matches compare 3 register value. 0: No match between master timer counter and compare 3 event. 1: Master timer counter matched with compare 3 event. This bit is only set by hardware and can be cleared by software by writing 0 to the register
[1]	MCMP2ITF	Master Compare 2 Interrupt Flag This interrupt line is asserted when enabled and when the master timer count matches compare 2 register value. 0: No match between master timer counter and compare 2 event. 1: Master timer counter matched with compare 2 event. This bit is only set by hardware and can be cleared by software by writing 0 to the register
[0]	MCMP1ITF	Master Compare 1 Interrupt Flag This interrupt line is asserted when enabled and when the master timer count matches compare 1 register value. 0: No match between master timer counter and compare 1 event. 1: Master timer counter matched with compare 1 event. This bit is only set by hardware and can be cleared by software by writing 0 to the register

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17.3.3 SHRTIM Master Timer Interrupt Clear Register（SHRTIM_MINTCLR）

Address offset: 0x08

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									MUPDIC	SYNCINIC	MREPTIC	MCMP4IC	MCMP3IC	MCMP2IC	MCMP1IC
									w	w	w	w	w	w	w

Bit Field	Name	Description
[31:7]	Reserved	Reserved, the reset value must be maintained
[6]	MUPDIC	Master update interrupt flag clear 0: SHRTIM_MINTSTS.MUPDITF holds it's value 1: SHRTIM_MINTSTS.MUPDITF value is cleared
[5]	SYNCINIC	Master sync interrupt flag clear 0: SHRTIM_MINTSTS.SYNCINITF holds it's value 1: SHRTIM_MINTSTS.SYNCINITF value is cleared
[4]	MREPTIC	Master repetition interrupt flag clear 0: SHRTIM_MINTSTS.MREPTITF holds it's value 1: SHRTIM_MINTSTS.MREPTITF value is cleared
[3]	MCMP4IC	Master compare4 interrupt flag clear 0: SHRTIM_MINTSTS.MCMP4ITF holds it's value 1: SHRTIM_MINTSTS.MCMP4ITF value is cleared
[2]	MCMP3IC	Master compare3 interrupt flag clear 0: SHRTIM_MINTSTS.MCMP3ITF holds it's value 1: SHRTIM_MINTSTS.MCMP3ITF value is cleared
[1]	MCMP2IC	Master compare2 interrupt flag clear 0: SHRTIM_MINTSTS.MCMP2ITF holds it's value 1: SHRTIM_MINTSTS.MCMP2ITF value is cleared
[0]	MCMP1IC	Master compare1 interrupt flag clear 0: SHRTIM_MINTSTS.MCMP1ITF holds it's value 1: SHRTIM_MINTSTS.MCMP1ITF value is cleared

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17.3.4 SHRTIM Master Timer Interrupt/DMA Enable Register （SHRTIM_MIDEN）

Address offset: 0x0C

Reset value: 0x 00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									MUPDDEN	SYNCINDEN	MREPTDEN	MCMP4DEN	MCMP3DEN	MCMP2DEN	MCMP1DEN
									rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									MUPDIEN	SYNCINIEN	MREPTIEN	MCMP4IEN	MCMP3IEN	MCMP2IEN	MCMP1IEN
									rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31:23]	Reserved	Reserved, the reset value must be maintained
[22]	MUPDDEN	Master registers update DMA request enable Software bit to enable DMA request on Master registers update. 0: Disables the Update register generated DMA request . 1: Enables the Update register generated DMA request.
[21]	SYNCINDEN	Synchronization input DMA request enable Software bit to enable Synchronization input DMA request enable 0: Disables the Synchronization input generated DMA request 1: Enables the Synchronization input generated DMA request
[20]	MREPTDEN	Master timer DMA request enable Software bit to enable Master Timer Repetition Counter DMA request enable 0: Disables the Master Timer Repetition Counter generated DMA request 1: Enables the Master Timer Repetition Counter generated DMA request
[19]	MCMP4DEN	Master timer compare 4 DMA request enable Software bit to enable Master Timer compare 4 DMA request enable 0: Disables the Master Timer compare 4 generated DMA request 1: Enables the Master Timer compare 4 generated DMA request .
[18]	MCMP3DEN	Master timer compare 3 DMA request enable Software bit to enable Master Timer compare 3 DMA request enable 0: Disables the Master Timer compare 3 generated DMA request 1: Enables the Master Timer compare 3 generated DMA request
[17]	MCMP2DEN	Master timer compare 2 DMA request enable Software bit to enable Master Timer compare 2 DMA request enable 0: Disables the Master Timer compare 2 generated DMA request

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		1: Enables the Master Timer compare 2 generated DMA request .
[16]	MCMP1DEN	Master timer compare 1 DMA request enable Software bit to enable Master Timer compare 1 DMA request enable 0: Disables the Master Timer compare 1 generated DMA request 1: Enables the Master Timer compare 1 generated DMA request .
[15:7]	Reserved	Reserved, the reset value must be maintained
[6]	MUPDIEN	Master registers update interrupt request enable Software bit to enable Interrupt request on Master registers update 0: Disables the Update register generated interrupt request. 1: Enables the Update register generated interrupt request.
[5]	SYNCINIEN	Synchronization input interrupt request enable Software bit to enable Synchronization input DMA request enable 0: Disables the Synchronization input generated interrupt request 1: Enables the Synchronization input generated interrupt request
[4]	MREPTIEN	Master repetition counter interrupt request enable Software bit to enable Master Timer Repetition Counter DMA request enable 0: Disables the Master Timer Repetition Counter generated interrupt request 1: Enables the Master Timer Repetition Counter generated interrupt request
[3]	MCMP4IEN	Master timer compare 4 interrupt request enable Software bit to enable Master Timer compare 4 DMA request enable 0: Disables the Master Timer compare 4 generated interrupt request 1: Enables the Master Timer compare 4 generated interrupt request .
[2]	MCMP3IEN	Master timer compare 3 interrupt request enable Software bit to enable Master Timer compare 3 DMA request enable 0: Disables the Master Timer compare 3 generated interrupt request 1: Enables the Master Timer compare 3 generated interrupt request.
[1]	MCMP2IEN	Master timer compare 2 interrupt request enable Software bit to enable Master Timer compare 2 DMA request enable 0: Disables the Master Timer compare 2 generated interrupt request 1: Enables the Master Timer compare 2 generated interrupt request.
[0]	MCMP1IEN	Master timer compare 1 interrupt request enable Software bit to enable Master Timer compare 1 interrupt request enable 0: Disables the Master Timer compare 1 generated interrupt request 1: Enables the Master Timer compare 1 generated interrupt request

17.3.5 SHRTIM Master Timer Counter Register（SHRTIM_MCNT）

Address offset: 0x10

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCOUNT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	MCOUNT	Master timer counter Holds the master timer counter value. This register can be written only when the Master Timer is disabled (SHRTIM_MCTRL.MCNTEN = 0). *Note: For SHRTIM_MCTRL.CKPSC[2:0] < 5 the least significant bits of the counter are not significant. They cannot be written and return 0 when read.* *Note: The counter value loaded into this register should never exceed the value written into SHRTIM_MPRD register value*

17.3.6 SHRTIM Master Timer Period Register（SHRTIM_MPRD）

Address offset: 0x14

Reset value: 0x0000FFDF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPRD															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	MPRD	Master timer period This register defines the counter overflow value. The period value must be above or equal to 3 periods of the f_{SHRTIM} clock, that is 0x60 if CKPSC[2:0] = 0, 0x30 if CKPSC[2:0] = 1, 0x18 if CKPSC[2:0] = 2,...

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		When SHRTIM_MCTRL.PLEN is set to 1, the register will configure the value to the period preload register. If SHRTIM_MCTRL.PLEN is reset, the register value will be directly loaded to the active period register.

17.3.7 SHRTIM Master Timer Repetition Register（SHRTIM_MREPT）

Address offset: 0x18

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MREPT							
								rw							

Bit Field	Name	Description
[31:8]	Reserved	Reserved, the reset value must be maintained
[7:0]	MREPT	Master timer repetition period This register holds the master timer repetition period value. This register configures the value into a repetition preload register when SHRTIM_MCTRL.PLEN bit is set. If SHRTIM_MCTRL.PLEN is reset then this register value is directly loaded to the active repetition register.

17.3.8 SHRTIM Master Timer Compare 1 Register（SHRTIM_MCMP1DAT）

Address offset: 0x1C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCMP1DAT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained

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[15:0]	MCMP1DAT	Master timer compare 1 data The compare 1 value must be greater than or equal to 3 cycles of the f_{SHRTIM} clock, i.e., if CKPSC[2:0] = 0, it is 0x60; if CKPSC[2:0] = 1, it is 0x30; if CKPSC[2:0] = 2, it is 0x18;... This register configures the value into a compare 1 preload register when SHRTIM_MCTRL.PLEN bit is set. If SHRTIM_MCTRL.PLEN is reset then this register value is directly loaded to the active compare 1 register.

17.3.9 SHRTIM Master Timer Compare 2 Register（SHRTIM_MCMP2DAT）

Address offset: 0x24

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCMP2DAT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	MCMP2DAT	Master timer compare 2 data The compare 2 value must be greater than or equal to 3 cycles of the f_{SHRTIM} clock, i.e., if CKPSC[2:0] = 0, it is 0x60; if CKPSC[2:0] = 1, it is 0x30; if CKPSC[2:0] = 2, it is 0x18;... This register configures the value into a compare 2 preload register when SHRTIM_MCTRL.PLEN bit is set. If SHRTIM_MCTRL.PLEN is reset then this register value is directly loaded to the active compare 2 register.

17.3.10 SHRTIM Master Timer Compare 3 Register（SHRTIM_MCMP3DAT）

Address offset: 0x28

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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MCMP3DAT

rw

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	MCMP3DAT	Master timer compare 3 data The compare 3 value must be greater than or equal to 3 cycles of the f_{SHRTIM} clock, i.e., if CKPSC[2:0] = 0, it is 0x60; if CKPSC[2:0] = 1, it is 0x30; if CKPSC[2:0] = 2, it is 0x18;... This register configures the value into a compare 3 preload register when SHRTIM_MCTRL.PLEN bit is set. If SHRTIM_MCTRL.PLEN is reset then this register value is directly loaded to the active compare 3 register.

17.3.11 SHRTIM Master Timer Compare 4 Register（SHRTIM_MCMP4DAT）

Address offset: 0x2C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCMP4DAT															

rw

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	MCMP4DAT	Master timer compare 4 data The compare 4 value must be greater than or equal to 3 cycles of the f_{SHRTIM} clock, i.e., if CKPSC[2:0] = 0, it is 0x60; if CKPSC[2:0] = 1, it is 0x30; if CKPSC[2:0] = 2, it is 0x18;... This register configures the value into a compare 4 preload register when SHRTIM_MCTRL.PLEN bit is set. If SHRTIM_MCTRL.PLEN is reset then this register value is directly loaded to the active compare 4 register.

17.3.12 SHRTIM Synchronous Output Register（SHRTIM_SYNCOUT）

Address offset: 0x30

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SYNCOUT2PUS		Reserved		SYNCOUT1PUS	
										rw				rw	

Bit Field	Name	Description
[31:8]	Reserved	Reserved, the reset value must be maintained
[7:6]	Reserved	Reserved, the reset value must be maintained
[5:4]	SYNCOUT2PUS	Synchronization output shrtim_out_sync2 to internal peripherals These bits define the routing and conditioning of the synchronization output event. 00: Disabled the synchronization output 01: Reserved. 10: Generate a positive pulse of 16 SHRTIM clock cycles on shrtim_out_sync2 11: Generate a negative pulse of 16 SHRTIM clock cycles on shrtim_out_sync2 *Note: This bitfield must not be modified once the counter is enabled (SHRTIM_MCTRL.TxCNTEN bit set)*
[3:2]	Reserved	Reserved, the reset value must be maintained
[1:0]	SYNCOUT1PUS	Synchronization output shrtim_out_sync1 to SHRTIMx_SCOUT pin These bits define the routing and conditioning of the synchronization output event. 00: Disabled the synchronization output 01: Reserved. 10: Generate a positive pulse of 16 SHRTIM clock cycles on SHRTIMx_SCOUT 11: Generate a negative pulse of 16 SHRTIM clock cycles on SHRTIMx_SCOUT *Note: This bitfield must not be modified once the counter is enabled (SHRTIM_MCTRL.TxCNTEN bit set)*

17.3.13 SHRTIM Debug Freeze Disable Register（SHRTIM_FRZDIS）

Address offset: 0x34

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ALLTIM	TFDBG	TEDBG	TDDBG	TCDBG	TBDBG	TADBG	MDBG
								rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31:8]	Reserved	Reserved, the reset value must be maintained

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[7]	ALLTIMEN	DBG_CTRL.SHRTIM1_STOP controls all timers (master timer + timing units) 0: When DBG_CTRL.SHRTIM1_STOP is set to 1, all timers stop operating when the microcontroller enters debug mode (Cortex®-M4F core halts). 1: When DBG_CTRL.SHRTIM1_STOP is set to 1, all timers are not affected when the microcontroller enters debug mode (Cortex®-M4F core halts).
[6]	TFDBGEN	Refer to the description of TADBGEN.
[5]	TEDBGEN	Refer to the description of TADBGEN.
[4]	TDDBGEN	Refer to the description of TADBGEN.
[3]	TCDBGEN	Refer to the description of TADBGEN.
[2]	TBDBGEN	Refer to the description of TADBGEN.
[1]	TADBGEN	Skip the control of Timer A by DBG_CTRL.SHRTIM1_STOP. 0: When DBG_CTRL.SHRTIM1_STOP is set to 1, Timer A stops operating when the microcontroller enters debug mode (Cortex®-M4F core halts). 1: When DBG_CTRL.SHRTIM1_STOP is set to 1, Timer A is not affected when the microcontroller enters debug mode (Cortex®-M4F core halts).
[0]	MDBGEN	Skip the control of Master Timer by DBG_CTRL.SHRTIM1_STOP. 0: When DBG_CTRL.SHRTIM1_STOP is set to 1, the master timer stops operating when the microcontroller enters debug mode (Cortex®-M4F core halts). 1: When DBG_CTRL.SHRTIM1_STOP is set to 1, the master timer is not affected when the microcontroller enters debug mode (Cortex®-M4F core halts).

17.3.14 SHRTIM Timer x Control Register（SHRTIM_TxCTRL）

Address offset: 0x80

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPDGAT				PLEN	DACTRIG		MUE	TEUE	TDUE	TCUE	TBUE	Reserv	RSTROU	REPTUE	TFUE
rw				rw	rw		rw	rw	rw	rw	rw		rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELCMP4M		DELCMP2M		SYNCST	SYNCR	RSYNCU	ILV		PP	HLF	RTG	CONT	CKPSC		
rw		rw		rw	rw	rw	rw		rw	rw	rw	rw	rw		

Bit Field	Name	Description
[31:28]	UPDGAT	Update Gating Updating the registers could share a relation with the DMA burst along with the input pins shrtim_upd_en[3:1]. The configuration register bits below show what this dependency is. 0000: The update occurs independently from the DMA burst transfer 0001: The update occurs when the DMA burst transfer is completed 0010: The update occurs on the update event following the DMA burst transfer completion

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		0011: The update occurs on a rising edge on shrtim_upd_en1 0100: The update occurs on a rising edge on shrtim_upd_en2 0101: The update occurs on a rising edge on shrtim_upd_en3 0110: The update occurs on the update event following a rising edge on shrtim_upd_en1 0111: The update occurs on the update event following a rising edge on shrtim_upd_en2 1000: The update occurs on the update event following a rising edge on shrtim_upd_en3 Others: Reserved
[27]	PLEN	Timer x preload enable This bit enables the registers preload mechanism and defines whether a write access into a preloadable register is done into the active or the preload register. 0: Preload register access disabled: the write access is directly done into the active register 1: Preload register access enabled: the write access is done into the preload register
[26:25]	DACTRIG	DAC Synchronization trig A DAC synchronization event is generated when the timer update occurs. These bits are defining on which output the DAC synchronization is sent (refer to Section : DAC triggers for connections details). 00 : No DAC trigger is selected 01 : Trigger generated on shrtim_dac_trig1 10 : Trigger generated on shrtim_dac_trig2 11 : Trigger generated on shrtim_dac_trig3
[24]	MUEN	Master timer update Register Update is triggered by Master timer update 0 : Master timer as register update trigger is disabled 1 : Master timer as register update trigger is enabled
[23]	TEUEN	It is available for SHRTIM_TACTRL、SHRTIM_TBCTRL、SHRTIM_TCCTRL、SHRTIM_TDCTRL、SHRTIM_TFCTRL: TIM E update Register Update is triggered by timer E update 0 : timer E as register update trigger is disabled 1 : timer E as register update trigger is enabled
[22]	TDUEN	It is available for SHRTIM_TACTRL、SHRTIM_TBCTRL、SHRTIM_TCCTRL、SHRTIM_TECTRL、SHRTIM_TFCTRL: TIM D update Register Update is triggered by timer D update 0 : timer D as register update trigger is disabled 1 : timer D as register update trigger is enabled
[21]	TCUEN	It is available for SHRTIM_TACTRL、SHRTIM_TBCTRL、SHRTIM_TDCTRL、SHRTIM_TECTRL、SHRTIM_TFCTRL: TIM C update Register Update is triggered by timer C update 0 : timer C as register update trigger is disabled

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		1 : timer C as register update trigger is enabled
[20]	TBUEN	It is available for SHRTIM_TACTRL 、 SHRTIM_TCCTRL 、 SHRTIM_TDCTRL、SHRTIM_TECTRL、SHRTIM_TFCTR: TIM B update Register Update is triggered by timer B update 0 : timer B as register update trigger is disabled 1 : timer B as register update trigger is enabled
[19]	TAUEN	It is available for SHRTIM_TBCTRL 、 SHRTIM_TCCTRL 、 SHRTIM_TDCTRL、SHRTIM_TECTRL、SHRTIM_TFCTRL: TIM A update Register Update is triggered by timer A update 0 : timer A as register update trigger is disabled 1 : timer A as register update trigger is enabled
[18]	RSTROUEN	Timerx reset update Register update is triggered by timer x counter reset or roll-over to 0 after reaching the period value in continuous mode. 0: Update by timer x reset / roll-over disabled 1: Update by timer x reset / roll-over enabled
[17]	REPTUEN	Timer x Repetition update Register update is triggered when the counter rolls over and SHRTIM_TxREPT = 0 0: Update on repetition disabled 1: Update on repetition enabled
[16]	TFUEN	It is available for SHRTIM_TACTRL 、 SHRTIM_TBCTRL 、 SHRTIM_TCCTRL、SHRTIM_TDCTRL、SHRTIM_TECTRL 中: TIM F update Register Update is triggered by timer F update 0 : timer F as register update trigger is disabled 1 : timer F as register update trigger is enabled
[15:14]	DELCMP4M	CMP4 auto-delayed mode Following bits determine if the SHRTIM_TxCMP4DAT behaves in standard mode or in various Auto-Delayed mode 00: SHRTIM_TxCMP4DAT is in regular compare mode 01: SHRTIM_TxCMP4DAT is in Auto Delayed mode with internal SHRTIM_TxCMP4DAT = SHRTIM_TxCPT.CPT2 register + original SHRTIM_TxCMP4DAT value. If capture 2 event failed to occur before SHRTIM_TxPRD, then the comparison is canceled until reset/rollover to next period and no CMP4 event occurs. 10: SHRTIM_TxCMP4DAT is in Auto Delayed mode with internal SHRTIM_TxCMP4DAT = SHRTIM_TxCPT.CPT2 register + original SHRTIM_TxCMP4DAT value. If capture 2 event is yet to happen meanwhile a timeout feature is implemented by waiting till the count reaches (SHRTIM_TxCMP4DAT + SHRTIM_TxCMP1DAT). The CMP4 event is issued when the match happens. 11: SHRTIM_TxCMP4DAT is in Auto Delayed mode with internal

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		SHRTIM_TxCMP4DAT = SHRTIM_TxCPT.CPT2 register + original SHRTIM_TxCMP4DAT value. If capture 2 event is yet to happen meanwhile a timeout feature is implemented by waiting till the count reaches (SHRTIM_TxCMP4DAT + SHRTIM_TxCMP3DAT). The CMP4 event is issued when the match happens.
[13:12]	DELCMP2M	CMP2 auto-delayed mode Following bits determine if the SHRTIM_TxCMP2DAT behaves in standard mode or in various Auto-Delayed mode 00: SHRTIM_TxCMP2DAT is in regular compare mode 01: SHRTIM_TxCMP2DAT is in Auto Delayed mode with internal SHRTIM_TxCMP2DAT = SHRTIM_TxCPT.CPT1 register + original SHRTIM_TxCMP2DAT value. If capture 1 event failed to occur before SHRTIM_TxPRD, then the comparison is canceled until reset/rollover to next period and no CMP2 event occurs. 10: SHRTIM_TxCMP2DAT is in Auto Delayed mode with internal SHRTIM_TxCMP2DAT = SHRTIM_TxCPT.CPT1 register + original SHRTIM_TxCMP2DAT value. If capture 1 event is yet to happen meanwhile a timeout feature is implemented by waiting till the count reaches (SHRTIM_TxCMP2DAT + SHRTIM_TxCMP1DAT). The CMP2 event is issued when the match happens. 11: SHRTIM_TxCMP2DAT is in Auto Delayed mode with internal SHRTIM_TxCMP2DAT = SHRTIM_TxCPT.CPT1 register + original SHRTIM_TxCMP2DAT value. If capture 1 event is yet to happen meanwhile a timeout feature is implemented by waiting till the count reaches (SHRTIM_TxCMP2DAT + SHRTIM_TxCMP3DAT). The CMP2 event is issued when the match happens.
[11]	SYNCSTRT	Synchronization Starts Timer x This bit defines the timer x behavior following the synchronization event: 0: No effect on timer x 1: A synchronization input event starts the timer x
[10]	SYNCRST	Synchronization Resets Timer x This bit defines the timer x behavior following the synchronization event: 0: No effect on timer x 1: A synchronization input event resets the timer x
[9]	RSYNCUPD	Update on resynchronization This bit specifies whether update source coming outside from the timing unit must be synchronized: 0: The update coming from adjacent timers (when MUEN, TAUEN, TBUEN, TCUEN, TDUEN, TEUEN, TFUEN bit is set) or from a software update (TxSWUPD bit) is taken into account immediately 1: The update coming from adjacent timers (when MUEN, TAUEN, TBUEN, TCUEN, TDUEN, TEUEN, TFUEN bit is set) or from a software update (TxSWUPD bit) is taken into account on the following reset/roll-over event.

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		Note: This bit is significant only when UPDGAT[3:0] = 4'b0000, it is ignored otherwise.
[8:7]	ILV	Interleaved mode This bitfield is significant only when the HLF bit is reset. It enables the interleaved mode. 00: Interleaved mode disabled 01: Triple interleaved mode: when SHRTIM_TxPRD register is written, the SHRTIM_TxCMP1DAT active register is automatically updated with SHRTIM_TxPRD/3 value, and the SHRTIM_TxCMP2DAT active register is automatically updated with 2x (SHRTIM_TxPRD/3) value. 10: Quad interleaved mode: when SHRTIM_TxPRD register is written, the SHRTIM_TxCMP1DAT active register is automatically updated with SHRTIM_TxPRD/4 value, the SHRTIM_TxCMP2DAT active register is automatically updated with SHRTIM_TxPRD/2 value and the SHRTIM_TxCMP3DAT active register is automatically updated with 3x (SHRTIM_TxPRD/4) value. 11: Interleaved mode disabled
[6]	PP	Push-Pull mode enable This bit enables the push-pull mode. 0: Push-pull mode disabled 1: Push-pull mode enabled Note: This bitfield must not be modified once the counter is enabled (*TxCNTEN* bit set).
[5]	HLF	Half mode enable This bit enables the half duty-cycle mode: the SHRTIM_TxCMP1DAT active register is automatically updated with SHRTIM_TxPRD/2 value when SHRTIM_TxPRD register is written. 0: Half mode disabled 1: Half mode enabled
[4]	RTG	Re-triggerable mode This bit defines the counter behavior in single shot mode. 0: The timer is not re-triggerable: a counter reset is done if the counter is stopped (period elapsed in single-shot mode or counter stopped in continuous mode) 1: The timer is re-triggerable: a counter reset is done whatever the counter state
[3]	CONT	Continuous mode 0: This setting configures timer x in single shot mode and stops counting on reaching SHRTIM_TxPRD. 1: Timer x works continuosly in Free run mode and rolls over to zero each time SHRTIM_TxPRD is reached.
[2:0]	CKPSC	Timer x clock prescaler These 3 bits define the 8 possible prescale clock factors for Timer x. The effective counting clock frequency ($f_{COUNTER}$) is equal to $F_{HRCK}/2^{PSC[2:0]}$.

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		The prescaling frequency must be made final before enabling the timer.

17.3.15 SHRTIM Timer x Interrupt Status Register（SHRTIM_TxINTSTS）

Address offset: 0x84

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										O2BCKUP	O1BCKUP	O2DIPSTS	O1DIPSTS	IPPSTS	CPPSTS
										r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DPITF	RSTROITF	RST2ITF	SET2ITF	RST1ITF	SET1ITF	CPT2ITF	CPT1ITF	UPDITF	REPTITF	CMP5ITF	CMP4ITF	CMP3ITF	CMP2ITF	CMP1ITF
	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
[31:22]	Reserved	Reserved, the reset value must be maintained
[21]	O2BCKUP	Timer x channel 2 output backup This status bit is a raw copy of the output 2 state, before the output stage (chopper, polarity). It allows to check the current output state before re-enabling the output after a delayed protection. 0: Output 2 is inactive 1: Output 2 is active
[20]	O1BCKUP	Timer x channel 1 output backup This status bit is a raw copy of the output 1 state, before the output stage (chopper, polarity). It allows to check the current output state before re-enabling the output after a delayed protection. 0: Output 1 is inactive 1: Output 1 is active
[19]	O2DIPSTS	Timer x channnel 2 delayed idle protection status This status bit indicates the output 2 state when the delayed idle protection was triggered. This bit is updated upon any new delayed protection entry. This bit is not updated in balanced idle. 0: Output 2 was inactive 1: Output 2 was active
[18]	O1DIPSTS	Timer x channnel 1 delayed idle protection status This status bit indicates the output 1 state when the delayed idle protection was triggered. This bit is updated upon any new delayed protection entry. This bit is not updated in balanced idle. 0: Output 1 was inactive 1: Output 1 was active
[17]	IPPSTS	Idle Push Pull Status

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		This status bit indicates on which output the signal was applied, in push-pull mode, balanced fault mode or delayed idle mode, when the protection was triggered (whatever the output state, active or inactive). 0: Protection occurred when the output 1 was active and output 2 forced inactive 1: Protection occurred when the output 2 was active and output 1 forced inactive
[16]	CPPSTS	Current Push Pull Status This status bit indicates on which output the signal is currently applied, in push-pull mode. It is only significant in this configuration. 0: Signal applied on output 1 and output 2 forced inactive 1: Signal applied on output 2 and output 1 forced inactive
[15]	Reserved	Reserved, the reset value must be maintained
[14]	DPITF	Delayed protection interrupt flag 0: No delayed protection interrupt occured 1: Delayed idle or balanced Idle mode entry occurred causing interrupt
[13]	RSTROITF	Reset and/or roll-over Interrupt Flag This bit is set by hardware when the timer x counter is reset or rolls over in continuous mode. 0: No TIMx counter reset/roll-over interrupt occurred 1: TIMX counter reset/roll-over interrupt occurred
[12]	RST2ITF	Output 2 reset interrupt flag Refer to the RST1ITF description.
[11]	SET2ITF	Output 2 set interrupt flag Refer to the SET1ITF description.
[10]	RST1ITF	Output 1 reset interrupt flag This bit is set by hardware when the Tx1 output is reset (goes from active to inactive mode). 0: No Tx1 output reset interrupt occurred 1: Tx1 output reset interrupt occurred
[9]	SET1ITF	Output 1 set interrupt flag This bit is set by hardware when the Tx1 output is set (goes from inactive to active mode). 0: No Tx1 output set interrupt occurred 1: Tx1 output set interrupt occurred
[8]	CPT2ITF	Capture 2 interrupt flag Refer to the CPT1ITF description.
[7]	CPT1ITF	Capture 1 interrupt flag This bit is set by hardware when the timer x capture 1 event occurs. 0: No timer x capture 1 interrupt occurred 1: Timer x capture 1 interrupt occurred
[6]	UPDITF	Update interrupt flag This bit is set by hardware when the timer x update event occurs.

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		0: No timer x update interrupt occurred 1: Timer x update interrupt occurred
[5]	REPTITF	Repetition interrupt flag This bit is set by hardware when the timer x repetition period has elapsed. 0: No timer x repetition interrupt occurred 1: Timer x repetition interrupt occurred
[4]	CMP5ITF	Compare 5 flag Refer to the CMP1ITF description.
[3]	CMP4ITF	Compare 4 flag Refer to the CMP1ITF description.
[2]	CMP3ITF	Compare 3 flag Refer to the CMP1ITF description.
[1]	CMP2ITF	Compare 2 flag Refer to the CMP1ITF description.
[0]	CMP1ITF	Compare 1 flag This bit is set by hardware when the timer x counter matches the value programmed in the compare 1 register. 0: No compare 1 interrupt occurred 1: Compare 1 interrupt occurred

17.3.16 SHRTIM Timer x Interrupt Clear Register（SHRTIM_TxINTCLR）

Address offset: 0x88

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DPIC	RSTROIC	RST2IC	SET2IC	RST1IC	SET1IC	CPT2IC	CPT1IC	UPDIC	REPTIC	CMP5IC	CMP4IC	CMP3IC	CMP2IC	CMP1IC
	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
[31:15]	Reserved	Reserved, the reset value must be maintained
[14]	DPIC	Delayed protection interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.DPIF
[13]	RSTROIC	Reset and/or roll-over interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.RSTROITF
[12]	RST2IC	Output channel 2 reset interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.RST2ITF
[11]	SET2IC	Output channel 2 set interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.SET2ITF

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[10]	RST1IC	Output channel 1 reset interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.RST1ITF
[9]	SET1IC	Output channel 1 set interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.SET1ITF
[8]	CPT2IC	Capture 2 interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CPT2ITF
[7]	CPT1IC	Capture 1 interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CPT1ITF
[6]	UPDIC	Update interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.UPDITF
[5]	REPTIC	Repetition interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.REPTITF
[4]	CMP5IC	Compare 5 flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CMP5ITF
[3]	CMP4IC	Compare 4 interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CMP4ITF
[2]	CMP3IC	Compare 3 interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CMP3ITF
[1]	CMP2IC	Compare 2 interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CMP2ITF
[0]	CMP1IC	Compare 1 interrupt flag clear Writing 1 to this bit clears the SHRTIM_TxINTSTS.CMP1ITF

17.3.17 SHRTIM Timer x Interrupt/DMA Enable Register（SHRTIM_TxIDEN）

Address offset: 0x8C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	DPDEN	RSTRODEN	RST2DEN	SET2DEN	RST1DEN	SET1DEN	CPT2DEN	CPT1DEN	UPDDEN	Reserved	REPTDEN	CMP4DEN	CMP3DEN	CMP2DEN	CMP1DEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DPIEN	RSTROIEN	RST2IEN	SET2IEN	RST1IEN	SET1IEN	CPT2IEN	CPT1IEN	UPDIEN	REPTIEN	Reserved	CMP4IEN	CMP3IEN	CMP2IEN	CMP1IEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw

Bit Field	Name	Description
[31]	Reserved	Reserved, the reset value must be maintained
[30]	DPDEN	Delayed protection DMA request enable This bit is set and cleared by software to enable/disable DMA requests on delayed protection. 0: Delayed protection DMA request disabled

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		1: Delayed protection DMA request enabled
[29]	RSTRODEN	Reset/roll-over DMA request enable This bit is set and cleared by software to enable/disable DMA requests on timer x counter reset or roll-over in continuous mode. 0: Timer x counter reset/roll-over DMA request disabled 1: Timer x counter reset/roll-over DMA request enabled
[28]	RST2DEN	Output 2 reset DMA request enable Refer to the RST1DEN description.
[27]	SET2DEN	Output 2 set DMA request enable Refer to the SET1DEN description.
[26]	RST1DEN	Output 1 reset DMA request enable This bit is set and cleared by software to enable/disable Tx1 output reset DMA requests. 0: Tx1 output reset DMA request disabled 1: Tx1 output reset DMA request enabled
[25]	SET1DEN	Output 1 reset DMA request enable This bit is set and cleared by software to enable/disable Tx1 output set DMA requests. 0: Tx1 output set DMA request disabled 1: Tx1 output set DMA request enabled
[24]	CPT2DEN	Capture 2 DMA request enable Refer to the CPT1DEN description.
[23]	CPT1DEN	Capture 1 DMA request enable This bit is set and cleared by software to enable/disable capture 1 DMA requests. 0: Capture 1 DMA request disabled 1: Capture 1 DMA request enabled
[22]	UPDDEN	Update DMA request enable This bit is set and cleared by software to enable/disable DMA requests on update event. 0: Update DMA request disabled 1: Update DMA request enabled
[21]	Reserved	Reserved, the reset value must be maintained
[20]	REPTDEN	Repetition DMA request enable This bit is set and cleared by software to enable/disable DMA requests on repetition event. 0: Repetition DMA request disabled 1: Repetition DMA request enabled
[19]	CMP4DEN	Compare 4 DMA request enable Refer to the CMP1DEN description.
[18]	CMP3DEN	Compare 3 DMA request enable Refer to the CMP1DEN description.

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[17]	CMP2DEN	Compare 2 DMA request enable Refer to the CMP1DEN description.
[16]	CMP1DEN	Compare 1 DMA request enable This bit is set and cleared by software to enable/disable the compare 1 DMA requests. 0: Compare 1 DMA request disabled 1: Compare 1 DMA request enabled
[15]	Reserved	Reserved, the reset value must be maintained
[14]	DPIEN	Delayed protection interrupt enable This bit is set and cleared by software to enable/disable interrupts on delayed protection. 0: Delayed protection interrupts disabled 1: Delayed protection interrupts enabled
[13]	RSTROIEN	Reset/roll-over interrupt enable This bit is set and cleared by software to enable/disable interrupts on timer x counter reset or rollover in continuous mode. 0: Timer x counter reset/roll-over interrupt disabled 1: Timer x counter reset/roll-over interrupt enabled
[12]	RST2IEN	Output 2 reset interrupt enable Refer to the RST1IEN description.
[11]	SET2IEN	Output 2 set interrupt enable Refer to the SET1IEN description.
[10]	RST1IEN	Output 1 reset interrupt enable This bit is set and cleared by software to enable/disable Tx1 output reset interrupts. 0: Tx1 output reset interrupts disabled 1: Tx1 output reset interrupts enabled
[9]	SET1IEN	Output 2 set interrupt enable This bit is set and cleared by software to enable/disable Tx1 output set interrupts. 0: Tx1 output set interrupts disabled 1: Tx1 output set interrupts enabled
[8]	CPT2IEN	Capture 2 interrupt enable Refer to the CPT1IEN description.
[7]	CPT1IEN	Capture 1 interrupt enable This bit is set and cleared by software to enable/disable capture 1 interrupts. 0: Capture 1 interrupts disabled 1: Capture 1 interrupts enabled
[6]	UPDIEN	Update interrupt enable This bit is set and cleared by software to enable/disable update event interrupts. 0: Update interrupts disabled 1: Update interrupts enabled

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[5]	REPTIEN	Repetition interrupt enable This bit is set and cleared by software to enable/disable repetition event interrupts. 0: Repetition interrupts disabled 1: Repetition interrupts enabled
[4]	Reserved	Reserved, the reset value must be maintained
[3]	CMP4IEN	Compare 4 interrupt enable Refer to the CMP1IEN description.
[2]	CMP3IEN	Compare 3 interrupt enable Refer to the CMP1IEN description.
[1]	CMP2IEN	Compare 2 interrupt enable Refer to the CMP1IEN description.
[0]	CMP1IEN	Compare 1 interrupt enable This bit is set and cleared by software to enable/disable the compare 1 interrupts. 0: Compare 1 interrupt disabled 1: Compare 1 interrupt enabled

17.3.18 SHRTIM Timer x Counter Register（SHRTIM_TxCNT）

Address offset: 0x90

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	COUNT	Timer x counter value Holds the timer x counter value. This register can be written only when the timer x is disabled (SHRTIM_MCTRL.TxCNTEN=0). *Note: For CKPSC[2:0] < 5 the least significant bits of the counter are not significant. They cannot be written and return 0 when read.* *Note: The count loaded into this register should never exceed the value written into PRD register value*

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17.3.19 SHRTIM Timer x Period Register（SHRTIM_TxPRD）

Address offset: 0x94

Reset value: 0x0000FFDF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRD															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	PRD	Timer x period value The period value must be above or equal to 3 periods of the f_{SHRTIM} clock, that is 0x60 if SHRTIM_TxCTRL.CKPSC[2:0] = 0, 0x30 if SHRTIM_TxCTRL.CKPSC[2:0] = 1, 0x18 if SHRTIM_TxCTRL.CKPSC[2:0] = 2,... When PLEN is set to 1, the register will configure the value to the period preload register. If PLEN is reset, the register value will be directly loaded to the active period register.

17.3.20 SHRTIM Timer x Repetition Register（SHRTIM_TxREPT）

Address offset: 0x98

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								REPT							
								rw							

Bit Field	Name	Description
[31:8]	Reserved	Reserved, the reset value must be maintained
[7:0]	REPT	Timer x repetition period value This register holds the timer x repetition period value. This register configures the value into a repetition preload register when PLEN bit is set. If PLEN is reset then this register value is directly loaded to the active repetition register.

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17.3.21 SHRTIM Timer x Compare 1 Register（SHRTIM_TxCMP1DAT）

Address offset: 0x9C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP1DAT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	CMP1DAT	Timer x compare 1 data The compare 1 value must be above or equal to 3 periods of the f_{SHRTIM} clock, that is 0x60 if SHRTIM_TxCTRL.CKPSC[2:0] = 0, 0x30 if SHRTIM_TxCTRL.CKPSC[2:0] = 1, 0x18 if SHRTIM_TxCTRL.CKPSC[2:0] = 2,... When PLEN is set to 1, the register will configure the value to the compare 1 preload register. If PLEN is reset, the register value will be directly loaded to the active compare 1 register.

17.3.22 SHRTIM Timer x Compare 1 Compound Register (SHRTIM_TxRCMP1DAT)

Address offset: 0xA0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								REPT							
								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP1DAT															
rw															

Bit Field	Name	Description
[31:24]	Reserved	Reserved, the reset value must be maintained
[23:16]	REPT	Timer x repetition value Aliased from SHRTIM_TxREPT register This bitfield is an alias from the REPT[7:0] bitfield in the SHRTIM_TxREPT

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		register.
[15:0]	CMP1DAT	Timer x compare 1 data This bitfield is an alias from the CMP1DAT[15:0] bitfield in the SHRTIM_TxCMP1DAT register.

17.3.23 SHRTIM Timer x Compare 2 Register（SHRTIM_TxCMP2DAT）

Address offset: 0xA4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP2DAT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	CMP2DAT	Timer x compare 2 data The compare 2 value must be above or equal to 3 periods of the f_{SHRTIM} clock, that is 0x60 if SHRTIM_TxCTRL.CKPSC[2:0] = 0, 0x30 if SHRTIM_TxCTRL.CKPSC[2:0] = 1, 0x18 if SHRTIM_TxCTRL.CKPSC[2:0] = 2,... When PLEN is set to 1, the register will configure the value to the compare 2 preload register. If PLEN is reset, the register value will be directly loaded to the active compare 2 register.

17.3.24 SHRTIM Timer x Compare 3 Register（SHRTIM_TxCMP3DAT）

Address offset: 0xA8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP3DAT															
rw															

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Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	CMP3DAT	Timer x compare 3 data The compare 3 value must be above or equal to 3 periods of the f_{SHRTIM} clock, that is 0x60 if SHRTIM_TxCTRL.CKPSC[2:0] = 0, 0x30 if SHRTIM_TxCTRL.CKPSC[2:0] = 1, 0x18 if SHRTIM_TxCTRL.CKPSC[2:0] = 2,... When PLEN is set to 1, the register will configure the value to the compare 3 preload register. If PLEN is reset, the register value will be directly loaded to the active compare 3 register.

17.3.25 SHRTIM Timer x Compare 4 Register（SHRTIM_TxCMP4DAT）

Address offset: 0xAC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP4DAT															

rw

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	CMP4DAT	Timer A compare 4 data The compare 4 value must be above or equal to 3 periods of the f_{SHRTIM} clock, that is 0x60 if SHRTIM_TxCTRL.CKPSC[2:0] = 0, 0x30 if SHRTIM_TxCTRL.CKPSC[2:0] = 1, 0x18 if SHRTIM_TxCTRL.CKPSC[2:0] = 2,... When PLEN is set to 1, the register will configure the value to the compare 4 preload register. If PLEN is reset, the register value will be directly loaded to the active compare 4 register.

17.3.26 SHRTIM Timer x Capture 1 Register（SHRTIM_TxCPT1）

Address offset: 0xB0

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															UDSTS1
															r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPT1															
r															

Bit Field	Name	Description
[31:17]	Reserved	Reserved, the reset value must be maintained
[16]	UDSTS1	Status for timer x counting direction while capture 1 happened 0: Timer x is up-counting 1: Timer x is down-counting In up-counting mode, the UDSTS1 bit is always read as 0.
[15:0]	CPT1	Timer x Capture 1 value This register holds the counter value when the capture 1 event occurred.

Notes: In up/down mode (UPDOWNM bit set to 1), the capture value is referred to:

- *The counting reset, when up-counting*
- *The PRD event when down counting and the capture value = counter value*

The UDSTS1 bit allows to discriminate the up-down phases when reading the captured value.

Note: This is a regular resolution register: for SHRTIMER clock prescaling ratio below 32 (CKPSC[2:0] < 5), the least significant bits of the counter are not significant. They cannot be written and return 0 when read.

17.3.27 SHRTIM Timer x Capture 2 Register（SHRTIM_TxCPT2）

Address offset: 0xB4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															UDSTS2
															r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPT2															
r															

Bit Field	Name	Description
[31:17]	Reserved	Reserved, the reset value must be maintained

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[16]	UDSTS2	Status for timer x counting direction while capture 2 happened 0: Timer x is up-counting 1: Timer x is down-counting In up-counting mode, the UDSTS2 bit is always read as 0.
[15:0]	CPT2	Timerx Capture 2 value This register holds the counter value when the capture 2 event occurred.

Notes: In up/down mode (UPDOWNM bit set to 1), the capture value is referred to:

- *The counting reset, when up-counting*
- *The PRD event when down counting and the capture value = counter value*

The UDSTS2 bit allows to discriminate the up-down phases when reading the captured value.

Note: This is a regular resolution register: for SHRTIMER clock prescaling ratio below 32 (CKPSC[2:0] < 5), the least significant bits of the counter are not significant. They cannot be written and return 0 when read.

17.3.28 SHRTIM Timer x Deadtime Register（SHRTIM_TxDT）

Address offset: 0xB8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTFLCK	DTFSLCK	Reserved				SDTF	DTF								
rw	rw					rw	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTRLCK	DTRSLCK	Reserved	DTPSC			SDTR	DTR								
rw	rw		rw			rw	rw								

Bit Field	Name	Description
[31]	DTFLCK	Deadtime Falling Lock This write-once bit prevents the deadtime (sign and value) to be modified, if enabled. 0: Deadtime falling value and sign is writable 1: Deadtime falling value and sign is read-only *Note: This bit is not preloaded*
[30]	DTFSLCK	Deadtime Falling Sign Lock This write-once bit prevents the sign of falling deadtime to be modified, if enabled. 0: Deadtime falling sign is writable 1: Deadtime falling sign is read-only *Note: This bit is not preloaded.*

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[29:26]	Reserved	Reserved, the reset value must be maintained
[25]	SDTF	Sign Deadtime Falling value This register determines whether the deadtime is positive (signals not overlapping) or negative (signals overlapping). 0: Positive deadtime on falling edge 1: Negative deadtime on falling edge
[24:16]	DTF	Deadtime Falling data value This register holds the value of the deadtime following a falling edge of reference PWM signal. t_{DTF} = DTF[8:0] x t_{DTG}
[15]	DTRLCK	Deadtime Rising Lock This write-once bit prevents the deadtime (sign and value) to be modified, if enabled. 0: Deadtime rising value and sign is writable 1: Deadtime rising value and sign is read-only *Note: This bit is not preloaded.*
[14]	DTRSLCK	Deadtime rising sign lock This write-once bit prevents the sign of deadtime to be modified, if enabled. 0: Deadtime rising sign is writable 1: Deadtime rising sign is read-only *Note: This bit is not preloaded.*
[13]	Reserved	Reserved, the reset value must be maintained
[12:10]	DTPSC	Deadtime prescaler This register holds the value of the deadtime clock prescaler. t_{DTG} = (2(DTPSC[2:0])) x (t_{SHRTIM} / 8) This bitfield is read-only as soon as any of the lock bit is enabled (DTFLCK, DTFSLCK, DTRLCK, DTRSLCK).
[9]	SDTR	Sign deadtime rising value This register determines whether the deadtime is positive or negative (overlapping signals). 0: Positive deadtime on rising edge 1: Negative deadtime on rising edge
[8:0]	DTR	Deadtime rising value This register holds the value of the deadtime following a rising edge of reference PWM signal. t_{DTR} = DTR[8:0] x t_{DTG}

17.3.29 SHRTIM Timer x Output 1 Set Register（SHRTIM_TxSET1）

Address offset: 0xBC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD	EXEV10	EXEV9	EXEV8	EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	TIMEV9	TIMEV8	TIMEV7	TIMEV6	TIMEV5

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rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEV 4	TIMEV 3	TIMEV 2	TIMEV 1	MCMP 4	MCMP 3	MCMP 2	MCMP 1	MPRD	CMP4	CMP3	CMP2	CMP1	PRD	RSYNC	SWT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31]	UPD	Registers update (transfer preload to active) Register update event forces the output to its active state.
[30]	EXEV10	External Event 10 Refer to the EXEV1 description
[29]	EXEV9	External Event 9 Refer to the EXEV1 description
[28]	EXEV8	External Event 8 Refer to the EXEV1 description
[27]	EXEV7	External Event 7 Refer to the EXEV1 description
[26]	EXEV6	External Event 6 Refer to the EXEV1 description
[25]	EXEV5	External Event 5 Refer to the EXEV1 description
[24]	EXEV4	External Event 4 Refer to the EXEV1 description
[23]	EXEV3	External Event 3 Refer to the EXEV1 description
[22]	EXEV2	External Event 2 Refer to the EXEV1 description
[21]	EXEV1	External Event 1 External event 1 forces the output to its active state.
[20]	TIMEV9	Timer Event 9 Refer to the TIMEV1 description
[19]	TIMEV8	Timer Event 8 Refer to the TIMEV1 description
[18]	TIMEV7	Timer Event 7 Refer to the TIMEV1 description
[17]	TIMEV6	Timer Event 6 Refer to the TIMEV1 description
[16]	TIMEV5	Timer Event 5 Refer to the TIMEV1 description
[15]	TIMEV4	Timer Event 4 Refer to the TIMEV1 description
[14]	TIMEV3	Timer Event 3 Refer to the TIMEV1 description

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[13]	TIMEV2	Timer Event 2 Refer to the TIMEV1 description
[12]	TIMEV1	Timer Event 1 Timers event 1 forces the output to its active state (refer to for timer events assignments)
[11]	MCMP4	Master Compare 4 Master timer compare 4 event forces the output to its active state.
[10]	MCMP3	Master Compare 3 Master timer compare 3 event forces the output to its active state.
[9]	MCMP2	Master Compare 2 Master timer compare 2 event forces the output to its active state.
[8]	MCMP1	Master Compare 1 Master timer compare 1 event forces the output to its active state.
[7]	MPRD	Master Period The master timer counter roll-over in continuous mode, or the master timer reset in single-shot mode forces the output to its active state.
[6]	CMP4	Timer x Compare 4 Timer x compare 4 event forces the output to its active state.
[5]	CMP3	Timer x Compare 3 Timer x compare 3 event forces the output to its active state.
[4]	CMP2	Timer x Compare 2 Timer x compare 2 event forces the output to its active state.
[3]	CMP1	Timer x Compare 1 Timer x compare 1 event forces the output to its active state.
[2]	PRD	Timer x Period Timer x period event forces the output to its active state
[1]	RSYNC	Timer x resynchronization Timer x reset event coming solely from software or SYNC input forces the output to its active state. *Note: Other timer reset are not affecting the output when RSYNC=1.*
[0]	SWT	Software Set trigger This bit forces the output to its active state. This bit can only be set by software and is reset by hardware. *Note: This bit is not preloaded.*

17.3.30 SHRTIM Timer x Output 1 Reset Register（SHRTIM_TxRST1）

Address offset: 0xC0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD	EXEV10	EXEV9	EXEV8	EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	TIMEV9	TIMEV8	TIMEV7	TIMEV6	TIMEV5

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rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEV4	TIMEV3	TIMEV2	TIMEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP3	CMP2	CMP1	PRD	RSYNC	SWT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Refer to SHRTIM_TxSET1 bits description. These bits are defining the source which can force the Tx1 output to its inactive state.

17.3.31 SHRTIM Timer x Output 2 Set Register（SHRTIM_TxSET2）

Address offset: 0xC4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD	EXEV10	EXEV9	EXEV8	EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	TIMEV9	TIMEV8	TIMEV7	TIMEV6	TIMEV5
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEV4	TIMEV3	TIMEV2	TIMEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP3	CMP2	CMP1	PRD	RSYNC	SWT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Refer to SHRTIM_TxSET1 bits description. These bits are defining the source which can force the Tx2 output to its active state.

17.3.32 SHRTIM Timer x Output 2 Reset Register（SHRTIM_TxRST2）

Address offset: 0xC8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD	EXEV10	EXEV9	EXEV8	EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	TIMEV9	TIMEV8	TIMEV7	TIMEV6	TIMEV5
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEV4	TIMEV3	TIMEV2	TIMEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP3	CMP2	CMP1	PRD	RSYNC	SWT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Refer to SHRTIM_TxSET2 bits description. These bits are defining the source which can force the Tx2 output to its inactive state.

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17.3.33 SHRTIM Timer x External Event Filtering Register 1 （SHRTIM_TxEXEVFLT1）

Address offset: 0xCC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			EXEV5FLT				EXEV5LATCH	Reserved	EXEV4FLT				EXEV4LATCH	Reserved	EXEV3FLT
			rw				rw		rw				rw	r	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			EXEV3LATCH	Reserved	EXEV2FLT				EXEV2LATCH	Reserved	EXEV1FLT				EXEV1LATCH
			rw		rw				rw		rw				rw

Bit Field	Name	Description
[31:29]	Reserved	Reserved, the reset value must be maintained
[28:25]	EXEV5FLT	External Event 5 filter Refer to the EXEV1FLT[3:0] description
[24]	EXEV5LATCH	External event 5 latch Refer to the EXEV1LATCH description
[23]	Reserved	Reserved, the reset value must be maintained
[22:19]	EXEV4FLT	External Event 4 filter Refer to the EXEV1FLT[3:0] description
[18]	EXEV4LATCH	External event 4 latch Refer to the EXEV1LATCH description
[17]	Reserved	Reserved, the reset value must be maintained
[16:13]	EXEV3FLT	External Event 3 filter Refer to the EXEV1FLT[3:0] description
[12]	EXEV3LATCH	External event 3 latch Refer to the EXEV1LATCH description
[11]	Reserved	Reserved, the reset value must be maintained
[10:7]	EXEV2FLT	External Event 2 filter Refer to the EXEV1FLT[3:0] description
[6]	EXEV2LATCH	External event 2 latch Refer to the EXEV1LATCH description
[5]	Reserved	Reserved, the reset value must be maintained
[4:1]	EXEV1FLT	External Event 1 filter 0000: No filtering 0001: Blanking from counter reset/roll-over to compare 1 0010: Blanking from counter reset/roll-over to compare 2 in up-counting mode (SHRTIM_TxCTRL2.UPDOWNM bit reset). In up-down counting mode (SHRTIM_TxCTRL2.UPDOWNM bit set): blanking from compare 1 to

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		compare 2, only during the up-counting phase. 0011: Blanking from counter reset/roll-over to compare 3 0100: Blanking from counter reset/roll-over to compare 4 0100: Blanking from counter reset/roll-over to compare 4 in up-counting mode (SHRTIM_TxCTRL2.UPDOWNM bit reset). In up-down counting mode (SHRTIM_TxCTRL2.UPDOWNM bit set): blanking from compare 3 to compare 4, only during the up-counting phase. 0101: Blanking from another timing unit: TIMFLTR1 source (refer to for details） 0110: Blanking from another timing unit: TIMFLTR2 source (refer to for details） 0111: Blanking from another timing unit: TIMFLTR3 source (refer to for details) 1000: Blanking from another timing unit: TIMFLTR4 source (refer to for details） 1001: Blanking from another timing unit: TIMFLTR5 source (refer to for details） 1010: Blanking from another timing unit: TIMFLTR6 source (refer to for details） 1011: Blanking from another timing unit: TIMFLTR7 source (refer to for details） 1100: Blanking from another timing unit: TIMFLTR8 source (refer to for details） 1101: Windowing from counter reset/roll-over to compare 2 in up-counting mode (SHRTIM_TxCTRL2.UPDOWNM bit reset). In up-down counting mode (SHRTIM_TxCTRL2.UPDOWNM bit set): windowing from compare 2 to compare 3, only during the up-counting phase. 1110: Windowing from counter reset/roll-over to compare 3 in up-counting mode (SHRTIM_TxCTRL2.UPDOWNM bit reset). In up-down counting mode (SHRTIM_TxCTRL2.UPDOWNM bit set): windowing from compare 2 to compare 3, only during the down-counting phase. 1111：Windowing from another timing unit: TIMWIN source (refer to for details）in upcounting mode (SHRTIM_TxCTRL2.UPDOWNM bit reset). In up-down counting mode (SHRTIM_TxCTRL2.UPDOWNM bit set): windowing from compare 2 during the up-counting phase to compare 3 during the down-counting phase. *Note: Whenever a compare register is used for filtering, the value must be strictly above 0.* *This bitfield must not be modified once the counter is enabled (TxCNTEN bit set)*
[0]	EXEV1LATCH	External Event 1 latch 0: Event 1 is ignored if it happens during a blank, or passed through during a window. 1: Event 1 is latched and delayed till the end of the blanking or windowing period. *Note: A timeout event is generated in window mode (EXEV1FLT[3:0]=1101、1110、1111) if EE1LTCH = 0, except if the external event is programmed in fast mode (EXEV1FM = 1).* *This bitfield must not be modified once the counter is enabled (TxCNTEN bit set)*

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17.3.34 SHRTIM Timer x External Event Filtering Register 2 （SHRTIM_TxEXEVFLT2）

Address offset: 0xD0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			EXEV10FLT				EXEV10LATCH	Reserved	EXE9VFLT				EXEV9LATCH	Reserved	EXE8VFLT
			rw				rw		rw				rw	r	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			EXEV8LATCH	Reserved	EXE7VFLT				EXEV7LATCH	Reserved	EXE6VFLT				EXEV6LATCH
			rw		rw				rw		rw				rw

Bit Field	Name	Description
[31:29]	Reserved	Reserved, the reset value must be maintained
[28:25]	EXEV10FLT	External Event 10 filter Refer to the EXEV1FLT[3:0] description
[24]	EXEV10LATCH	External Event 10 latch Refer to the EXEV1LATCH description
[23]	Reserved	Reserved, the reset value must be maintained
[22:19]	EXE9VFLT	External Event 9 filter Refer to the EXEV1FLT[3:0] description
[18]	EXEV9LATCH	External Event 9 latch Refer to the EXEV1LATCH description
[17]	Reserved	Reserved, the reset value must be maintained
[16:13]	EXE8VFLT	External Event 8 filter Refer to the EXEV1FLT[3:0] description
[12]	EXEV8LATCH	External Event 8 latch Refer to the EXEV1LATCH description
[11]	Reserved	Reserved, the reset value must be maintained
[10:7]	EXE7VFLT	External Event 7 filter Refer to the EXEV1FLT[3:0] description
[6]	EXEV7LATCH	External Event 7 latch Refer to the EXEV1LATCH description
[5]	Reserved	Reserved, the reset value must be maintained
[4:1]	EXE6VFLT	External Event 6 filter Refer to the EXEV1FLT[3:0]
[0]	EXEV6LATCH	External Event 6 latch Refer to the EXEV1LATCH description

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17.3.35 SHRTIM Timer A Counter Reset Register（SHRTIM_TACNTRST）

Address offset: 0xD4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCMP2	TECMP4	TECMP2	TECMP1	TDCMP4	TDCMP2	TDCMP1	TCCMP4	TCCMP2	TCCMP1	TBCMP4	TBCMP2	TBCMP1	EXEV10	EXEV9	EXEV8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP2	UPD	TFCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31]	TFCMP2	Timer F Compare 2 The timer A counter is reset upon timer F compare 2 event.
[30]	TECMP4	Timer E Compare 4 The timer A counter is reset upon timer E compare 4 event.
[29]	TECMP2	Timer E Compare 2 The timer A counter is reset upon timer E compare 2 event.
[28]	TECMP1	Timer E Compare 1 The timer A counter is reset upon timer E compare 1 event.
[27]	TDCMP4	Timer D Compare 4 The timer A counter is reset upon timer D compare 4 event.
[26]	TDCMP2	Timer D Compare 2 The timer A counter is reset upon timer D compare 2 event.
[25]	TDCMP1	Timer D Compare 1 The timer A counter is reset upon timer D compare 1 event.
[24]	TCCMP4	Timer C Compare 4 The timer A counter is reset upon timer C compare 4 event.
[23]	TCCMP2	Timer C Compare 2 The timer A counter is reset upon timer C compare 2 event.
[22]	TCCMP1	Timer C Compare 1 The timer A counter is reset upon timer C compare 1 event.
[21]	TBCMP4	Timer B Compare 4 The timer A counter is reset upon timer B compare 4 event.
[20]	TBCMP2	Timer B Compare 2 The timer A counter is reset upon timer B compare 2 event.
[19]	TBCMP1	Timer B Compare 1 The timer A counter is reset upon timer B compare 1 event.
[18]	EXEV10	External event 10 The timer A counter is reset upon external event 10.
[17]	EXEV9	External event 9

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		The timer A counter is reset upon external event 9.
[16]	EXEV8	External event 8 The timer A counter is reset upon external event 8.
[15]	EXEV7	External event 7 The timer A counter is reset upon external event 7.
[14]	EXEV6	External event 6 The timer A counter is reset upon external event 6.
[13]	EXEV5	External event 5 The timer A counter is reset upon external event 5.
[12]	EXEV4	External event 4 The timer A counter is reset upon external event 4.
[11]	EXEV3	External event 3 The timer A counter is reset upon external event 3.
[10]	EXEV2	External event 2 The timer A counter is reset upon external event 2.
[9]	EXEV1	External event 1 The timer A counter is reset upon external event 1.
[8]	MCMP4	Master timer compare 4 The timer A counter is reset upon master timer compare 4 event.
[7]	MCMP3	Master timer compare 3 The timer A counter is reset upon master timer compare 3 event.
[6]	MCMP2	Master timer compare 2 The timer A counter is reset upon master timer compare 2 event.
[5]	MCMP1	Master timer compare 1 The timer A counter is reset upon master timer compare 1 event.
[4]	MPRD	Master timer period The timer A counter is reset upon master timer period event.
[3]	CMP4	TIMA compare 4 The timer A counter is reset upon timer A compare 4 event.
[2]	CMP2	TIMA compare 2 The timer A counter is reset upon timer A compare 2 event.
[1]	UPD	TIMA update The timer A counter is reset upon update event.
[0]	TFCMP1	TIMF compare 1 The timer A counter is reset upon timer F compare 1 event.

17.3.36 SHRTIM Timer B Counter Reset Register（SHRTIM_TBCNTRST）

Address offset: 0x154

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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TFCMP2	TECMP4	TECMP2	TECMP1	TDCMP4	TDCMP2	TDCMP1	TCCMP4	TCCMP2	TCCMP1	TACMP4	TACMP2	TACMP1	EXEV10	EXEV9	EXEV8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP2	UPD	TFCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Please refer to the SHRTIM_TACNTRST description.

Bits 30:19 and bit 0 are different (the reset signals from TIMA, TIMC, TIMD, TIME, and TIMF).

17.3.37 SHRTIM Timer C Counter Reset Register（SHRTIM_TCCNTRST）

Address offset: 0x1D4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCMP2	TECMP4	TECMP2	TECMP1	TDCMP4	TDCMP2	TDCMP1	TBCMP4	TBCMP2	TBCMP1	TACMP4	TACMP2	TACMP1	EXEV10	EXEV9	EXEV8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP2	UPD	TFCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Please refer to the SHRTIM_TACNTRST description.

Bits 30:19 and bit 0 are different (the reset signals from TIMA, TIMC, TIMD, TIME, and TIMF).

17.3.38 SHRTIM Timer D Counter Reset Register（SHRTIM_TDCNTRST）

Address offset: 0x254

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCMP2	TECMP4	TECMP2	TECMP1	TCCMP4	TCCMP2	TCCMP1	TBCMP4	TBCMP2	TBCMP1	TACMP4	TACMP2	TACMP1	EXEV10	EXEV9	EXEV8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP2	UPD	TFCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Please refer to the SHRTIM_TACNTRST description.

Bits 30:19 and bit 0 are different (the reset signals from TIMA, TIMC, TIMD, TIME, and TIMF).

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17.3.39 SHRTIM Timer E Counter Reset Register（SHRTIM_TECNTRST）

Address offset: 0x2D4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCMP2	TDCMP4	TDCMP2	TDCMP1	TCCMP4	TCCMP2	TCCMP1	TBCMP4	TBCMP2	TBCMP1	TACMP4	TACMP2	TACMP1	EXEV10	EXEV9	EXEV8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP2	UPD	TFCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Please refer to the SHRTIM_TACNTRST description.

Bits 30:19 and bit 0 are different (the reset signals from TIMA, TIMC, TIMD, TIME, and TIMF).

17.3.40 SHRTIM Timer F Counter Reset Register（SHRTIM_TFCNTRST）

Address offset: 0x354

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TDCMP4	TDCMP2	TDCMP1	TCCMP4	TCCMP2	TCCMP1	TBCMP4	TBCMP2	TBCMP1	TACMP4	TACMP2	TACMP1	EXEV10	EXEV9	EXEV8
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV7	EXEV6	EXEV5	EXEV4	EXEV3	EXEV2	EXEV1	MCMP4	MCMP3	MCMP2	MCMP1	MPRD	CMP4	CMP2	UPD	TECMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Please refer to the SHRTIM_TACNTRST description.

Bits 30:19 and bit 0 are different (the reset signals from TIMA, TIMC, TIMD, TIME, and TIMF).

17.3.41 SHRTIM Timer x Chopper Register（SHRTIM_TxCHOP）

Address offset: 0xD8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	STARTPW	CARDCY	CARFRQ
	rw	rw	rw

Bit Field	Name	Description
[31:11]	Reserved	Reserved, the reset value must be maintained
[10:7]	STARTPW	Timer x start pulse width This register defines the initial pulsewidth following a rising edge on output signal. This bitfield cannot be modified when one of the SHRTIM_TxOUT.CHPy bits is set. t_{1STPW} = (STARTPW [3:0]+1) x 16 x t_{SHRTIM}. 0000：64.0 ns 0001：128.0 ns ... 1111：1024.0 ns
[6:4]	CARDCY	Timer x chopper duty cycle value This register defines the duty cycle of the carrier signal. This bitfield cannot be modified when one of the SHRTIM_TxOUT.CHPy bits is set. 000：0/8（i.e. only 1st pulse is present） ... 111：7/8
[3:0]	CARFRQ	Timer x carrier frequency value This register defines the carrier frequency f_{CHPFRQ} = f_{SHRTIM} / (16 x (CARFRQ[3:0]+1)). This bitfield cannot be modified when one of the SHRTIM_TxOUT.CHPCHy bits is set. 0000: 15.625 MHz (f_{SHRTIM}/16) ... 1111: 976.563khz (f_{SHRTIM}/256)

17.3.42 SHRTIM Timer A Capture 1 Control Register (SHRTIM_TACPT1CTRL)

Address offset: 0x0DC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFCMP2	TFCMP1	TF1RST	TF1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Bit Field	Name	Description
[31]	TECMP2	TIME compare 2 0: No action

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		1: Timer E compare 2 triggers the timer A capture 1
[30]	TECMP1	TIME compare 1 0: No action 1: Timer E compare 1 triggers the timer A capture 1
[29]	TE1RST	TIME channel 1 output reset 0: No action 1: The timer A capture 1 is triggered by TE1 output active to inactive
[28]	TE1SET	TIME channel 1 output set 0: No action 1: The timer A capture 1 is triggered by TE1 output inactive to active
[27]	TDCMP2	TIMD compare 2 0: No action 1: Timer D compare 2 triggers the timer A capture 1
[26]	TDCMP1	TIMD compare 1 0: No action 1: Timer D compare 1 triggers the timer A capture 1
[25]	TD1RST	TIMD output 1 reset 0: No action 1: The timer A capture 1 is triggered by TD1 output active to inactive
[24]	TD1SET	TIMD output 1 set 0: No action 1: The timer A capture 1 is triggered by TD1 output inactive to active
[23]	TCCMP2	TIMC compare 2 0: No action 1: Timer C compare 2 triggers the timer A capture 1
[22]	TCCMP1	TIMC compare 1 0: No action 1: Timer C compare 1 triggers the timer A capture 1
[21]	TC1RST	TIMC output 1 reset 0: No action 1: The timer A capture 1 is triggered by TC1 output active to inactive
[20]	TC1SET	TIMC output 1 set 0: No action 1: The timer A capture 1 is triggered by TC1 output inactive to active
[19]	TBCMP2	TIMB compare 2 0: No action 1: Timer B compare 2 triggers the timer A capture 1
[18]	TBCMP1	TIMB compare 1 0: No action 1: Timer B compare 1 triggers the timer A capture 1
[17]	TB1RST	TIMB ouput 1 reset 0: No action

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		1: The timer A capture 1 is triggered by TB1 output active to inactive transition
[16]	TB1SET	TIMB output 1 set 0: No action 1: The timer A capture 1 is triggered by TB1 output inactive to active transition
[15]	TFCMP2	TIMF compare 2 0: No action 1: Timer F compare 2 triggers the timer A capture 1
[14]	TFCMP1	TIMF compare 1 0: No action 1: Timer F compare 1 triggers the timer A capture 1
[13]	TF1RST	TIMF output 1 reset 0: No action 1: The timer A capture 1 is triggered by TF1 output active to inactive transition
[12]	TF1SET	TIMF output 1 set 0: No action 1: The timer A capture 1 is triggered by TF1 output inactive to active transition
[11]	EXEV10CPT	External event 10 capture 0: No action 1: The external event 10 triggers the timer A capture 1
[10]	EXEV9CPT	External event 10 capture 0: No action 1: The external event 9 triggers the timer A capture 1
[9]	EXEV8CPT	External event 8 capture 0: No action 1: The external event 8 triggers the timer A capture 1
[8]	EXEV7CPT	External event 7 capture 0: No action 1: The external event 7 triggers the timer A capture 1
[7]	EXEV6CPT	External event 6 capture 0: No action 1: The external event 6 triggers the timer A capture 1
[6]	EXEV5CPT	External event 5 capture 0: No action 1: The external event 5 triggers the timer A capture 1
[5]	EXEV4CPT	External event 4 capture 0: No action 1: The external event 4 triggers the timer A capture 1
[4]	EXEV3CPT	External event 3 capture

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		0: No action 1: The external event 3 triggers the timer A capture 1
[3]	EXEV2CPT	External event 2 capture 0: No action 1: The external event 2 triggers the timer A capture 1
[2]	EXEV1CPT	External event 1 capture 0: No action 1: The external event 1 triggers the timer A capture 1
[1]	UPDCPT	Update capture 0: No action 1: The update event triggers the timer A capture 1
[0]	SWCPT	Software capture 0: No action 1: This bit forces the timer A capture 1 by software Note: This bit is set only, reset by hardware

17.3.43 SHRTIM Timer A Capture 2 Control Register (SHRTIM_TACPT2CTRL)

Address offset: 0x0E0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFCMP2	TFCMP1	TF1RST	TF1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

17.3.44 SHRTIM Timer B Capture 1 Control Register (SHRTIM_TBCPT1CTRL)

Address offset: 0x15C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TFCMP2	TFCMP1	TF1RST	TF1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	Rw	rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	Rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMC, TIMD, TIME, and TIMF).

17.3.45 SHRTIM Timer B Capture 2 Control Register (SHRTIM_TBCPT2CTRL)

Address offset: 0x160

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TFCMP2	TFCMP1	TF1RST	TF1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMC, TIMD, TIME, and TIMF).

17.3.46 SHRTIM Timer C Capture 1 Control Register (SHRTIM_TCCPT1CTRL)

Address offset: 0x1DC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TFCMP2	TFCMP1	TF1RST	TF1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	Rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	Rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMD, TIME, and TIMF).

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17.3.47 SHRTIM Timer C Capture 2 Control Register (SHRTIM_TCCPT2CTRL)

Address offset: 0x1E0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TFCMP2	TFCMP1	TF1RST	TF1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMD, TIME, and TIMF).

17.3.48 SHRTIM Timer D Capture 1 Control Register (SHRTIM_TDCPT1CTRL)

Address offset: 0x25C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TFCMP2	TFCMP1	TF1RST	TF1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMC, TIME, and TIMF).

17.3.49 SHRTIM Timer D Capture 2 Control Register (SHRTIM_TDCPT2CTRL)

Address offset: 0x260

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TFCMP2	TFCMP1	TF1RST	TF1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMC, TIME, and TIMF).

17.3.50 SHRTIM Timer E Capture 1 Control Register (SHRTIM_TECPT1CTRL)

Address offset: 0x2DC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCMP2	TFCMP1	TF1RST	TF1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	Rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	Rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMC, TIMD, and TIMF).

17.3.51 SHRTIM Timer E Capture 2 Control Register (SHRTIM_TECPT2CTRL)

Address offset: 0x2E0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCMP2	TFCMP1	TF1RST	TF1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT

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rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMC, TIMD, and TIMF).

17.3.52 SHRTIM Timer F Capture 1 Control Register (SHRTIM_TFCPT1CTRL)

Address offset: 0x35C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMC, TIMD, and TIME).

17.3.53 SHRTIM Timer F Capture 2 Control Register (SHRTIM_TFCPT2CTRL)

Address offset: 0x360

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TECMP2	TECMP1	TE1RST	TE1SET	TDCMP2	TDCMP1	TD1RST	TD1SET	TCCMP2	TCCMP1	TC1RST	TC1SET	TBCMP2	TBCMP1	TB1RST	TB1SET
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TACMP2	TACMP1	TA1RST	TA1SET	EXEV10CPT	EXEV9CPT	EXEV8CPT	EXEV7CPT	EXEV6CPT	EXEV5CPT	EXEV4CPT	EXEV3CPT	EXEV2CPT	EXEV1CPT	UPDCPT	SWCPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Refer to the SHRTIM_TACPT1CTRL description.

Bits 31:12 are different (from TIMA, TIMB, TIMC, TIMD, and TIME).

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17.3.54 SHRTIM Timer x Output Register (SHRTIM_TxOUT)

Address offset: 0x0E4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								DIDL2	CHP2	FALT2		IDLES 2	IDLEM 2	POL2	Reserve d
								rw	rw	rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserve d	BIAR	Reserve d	DP			DPEN	DTEN	DIDL1	CHP1	FALT1		IDLES 1	IDLEM 1	POL1	Reserve d
	rw		rw			rw	rw	rw	rw	rw		rw		rw	

Bit Field	Name	Description
[31:24]	Reserved	Reserved, the reset value must be maintained
[23]	DIDL2	Output 2 Deadtime upon burst mode Idle entry This bit delays the idle mode entry by forcing a deadtime insertion before switching the outputs to their idle state. This setting only applies when entering in idle state during a burst mode operation. 0: The programmed idle state is applied immediately to the output 2 1: Deadtime (inactive level) is inserted on output 2 before entering the idle mode. The deadtime value is set by DTF[8:0]. *Note: This parameter cannot be changed once the timer x is enabled.* *Note: DIDL=1 is set only if one of the outputs is active during the burst mode (IDLES=1), and with positive deadtimes (SDTR/SDTF set to 0).*
[22]	CHP2	Output 2 Chopper enable This bit enables the chopper on output 2. 0: Output signal is not changed 1: Output signal is chopped by a carrier signal *Note: This parameter cannot be changed once the timer x is enabled.*
[21:20]	FALT2	Output 2 Fault state These bits select the output 2 state after a fault event. 00: No action: the output is not affected by the fault input and stays in run mode. 01: Active 10: Inactive 11: High-Z *Note: This parameter cannot be changed once the timer x is enabled (TxCNTEN bit set), if FALTENx bit is set or if the output is in FAULT state.*
[19]	IDLES2	Output 2 Idle State This bit selects the output 2 idle state. 0: Inactive 1: Active *Note: This parameter must be set prior to have the SHRTIM controlling the*

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		outputs
[18]	IDLEM2	This bit selects the output 2 idle mode. 0: No action: the output is not affected by the burst mode operation. 1: The output is in idle state when requested by the burst mode controller.
[17]	POL2	Output 2 polarity This bit selects the output 2 polarity. 0: Positive polarity (output active high) 1: Negative polarity (output active low) *Note: This parameter cannot be changed once the timer x is enabled.*
[16:15]	Reserved	Reserved, the reset value must be maintained
[14]	BIAR	Balanced idle automatic resume This bit selects the outputs are automatically re-enabled after a balanced idle event. This bit is only significant if DP[2:0] = 011 or 111, it is ignored otherwise. 0: Disabled 1: Enabled *Note: This parameter cannot be changed once the timer x is enabled.*
[13]	Reserved	Reserved, the reset value must be maintained
[12:10]	DP	Delayed Protection These bits define the source and outputs on which the delayed protection schemes are applied. **In SHRTIM_TAOUT, SHRTIM_TBOUT, SHRTIM_TCOUT:** 000: Output 1 enters delayed idle on external event 6 001: Output 2 enters delayed idle on external event 6 010: Output 1 and output 2 both enter delayed idle on external event 6 011: Enters balanced idle on external event 6 100: Output 1 enters delayed idle on external event 7 101: Output 2 enters delayed idle on external event 7 110: Output 1 and output 2 both enter delayed idle on external event 7 111: Enters balanced idle on external event 7 **In SHRTIM_TDOUT、SHRTIM_TEOUT、SHRTIM_TFOUT:** 000: Output 1 enters delayed idle on external event 8 001: Output 2 enters delayed idle on external event 8 010: Output 1 and output 2 both enter delayed idle on external event 8 011: Enters balanced idle on external event 8 100: Output 1 enters delayed idle on external event 9 101: Output 2 enters delayed idle on external event 9 110: Output 1 and output 2 both enter delayed idle on external event 9 111: Enters balanced idle on external event 9
[9]	DPEN	Delayed Protection Enable This bit enables the delayed protection scheme. 0: No action 1: Delayed protection is enabled, as per DP[2:0] bits *Note: This parameter cannot be changed once the timer x is enabled (TxCNTEN*

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		bit set).
[8]	DTEN	Deadtime enable This bit enables the deadtime insertion on output 1 and output 2. 0: Output 1 and output 2 signals are independent. 1: Deadtime is inserted between output 1 and output 2 (reference signal is output 1 signal generator) *Note: This parameter cannot be changed once the timer is operating (TxCNTEN bit set) or if its outputs are enabled and set/reset by another timer*
[7]	DIDL1	Output 1 Deadtime upon burst mode Idle entry This bit delays the idle mode entry by forcing a deadtime insertion before switching the outputs to their idle state. This setting only applies when entering in idle state during a burst mode operation. 0: The programmed idle state is applied immediately to the output 1 1: Deadtime (inactive level) is inserted on output 1 before entering the idle mode. The deadtime value is set by DTF[8:0]. *Note: This parameter cannot be changed once the timer x is enabled.* *Note: DIDL=1 is set only if one of the outputs is active during the burst mode (IDLES=1), and with positive deadtimes (SDTR/SDTF set to 0).*
[6]	CHP1	Output 1 Chopper enable This bit enables the chopper on output 1. 0: Output signal is not changed 1: Output signal is chopped by a carrier signal *Note: This parameter cannot be changed once the timer x is enabled.*
[5:4]	FALT1	Output 1 Fault state These bits select the output 1 state after a fault event. 00: No action: the output is not affected by the fault input and stays in run mode. 01: Active 10: Inactive 11: High-Z *Note: This parameter cannot be changed once the timer x is enabled (TxCNTEN bit set), if FALTENx bit is set or if the output is in FAULT state.*
[3]	IDLES1	Output 1 Idle State This bit selects the output 1 idle state. 0: Inactive 1: Active *Note: This parameter must be set prior to have the SHRTIM controlling the outputs*
[2]	IDLEM1	Output 1 Idle mode. This bit selects the output 1 idle mode. 0: No action: the output is not affected by the burst mode operation. 1: The output is in idle state when requested by the burst mode controller.
[1]	POL1	Output 1 polarity This bit selects the output 1 polarity.

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		0: Positive polarity (output active high) 1: Negative polarity (output active low) *Note: This parameter cannot be changed once the timer x is enabled.*
[0]	Reserved	Reserved, the reset value must be maintained

17.3.55 SHRTIM Timer x Fault Register (SHRTIM_TxFALT)

Address offset: 0x0E8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FALTLCK	Reserved														
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										FALT6EN	FALT5EN	FALT4EN	FALT3EN	FALT2EN	FALT1EN
										rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31]	FALTLCK	Fault sources lock 0: FALT1EN..FALT6EN bits are read/write 1: FALT1EN..FALT6EN bits are read only The FALTLCK bit is write-once. Once it has been set, it cannot be modified till the next system reset.
[30:6]	Reserved	Reserved, the reset value must be maintained
[5]	FALT6EN	FAULT 6 enable 0: Fault 6 input is ignored 1: Fault 6 input is active and disables SHRTIM outputs
[4]	FALT5EN	FAULT 5 enable 0: Fault 5 input is ignored 1: Fault 5 input is active and disables SHRTIM outputs
[3]	FALT4EN	FAULT 4 enable 0: Fault 4 input is ignored 1: Fault 4 input is active and disables SHRTIM outputs
[2]	FALT3EN	FAULT 3 enable 0: Fault 3 input is ignored 1: Fault 3 input is active and disables SHRTIM outputs
[1]	FALT2EN	FAULT 2 enable 0: Fault 2 input is ignored 1: Fault 2 input is active and disables SHRTIM outputs
[0]	FALT1EN	FAULT 1 enable 0: Fault 1 input is ignored 1: Fault 1 input is active and disables SHRTIM outputs

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17.3.56 SHRTIM Timer x Control Register 2 (SHRTIM_TxCTRL2)

Address offset: 0x0EC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											TRGHLF	Reserved		GTCMP3	GTCMP1
											rw			rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEROM		BMROM		ADCROM		OUTROM		ROM		Reserved	UPDOWNM	Reserved	DUDACRST	DUDACSTEP	DUDACEN
rw		rw		rw		rw		rw			rw		rw	rw	rw

Bit Field	Name	Description
[31:21]	Reserved	Reserved, the reset value must be maintained
[20]	TRGHLF	Triggered-half mode This bitfield defines whether the compare 2 register is behaving in standard mode (compare match issued as soon as counter equal compare), or in triggered-half mode (refer to Section). 0: The SHRTIM_TxCMP2DAT register value is written by the user only (standard compare mode) 1: The SHRTIM_TxCMP2DAT register value is set by hardware as soon as a capture 1 event occurs. It is loaded with the (capture 1 divided by 2) value. The initial value can be written by the user (as long as TRGHLF is reset), but is ignored once the first capture has been triggered (the preload mechanism is disabled for SHRTIM_TxCMP2DAT when the TRGHLF bit is set). Note: This bitfield must not be modified once the counter is enabled (*SHRTIM_MCTRL.TxCNTEN* bit set).
[19:18]	Reserved	Reserved, the reset value must be maintained
[17]	GTCMP3	Greater than compare 3 PWM mode This bit defines the compare 3 operating mode. 0: The compare 3 event is generated when the counter is equal to the compare value (compare match mode) 1: The compare 3 event is generated when the counter is greater than the compare value. If the compare value is changed on-the-fly, the new compare value is compared with the current counter value and an output SET or RESET can be generated.
[16]	GTCMP1	Greater than compare 1 PWM mode 0: The compare 1 event is generated when the counter is equal to the compare value (compare match mode) 1: The compare 1 event is generated when the counter is greater than the compare value. If the compare value is changed on-the-fly, the new compare value is compared with the current counter value and an output SET or RESET

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		can be generated.
[15:14]	FEROM	Fault and event roll-over mode This bit defines when the roll-over is generated in up-down counting mode. It only relates to the rollover event used by the fault and event counters. 00: An event is generated when the counter is equal to 0 or to SHRTIM_TxPRD value 01: An event is generated when the counter is equal to 0 10: An event is generated when the counter is equal to SHRTIM_TxPRD 11: Reserved *Note: This setting only applies when the SHRTIM_TxCTRL2.UPDOWNM bit is set. It is not significant otherwise.* *Note: This bitfield cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set).*
[13:12]	BMROM	Burst mode roll-over mode This bit defines when the roll-over is generated in up-down counting mode. It only relates to the rollover event used in the burst mode controller, as burst mode trigger clock. 00: An event is generated when the counter is equal to 0 or to SHRTIM_TxPRD value 01: An event is generated when the counter is equal to 0 10: An event is generated when the counter is equal to SHRTIM_TxPRD 11: Reserved *Note: This setting only applies when the SHRTIM_TxCTRL2.UPDOWNM bit is set. It is not significant otherwise.* *Note: This bitfield cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set).*
[11:10]	ADCROM	ADC roll-over mode This bit defines when the roll-over is generated in up-down counting mode. It only relates to the rollover event which is used for ADC trigger. 00: An event is generated when the counter is equal to 0 or to SHRTIM_TxPRD value 01: An event is generated when the counter is equal to 0 10: An event is generated when the counter is equal to SHRTIM_TxPRD 11: Reserved *Note: This setting only applies when the SHRTIM_TxCTRL2.UPDOWNM bit is set. It is not significant otherwise.* *Note: This bitfield cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set).*
[9:8]	OUTROM	Output roll-over mode This bit defines when the roll-over is generated in up-down counting mode. It only relates to the rollover event which sets and/or resets the ouputs, as per SHRTIM_TxSETy and SHRTIM_TxRSTy settings. 00: An event is generated when the counter is equal to 0 or to SHRTIM_TxPRD

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		value 01: An event is generated when the counter is equal to 0 10: An event is generated when the counter is equal to SHRTIM_TxPRD 11: Reserved *Note: This setting only applies when the SHRTIM_TxCTRL2.UPDOWNM bit is set. It is not significant otherwise.* *Note: This bitfield cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set)*
[7:6]	ROM	Roll-over mode This bit defines when the roll-over is generated in up-down counting mode. It only relates to the rollover event with the following destinations: update trigger (transfer content from preload to active registers), IRQ and DMA requests, repetition counter decrement and external event filtering. 00: An event is generated when the counter is equal to 0 or to SHRTIM_TxPRD value 01: An event is generated when the counter is equal to 0 10: An event is generated when the counter is equal to SHRTIM_TxPRD 11: Reserved *Note: This setting only applies when the SHRTIM_TxCTRL2.UPDOWNM bit is set. It is not significant otherwise.* *Note: This bitfield cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set)*
[5]	Reserved	Reserved, the reset value must be maintained
[4]	UPDOWNM	Up-down mode This bit defines whether the counter operates in up counting mode or up-down counting mode. 0: The counter operates in up counting mode 1: The counter operates in up-down counting mode *Note: This bit cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set).*
[3]	Reserved	Reserved, the reset value must be maintained
[2]	DUDACRST	Dual DAC reset trigger This bit defines when the shrtim_dac_reset_trgx trigger is generated. 0: The trigger is generated on counter reset or roll-over events 1: The trigger is generated on output 1 set events *Note: The DUDACRST bit is not significant when the DUDACEN bit is reset (dual DAC trigger disabled).*
[1]	DUDACSTEP	Dual DAC step trigger This bit defines when the shrtim_dac_step_trgx trigger is generated. 0: The trigger is generated on compare 2 events 1: The trigger is generated on output 1 reset events *Note: The DUDACSTEP bit is not significant when the DUDACEN bit is reset (dual DAC trigger disabled).*

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[0]	DUDACEN	Dual channel DAC trigger enable This bit enables the dual DAC trigger mechanism. 0: Disables the dual DAC trigger 1: Enables the dual DAC trigger *Note: This bit cannot be changed once the timer is operating (SHRTIM_MCTRL.TxCNTEN bit set).*

17.3.57 SHRTIM Timer x External Event Filtering Register 3 (SHRTIM_TxEXEVFLT3)

Address offset: 0x0F0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		EXEVCNT						EXEVSEL				Reserved	EXEVRSTM	EXEVCNTRST	EXEVCNTEN
		rw						rw					rw	rt_w	rw

Bit Field	Name	Description
[31:14]	Reserved	Reserved, the reset value must be maintained
[13:8]	EXEVCNT	Channel x (x = A~F)'s external event counter This bitfield selects the channel x (x = A~F)'s external event counter threshold. An event is taken into account valid when the number of events is equal to the (EXEVCNT[5:0]+1) value.
[7:4]	EXEVSEL	Channel x (x = A~F)'s s external event selection This bitfield selects the channel x (x = A~F)'s external event source 0000: The external event 1 is used as the channel x (x = A~F)'s external event source 0001: The external event 2 is used as the channel x (x = A~F)'s external event source ... 1001: The external event 10 is used as the channel x (x = A~F)'s external event source Others: Reserved
[3]	Reserved	Reserved, the reset value must be maintained
[2]	EXEVRSTM	Channel x (x = A~F)'s external event reset mode This bitfield selects the channel x (x = A~F)'s external event counter reset mode. 0: The channel x (x = A~F)'s external event counter is reset on each

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		reset/roll-over event 1: The channel x (x = A~F)'s external event counter is reset on each reset/roll-over event only if no event occurs during last counting period
[1]	EXEVCNTRST	Channel x (x = A~F)'s external event counter reset This bit resets the channel x (x = A~F)'s external event counter. It is set by software and reset by hardware. 0: No action 1: The channel x (x = A~F)'s external event counter is reset
[0]	EXEVCNTEN	Channel x (x = A~F)'s external event counter enable This bit enables the channel x (x = A~F)'s external event counter. 0: The channel x (x = A~F)'s external event counter disabled 1: The channel x (x = A~F)'s external event counter enabled

17.3.58 SHRTIM Timer x Compare 5 Register (SHRTIM_TxCMP5DAT)

Address offset: 0x0F4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP5DAT															
rw															

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15:0]	CMP5DAT	Timer x compare 5 data 1. The Compare unit 5 is dedicated to trigger ADC and does not have the same functions as CMP1 to CMP4. It only supports the following features: 2. CMP5 has regular resolution and does not has high-resolution characteristics. 3. When the counter matches CMP5 value, it will generate the CMP5 status flag, which can also be cleared. However, CMP5 events do not connect to NVIC, so they do not generate interrupts. 4. CMP5 events can be used to trigger the ADC.

17.3.59 SHRTIM Control Register 1 (SHRTIM_CTRL1)

Address offset: 0x380

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				ADTG4UPDSRC			ADTG3UPDSRC			ADTG2UPDSRC			ADTG1UPDSRC		
				rw			rw			rw			rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									TFUPDDIS	TEUPDDIS	TDUPDDIS	TCUPDDIS	TBUPDDIS	TAUPDDIS	MUPDDIS
									rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31:28]	Reserved	Reserved, the reset value must be maintained
[27:25]	ADTG4UPDSRC	ADC trigger 4 update source Refer to the ADTG1UPDSRC[2:0] description
[24:22]	ADTG3UPDSRC	ADC trigger 3 update source Refer to the ADTG1UPDSRC[2:0] description
[21:19]	ADTG2UPDSRC	ADC trigger 2 update source Refer to the ADTG1UPDSRC[2:0] description
[18:16]	ADTG1UPDSRC	ADC trigger 1 update source These bits define the source which triggers the update of the SHRTIM_ADTG1SRC1 and SHRTIM_ADTG1SRC2 register (transfer from preload to active register). It only defines the source timer. The precise condition is defined within the timer itself, in SHRTIM_MCTRL or SHRTIM_TxCTRL. 000: Master timer 001: Timer A 010: Timer B 011: Timer C 100: Timer D 101: Timer E 110: Timer F 111: Reserved
[15:7]	Reserved	Reserved, the reset value must be maintained
[6]	TFUPDDIS	TIM F update disable Refer to the TAUPDDIS description
[5]	TEUPDDIS	TIM E update disable Refer to the TAUPDDIS description
[4]	TDUPDDIS	TIM D update disable Refer to the TAUPDDIS description
[3]	TCUPDDIS	TIM C update disable Refer to the TAUPDDIS description
[2]	TBUPDDIS	TIM B update disable Refer to the TAUPDDIS description
[1]	TAUPDDIS	TIM A update disable This bit is set and cleared by software to enable/disable an update event

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		generation temporarily on timer A. 0: Update enabled. The update occurs upon generation of the selected source. 1: Update disabled. The updates are temporarily disabled to allow the software to write multiple registers that have to be simultaneously taken into account.
[0]	MUPDDIS	Master timer update disable This bit is set and cleared by software to enable/disable an update event generation temporarily on master timer. 0: Update enabled. 1: Update disabled. The updates are temporarily disabled to allow the software to write multiple registers that have to be simultaneously taken into account.

17.3.60 SHRTIM Control Register 2 (SHRTIM_CTRL2)

Address offset: 0x384

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										SWAPF	SWAPE	SWAPD	SWAPC	SWAPB	SWAPA
										rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TFSWCNTRST	TESWCNTRST	TDSWCNTRST	TCSWCNTRST	TBSWCNTRST	TASWCNTRST	MSWCNTRST	Reserved	TFSWUPD	TESWUPD	TDSWUPD	TCSWUPD	TBSWUPD	TASWUPD	MSWUPD
	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w

Bit Field	Name	Description
[31:22]	Reserved	Reserved, the reset value must be maintained
[21]	SWAPF	TIMF output swap Refer to the SWAPA description *Note: This bit is not significant when push-pull mode is enabled (PP = 1).*
[20]	SWAPE	TIME output swap Refer to the SWAPA description *Note: This bit is not significant when push-pull mode is enabled (PP = 1).*
[19]	SWAPD	TIMD output swap Refer to the SWAPA description *Note: This bit is not significant when push-pull mode is enabled (PP = 1).*
[18]	SWAPC	TIMC output swap Refer to the SWAPA description *Note: This bit is not significant when push-pull mode is enabled (PP = 1).*
[17]	SWAPB	TIMB output swap Refer to the SWAPA description

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		Note: This bit is not significant when push-pull mode is enabled (PP = 1).
[16]	SWAPA	TIMA output swap This bit allows to swap the timer A outputs. 0: SHRTIM_TARST1 and SHRTIM_TASET1 are coding for the output A1, SHRTIM_TARST2 and SHRTIM_TASET2 are coding for the output A2. 1: SHRTIM_TARST1 and SHRTIM_TASET1 are coding for the output A2, SHRTIM_TARST2 and SHRTIM_TASET2 are coding for the output A1. *Note: This bit is not significant when push-pull mode is enabled (PP = 1).*
[15]	Reserved	Reserved, the reset value must be maintained
[14]	TFSWCNTRST	TIMF's software counter reset Refer to the TASWCNTRST description
[13]	TESWCNTRST	TIME's software counter reset Refer to the TASWCNTRST description
[12]	TDSWCNTRST	TIMD's software counter reset Refer to the TASWCNTRST description
[11]	TCSWCNTRST	TIMC's software counter reset Refer to the TASWCNTRST description
[10]	TBSWCNTRST	TIMB's software counter reset Refer to the TASWCNTRST description
[9]	TASWCNTRST	TIMA's software counter reset Setting this bit resets the timer A counter. 0: No action 1: Timer A is reset by software The bit is automatically clear by hardware.
[8]	MSWCNTRST	Master timer's software counter reset Setting this bit resets the master timer counter. 0: No action 1: Master timer is reset by software The bit is automatically clear by hardware.
[7]	Reserved	Reserved, the reset value must be maintained
[6]	TFSWUPD	TIMF software update） Refer to the TASWUPD description
[5]	TESWUPD	TIME software update） Refer to the TASWUPD description
[4]	TDSWUPD	TIMD software update） Refer to the TASWUPD description
[3]	TCSWUPD	TIMC software update Refer to the TASWUPD description
[2]	TBSWUPD	TIMB software update Refer to the TASWUPD description
[1]	TASWUPD	Timer A Software Update This bit is set by software and automatically reset by hardware. It forces an

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		immediate transfer from the preload to the active register and any pending update request is canceled.
[0]	MSWUPD	Master Timer Software update This bit is set by software and automatically reset by hardware. It forces an immediate transfer from the preload to the active register in the master timer and any pending update request is canceled.

17.3.61 SHRTIM Interrupt Status Register (SHRTIM_INTSTS)

Address offset: 0x388

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														BMPRDITF	Reserved
														r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									FALT6ITF	SYSFALTITF	FALT5ITF	FALT4ITF	FALT3ITF	FALT2ITF	FALT1ITF
									r	r	r	r	r	r	r

Bit Field	Name	Description
[31:18]	Reserved	Reserved, the reset value must be maintained
[17]	BMPRDITF	Burst mode Period Interrupt Flag This bit is set by hardware when a single-shot burst mode operation is completed, or at the end of a burst mode period in continuous mode. It is cleared by software writing it at 1. 0: No burst mode period interrupt occurred 1: Burst mode period interrupt occurred
[16]	Reserved	Reserved, the reset value must be maintained
[15:7]	Reserved	Reserved, the reset value must be maintained
[6]	FALT6ITF	Fault 6 interrupt flag Refer to the FALT1ITF description
[5]	SYSFALTITF	System Fault Interrupt Flag Refer to the FALT1ITF description
[4]	FALT5ITF	Fault 5 interrupt flag Refer to the FALT1ITF description
[3]	FALT4ITF	Fault 4 interrupt flag Refer to the FALT1ITF description
[2]	FALT3ITF	Fault 3 interrupt flag Refer to the FALT1ITF description
[1]	FALT2ITF	Fault 2 interrupt flag Refer to the FALT1ITF description
[0]	FALT1ITF	Fault 1 Interrupt Flag

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		This bit is set by hardware when fault 1 event occurs. It is cleared by software writing it at 1. 0: No fault 1 interrupt occurred 1: Fault 1 interrupt occurred

17.3.62 SHRTIM Interrupt Clear Register (SHRTIM_INTCLR)

Address offset: 0x38C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														BMPRDIC	Reserved
														w	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									FALT6IC	SYSFALTIC	FALT5IC	FALT4IC	FALT3IC	FALT2IC	FALT1IC
									w	w	w	w	w	w	w

Bit Field	Name	Description
[31:18]	Reserved	Reserved, the reset value must be maintained
[17]	BMPRDIC	Burst mode period flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.BMPRDITF.
[16]	Reserved	Reserved, the reset value must be maintained
[15:7]	Reserved	Reserved, the reset value must be maintained
[6]	FALT6IC	Fault 6 interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.FALT6ITF
[5]	SYSFALTIC	System fault interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS. SYSFALTITF
[4]	FALT5IC	Fault 5 interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.FALT5ITF
[3]	FALT4IC	Fault 4 interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.FALT4ITF
[2]	FALT3IC	Fault 3 interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.FALT3ITF
[1]	FALT2IC	Fault 2 interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.FALT2ITF
[0]	FALT1IC	Fault 1 interrupt flag clear Writing a 1 to this bit will clear the SHRTIM_INTSTS.FALT1ITF

17.3.63 SHRTIM Interrupt Enable Register (SHRTIM_INTEN)

Address offset: 0x390

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														BMPRDIEN	Reserved
														rw	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									FALT6IEN	SYSFALTIEN	FALT5IEN	FALT4IEN	FALT3IEN	FALT2IEN	FALT1IEN
									rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31:18]	Reserved	Reserved, the reset value must be maintained
[17]	BMPRDIEN	Burst mode period interrupt enable This bit is set and cleared by software to enable/disable the burst mode period interrupt. 0: Disable burst mode period interrupt 1: Enable burst mode period interrupt
[16]	Reserved	Reserved, the reset value must be maintained
[15:7]	Reserved	Reserved, the reset value must be maintained
[6]	FALT6IEN	Fault 6 interrupt enable This bit is set and cleared by software to enable/disable the fault 6 interrupt. 0: Disable fault 6 interrupt 1: Enable fault 6 interrupt
[5]	SYSFALTIEN	System fault interrupt enable This bit is set and cleared by software to enable/disable the system fault interrupt. 0: Disable system fault interrupt 1: Enable system fault interrupt
[4]	FALT5IEN	Fault 5 interrupt enable This bit is set and cleared by software to enable/disable the fault 5 interrupt. 0: Disable fault 5 interrupt 1: Enable fault 5 interrupt
[3]	FALT4IEN	Fault 4 interrupt enable This bit is set and cleared by software to enable/disable the fault 4 interrupt. 0: Disable fault 4 interrupt 1: Enable fault 4 interrupt
[2]	FALT3IEN	Fault 3 interrupt enable This bit is set and cleared by software to enable/disable the fault 3 interrupt. 0: Disable fault 3 interrupt 1: Enable fault 3 interrupt
[1]	FALT2IEN	Fault 2 interrupt enable

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		This bit is set and cleared by software to enable/disable the fault 2 interrupt. 0: Disable fault 2 interrupt 1: Enable fault 2 interrupt
[0]	FALT1IEN	Fault 1 interrupt enable This bit is set and cleared by software to enable/disable the fault 1 interrupt. 0: Disable fault 1 interrupt 1: Enable fault 1 interrupt

17.3.64 SHRTIM Output Enable Register (SHRTIM_OEN)

Address offset: 0x394

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TF2OEN	TF1OEN	TE2OEN	TE1OEN	TD2OEN	TD1OEN	TC2OEN	TC1OEN	TB2OEN	TB1OEN	TA2OEN	TA1OEN
				rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w

Bit Field	Name	Description
[31:12]	Reserved	Reserved, the reset value must be maintained
[11]	TF2OEN	Timer F output 2 enable Refer to the TA1OEN description
[10]	TF1OEN	Timer F output 1 enable Refer to the TA1OEN description
[9]	TE2OEN	Timer E output 1 enable Refer to the TA1OEN description
[8]	TE1OEN	Timer E output 1 enable Refer to the TA1OEN description
[7]	TD2OEN	Timer D output 2 enable Refer to the TA1OEN description
[6]	TD1OEN	Timer D output 1 enable Refer to the TA1OEN description
[5]	TC2OEN	Timer C output 2 enable Refer to the TA1OEN description
[4]	TC1OEN	Timer C output 1 enable Refer to the TA1OEN description
[3]	TB2OEN	Timer B output 2 enable Refer to the TA1OEN description

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[2]	TB1OEN	Timer B output 1 enable Refer to the TA1OEN description
[1]	TA2OEN	Timer A output 2 enable Refer to the TA1OEN description
[0]	TA1OEN	Timer A output 1 enable Setting this bit to 1 will enable timer A output 1. Writing "0" has no effect. Reading this bit will return the output enable/disable status. This bit is asynchronously cleared by hardware immediately when the timer-related fault input/inputs is/are active. 0: SHRTIM_CHA1 output is disabled. The output is either in a fault or idle state. 1: SHRTIM_CHA1 output is enabled. *Note: The disabled state corresponds to both idle and fault states. The output disable state is provided by SHRTIM_ODISSTS.TA1ODISSTS.*

17.3.65 SHRTIM Output Disable Register (SHRTIM_ODIS)

Address offset: 0x398

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TF2ODIS	TF1ODIS	TE2ODIS	TE1ODIS	TD2ODIS	TD1ODIS	TC2ODIS	TC1ODIS	TB2ODIS	TB1ODIS	TA2ODIS	TA1ODIS
				w	w	w	w	w	w	w	w	w	w	w	w

Bit Field	Name	Description
[31:12]	Reserved	Reserved, the reset value must be maintained
[11]	TF2ODIS	TIMF output 2 disable Refer to the TA1ODIS description.
[10]	TF1ODIS	TIMF output 1 disable Refer to the TA1ODIS description.
[9]	TE2ODIS	TIME output 2 disable Refer to the TA1ODIS description.
[8]	TE1ODIS	TIME output 1 disable Refer to the TA1ODIS description.
[7]	TD2ODIS	TIMD output 2 disable Refer to the TA1ODIS description.
[6]	TD1ODIS	TIMD output 1 disable Refer to the TA1ODIS description.
[5]	TC2ODIS	TIMC output 2 disable

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		Refer to the TA1ODIS description.
[4]	TC1ODIS	TIMC output 1 disable Refer to the TA1ODIS description.
[3]	TB2ODIS	TIMB output 2 disable Refer to the TA1ODIS description.
[2]	TB1ODIS	TIMB output 1 disable Refer to the TA1ODIS description.
[1]	TA2ODIS	TIMA output 2 disable Refer to the TA1ODIS description.
[0]	TA1ODIS	TIMA output 1 disable Setting this bit to 1 will disable timer A output 1. The output will transition from the running or fault state to the idle state. Writing "0" has no effect.

17.3.66 SHRTIM Output Disable Status Register (SHRTIM_ODISSTS)

Address offset: 0x39C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TF2ODISSTS	TF1ODISSTS	TE2ODISSTS	TE1ODISSTS	TD2ODISSTS	TD1ODISSTS	TC2ODISSTS	TC1ODISSTS	TB2ODISSTS	TB1ODISSTS	TA2ODISSTS	TA1ODISSTS
				r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
[31:12]	Reserved	Reserved, the reset value must be maintained
[11]	TF2ODISSTS	TIMF output 2 disable status Refer to the TA1ODISSTS description.
[10]	TF1ODISSTS	TIMF output 1 disable status Refer to the TA1ODISSTS description.
[9]	TE2ODISSTS	TIME output 2 disable status Refer to the TA1ODISSTS description.
[8]	TE1ODISSTS	TIME output 1 disable status Refer to the TA1ODISSTS description.
[7]	TD2ODISSTS	TIMD output 2 disable status Refer to the TA1ODISSTS description.
[6]	TD1ODISSTS	TIMD output 1 disable status Refer to the TA1ODISSTS description.
[5]	TC2ODISSTS	TIMC output 2 disable status Refer to the TA1ODISSTS description.
[4]	TC1ODISSTS	TIMC output 1 disable status

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		Refer to the TA1ODISSTS description.
[3]	TB2ODISSTS	TIMB output 2 disable status Refer to the TA1ODISSTS description.
[2]	TB1ODISSTS	TIMB output 1 disable status Refer to the TA1ODISSTS description.
[1]	TA2ODISSTS	TIMA output 2 disable status Refer to the TA1ODISSTS description.
[0]	TA1ODISSTS	TIMA output 1 disable status Reading this bit will return the output disable state. This bit is not significant when the output is active (Tx1OEN or Tx2OEN = 1). 0: SHRTIM_CHA1 output is disabled, in idle state. 1: SHRTIM_CHA1 output is disabled, in fault state.

17.3.67 SHRTIM Burst Mode Control Register (SHRTIM_BMCTRL)

Address offset: 0x3A0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BMSTS	Reserved								TFBM	TEBM	TDBM	TCBM	TBBM	TABM	MBM
rc_w0									rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					BMPLEN	BMPSC				BMCK				BMOM	BMEN
					rw	rw				rw				rw	rw

Bit Field	Name	Description
[31]	BMSTS	Burst Mode Status This bit gives the current operating state 0: Normal operation 1: Burst operation on-going. Writing this bit to 0 causes a burst mode early termination.
[30:23]	Reserved	Reserved, the reset value must be maintained
[22]	TFBM	TIM F burst mode Refer to the TABM description.
[21]	TEBM	TIM E burst mode Refer to the TABM description.
[20]	TDBM	TIM D burst mode Refer to the TABM description.
[19]	TCBM	TIM C burst mode Refer to the TABM description.
[18]	TBBM	TIM B burst mode Refer to the TABM description.

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[17]	TABM	TIM A burst mode This bit defines the behavior of the timer during burst mode operation. This bit field cannot be changed once the burst mode is enabled. 0: Timer A counter clock is maintained, timer operates normally 1: Timer A counter clock is stopped, counter is reset *Note: This bit must not be set when the balanced idle mode is active (DP[2:0] = 0x11).*
[16]	MBM	Master timer Burst Mode This bit defines the behavior of the timer during burst mode operation. This bit field cannot be changed once the burst mode is enabled. 0: Master timer counter clock is maintained, timer operates normally 1: Master timer counter clock is stopped, counter is reset
[15:11]	Reserved	Reserved, the reset value must be maintained
[10]	BMPLEN	Burst mode Preload Enable This bit enables the register preload mechanism and defines whether write accesses to the preloadable registers (SHRTIM_BMCMP, SHRTIM_BMPRD) are done in the active registers or in the preload registers. 0: Disable preload: the write access is directly done into active registers 1: Enable preload: the write access is done into preload registers
[9:6]	BMPSC	Burst mode prescaler This bit field defines the prescaler ratio for the f_{SHRTIM} clock of the burst mode controller. It cannot be changed when burst mode is enabled. 0000: Clock not divided 0001: Division by 2 0010: Division by 3 0011: Division by 4 0100: Division by 5 0101: Division by 6 0110: Division by 7 0111: Division by 8 1000: Division by 9 1001: Division by 10 1010: Division by 11 1011: Division by 12 1100: Division by 13 1101: Division by 14 1110: Division by 15 1111: Division by 16
[5:2]	BMCK	Burst Mode Clock source) This bit field defines the clock source for the burst mode counter. It cannot be changed when burst mode is enabled (for detailed information on the on-chip events 1 to 4 connections, please refer to). 0000: Master timer counter reset/roll-over

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		0001 : Timer A counter reset/roll-over 0010 : Timer B counter reset/roll-over 0011 : Timer C counter reset/roll-over 0100 : Timer D counter reset/roll-over 0101 : Timer E counter reset/roll-over 0110: On-chip event 1 (shrtim_bm_ck1) serves as the clock for the burst mode counter. 0111: On-chip event 1 (shrtim_bm_ck2) serves as the clock for the burst mode counter. 1000: On-chip event 1 (shrtim_bm_ck3) serves as the clock for the burst mode counter. 1001: On-chip event 1 (shrtim_bm_ck4) serves as the clock for the burst mode counter. 1010: Prescaled f_{SHRTIM} clock (as per BMPSC[3:0] setting) Others: Reserved
[1]	BMOM	Burst Mode operating mode This bit defines whether to enter single-shot burst mode or continuous operation. 0: Single-shot mode 1: Continuous operation
[0]	BMEN	Burst Mode enable This bit is used to start the burst mode controller which is ready to receive the start trigger signal. Writing a 0 to this bit will cause a burst mode early termination. 0: Disable burst mode 1: Enable burst mode

17.3.68 SHRTIM Burst Mode Trigger Register (SHRTIM_BMTG)

Address offset: 0x3A4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OCEV	EXEV8	EXEV7	TDPRDEXEV8	TAPRDEXEV7	TECMP2	TECMP1	TEREPT	TFCMP1	TDCMP2	TFREPT	TDREPT	TDRSTRO	TFRSTRO	TCCMP1	TCREPT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCRSTRO	TBCMP2	TBCMP1	TBREPT	TBRSTRO	TACMP2	TACMP1	TAREPT	TARSTRO	MCMP4	MCMP3	MCMP2	MCMP1	MREPT	MRSTRO	SWSTRT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rt_w

Bit Field	Name	Description
[31]	OCEV	On-chip event A rising edge on the shrtim_bm_trg input triggers a burst mode entry (refer to).

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[30]	EXEV8	External event 8 (TIMD filters applied) The external event 8 conditioned by TIMD filters is starting the burst mode operation.
[29]	EXEV7	External event 7 (TIMA filters applied) The external event 7 conditioned by TIMA filters is starting the burst mode operation
[28]	TDPRDEXEV8	Timer D period following external event 8 The timer D period following an external event 8 (conditioned by TIMD filters) is starting the burst mode operation.
[27]	TAPRDEXEV7	Timer A period following external event 7 The timer A period following an external event 7 (conditioned by TIMA filters) is starting the burst mode operation.
[26]	TECMP2	Timer E compare 2 event Refer to the TACMP2 description.
[25]	TECMP1	Timer E compare 1 event Refer to the TACMP1 description.
[24]	TEREPT	Timer E repetition event Refer to the TAREPT description.
[23]	TFCMP1	Timer F compare 1event Refer to the TACMP1 description.
[22]	TDCMP2	Timer E Compare 2 event Refer to the TACMP2 description.
[21]	TFREPT	Timer F repetition event Refer to the TAREPT description.
[20]	TDREPT	Timer D repetition event Refer to the TAREPT description.
[19]	TDRSTRO	Timer D reset/roll-over event Refer to the TARSTRO description.
[18]	TFRSTRO	Timer F reset/roll-over event Refer to the TARSTRO description.
[17]	TCCMP1	Timer C compare 1 event Refer to the TACMP1 description.
[16]	TCREPT	Timer C repetition event Refer to the TAREPT description.
[15]	TCRSTRO	Timer C reset/roll-over event Refer to the TARSTRO description.
[14]	TBCMP2	Timer B compare 2 event Refer to the TACMP2 description.
[13]	TBCMP1	Timer B compare 1 event Refer to the TACMP1 description.
[12]	TBREPT	Timer B repetition event Refer to the TAREPT description.

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[11]	TBRSTRO	Timer B reset/roll-over event Refer to the TARSTRO description.
[10]	TACMP2	Timer A compare 2 event Refer to the TACMP1 description.
[9]	TACMP1	Timer A Compare 1 event Timer A compare 1 event will start burst mode operation.
[8]	TAREPT	Timer A repetition Timer A repetition event will start burst mode operation.
[7]	TARSTRO	Timer A counter reset or roll-over Timer A reset or roll-over event will start burst mode operation.
[6]	MCMP4	Master timer compare 4 Refer to the MCMP1 description.
[5]	MCMP3	Master timer compare 3 Refer to the MCMP1 description.
[4]	MCMP2	Master timer compare 2 Refer to the MCMP1 description.
[3]	MCMP1	Master timer compare 1 Master timer compare 1 event will start burst mode operation.
[2]	MREPT	Master timer repetition Master timer repetition event will start burst mode operation.
[1]	MRSTRO	Master timer reset/roll-over Master timer reset or roll-over event will start burst mode operation.
[0]	SWSTRT	Software start This bit is set by software and automatically reset by hardware. If this bit is set to 1, it starts the burst mode operation immediately. This bit is not active if the burst mode is not enabled (BMEM bit is reset).

17.3.69 SHRTIM Burst Mode Compare Register (SHRTIM_BMCMP)

Address offset: 0x3A8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BMCMP															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMCMP															
rw															

Bit Field	Name	Description
[31:0]	BMCMP	Burst Mode compare value This register defines the number of periods during which the selected timers

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		are in idle state. The register holds the contents of the preload register, or if preload is disabled, it holds the contents of the active register. *Note: The duration of IDLE and RUN in Burst mode must be greater than the duration of one PWM output period.*

17.3.70 SHRTIM Burst Mode Period Register (SHRTIM_BMPRD)

Address offset: 0x3AC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BMPRD															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMPRD															
rw															

Bit Field	Name	Description
[31:0]	BMPRD	Burst Mode Period This register defines the burst mode repetition period The register holds the contents of the preload register, or if preload is disabled, it holds the contents of the active register. *Note: The duration of IDLE and RUN in Burst mode must be greater than the duration of one PWM output period.*

17.3.71 SHRTIM External Event Control Register 1 (SHRTIM_EXEVCTRL1)

Address offset: 0x3B0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		EXEV5SENS		EXEV5POL	EXEV5SRC			EXEV4SENS		EXEV4POL	EXEV4SRC			EXEV3SENS	
		rw		rw	rw			rw		rw	rw			rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV3POL	EXEV3SRC			EXEV2SENS		EXEV2POL	EXEV2SRC			EXEV1SENS		EXEV1POL	EXEV1SRC		
rw	rw			rw		rw	rw			rw		rw	rw		

Bit Field	Name	Description
[31:30]	Reserved	Reserved, the reset value must be maintained
[29:28]	EXEV5SENS	External event 5 sensitivity Refer to the EXEV1SENS description.

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[27]	EXEV5POL	External event 5 polarity Refer to the EXEV1POL description.
[26:24]	EXEV5SRC	External event 5 source Refer to the EXEV1SRC description.
[23:22]	EXEV4SENS	External event 4 sensitivity Refer to the EXEV1SENS description.
[21]	EXEV4POL	External event 4 polarity Refer to the EXEV1POL description.
[20:18]	EXEV4SRC	External event 4 source Refer to the EXEV1SRC description.
[17:16]	EXEV3SENS	External event 3 sensitivity Refer to the EXEV1SENS description.
[15]	EXEV3POL	External event 3 polarity Refer to the EXEV1POL description.
[14:12]	EXEV3SRC	External event 3 source Refer to the EXEV1SRC description.
[11:10]	EXEV2SENS	External event 2 sensitivity Refer to the EXEV1SENS description.
[9]	EXEV2POL	External event 2 polarity Refer to the EXEV1POL description.
[8:6]	EXEV2SRC	External event 2 source Refer to the EXEV1SRC description.
[5:4]	EXEV1SENS	External event 1 sensitivity 00: On active level defined by EXEV1POL bit 01: Rising edge, whatever EXEV1POL bit value 10: Falling edge, whatever EXEV1POL bit value 11: Both edges, whatever EXEV1POL bit value
[3]	EXEV1POL	External event 1 polarity This bit is only significant if EXEV1SENS[1:0] = 00. 0: External event is active high 1: External event is active low *Note: This parameter cannot be changed once the timer x is enabled. It must be configured prior to setting EXEV1FM bit.*
[2:0]	EXEV1SRC	External event 4 source This bitfield selects the external event 1 source. 000: shrtim_exev1_1 001: shrtim_exev1_2 010: shrtim_exev1_3 011: shrtim_exev1_4 100: shrtim_exev1_5 101~111:Reserved *Note: This parameter cannot be changed once the timer x is enabled. It must*

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		be configured prior to setting EXEV1FM bit.

17.3.72 SHRTIM External Event Control Register 2 (SHRTIM_EXEVCTRL2)

Address offset: 0x3B4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		EXEV10SENS		EXEV10POL	EXEV10SRC			EXEV9SENS		EXEV9POL	EXEV9SRC			EXEV8SENS	
		rw		rw	rw			rw		rw	rw			rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV8POL	EXEV8SRC			EXEV7SENS		EXEV7POL	EXEV7SRC			EXEV6SENS		EXEV6POL	EXEV6SRC		
rw	rw			rw		rw	rw			rw		rw	rw		

Bit Field	Name	Description
[31:30]	Reserved	Reserved, the reset value must be maintained
[29:28]	EXEV10SENS	External event 10 sensitivity Refer to the EXEV1SENS description.
[27]	EXEV10POL	External event 10 polarity Refer to the EXEV1POL description.
[26:24]	EXEV10SRC	External event 10 source Refer to the EXEV1SRC description.
[23:22]	EXEV9SENS	External event 9 sensitivity Refer to the EXEV1SENS description.
[21]	EXEV9POL	External event 9 polarity Refer to the EXEV1POL description.
[20:18]	EXEV9SRC	External event 9 source Refer to the EXEV1SRC description.
[17:16]	EXEV8SENS	External event 8 sensitivity Refer to the EXEV1SENS description.
[15]	EXEV8POL	External event 8 polarity Refer to the EXEV1POL description.
[14:12]	EXEV8SRC	External event 8 source Refer to the EXEV1SRC description.
[11:10]	EXEV7SENS	External event 7 sensitivity Refer to the EXEV1SENS description.
[9]	EXEV7POL	External event 7 polarity Refer to the EXEV1POL description.
[8:6]	EXEV7SRC	External event 7 source Refer to the EXEV1SRC description.
[5:4]	EXEV6SENS	External event 6 sensitivity Refer to the EXEV1SENS description.

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[3]	EXEV6POL	External event 6 polarity Refer to the EXEV1POL description.
[2:0]	EXEV6SRC	External event 6 source Refer to the EXEV1SRC description.

17.3.73 SHRTIM External Event Control Register 3 (SHRTIM_EXEVCTRL3)

Address offset: 0x3B8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			EXEV5FM	EXEV5FLT				Reserved	EXEV4FM	EXEV4FLT				Reserved	EXEV3FM
			rw	rw					rw	rw					rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV3FLT				Reserved	EXEV2FM	EXEV2FLT				Reserved	EXEV1FM	EXEV1FLT			
rw				rw		rw				rw		rw			

Bit Field	Name	Description
[31:29]	Reserved	Reserved, the reset value must be maintained
[28]	EXEV5FM	External event 5 fast mode Refer to the EXEV1FM description.
[27:24]	EXEV5FLT	External event 5 filter Refer to the EXEV1FLT description.
[23]	Reserved	Reserved, the reset value must be maintained
[22]	EXEV4FM	External event 4 fast mode Refer to the EXEV1FM description.
[21:18]	EXEV4FLT	External event 4 filter Refer to the EXEV1FLT description.
[17]	Reserved	Reserved, the reset value must be maintained
[16]	EXEV3FM	External event 3 fast mode Refer to the EXEV1FM description.
[15:12]	EXEV3FLT	External event 3 filter Refer to the EXEV1FLT description.
[11]	Reserved	Reserved, the reset value must be maintained
[10]	EXEV2FM	External event 2 fast mode Refer to the EXEV1FM description.
[9:6]	EXEV2FLT	External event 2 filter Refer to the EXEV1FLT description.
[5]	Reserved	Reserved, the reset value must be maintained
[4]	EXEV1FM	External event 1 fast mode 0: External event 1 is re-synchronized by the SHRTIM logic before acting on outputs, which adds a f_{SHRTIM} clock-related latency 1: External event 1 is acting asynchronously on outputs (low latency mode)

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		Note: This bit must not be modified once the counter in which the event is used is enabled (SHRTIM_MCTRL.TxCNTEN bit set).
[3:0]	EXEV1FLT	External event 1 filter This bitfield defines the frequency used to sample external event 1 input and the length of the digital filter applied to shrtim_exev1. The digital filter is made of a counter in which N valid samples are needed to validate a transition on the output. 0000: Filter disabled 0001: $f_{SAMPLING}$= f_{SHRTIM}, N=2 0010: $f_{SAMPLING}$= f_{SHRTIM}, N=4 0011: $f_{SAMPLING}$= f_{SHRTIM}, N=8 0100: $f_{SAMPLING}$= f_{EXEVS}/2, N=6 0101: $f_{SAMPLING}$= f_{EXEVS}/2, N=8 0110: $f_{SAMPLING}$= f_{EXEVS}/4, N=6 0111: $f_{SAMPLING}$= f_{EXEVS}/4, N=8 1000: $f_{SAMPLING}$= f_{EXEVS}/8, N=6 1001: $f_{SAMPLING}$= f_{EXEVS}/8, N=8 1010: $f_{SAMPLING}$= f_{EXEVS}/16, N=5 1011: $f_{SAMPLING}$= f_{EXEVS}/16, N=6 1100: $f_{SAMPLING}$= f_{EXEVS}/16, N=8 1101: $f_{SAMPLING}$= f_{EXEVS}/32, N=5 1110: $f_{SAMPLING}$= f_{EXEVS}/32, N=6 1111: $f_{SAMPLING}$= f_{EXEVS}/32, N=8

17.3.74 SHRTIM External Event Control Register 4 (SHRTIM_EXEVCTRL4)

Address offset: 0x3BC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXEVSCD		Reserved	EXEV10FM	EXEV10FLT				Reserved	EXEV9FM	EXEV9FLT				Reserved	EXEV8FM
rw			rw	rw					rw	rw					rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXEV8FLT				Reserved	EXEV7FM	EXEV7FLT				Reserved	EXEV6FM	EXEV6FLT			
rw				rw		rw				rw		rw			

Bit Field	Name	Description
[31:30]	EXEVSCD	External event sampling clock division This bitfield indicates the division ratio between the timer clock frequency (f_{SHRTIM}) and the external event signal sampling clock (f_{EXEVS}) used by the digital filters.

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		00: $f_{EXEVS}=f_{SHRTIM}$ 01: $f_{EXEVS}=f_{SHRTIM}/2$ 10: $f_{EXEVS}=f_{SHRTIM}/4$ 11: $f_{EXEVS}=f_{SHRTIM}/8$
[29]	Reserved	Reserved, the reset value must be maintained
[28]	EXEV10FM	External event 10 fast mode Refer to the EXEV1FM description.
[27:24]	EXEV10FLT	External event 10 filter Refer to the EXEV1FLT description.
[23]	Reserved	Reserved, the reset value must be maintained
[22]	EXEV9FM	External event 9 fast mode Refer to the EXEV1FM description.
[21:18]	EXEV9FLT	External event 9 filter Refer to the EXEV1FLT description.
[17]	Reserved	Reserved, the reset value must be maintained
[16]	EXEV8FM	External event 8 fast mode Refer to the EXEV1FM description.
[15:12]	EXEV8FLT	External event 8 filter Refer to the EXEV1FLT description.
[11]	Reserved	Reserved, the reset value must be maintained
[10]	EXEV7FM	External event 7 fast mode Refer to the EXEV1FM description.
[9:6]	EXEV7FLT	External event 7 filter Refer to the EXEV1FLT description.
[5]	Reserved	Reserved, the reset value must be maintained
[4]	EXEV6FM	External event 6 fast mode Refer to the EXEV1FM description.
[3:0]	EXEV6FLT	External event 6 filter Refer to the EXEV1FLT description.

17.3.75 SHRTIM ADC Trigger 1 Sources Register 1 (SHRTIM_ADTG1SRC1)

Address offset: 0x3C0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					ADTG1 TCPRD	ADTG1 TCCMP5	ADTG1 TCCMP4	ADTG1 TCCMP3	ADTG 1TCCMP2	ADTG 1TCCMP1	ADTG1 TBRSTRO	ADTG 1TBPRD	ADTG 1TBCMP5	ADTG 1TBCMP4	ADTG 1TBCMP3
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG 1TBCMP2	ADTG 1TBCMP1	ADTG1 TARSTRO	ADTG 1TAPRD	ADTG1 TACMP5	ADTG1 TACMP4	ADTG1 TACMP3	ADTG1 TACMP2	ADTG1 TACMP1	Reserved	ADTG 1MPRD	Reserved	ADTG 1MCMP4	ADTG 1MCMP3	ADTG 1MCMP2	ADTG 1MCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw		rw		rw	rw	rw	rw

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Bit Field	Name	Description
[31:0]	Reserved	Reserved, the reset value must be maintained
[26]	ADTG1TCPRD	ADC trigger 1 driven by timer C period event 0: No action 1: ADC trigger 1 is configured to be driven by timer C period event
[25]	ADTG1TCCMP5	ADC trigger 1 driven by timer C compare 5 event 0: No action 1: ADC trigger 1 is configured to be driven by timer C compare 5 event
[24]	ADTG1TCCMP4	ADC trigger 1 driven by timer C compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by timer C compare 4 event
[23]	ADTG1TCCMP3	ADC trigger 1 driven by timer C compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by timer C compare 3 event
[22]	ADTG1TCCMP2	ADC trigger 1 driven by timer C compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by timer C compare 2 event
[21]	ADTG1TCCMP1	ADC trigger 1 driven by timer C compare 1 event 0: No action 1: ADC trigger 1 is configured to be driven by timer C compare 1 event
[20]	ADTG1TBRSTRO	ADC trigger 1 driven by timer B reset or roll-over event 0: No action 1: ADC trigger 1 is configured to be driven by timer B reset or roll-over event
[19]	ADTG1TBPRD	ADC trigger 1 driven by timer B period event 0: No action 1: ADC trigger 1 is configured to be driven by timer B period event
[18]	ADTG1TBCMP5	ADC trigger 1 driven by timer B compare 5 event 0: No action 1: ADC trigger 1 is configured to be driven by timer B compare 5 event
[17]	ADTG1TBCMP4	ADC trigger 1 driven by timer B compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by timer B compare 4 event
[16]	ADTG1TBCMP3	ADC trigger 1 driven by timer B compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by timer B compare 3 event
[15]	ADTG1TBCMP2	ADC trigger 1 driven by timer B compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by timer B compare 2 event
[14]	ADTG1TBCMP1	ADC trigger 1 driven by timer B compare 1 event 0: No action

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		1: ADC trigger 1 is configured to be driven by timer B compare 1 event
[13]	ADTG1TARSTRO	ADC trigger 1 driven by timer A reset/roll-over event 0: No action 1: ADC trigger 1 is configured to be driven by timer A reset/roll-over event
[12]	ADTG1TAPRD	ADC trigger 1 driven by timer A period event 0: No action 1: ADC trigger 1 is configured to be driven by timer A period event
[11]	ADTG1TACMP5	ADC trigger 1 driven by timer A compare 5 event 0: No action 1: ADC trigger 1 is configured to be driven by timer A compare 5 event
[10]	ADTG1TACMP4	ADC trigger 1 driven by timer A compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by timer A compare 4 event
[9]	ADTG1TACMP3	ADC trigger 1 driven by timer A compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by timer A compare 3 event
[8]	ADTG1TACMP2	ADC trigger 1 driven by timer A compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by timer A compare 2 event
[7]	ADTG1TACMP1	ADC trigger 1 driven by timer A compare 1 event 0: No action 1: ADC trigger 1 is configured to be driven by timer A compare 1 event
[6]	Reserved	Reserved, the reset value must be maintained
[5]	ADTG1MPRD	ADC trigger 1 driven by master timer period event 0: No action 1: ADC trigger 1 is configured to be driven by master timer period event
[4]	Reserved	Reserved, the reset value must be maintained
[3]	ADTG1MCMP4	ADC trigger 1 driven by master timer compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by master timer compare 4 event
[2]	ADTG1MCMP3	ADC trigger 1 driven by master timer compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by master timer compare 3 event
[1]	ADTG1MCMP2	ADC trigger 1 driven by master timer compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by master timer compare 2 event
[0]	ADTG1MCMP1	ADC trigger 1 driven by master timer compare 1 event 0: No action

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		1: ADC trigger 1 is configured to be driven by master timer compare 1 event

17.3.76 SHRTIM ADC Trigger 1 Sources Register 2 (SHRTIM_ADTG1SRC2)

Address offset: 0x3C4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						ADTG1 EXEV5	ADTG1 EXEV4	ADTG1 EXEV3	ADTG 1EXE V2	ADTG 1EXE V1	ADTG1 TFRSTR O	ADTG1 TFPRD	ADTG1 TFCMP 5	ADTG1 TFCMP 4	ADTG1 TFCMP 3
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG1 TFCMP 2	ADTG1 TFCMP 1	Res erve d	ADTG 1TEPR D	ADTG1 TECMP 5	ADTG1 TECMP 4	ADTG1 TECMP 3	ADTG1 TECMP 2	ADTG1 TECMP 1	Reserv ed	ADTG 1TDPR D	ADTG1 TDCMP 5	ADTG1 TDCMP 4	ADTG1 TDCMP 3	ADTG1 TDCMP 2	ADTG1 TDCMP 1
rw	rw		rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31]	Reserved	Reserved, the reset value must be maintained
[30]	Reserved	Reserved, the reset value must be maintained
[29]	Reserved	Reserved, the reset value must be maintained
[28]	Reserved	Reserved, the reset value must be maintained
[27]	Reserved	Reserved, the reset value must be maintained
[26]	Reserved	Reserved, the reset value must be maintained
[25]	ADTG1EXEV5	ADC trigger 1 driven by external event 5 0: No action 1: ADC trigger 1 is configured to be driven by external event 5
[24]	ADTG1EXEV4	ADC trigger 1 driven by external event 4 0: No action 1: ADC trigger 1 is configured to be driven by external event 4
[23]	ADTG1EXEV3	ADC trigger 1 driven by external event 3 0: No action 1: ADC trigger 1 is configured to be driven by external event 3
[22]	ADTG1EXEV2	ADC trigger 1 driven by external event 2 0: No action 1: ADC trigger 1 is configured to be driven by external event 2
[21]	ADTG1EXEV1	ADC trigger 1 driven by external event 1 0: No action 1: ADC trigger 1 is configured to be driven by external event 1
[20]	ADTG1TFRSTRO	ADC trigger 1 driven by timer F reset and roll-over events 0: No action 1: ADC trigger 1 is configured to be driven by timer F reset and roll-over events
[19]	ADTG1TFPRD	ADC trigger 1 driven by timer F period events

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		0: No action 1: ADC trigger 1 is configured to be driven by timer F period event
[18]	ADTG1TFCMP5	ADC trigger 1 driven by timer F compare 5 event 0: No action 1: ADC trigger 1 is configured to be driven by timer F compare 5 event
[17]	ADTG1TFCMP4	ADC trigger 1 driven by timer F compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by timer F compare 4 event
[16]	ADTG1TFCMP3	ADC trigger 1 driven by timer F compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by timer F compare 3 event
[15]	ADTG1TFCMP2	ADC trigger 1 driven by timer F compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by timer F compare 2 event
[14]	ADTG1TFCMP1	ADC trigger 1 driven by timer F compare 1 event 0: No action 1: ADC trigger 1 is configured to be driven by timer F compare 1 event
[13]	Reserved	Reserved, the reset value must be maintained
[12]	ADTG1TEPRD	ADC trigger 1 driven by timer E period event 0: No action 1: ADC trigger 1 is configured to be driven by timer E period event
[11]	ADTG1TECMP5	ADC trigger 1 driven by timer E compare 5 event 0: No action 1: ADC trigger 1 is configured to be driven by timer E compare 5 event
[10]	ADTG1TECMP4	ADC trigger 1 driven by timer E compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by timer E compare 4 event
[9]	ADTG1TECMP3	ADC trigger 1 driven by timer E compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by timer E compare 3 event
[8]	ADTG1TECMP2	ADC trigger 1 driven by timer E compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by timer E compare 2 event
[7]	ADTG1TECMP1	ADC trigger 1 driven by timer E compare 1 event 0: No action 1: ADC trigger 1 is configured to be driven by timer E compare 1 event
[6]	Reserved	Reserved, the reset value must be maintained
[5]	ADTG1TDPRD	ADC trigger 1 driven by timer D period event 0: No action 1: ADC trigger 1 is configured to be driven by timer D period event
[4]	ADTG1TDCMP5	ADC trigger 1 driven by timer D compare 5 event 0: No action

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		1: ADC trigger 1 is configured to be driven by timer D compare 5 event
[3]	ADTG1TDCMP4	ADC trigger 1 driven by timer D compare 4 event 0: No action 1: ADC trigger 1 is configured to be driven by timer D compare 4 event
[2]	ADTG1TDCMP3	ADC trigger 1 driven by timer D compare 3 event 0: No action 1: ADC trigger 1 is configured to be driven by timer D compare 3 event
[1]	ADTG1TDCMP2	ADC trigger 1 driven by timer D compare 2 event 0: No action 1: ADC trigger 1 is configured to be driven by timer D compare 2 event
[0]	ADTG1TDCMP1	ADC trigger 1 driven by timer D compare 1 event 0: No action 1: ADC trigger 1 is configured to be driven by timer D compare 1 event

17.3.77 SHRTIM ADC Trigger 2 Sources Register 1 (SHRTIM_ADTG2SRC1)

Address offset: 0x3C8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				ADTG2TCRSTRO	ADTG2TCPRD	ADTG2TCCMP5	ADTG2TCCMP4	ADTG2TCCMP3	ADTG2TCCMP2	ADTG2TCCMP1	Reserved	ADTG2TBPRD	ADTG2TBCMP5	ADTG2TBCMP4	ADTG2TBCMP3
				rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG2TBCMP2	ADTG2TBCMP1	Reserved	ADTG2TAPRD	ADTG2TACMP5	ADTG2TACMP4	ADTG2TACMP3	ADTG2TACMP2	ADTG2TACMP1	Reserved	ADTG2MPRD	Reserved	ADTG2MCMP4	ADTG2MCMP3	ADTG2MCMP2	ADTG2MCMP1
rw	rw		rw	rw	rw	rw	rw	rw		rw		rw	rw	rw	rw

Refer to the SHRTIM_ADTG1SRC1 description.

17.3.78 SHRTIM ADC Trigger 2 Sources Register 2 (SHRTIM_ADTG2SRC2)

Address offset: 0x3CC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						ADTG2EXEV10	ADTG2EXEV9	ADTG2EXEV8	ADTG2EXEV7	ADTG2EXEV6	Reserved	ADTG2TFPRD	ADTG2TFCMP5	ADTG2TFCMP4	ADTG2TFCMP3
						rw	rw	rw	rw	rw		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG2TFCMP2	ADTG2TFCMP1	ADTG2TERSTRO	Reserved	ADTG2TECMP5	ADTG2TECMP4	ADTG2TECMP3	ADTG2TECMP2	ADTG2TECMP1	ADTG2TDRSTRO	ADTG2TDPRD	ADTG2TDCMP5	ADTG2TDCMP4	ADTG2TDCMP3	ADTG2TDCMP2	ADTG2TDCMP1
rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Refer to the SHRTIM_ADTG1SRC2 description.

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17.3.79 SHRTIM ADC Trigger 3 Sources Register 1 (SHRTIM_ADTG3SRC1)

Address offset: 0x3D0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					ADTG3 TCPRD	ADTG3 TCCMP5	ADTG3 TCCMP4	ADTG3 TCCMP3	ADTG 3TCCMP2	ADTG 3TCCMP1	ADTG3 TBRSTRO	ADTG 3TBPRD	ADTG 3TBCMP5	ADTG 3TBCMP4	ADTG 3TBCMP3
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG 3TBCMP2	ADTG 3TBCMP1	ADTG3 TARSTRO	ADTG 3TAPRD	ADTG3 TACMP5	ADTG3 TACMP4	ADTG3 TACMP3	ADTG3 TACMP2	ADTG3 TACMP1	Reserved	ADTG 3MPRD	Reserved	ADTG 3MCMP4	ADTG 3MCMP3	ADTG 3MCMP2	ADTG 3MCMP1
rw	rw	rw	rw	rw	rw	rw	rw	rw		rw		rw	rw	rw	rw

Refer to the SHRTIM_ADTG1SRC1 description.

17.3.80 SHRTIM ADC Trigger 3 Sources Register 2 (SHRTIM_ADTG3SRC2)

Address offset: 0x3D4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						ADTG3 EXEV5	ADTG3 EXEV4	ADTG3 EXEV3	ADTG 3EXEV2	ADTG 3EXEV1	ADTG3 TFRSTRO	ADTG3 TFPRD	ADTG3 TFCMP5	ADTG3 TFCMP4	ADTG3 TFCMP3
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG3 TFCMP2	ADTG3 TFCMP1	Reserved	ADTG 3TEPRD	ADTG3 TECMP5	ADTG3 TECMP4	ADTG3 TECMP3	ADTG3 TECMP2	ADTG3 TECMP1	Reserved	ADTG 3TDPRD	ADTG3 TDCMP5	ADTG3 TDCMP4	ADTG3 TDCMP3	ADTG3 TDCMP2	ADTG3 TDCMP1
rw	rw		rw	rw	Rw	rw	rw	rw		rw	rw	rw	rw	rw	rw

Refer to the SHRTIM_ADTG1SRC2 description.

17.3.81 SHRTIM ADC Trigger 4 Sources Register 1 (SHRTIM_ADTG4SRC1)

Address offset: 0x3D8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				ADTG4 TCRSTRO	ADTG4 TCPRD	ADTG4 TCCMP5	ADTG4 TCCMP4	ADTG4 TCCMP3	ADTG4 TCCMP2	ADTG4 TCCMP1	Reserved	ADTG4 TBPRD	ADTG4 TBCMP5	ADTG4 TBCMP4	ADTG4 TBCMP3
				rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG4 TBCMP2	ADTG4 TBCMP1	Reserved	ADTG 4TAPRD	ADTG4 TACMP5	ADTG4 TACMP4	ADTG4 TACMP3	ADTG4 TACMP2	ADTG4 TACMP1	Reserved	ADTG4 MPRD	Reserved	ADTG4 MCMP4	ADTG4 MCMP3	ADTG4 MCMP2	ADTG4 MCMP1
rw	rw		rw	rw	rw	rw	rw	rw	r	rw		rw	rw	rw	rw

Refer to the SHRTIM_ADTG1SRC1 description.

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17.3.82 SHRTIM ADC Trigger 4 Sources Register 2 (SHRTIM_ADTG4SRC2)

Address offset: 0x3DC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						ADTG4 EXEV10	ADTG4 EXEV9	ADTG4 EXEV8	ADTG4 EXEV7	ADTG 4EXE V6	Reserve d	ADTG4 TFPRD	ADTG4 TFCMP 5	ADTG4 TFCMP 4	ADTG4 TFCMP 3
						rw	rw	rw	rw	rw		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADTG4 TFCMP 2	ADTG4 TFCMP 1	ADTG4 TERST RO	Res erve d	ADTG4 TECMP 5	ADTG4 TECMP 4	ADTG4 TECMP 3	ADTG4 TECMP 2	ADTG4 TECMP 1	ADTG4 TDRST RO	ADTG 4TDPR D	ADTG4 TDCM P5	ADTG4 TDCM P4	ADTG4 TDCM P3	ADTG4 TDCM P2	ADTG4 TDCM P1
rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Refer to the SHRTIM_ADTG1SRC2 description.

17.3.83 SHRTIM Fault Input Register 1 (SHRTIM_FALTIN1)

Address offset: 0x3E0

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FALT4L CK	FALT4FLT				FALT4SR C0	FALT4P OL	FALT 4E	FALT3L CK	FALT3FLT				FALT3SR C0	FALT3P OL	FALT 3E
rw	rw				rw	rw	rw	rw	rw				rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FALT2L CK	FALT2FLT				FALT2SR C0	FALT2P OL	FALT 2E	FALT1L CK	FALT1FLT				FALT1SR C0	FALT1P OL	FALT 1E
rw	rw				rw	rw	rw	rw	rw				rw	rw	rw

Bit Field	Name	Description
[31]	FALT4LCK	Fault 4 Lock Refer to the SHRTIM_FALTIN1.FALT1LCK description.
[30:27]	FALT4FLT	Fault 4 filter Refer to the SHRTIM_FALTIN1.FALT1FLT[3:0] description.
[26]	FALT4SRC0	Fault 4 source bit 0 Refer to the SHRTIM_FALTIN1.FALT1SRC0 description.
[25]	FALT4POL	Fault 4 polarity Refer to the SHRTIM_FALTIN1.FALT1POL description.
[24]	FALT4E	Fault 4 enable Refer to the SHRTIM_FALTIN1.FALT1E description.
[23]	FALT3LCK	Fault 3 Lock Refer to the SHRTIM_FALTIN1.FALT1LCK description.
[22:19]	FALT3FLT	Fault 3 filter Refer to the SHRTIM_FALTIN1.FALT1FLT[3:0] description.

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Address: 20 Science Park, #03-15/16
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[18]	FALT3SRC0	Fault 3 source bit 0 Refer to the SHRTIM_FALTIN1.FALT1SRC0 description.
[17]	FALT3POL	Fault 3 polarity Refer to the SHRTIM_FALTIN1.FALT1POL description.
[16]	FALT3E	Fault 3 enable Refer to the SHRTIM_FALTIN1.FALT1E description.
[15]	FALT2LCK	Fault 2 Lock Refer to the SHRTIM_FALTIN1.FALT1LCK description.
[14:11]	FALT2FLT	Fault 2 filter Refer to the SHRTIM_FALTIN1.FALT1FLT[3:0] description.
[10]	FALT2SRC0	Fault 2 source bit 0 Refer to the SHRTIM_FALTIN1.ALT1SRC0 description.
[9]	FALT2POL	Fault 2 polarity Refer to the SHRTIM_FALTIN1.FALT1POL description.
[8]	FALT2E	Fault 2 enable Refer to the SHRTIM_FALTIN1.FALT1Edescription.
[7]	FALT1LCK	Fault 1 Lock The FALT1LCK bit modifies the write attributes of the fault programming bit, so that they are protected against spurious write accesses. This bit is write-once. Once it has been set, it cannot be modified till the next system reset. 0: FALT1E, FALT1POL, FALT1SRC[1:0], FALT1FLT[3:0] and FALT1CSEL[2:0] bits are read/write. 1: FALT1E, FALT1POL, FALT1SRC[1:0], FALT1FLT[3:0] and FALT1CSEL[2:0] bits cannot be written (read-only mode)
[6:3]	FALT1FLT	Fault 1 filter This bitfield defines the frequency used to sample FALT1 input and the length of the digital filter applied to FALT1. The digital filter is made of an event counter in which N events are needed to validate a transition on the output. 0000: No filter, FALT1 acts asynchronously 0001: $f_{SAMPLING} = f_{SHRTIM}$, N = 2 0010: $f_{SAMPLING} = f_{SHRTIM}$, N = 4 0011: $f_{SAMPLING} = f_{SHRTIM}$, N = 8 0100: $f_{SAMPLING} = f_{FALTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{FALTS}$, N = 8 0110: $f_{SAMPLING} = f_{FALTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{FALTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{FALTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{FALTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{FALTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{FALTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{FALTS}/16$, N = 8

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		1101: $f_{SAMPLING} = f_{FALTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{FALTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{FALTS}/32$, N = 8 *Note: This bitfield is written only when FALT1E enable bit is reset.* *Note: This bitfield is modified when FALT1LCK has been programmed.*
[2]	FALT1SRC0	Fault 1 source bit 0 The FALT1SRC[1:0] bitfield selects the FAULT1 input source (refer to for connection details). 00: Fault 1 input is SHRTIM_FALT1 input pin 01: Fault 1 input is a COMPx output 10: Fault 1 input is EXEV1_muxout input pin *Note: This bitfield is written only when FALT1E enable bit is reset.*
[1]	FALT1POL	Fault 1 polarity This bit selects the FAULT1 input polarity. 0: Fault 1 input is active low 1: Fault 1 input is active high *Note: This bitfield is written only when FALT1E enable bit is reset.*
[0]	FALT1E	Fault 1 enable This bit enables the global FAULT1 input circuitry. 0: Fault 1 input disabled 1: Fault 1 input enabled

17.3.84 SHRTIM Fault Input Register 2 (SHRTIM_FALTIN2)

Address offset: 0x3E4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SFALTFLECCEN	SFALTPVDEN	SFALTLOCKUPEN	SFALTSMPAREN	SFALTSMECCEN	SFALTCKSECEN	FALTSCD		Reserved		FALT6SRC1	FALT5SRC1	FALT4SRC1	FALT3SRC1	FALT2SRC1	FALT1SRC1
rw	rw	rw	rw	rw	rw	rw				rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FALT6LCK	FALT6FLT				FALT6SRC0	FALT6POL	FALT6E	FALT5LCK	FALT5FLT				FALT5SRC0	FALT5POL	FALT5E
rw	rw				rw	rw	rw	rw	rw				rw	rw	rw

Bit Field	Name	Description
[31]	SFALTFLECCEN	The flash ECC double detection error as SHRTIM system fault input enable This bit is set by software and can only be cleared by a system reset or a power-on reset (POR).
[30]	SFALTPVDEN	The PVD error as SHRTIM system fault input enable This bit is set by software and can only be cleared by a system reset or a power-on reset (POR).
[29]	SFALTLOCKUPEN	The core lockup as SHRTIM system fault input enable

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		This bit is set by software and can only be cleared by a system reset or a power-on reset (POR).
[28]	SFALTSMPAREN	The sram parity error as SHRTIM system fault input enable This bit is set by software and can only be cleared by a system reset or a power-on reset (POR).
[27]	SFALTSMECCEN	The sram ECC error as SHRTIM system fault input enable This bit is set by software and can only be cleared by a system reset or a power-on reset (POR).
[26]	SFALTCKSECEN	The clock security system error as SHRTIM system fault input enable This bit is set by software and can only be cleared by a system reset or a power-on reset (POR).
[25:24]	FALTSCD	Fault Sampling clock division This bitfield indicates the division ratio between the timer clock frequency (f_{SHRTIM}) and the fault signal sampling clock (f_{FALTS}) used by the digital filters. 00: $f_{FALTS}=f_{SHRTIM}$ 01: $f_{FALTS}=f_{SHRTIM}/2$ 10: $f_{FALTS}=f_{SHRTIM}/4$ 11: $f_{FALTS}=f_{SHRTIM}/8$ *Note: This bitfield must be written prior to any of the FALTxE enable bits.*
[23:22]	Reserved	Reserved, the reset value must be maintained
[21]	FALT6SRC1	Fault 6 source bit 1 Refer to the FALT6SRC_0 description.
[20]	FALT5SRC1	Fault 5 source bit 1 Refer to the FALT5SRC_0 description.
[19]	FALT4SRC1	Fault 4 source bit 1 Refer to the FALT4SRC_0 description.
[18]	FALT3SRC1	Fault 3 source bit 1 Refer to the FALT3SRC_0 description.
[17]	FALT2SRC1	Fault 2 source bit 1 Refer to the FALT2SRC_0 description.
[16]	FALT1SRC1	Fault 1 source bit 1 Refer to the FALT1SRC_0 description.
[15]	FALT6LCK	Fault 6 Lock Refer to the SHRTIM_FALTIN1.FALT1LCK description.
[14:11]	FALT6FLT	Fault 6 filter Refer to the SHRTIM_FALTIN1.FALT1FLT[3:0] description.
[10]	FALT6SRC0	Fault 6 source bit 0 Refer to the SHRTIM_FALTIN1.FALT1SRC0 description.
[9]	FALT6POL	Fault 6 polarity Refer to the SHRTIM_FALTIN1.FALT1POL description.
[8]	FALT6E	Fault 6 enable

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		Refer to the SHRTIM_FALTIN1.FALT1E description.
[7]	FALT5LCK	Fault 5 Lock Refer to the SHRTIM_FALTIN1.FALT1LCK description.
[6:3]	FALT5FLT	Fault 5 filter Refer to the SHRTIM_FALTIN1.FALT1FLT[3:0] description.
[2]	FALT5SRC0	Fault 5 source bit 0 Refer to the SHRTIM_FALTIN1.FALT1SRC0 description.
[1]	FALT5POL	Fault 5 polarity Refer to the SHRTIM_FALTIN1.FALT1POL description.
[0]	FALT5E	Fault 5 enable Refer to the SHRTIM_FALTIN1.FALT1E description.

17.3.85 SHRTIM Fault Input Register 3 (SHRTIM_FALTIN3)

Address offset: 0x3E8

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FALT4RSTM	FALT4CRST	FALT4CNT				FALT4BLKS	FALT4BLKEN	FALT3RSTM	FALT3CRST	FALT3CNT				FALT3BLKS	FALT3BLKEN
rw	rt_w	rw				rw	rw	rw	rt_w	rw				rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FALT2RSTM	FALT2CRST	FALT2CNT				FALT2BLKS	FALT2BLKEN	FALT1RSTM	FALT1CRST	FALT1CNT				FALT1BLKS	FALT1BLKEN
rw	rt_w	rw				rw	rw	rw	rt_w	rw				rw	rw

Bit Field	Name	Description
[31]	FALT4RSTM	Fault 4 reset mode Refer to the FALT1RSTM description.
[30]	FALT4CRST	Fault 4 counter reset Refer to the FALT1CRST description.
[29:26]	FALT4CNT	Fault 4 counter Refer to the FALT1CNT description.
[25]	FALT4BLKS	Fault 4 blanking source Refer to the FALT1BLKS description.
[24]	FALT4BLKEN	Fault 4 blanking enable Refer to the FALT1BLKEN description.
[23]	FALT3RSTM	Fault 3 reset mode Refer to the FALT1RSTM description.
[22]	FALT3CRST	Fault 3 counter reset Refer to the FALT1CRST description.

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[21:18]	FALT3CNT	Fault 3 counter Refer to the FALT1CNT description.
[17]	FALT3BLKS	Fault 3 blanking source Refer to the FALT1BLKS description.
[16]	FALT3BLKEN	Fault 3 blanking enable Refer to the FALT1BLKEN description.
[15]	FALT2RSTM	Fault 2 reset mode Refer to the FALT1RSTM description.
[14]	FALT2CRST	Fault 2 counter reset Refer to the FALT1CRST description.
[13:10]	FALT2CNT	Fault 2 counter Refer to the FALT1CNT description.
[9]	FALT2BLKS	Fault 2 blanking source Refer to the FALT1BLKS description.
[8]	FALT2BLKEN	Fault 2 blanking enable Refer to the FALT1BLKEN description.
[7]	FALT1RSTM	Fault 1 reset mode This bit selects the FAULT1 counter reset mode 0: Fault 1 counter is reset on each reset/roll-over event 1: Fault 1 counter is reset on each reset/roll-over event only if no fault occurred during last counting period. *Note: This bitfield is written only when FALT1E enable bit is reset.*
[6]	FALT1CRST	Fault 1 counter reset This bit resets the FAULT1 counter. It is set by software and reset by hardware. 0: No action 1: Fault 1 counter is reset
[5:2]	FALT1CNT	Fault 1 counter This bitfield selects the FAULT1 counter threshold. A fault is considered valid when the number of events is equal to the (FALT1CNT[3:0]+1) value.
[1]	FALT1BLKS	Fault 1 blanking source The FATL1BLKS bit selects the FAULT1 blanking source (refer to for details). 0: Fault 1 reset-aligned blanking window 1: Fault 1 moving blanking window *Note: This bitfield is written only when FALT1E enable bit is reset.*
[0]	FALT1BLKEN	Fault 1 blanking enable The FATL1BLKEN bit selects the FAULT1 blanking mode. The blanking source is defined by the FALT1BLKS bit. 0: No blanking on fault 1 1: Fault 1 blanking mode *Note: This bitfield is written only when FALT1E enable bit is reset*

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17.3.86 SHRTIM Fault Input Register 4 (SHRTIM_FALTIN4)

Address offset: 0x3EC

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FALT6RSTM	FALT6CRST	FALT6CNT				FALT6BLKS	FALT6BLKEN	FALT5RSTM	FALT5CRST	FALT5CNT				FALT5BLKS	FALT5BLKEN
rw	rt_w	rw				rw	rw	rw	rt_w	rw				rw	rw

Bit Field	Name	Description
[31:16]	Reserved	Reserved, the reset value must be maintained
[15]	FALT6RSTM	Fault 6 reset mode Refer to the FALT1RSTM description.
[14]	FALT6CRST	Fault 6 counter reset Refer to the FALT1CRST description.
[13:10]	FALT6CNT	Fault 6 counter Refer to the FALT1CNT description.
[9]	FALT6BLKS	Fault 6 blanking source Refer to the FALT1BLKS description.
[8]	FALT6BLKEN	Fault 6 blanking enable Refer to the FALT1BLKEN description.
[7]	FALT5RSTM	Fault 5 reset mode Refer to the FALT1RSTM description.
[6]	FALT5CRST	Fault 5 counter reset Refer to the FALT1CRST description.
[5:2]	FALT5CNT	Fault 5 counter Refer to the FALT1CNT description.
[1]	FALT5BLKS	Fault 5 blanking source Refer to the FALT1BLKS description.
[0]	FALT5BLKEN	Fault 5 blanking enable Refer to the FALT1BLKEN description.

17.3.87 SHRTIM Burst DMA Master Timer Update Register (SHRTIM_BDMTUPD)

Address offset: 0x3F0

Reset value: 0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCMPDAT4	MCMPDAT3	MCMPDAT2	MCMPDAT1	MREPT	MPRD	MCNT	MIDEN	MINTCLR	MCTRL
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31:10]	Reserved	Reserved, the reset value must be maintained
[9]	MCMPDAT4	SHRTIM_MCMP4DAT register update enable 0: SHRTIM_MCMP4DAT register is not updated by burst DMA accesses 1: SHRTIM_MCMP4DAT register is updated by burst DMA accesses
[8]	MCMPDAT3	SHRTIM_MCMP3DAT register update enable 0：SHRTIM_MCMP3DAT register is not updated by burst DMA accesses 1：SHRTIM_MCMP3DAT register is updated by burst DMA accesses
[7]	MCMPDAT2	SHRTIM_MCMP2DAT register update enable 0：SHRTIM_MCMP2DAT register is not updated by burst DMA accesses 1：SHRTIM_MCMP2DAT register is updated by burst DMA accesses
[6]	MCMPDAT1	SHRTIM_MCMP1DAT register update enable 0：SHRTIM_MCMP1DAT register is not updated by burst DMA accesses 1：SHRTIM_MCMP1DAT register is updated by burst DMA accesses
[5]	MREPT	SHRTIM_MREPT register update enable 0：SHRTIM_MREPT register is not updated by burst DMA accesses 1：SHRTIM_MREPT register is updated by burst DMA accesses
[4]	MPRD	SHRTIM_MPRD register update enable 0：SHRTIM_MPRD register is not updated by burst DMA accesses 1：SHRTIM_MPRD register is updated by burst DMA accesses
[3]	MCNT	SHRTIM_MCNT register update enable 0：SHRTIM_MCNT register is not updated by burst DMA accesses 1：SHRTIM_MCNT register is updated by burst DMA accesses
[2]	MIDEN	SHRTIM_MIDEN register update enable 0：SHRTIM_MIDEN register is not updated by burst DMA accesses 1 ：SHRTIM_MIDEN register is updated by burst DMA accesses
[1]	MINTCLR	SHRTIM_MINTCLR register update enable 0：SHRTIM_MINTCLR register is not updated by burst DMA accesses 1：SHRTIM_MINTCLR register is updated by burst DMA accesses
[0]	MCTRL	SHRTIM_CTRL register update enable 0：SHRTIM_CTRL register is not updated by burst DMA accesses 1：SHRTIM_CTRL register is updated by burst DMA accesses

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17.3.88 SHRTIM Burst DMA Timer x Update Register (SHRTIM_BDTxUPD)

Address offset: 0x3F4

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									TxEXEVFLT3	TxCTRL2	TxFALT	TxOUT	TxCHOP	TxCNTRST	TxEXEVFLT2
									rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxEXEVFLT1	TxRST2	TxSET2	TxRST1	TxSET1	TxDT	TxCMP4DAT	TxCMP3DAT	TxCMP2DAT	TxCMP1DAT	TxREPT	TxPRD	TxCNT	TxIDEN	TxINTCLR	TxCTRL
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
[31:23]	Reserved	Reserved, the reset value must be maintained
[22]	TxEXEVFLT3	SHRTIM_TxEXEVFLT3 register update enable 0: Burst DMA access does not cause the TxEXEVFLT3 to update. 1: Burst DMA access causes the TxEXEVFLT3 to update.
[21]	TxCTRL2	SHRTIM_TxCTRL2 register update enable 0: Burst DMA access does not cause the SHRTIM_TxCTRL2 to update. 1: Burst DMA access cause the SHRTIM_TxCTRL2 to update.
[20]	TxFALT	SHRTIM_TxFALT register update enable 0: Burst DMA access does not cause the SHRTIM_TxFALT to update. 1: Burst DMA access cause the SHRTIM_TxFALT to update.
[19]	TxOUT	SHRTIM_TxOUT register update enable 0: Burst DMA access does not cause the SHRTIM_TxOUT to update. 1: Burst DMA access cause the SHRTIM_TxOUT to update.
[18]	TxCHOP	SHRTIM_TxCHOP register update enable 0: Burst DMA access does not cause the SHRTIM_TxCHOP to update. 1: Burst DMA access cause the SHRTIM_TxCHOP to update.
[17]	TxCNTRST	SHRTIM_TxCNTRST register update enable 0: Burst DMA access does not cause the SHRTIM_TxCNTRST to update. 1: Burst DMA access cause the SHRTIM_TxCNTRST to update.
[16]	TxEXEVFLT2	SHRTIM_TxEXEVFLT2 register update enable 0: Burst DMA access does not cause the SHRTIM_TxEXEVFLT2 to update. 1: Burst DMA access cause the SHRTIM_TxEXEVFLT2 to update.
[15]	TxEXEVFLT1	SHRTIM_TxEXEVFLT1 register update enable 0: Burst DMA access does not cause the SHRTIM_TxEXEVFLT1 to update. 1: Burst DMA access cause the SHRTIM_TxEXEVFLT1 to update.
[14]	TxRST2	SHRTIM_TxRST2 register update enable 0: Burst DMA access does not cause the SHRTIM_TxRST2 to update. 1: Burst DMA access cause the SHRTIM_TxRST2 to update.
[13]	TxSET2	SHRTIM_TxSET2 register update enable

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		0: Burst DMA access does not cause the SHRTIM_TxSET2 to update. 1: Burst DMA access cause the SHRTIM_TxSET2 to update.
[12]	TxRST1	SHRTIM_TxRST1 register update enable 0: Burst DMA access does not cause the SHRTIM_TxRST1 to update. 1: Burst DMA access cause the SHRTIM_TxRST1 to update.
[11]	TxSET1	SHRTIM_TxSET1 register update enable 0: Burst DMA access does not cause the SHRTIM_TxSET1 to update. 1: Burst DMA access cause the SHRTIM_TxSET1 to update.
[10]	TxDT	SHRTIM_TxDT register update enable 0: Burst DMA access does not cause the SHRTIM_TxDT to update. 1: Burst DMA access cause the SHRTIM_TxDT to update.
[9]	TxCMP4DAT	SHRTIM_TxCMP4DAT register update enable 0: Burst DMA access does not cause the SHRTIM_TxCMP4DAT to update. 1: Burst DMA access cause the SHRTIM_TxCMP4DAT to update.
[8]	TxCMP3DAT	SHRTIM_TxCMP3DAT register update enable 0: Burst DMA access does not cause the SHRTIM_TxCMP3DAT to update. 1: Burst DMA access cause the SHRTIM_TxCMP3DAT to update.
[7]	TxCMP2DAT	SHRTIM_TxCMP2DAT register update enable 0: Burst DMA access does not cause the SHRTIM_TxCMP2DAT to update. 1: Burst DMA access cause the SHRTIM_TxCMP2DAT to update.
[6]	TxCMP1DAT	SHRTIM_TxCMP1DAT register update enable 0: Burst DMA access does not cause the SHRTIM_TxCMP1DAT to update. 1: Burst DMA access cause the SHRTIM_TxCMP1DAT to update.
[5]	TxREPT	SHRTIM_TxREPT register update enable 0: Burst DMA access does not cause the SHRTIM_TxREPT to update. 1: Burst DMA access cause the SHRTIM_TxREPT to update.
[4]	TxPRD	SHRTIM_TxPRD register update enable 0: Burst DMA access does not cause the SHRTIM_TxPRD to update. 1: Burst DMA access cause the SHRTIM_TxPRD to update.
[3]	TxCNT	SHRTIM_TxCNT register update enable 0: Burst DMA access does not cause the SHRTIM_TxCNT to update. 1: Burst DMA access cause the SHRTIM_TxCNT to update.
[2]	TxIDEN	SHRTIM_TxIDEN register update enable 0: Burst DMA access does not cause the SHRTIM_TxIDEN to update. 1: Burst DMA access cause the SHRTIM_TxIDEN to update.
[1]	TxINTCLR	SHRTIM_TxINTCLR register update enable 0: Burst DMA access does not cause the SHRTIM_TxINTCLR to update. 1: Burst DMA access cause the SHRTIM_TxINTCLR to update.
[0]	TxCTRL	SHRTIM_TxCTRL register update enable 0: Burst DMA access does not cause the SHRTIM_TxCTRL to update. 1: Burst DMA access cause the SHRTIM_TxCTRL to update.

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17.3.89 SHRTIM Burst DMA Data Register (SHRTIM_BDDAT)

Address offset: 0x40C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BDMADATA															
w															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BDMADATA															
w															

Bit Field	Name	Description
[31:0]	BDMADATA	Burst DMA data register When a write operation is performed on this register, the register value will be loaded into the register enabled by SHRTIM_BDTxUPD or SHRTIM_BDMTUPD, which will also cause the increment of the register pointer to the next location to be filled.

17.3.90 SHRTIM ADC Trigger Extended Register 1 (SHRTIM_ADTGEX1)

Address offset: 0x410

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										ADTG9SRC					
										rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		ADTG7SRC						Reserved		ADTG5SRC					
		rw								rw					

Bit Field	Name	Description
[31:22]	Reserved	Reserved, the reset value must be maintained
[21:16]	ADTG9SRC	ADC trig 9 source select Refer to the ADTG5SRC description.
[15:14]	Reserved	Reserved, the reset value must be maintained
[13:8]	ADTG7SRC	ADC trig 7 source select Refer to the ADTG5SRC description.
[7:6]	Reserved	Reserved, the reset value must be maintained
[5:0]	ADTG5SRC	ADC trig 5 source select 0: Trigger on master timer compare 1

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		1: Trigger on master timer compare 2 2: Trigger on master timer compare 3 3: Trigger on master timer compare 4 4: Trigger on master timer period 5: Trigger on external event 1 6: Trigger on external event 2 7: Trigger on external event 3 8: Trigger on external event 4 9: Trigger on external event 5 10: Trigger on timer A compare 1 11: Trigger on timer A compare 2 12: Trigger on timer A compare 3 13: Trigger on timer A compare 4 14: Trigger on timer A compare 5 15: Trigger on timer A period 16: Trigger on timer A reset and counter roll-over 17: Trigger on timer B compare 1 18: Trigger on timer B compare 2 19: Trigger on timer B compare 3 20: Trigger on timer B compare 4 21: Trigger on timer B compare 5 22: Trigger on timer B period 23: Trigger on timer B reset and counter roll-over 24: Trigger on timer C compare 1 25: Trigger on timer C compare 2 26: Trigger on timer C compare 3 27: Trigger on timer C compare 4 28: Trigger on timer C compare 5 29: Trigger on timer C period 30: Trigger on timer D compare 1 31: Trigger on timer D compare 2 32: Trigger on timer D compare 3 33: Trigger on timer D compare 4 34: Trigger on timer D compare 5 35: Trigger on timer D period 36: Trigger on timer E compare 1 37: Trigger on timer E compare 2 38: Trigger on timer E compare 3 39: Trigger on timer E compare 4 40: Trigger on timer E compare 5 41: Trigger on timer E period 42: Trigger on timer F compare 1 43: Trigger on timer F compare 2

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		44: Trigger on timer F compare 3 45: Trigger on timer F compare 4 46: Trigger on timer F compare 5 47: Trigger on timer F period 48: Trigger on timer F reset and counter roll-over

17.3.91 SHRTIM ADC Trigger Extended Register 2 (SHRTIM_ADTGEX2)

Address offset: 0x414

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										ADTG10SRC					
										rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		ADTG8SRC						Reserved		ADTG6SRC					
		rw								rw					

Bit Field	Name	Description
[31:22]	Reserved	Reserved, the reset value must be maintained
[21:16]	ADTG10SRC	ADC trig 10 source select Refer to the ADTG5SRC description.
[15:14]	Reserved	Reserved, the reset value must be maintained
[13:8]	ADTG8SRC	ADC trig 8 source select Refer to the ADTG5SRC description.
[7:6]	Reserved	Reserved, the reset value must be maintained
[5:0]	ADTG6SRC	ADC trig 6 source select 0: Triggered on the master timer compare 1 1: Triggered on the master timer compare 2 2: Triggered on the master timer compare 3 3: Triggered on the master timer compare 4 4: Triggered on the master timer period 5: Triggered on the external event 6 6: Triggered on the external event 7 7: Triggered on the external event 8 8: Triggered on the external event 9 9: Triggered on the external event 10 10: Triggered on the timer A compare 1 11: Triggered on the timer A compare 2 12: Triggered on the timer A compare 3 13: Triggered on the timer A compare 4 14: Triggered on the timer A compare 5

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		1: Triggered on the timer A period 16: Triggered on the timer B compare 1 17: Triggered on the timer B compare 2 18: Triggered on the timer B compare 3 19: Triggered on the timer B compare 4 20: Triggered on the timer B compare 5 21: Triggered on the timer B period 22: Triggered on the timer C compare 1 23: Triggered on the timer C compare 2 24: Triggered on the timer C compare 3 25: Triggered on the timer C compare 4 26: Triggered on the timer C compare 5 2: Triggered on the timer C period 28: Triggered on the timer C reset and counter roll-over 29: Triggered on the timer D compare 1 30: Triggered on the timer D compare 2 31: Triggered on the timer D compare 3 32: Triggered on the timer D compare 4 33: Triggered on the timer D compare 5 34: Triggered on the timer D period 35: Triggered on the timer D reset and counter roll-over 36: Triggered on the timer E compare 1 37: Triggered on the timer E compare 2 38: Triggered on the timer E compare 3 39: Triggered on the timer E compare 4 40: Triggered on the timer E compare 5 41: Triggered on the timer E reset and counter roll-over 42: Triggered on the timer F compare 1 43: Triggered on the timer F compare 2 44: Triggered on the timer F compare 3 45: Triggered on the timer F compare 4 46: Triggered on the timer F compare 5 47: Triggered on the timer F period

17.3.92 SHRTIM ADC Trigger Update Register (SHRTIM_ADTGUPD)

Address offset: 0x418

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									ADTG10UPDSRC			Reserved	ADTG9UPDSRC		
										rw				rw	

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ADTG8UPDSRC			Reserved	ADTG7UPDSRC			Reserved	ADTG6UPDSRC			Reserved	ADTG5UPDSRC		
	rw				rw				rw				rw		

Bit Field	Name	Description
[31:23]	Reserved	Reserved, the reset value must be maintained
[22:20]	ADTG10UPDSRC	ADC trigger 10 update source Refer to the ADTG5UPDSRC[2:0] description
[19]	Reserved	Reserved, the reset value must be maintained
[18:16]	ADTG9UPDSRC	ADC trigger 9 update source Refer to the ADTG5UPDSRC[2:0] description
[15]	Reserved	Reserved, the reset value must be maintained
[14:12]	ADTG8UPDSRC	ADC trigger 8 update source Refer to the ADTG5UPDSRC[2:0] description
[11]	Reserved	Reserved, the reset value must be maintained
[10:8]	ADTG7UPDSRC	ADC trigger 7 update source Refer to the ADTG5UPDSRC[2:0] description
[7]	Reserved	Reserved, the reset value must be maintained
[6:4]	ADTG6UPDSRC	ADC trigger 6 update source Refer to the ADTG5UPDSRC[2:0] description
[3]	Reserved	Reserved, the reset value must be maintained
[2:0]	ADTG5UPDSRC	ADC trigger 5 update source These bits define the source which triggers the update of SHRTIM_ADTGEX1.ADTG5SRC[5:0] bitfield (from preload to active register transfer). It only defines the source timer. The exact conditions are defined by the SHRTIM_MCTRL.BRSTDMA[1:0] and SHRTIM_TxCTRL.UPDGAT[3:0] bit fields. 000: Master timer 001: Timer A 010: Timer B 011: Timer C 100: Timer D 101: Timer E 110: Timer F 111: Reserved

17.3.93 SHRTIM ADC Post Scaler Register 1 (SHRTIM_ADCPSC1)

Address offset: 0x41C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	ADC5PSC	Reserved	ADC4PSC	Reserved	ADC3PSC
	rw		rw		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC3PSC				Reserved	ADC2PSC					Reserved	ADC1PSC				
rw					rw						rw				

Bit Field	Name	Description
[31:29]	Reserved	Reserved, the reset value must be maintained
[28:24]	ADC5PSC	ADC trigger 5 post prescaler This bit selects the post-scaler ratio of ADC trigger 5.
[23]	Reserved	Reserved, the reset value must be maintained
[22:18]	ADC4PSC	ADC trigger 4 post prescaler This bit selects the post-scaler ratio of ADC trigger 4.
[17]	Reserved	Reserved, the reset value must be maintained
[16:12]	ADC3PSC	ADC trigger 3 post prescaler This bit selects the post-scaler ratio of ADC trigger 3.
[11]	Reserved	Reserved, the reset value must be maintained
[10:6]	ADC2PSC	ADC trigger 2 post prescaler This bit selects the post-scaler ratio of ADC trigger 2.
[5]	Reserved	Reserved, the reset value must be maintained
[4:0]	ADC1PSC	ADC trigger 1 post prescaler This bit selects the post-scaler ratio of ADC trigger 1.

17.3.94 SHRTIM ADC Post Scaler Register 2 (SHRTIM_ADCPSC2)

Address offset: 0x420

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			ADC10PSC					Reserved	ADC9PSC					Reserved	ADC8PSC
			rw						rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC8PSC				Reserved	ADC7PSC					Reserved	ADC6PSC				
rw					rw						rw				

Bit Field	Name	Description
[31:29]	Reserved	Reserved, the reset value must be maintained
[28:24]	ADC10PSC	ADC trigger 10 post prescaler This bit selects the post-scaler ratio of ADC trigger 10.
[23]	Reserved	Reserved, the reset value must be maintained
[22:18]	ADC9PSC	ADC trigger 9 post prescaler This bit selects the post-scaler ratio of ADC trigger 9.

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[17]	Reserved	Reserved, the reset value must be maintained
[16:12]	ADC8PSC	ADC trigger 8 post prescaler This bit selects the post-scaler ratio of ADC trigger 8.
[11]	Reserved	Reserved, the reset value must be maintained
[10:6]	ADC7PSC	ADC trigger 7 post prescaler This bit selects the post-scaler ratio of ADC trigger 7.
[5]	Reserved	Reserved, the reset value must be maintained
[4:0]	ADC6PSC	ADC trigger 6 post prescaler This bit selects the post-scaler ratio of ADC trigger 6.

17.3.95 SHRTIM Software Fault Register (SHRTIM_SFTFALT)

Address offset: 0x428

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SFTFALT6	SFTFALT5	SFTFALT4	SFTFALT3	SFTFALT2	SFTFALT1
										rt_w	rt_w	rt_w	rt_w	rt_w	rt_w

Bit Field	Name	Description
[31:6]	Reserved	Reserved, the reset value must be maintained
[5]	SFTFALT6	Soft fault 6 1: This bit is only set by software. If the fault is enabled, writing a 1 to this register will cause a software fault. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bit of both channels corresponding to the given timer output channel is set, this bit is cleared by hardware.
[4]	SFTFALT5	Soft fault 5 1: This bit is only set by software. If the fault is enabled, writing a 1 to this register will cause a software fault. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bit of both channels corresponding to the given timer output channel is set, this bit is cleared by hardware.
[3]	SFTFALT4	Soft fault 4 1: This bit is only set by software. If the fault is enabled, writing a 1 to this register will cause a software fault. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bit of both channels corresponding to the given timer output channel is set, this bit is cleared by hardware.

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[2]	SFTFALT3	Soft fault 3 1: This bit is only set by software. If the fault is enabled, writing a 1 to this register will cause a software fault. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bit of both channels corresponding to the given timer output channel is set, this bit is cleared by hardware.
[1]	SFTFALT2	Soft fault 2 1: This bit is only set by software. If the fault is enabled, writing a 1 to this register will cause a software fault. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bit of both channels corresponding to the given timer output channel is set, this bit is cleared by hardware.
[0]	SFTFALT1	Soft fault 1 1: This bit is only set by software. If the fault is enabled, writing a 1 to this register will cause a software fault. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bit of both channels corresponding to the given timer output channel is set, this bit is cleared by hardware.

17.3.96 SHRTIM Software Delay Protection Register (SHRTIM_SFTDP)

Address offset: 0x42C

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SFTDPF2	SFTDPE2	SFTDPD2	SFTDPC2	SFTDPB2	SFTDPA2	SFTDPF1	SFTDPE1	SFTDPD1	SFTDPC1	SFTDPB1	SFTDPA1
				rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w	rt_w

Bit Field	Name	Description
[31:12]	Reserved	Reserved, the reset value must be maintained
[11]	SFTDPF2	Software delay protection for timer F channel 2 1: This bit is only set by software. If the delayed/balanced idle mode of timer F channel 2 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[10]	SFTDPE2	Software delay protection for timer E channel 2 1: This bit is only set by software. If the delayed/balanced idle mode of timer

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		E channel 2 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[9]	SFTDPD2	Software delay protection for timer D channel 2 1: This bit is only set by software. If the delayed/balanced idle mode of timer D channel 2 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[8]	SFTDPC2	Software delay protection for timer C channel 2 1: This bit is only set by software. If the delayed/balanced idle mode of timer C channel 2 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[7]	SFTDPB2	Software delay protection for timer B channel 2 1: This bit is only set by software. If the delayed/balanced idle mode of timer B channel 2 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[6]	SFTDPA2	Software delay protection for timer A channel 2 1: This bit is only set by software. If the delayed/balanced idle mode of timer A channel 2 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[5]	SFTDPF1	Software delay protection for timer F channel 1 1: This bit is only set by software. If the delayed/balanced idle mode of timer F channel 1 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[4]	SFTDPE1	Software delay protection for timer E channel 1 1: This bit is only set by software. If the delayed/balanced idle mode of timer E channel 1 is enabled, writing a 1 to this register will cause the delayed/

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		balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[3]	SFTDPD1	Software delay protection for timer D channel 1 1: This bit is only set by software. If the delayed/balanced idle mode of timer D channel 1 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[2]	SFTDPC1	Software delay protection for timer C channel 1 1: This bit is only set by software. If the delayed/balanced idle mode of timer C channel 1 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[1]	SFTDPB1	Software delay protection for timer B channel 1 1: This bit is only set by software. If the delayed/balanced idle mode of timer B channel 1 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.
[0]	SFTDPA1	Software delay protection for timer A channel 1 1: This bit is only set by software. If the delayed/balanced idle mode of timer A channel 1 is enabled, writing a 1 to this register will cause the delayed/ balanced idle mode entry. 0: Writing a 0 to this bit has no effect. When the SHRTIM_OEN.TxyOEN bits of both channels corresponding to the given timer output channel are set, this bit is cleared by hardware.

17.3.97 SHRTIM Fault Input Register 5 (SHRTIM_FALTIN5)

Address offset: 0x430

Reset value: 0x00000000.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									FALT6CSEL			Reserved	FALT5CSEL		
										rw				rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	FALT4CSEL			Reserved	FALT3SEL			Reserved	FALT2SEL			Reserved	FALT1SEL		

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rw rw rw rw

Bit Field	Name	Description
[31:23]	Reserved	Reserved, the reset value must be maintained
[22:20]	FALT6CSEL	Fault 6 analog comparator select Refer to the FALT1CSEL[2:0] description.
[19]	Reserved	Reserved, the reset value must be maintained
[18:16]	FALT5CSEL	Fault 5 analog comparator select Refer to the FALT1CSEL[2:0] description.
[15]	Reserved	Reserved, the reset value must be maintained
[14:12]	FALT4CSEL	Fault 4 analog comparator select Refer to the FALT1CSEL[2:0] description.
[11]	Reserved	Reserved, the reset value must be maintained
[10:8]	FALT3CSEL	Fault 3 analog comparator select Refer to the FALT1CSEL[2:0] description.
[7]	Reserved	Reserved, the reset value must be maintained
[6:4]	FALT2CSEL	Fault 2 analog comparator select Refer to the FALT1CSEL[2:0] description.
[3]	Reserved	Reserved, the reset value must be maintained
[2:0]	FALT1CSEL	Fault 1 analog comparator select This bit can be locked by FALT1LCK 000: FAULT1 analog comparator input comes from comp1 out. 001: FAULT1 analog comparator input comes from comp2 out 010: FAULT1 analog comparator input comes from comp3 out 011: FAULT1 analog comparator input comes from comp4 out 100: FAULT1 analog comparator input comes from comp5 out 101: FAULT1 analog comparator input comes from comp6 out 110: FAULT1 analog comparator input comes from comp7 out Other: Reserved

17.3.98 SHRTIM External Event Control Register 5 (SHRTIM_EXEVCTRL5)

Address offset: 0x434

Reset value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		EXEV10CSEL			EXEV9CSEL			EXEV8CSEL			EXEV7CSEL			EXEV6CSEL	
		rw			rw			rw			rw			rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EXEV5CSEL			EXEV4CSEL			EXEV3CSEL			EXEV2CSEL			EXEV1CSEL		
rw	rw			rw			rw			rw			rw		

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Bit Field	Name	Description
[31:30]	Reserved	Reserved, the reset value must be maintained
[29:27]	EXEV10CSEL	External event 10's analog comparator select Refer to the EXEV1CSEL description.
[26:24]	EXEV9CSEL	External event 9's analog comparator select Refer to the EXEV1CSEL description.
[23:21]	EXEV8CSEL	External event 8's analog comparator select Refer to the EXEV1CSEL description.
[20:18]	EXEV7CSEL	External event 7's analog comparator select Refer to the EXEV1CSEL description.
[17:15]	EXEV6CSEL	External event 6's analog comparator select Refer to the EXEV1CSEL description.
[14:12]	EXEV5CSEL	External event 5's analog comparator select Refer to the EXEV1CSEL description.
[11:9]	EXEV4CSEL	External event 4's analog comparator select Refer to the EXEV1CSEL description.
[8:6]	EXEV3CSEL	External event 3's analog comparator select Refer to the EXEV1CSEL description.
[5:3]	EXEV2CSEL	External event 2's analog comparator select Refer to the EXEV1CSEL description.
[2:0]	EXEV1CSEL	External event 1's analog comparator select 000: External event 1's analog comparator input comes from comp1 out 001: External event 1's analog comparator input comes from comp2 out 010: External event 1's analog comparator input comes from comp3 out 011: External event 1's analog comparator input comes from comp4 out 100: External event 1's analog comparator input comes from comp5 out 101: External event 1's analog comparator input comes from comp6 out 110: External event 1's analog comparator input comes from comp7 out Other: Reserved

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18 Advanced-control Timers(ATIM1/ ATIM2/ ATIM3/ ATIM4)

18.1 ATIMx（x=1-4）Introduction

The advanced control timers are mainly used in the following scenarios: counting the input signals, measuring the pulse width of the input signals and generating the output waveforms, etc.

Advanced-control timers have complementary output function with dead-time insertion and break function, which are suitable for motor control.

18.1 ATIMx（x=1-4）Main Features

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- Up to 9 channels
- 4 capture/compare channels, the operating modes are PWM output, ouput compare, one-pulse mode output, input capture
- 2 break input signals with digital filter
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break signal input
- Complementary outputs with programmable dead-time
  - Channel 1,2,3,4 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Trigger input for external clock or cycle-by-cycle current management

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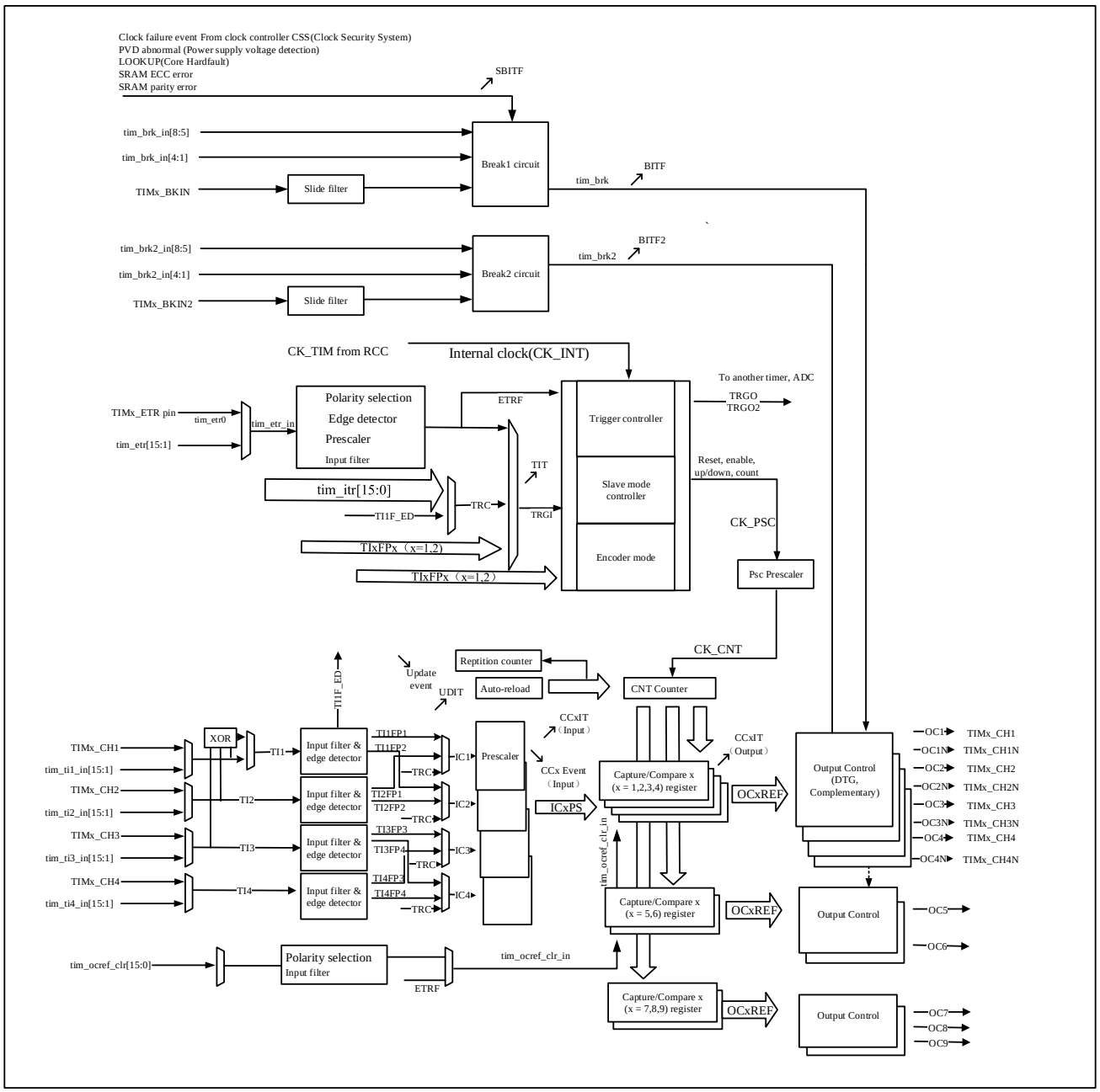
18.2 ATIMx（x=1-4）Block Diagram

Figure 18-1 Block Diagram of ATIMx



18.3 ATIMx(x=1-4)Pins and Internal Signals

The following table describes the input and output pins and internal signals of ATIMx.

Table 18-1 ATIMx Input/Output Pins

Pin Name	Type	Description

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TIMx_CH1 TIMx_CH2 TIMx_CH3 TIMx_CH4	Input/Output	Each channel can be used for capture, compare or PWM. TIM_CH1 and TIM_CH2 can also be used as external clock (below 1/4 of the tim_ker_ck clock), external trigger and quadrature encoder inputs. TIM_CH1, TIM_CH2 and TIM_CH3 can be used to interface with digital hall effect sensors.
TIM_CH1N TIM_CH2N TIM_CH3N TIM_CH4N	Output	Complementary outputs with programmable dead-time insertion
TIMx_ETR	Input	External trigger input. This input can be used as external trigger or as external clock source. This input can receive a clock with a frequency higher than the tim_ker_ck if the tim_etr_in prescaler is used.
TIMx_BKIN TIMx_BKIN2	Input/Output	Break and Break2 inputs. Both inputs can be configured in bidirectional mode.

Table 18-2 ATIMx Internal Input/Output Signals

Internal Signals	Type	Description
tim_ti1_in[15:0] tim_ti2_in[15:0] tim_ti3_in[15:0] tim_ti4_in[15:0]	Input	Channels 1/2/3/4 input signals. tim_ti1_in[15:0] and tim_ti2_in[15:0] inputs can be used for capture or as an external clock (lower than 1/4 of the system clock frequency) and for quadrature encoder signals.
tim_etr[15:0]	Input	External trigger channel input signals. These inputs can be used as triggers, external clocks, or for hardware per-cycle pulse width control. If a prescaler is used, the input signal tim_etr can be a signal with a frequency higher than the system clock frequency.
tim_itr[15:0]	Input	Internal trigger input signals. These inputs can be used in mode controllers or as input clocks (lower than 1/4 of the system clock frequency).
tim_trgo/tim_trgo2	Output	Internal trigger signal output. These trigger signals can be used by other timers and/or other peripheral devices.

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18.3.1 Interconnect of the tim_ti1/ tim_ti2/ tim_ti3/ tim_ti4 Input

Table 18-3 Interconnect to tim_ti1 Input Multiplexer

tim_ti1 inputs	Sources			
	ATIM1	ATIM2	ATIM3	ATIM4
tim_ti1_in0	ATIM1_CH1	ATIM2_CH1	ATIM3_CH1	ATIM4_CH1
tim_ti1_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti1_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti1_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti1_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti1_in[15:5]	Reserved			

Table 18-4 Interconnect to tim_ti2 Input Multiplexer

tim_ti2 inputs	Sources			
	ATIM1	ATIM2	ATIM3	ATIM4
tim_ti2_in0	ATIM1_CH2	ATIM2_CH2	ATIM3_CH2	ATIM4_CH2
tim_ti2_in1	GTIMA7_OC1	GTIMA7_OC2	GTIMA7_OC3	COMP1_OUT
tim_ti2_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti2_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti2_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti2_in[15:5]	Reserved			

Table 18-5 Interconnect to tim_ti3 Input Multiplexer

tim_ti3 inputs	Sources			
	ATIM1	ATIM2	ATIM3	ATIM4
tim_ti3_in0	ATIM1_CH3	ATIM2_CH3	ATIM3_CH3	ATIM4_CH3
tim_ti3_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT

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tim_ti3_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti3_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti3_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti3_in[15:5]	Reserved			

Table 18-6 Interconnect to tim_ti4 Input Multiplexer

tim_ti4 inputs	**Sources**			
	ATIM1	**ATIM2**	**ATIM3**	**ATIM4**
tim_ti4_in0	ATIM1_CH4	ATIM2_CH4	ATIM3_CH4	ATIM4_CH4
tim_ti4_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti4_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti4_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti4_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti4_in[15:5]	Reserved			

18.3.2 Interconnect of the tim_itr Input

Table 18-7 Interconnect to tim_itr Input Multiplexer

ATIMx	**ATIM1**	**ATIM2**	**ATIM3**	**ATIM4**
tim_itr0	Reserved	ATIM1_TRGO	ATIM1_TRGO	ATIM1_TRGO
tim_itr1	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO	GTIMA1_TRGO
tim_itr2	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO	GTIMA2_TRGO
tim_itr3	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO	GTIMA3_TRGO
tim_itr4	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO	GTIMA4_TRGO
tim_itr5	ATIM2_TRGO	Reserved	ATIM2_TRGO	ATIM2_TRGO
tim_itr6	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO	GTIMA5_TRGO

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tim_itr7	ATIM3_TRGO	ATIM3_TRGO	Reserved	ATIM3_TRGO
tim_itr8	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO	GTIMA6_TRGO
tim_itr9	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO	GTIMA7_TRGO
tim_itr10	ATIM4_TRGO	ATIM4_TRGO	ATIM4_TRGO	Reserved
tim_itr11	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO	GTIMB1_TRGO
tim_itr12	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO	GTIMB2_TRGO
tim_itr13	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO	GTIMB3_TRGO
tim_itr14	SHRTIM1_OUT_ SYNC2	SHRTIM1_OUT_ SYNC2	SHRTIM1_OUT_ SYNC2	SHRTIM1_OUT_ SYNC2
tim_itr15	SHRTIM2_OUT_ SYNC2	SHRTIM2_OUT_ SYNC2	SHRTIM2_OUT_ SYNC2	SHRTIM2_OUT_ SYNC2

18.3.3 Interconnect of the tim_etr Input

Table 18-8 Interconnect to tim_etr Input Multiplexer

ATIMx	ATIM1	ATIM2	ATIM3	ATIM4
tim_etr0	ATIM1_ETR	ATIM2_ETR	ATIM3_ETR	ATIM4_ETR
tim_etr1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_etr2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_etr3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_etr4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_etr5	ADC1_AWD1	ADC1_AWD1	ADC1_AWD1	ADC1_AWD1
tim_etr6	ADC1_AWD2	ADC1_AWD2	ADC1_AWD2	ADC1_AWD2
tim_etr7	ADC1_AWD3	ADC1_AWD3	ADC1_AWD3	ADC1_AWD3
tim_etr8	ADC2_AWD1	ADC2_AWD1	ADC2_AWD1	ADC2_AWD1
tim_etr9	ADC2_AWD2	ADC2_AWD2	ADC2_AWD2	ADC2_AWD2

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tim_etr10	ADC2_AWD3	ADC2_AWD3	ADC2_AWD3	ADC2_AWD3
tim_etr11	ADC3_AWD1	ADC3_AWD1	ADC3_AWD1	ADC3_AWD1
tim_etr12	ADC3_AWD2	ADC3_AWD2	ADC3_AWD2	ADC3_AWD2
tim_etr13	ADC3_AWD3	ADC3_AWD3	ADC3_AWD3	ADC3_AWD3
tim_etr_in[15:14]	Reserved			

18.3.4 Interconnect of the tim_brk Input

Table 18-9 ATIMx Break Interconnect

tim_brk input	ATIM1	ATIM2	ATIM3	ATIM4
TIM_BKIN	ATIM1_BKIN	ATIM2_BKIN	ATIM3_BKIN	ATIM4_BKIN
tim_brk_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_brk_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_brk_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_brk_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_brk_in5	DSMU_BRK[0]	DSMU_BRK[0]	DSMU_BRK[0]	Reserved
tim_brk_in6	Reserved			
tim_brk_in7	DSMU_BRK[2]	Reserved	DSMU_BRK[2]	DSMU_BRK[2]
tim_brk_in8	Reserved			

18.3.5 Interconnect of the tim_brk2 Input

Table 18-10 ATIMx Break2 Interconnect

tim_brk input	ATIM1	ATIM2	ATIM3	ATIM4
TIM_BKIN2	ATIM1_BKIN2	ATIM2_BKIN2	ATIM3_BKIN2	ATIM4_BKIN2
tim_brk2_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_brk2_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT

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tim_brk2_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_brk2_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_brk2_in5	Reserved			
tim_brk2_in6	DSMU_BRK[1]	DSMU_BRK[1]	DSMU_BRK[1]	Reserved
tim_brk2_in7	Reserved			
tim_brk2_in8	DSMU_BRK[3]	Reserved	DSMU_BRK[3]	DSMU_BRK[3]

18.3.6 Interconnect of the tim_ocref_clr Input

Table 18-11 Interconnect to the tim_ocref_clr Input Multiplexer

OCREF CLEAR	ATIMx OCREF clear signal source			
	ATIM1	ATIM2	ATIM3	ATIM4
tim_ocref_clr0	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ocref_clr1	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ocref_clr2	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ocref_clr3	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ocref_in[15:7]	Reserved			

18.4 ATIMx(x=1-4)Function Description

18.4.1 Time-base Unit

The advanced-control timer's time-base unit mainly includes: prescaler, counter, auto-reload and repetition counter. When the time base unit is operating, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. When TIMx_CTRL1.UPDIS=0, a counter overflow/underflow or software setting TIMx_EVTGEN.UDGN will generate an update event. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

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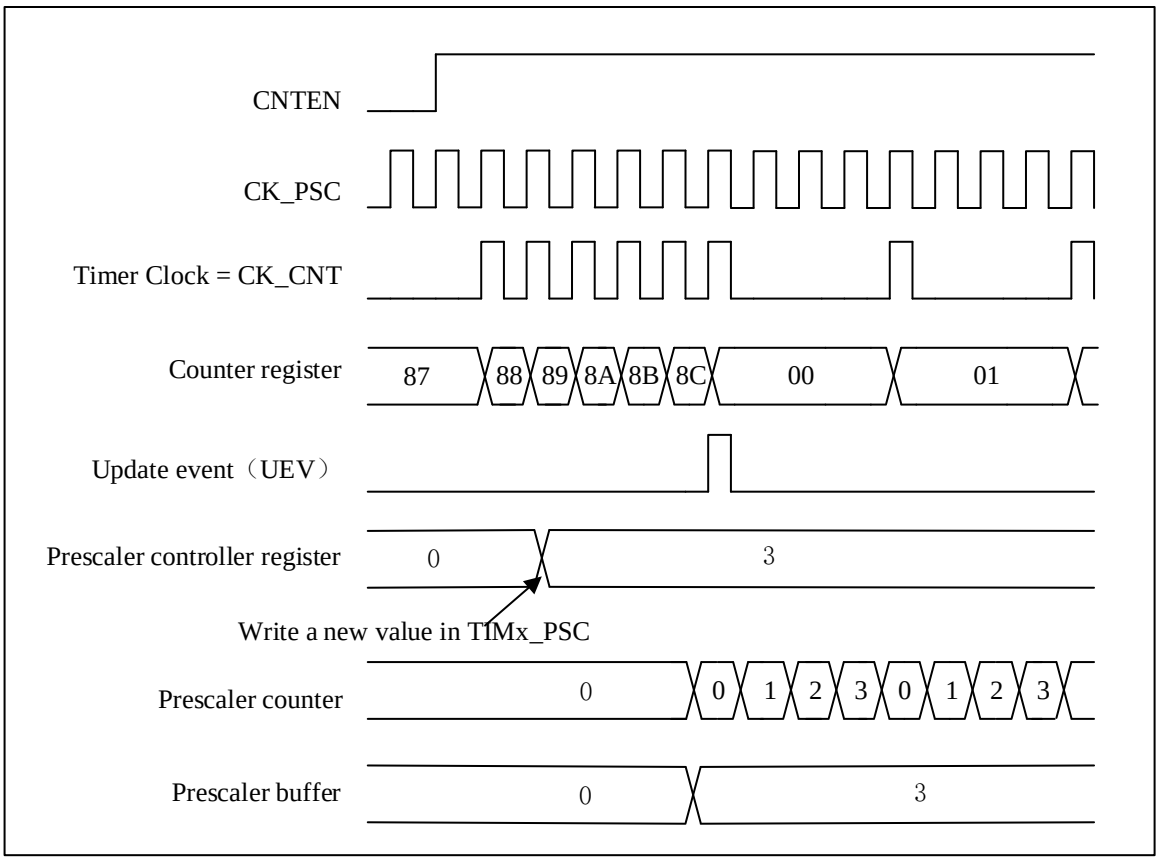
18.4.1.1 Prescaler Description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as this register is buffered. The new prescaler value is only taken into account at the next update event.

Figure 18-2 Counter Timing Diagram with Prescaler Division Change from 1 to 4



18.4.2 Counter Mode

18.4.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it restarts from 0 and a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will be generated, but the TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated.This is to avoid generating an update interrupt when clearing the counter.

Depending on the TIMx_CTRL1.UPRS, when an update event occurs, all registers are updated and the TIMx_STS.UDITF is set:

- The repetition counter reloads the contents of the TIMx_REPCNT
- The auto-reload shadow registers is updated with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

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To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update event by setting TIMx_CTRL1.UPDIS=1.

When an update event is generated, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior for different prescaler factors in the up-counting mode.

Figure 18-3 Timing Diagram of Up-Counting. The Internal Clock Divider Factor = 2/N

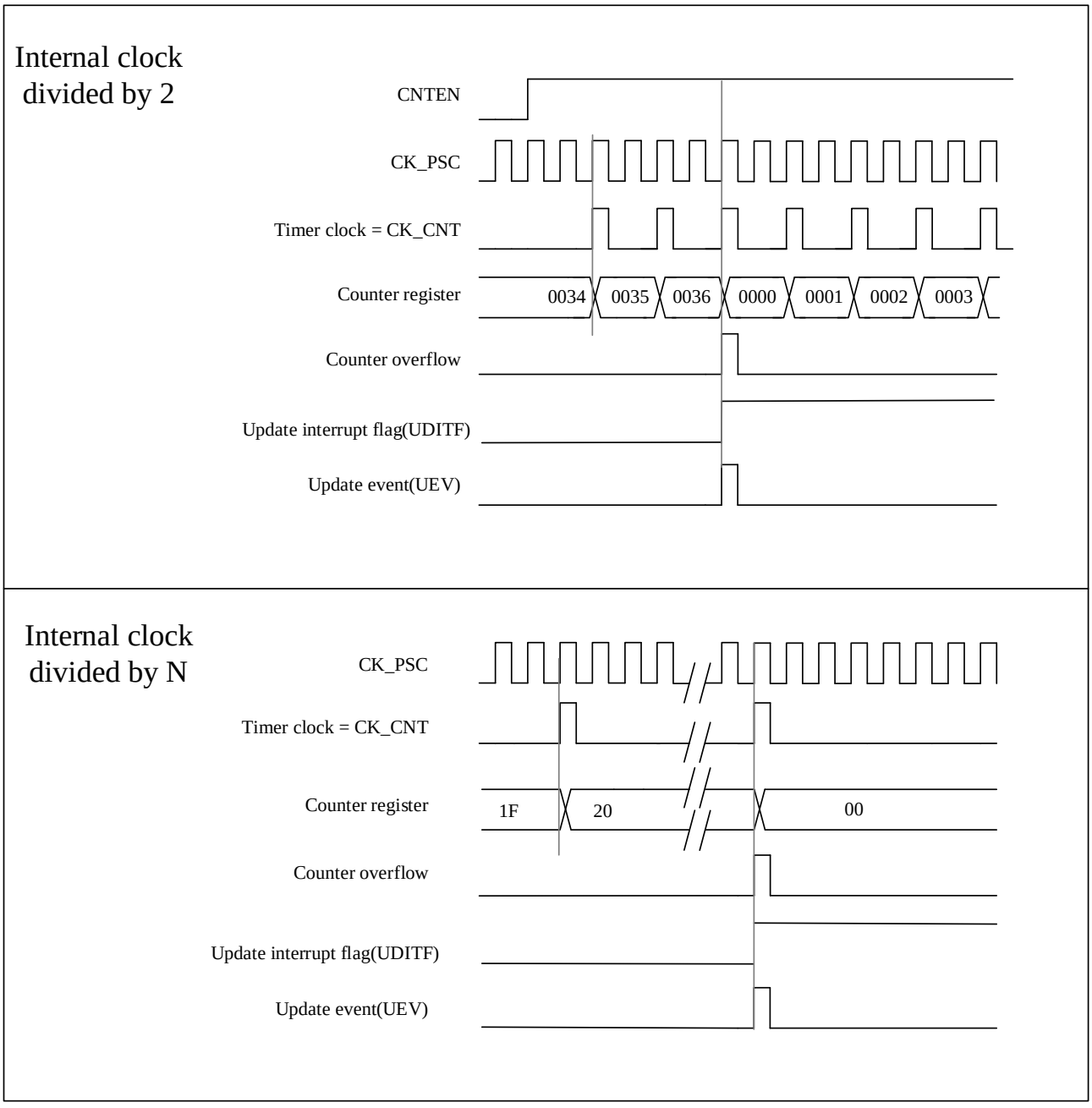

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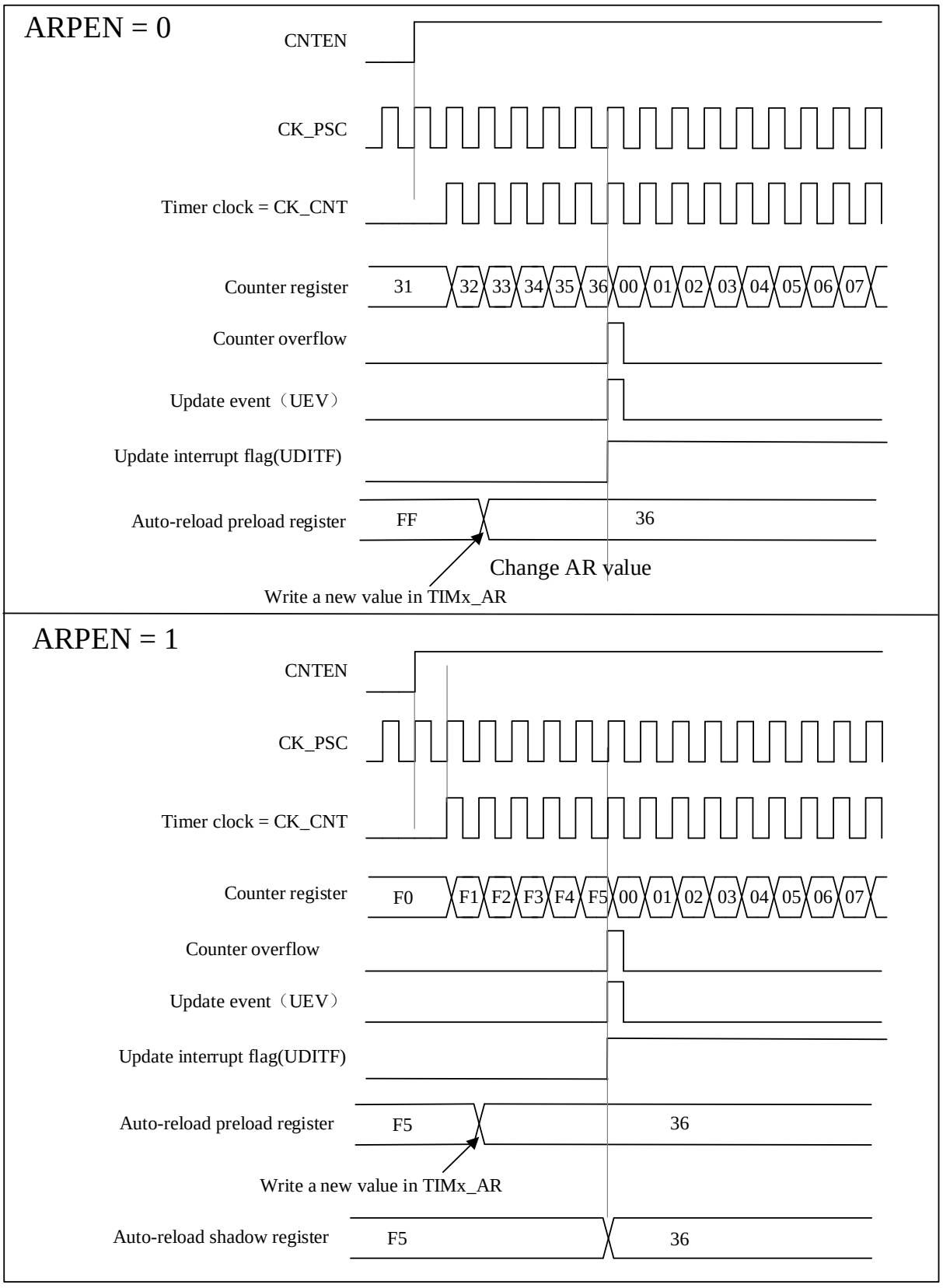
Figure 18-4 Timing Diagram of The Up-Counting, Update Event When ARPEN=0/1



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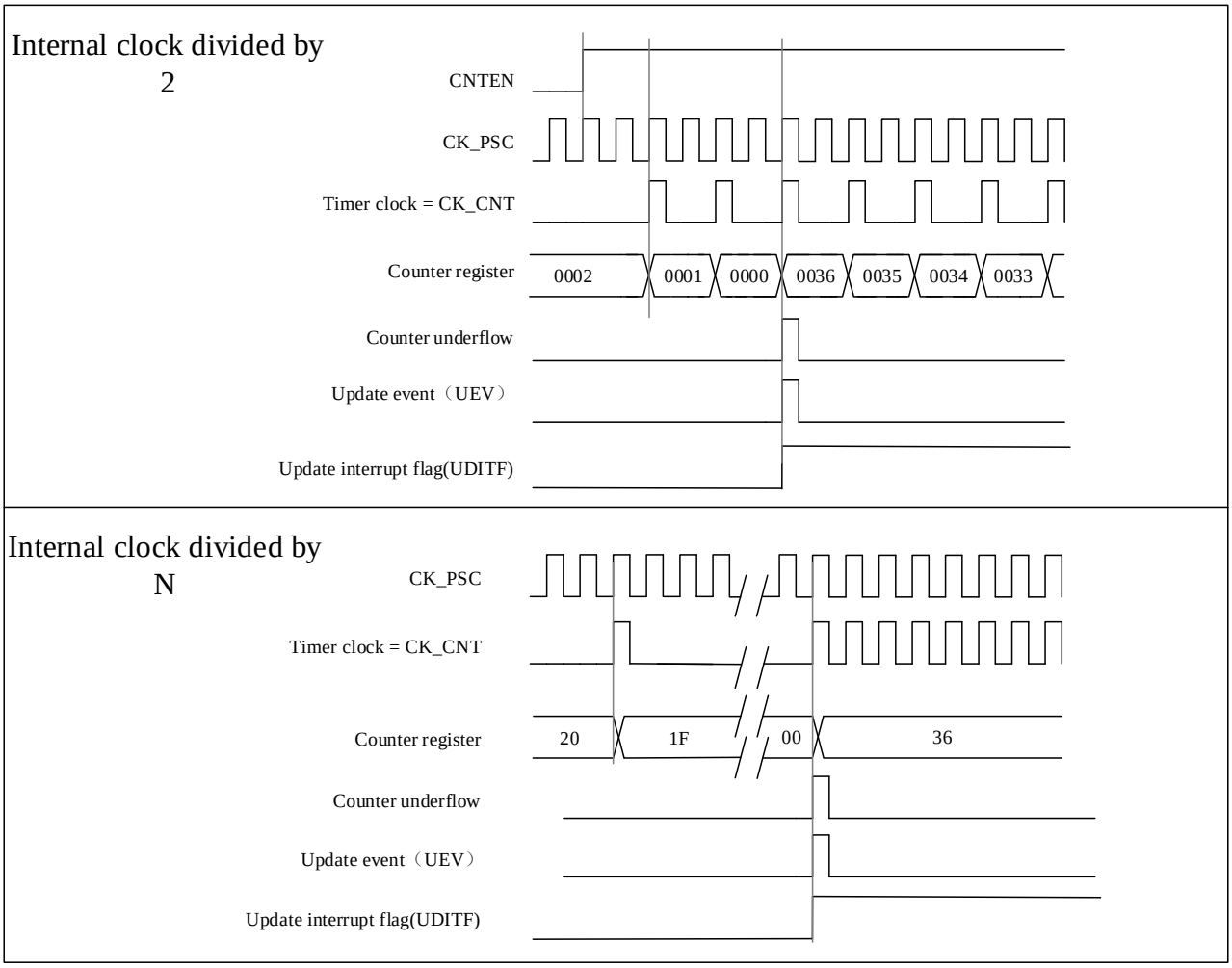
18.4.2.2 Down-counting mode

In down-counting mode, the counter will count from the value of the register TIMx_AR down to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, refer to Section18.4.2.1.

The figure below shows some examples of the counter behavior and the update flags for different prescaler factors in the down-counting mode.

Figure 18-5 Timing Diagram of The Down-Counting, Internal Clock Divided Factor = 2/N



18.4.2.3 Center-aligned mode

18.4.2.3.1 Center-aligned symmetric mode

In center-aligned symmetric mode, the counter counts from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts from the auto-reload value (TIMx_AR) down to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits cannot be written and the count direction is updated and specified by hardware. Center-aligned mode is active when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

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An update event can be generated at each counter overflows and at each counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note: if an update is generated due to a counter overflow, the auto-reload value will be updated before the counter is reload.

Figure 18-6 Timing Diagram of the Center-Aligned, Internal Clock Divided Factor =2/N

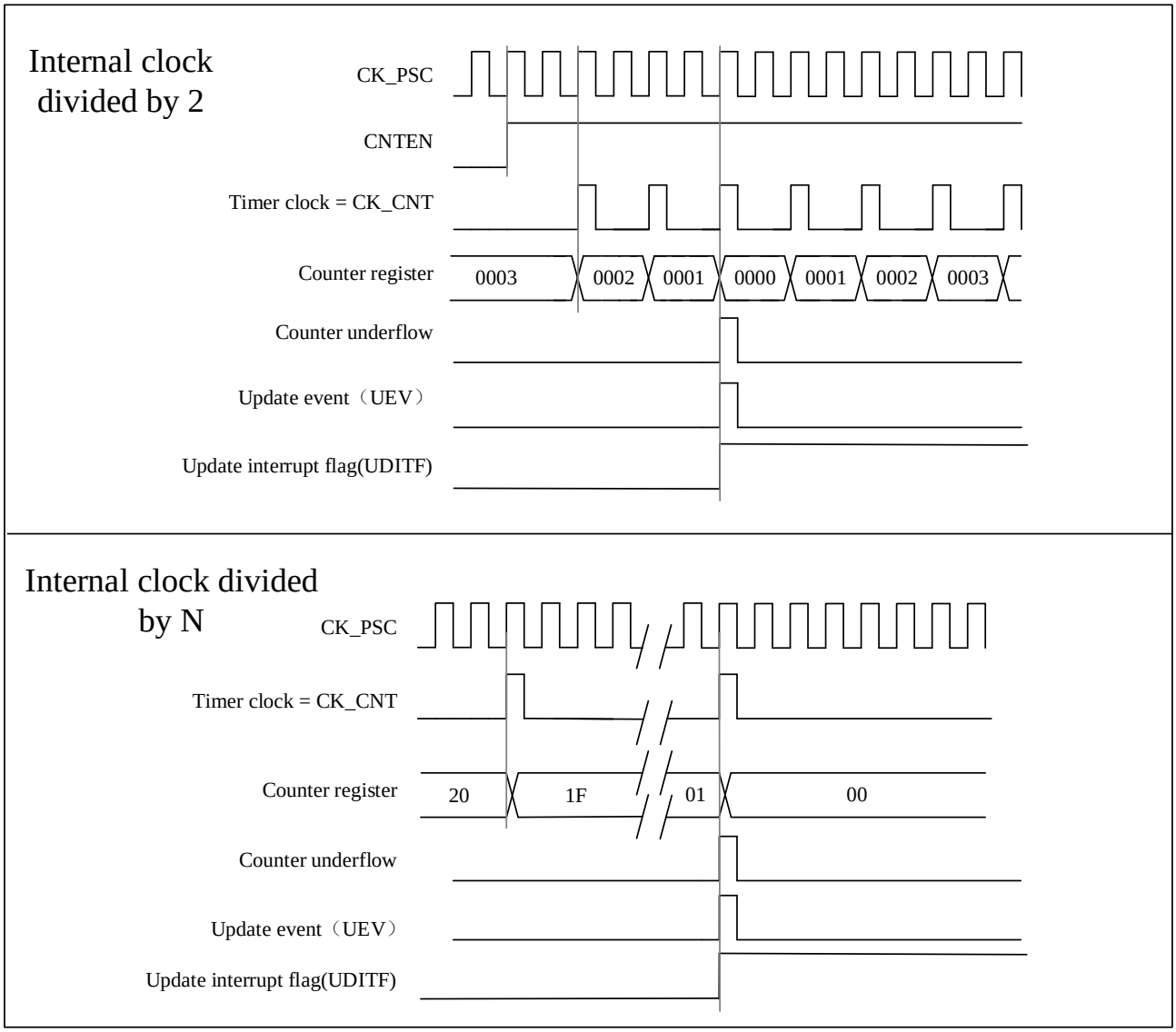

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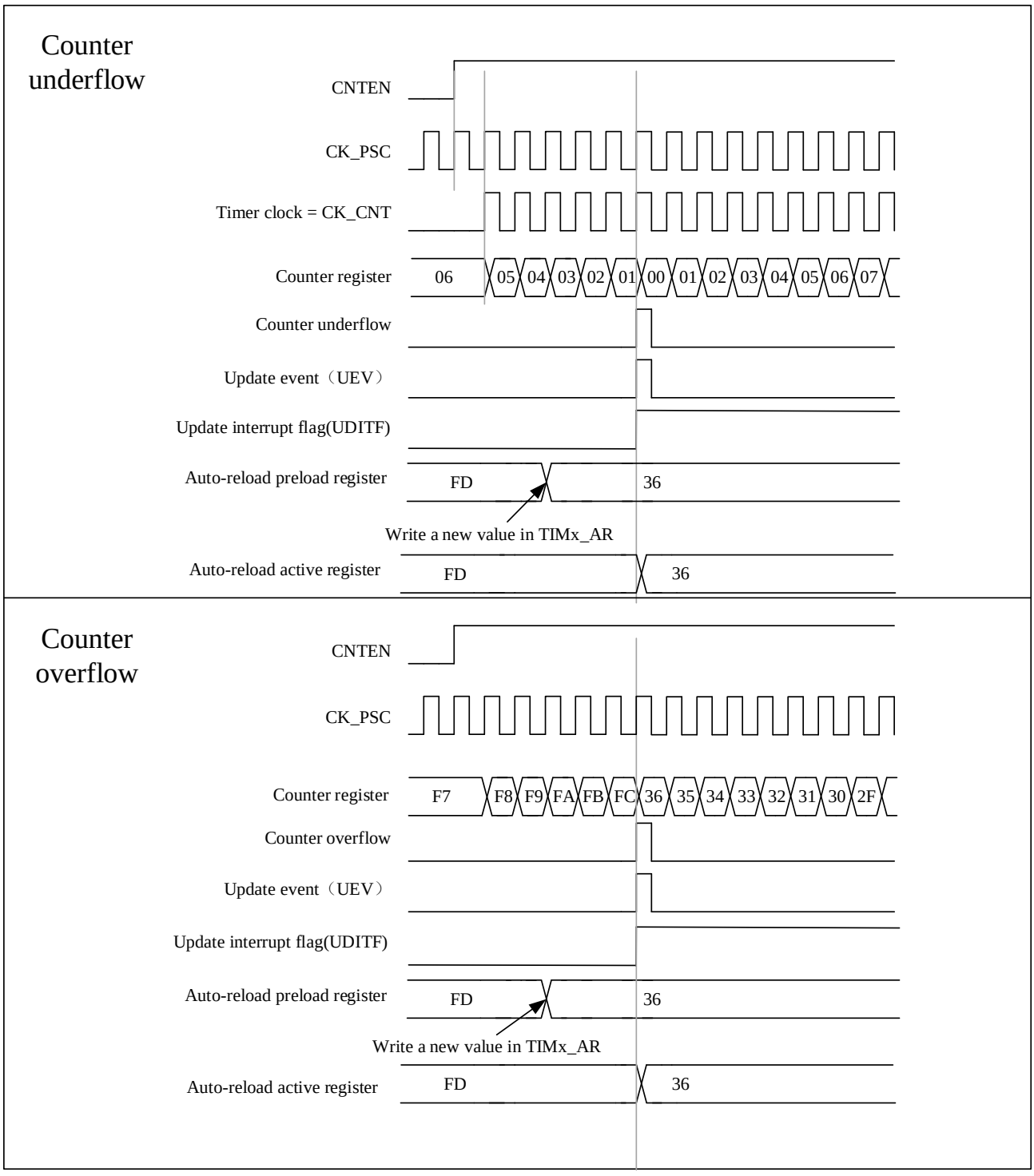
Figure 18-7 A Center-Aligned Sequence Diagram That Includes Counter Overflows and Underflows (ARPEN = 1)



18.4.2.3.2 Center-aligned asymmetric mode

In center-aligned asymmetric mode(TIMx_CTRL1. ASYMMETRIC is 1 and TIMx_CTRL1.CAMSEL[1:0] is non-zero), the counter counts from 0 to the auto-reload value (TIMx_AR) – 1 and generates a counter overflow event, then counts from the auto-reload value down to 1 and generates a counter underflow event and then restarts counting from 0.

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The TIMx_CTRL1.DIR cannot be written in this mode. It is updated by hardware and indicates the current direction of the counter.

When the channel is not 1,2,3,4, the comparison value are compared with CCDATx. When the dead time generator is turned on, note that when DIR = 0, the dead time insertion point is at which the counter value is equal to CCDATx(x=1,2,3,4), and when DIR = 1, the dead time insertion point is at which the counter value is equal to CCDDATx(x=1,2,3,4).

An update event can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, and the prescaler counter also restarts from 0.

Note: if an update is generated due to a counter overflow, the auto-reload value will be updated before the counter is reloaded.

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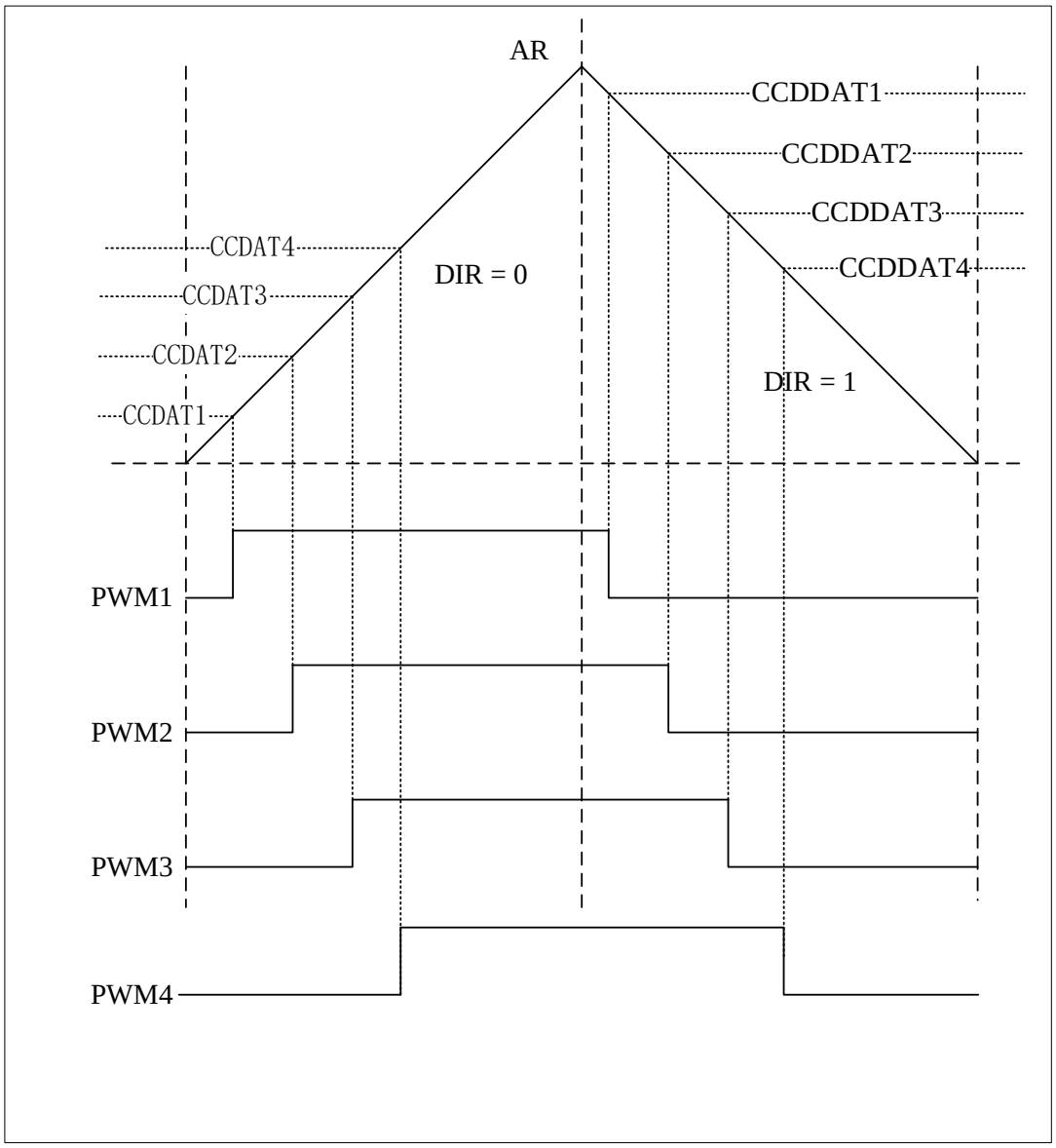
Figure 18-8 The Output Waveform Corresponding to the Asymmetric Mode



Since the triggering function of CC7/CC8/CC9 three channels is added, and the triggering function of CC4 has been modified, Here is the description of the CC4/CC7/CC8/CC9 channels triggering the ADC.

When the timer is operating in center-aligned asymmetric mode, each channel(CC4/CC7/CC8/CC9) can individually trigger the ADC only when MMSEL3 = 1.

If TIMx_CTRL1.CMODE[1:0]=00, the CCDATx.CCDAT (x=4,7,8,9) value will only trigger ADC when DIR =0.

Figure 18-9 CCDATx(x=4,7,8,9), Trigger ADC When DIR = 0

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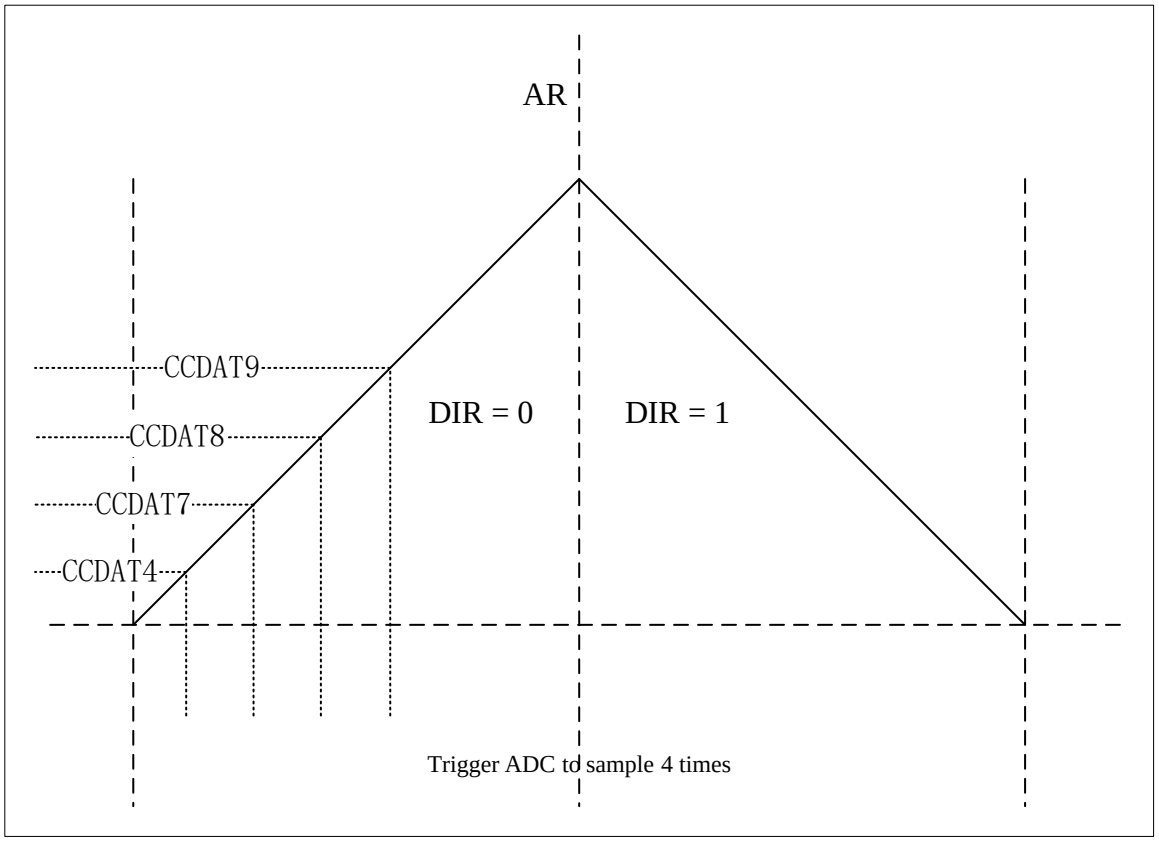

If TIMx_CTRL1.CMODE [1:0]=01, CCDATx.CCDDAT (x=4) and CCDATx.CCDAT (x=7,8,9) value will only trigger ADC when DIR =1.

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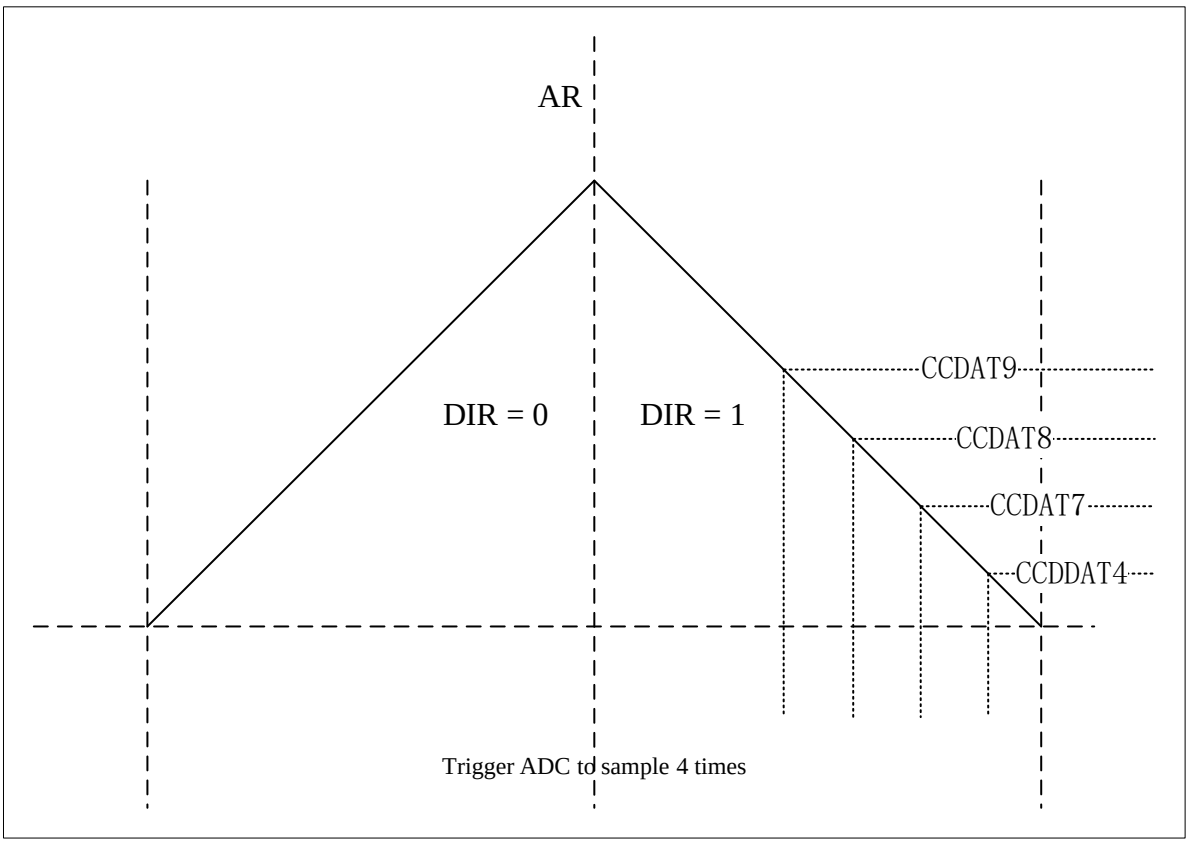
Figure 18-10 CCDATx(x=4,7,8,9),Trigger ADC When DIR = 1



If TIMx_CTRL1.CMODE[1:0]=1x, the CCDATx.CCDAT and CCDATx.CCDDAT (x=4,7,8,9) value will trigger ADC when DIR =0 or DIR=1.

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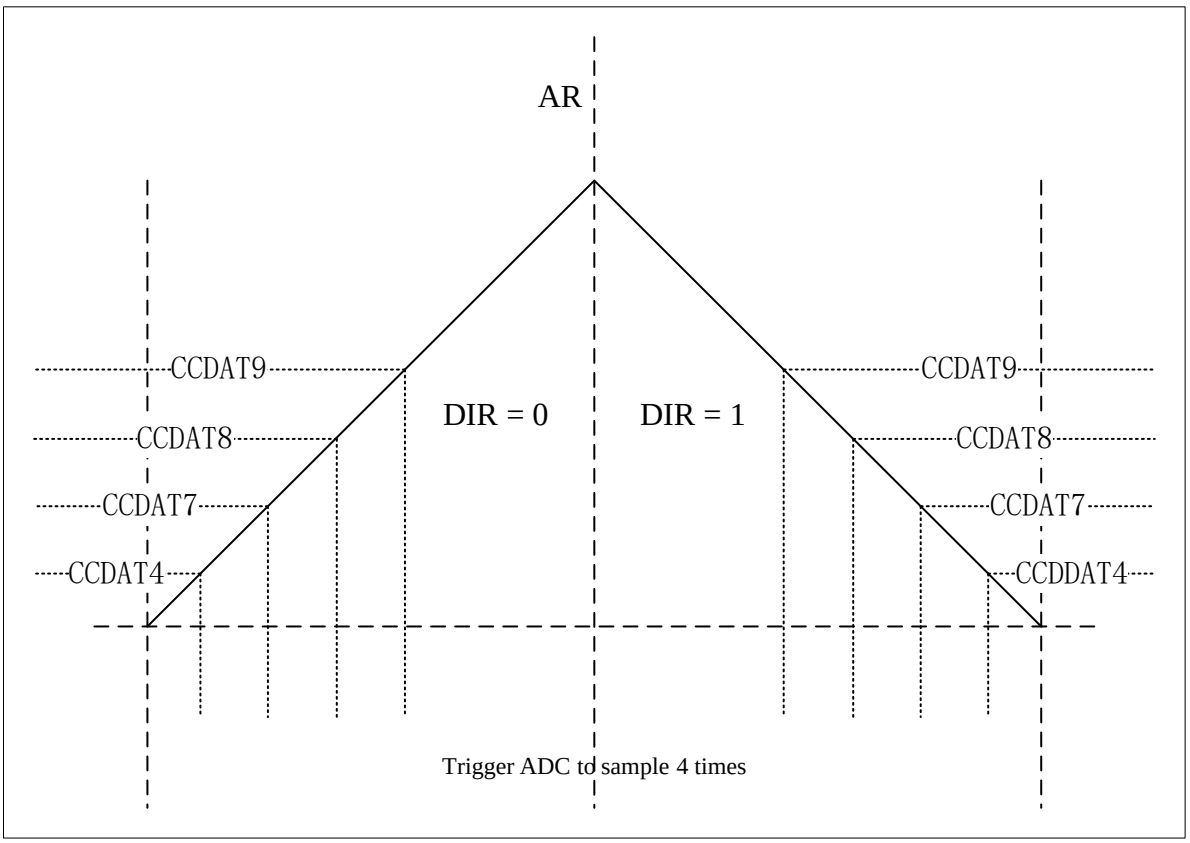
Figure 18-11 CCDATx(x=4,7,8,9), Trigger ADC When DIR = 0 or DIR = 1



In the above figure, channel 4 up counting to CCDAT4 or down counting to CCDDAT4, channel 7/8/9 up counting or down counting to CCDAT7/8/9, trigger valid.

18.4.3 Repetition Counter

The basic unit of Section 18.4.1 describes the conditions for generating an update event (UEV). An update event (UEV) is actually only generated when the repetition counter reaches zero, which is valuable for generating PWM signals.

This means that data are transferred from the preload registers to the shadow registers every N+1 counter overflow or underflow, where N is the value in the TIMx_REPCNT.

The repetition counter is decremented:

- In the up-counting mode, each time the counter reaches the maximum value, an overflow occurs.
- In down-counting mode, each time the counter decrements to the minimum value, an underflow occurs.
- In center-aligned mode, each time the counter overflows or underflows.

Its repetition rate is defined by the value of the TIMx_REPCNT register.

Repetition counters feature automatic reloading. The update event (generated by setting TIMx_EVTGEN.UDGN or hardware through slave mode controller) occurs immediately, regardless of the value of the repeatition counter.

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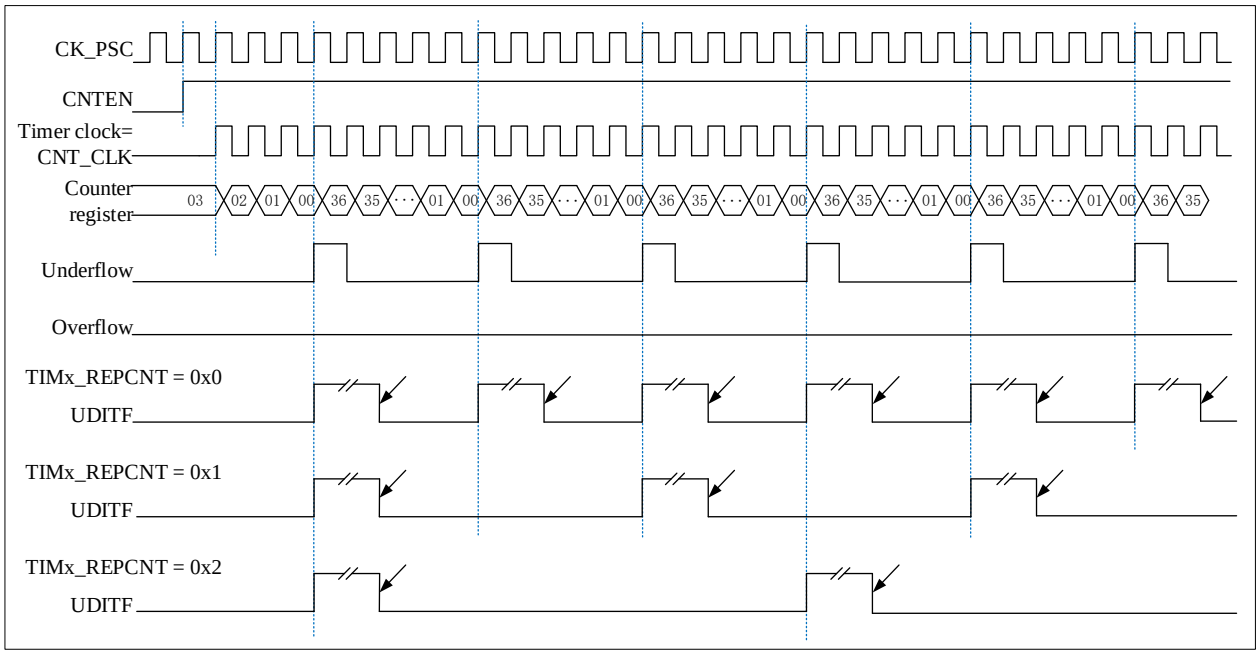
Figure 18-12 Repeat Count Sequence Diagram in Down-Counting Mode



software clear

Figure 18-13 Repeat Count Sequence Diagram in Up-Counting Mode

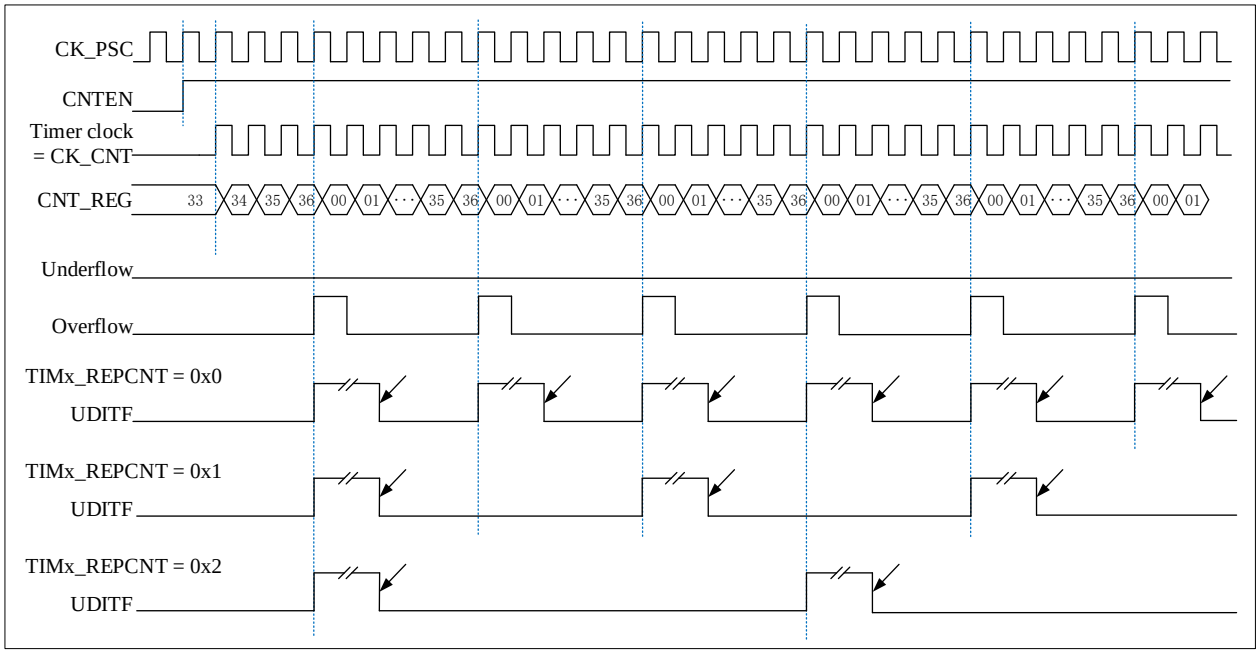


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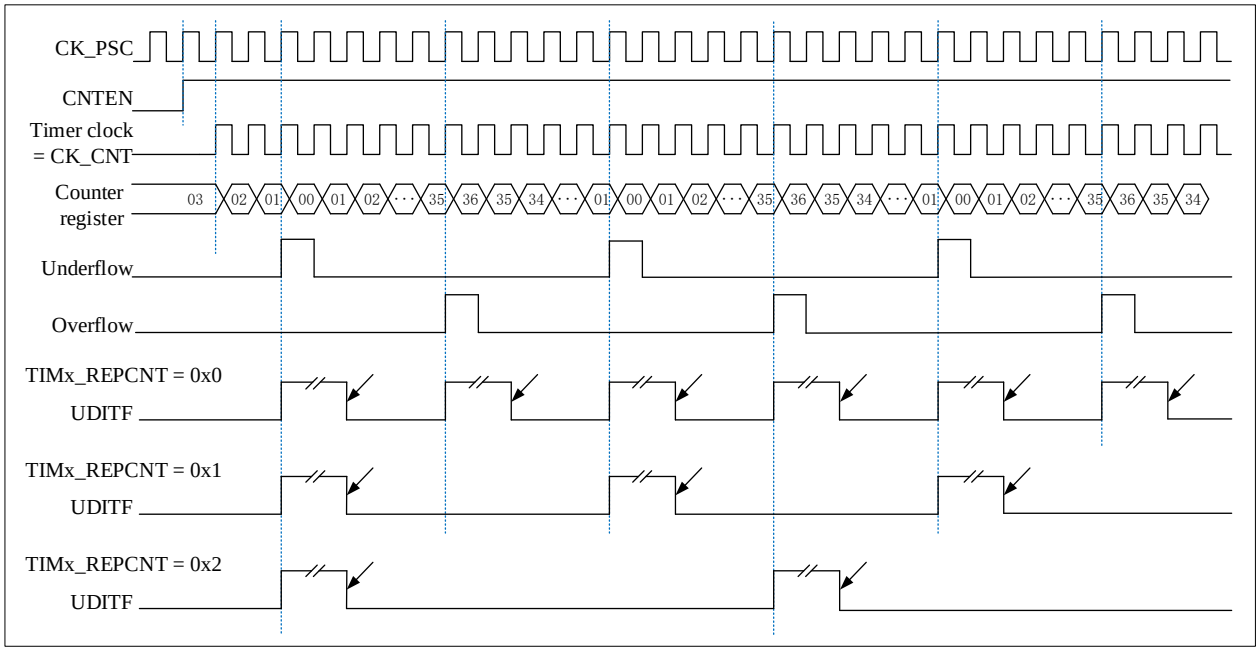
Figure 18-14 Repeat Count Sequence Diagram in Center-Aligned Mode



18.4.4 Clock Selection

- The internal clock of Advanced-control timers : CK_INT
- Two kinds of external clock mode :
  - External input pin
  - External trigger input ETR
- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

18.4.4.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as '1' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

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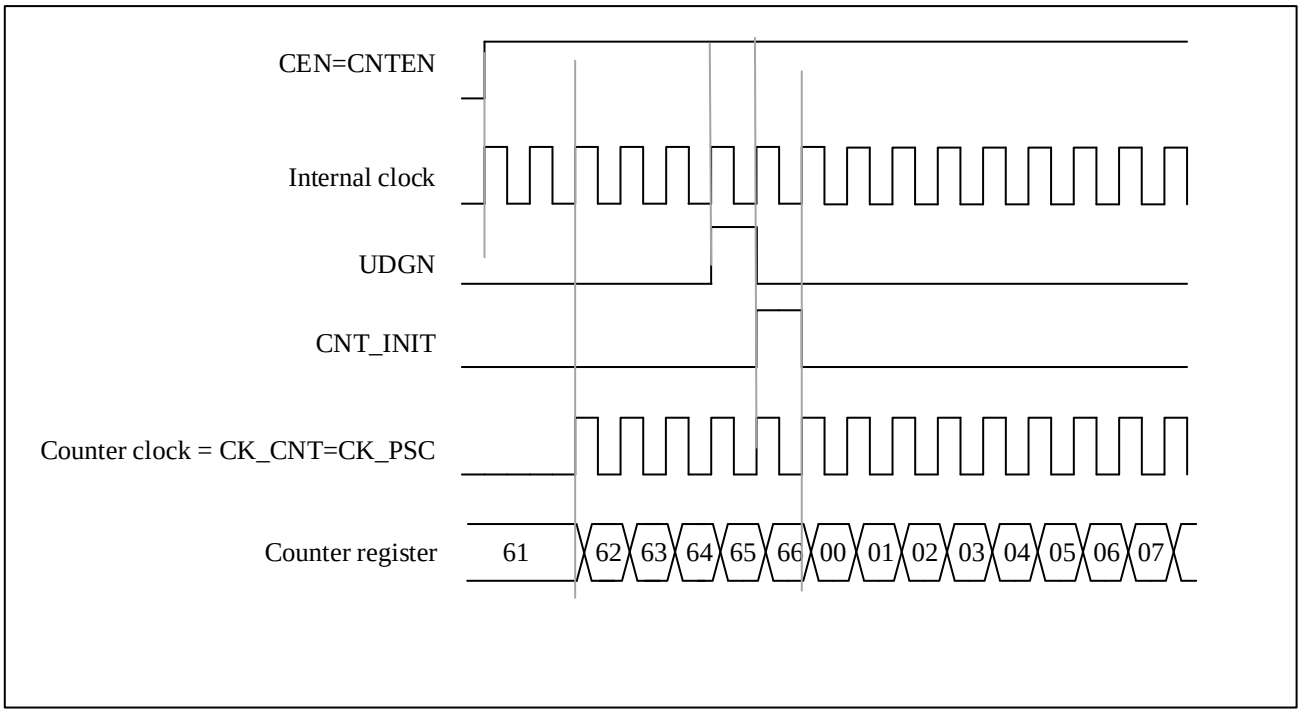
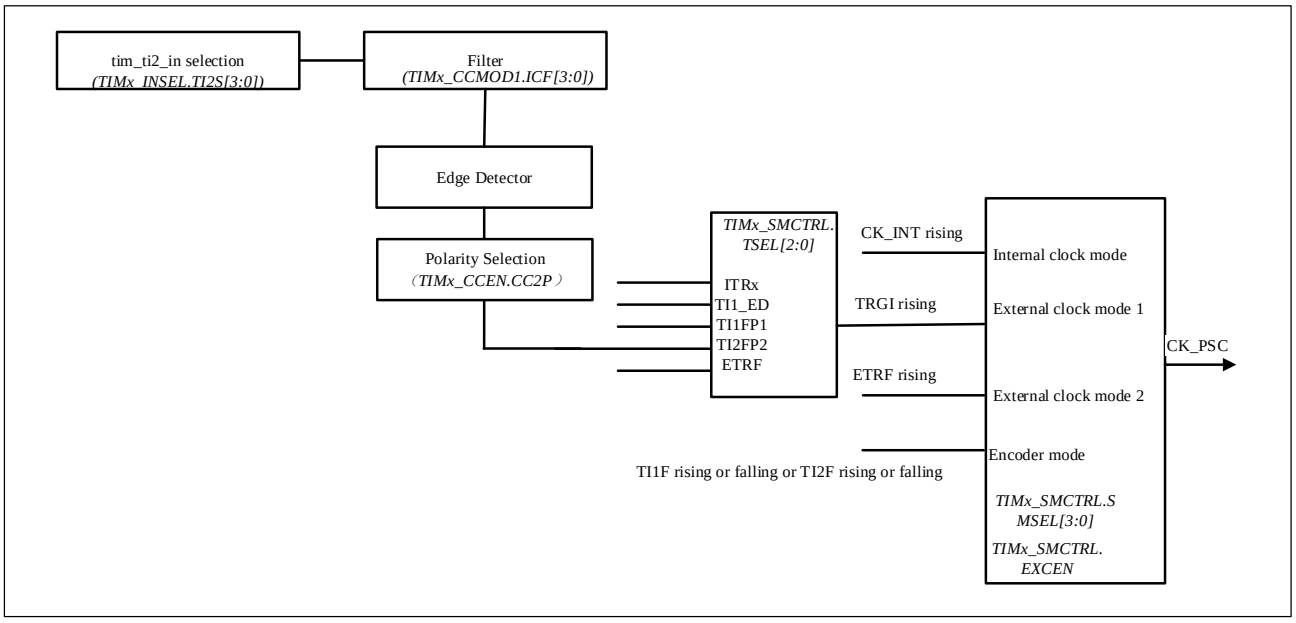
Figure 18-15 Control Circuit in Normal Mode, Internal Clock Divided by 1



18.4.4.2 External clock source mode 1

Figure 18-16 TI2 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

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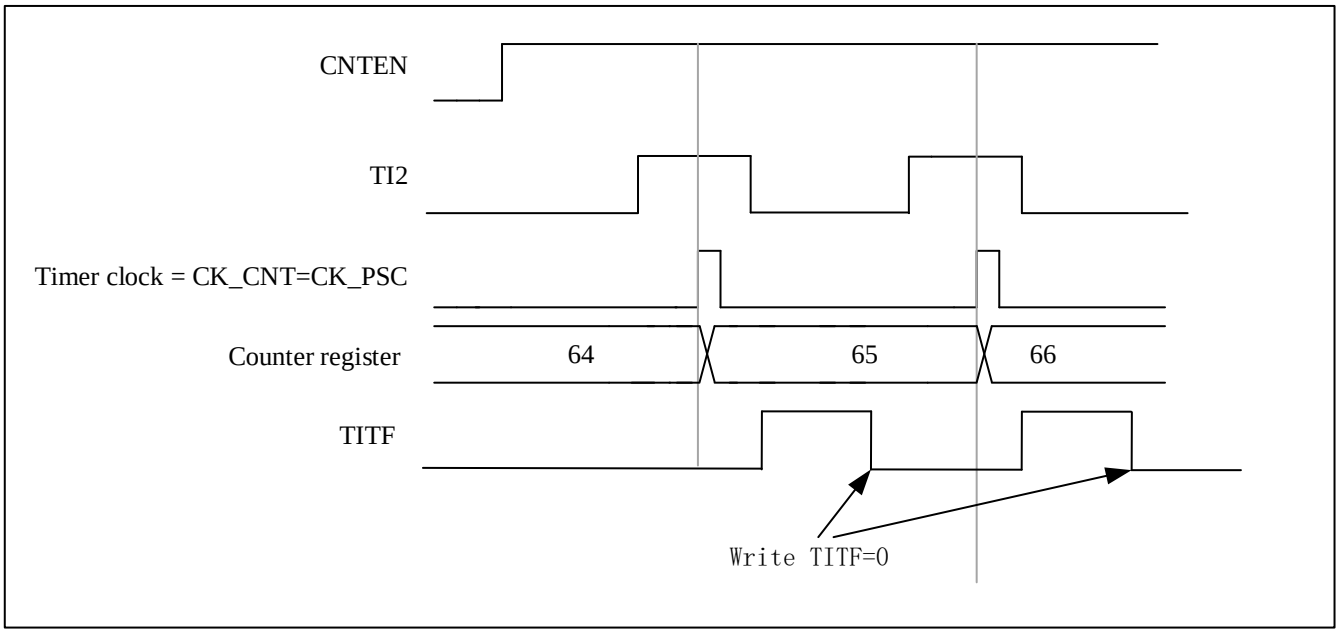
- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note: the capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is set.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

Figure 18-17 Control Circuit in External Clock Mode 1



18.4.4.3 External clock source mode 2

This mode is set by configuring TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in external clock source mode 2.

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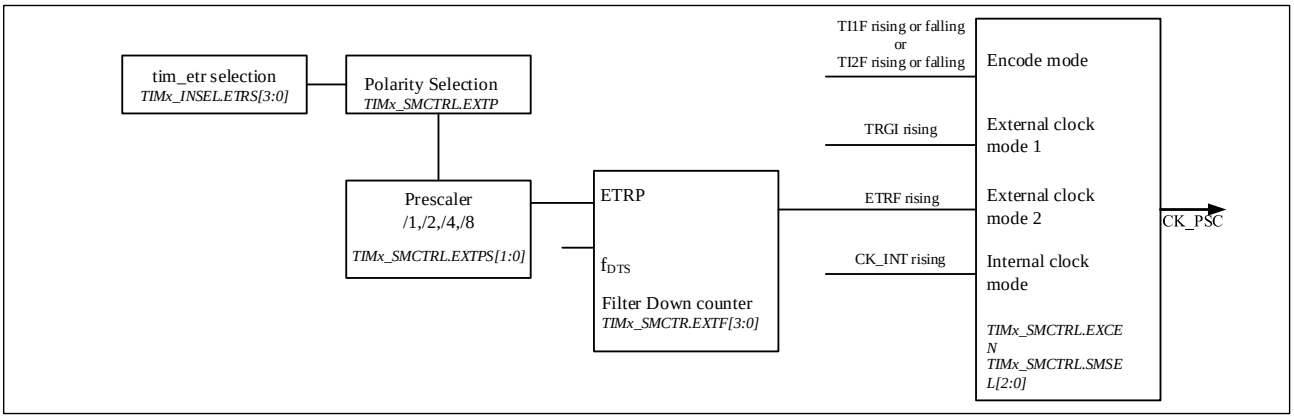
Figure 18-18 External Trigger Input Block Diagram

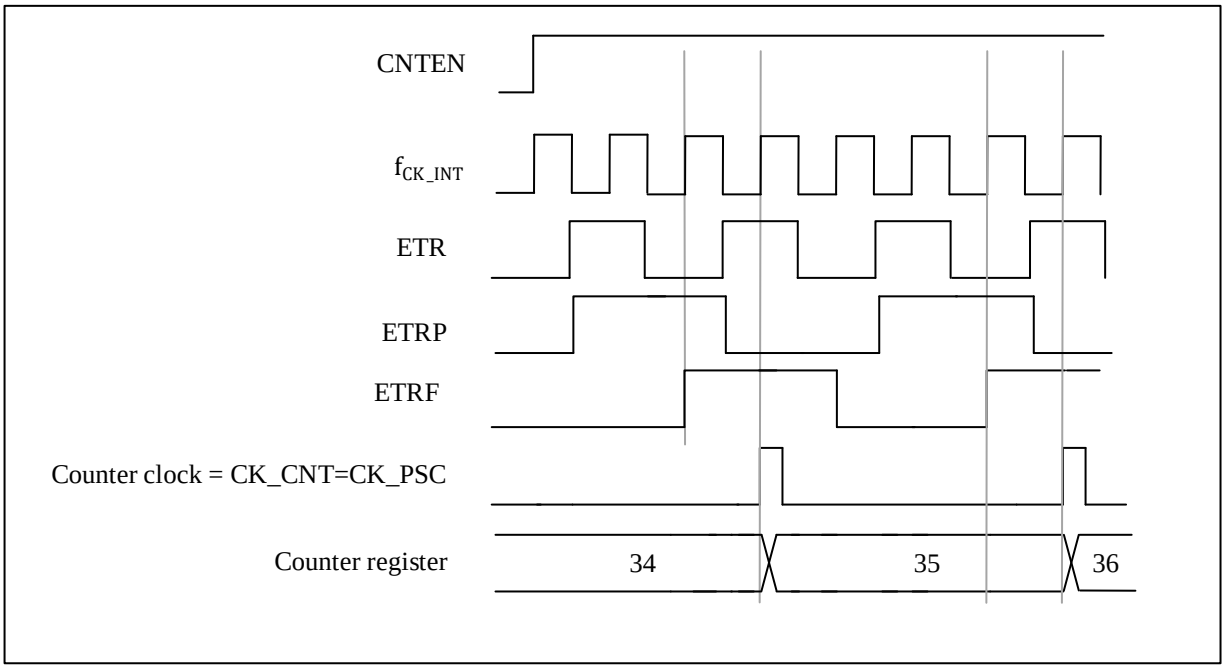


For example, use the following configuration steps to make the upcounter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', the rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock of the counter is due to a resynchronization circuit on the ETRP signal.

Figure 18-19 Control Circuit in External Clock Mode 2



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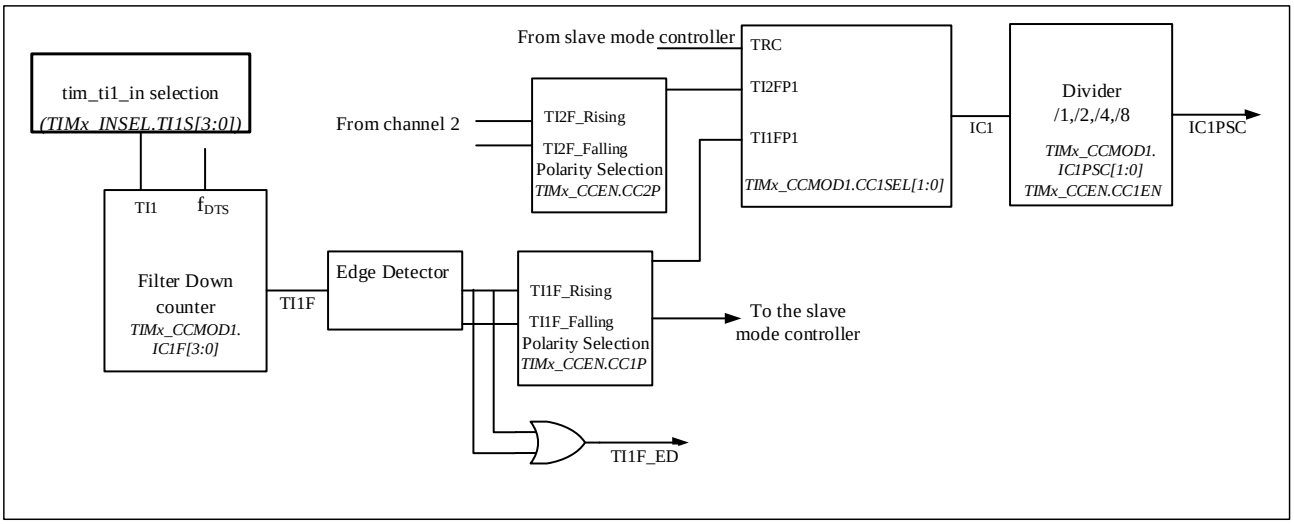
18.4.5 Capture/Compare Channels

The capture/compare channels include capture/compare registers and shadow registers. The input stage consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequencyprecaler. The following figure shows a block diagram of a capture/compare channel.

Figure 18-20 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output stage generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 18-21 Capture/Compare Channel 1 Main Circuit

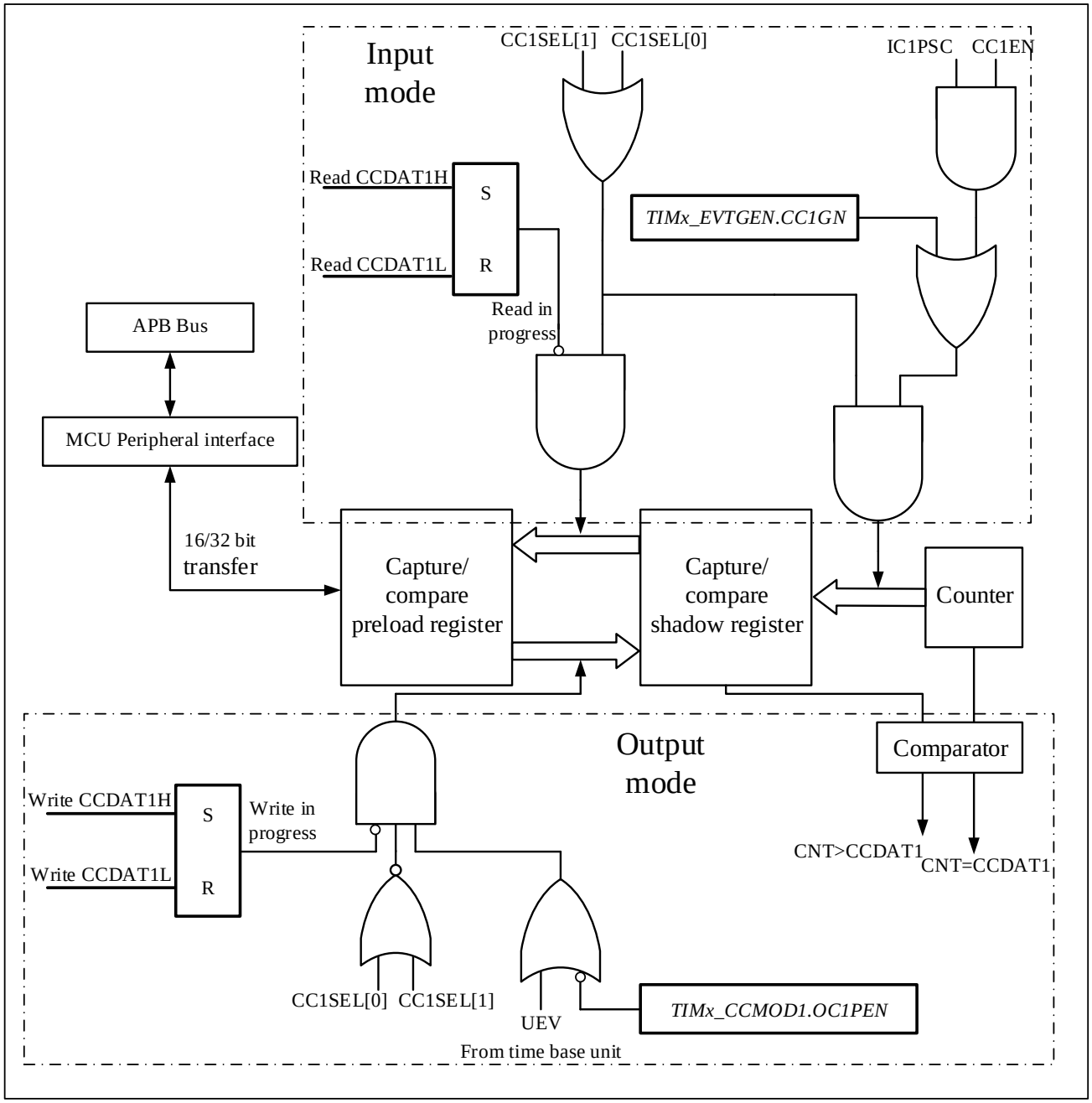

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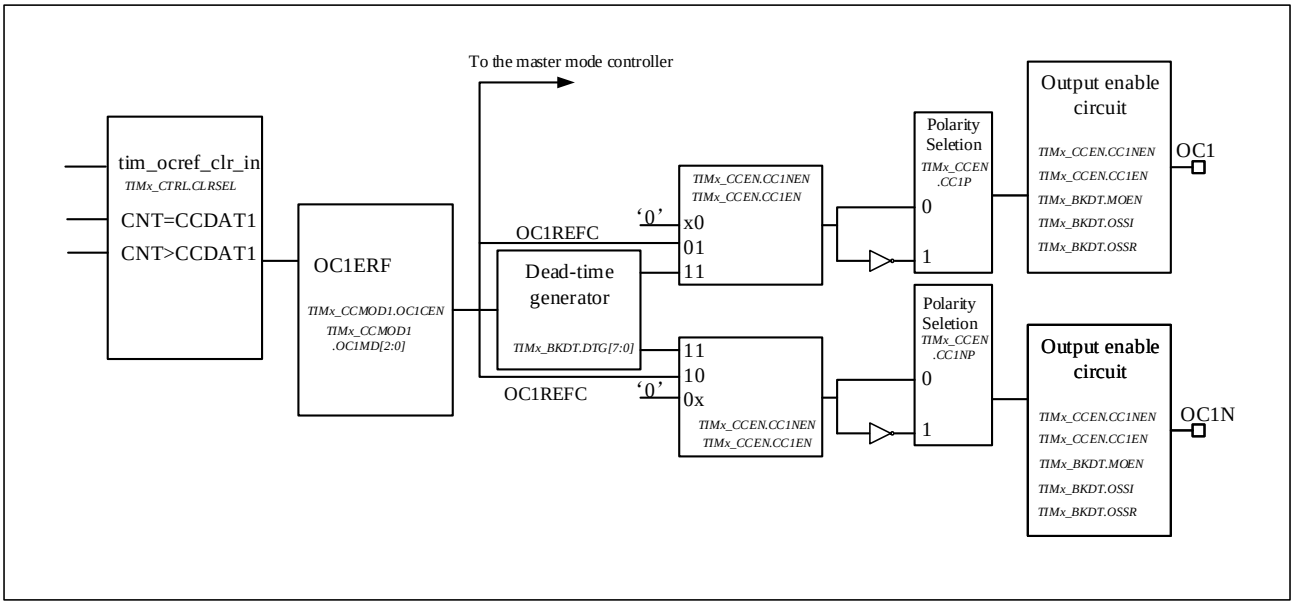
图 18-22 Output Part of Channelx (x= 1,2,3,4, Take Channel 1 as Example)



Reads and writes operations always access the preload registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

18.4.6 Input Capture Mode

In input capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can trigger an interrupt or DMA request if the corresponding interrupt enable is set.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already set. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Define the input filter duration required for programming:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the

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TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to '0011'.

- Select the rising edge as the valid transition polarity on the TI1 channel by configuring TIMx_CCEN .CC1P=0.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= '00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

18.4.7 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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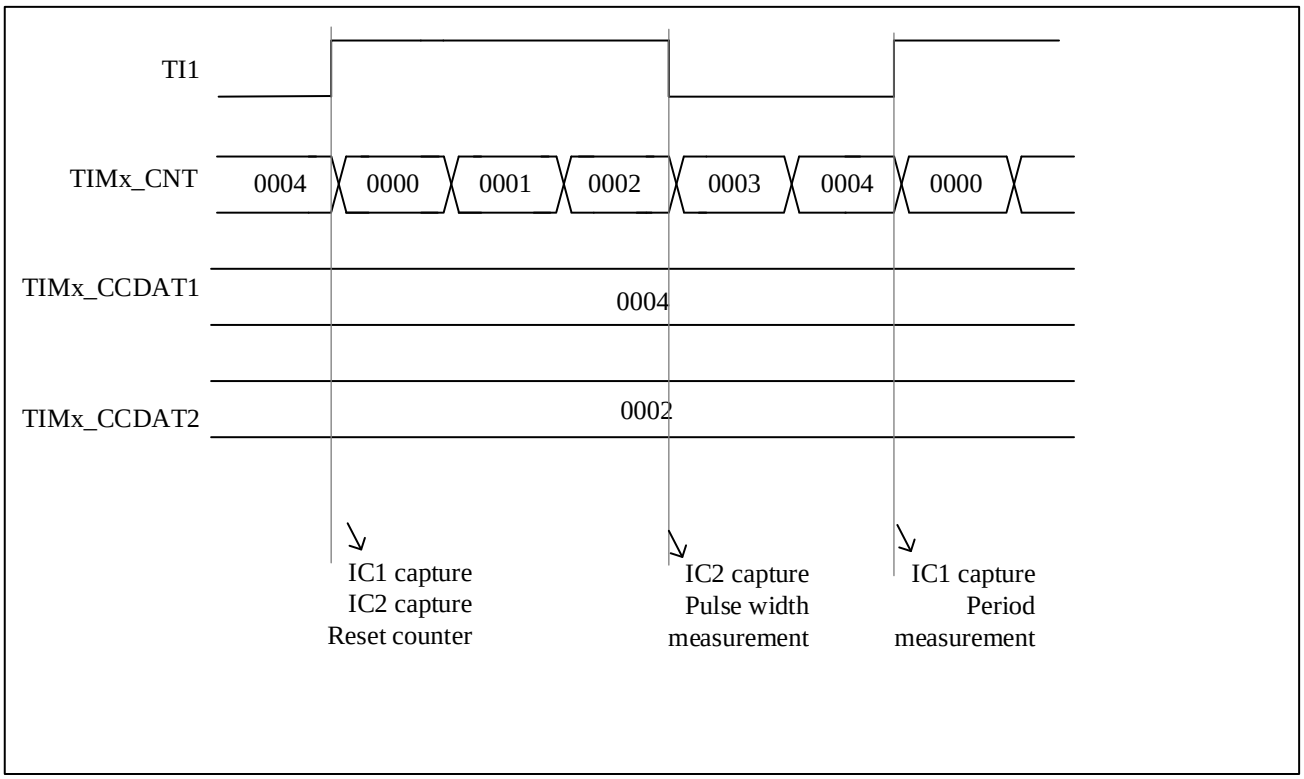
Figure 18-23 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

18.4.8 Forced Output Mode

In output mode (TIMx_CCMODx.CCxSEL=00) , software can force output compare signals to active or inactive level directly.

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to low level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

18.4.9 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set

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TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

The TIMx_CCDATx registers can be programmed with or without preload registers using the TIMx_CCMODx.OCxPEN register.

The time resolution is one count period of the counter.

In one-pulse mode, the output compare mode can also be used to output a single pulse.

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, write the desired data in the TIMx_AR and TIMx_CCDATxregisters.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by writting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

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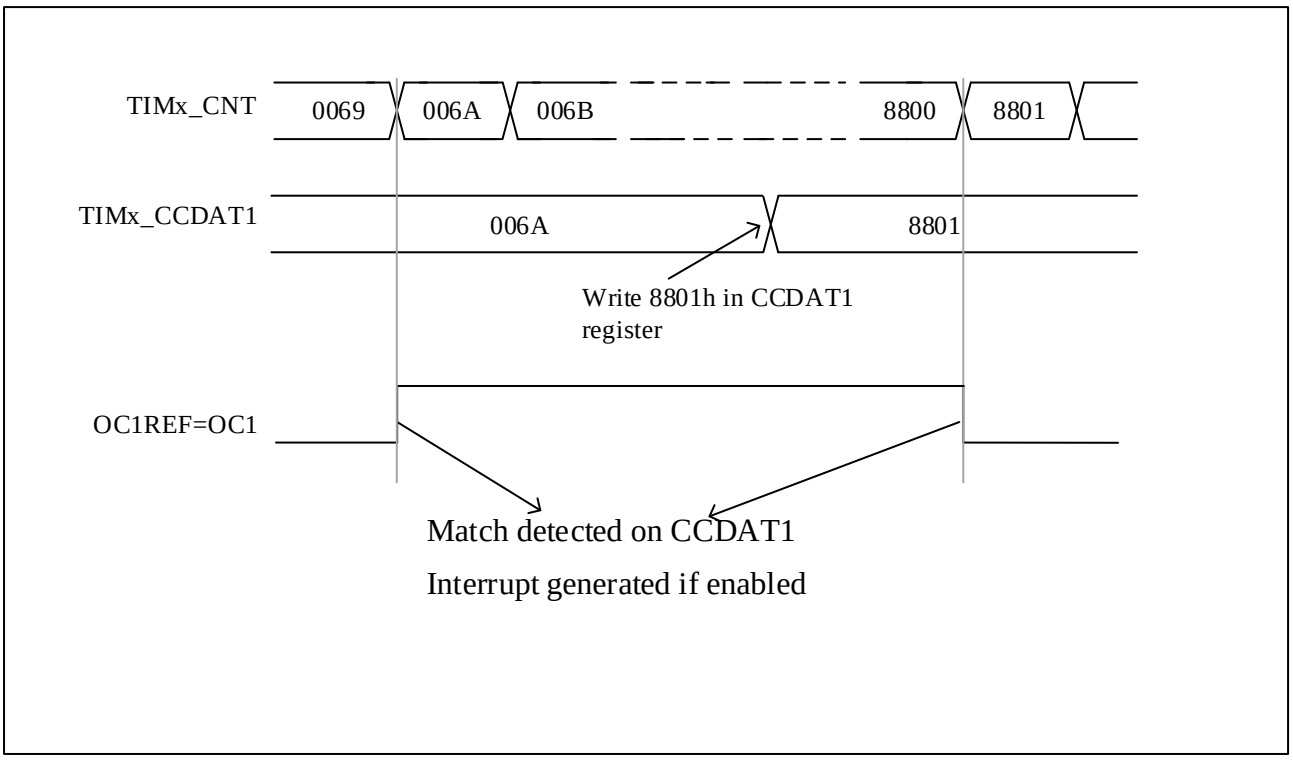
Figure 18-24 Output Compare Mode, Toggle on OC1



18.4.10 PWM Mode

Pulse width modulation mode is used to generate a signal with a frequency determined by the value of the TIMx_AR register and a duty cycle determined by the value of the TIMx_CCDATx register.. And depending on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can select PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN, and then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can program polarity of OCx by setting TIMx_CCEN.CCxP. On the other hand, to enable the output of OCx, user need to set the combination of the value of CCxEN, CCxNEN, MOEN, OSSI, and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only when an update event occurs, the preload register will be transferred to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

18.4.10.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal to 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or both when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

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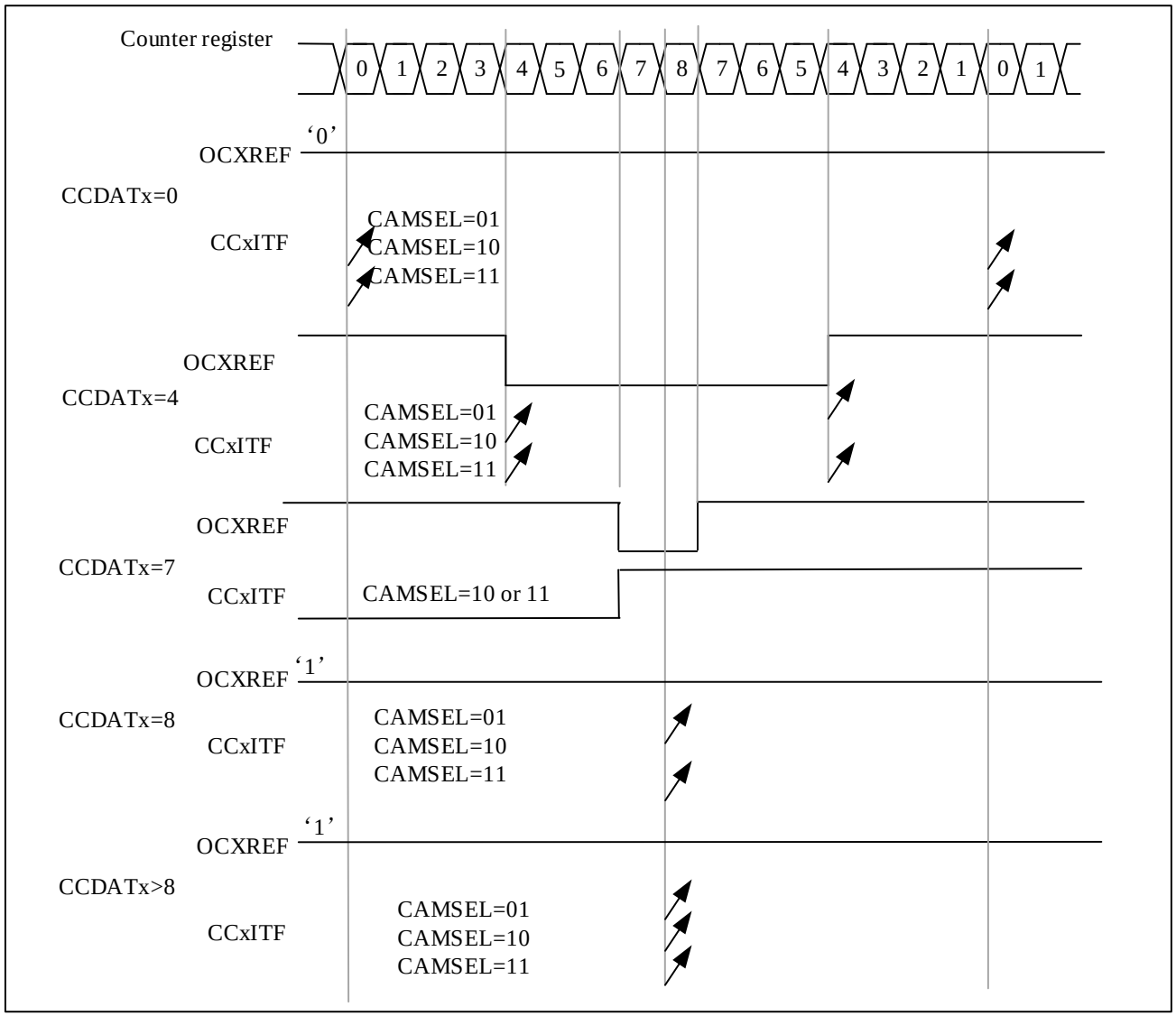
Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

Figure 18-25 Center-Aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considrations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- For safety reasons, It is recommended that users set TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and do not write the counter while it is running.

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18.4.10.2 PWM center-aligned asymmetric mode

About PWM center-aligned asymmetric mode, refer to Section18.4.2.3.2.

18.4.10.3 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

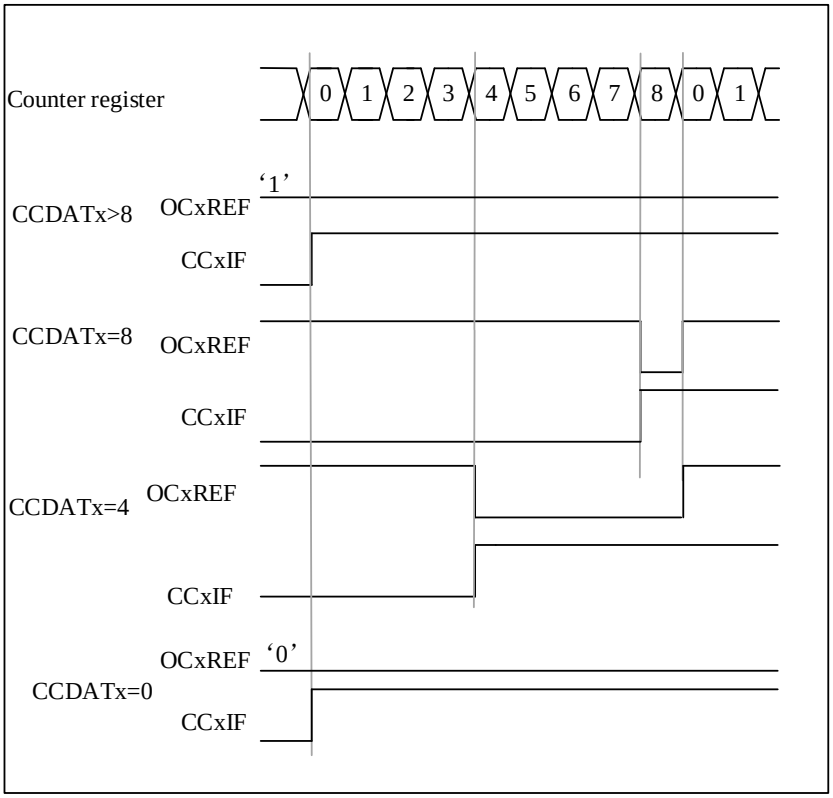
User can set TIMx_CTRL1.DIR=0 to make counter count up.

Example for PWM mode1:

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follows.

Figure 18-26 Edge-Aligned PWM Waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Example for PWM mode1:

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

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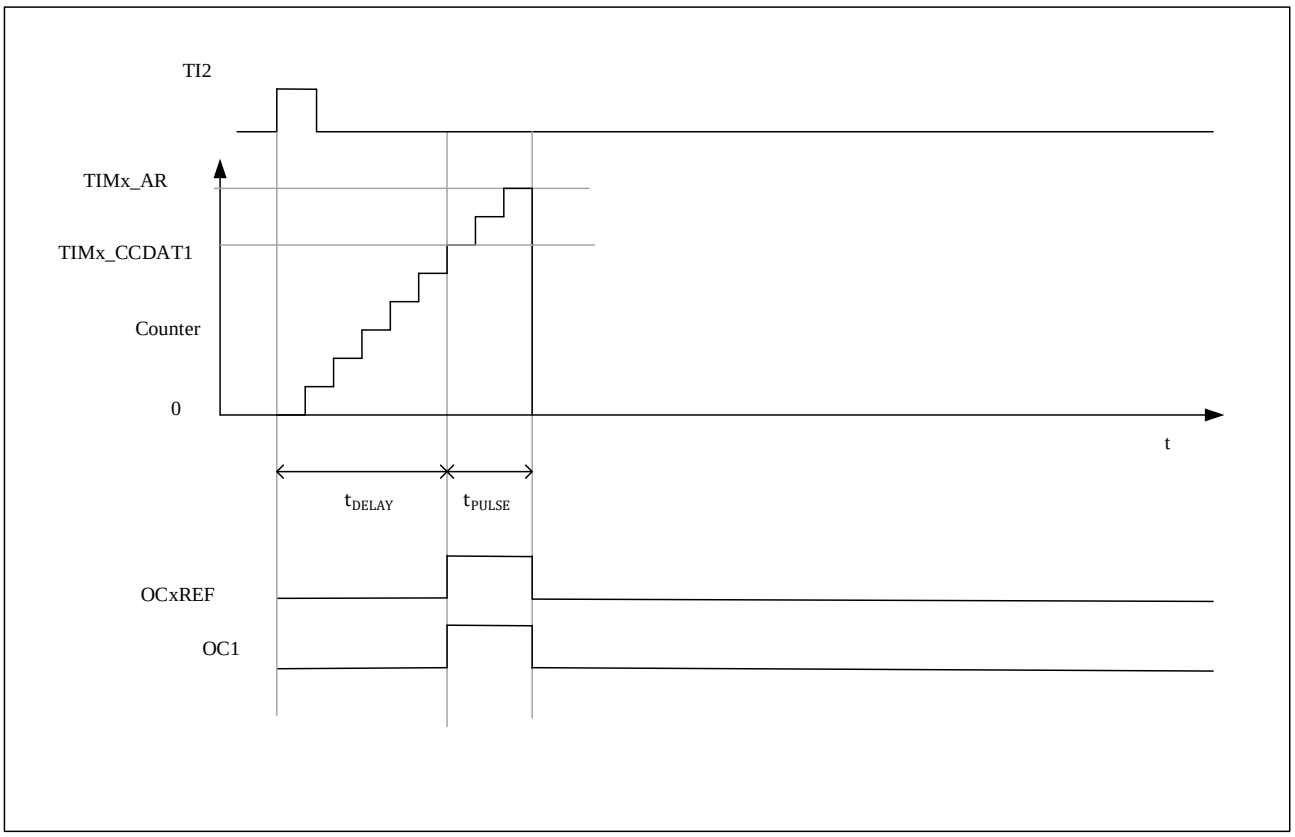
Note: if the n_{th} PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the $(n+1)_{th}$ PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

18.4.11 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay tDELAY. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 18-27 Example of One-Pulse Mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= '01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= '0';
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL= '110' (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value

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of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = '111' to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1.

18.4.11.1 Special case: OCx fast enable:

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

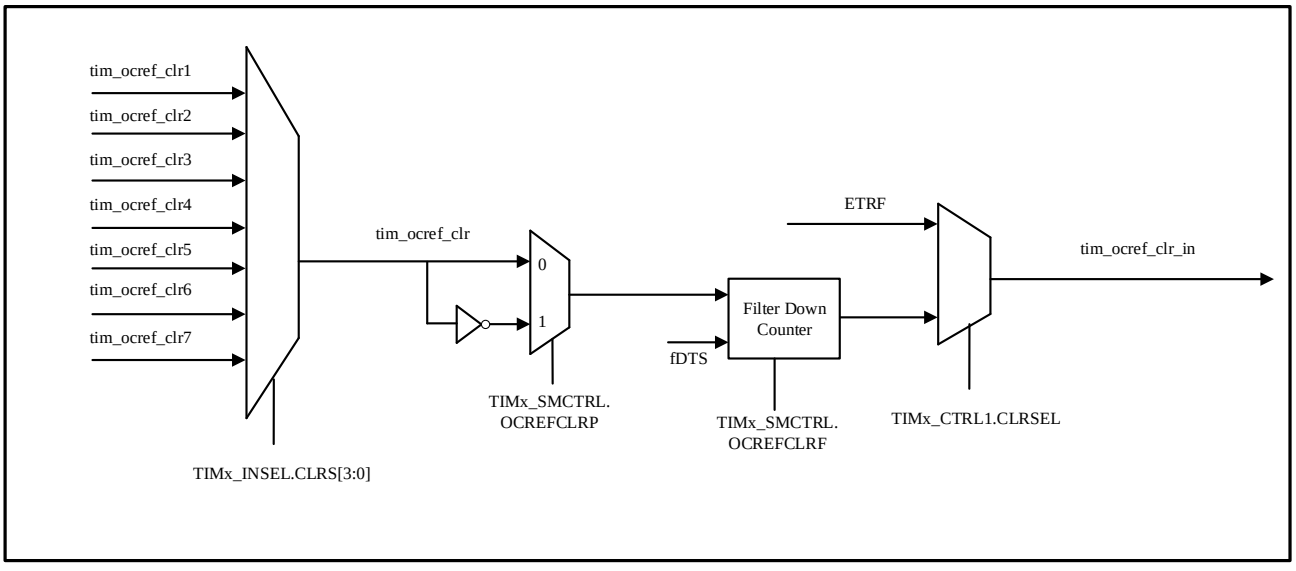
18.4.12 Clearing the Ocxref Signal on an External Event

If the user sets TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only Output Compare and PWM modes can use this function. This cannot be used when it is in forced mode.

The input clear signal tim_ocref_clr_in can be selected as tim_ocref_clr or ETRF through the CLRSEL bit in the TIMx_CTRL1 register.

The tim_ocref_clr signal can be selected through the CLRS[3:0] in the TIMx_INSEL register, as shown in the following diagram.

Figure 18-28 Diagram of External Event Clearing Ocxref Signal



Example: When the tim_ocref_clr_in signal is selected as ETRF, the tim_etr_in configuration is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.

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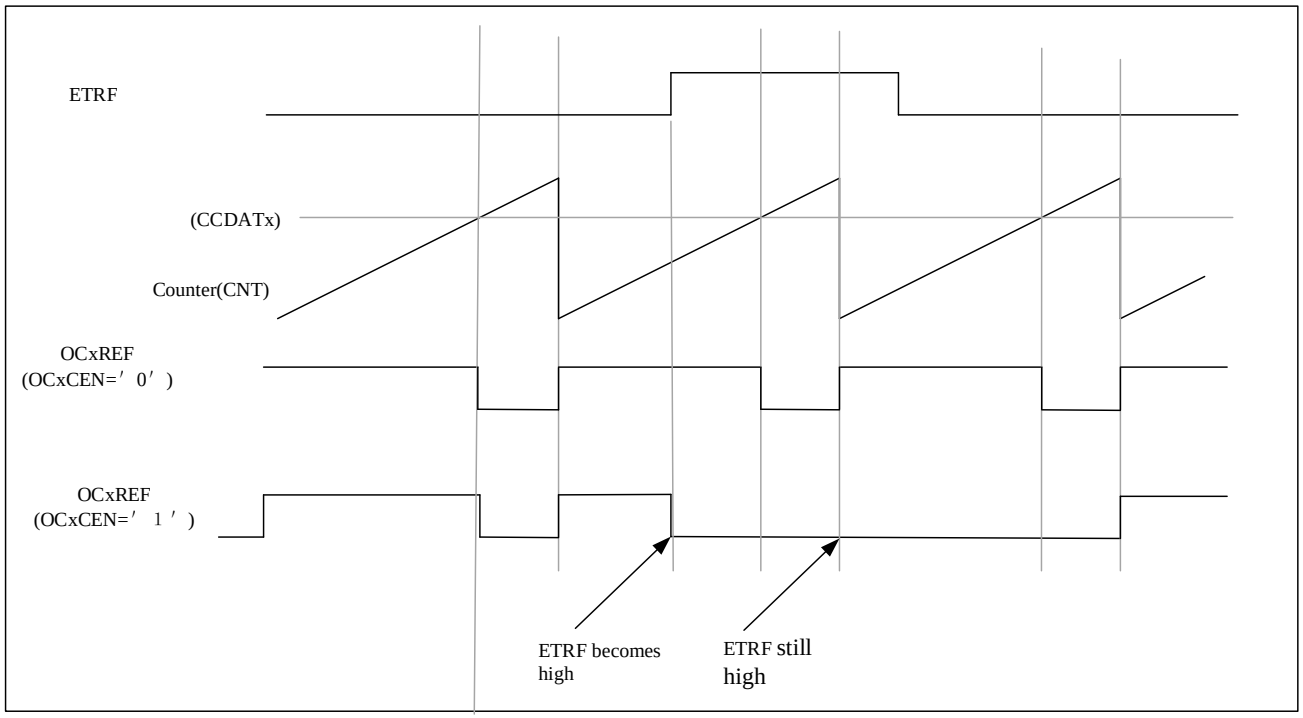
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

For example: The following diagram shows when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 18-29 Clearing the Ocxref of TIMx



18.4.13 Complementary Outputs with Dead-Time Insertion

The advanced-control timer can output two complementary signals, and manage the switching-off and switching-on instants of outputs. This time is generally known as dead-time. User should adjust dead-time depending on the devices connected to the outputs and their characteristics.

User can select the polarity of outputs by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP. And this selection is independently for each output.

User can control the complementary signals OCx and OCxN by setting the combination of several control bits, which are TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. When switching to the IDLE state, the dead-time will be activated.

If user set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN at the same time, a dead-time will be insert. If there is a break circuit, the TIMx_BKDT.MOEN should be set too. There are 10-bit dead-time generators for each channel.

Reference waveform OCxREF can generates 2 outputs OCx and OCxN. And if OCx and OCxN are active high, the OCx ouput signal is the same as the reference signal and the OCxN output signal is the opposite of the reference signal. However, OCx output signal will be delayed relative to the reference rising edge and the OCxN output signal will be delayed relative to the reference falling edge. If the delay is greater than the width of the active OCx or OCxN

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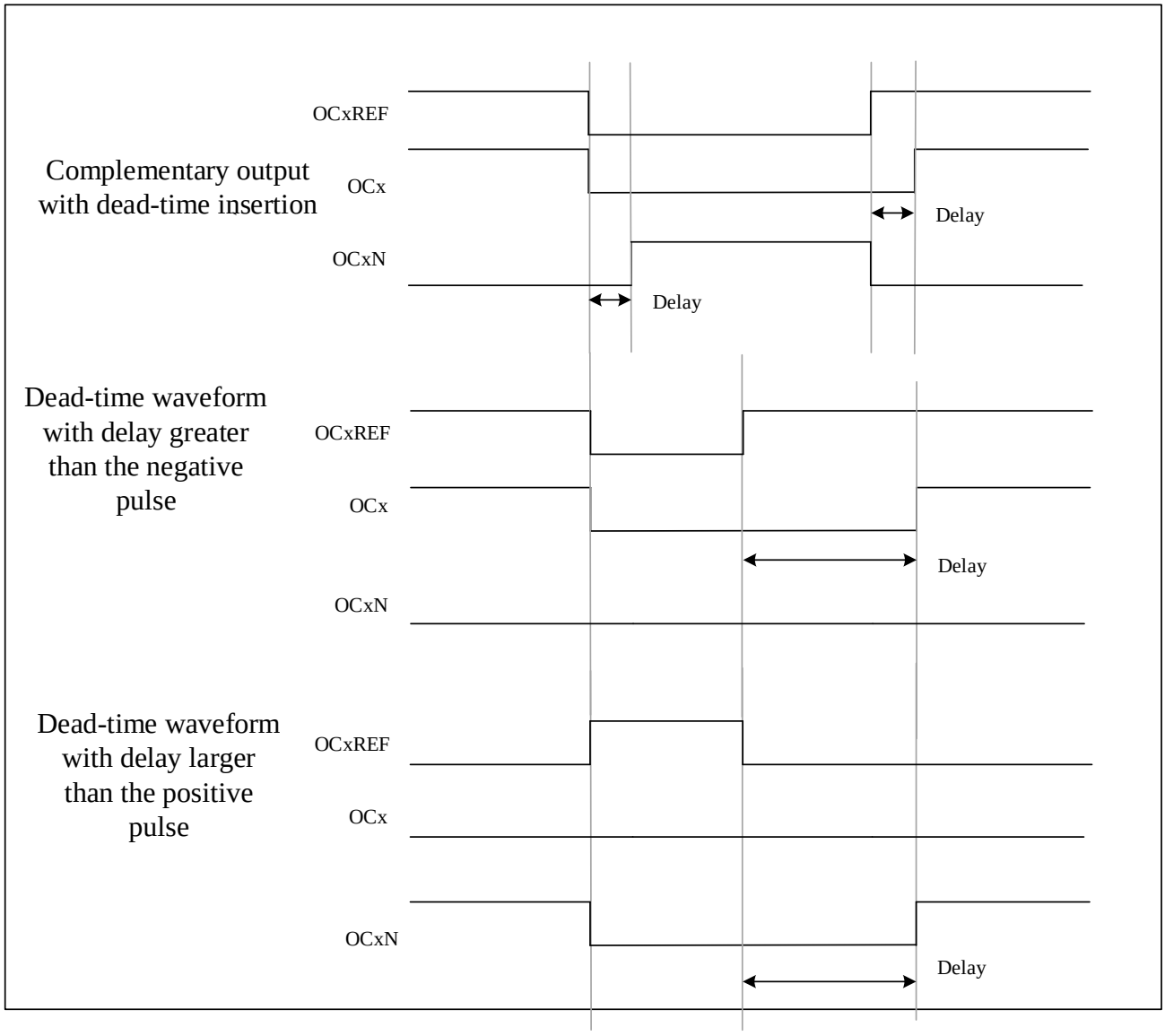
output, the corresponding pulse will not generated.

The relationships between the output signals of the dead-time generator and the reference signal OCxREF are as follow.

Assume that TIMx_CCEN.CCxP=0, TIMx_CCEN.CCxNP=0, TIMx_BKDT.MOEN=1, TIMx_CCEN.CCxEN=1, TIMx_CCEN.CCxNEN=1.

Figure 18-30 Complementary Output with Dead-Time Insertion



User can set TIMx_BKDT.DTGN to programme the dead-time delay for each of the channels.

18.4.13.1 Redirecting OCxREF to OCx or OCxN

In output mode, user can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to re-directed OCxREF to the OCx output or to OCxN output.

Here are two ways to use this function. When the complementary remains at its inactive level, user can use this function to send a specific waveform, such as PWM or static active level. User can also use this function to set both

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outputs in their inactive level or both outputs active and complementary with dead-time.

If user set TIMx_CCEN.CCxEN=0 and TIMx_CCEN.CCxNEN=1, it will not complemented, and OCxN will become active when OCxREF is high. On the other hand, if user set TIMx_CCEN.CCxEN=1 and TIMx_CCEN.CCxNEN=1, OCx will become active when OCxREF is high. On the contrary, OCxN will become active when OCxREF is low.

18.4.14 Break Function

The output enable signals and inactive levels will be modified when setting the corresponding control bits when using the break function. However, the output of OCx and OCxN cannot at the active level at the same time no matter when, that is, (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0.

When multiple break signals are enabled, each break signal constitutes an OR logic. Here are some signal which can be the source of break and break2.

Break：

- The break input pin
- A clock failure event, generated by the clock security system in the clock controller
- A PVD failure event
- Core Hardfault event
- SRAM ECC error
- SRAM parity check error
- The output signal of the DSMU
- The output signal of the comparator
- By software through the TIMx_EVTGEN.BGN

Break2：

- The break2 input pin
- The output signal of the DSMU
- The output signal of the comparator
- By software through the TIMx_EVTGEN.BGN

Perform an OR operation on all sources entering the tim_brk or tim_brk2 input before they are input, as shown in the diagram below.

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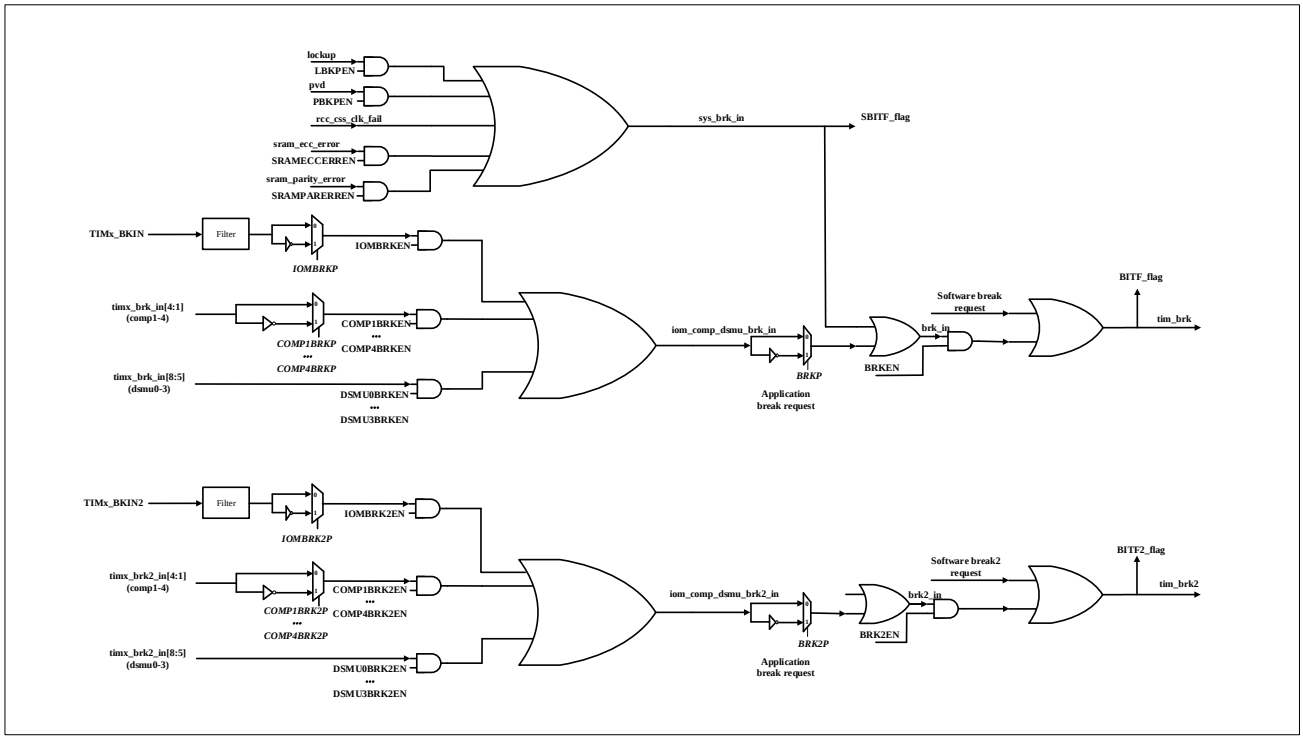
Figure 18-31 Break and Break2 circuitry overview



Note: An asynchronous (clockless) operation is only guaranteed when the programmable filter is disabled. If it is enabled, a fail safe clock mode (for example by using the internal PLL and/or the CSS) must be used to guarantee that break events are handled.

The break circuit will be disable after reset. And the MOEN bit will be low. User can set TIMx_BKDT.BKEN/ BK2EN to enable the break function. The polarity of break input signal can be selected by setting TIMx_BKDT.BKP/BK2P. User can modify the TIMx_BKDT.BKEN/BK2EN and TIMx_BKDT.BKP/BK2P at the same time. After user set the TIMx_BKDT.BKEN/BK2EN and TIMx_BKDT.BKP/BK2P, there is 1 APB clock cycle delay before the configuration take effect. Therefore, user need to wait 1 APB clock cycle to read back the written bit value.

The falling edge of MOEN can be asynchronous, so a resynchronization circuit has been inserted between the actual signal and the synchronous control bit. This circuit will cause a delay between the asynchronous and the synchronous signal. When user set TIMx_BKDT.MOEN while it is low, user need to insert a delay before reading the value. Because an asynchronous signal was written but user read the synchronous signal.

The behaviors that after a break occurs are as follow:

- TIMx_BKDT.MOEN will be cleared asynchronously, and then the outputs will be put in inactive state, idle state or reset state. The state of output is selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is off.
- Once TIMx_BKDT.MOEN=0, the output of each output channel will be driven with the level programmed in TIMx_CTRL2.OIx. Timer will release the enable outputs(taken over by GPIO controller) if TIMx_BKDT.OSSI=0, otherwise it will remain high.
- If user choose to use complementary outputs, the behaviors of TIM are as follow:

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- Depends on the polarity, the outputs will be set in reset state first. It is an asynchronous option so it still works even if there is no clock provided to the timer.
- The dead-time generator will be reactivated if the timer clock is still provided, and drive the outputs according to the value of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN after the dead-time when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0, that is, the OCx and OCxN still cannot be driven to active level at the same time. Note that the dead-time will be longer than usual because of the resynchronization on MOEN (almost 2 cycles of ck_tim).
- Timer will release the output control if TIMx_BKDT.OSSI=0. Otherwise, if the enable output was high, it will remain high. If it was low, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is high.

- If TIMx_DINTEN.BIEN=1, when TIMx_STS.BITF=1, an interrupt will be generated.
- If user set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will be set automatically when the next UEV happened. User can use this to regulate. If user did not set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will remain low until been set 1 again. At this situation, user can use this for security. User can connect the break input to thermal sensors, alarm for power drivers, or other security components.
- When the break input is active, TIMx_BKDT.MOEN cannot be set automatically or by software at the same time, and the TIMx_STS.BITF cannot be cleared. Because the break inputs are active on level.

To ensure the security of application, the break circuit has the write protection function, and there is break input and output management too. It allow user to freeze some parameters, such as dead-time duration, OCx/OCxN polarities and state when disabled, OCxMD configurations, break enable and polarity. User can choose one of the 3 levels of protection to use by setting TIMx_BKDT.LCKCFG. However, the TIMx_BKDT.LCKCFG can only be written once after an MCU reset.

An example for output behavior in response to a break is as follow:

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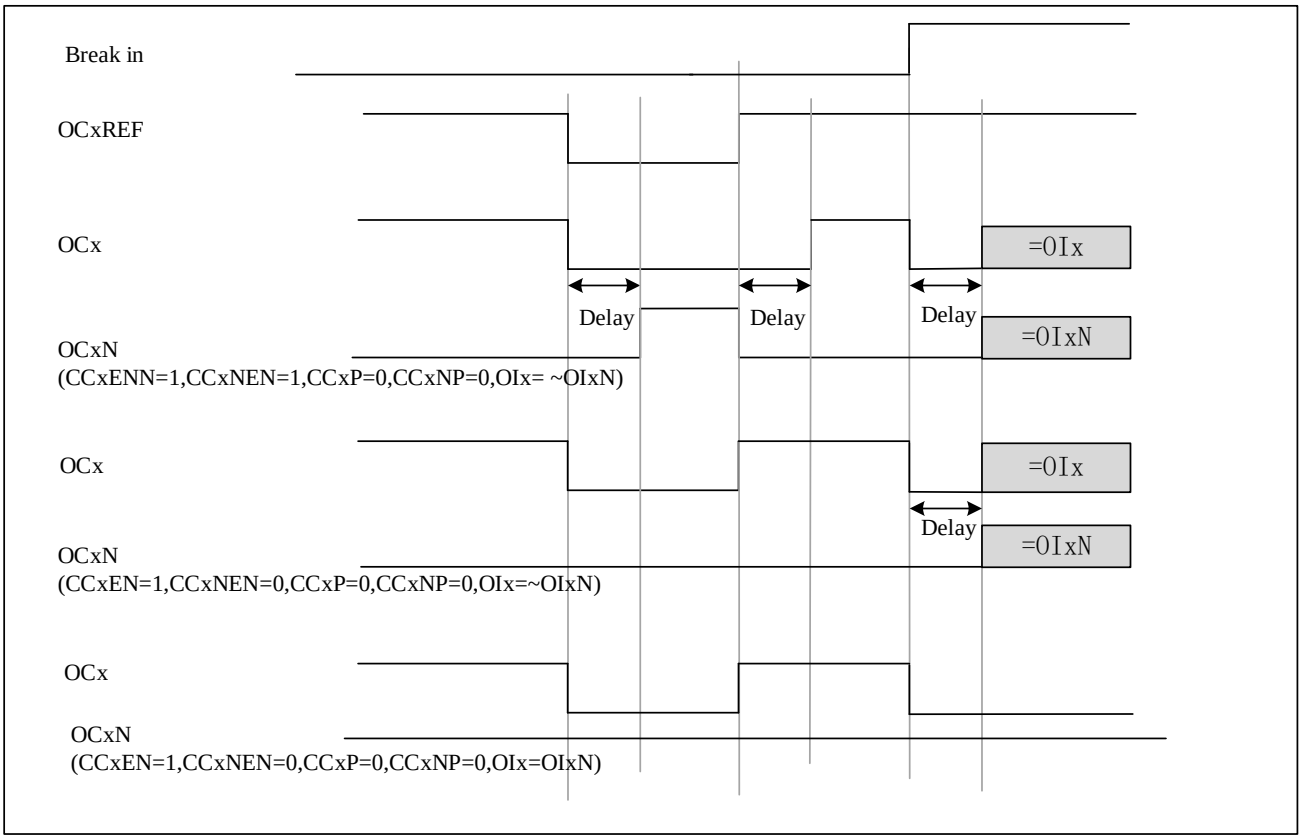
Figure 18-32 Output Behavior in Response to a Break



Two brake inputs have different behaviors for the timer output:

- The tim_brk input can disable (invalid state) the PWM output or force the PWM output to a predefined safe state.
- The tim_brk2 can only disable (invalid state) the PWM output.

The priority of the tim_brk input is higher than the tim_brk2 input, as shown in the table below.

Note: tim_brk2 must be used only when OSSR = OSSI = 1.

Figure 18-12 Behavior of Timer Outputs versus tim_brk/tim_brk2 Inputs

tim_brk	tim_brk2	Timer Outputs State	Typical Use Case	
			OCxN Output	OCx Output
Active	X	–Inactive, then forced output state (after a deadtime) –Outputs disabled if OSSI = 0 (control taken over	ON after deadtime insertion	OFF

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		by GPIO logic)		
Inactive	Active	Inactive	OFF	OFF

The following diagram provides an example of the behavior of OCx and OCxN outputs when a valid signal appears on the tim_brk and tim_brk2 inputs. In this case, the polarity of both outputs is active high (CCxP = CCxNP = 0 in the TIMx_CCEN register).

Figure 18-33 PWM Output State Following tim_brk and tim_brk2 Assertion (OSSI=1)

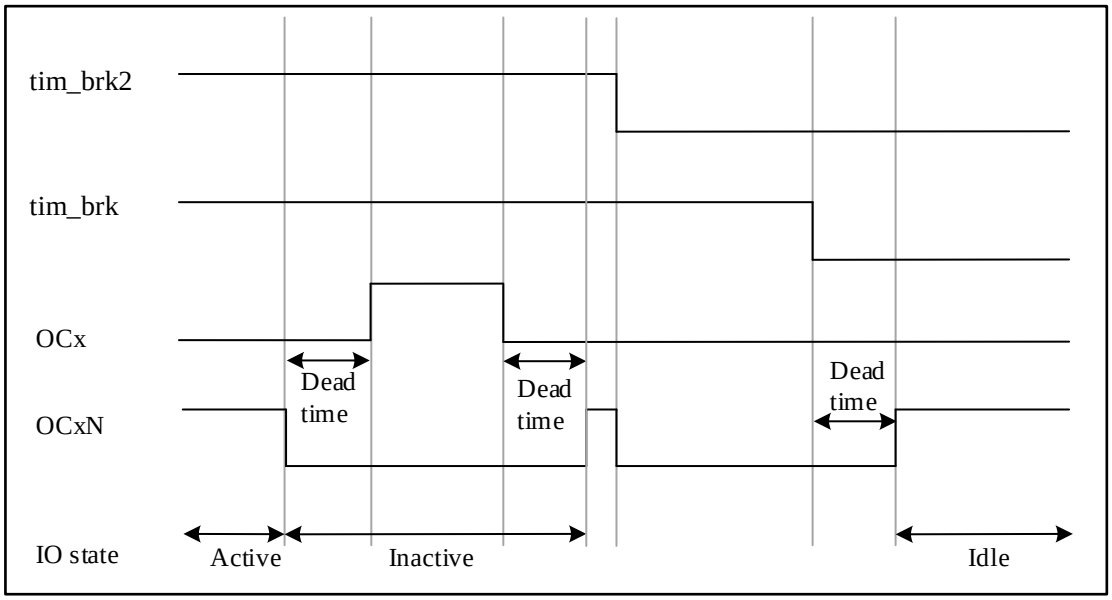
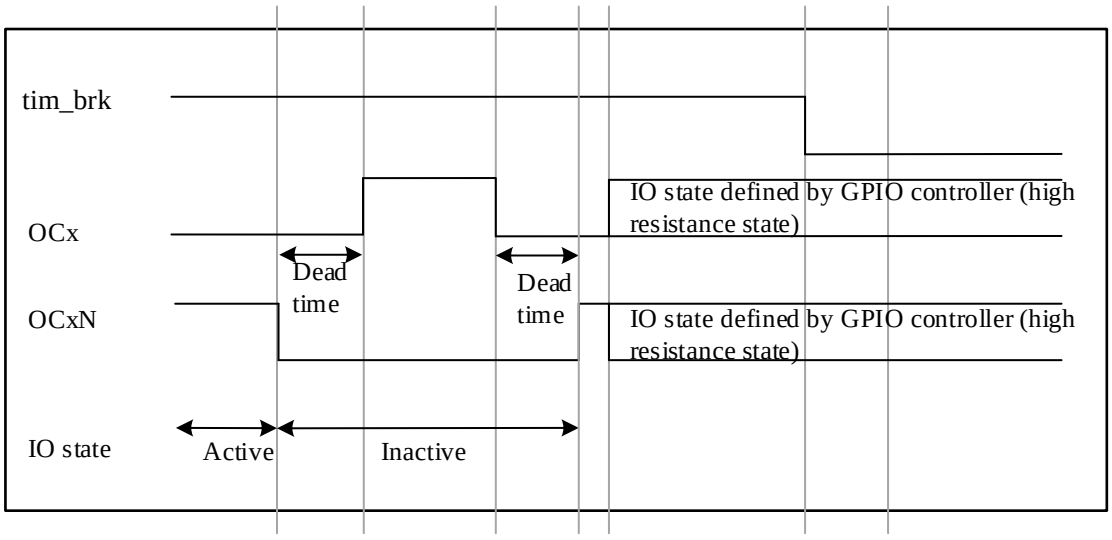


Figure 18-34 PWM Output State Following tim_brk Assertion (OSSI=0)



18.4.14.1 Break filter

Register TIMx_BKFR description are as follow:

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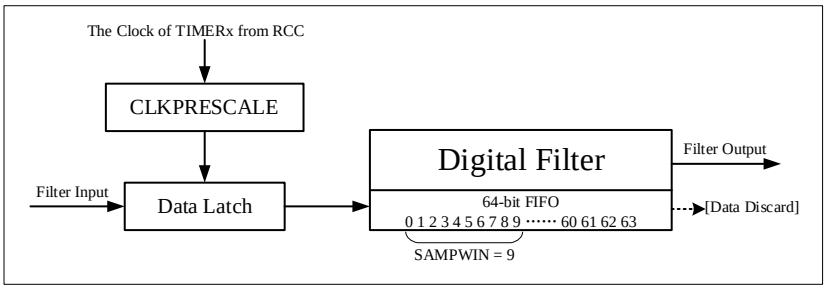
Figure 18-35 Slide Filter



- The digital filter samples break signal at the clock of TIMx from RCC, accumulating samples in a 64-bits FIFO. Only sampled data within window size defined in TIMx_BKFR.WSIZE [5:0] with maximum size 64.
- The filter outputs the majority value inside sample window which is defined by the threshold value in TIMx_BKFR.THRESH [5:0] with maximum threshold of 63. This value should be equal or more than half of window size. If neither logic 1 nor logic 0 counts inside sampling window is more than threshold, digital filter maintain previous output value.
- TIMx_ BKFR. SLIDFPSC[15:0] register determines sample rate of corresponding digital filter. Filter FIFO capture one sample value from input at every sample clock.
- If digital filter is off, filter input will bypass to output like a wire.

18.4.15 Bidirectional Break

ATIM1/ATIM2/ATIM3/ATIM4 have bidirectional brake I/O functionality.

This provides support for:

- A board-level global brake signal, which can be used to send a fault signal to an external MCU or gate driver through a unique IO (input and output status pin).
- When multiple internal and external brake sources need to be combined, they are connected together through an "OR" operation to generate a single brake event.

The tim_brk and tim_brk2 inputs are configured for bidirectional mode using the BRKBID/BRK2BID in the TIMx_BDTR register. BRKBID/BRK2BID can be locked in read-only mode using the LOCK bit in the TIMx_BDTR register (at LOCK level 1 or above).

Bidirectional mode is available for both the tim_brk and tim_brk2 inputs, requiring the I/O configuration to be in open-drain mode with a low-level polarity (through the TIMx_AF1.IOMBRKP, TIMx_BKDT.BKP, TIMx_AF1.IOMBRK2P, and TIMx_BKDT.BK2P bits). Any break request from the system (such as CSS), on-chip peripherals, or break inputs will force the break inputs to a low level to indicate a fault event. For safety reasons, if the polarity bit is not set correctly, bidirectional mode will be inhibited (e.g. set to active high, bidirectional mode will not take effect).

Software break events (TIMx_EVTGEN.BGN and BGN2) also force the break IO to "0" to indicate to external devices that the timer has entered a break state. However, this is only effective when the break is enabled (TIMx_BKDT.BKEN or BK2EN=1). When a software break event occurs (TIMx_BKDT.BKEN or BK2EN=0), the output is put in a safe state, and the break flag is set. However, it has no effect on the TIMx_BKIN and TIMx_BKIN2

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I/O.

A safe disarming mechanism prevents the system to be completely locked-up (a low level on the break input triggers a break which enforces a low level on the same input).

When the TIMx_BKDT.BRKDSRM (BRK2DSRM) bit is set to 1, the break output is released to clear a fault signal and provide the possibility to re-arm the system.

At any time, the break protection circuit cannot be disabled:

- The break input path is always active: the break event remains active even if the TIMx_BKDT.BRKDSRM (BRK2DSRM) bit is set and the open-drain control is released. This prevents the PWM output to be re-started when break conditions are present.
- As long as the output is enabled (TIMx_BKDT.MOEN bit is set), the TIMx_BKDT.BRKDSRM (BRK2DSRM) bit cannot disarm the break protection.

Table 18-13 Break Protection Disarming Conditions

MOEN	BRKBID (BRK2BID)	BRKDSRM (BRK2DSRM)	Break Protection State
0	0	X	Armed
0	1	0	Armed
0	1	1	Disarmed
1	X	X	Armed

Arming and re-arming break circuitry

The break circuit (in input or bidirectional mode) is armed by default (peripheral reset configuration).

After a break (break2) event, the following procedure must be followed to re-arm the protection:

- The TIMx_BKDT.BRKDSRM (BRK2DSRM) bit must be set to release the output control.
- The software must wait for the system break conditions to disappear (if any) and clear the TIMx_STS.SBIF status flag (or clears it systematically before re-arming).
- The software must poll the TIMx_BKDT.BRKDSRM (BRK2DSRM) bit until it is cleared by hardware (when the application break conditions disappear).

From this point, the break circuit is armed and active, and the TIMx_BKDT.MOEN bit can be set to re-enable the PWM output.

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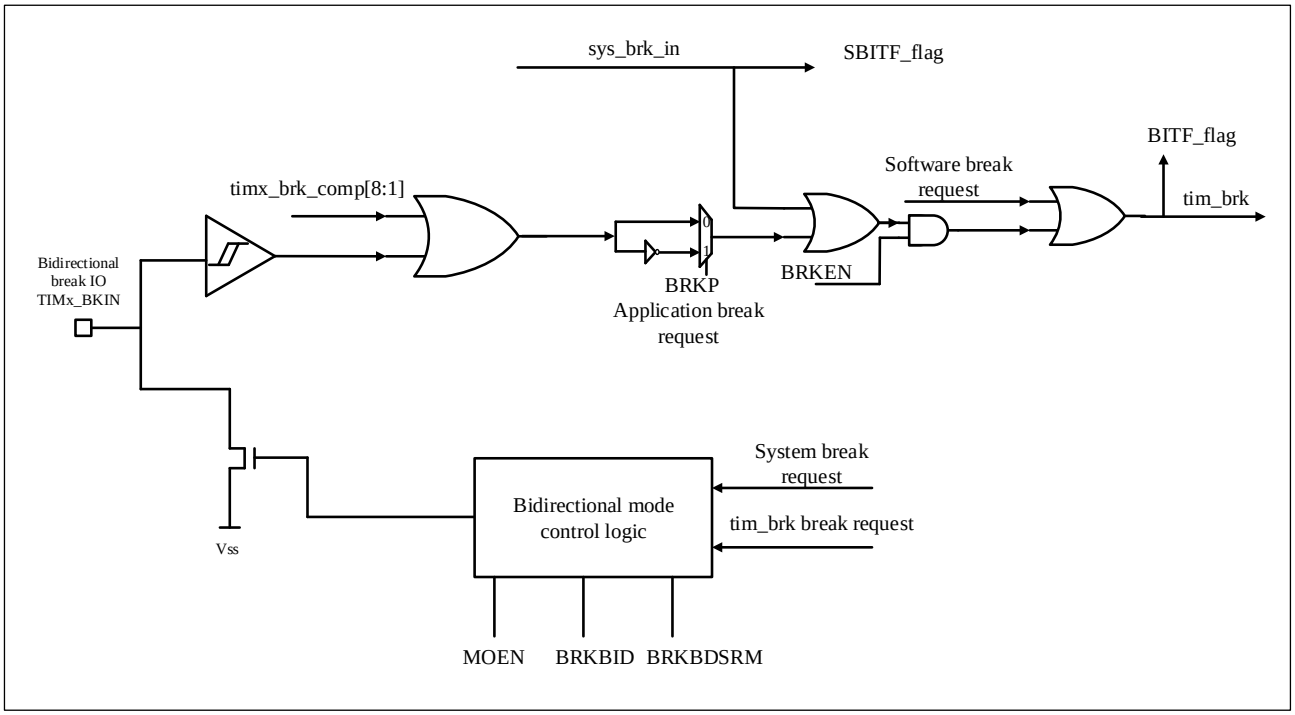
Figure 18-36 Output Redirection (tim_brk2 Request Not Represented)



18.4.16 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M4F core halted), depending on the DBG_TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details, refer to Section 50.

18.4.17 ATIMx and External Trigger Synchronization

TIMx can be synchronized by a trigger in slave modes (reset, trigger and gated).

18.4.17.1 Slave mode: Reset mode

In reset mode, the trigger event can reset the counter and the prescaler updates the preload registers TIMx_AR, TIMx_CCDATx, and generates the update event UEV (TIMx_CTRL1.UPRS=0).

The following is an example of a reset mode:

- Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);
- The slave mode is selected as reset mode (TIMx_SMCTRL.SMSEL=0100), and the trigger input is selected as TI1 (TIMx_SMCTRL.TSEL=101);
- Setting TIMx_CTRL1.CNTEN = 1 to start counter;

After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1);

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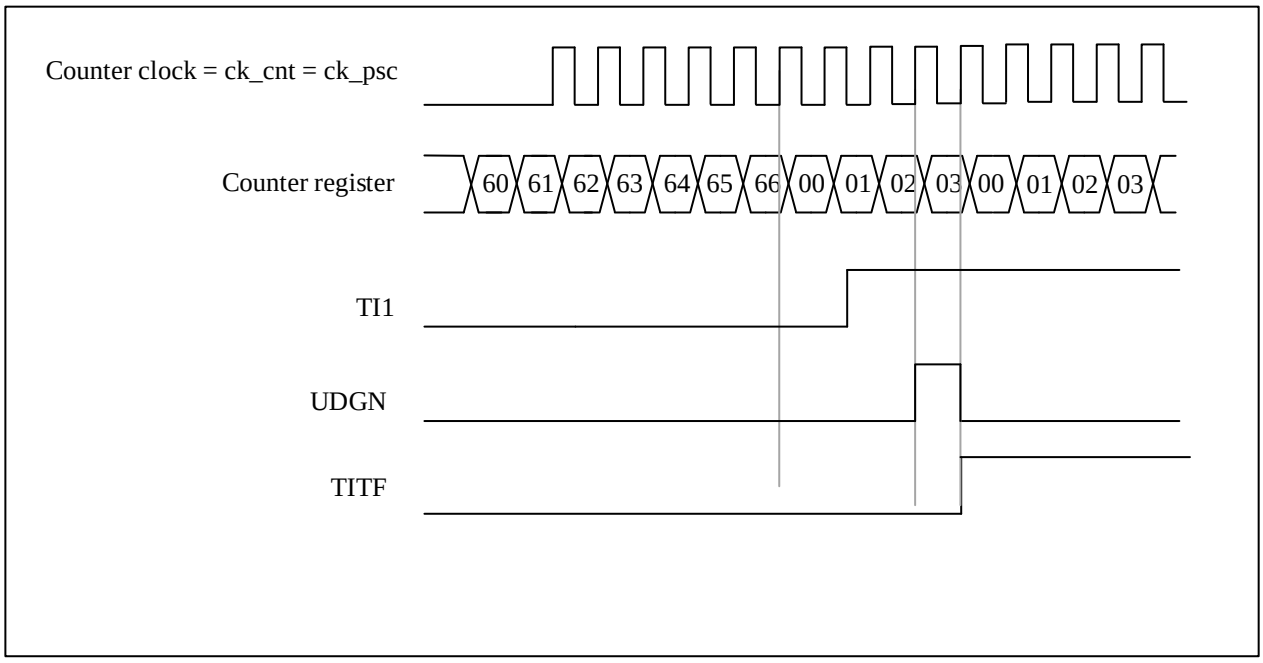
The delay between the rising edge on TI1 and the actual reset of the counter is due to the resynchronization circuit on TI1 input.

Figure 18-37 Control Circuit in Reset Mode



18.4.17.2 Slave mode: Trigger mode

In trigger mode, the trigger event (rising edge/falling edge) of the input port can trigger the counter to start counting.

The following is an example of a trigger pattern:

- Channel 2 is configured as input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01, TIMx_CCEN.CC2P=0);
- Select from mode to trigger mode (TIMx_SMCTRL.SMSEL=0110), select TI2 for trigger input (TIMx_SMCTRL.TSEL=110);

When a rising edge is detected on TI2, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI2 and the actual start of the counter is due to the resynchronization circuit on TI2 input.

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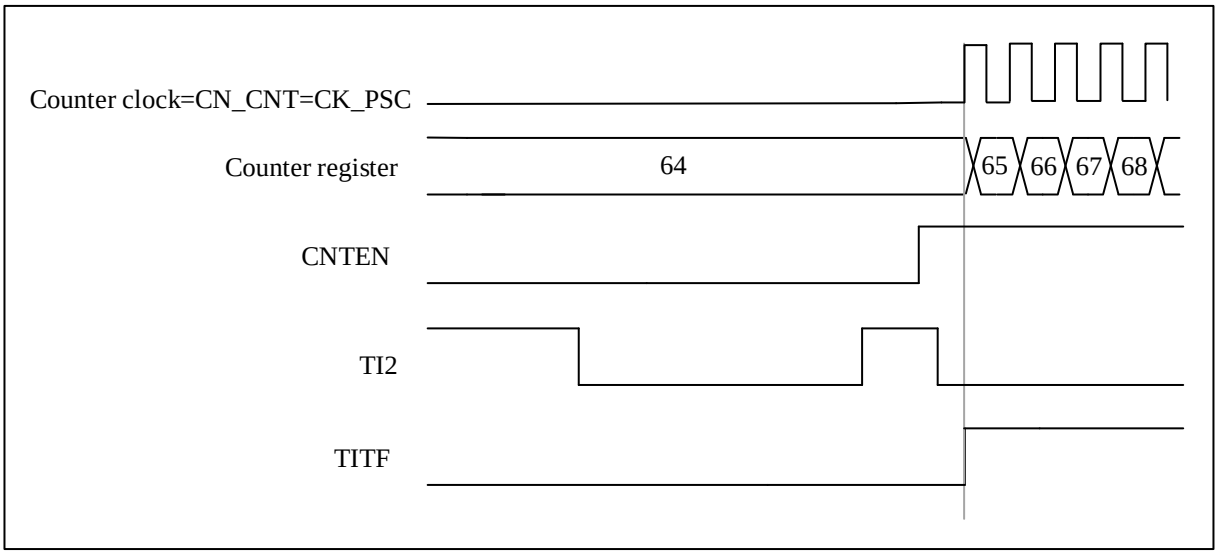
Figure 18-38 Control Circuit in Trigger Mode



18.4.17.3 Slave mode: Gated mode

In gated control mode, the level polarity of the input port can control whether the counter counts or not.

The following is an example of a gated mode:

- Channel 1 is configured as input detection active low on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1);
- Select the slave mode as the gated mode (TIMx_SMCTRL.SMSEL=0101), and select TI1 as the trigger input (TIMx_SMCTRL.TSEL=101);
- Setting TIMx_CTRL1.CNTEN = 1 to start counter

When TI1 detects that the level changes from low to high, the counter stops counting, and when TI1 detects that the level changes from high to low, the counter starts counting, and the trigger flag will be set (TIMx_STS.TITF=1) when it starts or stops counting;

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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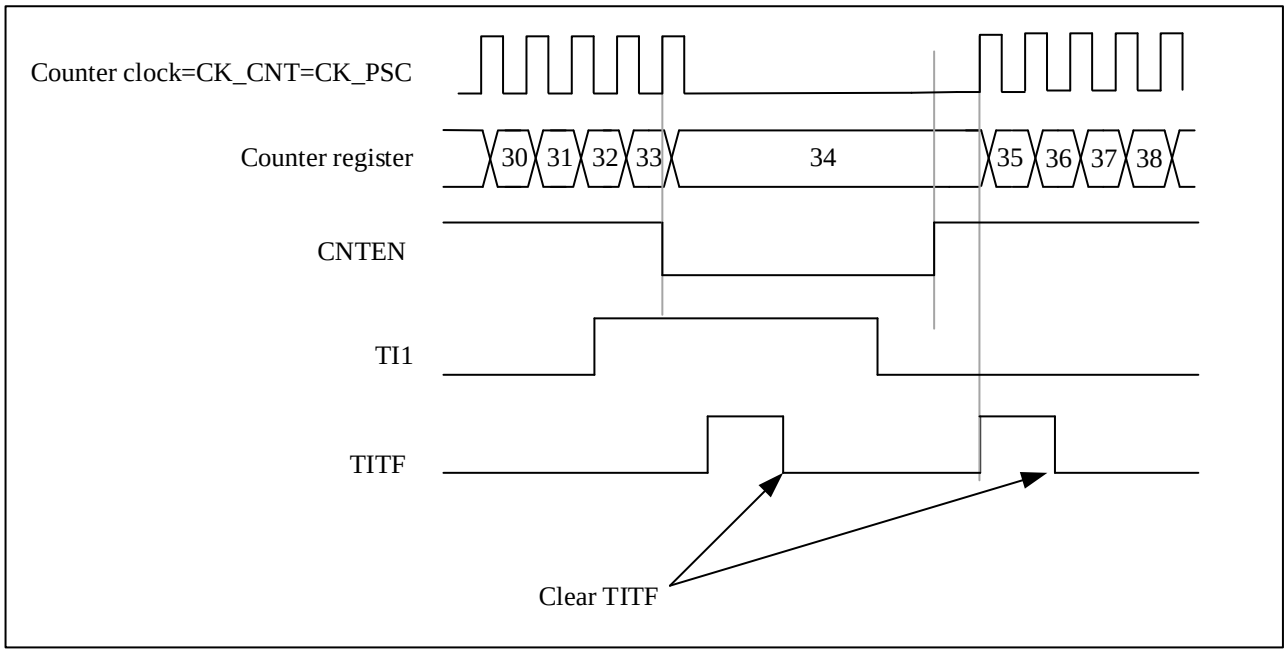
Figure 18-39 Control Circuit in Gated Mode



18.4.17.4 Slave mode: Trigger mode + External clock mode 2

In reset mode, trigger mode and gate control mode, the counter clock can be selected as external clock mode 2, and the ETR signal is used as the external clock source input. At this time, the trigger selection needs to select non-ETRF (TIMx_SMCTRL.TSEL=111).

Here is an example:

- Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0),
- Enable external clock mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=0110), select TI1 for trigger input (TIMx_SMCTRL.TSEL=101),

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and the trigger flag is set (TIMx_STS.TITF=1).

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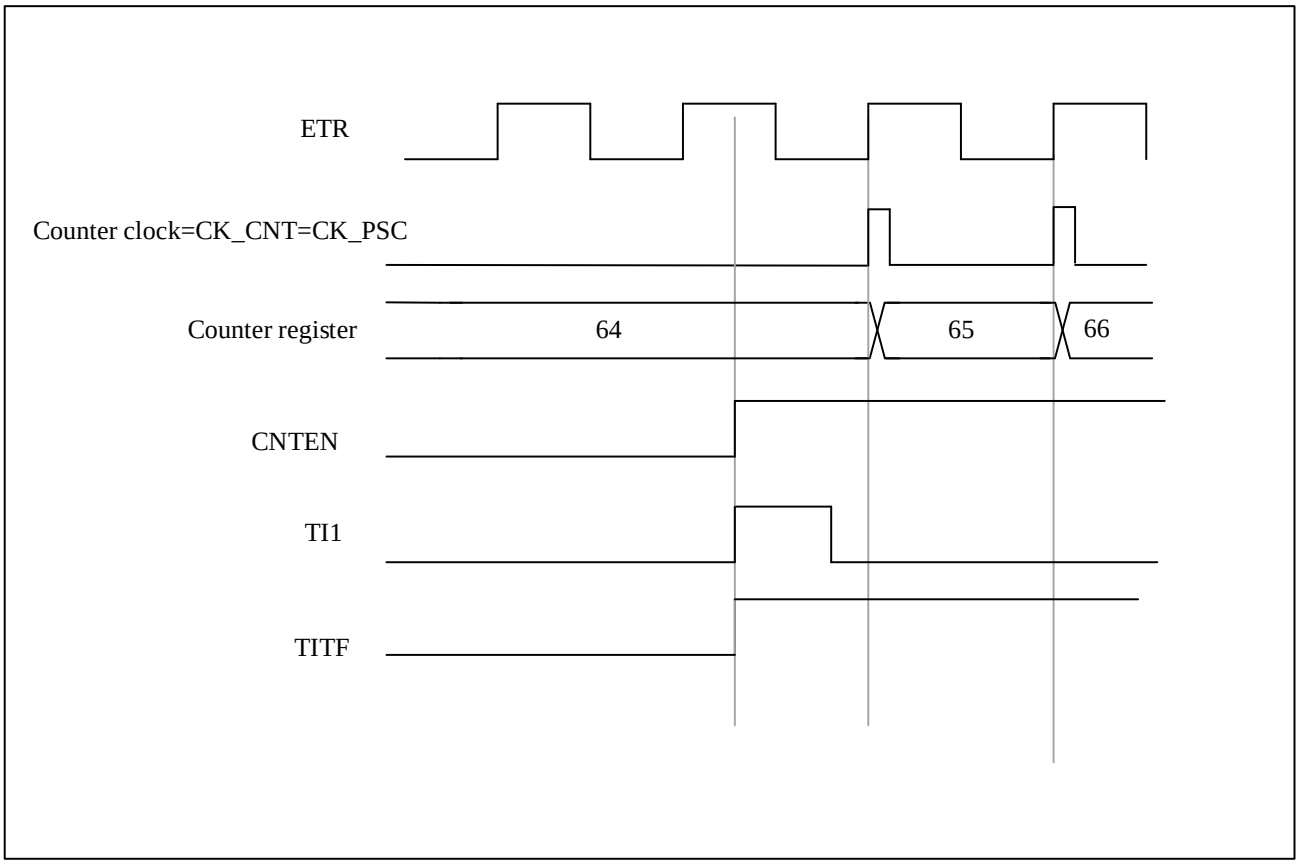
Figure 18-40 Control Circuit in Trigger Mode + External Clock Mode2



18.4.17.5 Slave mode: Combined Reset + Trigger Mode

In this case, the rising edge of the selected trigger input (TRGI) will reset the counter, generate register updates, and start the counter.

This mode is used for one-pulse mode.

The event selected on the input resets and enables the counter.

In the following example, the counter is reset and starts counting up on the rising edge of the TI2 input:

- Configure channel 2 to detect the rising edge of TI2. Set the input filter bandwidth (in this example, no filter is needed, keep TIMx_CCMOD1.IC2F=0000). No capture prescaler is used in the trigger operation, so no configuration is required. The TIMx_CCMOD1.CC2SEL bit is used to select the input capture source, set TIMx_CCMOD1.CC2SEL=01. Set TIMx_CCEN.CC2P=1 to determine the polarity (detect only low level).
- Configure TIMx_SMCTRL.SMSEL=1110 to set the timer in Combined Reset + Trigger mode; set TIMx_SMCTRL.TSEL=110 to select TI2 as the input source.

When a rising edge occurs on TI2, the counter starts counting under the internal clock drive, and the TITF flag is set.

The delay between the rising edge on TI2 and the actual stop of the counter is due to the resynchronization circuit on TI2 input.

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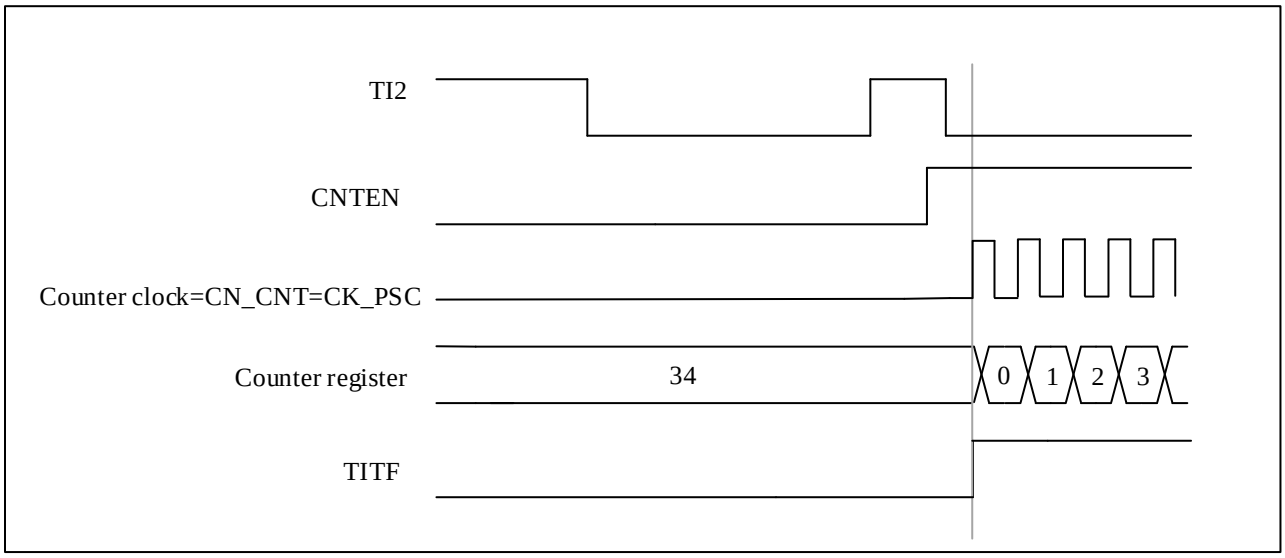
Figure 18-41 Control Circuit in Combined Reset + Trigger Mode



18.4.17.6 Slave mode: Combined Gated + Reset Mode

When the trigger input (TRGI) is high, the counter is enabled. Once the trigger goes low, the counter stops and is reset. The start and stop of the counter are both controlled.

This mode can detect out-of-range PWM signals (duty cycle exceeding the maximum expected value).

In the following example, the counter counts up only when TI1 is low, and the counter stops and resets when TI1 goes high:

- Configure channel 1 to detect low level on TI1. Set the input filter bandwidth (in this example, no filter is needed, so keep TIMx_CCMOD1.IC1F=0000). No capture prescaler is used in the trigger operation, so no configuration is required. The TIMx_CCMOD1.CC1SEL bit is used to select the input capture source, set TIMx_CCMOD1.CC1SEL=01. Set TIMx_CCEN.CC1P=1 to determine the polarity (detect only low level).
- Configure TIMx_SMCTRL.SMSEL=1101 to set the timer in Gated + Reset mode; set TIMx_SMCTRL.TSEL=101 to select TI1 as the input source.
- Set CNTEN=1 in the TIMx_CTRL1 register to start the counter. In Gated + Reset mode, if CNTEN=0, the counter cannot start, regardless of the trigger input level.

The counter starts counting based on the internal clock as long as TI1 is low, and it stops counting once TI1 goes high. The TITF flag in TIMx_STS is set when the counter starts or stops.

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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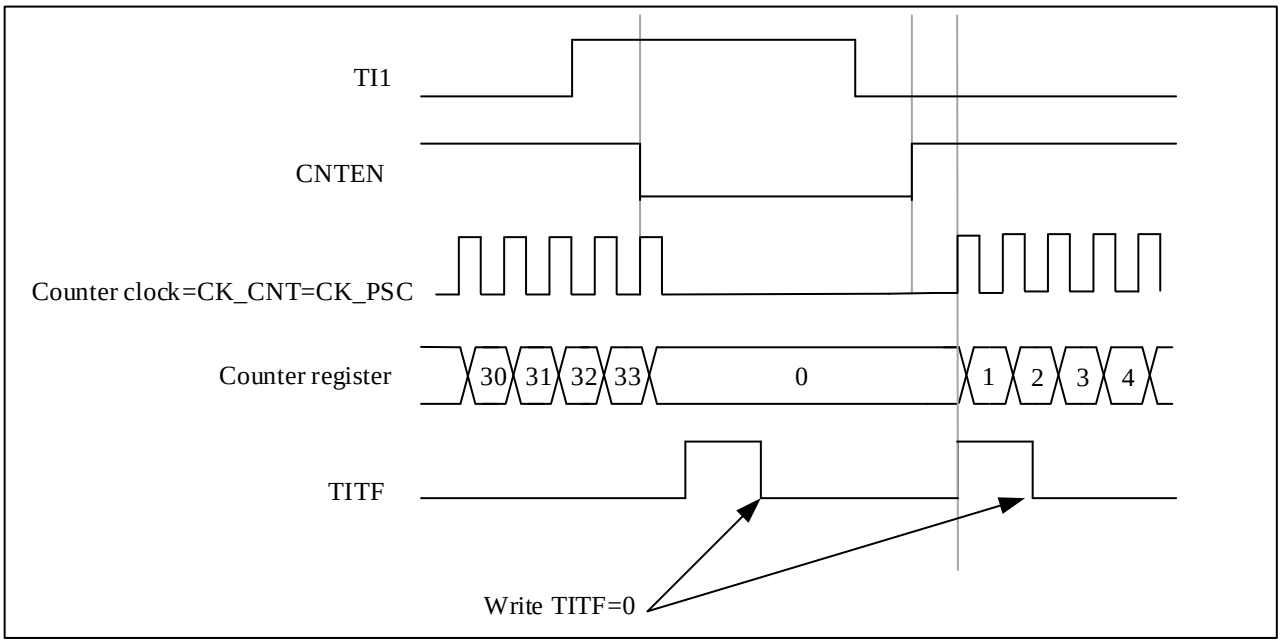
Figure 18-42 Control Circuit in Combined Gated + Reset Mode



18.4.18 Timer Synchronization

All TIMx are internally interconnected for timer synchronization or chaining. For more details, refer to Section 20.5.20.

18.4.19 ADC Triggers

The timer can generate ADC trigger events through various internal signals, such as reset, enable, or comparison events, and can also generate pulse triggers issued by internal edge detectors.

users can trigger the ADC by selecting the internal lines TRGO/TRGO2 using the MMSEL2[3:0] and MMSEL[3:0] bits in the TIMx_CTRL2 register.

Channels 4/7/8/9 can also trigger the ADC by configuring TRIG4/TRIG7/TRIG8/TRIG9 to '1', causing channels 4/7/8/9 to generate pulse triggers for the ADC during comparison matches.

18.4.20 Generating Six-step PWM Output

In order to modify the configuration of all channels at the same time, the configuration of the next step can be set in advance (the preloaded bits are OCxMD, CCxEN and CCxNEN). When a COM commutation event occurs, the OCxMD, CCxEN, and CCxNEN preload bits are transferred to the shadow register bits.

Methods to generate a COM commutation event:

- A software sets TIMx_EVTGEN.CCUDGN;
- Generated by hardware on the rising edge of TRGI;

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, enabling interrupts

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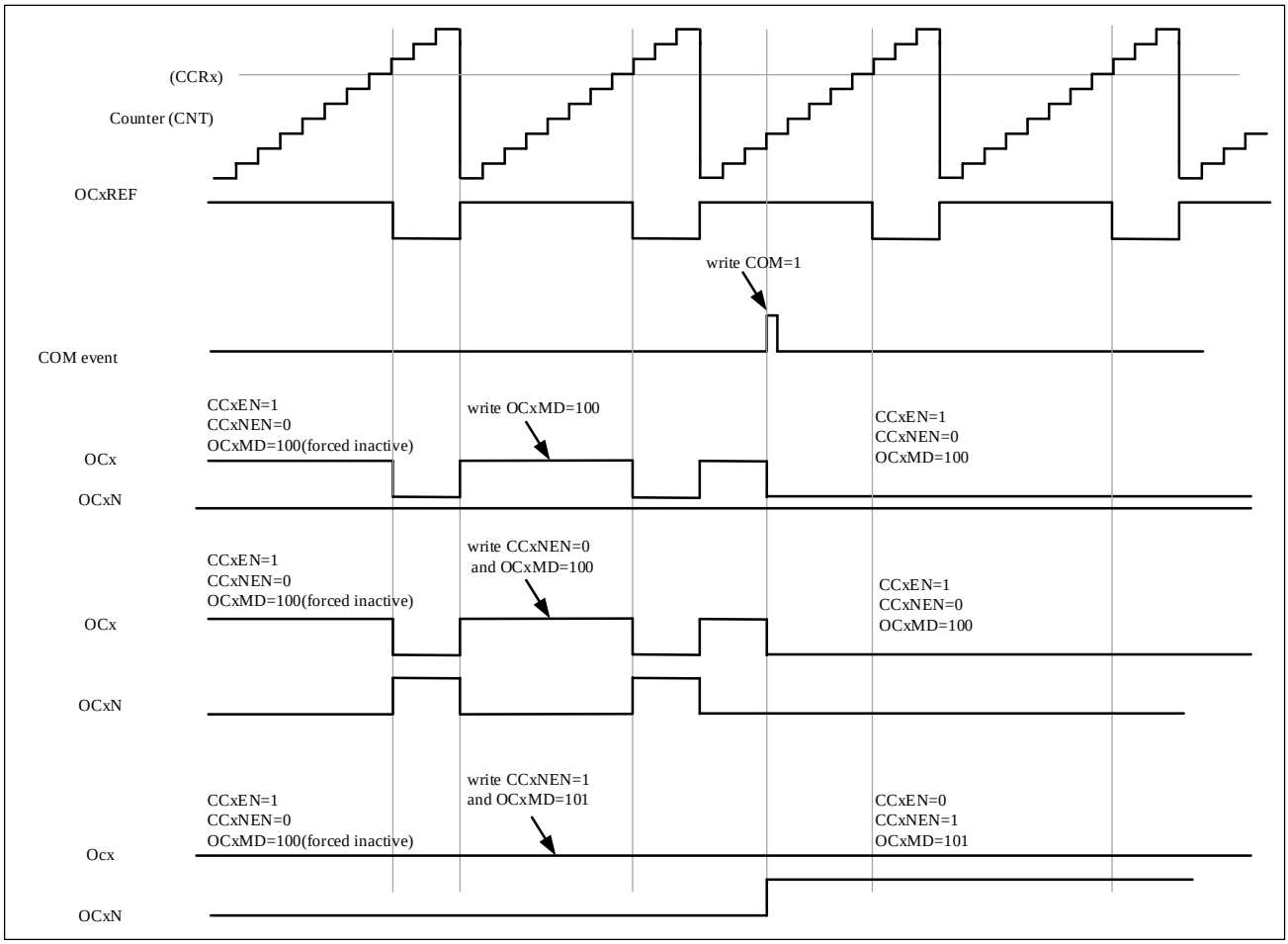
(TIMx_DINTEN.COMIEN) will generate interrupts, and enabling DMA requests (TIMx_DINTEN.COMDEN) will generate DMA requests.

The following figure shows the output timing diagram of OCx and OCxN when a COM commutation event occurs in three different configurations:

Figure 18-43 6-Step PWM Generation, COM Example (OSSR=1)



18.4.21 Encoder Interface Mode

18.4.21.1 Quadrature Encoder Mode

The encoder uses two inputs, TI1 and TI2 as the interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are five types of quadrature encoder counting modes:

- Encoder mode 1: The counter counts only on the edges of TI1, TIMx_SMCTRL.SMSEL = '0001';
- Encoder mode 2: The counter counts only on the edges of TI2, TIMx_SMCTRL.SMSEL = '0010';
- Encoder mode 3: The counter counts on the edges of both TI1 and TI2, TIMx_SMCTRL.SMSEL = '0011';
- Encoder mode 4: The counter counts only on the edges of TI1 when T2 is high, TIMx_SMCTRL.SMSEL = '1001';

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- Encoder mode 5: The counter counts only on the edges of TI2 when T1 is high, TIMx_SMCTRL.SMSEL = '1010';

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is as follows:

Table 18-14 The Relationship between the Counting Direction and the Encoder Signal（CC1P=CC2P=0）

Active Edge	SMSEL[3:0]	Level on Opposite Signals (TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rising	Falling	Rising	Falling
Counting only on TI1	0001	Hign	Counting down	Counting up	Don't count	Don't count
		Low	Counting up	Counting down	Don't count	Don't count
Counting only on TI2	0010	Hign	Don't count	Don't count	Counting up	Counting down
		Low	Don't count	Don't count	Counting down	Counting up
Counting on Both TI1 and TI2	0011	Hign	Counting down	Counting up	Counting up	Counting down
		Low	Counting up	Counting down	Counting down	Counting up
Counting only on TI1 when T2 is high	1001	Hign	Counting down	Counting up	Don't count	Don't count
		Low	Don't count	Don't count	Don't count	Don't count
Counting only on TI2 when T1 is high	1010	Hign	Don't count	Don't count	Counting up	Counting down
		Low	Don't count	Don't count	Don't count	Don't count

The change in the counter value in each encoder mode is as follows:

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Figure 18-44 The Encoder Counts Only on TI1

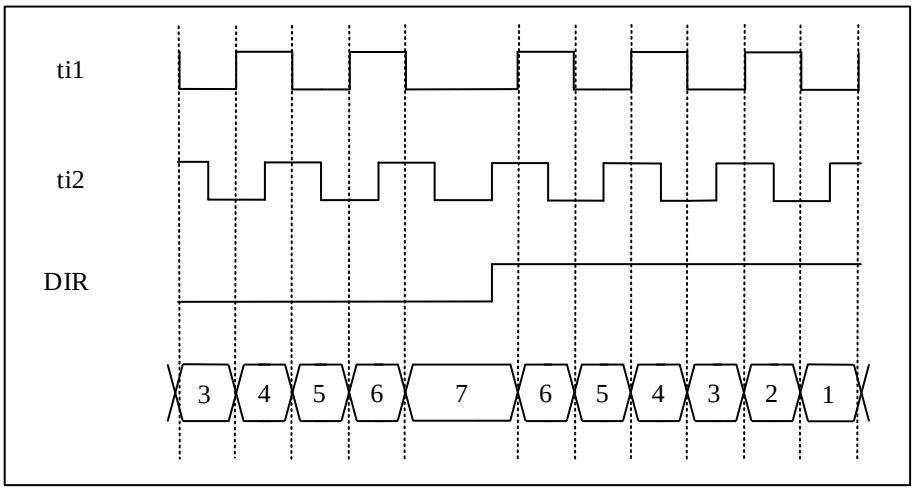

Figure 18-45 The Encoder Counts Only on TI2

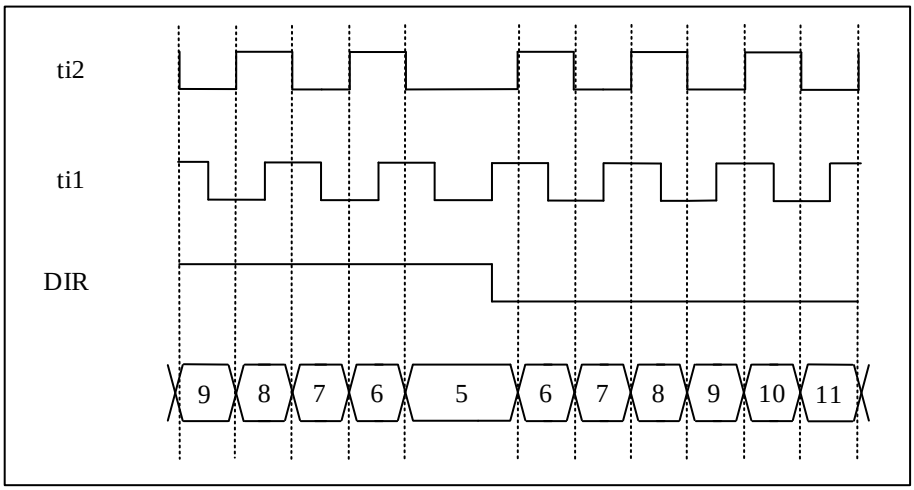

Figure 18-46 The Encoder Counts on Both TI1 and TI2

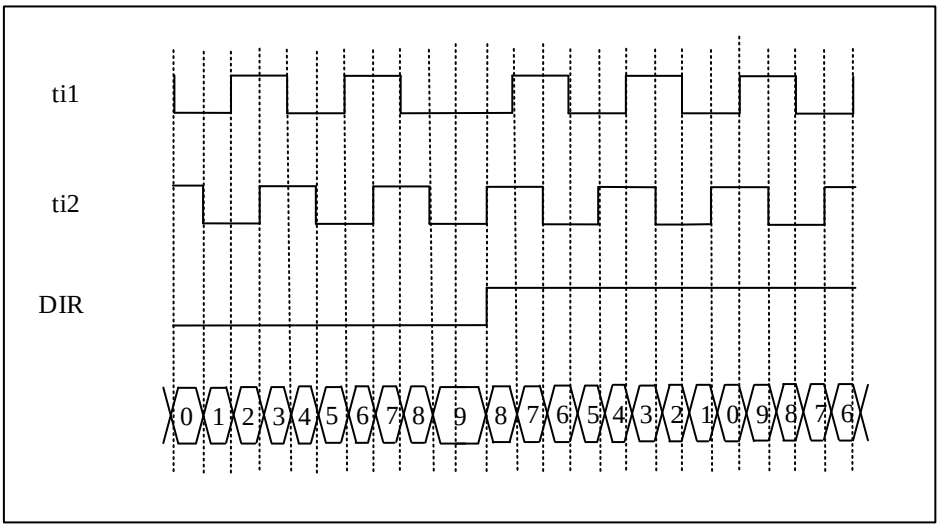

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Figure 18-47 The Counter Counts Only on TI1 When T2 is High

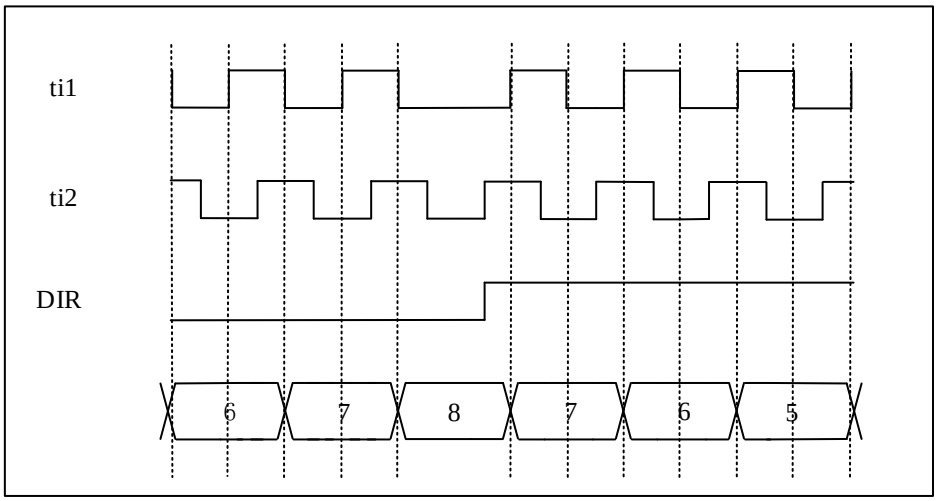
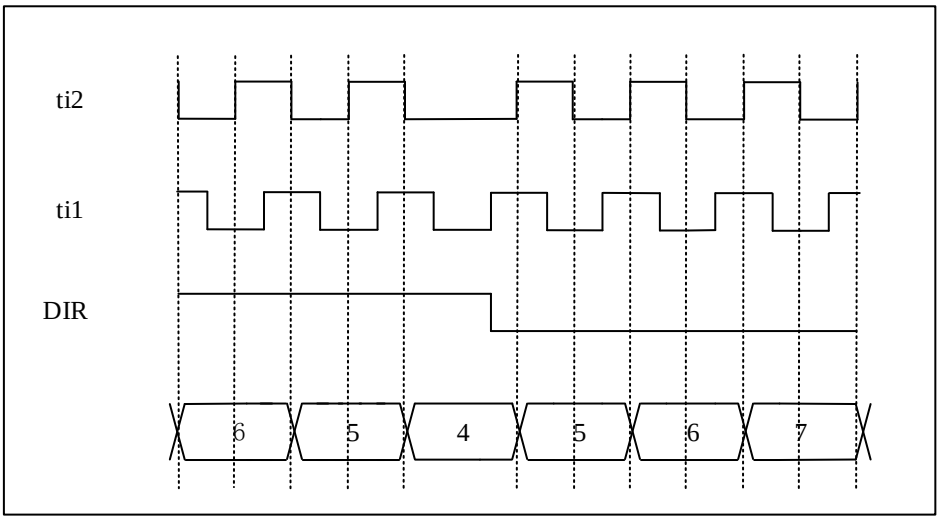


Figure 18-48 The Counter Counts Only on TI2 When TI1 is High



Here is an example of an encoder with dual edge selected for triggering to suppress input jitter:

- IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= ‘01’), IC1FP1 is not inverted (TIMx_CCEN.CC1P= ‘0’);
- IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= ‘01’), IC2FP2 is not inverted (TIMx_CCEN.CC2P= ‘0’);
- The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = ‘011’);
- Enable counter TIMx_CTRL1.CNTEN= ‘1’.

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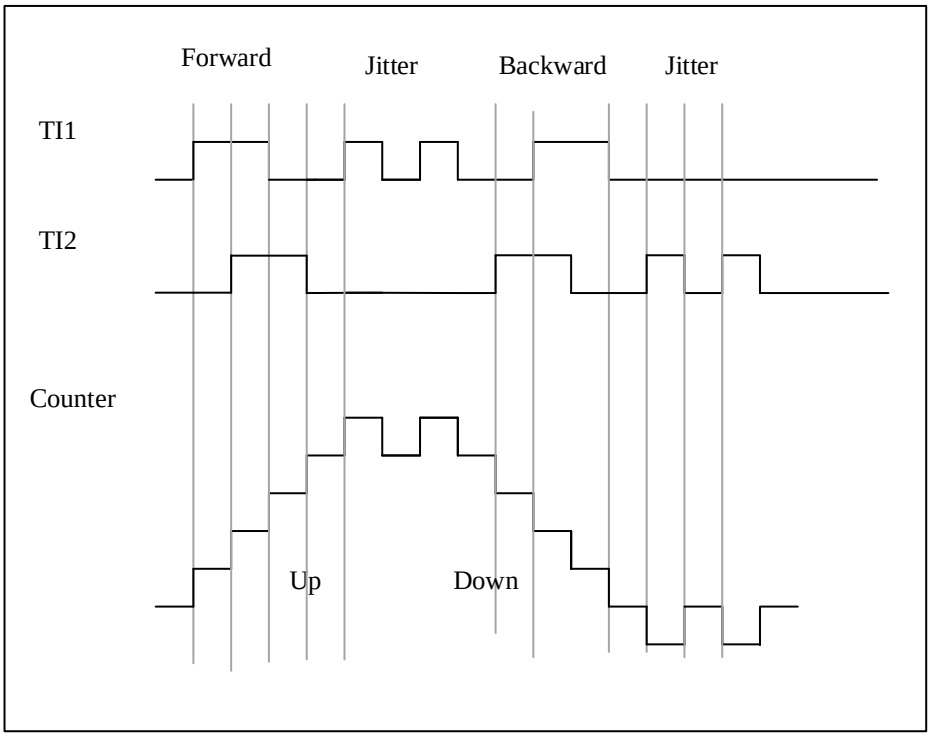
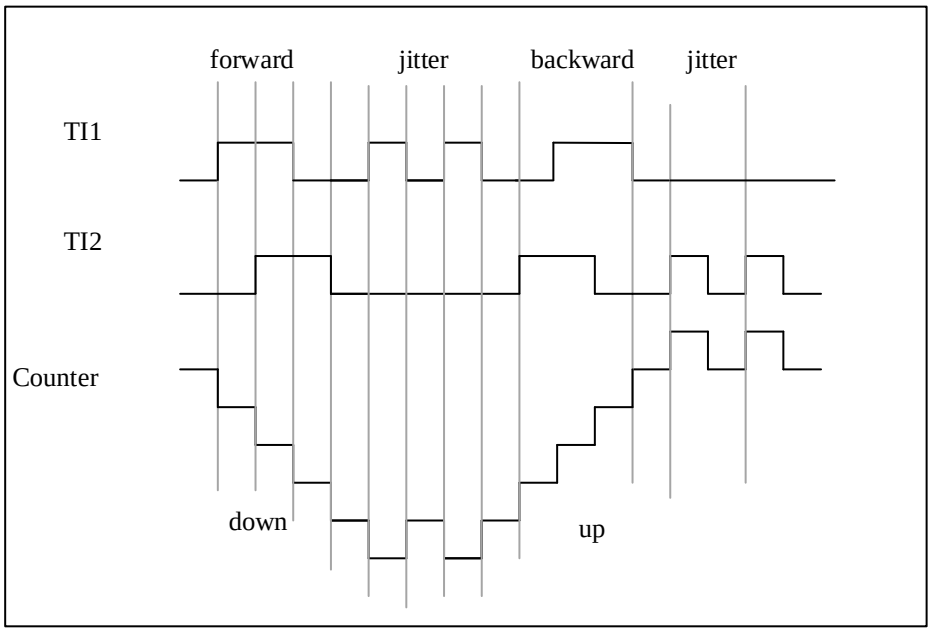
Figure 18-49 Example of Counter Operation in Encoder Interface Mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above).

Figure 18-50 Encoder Interface Mode Example with IC1FP1 Polarity Inverted



18.4.21.2 Pulse-Level Encoder Mode

In the Pulse-Level encoder mode, the clock is provided on a single line on TI2, while the counting direction is provided by the TI1 input.

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This mode is enabled through the SMSEL[3:0] in the TIMx_SMCTRL register, as follows.

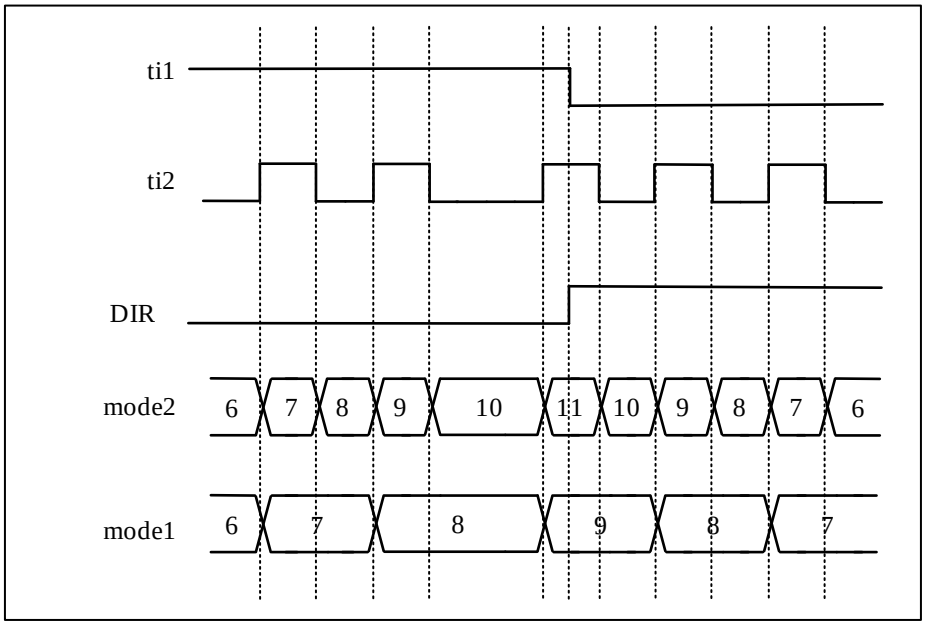
1011：Pulse-Level encoder mode 2, the counter is updated on both the rising and falling edges of the clock.

1100：Pulse-Level encoder mode 1, the counter is updated on a single clock edge based on the value of CC2P. CC2P = 0 corresponds to counting on the rising edge, and CC2P = 1 corresponds to counting on the falling edge.

The polarity of the direction signal for TI1 is set by the CC1P bit. When CC2P = 0, counting up occurs when TI1 is high and counting down occurs when TI1 is low; when CC1P = 1, counting up occurs when TI1 is low and counting down occurs when TI1 is high.

The following diagram illustrates the case where CC1P=CC2P=0:

Figure 18-51 Pulse-Level Encoder Mode（CC1P=CC2P=0）



18.4.21.3 Dual-Pulse Encoder Mode

In the Dual-Pulse encoder mode, the clock is provided on two lines, with only one line provided at a time based on the direction. This results in one clock line for counting up and another clock line for counting down.

This mode is enabled through the SMSEL[3:0] field in the TIMx_SMCTRL register, as follows.

- 1000：Dual-Pulse encoder mode 2, The counter is updated on both the rising and falling edges of any of the two clock line. The CC1P and CC2P bits encode the idle state of the clock. CCxP=0 corresponds to a high-level idle state, while CCxP=1 corresponds to a low-level idle state.
- 1111：Dual-Pulse encoder mode 1, the counter is updated on a single clock edge based on the values of the CC1P and CC2P bits. CCxP = 0 corresponds to the falling edge and high-level state, while CCxP = 1 corresponds to the rising edge and low-level state.

The following table describes the relationship between counting direction, encoder signals, and polarity settings:

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Table 18-15 The Relationship between Counting Direction, Encoder Signals, and Polarity Settings

Dual-Pulse Encoder Mode	SMSEL [3:0]	Level on Opposite Signal (TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rising	Falling	Rising	Falling
Mode 2 CCxP=0	1000	High	Counting down	Counting down	Counting up	Counting up
		Low	Don't count	Don't count	Don't count	Don't count
Mode 2 CCxP=1	1000	High	Don't count	Don't count	Don't count	Don't count
		Low	Counting down	Counting down	Counting up	Counting up
Mode 1 CCxP=0	1111	High	Don't count	Counting down	Don't count	Counting up
		Low	Don't count	Don't count	Don't count	Don't count
Mode 1 CCxP=1	1111	High	Don't count	Don't count	Don't count	Don't count
		Low	Counting down	Don't count	Counting up	Don't count

The following diagram illustrates the counting method of the counter in Dual-Pulse encoder mode:

Figure 18-52 Dual-Pulse Encoder Mode (CC1P = CC2P = 0)

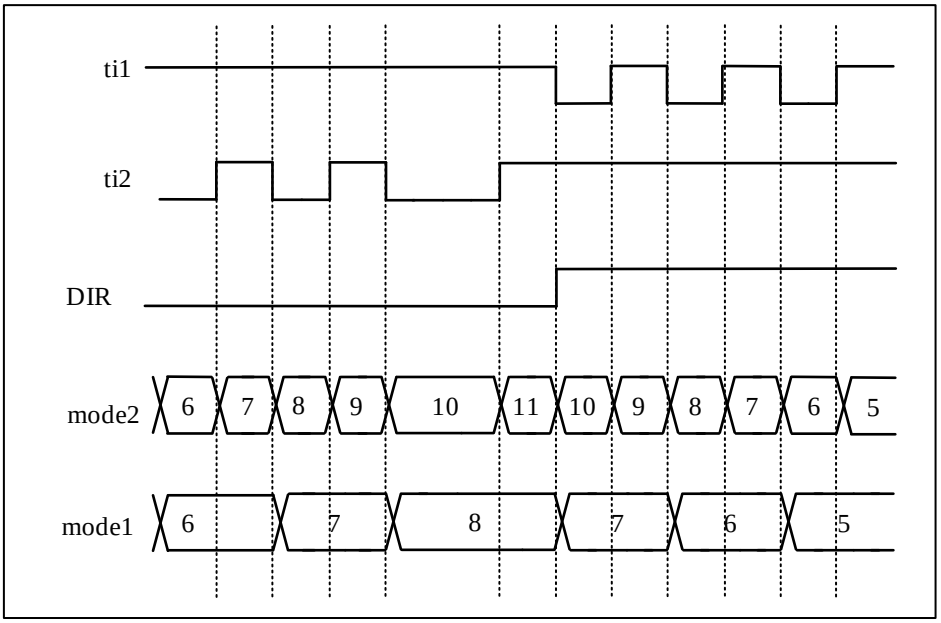

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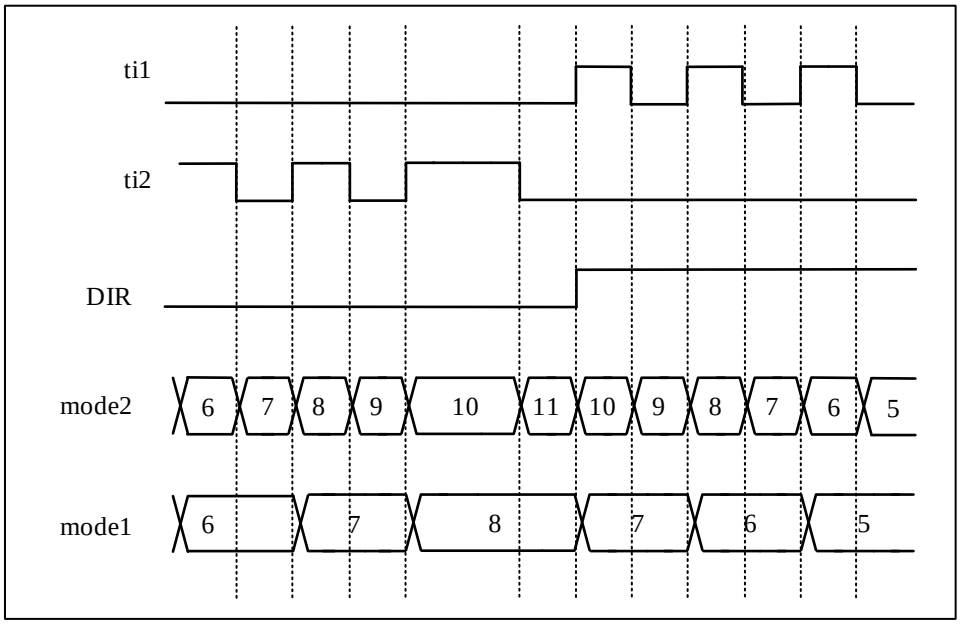
Figure 18-53 Dual-Pulse Encoder Mode (CC1P = CC2P = 1)



18.4.22 Interfacing with Hall Sensor

Connect the Hall sensor to the three input pins (CC1, CC2 and CC3) of the timer, and then select the XOR function to pass the inputs of TIMx_CH1, TIMx_CH2 and TIMx_CH3 through the XOR gate as the output of TI1 to channel 1 for capture signal.

The timer needs to be configured as the reset mode in slave mode (TIMx_SMCTRL.SMSEL= '0100'); the edge of the trigger select TI1 triggers TI1F_ED (TIMx_SMCTRL.TSEL= '100'), any change in the Hall 3 inputs will trigger the counter to recount, so it is used as a time reference; the capture/compare channel 1 is configured to capture the TRC signal in capture mode (TIMx_CCMOD1.CC1SEL= '11'), which is used to calculate the two input time intervals, thereby reflecting the motor speed.

Select timer channel 2 to output pulses to the advanced timer to trigger the COM event of the advanced timer to update the control bits of the output PWM. The trigger selection of the advanced timer needs to select the corresponding internal trigger signal (TIMx_SMCTRL.TSEL="ITRx"), the capture/compare preload control bit needs to be configured to support preload (TIMx_CTRL2.CCPCTL=1) and support the rising edge of TRGI Trigger an update (TIMx_CTRL2.CCUSEL=1).

This example is shown in the following figure.

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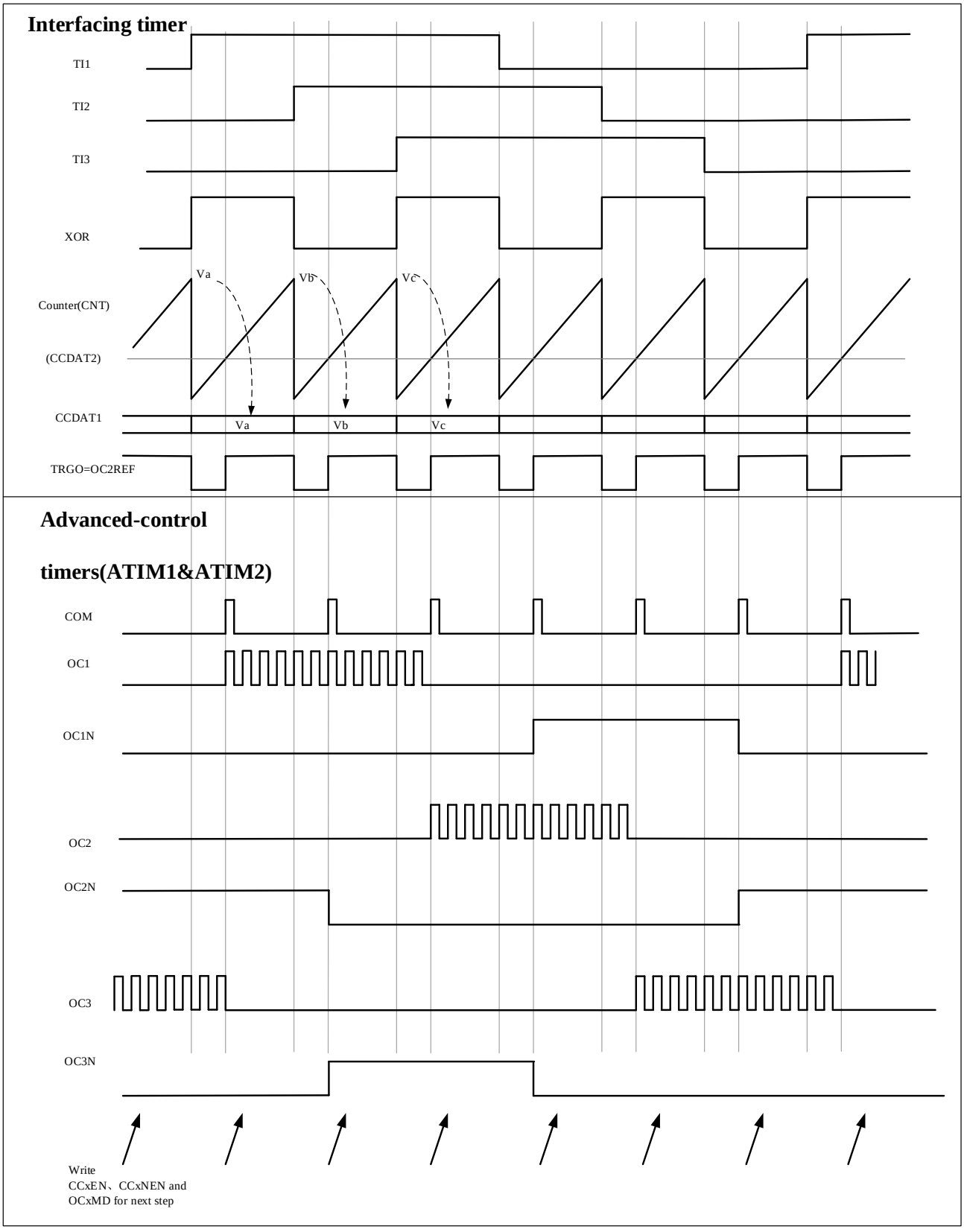
Figure 18-54 Example of Hall Sensor Interface



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18.5 ATIMx Register Description

For abbreviations used in registers, refer to Section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

18.5.1 Control Register 1（TIMx_CTRL1）

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								ASYMMETRIC	Reserved	CMODE[1:0]		Reserved			
								rw		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAMECCERREN	Reserved	CLRSEL	SRAMPARERREN	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
rw		rw	rw	rw	rw	rw	rw	rw		rw	rw	rw		rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	ASYMMETRIC	Asymmetric mode enable in center-aligned mode 0：Disabled 1：Enabled (valid when TIMx_CTRL1.CAMSEL[1:0] is non-zero, each channel will compare to CCDATx when counting up, and compare to CCDDATx when counting down)
22	Reserved	Reserved, the reset value must be maintained
21:20	CMODE	In center-aligned asymmetric mode, channel 4/7/8/9 trigger mode, only when TIMx_CTRL2.MMSEL3 = ‘1xxx’, the TRGO output will be valid. 00：Up-counting to CCDAT4/7/8/9, trigger valid 01：Down-counting, channel 4 count to CCDDAT4, channel 7/8/9 count to CCDAT7/8/9, trigger valid 1x：Channel 4 up-counting to CCDAT4 or down-counting to CCDDAT4, channel 7/8/9 up-counting or down-counting to CCDAT7/8/9, trigger valid In center-aligned symmetry mode, channel 4/7/8/9 trigger mode, only when TIMx_CTRL2.MMSEL3 = ‘1xxx’, the TRGO output will be valid. 00: Up-counting to CCDAT4/7/8/9, trigger valid 01: Down-counting to CCDAT4/7/8/9, trigger valid 1x: Up-counting or down-counting to CCDAT4/7/8/9, trigger valid
19:16	Reserved	Reserved, the reset value must be maintained
15	SMECCERREN	SRAM ECC error break Enable 0: Disable 1: Enable

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Bit Field	Name	Description
		Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.
14	Reserved	Reserved, the reset value must be maintained
13	CLRSEL	OcxRef clear selection 0：Select the external Ocxclr (TIMx_ETR) signal，Specific selection can refer to TIMx_INSEL.ETRS register 1：Select the internal Ocxclr (tim_ocref_clr) signal，Specific selection can refer to TIMx_INSEL.CLRS register
12	SMPARERREN	SRAM parity error break Enable 0: Disable 1: Enable *Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.*
11	PBKPEN	PVD break Enable 0: Disable 1: Enable *Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.*
10	LBKPEN	LockUp break Enable（Core Hardfault） 0: Disable 1: Enable *Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.*
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and DTS (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK_INT}$. 01: $t_{DTS} = 2 \times t_{CK_INT}$ 10: $t_{DTS} = 4 \times t_{CK_INT}$ 11: Reserved, do not use this configuration

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Bit Field	Name	Description
5	UPDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV Enable. UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
1	DIR	Direction 0: Up-counting 1: Down-counting *Note: this bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

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18.5.2 Control Register 2（TIMx_CTRL2）

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				MMSEL2[3:0]				TRIG9	TRIG8	TRIG7	TRIG4	TI1SEL	CCPCTL	CCDSEL	CCUSEL
				rw				rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved	OI6	Reserved	OI5	OI4N	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1
rw					rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	MMSEL2[3:0]	Master mode selection 2 These 4 bits are used to select the synchronization information (TRGO2) sent to the slave timer in the master mode. Possible combinations are as follows: 0000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO2 pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 0001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO2). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO2 except if the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). 0010: Update - The update event is selected as the trigger output (TRGO2). For example, a master timer clock can be used as a slave timer prescaler. 0011: Compare pulse - Triggers the output to send a positive pulse (TRGO2) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 0100: Compare - OC1REF signal is used as the trigger output (TRGO2) 0101: Compare – OC2REF signal is used as the trigger output (TRGO2) 0110: Compare – OC3REF signal is used as the trigger output (TRGO2) 0111: Compare – OC4REF signal is used as the trigger output (TRGO2) 1000: Compare – OC5REF signal is used as the trigger output (TRGO2) 1001: Compare – OC6REF signal is used as the trigger output (TRGO2) 1010: Compare Pulse - OC4REF rising or falling edges generate a positive pulses on TRGO2 1011: Compare Pulse – OC6REF rising or falling edges generate a positive pulses on TRGO2 1100: Compare Pulse - OC4REF rising edges or OC6REF rising edges generate a positive

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Bit Field	Name	Description
		pulses on TRGO2 1101: Compare Pulse - OC4REF rising edges or OC6REF falling edges generate a positive pulses on TRGO2 1110: Compare Pulse – OC5REF rising edges or OC6REF rising edges generate a positive pulses on TRGO2 1111: Compare Pulse – OC5REF rising edges or OC6REF falling edges generate a positive pulses on TRGO2
23	TRIG9	Enable triggering ADC when channel 9 comparison matches 0: Trigger disable 1: Trigger enable
22	TRIG8	Enable triggering ADC when channel 8 comparison matches 0: Trigger disable 1: Trigger enable
21	TRIG7	Enable triggering ADC when channel 7 comparison matches 0: Trigger disable 1: Trigger enable
20	TRIG4	Enable triggering ADC when channel 4 comparison matches 0: Trigger disable 1: Trigger enable
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	CCPCTL	Capture/compare preloaded control 0: CCxEN, CCxNEN and OCxMD bits are not preloaded. 1: CCxEN, CCxNEN and OCxMD bits are preloaded. they are updated only when a commutation event COM occurs (CCUDGN bit set or rising edge on TRGI depending on CCUSEL bit) *Note: this bit only applied to channels with complementary outputs.*
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
16	CCUSEL	Capture/compare control update selection 0: If TIMx_CTRL2.CCPCTL = 1, they can only be updated by setting CCUDGN bit 1: If TIMx_CTRL2.CCPCTL = 1, they can be updated by setting CCUDGN bit or a rising edge on TRGI. *Note: this bit only applied to channels with complementary outputs.*
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 0000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 0001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes

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Bit Field	Name	Description
		you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). 0010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 0011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 0100: Compare - OC1REF signal is used as the trigger output (TRGO). 0101: Compare - OC2REF signal is used as the trigger output (TRGO). 0110: Compare - OC3REF signal is used as the trigger output (TRGO). 0111: Compare - OC4REF signal is used as the trigger output (TRGO). 1xxx: Compare-If the counter is center-aligned mode: The corresponding edge signal of OC4REF/OC7REF/OC8REF/OC9REF used as the trigger output (TRGO), up counting and down counting are configurable, refer specifically to the TIMx_CTRL1.CMODE. If the counter is edge alignment mode: The OC4REF signal is used as the trigger output (TRGO).
11	Reserved	Reserved, the reset value must be maintained
10	OI6	Output idle state 6 (OC6 output). Refer to TIMx_CTRL2.OI1 bit.
9	Reserved	Reserved, the reset value must be maintained
8	OI5	Output idle state 5 (OC5 output). Refer to TIMx_CTRL2.OI1 bit.
7	OI4N	Output idle state 4 (OC4N output). Refer to TIMx_CTRL2.OI1N bit.
6	OI4	Output idle state 4 (OC4 output). Refer to TIMx_CTRL2.OI1 bit.
5	OI3N	Output idle state 3 (OC3N output). Refer to TIMx_CTRL2.OI1N bit.
4	OI3	Output idle state 3 (OC3 output). Refer to TIMx_CTRL2.OI1 bit.
3	OI2N	Output idle state 2 (OC2N output). Refer to TIMx_CTRL2.OI1N bit.
2	OI2	Output idle state 2 (OC2 output). Refer to TIMx_CTRL2.OI1 bit.
1	OI1N	Output Idle state 1 (OC1N Output) 0: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 0 1: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*
0	OI1	Output Idle state 1 0: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 0 1: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 1 *Note: Once TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*

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Email: sales@nsing.com.sg

18.5.3 Status Registers（TIMx_STS）

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					CC9ITF	CC8ITF	CC7ITF	Reserved		SBITF	BITF2	BITF	TITF	COMITF	UDITF
					rc_w0	rc_w0	rc_w0			rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved		CC6ITF	CC5ITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0			rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained
26	CC9ITF	Capture/Compare 9 interrupt flag Refer to TIMx_STS.CC1ITF description.
25	CC8ITF	Capture/Compare 8 interrupt flag Refer to TIMx_STS.CC1ITF description.
24	CC7ITF	Capture/Compare 7 interrupt flag Refer to TIMx_STS.CC1ITF description.
23:22	Reserved	Reserved, the reset value must be maintained
21	SBITF	System break interrupt flag This bit is set by hardware once the system break input is active. This bit is cleared by software when the system break input becomes inactive. 0: No system break event occurred 1: An active level has been detected on system break input
20	BITF2	Break2 interrupt flag This bit is set by hardware once the break2 input is active. This bit is cleared by software when the break2 input becomes inactive. 0: No break2 event occurred 1: An active level has been detected on break2 input
19	BITF	Break1 interrupt flag This bit is set by hardware once the break1 input is active. This bit is cleared by software when the break input becomes inactive. 0: No break1 event occurred 1: An active level has been detected on break1 input
18	TITF	Trigger interrupt flag When a trigger event occurs (when an effective edge is detected at the TRGI input, except in gated mode, or any edge in gated mode) the hardware sets this bit to '1'. It is cleared by software to '0'. 0: No trigger event occurred

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Email: sales@nsing.com.sg

Bit Field	Name	Description
		1: Trigger interrupt pending
17	COMITF	COM interrupt flag This bit is set by hardware once a COM event is generated (when TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_CCMOD1.OCxMD have been updated). This bit is cleared by software. 0: No COM event occurred 1: COM interrupt pending
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, and repeat counter value overflow or underflow (An update event is generated when the repeat counter equals 0). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag Refer to TIMx_STS.CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag Refer to TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag Refer to TIMx_STS.CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7:6	Reserved	Reserved, the reset value must be maintained
5	CC6ITF	Capture/Compare 6 interrupt flag Refer to TIMx_STS.CC1ITF description.
4	CC5ITF	Capture/Compare 5 interrupt flag Refer to TIMx_STS.CC1ITF description.
3	CC4ITF	Capture/Compare 4 interrupt flag Refer to TIMx_STS.CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag Refer to TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag

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Bit Field	Name	Description
		Refer to TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **If channel CC1 is configured as an output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **If channel CC1 is configured as an input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

18.5.4 Event Generation Registers（TIMx_EVTGEN）

Offset address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			BGN2	BGN	TGN	CCUDGN	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
			w	w	w	w	w					w	w	w	w

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	BGN2	Break2 generation This bit can generate a break2 event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF2 = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a break2 event

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Email: sales@nsing.com.sg

Bit Field	Name	Description
11	BGN	Break1 generation This bit can generate a break1 event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a break1 event
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
9	CCUDGN	Capture/Compare control update generation This bit is set by software. And if TIMx_CTRL2.CCPCTL = 1 at this time, the CCxEN, CCxNEN and OCxMD bits are allowed to be updated. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event *Note: This bit is only valid for channels with complementary outputs.*
8	UDGN	Update generation This bit is set to '1' by software and automatically cleared to '0' by hardware. This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.

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Email: sales@nsing.com.sg

Bit Field	Name	Description
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be set to 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be set to 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If the TIMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

18.5.5 Slave Mode Control Register（TIMx_SMCTRL）

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								OCREFCLRF[3:0]				OCREF CLRP	Reserved		MSMD
									rw			rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS[1:0]		SMSEL[3:0]				Reserved	TSEL[2:0]		
rw				rw	rw	rw		rw					rw		

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	OCREFCLRF[3:0]	tim_ocref_clr signal filter These bits are used to define the frequency at which the tim_ocref_clr signal is sampled and the bandwidth of the tim_ocref_clr digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

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19	OCREFCLRP	tim_ocref_clr signal polarity This bit is used to select whether the trigger operation is to use tim_ocref_clr or the inversion of tim_ocref_clr. 0: tim_ocref_clr active at high level or rising edge. 1: tim_ocref_clr active at low level or falling edge.
18:17	Reserved	Reserved, the reset value must be maintained
16	MSMD	Master/slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: fSAMPLING=fDTS/8, N=6 0001: fSAMPLING=fCK_INT, N=2 1001: fSAMPLING=fDTS/8, N=8 0010: fSAMPLING=fCK_INT, N=4 1010: fSAMPLING=fDTS/16, N=5 0011: fSAMPLING=fCK_INT, N=8 1011: fSAMPLING=fDTS/16, N=6 0100: fSAMPLING=fDTS/2, N=6 1100: fSAMPLING=fDTS/16, N=8 0101: fSAMPLING=fDTS/2, N=8 1101: fSAMPLING=fDTS/32, N=5 0110: fSAMPLING=fDTS/4, N=6 1110: fSAMPLING=fDTS/32, N=6 0111: fSAMPLING=fDTS/4, N=8 1111: fSAMPLING=fDTS/32, N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: the following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 0111 and TIMx_SMCTRL.TSEL = 111).*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency.

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Email: sales@nsing.com.sg

		When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
7:4	SMSEL[3:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (refer to input control register and control register description) 0000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 0001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 0010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 0011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 0100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 0101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 0110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 0111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). 1000: Dual-Pulse encoder mode 2 1001: Quadrature encoder mode 4 - The counter counts up/down on the edge of TI1FP1 based on the level of TI2FP2. The counting edge is selected by CC1P. 1010: Quadrature encoder mode 5 - The counter counts up/down on the edge of TI2FP2 based on the level of TI1FP1. The counting edge is selected by CC2P. 1011: Pulse-Level encoder mode 2 1100: Pulse-Level encoder mode 1. Set the counting edge of TI2FP2 through CC2P. 1101: Combined Gated + Reset mode, the counter is enabled when the trigger input (TRGI) is high. Once the trigger input goes low, the counter stops (and resets). The start and stop of the counter are both controlled. 1110: Combined Reset + Trigger Mode - The counter starts (and resets) on the rising edge of the trigger input TRGI, only the start of the counter is controlled. 1111: Dual-Pulse encoder mode 1. Set the counting edge of TI1FP1 and TI2FP2 through CC1P and CC2P.

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Email: sales@nsing.com.sg

		Note: do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.
3	Reserved	Reserved, the reset value must be maintained
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 0xx: Internal trigger (ITRx) , Select the ITR signal source based on TIMx_INSEL. 100: TI1 edge detector (TI1F_ED) 101: Filtered timer input 1 (TI1FP1) 110: Filtered timer input 2 (TI2FP2) 111: External triggered Input (ETRF) *Note: these bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*

18.5.6 DMA/Interrupt Enable Registers（TIMx_DINTEN）

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CC9IEN	COMIEN	TDEN	COMDEN	UDEN	BIEN	TIEN	UIEN
								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	CC8IEN	CC7IEN	CC6IEN	CC5IEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
23	CC9IEN	Capture/Compare 9 interrupt enable 0: Disable capture/compare 9 interrupt 1: Enable capture/compare 9 interrupt
22	COMIEN	COM interrupt enable 0: Disable COM interrupt 1: Enable COM interrupt
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
20	COMDEN	COM DMA request enable 0: Disable COM DMA request 1: Enable COM DMA request

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Email: sales@nsing.com.sg

Bit Field	Name	Description
19	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
18	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7	CC8IEN	Capture/Compare 8 interrupt enable 0: Disable capture/compare 8 interrupt 1: Enable capture/compare 8 interrupt
6	CC7IEN	Capture/Compare 7 interrupt enable 0: Disable capture/compare 7 interrupt 1: Enable capture/compare 7 interrupt
5	CC6IEN	Capture/Compare 6 interrupt enable 0: Disable capture/compare 6 interrupt 1: Enable capture/compare 6 interrupt
4	CC5IEN	Capture/Compare 5 interrupt enable 0: Disable capture/compare 5 interrupt 1: Enable capture/compare 5 interrupt
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt

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Email: sales@nsing.com.sg

Bit Field	Name	Description
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 terrupt 1: Enable capture/compare 3 nterrupt
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 nterrupt 1: Enable capture/compare 2 nterrupt
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 nterrupt 1: Enable capture/compare 1 nterrupt

18.5.7 Capture/Compare Mode Register 1（TIMx_CCMOD1）

Offset address: 0x18

Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL.

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Email: sales@nsing.com.sg

Bit Field	Name	Description
		Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by tim_ocref_clr_in input level 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high (tim_ocref_clr_in is controlled by the TIMx_CTRL1.CLRSEL register).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register.

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Email: sales@nsing.com.sg

Bit Field	Name	Description
		Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.
1:0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input Capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 1000: $f_{SAMPLING}=f_{DTS}/8$，N=6 0001: $f_{SAMPLING}=f_{CK_INT}$，N=2 1001: $f_{SAMPLING}=f_{DTS}/8$，N=8 0010: $f_{SAMPLING}=f_{CK_INT}$，N=4 1010: $f_{SAMPLING}=f_{DTS}/16$，N=5 0011: $f_{SAMPLING}=f_{CK_INT}$，N=8 1011: $f_{SAMPLING}=f_{DTS}/16$，N=6 0100: $f_{SAMPLING}=f_{DTS}/2$，N=6 1100: $f_{SAMPLING}=f_{DTS}/16$，N=8

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		0101: $f_{SAMPLING}=f_{DTS}/2$，N=8 0110: $f_{SAMPLING}=f_{DTS}/4$，N=6 0111: $f_{SAMPLING}=f_{DTS}/4$，N=8 1101: $f_{SAMPLING}=f_{DTS}/32$，N=5 1110: $f_{SAMPLING}=f_{DTS}/32$，N=6 1111: $f_{SAMPLING}=f_{DTS}/32$，N=8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

18.5.8 Capture/Compare Mode Register 2（TIMx_CCMOD2）

Offset address: 0x1C

Reset value: 0x0000 0000

Refer to the description of the CCMOD1 register above.

Output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode
12	OC4CEN	Output compare 4 clear enable

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

18.5.9 Capture/Compare Mode Register 3（TIMx_CCMOD3）

Offset address: 0x20

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							OC9PEN	Reserved			OC8PEN	Reserved			OC7PEN
							rw				rw				rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC6MD[2:0]			OC6CEN	OC6FEN	OC6PEN	Reserved		OC5MD[2:0]			OC5CEN	OC5FEN	OC5PEN	Reserved	
rw			rw	rw	rw			rw			rw	rw	rw		

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	OC9PEN	Output compare 9 preload enable
23:21	Reserved	Reserved, the reset value must be maintained
20	OC8PEN	Output compare 8 preload enable
19:17	Reserved	Reserved, the reset value must be maintained
16	OC7PEN	Output compare 7 preload enable
15:13	OC6MD[2:0]	Output compare 6 mode

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Bit Field	Name	Description
12	OC6CEN	Output compare 6 clear enable
11	OC6FEN	Output compare 6 fast enable
10	OC6PEN	Output compare 6 preload enable
9:8	Reserved	Reserved, the reset value must be maintained
7:5	OC5MD[2:0]	Output compare 5 mode
4	OC5CEN	Output compare 5 clear enable
3	OC5FEN	Output compare 5 fast enable
2	OC5PEN	Output compare 5 preload enable
1:0	Reserved	Reserved, the reset value must be maintained

18.5.10 Capture/Compare Enable Registers（TIMx_CCEN）

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CC6P	CC6EN	Reserved		CC5P	CC5EN	Reserved	
								rw	rw			rw	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	CC4NP	CC4NEN	CC3P	CC3EN	CC3NP	CC3NEN	CC2P	CC2EN	CC2NP	CC2NEN	CC1P	CC1EN	CC1NP	CC1NEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	CC6P	Capture/Compare 6 output polarity See TIMx_CCEN.CC1P description.
22	CC6EN	Capture/Compare 6 output enable See TIMx_CCEN.CC1EN description.
21:20	Reserved	Reserved, the reset value must be maintained
19	CC5P	Capture/Compare 5 output polarity See TIMx_CCEN.CC1P description.
18	CC5EN	Capture/Compare 5 output enable See TIMx_CCEN.CC1EN description.
17：16	Reserved	Reserved, the reset value must be maintained
15	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
14	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.

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Bit Field	Name	Description
13	CC4NP	Capture/Compare 4 complementary output polarity See TIMx_CCEN.CC1NP description.
12	CC4NEN	Capture/Compare 4 complementary output enable See TIMx_CCEN.CC1NEN description.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
9	CC3NP	Capture/Compare 3 complementary output polarity See TIMx_CCEN.CC1NP description.
8	CC3NEN	Capture/Compare 3 complementary output enable See TIMx_CCEN.CC1NEN description.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5	CC2NP	Capture/Compare 2 complementary output polarity See TIMx_CCEN.CC1NP description.
4	CC2NEN	Capture/Compare 2 complementary output enable See TIMx_CCEN.CC1NEN description.
3	CC1P	Capture/Compare 1 output polarity **When the corresponding channel of CC1 is in output mode:** 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: If TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. The level of OC1 depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. 1: Enable - Enable output OC1 signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. **When the corresponding channel of CC1 is in input mode:**

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Bit Field	Name	Description
		At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N active high 1: OC1N active low
0	CC1NEN	Capture/Compare 1 complementary output enable 0: Disable - Disable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN. 1: Enable - Enable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN.

Table 18-16 Output Control Bits Of Complementary OCx And OCxN Channels With Break Function

Control Bits					Output State (1)	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output State	OCxN Output State
1	X	0	0	0	Output disabled（not driven by timer） OCx=0，OCx_EN=0	Output disabled（not driven by timer） OCxN=0，OCxN_EN=0
		0	0	1	Output disabled（not driven by timer） OCx=0，OCx_EN=0	OCxREF + polarity OCxN= OCxREF xor CCxNP， OCxN_EN=1
		0	1	0	OCxREF + polarity OCx= OCxREF xor CCxP， OCx_EN=1	Output disabled（not driven by timer） OCxN=0，OCxN_EN=0
		0	1	1	OCxREF + polarity + dead-time, OCx_EN=1	Complementary to OCxREF + polarity + dead-time , OCxN_EN=1
		1	0	0	Output disabled（not driven by timer） OCx=CCxP，OCx_EN=0	Output disabled（not driven by timer） OCxN=CCxNP，OCxN_EN=0
		1	0	1	Off-state (Output enabled with inactive state) OCx=CCxP，OCx_EN=1	OCxREF + polarity OCxN= OCxREF xor CCxNP， OCxN_EN=1
		1	1	0	OCxREF + polarity OCx= OCxREF xor CCxP， OCx_EN=1	Off-state (Output enabled with inactive state) OCxN=CCxNP，OCxN_EN=1

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		1	1	1	OCxREF + polarity + dead-time OCx_EN=1	Complementary to OCxREF + polarity + dead-time OCxN_EN=1
0	0	X	0	0	Output disabled（not driven by timer） Asynchronously: OCx=CCxP, OCx_EN=0, OCxN=CCxNP,OCxN_EN=0; If clock exists: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0， OCx=OIx, OCxN=OIxN after a dead-time	
	0		0	1		
	0		1	0		
	0		1	1		
	1		0	0	Off-state (Output enabled with inactive state) Asynchronously: OCx=CCxP, OCx_EN=1, OCxN=CCxNP,OCxN_EN=1; If clock exists: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0， OCx=OIx , OCxN=OIxN after a dead-time	
	1		0	1		
	1		1	0		
	1		1	1		

1. If both outputs of a channel are not used (CCxEN = CCxNEN = 0), OIx, OIxN, CCxP and CCxNP must all be cleared.

Note: the status of external I/O pins connected to complementary OCx and OCxN channels depends on the OCx and OCxN channel states and GPIO and AFIO registers.

18.5.11 Capture/Compare Register 1（TIMx_CCDAT1）

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT1[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															
rw															

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Bit Field	Name	Description
31:16	CCDDAT1[15:0]	Capture/Compare 1 down-counting value, dedicated to center-aligned asymmetric mode. ■ CC1 channel can only configured as output: CCDDAT1 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT1[15:0]	Capture/Compare 1 value ■ CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 and CCDDAT1 are only readable. When configured as output mode, register CCDAT1 and CCDDAT1 are readable and writable.

18.5.12 Capture/Compare Register 2（TIMx_CCDAT2）

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT2[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[15:0]															
rw															

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Bit Field	Name	Description
31:16	CCDDAT2[15:0]	Capture/Compare 2 down-counting value, dedicated to center-aligned asymmetric mode ■ CC2 channel can only configured as output: CCDDAT2 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT2[15:0]	Capture/Compare 2 value ■ CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 and CCDDAT2 are only readable. When configured as output mode, register CCDAT2 and CCDDAT2 are readable and writable.

18.5.13 Capture/Compare Register 3（TIMx_CCDAT3）

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT3[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															
rw															

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Bit Field	Name	Description
31:16	CCDDAT3[15:0]	Capture/Compare 3 down-counting value, dedicated to center-aligned asymmetric mode ■ CC3 channel can only configured as output: CCDDAT3 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.
15:0	CCDAT3[15:0]	Capture/Compare 3 value ■ CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signal is sent out on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 and CCDDAT3 are only readable. When configured as output mode, register CCDAT3 and CCDDAT3 are readable and writable.

18.5.14 Capture/Compare Register 4（TIMx_CCDAT4）

Offset address: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT4[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT4[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT4[15:0]	Capture/Compare 4 down-counting value, dedicated to center-aligned asymmetric mode ■ CC4 channel can only configured as output: CCDDAT4 contains the value to be compared to the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the

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		active register only when an update event occurs.
15:0	CCDAT4[15:0]	Capture/Compare 4 value ■ CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT (except when TIMx_CTRL1.DIR = 1 and in asymmetric mode), signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 and CCDDAT4 are only readable. When configured as output mode, register CCDAT4 and CCDDAT4 are readable and writable.

18.5.15 Capture/Compare Register 5（TIMx_CCDAT5）

Offset address: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT5[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT5[15:0]	Capture/Compare 5 value ■ CC5 channel can only configured as output: CCDAT5 contains the value to be compared with the counter TIMx_CNT, and signal is sent out on the OC5 output. If the preload function is not selected in the TIMx_CCMOD3.OC5PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. CC5 is used for comparator blanking.

18.5.16 Capture/Compare Register 6（TIMx_CCDAT6）

Offset address: 0x3C

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT6[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT6[15:0]	Capture/Compare 6 value ■ CC6 channel can only configured as output: CCDAT6 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on the OC6 output. If the preload function is not selected in the TIMx_CCMOD3.OC6PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

18.5.17 Prescaler（TIMx_PSC）

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK_CNT} = f_{CK_PSC}/ (PSC [15:0] +1)$. The PSC value is loaded into the shadow register of the prescaler each time an update event occurs.

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18.5.18 Auto-Reload Register（TIMx_AR）

Offset address: 0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	AR[15:0]	Auto-reload value AR contains the value to be loaded into the actual auto-reload register. Refer to section18.4.1 for details on the update and action of AR. When the value for auto-reload is empty, the counter will not operate.

18.5.19 Counters（TIMx_CNT）

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CNT[15:0]	Counter value

18.5.20 Repeat Count Registers（TIMx_REPCNT）

Offset address: 0x4C

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								REPCNT[7:0]							
								rw							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value Repetition counter is used to generate the update event or update the timer registers only after a given number (N+1) cycles of the counter, where N is the value of TIMx_REPCNT.REPCNT . The repetition counter is decremented at each counter overflow in up-counting mode, at each counter underflow in down-counting mode or at each counter overflow and at each counter underflow in center-aligned mode. Setting the TIMx_EVTGEN.UDGN bit will reload the content of TIMx_REPCNT.REPCNT and generate an update event.

18.5.21 Break and Dead-Time Registers（TIMx_BKDT）

Offset address: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										BRK2BID	BRKBID	BRK2 DSRM	BRK DSRM	BK2EN	BK2P
										rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCKCFG[1:0]		OSSR	OSSI	BKEN	BKP	AOEN	MOEN	DTGN[7:0]							
rw		rw	rw	rw	rw	rw	rw	rw							

Note: BRK2BID、BRKBID、BK2EN、BK2P、AOEN、BKP、BKEN、OSSI、OSSR and DTGN[7:0] bits can all be write protected depending on the LOCK configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	BRK2BID	Break2 bidirectional enable 0: Break 2 is in input mode. 1: Break 2 is in bidirectional mode. In bidirectional mode, the break 2 input is configured in input and open-drain output modes. Any break 2 event will generate a low level on the break 2 input IO, indicating an internal break 2 event to the external device.

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		Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified. *Note: Any write operation on this bit will take effect after a delay of one APB clock cycle.*
20	BRKBID	Break1 bidirectional enable 0: Break 1 is in input mode. 1: Break 1 is in bidirectional mode. In bidirectional mode, the break 1 input is configured in input and open-drain output modes. Any break 1 event will generate a low level on the break 1 input IO, indicating an internal break 1 event to the external device. *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.* *Note: Any write operation on this bit will take effect after a delay of one APB clock cycle.*
19	BRK2DSRM	Break 2 disarm 0: Break 2 input is armed 1: Break 2 input is disarmed When the break 2 input is invalid, this bit is automatically cleared by the hardware. BRK2DSRM is set by software to release the bidirectional output control of break 2 (open-drain output in high-impedance state), and then software polls this bit until it is reset by hardware, indicating that the break 2 event has disappeared. *Note: Any write operation on this bit will take effect after a delay of one APB clock cycle.*
18	BRKDSRM	Break 1 disarm 0: Break 1 input is armed 1: Break 1 input is disarmed When the break 1 input is invalid, this bit is automatically cleared by the hardware. BRKDSRM is set by software to release the bidirectional output control of break 1 (open-drain output in high-impedance state), and then software polls this bit until it is reset by hardware, indicating that the break 1 event has disappeared. *Note: Any write operation on this bit will take effect after a delay of one APB clock cycle.*
17	BK2EN	Break 2 enable. This bit enables the entire break 2 protection circuit. 0: Disable break 2 input 0: Enable break 2 input *Note: Break 2 can only be used when OSSI=OSSR=1.* *Note: When LOCK level 1 is set (LCKCFG bit in the TIMx_BKDT register), this bit cannot be modified.* *Note: Any write operation on this bit will take effect after a delay of one APB clock cycle.*
16	BK2P	Break 2 polarity 0: Low level of the break 2 input is valid 1: High level of the break 2 input is valid *Note: When LOCK level 1 is set (LCKCFG bit in the TIMx_BKDT register), this bit cannot be modified.* *Note: Any write operation on this bit will take effect after a delay of one APB clock cycle.*
15:14	LCKCFG[1:0]	Lock configuration. This bit provides write protection to prevent software errors. These bits offer a write protection against software errors.

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		00: – No write protected. 01： – LOCK Level 1 TIMx_BKDT.DTGN、TIMx_BKDT.BKEN、TIMx_BKDT.BKP、TIMx_BKDT.AOEN、TIMx_CTRL2.OIx、TIMx_CTRL2.OIxN bits enable write protection. 10： – LOCK Level 2 Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection 11: – LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: After the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
13	OSSR	Off-state Selection for Run Mode This bit is used when TIMx_BKDT.MOEN=1 and the channel is a complementary output. The OSSR bit does not exist in timer without complementary outputs. 0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal = 0) 1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxEN = 1 or CCxNEN = 1. Then, OC/OCN enable output signal = 1 For more details, See Section 18.5.9 capture/compare enable registers (TIMx_CCEN)。
12	OSSI	Off-state selection for Idle mode This bit is used when TIMx_BKDT.MOEN=0 and the channels configured as outputs. 0: When inactive, OC/OCN outputs are disabled (OC/OCN enable output signal = 0) 1: When inactive, OC/OCN outputs are forced with their with their idle level as soon as CCxEN = 1 or CCxNEN = 1. Then, OC/OCN enable output signal = 1 For more details, See Section 18.5.9 capture/compare enable registers (TIMx_CCEN)。
11	BKEN	Break1 enable 0: Disable break 1 input 1: Enable break 1 input *Note: Any write to this bit requires an APB clock delay to take effect.*
10	BKP	Break1 polarity 0: Low level of the break 1 input is valid 1: High level of the break 1 input is valid *Note: Any write to this bit requires an APB clock delay to take effect.*
9	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.

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8	MOEN	Main output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the break input is active. It is only valid for channels configured as outputs. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set.For more details, see Section 18.5.9 Capture/Compare enable registers (TIMx_CCEN)。
7:0	DTGN[7:0]	Dead-time generator setup These bits define the dead-time duration between inserted complementary outputs. The relationship between the DTGN value and the dead time is as follows: DTGN[7:5]=0xx => DT=DTGN[7:0] × T_{dtgn}， T_{dtgn} = T_{DTS}； DTGN[7:5]=10x => DT=(64+DTGN[5:0]) × T_{dtgn}， T_{dtgn} = 2 × T_{DTS}； DTGN[7:5]=110 => DT=(32+DTGN[4:0]) × T_{dtgn}， T_{dtgn} = 8 × T_{DTS}； DTGN[7:5]=111 => DT=(32+DTGN[4:0])× T_{dtgn}， T_{dtgn} = 16 × T_{DTS}；

18.5.22 Capture/Compare Register 7（TIMx_CCDAT7）

Offset address: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT7[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT7[15:0]	Capture/Compare 7 value ■ CC7 channel can only configured as output: CCDAT7 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC7 output. If the preload function is not selected in the TIMx_CCMOD3.OC7PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

18.5.23 Capture/Compare Register 8（TIMx_CCDAT8）

Offset address: 0x58

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT8[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT8[15:0]	Capture/Compare 8 value ■ CC7 channel can only configured as output: CCDAT8 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC8 output. If the preload function is not selected in the TIMx_CCMOD3.OC8PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

18.5.24 Capture/Compare Register 9（TIMx_CCDAT9）

Offset address: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT9[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT9[15:0]	Capture/Compare 9 value ■ CC7 channel can only configured as output: CCDAT9 contains the value to be compared with the counter TIMx_CNT, and signals are sent out on OC9 output. If the preload function is not selected in the TIMx_CCMOD3.OC9PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs.

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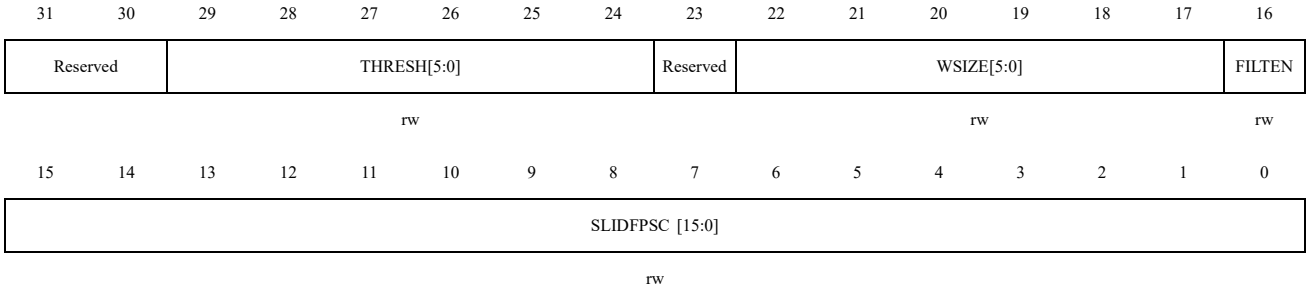
18.5.25 Break 1 Filter Register（TIMx_BKFR）

Offset address: 0x60

Reset value: 0x0000 0000



Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold number of sample logic level to be valid, maximum 63: Threshold value for a valid logic level. Within sample window if number of logic high is more than or equal to threshold value, next logic level will be logic high. Same rule applies to logic low. If both number of 1's and 0's inside window are smaller than threshold, filter output stays unchanged. Threshold value should set to more than or equal to half of window value. Recommend threshold range is: **Minimum**: 1 pre-scale clock cycle more than ceiling value of max glitch size (in pre-scale clock cycle) and need to larger than half of window size. for example, if glitch size is 3.2*(pre-scale clock period), threshold should be ┌3.2┐= 4 + 1 =5 **Maximum**: floor value of minimum size of valid signal (in pre-scale clock cycle) and need to be smaller than window size. For example, if minimum message size is 3.2*(pre-scale clock period), threshold should be floor (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	Window size value for logic level check, maximum 63: Window size decides how many sampled values will take into consideration for getting next logic level. Build-in FIFO is 64 bits with maximum index 63 which can only set window size to be 63.
16	FILTEN	Filter enable 0: Disable filter 1: Enable filter
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a 65535 division (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the valid values of the sampling points are considered for logical level calculation. By configuring these bits, the sampling clock division for break 1 input sliding filter and break 2 input

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		sliding filter can be determined.

18.5.26 Input Selection Register（TIMx_INSEL）

Offset address: 0x78

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				CLRS[3:0]				ITRS[3:0]				ETRS[3:0]			
				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TI4S[3:0]				TI3S[3:0]				TI2S[3:0]				TI1S[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	CLRS[3:0]	Selects tim_ocref_clr input signal 0000：tim_ocref_clr0 0001：tim_ocref_clr1 … 1111 ： tim_ocref_clr15 *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.*
23:20	ITRS[3:0]	Selects tim_itr input signal 0000：tim_itr0 0001：tim_itr1 … 1111 ： tim_itr15
19:16	ETRS[3:0]	Selects tim_etr input signal 0000：tim_etr0 0001：tim_etr1 … 1111 ： tim_etr15 *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.*
15:12	TI4S[3:0]	Selects tim_ti4[15:0] input signal 0000：tim_ti4_in0 0001：tim_ti4_in1 … 1111 ： tim_ti4_in15
11:8	TI3S[3:0]	Selects tim_ti3[15:0] input signal

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		0000：tim_ti3_in0 0001：tim_ti3_in1 … 1111 ： tim_ti3_in15
7:4	TI2S[3:0]	Selects tim_ti2[15:0] input signal 0000：tim_ti2_in0 0001：tim_ti2_in1 … 1111 ： tim_ti2_in15
3:0	TI1S[3:0]	Selects tim_ti1[15:0] input signal 0000：tim_ti1_in0 0001：tim_ti1_in1 … 1111 ： tim_ti1_in15

18.5.27 Alternate Function Option Register 1（TIMx_AF1）

Offset address: 0x7C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				DSMU3BRKEN	DSMU2BRKEN	DSMU1BRKEN	DSMU0BRKEN	Reserved							
				rw	rw	rw	rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		COMP4BRKP	COMP3BRKP	COMP2BRKP	COMP1BRKP	IOMBRKP	Reserved				COMP4BRKEN	COMP3BRKEN	COMP2BRKEN	COMP1BRKEN	IOMBRKEN
		rw	rw	rw	rw	rw					rw	rw	rw	rw	rw

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	DSMU3BRKEN	tim_brk_dsmu3 input enable 0：tim_brk_dsmu3 input disabled 1：tim_brk_dsmu3 input enabled
26	DSMU2BRKEN	tim_brk_dsmu2 input enable 0：tim_brk_dsmu2 input disabled 1：tim_brk_dsmu2 input enabled
25	DSMU1BRKEN	tim_brk_dsmu1 input enable 0：tim_brk_dsmu1 input disabled 1：tim_brk_dsmu1 input enabled
24	DSMU0BRKEN	tim_brk_dsmu0 input enable 0：tim_brk_dsmu0 input disabled

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		1：tim_brk_dsmu0 input enabled
23:14	Reserved	Reserved, the reset value must be maintained
13	COMP4BRKP	tim_brk_comp4 input polarity 0：tim_brk_comp4 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：tim_brk_comp4 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
12	COMP3BRKP	tim_brk_comp3 input polarity 0：tim_brk_comp3 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：tim_brk_comp3 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
11	COMP2BRKP	tim_brk_comp2 input polarity 0：tim_brk_comp2 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：tim_brk_comp2 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
10	COMP1BRKP	tim_brk_comp1 input polarity 0：tim_brk_comp1 input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：tim_brk_comp1 input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
9	IOMBRKP	TIMx_BKIN input polarity 0：TIMx_BKIN input polarity is not inverted (active low if BKP = 0, active high if BKP = 1) 1：TIMx_BKIN input polarity is inverted (active high if BKP = 0, active low if BKP = 1)
8:5	Reserved	Reserved, the reset value must be maintained
4	COMP4BRKEN	tim_brk_comp4 input enable 0：tim_brk_comp4 input disabled 1：tim_brk_comp4 input enabled
3	COMP3BRKEN	tim_brk_comp3 input enable 0：tim_brk_comp3 input disabled 1：tim_brk_comp3 input enabled
2	COMP2BRKEN	tim_brk_comp2 input enable 0：tim_brk_comp2 input disabled 1：tim_brk_comp2 input enabled
1	COMP1BRKEN	tim_brk_comp1 input enable 0：tim_brk_comp1 input disabled 1：tim_brk_comp1 input enabled
0	IOMBRKEN	TIMx_BKIN input enable 0：TIMx_BKIN input disabled 1：TIMx_BKIN input enabled

18.5.28 Alternate Function Option Register 2（TIMx_AF2）

Offset address: 0x80

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				DSMU3BRK2EN	DSMU2BRK2EN	DSMU1BRK2EN	DSMU0BRK2EN	Reserved							
				rw	rw	rw	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	COMP4 BRK2P	COMP3 BRK2P	COMP2 BRK2P	COMP1 BRK2P	IOM BRK2P	Reserved	COMP4 BRK2EN	COMP3 BRK2EN	COMP2 BRK2EN	COMP1 BRK2EN	IOM BRK2EN
	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	DSMU3BRK2EN	tim_brk2_dsmu3 input enable 0：tim_brk2_dsmu3 input disabled 1：tim_brk2_dsmu3 input enabled
26	DSMU2BRK2EN	tim_brk2_dsmu2 input enable 0：tim_brk2_dsmu2 input disabled 1：tim_brk2_dsmu2 input enabled
25	DSMU1BRK2EN	tim_brk2_dsmu1 input enable 0：tim_brk2_dsmu1 input disabled 1：tim_brk2_dsmu1 input enabled
24	DSMU0BRK2EN	tim_brk2_dsmu0 input enable 0：tim_brk2_dsmu0 input disabled 1：tim_brk2_dsmu0 input enabled
23:14	Reserved	Reserved, the reset value must be maintained
13	COMP4BRK2P	tim_brk2_comp4 input polarity 0：tim_brk2_comp4 input polarity is not inverted (active low if BK2P = 0, active high if BK2P = 1) 1：tim_brk2_comp4 input polarity is inverted (active high if BK2P = 0, active low if BK2P = 1)
12	COMP3BRK2P	tim_brk2_comp3 input polarity 0：tim_brk2_comp3 input polarity is not inverted (active low if BK2P = 0, active high if BK2P = 1) 1：tim_brk2_comp3 input polarity is inverted (active high if BK2P = 0, active low if BK2P = 1)
11	COMP2BRK2P	tim_brk2_comp2 input polarity 0：tim_brk2_comp2 input polarity is not inverted (active low if BK2P = 0, active high if BK2P = 1) 1：tim_brk2_comp2 input polarity is inverted (active high if BK2P = 0, active low if BK2P = 1)
10	COMP1BRK2P	tim_brk2_comp1 input polarity 0：tim_brk2_comp1 input polarity is not inverted (active low if BK2P = 0, active high if BK2P = 1) 1：tim_brk2_comp1 input polarity is inverted (active high if BK2P = 0, active low if BK2P = 1)
9	IOMBRK2P	TIMx_BKIN2 input polarity 0：TIMx_BKIN2 input polarity is not inverted (active low if BK2P = 0, active high if BK2P = 1) 1：TIMx_BKIN2 input polarity is inverted (active high if BK2P = 0, active low if BK2P = 1)
8:5	Reserved	Reserved, the reset value must be maintained
4	COMP4BRK2EN	tim_brk2_comp4 input enable 0：tim_brk2_comp4 input disabled 1：tim_brk2_comp4 input enabled

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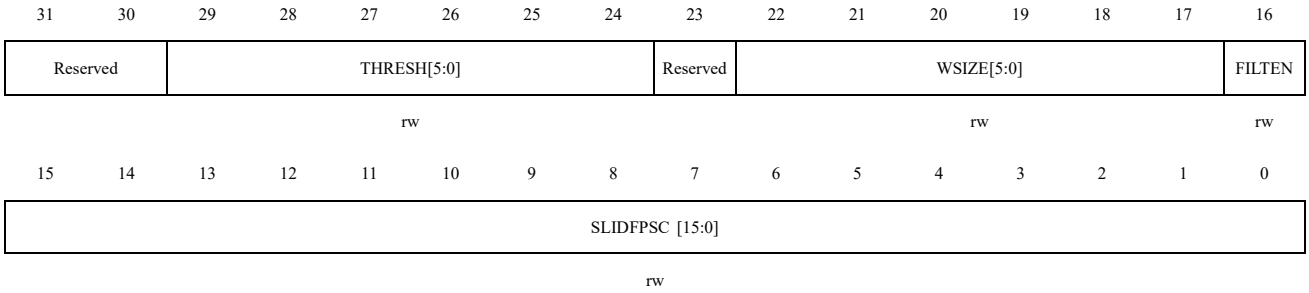
3	COMP3BRK2EN	tim_brk2_comp3 input enable 0：tim_brk2_comp3 input disabled 1：tim_brk2_comp3 input enabled
2	COMP2BRK2EN	tim_brk2_comp2 input enable 0：tim_brk2_comp2 input disabled 1：tim_brk2_comp2 input enabled
1	COMP1BRK2EN	tim_brk2_comp1 input enable 0：tim_brk2_comp1 input disabled 1：tim_brk2_comp1 input enabled
0	IOMBRK2EN	TIMx_BKIN2 input enable 0：TIMx_BKIN2 input disabled 1：TIMx_BKIN2 input enabled

18.5.29 Break 2 Filter Register（TIMx_ BKFR2）

Offset address: 0x84

Reset value: 0x0000 0000



Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH2[5:0]	Threshold number of sample logic level to be valid, maximum 63: Threshold value for a valid logic level. Within sample window if number of logic high is more than or equal to threshold value, next logic level will be logic high. Same rule applies to logic low. If both number of 1's and 0's inside window are smaller than threshold, filter output stays unchanged. Threshold value should set to more than or equal to half of Window value. Recommend threshold range is: **Minimum:** 1 pre-scale clock cycle more than ceiling value of max glitch size (in pre-scale clock cycle) and need to larger than half of window size. for example, if glitch size is 3.2*(pre-scale clock period), threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum:** floor value of minimum size of valid signal (in pre-scale clock cycle) and need to be smaller than window size. For example, if minimum message size is 3.2*(pre-scale clock period), threshold should be floor (3.2) = 3.

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23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE2[5:0]	Window size value for logic level check, maximum 63: Window size decides how many sampled values will take into consideration for getting next logic level. Build-in FIFO is 64 bits with maximum index 63 which can only set window size to be 63.
16	FILTEN2	Filter enable 0: Disable filter 1: Enable filter
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a 65535 division (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the valid values of the sampling points are considered for logical level calculation. By configuring these bits, the sampling clock division for break 1 input sliding filter and break 2 input sliding filter can be determined.

18.5.30 DMA Control Register（TIMx_DCTRL）

Offset address: 0x94

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBADDR[5:0]						Reserved		DBLEN[5:0]					
		rw								rw					

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	DBADDR[5:0]	DMA base address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of “DMA Base Address + 4” 00000：TIMx_CTRL1, 00001：TIMx_CTRL2, 00010：TIMx_SMCTRL, ... 10001：TIMx_BKDT, 10010：TIMx_DCTRL

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Bit Field	Name	Description
7:6	Reserved	Reserved, the reset value must be maintained
5:0	DBLEN[5:0]	DMA burst length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 000000: 1 time transfer 000001: 2 time transfer 000010: 3 time transfer … 010001: 18 time transfer ..... 100010: 35 time transfer Example: Consider the following transfer: DBLEN=7, DBADDR=TIMx_CTRL1 If DBLEN=7 and DBADDR=TIMx_CTRL1 represent the address of the data to be transferred, then the address of the transfer is given by the following formula: (Address of TIMx_CTRL1) + DBADDR + (DMA index), where DMA index = DBLEN. Adding 7 to (Address of TIMx_CTRL1) + DBADDR gives the address where the data will be written or read, and the data transfer will occur in 7 registers starting from the address (Address of TIMx_CTRL1) + DBADDR. If the data is set to half-word (16 bits), the data will be transferred to all 7 registers. If the data is set to byte, the data will still be transferred to all 7 registers: the first register contains the first MSB byte, the second register contains the first LSB byte, and so on. Therefore, for the timer, the user must specify the data width to be transferred by DMA.

18.5.31 DMA Address For Full Transfer Register（TIMx_DADDR）

Offset address: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BURST[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[31:0]															
rw															

Bit Field	Name	Description
31:0	BURST[31:0]	DMA Access Buffer When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length × 4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example:

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Bit Field	Name	Description
		If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

19 General-Purpose Timers GTIMAx(x=1-7)

19.1 General-Purpose Timers Introduction

The general-purpose timers (GTIMA1/GTIMA2/GTIMA3/GTIMA4/GTIMA5/GTIMA6/GTIMA7) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

19.2 Main Features Of GTIMAx(x=1-7)

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- GTIMAx up to 4 channels.
- Channel’s working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signal.

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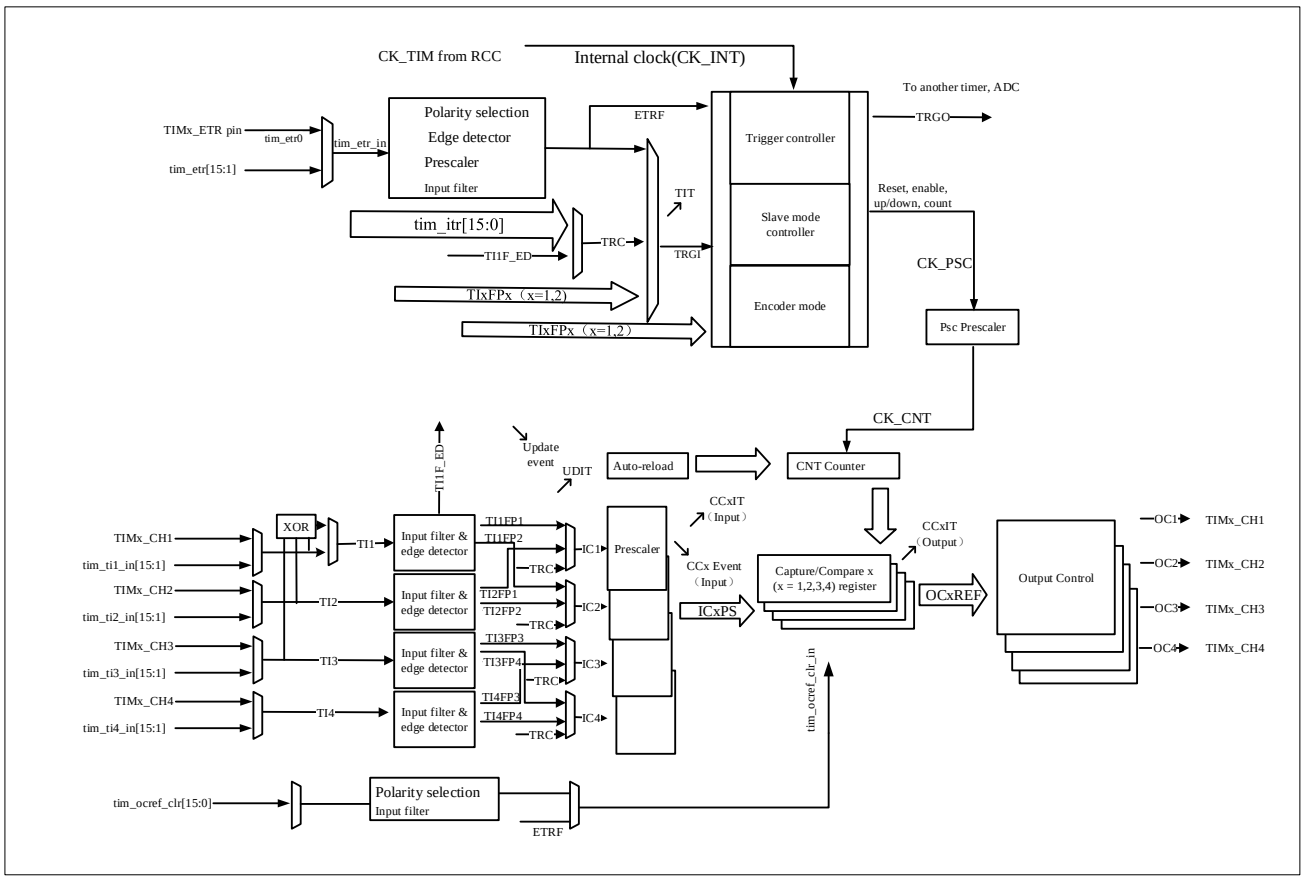
19.3 Block Diagram Of GTIMAx(x=1-7)

Figure 19-1 Block Diagram Of GTIMAx(x=1-7)



19.4 Pinout and Internal Signals of GTIMAx(x=1-7)

The following table describes the input and output pins and signals of GTIMAx

Table 19-1 GTIMAx Input/Output Pins

Pin	Type	Description
TIMx_CH1 TIMx_CH2 TIMx_CH3 TIMx_CH4	Input/Output	Timer multi-purpose channel. Each channel can be used for capture, compare or generating PWM. TIM_CH1 and TIM_CH2 can also be used as an external clock (less than 1/4 of the internal clock frequency), external trigger, and quadrature encoder input. TIM_CH1, TIM_CH2, TIM_CH3 can also be used for interfacing with Hall effect sensors.
TIMx_ETR	Input	External trigger input. This input can be used as an external trigger or

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		external clock source. If uses prescaler, the input signal TIMx_ETR can be a signal with a frequency higher than the system clock frequency.

Table 19-2 GTIMAx Internal Input/Output Signals

Internal signal	Type	Description
tim_ti1_in[15:0] tim_ti2_in[15:0] tim_ti3_in[15:0] tim_ti4_in[15:0]	Input	Timer channels 1/2/3/4 input signals. The tim_ti1_in[15:0] and tim_ti2_in[15:0] inputs can be used for capture or as an external clock (less than 1/4 of the system clock frequency) and for quadrature encoder signals.
tim_etr[15:0]	Input	External trigger channel input signals. These inputs can be used as triggers, external clocks, or for hardware pulse-width modulation control. If uses prescaler , the input signal TIMx_ETR can be a signal with a frequency higher than the system clock frequency.
tim_itr[15:0]	Input	Internal trigger input signals. These inputs can be used in mode controllers or as input clocks (less than 1/4 of the system clock frequency).
tim_trgo	Output	Internal trigger output signals. These trigger signals can be used by other timers and/or other peripheral devices.

19.4.1 Interconnect of the tim_ti1/ tim_ti2/ tim_ti3/ tim_ti4 Input

Table 19-3 tim_ti1 Input Signal Sources

tim_ti1 inputs	**Signal Sources**						
	GTIMA1	**GTIMA2**	**GTIMA3**	**GTIMA4**	**GTIMA5**	**GTIMA6**	**GTIMA7**
tim_ti1_in0	GTIMA1_CH1	GTIMA2_CH1	GTIMA3_CH1	GTIMA4_CH1	GTIMA5_CH1	GTIMA6_CH1	GTIMA7_CH1
tim_ti1_in1	LSE_CSS_OUT	LSE	Reserved	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti1_in2	COMP1_OUT	MCO1	MCO2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti1_in3	COMP2_	HSE_	HSE_	COMP3_	COMP3_	COMP3_	COMP3_

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	OUT	DIV32	DIV32	OUT	OUT	OUT	OUT
tim_ti1_in4	COMP3_ OUT	RTC_ WAKEUP	RTC_ WAKEUP	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT
tim_ti1_in5	COMP4_ OUT	LSE_CSS _OUT	LSE_CSS _OUT	CAN1_ TMP	CAN2_ TMP	CAN3_ TMP	CAN4_ TMP
tim_ti1_in6	Reserved	LSI	LSI	CAN1_ RTP	CAN2_ RTP	CAN3_ RTP	CAN4_ RTP
tim_ti1_in[15:7]	Reserved						

Table 19-4 tim_ti2 Input Signal Sources

tim_ti2 inputs	**Signal Sources**						
	GTIMA1	**GTIMA2**	**GTIMA3**	**GTIMA4**	**GTIMA5**	**GTIMA6**	**GTIMA7**
tim_ti2_in0	GTIMA1_ CH2	GTIMA2_ CH2	GTIMA3_ CH2	GTIMA4_ CH2	GTIMA5_ CH2	GTIMA6_ CH2	GTIMA7_ CH2
tim_ti2_in1	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT
tim_ti2_in2	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT
tim_ti2_in3	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT
tim_ti2_in4	GTIMA6_ OC1	GTIMA6_ OC2	GTIMA6_ OC3	GTIMA6_ OC4	COMP4_ OUT	COMP4_ OUT	COMP4_ OUT
tim_ti2_in[15:5]	Reserved						

Table 19-5 tim_ti3 Input Signal Sources

tim_ti3 inputs	**Signal Sources**

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	GTIMA1	GTIMA2	GTIMA3	GTIMA4	GTIMA5	GTIMA6	GTIMA7
tim_ti3_in0	GTIMA1_CH3	GTIMA2_CH3	GTIMA3_CH3	GTIMA4_CH3	GTIMA5_CH3	GTIMA6_CH3	GTIMA7_CH3
tim_ti3_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti3_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti3_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti3_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti3_in[15:5]	Reserved						

Table 19-6 tim_ti4 Input Signal Sources

tim_ti4 inputs	Signal Sources						
	GTIMA1	GTIMA2	GTIMA3	GTIMA4	GTIMA5	GTIMA6	GTIMA7
tim_ti4_in0	GTIMA1_CH4	GTIMA2_CH4	GTIMA3_CH4	GTIMA4_CH4	GTIMA5_CH4	GTIMA6_CH4	GTIMA7_CH4
tim_ti3_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti3_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti3_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti3_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT

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tim_ti4_in[15:5]	Reserved

19.4.2 Interconnect of the tim_itr Input

Table 19-7 tim_itr Input Signal Sources

GTIMAx	**GTIMA1**	**GTIMA2**	**GTIMA3**	**GTIMA4**	**GTIMA5**	**GTIMA6**	**GTIMA7**
tim_itr0	ATIM1_ TRGO	ATIM1_ TRGO	ATIM1_ TRGO	ATIM1_ TRGO	ATIM1_ TRGO	ATIM1_ TRGO	ATIM1_ TRGO
tim_itr1	Reserve	GTIMA1_ TRGO	GTIMA1_ TRGO	GTIMA1_ TRGO	GTIMA1_ TRGO	GTIMA1_ TRGO	GTIMA1_ TRGO
tim_itr2	GTIMA2_ TRGO	Reserve	GTIMA2_ TRGO	GTIMA2_ TRGO	GTIMA2_ TRGO	GTIMA2_ TRGO	GTIMA2_ TRGO
tim_itr3	GTIMA3_ TRGO	GTIMA3_ TRGO	Reserve	GTIMA3_ TRGO	GTIMA3_ TRGO	GTIMA3_ TRGO	GTIMA3_ TRGO
tim_itr4	GTIMA4_ TRGO	GTIMA4_ TRGO	GTIMA4_ TRGO	CAN1_ SOC	GTIMA4_ TRGO	GTIMA4_ TRGO	GTIMA4_ TRGO
tim_itr5	ATIM2_ TRGO	ATIM2_ TRGO	ATIM2_ TRGO	ATIM2_ TRGO	ATIM2_ TRGO	ATIM2_ TRGO	ATIM2_ TRGO
tim_itr6	GTIMA5_ TRGO	GTIMA5_ TRGO	GTIMA5_ TRGO	GTIMA5_ TRGO	CAN2_ SOC	GTIMA5_ TRGO	GTIMA5_ TRGO
tim_itr7	ATIM3_ TRGO	ATIM3_ TRGO	ATIM3_ TRGO	ATIM3_ TRGO	ATIM3_ TRGO	ATIM3_ TRGO	ATIM3_ TRGO
tim_itr8	GTIMA6_ TRGO	GTIMA6_ TRGO	GTIMA6_ TRGO	GTIMA6_ TRGO	GTIMA6_ TRGO	CAN3_ SOC	GTIMA6_ TRGO
tim_itr9	GTIMA7_ TRGO	GTIMA7_ TRGO	GTIMA7_ TRGO	GTIMA7_ TRGO	GTIMA7_ TRGO	GTIMA7_ TRGO	CAN4_ SOC
tim_itr10	ATIM4_	ATIM4_	ATIM4_	ATIM4_	ATIM4_	ATIM4_	ATIM4_

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	TRGO	TRGO	TRGO	TRGO	TRGO	TRGO	TRGO
tim_itr11	GTIMB1_ TRGO	GTIMB1_ TRGO	GTIMB1_ TRGO	GTIMB1_ TRGO	GTIMB1_ TRGO	GTIMB1_ TRGO	GTIMB1_ TRGO
tim_itr12	GTIMB2_ TRGO	GTIMB2_ TRGO	GTIMB2_ TRGO	GTIMB2_ TRGO	GTIMB2_ TRGO	GTIMB2_ TRGO	GTIMB2_ TRGO
tim_itr13	GTIMB3_ TRGO	GTIMB3_ TRGO	GTIMB3_ TRGO	GTIMB3_ TRGO	GTIMB3_ TRGO	GTIMB3_ TRGO	GTIMB3_ TRGO
tim_itr14	SHRTIM1_ OUT_ SYNC2	SHRTIM1_ OUT_ SYNC2	SHRTIM1_ OUT_ SYNC2	USB1_HS _SOF	USB1_HS _SOF	SHRTIM1_ OUT_ SYNC2	SHRTIM1_ OUT_ SYNC2
tim_itr15	ETH2_PPS _OUT	ETH2_PPS _OUT	Reserve	USB2_HS _SOF	USB2_HS _SOF	SHRTIM2_ OUT_ SYNC2	SHRTIM2_ OUT_ SYNC2

19.4.3 Interconnect of the tim_etr Input

Table 19-8 tim_etr Input Signal Sources

GTIMAx	**GTIMA1**	**GTIMA2**	**GTIMA3**	**GTIMA4**	**GTIMA5**	**GTIMA6**	**GTIMA7**
tim_etr0	GTIMA1_ ETR	GTIMA2_ ETR	GTIMA3_ ETR	GTIMA4_ ETR	GTIMA5_ ETR	GTIMA6_ ETR	GTIMA7_ ETR
tim_etr1	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT	COMP1_ OUT
tim_etr2	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT	COMP2_ OUT
tim_etr3	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT	COMP3_ OUT
tim_etr4	COMP4_	COMP4_	COMP4_	COMP4_	COMP4_	COMP4_	COMP4_

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	OUT	OUT	OUT	OUT	OUT	OUT	OUT
tim_etr5	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1
tim_etr6	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2
tim_etr7	GTIMA2_ ETR	GTIMA1_ ETR	GTIMA2_ ETR	GTIMA1_ ETR	GTIMA6_ ETR	GTIMA5_ ETR	GTIMA5_ ETR
tim_etr8	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1
tim_etr9	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2
tim_etr10	GTIMB1_ ETR	GTIMA3_ ETR	GTIMA4_ ETR	GTIMA2_ ETR	GTIMA7_ ETR	GTIMA7_ ETR	GTIMA6_ ETR
tim_etr11	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1
tim_etr12	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2
tim_etr13	LSE	GTIMB2_ ETR	GTIMB3_ ETR	GTIMB1_ ETR	GTIMB2_ ETR	GTIMB3_ ETR	GTIMB1_ ETR
tim_etr_in[15:14]	Reserved						

19.4.4 Interconnect of the tim_ocref_clr Input

Table 19-9 tim_ocref_clr Input Signal Sources

OCREF clear signal	GTIMAx **OCREF clear signal assignment**						
	GTIMA1	**GTIMA2**	**GTIMA3**	**GTIMA4**	**GTIMA5**	**GTIMA6**	**GTIMA7**

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tim_ocref_clr0	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ocref_clr1	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ocref_clr2	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ocref_clr3	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ocref_in[15:4]	Reserved						

19.5 GTIMAx(x=1-7)Function Description

19.5.1 Time-Base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

19.5.1.1 Prescaler Description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

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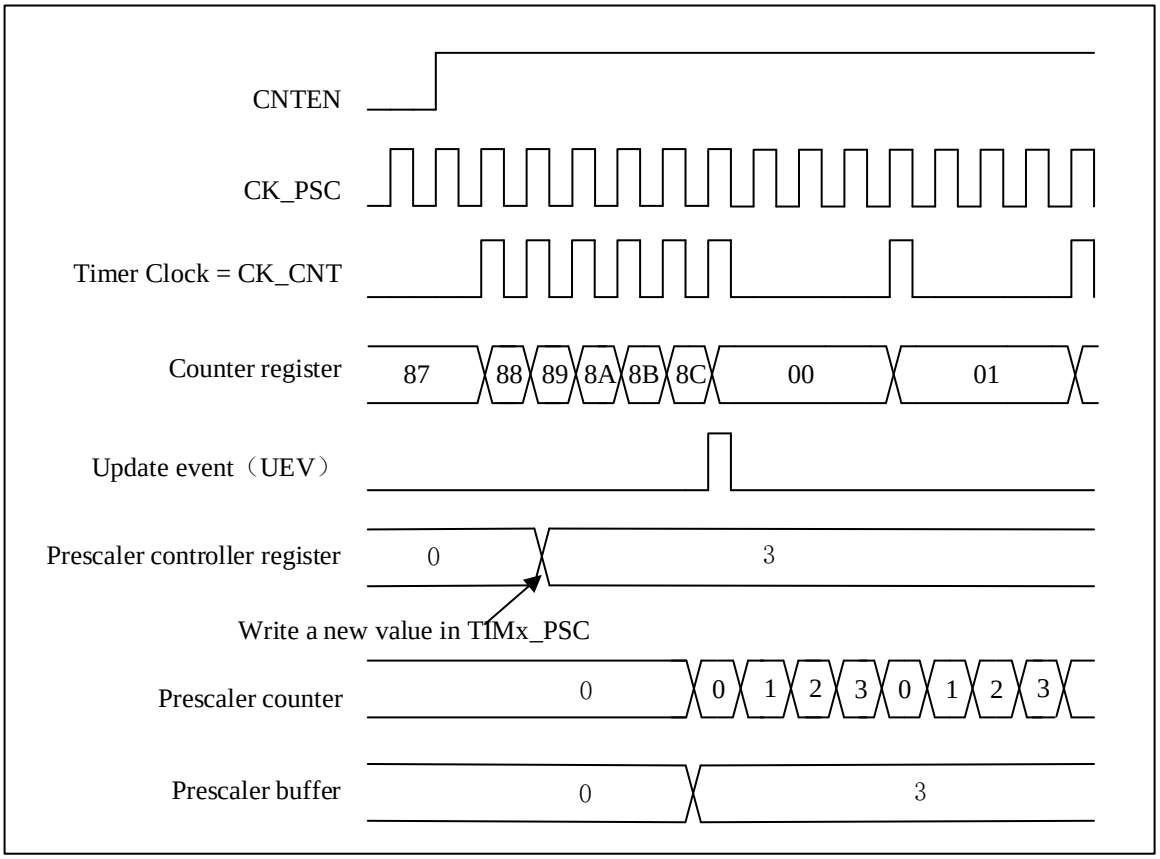
Figure 19-2 Counter Timing Diagram With Prescaler Division Change From 1 To 4



19.5.2 Counter Mode

19.5.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the

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prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 19-3 Timing Diagram Of Up-Counting. The Internal Clock Divider Factor = 2/N

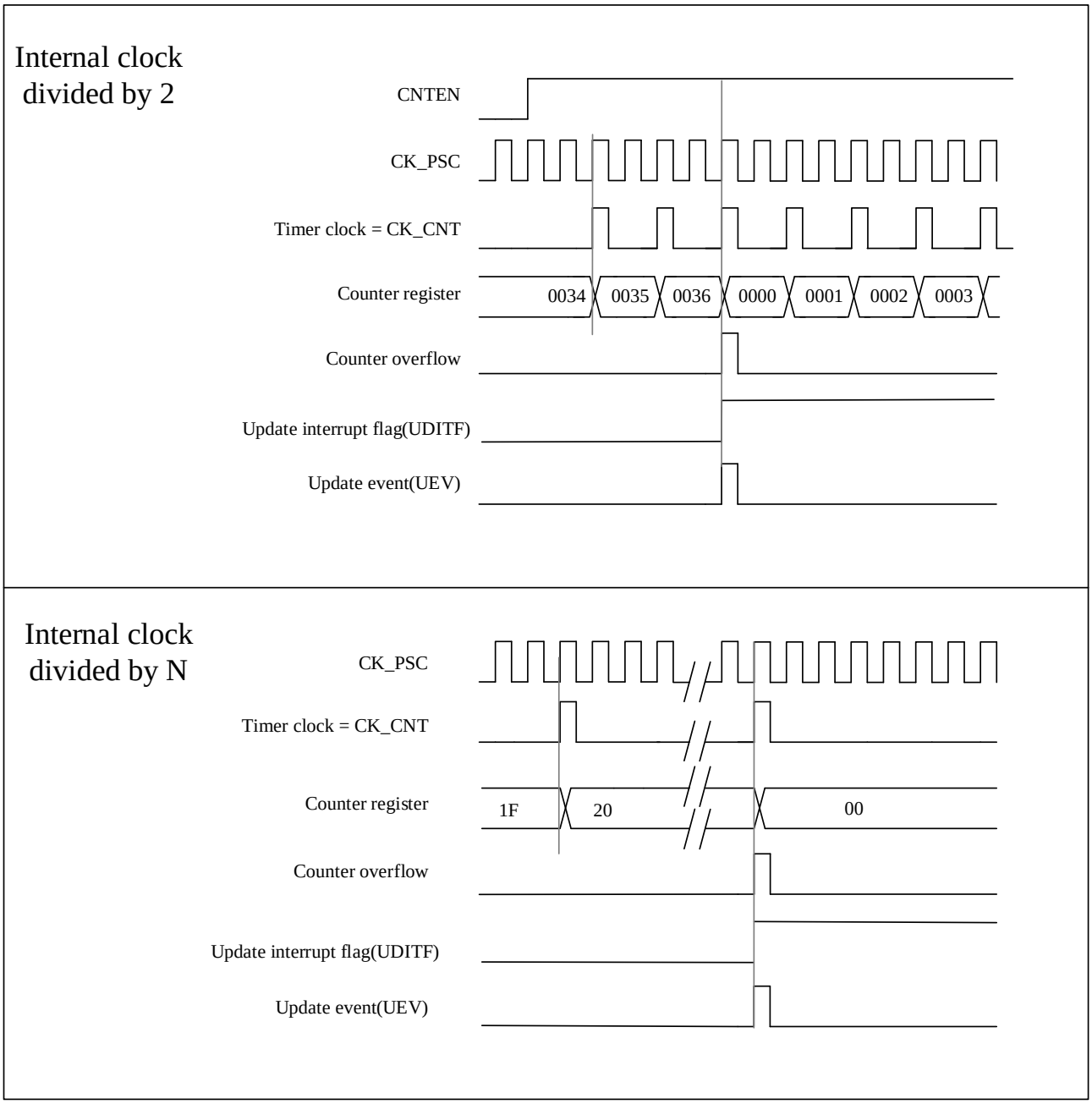

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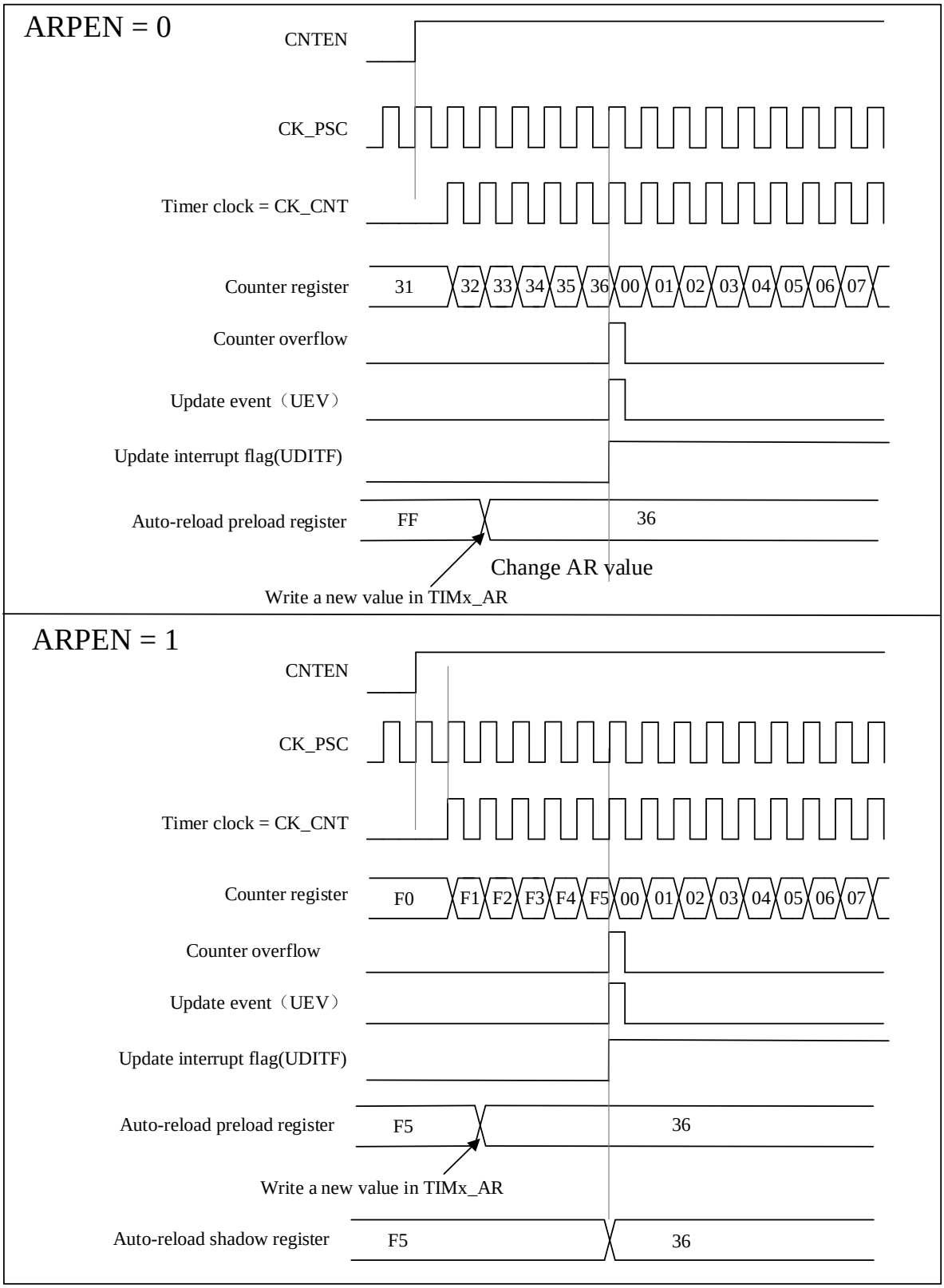
Figure 19-4 Timing Diagram Of The Up-Counting, Update Event When ARPEN=0/1



19.5.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from

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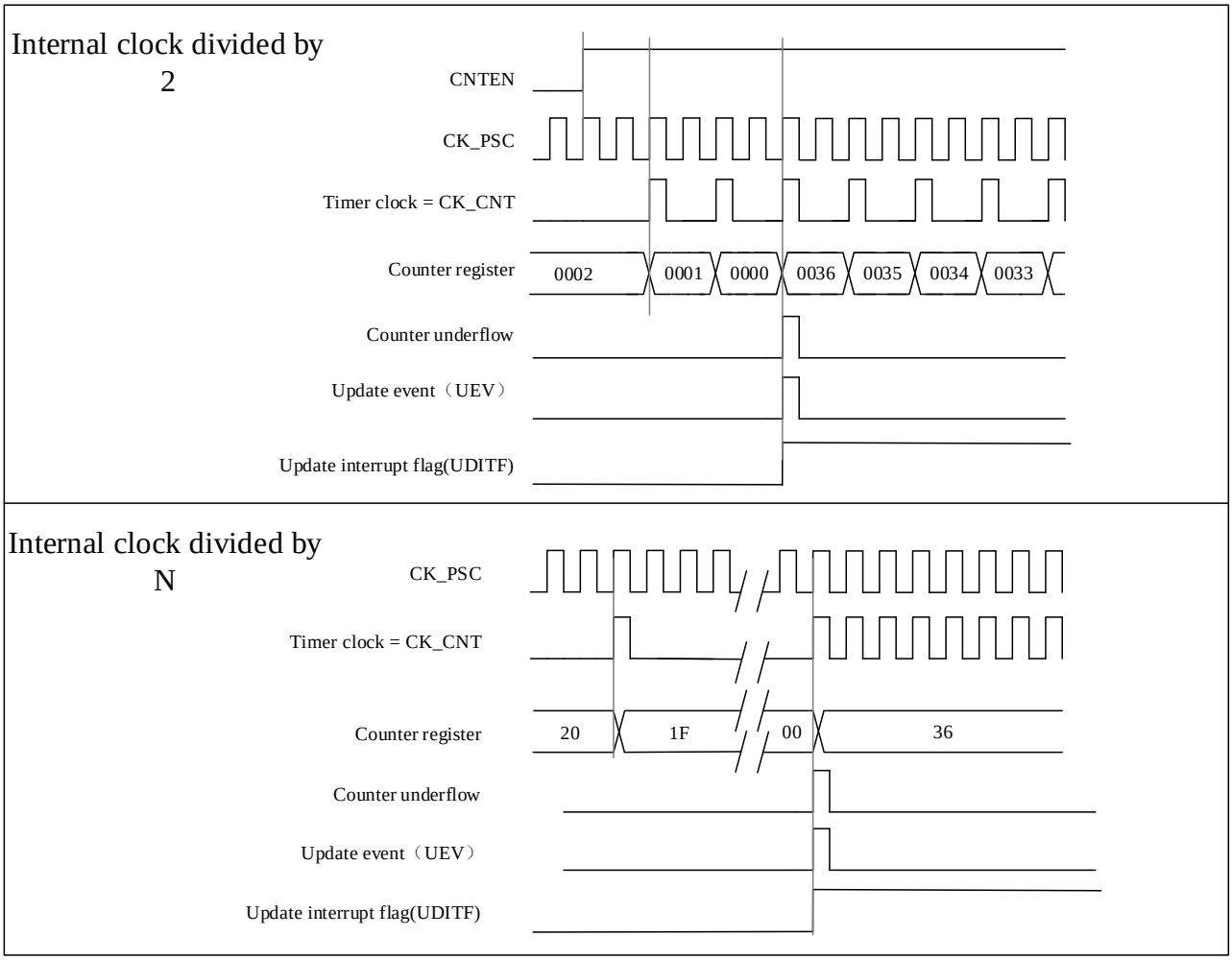
the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see Section19.5.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 19-5 Timing Diagram Of The Down-Counting, Internal Clock Divided Factor = 2/N



19.5.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Note: if the update source is a counter overflow, auto-reload update before reloading the counter.

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Figure 19-6 Timing Diagram Of The Center-Aligned, Internal Clock Divided Factor =2/N

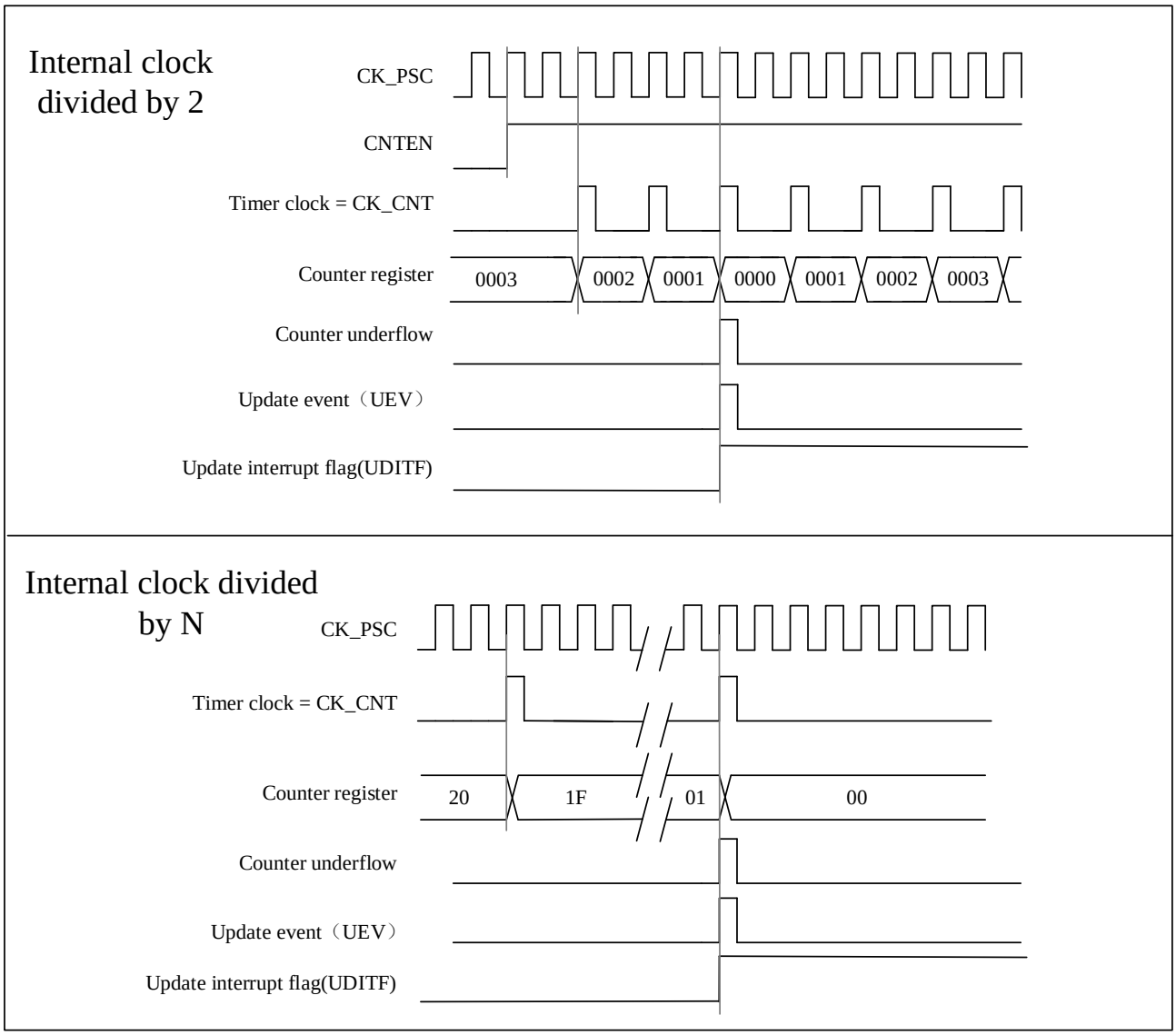

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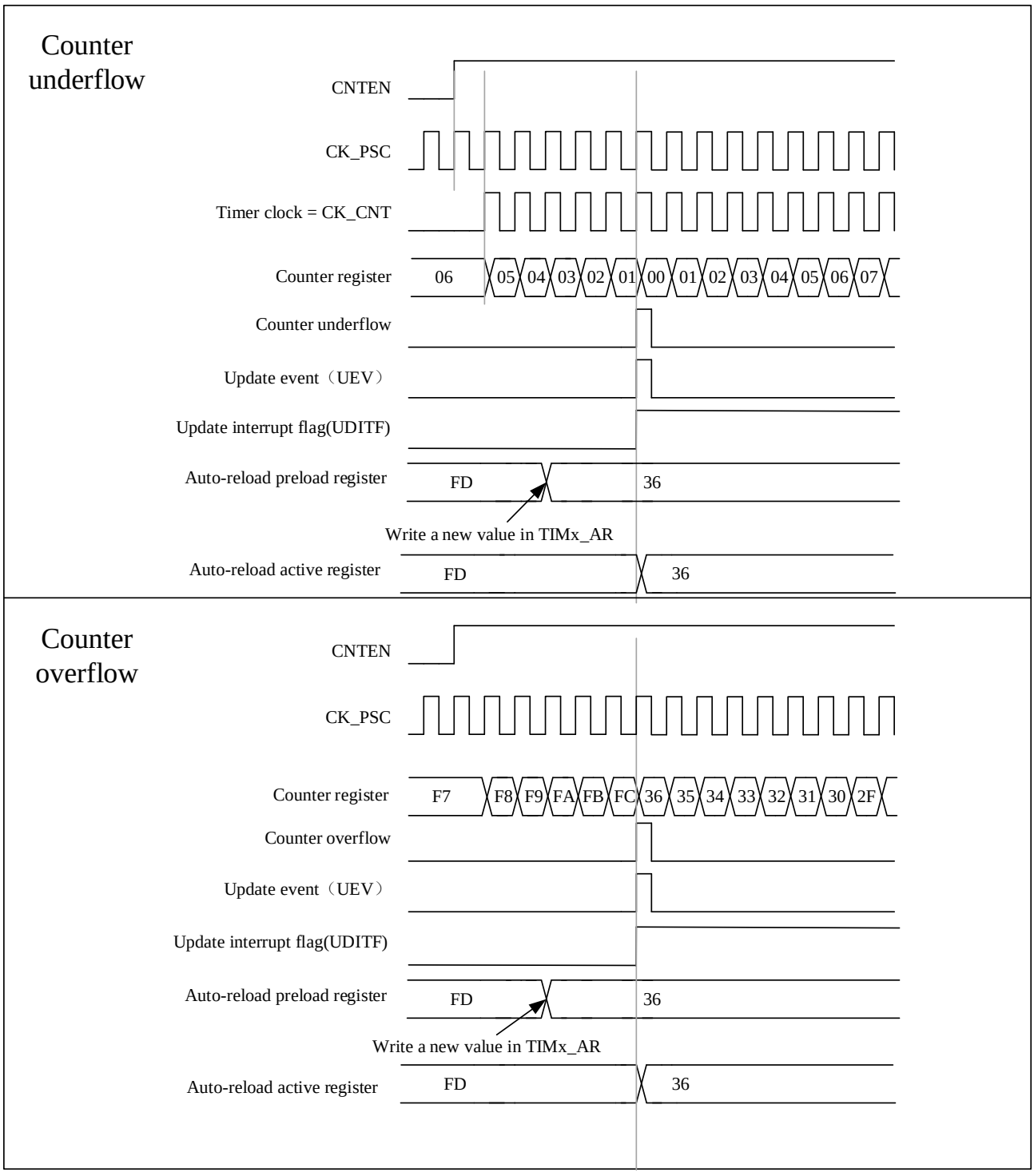
Figure 19-7 A Center-Aligned Sequence Diagram That Includes Counter Overflows And Underflows (ARPEN = 1)



19.5.3 Clock Selection

- The internal clock of timers：CK_INT
- Two kinds of external clock mode:

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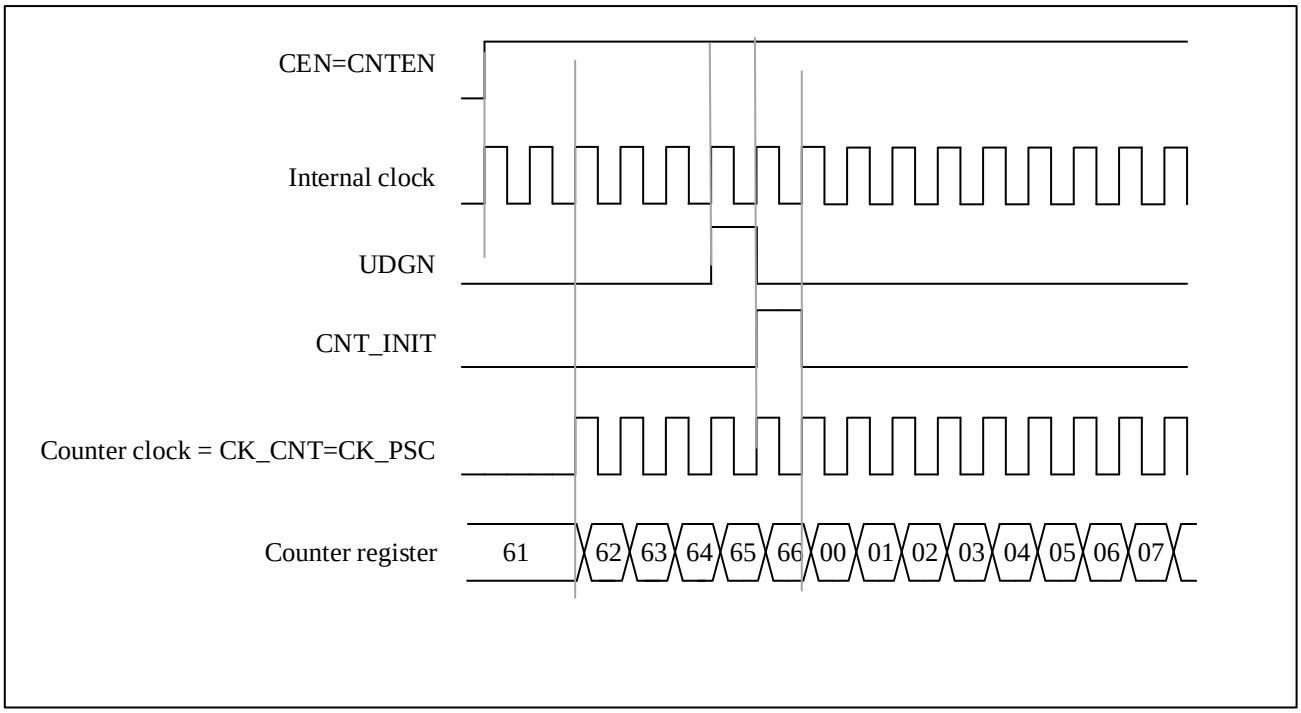
- external input pin
- external trigger input ETR

- Internal trigger input(ITRx): one timer is used as a prescaler for another timer

19.5.3.1 Internal clock source(CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “0000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 19-8 Control Circuit In Normal Mode, Internal Clock Divided By 1



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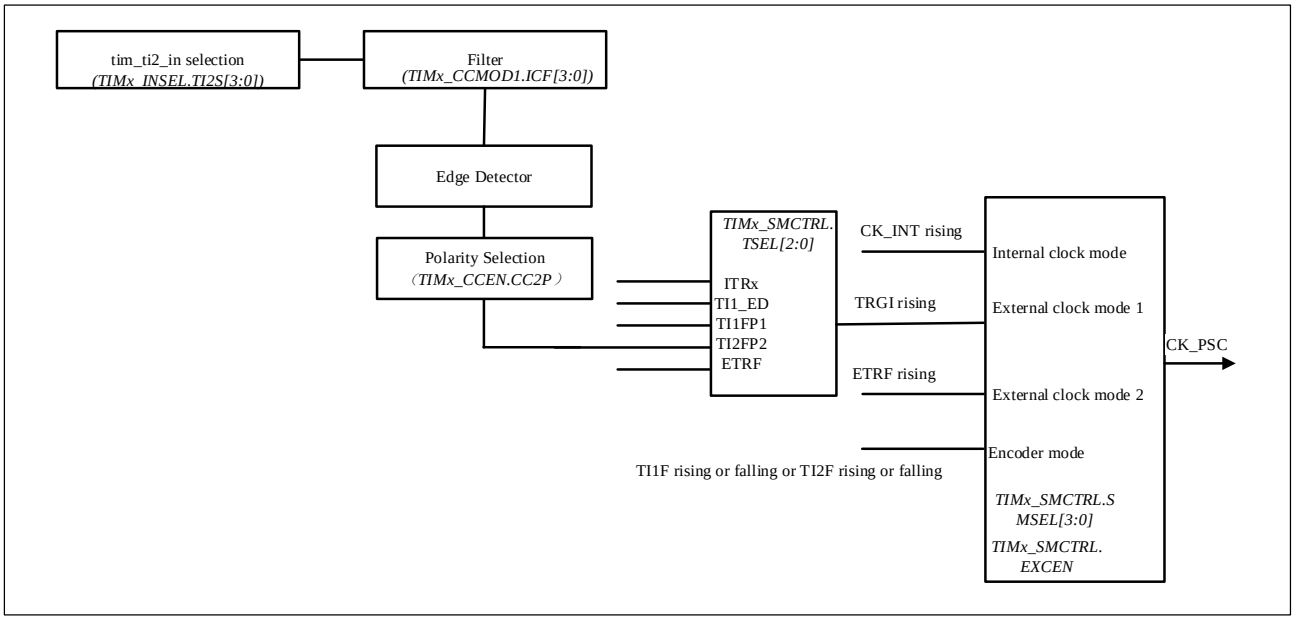
19.5.3.2 External clock source mode 1

Figure 19-9 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=0111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to '01', CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to '0', select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000')
- Configure TIMx_SMCTRL.SMSEL equal to '0111', select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to '110', select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to '1' to start the counter

Note：The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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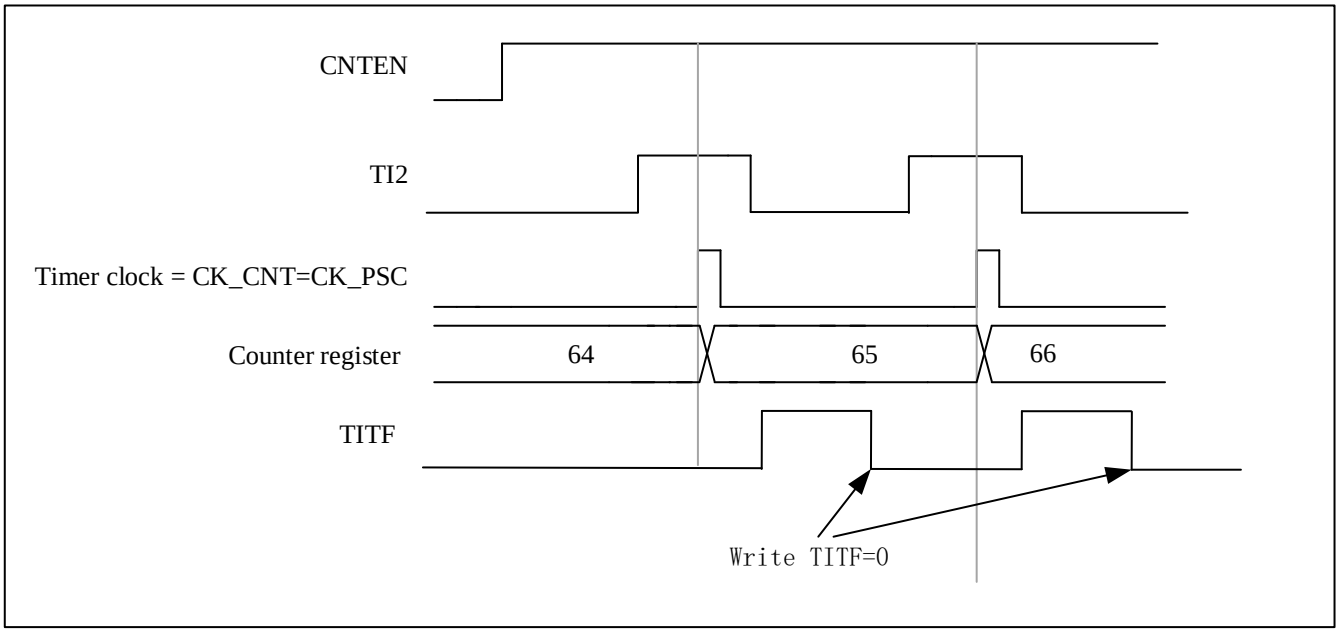
Figure 19-10 Control Circuit In External Clock Mode 1

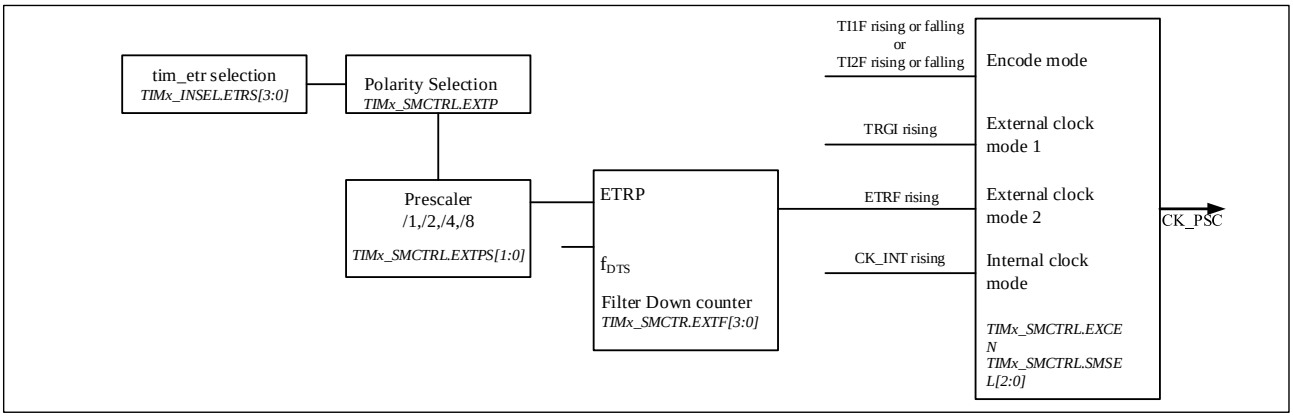


19.5.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 19-11 External Trigger Input Block Diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

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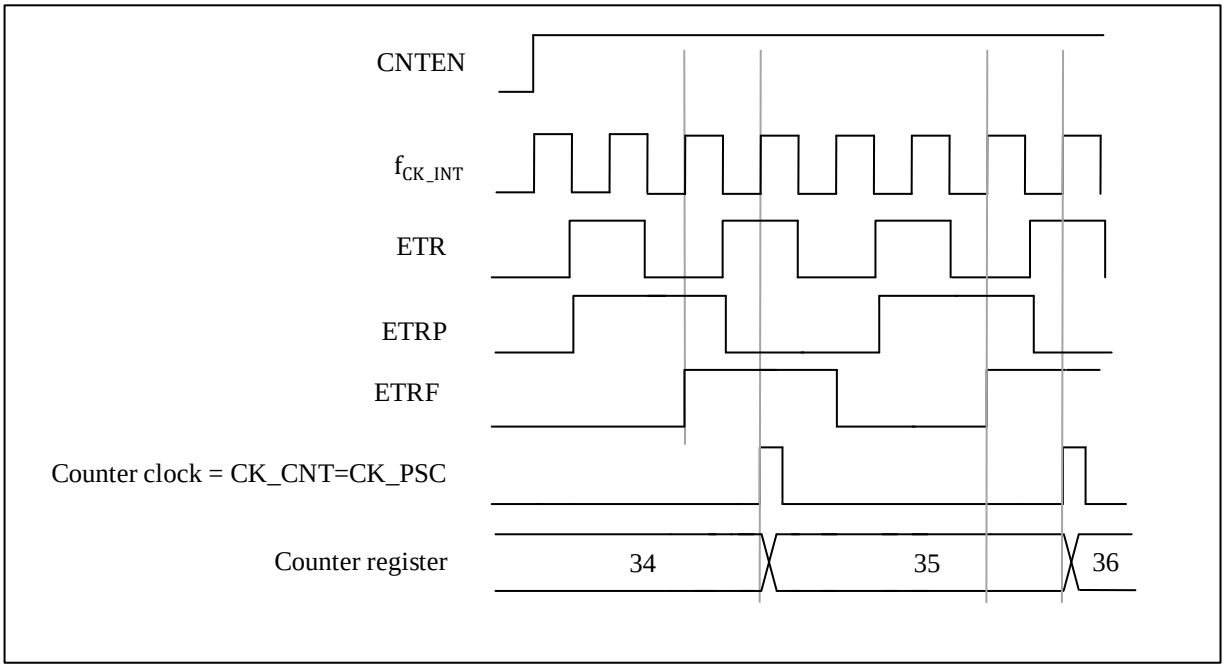
The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 19-12 Control Circuit In External Clock Mode 2



19.5.4 Capture/Compare Channels

Capture/Compare channels include Capture/Compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after prescale. The following figure shows a block diagram of a capture/compare channel.

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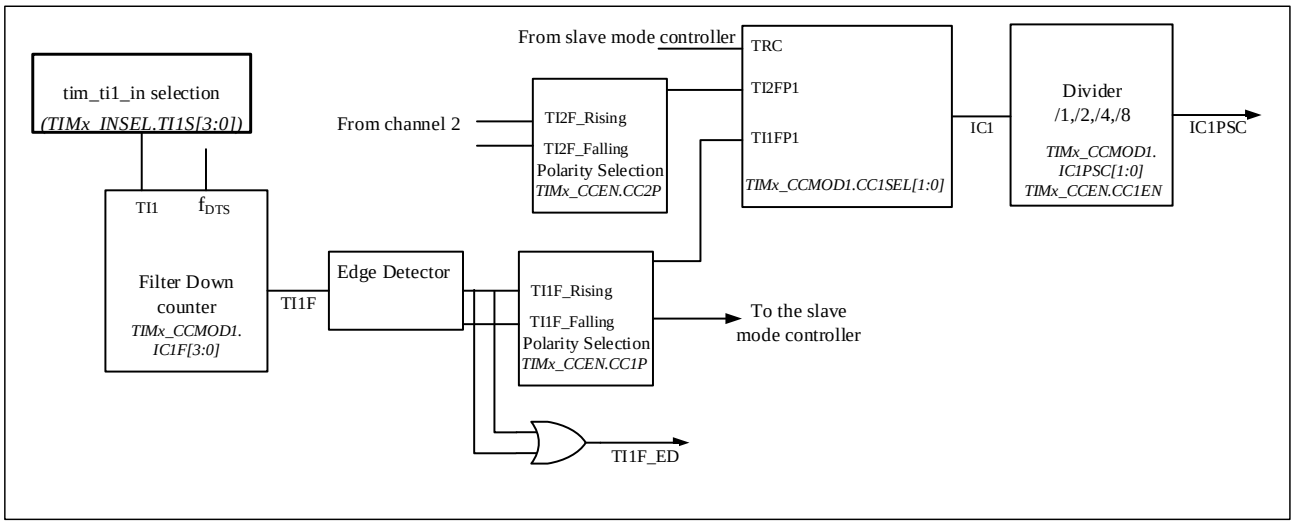
Figure 19-13 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 19-14 Capture/Compare Channel 1 Main Circuit

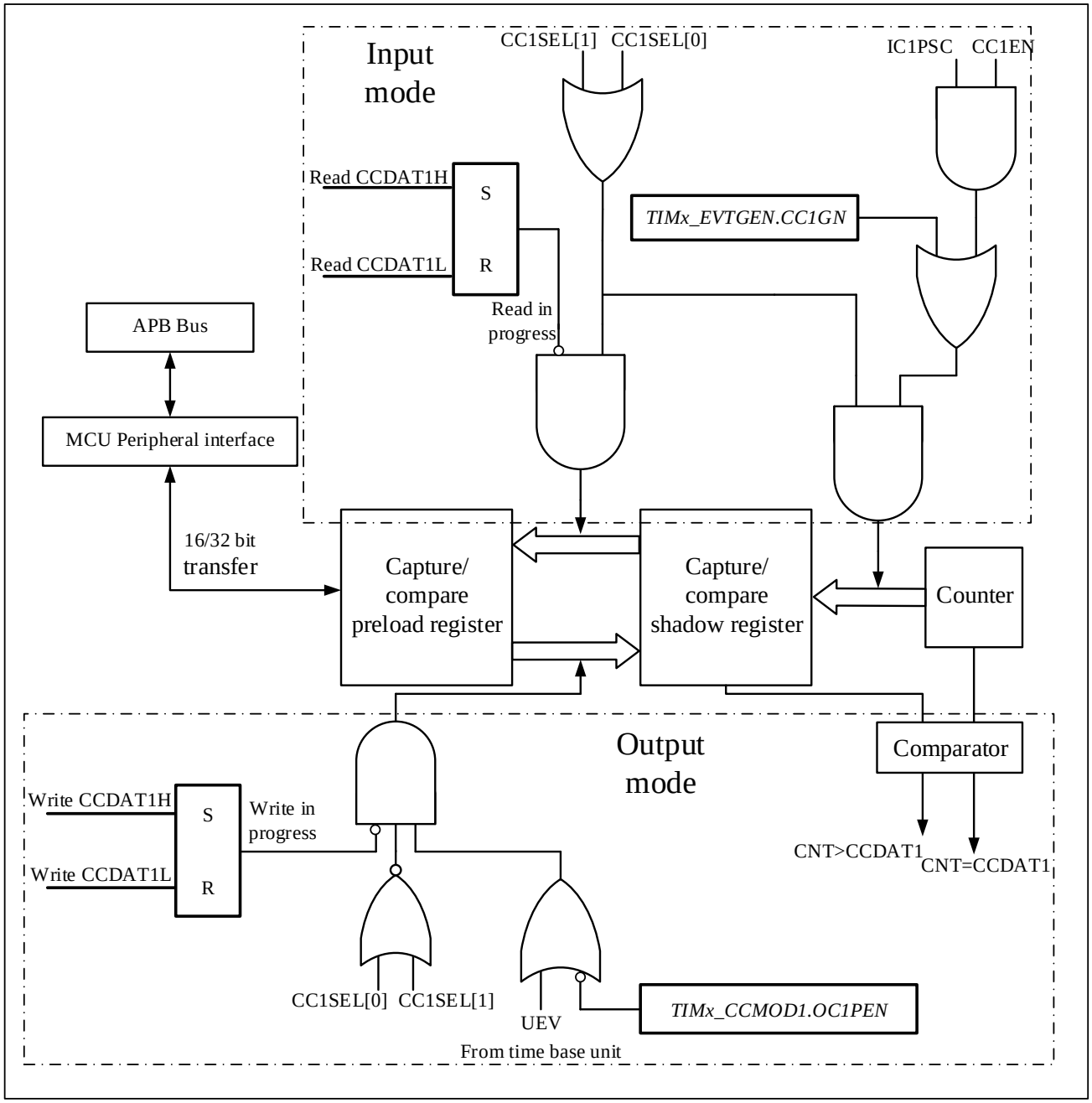

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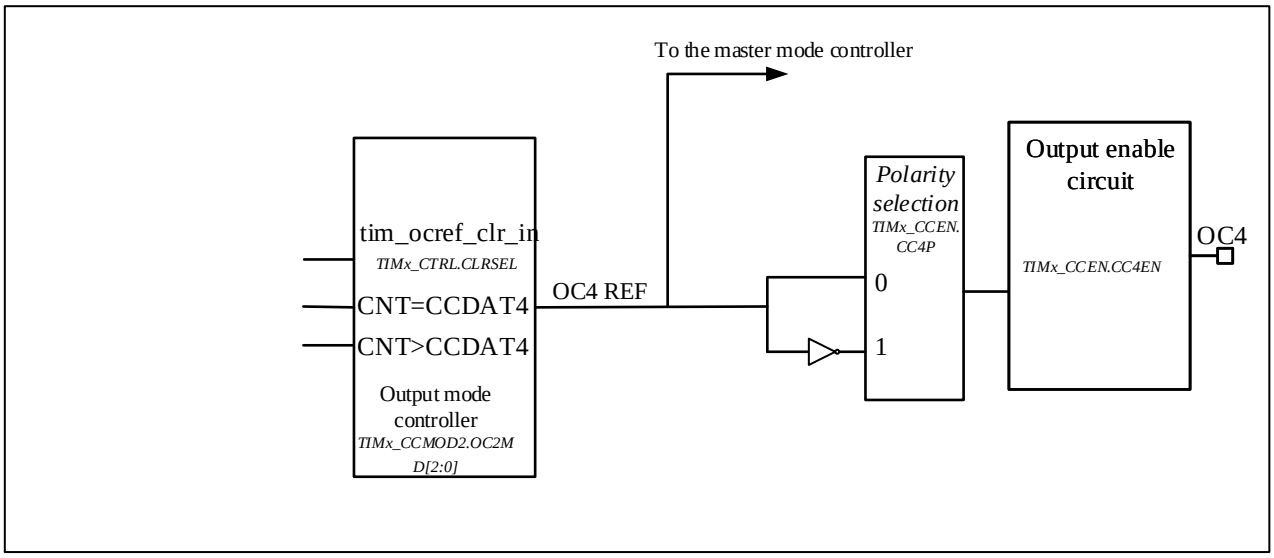
Figure 19-15 Output Part Of Channelx (x=1,2,3,4; Take Channel 4 As An Example)



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

19.5.5 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- The duration of the input filter required for programming：

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the

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TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1.IC1F to '0011'.

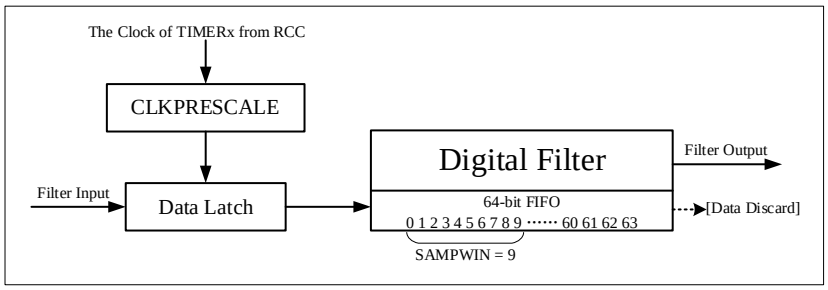
- By configuring TIMx_CCEN.CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC='00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN.CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

19.5.5.1 Channel Input Filtering

The register TIMx_CxFILT(x=1,2,3,4) is described as follows:

Figure 19-16 Sliding Filtering



- Digital filters sample the channel input signal using the RCC's TIMx clock and accumulate the samples in a 64-bit FIFO. Only data sampled within the window size defined in TIMx_CxFILT.WSIZE [5:0] is considered, with a maximum window size of 64.
- The filter outputs the majority value within the sampling window, which is defined by the threshold in TIMx_CxFILT.THRESH [5:0], with a maximum threshold of 63. This value should be equal to or greater than half the window size. If the counts of logic 1 and logic 0 within the sampling window are not greater than the threshold, the digital filter maintains the previous output value.
- TIMx_SLIDFPSC.PSC register determines the sampling rate of the corresponding digital filter. The filter FIFO captures a sample value from the input at each sampling clock.
- If the digital filter is disabled, the filter input is directly output.

19.5.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.

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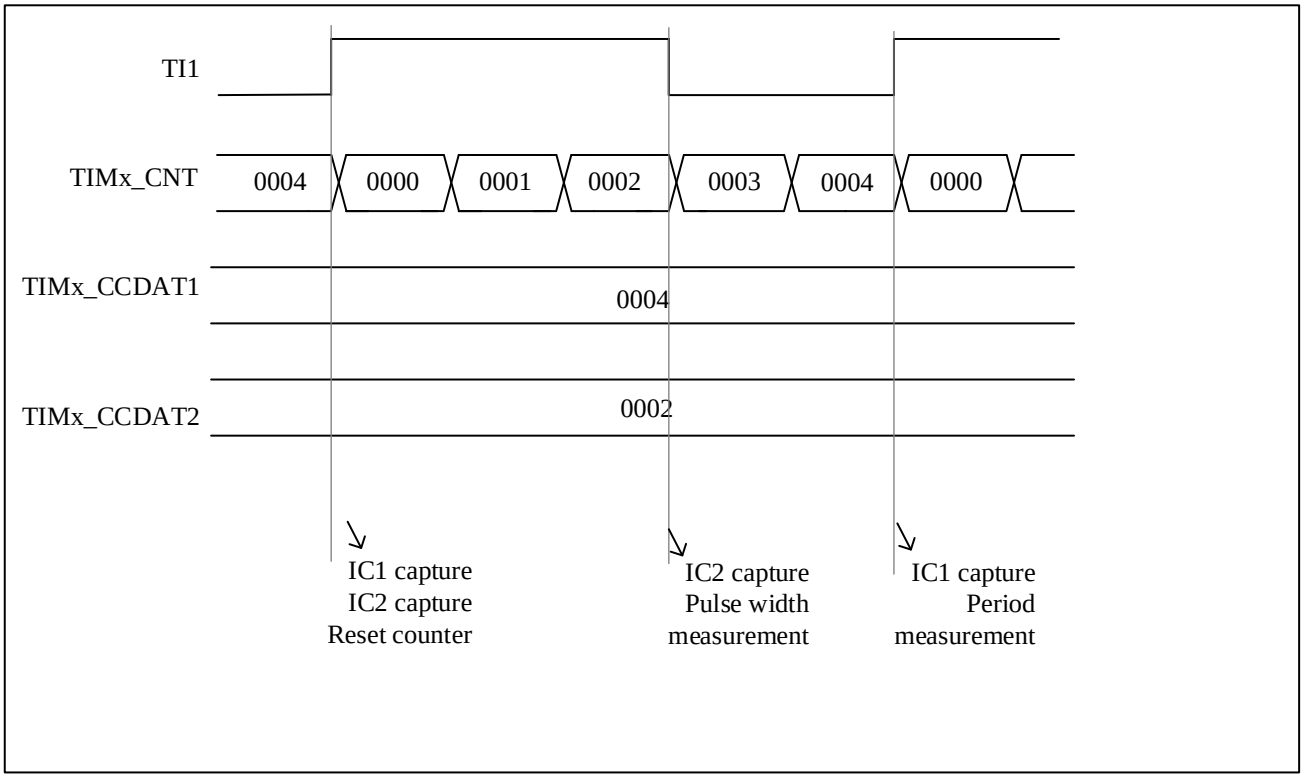
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active at the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active at the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

Figure 19-17 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

19.5.7 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

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User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level, the OCxREF will be forced low.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

19.5.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed。

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow：

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.
- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers(TIMx_CCDATx) or not

The time resolution is one counting period of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with required data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event

Here is an example.

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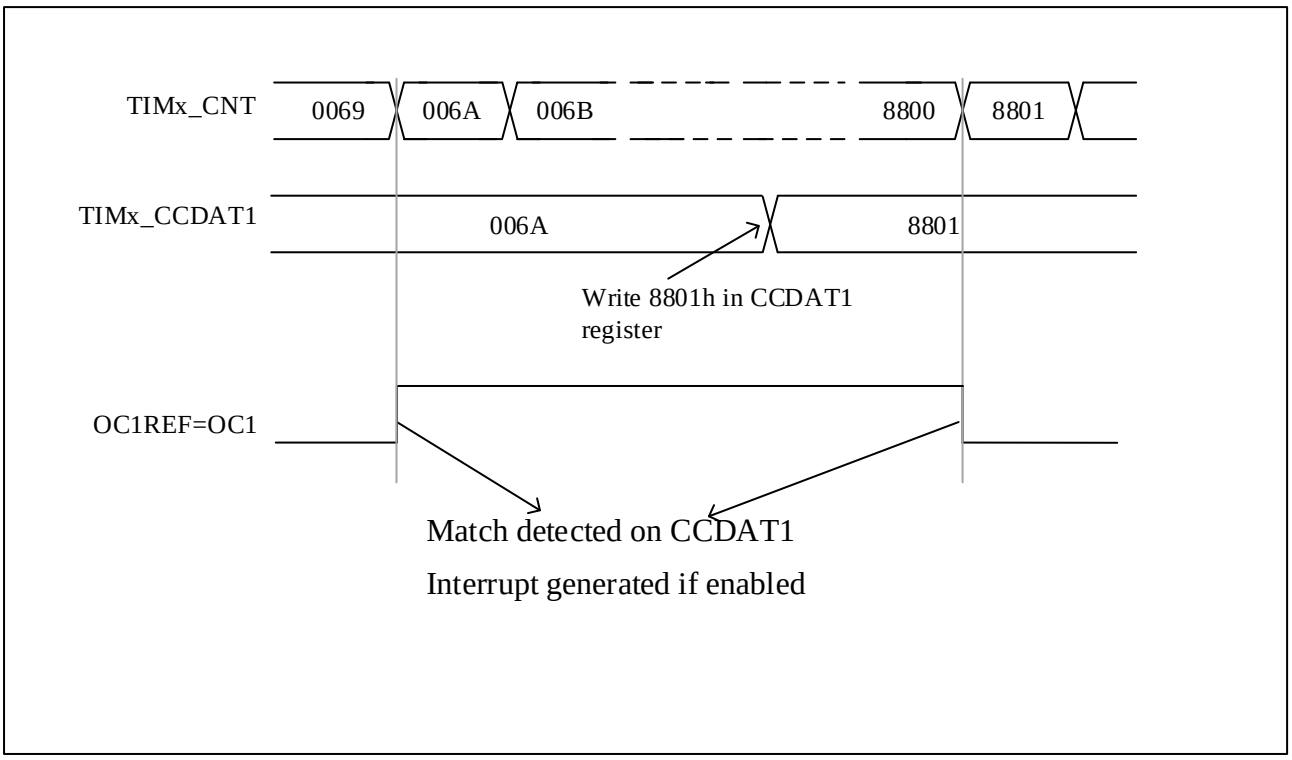
Figure 19-18 Output Compare Mode, Toggle On OC1



19.5.9 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

19.5.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM

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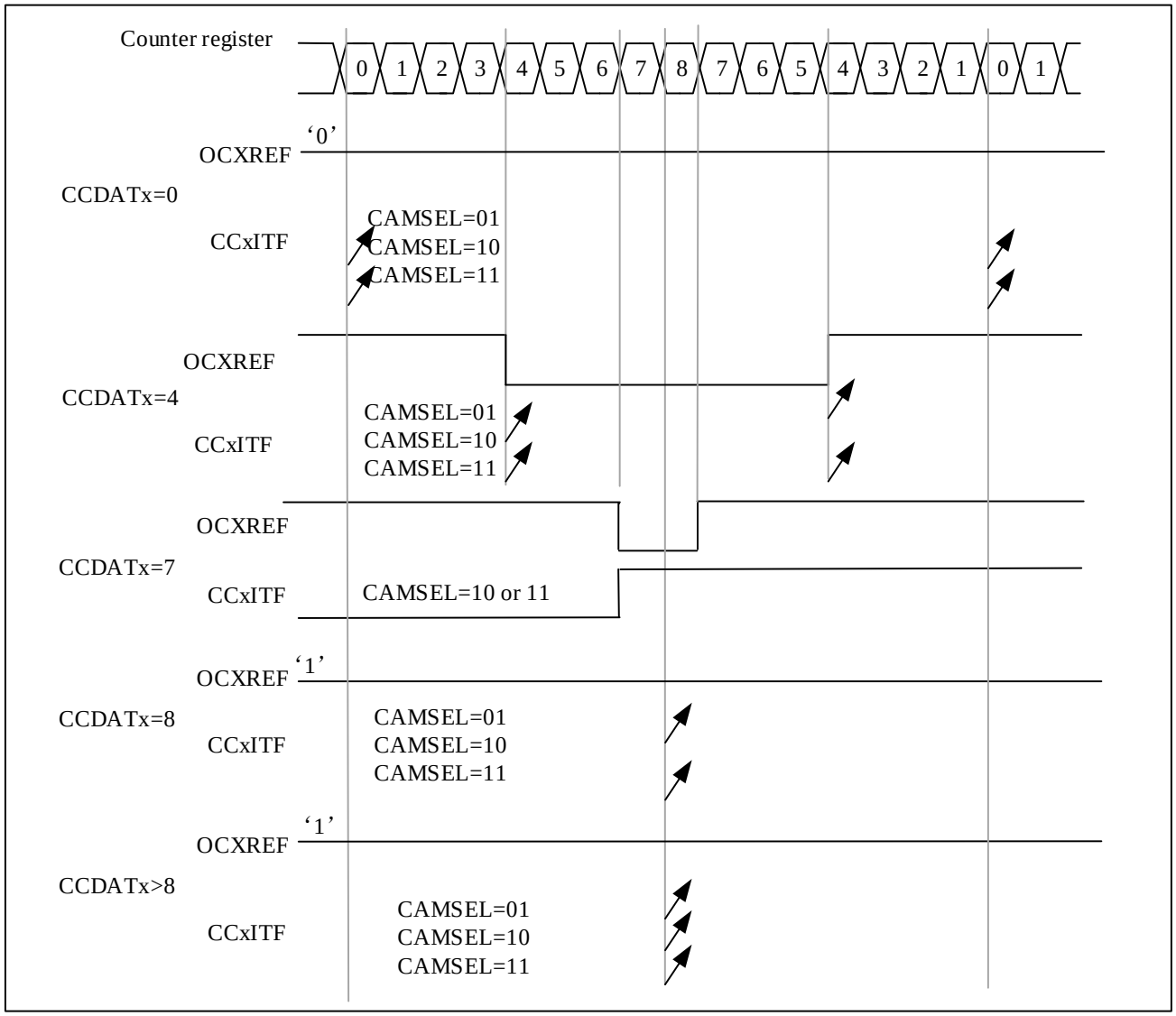
mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1.CAMSEL=01.

Figure 19-19 Center-Aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considerations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some examples:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and not writing the counter while it is running.

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19.5.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

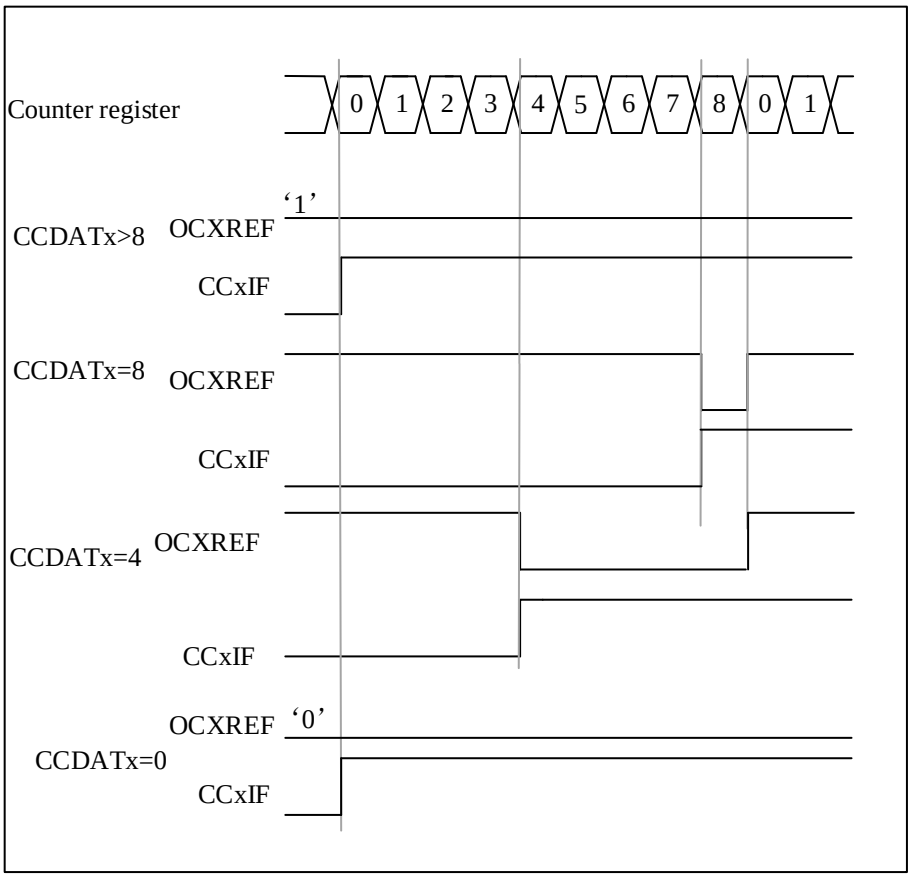
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Example for PWM mode1：

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow:

Figure 19-20 Edge-Aligned PWM waveform (AR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.
Example for PWM mode1：

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the

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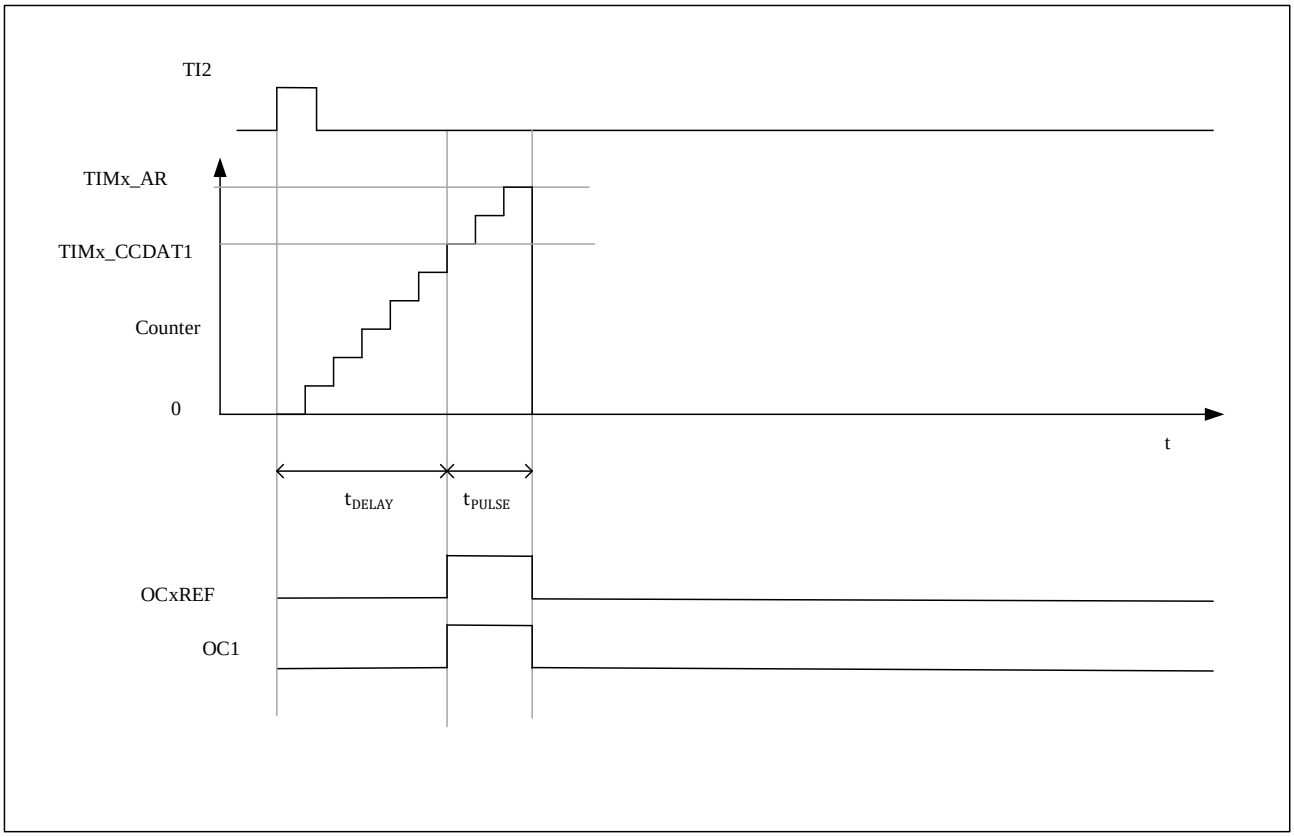
(n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

19.5.10 One-Pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated

Figure 19-21 Example Of One-pulse Mode



The following is an example of a one-pulse mode：

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL='01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P='0';
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL='110' (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};

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5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD='111' to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

19.5.10.1 Special case: Ocx fast enable:

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

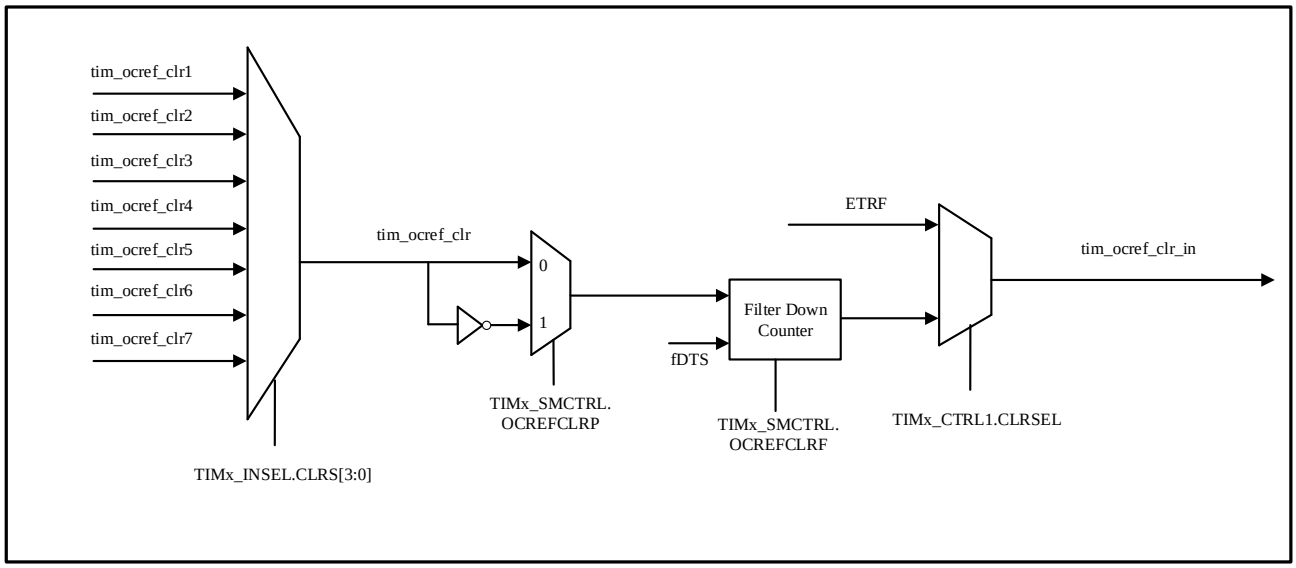
19.5.11 Clearing The OCxref Signal On An External Event

If user set TIMx_CCMODx.OCxCEN=1, high level of tim_ocref_clr_in input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

The input clear signal tim_ocref_clr_in can be selected as tim_ocref_clr or ETRF through the CLRSEL bit in the TIMx_CTRL1 register.

The tim_ocref_clr signal can be selected through the CLRS[3:0] in the TIMx_INSEL register, as shown in the following figure.

Figure 19-22 Clearing OCxREF Signal By External Event



For example, when the tim_ocref_clr_in signal selects ETRF, the tim_etr_in configuration is as follows:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external

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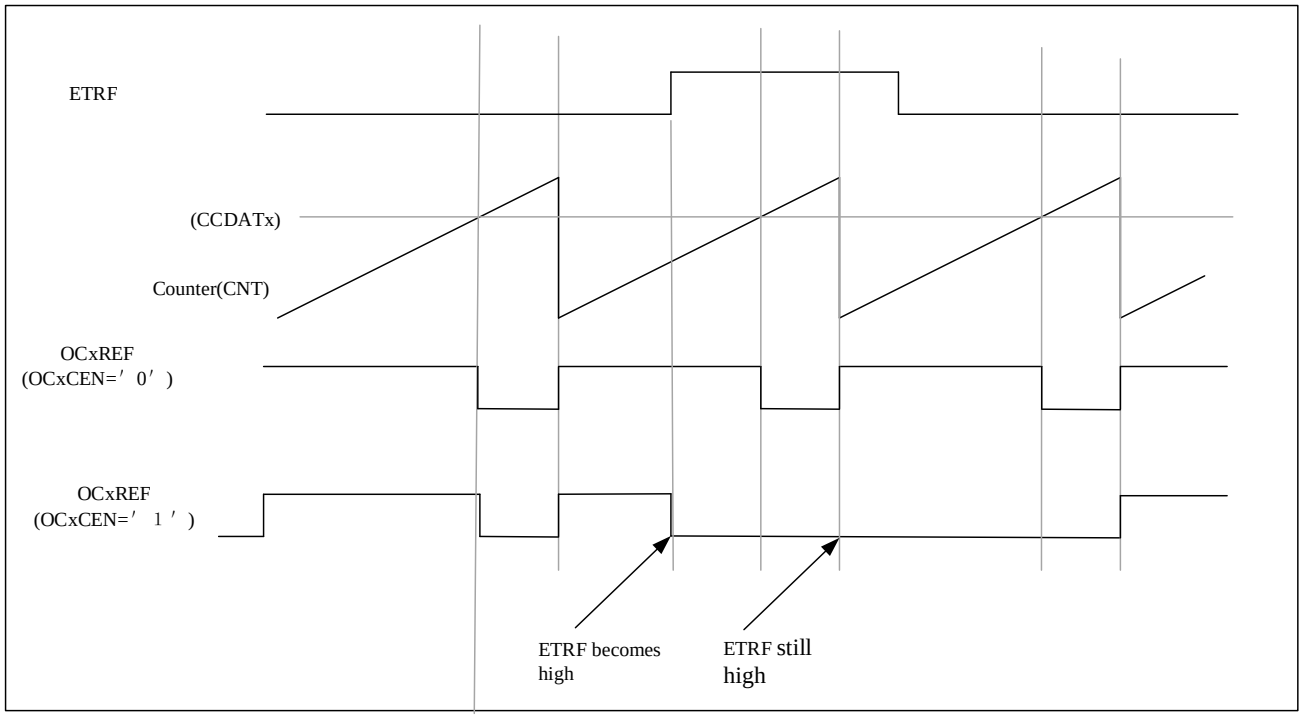
trigger filter as needed.

- Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 19-23 Clearing OCxREF of TIMx



19.5.12 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M4F core halted), depending on the DBG_CTRL. GTIMAx _STOP configuration, the TIMx counter can either continue to work normally or stop.

19.5.13 GTIMAx and External Trigger Synchronization

The timer can be synchronized through triggers in the slave modes (reset, trigger, and gated).

19.5.13.1 Slave Mode: Reset Mode

In reset mode, the trigger event can reset the counter and prescaler. Update the preload register TIMx_AR, TIMx_CCDATx, and generate an update event UEV (TIMx_CTRL1.UPRS=0).

Here is an example of the reset mode:

1. Channel 1 is configured to detect the rising edge of input TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0).
2. Select the mode as reset mode (TIMx_SMCTRL.SMSEL=0100), and trigger input selection as TI1 (TIMx_SMCTRL.TSEL=101).
3. Start the counter (TIMx_CTRL1.CNTEN = 1).

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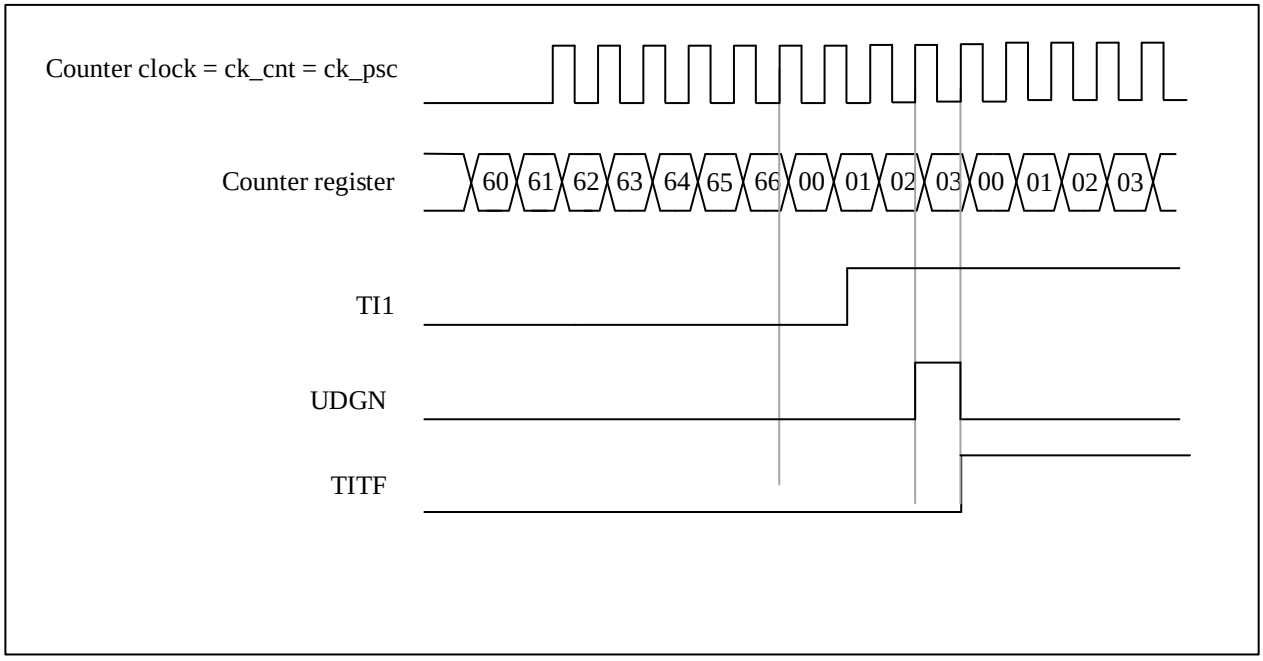
After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and sets the trigger flag (TIMx_STS.TITF=1).

The delay between the rising edge of TI1 and the actual counter reset is caused by the resynchronization circuit of the TI1 input.

Figure 19-24 Control Circuit In Reset Mode



19.5.13.2 Slave Mode : Trigger Mode

In trigger mode, the trigger event (rising edge/falling edge) at the input port can start the counter counting

Here is an example of the trigger mode:

1. Channel 2 is configured as an input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01，TIMx_CCEN.CC2P=0)
2. Select the mode as trigger mode (TIMx_SMCTRL.SMSEL=0110), and trigger input selection as TI2 (TIMx_SMCTRL.TSEL=110).

When TI2 detects a rising edge, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge of TI2 and the actual start of the counter is caused by the resynchronization circuit of the TI2 input.

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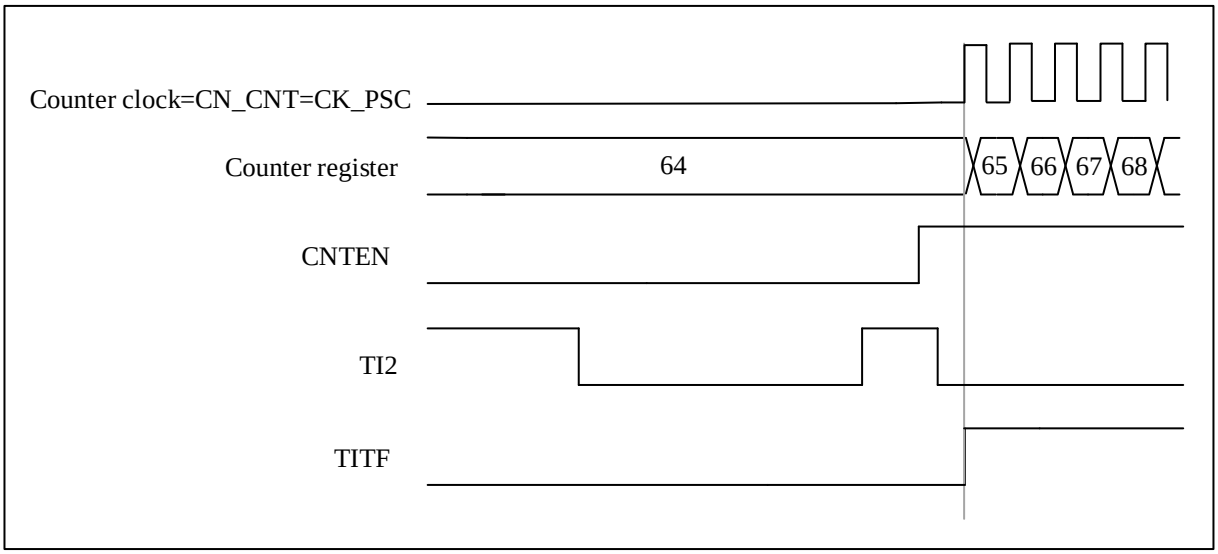
Figure 19-25 Control Circuit In Trigger Mode



19.5.13.3 Slave Mode: Gated Mode

In gated mode, the level polarity of the input port can control whether the counter counts.

Here is an example of the gated mode:

1. Channel 1 is configured to detect low-level effective input on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1);
2. Select the mode as gated mode (TIMx_SMCTRL.SMSEL=0101), and choose TI1 as TRGI (TIMx_SMCTRL.TSEL=101);
3. Start the counter（TIMx_CTRL1.CNTEN = 1）;

When TI1 detects a transition from low to high level, the counter stops counting. When TI1 detects a transition from high to low level, the counter starts counting. The trigger flag is set when counting starts or stops (TIMx_STS.TITF=1).

The delay between the rising edge of TI1 and the actual stop of the counter is caused by the resynchronization circuit of the TI1 input.

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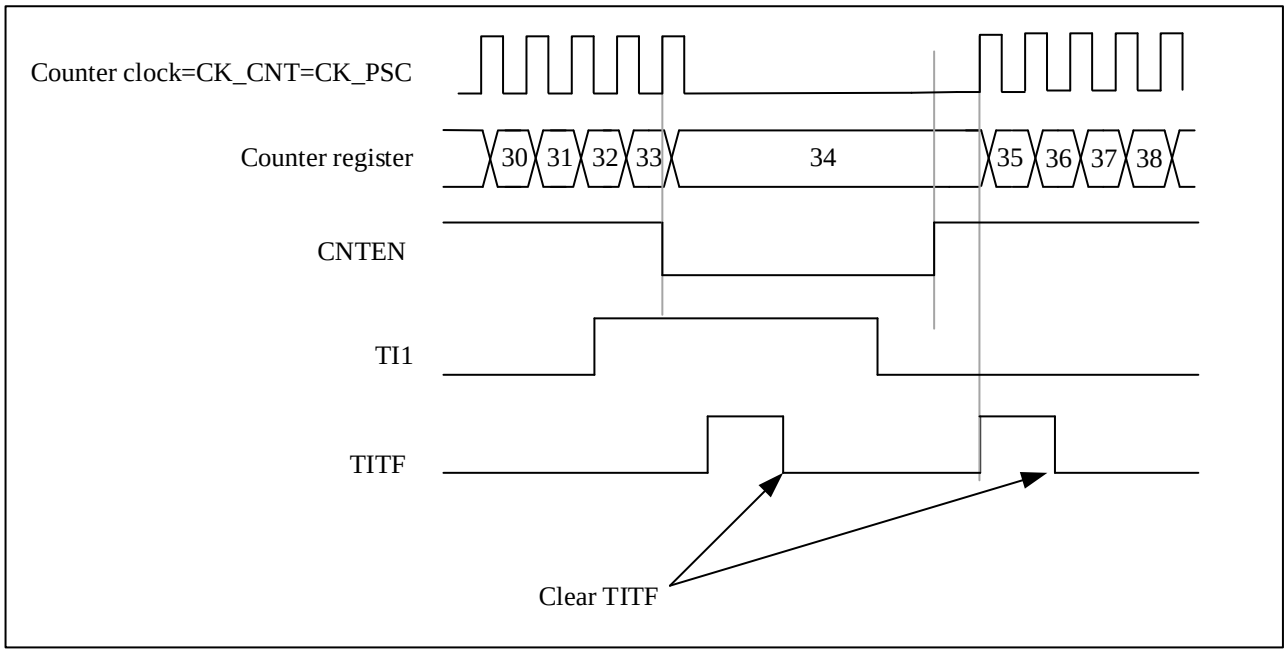
Figure 19-26 Control Circuit In Gated Mode



19.5.13.4 SlaveMode: Trigger Mode + External Clock Mode 2

In reset mode, trigger mode, and gated mode, the counter clock can be selected as External Clock Mode 2, with the ETR signal as the external clock source input. In this case, the trigger selection needs to choose non-ETRF (TIMx_SMCTRL.TSEL=111).

For example:

1. Channel 1 is configured as an input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);
2. Enable External Clock Mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), choose trigger mode as slave mode (TIMx_SMCTRL.SMSEL=0110), and select TRGI as TI1 (TIMx_SMCTRL.TSEL=101);

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and sets the trigger flag (TIMx_STS.TITF=1).

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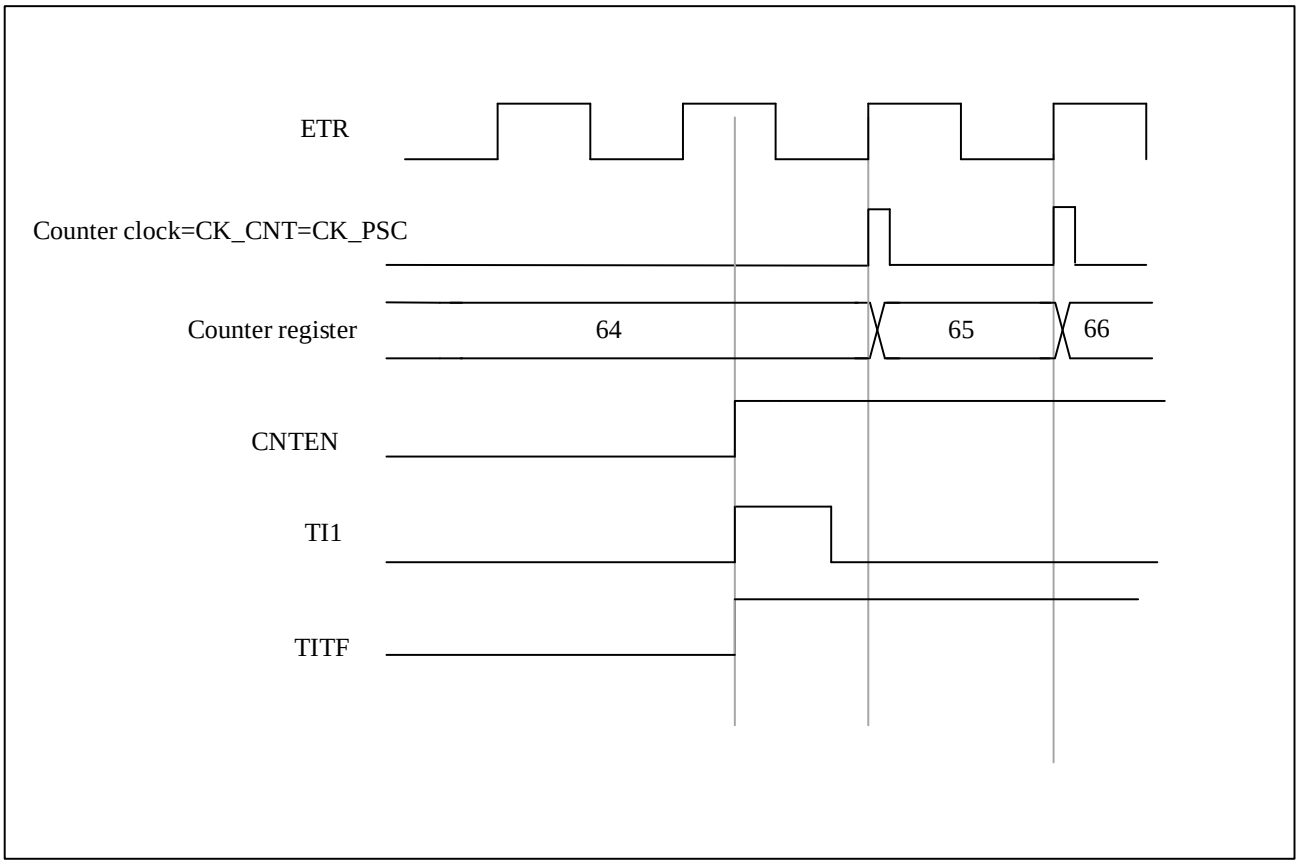
Figure 19-27 Control circuit in External Clock Mode 2 + Trigger Mode.



19.5.14 Timer Synchronization

All TIMx timers are internally interconnected to each other. This implementation allows a master timer to provide trigger to reset, start, stop or provide a clock for the other slave timers. The master clock is used for internal counter and can be prescaled. Below figure shows a block diagram of timer interconnection. The synchronization function does not support dynamic change of the connection. User should configure and enable the slave timer before enabling the master timer's trigger or clock.

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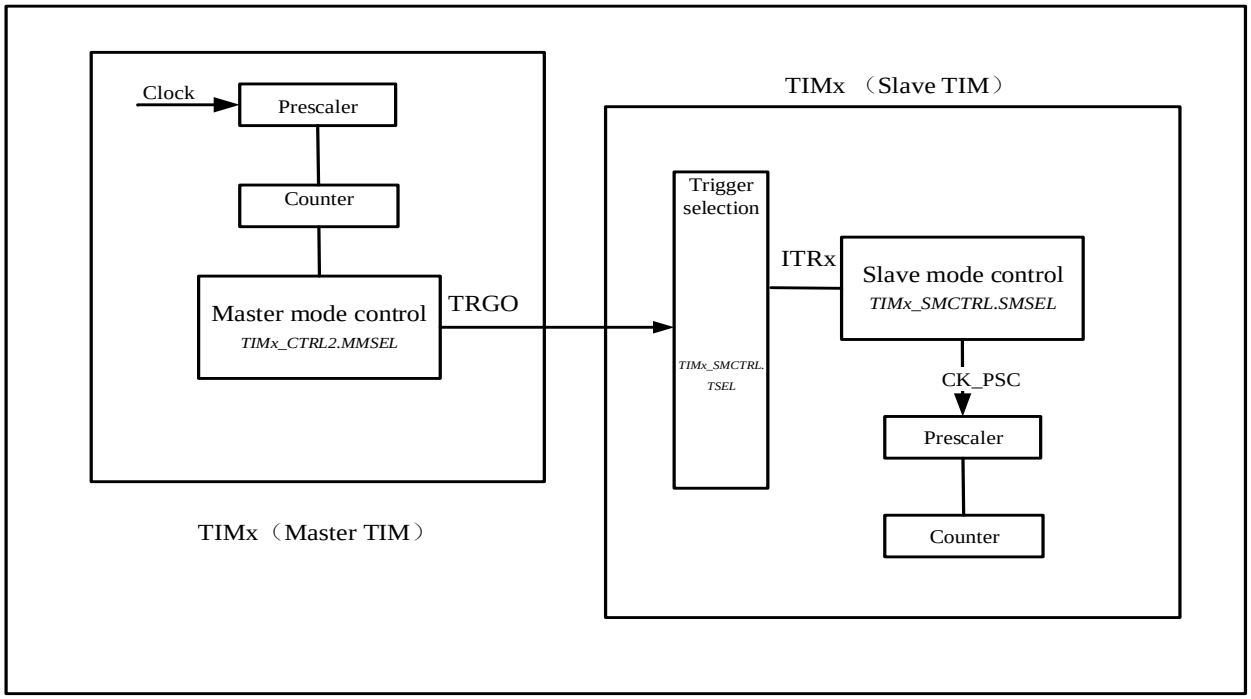
Figure 19-28 Master/Slave Timer Connection



19.5.14.1 Master timer as a prescaler for another timer

ATIM1 acts as the prescaler for GTIMA1. ATIM1 is master timer, and GTIM 1 is slave timer.

User needs to do the following steps for this configuration.

- Set ATIM1_CTRL2.MMSEL='0010' to use the update event of ATIM1 as trigger output.
- Configure GTIMA2_SMCTRL.TSEL= '000'、GTIMA2_INSEK.ITRS='000' to connect the TRGO of ATIM1 to GTIMA2.
- Configure GTIMA2_SMCTRL.SMSEL = '0111' so that the slave mode controller will be configured in external clock mode 1.
- Start GTIMA2 by setting GTIMA2_CTRL1. CNTEN = '1'.
- Start ATIM1 by setting ATIM1_CTRL1. CNTEN = '1'.

Note: If user select OCx as the trigger output of ATIM1 by configuring MMSEL = '01xx', OCx rising edge will be used to drive TIM2.

19.5.14.2 Master timer to enable another timer

In this example, GTIMA2 is enabled by the output compare of ATIM1. GTIMA2 counter will start to count after the OC1REF output from ATIM1 is high. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK_CNT} = f_{CK_INT}/3$).

The configuration steps are shown as below。

- Set ATIM1_CTRL2.MMSEL='0100' to use the OC1REF of ATIM1 as trigger output.
- Configure ATIM1_CCMOD1 register to configure the OC1REF output waveform.

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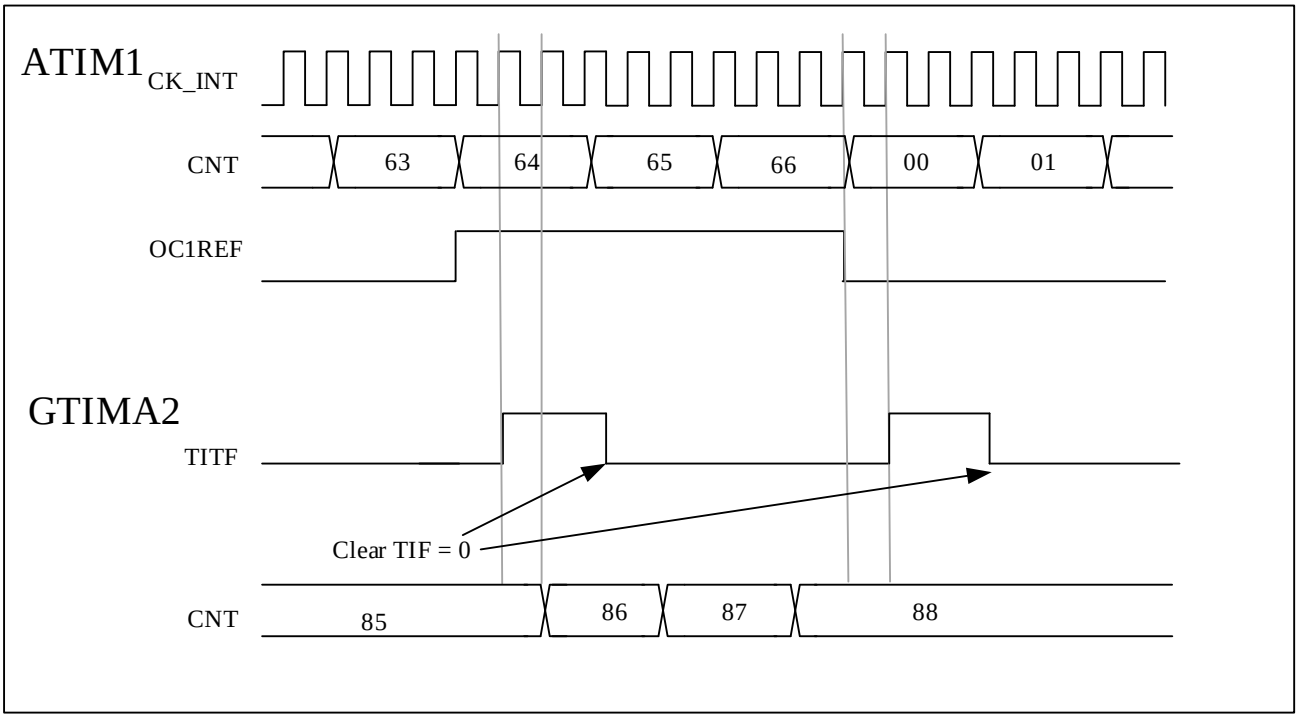
- Set GTIMA2_SMCTRL.TSEL = ‘000’、GTIMA2_INSEL.ITRS=‘000’ to connect ATIM1 trigger output to GTIMA2.
- Set GTIMA2_SMCTRL.SMSEL= ‘0101’ to set GTIMA2 to gated mode.
- Set GTIMA2_CTRL1.CNTEN= ‘1’ to start GTIMA2.
- Set ATIM1_CTRL1.CNTEN= ‘1’ to start ATIM1.

Note: The GTIMA2 clock is not synchronized with the ATIM1 clock, this mode only affects the GTIMA2 counter enable signal.

Figure 19-29 GTIMA2 Gated By OC1REF Of ATIM1



In the next example, it sets the enable of GTIMA2 with enable signal of ATIM1. Set ATIM1.CTRL1.CNTEN = ‘0’ to stop ATIM1. GTIMA2 counts on the divided internal clock only when ATIM1 is enable. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK_CNT} = f_{CK_INT}/3$).

The configuration steps are shown as below:

- Set ATIM1_CTRL2.MMSEL=’0001’ to use the enable signal of ATIM1 as trigger output.
- Set GTIMA2_SMCTRL.TSEL = ‘000’、 GTIMA2__INSEL. ITRS=‘000’ to configure GTIMA2 to get the trigger input from ATIM1.
- Set GTIMA2_SMCTRL.SMSEL = ‘0101’ to configure GTIMA2 in gated mode.
- Set GTIMA2_CTRL1.CNTEN= ‘1’ to start GTIMA2.
- Set ATIM1_CTRL1.CNTEN= ‘1’ to start ATIM1.
- Set ATIM1_CTRL1.CNTEN= ‘0’ to stop ATIM1.

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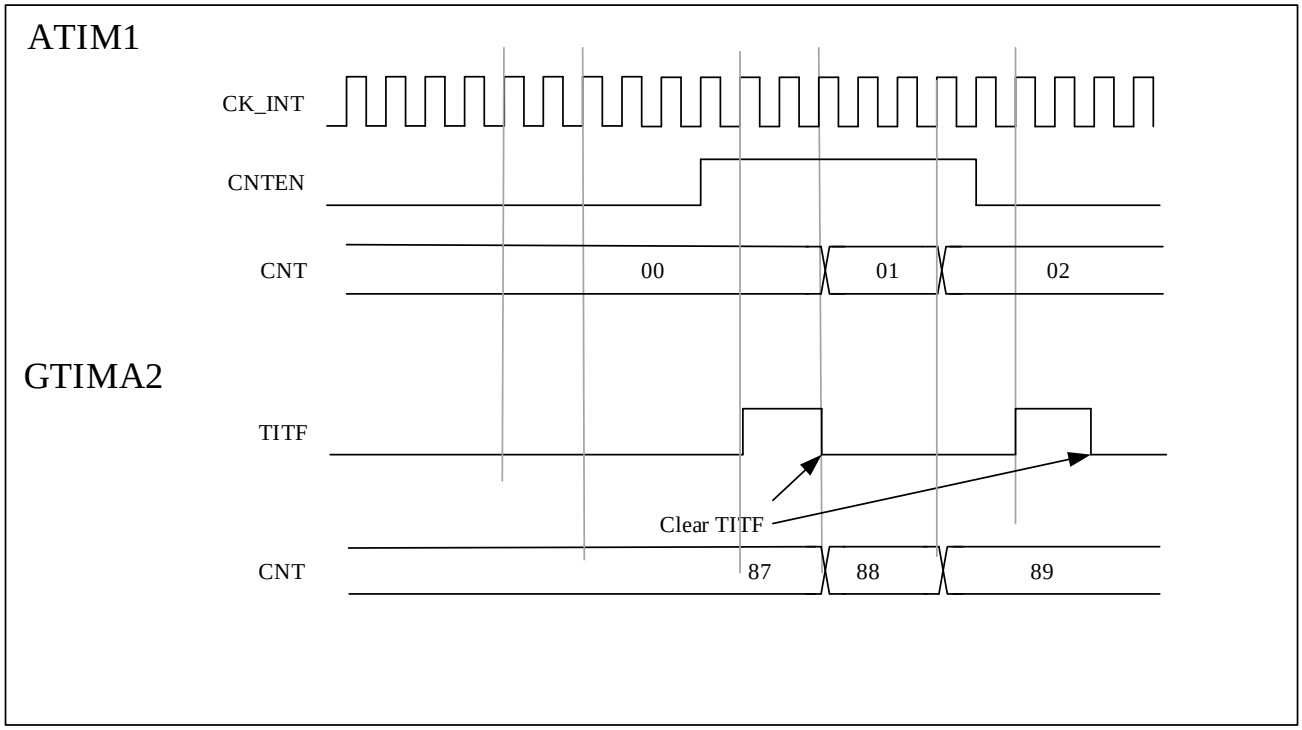
Figure 19-30 GTIMA2 Gated By Enable Signal Of TIM1



19.5.14.3 Master timer to start another timer

In this example, we can use update event as trigger source.ATIM1 is master, GTIMA2 is slave.

The configuration steps are shown as below:

- Set ATIM1_CTRL2.MMSEL=’ 0010’ to use the update event of ATIM1 as trigger output.
- Configure ATIM1_AR register to set the output period.
- Set GTIMA2_SMCTRL .TSEL= ‘000’、 GTIMA2_INSEL. ITRS=‘000’ to connect TIM1 trigger output to GTIMA2.
- Set GTIMA2_SMCTRL. SMSEL = ‘110’ to set GTIMA2 to trigger mode.
- Set ATIM1_CTRL1.CNTEN=1 to start ATIM1.

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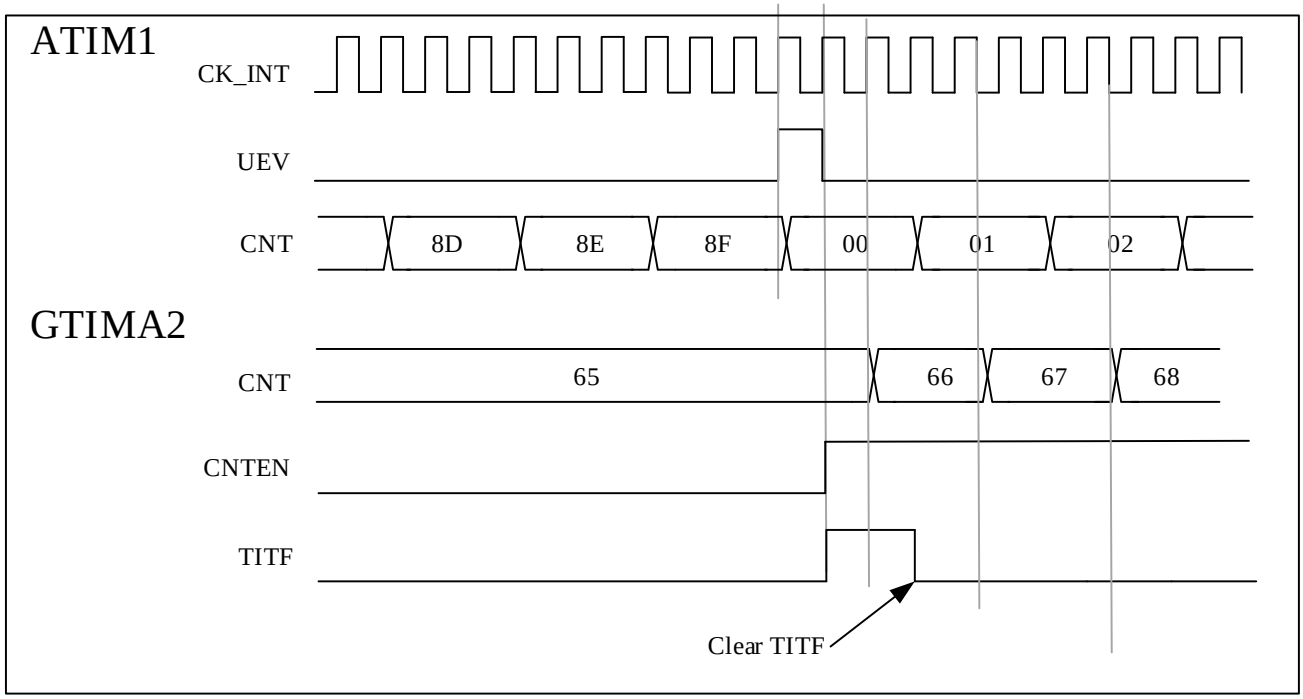
Figure 19-31 Trigger GTIMA2 with An Update Of ATIM1



19.5.14.4 Start 2 timer synchronously using an external trigger

In this example, ATIM1 is enabled when ATIM1's TI1 input rises, and GTIMA2 is enabled when ATIM1 is enabled. To ensure the alignment of counters, ATIM1 must be configured in master/slave mode. For TI1, ATIM1 is the slave; for GTIMA2, ATIM1 is the master.

The configuration steps are shown as below:

- Set ATIM1.MMSEL = '0001' to use the enable signal as trigger output.
- Set ATIM1_SMCTRL.TSEL = '100' to configure the ATIM1 to slave mode and receive the trigger input of TI1.
- Set ATIM1_SMCTRL.SMSEL = '0110' to configure ATIM1 to trigger mode.
- Set ATIM1_SMCTRL.MSMD = '1' to configure ATIM1 to master/slave mode.
- Set GTIMA2_SMCTRL.TSEL = '000'、GTIMA2_INSEL. ITRS='000' to connect ATIM1 trigger output to GTIMA2.
- Set GTIMA2_SMCTRL.SMSEL = '0110' to configure GTIMA2 to trigger mode.

When TI1 rising edge arrives, both timers start counting synchronously according to the internal clock, and both TITF flags are set simultaneously.

Note：The following figure shows a delay between CNTEN and CK_PSC of ATIM1 in master/slave mode.

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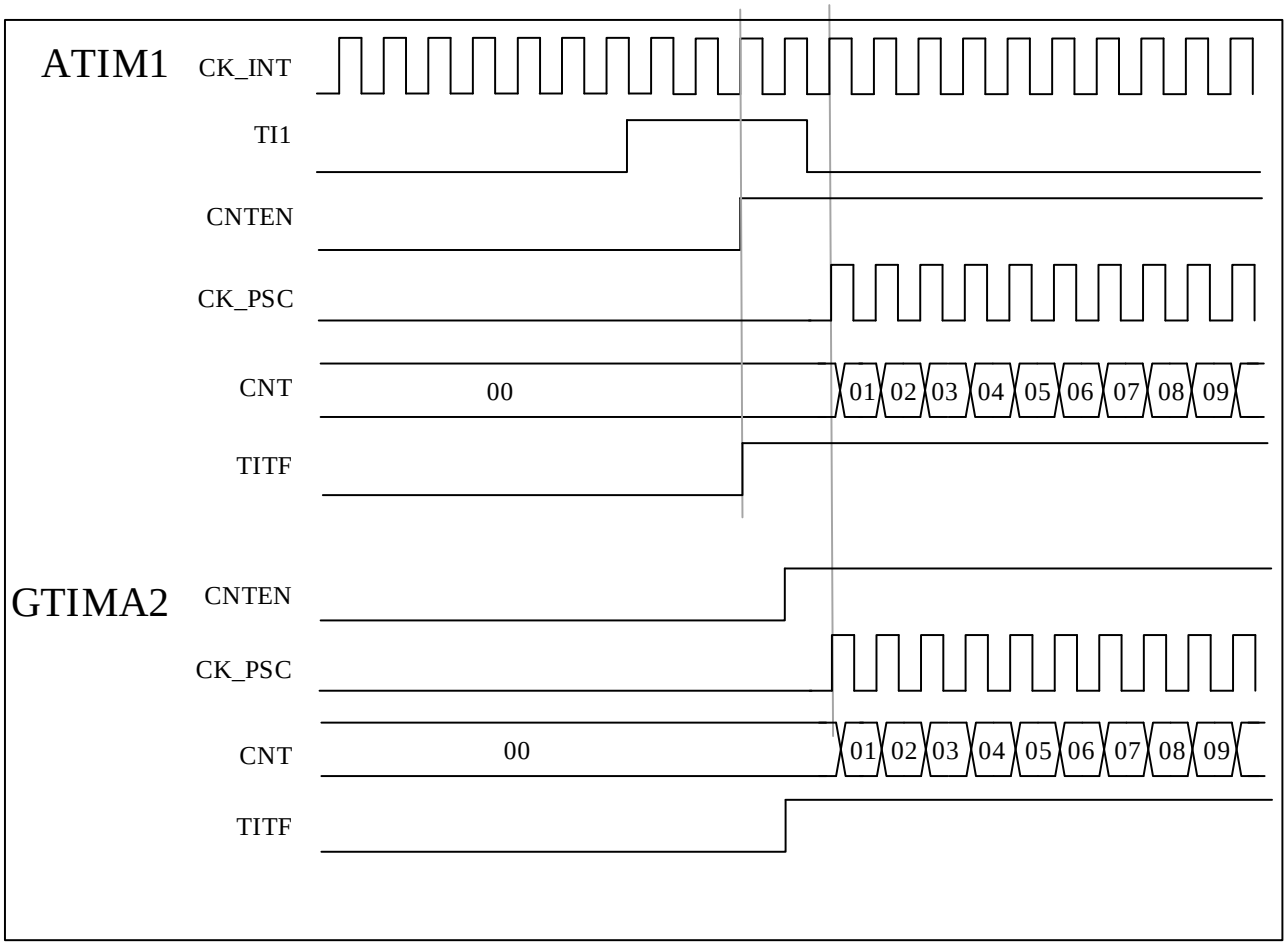
Figure 19-32 Triggers ATIM1 And GTIMA2 Using The TI1 Input Of ATIM1



19.5.15 Trigger ADC

The timer can generate ADC trigger events through various internal signals, such as reset, enable, or comparison events, and can also generate pulse triggers issued by the internal edge detector. The triggering signal issued on the internal line redirected to the ADC can be selected through the MMSEL[3:0] bits in the TIMx_CTRL2 register.

19.5.16 Encode interface mode

19.5.16.1 Quadrature Coding Mode

The encoder uses two inputs TI1 and TI2 as an interface. And the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are five types of quadrature encoder counting modes:

- Encode Mode 1: The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘0001’;
- Encode Mode 2: The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’0010’;
- Encode Mode 3: The counter counts on both TI1 and TI2 edges, TIMx_SMCTRL.SMSEL = ‘0011’;
- Encode Mode 4: T2 in high level, the counter counts on TI1 edges, TIMx_SMCTRL.SMSEL = ‘1001’;

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■ Encode Mode 5: T1 in high level, the counter counts on TI2 edges, TIMx_SMCTRL.SMSEL = '1010'.

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in following table:

Table 19-10 The Relationship Between The Counting Direction And The Encoder Signal (CC1P=CC2P=0)

Active Edge	SMSEL[3:0]	Relative Signal Level (TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rising	Falling	Rising	Falling
Counting only at TI1	0001	High	Counting down	Counting up	Don't count	Don't count
		Low	Counting up	Counting down	Don't count	Don't count
Counting only at TI2	0010	High	Don't count	Don't count	Counting up	Counting down
		Low	Don't count	Don't count	Counting down	Counting up
Counting on TI1 and TI2	0011	High	Counting down	Counting up	Counting up	Counting down
		Low	Counting up	Counting down	Counting down	Counting up
Counting only at TI1 and T2 in high level	1001	High	Counting down	Counting up	Don't count	Don't count
		Low	Don't count	Don't count	Don't count	Don't count
Counting only at T2 and T1 in high level	1010	High	Don't count	Don't count	Counting up	Counting down
		Low	Don't count	Don't count	Don't count	Don't count

The changes in the counter value of the counter in each mode are as follows:

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Figure 19-33 The Encode Counts Only on TI1

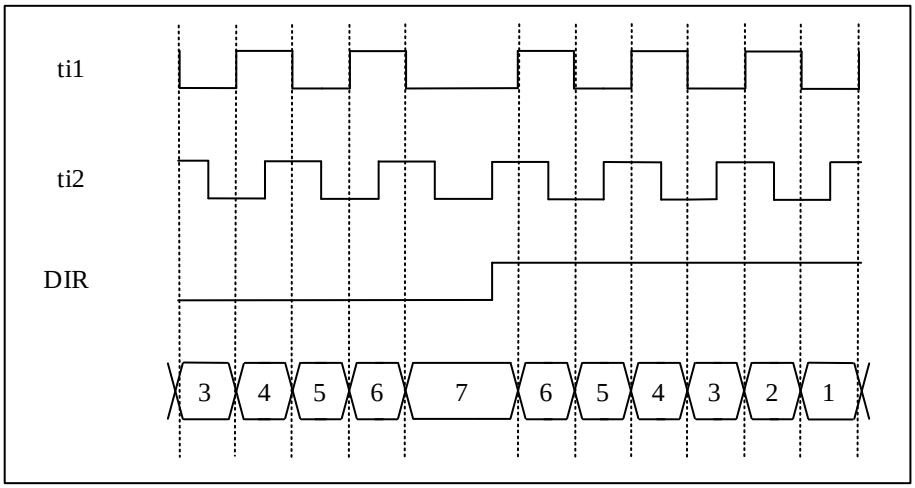

Figure 19-34 The Encode Counts Only on TI2

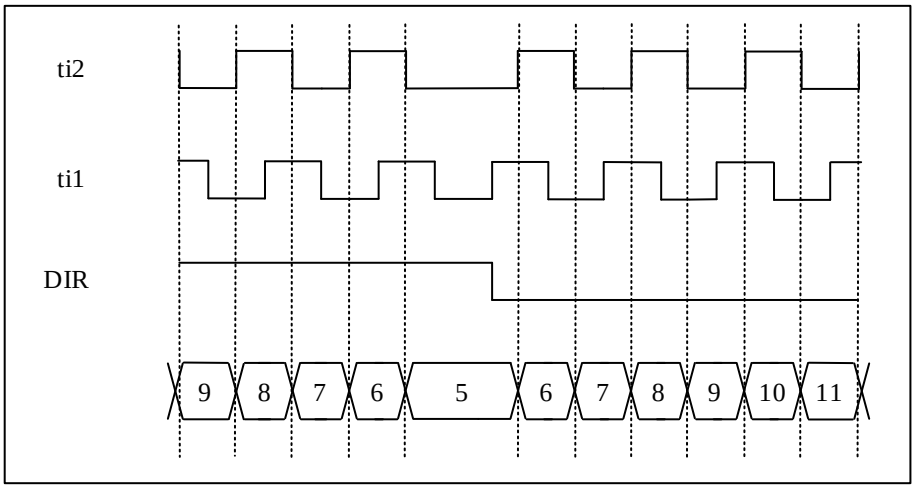

Figure 19-35 The Encoder Counts on Both TI1 and TI2

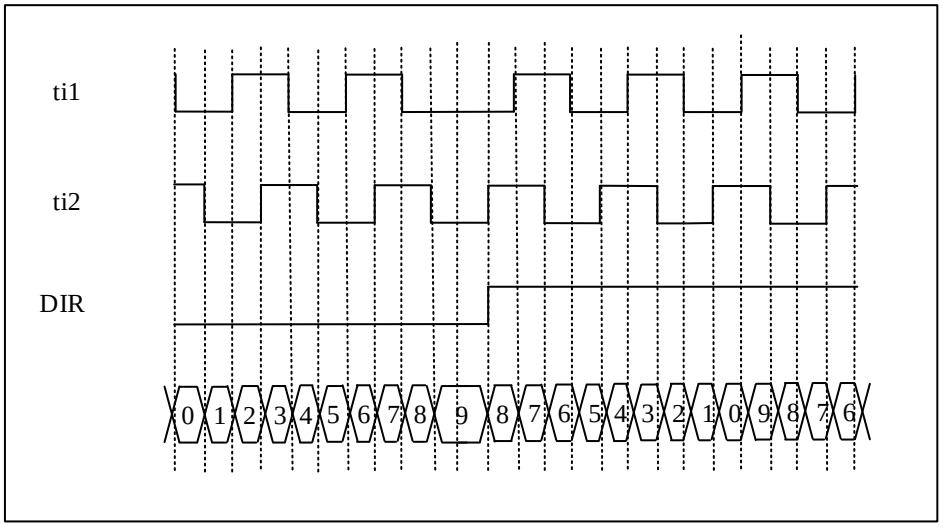

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Figure 19-36 When T2 is high level, the counter only counts on TI1

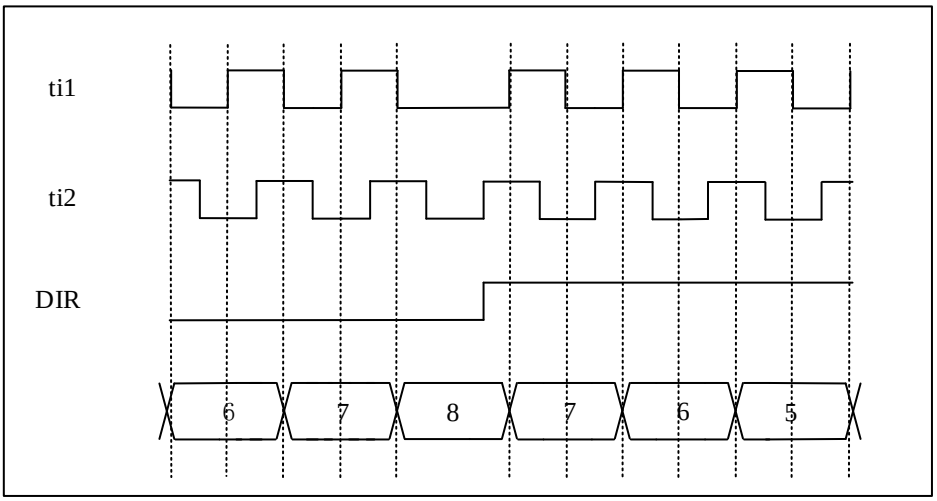
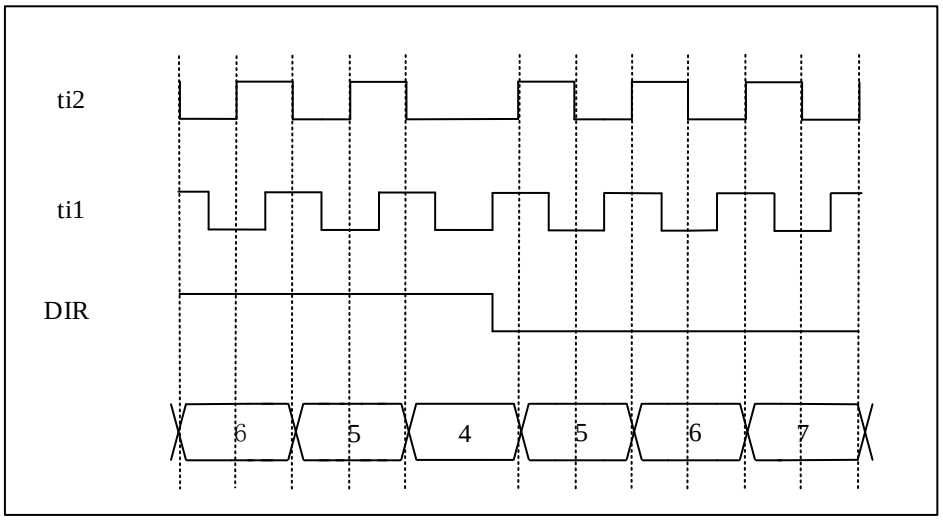


Figure 19-37 When T1 is high level, the counter only counts on TI2



Here is an example of an encoder with dual edges triggering selected to suppress input jitter：

1. IC1FP1 is mapped to TI1(TIMx_CCMOD1.CC1SEL=‘01’), IC1FP1 is not inverted(TIMx_CCEN.CC1P=‘0’);
2. IC1FP2 is mapped to TI2(TIMx_CCMOD2.CC2SEL=‘01’), IC2FP2 is not inverted(TIMx_CCEN.CC2P=‘0’);
3. The input is valid on both rising and falling edges(TIMx_SMCTRL.SMSEL=‘0011’);
4. Enable counter TIMx_CTRL1.CNTEN=‘1’;

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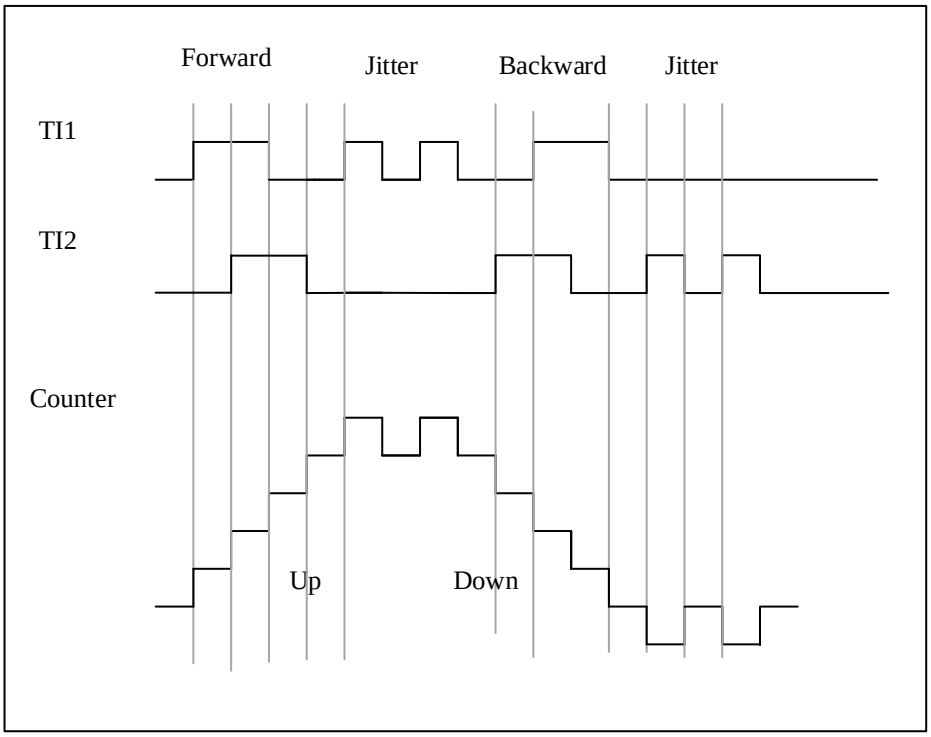
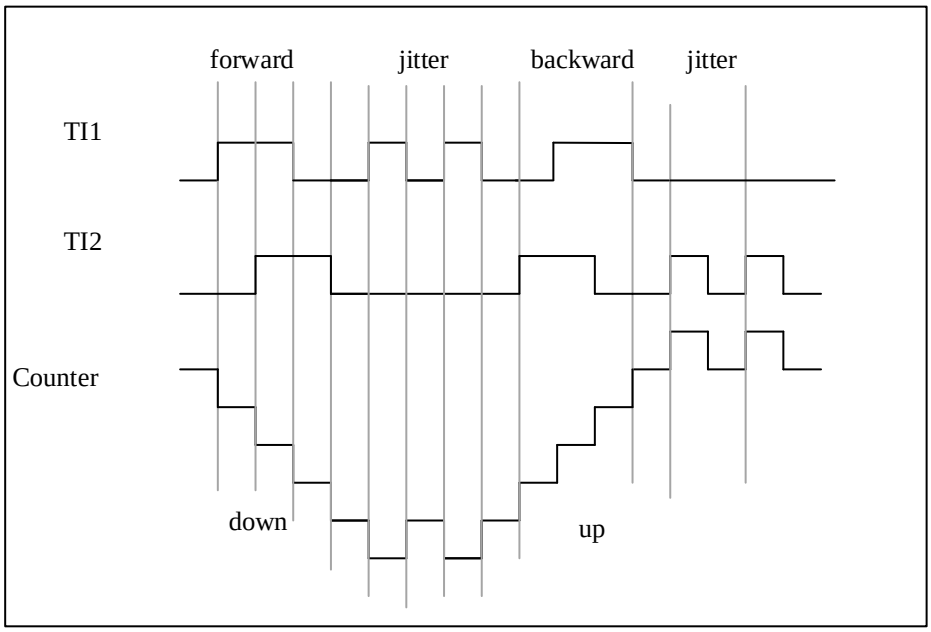
Figure 19-38 Example Of Counter Operation In Encoder Interface Mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P='1', other configurations are the same as above)

Figure 19-39 Encoder Interface Mode Example With IC1FP1 Polarity Inverted



19.5.16.2 Pulse Level Encoding Mode

In the pulse level encoding mode, the clock is provided on a single line on TI2, while the counting direction is provided by the TI1 input.

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This mode is enabled through the SMSEL[3:0] in the TIMx_SMCTRL register, as follows。

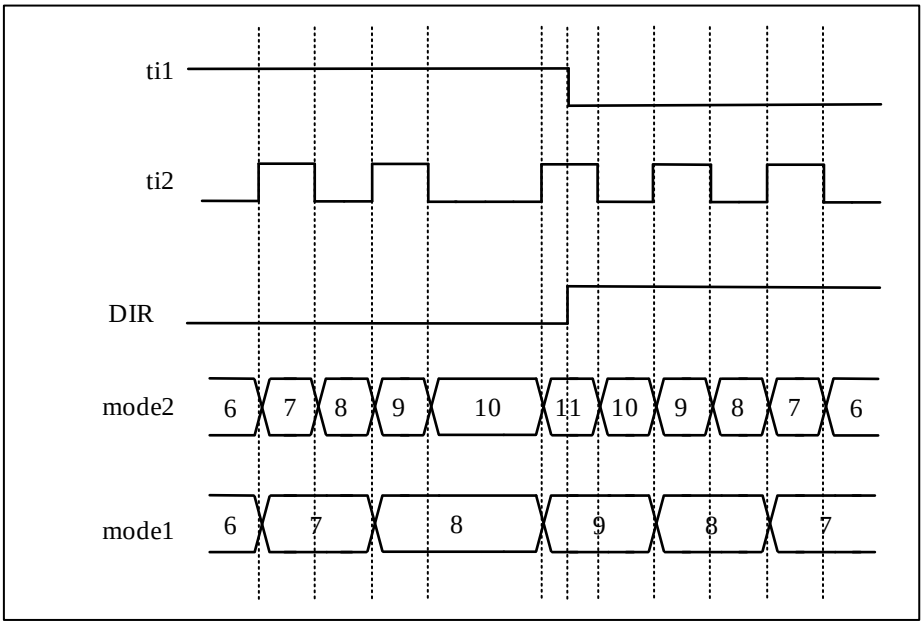
1011：In pulse level encoding mode 2, the counter is updated on both the rising and falling edges of the clock.

1100：In pulse level encoding mode 1, the counter is updated on a single clock edge based on the value of CC2P. CC2P=0 corresponds to counting on the rising edge, and CC2P=1 corresponds to counting on the falling edge.

The polarity of the direction signal of TI1 is set through the CC1P bit. When CC2P=0, counting is up when TI1 is high, counting down when TI1 is low; when CC1P=1, counting is up when TI1 is low, counting down when TI1 is high.

The following diagram takes CC1P=CC2P=0 as an example：

Figure 19-40 Pulse Level Encoding Mode (CC1P=CC2P=0)



19.5.16.3 Dual Pulse Encoding Mode

In the dual pulse encoding mode, the clock is provided on two lines, and only one line is provided at a time based on different direction. This results in one clock line for counting up and one clock line for counting down.

This mode is enabled through the SMSEL[3:0] field in the TIMx_SMCTRL register, as follows:

- 1000: In Dual Pulse Encoding Mode 2, the counter is updated on both the rising and falling edges of either of the two clock lines. The CC1P and CC2P bits encode the idle state of the clock. CCxP=0 corresponds to a high level idle state, and CCxP=1 corresponds to a low level idle state.
- 1111: In Dual Pulse Encoding Mode 1, the counter is updated on a single clock edge based on the values of the CC1P and CC2P bits. CCxP=0 corresponds to the falling edge and high level state, while CCxP=1 corresponds to the rising edge and low level state.

The table below describes the relationship between counting direction and encoder signal and polarity settings.

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Table 19-11 Relationship Between Counting Direction And Encoder Signal And Polarity Settings

Dual pulse encoding mode	SMSEL[3:0]	Relative Signal Level (TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rising	Falling	Rising	Falling
Mode 2 CCxP=0	1000	high	Counting down	Counting down	Counting up	Counting up
		low	Don't count	Don't count	Don't count	Don't count
Mode 2 CCxP=1	1000	high	Don't count	Don't count	Don't count	Don't count
		low	Counting down	Counting down	Counting up	Counting up
Mode 1 CCxP=0	1111	high	Don't count	Counting down	Don't count	Counting up
		low	Don't count	Don't count	Don't count	Don't count
Mode 1 CCxP=1	1111	high	Don't count	Don't count	Don't count	Don't count
		low	Counting down	Don't count	Counting up	Don't count

The following diagram shows the counting method of the dual pulse encoding mode counter.

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Figure 19-41 Dual Pulse Encoding Mode (CC1P = CC2P = 0)

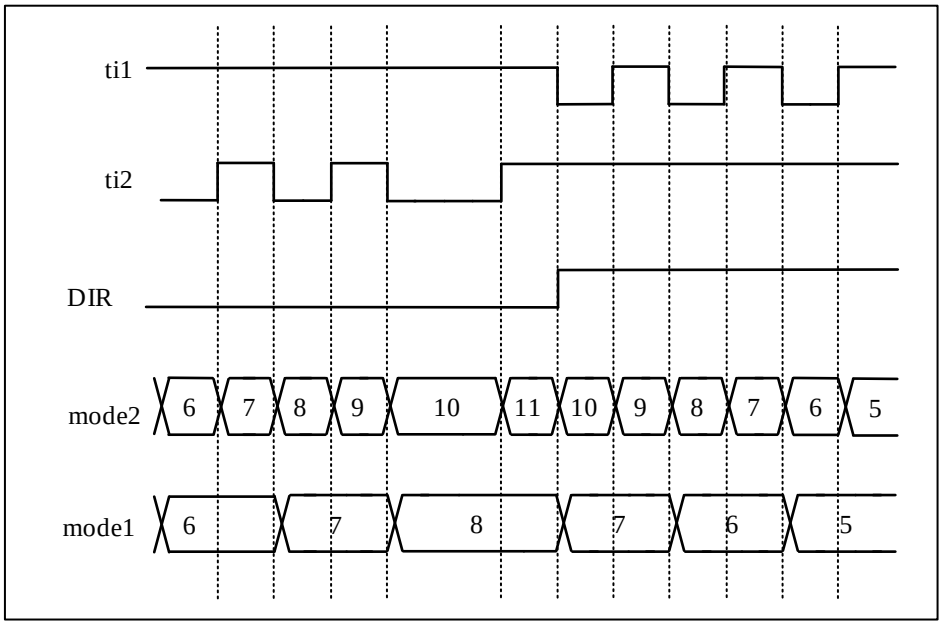
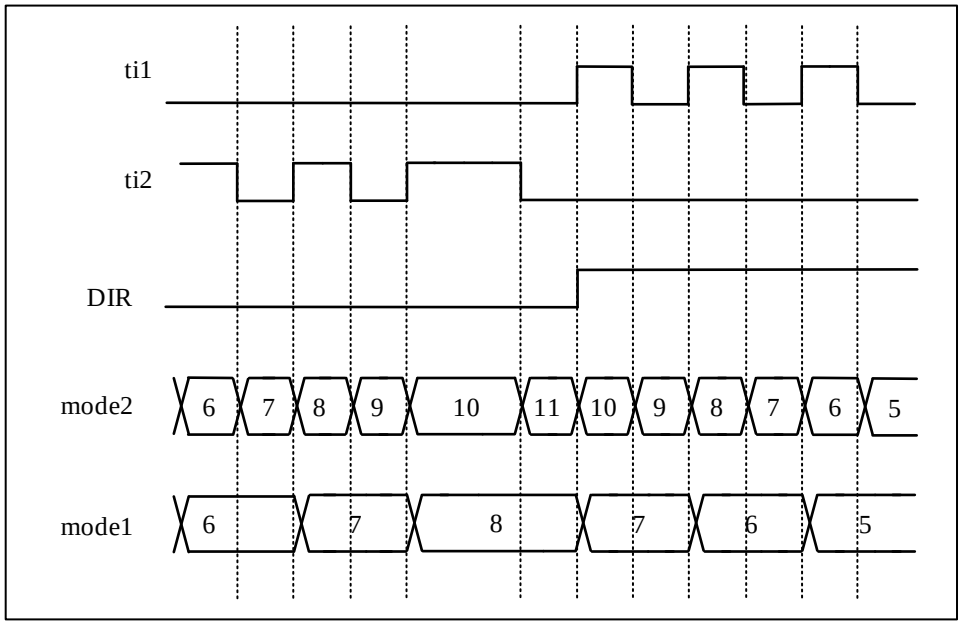


Figure 19-42 Dual Pulse Encoding Mode (CC1P = CC2P = 1)



19.5.17 Interface with Hall Sensors

See Section18.4.22.

19.6 GTIMAx(x=1-7)Register Description

For abbreviations used in the register description, refer to Section 1.1.

These peripheral registers can be accessed in half-word (16-bit) or word (32-bit) mode.

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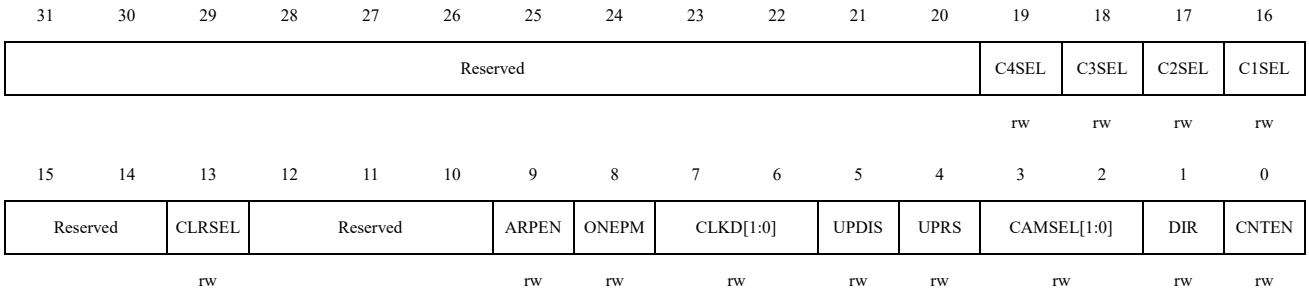
19.6.1 Control Register 1（TIMx_CTRL1）

Offset address：0x00

Reset value：0x0000 0000



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
19	C4SEL	Channel 4 Selection 0: Select CH4 signal (Specific selection can be seen in TIMx_INSEL.TI4S) 1: For GTIMA1, select the HSE/128 input, select the CH4 signal (from HSE/128)
18	C3SEL	Channel 3 Selection 0: Select CH3 signal（Specific selection can be seen in TIMx_INSEL.TI3S） 1: For GTIMA1, select the LSI input, select the CH3 signal (from LSI)
17	C2SEL	Channel 2 Selection 0: Select CH2 signal（Specific selection can be seen in TIMx_INSEL.TI2S） 1: For GTIMA1, select the LSE input, select the CH2 signal (from LSE)
16	C1SEL	Channel 1 Selection 0: Choose the CH1 signal (specific selection can be seen in TIMx_INSEL.TI1S) 1: Reserved
15:14	Reserved	Reserved, the reset value must be maintained
13	CLRSEL	OcxRef Clear Selection 0: Select the external Ocxclr (TIMx_ETR) signal, specific selection can be seen in TIMx_INSEL.ETRS 1: Choose the internal Ocxclr (tim_ocref_clr) signal, specific selection can be seen in TIMx_INSEL.CLRS
12:10	Reserved	Reserved, the reset value must be maintained
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs。 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	CLKD[1:0]	Clock division

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Bit Field	Name	Description
		CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and t_{DTS} (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK_INT}$. 01: $t_{DTS} = 2 \times t_{CK_INT}$ 10: $t_{DTS} = 4 \times t_{CK_INT}$ 11: Reserved, do not use this configuration
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request – Counter overflow/underflow – TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting。 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting。 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting。 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting。 *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1)*
1	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*

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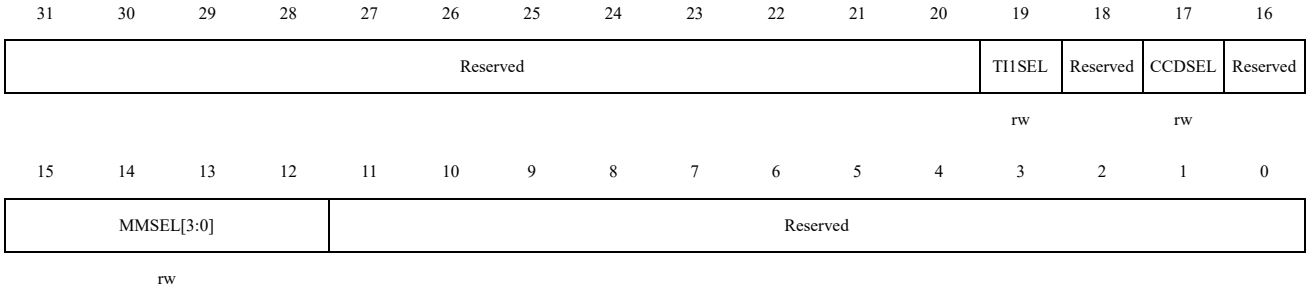
Bit Field	Name	Description
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

19.6.2 Control Register 2（TIMx_CTRL2）

Offset address: 0x04

Reset value: 0x0000 0000



Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input; 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
18	Reserved	Reserved, the reset value must be maintained
17	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent； 1: When an update event occurs, a DMA request for CCx is sent.
16	Reserved	Reserved, the reset value must be maintained
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits (TIMx_CTRL2. MMSEL [3:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows： x000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the later case, the signal on TRGO is delayed compared to the actual reset. x001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO

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Bit Field	Name	Description
		except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). x010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. x011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. x100: Compare - OC1REF signal is used as the trigger output (TRGO). x101: Compare - OC2REF signal is used as the trigger output (TRGO). x110: Compare - OC3REF signal is used as the trigger output (TRGO). x111: Compare - OC4REF signal is used as the trigger output (TRGO)
11:0	Reserved	Reserved, the reset value must be maintained

19.6.3 Status Registers（TIMx_STS）

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TITF	Reserved	UDITF
													rc_w0		rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved				CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0					rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred； 1: Trigger interrupt occurred.
17	Reserved	Reserved, the reset value must be maintained
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and repetition counter value overflow or underflow (when repetition counter equal to 0 an update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT.

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Bit Field	Name	Description
		–When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag See TIMx_STS.CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred; 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
7:4	Reserved	Reserved, the reset value must be maintained.
3	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode：** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.

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19.6.4 Event Generation Registers（TIMx_EVTGEN）

Offset address: 0x0C

Reset values: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TGN	Reserved	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
					w		w					w	w	w	w

Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action No action 1: Generated a trigger event
9	Reserved	Reserved, the reset value must be maintained
8	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
2	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
1	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated.

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Bit Field	Name	Description
		When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

19.6.5 Slave Mode Control Register（TIMx_SMCTRL）

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								OCREFCLRF[3:0]				OCREF CLRP	Reserved		MSMD
									rw			rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS		SMSEL[3:0]				Reserved	TSEL[2:0]		
rw				rw	rw	rw		rw					rw		

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	OCREFCLRF	tim_ocref_clr signal filter These bits are used to define the frequency at which the tim_ocref_clk signal is sampled and the bandwidth of the tim_ocref_clr digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS/8}$，N=6 0001: $f_{SAMPLING}=f_{CK_INT}$，N=2 1001: $f_{SAMPLING}=f_{DTS/8}$，N=8 0010: $f_{SAMPLING}=f_{CK_INT}$，N=4 1010: $f_{SAMPLING}=f_{DTS/16}$，N=5 0011: $f_{SAMPLING}=f_{CK_INT}$，N=8 1011: $f_{SAMPLING}=f_{DTS/16}$，N=6 0100: $f_{SAMPLING}=f_{DTS/2}$，N=6 1100: $f_{SAMPLING}=f_{DTS/16}$，N=8 0101: $f_{SAMPLING}=f_{DTS/2}$，N=8 1101: $f_{SAMPLING}=f_{DTS/32}$，N=5 0110: $f_{SAMPLING}=f_{DTS/4}$，N=6 1110: $f_{SAMPLING}=f_{DTS/32}$，N=6 0111: $f_{SAMPLING}=f_{DTS/4}$，N=81111: $f_{SAMPLING}=f_{DTS/32}$，N=8
19	OCREFCLRP	tim_ocref_clr signal polarity This bit is used to select whether the trigger operation is to use tim_ocref_clr or the inversion of tim_ocref_clr. 0: tim_ocref_clr active at high level or rising edge. 1: tim_ocref_clr active at a low level or falling edge.
18:17	Reserved	Reserved, the reset value must be maintained

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16	MSMD	Master/slave mode 0: No effect; 1: The event on the trigger input (TRGI) is delayed to allow perfect synchronization between the current timer (via TRGO) and its slave timers. This is very useful for cases where multiple timers need to be synchronized to a single external event.
15:12	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS/8}$，N=6 0001: $f_{SAMPLING}=f_{CK_INT}$，N=2 1001: $f_{SAMPLING}=f_{DTS/8}$，N=8 0010: $f_{SAMPLING}=f_{CK_INT}$，N=4 1010: $f_{SAMPLING}=f_{DTS/16}$，N=5 0011: $f_{SAMPLING}=f_{CK_INT}$，N=8 1011: $f_{SAMPLING}=f_{DTS/16}$，N=6 0100: $f_{SAMPLING}=f_{DTS/2}$，N=6 1100: $f_{SAMPLING}=f_{DTS/16}$，N=8 0101: $f_{SAMPLING}=f_{DTS/2}$，N=8 1101: $f_{SAMPLING}=f_{DTS/32}$，N=5 0110: $f_{SAMPLING}=f_{DTS/4}$，N=6 1110: $f_{SAMPLING}=f_{DTS/32}$，N=6 0111: $f_{SAMPLING}=f_{DTS/4}$，N=8 1111; $f_{SAMPLING}=f_{DTS/32}$，N=8
11	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use tim_etr_in or the inversion of tim_etr_in. 0: tim_etr_in active at high level or rising edge. 1: tim_etr_in active at low level or falling edge.
10	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0：External clock mode 2 disable. 1：External clock mode 2 enable. *Note1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
7:4	SMSEL[3:0]	Slave mode selection

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		When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 0000 : Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock.。 0001 : Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1。 0010 : Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 0011 : Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2 0100 : Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated 0101 : Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled 0110 : Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 0111 : External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). 1000 : Dual input mode2. 1001 : Quadrature encoder mode 4 - The counter counts up/down on the edge of TI1FP1 according to the level of TI2FP2. Select the counting edge with CC1P. 1010 : Quadrature encoder mode 5 - The counter counts up/down on the edge of TI2FP2 according to the level of TI1FP1. Select the counting edge with CC2P 1011 : Pulse level encoding mode 2. 1100 : Pulse level encoding mode 1. Set the counting edge of TI2FP2 with CC2P. 1101 : Combined gated + reset mode - When the trigger input (TRGI) is high, the counter's clock is enabled. Once the trigger input becomes low, the counter stops (and resets). The start and stop of the counter are both controlled. 1110 : Combined reset + trigger mode - The counter starts (and resets) on the rising edge of the trigger input TRGI, with only the start of the counter being controlled 1111 : Dual input mode 1. Set the counting sensitive edges of TI1FP1 and TI2FP2 with CC1P and CC2P. *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*
3	Reserved	Reserved, the reset value must be maintained
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter.

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		0xx：Internal trigger x (ITRx), Select the ITR signal source based on TIMx_INSEL. ITRS 100：Edge detector for TI1 (TI1F_ED) 101：Filtered timer input 1 (TI1FP1) 110：Filtered timer input 2 (TI2FP2) 111：External trigger input (ETRF) *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*

19.6.6 DMA/Interrupt Enable Register（TIMx_DINTEN）

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										TDEN	Reserved	UDEN	Reserved	TIEN	UIEN
										rw		rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved				CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request. 1: Enable trigger DMA request
20	Reserved	Reserved, the reset value must be maintained
19	UDEN	Update DMA request enable 0: Disable update DMA request. 1: Enable update DMA request
18	Reserved	Reserved, the reset value must be maintained
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request

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Bit Field	Name	Description
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt

19.6.7 Capture/Compare Mode Register 1（TIMx_CCMOD1）

Offset address: 0x18
Reset value: 0x0000 0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode：

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output. 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:5	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by tim_ocref_clr_in input level. 1: OC1REF is cleared immediately when the tim_ocref_clr_in input level is detected as high(the source of tim_ocref_clr_in is controlled by TIMx_CTRL1.CLRSEL).
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is

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Bit Field	Name	Description
		ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
2	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output. 01: CC1 channel is configured as input, IC1 is mapped on TI1. 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

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Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel: 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS}/8$，N=6 0001: $f_{SAMPLING}=f_{CK_INT}$，N=2 1001: $f_{SAMPLING}=f_{DTS}/8$，N=8 0010: $f_{SAMPLING}=f_{CK_INT}$，N=4 1010: $f_{SAMPLING}=f_{DTS}/16$，N=5 0011: $f_{SAMPLING}=f_{CK_INT}$，N=8 1011: $f_{SAMPLING}=f_{DTS}/16$，N=6 0100: $f_{SAMPLING}=f_{DTS}/2$，N=6 1100: $f_{SAMPLING}=f_{DTS}/16$，N=8 0101: $f_{SAMPLING}=f_{DTS}/2$，N=8 1101: $f_{SAMPLING}=f_{DTS}/32$，N=5 0110: $f_{SAMPLING}=f_{DTS}/4$，N=6 1110: $f_{SAMPLING}=f_{DTS}/32$，N=6 0111: $f_{SAMPLING}=f_{DTS}/4$，N=8 1111: $f_{SAMPLING}=f_{DTS}/32$，N=8
3:2	IC1PSC[1:0]	Input capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events

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1:0	CC1SEL[1:0]	Capture/Compare 1 Selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

19.6.8 Capture/Compare Mode Register 2（TIMx_CCMOD2）

Offset address: 0x1C
Reset value: 0x0000 0000

See the description of the CCMOD1 register above

Output comparison mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode
12	OC4CEN	Output compare 4 clear enable
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:5	OC3MD[2:0]	Output compare 3 mode
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable

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1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

19.6.9 Capture/Compare Enable Registers（TIMx_CCEN）

Offset address: 0x24

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN	Reserved	
rw	rw			rw	rw			rw	rw			rw	rw		

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
14	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
13:12	Reserved	Reserved, the reset value must be maintained.
11	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
10	CC3EN	Capture/Compare 3 output enabl） See TIMx_CCEN.CC1EN description.
9:8	Reserved	Reserved, the reset value must be maintained.
7	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
6	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
5:4	Reserved	Reserved, the reset value must be maintained.
3	CC1P	Capture/Compare 1 output polarity **When the corresponding channel of CC1 is in output mode:** 0: OC1 active high 1: OC1 active low **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted.
2	CC1EN	Capture/Compare 1 output enable **When the corresponding channel of CC1 is in output mode:** 0: Disable - Disable output OC1 signal. Therefore, the output level of OC1 depends on the values of MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits.

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Bit Field	Name	Description
		1: Enable - Enable output OC1 signal. The OC1 signal is output to the corresponding output pin, and its output level depends on the values of the MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. **When the corresponding channel of CC1 is in input mode:** At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture
1:0	Reserved	Reserved, the reset value must be maintained.

Table 19-12 Output Control Bits Of Standard Ocx Channel

CCxEN	OCx output status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: The state of external I/O pins connected to standard OCx channels depends on the OCx channel state and GPIO and AFIO registers.

19.6.10 Capture/Compare Register 1（TIMx_CCDAT1）

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT1[15:0]	Capture/Compare 1 value **CC1 channel is configured as output:** CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. **CC1 channel is configured as input:** CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

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19.6.11 Capture/Compare Register 2（TIMx_CCDAT2）

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT2[15:0]	Capture/Compare 2 value **CC2 channel is configured as output:** CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. **CC2 channel is configured as input:** CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

19.6.12 Capture/Compare Register 3（TIMx_CCDAT3）

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT3[15:0]	Capture/Compare 3 value **CC3 channel is configured as output:**

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Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
		CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. **CC3 channel is configured as input:** CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 is only readable. When configured as output mode, register CCDAT3 is readable and writable.

19.6.13 Capture/Compare Register 4（TIMx_CCDAT4）

Offset address: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT4[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CCDAT4[15:0]	Capture/Compare 4 value **CC4 channel is configured as output:** CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. **CC4 channel is configured as input:** CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 is only readable. When configured as output mode, register CCDAT4 is readable and writable.

19.6.14 Prescaler（TIMx_PSC）

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK_CNT} = f_{CK_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

19.6.15 Auto-Reload Register（TIMx_AR）

Offset address: 0x44

Reset value: 0x0000FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register.。See Section 19.5.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

19.6.16 Counter（TIMx_CNT）

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
rw															

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Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CNT[15:0]	Counter value

19.6.17 Channel 1 Filter Register（TIMx_C1FILT）

Offset address: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH[5:0]						Reserved	WSIZE[5:0]						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															
rw															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 65535 division (16 bits).

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		The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations. These bits can be configured to determine the sampling clock division for the sliding filter of channel 1.

19.6.18 Channel 2 Filter Register（TIMx_C2FILT）

Offset address: 0x68

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH[5:0]						Reserved	WSIZE[5:0]						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															
rw															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌈3.2⌉ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable

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15:0	SLIDFPSC [15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 65535 division (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations. These bits can be configured to determine the sampling clock division for the sliding filter of channel 2.

19.6.19 Channel 3 Filter Register（TIMx_C3FILT）

Offset address: 0x6C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				THRESH[5:0]				Reserved	WSIZE[5:0]						FILTEN
				rw					rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															
rw															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌜3.2⌝ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable:

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		0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 65535 division (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations. These bits can be configured to determine the sampling clock division for the sliding filter of channel 3.

19.6.20 Channel 4 Filter Register（TIMx_C4FILT）

Offset address: 0x70

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				THRESH[5:0]				Reserved	WSIZE[5:0]						FILTEN
				rw					rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															
rw															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	THRESH[5:0]	Threshold number of valid logic level samples, maximum 63: the threshold for valid logic levels. Within the sampling window, if the quantity of logic highs is greater than or equal to the threshold, the next logic level will be a logic high. The same rule applies to logic lows. If the quantity of high and low logic levels within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to a value greater than or equal to half of the Window value Recommended threshold range: **Minimum value:** one additional pre-scaler clock period beyond the maximum glitch size limit (pre-scaler clock period), and must be greater than half of the window size. For example, if the glitch size is 3.2 * (the pre-scaler clock period), then the threshold should be ⌜3.2⌝ = 4 + 1 =5 **Maximum value:** the lower limit of the minimum size of the valid signal (in pre-scaler clock periods), and must be less than the window size. For example, if the minimum signal size is 3.2 * (the pre-scaler clock period), then the threshold should be the lower limit (3.2) = 3.
23	Reserved	Reserved, the reset value must be maintained.
22:17	WSIZE[5:0]	Window size value for logic level checking, maximum 63: The window size determines how many sample values will be considered when obtaining the next logic level. The built-in FIFO is 64 bits, with a maximum index of 63, so the window size

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		can only be set to 63.
16	FILTEN	Filter enable: 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Prescaler value for the sliding filter sampling clock: For this filter, it supports a 65535 division (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculations. These bits can be configured to determine the sampling clock division for the sliding filter of channel 4.

19.6.21 Input Channel Filter Output Register（TIMx_FILTO）

Offset address: 0x74

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												C4FILTO	C3FILTO	C2FILTO	C1FILTO
												r	r	r	r

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	C4FILTO	Channel 4 filter output level status 0: Output low level; 1: Output high level;
2	C3FILTO	Channel 3 filter output level status 0: Output low level; 1: Output high level;
1	C2FILTO	Channel 2 filter output level status 0: Output low level; 1: Output high level;
0	C1FILTO	Channel 1 filter output level status 0: Output low level; 1: Output high level;

19.6.22 Input Selection（TIMx_INSEL）

Offset address: 0x78

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	CLRS[3:0]	ITRS[3:0]	ETRS[3:0]
	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TI4S[3:0]				TI3S[3:0]				TI2S[3:0]				TI1S[3:0]			
rw				rw				rw				rw			

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:24	CLRS[3:0]	Selects tim_ocref_clr input signal 0000: tim_ocref_clr0 0001: tim_ocref_clr1 … 1111: tim_ocref_clr15 *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.*
23:20	ITRS[3:0]	Selects tim_itr input signal 0000: tim_itr0 0001: tim_itr1 … 1111: tim_itr15
19:16	ETRS[3:0]	Selects tim_etr input signal 0000: tim_etr0 0001: tim_etr1 … 1111: tim_etr15 *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.*
15:12	TI4S[3:0]	Selects tim_ti4[15:0] input signal 0000: tim_ti4_in0 0001: tim_ti4_in1 … 1111: tim_ti4_in15
11:8	TI3S[3:0]	Selects tim_ti3[15:0] input signal 0000: tim_ti3_in0 0001: tim_ti3_in1 … 1111: tim_ti3_in15
7:4	TI2S[3:0]	Selects tim_ti2[15:0] input signal 0000: tim_ti2_in0 0001: tim_ti2_in1 … 1111: tim_ti2_in15

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3:0	TI1S[3:0]	Selects tim_ti1[15:0] input signal 0000: tim_ti1_in0 0001: tim_ti1_in1 … 1111: tim_ti1_in15

19.6.23 DMAControl Register（TIMx_DCTRL）

Offset address：0x94

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBADDR[5:0]						Reserved		DBLEN[5:0]					
		rw								rw					

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:8	DBADDR[5:0]	DMA base address This Bit Field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of “DMA Base Address + 4” 00000: TIMx_CTRL1, 00001: TIMx_CTRL2, 00010: TIMx_SMCTRL, ... 10001: TIMx_BKDT, 10010: TIMx_DCTRL,
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	DBLEN[5:0]	DMA burst length This Bit Field defines the number DMA will accesses (write/read) TIMx_DADDR register. 000000: 1 time transfer 000001: 2 times transfer 000010: 3 times transfer … 010001: 18 times transfer ..... 100010: 35 times transfer Example: We consider the following transfer: DBLEN=7, DBADDR=TIMx_CTRL1

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Bit field	Name	Description
		If DBLEN=7 and DBADDR=TIMx_CTRL1 represent the address of the data to be transferred, then the address of the transfer is given by the following equation ((Address of TIMx_CTRL1) + DBADDR + (DMA index)), where DMA index = DBLEN. Adding 7 to ((Address of TIMx_CTRL1) + DBADDR) gives the address where data will be written to or read from, resulting in data transfer occurring in 7 registers starting from the address ((Address of TIMx_CTRL1) + DBADDR). If the data is set as half-word (16 bits), then the data will be transferred to all 7 registers If the data is set as bytes, the data will still be transferred to all 7 registers: the first register contains the first MSB byte, the second register contains the first LSB byte, and so on. Therefore, for the timer, the user must specify the data width to be transferred by DMA.

19.6.24 DMA Transfer Buffer Register（TIMx_DADDR）

Offset address: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BURST[31:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[31:0]															
rw															

Bit field	Name	Description
31:0	BURST[31:0]	DMA accessing buffer When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length × 4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4; DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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20 General-Purpose Timers GTIMBx(x=1-3)

20.1 GTIMBx(x=1-3)Introduction

The general-purpose timers (GTIMBx) is mainly used in the following scenarios: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

General timers feature complementary output, dead-time insertion, and break functions. They are suitable for motor control applications.

20.2 Main Features Of GTIMBx(x=1-3)

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- GTIMBx up to 5 channels
- 4 capture/compare channels, working modes: PWM output, ouput compare, one-pulse mode output, input capture
- 1 break input signal with digital filtering support, used to place the timer's output signal in a safe user-selectable configuration.
- The events that generate the interrupt/DMA are as follows：
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break signal input
- Programmable dead-time for complementary outputs
  - For GTIMBx, Channel 1 supports this function
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

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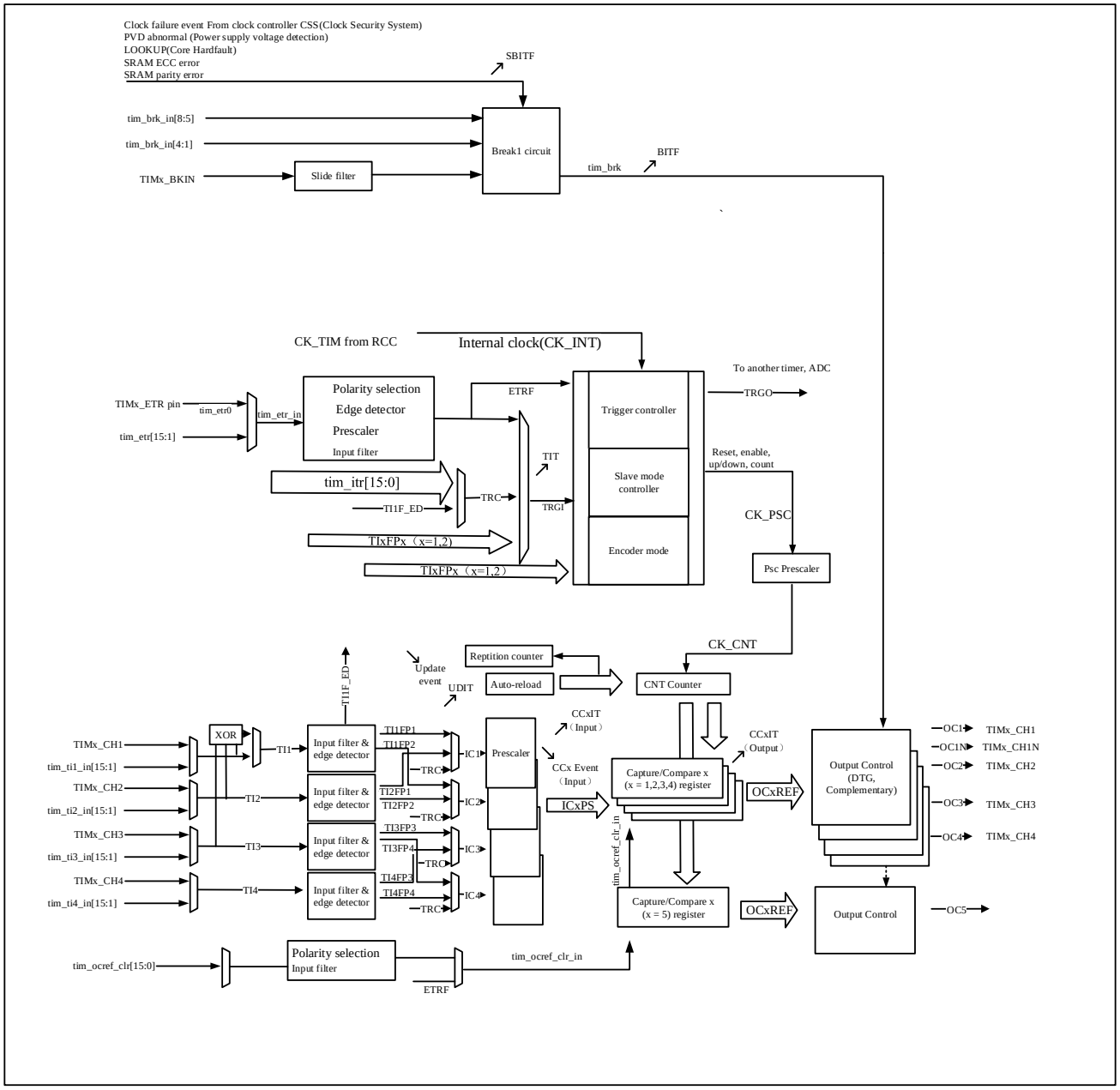
20.3 Block Diagram Of GTIMBx (x=1-3)

Figure 20-1 Block Diagram Of GTIMBx



20.4 Pin and Internal Signals of GTIMBx (x=1-3)

The following table describes the input and output pins and signals of GTIMBx.

Table 20-1 GTIMBx input/output pins

Pins	Type	Description

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TIMx_CH1 TIMx_CH2 TIMx_CH3 TIMx_CH4	Input/Output	Timer multi-purpose channel. Each channel can be used for capture, compare or PWM generation. TIM_CH1 and TIM_CH2 can also be used as external clock (less than 1/4 of the internal clock frequency), external trigger, and quadrature encoder inputs. TIM_CH1, TIM_CH2, and TIM_CH3 can also be used for interfacing with Hall effect sensors.
TIM_CH1N	Output	Timer complementary output channels with dead-time insertion.
TIMx_ETR	Input	External trigger input. This input can serve as an external trigger or external clock source. If a prescaler is used, the input signal TIMx_ETR can be a signal with a frequency higher than the system clock frequency
TIMx_BKIN	Input/Output	Break input. Can be configured as bidirectional mode.

Table 20-2 GTIMBx Internal Input/Output Signal

Internal Signal	**Type**	**Description**
tim_ti1_in[15:0] tim_ti2_in[15:0] tim_ti3_in[15:0] tim_ti4_in[15:0]	Input	Timer channels 1/2/3/4 input signals. The tim_ti1_in[15:0] and tim_ti2_in[15:0] inputs can be used for capture or as an external clock (less than 1/4 of the system clock frequency) and for quadrature encoder signals.
tim_etr[15:0]	Input	External trigger channel input signals. These inputs can be used as triggers, external clocks, or for hardware per-cycle pulse width control. If a prescaler is used, the input signal TIMx_ETR can be a signal with a frequency higher than the system clock frequency.
tim_itr[15:0]	Input	Internal trigger input signals. These inputs can be used in mode controllers or as input clocks (less than 1/4 of the system clock frequency).
tim_trgo	Output	Internal trigger signal output. These trigger signals can be used by other timers and/or other peripheral devices.

20.4.1 Interconnect of the tim_ti1/ tim_ti2/ tim_ti3/ tim_ti4 Input

Table 20-3 Source of input signal tim_ti1

tim_ti1 inputs	**Signal Source**

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	GTIMB1	GTIMB2	GTIMB3
tim_ti1_in0	GTIMB1_CH1	GTIMB2_CH1	GTIMB3_CH1
tim_ti1_in1	COMP1_OUT	LSI	COMP1_OUT
tim_ti1_in2	COMP2_OUT	LSE_CSS _OUT	COMP2_OUT
tim_ti1_in3	COMP3_OUT	RTC_ WAKEUP	COMP3_OUT
tim_ti1_in4	COMP4_OUT	COMP1_OUT	COMP4_OUT
tim_ti1_in5	Reserved	COMP2_OUT	Reserved
tim_ti1_in6	Reserved	COMP3_OUT	Reserved
tim_ti1_in7	Reserved	COMP4_OUT	Reserved
tim_ti1_in[15:8]	Reserved		

Table 20-4 Source of input signal tim_ti2

tim_ti2 inputs	Signal Source		
	GTIMB1	GTIMB2	GTIMB3
tim_ti2_in0	GTIMB1_CH2	GTIMB2_CH2	GTIMB3_CH2
tim_ti2_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti2_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti2_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti2_in4	GTIMA7_OC3	GTIMA7_OC4	GTIMA7_OC3
tim_ti2_in[15:5]	Reserved		

Table 20-5 Source of input signal tim_ti3

tim_ti3 inputs	Signal Source

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	GTIMB1	GTIMB2	GTIMB3
tim_ti3_in0	GTIMB1_CH3	GTIMB2_CH3	GTIMB3_CH3
tim_ti3_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti3_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti3_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti3_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti3_in[15:5]	Reserved		

Table 20-6 Source of input signal tim_ti4

tim_ti4 inputs	Signal Source		
	GTIMB1	GTIMB2	GTIMB3
tim_ti4_in0	GTIMB1_CH4	GTIMB2_CH4	GTIMB3_CH4
tim_ti4_in1	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_ti4_in2	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ti4_in3	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ti4_in4	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ti4_in[15:5]	Reserved		

20.4.2 Interconnect of the tim_itr Input

Table 20-7 Source of input signal tim_itr

GTIMBx	GTIMB1	GTIMB2	GTIMB3
tim_itr0	ATIM1_ TRGO	ATIM1_ TRGO	ATIM1_ TRGO
tim_itr1	GTIMA1_ TRGO	GTIMA1_ TRGO	GTIMA1_ TRGO

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tim_itr2	GTIMA2_ TRGO	GTIMA2_ TRGO	GTIMA2_ TRGO
tim_itr3	GTIMA3_ TRGO	GTIMA3_ TRGO	GTIMA3_ TRGO
tim_itr4	GTIMA4_ TRGO	GTIMA4_ TRGO	GTIMA4_ TRGO
tim_itr5	ATIM2_ TRGO	ATIM2_ TRGO	ATIM2_ TRGO
tim_itr6	GTIMA5_ TRGO	GTIMA5_ TRGO	GTIMA5_ TRGO
tim_itr7	ATIM3_ TRGO	ATIM3_ TRGO	ATIM3_ TRGO
tim_itr8	GTIMA6_ TRGO	GTIMA6_ TRGO	GTIMA6_ TRGO
tim_itr9	GTIMA7_ TRGO	GTIMA7_ TRGO	GTIMA7_ TRGO
tim_itr10	ATIM4_ TRGO	ATIM4_ TRGO	ATIM4_ TRGO
tim_itr11	Reserve	GTIMB1_ TRGO	GTIMB1_ TRGO
tim_itr12	GTIMB2_ TRGO	Reserve	GTIMB2_ TRGO
tim_itr13	GTIMB3_ TRGO	GTIMB3_ TRGO	Reserve
tim_itr14	SHRTIM1_ OUT_ SYNC2	SHRTIM1_ OUT_ SYNC2	SHRTIM1_ OUT_ SYNC2

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tim_itr15	ETH1_PPS _OUT	ETH1_PPS _OUT	Reserve

20.4.3 Interconnect of the tim_etr Input

Table 20-8 Source of input signal tim_etr

GTIMBx	**GTIMB1**	**GTIMB2**	**GTIMB3**
tim_etr0	GTIMB1_ETR	GTIMB2_ETR	GTIMB3_ETR
tim_etr1	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_etr2	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_etr3	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_etr4	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_etr5	ADC1_ AWD1	ADC1_ AWD1	ADC1_ AWD1
tim_etr6	ADC1_ AWD2	ADC1_ AWD2	ADC1_ AWD2
tim_etr7	GTIMB2_ ETR	GTIMB1_ ETR	GTIMB1_ ETR
tim_etr8	ADC2_ AWD1	ADC2_ AWD1	ADC2_ AWD1
tim_etr9	ADC2_ AWD2	ADC2_ AWD2	ADC2_ AWD2
tim_etr10	GTIMB3_ ETR	GTIMB3_ ETR	GTIMB2_ ETR
tim_etr11	ADC3_ AWD1	ADC3_ AWD1	ADC3_ AWD1

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tim_etr12	ADC3_ AWD2	ADC3_ AWD2	ADC3_ AWD2
tim_etr13	GTIMA1_ ETR	GTIMA2_ ETR	GTIMA3_ ETR
tim_etr_in[15:14]	Reserved		

20.4.4 Interconnect of the Break 1 Input

Table 20-9 Break 1 input signal source of GTIMBx

tim_brk input	**GTIMB1**	**GTIMB2**	**GTIMB3**
TIM_BKIN	GTIMB1_BKIN pin	GTIMB2_BKIN pin	GTIMB3_BKIN pin
tim_brk_cmp1	COMP1_OUT	COMP1_OUT	COMP1_OUT
tim_brk_cmp2	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_brk_cmp3	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_brk_cmp4	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_brk_cmp5	DSMU_BRK[0]	Reserved	Reserved
tim_brk_cmp6	Reserved	DSMU_BRK[1]	Reserved
tim_brk_cmp7	Reserved	Reserved	DSMU_BRK[2]
tim_brk_ cmp8	Reserved		

20.4.5 Interconnect of the tim_ocref_clr Input

Table 20-10 tim_ocref_clr input signal source of GTIMBx

OCREF clear signal	GTIMBx **OCREF clear signal assignment**		
	GTIMB1	**GTIMB2**	**GTIMB3**
tim_ocref_clr0	COMP1_OUT	COMP1_OUT	COMP1_OUT

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tim_ocref_clr1	COMP2_OUT	COMP2_OUT	COMP2_OUT
tim_ocref_clr2	COMP3_OUT	COMP3_OUT	COMP3_OUT
tim_ocref_clr3	COMP4_OUT	COMP4_OUT	COMP4_OUT
tim_ocref_in[15:4]	Reserved		

20.5 GTIMBx (x=1-3) Description

20.5.1 Time-Base Unit

The time-base unit mainly includes: prescaler, counter, auto-reload register and repetition counter. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software set TIMx_EVTGEN.UDGN when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

20.5.1.1 Prescaler Description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

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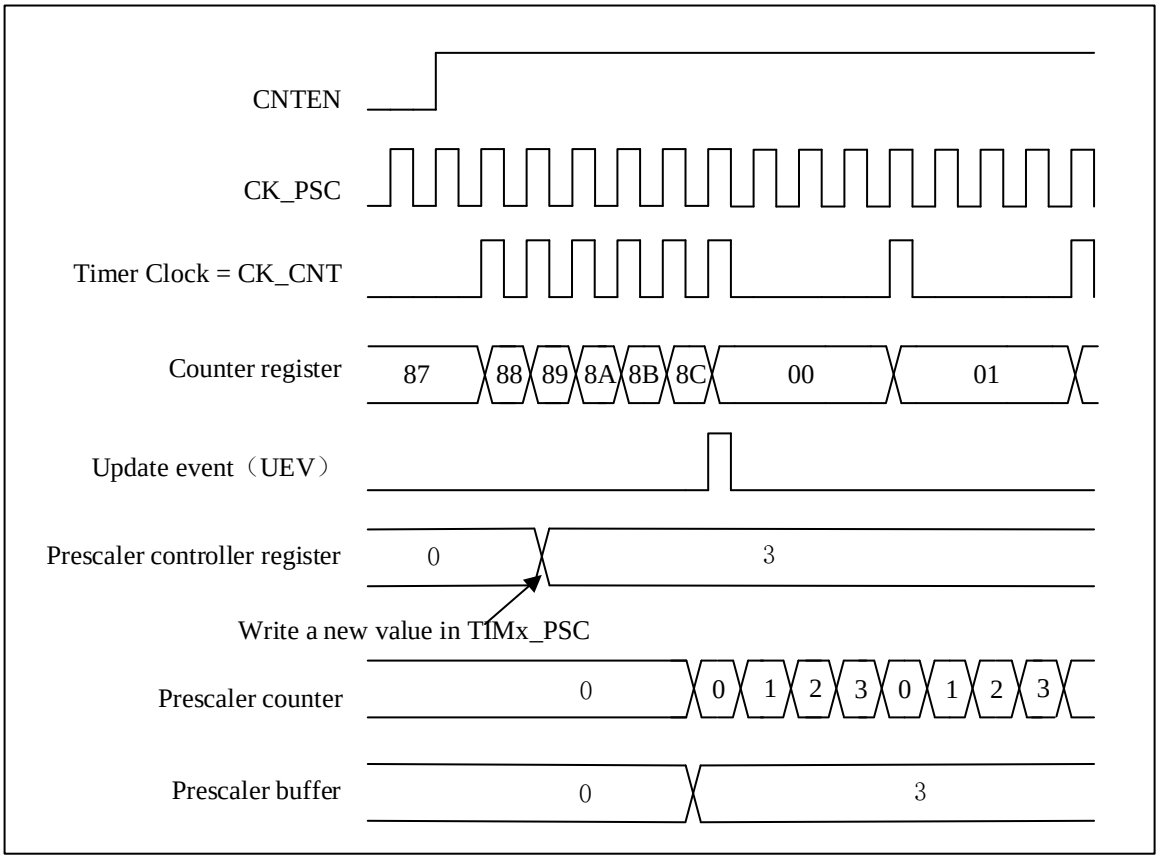
Figure 20-2 Counter Timing Diagram With Prescaler Division Change From 1 To 4



20.5.2 Counter Mode

20.5.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

- The repetition counter is reloaded with the content of TIMx_REPCNT.
- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC)

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the

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prescaler value will remain unchanged)。

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode

Figure 20-3 Timing Diagram Of Up-Counting. The Internal Clock Divider Factor = 2/N

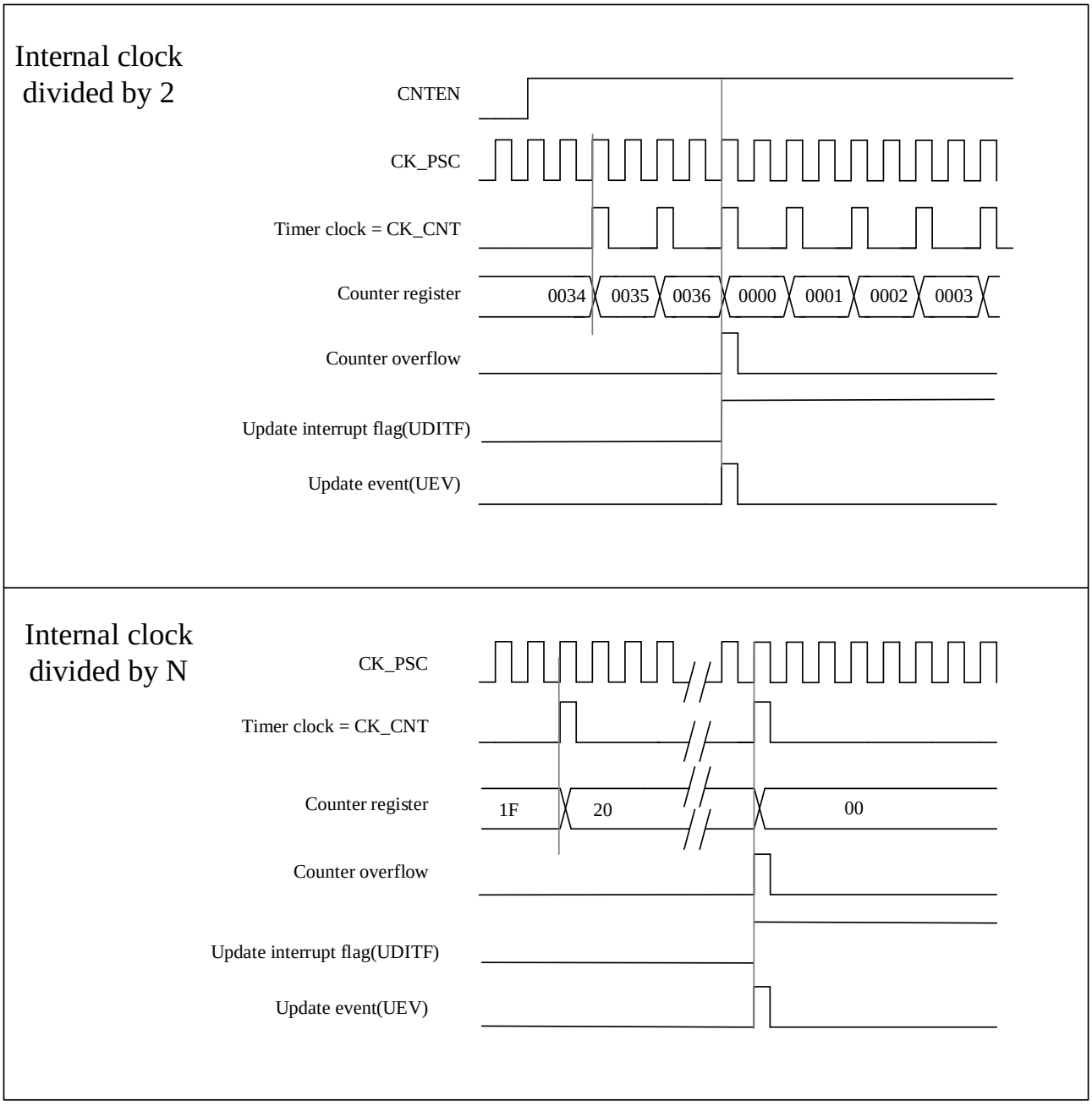

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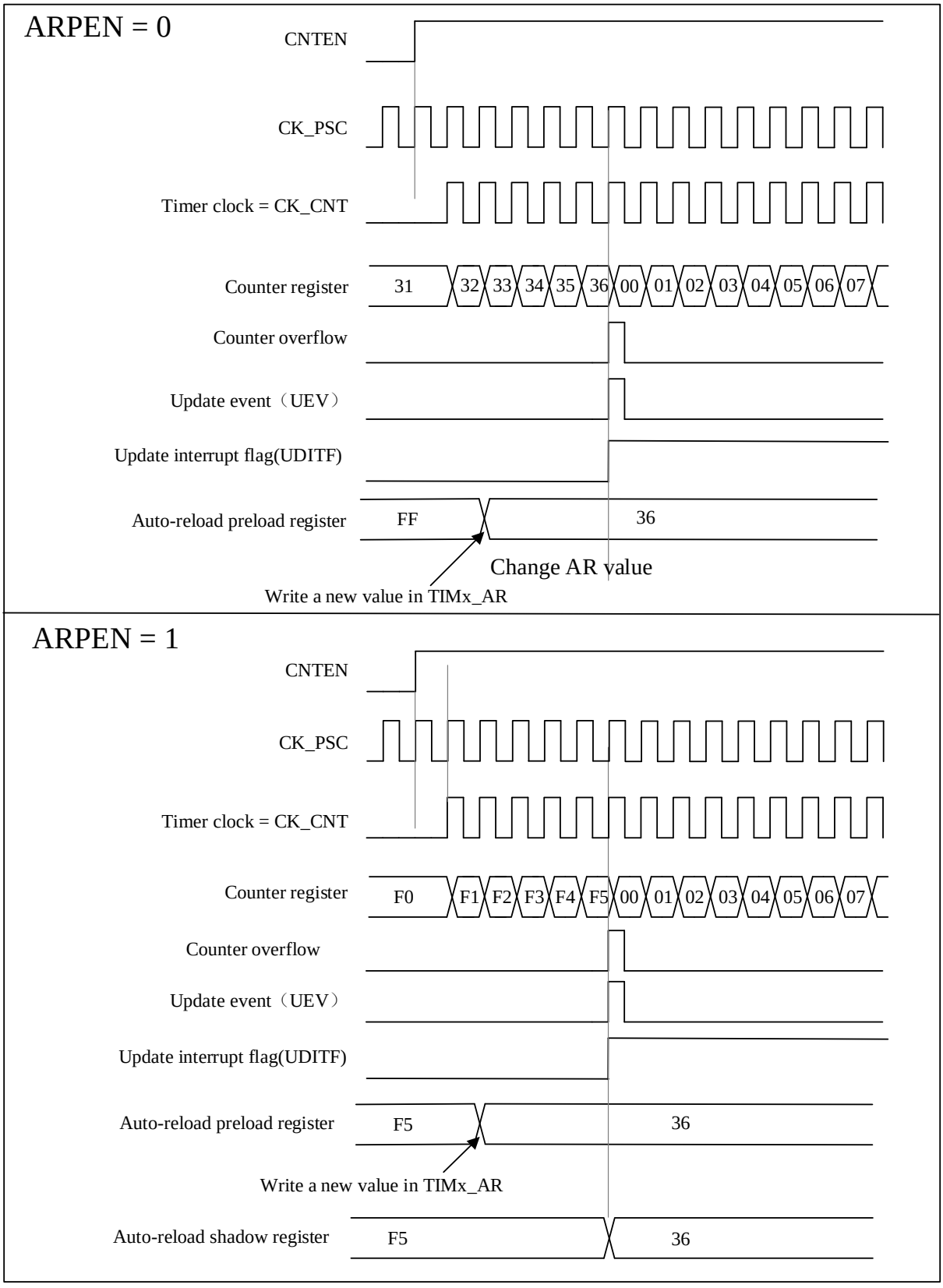
Figure 20-4 Timing Diagram Of The Up-Counting, Update Event When ARPEN=0/1



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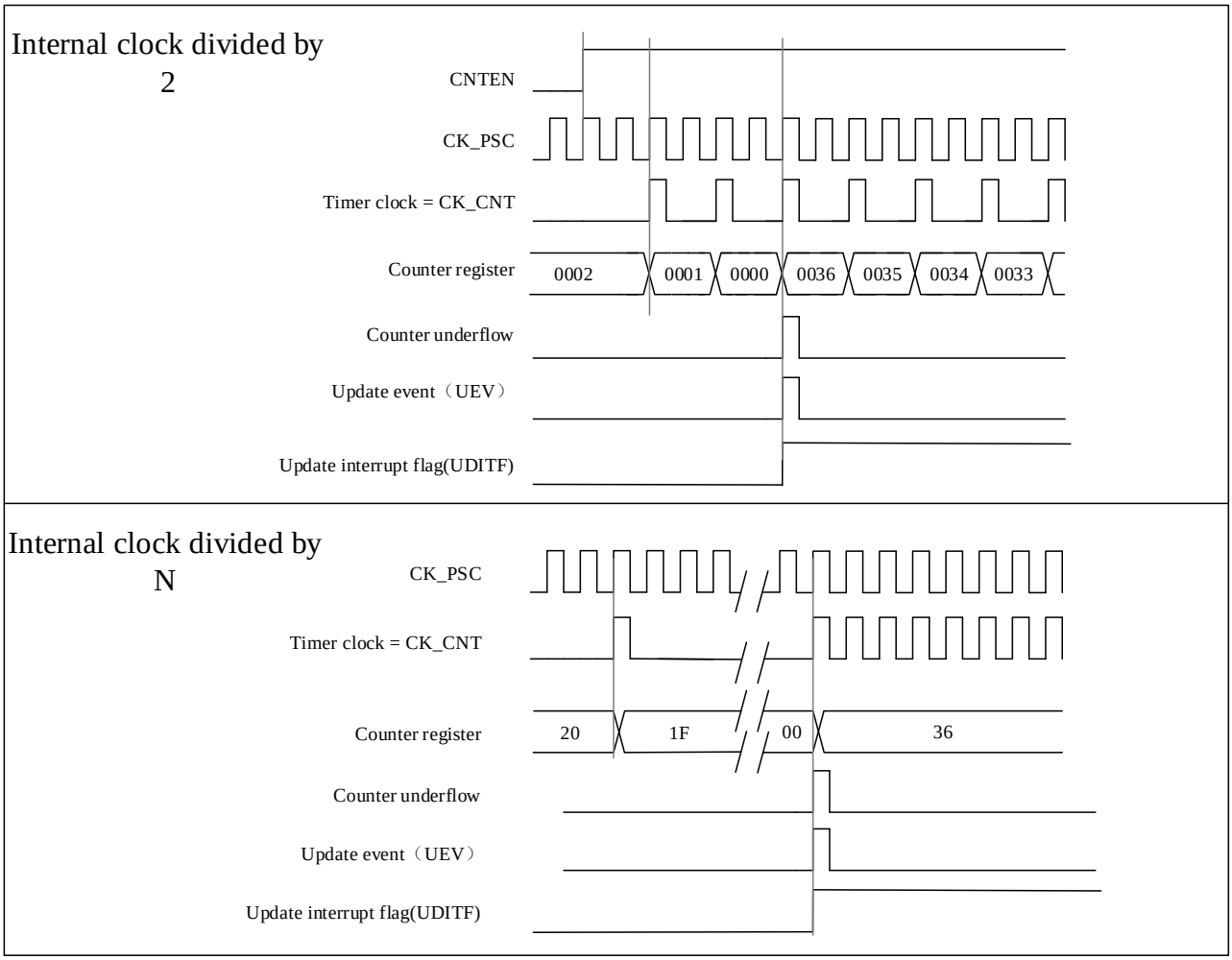
20.5.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see Section20.5.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 20-5 Timing Diagram Of The Down-Counting, Internal Clock Divided Factor = 2/N



20.5.2.3 Center-aligned mode

20.5.2.3.1 Center-aligned symmetric mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again。

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00"。

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The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Note: if the update source is a counter overflow, auto-reload update before reloading the counter。

Figure 20-6 Timing Diagram Of The Center-Aligned, Internal Clock Divided Factor =2/N

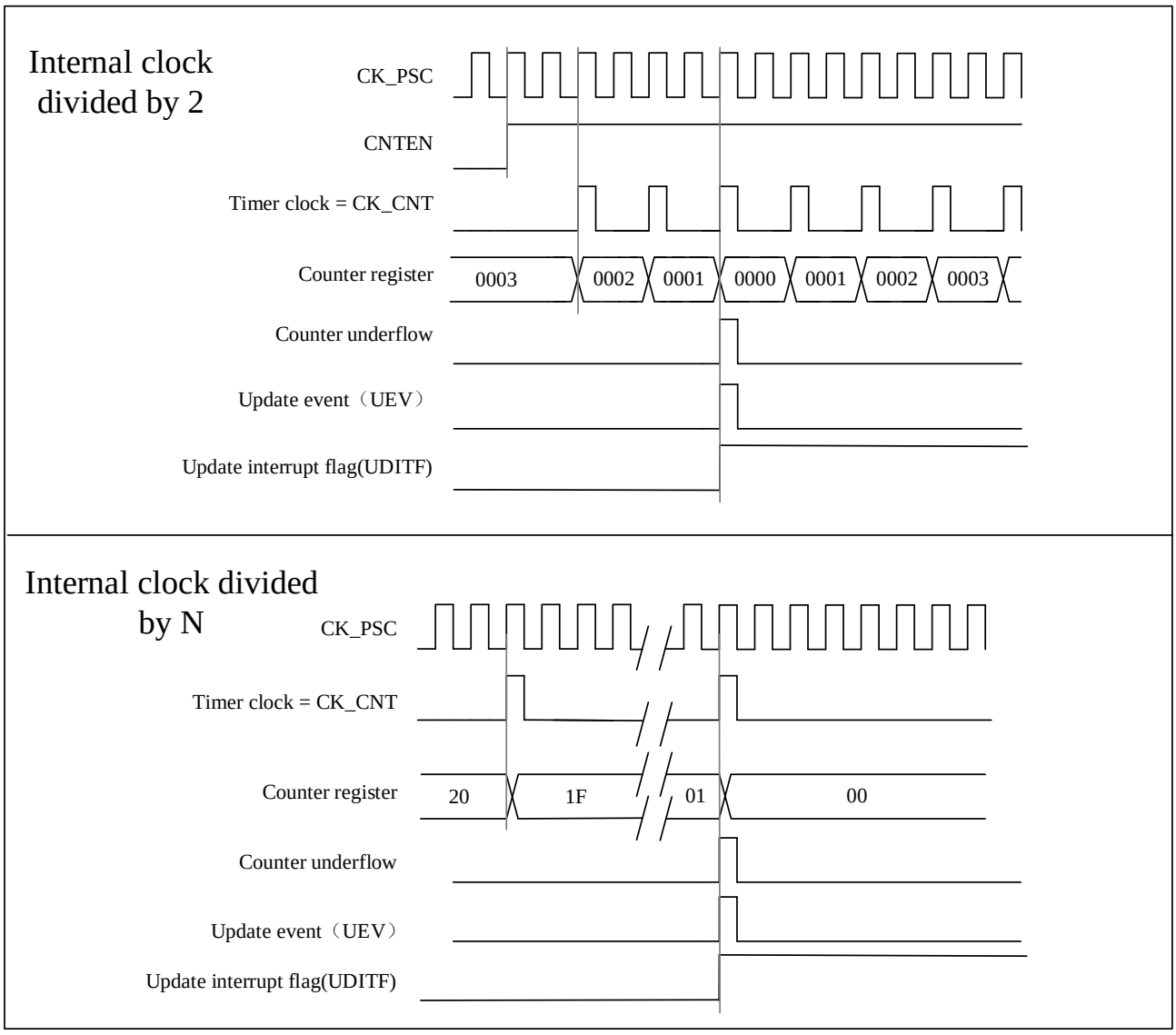

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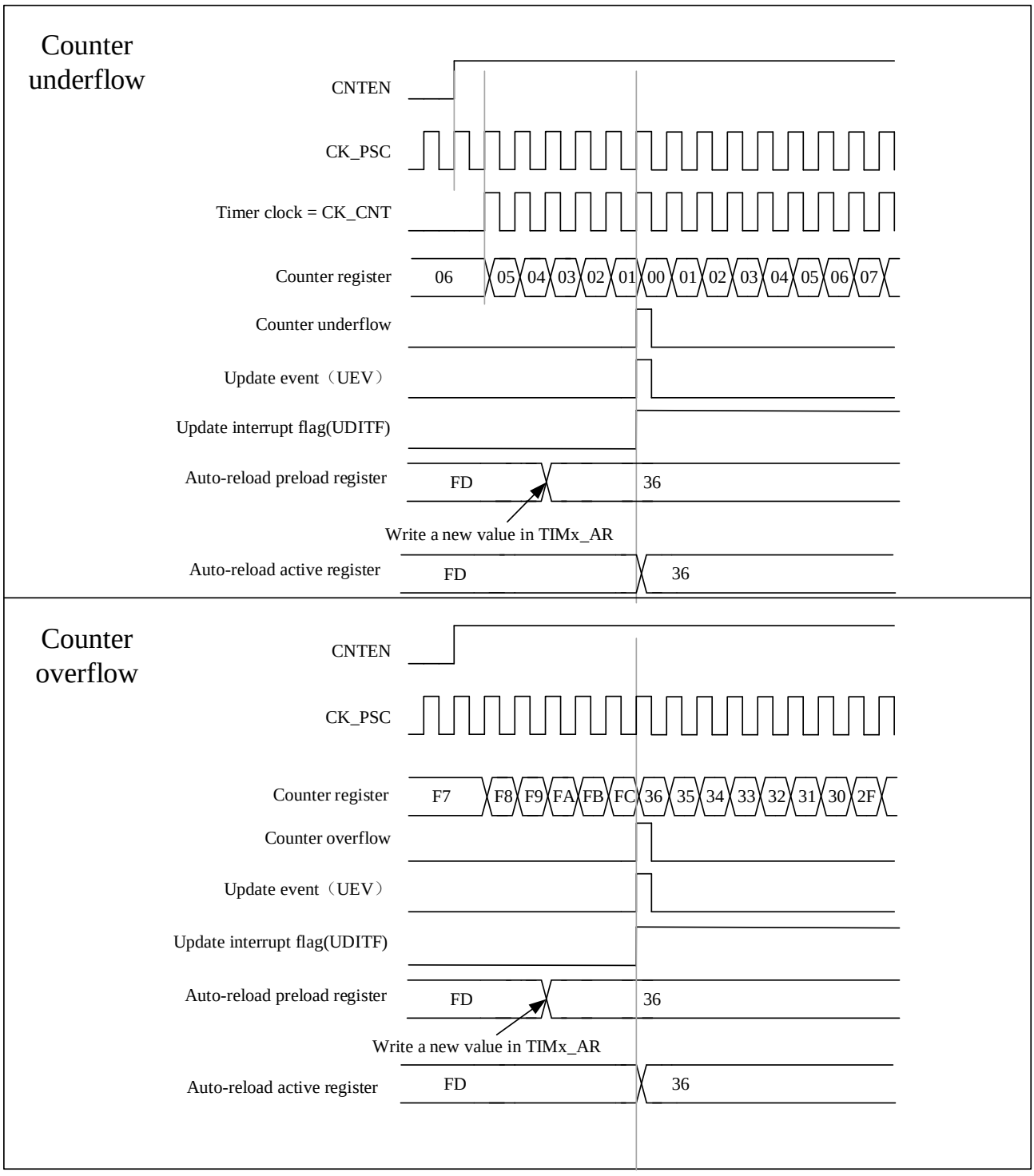
Figure 20-7 A Center-Aligned Sequence Diagram That Includes Counter Overflows And Underflows (ARPEN = 1)



20.5.2.3.2 Central Aligned Asymmetric Mode

In the central aligned asymmetric mode (TIMx_CTRL1. ASYMMETRIC is 1, TIMx_CTRL1.CAMSEL[1:0] is non-zero), the counter counts from 0 to the auto-reload value (TIMx_AR) - 1, generates a counter overflow event, then counts from the auto-reload value to 1, and generates a counter underflow event, then restarts counting from 0

The value of TIMx_CTRL1.DIR cannot be written in this mode; it is updated by hardware and specifies the current

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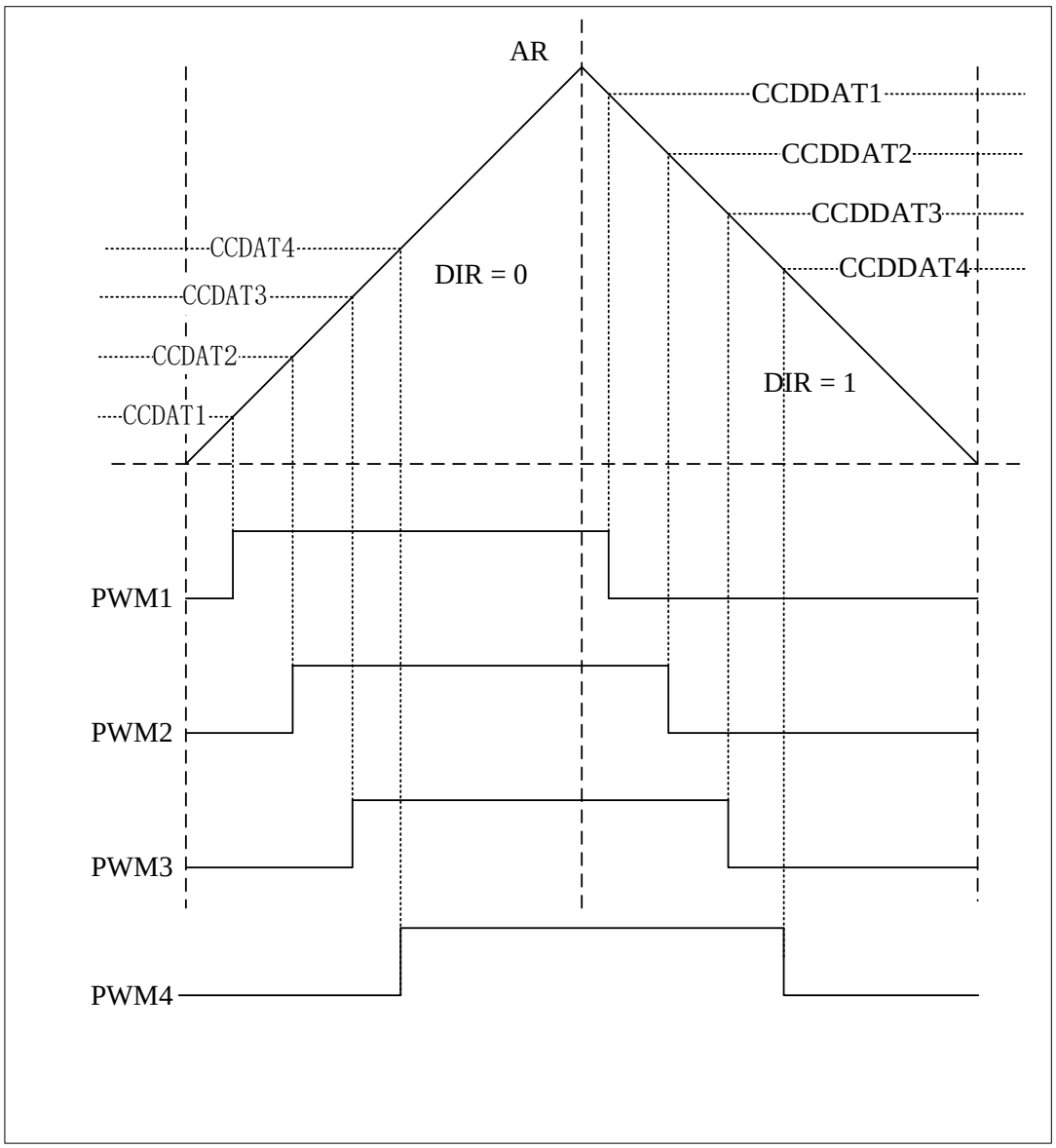
counting direction.

When the channel is not 1, 2, 3, or 4, the comparison value is CCDATx. When the dead-time generator is enabled, please note that when DIR=0, the dead-time insertion point is when the counter value is equal to CCDATx (x=1,2,3,4), and when DIR=1, the dead-time insertion point is when the counter value is equal to CCDDATx (x=1,2,3,4).

An update event occurs each time there is a counter overflow or underflow. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN.UDGN bit (either through software or by using the mode controller). In this case, the counter restarts counting from 0, and the prescaler counter also restarts counting from 0.

Note: If an update is generated due to a counter overflow, the auto-reload will be updated before the counter is reloaded.

Figure 20-8 Asymmetric mode corresponds to the output waveform



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20.5.3 Repetition Counter

The basic unit of Section 20.5.1 describes the conditions for generating Update Events (UEV). Update Events (UEV) are actually generated only when the repetition counter reaches zero, which is very useful for generating PWM signals

This means that every time the N+1 counter overflows or underflows, data is transferred from the preload register to the shadow register, where N is the value in TIMx_REPCNT.

Decrementing repetition counter:

- In up-count mode, overflow occurs each time the counter reaches its maximum value.
- In down-count mode, underflow occurs each time the counter reaches its minimum value.
- In center-aligned mode, the repetition rate is determined by the value of the TIMx_REPCNT register each time the counter overflows or underflow.

The repetition counter has an automatic reload function. Regardless of the value of the repetition counter, the update event (triggered by setting TIMx_EVTGEN.UDGN in the mode controller or generated by hardware) occurs immediately.

Figure 20-9 Timing diagram of the repetition counter in down-count mode

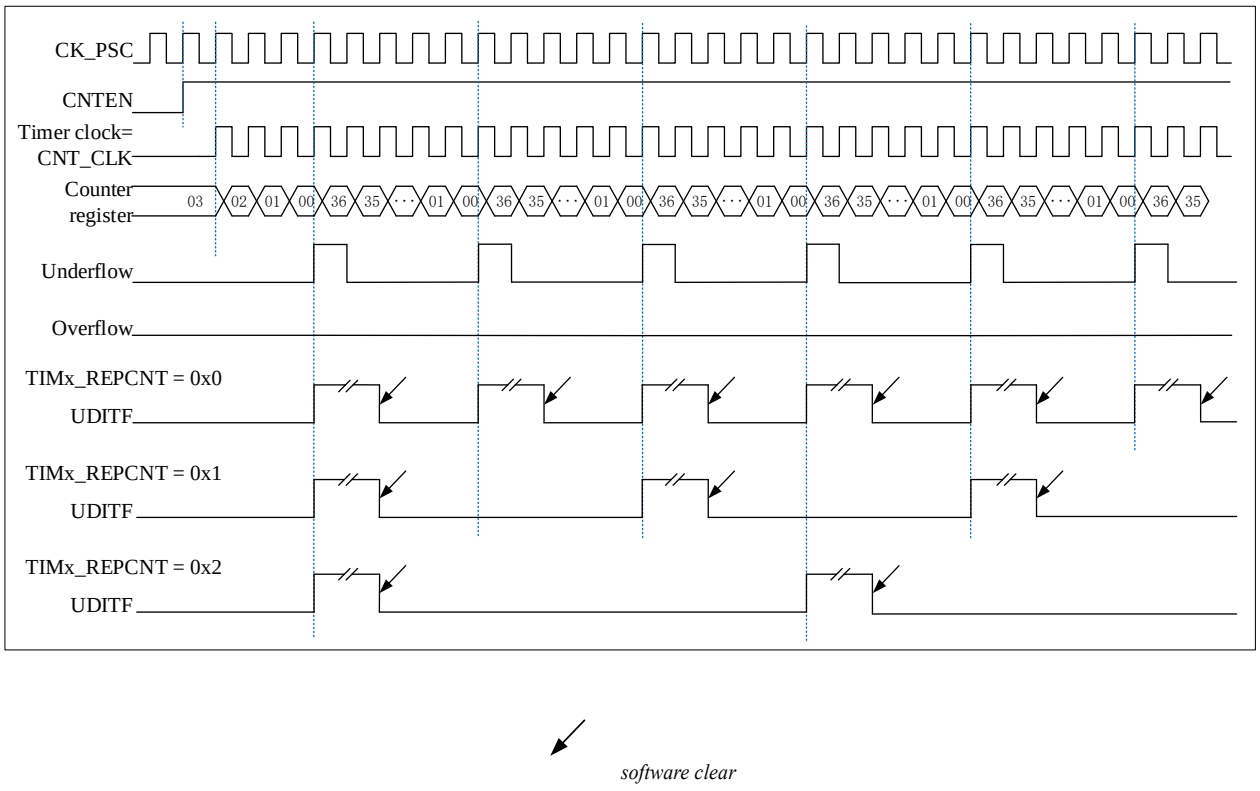

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Figure 20-10 Timing diagram of the repetition counter in up-count mode

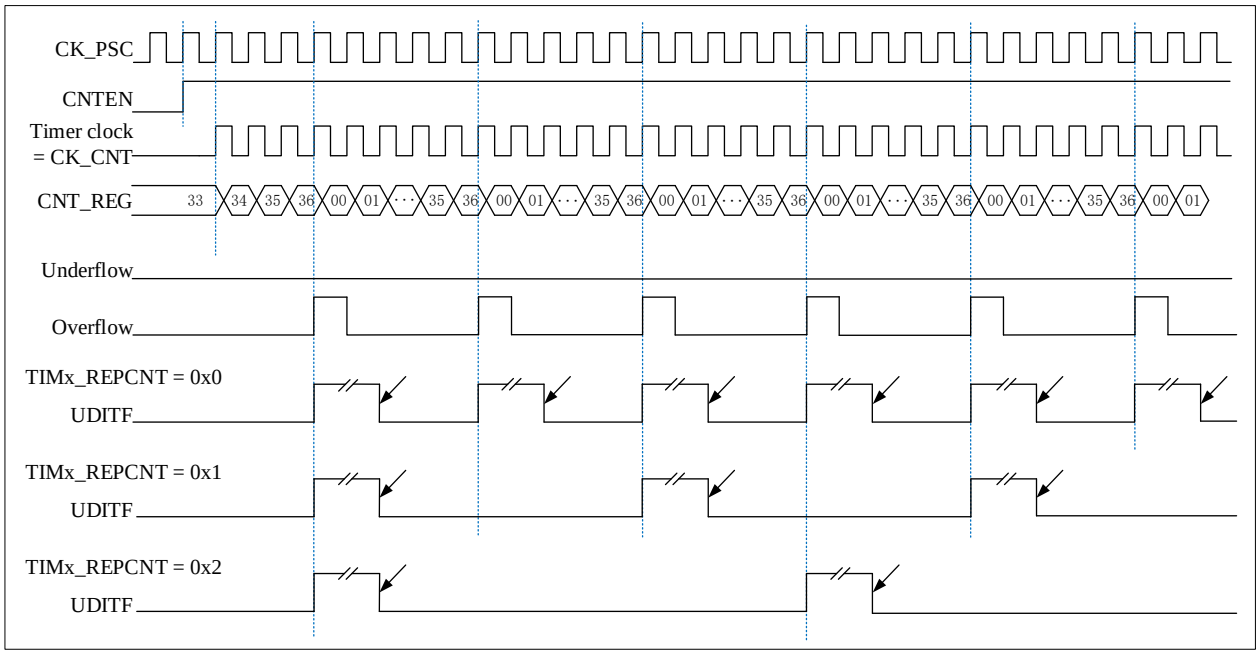
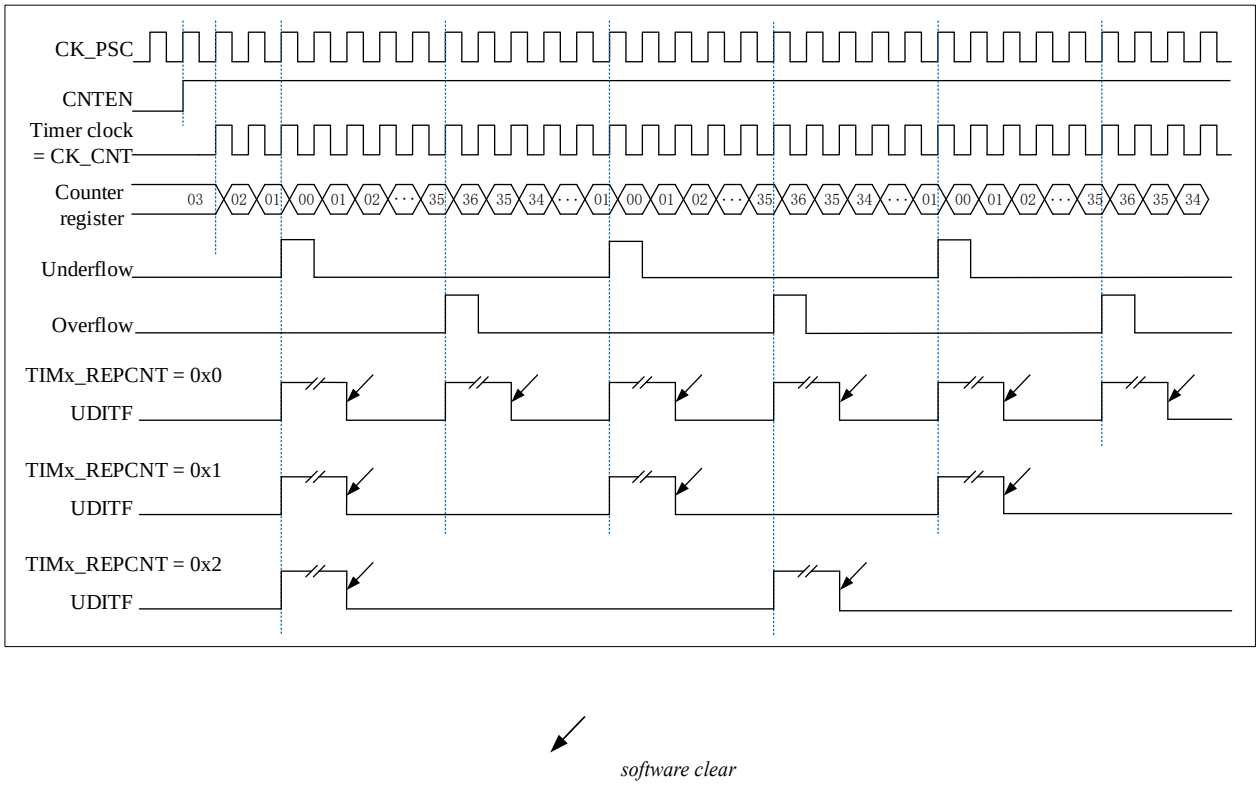


Figure 20-11 Timing diagram of the repetition counter in center-aligned mode



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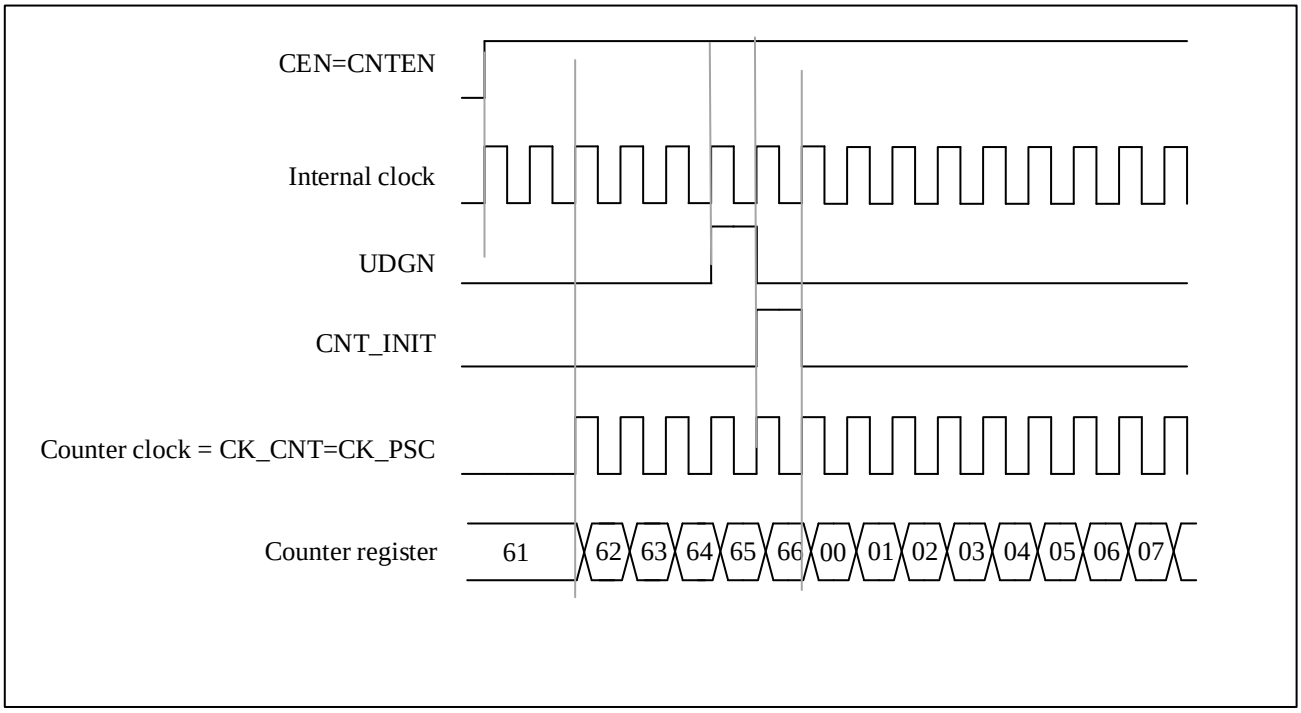
20.5.4 Clock Selection

- The internal clock of timers: CK_INT
- Two kinds of external clcock mode:
  - external input pin.
  - external trigger input ETR.
- Internal trigger input(ITRx): one timer is used as a prescaler for another timer.

20.5.4.1 Internal Clock Source(CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “0000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 20-12 Control Circuit In Normal Mode, Internal Clock Divided By 1



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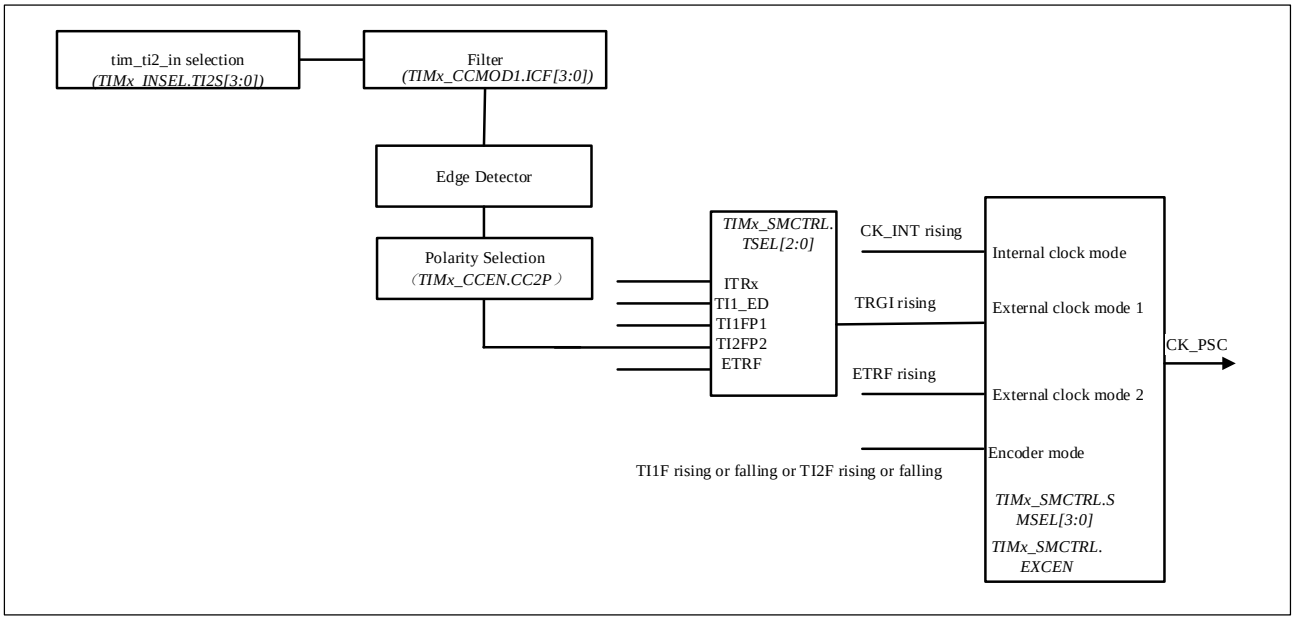
20.5.4.2 External clock source mode 1

Figure 20-13 TI2 External Clock Connection Example



This mode is selected by configuring TIMx_SMCTRL.SMSEL='0111'. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows：

- Configure TIMx_CCMOD1.CC2SEL equal to '01', CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to '0', select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000')
- Configure TIMx_SMCTRL.SMSEL equal to '0111', select timer external clock mode 1
- Configure TIMx_INSEL.TI2S[3:0] to '0000', select TIM_CH2 as the TI2 input
- Configure TIMx_SMCTRL.TSEL equal to '110', select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to '1' to start the counter

Note: The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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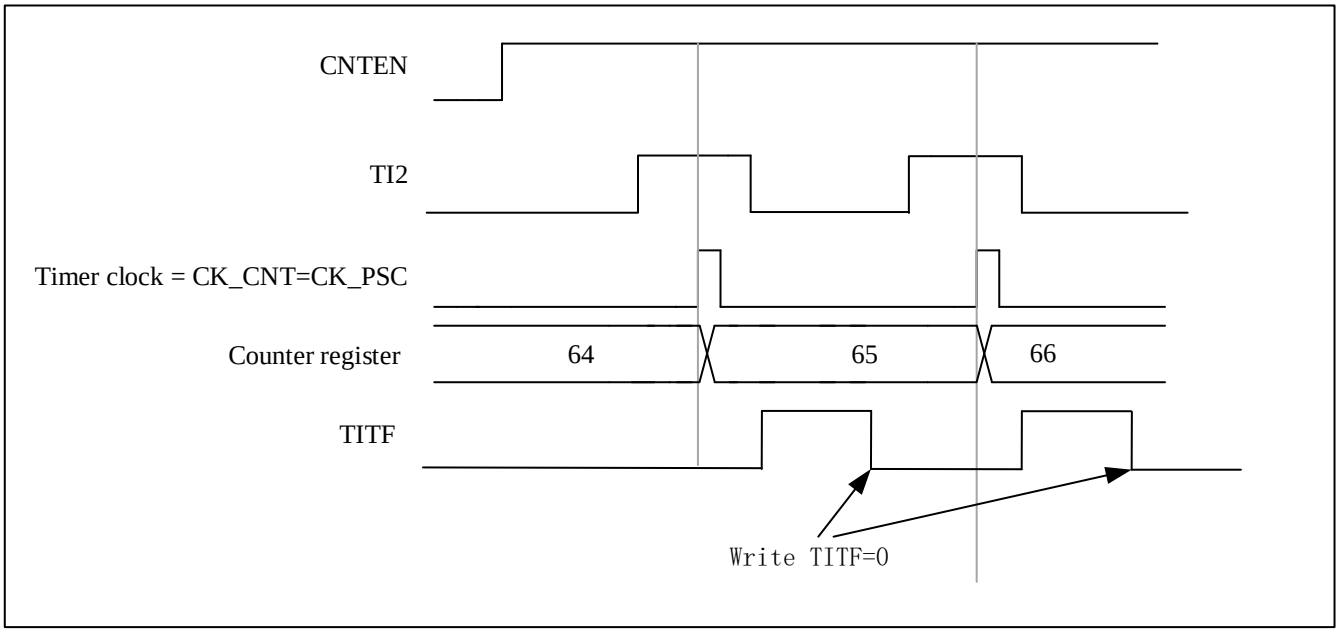
Figure 20-14 Control Circuit In External Clock Mode 1

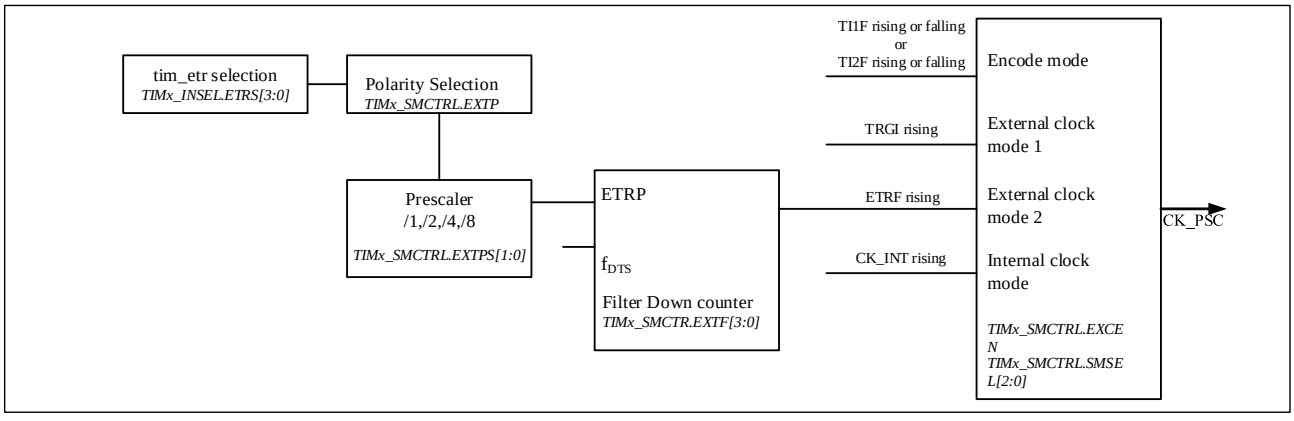


20.5.4.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 20-15 External Trigger Input Block Diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR。

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by setting TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

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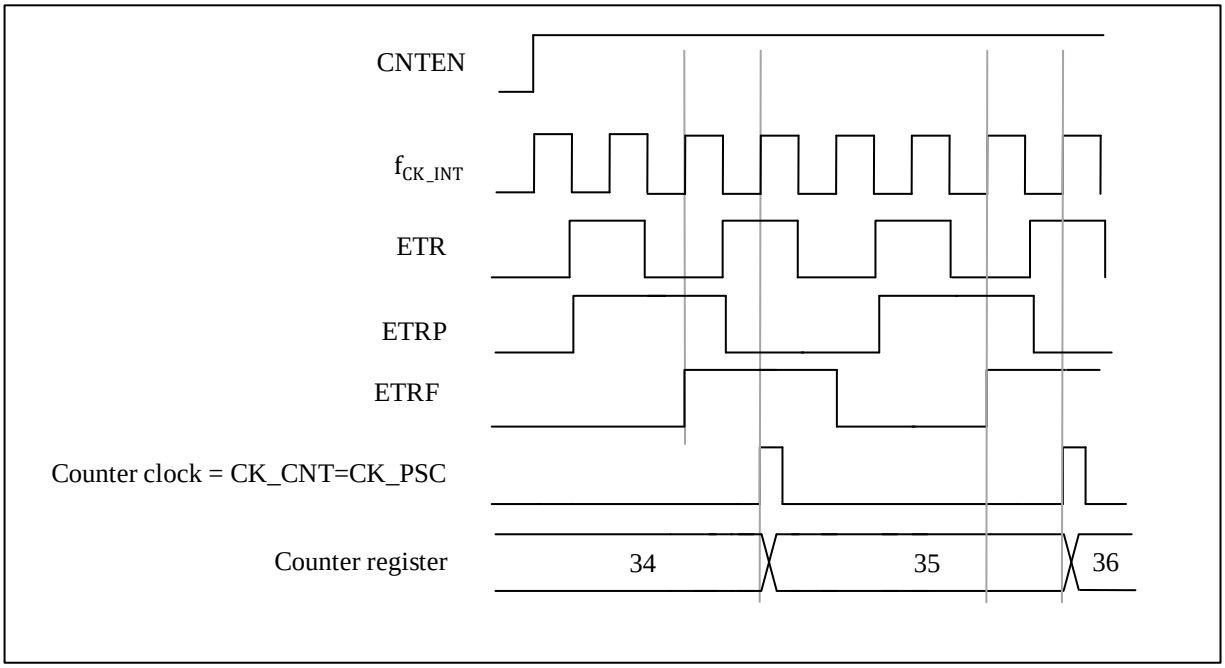
The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 20-16 Control Circuit In External Clock Mode 2



20.5.5 Capture/Compare Channels

Capture/compare channels include capture/compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls。

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after prescale. The following figure shows a block diagram of a capture/compare channel.

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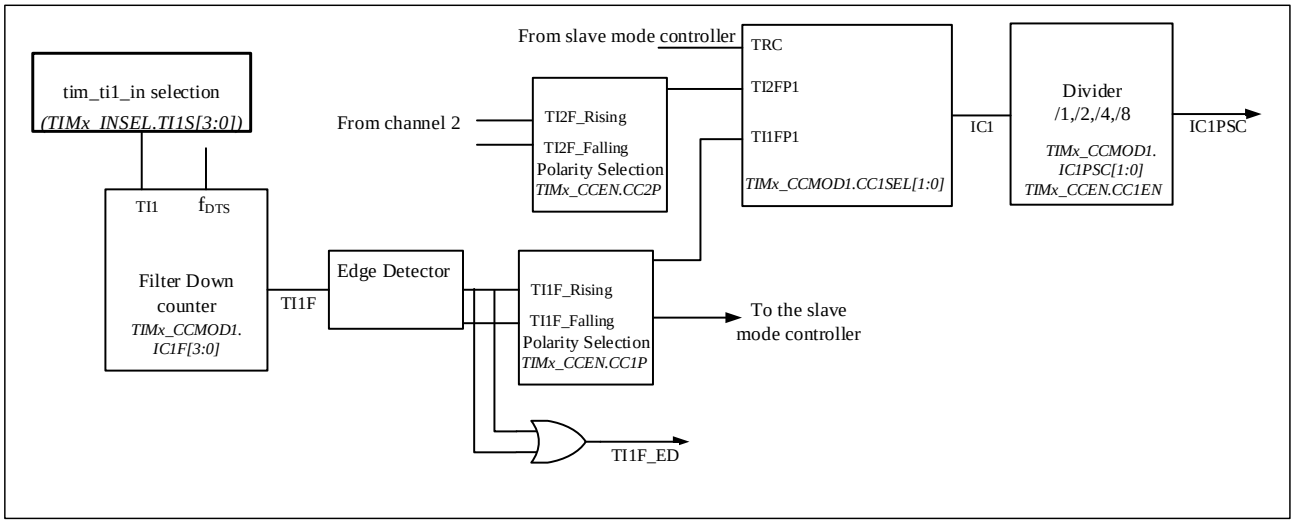
Figure 20-17 Capture/Compare Channel (Example: Channel 1 Input Stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain。

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Figure 20-18 Capture/Compare Channel 1 Main Circuit

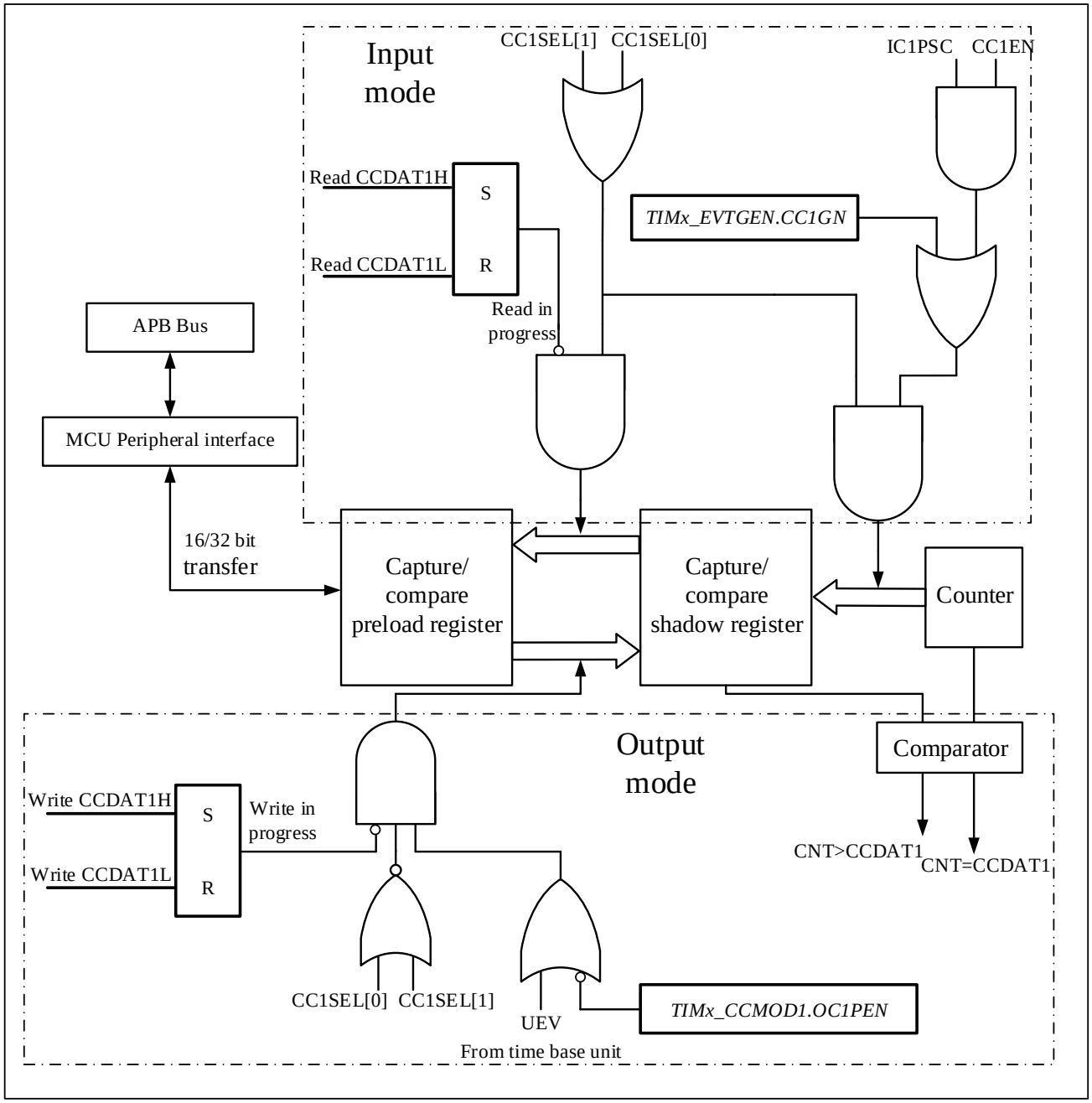

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Figure 20-19 Output Part Of Channelx (x= 1; Take Channel 1 As An Example)

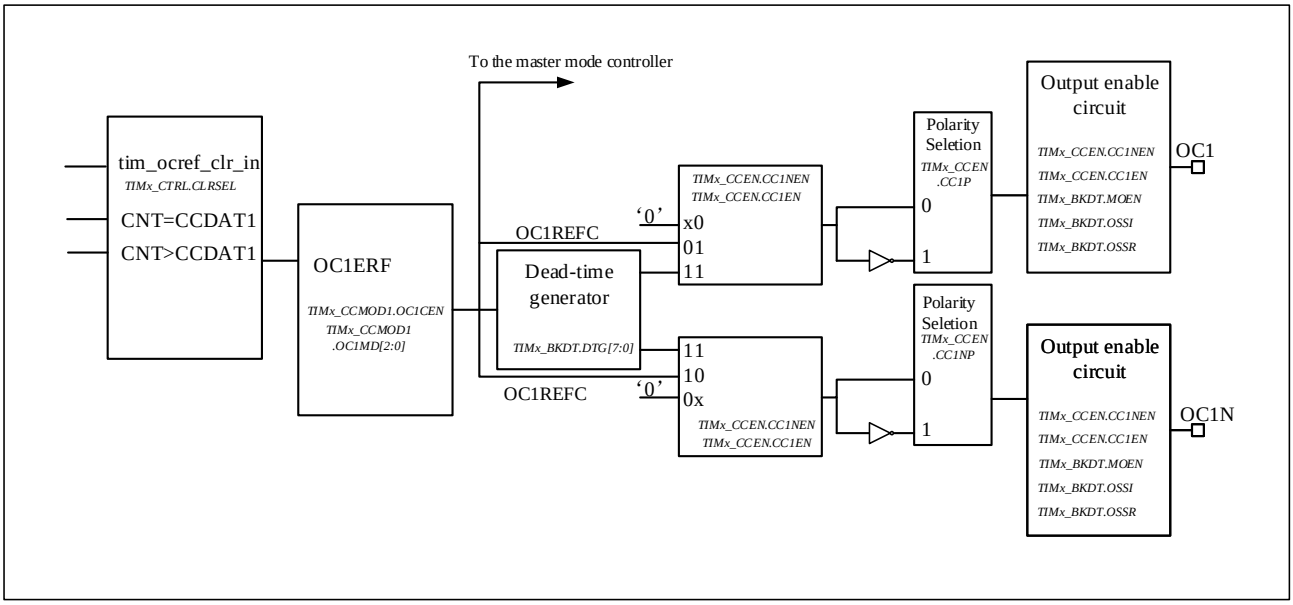
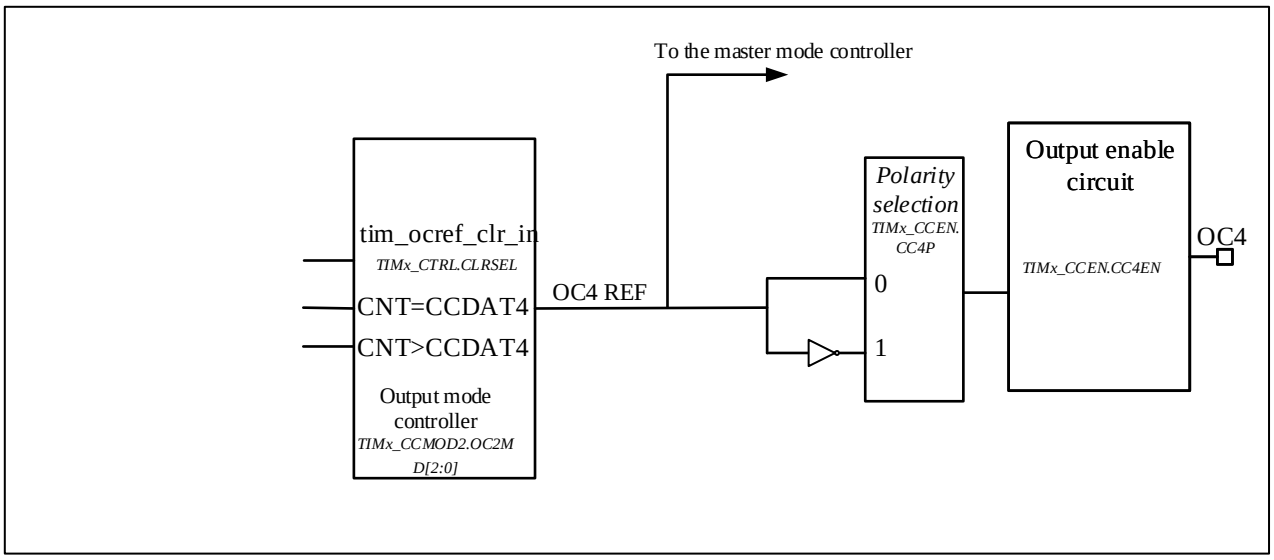


Figure 20-20 Output Part Of Channelx （X = 1,2,3,4;Take Channel 4 As An Example）



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

20.5.6 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

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There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS.CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register。

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- The duration of the input filter required for programming:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1.IC1F to '0011'.

- By configuring TIMx_CCEN.CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC='00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN.CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configure TIMx_DINTEN.CC1IEN=1.

20.5.7 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01', select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), active

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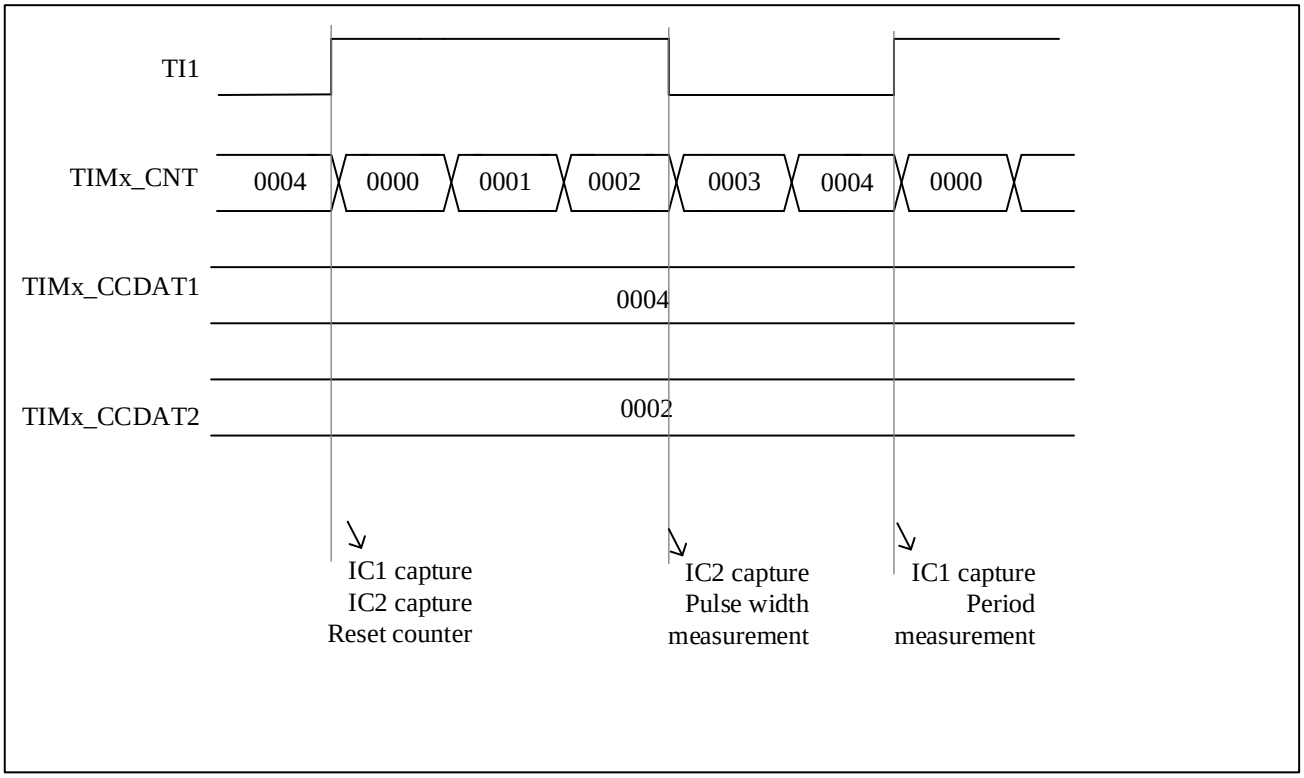
at the rising edge.

- Configure TIMx_CCMOD1.CC2SEL equal to ‘10’, select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), active at the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=‘0100’ to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

Figure 20-21 PWM Input Mode Timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

20.5.8 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=‘00’).

User can set TIMx_CCMODx. OCxMD=‘101’ to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=‘100’ to force the output compare signal to inactive level, the OCxREF will be forced low.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on

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OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

20.5.9 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow：

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD='000', the output pin will keep its level;if set TIMx_CCMODx.OCxMD='001', the output pin will be set active;if set TIMx_CCMODx.OCxMD='010', the output pin will be set inactive;if set TIMx_CCMODx.OCxMD='011', the output pin will be set to toggle.
- Set TIMx_STS.CCxITF
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers(TIMx_CCDATx) or not.

The time resolution is one counting period of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse.

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with required data
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc
- At last, set TIMx_CTRL1.CNTEN to enable the counter

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event。

Here is an example：

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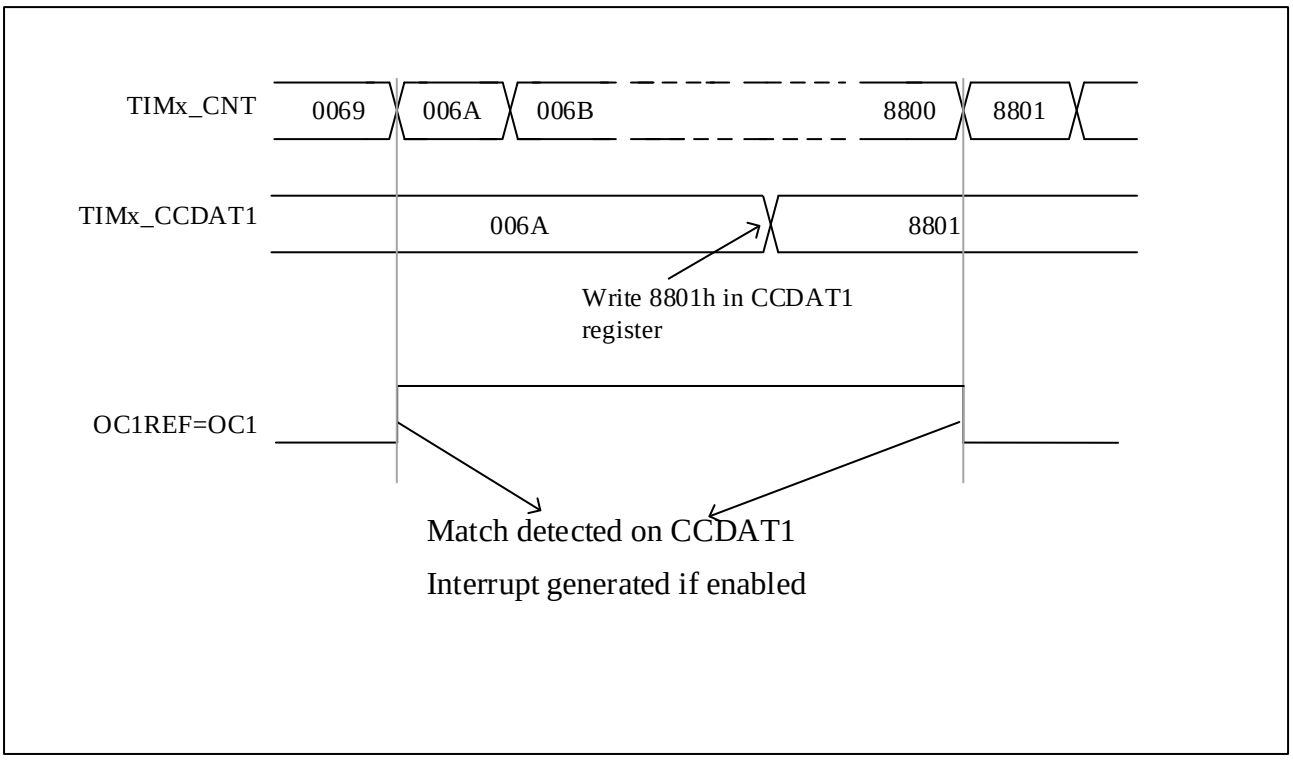
Figure 20-22 Output Compare Mode, Toggle On OC1



20.5.10 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD='110' or setting TIMx_CCMODx. OCxMD='111'. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. To enable the output of OCx, user need to set the combination of the value of CCxEN,CCxNEN,MOEN,OSSI and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

20.5.10.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal '01', '10' or '11', the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

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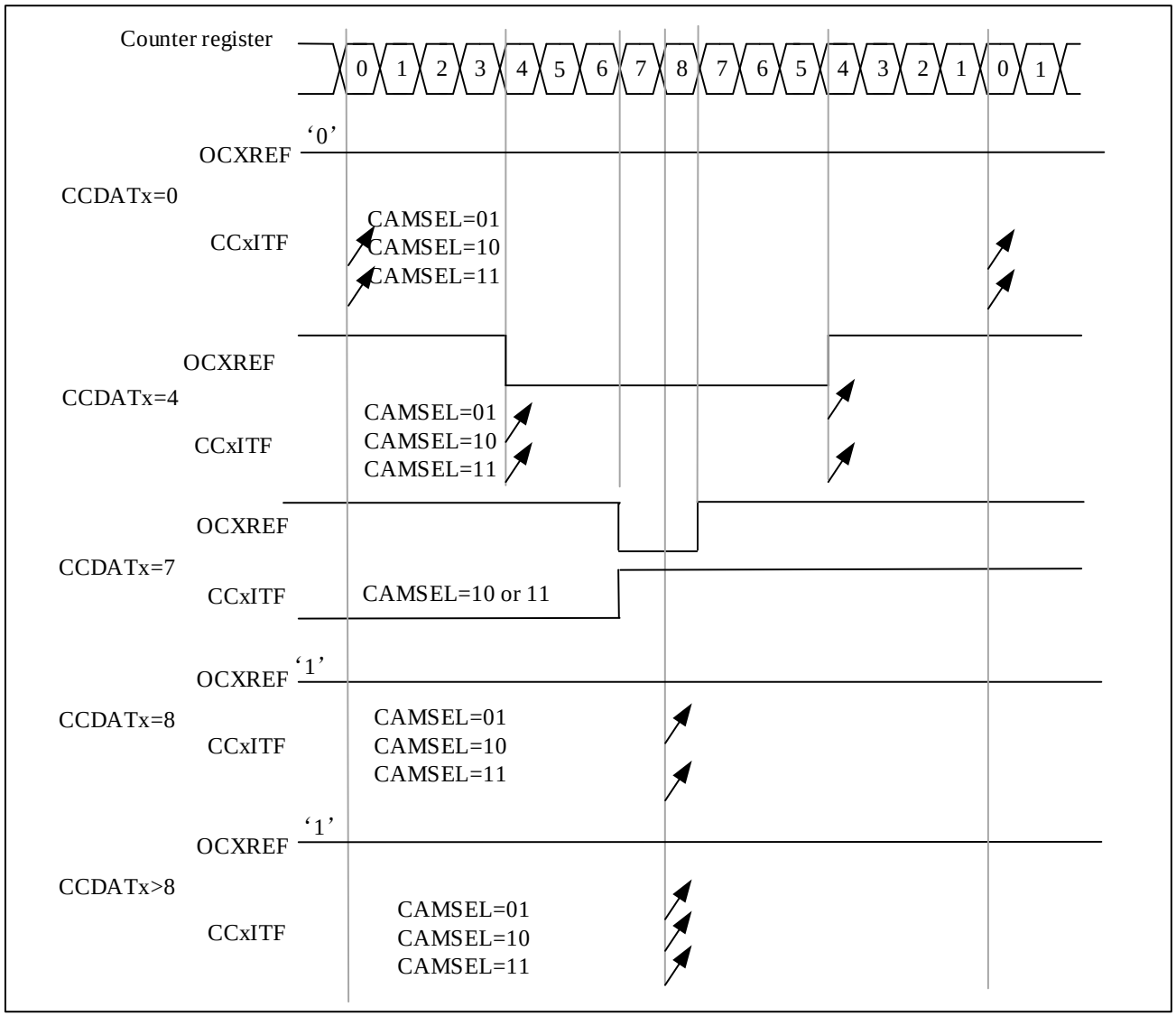
Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL='01'.

Figure 20-23 Center-Aligned PWM Waveform (AR=8)



When using center-aligned mode, users should pay attention to the following considerations:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some examples:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and not writing the counter while it is running.

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20.5.10.2 PWM Center-Aligned Asymmetric Mode

Please refer to Section 20.5.2.3.2 for information on PWM Center-Aligned Asymmetric Mode.

20.5.10.3 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

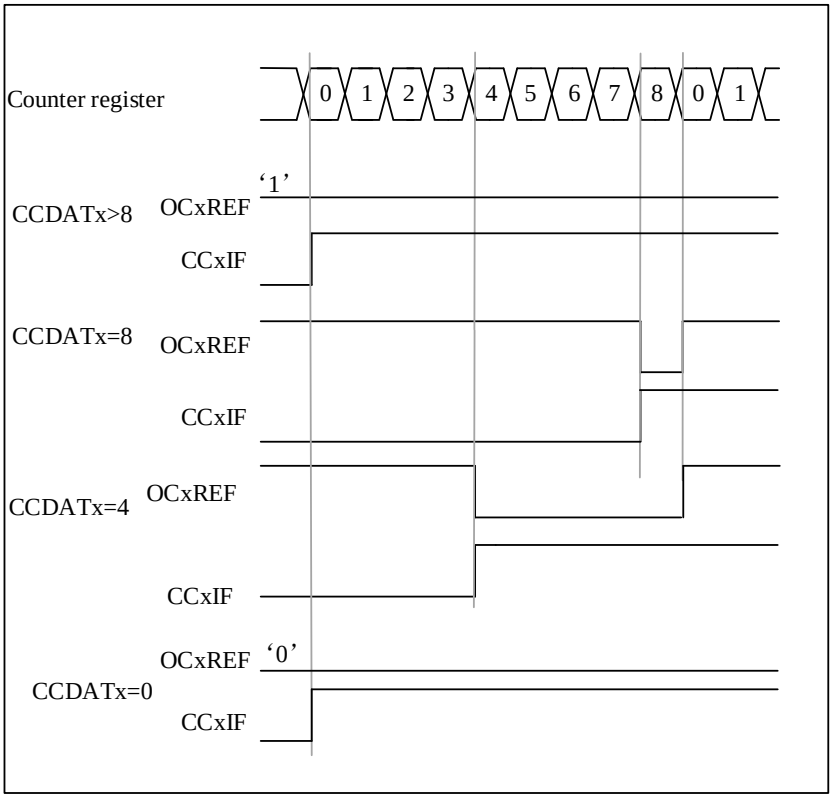
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Example for PWM mode1:

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow：

Figure 20-24 Edge-Aligned PWM Waveform (AR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.
Example for PWM mode1：

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the

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(n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated。

20.5.11 Combined PWM Mode

In the combined PWM mode, programmable delays and phase shifts are allowed between the pulses of the two generated edge-aligned or center-aligned PWM signals. The frequency is determined by the value of the TIMx_AR register, while the duty cycle and delays are determined by two TIMx_CCMODx registers. The generated signal OCxREFC is composed of a logical OR or logical AND combination of the two reference PWM signals.

- OC1REFC (or OC2REFC) is controlled by TIMx_CCDAT1 and TIMx_CCDAT2.
- OC3REFC (or OC4REFC) is controlled by TIMx_CCDAT3 and TIMx_CCDAT4.

Two channels can independently select the combined PWM mode (one OCx output for each pair of TIMx_CCDATx registers) by writing ’1’ to the OCxMD3 bit of the TIMx_CCMODx register, writing ’110’ to the OCxMD bit (Combined PWM mode 1), or writing ’1’ to the OCxMD3 bit and ’111’ to the OCxMD bit (Combined PWM mode 2).

When a given channel is used as a combined PWM channel, its complementary channel must be configured in the opposite PWM mode (for example, one channel configured in Combined PWM mode 1 and the other channel configured in Combined PWM mode 2).

The following diagram illustrates signal examples that can be generated in combined PWM mode, and these signals can be obtained through the following configurations:

- Channel 1 configured in Combined PWM mode 1.
- Channel 2 configured in PWM mode 2.
- Channel 3 configured in Combined PWM mode 2.
- Channel 4 configured in PWM mode 1.

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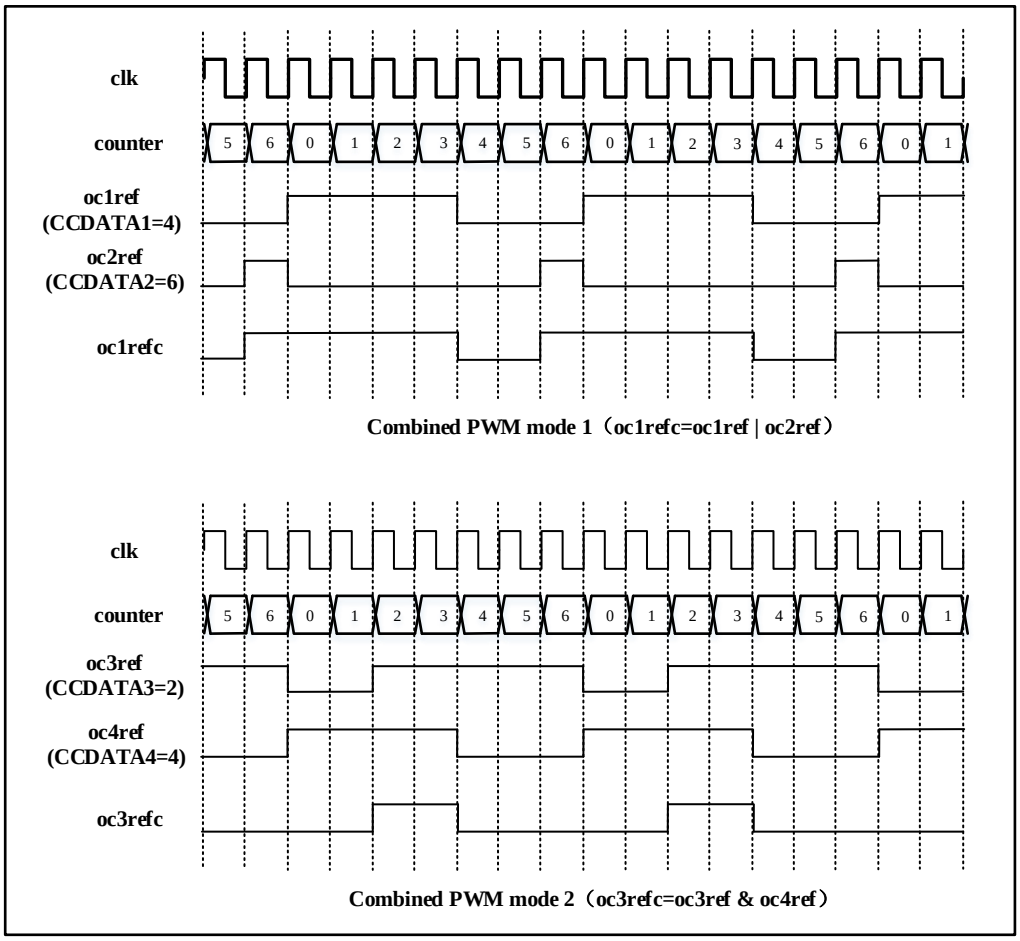
Figure 20-25 Combined PWM mode on channels 1 and 3



20.5.12 One-Pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

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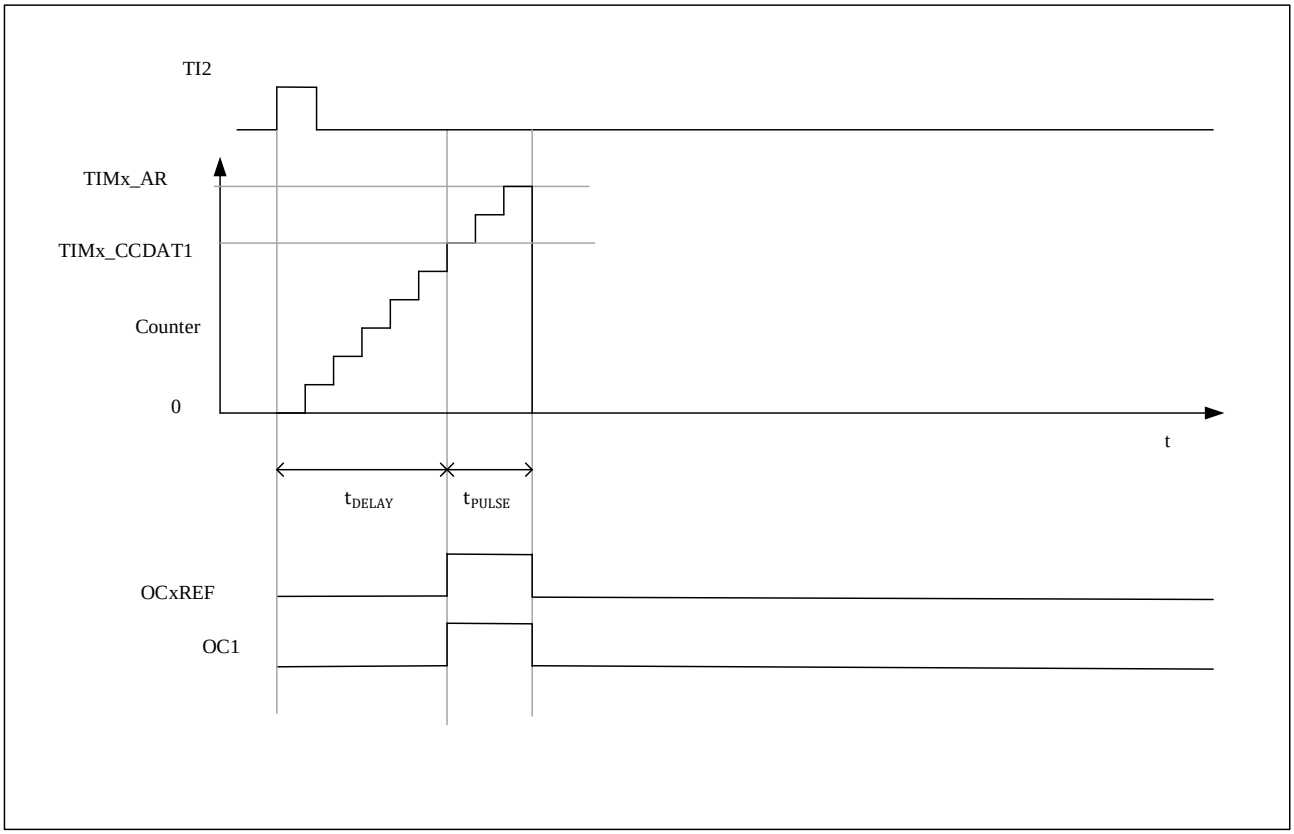
Figure 20-26 Example Of One-Pulse Mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;
2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= '01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= '0';
3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL= '0110' (trigger mode);
4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};
5. Configure TIMx_CTRL1.ONEPM='01' to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = '111' to select PWM2 mode;
6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1.

20.5.12.1 Special case: OCx fast enable

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

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You can set TIMx_CCMODx.OCxFEN='1' to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes。

20.5.13 Retriggerable Single Pulse Mode

This mode allows the counter to start on a trigger signal and generate a programmable-length pulse, but there are differences between this and the non-retriggerable single pulse mode:

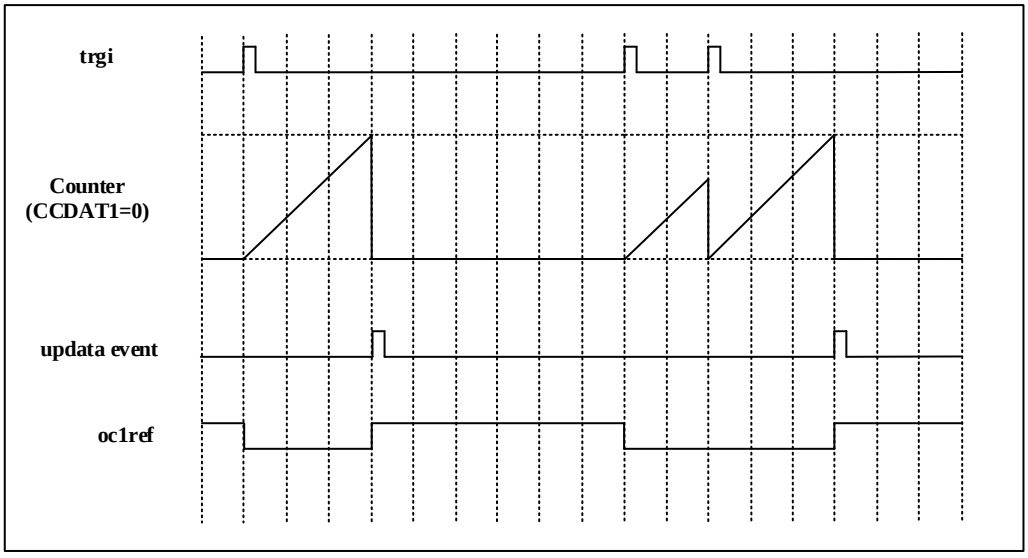
- When triggered, the pulse is generated immediately.
- If a new trigger occurs before the previous one is completed, the pulse will be extended.

The timer must be in slave mode with the TIMx_SMCTRL register bit SMSEL[3:0] = '1110' (Combined reset + trigger mode). For retriggerable single pulse mode 1 or mode 2, write '1' to the OCxMD3 bit and '000' or '001' to the OCxMD bit.

When the timer is configured in up-count mode, the corresponding TIMx_CCDATx must be set to 0 (AR register sets the pulse length). If the timer is configured in down-count mode, CCDATx must be greater than or equal to AR.

The following diagram show the retriggerable single pulse mode 1 as an example:

Figure 20-27 Retriggerable Single Pulse Mode 1



20.5.14 Clearing the OCxREF Signal On An External Event

If user set TIMx_CCMODx.OCxCEN=1, tim_ocref_clr_in input high level can be used to driven the OCxREF signal to low level, and the OCxREF signal will remains low level, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

The clear signal input tim_ocref_clr_in can be selected as tim_ocref_clr or ETRF through the CLRSEL bit in the TIMx_CTRL1 register.

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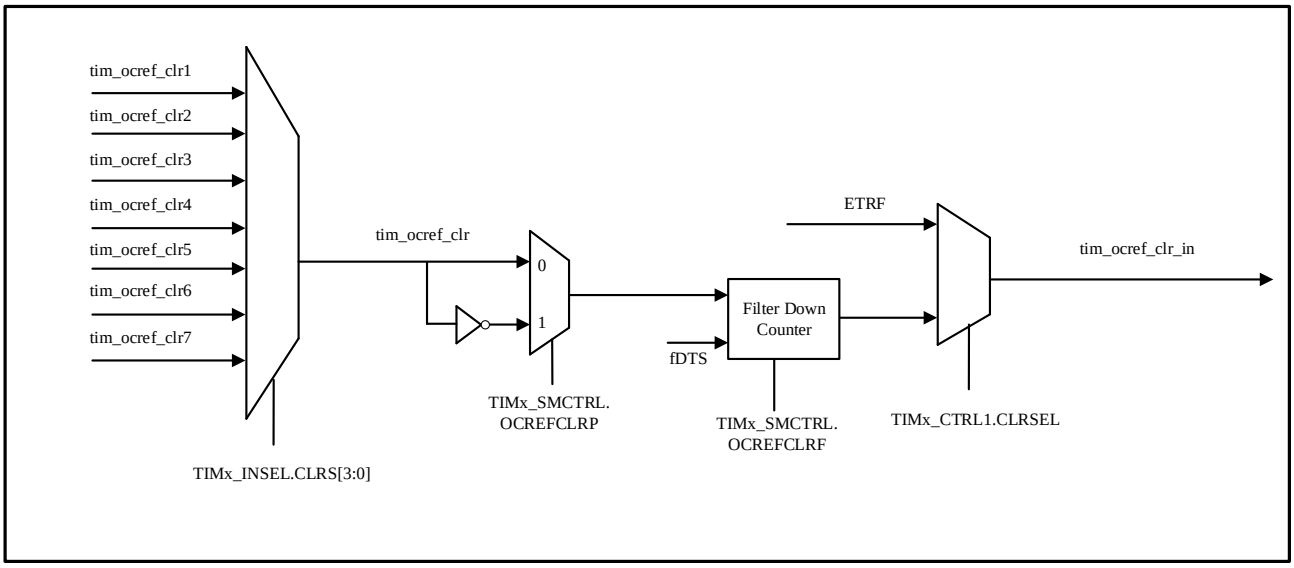
The tim_ocref_clr signal can be selected through the CLRS[3:0] in the TIMx_INSEL register, as shown in the following diagram

Figure 20-28 External event clearing OCxREF signal



For example, when the tim_ocref_clr_in signal is selected as ETRF, the tim_etr_in configuration is as follows：

- Set TIMx_SMCTRL.EXTPS=‘00’, disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=‘0’, disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.
- When the ETRF input goes high, the behavior of the OCxREF signal varies for different OCxCEN values. In this case, the timer is set to PWM mode.

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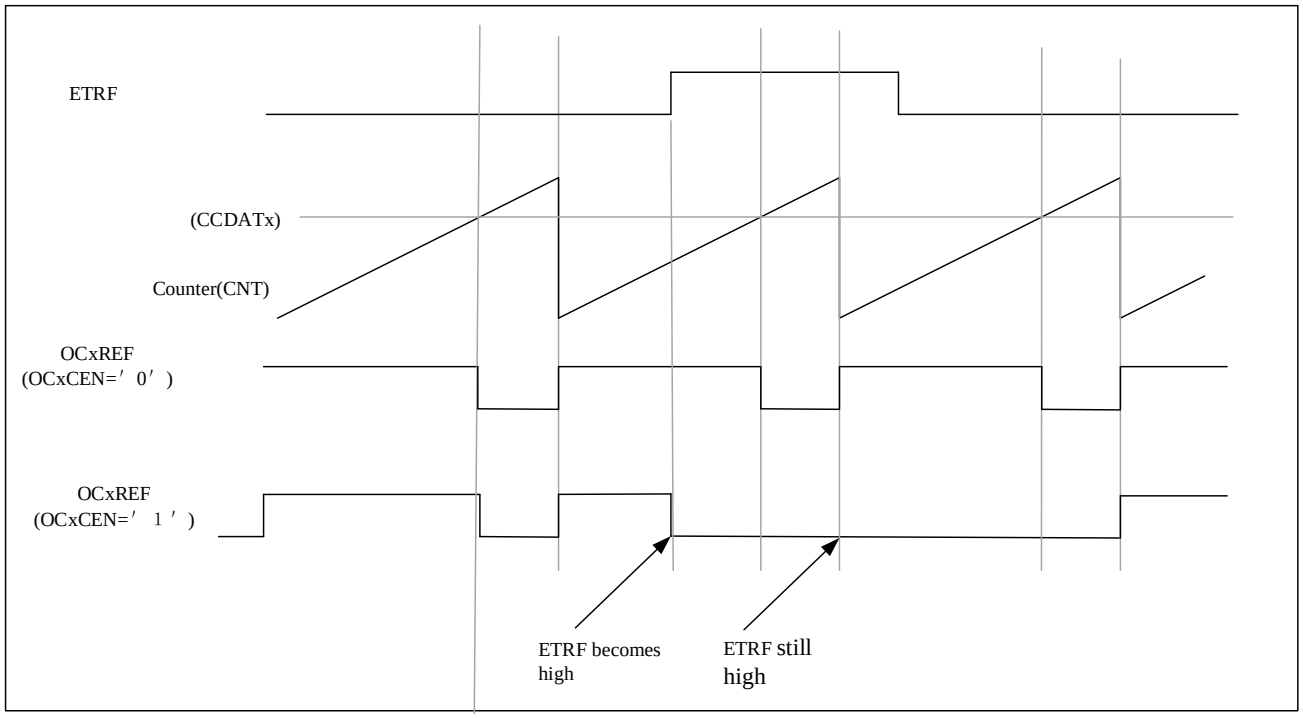
Figure 20-29 Clearing the OCxREF of TIMx



20.5.15 Complementary Output and Dead-Time Insertion

GTIMBx (x=1-3) can output two complementary signals (CH1 and CH1N) and manage the closing and opening of the output. This is referred to as dead time. Users should adjust the dead time based on the device connected to the output and its characteristics.

Users can select the polarity of the output by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP, and this selection is independent for each output.

Users can control the complementary signals OCx and OCxN by setting a combination of control bits, namely TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. The dead time will be activated when switching to the idle state.

If the user sets both TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN, dead time will be inserted. If there is breaking, TIMx_BKDT.MOEN should also be set. Each channel has a 10-bit dead-time generator.

The reference waveform OCxREF can generate two outputs, OCx and OCxN. If OCx and OCxN are active high, the OCx output signal will be the same as the reference signal, while the OCxN output signal will be the inverse of the reference signal. However, the OCx output signal will have a delay relative to the reference rising edge, and the OCxN output signal will have a delay relative to the reference falling edge. If the delay is greater than the width of the effective OCx or OCxN output, the corresponding pulse will not be generated.

The relationship between the output signal of the dead-time generator and the reference signal OCxREF is as follows:

If TIMx_CCEN.CCxP=0， TIMx_CCEN.CCxNP=0， TIMx_BKDT.MOEN=1， TIMx_CCEN.CCxEN=1， TIMx_CCEN.CCxNEN=1.

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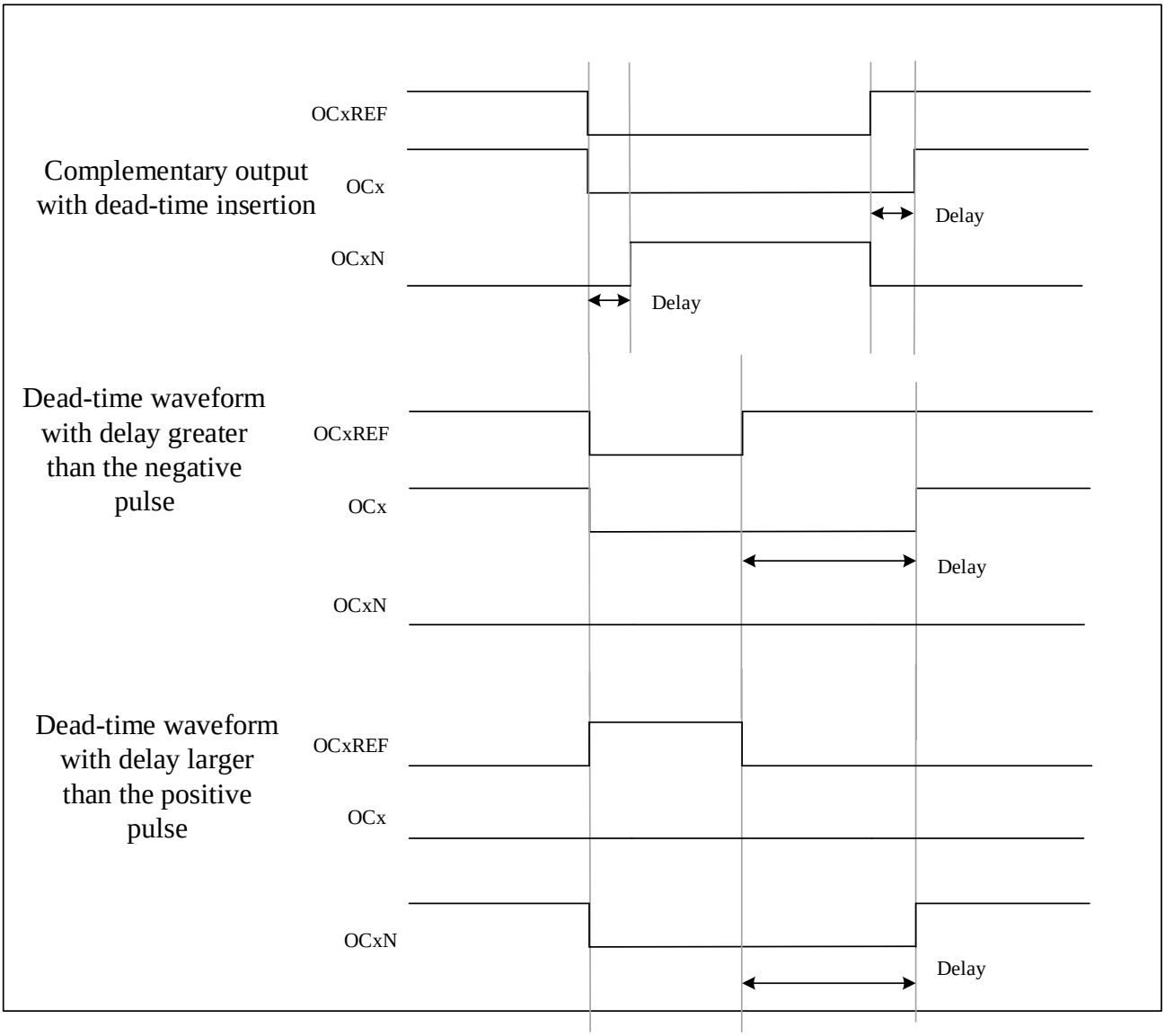
Figure 20-30 Complementary Output with Dead-Time Insertion



Users can set TIMx_BKDT.DTGN to program the dead-time delay for each channel.

20.5.15.1 Redirecting OCxREF to OCx or OCxN

In output mode, users can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to redirect OCxREF to the OCx output or OCxN output.

There are two ways to use this feature. When the complementary is held at its inactive level, users can use this feature to send specific waveforms, such as PWM or static active levels. Users can also use this feature to set both outputs to inactive levels, or set both outputs to active levels, complementary and with dead time.

If the user sets TIMx_CCEN.CCxEN=0 and TIMx_CCEN.CCxNEN=1, they are not complementary. When OCxREF is high, OCxN will become active. On the other hand, if the user sets TIMx_CCEN.CCxEN=1 and TIMx_CCEN.CCxNEN=1, OCx will become active when OCxREF is high. Conversely, when OCxREF is low, OCxN will become active.

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20.5.16 Breaking Function

When using the breaking function, setting the corresponding control bits will modify the output enable signal and inactive level. However, at any time, the outputs of OCx and OCxN cannot be at active levels simultaneously, meaning that the condition (CCxP ^ OIx) ^ (CCxNP ^ OIxN) != 0 must be satisfied.

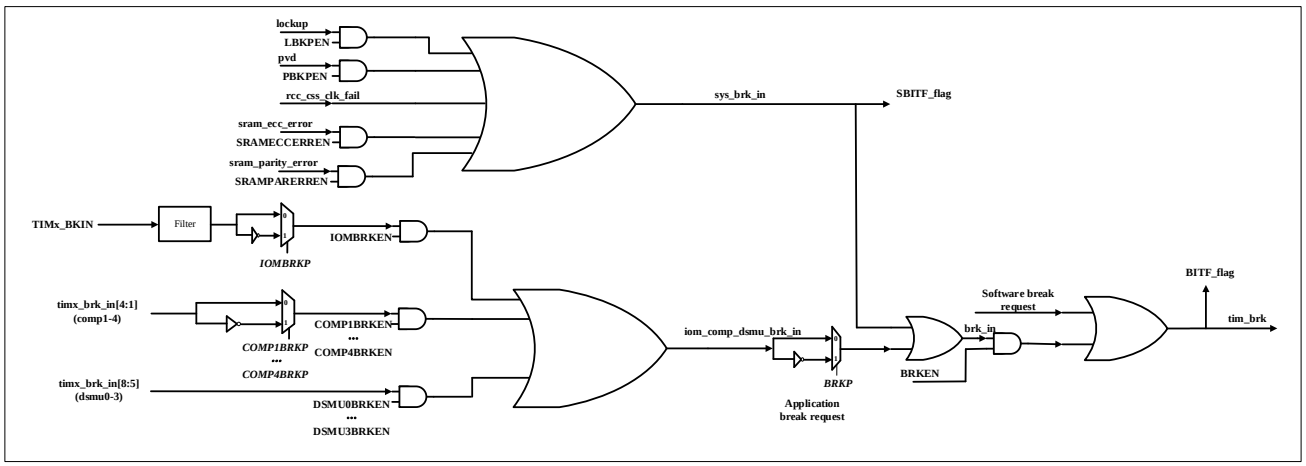
When multiple breaking signals are enabled, each breaking signal forms an OR logic. There are several signals that may act as sources of breaking.

Break 1：

- Break 1 input pin.
- Clock failure event, generated by the Clock Security System(CSS) in the RCC clock.
- PVD event.
- Core Hardfault event.
- SRAM ECC error.
- SRAM parity error.
- FLASH ECC error.
- Comparator output signal.
- Software set TIMx_EVTGEN.BGN.

Perform OR operation on all sources before entering the timer tim_brk input, as shown in the diagram.

Figure 20-31 Break input



Note: Asynchronous (clockless) operation can only be guaranteed when the programmable filters are disabled. If the programmable filters are enabled, the fault-safe clock mode (e.g., using internal PLL and/or CSS) must be used to ensure handling of open circuit events.

After reset, the break circuit will be disabled. The MOEN bit will be at a low level. Users can set TIMx_BKDT.BKEN to enable the break function. By setting TIMx_BKDT.BKP, you can select the polarity of the break input signal. Users can simultaneously modify TIMx_BKDT.BKEN and TIMx_BKDT.BKP. After users set TIMx_BKDT.BKEN

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and TIMx_BKDT.BKP, there is a 1 APB clock cycle delay before it takes effect. Therefore, users need to wait for 1 APB clock cycle before reading back the written value.

The falling edge of MOEN can be asynchronous, so a synchronization circuit is placed between the actual signal and the synchronous control bit. This circuit will introduce a delay between the asynchronous and synchronous signals. When the user sets TIMx_BKDT.MOEN to a low level, a delay needs to be inserted before reading this value. This is because an asynchronous signal is written, but the user is reading a synchronous signal.

The behavior after the break occurs is as follows:

- TIMx_BKDT.MOEN will be asynchronously cleared, and then the output will enter an invalid state, idle state, or reset state. The output state can be selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is turned off.
- Once TIMx_BKDT.MOEN=0,the output of each output channel will be driven by the level programmed in TIMx_CTRL2.OIx. If TIMx_BKDT.OSSI=0, the timer will release the enable output (taken over by the GPIO controller), otherwise, it will remain at a high level.
- If the user chooses to use complementary outputs, the behavior of TIM is as follows:
  - Depending on the polarity, the output will first be set to the reset state. This is an asynchronous option, so it can still working even if no clock is provided to the timer.
  - If the timer clock is still provided, the dead-time generator will be reactivated when (CCxP ^ OIx) ^ (CCxNP^OIxN) != 0, meaning that OCx and OCxN still cannot be simultaneously driven to valid levels. After the dead time, the outputs will be driven based on the values of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN. Please note that due to the synchronization circuit on MOEN (approximately 2 ck_tim periods), the dead time will be longer than usual.
  - If TIMx_BKDT.OSSI=0, the timer will release output control. Otherwise, if the enable output is at a high level, it will remain high. If it is at a low level, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is at a high level.
- If TIMx_DINTEN.BIEN=1, an interrupt will be generated when TIMx_STS.BITF=1.
- If the user sets TIMx_BKDT.AOEN, TIMx_BKDT.MOEN will be automatically set on the next UEV occurrence. The user can adjust it using this feature. If the user does not set TIMx_BKDT.AOEN, TIMx_BKDT.MOEN will remain at a low level until set to 1 again. In this case, the user can use it to ensure safety. The user can connect the break input to a thermal sensor, power driver alarm, or other safety components.
- When the break input is active, TIMx_BKDT.MOEN cannot be automatically set or set simultaneously by software, and TIMx_STS.BITF cannot be cleared. This is because the break input is in an active state at the level.

To ensure application safety, the break circuit has write protection functionality and break input-output management. It allows users to freeze certain parameters, such as dead-time duration, OCx/OCxN polarity and disabled state, OCxMD configuration, break enable and polarity. Users can choose one of three protection levels by setting TIMx_BKDT.LCKCFG. However, TIMx_BKDT.LCKCFG can only be written once after MCU reset.

The output behavior in response to the break is shown as follows:

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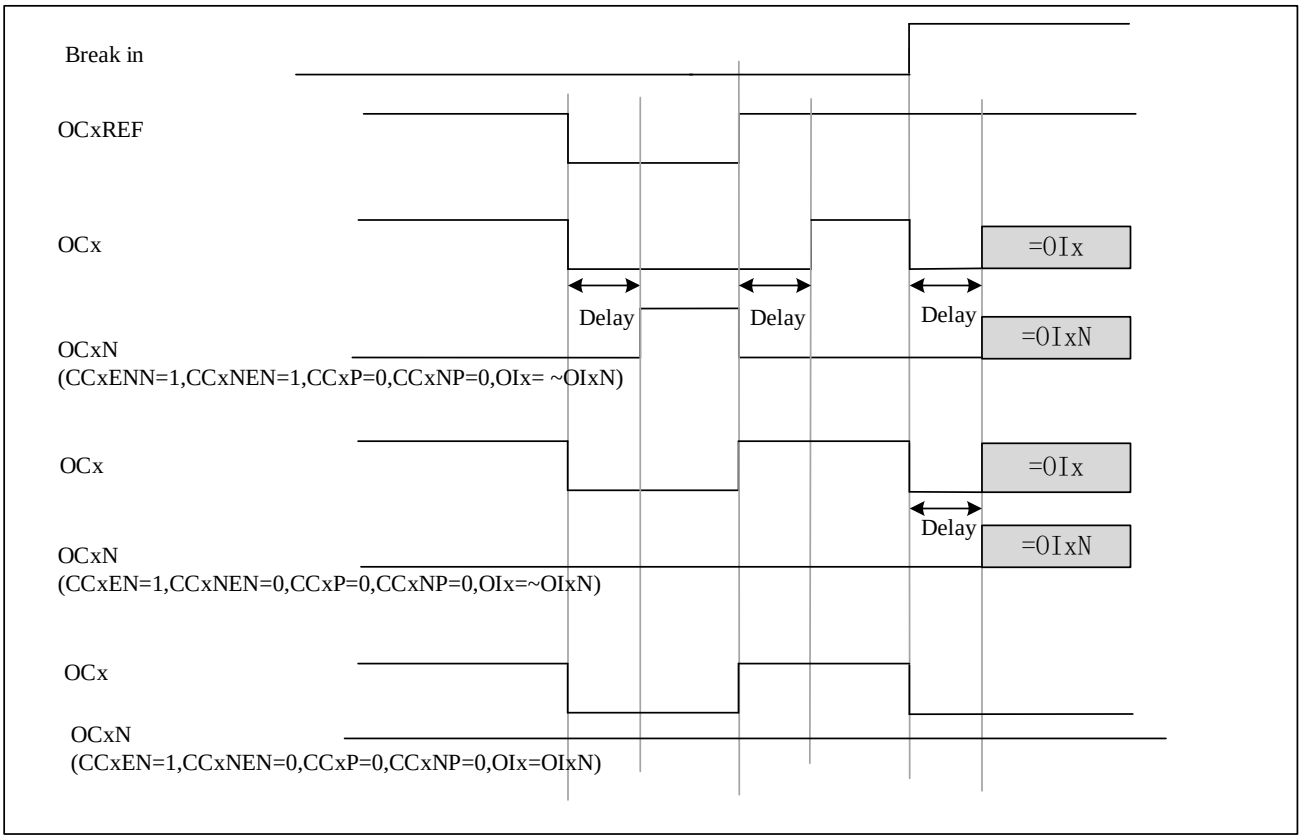
Figure 20-32 The output behavior in response to the break

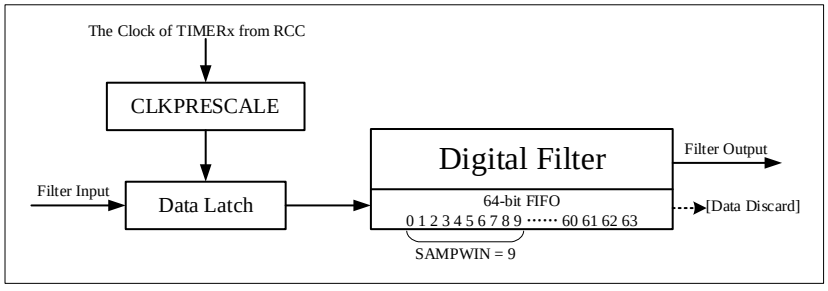


- The tim_brk input can disable (invalid state) the PWM output, or force the PWM output to a predefined safe state.

20.5.16.1 Break Filter

The register TIMx_BKFR is described as follows：

Figure 20-33 Sliding filter



- The digital filter samples the brake signal using the RCC's TIMx clock and accumulates the samples in a 64-bit FIFO. It samples data only within the window size defined in TIMx_BKFR.WSIZE [5:0], with a maximum size of 64.
- The filter output samples the majority value within the sampling window, which is defined by the threshold in TIMx_BKFR.THRESH [5:0], with a maximum threshold of 63. This value should be equal to or greater than half the window size. If the count of logic 1s and logic 0s within the sampling window is not greater than the

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threshold, the digital filter will maintain the previous output value.

- The TIMx_BKFR.SLIDFPSC[15:0] register determines the sampling rate of the corresponding digital filter. The filter FIFO captures a sample value from the input at each sampling clock.
- If the digital filter is disabled, the filter input is directly output.

20.5.17 Bidirectional Break

GTIMBx (x=1-3) has bidirectional break I/O function.

Application support :

● A board-level global break signal, which can send a fault signal to an external MCU or gate driver through a unique IO pin that is both an input and output.

●When multiple internal and external break sources need to be merged, they are connected together through "OR" operation to generate a single break event.

The tim_brk input can be configured as bidirectional mode by controlling the BRKBID in the TIMx_BDTR register. The BRKBID can be locked in read-only mode (at LOCK level 1 or above) using the LOCK bit in the TIMx_BKDT register.

Bidirectional mode is available for the tim_brk input, requiring the I/O configuration to be in open-drain mode with a low-level polarity (through TIMx_AF1.IOMBRKP, TIMx_BKDT.BKP bits). Any break request from the system (such as CSS), on-chip peripherals, or break input will force the break input to a low level to indicate a fault event. For safety reasons, if the polarity bit is not set correctly, the bidirectional mode will be suppressed (for example, if set to high-level effective, bidirectional mode will not take effect).

A software break event (TIMx_EVTGEN.BGN) will also force the break IO to "0" to indicate to external devices that the timer has entered the break state. However, this is only effective when the break is enabled (TIMx_BKDT.BKEN=1). When a software break event occurs (TIMx_BKDT.BKEN=0), the output is placed in a safe state, and the break flag is set. However, this has no effect on the TIMx_BKIN I/O.

The safety release mechanism prevents the system from being completely locked (breaking triggered by a low level on the break input, thereby forcing a low level on the same input).

When the TIMx_BKDT.BRKDSRM bit is set to 1, the brake output will be released to clear a fault signal and provide the possibility for system restart.

At any time, the brake protection circuit cannot be disabled：

●The break input path is always active: even if the TIMx_BKDT.BRKDSRM bit is set and the open-drain control is released, the break event remains active. This prevents the PWM output from restarting when break conditions are present.

●The TIMx_BKDT.BRKDSRM bit cannot release the brake protection as long as the output is enabled (TIMx_BKDT.MOEN bit is set).

Table 20-11 Conditions For Releasing The Break Protection State

MOEN	BRKBID	BRKDSRM	Break Protection State

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0	0	X	Protection
0	1	0	Protection
0	1	1	Release Protection
1	X	X	Protection

Enable and Re-enable the break circuit :

By default (in input or bidirectional mode), the break circuit is in standby mode (peripheral reset configuration).

After a break event, the following procedure must be followed to re-enable the protection:

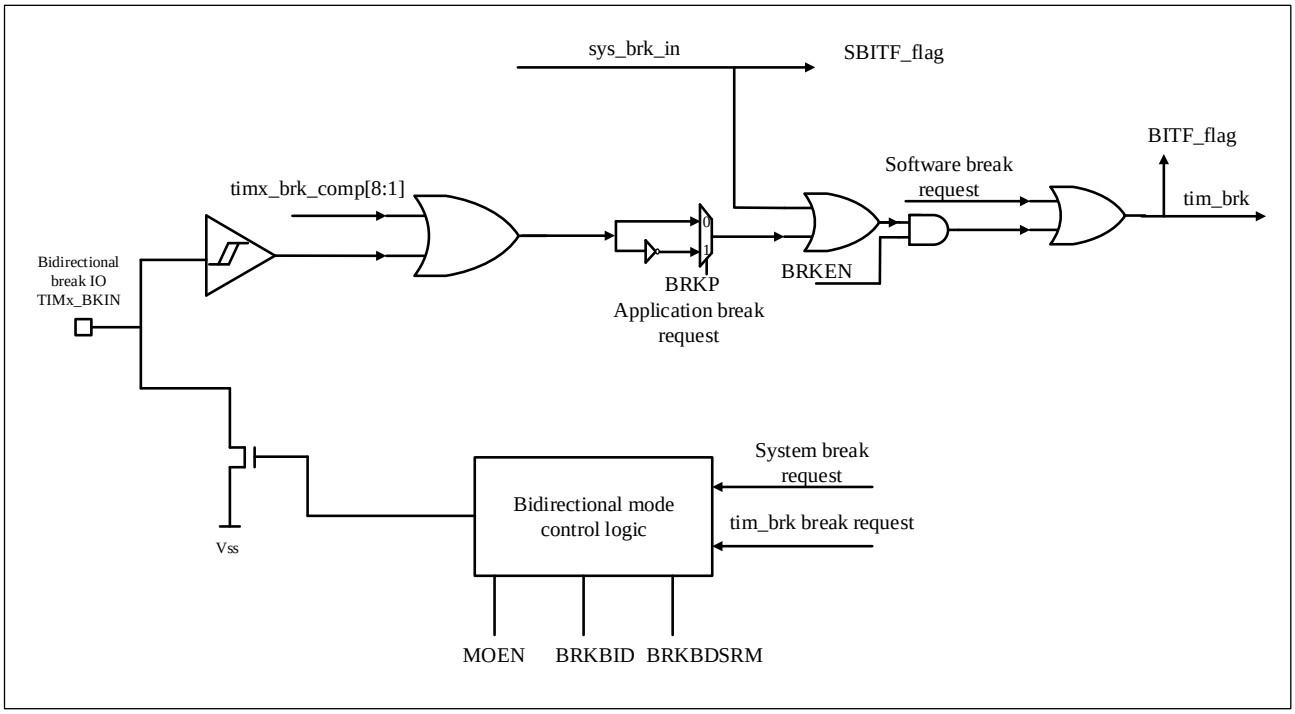
●The TIMx_BKDT.BRKDSRM bit must be set to release the output control

●The software must wait for the system break condition to disappear and clear the TIMx_STS.SBIF status flag (or have the system clear it before re-enabling)

●The software must poll the TIMx_BKDT.BRKDSRM bit until it is cleared by hardware (when the application's break condition disappears)

From this point, the break circuit is in standby and active state, and the TIMx_BKDT.MOEN bit can be set to re-enable the PWM output.

Figure 20-34 Output Redirection



20.5.18 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M4F core halted), depending on the

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DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop..

20.5.19 Synchronization of GTIMBx and External Trigger

The timer can be synchronized through triggers in the slave mode(reset、trigger and gated).

20.5.19.1 Slave Mode: Reset Mode

In the reset mode, the trigger event can reset the counter and prescaler. It updates the preload registers TIMx_AR, TIMx_CCDATx, and generates an update event UEV (TIMx_CTRL1.UPRS=0).

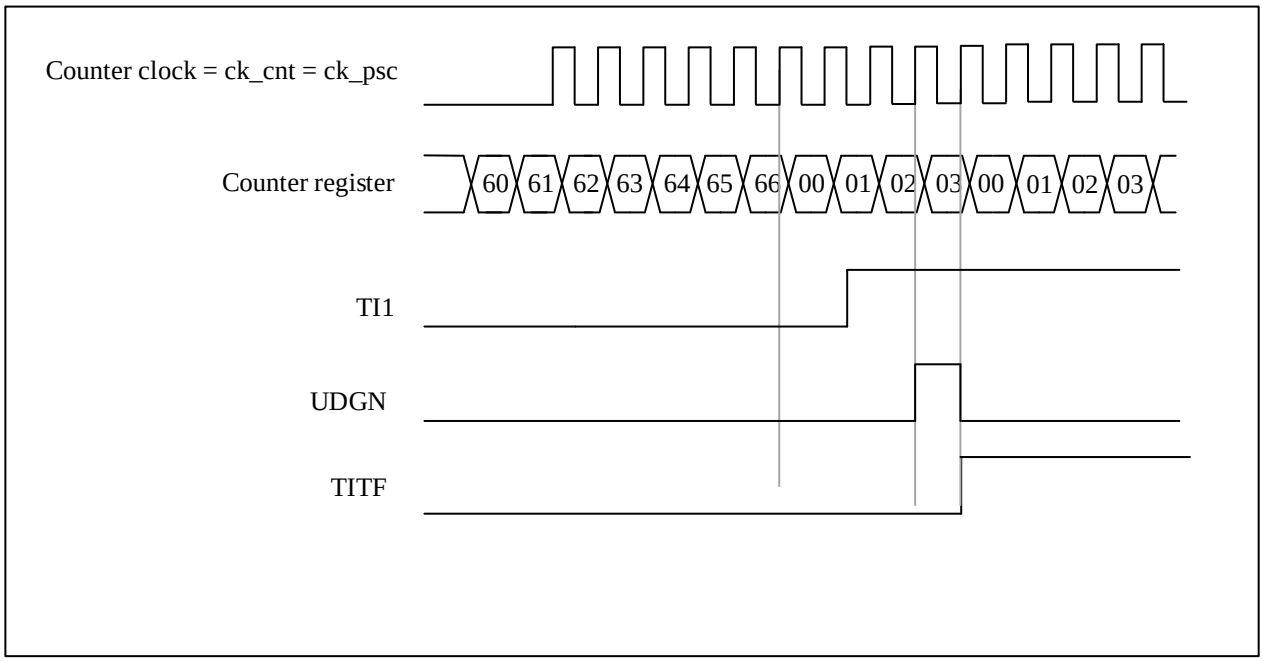
Here is an example of the reset mode:

4. Channel 1 is configured to detect the rising edge of TI1 input (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0) ;
5. Select the slave mode as reset mode (TIMx_SMCTRL.SMSEL=0100), and choose TI1 as the trigger input selection (TIMx_SMCTRL.TSEL=101) ;
6. Start the counter (TIMx_CTRL1.CNTEN=1).

After starting the timer, when a rising edge is detected by TI1, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1) ;

The delay between the rising edge of TI1 and the actual counter reset is caused by the synchronization circuit of the TI1 input.

Figure 20-35 Control Circuit in the Reset Mode



20.5.19.2 Slave Mode: Trigger Mode

In trigger mode, the trigger event (rising edge/falling edge) on the input port can trigger the counter to start counting.

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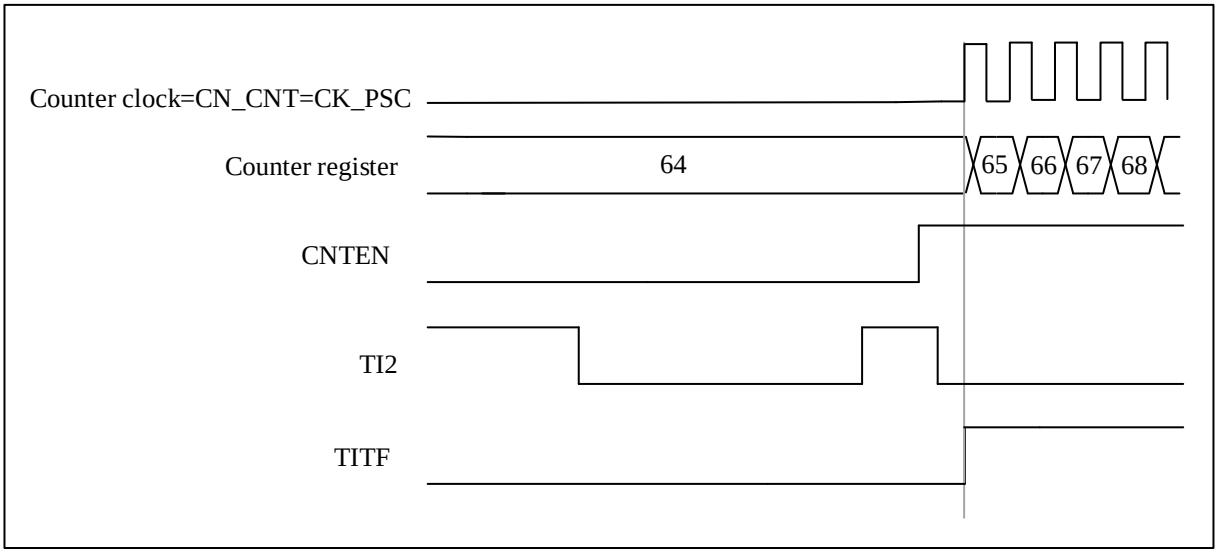
Here is an example of the trigger mode:

3. Channel 2 is configured as input, detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01, TIMx_CCEN.CC2P=0) ;
4. Select the slave mode as trigger mode (TIMx_SMCTRL.SMSEL=0110), and select TI2 as the trigger input (TIMx_SMCTRL.TSEL=110) ;

When a rising edge is detected by TI2, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1) ;

The delay between the rising edge of TI2 and the actual start of the counter is caused by the synchronization circuit of the TI2 input.

Figure 20-36 Control Circuit in Trigger Mode



20.5.19.3 Slave Mode: Gated Mode

In gated mode, the logic level polarity of the input port can determine whether the counter counts.

Here is an example of gated mode :

4. Channel 1 is configured to detect low level input on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1) ;
5. Select the slave mode as gated mode (TIMx_SMCTRL.SMSEL=0101), and choose TI1 as the TRGI (TIMx_SMCTRL.TSEL=101) ;
6. Start the counter (TIMx_CTRL1.CNTEN=1) ;

When TI1 detects a transition from low to high level, the counter stops counting. When TI1 detects a transition from high to low level, the counter starts counting. The trigger flag is set when counting starts or stops (TIMx_STS.TITF=1).

The delay between the rising edge of TI1 and the actual stop of the counter is caused by the synchronization circuit of the TI1 input.

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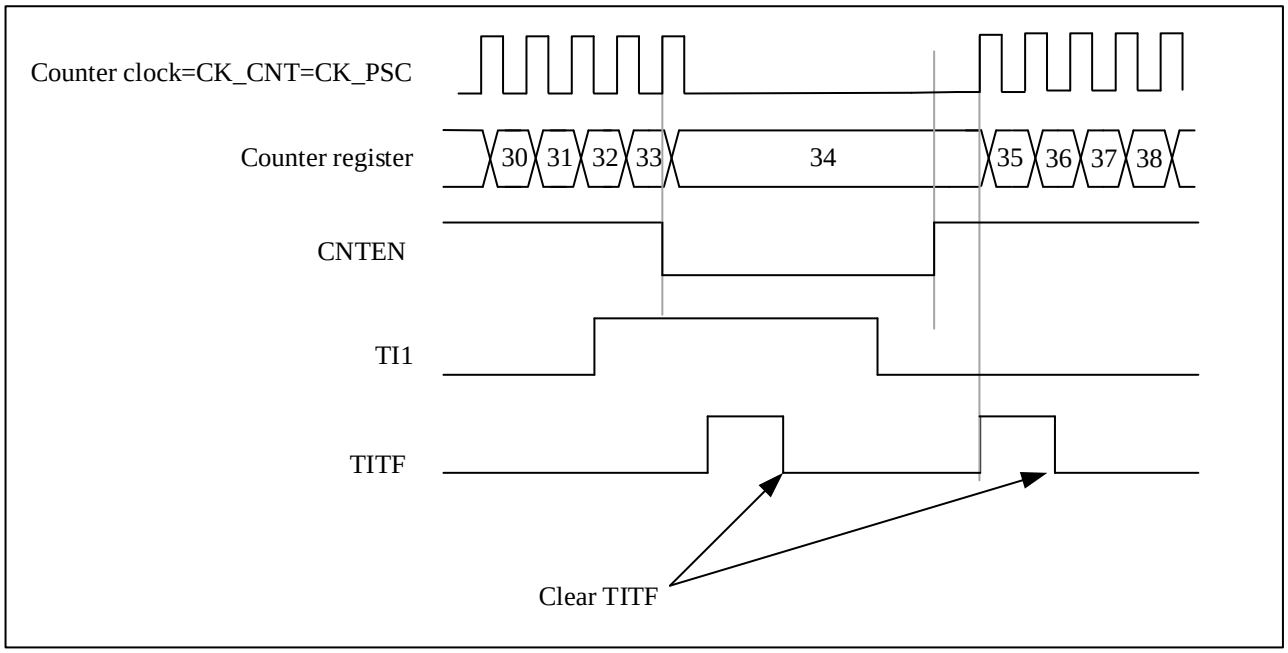
Figure 20-37 Control Circuit in Gated Mode



20.5.19.4 Slave Mode: Trigger mode + External Clock Mode 2

In reset mode, trigger mode, and gated mode, the counter clock can be selected as External Clock Mode 2, with the ETR signal as the external clock source input. In this case, the trigger selection should choose a non-ETRF option (TIMx_SMCTRL.TSEL=111).

This is an example：

3. Channel 1 is configured to detect the rising edge of TI1 as input (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0) ;
4. Enable External Clock Mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), set trigger mode as slave mode (TIMx_SMCTRL.SMSEL=0110), and choose TI1 as the TRGI (TIMx_SMCTRL.TSEL=101) ;

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR and sets the trigger flag (TIMx_STS.TITF=1) ;

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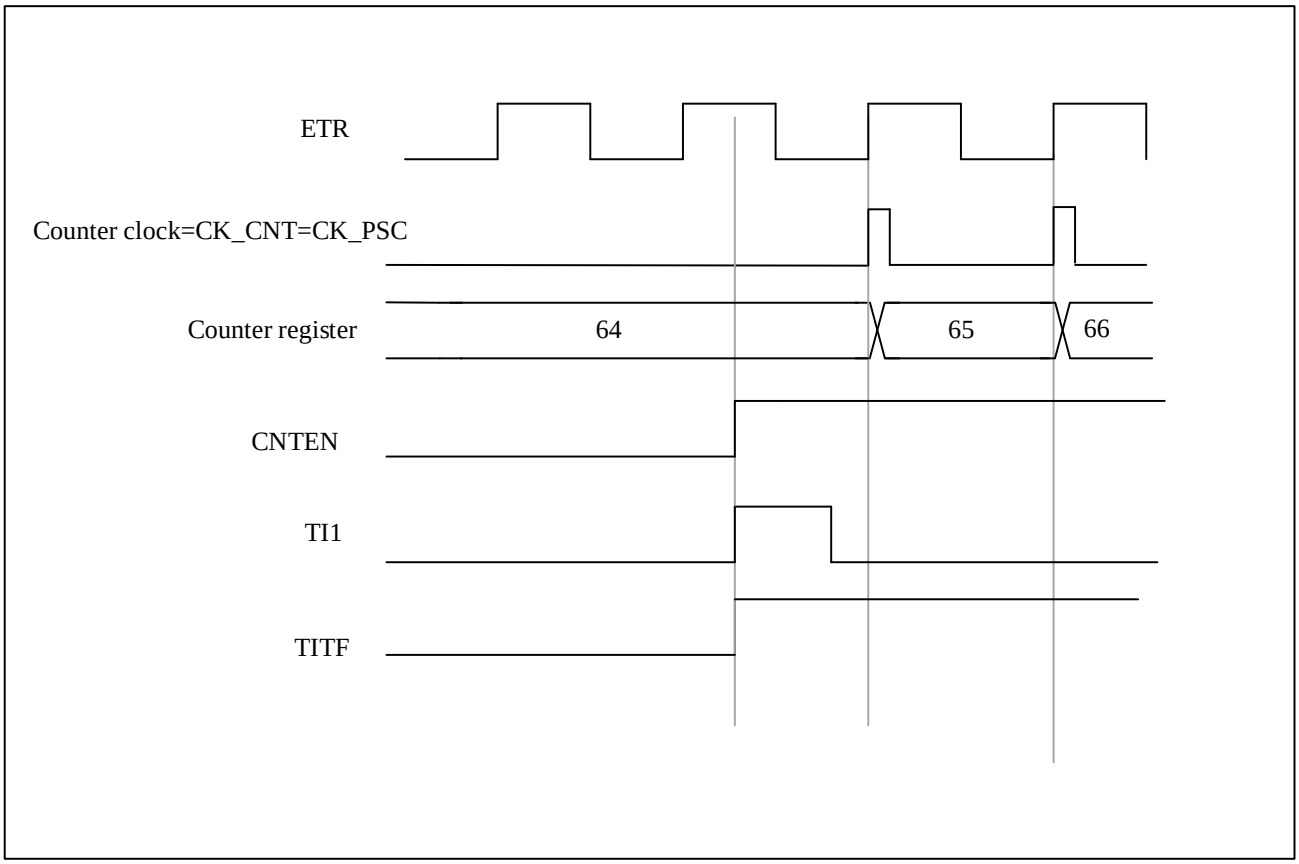
Figure 20-38 Control circuit in External Clock Mode 2 + Trigger Mode



20.5.19.5 Slave Mode: Combined Reset + Trigger Mode

In this case, the rising edge of the selected trigger input (TRGI) will reinitialize the counter, update the generation of registers, and start the counter.

This mode is used for one pulse mode.

The selected event on the input port resets and enables the counter.

In the following example, the counter resets on the rising edge of the TI2 input and starts counting up.

- Configure channel 2 to detect the rising edge of TI2. Set the input filter bandwidth (in this case, no filter is needed, keep TIMx_CCMOD1.IC2F=0000). Capture prescaler is not used in the trigger operation, so no configuration is needed. The TIMx_CCMOD1.CC2SEL bit is only used to select the input capture source, set TIMx_CCMOD1.CC2SEL=01. Set TIMx_CCEN.CC2P=1 to determine the polarity (detect only low level).
- Set TIMx_SMCTRL.SMSEL=1110 to configure the timer for combined reset + trigger mode； Set TIMx_SMCTRL.TSEL=110 to select TI2 as the input source.

When a rising edge occurs on TI2, the counter starts counting under the internal clock drive and sets the TITF flag。

The delay between the rising edge of TI2 and the start of counting by the counter depends on the synchronization circuit of the TI2 input terminal。

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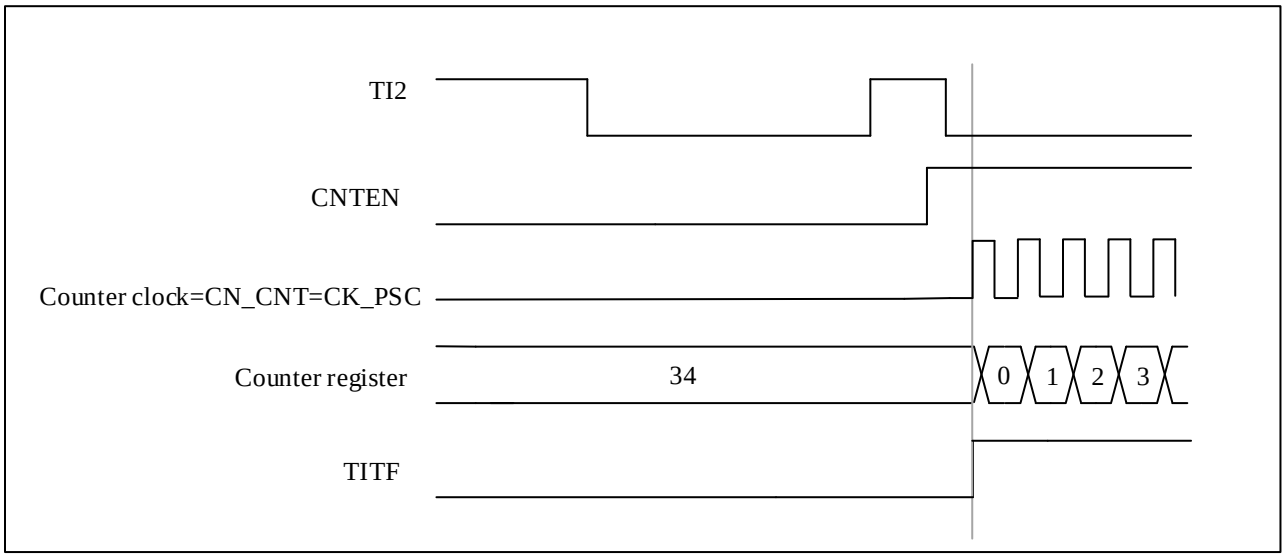
Figure 20-39 Control Circuit in Combined Reset + Trigger Mode



20.5.19.6 Slave Mode : Combined Gated + Reset Mode

When the trigger input (TRGI) is high level, the counter clock is enabled. Once the trigger goes low level, the counter will stop and be reset. The start and stop of the counter are both controlled.

This mode can detect out-of-range PWM signals (duty cycle exceeding the maximum expected value).

In the following example, the counter only counts up when TI1 is low level, and stops and resets when TI1 becomes high level :

- Configure channel 1 to detect low level on TI1. Set the input filter bandwidth (in this case, no filter is needed, so keep TIMx_CCMOD1.IC1F=0000). Capture prescaler is not used in the trigger operation, so no configuration is needed. The TIMx_CCMOD1.CC1SEL bit is used to select the input capture source, set TIMx_CCMOD1.CC1SEL=01. Set TIMx_CCEN.CC1P=1 to determine the polarity (detect only low level).
- Set TIMx_SMCTRL.SMSEL=1101 to configure the timer for gated + reset mode; Set TIMx_SMCTRL.TSEL=101 to select TI1 as the input source.
- Set CNTEN=1 in the TIMx_CTRL1 register to start the counter. In gated + reset mode, if CNTEN=0, the counter cannot start, regardless of the trigger input level.

As long as TI1 is low, the counter starts counting based on the internal clock; once TI1 goes high, the counting stops. The TITF flag in TIMx_STS is set whenever the counter starts or stops.

The delay between the rising edge of TI1 and the actual stop of the counter depends on the synchronization circuit of the TI1 input terminal.

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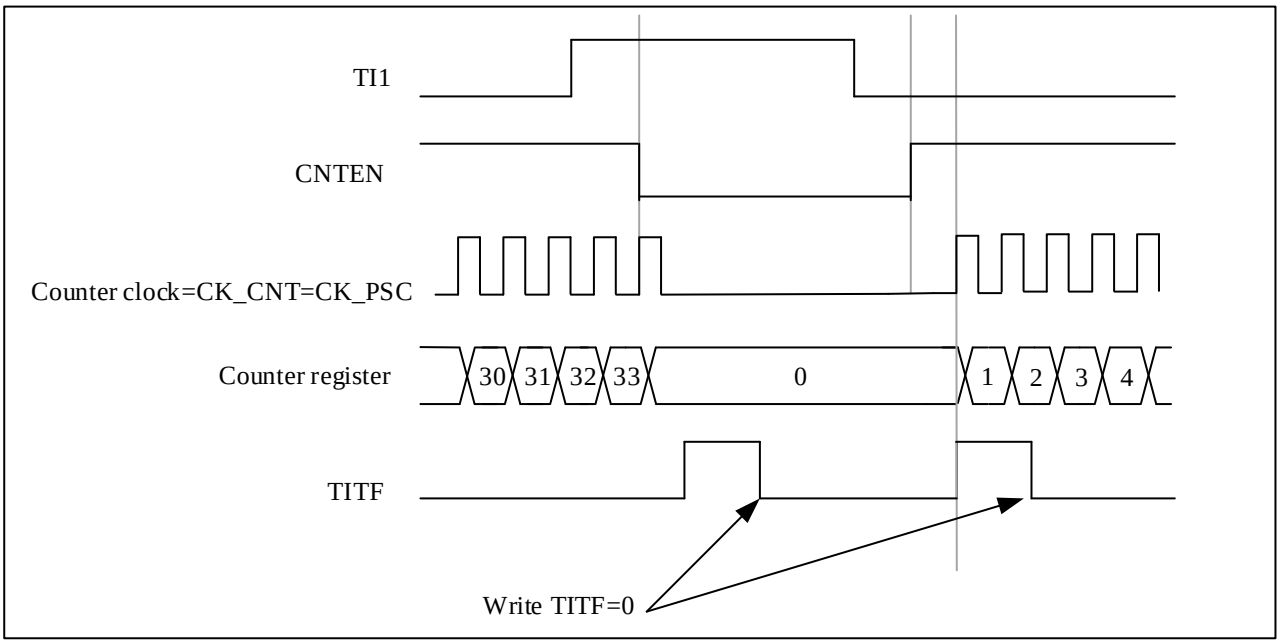
Figure 20-40 Control Circuit in Combined Gated + Reset Mode



20.5.20 Timer Synchronization

All TIM timers are internally connected for timer synchronization or chaining. Refer to Section 19.5.14.

20.5.21 Trigger ADC

The timer can generate ADC trigger events through various internal signals, such as reset, enable, or compare events, and can also generate pulse triggers issued by internal edge detectors. The selection of issuing trigger signals on the internal line redirected to ADC TRGO can be done by selecting the MMSEL[3:0] bits in the TIMx_CTRL2 register.

20.5.22 Generating Six-Step PWM Output

To simultaneously modify the configuration of all channels, you can pre-set the configuration for the next step (preload bits for OCxMD, CCxEN, and CCxNEN). When a COM commutation event occurs, the preload bits for OCxMD, CCxEN, and CCxNEN are transferred to the shadow register bits.

Method of generating COM commutation events :

1. Software set TIMx_EVTGEN.CCUDGN ;
2. Generated by hardware on the rising edge of TRGI ;

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, enabling the interrupt (TIMx_DINTEN.COMIEN) to generate an interrupt, and enabling the DMA request (TIMx_DINTEN.COMDEN) will generate a DMA request.

The following diagram shows the timing diagram of the output of OCx and OCxN when a COM commutation event occurs under three different configurations :

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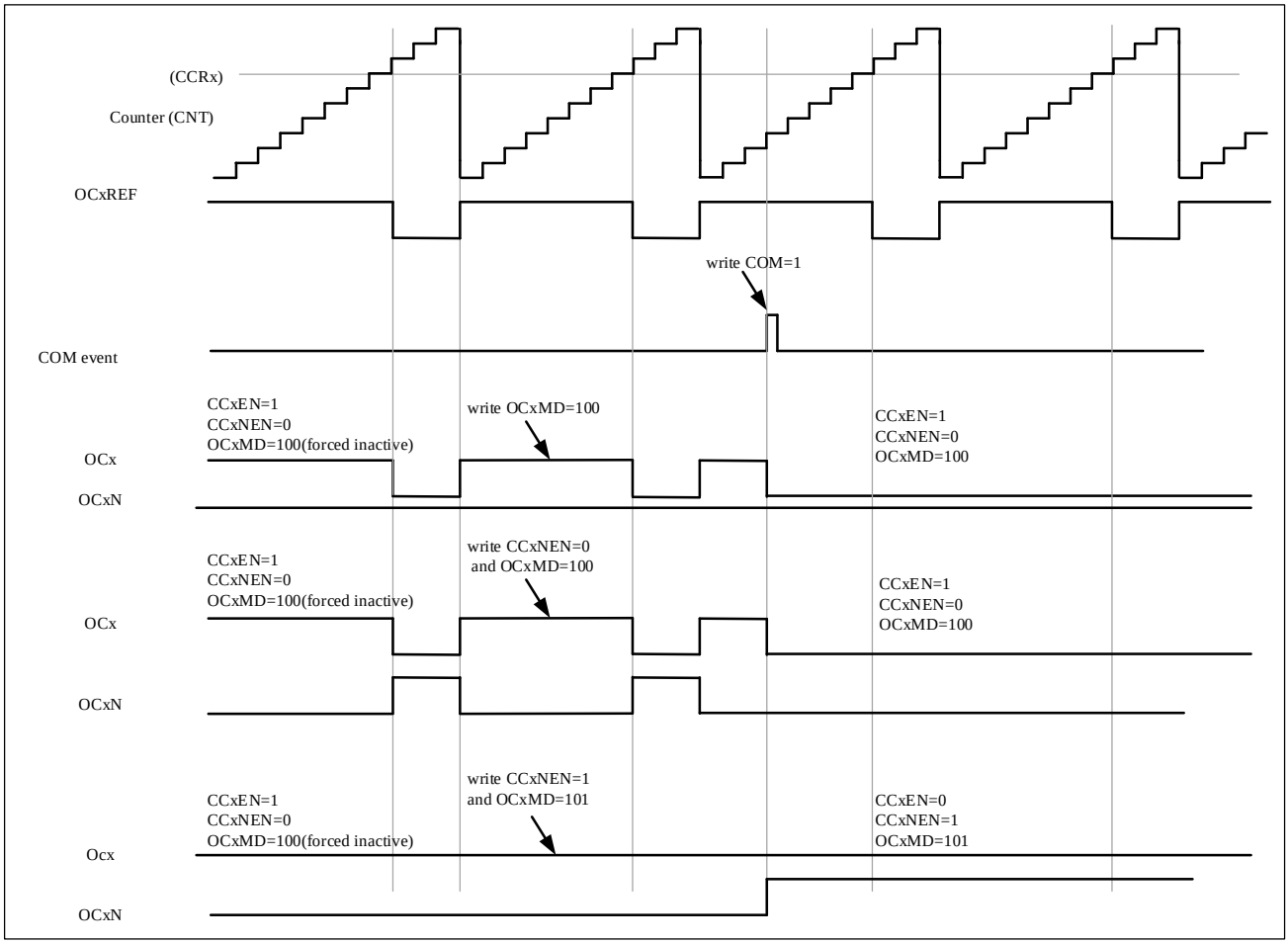
Figure 20-41 Generating Six-Step PWM Using COM as Example (OSSR=1)



20.5.23 Encoder Interface Mode

20.5.23.1 Quadrature Encoder Mode

The encoder uses two inputs, TI1 and TI2 as interfaces, and the counter counts each edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by the hardware TIMx_CTRL1.DIR. There are a total of five modes for quadrature encoder counting :

- Encoder Mode 1: The counter counts only on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘0001’;
- Encoder Mode 2: The counter counts only on the edge of TI2, TIMx_SMCTRL.SMSEL = ‘0010’;
- Encoder Mode 3: The counter counts on the edges of both TI1 and TI2 simultaneously, TIMx_SMCTRL.SMSEL = ‘0011’;
- Encoder Mode 4: When T2 is high level, the counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘1001’;
- Encoder Mode 5: When T1 is high, the counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL = ‘1010’;

The encoder interface is equivalent to using an external clock with direction selection, where the counter continuously

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counts between 0 and the automatic reload value (TIMx_AR.AR [15:0]). Therefore, the automatic reload register TIMx_AR needs to be configured in advance.

Note: Encoder mode and External Clock Mode 2 are not compatible and cannot be selected simultaneously.

The relationship between counting direction and encoder signals is shown in the following table：

Table 20-12 The Relationship Between Counting Direction And Encoder Signals (CC1P=CC2P=0)

Valid Edges	SMSEL[3:0]	The level of the relative signal (TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rising	Falling	Rising	Falling
Counting only on TI1	0001	high	Counting down	Counting up	Don't count	Don't count
		low	Counting up	Counting down	Don't count	Don't count
Counting only on TI2	0010	high	Don't count	Don't count	Counting up	Counting down
		low	Don't count	Don't count	Counting down	Counting up
Counting on both TI1 and TI2	0011	high	Counting down	Counting up	Counting up	Counting down
		low	Counting up	Counting down	Counting down	Counting up
Counting only on TI1 and T2 is high	1001	high	Counting down	Counting up	Don't count	Don't count
		low	Don't count	Don't count	Don't count	Don't count
Counting only on TI2 and T1 is high	1010	high	Don't count	Don't count	Counting up	Counting down
		low	Don't count	Don't count	Don't count	Don't count

The change in the counter value when the counter is in each mode is as follows：

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Figure 20-42 The Encoder Counts Only On TI1

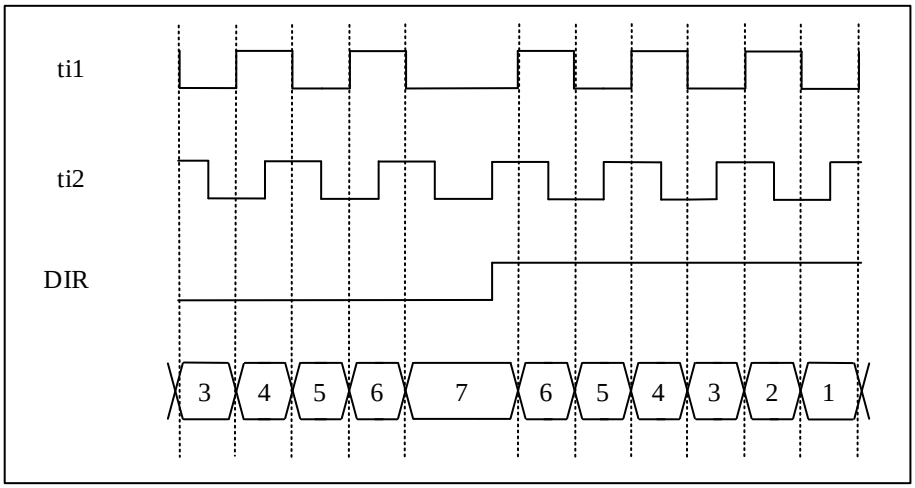

Figure 20-43 The Encoder Counts Only On TI2

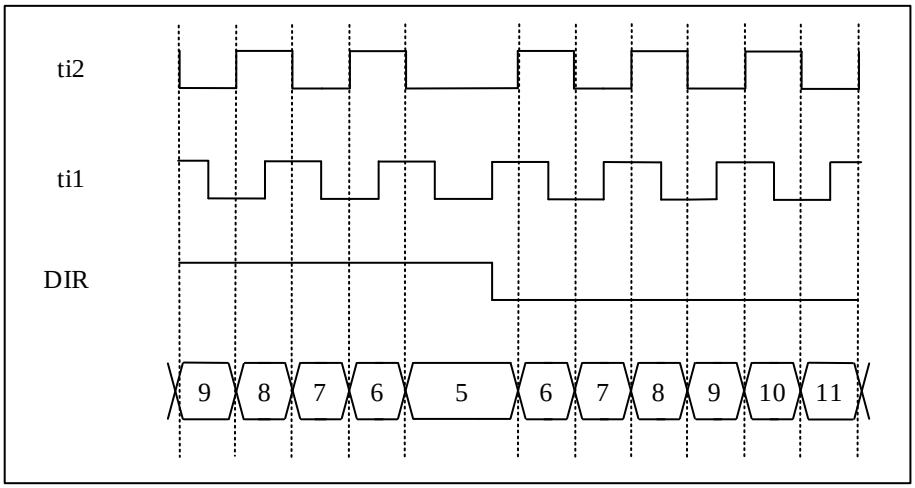

Figure 20-44 The Encoder Counts On Both TI1 and TI2

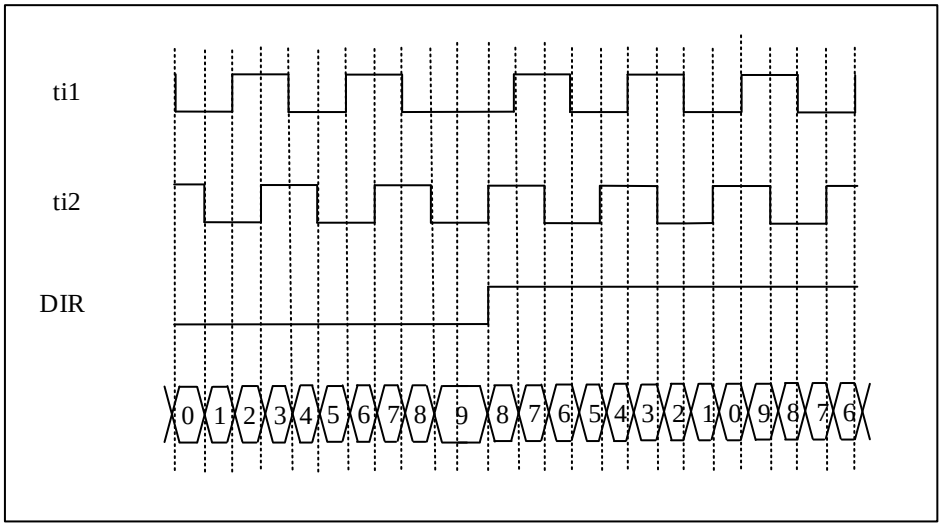

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Figure 20-45 When T2 is high level, the counter counts only on TI1

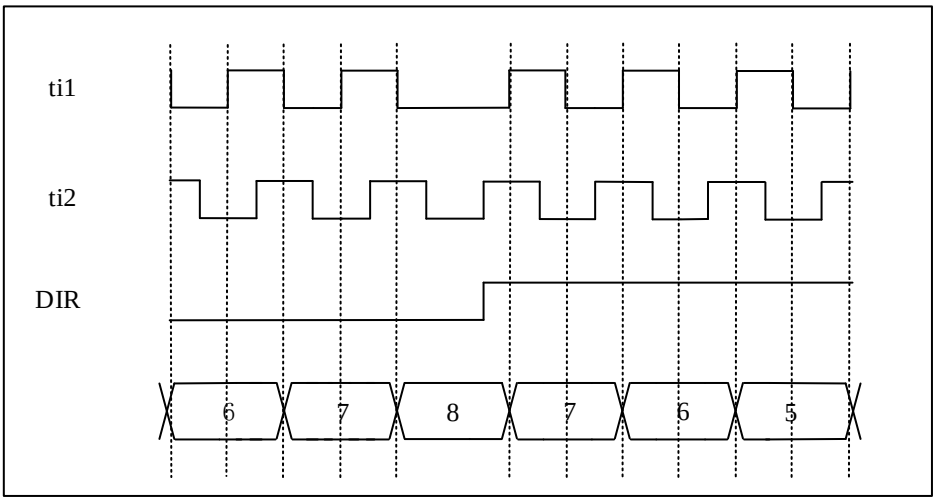
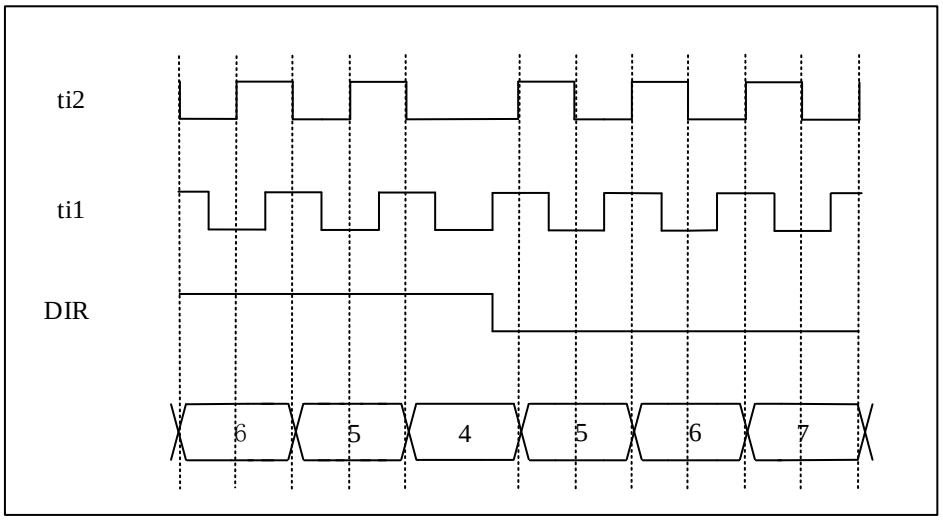


图 20-46 When T1 is high level, the counter counts only on TI2



Here is an example of an encoder that has selected double-edge triggering to suppress input jitter：

1. IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL='01'), IC1FP1 is not inverted (TIMx_CCEN.CC1P='0')；
2. IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL='01'), IC2FP2 is not inverted (TIMx_CCEN.CC2P='0')；
3. Inputs are valid both rising and falling edges (TIMx_SMCTRL.SMSEL='0011') ;
4. Start the counter TIMx_CTRL1.CNTEN='1'；

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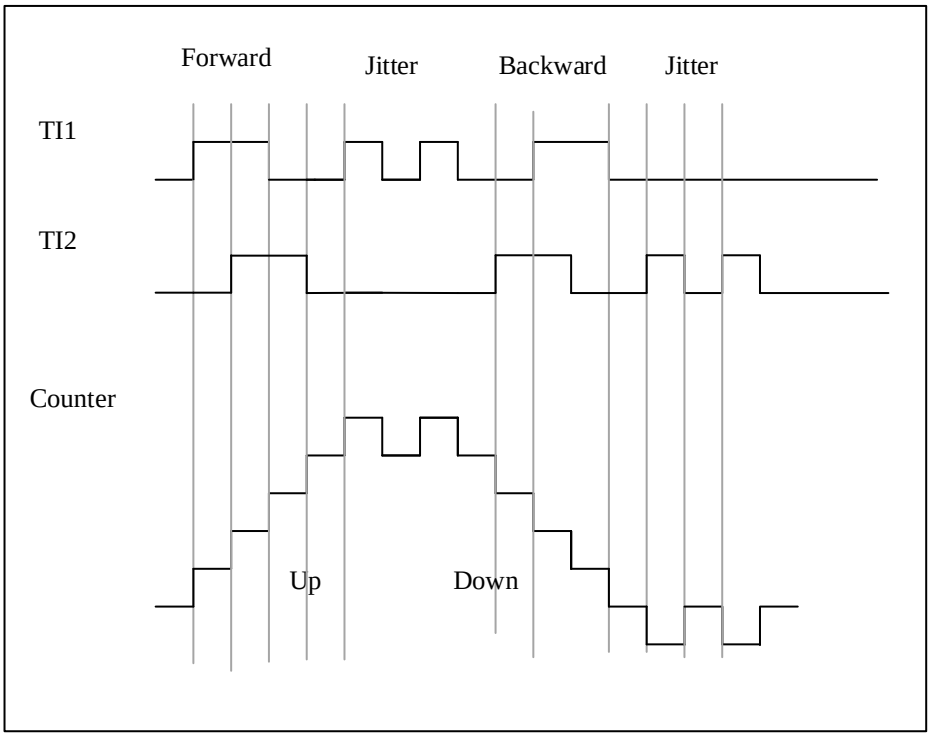
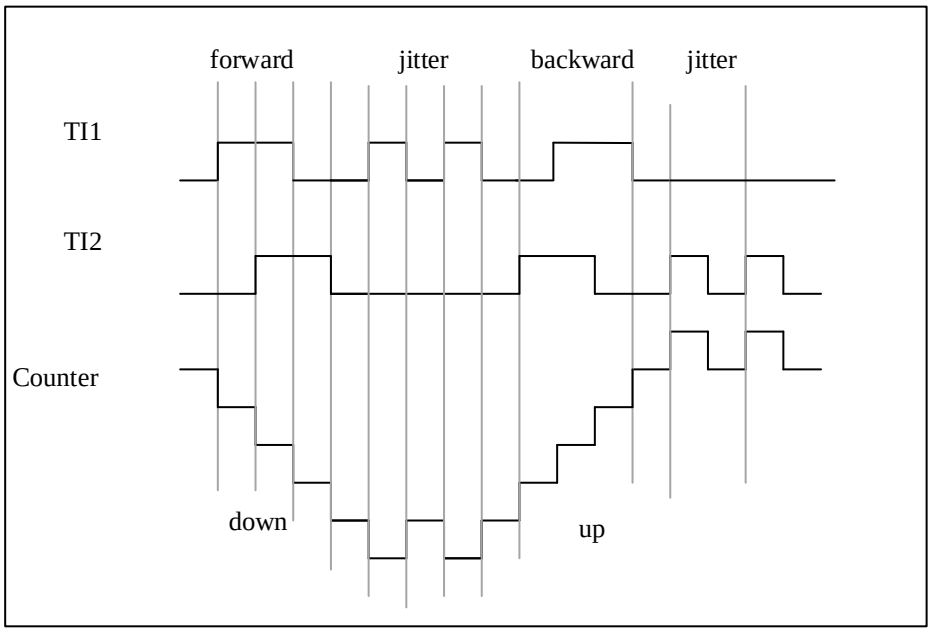
Figure 20-47 Example of counter operation in encoder mode



The following diagram shows an example of counter behavior when IC1FP1 polarity is inverted (CC1P = '1', other configurations are the same as above)

图 20-48 Example of an inverted encoder interface mode with IC1FP1 inverted



20.5.23.2 Pulse Level Encoding Mode

In the pulse level encoding mode, the clock is provided on a single line on TI2, while the counting direction is provided by the TI1 input.

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This mode is enabled through the SMSEL[3:0] in the TIMx_SMCTRL register, as detailed below.

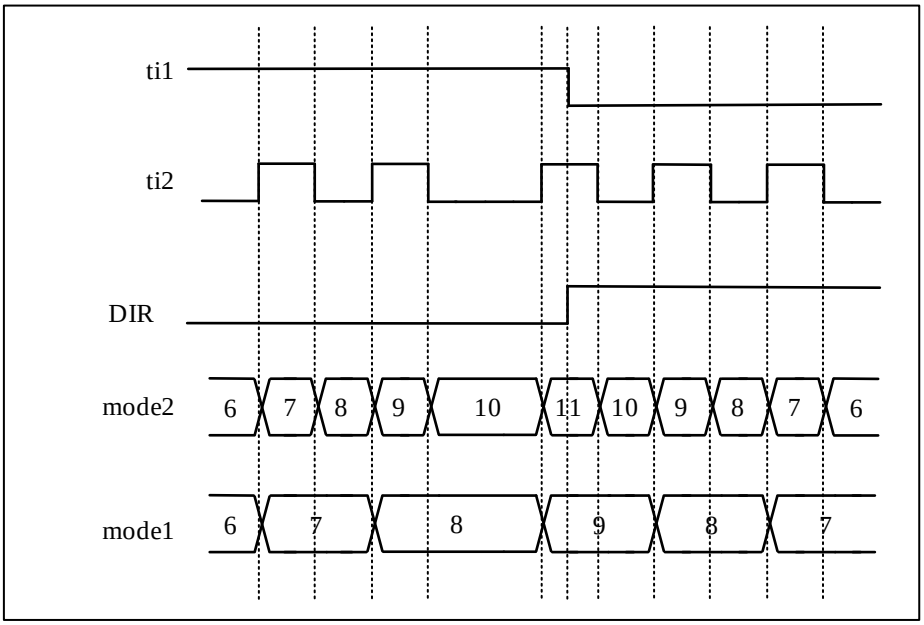
1011：In Pulse Level Encoding Mode 2, the counter is updated on both the rising and falling edges of the clock.

1100：In Pulse Level Encoding Mode 1, the counter is updated on a single clock edge based on the value of CC2P. CC2P = 0 corresponds to counting on the rising edge, CC2P = 1 corresponds to counting on the falling edge.

The polarity of the direction signal of TI1 is set by the CC1P bit. When CC2P = 0, the counter counts up when TI1 is high and counts down when TI1 is low; when CC1P = 1, the counter counts up when TI1 is low and counts down when TI1 is high.

The following diagram is an example with CC1P=CC2P=0 :

Figure 20-49 Pulse Level Encoding Mode (CC1P=CC2P=0)



20.5.23.3 Dual Pulse Encoding Mode

In the Dual Pulse Encoding Mode, the clock is provided on two lines, with only one line provided at a time depending on the direction. This results in one clock line for counting up and one clock line for counting down.

This mode is enabled through the SMSEL[3:0] field in the TIMx_SMCTRL register, as detailed below.

- 1000 : Dual Pulse Encoding Mode 2, the counter is updated on both the rising and falling edges of either of the two clock lines. The CC1P and CC2P bits encode the clock idle state. CCxP=0 corresponds to a high-level idle state, and CCxP=1 corresponds to a low-level idle state.
- 1111：Dual Pulse Encoding Mode 1, the counter updates on a single clock edge based on the values of the CC1P and CC2P bits. CCxP=0 corresponds to the falling edge and high-level state, CCxP=1 corresponds to the rising edge and low-level state.

The table below describes the relationship between counting direction and encoder signals and polarity settings.

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Table 20-13 The relationship between counting direction and encoder signals and polarity settings

Dual Pulse Encoding Mode	SMSEL[3:0]	The level of the relative signal(TI1FP1 for TI2, TI2FP2 for TI1)	TI1FP1 Signal		TI2FP2 Signal	
			Rising	falling	Rising	falling
Mode 2 CCxP=0	1000	High	Counting Down	Counting Down	Counting Up	Counting Up
		Low	Don't Count	Don't Count	Don't Count	Don't Count
Mode 2 CCxP=1	1000	High	Don't Count	Don't Count	Don't Count	Don't Count
		Low	Counting Down	Counting Down	Counting Up	Counting Up
Mode 1 CCxP=0	1111	High	Don't Count	Counting Down	Don't Count	Counting Up
		Low	Don't Count	Don't Count	Don't Count	Don't Count
Mode 1 CCxP=1	1111	High	Don't Count	Don't Count	Don't Count	Don't Count
		Low	Counting Down	Don't Count	Counting Up	Don't Count

The diagram below shows the counting method of the counter in the Dual Pulse Encoding Mode

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Figure 20-50 Dual Pulse Encoding Mode (CC1P=CC2P=0)

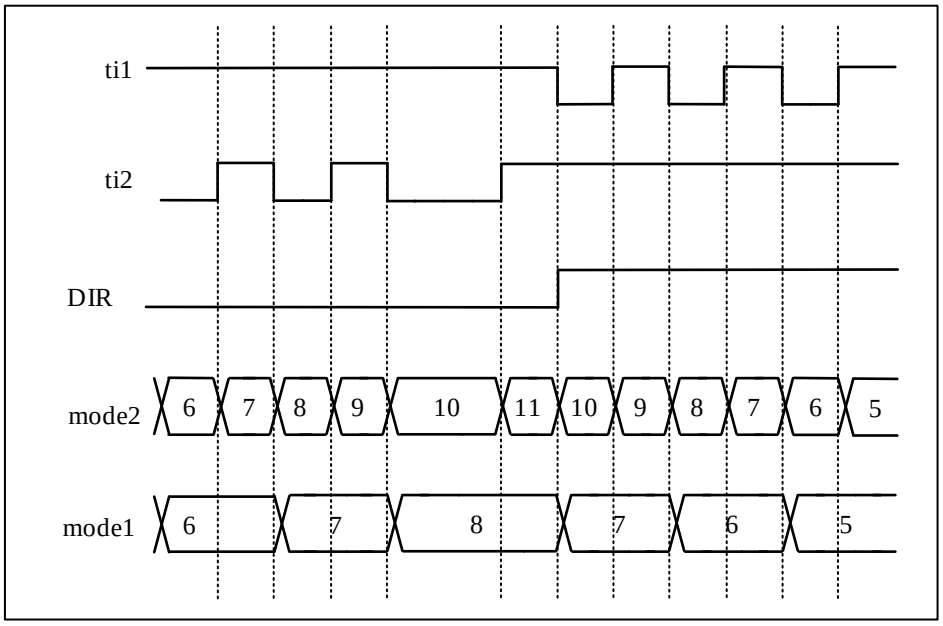
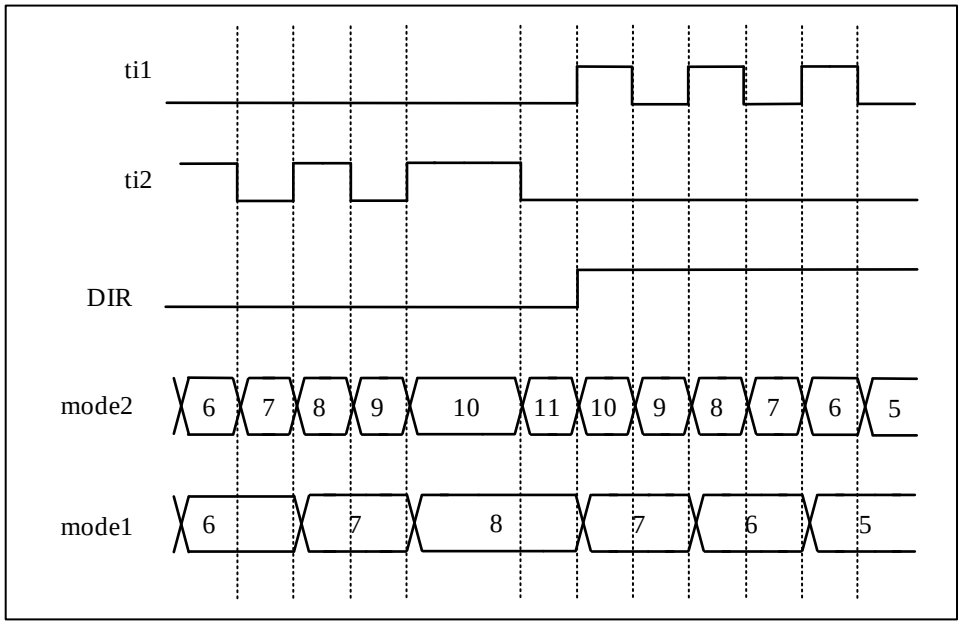


Figure 20-51 Dual Pulse Encoding Mode (CC1P = CC2P = 1)



20.5.24 Interface with Hall Sensors

See Section 18.4.22

20.5.25 UDITF Bit Remapping

The UDITFREMAP bit in the TIMx_CTRL1 register forces the update interrupt flag UDITF to be continuously copied to bit 31 (TIMx_CNT[31]) of the timer counter register, i.e., the UDITFCPY bit. This allows for automatic

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reading of the counter value and the flip of the UDITFCPY flag. In specific scenarios, this can avoid race conditions between background tasks (counter reads) and interrupts (update interrupts), simplifying calculations.

There is no delay between the enablement of the UDITF and UDITFCPY flags.

20.6 GTIMBx (x=1-3) Register Description

For abbreviations used in the register descriptions, please refer to Section 1.1.

These peripheral registers can be operated as half-word (16-bit) or one word (32-bit).

20.6.1 Control Register 1（TIMx_CTRL1）

Offset address : 0x00

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							UDITF REMAP	ASYMME TRIC	Reserved						
							rw	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAMEC CERREN	Reserved	CLRSEL	SMPARER REN	PBKPEN	LBKPEN	ARPEN	ONEPM	CLKD[1:0]		UPDIS	UPRS	CAMSEL[1:0]		DIR	CNTEN
rw		rw	rw	rw	rw	rw	rw	rw		rw	rw	rw		rw	rw

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	UDITFREMAP	UDITF status bit remapping 0: No remapping. The UDITF status bit is not copied to bit 31 of the TIMx_CNT register. 1: Enable remapping. Copy the status bit UDITF to bit 31 of the TIMx_CNT register.
23	ASYMMETRIC	Asymmetric mode enable in center-aligned mode 0: Disable 1: Enable (When TIMx_CTRL1.CAMSEL[1:0] is non-zero, each channel is compared with CCDATx when counting up and with CCDDATx when counting down)
22:16	Reserved	Reserved, the reset value must be maintained.
15	SMECCERREN	SRAM ECC error as brk Enable 0: Disable 1: Enable *Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.*
14	Reserved	Reserved, the reset value must be maintained.
13	CLRSEL	OcxRef clear selection 0: Select the external Ocxclr (TIMx_ETR) signal, specific selection see TIMx_INSEL.ETRS. 1: Select the internal Ocxclr (tim_ocref_clr) signal, specific selection see TIMx_INSEL.CLRS
12	SMPARERREN	SRAM parity error as brk Enable 0: Disable 1: Enable

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Bit Field	Name	Description
		Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.
11	PBKPEN	PVD as brk Enable 0: Disable 1: Enable *Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.*
10	LBKPEN	LockUp as brk Enable (Core Hardfault) 0: Disable 1: Enable *Note: System reset and power-on reset can clear this bit to 0, timer reset cannot clear this bit to 0.*
9	ARPEN	Auto-reload preload enable 0: Disable the shadow register of the TIMx_AR register 1: Enabling the shadow register of the TIMx_AR register
8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs
7:6	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and t_{DTS} (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK_INT}$. 01: $t_{DTS} = 2 \times t_{CK_INT}$ 10: $t_{DTS} = 4 \times t_{CK_INT}$ 11: Reserved, do not use this configuration
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable. UEV will be generated if one of following condition been fulfilled – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: Disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.

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Bit Field	Name	Description
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request： – Counter overflow/underflow – TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
3:2	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting。 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting。 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting。 *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
1	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
0	CNTEN	Counter enable 0: Disable counter; 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

20.6.2 Control Register 2（TIMx_CTRL2）

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												TI1SEL	CCPCTL	CCDSEL	CCUSEL
												rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved			OI5	Reserved	OI4	Reserved	OI3	Reserved	OI2	OI1N	OI1

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rw rw rw rw rw rw rw

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input; 1: TIMx_CH1、TIMx_CH2 and TIMx_CH3 pins are XOR connected to the TI1 input.
18	CCPCTL	Capture/compare preloaded control 0: CCxEN, CCxNEN and OCxMD are not preload; 1: CCxEN, CCxNEN and OCxMD are preload; After setting this bit, they are only updated when the CCUDGN bit is set. *Note: This function only works for channels with complementary outputs*
17	CCDSEL	Capture/Compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent； 1: When an update event occurs, a DMA request for CCx is sent.
16	CCUSEL	Capture/Compare control update selection 0: If the Capture/Compare control bits are preloaded (CCPCTL=1), they can only be updated by setting the CCUDGN bit ; 1: If the Capture/compare control bits are preloaded (CCPCTL=1), they can be updated by setting the CCUDGN bit or by a rising edge on TRGI. *Note: This bit only applies to channels with complementary outputs*
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 0000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 0001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high。 When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). 0010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler 0011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 0100: Compare - OC1REF signal is used as the trigger output (TRGO). 0101: Compare – OC2REF signal is used as the trigger output (TRGO). 0110: Compare – OC3REF signal is used as the trigger output (TRGO). 0111: Compare – OC4REF signal is used as the trigger output (TRGO).

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Bit Field	Name	Description
		1xxx：Reserved.
11:9	Reserved	Reserved, the reset value must be maintained
8	OI5	Output Idle State 5 (OC5 output). See bit OI1.
7	Reserved	Reserved, the reset value must be maintained
6	OI4	Output Idle State 4 (OC4 output). See bit OI1.
5	Reserved	Reserved, the reset value must be maintained
4	OI3	Output Idle State 3 (OC3 output). See bit OI1.
3	Reserved	Reserved, the reset value must be maintained
2	OI2	Output Idle State 2 (OC2 output). See bit OI1.
1	OI1N	Output Idle state 1N 0: when MOEN=0, OC1N=0 after the dead time; 1: when MOEN=0, OC1N=1 after the dead time; *Note: Once the TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*
0	OI1	Output Idle state 1 0: when MOEN=0, If OC1N is implemented, then OC1=0 after the dead time; 1: when MOEN=0, If OC1N is implemented, then OC1=1 after the dead time; *Note: Once the TIMx_BKDT.LCKCFG level 1, 2, or 3 has been set, this bit cannot be modified.*

20.6.3 Status Register（TIMx_STS）

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										SBITF	Reserved	BITF	TITF	COMITF	UDITF
										rc_w0		rc_w0	rc_w0	rc_w0	rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved			CC5ITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF
				rc_w0	rc_w0	rc_w0	rc_w0				rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	SBITF	System break interrupt flag Once the system break input is active, it is set to '1' by hardware. If the system break input is inactive, this bit can be cleared to '0' by software. 0: No break event generated; 1: Valid level detected on system break input;
20	Reserved	Reserved, the reset value must be maintained
19	BITF	Break 1 interrupt flag Once break 1 input is active, it is set to '1' by hardware. If break 1 input is inactive, this bit can

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Bit Field	Name	Description
		be cleared to '0' by software. 0: No break 1 event generated; 1: Valid level detected on break 1 input;
18	TITF	Trigger interrupt flag When a trigger event occurs (valid edge detected at the TRGI input terminal when the slave mode controller is in a mode other than gated mode, or any edge in gated mode), it is set to '1' by hardware. It can be cleared to '0' by software. 0: No trigger event generated; 1: Interrupt triggered waiting for response;
17	COMITF	COM interrupt flag Once a COM event occurs (when the capture/compare control bits: CCxEN, CCxNEN, OCxMD have been updated), this bit is set to '1' by hardware. It is cleared to '0' by software. 0: No COM event generated; 1: COM interrupt waiting for response;
16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, And the repetition counter value overflow or underflow (generating an update event UEV when the repetition counter equals 0) –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT。 –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (Refer to the TIMx_SMCTRL register description) This bit is cleare by software。 0: No update event occurred; 1: Update interrupt occurred;
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4OCF	Capture/Compare 4 overcapture flag Refer to CC1OCF description.
10	CC3OCF	Capture/Compare 3 overcapture flag Refer to CC1OCF description.
9	CC2OCF	Capture/Compare 2 overcapture flag Refer to CC1OCF description.
8	CC1OCF	Capture/Compare 1 overcapture flag This flag can only be set to 1 by hardware when the corresponding channel is configured for input capture. Writing 0 can clear this bit 0: No repeated capture generated. 1: When the value of the counter is captured into the TIMx_CCDAT1 register, the status of CC1ITF is already '1'
7:5	Reserved	Reserved, the reset value must be maintained
4	CC5ITF	Capture/Compare 5 interrupt flag Refer to CC1ITF description.

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Bit Field	Name	Description
3	CC4ITF	Capture/Compare 4 interrupt flag Refer to CC1ITF description.
2	CC3ITF	Capture/Compare 3 interrupt flag Refer to CC1ITF description.
1	CC2ITF	Capture/Compare 2 interrupt flag Refer to CC1ITF description.
0	CC1ITF	Capture/Compare 1 interrupt flag **If channel CC1 is configured as an output mode:** Except in center-aligned mode, when the counter value is equal to the comparison value, this bit is set by hardware (refer to the TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred; 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1 When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, if the counter overflows (in upcounting and up/downcounting modes) and underflows in downcounting mode, the TIMx_STS.CC1ITF bit will be set to '1'. **If channel CC1 is configured in input mode :** When a capture event occurs, this bit is set by hardware. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred; 1: Input capture occurred; The counter value has been captured in TIMx_CCDAT1. An edge with the same selected polarity has been detected on IC1.

20.6.4 Event Generation Registers (TIMx_EVTGEN)

Offset address : 0x0C

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				BGN	TGN	CCUDGN	UDGN	Reserved				CC4GN	CC3GN	CC2GN	CC1GN
				w	w	w	w					w	w	w	w

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	BGN	Break 1 generation When set by the software, this bit can generate a break 1 event. At this time, TIMx_BKDT.MOEN = 0 and TIMx_STS.BITF = 1. If the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware.

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Bit Field	Name	Description
		0: No action 1: Generated Break 1 event
10	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
9	CCUDGN	Capture/Compare control update generation This bit is set by software. If TIMx_CTRL2.CCPCTL=1 at this time, it allows updating the CCxEN, CCxNEN, and OCxMD bits. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event *Note: This bit is only valid for channels with complementary outputs*
8	UDGN	Update generation This bit is set by software and automatically cleared by hardware. This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event
7:4	Reserved	Reserved, the reset value must be maintained.
3	CC4GN	Capture/Compare 4 generation Refer to CC1GN description
2	CC3GN	Capture/Compare 3 generation Refer to CC1GN description
1	CC2GN	Capture/Compare 2 generation Refer to CC1GN description
0	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. **When the corresponding channel of CC1 is in output mode:** The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. **When the corresponding channel of CC1 is in input mode:** TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull

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Bit Field	Name	Description
		TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event

20.6.5 Slave Mode Control（TIMx_SMCTRL）

Offset address：0x10

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								OCREFCLRF[3:0]				OCREF CLRP	Reserved		MSMD
								rw				rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTF[3:0]				EXTP	EXCEN	EXTPS		SMSEL[3:0]				Reserved	TSEL[2:0]		
rw				rw	rw	rw		rw					rw		

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:20	OCREFCLRF	tim_ocref_clr signal filter These bits are used to define the sampling frequency of the tim_ocref_clr signal and the bandwidth of the tim_ocref_clr digital filter. In fact, the digital filter is an event counter that generates a validated output after recording a continuous N events. 0000: No filter, sampled at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS/8}$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS/8}$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS/16}$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS/16}$, N=6 0100: $f_{SAMPLING}=f_{DTS/2}$, N=6 1100: $f_{SAMPLING}=f_{DTS/16}$, N=8 0101: $f_{SAMPLING}=f_{DTS/2}$, N=8 1101: $f_{SAMPLING}=f_{DTS/32}$, N=5 0110: $f_{SAMPLING}=f_{DTS/4}$, N=6 1110: $f_{SAMPLING}=f_{DTS/32}$, N=6 0111: $f_{SAMPLING}=f_{DTS/4}$, N=8 1111: $f_{SAMPLING}=f_{DTS/32}$, N=8
19	OCREFCLRP	tim_ocref_clr signal polarity This bit selects whether to use tim_ocref_clr or the invert of tim_ocref_clr as the trigger operation 0: tim_ocref_clr is active high or on the rising edge; 1: tim_ocref_clr is active low or on the falling edge;
18:17	Reserved	Reserved, the reset value must be maintained.
16	MSMD	Master/slave mode 0: No action;

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		1: The event on the trigger input (TRGI) is delayed to allow perfect synchronization between the current timer (via TRGO) and its slave timers. This is very useful when multiple timers need to be synchronized to a single external event;
15:12	EXTF[3:0]	External trigger filter These bits are used to define the sampling frequency of the ETRP signal and the bandwidth of the ETRP digital filter. In fact, the digital filter is an event counter that generates a validated output after recording a continuous N events. 0000: No filter, sampled at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS/8}$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS/8}$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS/16}$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS/16}$, N=6 0100: $f_{SAMPLING}=f_{DTS/2}$, N=6 1100: $f_{SAMPLING}=f_{DTS/16}$, N=8 0101: $f_{SAMPLING}=f_{DTS/2}$, N=8 1101: $f_{SAMPLING}=f_{DTS/32}$, N=5 0110: $f_{SAMPLING}=f_{DTS/4}$, N=6 1110: $f_{SAMPLING}=f_{DTS/32}$, N=6 0111: $f_{SAMPLING}=f_{DTS/4}$, N=8 1111: $f_{SAMPLING}=f_{DTS/32}$, N=8
11	EXTP	External trigger polarity This bit selects whether to use tim_etr_in or the invert of tim_etr_in as the trigger operation 0：tim_etr_in is active high or on the rising edge; 1：tim_etr_in is active low or on the falling edge;
10	EXCEN	External clock enable This bit enables External Clock Mode 2. When enabled, the counter is driven by any valid edge on the ETRF signal. 0: Disable External Clock Mode 2; 1: Enable External Clock Mode 2; *Note 1: When External Clock Mode 1 and External Clock Mode 2 are enabled simultaneously, the input for external clock is ETRF.* *Note 2: The following slave modes can be used simultaneously with External Clock Mode 2: Reset Mode, Gated Mode, and Trigger Mode; however, TRGI cannot be connected to ETRF (TIMx_SMCTRL.TSEL≠'111').* *Note 3: Setting the TIMx_SMCTRL.EXCEN bit to select External Clock Mode 1 and connect TRGI to ETRF (TIMx_SMCTRL.SMSEL=111 and TIMx_SMCTRL.TSEL=111) has the same effect.*
9:8	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of the TIMxCLK frequency. When using a faster external clock input, a prescaler can be used to reduce the frequency of ETRP. 00: Disable prescaling; 01: ETRP frequency divided by 2; 10: ETRP frequency divided by 4; 11: ETRP frequency divided by 8;
7:4	SMSEL[3:0]	Slave mode selection When an external signal is selected, the effective edge of the trigger signal (TRGI) is related to the selected external input polarity (refer to the description of the input control register and control register) 0000: Disable Slave Mode - If CNTEN = 1, the prescaler is directly driven by the internal clock。

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		0001: Encoder Mode 1 - The counter counts up/down on the edges of TI1FP1 based on the level of TI2FP2. 0010: Encoder Mode 2 - The counter counts up/down on the edges of TI2FP2 based on the level of TI1FP1. 0011: Encoder Mode 3 - The counter counts up/down on the edges of TI1FP1 and TI2FP2 based on the input level of another signal. 0100: Reset Mode - On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow registers are updated. 0101: Gated Mode - When the trigger input (TRGI) is high, the counter clock is enabled. Once the trigger input becomes low, the counter stops (but does not reset). The start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts on the rising edge of the trigger input TRGI (but does not reset), only the start of the counter is controlled. 0111: External Clock Mode 1 - The rising edge of the selected trigger input (TRGI) drives the counter. 1000: Dual input pulse encoder mode 2. 1001：Quadrature Encoder Mode 4 - The counter counts up/down on the edges of TI1FP1 based on the level of TI2FP2. The counting edge is selected via CC1P. 1010：Quadrature Encoder Mode 5 - The counter counts up/down on the edges of TI2FP2 based on the level of TI1FP1. The counting edge is selected via CC2P 1011: Pulse Width Encoder Mode 2. 1100: Pulse Width Encoder Mode 1. The counting edge of TI2FP2 is set via CC2P 1101: Combined Gated + Reset Mode - When the trigger input (TRGI) is high, the counter clock is enabled. Once the trigger input becomes low, the counter stops (and resets). The start and stop of the counter are both controlled。 1110: Combined Reset + Trigger Mode - The counter starts and resets on the rising edge of the trigger input TRGI, with only the start of the counter being controlled 1111: Dual Input Pulse Encoder Mode 1. The counting sensitive edges of TI1FP1 and TI2FP2 are set via CC1P and CC2P。 Note: Do not use Gated Mode when TI1F_ED is selected as the trigger input (TSEL=100). This is because TI1F_ED outputs a pulse every time TI1F changes, whereas Gated Mode checks the level of the trigger input。
3	Reserved	Reserved, the reset value must be maintained.
2:0	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input for synchronizing the counter 0xx: Internal Trigger (ITRx) selects the ITR signal source based on TIMx_INSEL 100: Edge Detector for TI1 (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2)

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		111: External Trigger input（ETRF） *Note: These bits can only be changed when not in use (e.g., SMSEL=000) to avoid incorrect edge detection when changed*

20.6.6 DMA/Interrupt Enable Register（TIMx_DINTEN）

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									COMIEN	TDEN	COMDEN	UDEN	BIEN	TIEN	UIEN
									rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CC4DEN	CC3DEN	CC2DEN	CC1DEN	Reserved				CC4IEN	CC3IEN	CC2IEN	CC1IEN
				rw	rw	rw	rw					rw	rw	rw	rw

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	COMIEN	COM interrupt enable 0: Disable COM interrupt; 1: Enable COM interrupt;
21	TDEN	Trigger DMA request enable 0: Disable trigger DMA request; 1: Enable trigger DMA request.
20	COMDEN	COM DMA request enable 0: Disable COM DMA request; 1: Enable COM DMA request.
19	UDEN	Update DMA request enable 0: Disable update DMA request; 1: Enable update DMA request.
18	BIEN	Break interrupt enable 0: Disable break interrupt; 1: Enable break interrupt.
17	TIEN	Trigger interrupt enable 0: Disable trigger interrupt; 1: Enable trigger interrupt.
16	UIEN	Update interrupt enable 0: Disable update interrupt; 1: Enable update interrupt.
15:12	Reserved	Reserved, the reset value must be maintained
11	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable Capture/Compare 4 DMA request; 1: Enable Capture/Compare 4 DMA request

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Bit Field	Name	Description
10	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable Capture/Compare 3 DMA request; 1: Enable Capture/Compare 3 DMA request
9	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable Capture/Compare 2 DMA request; 1: Enable Capture/Compare 2 DMA request
8	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable Capture/Compare 1 DMA request; 1: Enable Capture/Compare 1 DMA request
7:4	Reserved	Reserved, the reset value must be maintained
3	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt; 1: Enable capture/compare 4 interrupt.
2	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt; 1: Enable capture/compare 3 interrupt.
1	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt; 1: Enable capture/compare 2 interrupt.
0	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt; 1: Enable capture/compare 1 interrupt.

20.6.7 Capture/Compare Mode Register 1（TIMx_CCMOD1）

Offset address: 0x18

Reset value: 0x0000 0000

The channel can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The functions of the other bits in this register are different in input and output modes. OCx describes the function of the channel in output mode, while ICx describes the function of the channel in input mode. Therefore, it is important to note that the functionality of the same bit is different in output and input modes。

Output Compare Mode：

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													OC2MD3	OC1MD3	Reserved
													rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2MD[2:0]			OC2CEN	OC2FEN	OC2PEN	CC2SEL[1:0]		OC1MD[2:0]			OC1CEN	OC1FEN	OC1PEN	CC1SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

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Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	OC2MD3	Used with OC2MD, see the description of OC2MD for details.
17	OC1MD3	Used with OC1MD, see the description of OC1MD for details.
16	Reserved	Reserved, the reset value must be maintained
15:13	OC2MD[2:0]	Output Compare 2 mode OC2MD3 is used with OC2MD to manage the output reference signal OC2REF, which determines the values of OC2 and OC2N. The effective levels of OC2 and OC2N depend on the TIMx_CCEN.CC2P and TIMx_CCEN.CC2NP bits when it is high level effective. The 4-bit signals {OC2MD_3, OC2MD} correspond to the following Output Compare 1 modes: 0000: Frozen. The comparison between the TIMx_CCDAT2 register and the counter TIMx_CNT has no effect on the OC2REF signal. 0001: Set channel 2 to the active level when a match occurs. When TIMx_CCDAT2 = TIMx_CNT, the OC2REF signal will be forced to a high level. 0010: Set channel 2 to the inactive level when a match occurs. When TIMx_CCDAT2 = TIMx_CNT, the OC2REF signal will be forced to a low level. 0011: Toggle. When TIMx_CCDAT2 = TIMx_CNT, the OC2REF signal will be toggled. 0100: Force Inactive Level. The OC2REF signal is forced to a low level. 0101: Force Active Level. The OC2REF signal is forced to a high level. 0110: PWM Mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT2, channel 2's OC2REF signal is high; otherwise, it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT2, channel 2's OC2REF signal is low; otherwise, it is high. 0111: PWM Mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT2, channel 2's OC2REF signal is low; otherwise, it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT2, channel 2's OC2REF signal is high; otherwise, it is low. 1000: Retriggerable Single Pulse Mode 1 - In the up-counting mode, the channel is in the active state until a trigger event is detected (on the TRGI signal). Then, a comparison is made in PWM mode 1, and the channel will become active again on the next update. In the down-counting mode, the channel is in the inactive state until a trigger event is detected (on the TRGI signal). Then, a comparison is made in PWM mode 1, and the channel will become inactive again on the next update. 1001: Retriggerable Single Pulse Mode 2 - In the up-counting mode, the channel is in the inactive state until a trigger event is detected (on the TRGI signal). Then, a comparison is made in PWM mode 2, and the channel will become inactive again on the next update. In the down-counting mode, the channel is in the active state until a trigger event is detected (on the TRGI signal). Then, a comparison is made in PWM mode 2, and the channel will become active again on the next update. 1010-1101：Reserved 1110: Combined PWM Mode 1 - OC2REF behaves the same as in PWM Mode 1. OC2REFC is the logical OR of OC1REF and OC2REF. 1111: Combined PWM Mode 2 - OC2REF behaves the same as in PWM Mode 2. OC2REFC is the logical AND of OC1REF and OC2REF。

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Bit Field	Name	Description
		Note: In PWM Mode 1 or PWM Mode 2, the OC2REF level changes only when the comparison result changes or when the output compare mode switches from frozen mode to PWM mode.
12	OC2CEN	Output Compare 2 clear enable
11	OC2FEN	Output Compare 2 fast enable
10	OC2PEN	Output Compare 2 preload enable
9:8	CC2SEL[1:0]	Capture/Compare 2 selection This bit defines the direction (input/output) of the channel and the selection of the input pin： 00: CC2 channel is configured as an output; 01: CC2 channel is configured as an input, IC2 is mapped to TI2; 10: CC2 channel is configured as an input, IC2 is mapped to TI1; 11: CC2 channel is configured as an input, IC2 is mapped to TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). *Note: CC2SEL is writable only when the channel is disabled (CC2EN=0 in the TIMx_CCEN register).*
7:5	OC1MD[2:0]	Output Compare 1 mode OC1MD3 and OC1MD are used together to control the output reference signal OC1REF, which determines the values of OC1 and OC1N, when high-level effectiveness. The effective level of OC1 and OC1N depends on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. The 4-bit signal {OC1M_3, OC1M} corresponds to the following output comparison mode 1: 0000: Freeze. The comparison between the TIMx_CCDAT1 register and the TIMx_CNT counter has no effect on the OC1REF signal. 0001: Setting channel 1 to the effective level when matched. When TIMx_CCDAT1=TIMx_CNT, the OC1REF signal will be forced to a high level. 0010: Setting channel 1 to the ineffective level when matched. When TIMx_CCDAT1=TIMx_CNT, the OC1REF signal will be forced to a low level. 0011: Toggle. When TIMx_CCDAT1=TIMx_CNT, the OC1REF signal will be toggled. 0100: Force inactive level. The OC1REF signal is forced to a low level. 0101: Force active level. The OC1REF signal is forced to a high level. 0110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, the OC1REF signal of channel 1 is high, otherwise low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, the OC1REF signal of channel 1 is low, otherwise high. 0111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, the OC1REF signal of channel 1 is low, otherwise high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, the OC1REF signal of channel 1 is high, otherwise low. 1000: Retriggerable single pulse mode 1 - In the upcounting mode, the channel is in the active state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 1 comparison is done, the channel will return to the active state at the next update. In the downcounting mode, the channel is in the inactive state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 1 comparison is done, the channel will return to the inactive state at the

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Bit Field	Name	Description
		next update. 1001: Retriggerable single pulse mode 2 - In the upcounting mode, the channel is in the inactive state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 2 comparison is done, the channel will return to the inactive state at the next update. In the downcounting mode, the channel is in the active state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 2 comparison is done, the channel will return to the active state at the next update. 1010-1101：Reserved 1110: Combined PWM mode 1 - OC1REF behaves the same as in PWM mode 1. OC1REFC is the logical OR operation result of OC1REF and OC2REF. 1111: Combined PWM mode 2 - OC1REF behaves the same as in PWM mode 2. OC1REFC is the logical AND operation result of OC1REF and OC2REF. *Note: In PWM mode 1 or PWM mode 2, the OC1REF level only changes when the comparison result changes or when the output comparison mode switches from freeze mode to PWM mode.*
4	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by the tim_ocref_clr_in input; 1: Once a high level is detected on the tim_ocref_clr_in input (The tim_ocref_clr_in is controlled by the TIMx_CTRL1.CLRSEL source), OC1REF will be set to 0.
3	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to trigger input events. 0: Based on the values of the counter and CCDAT1, CC1 operates normally even if the trigger is enabled. When the trigger input has a valid edge, the minimum delay for activating the CC1 output is 5 clock cycles. 1: The effect of a valid edge input to the trigger is as if a comparison match occurred. Therefore, OC1 is set to the comparison level regardless of the comparison result. The delay between the valid edge of the sampling trigger and the CC1 output is shortened to 3 clock cycles. OCxFEN only works when the channel is configured in PWM1 or PWM2 mode
2	OC1PEN	Output Compare 1 preload enable 0: Disable the preload function of the TIMx_CCDAT1 register. Support writing to the TIMx_CCDAT1 register at any time, and the written value takes effect immediately. 1: Enable the preload function of the TIMx_CCDAT1 register. Only read and write operations are performed on the preload register. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the shadow register. *Note: Only when TIMx_CTRL1.ONEPM=1 (in single pulse mode) can the PWM mode be used without validating the preload register; otherwise, other behaviors cannot be predicted.*
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These 2 bits define the direction (input/output) of the channel and the selection of the input pin： 00: CC1 channel is configured as an output； 01: CC1 channel is configured as an input, and IC1 is mapped to TI1；

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Bit Field	Name	Description
		10: CC1 channel is configured as an input, and IC1 is mapped to TI2； 11: CC1 channel is configured as an input, and IC1 is mapped to TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). *Note: CC1SEL is only writable when the channel is disabled (CC1EN = 0 in the TIMx_CCEN register)*

Input capture mode :

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC2F[3:0]	Input capture 2 filter
11:10	IC2PSC[1:0]	Input capture 2 prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These 2 bits define the direction of the channel (input/output) and the selection of the input pin： 00: CC2 channel is configured as an output； 01: CC2 channel is configured as an input, and IC2 is mapped to TI2； 10: CC2 channel is configured as an input, and IC2 is mapped to TI1； 11: CC2 channel is configured as an input, and IC2 is mapped to TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). *Note: CC2SEL is only writable when the channel is disabled (CC2EN = 0 in the TIMx_CCEN register).*
7:4	IC1F[3:0]	Input capture 1 filter These bits define the sampling frequency of the TI1 input and the length of the digital filter. The digital filter consists of an event counter, which generates an output change after counting N events： 0000: No filter, sampled at f_{DTS} 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 0001: $f_{SAMPLING}=f_{CK_INT}$, N=2 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 0010: $f_{SAMPLING}=f_{CK_INT}$, N=4 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 0011: $f_{SAMPLING}=f_{CK_INT}$, N=8 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

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3:2	IC1PSC[1:0]	Input capture 1 prescaler These 2 bits define the prescaler factor for the CC1 input (IC1). Once TIMx_CCEN.CC1EN=0, the prescaler is reset. 00: No prescaler, each edge detected on the capture input triggers a capture; 01: Capture is triggered every 2 events; 10: Capture is triggered every 4 events; 11: Capture is triggered every 8 events.
1:0	CC1SEL[1:0]	Capture/Compare 1 Selection These 2 bits define the direction of the channel (input/output) and the selection of the input pin: 00: CC1 channel is configured as an output; 01: CC1 channel is configured as an input, and IC1 is mapped to TI1; 10: CC1 channel is configured as an input, and IC1 is mapped to TI2; 11: CC1 channel is configured as an input, and IC1 is mapped to TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). *Note: CC1SEL is only writable when the channel is disabled (CC1EN = 0 in the TIMx_CCEN register).*

20.6.8 Capture/Compare Mode Register 2（TIMx_CCMOD2）

Offset address：0x1C

Reset value：0x0000 0000

Refer to the description of the CCMOD1 register above

output compare mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													OC4MD3	OC3MD3	Reserved
													rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4MD[2:0]			OC4CEN	OC4FEN	OC4PEN	CC4SEL[1:0]		OC3MD[2:0]			OC3CEN	OC3FEN	OC3PEN	CC3SEL[1:0]	
rw			rw	rw	rw	rw		rw			rw	rw	rw	rw	

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	OC4MD3	Used with OC4MD, refer to the description of OC4MD for details
17	OC3MD3	Used with OC3MD, refer to the description of OC3MD for details
16	Reserved	Reserved, the reset value must be maintained
15:13	OC4MD[2:0]	Output compare 4 mode OC4MD3 and OC4MD define the action of the output reference signal OC4REF, which determines the value of OC4. OC4REF is active at high level, and the effective level of OC4 depends on the CC4P bit. The 4-bit signal {OC4MD3, OC4MD} corresponds to the following output compare 4 modes： 0000: Freeze. The comparison between the output compare register TIMx_CCDAT4 and the

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Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
		counter TIMx_CNT does not affect OC4REF; 0001: Set channel 4 to active level when a match occurs. When the value of counter TIMx_CNT is the same as the capture/compare register 4 (TIMx_CCDAT4), force OC4REF to high. 0010: Set channel 4 to an inactive level when a match occurs. When the value of counter TIMx_CNT is the same as the capture/compare register 4 (TIMx_CCDAT4), force OC4REF to low. 0011: Toggle. When TIMx_CCDAT4 = TIMx_CNT, toggle the level of OC4REF. 0100: Force to an inactive level. Force OC4REF to low. 0101: Force to an active level. Force OC4REF to high. 0110: PWM mode 1 - During up-counting, channel 4 is at an active level when TIMx_CNT < TIMx_CCDAT3, otherwise it is at an inactive level. During down-counting, channel 4 is at an inactive level (OC4REF=0) when TIMx_CNT > TIMx_CCDAT4, otherwise it is at an active level (OC4REF=1). 0111: PWM mode 2 - During up-counting, channel 4 is at an inactive level when TIMx_CNT < TIMx_CCDAT4, otherwise it is at an active level. During down-counting, channel 4 is at an active level when TIMx_CNT > TIMx_CCDAT4, otherwise it is at an inactive level. 1000: Retriggerable single pulse mode 1 - In the up-counting mode, channel 4 is in the active state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 1, channel 4 will return to the active state on the next update. In the down-counting mode, channel 4 is in the inactive state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 1, channel 4 will return to the inactive state on the next update。 1001: Retriggerable single pulse mode 2 - In the up-counting mode, channel 4 is inactive until a trigger event is detected (on the TRGI signal). Then, in PWM mode 2 comparison, channel 4 will return to the inactive state on the next update. In the down-counting mode, channel 4 is active until a trigger event is detected (on the TRGI signal). Then, in PWM mode 2 comparison, channel 4 will return to the active state on the next update. 1010-1101：Reserved 1110: Combined PWM mode 1 - OC4REF behaves the same as in PWM mode 1. OC4REFC is the logical OR operation result of OC4REF and OC3REF. 1111: Combined PWM mode 2 - OC4REF behaves the same as in PWM mode 2. OC4REFC is the logical AND operation result of OC4REF and OC3REF. *Note: In PWM mode 1 or PWM mode 2, the OC4REF level changes only when the comparison result changes or when switching from freeze mode to PWM mode in the output compare mode.*
12	OC4CEN	Output compare 4 clear enable
11	OC4FEN	Output compare 4 fast enable
10	OC4PEN	Output compare 4 preload enable

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Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These 2 bits define the direction (input/output) of the channel and the selection of the input pin： 00: CC4 channel is configured as an output; 01: CC4 channel is configured as an input, with IC4 mapped on TI4; 10: CC4 channel is configured as an input, with IC4 mapped on TI3； 11: CC4 channel is configured as an input, with IC4 mapped on TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). Note: CC4SEL is writable only when the channel is disabled (CC4EN=0 in the TIMx_CCEN register).
7:5	OC3MD[2:0]	Output compare 3 mode OC3MD3 and OC3MD define the action of the output reference signal OC3REF, which determines the value of OC3. OC3REF is active at high level, and the effective level of OC3 depends on the CC3P bit. The 4-bit signal {OC3MD3, OC3MD} corresponds to the following output compare 3 modes： 0000: Freeze. The comparison between the output compare register TIMx_CCDAT3 and the counter TIMx_CNT does not affect OC3REF; 0001: Set channel 3 to an active level when a match occurs. When the value of counter TIMx_CNT is the same as the capture/compare register 3 (TIMx_CCDAT3), force OC3REF to high. 0010: Set channel 3 to an inactive level when a match occurs. When the value of counter TIMx_CNT is the same as the capture/compare register 3 (TIMx_CCDAT3), force OC3REF to low. 0011: Toggle. When TIMx_CCDAT3 = TIMx_CNT, toggle the level of OC3REF. 0100: Force to an inactive level. Force OC3REF to low. 0101: Force to an active level. Force OC3REF to high. 0110: PWM mode 1 - During up-counting, channel 3 is at an active level when TIMx_CNT < TIMx_CCDAT3, otherwise it is at an inactive level. During down-counting, channel 3 is at an inactive level (OC3REF=0) when TIMx_CNT > TIMx_CCDAT3, otherwise it is at an active level (OC3REF=1). 0111: PWM mode 2 - During up-counting, channel 3 is at an inactive level when TIMx_CNT < TIMx_CCDAT3, otherwise it is at an active level. During down-counting, channel 3 is at an active level when TIMx_CNT > TIMx_CCDAT3, otherwise it is at an inactive level. 1000: Retriggerable single pulse mode 1 - In the up-counting mode, channel 3 is in the active state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 1 comparison, channel 3 will return to the active state on the next update. In the down-counting mode, channel 3 is in the inactive state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 1 comparison, channel 3 will return to the inactive state on the next update. 1001: Retriggerable single pulse mode 2 - In the up-counting mode, channel 3 is in the inactive state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 2 comparison,

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Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
		channel 3 will return to the inactive state on the next update. In the down-counting mode, channel 3 is in the active state until a trigger event is detected (on the TRGI signal). Then, in PWM mode 2 comparison, channel 3 will return to the active state on the next update. 1010-1101：Reserved 1110: Combined PWM mode 1 - OC3REF behaves the same as in PWM mode 1. OC3REFC is the logical OR operation result of OC3REF and OC4REF. 1111: Combined PWM mode 2 - OC3REF behaves the same as in PWM mode 2. OC3REFC is the logical AND operation result of OC3REF and OC4REF. *Note: In PWM mode 1 or PWM mode 2, the OC3REF level changes only when the comparison result changes or when switching from freeze mode to PWM mode in the output compare mode.*
4	OC3CEN	Output compare 3 clear enable
3	OC3FEN	Output compare 3 fast enable
2	OC3PEN	Output compare 3 preload enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These 2 bits define the direction (input/output) of the channel and the selection of the input pin: 00: CC3 channel is configured as an output; 01: CC3 channel is configured as an input, with IC3 mapped on TI3; 10: CC3 channel is configured as an input, with IC3 mapped on TI4; 11: CC3 channel is configured as an input, with IC3 mapped on TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). *Note: CC3SEL is writable only when the channel is disabled (CC3EN=0 in the TIMx_CCEN register).*

Input capture mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
rw				rw		rw		rw				rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	IC4F[3:0]	Input capture 4 filter
11:10	IC4PSC[1:0]	Input capture 4 prescaler

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
9:8	CC4SEL[1:0]	Capture/Compare 4 selection Note: These 2 bits define the direction (input/output) of the channel and the selection of the input pin: 00: CC4 channel is configured as an output； 01: CC4 channel is configured as an input, with IC4 mapped on TI4； 10: CC4 channel is configured as an input, with IC4 mapped on TI3； 11: CC4 channel is configured as an input, with IC4 mapped on TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). Note: CC4SEL is writable only when the channel is disabled (CC4EN=0 in the TIMx_CCEN register).
7:4	IC3F[3:0]	Input capture 3 filter
3:2	IC3PSC[1:0]	Input capture 3 prescaler
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These 2 bits define the direction (input/output) of the channel and the selection of the input pin： 00: CC3 channel is configured as an output； 01: CC3 channel is configured as an input, with IC3 mapped on TI3； 10: CC3 channel is configured as an input, with IC3 mapped on TI4； 11: CC3 channel is configured as an input, with IC3 mapped on TRC. This mode only works when the internal trigger input is selected (chosen by the TSEL bit of the TIMx_SMCTRL register). Note: CC3SEL is writable only when the channel is disabled (CC3EN=0 in the TIMx_CCEN register).

20.6.9 Capture/Compare Mode Register 3（TIMx_CCMOD3）

Offset address：0x20

Reset value：0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								OC5MD[2:0]			OC5CEN	OC5FEN	OC5PEN	Reserved	
								rw			rw	rw	rw		

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:5	OC5MD[2:0]	Output compare 5 mode
4	OC5CEN	Output compare 5 clear enable
3	OC5FEN	Output compare 5 fast enable
2	OC5PEN	Output compare 5 preload enable

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Bit Field	Name	Description
1:0	Reserved	Reserved, the reset value must be maintained

20.6.10 Capture/Compare Enable Register（TIMx_CCEN）

Offset address：0x24

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												CC5P	CC5EN	Reserved	
												rw	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN	CC1NP	CC1NEN
rw	rw			rw	rw			rw	rw			rw	rw	rw	rw

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	CC5P	Capture/Compare 5 output polarity Refer to the description of TIMx_CCEN.CC1P.
18	CC5EN	Capture/Compare 5 output enable Refer to the description of TIMx_CCEN.CC1EN.
17：16	Reserved	Reserved, the reset value must be maintained
15	CC4P	Capture/Compare 4 output polarity Refer to the description of TIMx_CCEN.CC1P.
14	CC4EN	Capture/Compare 4 output enable Refer to the description of TIMx_CCEN.CC1EN.
13:12	Reserved	Reserved, the reset value must be maintained
11	CC3P	Capture/Compare 3 output polarity Refer to the description of TIMx_CCEN.CC1P.
10	CC3EN	Capture/Compare 3 output enable Refer to the description of TIMx_CCEN.CC1EN.
9:8	Reserved	Reserved, the reset value must be maintained
7	CC2P	Capture/Compare 2 output polarity Refer to the description of TIMx_CCEN.CC1P.
6	CC2EN	Capture/Compare 2 output enable Refer to the description of TIMx_CCEN.CC1EN.
5:4	Reserved	Reserved, the reset value must be maintained
3	CC1P	Capture/Compare 1 output polarity **When CC1 corresponds to the output mode:** 0: OC1 is active high 1: OC1 is active low **When CC1 corresponds to the input mode:**

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Bit Field	Name	Description
		In this case, this bit is used to select whether to use IC1 or the inverted signal of IC1 as the trigger or capture signal. 0: Non-inverted: A capture action occurs when IC1 generates a rising edge. When used as an external trigger, IC1 is non-inverted. 1: Inverted: A capture action occurs when IC1 generates a falling edge. When used as an external trigger, IC1 is inverted.
2	CC1EN	Capture/Compare 1 output enable **CC1 channel configured as output：** 0: Disabled - OC1 output is disabled, so the output level of OC1 depends on the values of MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. 1: Enabled - OC1 signal is output to the corresponding output pin, and its output level depends on the values of the MOEN, OSSI, OSSR, OI1, OI1N, and CC1NEN bits. **CC1 channel configured as input：** This bit determines whether the value of the counter can be captured into the TIMx_CCDAT1 register. 0: Capture disable; 1: Capture enable;
1	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N high level active; 1: OC1N low level active;
0	CC1NEN	Capture/Compare 1 complementary output enable 0: Disabled - Disables the output of the OC1N signal. The level of OC1N depends on the values of TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N, and TIMx_CCEN.CC1EN. 1: Enabled - Enables the output of the OC1N signal. The level of OC1N depends on the values of TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N, and TIMx_CCEN.CC1EN.

Table 20-14 Control bits for complementary output channels OCx and OCxN with brake function

Control Bit					Output State(1)	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output State	OCxN Output State
1	X	0	0	0	Output disabled (disconnected from the timer) OCx=0，OCx_EN=0	Output disabled (disconnected from the timer) OCxN=0，OCxN_EN=0
		0	0	1	Output disabled (disconnected from the timer) OCx=0，OCx_EN=0	OCxREF + Polarity， OCxN= OCxREF xor CCxNP， OCxN_EN=1
		0	1	0	OCxREF + Polarity， OCx= OCxREF xor CCxP， OCx_EN=1	Output disabled (disconnected from the timer) OCxN=0，OCxN_EN=0

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		0	1	1	OCxREF + Polarity + Deadtime，OCx_EN=1	OCxREF Invert + Polarity + Deadtime，OCxN_EN=1
		1	0	0	Output disabled (disconnected from the timer) OCx=CCxP，OCx_EN=0	Output disabled (disconnected from the timer) OCxN=CCxNP，OCxN_EN=0
		1	0	1	Disabled state (output enabled but at an inactive level) OCx=CCxP，OCx_EN=1	OCxREF + Polarity， OCxN= OCxREF xor CCxNP， OCxN_EN=1
		1	1	0	OCxREF + Polarity， OCx= OCxREF xor CCxP， OCx_EN=1	Disabled state (output enabled but at an inactive level) OCxN=CCxNP，OCxN_EN=1
		1	1	1	OCxREF + Polarity + Deadtime， OCx_EN=1	OCxREF Invert + Polarity + Deadtime， OCxN_EN=1
0	0	X	0	0	Output disabled (disconnected from the timer) Asynchronous: OCx=CCxP， OCx_EN=0， OCxN=CCxNP， OCxN_EN=0； If clock exists: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0， After a dead time OCx=OIx，OCxN=OIxN	
	0		0	1		
	0		1	0		
	0		1	1		
	1		0	0	Disabled state (output enabled but at an inactive level) Asynchronous: OCx=CCxP, OCx_EN=1, OCxN=CCxNP, OCxN_EN=1； If clock exists: if (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0， After a dead time OCx=OIx, OCxN=OIxN，	
	1		0	1		
	1		1	0		
	1		1	1		

1. If both outputs of a channel are not used (CCxEN = CCxNEN = 0), then OIx, OIxN, CCxP, and CCxNP must all be cleared.

Note: The state of the pins connected to the external I/O pins of the complementary OCx and OCxN channels depends on the states of the OCx and OCxN channels and the GPIO and AFIO registers.

20.6.11 Capture/Compare Register 1（TIMx_CCDAT1）

Offset address：0x28

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT1[15:0]															
rw															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT1[15:0]															
rw															

Bit Field	Name	Descriptions
31:16	CCDDAT1[15:0]	Capture/Compare 1 down-counting value Dedicated to center-aligned asymmetric mode ■ **CC1 channel can only be configured as an output：** CCDDAT1 contains the value to be compared with the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), to generate a signal on the OC1 output. If the preload function is not selected in the TIMx_CCMOD1.OC1PEN bit, the written value will be immediately transferred to the active register. Otherwise, the preload value will only be transferred to the active register when an update event occurs.
15:0	CCDAT1[15:0]	Capture/Compare 1 value ■ **CC1 Channel configured as output:** CCDAT1 contains the value to be compared with the counter TIMx_CNT, to generate a signal on the OC1 output. If the preload function is not selected in the TIMx_CCMOD1.OC1PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be transferred to the active register when an update event occurs. ■ **CC1 channel configured as input:** CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured in input mode, registers CCDAT1 and CCDDAT1 can only be read. When configured in output mode, registers CCDAT1 and CCDDAT1 are readable and writable.

20.6.12 Capture/Compare Register 2（TIMx_CCDAT2）

Offset address：0x2C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT2[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT2[15:0]															
rw															

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Bit Field	Name	Description
31:16	CCDDAT2[15:0]	Capture/Compare 2 down-counting value Dedicated to center-aligned asymmetric mode. ■ **CC2 channel can only be configured as an output：** CCDDAT2 contains the value to be compared with the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), to generate a signal on the OC2 output. If the preload function is not selected in the TIMx_CCMOD1.OC2PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be transferred to the active register when an update event occurs.
15:0	CCDAT2[15:0]	Capture/Compare 2 value ■ **CC2 channel configured as output:** CCDAT2 contains the value to be compared with the counter TIMx_CNT, to generate a signal on the OC2 output. If the preload function is not selected in the TIMx_CCMOD1.OC2PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be transferred to the active register when an update event occurs. ■ **CC2 channel configured as input:** CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured in input mode, registers CCDAT2 and CCDDAT2 can only be read. When configured in output mode, registers CCDAT2 and CCDDAT2 are readable and writable.

20.6.13 Capture/Compare Register 3（TIMx_CCDAT3）

Offset address：0x30

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT3[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT3[15:0]															
rw															

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Bit Field	Name	Description
31:16	CCDDAT3[15:0]	Capture/Compare 3 down-counting value **Dedicated to center-aligned asymmetric mode**. ■ CC3 channel can only be configured as an output： CCDDAT3 contains the value to be compared with the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), to generate a signal on the OC3 output. If the preload function is not selected in the TIMx_CCMOD2.OC3PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be transferred to the active register when an update event occurs.
15:0	CCDAT3[15:0]	Capture/Compare 3 value ■ **CC3 channel configured as output:** CCDAT3 contains the value to be compared with the counter TIMx_CNT, to generate a signal on the OC3 output. If the preload function is not selected in the TIMx_CCMOD2.OC3PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be transferred to the active register when an update event occurs. ■ **CC3 channel configured as input:** CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured in input mode, registers CCDAT3 and CCDDAT3 can only be read. When configured in output mode, registers CCDAT3 and CCDDAT3 are readable and writable.

20.6.14 Capture/Compare Register 4（TIMx_CCDAT4）

Offset address：0x34

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCDDAT4[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT4[15:0]															
rw															

Bit Field	Name	Description
31:16	CCDDAT4[15:0]	Capture/Compare 4 down-counting value Dedicated to center-aligned asymmetric mode. ■ **CC4 channel can only be configured as an output:** CCDDAT4 contains the value to be compared with the counter TIMx_CNT (only when TIMx_CTRL1.DIR = 1 and in asymmetric mode), to generate a signal on the OC4 output. If the preload function is not selected in the TIMx_CCMOD2.OC4PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be

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		transferred to the active register when an update event occurs.
15:0	CCDAT4[15:0]	Capture/Compare 4 value ■ **CC4 channel configured as output:** CCDAT4 contains the value to be compared with the counter TIMx_CNT, to generate a signal on the OC4 output. If the preload function is not selected in the TIMx_CCMOD2.OC4PEN bit, the written value will be immediately transferred to the effective register. Otherwise, this preload value will only be transferred to the active register when an update event occurs. ■ **CC4 channel configured as input:** CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured in input mode, registers CCDAT4 and CCDDAT4 can only be read. When configured in output mode, registers CCDAT4 and CCDDAT4 are readable and writable.

20.6.15 Capture/Compare Register 5（TIMx_CCDAT5）

Offset address：0x38

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCDAT5[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CCDAT5[15:0]	Capture/Compare 5 value ■ **CC5 channel can only be configured as an output:** CCDAT5 contains the value to be compared with the counter TIMx_CNT, and signals on the OC5 output. If the preload function is not selected in the TIMx_CCMOD3.OC5PEN bit, the written value will be immediately transferred to the active register. Otherwise, the preload value will only be transferred to the active register when an update event occurs. CC5 is used for comparator blanking.

20.6.16 Prescaler（TIMx_PSC）

Offset address：0x40

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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PSC[15:0]

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK_CNT} = f_{CK_PSC}/ (PSC [15:0] +1)$。 Each time an update event occurs, the PSC value is loaded into the shadow register of the prescaler.

20.6.17 Auto-Reload Register（TIMx_AR）

Offset address:0x44

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[15:0]															

rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	AR[15:0]	Auto-reload value AR contains the value that will be loaded into the actual auto-reload register. Refer to section 20.5.1 for details on the update and actions of AR. When the value of auto-reload is zero, the counter does not work.

20.6.18 Counter（TIMx_CNT）

Offset address：0x48

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UDITFCPY	Reserved														

r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															

rw

Bit Field	Name	Description
31	UDITFCPY	UDITF copy This bit is a read-only copy of the UDITF bit in the TIMx_STS register. If the

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Bit Field	Name	Description
		TIMx_CTRL1.UDITFREMAP bit is reset, bit 31 is reserved and reads as 0.
30:16	Reserved	Reserved, the reset value must be maintained
15:0	CNT[15:0]	Counter value

20.6.19 Repetition Counter Register（TIMx_REPCNT）

Offset address：0x4C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								REPCNT[7:0]							
								rw							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value The repetition counter is used to generate an update event or update the timer registers after a given number (N+1) of counter periods, where N is the value of TIMx_REPCNT.REPCNT. In up-counting mode, the repetition counter decrements on each counter overflow, in down-counting mode it decrements on each counter underflow, and in center-aligned mode it decrements on each counter overflow and underflow. Setting the TIMx_EVTGEN.UDGN bit reloads the content of TIMx_REPCNT.REPCNT and generates an update event.

20.6.20 Break and Deadtime Register（TIMx_BKDT）

Offset address：0x50

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											BRKBID	Reserved	BRK DSRM	Reserved	
											rw		rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCKCFG[1:0]		OSSR	OSSI	BKEN	BKP	AOEN	MOEN	DTGN[7:0]							
rw		rw	rw	rw	rw	rw	rw	rw							

Note: Depending on the lock settings, the BRK2BID, BRKBID, BK2EN, BK2P, AOEN, BKP, BKEN, OSSI, OSSR, and DTGN[7:0] bits can be write-protected. It is necessary to configure them when writing to the TIMx_BKDT register for the first time.

Bit Field	Name	Description

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31:21	Reserved	Reserved, the reset value must be maintained
20	BRKBID	Break 1 bidirectional enable 0: Break 1 is the input mode 1: Break 1 is the bidirectional mode In bidirectional mode, Break 1 input is configured to operate in both input and open-drain output modes. Any Break 1 event will generate a low level on the Break 1 input IO, indicating to external devices that an internal Break 1 event has occurred. *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.* *Note: Any write operation to this bit will take effect after a delay of an APB clock cycle.*
18	BRKDSRM	Break 1 disarm 0: Break 1 input preparation 1: Break 1 input disarm When the Break 1 input is invalid, this bit will be automatically cleared by the hardware. BRKDSRM is set by software to release Break 1 bidirectional output control (open-drain output in high-impedance state), then software polls this bit until it is reset by hardware, indicating that the Break 1 event has disappeared. *Note: Any write operation to this bit will take effect after a delay of an APB clock cycle.*
15:14	LCKCFG[1:0]	Lock configuration These bits provide write protection against software errors. 00:– No write protection. 01:– LOCK Level 1 TIMx_BKDT.DTGN、TIMx_BKDT.BKEN、TIMx_BKDT.BKP、TIMx_BKDT.AOEN、TIMx_CTRL2.OIx、TIMx_CTRL2.OIxN enable write protection. 10: – LOCK Level 2 In addition to register write protection in LOCK Level 1 mode, write protection is also enabled for TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (if the corresponding channel is configured in output mode), as well as for the TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits. 11:– LOCK Level 3 In addition to register write protection in LOCK Level 2, write protection is also enabled for TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (if the corresponding channel is configured in output mode). *Note: After system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
13	OSSR	This bit is used when TIMx_BKDT.MOEN=1 and the channel is configured as complementary output. There is no OSSR bit in timers without complementary output. 0: When the timer is not operating, disable OC/OCN output (OC/OCN enable output signal = 0)； 1: When the timer is not operating, if CCxEN=1 or CCxNEN=1, OC/OCN will first be enabled to output an invalid level, and then set OC/OCN enable output signal to 1. For more detailed information, please refer to Section18.5.9, Capture/Compare Enable Register (TIMx_CCEN).

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12	OSSI	Off-state selection for Idle mode This bit is used when TIMx_BKDT.MOEN=0 and the channel is configured as an output. 0: When the timer is not operating, disable OC/OCN output (OC/OCN enable output signal = 0); 1: When the timer is not operating, if CCxEN=1 or CCxNEN=1, OC/OCN first outputs its idle level, and then OC/OCN enables the output signal to 1. For more detailed information, please refer to Section18.5.9节， Capture/Compare Enable Register (TIMx_CCEN).
11	BKEN	Break 1 enable 0: Disable Break 1 input; 1: Enable Break 1 input; *Note: Any write operation to this bit will take effect after a delay of an APB clock cycle*
10	BKP	Break 1 polarity 0: Break 1 input low level effective; 1: Break 1 input high level effective; *Note: Any write operation to this bit will take effect after a delay of one APB clock cycle*
9	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not activated, hardware automatically sets TIMx_BKDT.MOEN at the next update event.
8	MOEN	Main output enable This bit can be set by software or hardware based on the TIMx_BKDT.AOEN bit. Once the break input is valid, this bit is asynchronously cleared by hardware. It is only effective for channels configured as outputs. 0: OC and OCN outputs are disabled or forced into the idle state。 1: If the TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set, the OC and OCN outputs are enabled. For more detailed information, please refer to Section 18.5.9, Capture/Compare Enable Register (TIMx_CCEN).
7:0	DTGN[7:0]	Dead-time generator setup These bits define the dead-time duration between the inserted complementary outputs. The relationship between the DTGN value and the dead-time is as follows: DTGN[7:5]=0xx => DT=DTGN[7:0] × T_{dtgn}， $T_{dtgn} = T_{DTS}$; DTGN[7:5]=10x => DT=(64+DTGN[5:0]) × T_{dtgn}， $T_{dtgn} = 2 \times T_{DTS}$; DTGN[7:5]=110 => DT=(32+DTGN[4:0]) × T_{dtgn}， $T_{dtgn} = 8 \times T_{DTS}$; DTGN[7:5]=111 => DT=(32+DTGN[4:0])× T_{dtgn}， $T_{dtgn} = 16 \times T_{DTS}$;

20.6.21 Break 1 Filter Register（TIMx_BKFR）

Offset address：0x60

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				THRESH[5:0]				Reserved	WSIZE[5:0]						FILTEN

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rw															rw															rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
SLIDFPSC [15:0]																													
rw																													

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold: The number of valid logic levels in the sampling logic, with a maximum of 63. Within the sampling window, if the number of logic highs is greater than or equal to the threshold, the next logic level will be high. The same rule applies to logic lows. If the number of 1s and 0s within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to be greater than or equal to half of the Window value. The recommended threshold range is: **Minimum value:** It is one additional prescaler clock cycle beyond the upper limit of the maximum glitch size (prescaler clock cycles) and must be greater than half of the window size. For example, if the glitch size is 3.2 * (prescaler clock cycles), the threshold should be ┌3.2┐=4+1=5. **Maximum value:** It is the lower limit of the minimum valid signal size (in prescaler clock cycles) and must be less than the window size. For example, if the minimum signal size is 3.2 * (prescaler clock cycles), the threshold should be the floor value of 3.2, which is 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	The window size value for logic level checking, with a maximum of 63: The window size determines how many samples will be considered when obtaining the next logic level. The built-in FIFO is 64 bits with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a division of 65535 (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculation. Configure these bits to determine the sampling clock division for the break input sliding filter.

20.6.22 Channel 1 Filter Register（TIMx_C1FILT）

Offset address：0x64

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH[5:0]						Reserved	WSIZE[5:0]						FILTEN
		rw							rw						rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															
rw															

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold: The number of valid logic levels in the sampling logic, with a maximum of 63. Within the sampling window, if the number of logic highs is greater than or equal to the threshold, the next logic level will be high. The same rule applies to logic lows. If the number of 1s and 0s within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to be greater than or equal to half of the Window value. The recommended threshold range is: **Minimum value:** It is one additional prescaler clock cycle beyond the upper limit of the maximum glitch size (prescaler clock cycles) and must be greater than half of the window size. For example, if the glitch size is 3.2 * (prescaler clock cycles), the threshold should be ⌈3.2⌉ =4+1=5. **Maximum value:** It is the lower limit of the minimum valid signal size (in prescaler clock cycles) and must be less than the window size. For example, if the minimum signal size is 3.2 * (prescaler clock cycles), the threshold should be the floor value of 3.2, which is 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	The window size value for logic level checking, with a maximum of 63: The window size determines how many samples will be considered when obtaining the next logic level. The built-in FIFO is 64 bits with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a division of 65535 (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculation. Configure these bits to determine the sampling clock division for the channel 1 sliding filter.

20.6.23 Channel 2 Filter Register（TIMx_C2FILT）

Offset address：0x68

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		THRESH[5:0]						Reserved	WSIZE[5:0]						FILTEN
		rw							rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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SLIDFPSC [15:0]

rw

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold: The number of valid logic levels in the sampling logic, with a maximum of 63. Within the sampling window, if the number of logic highs is greater than or equal to the threshold, the next logic level will be high. The same rule applies to logic lows. If the number of 1s and 0s within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to be greater than or equal to half of the Window value. The recommended threshold range is: **Minimum value:** It is one additional prescaler clock cycle beyond the upper limit of the maximum glitch size (prescaler clock cycles) and must be greater than half of the window size. For example, if the glitch size is 3.2 * (prescaler clock cycles), the threshold should be ⌈3.2⌉ =4+1=5. **Maximum value:** It is the lower limit of the minimum valid signal size (in prescaler clock cycles) and must be less than the window size. For example, if the minimum signal size is 3.2 * (prescaler clock cycles), the threshold should be the floor value of 3.2, which is 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	The window size value for logic level checking, with a maximum of 63: The window size determines how many samples will be considered when obtaining the next logic level. The built-in FIFO is 64 bits with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a division of 65535 (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculation. Configure these bits to determine the sampling clock division for the channel 2 sliding filter.

20.6.24 Channel 3 Filter Register（TIMx_C3FILT）

Offset address：0x6C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				THRESH[5:0]				Reserved				WSIZE[5:0]			FILTEN
				rw								rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															

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rw

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold: The number of valid logic levels in the sampling logic, with a maximum of 63. Within the sampling window, if the number of logic highs is greater than or equal to the threshold, the next logic level will be high. The same rule applies to logic lows. If the number of 1s and 0s within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to be greater than or equal to half of the Window value. The recommended threshold range is: **Minimum value:** It is one additional prescaler clock cycle beyond the upper limit of the maximum glitch size (prescaler clock cycles) and must be greater than half of the window size. For example, if the glitch size is 3.2 * (prescaler clock cycles), the threshold should be ⌈3.2⌉ =4+1=5. **Maximum value:** It is the lower limit of the minimum valid signal size (in prescaler clock cycles) and must be less than the window size. For example, if the minimum signal size is 3.2 * (prescaler clock cycles), the threshold should be the floor value of 3.2, which is 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	The window size value for logic level checking, with a maximum of 63: The window size determines how many samples will be considered when obtaining the next logic level. The built-in FIFO is 64 bits with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a division of 65535 (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculation. Configure these bits to determine the sampling clock division for the channel 3 sliding filter.

20.6.25 Channel 4 Filter Register（TIMx_C4FILT）

Offset address：0x70

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				THRESH[5:0]				Reserved	WSIZE[5:0]						FILTEN
				rw					rw						rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLIDFPSC [15:0]															
rw															

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Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:24	THRESH[5:0]	Threshold: The number of valid logic levels in the sampling logic, with a maximum of 63. Within the sampling window, if the number of logic highs is greater than or equal to the threshold, the next logic level will be high. The same rule applies to logic lows. If the number of 1s and 0s within the window is less than the threshold, the filter output remains unchanged. The threshold should be set to be greater than or equal to half of the Window value. The recommended threshold range is: **Minimum value:** It is one additional prescaler clock cycle beyond the upper limit of the maximum glitch size (prescaler clock cycles) and must be greater than half of the window size. For example, if the glitch size is 3.2 * (prescaler clock cycles), the threshold should be ⌜3.2⌝=4+1=5. **Maximum value:** It is the lower limit of the minimum valid signal size (in prescaler clock cycles) and must be less than the window size. For example, if the minimum signal size is 3.2 * (prescaler clock cycles), the threshold should be the floor value of 3.2, which is 3.
23	Reserved	Reserved, the reset value must be maintained
22:17	WSIZE[5:0]	The window size value for logic level checking, with a maximum of 63: The window size determines how many samples will be considered when obtaining the next logic level. The built-in FIFO is 64 bits with a maximum index of 63, so the window size can only be set to 63.
16	FILTEN	Filter enable 0: Filter disable 1: Filter enable
15:0	SLIDFPSC [15:0]	Sliding Filter Sampling Clock Prescaler Register (Prescaler): For this filter, it supports a division of 65535 (16 bits). The clock prescaler scales the system clock to the sampling clock. The sampling clock determines the distance between two sampling points. Only the values of the sampling points are considered for logic level calculation. Configure these bits to determine the sampling clock division for the channel 4 sliding filter.

20.6.26 Input Channel Filter Output Register（TIMx_FILTO）

Offset address：0x74

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												C4FILTO	C3FILTO	C2FILTO	C1FILTO
												r	r	r	r

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained

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3	C4FILTO	Channel 4 filter output level status 0: Output low level 1: Output high level
2	C3FILTO	Channel 3 filter output level status 0: Output low level 1: Output high level
1	C2FILTO	Channel 2 filter output level status 0: Output low level 1: Output high level
0	C1FILTO	Channel 1 filter output level status 0: Output low level 1: Output high level

20.6.27 Input Selection Register（TIMx_INSEL）

Offset address：0x78

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				CLRS[3:0]				ITRS[3:0]				ETRS[3:0]			
				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TI4S[3:0]				TI3S[3:0]				TI2S[3:0]				TI1S[3:0]			
rw				rw				rw				rw			

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	CLRS[3:0]	Selects tim_ocref_clr[0:15] input signal 0000: tim_ocref_clr0 0001: tim_ocref_clr1 … 1111: tim_ocref_clr15 *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.*
23:20	ITRS[3:0]	Selects tim_itr[0:15] input signal 0000: tim_itr0 0001: tim_itr1 … 1111: tim_itr15
19:16	ETRS[3:0]	Selects tim_etr[0:15] input signal 0000: tim_etr0

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		0001: tim_etr1 … 1111: tim_etr15 *Note: Once the LOCK level (LCKCFG bit in the TIMx_BKDT register) is set to '1', this bit cannot be modified.*
15:12	TI4S[3:0]	Selects tim_ti4[0:15] input signal 0000: tim_ti4_in0 0001: tim_ti4_in1 … 1111: tim_ti4_in15
11:8	TI3S[3:0]	Selects tim_ti3[0:15] input signal 0000: tim_ti3_in0 0001: tim_ti3_in1 … 1111: tim_ti3_in15
7:4	TI2S[3:0]	Selects tim_ti2[0:15] input signal 0000: tim_ti2_in0 0001: tim_ti2_in1 … 1111: tim_ti2_in15
3:0	TI1S[3:0]	Select tim_ti1[0:15] input signal 0000: tim_ti1_in0 0001: tim_ti1_in1 … 1111: tim_ti1_in15

20.6.28 Alternate Function Register 1（TIMx_AF1）

Offset address：0x7C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				DSMU3BRKEN	DSMU2BRKEN	DSMU1BRKEN	DSMU0BRKEN	Reserved							
				rw	rw	rw	rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		COMP4BRKP	COMP3BRKP	COMP2BRKP	COMP1BRKP	IOMBRKP	Reserved				COMP4BRKEN	COMP3BRKEN	COMP2BRKEN	COMP1BRKEN	IOMBRKEN
		rw	rw	rw	rw	rw					rw	rw	rw	rw	rw

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	DSMU3BRKEN	tim_brk_dsmu3 input enable 0：tim_brk_dsmu3 input disabled 1：tim_brk_dsmu3 input enabled

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26	DSMU2BRKEN	tim_brk_dsmu2 input enable 0：tim_brk_dsmu2 input disabled 1：tim_brk_dsmu2 input enabled
25	DSMU1BRKEN	tim_brk_dsmu1 input enable 0：tim_brk_dsmu1 input disabled 1：tim_brk_dsmu1 input enabled
24	DSMU0BRKEN	tim_brk_dsmu0 input enable 0：tim_brk_dsmu0 input disabled 1：tim_brk_dsmu0 input enabled
23:14	Reserved	Reserved, the reset value must be maintained
13	COMP4BRKP	tim_brk_comp4 Break Input Polarity Selection 0: tim_brk_comp4 Break Input Polarity Non-Inverted (Low level effective if BKP=0; High level effective if BKP=1) 1: tim_brk_comp4 Brake Input Polarity Inverted (High level effective if BKP=0; Low level effective if BKP=1)
12	COMP3BRKP	tim_brk_comp3 Break Input Polarity Selection 0: tim_brk_comp3 Break Input Polarity Non-Inverted (Low level effective if BKP=0; High level effective if BKP=1) 1: tim_brk_comp3 Brake Input Polarity Inverted (High level effective if BKP=0; Low level effective if BKP=1)
11	COMP2BRKP	tim_brk_comp2 Break Input Polarity Selection 0: tim_brk_comp2 Break Input Polarity Non-Inverted (Low level effective if BKP=0; High level effective if BKP=1) 1: tim_brk_comp2 Brake Input Polarity Inverted (High level effective if BKP=0; Low level effective if BKP=1)
10	COMP1BRKP	tim_brk_comp1 Break Input Polarity Selection 0: tim_brk_comp1 Break Input Polarity Non-Inverted (Low level effective if BKP=0; High level effective if BKP=1) 1: tim_brk_comp2 Brake Input Polarity Inverted (High level effective if BKP=0; Low level effective if BKP=1)
9	IOMBRK	TIMx_BKIN Brake Input Polarity Selection 0: TIMx_BKIN Break Input Polarity Non-Inverted (Low level effective if BKP=0; High level effective if BKP=1) 1: TIMx_BKIN Break Input Polarity Inverted (High level effective if BKP=0; Low level effective if BKP=1)
8:5	Reserved	Reserved, the reset value must be maintained
4	COMP4BRKEN	tim_brk_comp4 break input enable 0: tim_brk_comp4 break input disable 1: tim_brk_comp4 break input enable
3	COMP3BRKEN	tim_brk_comp3 break input enable 0: tim_brk_comp3 break input disable 1: tim_brk_comp3 break input enable

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2	COMP2BRKEN	tim_brk_comp2 break input enable 0: tim_brk_comp2 break input disable 1: tim_brk_comp2 break input enable
1	COMP1BRKEN	tim_brk_comp1 break input enable 0: tim_brk_comp1 break input disable 1: tim_brk_comp1 break input enable
0	IOMBRKEN	TIMx_BKIN break input enable 0: TIMx_BKIN break input disable 1: TIMx_BKIN break input enable

20.6.29 DMA Control Register（TIMx_DCTRL）

Offset address：0x94

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBADDR[5:0]						Reserved		DBLEN[5:0]					
		rw								rw					

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	DBADDR[5:0]	DMA base address This field defines the first address for DMA access to the TIMx_DADDR register. When accessing TIMx_DADDR for the first time, this field specifies the address that was just accessed. Subsequent accesses to TIMx_DADDR will access the address of "DMA Base Address + 4" 00000: TIMx_CTRL1 00001: TIMx_CTRL2 00010: TIMx_SMCTRL ..... 10001: TIMx_BKDT 10010: TIMx_DCTRL
7:6	Reserved	Reserved, the reset value must be maintained

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Bit Field	Name	Description
5:0	DBLEN[5:0]	DMA burst length This field defines the number of times DMA will access (write/read) the TIMx_DADDR register. 000000: One time transfer 000001: Two times transfer 000010: Three times transfer ..... 010001: Eighteen times transfer ..... 100010: Thirty-five times transfers For example, we consider the following transfer: DBLEN=7, DBADDR=TIMx_CTRL1 If DBLEN=7 and DBADDR=TIMx_CTRL1 represents the address of the data to be transferred, then the address of the transfer is given by the following formula: ((Address of TIMx_CTRL1) + DBADDR + (DMA index)), where DMA index = DBLEN. Adding 7 to ((Address of TIMx_CTRL1) + DBADDR) gives the address where data will be written to or read from. This means the data transfer will occur in the 7 registers starting from the address ((Address of TIMx_CTRL1) + DBADDR). If the data is set to half-word (16 bits), then the data will be transferred to all 7 registers. If the data is set to byte, the data will still be transferred to all 7 registers: the first register contains the first MSB byte, the second register contains the first LSB byte, and so on. Therefore, for the timer, the user must specify the data width to be transferred by DMA.

20.6.30 Continuous Mode DMA Address（TIMx_DADDR）

Offset address：0x98

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BURST[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BURST[31:0]															
rw															

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Bit Field	Name	Description
31:0	BURST[31:0]	DMA access buffer When a read or write operation is assigned to this register, the registers located at the address range (DMA base address + DMA burst length × 4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example： If TIMx_DCTRL.DBLEN = 0x3 (4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half-word, DMA memory address = buffer address in SRAM, and DMA peripheral address = TIMx_DADDR address. When the event occurs, TIMx will send a request to DMA and transfer data 4 times. The first time, DMA access to the TIMx_DADDR register will be mapped to access the TIMx_CCDAT1 register; The second time, DMA access to the TIMx_DADDR register will be mapped to access the TIMx_CCDAT2 register; …… The fourth time, DMA access to the TIMx_DADDR register will be mapped to access the TIMx_CCDAT4 register;

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21 Basic Timers (BTIM1/BTIM2/BTIM3/BTIM4)

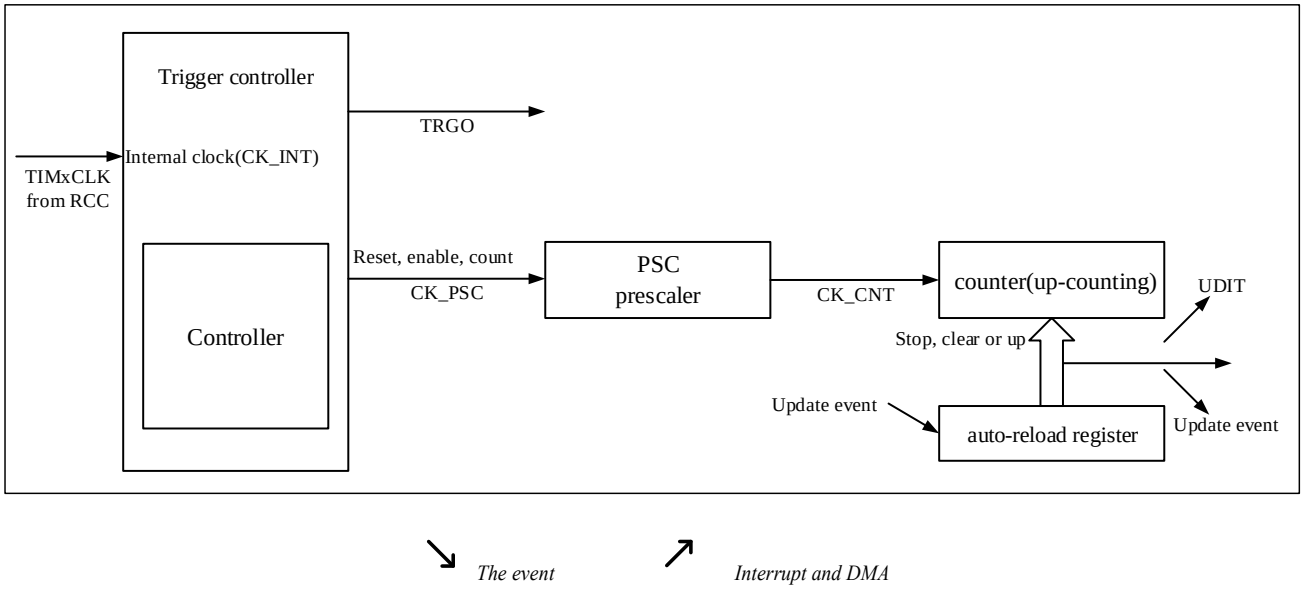
21.1 BTIMx(x=1-4)Introduction

Basic timers each contain a 32-bit auto-reload counter.

21.2 BTIMx(x=1-4)Main Features

- 32-bit auto-reload up-counting counter.
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536).
- The events that generate the interrupt/DMA are as follows:
  - Update event

Figure 21-1 Block Diagram Of BTIMx (x = 1,2,3,4)



21.3 BTIMx (x=1-4) Description

21.3.1 Time-Base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload register. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. When TIMx_CTRL1.UPDIS=0, an update event is generated when the counter reaches the overflow condition, or when the TIMx_EVTGEN.UDGN bit is set by software. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

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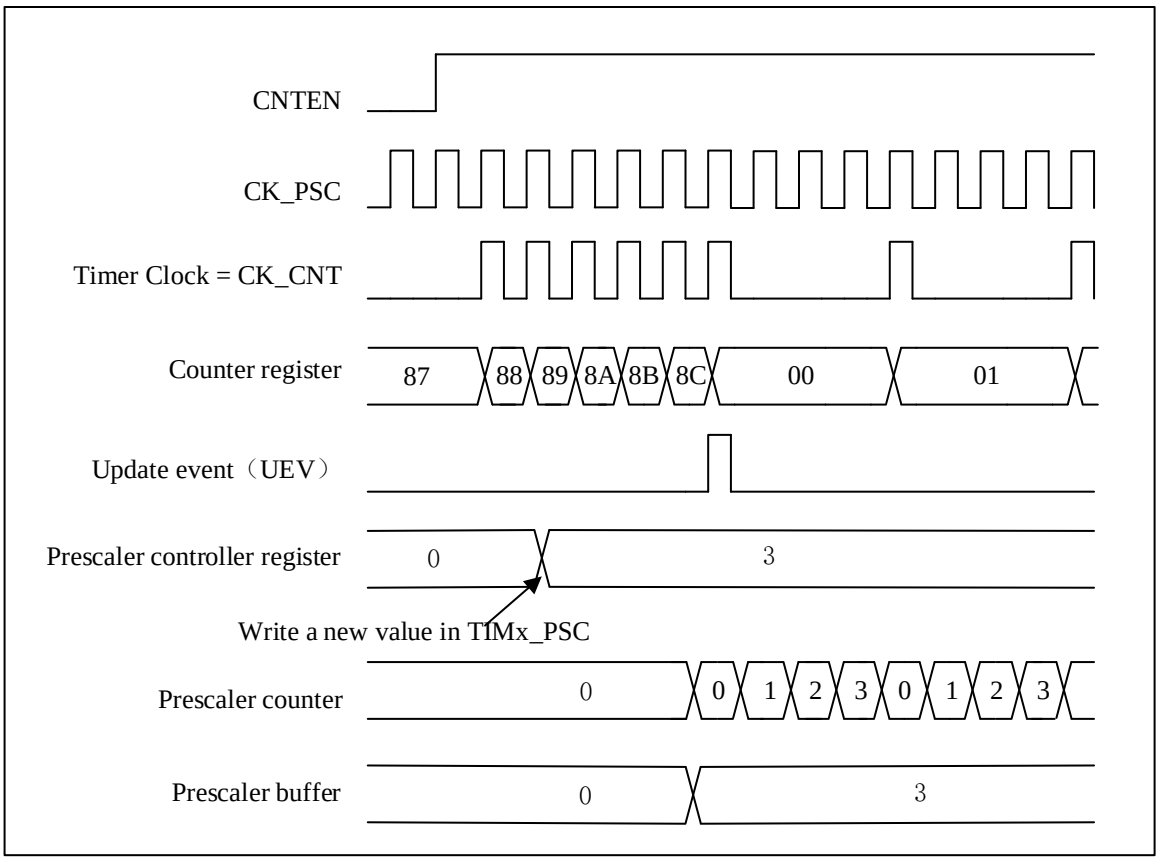
21.3.1.1 Prescaler Description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 21-2 Counter Timing Diagram With Prescaler Division Change From 1 To 4



21.3.2 Counting Mode

21.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate, but TIMx_STS.UDITF will not be set by hardware. Therefore, no update interrupts or DMA update requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in TIMx_CTRL1.UPRS, when an update event occurs, TIMx_STS.UDITF is set and all registers are updated：

- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

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To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

In this way,when an update event occurs, the counter and the prescaler counter will also be reset to 0 (but the prescaler rate will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different clock frequencies in the up-counting mode.

Figure 21-3 Timing Diagram Of Up-Counting. The Internal Clock Divider Factor = 2/N

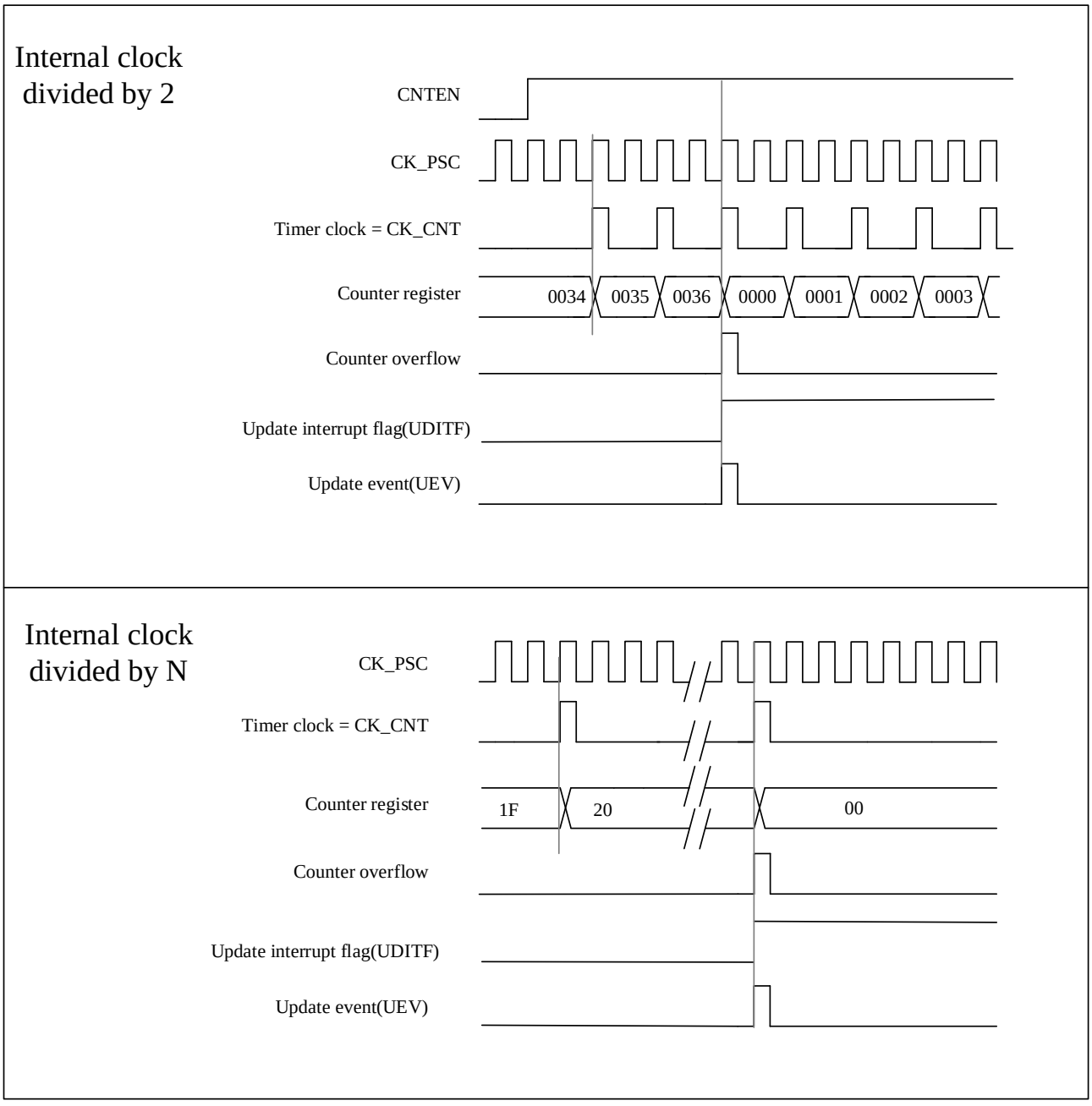

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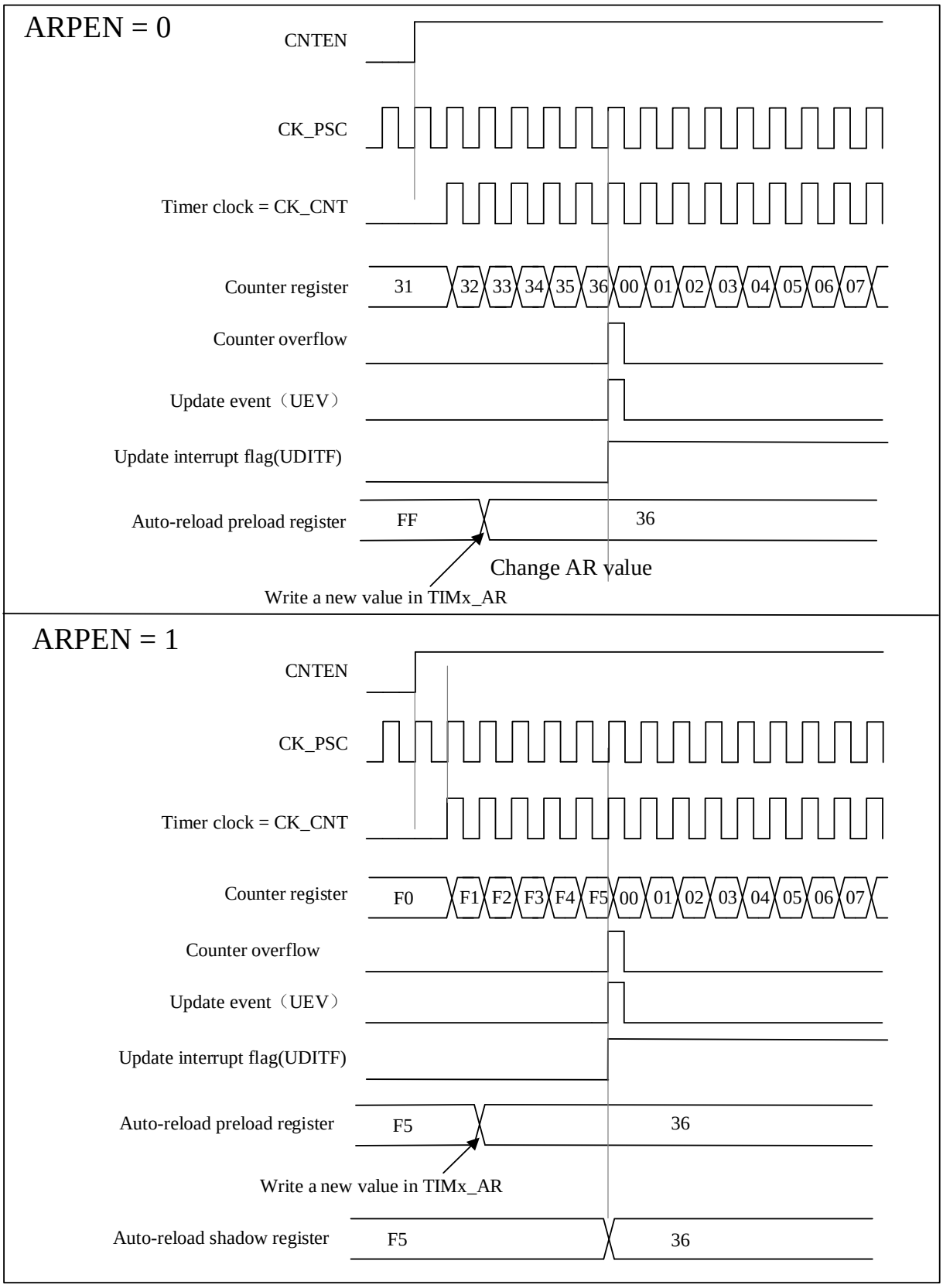
图 21-4 Timing diagram of up-counting and update event when ARPEN=0/1



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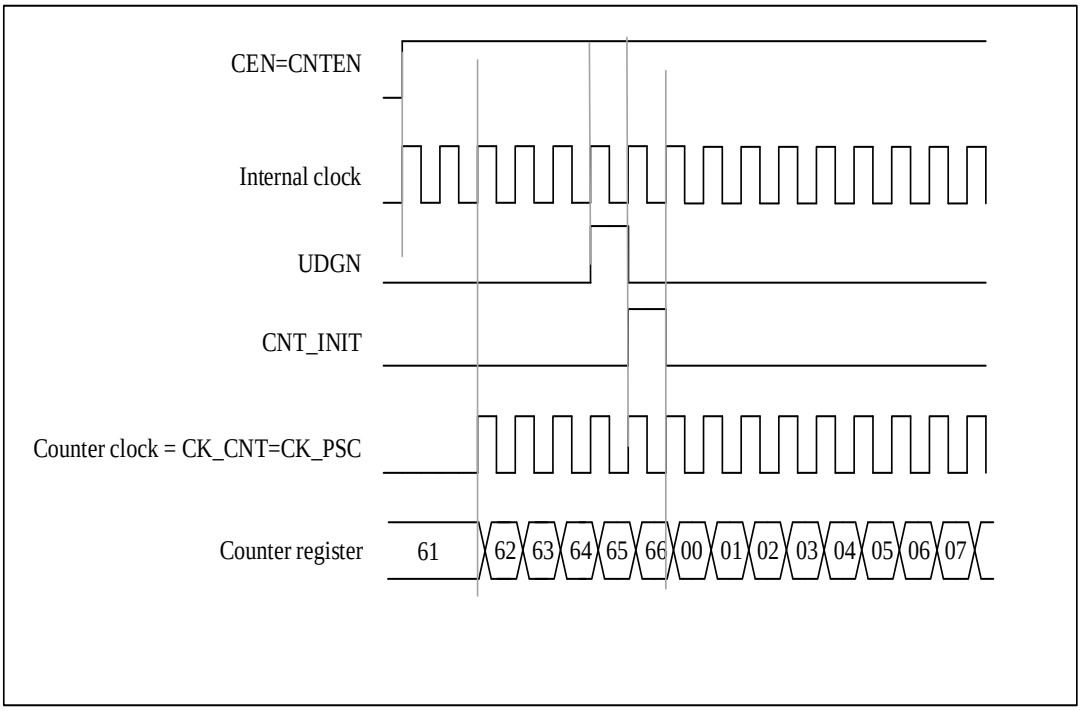
21.3.3 Clock Selection

- The internal clock of timers : CK_INT

21.3.3.1 Internal clock source (CK_INT)

It is provided that the TIMx_CTRL1.CNTEN bit is written as '1' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 21-5 Control Circuit In Normal Mode, Internal Clock Divided By 1



21.3.4 Debug Mode

When the microcontroller is in debug mode (the Cortex®-M4F core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop.

21.4 BTIMx(x=1-4) Register Description

For abbreviations used in registers, see Section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

21.4.1 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						ARPEN	ONEPM	Reserved		UPDIS	UPRS	Reserved			CNTEN
						rw	rw			rw	rw				rw

Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained
9	ARPEN	Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
8	ONEPM	One pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit).
7:6	Reserved	Reserved, the reset value must be maintained
5	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled： – Counter overflow – The TIMx_EVTGEN.UDGN bit is set Shadow registers will update with preload value。 1: Disabled UEV. No update event is generated, and the shadow registers (AR, PSC) keep their values. If the TIMx_EVTGEN.UDGN bit is set, the counter and prescaler are reinitialized.
4	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request： – Counter overflow – The TIMx_EVTGEN.UDGN bit is set 1: If update interrupt or DMA request is enabled, only counter overflow will generate update interrupt or DMA request
3:1	Reserved	Reserved, the reset value must be maintained
0	CNTEN	Counter enable 0: Disable counter 1: Enable counter

21.4.2 Control Register 2（TIMx_CTRL2）

Offset address：0x04

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Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMSEL[3:0]				Reserved											
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:12	MMSEL[3:0]	Master Mode Selection These 4 bits are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows： x000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. x001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO unless the master/slave mode is selected (refer to the description of the TIMx_SMCTRL.MSMD bit). x010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. other：Reserved.
11:0	Reserved	Reserved, the reset value must be maintained

21.4.3 Status Registers (TIMx_STS)

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															UDITF
															rc_w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained

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16	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions： –When TIMx_CTRL1.UPDIS = 0, and counter value overflow。 –When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT。 This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred
15:0	Reserved	Reserved, the reset value must be maintained

21.4.4 Event Generation Register (TIMx_EVTGEN)

Offset address: 0x0C

Reset value: 0 x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							UDGN	Reserved							
							w								

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	UDGN	Update generation Software can set this bit to update configuration register value and hardware will clear it automatically. 0: No effect. 1: Timer will restart and all shadow register will be updated. It will restart prescaler counter also.
7:0	Reserved	Reserved, the reset value must be maintained.

21.4.5 DMA/Interrupt Enable Register (TIMx_DINTEN)

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												UDEN	Reserved		UIEN
												rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

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Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
18:17	Reserved	Reserved, the reset value must be maintained
16	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enable update interrupt
15:0	Reserved	Reserved, the reset value must be maintained

21.4.6 Prescaler (TIMx_PSC)

Offset address: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	PSC[15:0]	Prescaler value PSC register value will be updated to prescaler register at update event. Counter clock frequency is input clock frequency divide PSC + 1。

21.4.7 Automatic Reload Register (TIMx_AR)

Offset address: 0x44

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR[31:0]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR[31:0]															

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rw

Bit field	Name	Description
31:0	AR[31:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See 21.3.1 for more details。 When the TIMx_AR.AR [15:0] value is null, the counter does not work.

21.4.8 Counter (TIMx_CNT)

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNT[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[31:0]															
rw															

Bit Field	Name	Description
31:0	CNT[31:0]	Counter value

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22 Low Power Timer(LPTIM)

22.1 Introduction

Supports five low-power timers.The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes. LPTIM can run without internal clock source, it can be used as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extremely low power consumption.

22.2 Main Features

- 16-bit up counter
- 3-bit prescaler, 8 kinds of prescaler factors（1、2、4、8、16、32、64、128）
- Multiple clock sources:
  - Internal clock source: LSE, LSI, HSI, MSI or APB clock
  - External clock source: External clock source through LPTIM Input1(operating without LP oscillator, for pulse counter applications).
- 16-bit auto-load register（LPTIM_ARR）
- 16-bit compare register（LPTIM_CMP）
- Continuous or one-shot mode counting mode.
- Programmable software or hardware input trigger.
- Programmable digital filter for glitch filtering.
- Configureable output (PWM)
- Configurable IO polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting(quadrature and non-quadrature)

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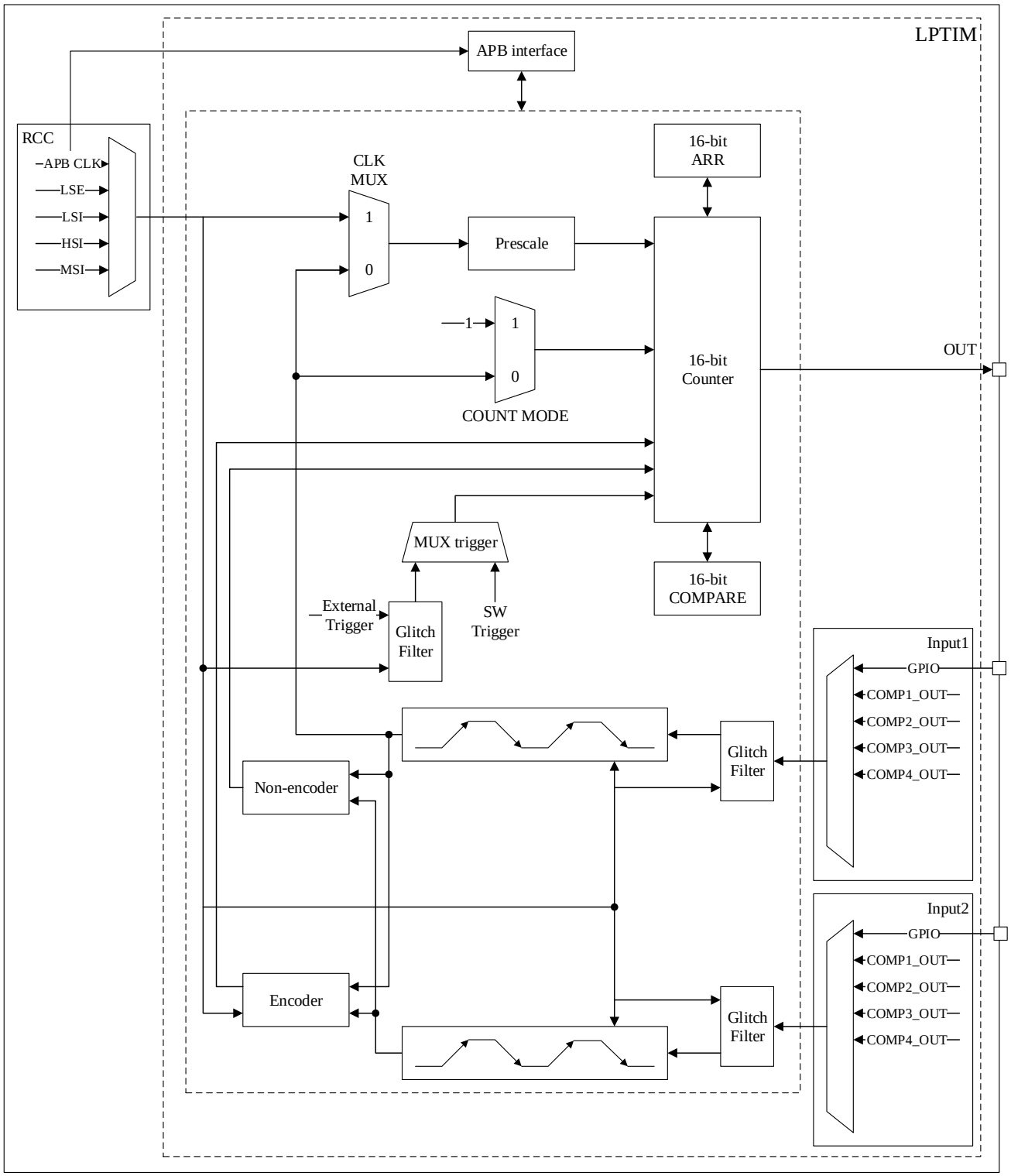
22.3 Block Diagram

Figure 22-1 LPTIM Diagram



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22.4 Function Description

22.4.1 Clocks and Reset

The LPTIM can use an internal clock source or an external clock source. The internal clock source can configure by RCC_RDCTRL.LPTIMSEL[2:0] bits.The external clock source can be selected from GPIO or Comparator 1、2、3、4.For external clock source, LPTIM has two configurations:

- The LPTIM uses both external clock and internal clock.
- The LPTIM only use external clock from comparator or external Input1. This configuration is suitable for low power application.

LPTIM_CFG.CLKSEL and LPTIM_CFG.CNTMEN bits are used for the clock source configuration. The active clock edge is configured through LPTIM_CFG.CLKPOL[1:0] bits.

When the LPTIM only uses external clock source. It can only select one active clock edge. LPTIM can select both active clock edges only when it is using internal clock source or both external and internal clock sources.

Note:when using both active edges for external clock, LPTIM needs to use an internal clock to oversample the external clock. The internal clock frequency should be at least 4 times higher than the external clock frequency.

22.4.2 Prescaler

The LPTIM counter is preceded by a configurable power-of-2 prescaler. The prescaler ratio is controlled by LPTIM_CFG.CLKPRE[2:0]. The table below lists all possible division ratios:

Table 22-1 Pre-scaler division ratios

Control Bits	The Corresponding Frequency Division factor
000	/1
001	/2
010	/4
011	/8
100	/16
101	/32
110	/64
111	/128

22.4.3 Glitch Filter

LPTIM has glitch filters for inputs to remove glitches and prevent unexpected counts or triggers.Glitch filter needs an internal clock source to operate. And the clock source should be provided before the glitch filter is enabled. This is necessary to guarantee the proper operation of the filters.

The glitch filters has two major purposes：

- For the external inputs: The filter sensitivity is configured through the LPTIM_CFG.CLKFLT[1:0] bits.

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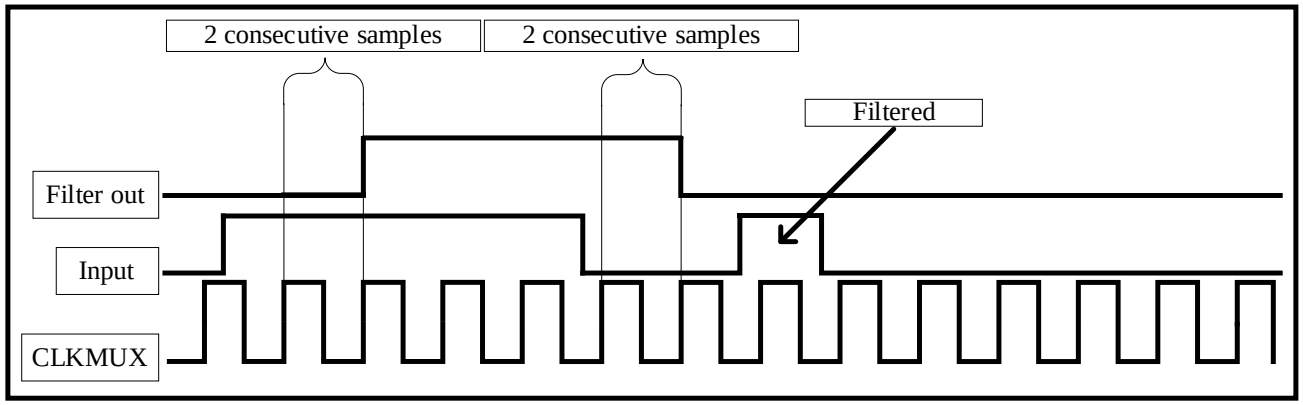
- For the internal trigger inputs: The filter sensitivity is configured through the LPTIM_CFG.RIGFLT[1:0] bits.

Note: The detection configuration is only applicable for its corresponding inputs.

The filter sensitivity acts on the number of consecutive equal samples that should be detected on one of the LPTIM inputs to consider a signal level change as a valid transition.

Figure 22-2 shows an example of glitch filter behavior when detected a 2 consecutive samples

Figure 22-2 Glitch filter timing diagram



Note: If no internal clock is used, the glitch filter needs to be turned off by clearing LPTIM_CFG.CLKFLT[1:0] and LPTIM_CFG.TRIGFLT[1:0] bits. If glitch filter is not used, the user can use a digital filter in the comparator or an external analog filter to remove the glitch.

22.4.4 Timer Enable

The LPTIM_CTRL.LPTIMEN bit is used to enable/disable the LPTIM kernel logic. After setting the LPTIM_CTRL.LPTIMEN bit, a delay of two counter clock is needed before the LPTIM is turned on.

The LPTIM_CFG and LPTIM_INTEN registers must be modified only when the LPTIM is turned off.

22.4.5 Trigger Multiplexer

The LPTIM counter can be triggered either by software or by an effective edge on one of the 10 trigger inputs. The trigger source is configured through LPTIM_CFG.TRGEN[1:0] bits. LPTIM_CFG.TRGEN[1:0] = '00', the trigger is selected as LPTIM_CTRL.TSTCM or LPTIM_CTRL.SNGMST bit, which can be set by software. The other values of LPTIM_CFG.TRGEN[1:0] are for the effective edge configuration of the trigger. The internal counter will start once an effective edge is detected.

LPTIM_CFG.TRGSEL[3:0] is used to select one of the 10 trigger inputs only when LPTIM_CFG.TRGEN[1:0] is not equal to '00'.

If LPTIM is using external trigger, which will be considered as asynchronous triggers. For asynchronous triggers, the LPTIM needs two counter clock cycles latency for synchronization.

If timeout function is disabled, new trigger event will be ignored if the LPTIM is already started.

Note: Any write to the LPTIM_CTRL.SNGMST/ LPTIM_CTRL.TSTCM bit will be discarded if the LPTIM is not enabled.

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Table 22-2 Trigger inputs corresponding to LPTIM_CFG.TRGSEL[3:0] Bits

Control Bits	Corresponding Trigger Input
0000	LPTIM_ETR Pin
0001	RTC alarm A
0010	RTC alarm B
0011	RTC_TAMP1
0100	RTC_TAMP2
0101	RTC_TAMP3
0110	COMP1_OUT
0111	COMP2_OUT
1000	COMP3_OUT
1001	COMP4_OUT

22.4.6 Operating Mode

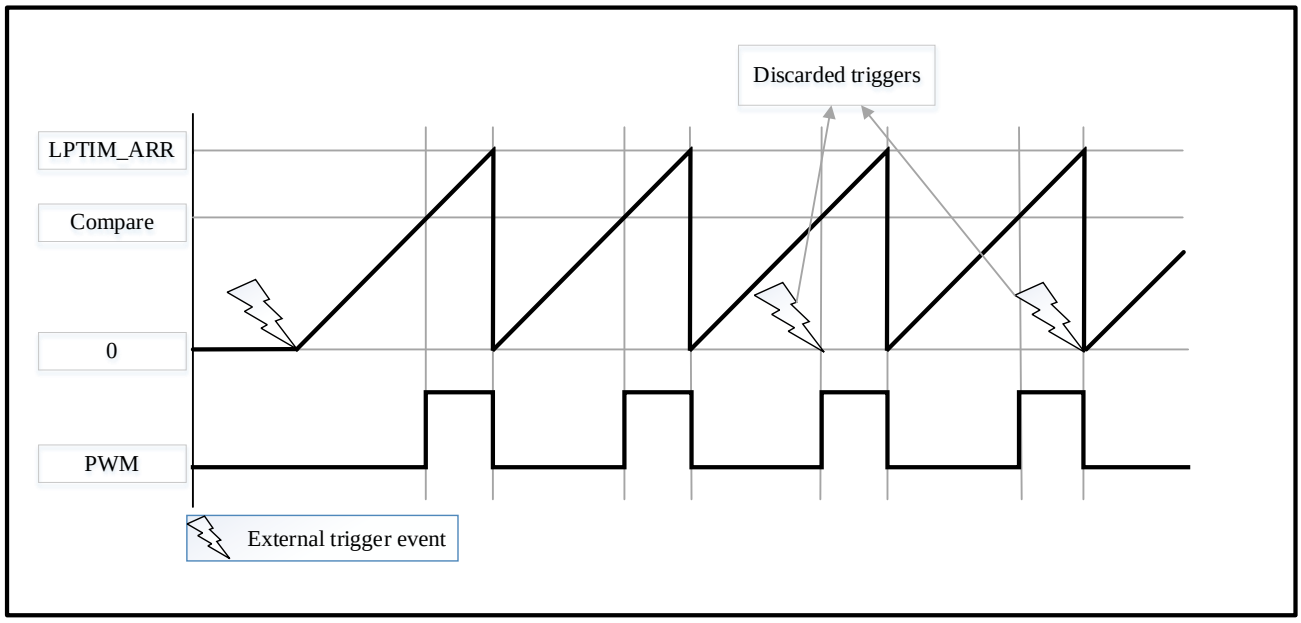
The LPTIM has two operating modes：

- Continuous mode: A trigger event will start the LPTIM and it will continue running until the user switched off the LPTIM.
- One-shot mode: A trigger event will start the LPTIM and it will stop when the counter value reaches LPTIM_ARR.ARRVAL[15:0].

Continuous mode:

LPTIM_CTRL.TSTCM bit must be set to enable the continuous mode. If LPTIM uses external trigger, the internal counter will start when an external trigger event arrives after LPTIM_CTRL.TSTCM bit is set. After the continuous mode starts, hardware will discard any subsequent external trigger event. Figure 22-3.

Figure 22-3 LPTIM Output Waveform, Continuous Counting Mode Configuration



PTIM_CTRL.SNGMST and LPTIM_CTRL.TSTCM bits can only be set when the LPTIM is enabled (The

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LPTIM_CTRL. LPTIMEN bit is set to ‘1’).

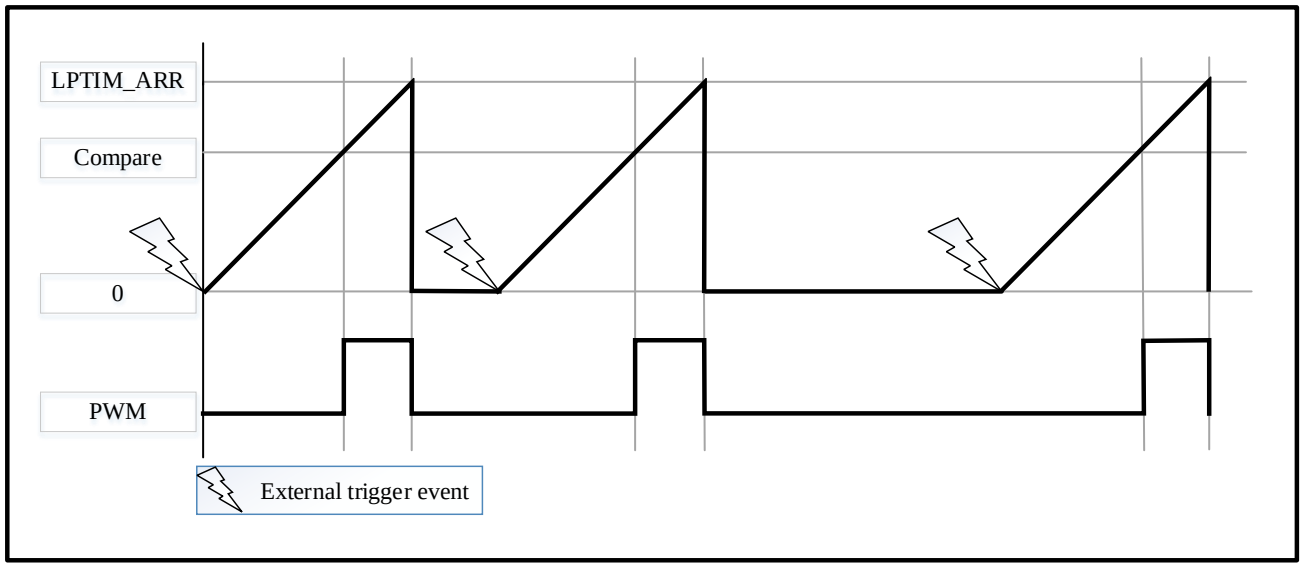
It is possible to switch from one-shot mode to continuous mode. Setting LPTIM_CTRL.SNGMST bit will switch the LPTIM to one-shot counting mode if continuous counting mode was previously selected. The counter stops as soon as it reaches the LPTIM_ARR register value. If the one-shot counting mode was previously selected, setting LPTIM_CTRL.TSTCM bit to 1 will switch the LPTIM to continuous counting mode. Counter will restart as soon as LPTIM_ARR register value is reached.

One-shot mode：

LPTIM_CTRL.SNGMST bit must be set to enable the one-shot mode. A trigger event will re-start the LPTIM. Hardware will abandon all the trigger events after the internal counter starts and before the counter value equal to LPTIM_ARR.ARRVAL[15:0] value.

If an external trigger is selected, each external trigger event arriving after the LPTIM_CTRL.SNGMST bit is set, and after the timer register is stopped (containing a zero value), the timer is restarted for a new count cycle, as shown in Figure Figure 22-4.

Figure 22-4 LPTIM Output Waveform, Single Counting Mode Configuration



Set-once mode actived：

The Set-once mode is used when the LPTIM_CFG.WAVE bit is set. In Set-once mode, the counter is started once when the first trigger event happens, the hardware will discard any subsequent trigger event, as shown Figure Figure 22-5.

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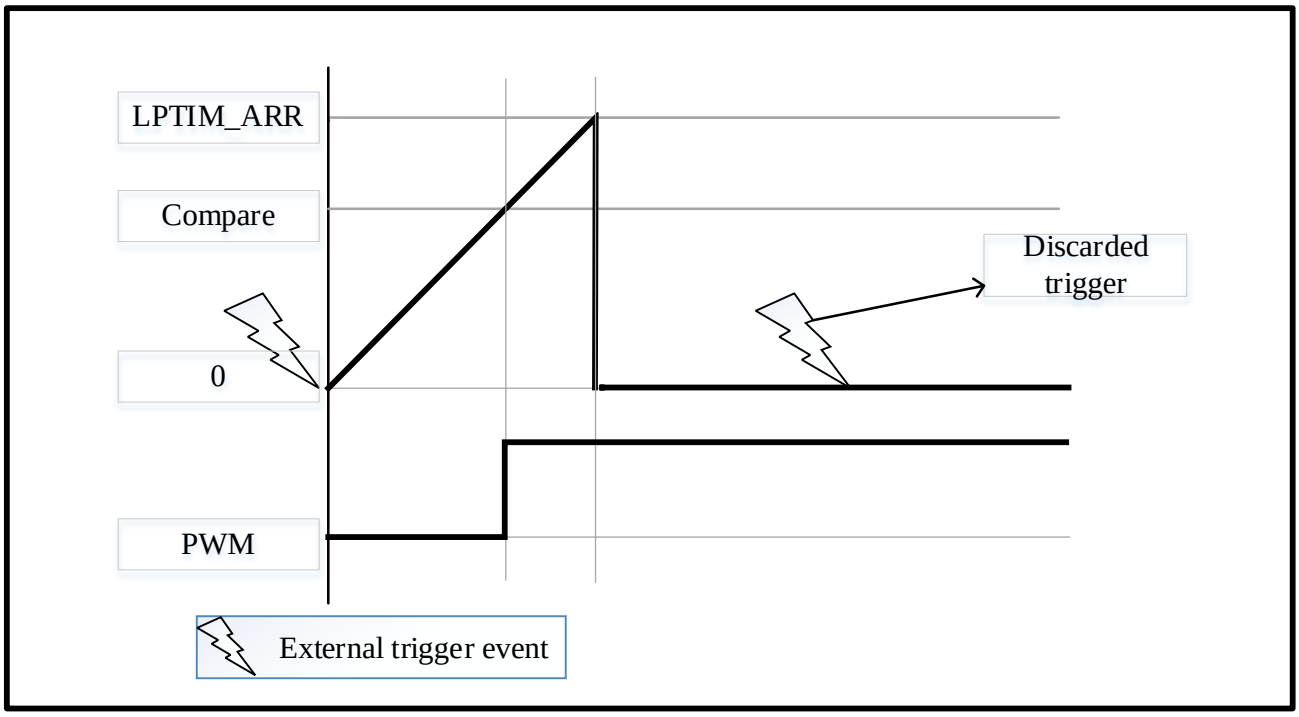
Figure 22-5 LPTIM Output Waveform, Single Counting Mode configCration And Set-One Mode Activated



In case of software start (LPTIM_CFG.TRGEN[1:0] = '00'), the LPTIM_CTRL.SNGMST setting will start the counter for one-shot counting.

22.4.7 Waveform Generation

The LPTIM auto-reload register (LPTIM_ARR) and compare register (LPTIM_CMP) are used for generating LPTIM output waveforms

The waveforms supported by LPTIM are shown as below：

- PWM mode: LPTIM output is set when a CMP match event happens. (I.E. the LPTIM_CNT register value matched the LPTIM_CMP register value.) The LPTIM output is reset when a ARR match happens. (I.E. the LPTIM_CNT register value matched the LPTIM_ARR register value).
- One-pulse mode: The first pulse is triggered same as PWM mode, then the output is permanently reset when the ARR match happens.
- Set-once mode: the output waveform is similar to the One-pulse mode except that the output is kept to the last signal level (depends on the output configured polarity).

Above waveform configuration require that LPTIM_ARR register value must be configured bigger than the LPTIM_CMP register value.

The LPTIM output waveform can be configured through the LPTIM_CFG.WAVE bit as follow：

- Clearing the LPTIM_CFG.WAVE bit will force the LPTIM to generate a PWM waveform or a One-pulse

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waveform depending on the set bit (LPTIM_CTRL.TSTCM or LPTIM_CTRL.SNGMST).

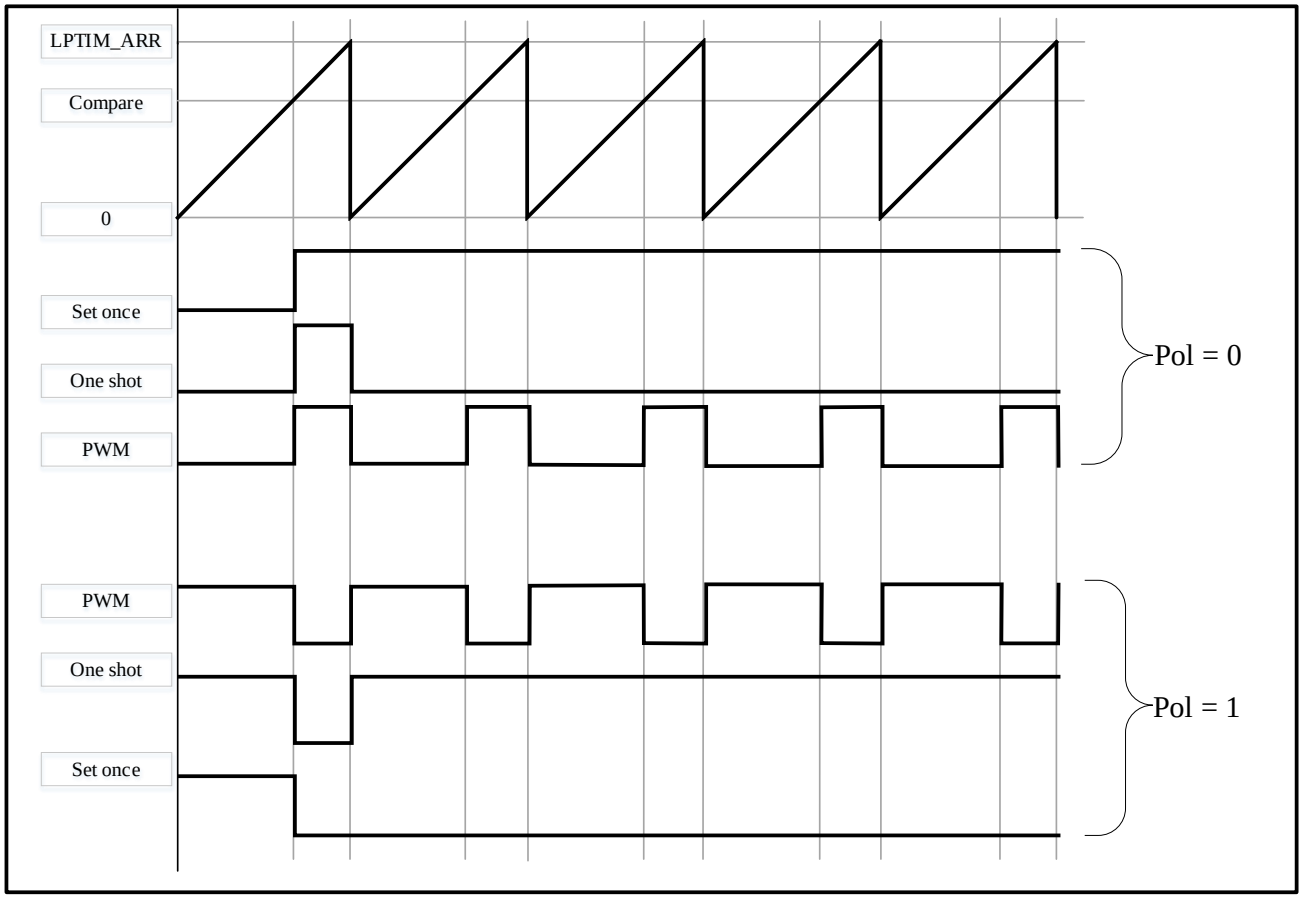
- LPTIM_CTRL.WAVE bit equals to '1' forces the LPTIM to generate a Set-once mode waveform.

The LPTIM_CFG.WAVEPOL bit controls LPTIM output polarity. The output default value will change immediately after the user configured the polarity, even when the timer is disabled.

Signals with frequencies up to the LPTIM clock frequency divided by 2 can be generated. Only when LPTIM counter counting external clock active edge can achieve clock frequency divided by 2. (I.E. LPTIM_CFG.CLKSEL=0, LPTIM_CFG.CLKPOL[1:0]=10, LPTIM_COMP.CMPVAL[15:0]='d1(50% duty cycle)/'d2, LPTIM_ARR.ARRVAL[15:0]='d3. d1,d2 and d3 means decimal 1, 2, 3).

Figure 22-6 below shows the three possible waveforms that can be generated on the LPTIM output. Also, it shows the effect of the polarity change using the LPTIM_CFG.WAVEPOL bit.

Figure 22-6 Waveform generation



22.4.8 Register Update

The LPTIM_ARR register and LPTIM_CMP register can be updated immediately after a software write operation. If the LPTIM is started, the LPTIM_ARR register and LPTIM_CMP register can be updated when counter overflow.

The LPTIM APB interface and the LPTIM kernel logic use different clocks, so there is some latency between the

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software write through APB bus and the moment when these values are available to the kernel logic. During this latency period, any additional write into these registers must be avoided。

The update method of LPTIM_ARR and LPTIM_CMP registers is determined by the LPTIM_CFG.RELOAD bit：

- LPTIM_CFG.RELOAD bit equals to '1': LPTIM_ARR and LPTIM_CMP registers are updated when counter overflow, if the LPTIM already started. When counter overflow, latency = 2~3 APB clock period.
- LPTIM_CFG.RELOAD bit equals to '0': LPTIM_ARR and LPTIM_CMP registers are updated after any software write access. Latency = 2~3 APB clock period + 2~3 LPTIM internal prescaled clock period.

The LPTIM_INTSTS.ARRUPD flag and the LPTIM_INTSTS.CMPUPD flag indicate when the write operation is completed to respectively the LPTIM_ARR register and the LPTIM_COMP register.

After a write to the LPTIM_ARR register or the LPTIM_CMP register, any successive write before respectively the LPTIM_INTSTS.ARRUPD flag or the LPTIM_INTSTS.CMPUPD flag be set, will lead to unpredictable results. So a new write operation to the same register can only be performed when the previous write operation is completed.

22.4.9 Counter Mode

The internal counter can count external trigger events from LPTIM Input1 or internal clock cycles. This can be configured through LPTIM_CFG.CLKSEL and LPTIM_CFG.CNTMEN bits.

If LPTIM is counting external triggers, user can configure LPTIM_CFG.CLKPOL[1:0] bits to select the active edge from rising edge, falling edge or both edges. The count modes below can be selected, depending on LPTIM_CFG.CLKSEL and LPTIM_CFG.CNTMEN bits values：

- LPTIM_CFG.CLKSEL = 0: the LPTIM use an internal clock source to clock。
  - LPTIM_CFG.CNTMEN=0, The LPTIM is configured to be clocked by an internal clock source and the LPTIM counter is configured to be updated following each internal clock pulse.
  - LPTIM_CFG.CNTMEN=1, The LPTIM external Input1 is sampled with the internal clock provided to the LPTIM. In order to not miss any event, the frequency of the changes on the external Input1 signal should never exceed the frequency of the internal clock provided to the LPTIM. Also, the internal clock provided to the LPTIM must not be pre-scaled (LPTIM_CFG.CLKPRE[2:0] = 000).
- LPTIM_CFG.CLKSEL = 1: the LPTIM use an external clock source to clock。
  - LPTIM_CFG.CNTMEN bit value is don't care. In this configuration, the LPTIM has no need for an internal clock source (except if the glitch filters are enabled). The signal injected on the LPTIM external Input1 is used as system clock for the LPTIM. This configuration is suitable for operation modes where no embedded oscillator is enabled.
  - For this configuration, the LPTIM counter can be updated either on rising edges or falling edges of the input1 clock signal but not on both rising and falling edges.
  - Since the signal injected on the LPTIM external Input1 is also used to clock the LPTIM kernel logic, there is some initial latency (after the LPTIM is enabled) before the counter is incremented. More precisely, the first five active edges on the LPTIM external Input1 (after LPTIM is enable) are lost.

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22.4.10 Encode Mode

The Encoder mode can handle signals from quadrature encoders which used to detect angular position of rotary elements. The encoder mode allows the counter counts the events within 0 and LPTIM_ARR.ARRVAL[15:0] value. (0 up to LPTIM_ARR.ARRVAL[15:0] or LPTIM_ARR.ARRVAL[15:0] to 0). In this case, user must configure LPTIM_ARR.ARRVAL[15:0] before enable the counter. From external Input1 and Input2, a clock is generated for the counter. The counting direction depends on the phase between these two input signals.

The Encoder mode is only available when the LPTIM use an internal clock source to clock. The signals frequency on both Input1 and Input2 inputs must not exceed the LPTIM internal clock frequency divided by 4. This is mandatory in order to guarantee a proper operation of the LPTIM.

The change of counting direction is updated by the two Down and Up flags in the LPTIM_INTSTS register. Also, an interrupt can be generated for both direction change events if enabled through the LPTIM_INTEN.DOWNIE and LPTIM_INTEN.UPIE register.

User can enable Encoder mode by setting LPTIM_CFG.ENC bit. And the LPTIM need to be configured in continuous mode first.

When Encoder mode is active, the LPTIM counter is modified automatically following the speed and the direction of the incremental encoder. Therefore, its content always represents the encoder's position. The count direction, signaled by the Up and Down flags, correspond to the rotation direction of the encoder rotor.

Different counting scenarios may occur based on the different trigger edges configured by the LPTIM_CFG.CLKPOL[1:0] bits. The following table summarizes the possible combinations, assuming that Input1 and Input2 do not switch at the same time.

Table 22-3 Encoder Counting Scenarios

Trigger edge	The signals is opposite（Input1 For Input2, Input2 For Input1）	Input1 Signal		Input2 Signal	
		Rising	Falling	Rising	Falling
Rising Edge	High	Down	No count	Up	No count
	Low	Up	No count	Down	No count
Falling Edge	High	No count	Up	No count	Down
	Low	No count	Down	No count	Up
Both Edges	High	Down	Up	Up	Down
	Low	Up	Down	Down	Up

The following figure shows a counting sequence for Encoder mode where both-edge polarity is configured.

Caution: *In this mode the LPTIM must be clocked by an internal clock source, so the LPTIM_CFG.CLKSEL bit must be maintained to its reset value which is equal to '0'. Also, the prescaler division ratio must be equal to its reset value which is 1 (LPTIM_CFG.CLKPRE[2:0] bits must be '000').*

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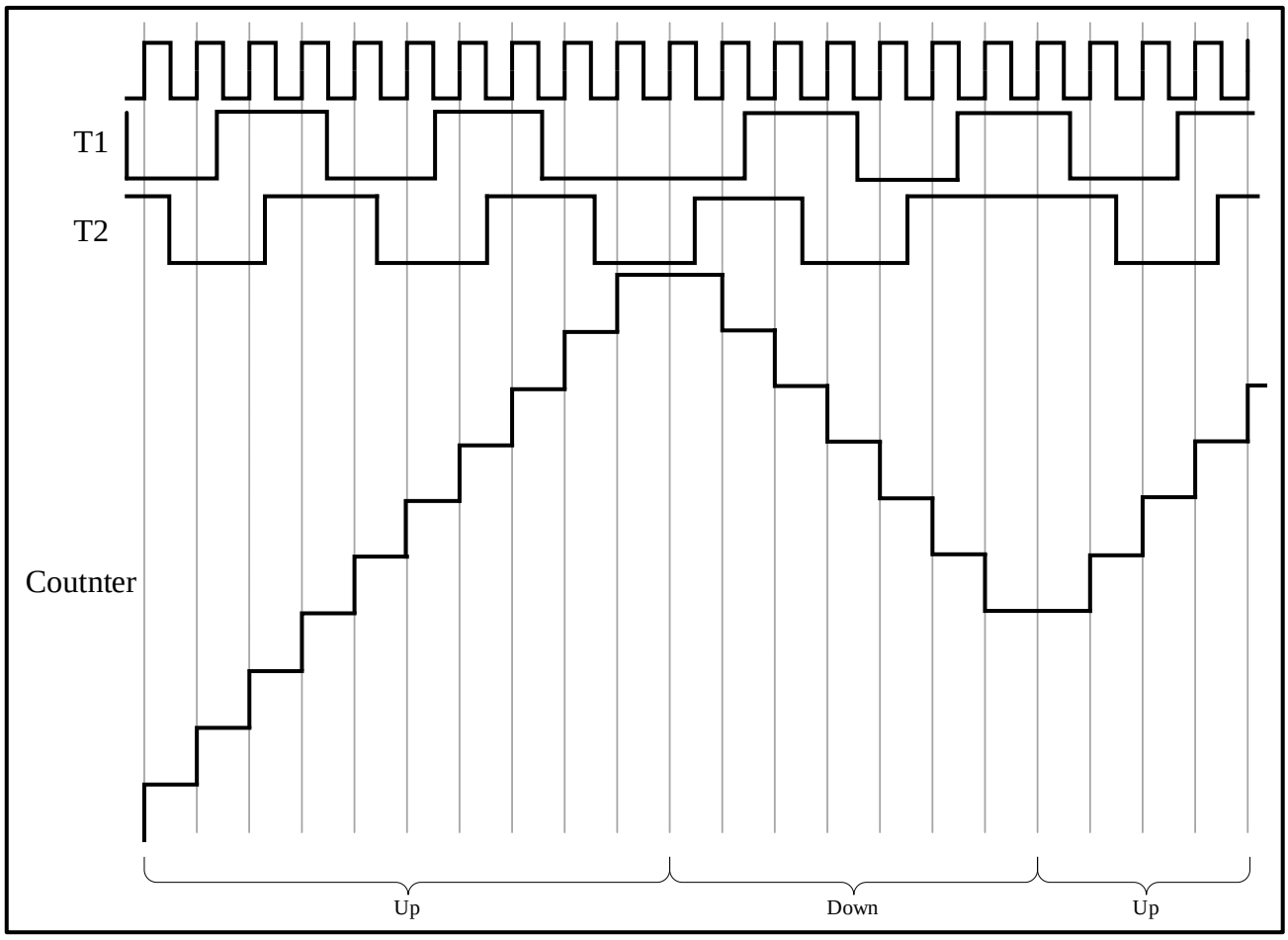
Figure 22-7 Encoder Mode Counting Sequence



22.4.11 Non-Quadrature Encoder Mode

This mode allows handling signals from non-quadrature encoders, which is used to detect sub-sequent positive pulses from external interface. Non-Encoder interface mode acts simply as an external clock with direction selection. This means that the counter just counts continuously between 0 and the auto-reload value programmed into the LPTIM_ARR register (0 up to LPTIM_ARR.ARRVAL[15:0] or LPTIM_ARR.ARRVAL[15:0] down to 0 depending on the direction). Therefore you must configure LPTIM_ARR before starting. From the two external input signals, Input1 and Input2, a clock signal is generated to clock the LPTIM counter. The order between those two signals determines the counting direction.

The Non-Encoder mode is only available when the LPTIM is clocked by an internal clock source. The signals frequency on both Input1 and Input2 inputs must not exceed the LPTIM internal clock frequency divided by 4. This is mandatory in order to guarantee a proper operation of the LPTIM.

Direction change is signalized by the two Down and Up flags in the LPTIM_INTSTS register. Also, an interrupt can be generated for both direction change events if enabled through the LPTIM_INTEN.DOWNIE and LPTIM_INTEN.UPIE register。

To activate the Non-Encoder mode the LPTIM_CFG.NENC bit has to be set to ‘1’. The LPTIM must first be configured in Continuous mode.

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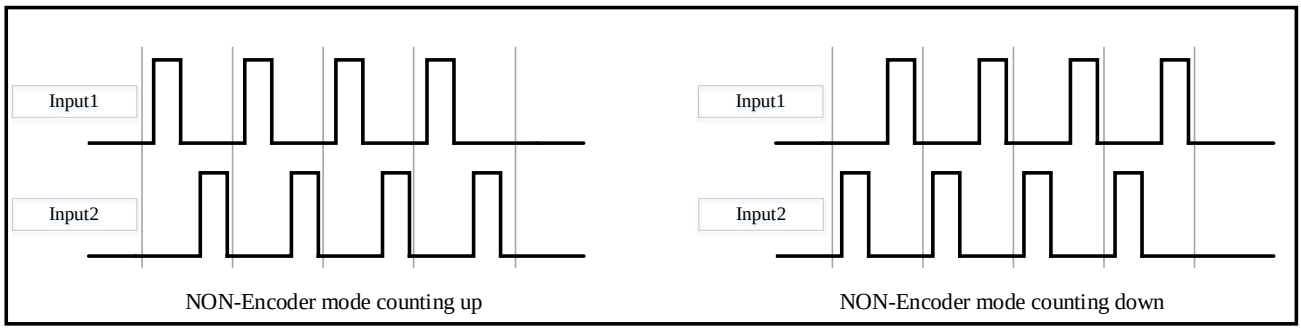
When Non-Encoder mode is active, the LPTIM counter is modified automatically following the speed and the direction of the incremental encoder. Therefore, its content always represents the encoder's position. The count direction, signaled by the Up and Down flags, correspond to the rotation direction of the encoder rotor.

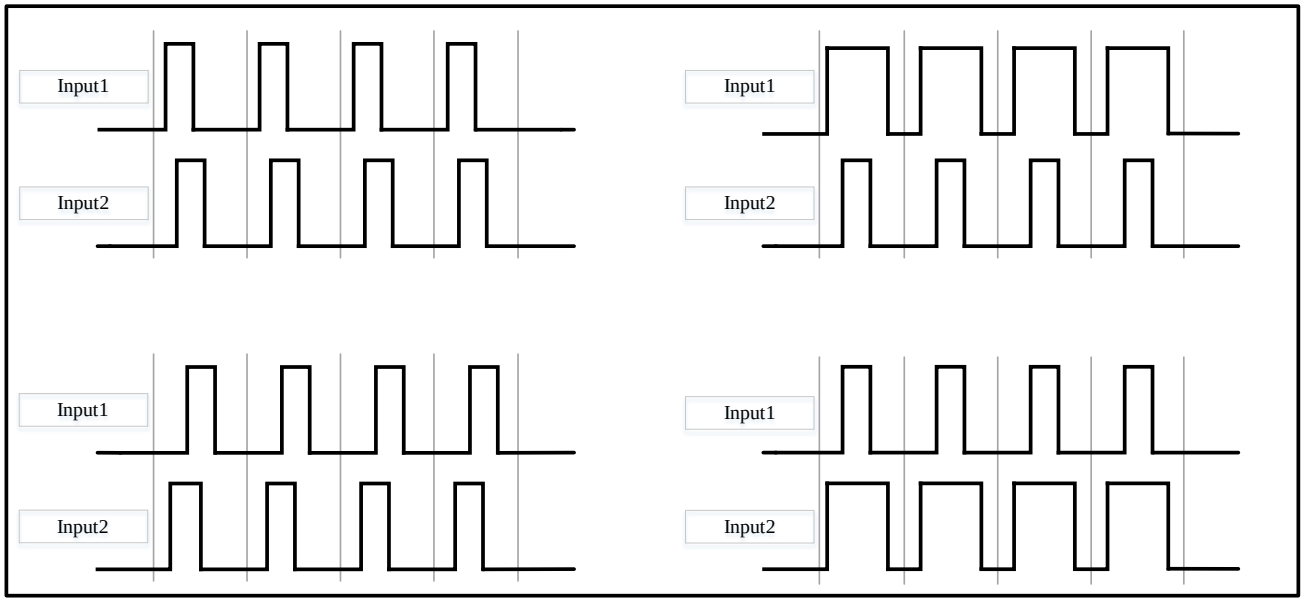
Figure 22-8 shown, the decoder module can work properly, when there is no case that both Input1 and Input2 are high

Figure 22-8 Input waveforms of Input1 and Input2 when the decoder module is working normally



If the Input1 and Input2 waveform is as Figure 22-9, the decoder module can't work properly. The counter will ignore these waveforms and keep the previous value.

Figure 22-9 Input1 and Input2 input waveforms when decoder module is not working



22.4.12 Timeout Function

When the LPTIM_CFG.TIMOUTEN bit is enable, the LPTIM counter will be reset by an active edge from one selected trigger input.

When timeout function is used, the LPTIM counter will be reset and re-start by a selected trigger input event. If no trigger occurs within the configured time, the compare match event will happen. The waiting time is configured through the timeout value.

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22.4.13 LPTIM Interrupts

The following events generate an interrupt/wake-up event, if they are enabled through the LPTIM_INTEN register:

- Compare match.
- Auto-reload match (whatever the direction if encoder mode).
- External trigger event.
- Autoreload register write completed.
- Compare register write completed.
- Direction change (encoder mode), programmable (up / down / both).

Note: If any bit in the LPTIM_INTEN register (Interrupt Enable Register) is set after that its corresponding flag in the LPTIM_INTSTS register (Status Register) is set, the interrupt is not asserted.

Table 22-4 Interruption Events

Interrupt Event	Description
Compare match	Interrupt flag LPTIM_INSTS.CMPM is set when LPTIM_CNT(counter register value) = LPTIM_COMP(compare register value).
Auto reload match	Interrupt flag LPTIM_INSTS.ARRM is set when LPTIM_CNT(counter register value) = LPTIM_ARR (auto-reload register value)
External trigger event	Interrupt flag LPTIM_INSTS.EXTRIG is set when an external trigger event is detected
Autoreload register write completed	Interrupt flag LPTIM_INSTS.CMPUPD is set when the write operation to the LPTIM_ARR register is complete
Compare register write completed	Interrupt flag LPTIM_INSTS.ARRUPD is set when the write operation to the LPTIM_COMP register is complete
Direction change	Used in Encoder mode. Two interrupt flags are embedded to signal direction change： - LPTIM_INSTS.Up flag indicated that the count direction is changed to count up - LPTIM_INSTS.Down flag indicated that the count direction is changed to count down.

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22.5 LPTIM Registers

22.5.1 LPTIM Interrupt And Status Register（LPTIM_INTSTS）

Offset address：0x00

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									DOWN	UP	ARRUPD	CMPUPD	EXTRIG	ARRM	CMPM
									r	r	r	r	r	r	r

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	DOWN	Change counter direction to down. In Encoder mode, hardware will set DOWN bit to inform the application the counter direction.
5	UP	Change counter direction up. In Encoder mode, hardware will set UP bit to inform the application the counter direction.
4	ARRUPD	Auto-reload value updated to register. Hardware sets ARRUPD to inform application that LPTIM_ARR register has been written by the APB bus successfully. For more details, see 22.4.8
3	CMPUPD	Compare value updated to register. Hardware sets COMPUPD to inform application that LPTIM_COMP register has been written by the APB bus successfully. For more details, see 22.4.8
2	EXTRIG	External trigger valid event. Hardware sets EXTRIG to inform application that a valid external trigger edge has occurred. If the trigger is discarded when timer has already started, then this flag is not set.
1	ARRM	Auto-reload match. Hardware set this to inform application that LPTIM_CNT register value reached the LPTIM_ARR register's value.
0	CMPM	Compare match. Hardware set this to inform application that LPTIM_CNT register value reached the LPTIM_COMP register's value.

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22.5.2 LPTIM Interrupt Clear Register（LPTIM_INTCLR）

Offset address：0x04

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									DOWNCF	UPCF	ARRUPDCF	CMPUPDCF	EXTRIGCF	ARRMCF	CMPMCF
									w	w	w	w	w	w	w

Bit Field	Name	Description
31：7	Reserved	Reserved, the reset value must be maintained.
6	DOWNCF	Direction change to down Clear Flag Writing 1 to this bit clear the DOWN flag in the LPTIM_INTSTS register
5	UPCF	Direction change to UP Clear Flag Writing 1 to this bit clear the UP flag in the LPTIM_INTSTS register
4	ARRUPDCF	Autoreload register update completed Clear Flag Writing 1 to this bit clears the ARRUPD flag in the LPTIM_INTSTS register
3	CMPUPDCF	Compare register update completed Clear Flag Writing 1 to this bit clears the CMPUPD flag in the LPTIM_INTSTS register
2	EXTRIGCF	External trigger valid edge Clear Flag Writing 1 to this bit clears the EXTRIG flag in the LPTIM_INTSTS register
1	ARRMCF	Autoreload match Clear Flag Writing 1 to this bit clears the ARRM flag in the LPTIM_INTSTS register
0	CMPMCF	compare match Clear Flag Writing 1 to this bit clears the CMPM flag in the LPTIM_INTSTS register

22.5.3 LPTIM Interrupt Enable Register（LPTIM_INTEN）

Offset address：0x08

Reset value：0x0000 0000

Note: The LPTIM_INTEN register must only be modified when the LPTIM is disabled (LPTIM_CTRL.LPTIMEN bit reset to '0')

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									DOWNIE	UPIE	ARRUPDIE	CMPUPDIE	EXTRIGIE	ARRMIE	CMPMIE

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rw	rw	rw	rw	rw	rw	rw	

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	DOWNIE	Direction change to down interrupt enable bit. 0: DOWN interrupt disabled 1: DOWN interrupt enabled
5	UPIE	Direction change to up interrupt enable bit. 0: UP interrupt disabled 1: UP interrupt enabled
4	ARRUPDIE	Auto reload register update succeeded interrupt enable bit. 0: ARRUPD interrupt disable 1: ARRUPD interrupt enable
3	CMPUPDIE	Compare register update succeeded interrupt enable bit. 0: CMPUPD interrupt disabled 1: CMPUPD interrupt enabled
2	EXTRIGIE	External trigger valid edge interrupt enable bit. 0: EXTRIG interrupt disabled 1: EXTRIG interrupt enabled
1	ARRMIE	Auto reload match interrupt enable bit. 0: ARRM interrupt disabled 1: ARRM interrupt enabled
0	CMPMIE	Compare match interrupt enable bit. 0: CMPM interrupt disabled 1: CMPM interrupt enabled

22.5.4 LPTIM Configuration Register（LPTIM_CFG）

Offset address：0x0C

Reset value：0x0000 0000

Note: The LPTIM_CFG register must only be modified when the LPTIM is disabled (LPTIM_CTRL.LPTIMEN bit reset to '0')

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						NENC	ENC	CNTMEN	RELOAD	WAVEPOL	WAVE	TIMOUTEN	TRGEN[1:0]		TRGSEL[3]
						rw	rw	rw	rw	rw	rw	rw	rw		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRGSEL[2:0]			Reserved	CLKPRE[2:0]			Reserved	TRIGFLT[1:0]		Reserved	CLKFLT[1:0]		CLKPOL[1:0]		CLKSEL
rw				rw				rw			rw		rw		rw

Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	NENC	Non-orthogonal mode enable 0: Non-orthogonal Encoder mode disabled

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Bit Field	Name	Description
		1: Non-orthogonal Encoder mode enabled
24	ENC	Encoder mode enable 0: Encoder mode disabled 1: Encoder mode enabled
23	CNTMEN	counter mode enabled The CNTMEN bit selects clock source for the LPTIM counter: 0: Counter is incremented following each internal clock pulse 1: Counter is incremented following each valid clock pulse on the LPTIM external Input1
22	RELOAD	Registers update mode The RELOAD bit controls the LPTIM_ARR and the LPTIM_COMP registers update mode 0: Registers are updated after each APB bus write access 1: Registers are updated at the end of the current LPTIM period
21	WAVEPOL	Waveform shape polarity The WAVEPOL bit controls the output polarity 0: The LPTIM output reflects the compare results between LPTIM_ARR and LPTIM_CMP registers 1: The LPTIM output reflects the inverse of the compare results between LPTIM_ARR and LPTIM_CMP registers
20	WAVE	Waveform shape The WAVE bit controls the output shape 0: Deactivate Set-once mode, PWM / One Pulse waveform (depending on LPTIM_CTRL.TSTCM or LPTIM_CTRL.SNGMST bit) 1: Activate the Set-once mode
19	TIMOUTEN	Timeout enable 0: A trigger event arriving when the timer is already started will be ignored 1: A trigger event arriving when the timer is already started will reset and restart the counter
18:17	TRGEN[1:0]	Trigger enable and polarity The TRGEN bits controls whether the LPTIM counter is started by an external trigger or not. If the external trigger option is selected, three configurations are possible for the trigger active edge: 00: Software trigger (counting start is initiated by software) 01: Falling edge is the active edge 10: rising edge is the active edge 11: Both edges are active edges
16:13	TRGSEL[3:0]	Trigger selector The TRGSEL bits select the trigger source that will serve as a trigger event for the LPTIM among the below 13 available sources: 0000：LPTIM_ETR Pin 0001：RTC alarm A

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Bit Field	Name	Description
		0010：RTC alarm B 0011：RTC_TAMP1 0100：RTC_TAMP2 0101：RTC_TAMP3 0110：COMP1_OUT 0111：COMP2_OUT 1000：COMP3_OUT 1001：COMP4_OUT Other: reserved
12	Reserved	Reserved, the reset value must be maintained.
11:9	CLKPRE[2:0]	Clock division factor bit. 000：/1 001：/2 010：/4 011：/8 100：/16 101：/32 110：/64 111：/128
8	Reserved	Reserved, the reset value must be maintained.
7:6	TRIGFLT[1:0]	Configure the data filter trigger bit. The TRIGFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an internal trigger before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: Any trigger active level change is considered as a valid trigger. 01: Trigger active level change must be stable for at least 2 clock periods before it is considered as valid trigger. 10: Trigger active level change must be stable for at least 4 clock periods before it is considered as valid trigger. 11: Trigger active level change must be stable for at least 8 clock periods before it is considered as valid trigger.
5	Reserved	Reserved, the reset value must be maintained.
4:3	CLKFLT[1:0]	Digital filter external clock input configuration The CLKFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an external clock signal before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: Any external clock signal level change is considered as a valid transition. 01: External clock signal level change must be stable for at least 2 clock periods before it is considered as valid transition. 10: External clock signal level change must be stable for at least 4 clock periods before it is considered as valid transition. 11: External clock signal level change must be stable for at least 8 clock periods

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Bit Field	Name	Description
		before it is considered as valid transition.
2:1	CLKPOL[1:0]	Clock Polarity If LPTIM is clocked by an external clock source: When the LPTIM is clocked by an external clock source, CLKPOL bits is used to configure the active edge or edges used by the counter: 00: The rising edge is the active edge used for counting 01: The falling edge is the active edge used for counting 10: Both edges are active edges. 11: Not allowed *Note: When both external clock signal edges are considered active ones, the LPTIM must also be clocked by an internal clock source with a frequency equal to at least four time the external clock frequency.* If the LPTIM is configured in Encoder mode (LPTIM_CFG.ENC bit is set): 00: The encoder rising edgecounting mode. 01: The encoder falling edge counting mode. 10: The encoder both edges counting mode.
0	CLKSEL	Clock selector The CKSEL bit selects which clock source the LPTIM will use: 0: LPTIM is clocked by internal clock source (APB clock or any of the embedded oscillators) 1: LPTIM is clocked by an external clock source through the LPTIM external Input1

22.5.5 LPTIM Control Register（LPTIM_CTRL）

Offset address：0x10

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													TSTCM	SNGMST	LPTIMEN
													rw	rw	rw

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	TSTCM	Timer start in Continuous mode This bit is set by software and cleared by hardware. In case of software start (LPTIM_CFG.TRGEN[1:0] = ‘00’), setting this bit starts the LPTIM in Continuous mode. If the software start is disabled (TRGEN[1:0] ≠ ‘00’), setting this bit starts the timer in

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Bit Field	Name	Description
		Continuous mode as soon as an external trigger is detected. If this bit is set when a single pulse mode counting is ongoing, then the timer will not stop at the next match between the LPTIM_ARR and LPTIM_CNT registers and the LPTIM counter keeps counting in Continuous mode. This bit can be set only when the LPTIM is enabled. It will be automatically reset by hardware.
1	SNGMST	LPTIM start in Single pulse mode This bit is set by software and cleared by hardware. In case of software start (LPTIM_CFG.TRGEN[1:0] = '00'), setting this bit starts the LPTIM in single pulse mode. If the software start is disabled (LPTIM_CFG.TRGEN[1:0] ≠ '00'), setting this bit starts the LPTIM in single pulse mode as soon as an external trigger is detected. If this bit is set when the LPTIM is in continuous counting mode, then the LPTIM will stop at the following match between LPTIM_ARR and LPTIM_CNT registers. This bit can only be set when the LPTIM is enabled. It will be automatically reset by hardware.
0	LPTIMEN	LPTIM enable The LPTIMEN bit is set and cleared by software. 0: LPTIM is disabled 1: LPTIM is enabled

22.5.6 LPTIM Compare Register（LPTIM_CMP）

Offset address：0x14

Reset value：0x0000 0000

Note: The LPTIM_CMP register must only be modified when the LPTIM is enabled (LPTIM_CTRL.LPTIMEN bit reset to '1')

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPVAL[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CMPVAL[15:0]	Compare value CMPVAL is the compare value used by the LPTIM.

22.5.7 LPTIM Auto-Reload Register（LPTIM_ARR）

Offset address：0x18

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Reset value：0x0000 0001

Note: The LPTIM_ARR register must only be modified when the LPTIM is enabled (LPTIM_CTRL.LPTIMEN bit reset to '1')

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARRVAL[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	ARRVAL[15:0]	Auto reload value ARRVAL is the autoreload value for the LPTIM. This value must be strictly greater than the LPTIM_COMP.CMPVAL[15:0] value.

22.5.8 LPTIM Counter Register（LPTIM_CNT）

Offset address：0x1C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTVAL[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CNTVAL[15:0]	Counter value When the LPTIM is running with an asynchronous clock, reading the LPTIM_CNT register may return unreliable values. So in this case it is necessary to perform two consecutive read accesses and verify that the two returned values are identical. If identical, the reading is reliable.

22.5.9 LPTIM Option Register（LPTIM_OPT）

Offset address：0x20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	OPT2[2:0]	OPT1[2:0]
	rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:3	OPT2[2:0]	LPTIM Input2 Connection selection bit 000：LPTIM Input 2 connection to I/O 100：LPTIM Input 2 connection to COMP1_OUT 101：LPTIM Input 2 connection to COMP2_OUT 110：LPTIM Input 2 connection to COMP3_OUT 111：LPTIM Input 2 connection to COMP4_OUT Other: reserved
2:0	OPT1[2:0]	LPTIM Input1 Connection selection bit 000：LPTIM Input 1 connection to I/O 100：LPTIM Input 1 connection to COMP1_OUT 101：LPTIM Input 1 connection to COMP2_OUT 110：LPTIM Input 2 connection to COMP3_OUT 111：LPTIM Input 1 connection to COMP4_OUT Other: reserved

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Email: sales@nsing.com.sg

23 Independent Watchdog（IWDG）

23.1 Introduction

The Chip has embedded independent watchdog (IWDG) and window watchdog (WWDG) timers to solve the problems caused by software errors. The watchdog timer is very flexible to use, which improves the security of the system and the accuracy of timing control

The independent Watchdog (IWDG) is driving by Low-speed internal clock (LSI clock) running at 32KHz, which will still running event dead loop or MCU stuck is happening. This can provide higher safety level, timing accuracy and flexibility of watchdog. It can reset and resolve system malfunctions due to software failure. The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.

When the IWDG counter reaches 0, a system reset will be generated.

23.2 Main Features

- Independent 12-bit down-counter
- RC oscillator provides independent clock source, which can also operate in SLEEP, STOP0 and STANDBY mode
- Reset and low-power wake-up can be matched
- A system reset occurs when the down counter reaches 0x0000 (if watchdog activated)

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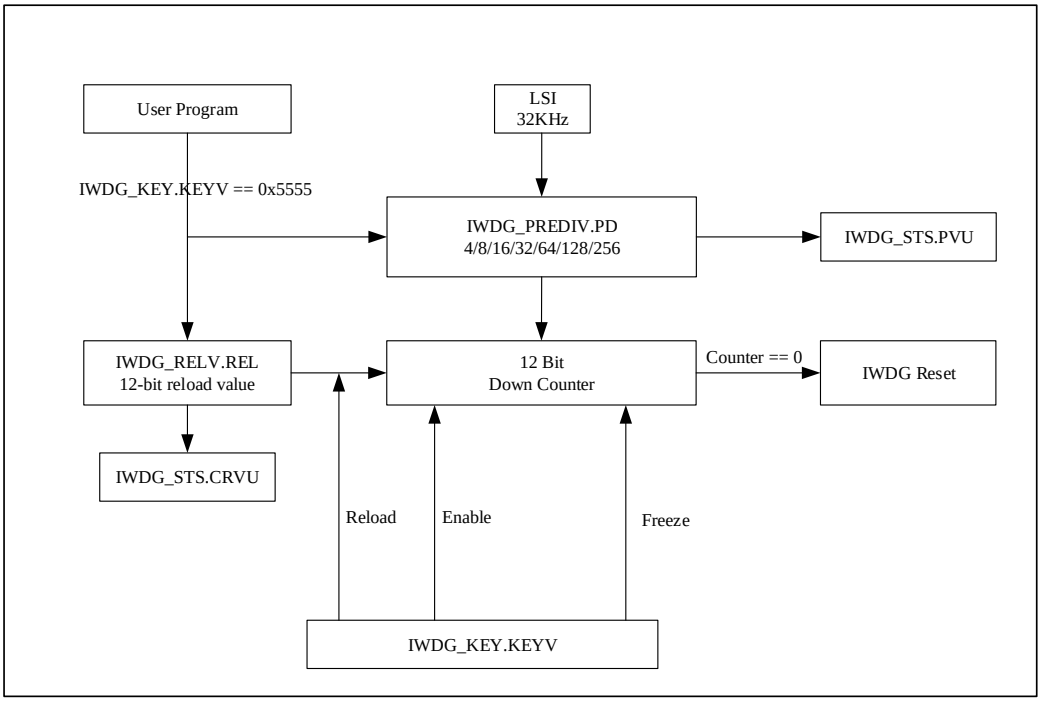
23.3 Function Description

Figure 23-1 Functional Block Diagram Of The Independent Watchdog Module



Note: Watchdog function is in V_{DD} power supply area, and it can still work normally in SLEEP, STOP0 and STANDBY modes.

To enable IWDG, we need to write 0xCCCC to IWDG_KEY.KEYV[15:0] bits. Counter starts counting down from reset value (0xFFF). When counter count to 0x000, it generates a reset signal (IWDG_RESET) to MCU. Other than that, as long as 0xAAAA (reload request) is write to IWDG_KEY.KEYV[15:0] bits before reset, the counter value is set to the reload value in the IWDG_RELV.REL[11:0] bits and prevents the watchdog from resetting the entire device.

If the "hardware watchdog timer" function is enabled through the selection byte, the watchdog will automatically start running after the system is powered on and will generate a system reset, unless the software reloads the counter before it reaches ‘0’.

23.3.1 Register Access Protection

IWDG_PREDIV and IWDG_RELV register are write protected. To modify the value of those two register, user needs to write 0x5555 to IWDG_KEY.KEYV[15:0] bits. Writing other value enables write protections again. IWDG_STS.PVU indicates whether the pre-scaler value update is on going. IWDG_STS.CRVU indicates whether the IWDG is updating the reload value. The hardware sets the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit when the pre-scaler value and/or reload value is updating. After the pre-scaler value and/or reload value update is complete, the hardware clears the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit.

The reload operation (IWDG_KEY.KEYV[15:0] configured with value of 0xAAAA) will also cause the registers to become write protected again.

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23.3.2 Debug Mode

In debug mode (Cortex-M4F_HALTED or Cortex-M7F_HALTED), IWDG counter will either continue to work normally or stops, depending on DBG_M7APB5FZ [7:6]/ DBG_M4APB5FZ[7:6] bits in Debug Support module. If this bit is set to '1', the counter stops. The counter works normally when the bit is '0'.See the Section on DEBUG Support 50.1 for details.

23.3.3 IWDG Freeze

Once the IWDG is enabled, either by hardware or software, the IWDG will not stop counting unless a system reset is generated or runtime freeze is configured by writing 0x4567 to IWDG_KEY.KEYV[15:0] bits. Users can also configure IWDG freeze in certain operating modes. IWDG provides freeze options in SLEEP, STOP0, and STANDBY modes. When the IWDG is enabled, it forces the LSI clock to turn on.

23.4 User Interface

IWDG module user interface contains 4 registers: Key Register (IWDG_KEY), Pre-scale Register (IWDG_PREDIV), Reload Register (IWDG_RELV) and Status Register (IWDG_STS).

23.4.1 Operate Process

When IWDG is reset enabled by software (write 0xAAAA to IWDG_KEY.KEYV[15:0] bits) or hardware, it starts counting down from 0xFFF. Down counting gap is determined by pre-scale LSI clock. Once the counter is reloaded, each new round will start from the value in IWDG_RELV.REL[11:0] instead of 0xFFF.

When program is running normally, software needs to feed IWDG before counter reaches 0 and start a new round of down counting. When counter reaches 0, this indicates program malfunction. IWDG generates reset signal under this circumstance.

If user wants to configure IWDG prescaler and reload value register, it needs to write 0x5555 to IWDG_KEY.KEYV[15:0] first, then confirm IWDG_STS.CRVU bit and IWDG_STS.PVU bit. IWDG_STS.CRVU bit indicates reload value update is ongoing, IWDG_STS.PVU indicates prescale divider ratio is updating. Only when those two bit are 0 then user can update corresponding value. When update is on-going, hardware sets corresponding bit to 1. At this time, reading IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] is invalid since data needs to be synchronized to LSI clock domain. The value read from IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] will be valid after hardware clears the IWDG_STS.PVU bit or IWDG_STS.CRVU bit.

If the application uses more than one reload value or pre-scaler value, it must wait until the IWDG_STS.CRVU bit is reset before changing the reload value, the same as changing the pre-scaler value. However, after updating the pre-scale and/or the reload value, it is not necessary to wait until IWDG_STS.CRVU bit or IWDG_STS.PVU bit are reset before continuing code execution (even in case of low-power mode entry, the write operation is taken into account and will complete).

Prescale register and reload register controls the time that generates reset, as shown in Table 23-1.

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Table 23-1 IWDG Counting Maximum And Minimum Reset Time

Pre-Scale Factor	PD[2:0]	Minmum（ms） RL[11:0]=0	Maximum（ms） RL[11:0]=0xFFF
/4	000	0.125	512
/8	001	0.25	1024
/16	010	0.5	2048
/32	011	1.0	4096
/64	100	2.0	8192
/128	101	4.0	16384
/256	11x	8.0	32768

23.4.2 IWDG Configuration Flow

Software flow：

1. Write 0x5555 to IWDG_KEY.KEYV[15:0] bits to enable write access of IWDG_PREDIV and IWDG_RELV registers；
2. Check IWDG_STS.PVU bit or IWDG_STS.CRVU bit, if they are 0, continue next step；
3. Configure IWDG_PREDIV.PD[2:0] bits to select pre-scale value；
4. Configure IWDG_RELV.REL[11:0] bits reload value；
5. Writing 0xAAAA to IWDG_KEY.KEYV[15:0] bits to upload counter with reload value；
6. Enable watchdog by software or hardware writing 0xCCCC to IWDG_KEY.KEYV[15:0] bits。

If user wants change pre-scale and reload value, repeat step 1~5. If not, just feed the dog with step 5.

23.5 IWDG Registers

23.5.1 IWDG Key Register（IWDG_KEY）

Address offset: 0x0000

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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KEYV[15:0]

rc_w0

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	KEYV[15:0]	Key value register: only certain value will serve particular function 0xCCCC: Start watch dog counter, does not have any effect if hardware watchdog is enable, (if hardware watchdog is selected, it is not limited by this command word) 0xAAAA: Reload counter with REL value in IWDG_RELV register to prevent reset. 0x5555: Disable write protection of IWDG_PREDIV and IWDG_RELV register 0x4567: IWDG freeze, stop the IWDG counter in RUN mode 0x89AB: IWDG unfreeze, the counter resumes counting

23.5.2 IWDG Status Register（IWDG_STS）

Offset address：0x04

Reset value：0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													FRZF	CRVU	PVU
													r	r	r

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	FRZF	IWDG freeze flag： 0: No freeze occurred 1: Freeze occurred
1	CRVU	Watchdog reload value update Reload value update: This bit indicates that the reload value is being updated. It is set by hardware and cleared by hardware. Software can only attempt to change the value of IWDG_RELV.REL[11:0] when the value of IWDG_KEY.KEYV[15:0] is 0x5555 and this bit is 0.
0	PVU	Watchdog prescaler value update Prescaler value update: This bit indicates that the prescaler value is being updated. It is set by hardware and cleared by hardware. Software can only attempt to change the value of IWDG_PREDIV.PD[2:0] when the value of IWDG_KEY.KEYV[15:0] is 0x5555 and this bit is 0.

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23.5.3 IWDG Pre-Scaler Register（IWDG_PREDIV）

Offset address：0x08

Reset value：0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													PD[2:0]		
													rw		

Bit Field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2:0	PD[2:0]	Prescaler- factor Prescaler divider: with write access protection when IWDG_KEY.KEYV[15:0] is not 0x5555. The IWDG_STS.PVU bit must be 0 otherwise PD [2:0] value cannot be changed. Divide number is as follow: 000：divider /4 001：divider /8 010：divider /16 011：divider /32 100：divider /64 101：divider /128 Other : divider /256 *Note: Reading this register will return the pre-divided value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.PVU bit is '0'.*

23.5.4 IWDG Reload Register（IWDG_RELV）

Offset address：0x0C

Reset value：0x00000FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				REL[11:0]											

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rw

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	REL[11:0]	Watchdog counter reload value. With write protection. Defines the reload value of the watchdog counter, which is loaded to the counter every time 0xAAAA is written to IWDG_KEY.KEYV[15:0] bits. The counter then starts to count down from this value. The watchdog timeout period can be calculated from this reloading value and the clock pre-scaler value, refer to Table 23-1. This register can only be modified when the IWDG_STS.CRVU bit is '0'. *Note: Reading this register will return the reload value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.CRVU bit is '0'.*

24 Window Watchdog（WWDG）

24.1 Introduction

The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock frequency by 4096, and it is used to detect abnormal program operation through the configuration of the time window. Therefore, WWDG is suitable for precise timing, and is often used to monitor software failures caused by external disturbances or unforeseen logic conditions, which cause an application to deviate from its normal operating sequence. A system reset occurs when the WWDG down counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0.

24.2 Main Features

- 14-bit programmable running down counter
- After WWDG is enabled, a reset occurs under the following conditions
  - The value of the down counter is less than 0x40.
  - When the down counter value is greater than the value of the window register, it is reloaded.
- Early wake-up interrupt: If the watchdog is started and the interrupt is enabled, wake-up interrupt (WWDG_CFG.EWINT) will be generated when the count value reaches 0x40.

24.3 Function Description

If the watchdog is activated (the WWDG_CTRL.ACTB bit), when the 14-bit (WWDG_CTRL.T[13:0]) down-counter reaches 0x3F(WWDG_CTRL.T6 bit is cleared), or the software reloads the counter when the counter value

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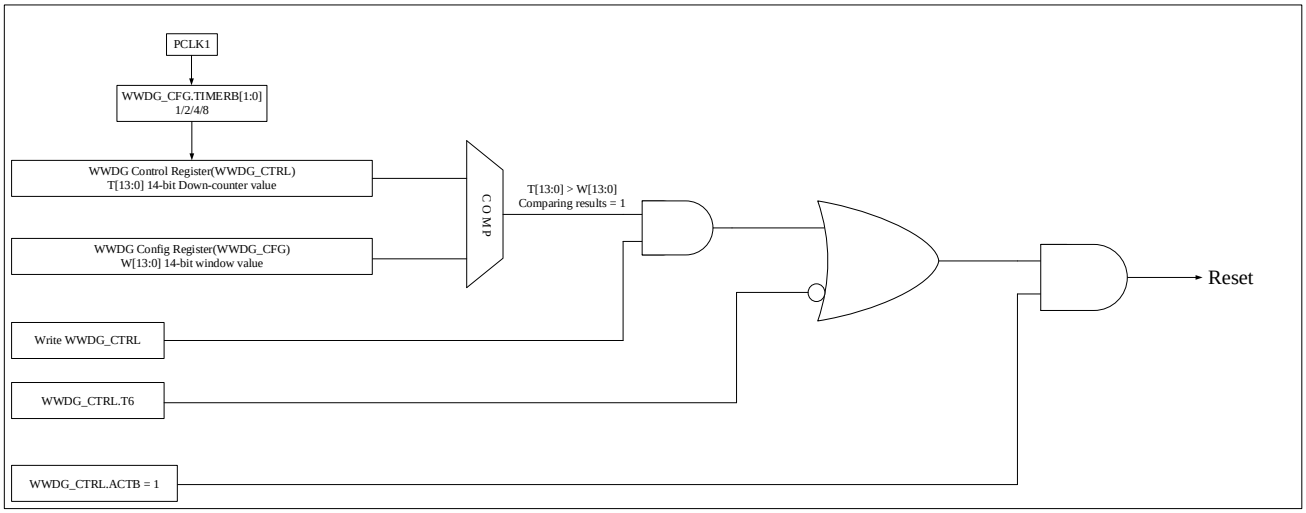
is greater than the value of the window register, a system reset will be generated. In order to avoid system reset, the software must periodically refresh the counter value in the window during normal operation.

Figure 24-1 Watchdog Block Diagram



Set the WWDG_CTRL.ACTB bit to enable the watchdog, and thereafter, the WWDG will remain on until reset occurs. The 14-bit down-counter runs independently, and the counter keeps counting down whether WWDG is enabled or not. Therefore, before enabling the watchdog, Need to set one of the high 8 bits MSB (WWDG_CTRL.T[13:6]) to 1, preventing reset immediately after enable. The prescaler value set by the clock APB1 and WWDG_CFG.TIMERB[1:0] bits determine the decrement speed of the counter. WWDG_CFG.W[13:0] bits set the upper limit of the window.

When the down-counter is refreshed before reaching the window register value or after WWDG_CTRL.T6 bit becomes 0, a system reset will be generated. Figure 24-2 describes the operating process of the window registers.

Set the WWDG_CFG.EWINT bit to enable early wake-up interrupt. When the count-down counter reaches 0x40, an interrupt will be generated. You can analyze the cause of software failure or save important data in the corresponding interrupt service routine (ISR), and reload the counter to prevent WWDG from resetting. Write '0' to the WWDG_STS.EWINTF bit to clear the interrupt.

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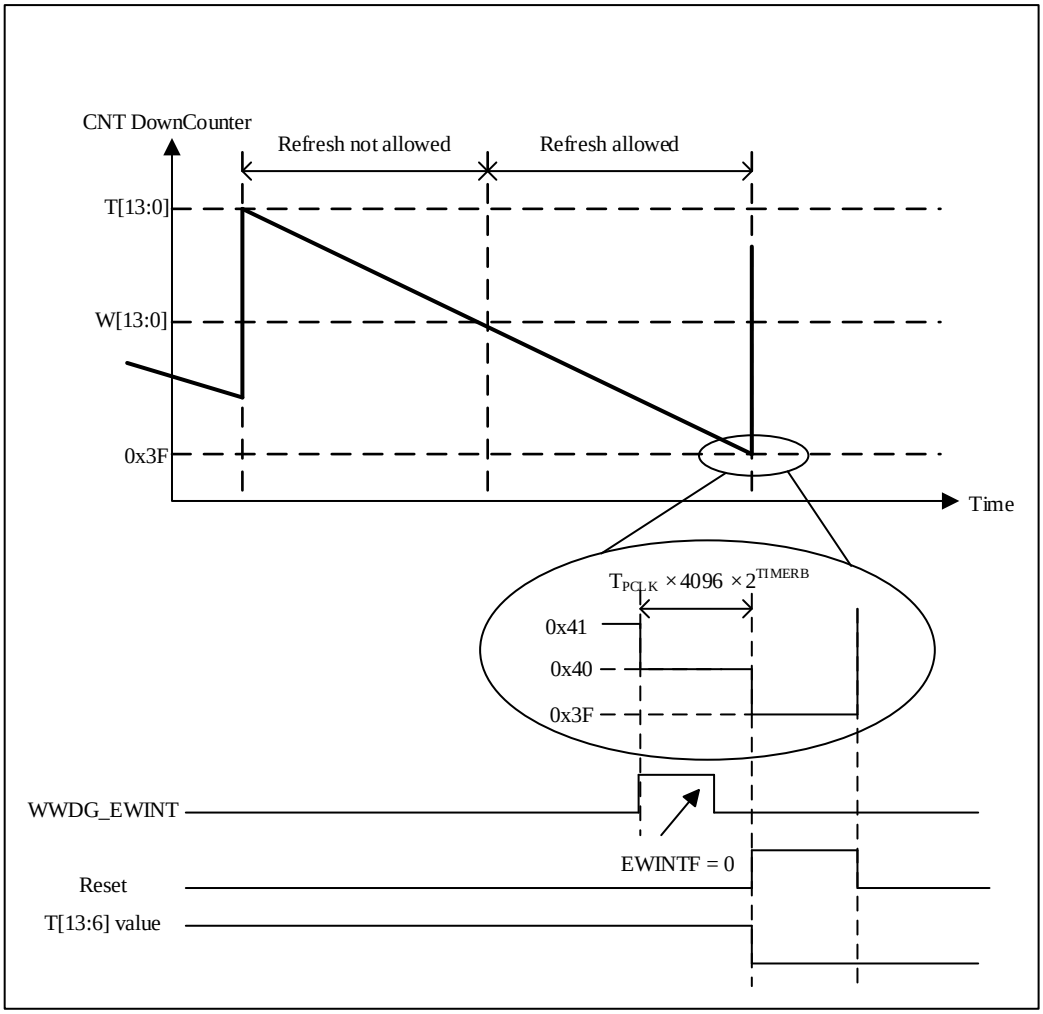
24.4 Timing For Refresh Watchdog And Interrupt Generation

Figure 24-2 Refresh Window And Interrupt Timing Of WWDG



Watchdog refreshing window is between WWDG_CFG.W[13:0] value (maximum value 0x3FFF) and 0x3F, refresh outside this window will generates reset request to MCU. Counter count down from 0x3FFF to 0x3F using scaled APB clock, the maximum counting time and minimum counting time is shown in following Table（assuming APB clock 150 MHz），with calculate equation：

$$T_{WWDG} = T_{PCLK1} \times 4096 \times 2^{TIMERB} \times (T[13:0] - 0X3F + 1)$$

In which：

T_{WWDG}:WWDG timeout

T_{PCLK1}:APB1 clock interval in ms

Minimum-maximum timeout value at PCLK1=150MHz

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Table 24-1 Maximum And Minimum Counting Time Of WWDG

TIMERB	Maximum counting（ms）	Minimum counting（ms）
0	445.54	0.02728
1	891.07	0.05456
2	1782.14	0.1088
3	3564.29	0.2184

24.5 Debug Mode

In debug mode (Cortex-M4F_HALTED or Cortex-M7F_HALTED), WWDG counter will either continue to work normally or stop, depending on DBG_M7APB6FZ[0]/ DBG_M4APB6FZ[0]/ DBG_M7APB1FZ[14]/ DBG_M4APB1FZ[14] bits in Debug Support module. If this bit is set to '1', the counter stops. The counter works normally when the bit is '0'. See the DBG (debugging) module for details.

24.6 User Interface

24.6.1 WWDG Configuration Flow

1. Configure RCC_AXIEN2[3:0] bit to enable the clock of WWDG module.
2. Software setting WWDG_CFG.TIMERB[15:14] bits to configure pre-scale factor for WWDG.
3. Software configure WWDG_CTRL.T[13:0] bits, setting starting value of counter. Need to set one of the high 8 bits MSB (WWDG_CTRL.T[13:6]) to 1, preventing reset right after enable.
4. Configure WWDG_CFG.W[13:0] bits to configure upper boundary window value.
5. Setting WWDG_CTRL.ACTB[14] bit to enable WWDG.
6. Software operates WWDG_STS.EWINTF[0] bit to clear wake-up interrupt flag.
7. Configure WWDG_CFG.EWINT[16] bit to enable early wake-up interrupt.

24.7 WWDG Registers

24.7.1 WWDG Config Register（WWDG_CFG）

Offset address：0x00

Reset value：0x00003FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															EWINT
															rs

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMERB[1:0]		W[13:0]													

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rw rw

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	EWINT	Early wake-up interrupt When set, an interrupt occurs whenever the counter reaches the value 0x40. This interrupt is only cleared by hardware after a reset.
15:14	TIMERB[1:0]	Timer base The time base of the pre-scaler can be modified as follows： 00：CK Counter Clock（PCLK1 div 4096）div 1 01：CK Counter Clock（PCLK1 div 4096）div 2 10：CK Counter Clock（PCLK1 div 4096）div 4 11：CK Counter Clock（PCLK1 div 4096）div 8
13:0	W[13:0]	14-bit window value These bits contain the window value to be compared to the down counter

24.7.2 WWDG Control Register（WWDG_CTRL）

Offset address：0x04

Reset value：0x00003FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ACTB	T[13:0]													

rs rw

Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	ACTB	Activation bit When ACTB=1, the watchdog can generate a reset. This bit is set by software and only cleared by hardware after a reset. When ACTB = 1, the watchdog can generate a reset. 0: Disable watchdog 1: Enable warchdong
13:0	T[13:0]	These bits contain the value of the watchdog counter. It is decremented every (4096x2^{TIMERB}) PCLK1 cycles. A reset is produced when it rolls over from 0x40 to 0x3F (T6 becomes cleared).

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24.7.3 WWDG Status Register（WWDG_STS）

Offset address：0x08

Reset value：0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EWINTF
															rc_w0

Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EWINTF	Early wake-up interrupt flag This bit is set by hardware when the counter has reached the value 0x40. It must be cleared by software by writing ‘0’. A write of ‘1’ has no effect. This bit is also set if the interrupt is not enabled.

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25 Real-Time Clock (RTC)

25.1 Introduction

- The real-time clock (RTC) is an independent BCD timer/counter.
- Daylight saving time compensation supported by software.
- A periodic automatic programmable wakeup timer.
- Two 32-bit registers contain the seconds, minutes, hours, day (day of week), date (day of month), month, and year.
- Independent 32-bit register contain sub-seconds value.
- Two programmable alarms.
- Two 32-bit registers contain two programmable alarms seconds, minutes, hours, day (day of week), and date (day of month).
- Two 32-bit registers contain two programmable alarms sub-seconds.
- Digital calibration function.
- Reference clock detection: A more accurate external clock source (50 or 60Hz) can be used to improve calendar accuracy.
- Three configurable filtering and internal pull-up tamper detection events, five internal tamper dedection event .
- Time-Stamp function.
- 32 backup registers, capable of maintaining data in low-power mode.
- Multiple Wakeup sources of Interrupt/Event. These include Alarm A, Alarm B, Wakeup Timer, Time-Stamp.
- After RTC is enabled by the RCC register and voltage remains in the operating range, RTC will not stop timing in any mode (include RUN mode, SLEEP mode, STOP0 mode, STOP2 mode, VBAT mode and STANDBY mode).
- RTC provides a variety of ways to wakeup from all low-power modes (SLEEP mode, STOP0 mode, STOP2 mode and STANDBY mode).

25.1.1 Main Features

Table 25-1 RTC Feature Support

Main Function	Description
Clock	RTC clock can be selected from LSI, LSE and HSE/2,3,4…63 respectively, maximum frequency for RTC is 4MHz.
Reset	The APB interface is reset by the system. Some registers synchronized through APB in the RTC module will be reset. The following registers will be cleared when the system is reset. ● RTC_SUBS ● RTC_TSH ● RTC_DATE

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Main Function	Description
	● RTC_INITSTS(some bits) RTC core is reset by backup domain reset. Reset the RTC, and retain the contents of some registers in low-power mode, including: ● RTC_CTRL ● RTC_PRE ● RTC_CALIB ● RTC_SCTRL ● RTC_TSSS, RTC_TST and RTC_TSD ● RTC_TMPCFG ● RTC_WKUPT ● RTC_ALRMASS/RTC_ALRMA ● RTC_ALRMBSS/RTC_ALRMB ● RTC_OPT ● RTC_BKP(1~31) ● RTC_TMPxCTRL(x = 1~8)
Calendar	Calendar consists of sub second, second, minute, hour (12 or 24 format), day (day of the week), date, month and year. These data are stored in the shadow register of APB module.
Wakeup Timer	Output 'RTC_OUT' can be configured to transmit wakeup events to GPIO. At the same time, it also can be configured as an interrupt/event to wake up the system from SLEEP, STOP0, STOP2, STANDBY modes.
Alarm	'RTC_OUT' is configured to output to GPIO, and can also wake up the CPU or trigger PWR to wake up from SLEEP, STOP0, STOP2 and STANDBY modes when a match occurs.
Tamper	The three tamper detection logics are a source of system wake-up. If an tamper event occurs on any of the input lines or internal tamper event occurs, when enabled, tamper events also result in the deletion of backup registers. It is also a source for hardware triggering of the LP timer.
Timestamp	GPIO events can trigger the timestamp saving function. It is a source of wake-up from low-power mode. Additionally, tamper events can be a source of timestamp events.
Interrupts/events	Alarm A/Alarm B interrupt/event, Wakeup interrupt/event, Timestamp interrupt/event, Tamper interrupt/event
Backup registers	32 backup registers

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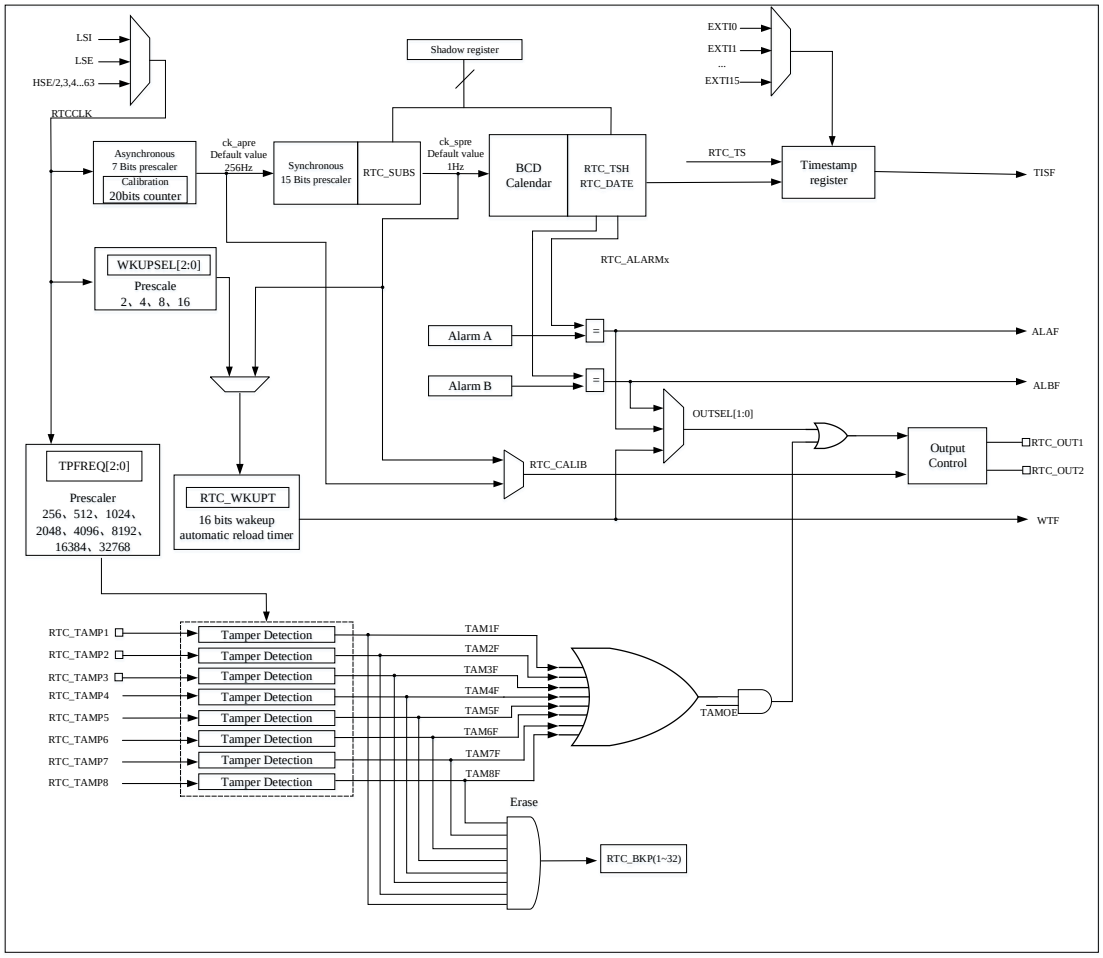
25.2 RTC Function Description

25.2.1 RTC Block Diagram

Figure 25-1 RTC Block Diagram



RTC includes the following functions:

- Alarm A and Alarm B event/interrupt
- Timestamp event/interrupt
- Tamper event/interrupt
- 32 32-bit backup registers
- RTC output functions
  - 256 Hz or 1Hz clock output (LSE frequency is 32.768 kHz).
  - Alarm clock output (polarity configurable), Alarm A and Alarm B are optional.
  - Auto wakeup output (polarity configurable).
- RTC input functions:
  - Timestamp event detection
  - 50 or 60Hz reference clock input
  - Tamper event detection

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Email: sales@nsing.com.sg

- Control PC13/PB2/PI8 by configuring output register:
  - Set RTC_OPT.TYPE bit to configure open-drain/push-pull output of PC13/PB2/PI8

25.2.2 GPIOs Controlled by RTC

Timestamp input come from IOM (mapped to PC13 or EXTI module, if EXTI module is needed to start, please refer to the timestamp trigger source selection register (EXTI_TS_SEL) for details.

RTC_OUT (Alarm, Wakeup event, Tamper event or calibration output (256Hz or 1Hz)) is mapped to PC13, PB2 and PI8. Regardless of the configuration of PC13, PB2 and PI8 GPIO pins, the pin configuration of PC13, PB2 and PI8 is controlled by RTC as output.

The PC13 pin is used as the TAMPER1 tamper detection pin, the PI8 pin is used as the TAMPER2 tamper detection pin, and the PC1 pin is used as the TAMPER3 tamper detection pin.

PB15 can be used as the RTC_REFCLKIN reference clock input pin.

25.2.3 RTC Register Write Protection

The PWR_CTRL.DBKP bit (refer to the power control register (PWR_CTRL)) is cleared by default, so PWR_CTRL.DBKP must be set to 1 to enable RTC register write functionality. Once the backup domain is reset, all RTC write-protected registers will have write protection enabled. All RTC write-protected registers need to be unlocked by following the steps below:

- Write “0xCA” into RTC_WRP register.
- Write “0x53” into RTC_WRP register.

After unlocking these registers, writing an incorrect key or resetting the RTC by software or power cycling will re-enable the write protection. The unlocking mechanism only checks the write operation to the RTC_WRP register. During the unlocking process, before unlocking, and after unlocking, writing to other registers will not affect the unlocking result.

After the backup domain reset, all configurable RTC registers and backup registers RTC_BKP (20) are write-protected.

25.2.4 RTC Clock and Prescaler

RTC clock source:

- LSE clock
- LSI clock
- HSE/2,3,4…63 clock, maximum frequency for RTC is 4MHz.

To reduce power consumption, the prescaler is divided into an asynchronous prescaler and a synchronous prescaler. If both prescalers are used simultaneously, it is recommended to set the value of the asynchronous prescaler as large as possible.

By configuring RTC_PRE.DIVA[6:0] and RTC_PRE.DIVS[14:0], the user can obtain a ck_spre clock of 1Hz.

- A 7-bit asynchronous prescaler which is given by RTC_PRE.DIVA[6:0] bits

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Email: sales@nsing.com.sg

- A 15-bit synchronous prescaler which is given by RTC_PRE.DIVS[14:0] bits

The formula for f_{ck_apre} and f_{ck_spre} are given below:

$$f_{ck_apre} = \frac{f_{RTCCLK}}{RTC_PRE.DIVA[6:0]+1}$$

$$f_{ck_spre} = \frac{f_{RTCCLK}}{(RTC_PRE.DIVS[14:0]+1)*(RTC_PRE.DIVA[6:0]+1)}$$

The ck_apre clock is used to driven RTC_SUBS sub-second down counter. When it reaches 0, RTC_SUBS is reloaded with the value of RTC_PRE.DIVS[14:0].

Note: RTC_PRE.DIVA[6:0] cannot be configured to 0.

25.2.5 RTC Calendar

There are three shadow registers, they are RTC_DATE, RTC_TSH and RTC_SUBS. The RTC time and date registers can be accessed through the shadow registers. It is also possible to access them directly to avoid the synchronization waiting time. The three shadow registers are as follow:

- RTC_DATE: set and read date
- RTC_TSH: set and read time
- RTC_SUBS: read sub-second

Every two RTCCLK cycles, the current calendar value is copied to the shadow registers, and the RTC_INITSTS.RSYF bit is set to 1. This process is not executed in low-power (stop and standby) modes. When exiting these modes, the shadow registers update their values after 2 RTCCLK cycles.

By default, when user try to access the calendar register, it will access the contents of the shadow register instead. User can access the calendar register directly by setting the RTC_CTRL.BYPS bit.

When RTC_CTRL.BYPS=0, calendar values are from shadow registers, when reading RTC_SUBS, RTC_TSH or RTC_DATE register, it is necessary to make ensure the frequency of APB1 clock (f_{APB1}) is at least 7 times the frequency of RTC clock (f_{RTCCLK}), and APB1 clock frequency lower than RTC clock frequency is not allowed in any case. System reset will reset shadow registers.

25.2.6 Calendar Initialization and Configuration

The value of prescaler and calendar can be initialized by the following steps:

- Set the RTC_INITSTS.INITM bit to 1 to enter the initialization mode, and then wait for the RTC_INITSTS.INITF bit to be set to 1.
- Set RTC_PRE.DIVS[14:0] and RTC_PRE.DIVA[6:0] value.
- Write the initial calendar values include time and date into the shadow registers (RTC_TSH and RTC_DATE) and configure the time format (12 or 24 hours) through the RTC_CTRL.HFMT bit.
- Exit initialization mode by clearing the RTC_INITSTS.INITM bit.

The values of calendar counter will automatically loaded from shadow registers after 4 RTCCLK clock cycles, then the calendar counter restarts.

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Note: Before entering the initialization mode, ensure that the value of RTC_SUBS.SS[15:0] is not less than 2.

25.2.7 Calendar Reading

1. Reading calendar value when RTC_CTRL.BYPS=0

Calendar value is read from shadow registers if RTC_CTRL.BYPS=0. In order to read RTC calendar registers (RTC_SUBS, RTC_TSH and RTC_DATE) correctly, APB1 clock frequency must be set greater than 7 times of RTC clock frequency. In any case, APB1 clock frequency must not be less than RTC clock frequency.

If APB1 clock frequency is not equal to or greater than 7 times of RTC clock frequency, refer to the following process to read calendar value.

- Read the data of RTC_SUBS, RTC_TSH and RTC_DATE twice.
- Compare the data read on two occasions, if they are equal, the read data can be considered correct; if they are not equal, read the data for the third time.
- The third time read data can be considered correctly.
- To ensure that the calendar is read from the same time point, the value in the RTC_DATE register is locked when reading RTC_SUBS or RTC_TSH. Until RTC_DATE is read, it will not be updated in real-time, so after reading RTC_SUBS or RTC_TSH, RTC_DATE needs to be read again.

Shadow registers (RTC_SUBS, RTC_TSH and RTC_DATE) are updated every two RTCCLK cycles. If user want to read calendar value in a short time(less than two RTCCLK cycles), RTC_INITSTS.RSYF bit must be cleared by software after the first time read.

In some cases, it is necessary to wait until RTC_INITSTS.RSYF bit is set to 1 before read calendar value.

- After waking up from the low power modes (STANDBY mode), clear RTC_INITSTS.RSYF bit, then wait for the RTC_INITSTS.RSYF bit to be set to 1 again..
- System reset.
- Calendar complete initialization.
- Calendar complete synchronization.

2. Reading calendar value when RTC_CTRL.BYPS=1

If RTC_CTRL.BYPS=1, read the calendar value directly from the calendar counter. The advantage of this configuration is that there is no delay in reading the calendar value after waking up from low-power mode. The disadvantage is that the data from RTC_SUBS, RTC_TSH, and RTC_DATE may not be from the same moment.

To ensure the correctness of read calendar value, it is necessary to read RTC_SUBS, RTC_TSH and RTC_DATE twice, the data read on two occasions should then be compared, and if they are equal, the read data is considered correct.

25.2.8 Calibration Clock Output

When RTC_CTRL.COEN is set to 1, the PC13 or PB2 pins will output the calibration clock. If RTC_CTRL.CALOSEL=0 and RTC_PRE.DIVA[6:0]=0x7F, the frequency of RTC_CALIB is fRTCCLK / RTC_PRE.DIVA[6:0].When the frequency of RTCCLK is 32.768 kHz, the calibration output is 256Hz. Due to slight jitter on the falling edge, it is recommended to use the rising edge.

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When RTC_CTRL.CALOSEL=1 and "RTC_PRE.DIVS[14:0]+1" is a non-zero integer multiple of 256, the frequency of RTC_CALIB is given by the formula f_{RTCCLK}/(256 * (DIVA+1)). When the frequency of RTCCLK is 32.768 kHz and RTC_PRE.DIVA[6:0]=0x7F, the calibration output is 1Hz.

Note:

1) *When selecting RTC_CALIB as the output, the RTC_OUT pin (PC13/PB2) is automatically configured as an output.*
2) *The duty cycle of the RTC_OUT output at 256Hz or 1Hz is fixed at 50% (+-20%).*

25.2.9 Programmable Alarm

RTC has 2 programmable alarms: Alarm A and Alarm B.

RTC alarm can be enabled or disabled by configuring RTC_CTRL.ALxEN bit. If the Alarm value matches the calendar value, the RTC_INITSTS.ALxF flag is set to 1. If RTC_CTRL.ALxIEN is enabled, any calendar field can be selected to trigger the alarm interrupt.

Alarm Output: After configuring RTC_CTRL.OUTSEL[1:0], Alarm A or Alarm B can be mapped to the RTC_ALxRM output, and the output polarity can be configured by the RTC_CTRL.OPOL bit.

Note: When the second field is selected (RTC_ALARMx.MASK1 bit reset), RTC_PRE.DIVS[14:0] must be greater than 3 to ensure correct operation.

25.2.10 Alarm Configuration

Alarm A and Alarm B should be configured in the following below:

- Disable Alarm A/Alarm B by clearing RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit.
- Configure the Alarm x registers (RTC_ALRMxSS/RTC_ALARMx)
- Enable the Alarm A/Alarm B interrupt by setting the RTC_CTRL.ALAIEN/RTC_CTRL.ALBIEN bit to 1 (add this step as needed).
- Enable Alarm A/Alarm B by setting the RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit to 1.

25.2.11 Alarm Output

When RTC_CTRL.OUTSEL[1:0] != 0, the RTC_ALARM output function is enabled. Depending on the value of RTC_CTRL.OUTSEL[1:0], select Alarm A output, Alarm B output, or wakeup output.

The RTC_CTRL.OPOL bit controls the polarity of Alarm A, Alarm B, or wakeup output.

The RTC_OPT.TYPE bit controls the RTC_ALARM pin open-drain or push-pull output.

When selecting RTC_ALARM output, the RTC_OUT pin (PC13/PB2) is automatically configured as an output.

25.2.12 Periodic Automatic Wakeup

A 16-bit programmable auto-reload counter can generate a periodic wakeup flag upon reaching 0. It can also extend the range of the wakeup timer to 17 bits. Enabling the periodic auto-wakeup function can be done by setting RTC_CTRL.WTEN

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There are two wake-up input clock sources can be selected:

- RTC clock (RTCCLK) divided by 2/ 4/8/16.

  Assume RTCCLK comes from LSE (32.768KHz), wake-up interrupt period can be configured range from 122us to 32s under the resolution down to 61us.

- Internal clock ck_spre.

  Assume ck_spre frequency is 1Hz, the available wake-up time range from 2s to 18h, and the resolution is 1 second.

  - When RTC_CTRL.WKUPSEL [2:0] = 10x, the period is range from 2s to 18h.
  - When RTC_CTRL.WKUPSEL [2:0] = 11x, the period is range from 18h to 36h.

When the RTC_CTRL.WTEN bit is set to 1, the countdown counter is running, and when it reaches 0, the RTC_INITSTS.WTF bit is set to 1. By setting the RTC_CTRL.WTIEN bit to 1, the device can exit low-power mode when the periodic wakeup interrupt is triggered and enabled.

Periodic Wakeup Output: When RTC_CTRL.OUTSEL[1:0] selects the periodic wakeup, the RTC_OUT pin (PC13/PB2) is automatically configured as an output, and the output polarity can be configured by the RTC_CTRL.OPOL bit.

25.2.13 Wakeup Timer Configuration

The configuration of the automatic reload value for the wakeup timer is as follows:

- Disable the wakeup timer by clearing RTC_CTRL.WTEN, then wait for the RTC_INITSTS.WTWF flag to be set to 1.
- Select the wakeup timer clock by setting RTC_CTRL.WKUPSEL[2:0].
- Configure the wake-up automatic reload value by setting RTC_WKUPT.WKUPT[15:0] bits.
- Enable Wakeup interrupt by setting RTC_CTRL.WTIEN bit(this step can be selected as needed)
- Enable wakeup timer by setting RTC_CTRL.WTEN bit

25.2.14 Timestamp Function

Timestamp can be enabled by setting RTC_CTRL.TSEN bit to 1. When a timestamp event is detected on the RTC_TS pin, the calendar values of the event will be stored in the timestamp register (RTC_TSSS, RTC_TST, RTC_TSD), and RTC_INITSTS.TISF is set to 1. If RTC_CTRL.TSIEN is set to 1, a timestamp event can generate an interrupt. If a new timestamp event is detected while RTC_INITSTS.TISF is already set to 1, the hardware will set the RTC_INITSTS.TISOVF flag to 1. The timestamp registers (RTC_TST and RTC_TSD) will continue to hold the values of the previous event, meaning that the data in the timestamp registers (RTC_TST and RTC_TSD) will not change when RTC_INITSTS.TISF=1.

After the timestamp event caused by the synchronization process occurs again, RTC_INITSTS.TISF is set to 1 in 2 RTC_CLK cycles. There is no delay in the generation of RTC_INITSTS.TISOVF. This means that if two timestamp events are very close, this can cause RTC_INITSTS.TISOVF to be "1" and RTC_INITSTS.TISF to be "0". Therefore, after detecting RTC_INITSTS.TISF as "1", check the RTC_INITSTS.TISOVF bit. When RTC_TMPCFG.TPTS bit is set to 1, tamper events can trigger timestamp events.

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If timestamp events are enabled, the timestamp will capture the read calendar in the timestamp registers.Timestamp events can be generated on any of the GPIO ports selected by EXTI. The GPIO pins in each port are selected by setting the corresponding EXTI_TS_SEL.TSSEL[3:0] bits.

25.2.15 Tamper Detection

There are three tamper detection pins, RTC_TAMP1 pin is PC13, RTC_TAMP2 pin is PI8, and RTC_TAMP3 pin is PC1. The RTC_TAMPx pins can be used as input pins for tamper event detection. There are two detection modes, edge detection mode and level detection mode with configurable filtering function.

There are five internal tamper event, RTC_TAMP4 related to LSE monitor, RTC_TAMP5 related to HSI monitor, RTC_TAMP6 related to RTC calendar overflow, RTC_TAMP7 related to VBAT monitor, RTC_TAMP8 related to temperature monitor.

When a RTC_TAMPx event is detected, if RTC_TMPxCTRL.TPNOE=0, the RTC_BKP(1~32) registers will be cleared.

Tamper Detection Initialization

There are three tamper detection pins, each pin can be configured independently. Users need to configure tamper detection before setting the RTC_TMPxCTRL.TPEN bit. When tamper detection is enabled and a tamper event is detected, if RTC_TMPxCTRL.TPINTEN is set to 1, the tamper event can generate an interrupt and the RTC_INITSTS.TAMxF bit will be set to 1.

When the RTC_INITSTS.TAMxF bit is set to 1, new tamper events on the same pin cannot be detected.

Timestamp on tamper event

When RTC_TMPCFG.TPTS bit is set to 1, any tamper event can trigger a timestamp event, and the RTC_INITSTS.TISF bit and RTC_INITSTS.TISOVF bit will be set for normal timestamp events.

Edege detection on tamper inputs

When the RTC_TMPCFG.TPFLT[1:0] bit is set to 0, tamper detection is set to edge detection, with the rising or falling edge controlled by the RTC_TMPCFG.TPxTRG bit. When the corresponding edge is detected, the RTC_TAMPx pin will generate a tamper detection event.

Since RTC_BKP(1~32) can be reset when a tamper event is detected, it is necessary to ensure that tamper event detection and writing to RTC_BKP(1~32) do not occur simultaneously. It is recommended to enable the tamper detection function after writing to RTC_BKP(1~32).

Note: When selecting edge triggering, external pull-up or pull-down is required

Level detection with filtering on RTC_TAMPx input

When RTC_TMPCFG.TPFLT[1:0] bits are set to 1/2/3, tamper detection is set to level detection. The value of RTC_TMPCFG.TPFLT[1:0] determines the number of samples.

Before each sampling, pre-charging can be performed through the internal pull-up resistor of the tamper pin, and the pre-charging time is controlled by the RTC_TMPCFG.TPPRCH[1:0] bits. When RTC_TMPCFG.TPPUDIS is set to 1, pre-charging will be disabled.

Using RTC_TMPCFG.TPFREQ[2:0] to determine the sampling frequency of level detection can optimize the best

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Email: sales@nsing.com.sg

balance between tamper detection delay and pull-up power consumption.

25.2.16 Daylight Saving Time Configuration

Daylight saving time function can be controlled through RTC_CTRL.SU1H, RTC_CTRL.AD1H, and RTC_CTRL.BAKP bits. Calendar will subtract one hour when set RTC_CTRL.SU1H bit to 1, and add one hour when set RTC_CTRL.AD1H to 1. RTC_CTRL.BAKP can be used to memorize this adjustment.

Setting the RTC_CTRL.SU1H bit to 1 will subtract one hour for the calendar, while setting the RTC_CTRL.AD1H to 1 will add one hour. The RTC_CTRL.BAKP bit can be used to remember or not remember this adjustment.

25.2.17 RTC Sub-Second Register Shift Operation

When the value of calendar has a sub-second deviation compared to the external precision clock, the shift function can be used to improve the precision of calendar.

The calendar can be controlled to delay or advance by 1 second using the RTC_SCTRL.AD1S and RTC_SCTRL.SUBF[14:0] bits. The adjustment resolution is 1/(RTC_PRE.DIVS[14:0]+1), where a higher value of RTC_PRE.DIVS[14:0] indicates a higher resolution. To keep the synchronized prescaler output at 1Hz, a higher value of RTC_PRE.DIVS[14:0] means a lower value of RTC_PRE.DIVA[6:0], resulting in higher power consumption

Note: Before starting the shift operation, the user must check if the RTC_SUBS.SS[15] bit is 0

Whenever writing to the RTC_SCTRL register, the hardware sets the RTC_INITSTS.SHOPF flag, indicating that the shift operation is in a suspended state. Once the shift operation is completed, this bit is cleared by the hardware.

25.2.18 RTC Digital Clock Precision Calibration

Digital precision calibration is achieved by adjusting the number of RTC clock pulses in the calibration period. Digital precision calibration resolution is 0.954 PPM with the range from -487.1 PPM to +488.5 PPM.

When the input frequency is 32768 Hz, calibration period can be configured as $2^{20}/2^{19}/2^{18}$ RTCCLK cycles or 32/16/8 seconds. The precision calibration register (RTC_CALIB) indicates that there has RTC_CALIB.CM[8:0] RTCCLK clock cycles will be reduced during the specified period.

The value of RTC_CALIB.CM[8:0] represents the number of RTCCLK pulses to be reduced within a specified period. RTC_CALIB.CP can be used to increase by 488.5PPM, where every 2^{11} RTCCLK periods will insert an RTCCLK pulse

When using RTC_CALIB.CM[8:0] and RTC_CALIB.CP in combination, it can increase cycles range from -511 to +512 RTCCLK cycles, and the calibration range from -487.1 ppm to +488.5 ppm, with the resolution is about 0.954 ppm.

The valid calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * (1 + \frac{RTC_CALIB.CP*512 - RTC_CALIB.CM[8:0]}{2^n + RTC_CALIB.CM[8:0] - RTC_CALIB.CP * 512})$$

Note:n=20/19/18

Note: When calibrating, the RTC_PRE.DIVA[6:0] must not be set to a value smaller than 3.

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Email: sales@nsing.com.sg

The valid calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * \left(1 + \frac{256 - RTC_CALIB.CM[8:0]}{2^n + RTC_CALIB.CM[8:0] - 265}\right)$$

Verify RTC calibration

RTC outputs waveform (1Hz) for measuring and verifying RTC precision.

Up to 2 RTCCLK cycles measurement error may occur when measure the RTC frequency in a limit measurement period. If the measurement period is the same as calibration period, the error can be eliminated.

- The calibration period is 32 seconds (default).

  Using an accurate 32-second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.447ppm (0.5 RTCCLK cycles within 32 seconds).

- The calibration period is 16 seconds.

  Using an accurate 16-second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.954ppm (0.5 RTCCLK cycles within 16 seconds).

- The calibration period is 8 seconds.

  Using an accurate 8-second period to measure the 1Hz calibration output can ensure that the measurement error is within 1.907ppm (0.5 RTCCLK cycles within 8 seconds).

Dynamic recalibration

When RTC_INITSTS.INITF=0, RTC_CALIB register can be updated through following steps:

- Wait RTC_INITSTS.RECPF=0.
- A new value is written to the RTC_CALIB, then RTC_INITSTS.RECPF is automatically set to 1.
- The new calibration settings will take effect within 3 ck_apre cycles after a data write to the RTC_CALIB.

25.2.19 RTC Low Power Mode

The operating state of RTC in low power mode:

Table 25-2 RTC in low power mode

Lower Power Mode	RTC Operating State	Exit Low Power Mode
SLEEP	Normal operation	Alarm A, Alarm B, Periodic Wakeup, tamper enent and Timestamp event
STOP0	Normal operation when RTC clock source is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup, tamper enent and Timestamp event
STANDBY	Normal operation when RTC clock source is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup, tamper enent and Timestamp event

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

25.2.20 Mapping Relationship for RTC_OUT1 (PC13) and RTC_OUT2 (PB2/PI8) Configuration

Table 25-3 RTC OUT Mapping

RTC_CTRL			RTC_OPT	RTC_OUT1(PC13)	RTC_OUT2(PB2/PI8)
TAMPOE	OUTSEL[1:0]	COEN	OUTMAP		
0	00	1	0	CALIB	-
1	00	Don't care		TAMPER	-
0	01	Don't care		ALARMA	-
0	10	Don't care		ALARMB	-
0	11	Don't care		WAKEUP	
1	01/10/11	Don't care		TAMPER_ALARM(1)	-
0	00	1	1	-	CALIB
1	00	0		-	TAMER
0	01	0		-	ALARMA
0	10	0		-	ALARMB
0	11	0		-	WAKEUP
1	01/10/11	0		-	TAMPER_ALARM(1)
1	00	1		TAMPER	CALIB
0	01	1		ALARMA	CALIB
0	10	1		ALARMB	CALIB
0	11	1		WAKEUP	CALIB
1	01/10/11	1		TAMPER_ALARM(1)	CALIB

1. TAMPER_ALARM mean output TAMPER and ALARMA or ALARMB or WAKEUP.

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

25.3 RTC Registers

25.3.1 RTC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
008h	RTC_TSH	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SCT[2:0]			SCU[3:0]			
	Reset Value										0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	0
00Ch	RTC_DATE	Reserved							YRT[3:0]					YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved		DAT[1:0]		DAU[3:0]			
	Reset Value								0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1			0	0	0	0	0	1
004h	RTC_CTRL	Reserved				CAOVIEN	TAMPOE	Reserved	IETSEN	COEN	OUTSEL[1:0]		OPOL	CALOSEL	BAKP	SU1H	AD1H	TSIEN	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	CAOVEN	HFMT	BYPS	REFCLKEN	TEDGE	WKUPSEL[2:0]		
	Reset Value					0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000h	RTC_INITSTS	Reserved							BKSRAMEF	IETSF	CAOVF	TAM8F	TAM7F	TAM6F	TAM5F	TAM4F	RECPF	TAM3F	TAM2F	TAM1F	TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
	Reset Value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
004h	RTC_PRE	Reserved							DIVA[6:0]									Reserved	DIVS[14:0]														
	Reset Value								1	1	1	1	1	1	1				0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
008h	RTC_WKUPT	Reserved																WKUPT[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
01Ch	RTC_ALARMA	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	RTC_ALARMB	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	RTC_WRP	Reserved																								PKEY[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
028h	RTC_SUBS	Reserved																SS[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	RTC_SCTRL	AD1S	Reserved																SUBF[14:0]														
	Reset Value	0																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	RTC_TST	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SET[2:0]			SEU[3:0]			
	Reset Value										0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	0
034h	RTC_TSD	Reserved							YRT[3:0]					YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved	DAT[1:0]		DAU[3:0]				

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	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	RTC_TSSS	Reserved								SSE[15:0]																	
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	RTC_CALIB	Reserved													CP	CW8	CW16	CM[8:0]									
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0
044h	RTC_ALRM ASS	Reserved								MASKSSA[3:0]				Reserved	SSV[14:0]												
	Reset Value									0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
048h	RTC_ALRM BSS	Reserved								MASKSSB[3:0]				Reserved	SSV[14:0]												
	Reset Value									0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	RTC_OPT	Reserved																									TYPE
	Reset Value																										0
050h ~ 0CCh	RTC_BKPx	BF[31:0]																									
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0D4h	RTC_TMPC FG	Reserved													TPPUDIS	TPPRCH[1:0]		TPFLT[1:0]		TPFREQ[2:0]			TPTS	Reserved		TPINTEN	Reserved
	Reset Value														0	0	0	0	0	0	0	0	0				0	
0D8h ~ 0F4h	RTC_TMPxC TRL	Reserved																							TPMF	TPNOE	TPINTEN	TP1TRG	TPEN
	Reset Value																								0	0	0	0	0

25.3.2 RTC Calendar Time Register (RTC_TSH)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									APM	HOT[1:0]		HOU[3:0]			
									rw	rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	MIT[2:0]			MIU[2:0]				Reserved	SCT[2:0]			SCU[3:0]			
	rw			rw					rw			rw			

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM format.

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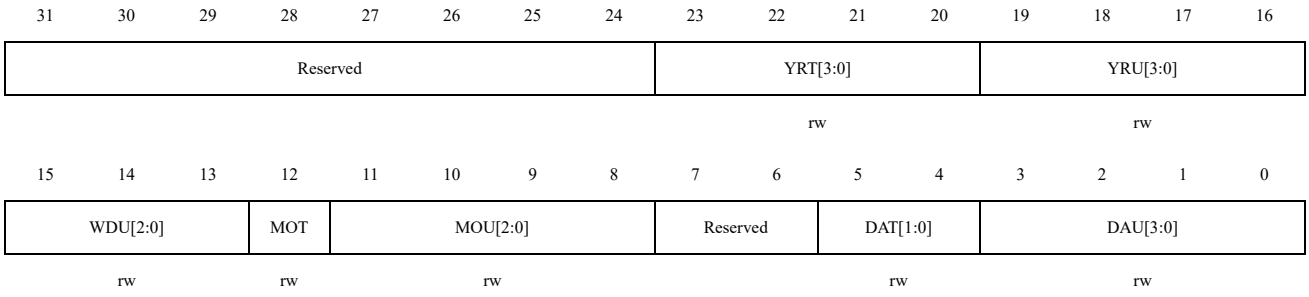
		0:AM format or 24-hour format 1:PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT [2: 0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SCT[2:0]	Describes the second tens value in BCD format
3:0	SCU[3:0]	Describes the second units value in BCD format

25.3.3 RTC Calendar Date Register (RTC_DATE)

Address offset: 0x04

Reset value: 0x0000 2101



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	YRT[3:0]	Describes the year tens value in BCD format
19:16	YRU[3:0]	Describes the year units value in BCD format
15:13	WDU[2:0]	Describes which Week day 000: Forbidden

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Bit Field	Name	Description
		001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

25.3.4 RTC Control Register (RTC_CTRL)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				CAOVIEN	TAMPOE	Reserved	IETSEN	COEN	OUTSEL[1:0]		OPOL	CALOSEL	BAKP	SU1H	AD1H
				rw	rw		rw	rw	rw		rw	rw	rw	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSIEN	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	CAOVEN	HFMT	BYPS	REFCLKEN	TEDGE	WKUPSEL[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27	CAOVIEN	Calendar overflow interrupt enable 0: Calendar overflow Interrupt disable 1: Calendar overflow Interrupt enable
26	TAMPOE	Tamper output enable 0: Disable Tamper output 1: Enable Tamper output

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25	Reserved	Reserved, the reset value must be maintained
24	IETSEN	Internal event trigger Timestamp Enable 0: Internal event trigger Timestamp disabled 1: Internal event trigger Timestamp enabled
23	COEN	Calibration output enable 0: Disable calibration output 1: Enable calibration output
22:21	OUTSEL[1:0]	Output selection These bits are used to select the alarm/wakeup output 00: Disable output 01: Enable Alarm A output 10: Enable Alarm B output 11: Enable Wakeup output
20	OPOL	Output polarity bit This bit is used to configure the polarity of output. 0: When the ALAF/ALBF/WTF flag is set to 1 (depending on OUTSEL [1:0]), the pin outputs a high level pulse 1: When the ALAF/ALBF/WTF flag is set to 1 (depending on OUTSEL [1:0]), the pin outputs a low level pulse
19	CALOSEL	Calibration output selection When COEN=1, this bit selects which signal is output on RTC_CALIB Under the conditions of RTCCLK at 32.768 kHz and default prescaler values (RTC_PRE.DIVA[6:0]=127 and RTC_PRE.DIVS[14:0]=255), these frequencies are valid. 0: Calibration output is 256 Hz 1: Calibration output is 1 Hz
18	BAKP	This bit can be written by the user to remember if daylight saving time changes have been applied.
17	SU1H	Subtract 1 hour (winter time change) 1 hour will be subtracted to the calendar time when the current hour value is not 0. This bit is always read as 0. Setting this bit is invalid when the current hour is 0

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		0: No effect. 1: Subtracts 1 hour to the current time. This can be used to change the outdoor initialization mode in winter.
16	AD1H	Add 1 hour (summer time change) When this bit is set, 1 hour can be added to the calendar time. This bit is always read as. 0: No effect. 1: Adds 1 hour to the current time. This can be used to change the outdoor initialization mode in summer.
15	TSIEN	Timestamp interrupt enable. 0: Disable Timestamp interrupt 1: Enable Timestamp interrupt
14	WTIEN	Wakeup timer interrupt enable 0: Disable wakeup timer interrupt. 1: Enable wakeup timer interrupt.
13	ALBIEN	Alarm B interrupt enable 0: Disable Alarm B interrupt 1: Enable Alarm B Interrupt
12	ALAIEN	Alarm A interrupt enable 0: Disable Alarm A interrupt 1: Enable Alarm A interrupt
11	TSEN	Timestamp enable 0: Disable timestamp 1: Enable timestamp
10	WTEN	Wakeup timer enable 0: Disable wakeup timer 1: Enable wakeup timer
9	ALBEN	Alarm B enable 0: Disable Alarm B 1: Enable Alarm B

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8	ALAEN	Alarm A enable 0: Disable Alarm A 1: Enable Alarm A
7	CAOVEN	Calendar overflow detection enable 0: Calendar overflow detection disabled 1: Calendar overflow detection enabled
6	HFMT	Hour format bit 0: 24 hour format 1: Am/PM format
5	BYPS	Bypass values from the shadow registers 0: Calendar values(when reading from RTC_SUBS、RTC_TSH and RTC_DATE) are copied from the shadow registers, which are refreshed every two RTCCLK cycles. 1: Calendar values(when reading from RTC_SUBS、RTC_TSH and RTC_DATE) are copied directly from the calendar counters. *Note: If the frequency of the APB1 clock falls below seven times the frequency of RTCCLK, RTC_CTRL.BYPS bit must be set to '1'*
4	REFCLKEN	RTC_REFIN reference clock detection bit (50 or 60Hz). 0: Disable RTC_REFIN detection 1: Enable RTC_REFIN detection *Note: RTC_PRE.DIVS[14:0] must be 0x00FF*
3	TEDGE	Time-stamp event active edge 0: Generate a timestamp event on the rising edge of the RTC_TS input 1: Generate a timestamp event on the falling edge of the RTC_TS input Note: When changing TEDGE, RTC_CTRL.TSEN must be reset to avoid accidentally setting RTC_INITSTS.TISF to 1
2:0	WKUPSEL[2:0]	Wakeup clock selection 000: RTC clock is divided by 16 001: RTC clock is divided by 8 010: RTC clock is divided by 4 011: RTC clock is divided by 2

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		10x: ck_spre (usually 1Hz) clock is selected 11x: ck_spre (usually 1Hz) clock is selected and configure the wake-up timer counter value to 2^{16}

25.3.5 RTC Initial Status Register (RTC_INITSTS)

Address offset: 0x0C

Reset value: 0x0000 0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							BKSRAMEF	IETSF	CAOVF	TAM8F	TAM7F	TAM6F	TAM5F	TAM4F	RECPF
							r	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAM3F	TAM2F	TAM1F	TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rw	r	rc_w0	r	r	r	r	r

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	BKSRAMERF	The back up sram is erased whenever the tampx_noerase bit is reset. This bit indicate that if the erase operation is in progress 0: BKP_SRAM erase operation is either complete or not triggered. 1: BKP_SRAM erase operation is in progress. This is a software read-only bit and is controlled entirely by hardware.
23	IETSF	Internal event Timestamp Flag This flag is set by hardware when an internal timestamp event is detected on the RTC_ITS input. It is cleared by software writing 0
22	CAOVF	CALOVFF detection flag This flag is set by hardware when calendar overflow detection was enabled and calender date reads 31/12/99 and time 23:59:59 occurred.It is cleared by software writing 0 after the calendar is reinitialized.
21	TAMP8F	RTC_TAMP8 detection flag When a tamper event is detected on the RTC_TAMP8 input, the hardware sets this flag.

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Bit Field	Name	Description
		Writing 0 through software clears it.
20	TAMP7F	RTC_TAMP7 detection flag When a tamper event is detected on the RTC_TAMP7 input, the hardware sets this flag. Writing 0 through software clears it.
19	TAMP6F	RTC_TAMP6 detection flag When a tamper event is detected on the RTC_TAMP6 input, the hardware sets this flag. Writing 0 through software clears it.
18	TAMP5F	RTC_TAMP5 detection flag When a tamper event is detected on the RTC_TAMP5 input, the hardware sets this flag. Writing 0 through software clears it.
17	TAMP4F	RTC_TAMP4 detection flag When a tamper event is detected on the RTC_TAMP4 input, the hardware sets this flag. Writing 0 through software clears it.
16	RECPF	Recalibration pending flag The RECPF status flag is automatically set to '1' when software writes to the RTC_CALIB register, indicating that the RTC_CALIB register is blocked. After the new calibration settings are processed, this bit returns to '0'.
15	TAM3F	RTC_TAMP3 detection flag When a tamper event is detected on the RTC_TAMP3 input, the hardware sets this flag. Writing 0 through software clears it.
14	TAM2F	RTC_TAMP2 detection flag. When a tamper event is detected on the RTC_TAMP2 input, the hardware sets this flag. Writing 0 through software clears it
13	TAM1F	RTC_TAMP1 detection flag. When a tamper event is detected on the RTC_TAMP1 input, the hardware sets this flag. Writing 0 through software clears it.
12	TISOVF	The time-stamp overflow flag When a timestamp event occurs while the TISF bit has already been set to 1, the hardware sets this flag to 1. It is recommended to check and clear the TISOVF bit after clearing the TISF bit. Otherwise, if the timestamp event occurs just before clearing the TISF bit, the

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Bit Field	Name	Description
		overflow event might be missed
11	TISF	Time-stamp flag This flag is set to '1' by hardware when a time-stamp event occurs. This flag can be cleared by software by writing 0
10	WTF	Wake up timer flag When the wake-up auto-reload counter reaches 0, the hardware sets this flag. This flag is cleared by software by writing 0. Before the WTF is set to 1 again, this flag must be cleared by software for at least 1.5 RTCCLK cycles
9	ALBF	Alarm B flag This flag is set to '1' by hardware when the time/date registers(RTC_TSH and RTC_DATE) value match the Alarm B register(RTC_ALARMB) values. This flag can be cleared by software by writing 0
8	ALAF	Alarm A flag This flag is set to '1' by hardware when the time/date registers(RTC_TSH and RTC_DATE) value match the Alarm A register(RTC_ALARMA) values. This flag can be cleared by software by writing 0
7	INITM	Enter Initialization mode 0: Free operating mode 1: Enter initialization mode and set calendar time value, date value, and prescale value.
6	INITF	Initialization flag RTC is in initialization state when this bit is '1', and calendar time, date and prescale value can be updated. 0: Calendar register can not be updated 1: Calendar register can be updated
5	RSYF	Register synchronization flag This flag is set to '1' by hardware when the calendar value are copied into the shadow registers. This bit is cleared by hardware when in initialization mode, while a shift operation is pending (SHOPF = 1), or when in bypass shadow register mode (RTC_CTRL.BYPS = 1). This bit can also be cleared by software. It is cleared either by software or by hardware in initialization mode.

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Bit Field	Name	Description
		0: Calendar shadow register not yet synchronized 1: Calendar shadow register synchronized
4	INITSF	Initialization status flag This flag is set to '1' by hardware when the calendar year field is different from 0 (which is the RTC domain reset state). 0: Calendar has not been initialized 1: Calendar has been initialized
3	SHOPF	Shift operation pending flag This flag is set to '1' by hardware as soon as a shift operation is initiated by a write to the RTC_SCTRL register. It is cleared by hardware when the corresponding shift operation has been completed, note that writing to the SHOPF bit has no effect. 0: No shift operation is pending 1: A shift operation is pending
2	WTWF	Wakeup timer write flag 0: Wakeup timer configuration update is not allowed 1: Wakeup timer configuration update is allowed
1	ALBWF	Alarm B write flag This flag is set to '1' by hardware when Alarm B values can be changed, after the RTC_CTRL.ALBEN bit has been set to 0. 0: Alarm B update is not allowed 1: Alarm B update is allowed
0	ALAWF	Alarm A write flag. This flag is set to '1' by hardware when Alarm A values can be changed, after the RTC_CTRL.ALAEN bit has been set to 0. 0: Alarm A update is not allowed 1: Alarm A update is allowed

25.3.6 RTC Prescaler Register (RTC_PRE)

Address offset: 0x10

Reset value: 0x007F 00FF

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									DIVA[6:0]						
									rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DIVS[14:0]														
	rw														

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22:16	DIVA[6:0]	Asynchronous prescaler factor f_{ck_apre} = RTCCLK/(DIVA[6:0]+1) *Note: RTC_PRE.DIVA[6:0] cannot be configured to 0.*
15	Reserved	Reserved, the reset value must be maintained
14:0	DIVS[14:0]	Synchronous prescaler factor $f_{ck_spre} = f_{ck_apre}$/(DIVS[14:0]+1)

25.3.7 RTC Wakeup Timer Register (RTC_WKUPT)

Address offset: 0x14

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUPT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WKUPT[15:0]	Wake up auto-reload value bits The RTC_INITSTS.WTF flag is set every (WKUPT[15:0] + 1) ck_wut cycles when the RTC_CTRL.WTEN=1. The wakeup timer becomes 17-bits When RTC_CTRL.WKUPSEL[2]=1.

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		Note: This register change (such as the second setting or later Settings) needs to be changed in the wakeup interrupt, otherwise the changed settings will not take effect immediately, but will take effect after the next wakeup; *In particular, when RTC_CTRL.WKUPSEL[2:0] is set to 010, the modified setting does not take effect immediately, but will take effect after wake up in the next cycle.*

25.3.8 RTC Alarm A Register (RTC_ALARMA)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	
MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]			
rw	rw	rw		rw				rw	rw	rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
rw	rw			rw				rw	rw			rw			

Bit Field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format

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21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

25.3.9 RTC Alarm B Register (RTC_ ALARMB)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	1
MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]			
rw	rw	rw		rw				rw	rw	rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
rw	rw			rw				rw	rw			rw			

Bit Field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units

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		1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

25.3.10 RTC Write Protection register (RTC_WRP)

Address offset: 0x24

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PKEY[7:0]							
								w							

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	PKEY[7:0]	Write protection key Reading this byte always returns 0x00. For detail on how to unlock RTC register write protection, see chapter RTC write protection register.

25.3.11 RTC Sub-second Register (RTC_SUBS)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SS[15:0]	Sub-second value. The value is the counter value of synchronous prescaler. This sub-second value is calculated by the below formula: Sub-second value = (RTC_PRE.DIVS[14:0]-SS)/(RTC_PRE.DIVS[14:0]+1) *Note: SS[15:0] can be larger than RTC_PRE.DIVS[14:0] only after the shift operation is completed. In this case, the correct time/date is one second slower than the time/date indicated by RTC_TSH/RTC_DATE.*

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25.3.12 RTC Shift Control Register (RTC_ SCTRL)

Address offset: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	1
AD1S	Reserved														
w															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SUBF[14:0]														
	w														

Bit Field	Name	Description
31	AD1S	Add one second 0: No impact. 1: Add one second to the clock/calendar This bit can only be written and read as zero. Writing to this bit does not have an impact when RTC_INITSTS.SHOPF=1.
30:15	Reserved	Reserved, the reset value must be maintained
14:0	SUBF [14:0]	Subtract a fraction of a second These bits can only be written and read as zero. Writing to these bits has no effect when RTC_INITSTS.SHOPF=1. The value written to SUBF[14:0] is added to the synchronized prescaler counter, causing a delay in the clock: delay(seconds)= (SUBF[14:0]+1) / (DIVS[14:0] + 1) The AD1S bit can be used together with the SUBF[14:0] bits "Advance (seconds)= (1 - ((SUBF[14:0]+1) / (DIVS[14:0] + 1))) *Note: The RTC_INITSTS.RSYF bit will be cleared when writing to SUBF[14:0]. When RTC_INITSTS.RSYF=1, the shadow registers have been updated to the shifted time.*

25.3.13 RTC Timestamp Time Register (RTC_TST)

Address offset: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Rserved									APM	HOT[1:0]		HOU[3:0]			

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									r		r			r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rserved	MIT[2:0]			MIU[3:0]				Rserved	SET[2:0]			SEU[3:0]			
	r			r					r			r			

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM notation 0: AM or 24-hour format 1: PM
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

25.3.14 RTC Timestamp Date Register (RTC_TSD)

Address offset: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDU[2:0]			MOT	MOU[2:0]				Reserved		DAT[1:0]		DAU[3:0]			
r			r	r						r		r			

Bit Field	Name	Description

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31:16	Reserved	Reserved, the reset value must be maintained
15:13	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

25.3.15 RTC Timestamp Sub-Second Register (RTC_TSSS)

Address offset: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	1
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSE[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SSE[15:0]	Sub second value SSE[15:0] is the value in the synchronous prescaler counter. The fraction of a second is provided by the formula below: Second fraction = (RTC_PRE.DIVS[14:0] – SSE[15:0]) / (RTC_PRE.DIVS[14:0] + 1) *Note: SSE[15:0] can be larger than RTC_PRE.DIVS[14:0] only after a shift operation. In that*

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		case, the correct time/date is one second less than as indicated by RTC_TSH/RTC_DATE.

25.3.16 RTC Calibration Register (RTC_CALIB)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	1
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP	CW8	CW16	Reserved				CM[8:0]								
rw	rw	rw					rw								

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	CP	Increase frequency of RTC by 488.5 ppm This feature is intended to be used along with CM[8:0]. When frequency of RTCCLK is 32768 Hz, the number of RTCCLK pulses added during a 32-second window is ((512 * CP) – CM[8:0]). 0: No add pulse. 1: One RTCCLK pulse is inserted every 2^{11} pulses.
14	CW8	Select an 8-second calibration cycle period 0: Not effect. 1: Select an 8-second calibration period. When CW8 is set to ‘1’, the 8-second calibration cycle period is selected. *Note: when CW8 = 1, CM[1:0] will always be' 00'*
13	CW16	To select a 16-second calibration cycle period 0: Not effect. 1: Select a calibration period of 16 seconds. If CW8 = 1, this bit cannot be set to 1. *Note: when CW16 = 1, CM[0] will always be '0'*
12:9	Reserved	Reserved, the reset value must be maintained

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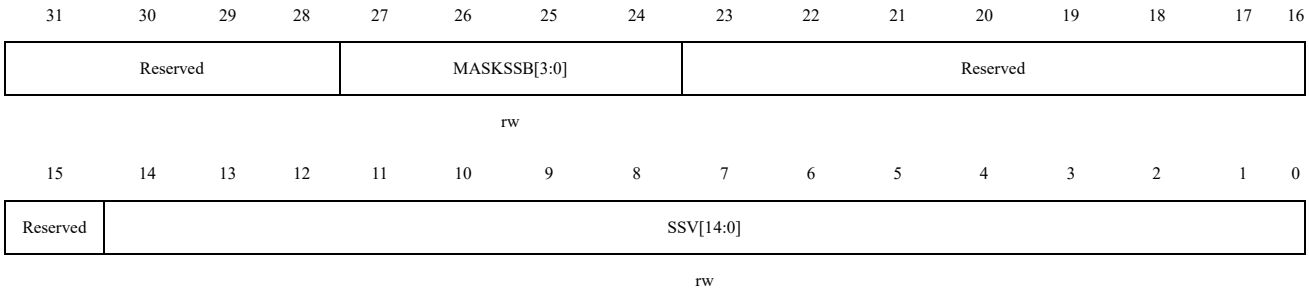
8:0	CM[8:0]	Negative calibration bits The number of mask pulse out of 2^{20} RTCCLK pulses. This effectively decreases the frequency of the calendar with a resolution of 0.9537 ppm.

25.3.17 RTC Alarm A Sub-Second Register (RTC_ ALRMASS)

Address offset: 0x44

Reset value: 0x0000 0000



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ... 0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
23:15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and

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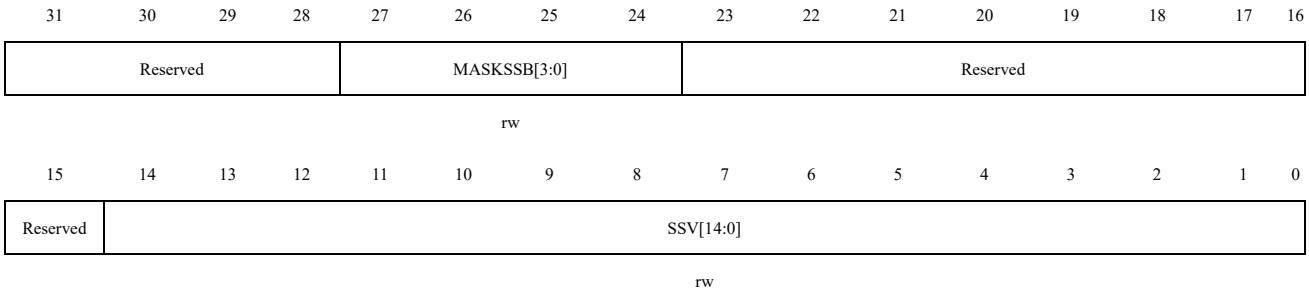
		bit number of compared is controlled by MASKSSB[3:0].

25.3.18 RTC Alarm B Sub-Second Register (RTC_ ALRMBSS)

Address offset: 0x48

Reset value: 0x0000 0000



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ... 0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
23:15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and bit number of compared is controlled by MASKSSB[3:0].

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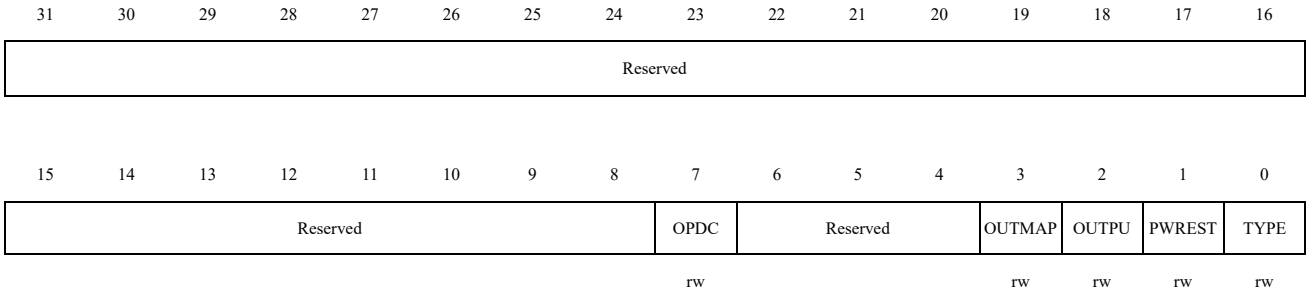
25.3.19 RTC Option Register (RTC_ OPT)

Address offset: 0x4C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7	OPDC	This bit is used to control the duty cycle when the output is selected as calibrateion clock output 0: calibrateion clock output dutycycle 50% 1: calibrateion clock output dutycycle 1/(RTC_PRES.DIVA/DIVS) This bit must be set while in Initialization mode
6:4	Reserved	Reserved, the reset value must be maintained
3	OUTMAP	This bit is used to decide the remapping of the outputs between RTC_OUT1 and RTC_OUT2. 0: No outputs on the RTC_OUT2. All are contained within RTC_OUT1. Mostly in Standby mode. 1: Used to route CALIB or TAMPALARM or WAKEUP to RTC_OUT2, freeing RTC_OUT1. For detail refer to
2	OUTPU	This bit is used to decide if RTC_OUTx should have a pull-up resistor to support open-drain configuration. (x=1,2) 0: Pull-up resistor not enabled on pad RTC_OUTx 1: Pull-up resistor enabled on pad RTC_OUTx
1	PWREST	Used to select between the signal type for power event 0: Power event is a pulse 1: Power event is a level signal that is disabled when the Status flag of the source responsible for pwr_event is disabled.

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Bit Field	Name	Description
0	TYPE	Output type on RTC_OUTx (x=1,2) 0: Push-pull output 1: Open-drain output

25.3.20 RTC Backup Register(RTC_ BKP(1~32))

Address offset：0x50-0xCC

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BF[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BF[15:0]															
rw															

Bit Field	Name	Description
31:0	BF[31:0]	Backup data These registers can be read and written by software. These registers are powered by BKR when MR is switched off, so they are not reset when the system resets, and the contents of the registers remain valid when the device is operating in low-power mode. If RTC_TMPCFG.TPxNOE=0, these registers are reset when an tamper event is detected

25.3.21 RTC Tamper Configuration Register（RTC_ TMPCFG）

Address offset：0xD4

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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TPPUDIS	TPPRCH[1:0]	TPFLT[1:0]	TPFREQ[2:0]	TPTS	Reserved	TPINTEN	Reserved
rw	rw	rw	rw	rw		rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	TPPUDIS	RTC_TAMPx pull-up disable bit. (x= 1,2,3) 0: Enable pre-charging of RTC_TAMPx pin before each sampling. 1: Disable pre-charging of RTC_TAMPx pin
14:13	TPPRCH[1:0]	RTC_TAMPx pre-charging duration. These bits determine the pre-charging time before each sampling. (x= 1,2,3) 0x0: 1 RTCCLK period 0x1: 2 RTCCLK periods 0x2: 4 RTCCLK periods 0x3: 8 RTCCLK periods
12:11	TPFLT[1:0]	RTC_TAMPx filter count. These bits determine the number of consecutive samples on a valid level. (x= 1,2,3,4,5,6,7,8) 0x0: Trigger tamper event after 1 sample on a valid level 0x1: Trigger tamper event after 2 consecutive samples on a valid level 0x2: Trigger tamper event after 4 consecutive samples on a valid level 0x3: Trigger tamper event after 8 consecutive samples on a valid level
10:8	TPFREQ[2:0]	Tamper sampling frequency. This bit determines the frequency at which each RTC_TAMPx input is sampled. (x= 1,2,3) 0x0: Sample once every 32768 RTCCLKs (frequency of 1 Hz when RTCCLK = 32.768 KHz) 0x1: Sample once every 16384 RTCCLKs 0x2: Sample once every 8192 RTCCLKs 0x3: Sample once every 4096 RTCCLKs 0x4: Sample once every 2048 RTCCLKs 0x5: Sample once every 1024 RTCCLKs 0x6: Sample once every 512 RTCCLKs 0x7: Sample once every 256 RTCCLKs

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7	TPTS	Enable timestamp on tamper detection event. 0: Do not save timestamp on tamper detection event 1: Save timestamp on tamper detection event TPTS remains valid even if RTC_CTRL.TSEN=0
6:3	Reserved	Reserved, the reset value must be maintained
2	TPINTEN	Tamper event interrupt enable. 0: Disable tamper interrupt 1: Enable tamper interrupt *Note: This bit enables interrupts for all tamper pin events, regardless of the RTC_TMPCTRL.TPINTEN level. If this bit is cleared, each tamper event interrupt can be individually enabled by setting RTC_TMPCTRLx.TPINTEN*
1:0	Reserved	Reserved, the reset value must be maintained

25.3.22 RTC Tamper Control Register（RTC_ TMPCTRLx）(x=[1..8])

Address offset：0xD8 + (x-1)×4

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved											TPMF	TPNOE	TPINTEN	TPTRG	TPEN
											rw	rw	rw	rw	rw

Bit Field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained
4	TPMF	Tamper mask flag. 0: Do not mask Tamper events. 1: Mask Tamper events. *Note: When TPMF is set, Tamper interrupt must not be enabled*
3	TPNOE	Tamper non-erase bit.

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		0: Tamper event erases backup registers. 1: Tamper event does not erase backup registers
2	TPINTEN	Tamper event interrupt enable. 0: Disable tamper interrupt 1: Enable tamper interrupt *Note: This bit enables interrupts for tamper events.*
1	TPTRG	Tamper event trigger mode. If TPFLT[1:0] != 00, tamper detection is in level mode: 0: High level triggers tamper detection event. 1: Low level triggers tamper detection event. If TPFLT[1:0] = 00, tamper detection is in edge mode: 0: Rising edge triggers tamper detection event. 1: Falling edge triggers tamper detection event. Note: Only used for TAMP1, TAMP2 and TAMP3
0	TPEN	RTC_TAMP detection enable bit. 0: Disable RTC_TAMP input detection 1: Enable RTC_TAMP input detection

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26 Analog-to-digital converters (ADC)

26.1 Introduction

There are up to 3 ADCs (Analog-to-digital converter) devices, which can be operating independently or combined as dual ADC (ADC1/ADC2); or as triple ADC (ADC1/ADC2/ADC3). Each ADC is a 12-bit/10-bit SAR ADC and has maximum 20 channels. Each channel input can be configured as single-ended or differential mode. ADC conversion can be started on only one channel (single mode), or a group of channels (scan mode). It can also automatically repeat the conversion without the next trigger if continuous or discontinuous mode is used. It also supports the oversampling mode to improve the accuracy of conversion by repeating the measurement of input and calculating the average result. The conversion results are reformatted before storing into 16-bit data registers, or directly transferred to DSMU. It supports the analog watchdogs to monitor whether some channels remain within a configured voltage range.

26.2 Main Features

The main features supported by ADC are shown below:

- Resolution: 12-bit, 10-bit.
- Differential mode, Single-ended mode (configurable per channel)
- 20 channels each ADC (total is 60), configurable for each conversion.
- Supports triggering the ADC using software trigger, hardware trigger (Timer, EXTI).
- Three Analog watchdog allow software to detect when the input voltage is above or below the specified value.
- Interrupt generation at ADC ready, the end of sampling, the end of conversion (regular or injected), end of sequence conversion (regular or injected), analog watchdog.
- Conversion modes
  - Single mode: convert a single selected channel once per trigger
  - Continuous mode: convert selected channels (single or scan) continuously
  - Scan mode: convert a group of selected channels once per trigger
  - Discontinuous mode
- Self-calibration
- Data alignment (left or right)
- Sampling time configurable for each channel
- ADC working clock is from PLL clock or AHB clock
- Data can be managed by DMA, DSMU
- FIFO for conversion data
- Start and stop conversion mode

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- Start and stop regular and injected conversions by software
- Start and stop regular and injected conversions using externally configurable polarity triggers (GPIO input events or internal timer events)

- Oversampling
  - Adjustable oversampling ratios x1, x2, x4, x8, x16, x32, x64, x128, x256, x512, x1024
  - Data right shift of 0-10 bits (configurable)
  - 1 Conversion result is stored in 16-bit unsigned data format (truncating if overflow)
- Data preprocessing
  - Support gain compensation
  - Support offset compensation
- Multiple ADC modes
  - Dual ADC mode: Combination of ADC1 (Master) and ADC2 (Slave)
  - Triple ADC mode: Combination of ADC1 (Master), ADC2 and ADC3 (Slaves)
- ADC Power supply requirements ： 1.7V to 3.6V
- ADC input range：$V_{REF-} \leq V_{IN} \leq V_{REF+}$

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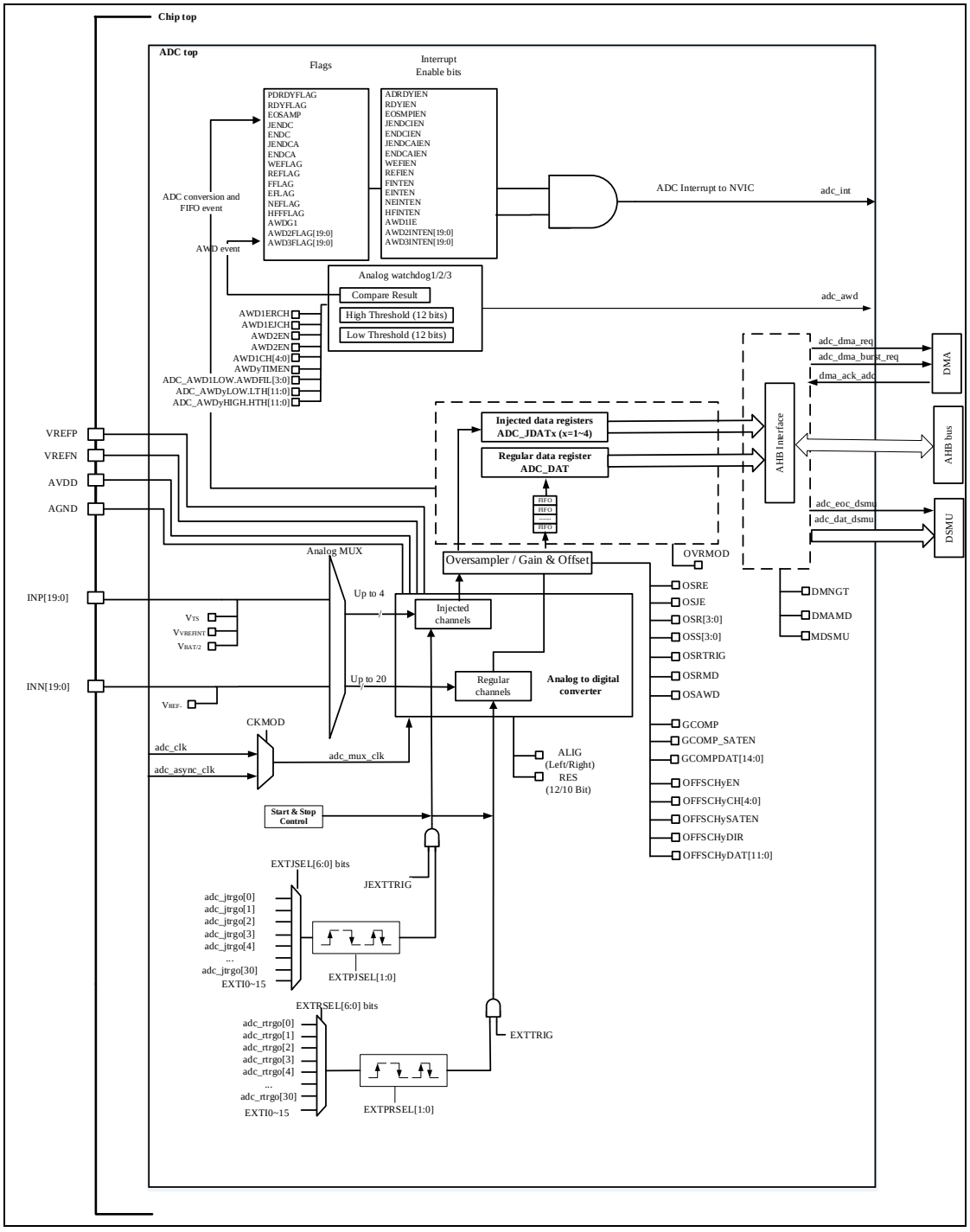
26.3 Block diagram

Figure 26-1 Block Diagram



26.4 ADC pins and internal signals

Table 26-1 ADC Pin Definitions

Name	Signal type	Description

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VREFP	Input, positive analog reference voltage	The higher/positive reference voltage used by the ADC 2.3V ≤ VREFP ≤ AVDD（3.6V）
VREFN	Input, negative analog reference voltage	The lower/negative reference voltage used by the ADC
AVDD	Input, analog power supply	Analog power supply: 2.3V ≤ AVDD ≤3.6V
AGND	Input, analog power ground	Analog ground
INP[19:0]	Positive analog input signal	Support for up to 20 external analog input channels
INN[19:0]	Negative analog input signal	Support for up to 20 external analog input channels

26.5 Function Description

Figure 26-2 Clock scheme

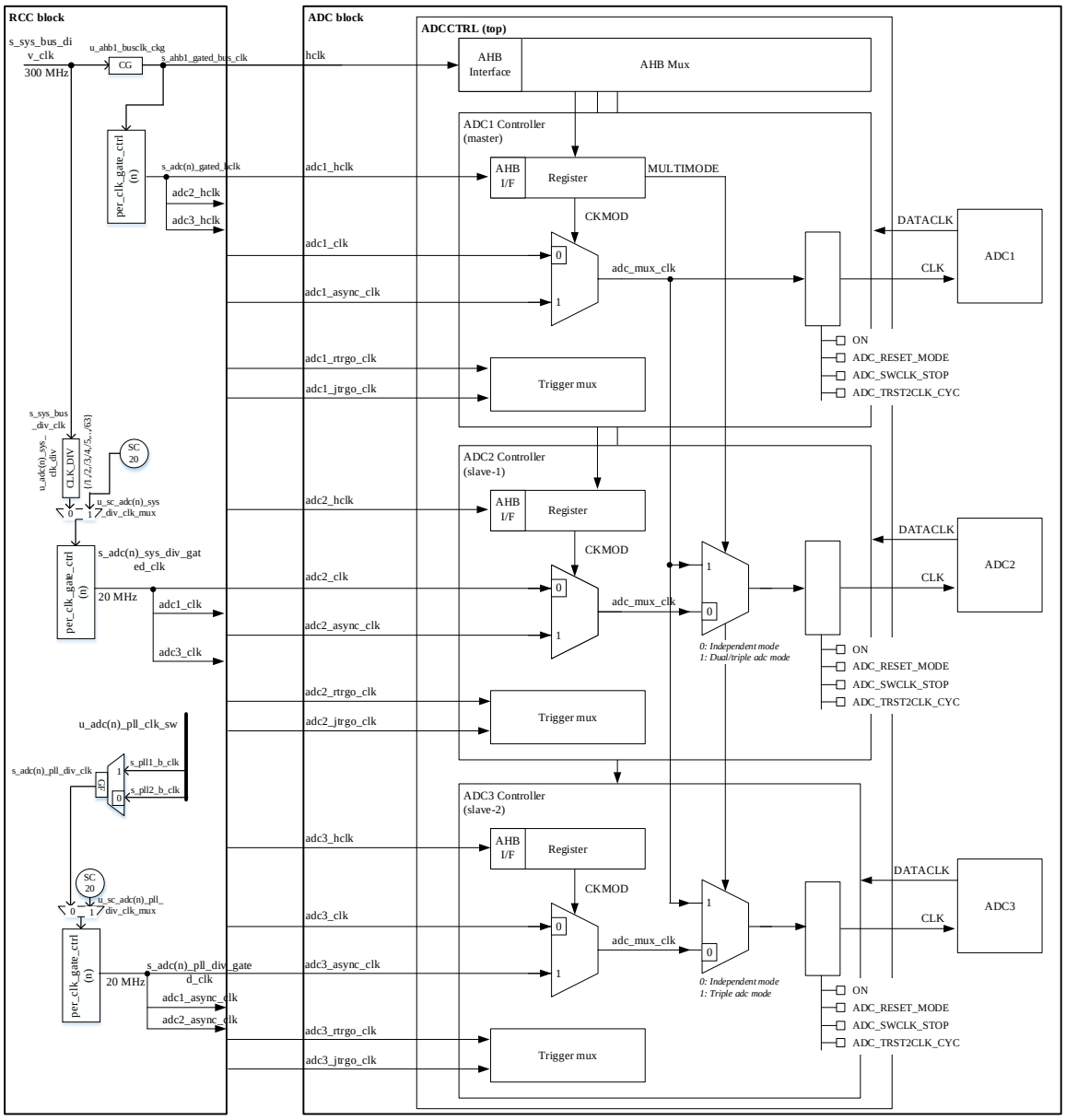

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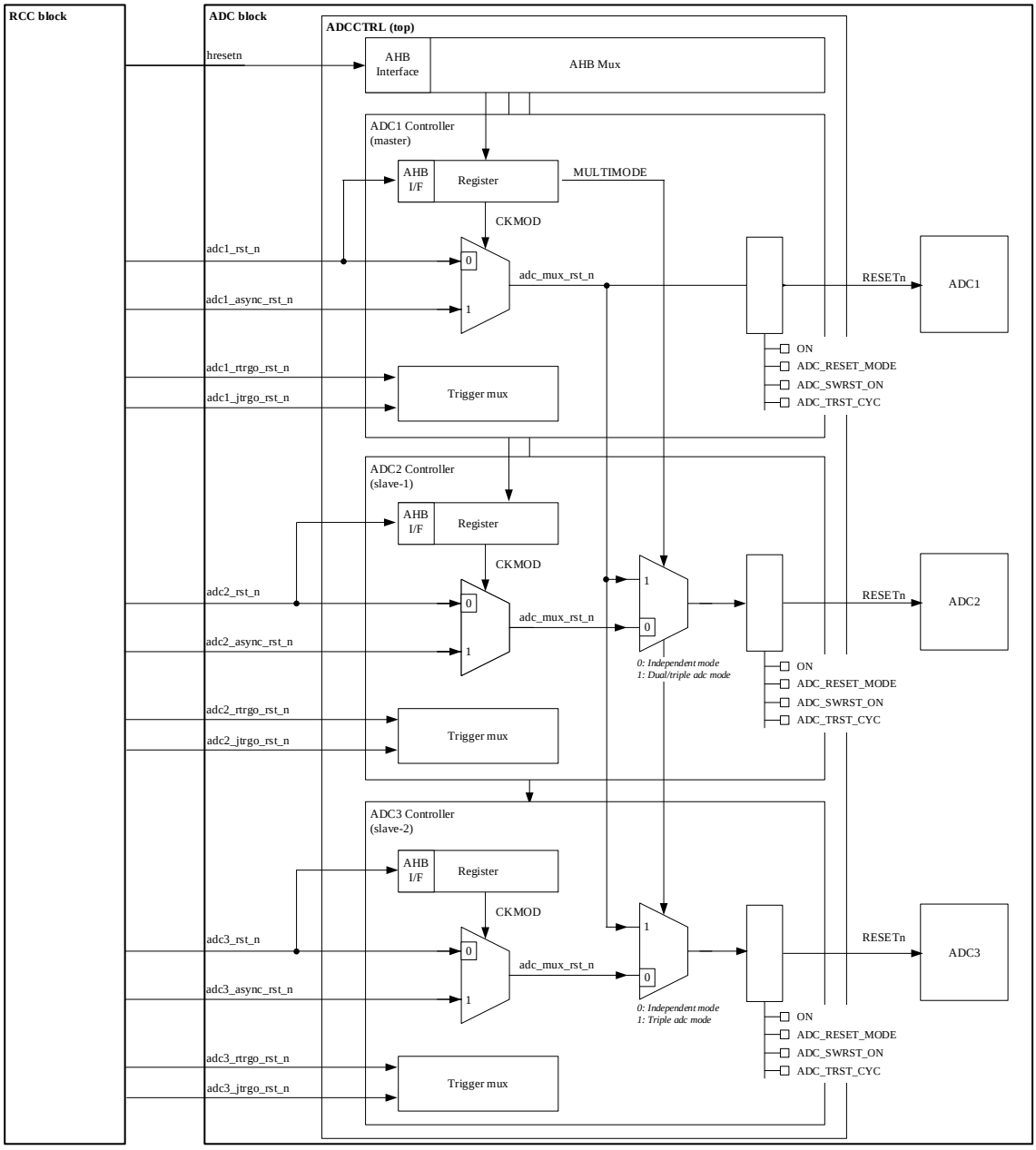
Figure 26-3 Reset scheme



All clock and reset inputs to ADC block are configured by RCC register. There is no pre-scaler or divider inside ADC controller. ADC_CTRL3.CKMOD register bit is to select between AHB synchronous clock or PLL asynchronous clock provided to ADC kernel clocks. Clock and reset are controlled by ADC_CTRL2.ON and ADC_PUCFG register bits. Below is some notes for clock input configuration:

Note:

1. *hclk, adc1_hclk, adc2_hclk, adc3_hclk are same clocks*
2. *adc1_clk, adc2_clk, adc3_clk can be different clocks*
3. *adc1_async_clk, adc2_async_clk, adc3_async_clk can be different clocks. However, since only two pll clocks (s_pll1_b_clk, s_pll2_b_clk) can be set for ADCs, at least two of them are same, e.g. adc1_async_clk =*

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adc2_async_clk, adc3_async_clk is different.

4. *adc1_rst_n, adc2_rst_n, adc_3_rst_n are used for register configuration of each ADC, instead of hresetn. This allows each ADC can be soft reset independently with AHB bus reset.*
5. *In dual mode, ADC_CTRL3.CKMOD of ADC1 and ADC2 must be same, ADC_CTRL3.CKMOD of ADC3 is independent.*
6. *In triple mode, ADC_CTRL3.CKMOD of ADC1, ADC2 and ADC3 must be same.*

26.5.1 ADC enable-disable control

ADC is enable or disable by controlling ADC_CTRL2.ON bit.

There is a set of status register bits available during ADC enabling sequence:

- PDRDY: Indicating ADC is currently in power-down state. It is set and clear by hardware.

Software can check it to configure ADC_CTRL3.CKMOD and ADC_PUCFG register bits before setting ON=1.

- RDY: Indicating ADC is enable and ready for operation. It is set and clear by hardware. Software can check it to start ADC operation (set ADC_CTRL3.RSTART or ADC_CTRL3.JSTART).
- PDRDYFLAG: Indicating the disable ADC procedure is finished. It is set by hardware and cleared by software. An interrupt is associated to it.
- RDYFLAG: Indicating the enable ADC procedure is finished. It is set by hardware and cleared by software. An interrupt is associated to it.

Clock and reset during ADC enable-disable sequence can be controlled by hardware or software.

In case of hardware-controlled: Set ADC_PUCFG.RSTMD=0, configure ADC_PUCFG.RST_TIMESEL and ADC_PUCFG.RSTCLK_TIMESEL as shown as below.

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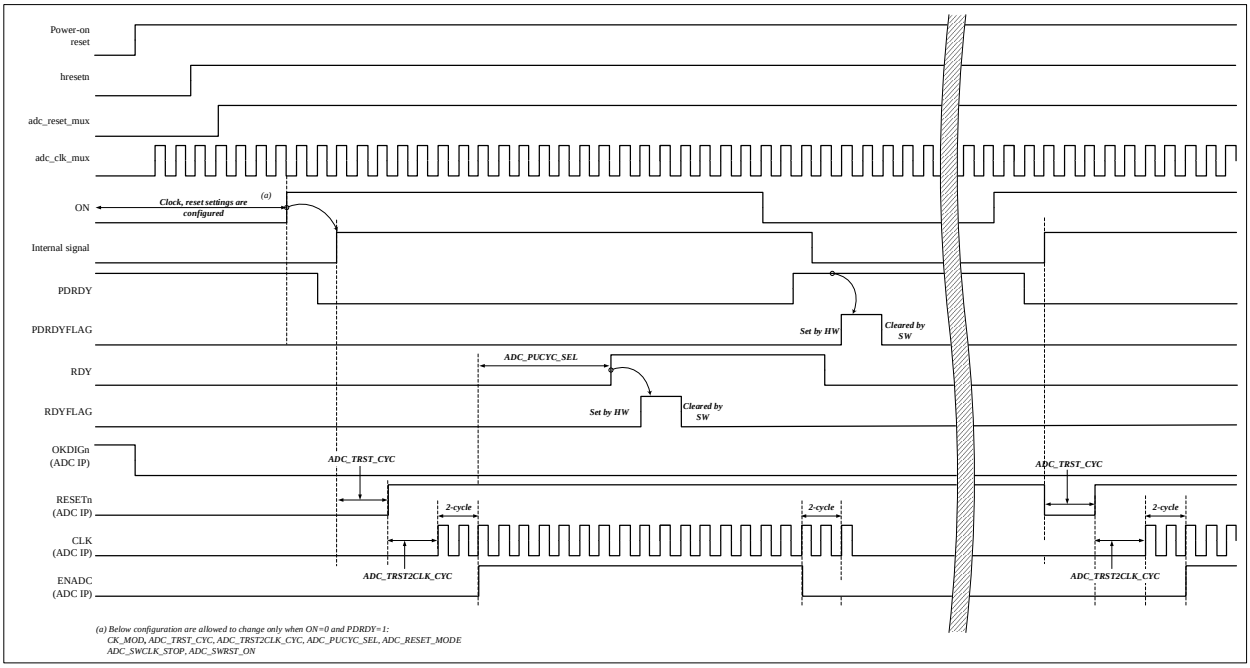
Figure 26-4 ADC enable-disable sequence (ADC_PUCFG.RSTMD=0)



In case of software-controlled: Set ADC_PUCFG.RSTMD=1, and write to ADC_PUCFG.SWRSTEN, ADC_PUCFG.SWCLKSTOP. When ADC_PUCFG.SWRSTEN=1, the RESETn=0 and vice versa. When ADC_PUCFG.SWCLKSTOP=1, the clock (CLK) is disable to ADC IP and vice versa.

In both of cases, check below notes of ADC IP Vervesemi specification for timing requirement to control properly.

Software procedure to enable ADC:

1. Read PDRDY bit to ensure it is 1.
2. Configure ADC_CTRL3.CKMOD, and ADC_PUCFG register bits.

   In case ADC_PUCFG.RSTMD=1 (software-controlled), setting ADC_PUCFG.SWRSTEN and ADC_PUCFG.SWCLKSTOP to control the reset and clock provided to ADC IP (see Note-3 for ADC IP specification) before set ON.
3. Set ADC_CTRL3.ON=1.
4. Wait until RDYFLAG=1. This can be done using the associated interrupt (set RDYIEN = 1).
5. Clear RDYFLAG by writing 0 to this bit.
6. ADC is now enabled; it is possible to start operation on it (set ADC_CTRL3.RSTART or ADC_CTRL3.JSTART)

Software procedure to disable ADC:

1. Check that both ADC_CTRL3.RSTART = 0 and ADC_CTRL3.JSTART = 0 to ensure that no conversion is ongoing. If required, stop any regular and injected conversion ongoing by setting SWRSTOP = 1 and SWJSTOP = 1 and then wait until ADC_CTRL3.RSTART = 0 and ADC_CTRL3.JSTART = 0. In case of multi-adc mode, check all ADC_CTRL3.RSTART and ADC_CTRL3.JSTART bits of both master and associated slave(s).
2. Reset ADC_CTRL3.ON=0.

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3. Wait until PDRDYFLAG is 1. This can be done using the associated interrupt (set PDRDYIEN = 1).
4. ADC is now disabled.

Note:

1. *It is recommended to set ADC_CTRL3.ON=1 again only after ADC is completely disabled (PDRDY = 1).*
2. *ADC_CTRL3.CKMOD, and ADC_PUCFG register bits are allowed to change only when ON = 0 and PDRDY = 1.*

26.5.2 Start and stop ADC operation

26.5.2.1 Start ADC operation:

After enabling ADC and PRDY=1, user can start ADC operation by setting ADC_CTRL3.RSTART = 1 (regular) or ADC_CTRL3.JSTART = 1 (injected). Only when ADC operation started, user can set triggers to start conversion on ADC channels. See 26.5.4 for more detail on trigger sources.

If software trigger is selected (ADC_CTRL2.EXTPRSEL[1:0]=00 for regular, ADC_CTRL2.EXTPJSEL[1:0]=00 for injected), set ADC_CTRL2.SWSTRRCH=1 to start the regular conversion, or set ADC_CTRL2.SWSTRJCH=1 to start the injected conversion.

If hardware trigger is selected (ADC_CTRL2.EXTPRSEL[1:0] = 01, 10 or 11) for regular, ADC_CTRL2.EXTPJSEL[1:0] = 01, 10 or 11 for injected), the conversion is started when the corresponding trigger is active.

Note:

In auto-injection mode (ADC_CTRL1.AUTOJC = 1), the injected conversion is auto-started after the related regular conversion. It must not use ADC_CTRL3.JSTART in that mode.

The ADC_CTRL3.RSTART or ADC_CTRL3.JSTART is cleared after stopping ADC operation by setting ADC_CTRL3.SWRSTOP=1 (regular) or ADC_CTRL3.SWJSTOP=1 (injected). Especially, in case of non-continuous mode (ADC_CTRL2.CTU=0) and software trigger is selected, the ADC_CTRL3.RSTART or ADC_CTRL3.JSTART can be auto-cleared after each conversion completed if DREGCH=0, or can be auto-cleared after end of subgroup of conversion sequences if ADC_CTRL1.DREGCH=1 (discontinuous mode).

Note:

1. *In discontinuous mode case, although the ADC_CTRL3.RSTART or ADC_CTRL3.JSTART is auto-cleared, but internal signals for discontinuous conversion group are still kept. Therefore, user should not change configuration until last channel (defined by ADC_RSEQ1.LEN[4:0] or ADC_JSEQ.JLEN[1:0])*
2. *When the software trigger is selected, ADC_CTRL3.RSTART/ADC_CTRL3.JSTART bit should not be set if the ADC_STS.ENDCA, ADC_STS.ENDC/ADC_STS.JENDCA, ADC_STS.JENDC is still high.*

26.5.2.2 Stop ADC operation:

User can terminate the on-going conversions by setting ADC_CTRL3.SWRSTOP = 1 for regular conversions or ADC_CTRL3.SWJSTOP = 1 for injected conversions.

Terminating the regular conversion is independent with injected conversion and vice versa. It means that setting

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ADC_CTRL3.SWRSTOP = 1 doesn't affect to on-going injected conversion, and ADC_CTRL3.SWJSTOP = 1 doesn't affect to on-going regular conversion.

If the conversion is terminated at middle, the conversion data is aborted and not updated to data register. In case of scan mode, continuous or discontinuous mode, the sequence is also terminated.

Note: *In auto-injection mode (ADC_CTRL1.AUTOJC = 1), setting ADC_CTRL3.SWRSTOP=1 terminates both regular and injected conversions It must not use ADC_CTRL1.SWJSTOP in that mode.*

Figure 26-5 and Figure 26-6 show timing diagram to start and stop ADC operation on regular and injected channel respectively.

Figure 26-5 Start and stop regular channel conversion

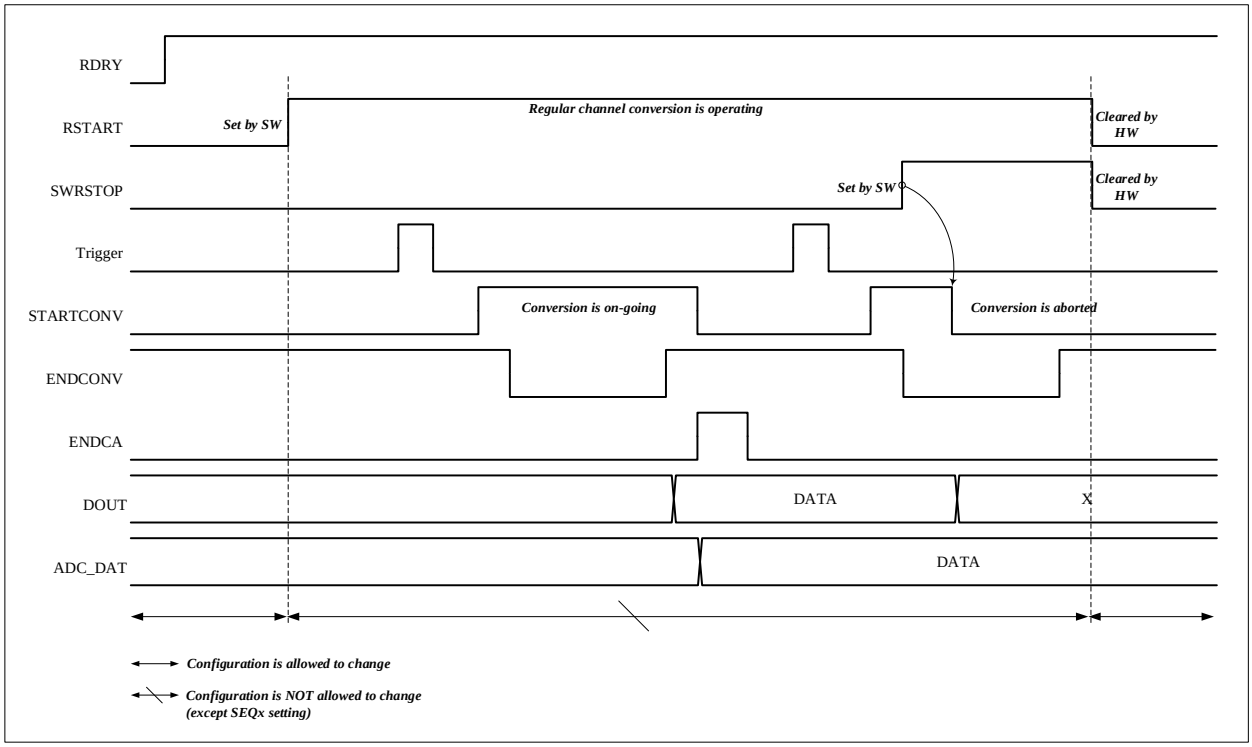

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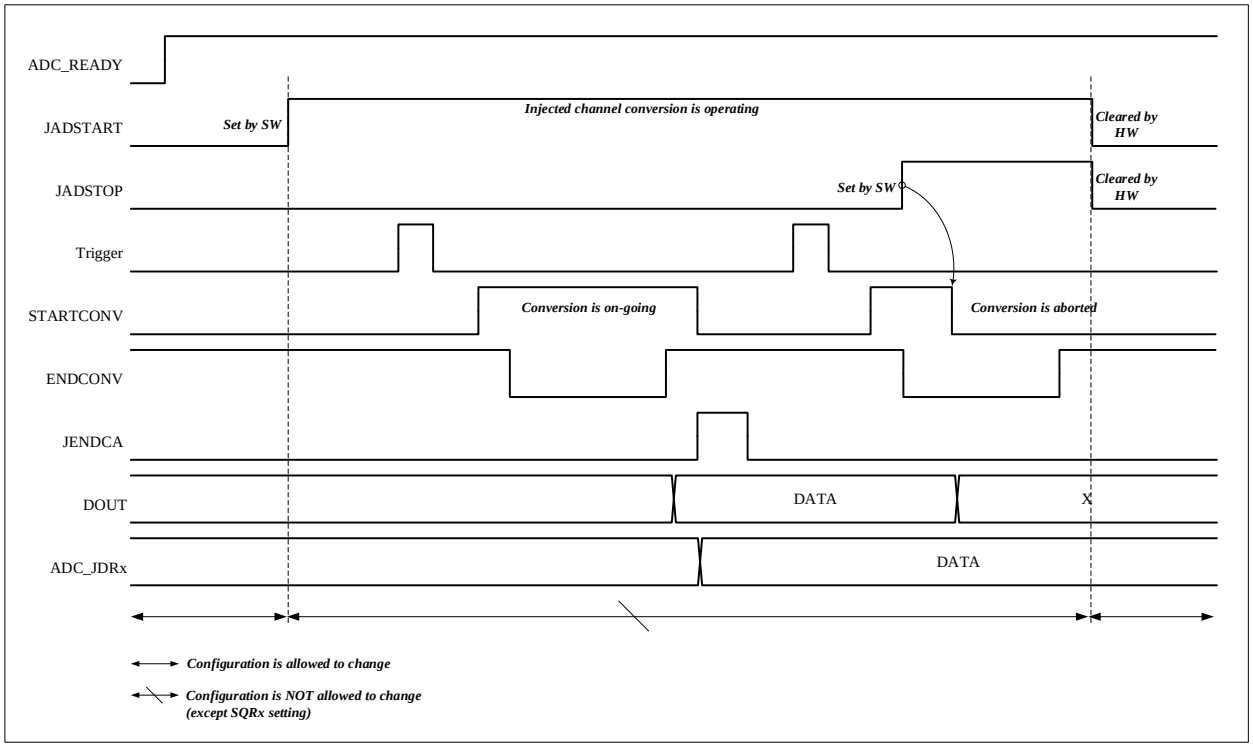
Figure 26-6 Start and stop injected channel conversion



26.5.3 Channel configuration

It supports a maximum of 20 multiplexed channels each ADC.

Each channel can be configured as a regular conversion type or an injected conversion type.

The regular sequence is configured to perform multiple conversions, up to a maximum of 20. The ADC_RSEQx registers specify the regular channels and the conversion sequence of the regular channels. The ADC_RSEQ1.LEN[4:0] bits specified regular channel sequence length.

The injection sequence is also configured to perform multiple conversions, up to a maximum of 4. The ADC_JSEQ register specifies the injection channel and the conversion sequence of the injection channel. The ADC_JSEQ.JLEN[1:0] bits specified injection sequence length.

Note that an injected conversion can interrupt the regular conversion sequence. When that injected conversion is finished, the regular conversion sequence can be restored. However, a regular cannot interrupt the injected conversion. If regular conversion is triggered at middle of an injected conversion sequence, it must wait until that injected conversion sequence completed before executing the regular conversion. This is also applied in case of single conversion with sequence length is 1.

The software is allowed to modify on-the-fly the ADC_RSEQx register (include LEN) when ADC_CTRL3.RSTART is set (regular conversions ongoing), and modify on-the-fly the ADC_JSEQ register (include JLEN) when ADC_CTRL3.JSTART is set (injected conversions ongoing). However, the new sequence configuration is effective depended on SEQUPMD:

- SEQUPMD=0 (default): on current sequence

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- SEQUPMD=1: on next sequence

See Figure 26-7 and Figure 26-9 for detail.

When SEQUPMD=0: if the length of new sequence is shorter than old sequence and current conversion is over the new length, the current sequence is early completed to start next sequence with new configuration (Figure 26-8).

Figure 26-7 Change sequence's length on-the-fly

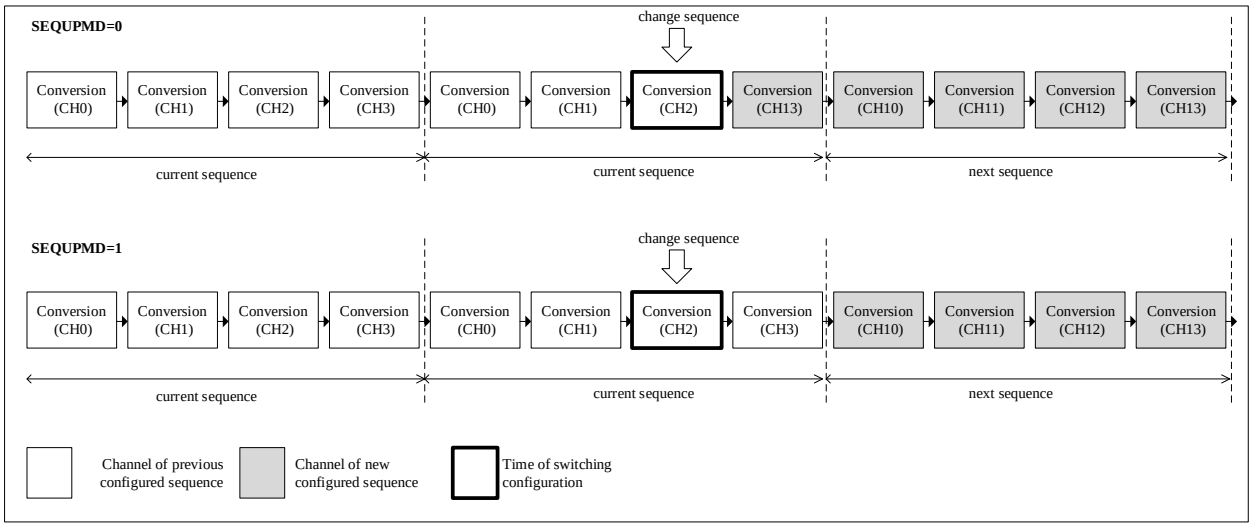

Figure 26-8 Change sequence's length on-the-fly (SEQUPMD=0)

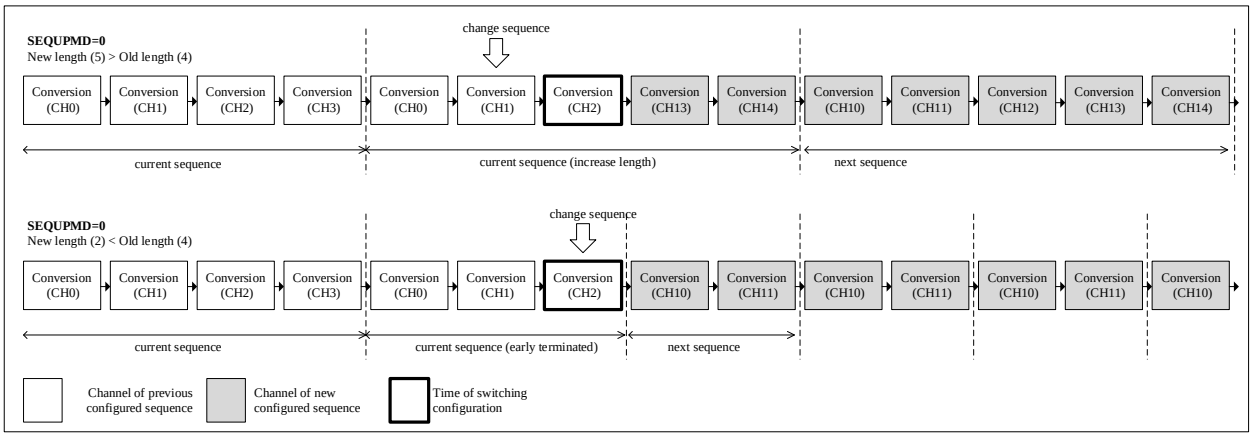

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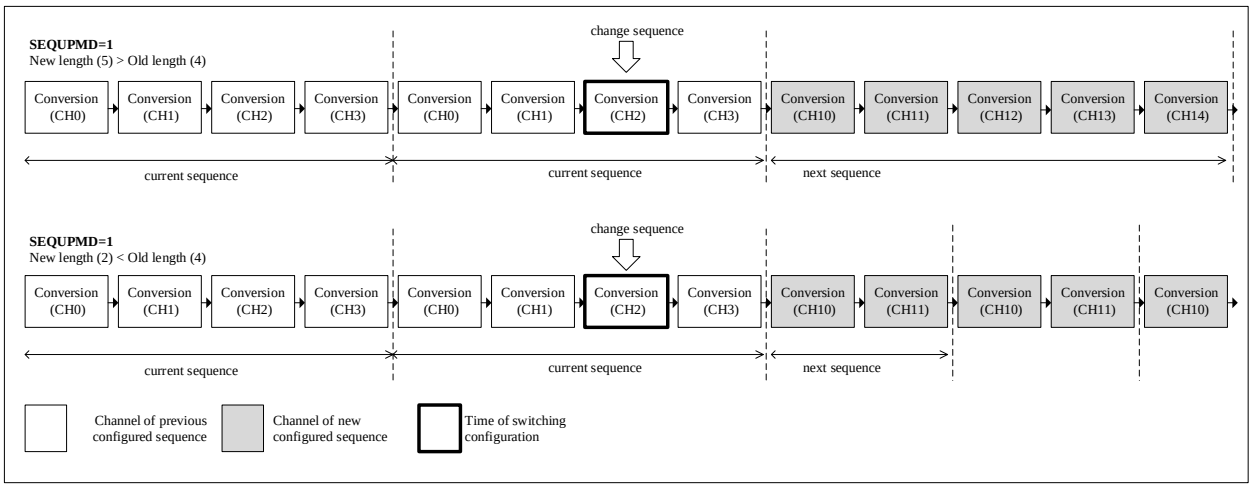
Figure 26-9 Change sequence's length on-the-fly (SEQUPMD=1)



Note:

1. *Time of switching the configuration in the figures here is hardware effect time, it will have some latency from software setting.*
2. *In order to prevent the channel from changing during sampling or conversion time, the channel is latched and masked until end of current conversion. The new configuration takes effect from next conversion.*
3. *Since it has a synchronizer from AHB clock to ADC kernel clocks for ADC_RSEQx/JSEQ register setting, it requires the minimum time between two consecutive write setting.*

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Figure 26-10 ADC1 channel connection

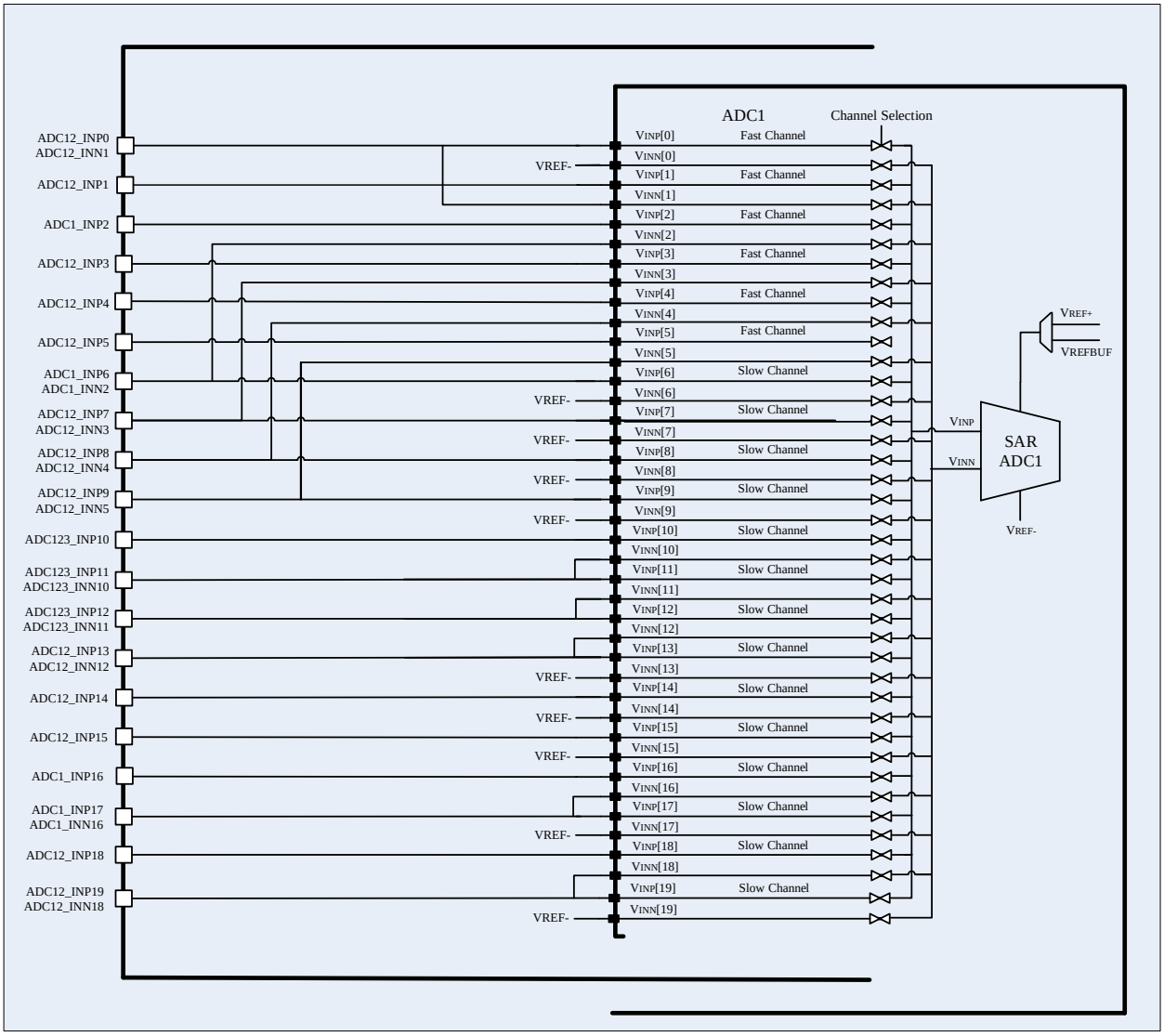

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Figure 26-11 ADC2 channel connection

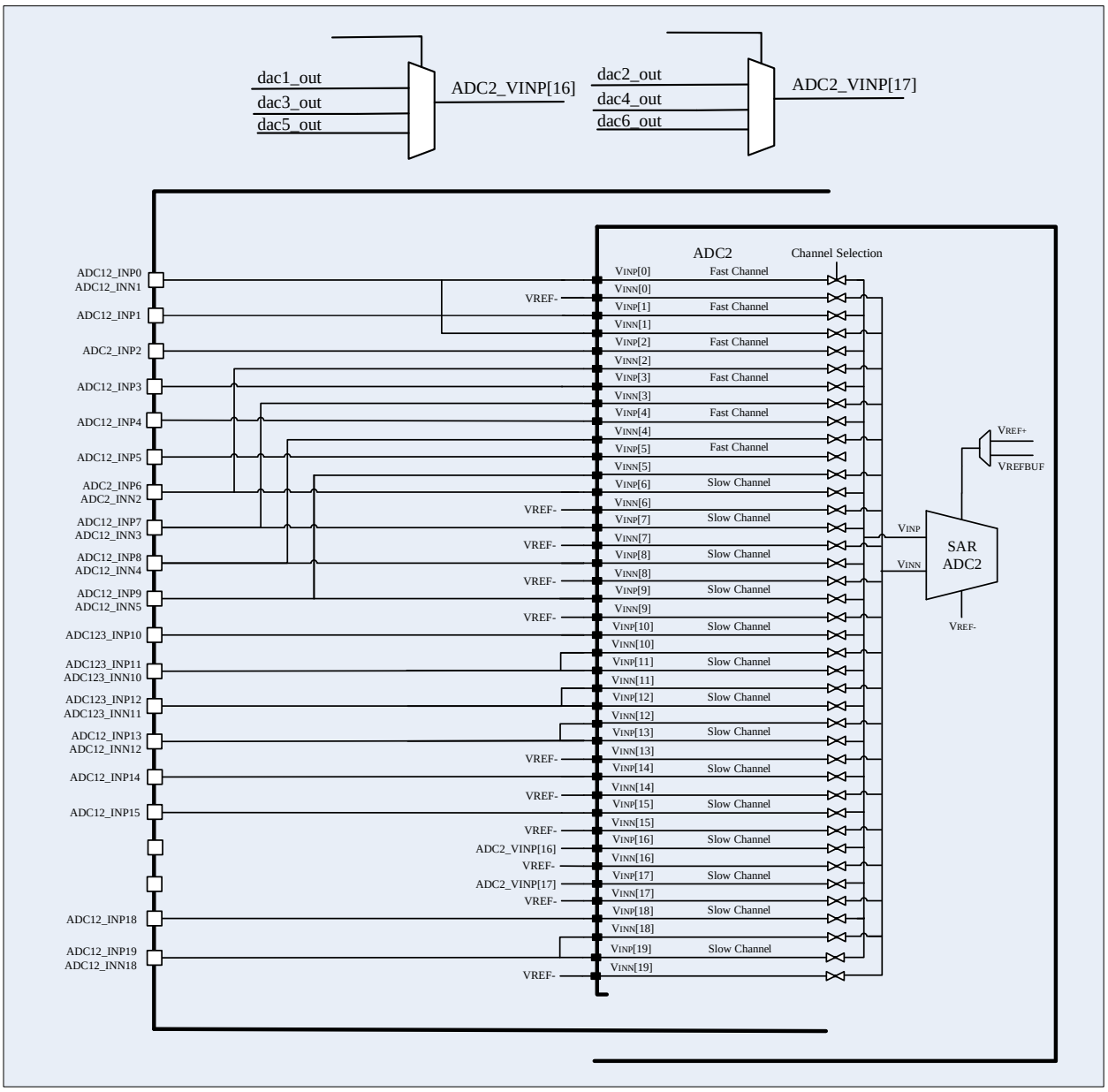

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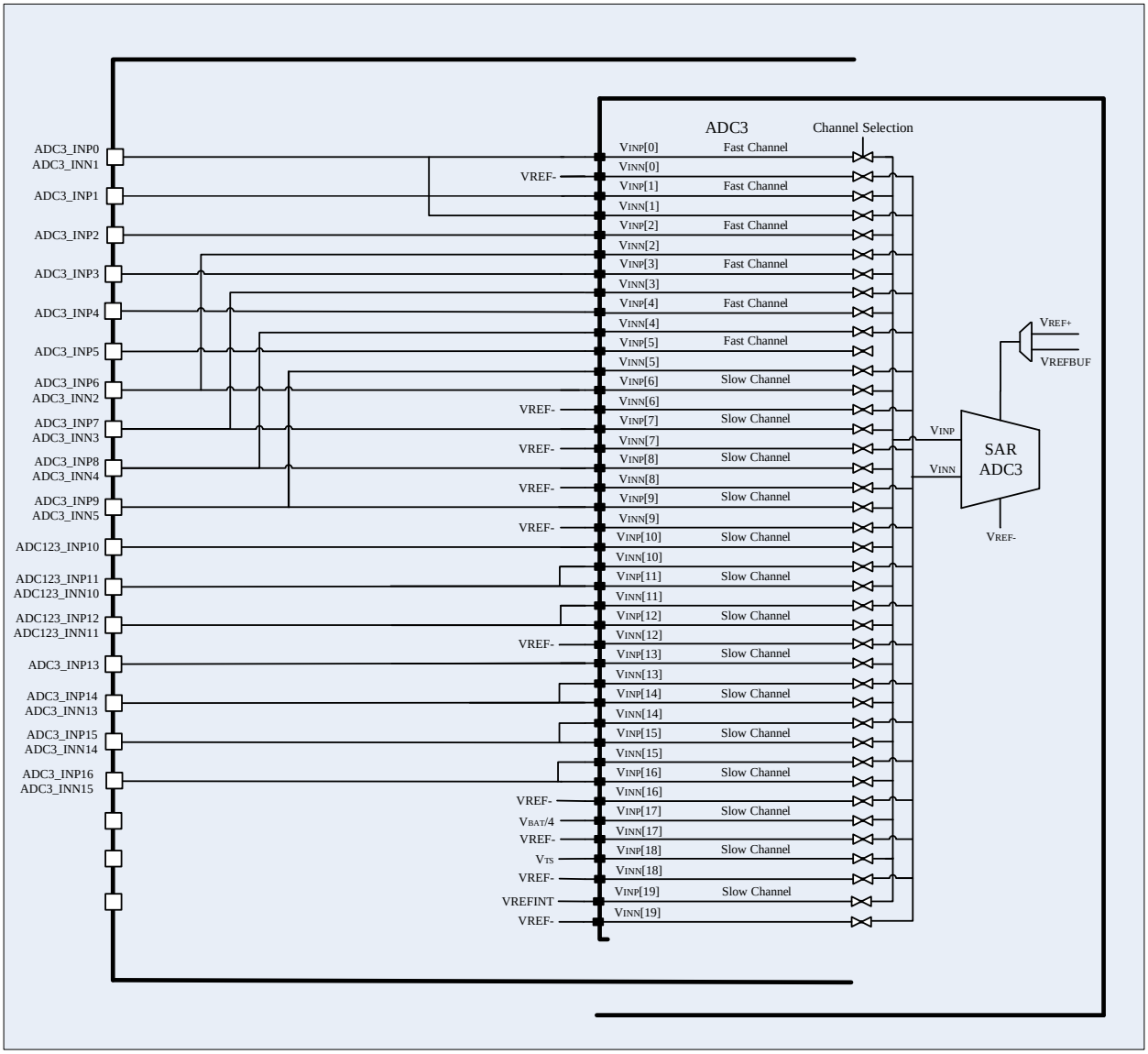
Figure 26-12 ADC3 channel connection



26.5.4 Trigger sources

A conversion or a sequence of conversions can be triggered either by software or by hardware (an external event, e.g. timer capture, input pins). When EXTPRSEL/EXTPJSEL=00, the software trigger is valid. When EXTPRSEL/EXTPJSEL ≠00, the hardware triggers are valid; they are enable by EXTRIG/JEXTRIG and selected by EXTRSEL/EXTJSEL as shown as below (total 32 external hardware triggers).

Table 26-2 ADC external hardware trigger selection

ADC trigger selection EXTRSEL[4:0] or	ADC1/2/3	
	Regular	Injected
0	atim1_cc1	atim1_cc1
1	atim1_cc2	atim1_cc2
2	atim1_cc3	atim1_cc3

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3	atim1_cc4	atim1_cc4
4	atim1_trgo	atim1_trgo
5	atim2_cc1	atim2_cc1
6	atim2_cc2	atim2_cc2
7	atim2_cc3	atim2_cc3
8	atim1_trgo2	atim1_trgo2
9	atim2_trgo	atim2_trgo
10	atim3_cc1	atim3_cc1
11	atim3_cc2	atim3_cc2
12	atim3_cc3	atim3_cc3
13	atim3_cc4	atim3_cc4
14	atim2_trgo2	atim2_trgo2
15	atim3_trgo	atim3_trgo
16	atim4_trgo2	atim4_trgo2
17	atim3_trgo2	atim3_trgo2
18	atim4_trgo	atim4_trgo
19	Gtimb1_trgo	Gtimb1_trgo
20	Gtimb2_trgo	Gtimb2_trgo
21	Gtimb3_trgo	Gtimb3_trgo
22	Gtima1_trgo	Gtima1_trgo
23	Gtimb1_cc2	Gtimb1_cc2
24	Gtimb2_cc4	Gtimb2_cc4
25	Gtimb3_cc2	Gtimb3_cc2
26	Gtima1_cc4	Gtima1_cc4
27	Shrtim1_adc_trg1	Shrtim1_adc_trg2
28	Shrtim1_adc_trg3	Shrtim1_adc_trg4
29	shrtim2_adc_trg1	Shrtim2_adc_trg2
30	shrtim2_adc_trg3	Shrtim2_adc_trg4
31	EXTI0~15	EXTI0~15

For hardware triggers, it can be configured as rising edge active or falling edge active, or both.

Table 26-3 provides the correspondence between the EXTPRSEL[1:0] and EXTPJSEL[1:0] values and the trigger polarity.

Table 26-3 ADC trigger polarity selection

EXTPRSEL[1:0] / EXTPJSEL[1:0]	**Trigger polarity**
00	Hardware Trigger detection disabled. Software Trigger detection enabled.
01	Hardware Trigger with detection on the rising edge. (*1) Software Trigger detection disabled.
10	Hardware Trigger with detection on the falling edge. (*1) Software Trigger detection disabled.
11	Hardware Trigger with detection on both the rising and falling edges. (*1)

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	Software Trigger detection disabled.

Note:

1. *The polarity of the hardware triggers cannot be changed on-the-fly*.

2. A *trigger is ignored in below scenarios:*

- *ADC_CTRL3.RSTART = 0 (regular trigger, or injected trigger when AUTOJC=1) or ADC_CTRL3.JSTART =0 (injected trigger)*
- *A regular trigger occurs when current regular conversion is ongoing*
- *An injected trigger occurs when current injected regular conversion is ongoing*

There is no status bit to notify a trigger is ignored.

26.5.5 Internal channel

There are 3 configurable register bit to enable or disable for Temperature Sensor, VBAT, and Internal refence voltage:

- TEMPEN of register ADC_CTRL2
- VBATMEN of register ADC_CTRL3
- VREFINTEN of register ADC_CTRL3

These bits are only available on ADC3.

26.5.6 ADC basic timing

Figure 26-13 shows the basic timing on regular channel.

rtrgo: actual regular trigger after multiplexer of triggers sources (include software trigger) and synchronizer

DLYVAL: when independent mode (MULTMODE=00000) and DLYSAMPEN=1, this value inserts the delay time to start conversion sequence. Otherwise, it is invalid and considered as 0 delay.

tSAMPx: sample time of each channel, set by ADC_SAMPTx registers, minimum = 1-cycle of ADC kernel clock

tCONV: 3-cycle

tsuch: channel set up time, minimum = 1.5-cycle of ADC kernel clock

thch: channel hold time, minimum = 1.5-cycle of ADC kernel clock

For RESSEL, it is set by RES bit (ADC_CTRL3 register) and not change during ADC_CTRL3.RSTART/ADC_CTRL3.JSTART=1.

For DIFFSEL, it is set by DIFSEL bit (ADC_DIFSEL register) and depended on channel. Thererefore, its minimum setup time and hold time is the same as channel select.

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Figure 26-13 ADC conversion basic timing on regular channel

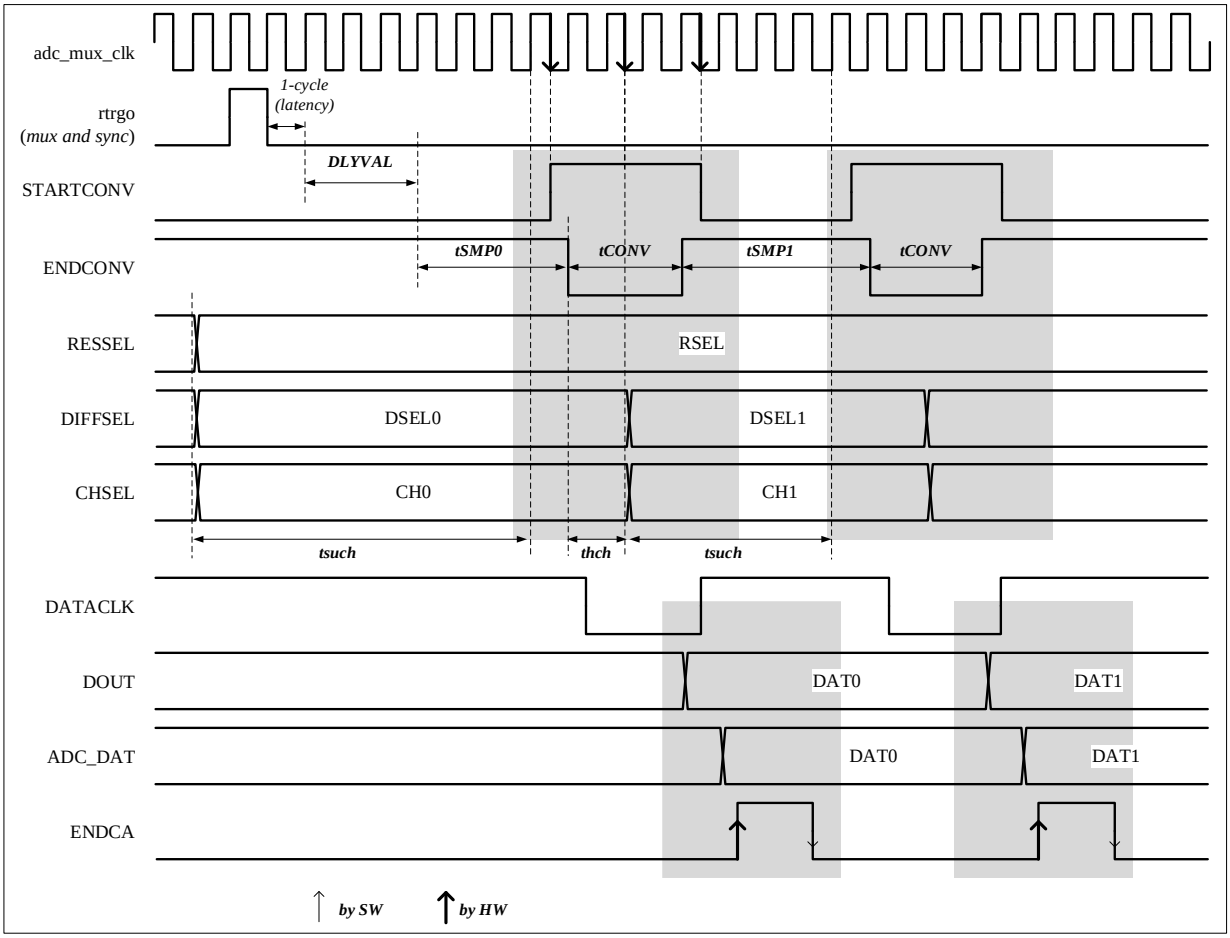

Figure 26-14 shows the basic timing on inject channel.

It is similar to regular conversion timing, however, since the injected conversion need a time to complete interrupting the regular conversion in general case, it inserts 5-cycle for that.

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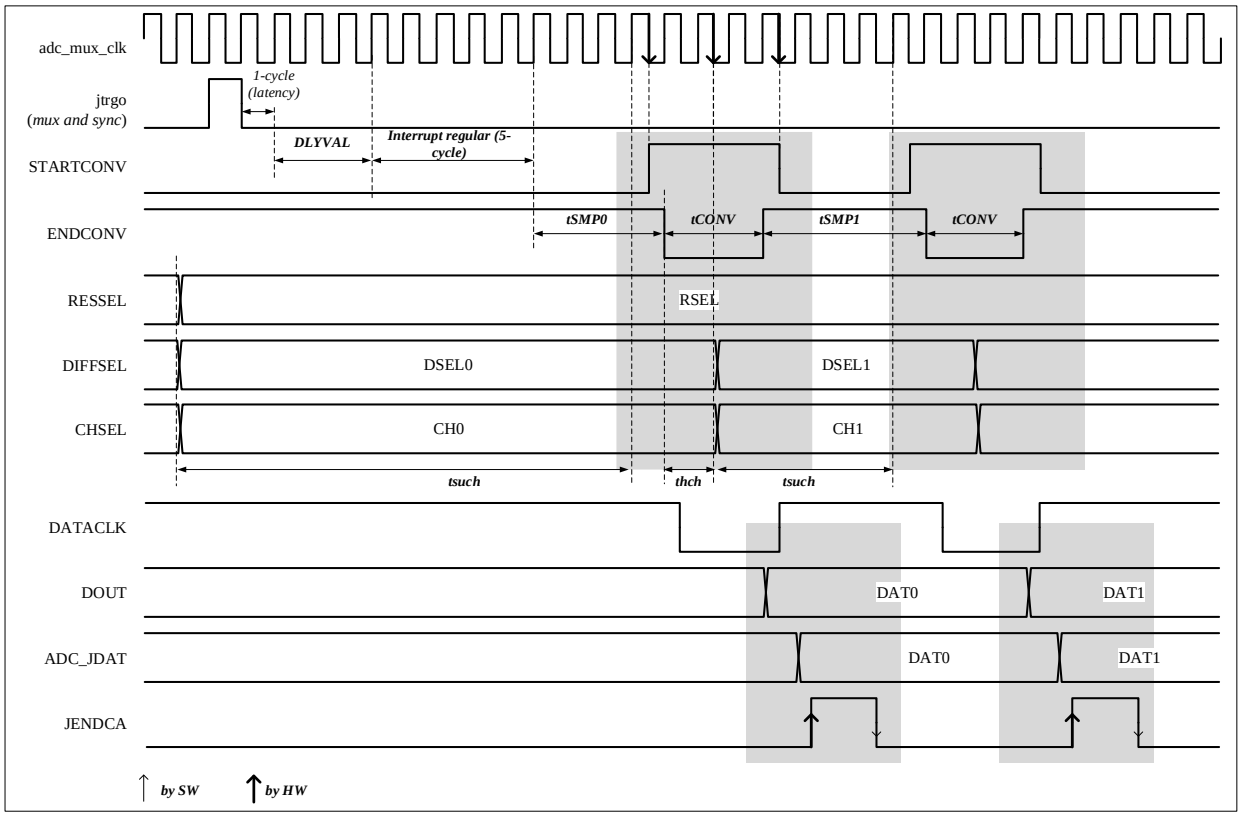
Figure 26-14 ADC conversion basic timing on injected channel



Note:The ADC conversion speed can be defined by sample time and conversion time by following formula:
ADC conversion speed (Mega samples per second-MSPS) = 1 / (Sample time + Conversion time) = 1 / (tSAMPx+3)

For example: ADC kernel clock max (20Mhz) = 50ns, SAMPx = 0 => tSAMPx = 1-cycle:

ADC conversion speed = 1 / ((1+3).50ns) = 5 MSPS

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Figure 26-15 shows the basic timing when an inject conversion interrupts the regular conversion sequence.

This case, the interrupted regular conversion is aborted: the conversion is performed until ENDCONV=H but the ADC_DAT not updated and ENDCA flag not asserted. It is resumed after the injected conversion completed.

Figure 26-15 Injected trigger interrupts regular conversion

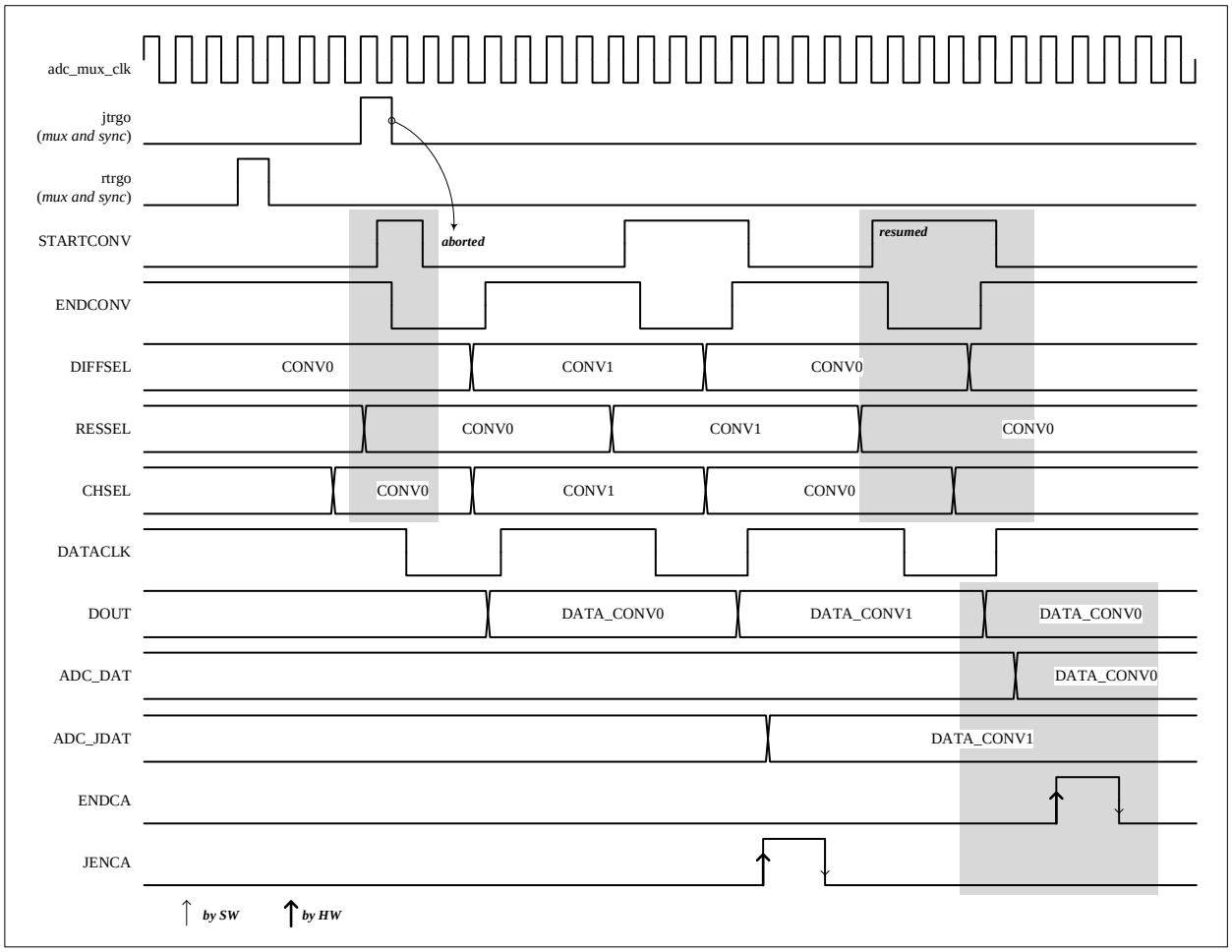

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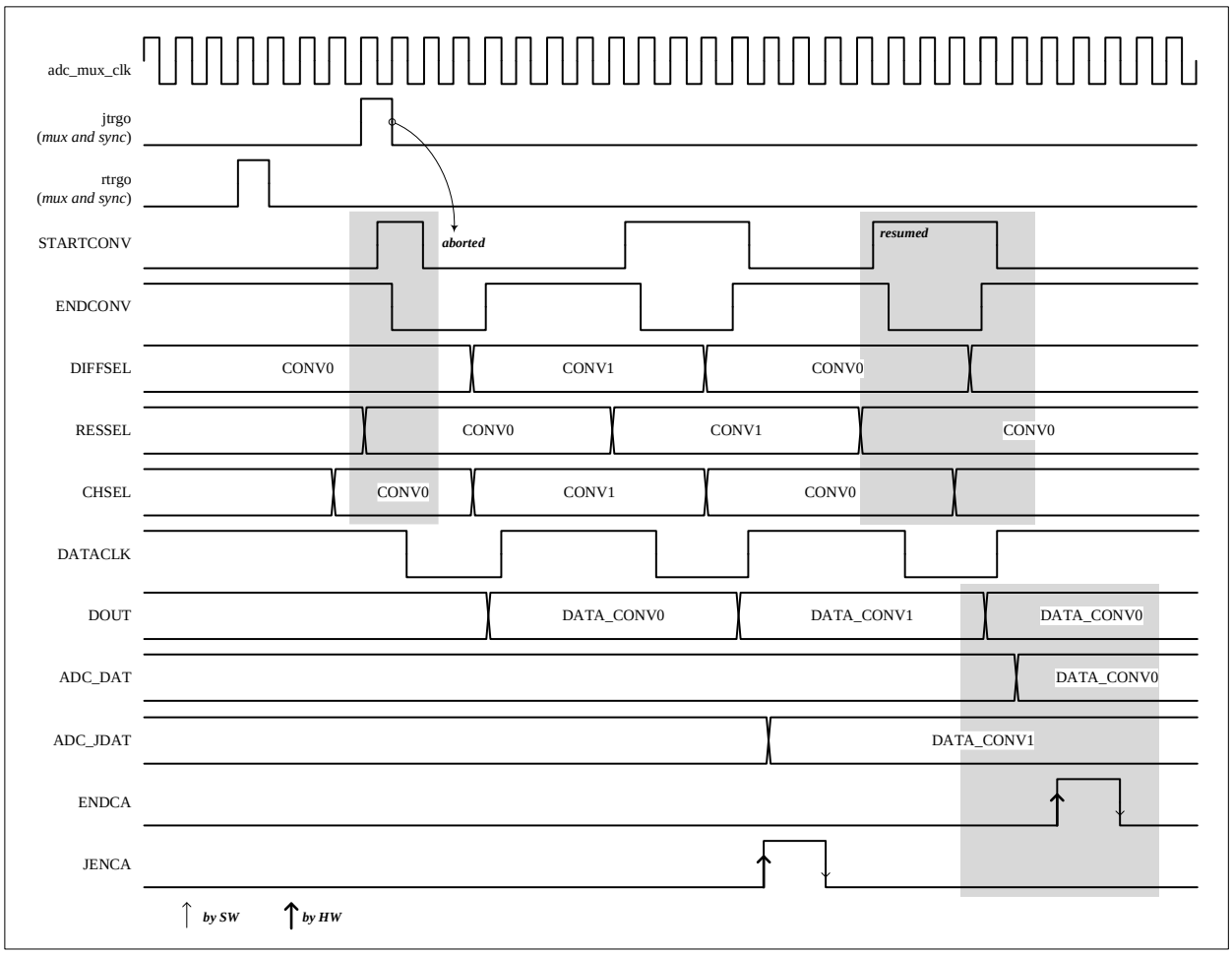
Figure 26-16 Injected trigger interrupts regular conversion



26.5.7 ADC conversion modes

Table 26-4 summarizes the conversion modes.

For detail of each mode, refer to sections 26.5.7.1-26.5.9

Table 26-4 Summary of conversion modes

Conversion mode	Configuration	Remark
Single conversion	SCANMD(=0), ADC_CTRL2.CTU(=0)	ADC_CTRL2.CTU is valid only for regular
Scan conversion	SCANMD(=1), LEN, JLEN	
Continuous conversion	ADC_CTRL2.CTU(=1)	Only regular
Discontinuous conversion	DREGCH, DCTU (regular) DJCH (injected)	Injected: DCTU is considered as 1
Auto-injection	AUTOJC	
Oversample	OSRE, OSJE, OSRMD, OSRTRIG, OSR, OSS, OSAWD	

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26.5.7.1 Single conversion

In Single conversion mode, the ADC does one conversion. This mode is started with the CTU=0 and SCANMD =0 by either:

- Write 1 to SWSTRRCH bit in the ADC_CTRL2 register (for a regular channel)
- Write 1 to SWSTRJCH bit (for an injected channel)
- External hardware trigger (for a regular or injected channel)

In this mode, LEN and JLEN is ignored and considered as 0 regardless of their setting.

For regular conversion, the channel is set by SEQ1 bit of ADC_RSEQ3 register. For injected conversion, the channel is set by JSEQ4 bit of ADC_JSEQ register.

Once the conversion of the selected channel is complete:

- If a regular channel was converted:
  - The converted data are stored into the 16-bit ADC_DAT register
  - The ENDCA (end of conversion) flag is set
  - An interrupt is generated if the ENDCAIEN bit is set
- If an injected channel was converted:
  - The converted data are stored into the 16-bit ADC_JDAT1 register (ADC_JDAT2-4 are not used)
  - The JENDCA (end of conversion injected) flag is set
  - An interrupt is generated if the JENDCAIEN bit is set

Then the ADC stops.

During the conversion, it can be terminated by SWRSTOP/SWJSTOP command.

Figure 26-17 shows an example of single conversion flow on regular channel.

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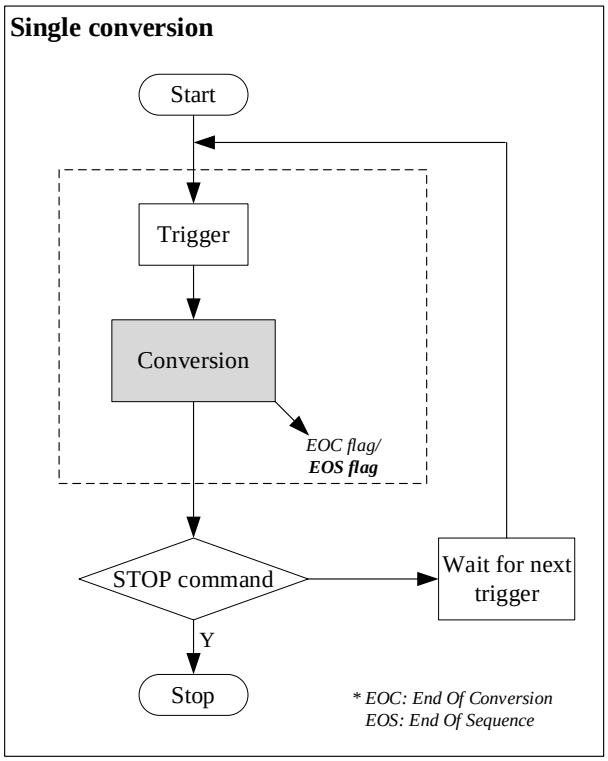
Figure 26-17 Single conversion



26.5.7.2 Scan conversion

This mode is used to scan a group of channels.

The Scan mode is selected by setting the ADC_CTRL1.SCANMD bit. Once this bit has been set, the ADC scans all the channels selected in the ADC_RSEQx registers (for regular channels) or in the ADC_JSEQ register (for injected channels). The number of channels is configured in LEN bits (for regular channels), or JLEN bits (for injected channels). A single conversion is performed for each channel of the group. After each end of conversion, the next channel in the group is converted automatically until last channel.

The ENDC bit is set in the ADC_STS register at the end of each regular group sequence. The JENDC bit is set in the ADC_STS register at the end of each injected group sequence.

The data converted from an regular channel are stored into the ADC_DAT register. The data converted from an injected channel are stored into the ADC_JDATx registers, x=1,2,3,4 according to the order of conversion.

With regular conversion, the channel are converted in the order: SEQ1 → SEQ2 → SEQ3 → … → SEQn, n=LEN+1.

With injected conversion:

- When JLEN[1:0]=3 (4 injected conversions in the sequencer), the ADC converts the channels in the following order: JSEQ1[4:0], JSEQ2[4:0], JSEQ3[4:0], and JSEQ4[4:0].
- When JLEN=2 (3 injected conversions in the sequencer), the ADC converts the channels in the following order: JSEQ2[4:0], JSEQ3[4:0], and JSEQ4[4:0].
- When JLEN=1 (2 injected conversions in the sequencer), the ADC converts the channels in starting from JSEQ3[4:0], and then JSEQ4[4:0].

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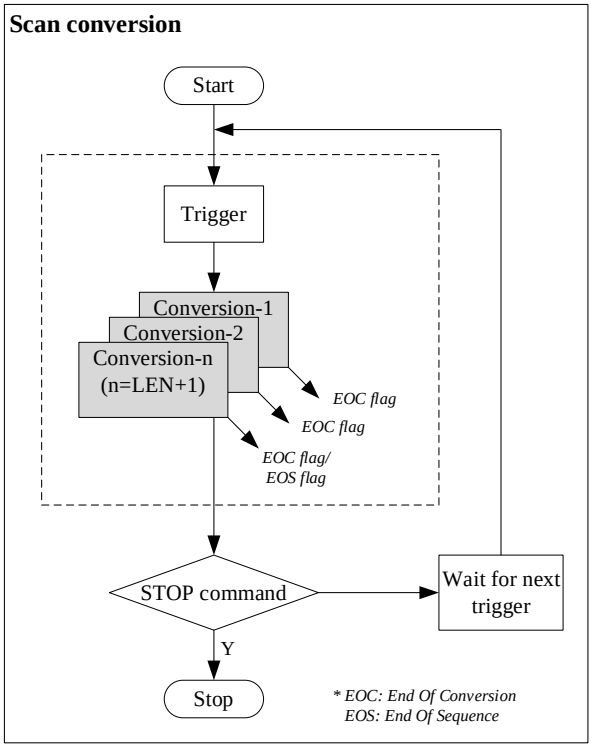
– When JLEN=0 (1 injected conversion in the sequencer), the ADC converts only JSEQ4[4:0]channel.

The figure below shows an example of scan conversion flow on regular channel.

Figure 26-18 Scan conversion



26.5.7.3 Continuous conversion

In continuous conversion mode, the ADC starts a new conversion as soon as it finishes one. When SCANMD=1, it does not stop at the last selected channel in the group but continues again from the first selected channel.This mode is started with the ADC_CTRL2.CTU bit at 1 either by external hardware trigger or by setting the SWSTRRCH bit in the ADC_CTRL2 register (for regular channels only).

After each conversion:

- If a regular group of channels was converted:
  - The last converted data are stored into the 16-bit ADC_DAT register
  - The EOC (end of conversion) flag is set
  - An interrupt is generated if the EOC interrupt enable bit is set

During the conversion, it can be terminated by SWRSTOP (SWJSTOP is not valid even if AUTOJC=1) command.

Note: Injected channels cannot be converted continuously. The only exception is when an injected channel is configured to be converted automatically after regular channels in continuous mode (using AUTOJC bit).

Figure 26-19 shows an example of continuous conversion flow on regular channel.

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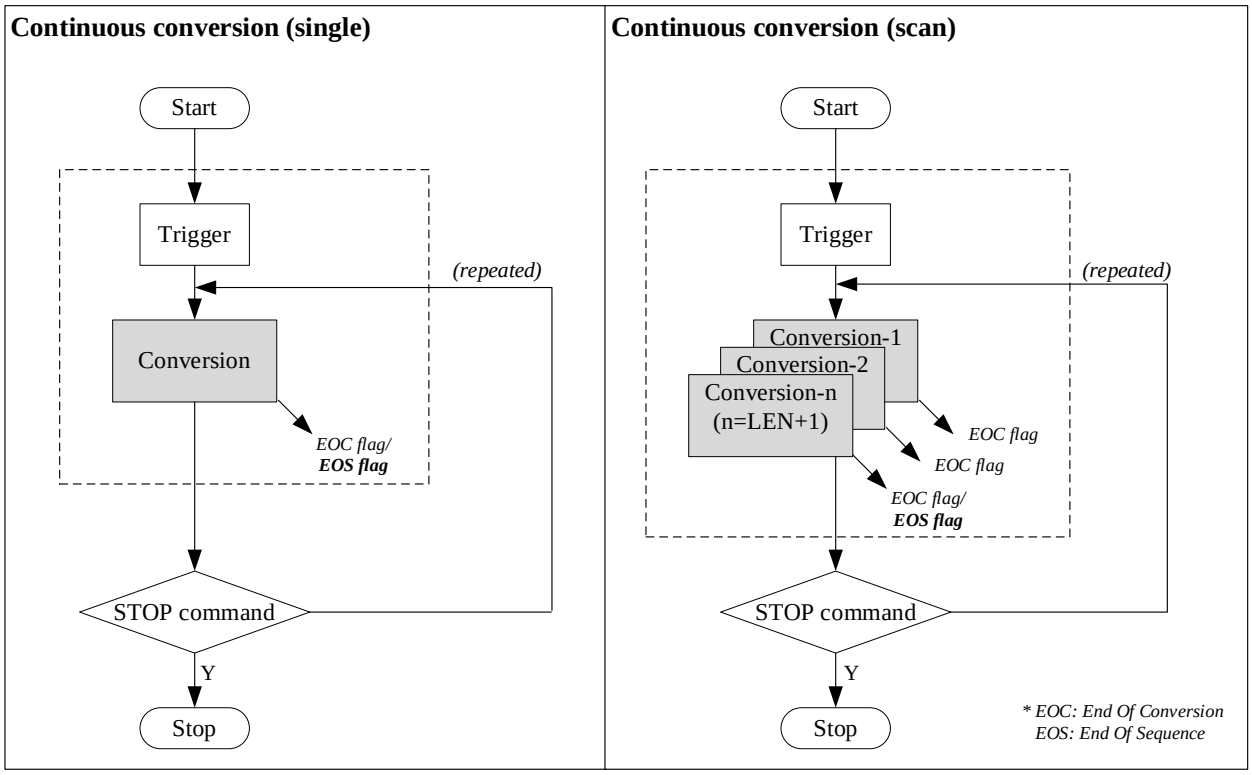
Figure 26-19 Continuous conversion



26.5.7.4 Discontinuous conversion

Figure 26-20 shows an example of scan conversion flow on regular channel.

This mode can be set separately for regular (section 26.5.7.5) and injected conversion (section 26.5.7.6).

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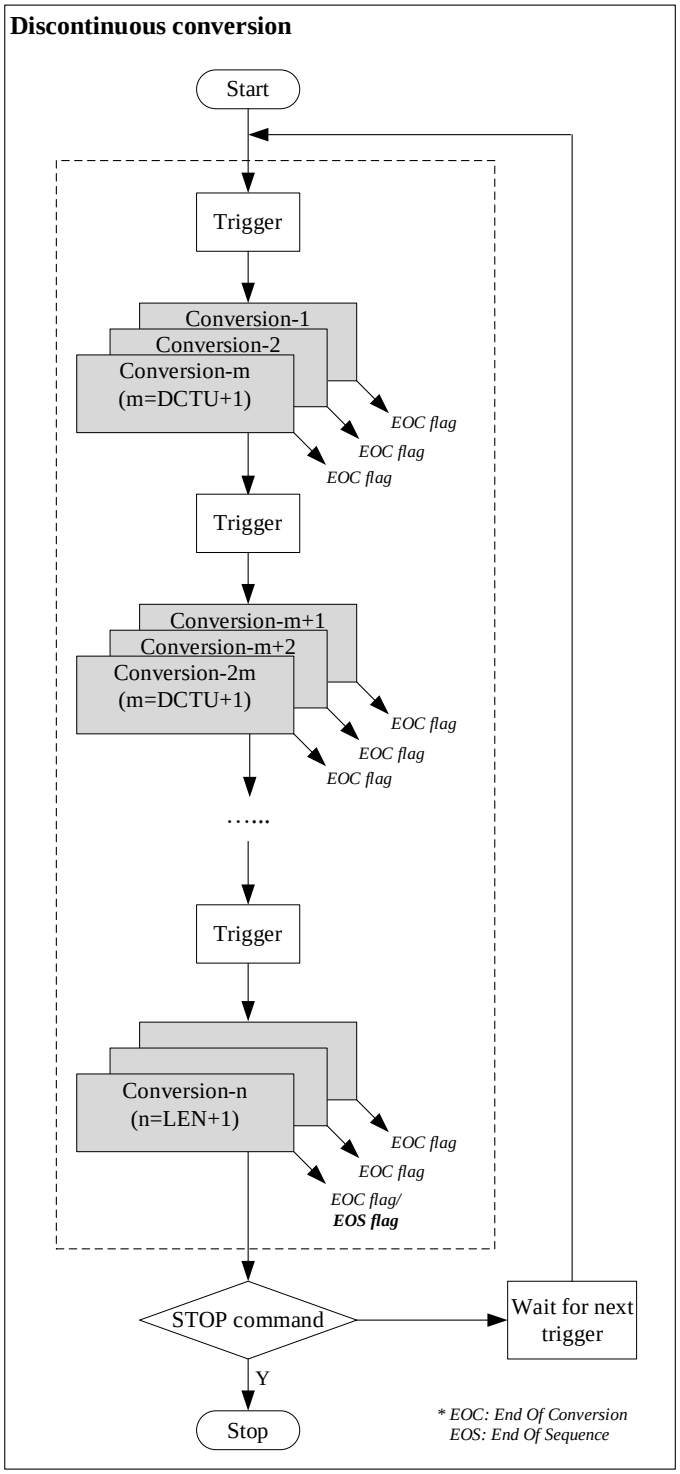
Figure 26-20 Discontinuous conversion



26.5.7.5 Regular group

This mode is enabled by setting the DREGCH bit in the ADC_CTRL1 register. It is used to convert a short sequence (subgroup) of n conversions (n ≤ 8) that is part of the sequence of conversions selected in the ADC_RSEQy registers. The value of n is specified by writing to the DCTU[2:0] bits in the ADC_CTRL1 register.

When an external trigger occurs, it starts the next n conversions selected in the ADC_RSEQy registers until all the

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conversions in the sequence are done. The total sequence length is defined by the LEN[4:0] bits in the ADC_RSEQ1 register.

Example:

- DREGCH = 1, n = 3, channels to be converted = 1, 2, 3, 6, 7, 8, 9, 10, 11
  - 1st trigger: channels converted are 1, 2, 3 (an ENDCA event is generated at each conversion).
  - 2nd trigger: channels converted are 6, 7, 8 (an ENDCA event is generated at each conversion).
  - 3rd trigger: channels converted are 9, 10, 11 (an ENDCA event is generated at each conversion) and an ENDC event is generated after the conversion of channel 11.
  - 4th trigger: channels converted are 1, 2, 3 (an ENDCA event is generated at each conversion).
  - ...
- DREGCH = 0, channels to be converted = 1, 2, 3, 6, 7, 8, 9, 10,11
  - 1st trigger: the complete sequence is converted: channel 1, then 2, 3, 6, 7, 8, 9, 10 and 11. Each conversion generates an ENDCA event and the last one also generates an ENDC event.
  - All the next trigger events relaunch the complete sequence.

Note: When a regular group is converted in discontinuous mode, no rollover occurs (the last subgroup of the sequence can have less than n conversions).

When all subgroups are converted, the next trigger starts the conversion of the first subgroup. In the example above, the 4th trigger reconverts the channels 1, 2 and 3 in the1st subgroup.

It is not possible to have both discontinuous mode and continuous mode enabled. In this case (if DREGCH = 1, CTU = 1), the ADC behaves as if continuous mode was disabled.

26.5.7.6 Injected group

This mode is enabled by setting the DJCH bit in the ADC_CTRL1 register. It converts the sequence selected in the ADC_JSEQ register, channel by channel, after an external injected trigger event. This is equivalent to discontinuous mode for regular channels where ‘n’ is fixed to 1.

When an external trigger occurs, it starts the next channel conversions selected in the ADC_JSEQ registers until all the conversions in the sequence are done. The total sequence length is defined by the JLEN[1:0] bits in the ADC_JSEQ register.

Example:

- DJCH = 1, channels to be converted = 1, 2, 3
  - 1st trigger: channel 1 converted (a JENDCA event is generated)
  - 2nd trigger: channel 2 converted (a JENDCA event is generated)
  - 3rd trigger: channel 3 converted and a JENDCA event + a JENDC event are generated
  - ...

Note: When all injected channels have been converted, the next trigger starts the conversion of the first injected

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channel. In the example above, the 4th trigger reconverts the 1st injected channel 1.

It is not possible to use both auto-injected mode and discontinuous mode simultaneously: the bits DREGCH and DJCH must be kept cleared by software when AUTOJC is set.

26.5.8 Auto-injection conversion

If the AUTOJC bit is set, then the channels in the injected group are automatically converted after the regular group of channels. This can be used to convert a sequence of up to 20 conversions programmed in the ADC_RSEQx and ADC_JSEQ registers.

In this mode, external trigger on injected channels must be disabled.

If the ADC_CTRL2.CTU bit is also set in addition to the AUTOJC bit, regular channels followed by injected channels are continuously converted.

Note: It is not possible to use both the auto-injected and discontinuous modes simultaneously.

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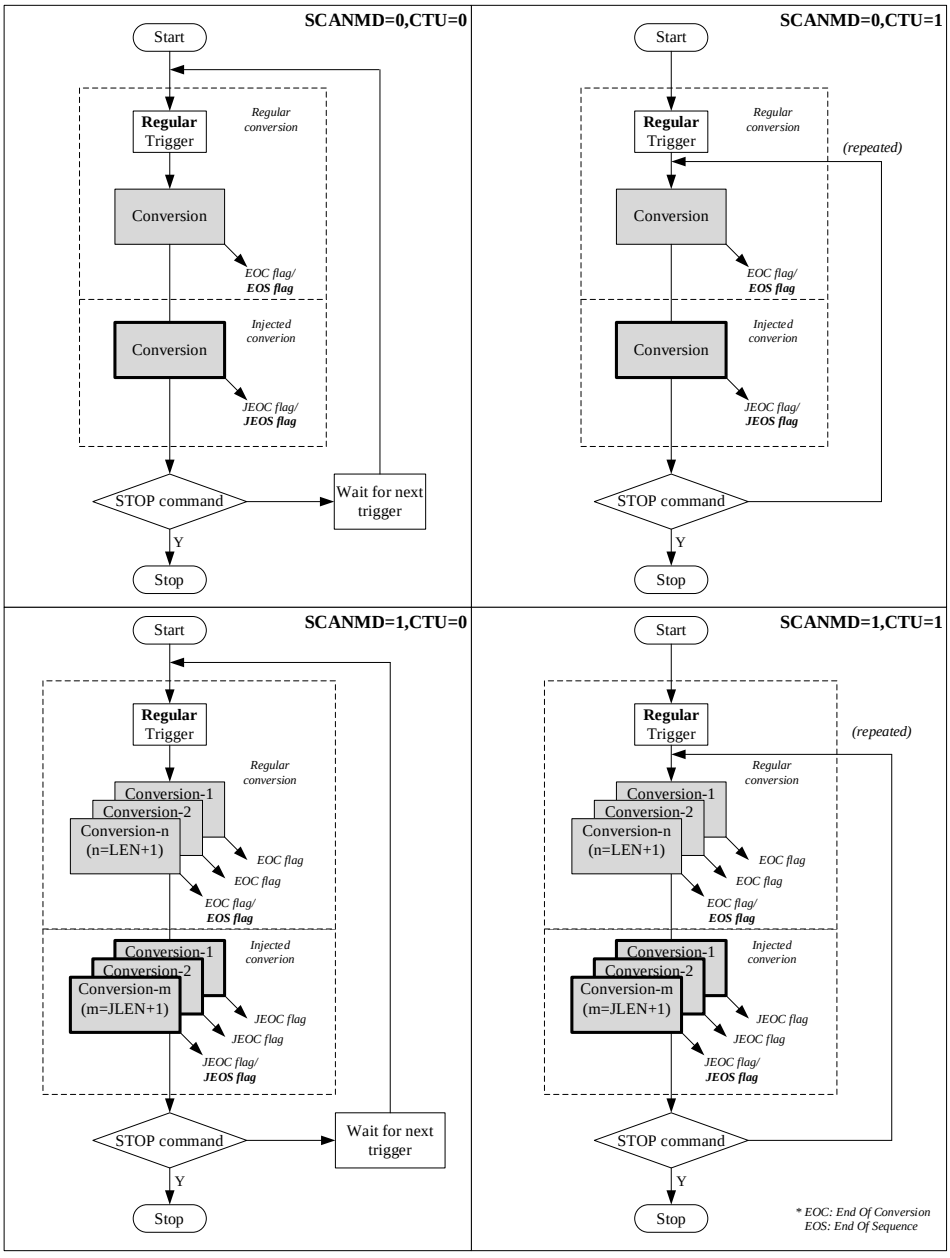
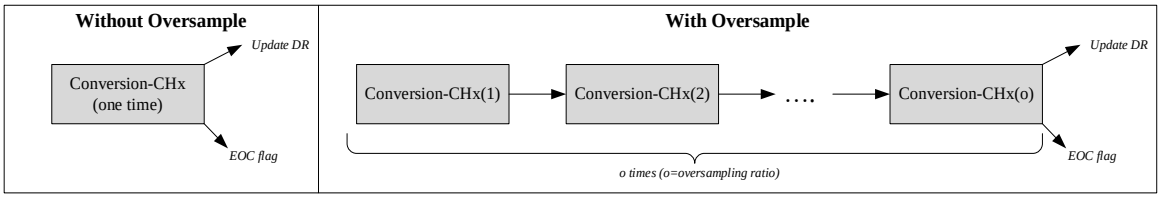
Figure 26-21 Auto-injection conversion



26.5.9 Oversample

When oversampling conversion, each channel is converted repeatedly o times (o=oversampling ratio).

Figure 26-22 Oversample



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The conversion data is accumulated each conversion time. After last time, it averages the conversion data for that channel by below formula:

$$Result = \frac{1}{M} \times \sum_{n=0}^{N-1} Conversion\ (t_n)$$

(N = oversample ratio, setting with OSR bits. M = division coefficient, setting with OSS bits)

The summation unit can yield a result up to 22 bits (1024x 12-bit results), which is first shifted right. It is then rounded to the nearest value using the least significant bits left apart by the shifting, and truncated to the 16 least significant bits, before being finally transferred into the ADC_DAT and ADC_JDATx data register.

This result is stored to ADC_DAT/JDATy as conversion result for that channel. The ENDCA (for regular) or JENDCA (for injected) is asserted only after last time of oversampling.

Note: If the intermediary result after the shifting exceeds 16-bit, the result is truncated as is, without saturation. If this case occurs, the status bit ROSOVF (regular) or JOSOVF (injected) is asserted.

The basic purpose of oversample is to increase the accuracy of conversion result. Oversampler is implemented in this controller is to off-load CPU for this function.

All basic conversion modes can be used with oversampling:

- Single mode.
- Scan mode.
- Continuous mode.
- Discontinuous mode.
- Auto-injection conversion.

The oversample conversion can be applied for both regular and injected channel. Below cases are supported:

- Oversample with regular only (OSRE=1, OSJE=0). A normal injected (non-oversample) can be run, and can interrupt the regular oversample.
- Oversample with injected only (OSRE=0, OSJE=1). A normal regular (non-oversample) can be run, and can be interrupted by the injected oversample.
- Oversample with both regular and injected (OSRE=1, OSJE=1). The injected oversample can interrupt the regular oversample. This case OSRMD is ignored, the behavior is as OSRMD=1, resumed mode.

For regular oversample, there are some special control modes:

1. Continued/Resumed mode (OSRMD): To control when a regular oversample is interrupted by an injected conversion:
   - Continued mode(OSRMD=0): the accumulation restarts from the last valid data (prior to the conversion abort request due to the injected trigger).
   - Resumed mode(OSRMD=1): the accumulation restarts from 0 (previous conversion results are ignored)
2. Triggered mode (OSRTRIG): To allow user decide the frequency of oversampling, instead of only depended on

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conversion time itself.

- OSRTRIG=0: next conversion time of oversampling on specific channel can be automatically started
- OSRTRIG=1: next conversion time of oversampling on specific channel needs a trigger to start. DREGCH is ignored this case and considered as 1. This mode operates as if a special discontinuous mode with DCTU=0.

The analog watchdog functionality is maintained (AWDSGL and AWDEN bits), with the following difference:

- The RES bits are ignored, comparison is always done using the full 12-bit values HT[11:0] and LT[11:0]
- The comparison is performed on:
- the most significant 12-bit of the 16-bit oversampled results ADC_DAT[15:4] if OSAWD=0 (default).
- the least significant 12-bit of the 16-bit oversampled results ADC_DAT[11:0] if OSAWD=1.

Note: The alignment mode is not available when working with oversampled data. The ALIG bit in ADC_CFGR1 is ignored and the data are always provided right-aligned.

Offset correction is not supported in oversampling mode. When OSRE and/or OSJE bit is set, the value of the OFFSCHyEN bit in ADC_OFFSETy register is ignored (considered as reset).

It is possible to have oversampling enabled when working in dual or triple ADC configuration, for the injected simultaneous mode and regular simultaneous mode. In this case, the two ADCs (dual) or three ADCs (triple) must be programmed with the very same settings (including oversampling).

All other dual/triple ADC modes are not supported when either regular or injected oversampling is enabled (OSRE = 1 or OSJE = 1).

Table 26-5 Summary of oversample modes

Regular oversample enable OSRE	Injected oversample enable OSJE	Regular oversample mode OSRMD	Triggered regular mode OSRTRIG	Description
1	0	0	0	Regular continued mode
1	0	0	1	NOT supported
1	0	1	0	Regular resumed mode
1	0	1	1	Triggered regular resumed mode
1	1	0	x	NOT supported
1	1	1	0	Regular resumed and injected mode
1	1	1	1	NOT supported
0	1	x	x	Injected oversample

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Figure 26-23 Oversample conversion (CTU=0)

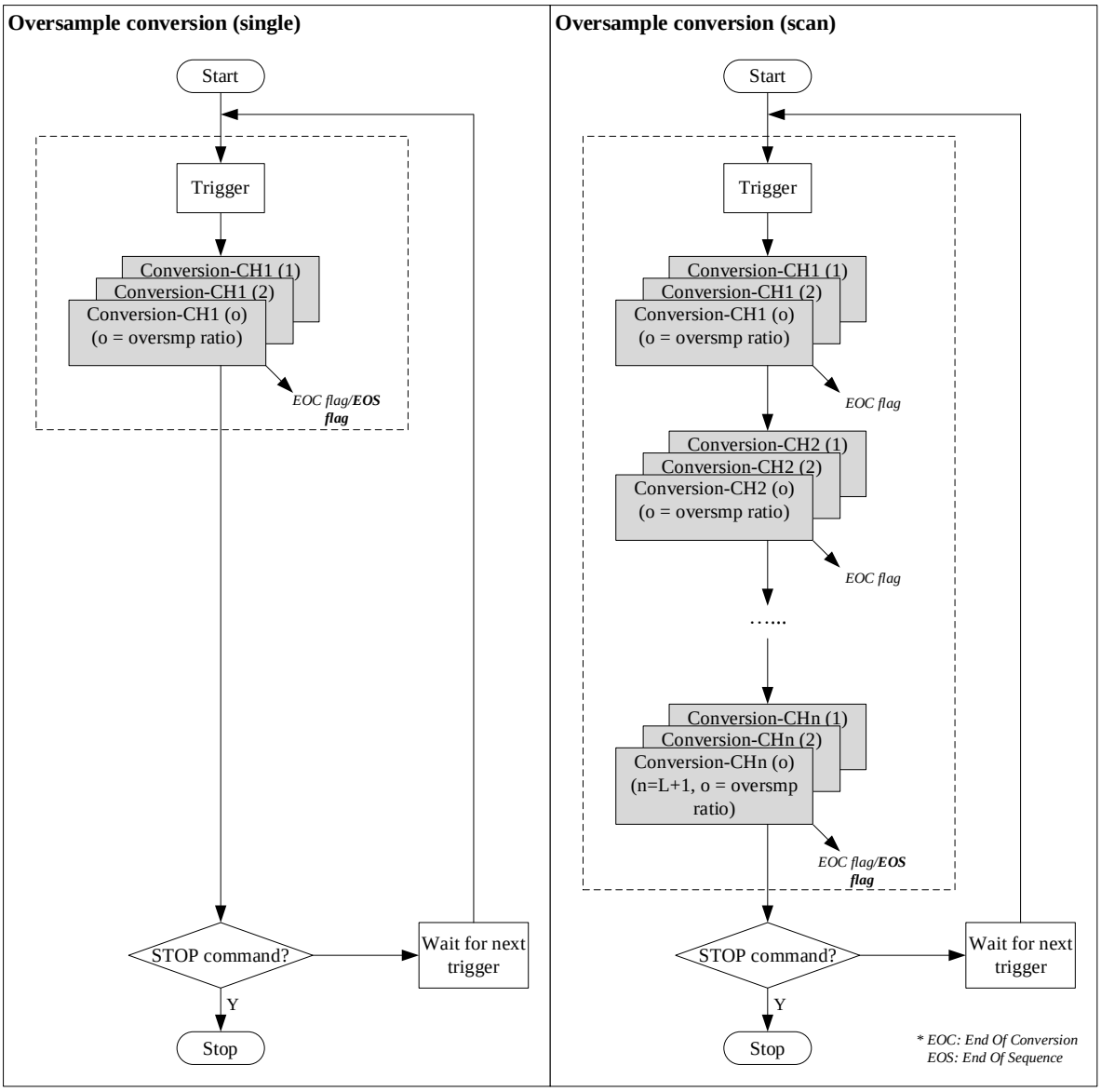

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Figure 26-24 Oversample conversion (CTU=1)

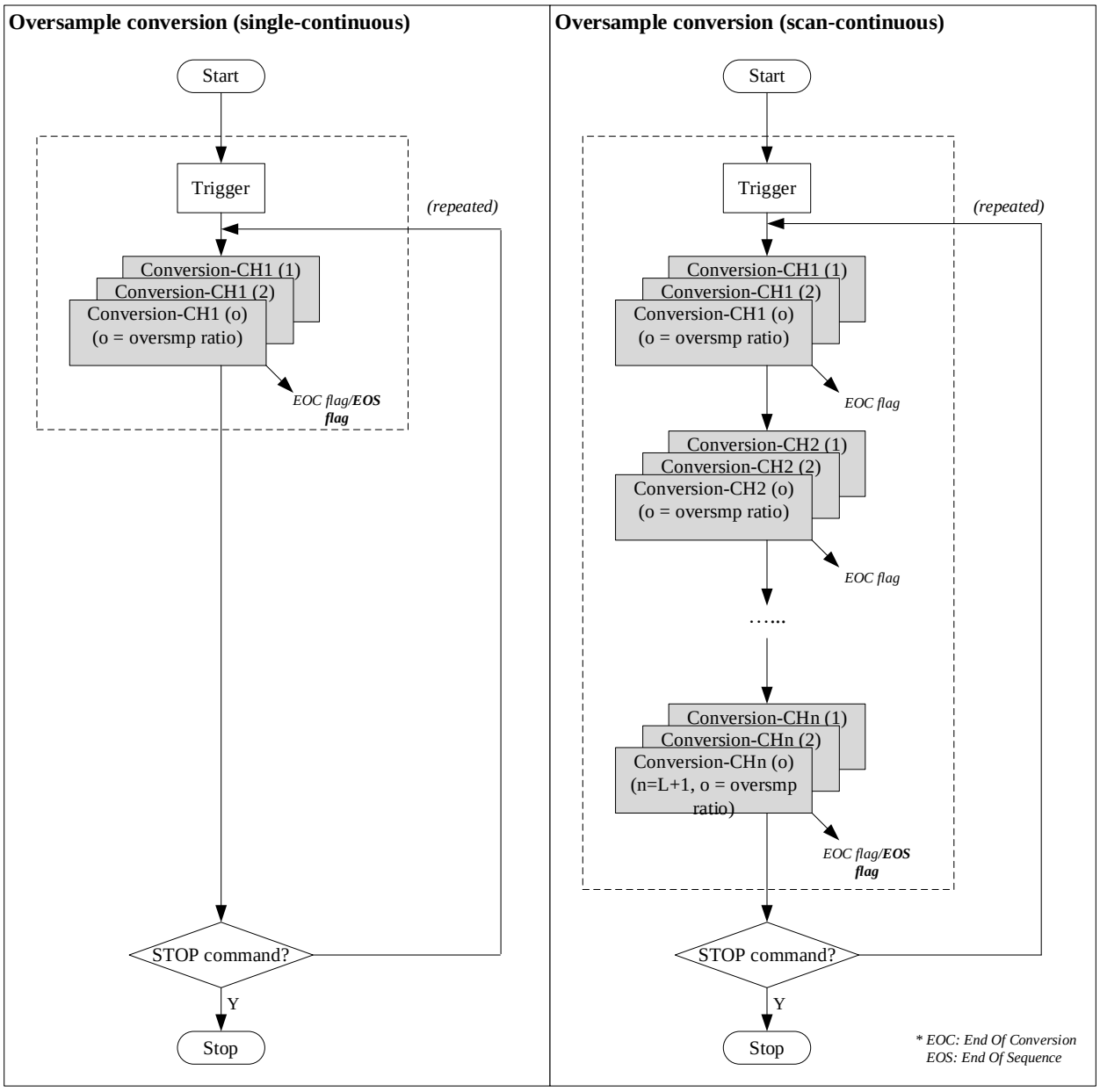

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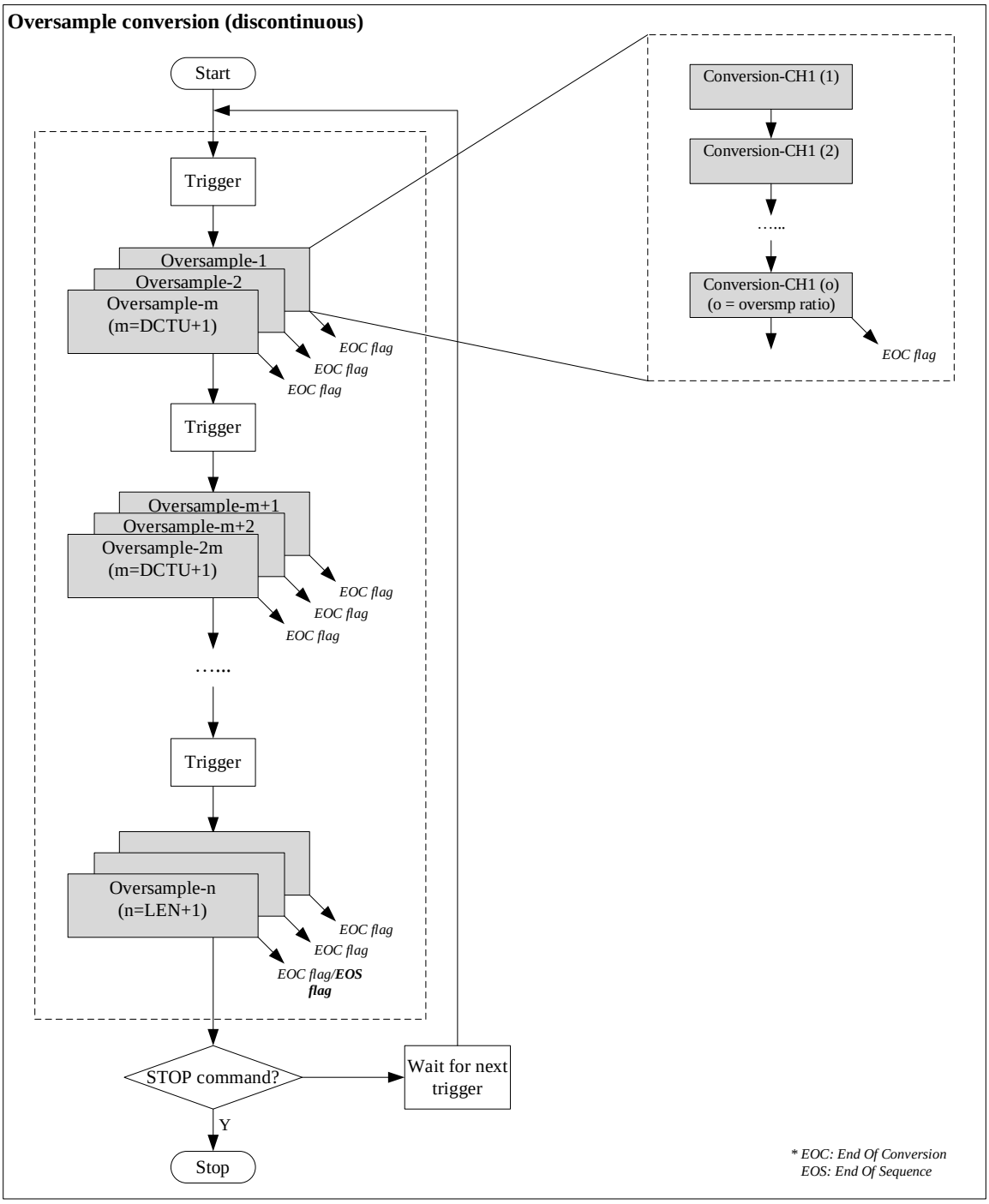
Figure 26-25 Oversample conversion (Discontinuous)



26.5.10 Mode combination

Table 26-6 Conversion mode combination

	Single conversion	Scan conversion	Continuous conversion	Dis-continuous conversion	Auto-injection	Oversample

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Single conversion		×	○	×	×	○
Scan conversion			○	○	○	○
Continuous conversion				×	○	○
Discontinuous conversion					○	○
Auto-injection						○
Oversample						

×: Not allowed, ○: Allowed

26.5.11 ADC operation modes

Table 26-7 ADC operation modes

Operation mode		MULTMODE	Note
Independent		00000	ADC1,2,3 work independenly
Dual ADC	Combined regular simultaneous + injected simultaneous	00001	ADC1,2 work together ADC3 independent
	Combined regular simultaneous + injected alternate trigger	00010	
	Combined regular interleaved + injected simultaneous	00011	
	Injected simultaneous only	00101	
	Regular simultaneous only * *Independent injected is allowed*	00110	
	Regular interleaved only * *Independent injected is allowed*	00111	
	Injected alternate trigger only	01001	
Triple ADC	Combined regular simultaneous + injected simultaneous	10001	ADC1,2,3 work together
	Combined regular simultaneous + injected alternate trigger	10010	
	Combined regular interleaved + injected simultaneous	10011	
	Injected simultaneous only	10101	
	Regular simultaneous only	10110	

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	* *Independent injected is allowed*		
	Regular interleaved only * *Independent injected is allowed*	10111	
	Injected alternate trigger only	11001	

***[Note]**: Only MULTMODE register bits on ADC1 (master) is valid to set operation mode. The MULTMODE register bits on ADC2, ADC3 are ignored.*

26.5.12 Independent mode

This mode is selected by programming bits MULTMODE[4:0] = 00000.

In this mode, each ADC can start conversion independently with other ADCs.

All configuration can be set individually for the ADC.

All conversion modes described in section 26.5.7 ADC conversion modes can be applied for the ADC.

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26.5.13 Dual ADC mode

In dual ADC mode the start of conversion is triggered alternately or simultaneously by the ADC1 master to the ADC2 slave depending on the mode selected by the bits MULTMODE[4:0] in the ADC_CTRL1 register. ADC3 can operate in independent mode.

Four possible modes are implemented:

- Injected simultaneous mode
- Regular simultaneous mode
- Interleaved mode
- Alternate trigger mode

It is also possible to use these modes combined in the following ways:

- Injected simultaneous mode + Regular simultaneous mode
- Regular simultaneous mode + Alternate trigger mode
- Injected simultaneous mode + Interleaved mode

In dual ADC mode, the following bits are only valid to set on master ADC (ADC1):

- SCANMD
- CTU
- DREGCH, DCTU, DJCH
- AUTOJC
- EXTPRSEL, EXTPJSEL
- DMNGT
- DMAMD
- MDSMU
- EN (applied only when DMNGT=11 and DMAMD=01 or 10)
- ADC_CTRL3.RSTART, ADC_CTRL3.JSTART
- SWRSTOP, SWJSTOP

Above bits in the slave ADC (ADC2) are always equal to the corresponding bits of the master ADC.

To start a conversion in dual mode, the user must program the bits EXTPRSEL[1:0], EXTRSEL,EXTPJSEL[1:0], EXTJSEL of the master ADC only, to configure a software or hardware trigger, and a regular or injected trigger. **Only trigger on master is allowed to use, the trigger on slave is prohibited.**

In regular simultaneous or interleaved modes: once the user sets bit ADC_CTRL3.RSTART or bit SWRSTOP of the master ADC, the corresponding bit of the slave ADC is also automatically set. However, bit ADC_CTRL3.RSTART or bit SWRSTOP of the slave ADC is not necessary cleared at the same time as the master ADC bit.

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In injected simultaneous or alternate trigger modes: once the user sets bit ADC_CTRL3.JSTART or bit SWJSTOP of the master ADC, the corresponding bit of the slave ADC is also automatically set. However, bit ADC_CTRL3.JSTART or bit SWJSTOP of the slave ADC is not necessary cleared at the same time as the master ADC bit.

In dual ADC mode, the converted data of the master and slave ADC can be read in parallel, by reading the ADC1_DAT and ADC1_JDATx. These registers are in 32-bit: the upper 16-bit apart used for ADC2, the lower apart used for ADC1. Note that ADC2_DAT and ADC2_JDATx still store the converted data of ADC2 which can be read separately.

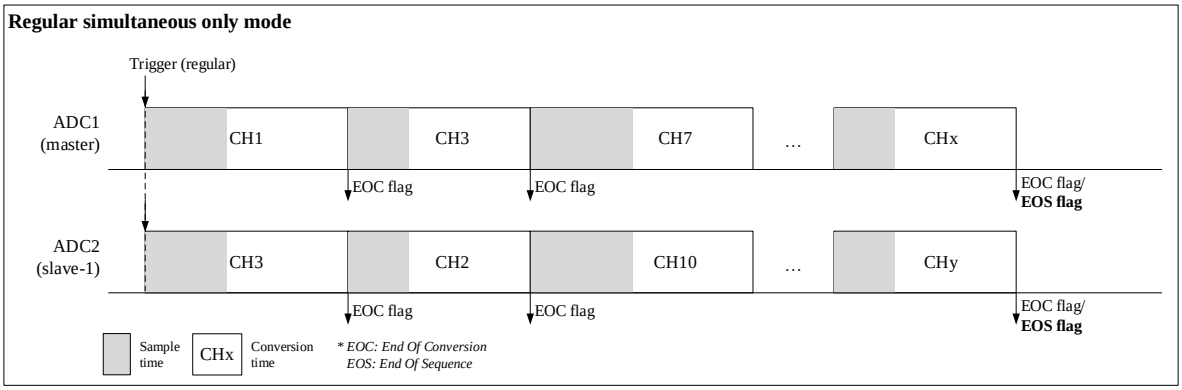
Note: In multi ADC mode, when configuring conversion trigger by an external event, the application must set trigger by the master only and disable trigger by slaves to prevent spurious triggers that would start unwanted slave conversions.

26.5.13.1 Regular simultaneous only

This mode is selected by programming bits MULTMODE[4:0] = 00110.

This mode is performed on a regular group of channels. The external trigger source comes from the regular group multiplexer of the master ADC (selected by the EXTRSEL bits). A simultaneous trigger is provided to the slave ADC.

Figure 26-26 Dual ADC regular simultaneous only mode



In this mode, independent injected conversions are supported. An injection request (either on master or on the slave) aborts the current simultaneous conversions, which are restarted once the injected conversion is completed.

Note: Do not convert the same channel on the two ADCs (no overlapping sampling times for the two ADCs when converting the same channel).

In regular simultaneous mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the longer conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

Software is notified by interrupts when it can read the data:

- At the end of each conversion event (ENDCA) on the master ADC, a master EOC interrupt is generated (if ENDCAIEN is enabled) and software can read the ADC_DAT of the master ADC.
- At the end of each conversion event (ENDCA) on the slave ADC, a slave EOC interrupt is generated (if ENDCAIEN is enabled) and software can read the ADC_DAT of the slave ADC.

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It allows sequence length on ADC1 master and ADC2 slave different from each other. This means below configuration settings can be different between master and slave:

1. Trigger delay (DLYVAL)
2. Sample time (SAMPx)
3. Number of channels (LEN)

However, in case of different sequence length, user must calculate to ensure below:

- One ADC does not sample an input while another one is converting that input
- The interval between triggers is longer than the longer conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

It is also possible to read the regular data using the DMA.

- Using two DMA channels (one for the master and one for the slave):
  - Configure the DMA master ADC channel to read ADC_DAT from the master. DMA requests are generated at each EOC event of the master ADC.
  - Configure the DMA slave ADC channel to read ADC_DAT from the slave. DMA requests are generated at each EOC event of the slave ADC.

    To apply this method, set DMAMD=01 in ADC1 register. It is normally used in case the sequence length is different between master and slave.
- Using one DMA on ADC1 master (leave DMA on ADC2 free)
  - Configure the DMA master ADC channel to read ADC_DAT from the master. DMA requests are generated at each EOC event of the master ADC.

    To apply this method, set DMAMD=10 in ADC1 register. It is normally used in case the sequence length is same between master and slave. In case of different sequence length, it must not be used since the data cannot be synchronized correctly and can be lost.

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Figure 26-27 Dual ADC regular simultaneous only mode DMAMD=01

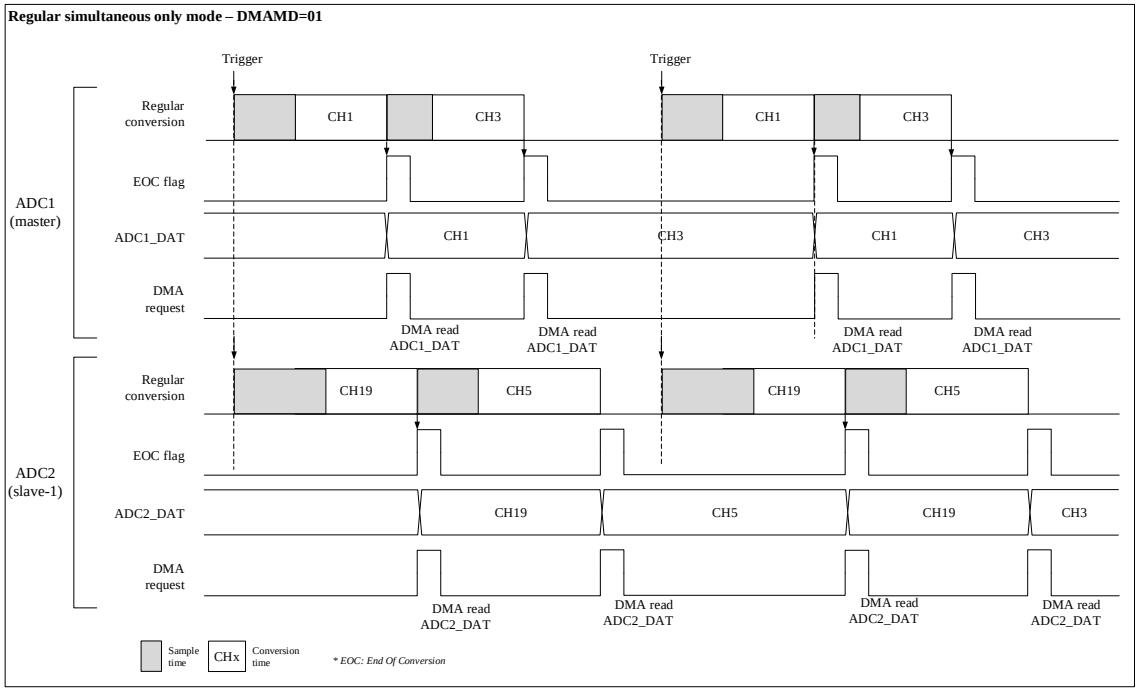
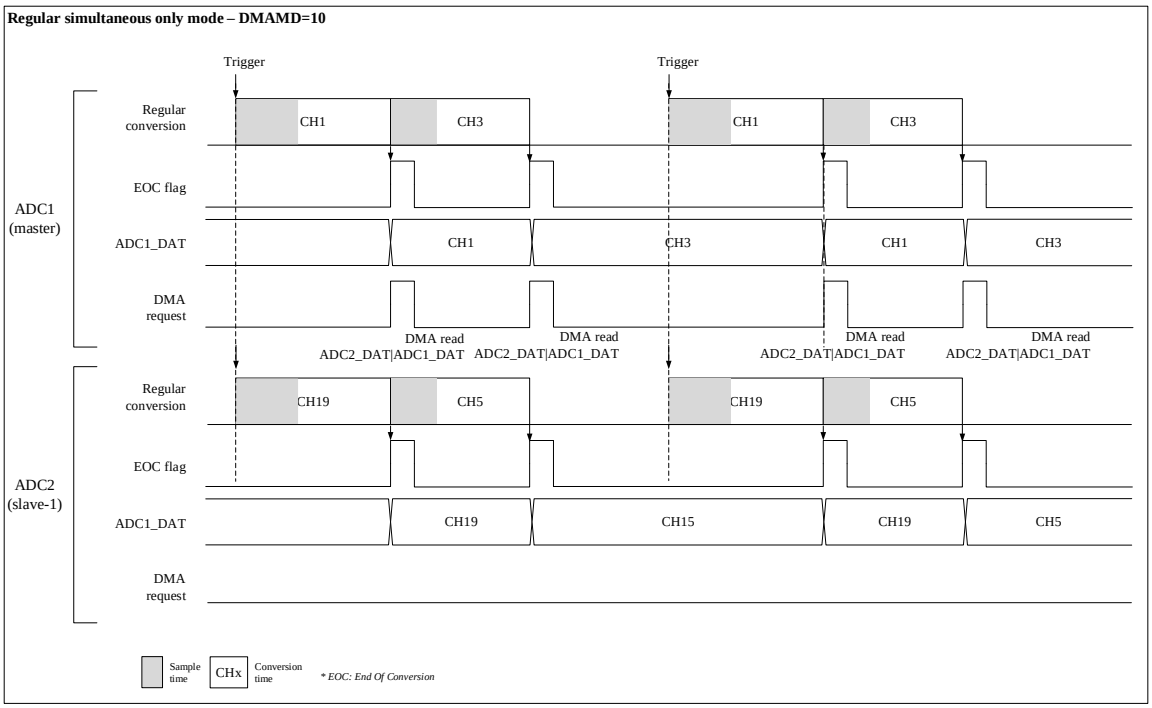


Figure 26-28 Dual ADC regular simultaneous only mode DMAMD=10



If DREGCH = 1 then each “n” simultaneous conversions of the regular sequence require a regular trigger event to occur (“n” is defined by DCTU).

26.5.13.2 Regular interleaved only

This mode is selected by programming bits MULTMODE[4:0] = 00111.

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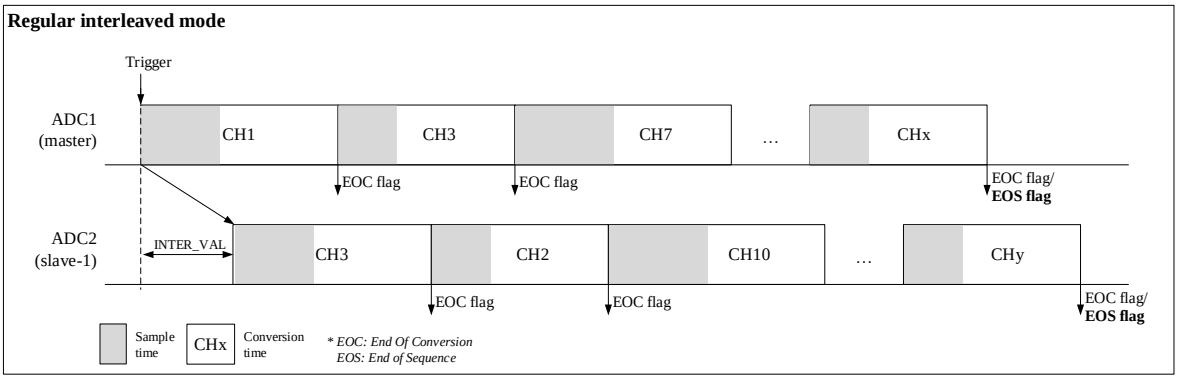
This mode can be started only on a regular group (usually one channel). The external trigger source comes from the regular channel multiplexer of the master ADC.

After an external trigger occurs:

- The master ADC starts immediately.
- The slave ADC starts after a delay of several ADC clock cycles after the sampling phase of the master ADC has complete.

Figure 26-29 Dual ADC regular simultaneous only mode



The minimum delay which separates two conversions in interleaved mode is configured in the INTLEADVAL bits in the ADC_DLYSMP register. User must properly calculate this delay to ensure that an ADC does not start a conversion while the other ADC is still sampling its input.

If the ADC_CTRL2.CTU bit is set on both master and slave ADCs, the selected regular channels of both ADCs are continuously converted.

The software is notified by interrupts when it can read the data at the end of each conversion event (ENDCA) on the slave ADC. A slave and master EOC interrupts are generated (if ENDCAIEN is enabled) and the software can read the ADC_DAT of the slave/master ADC.

It is also possible to have the regular data transferred by DMA.

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Figure 26-30 Dual ADC regular interleaved mode (DMAMD=01)

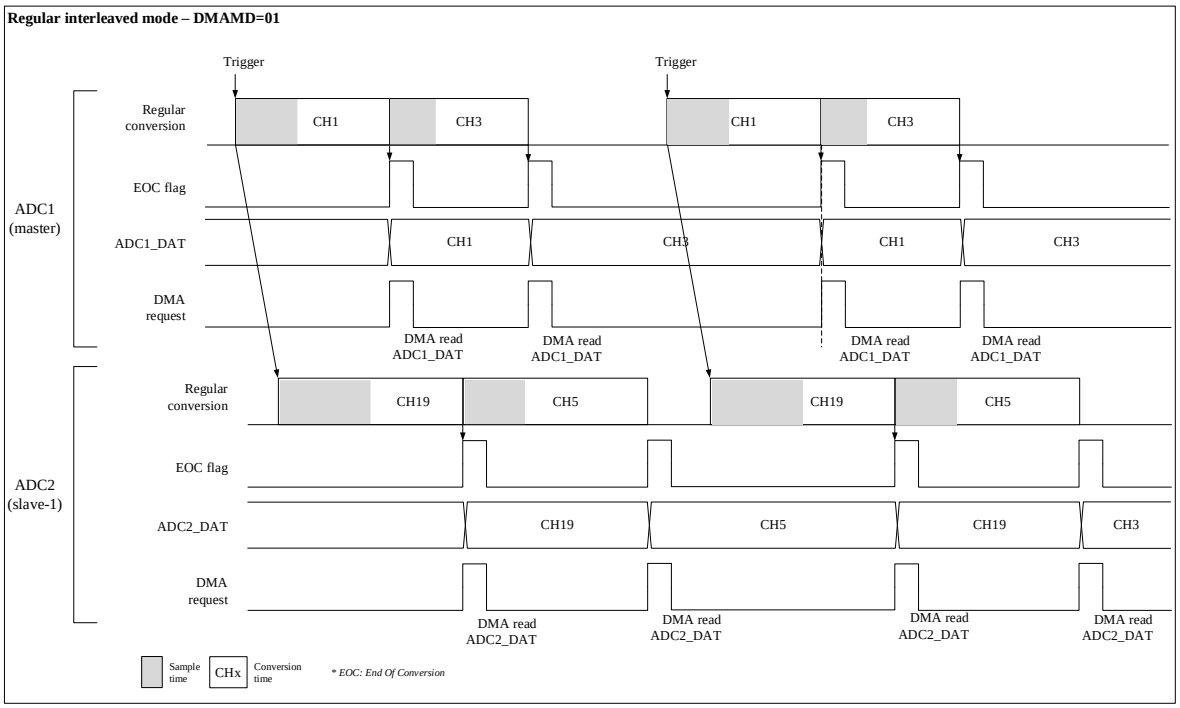
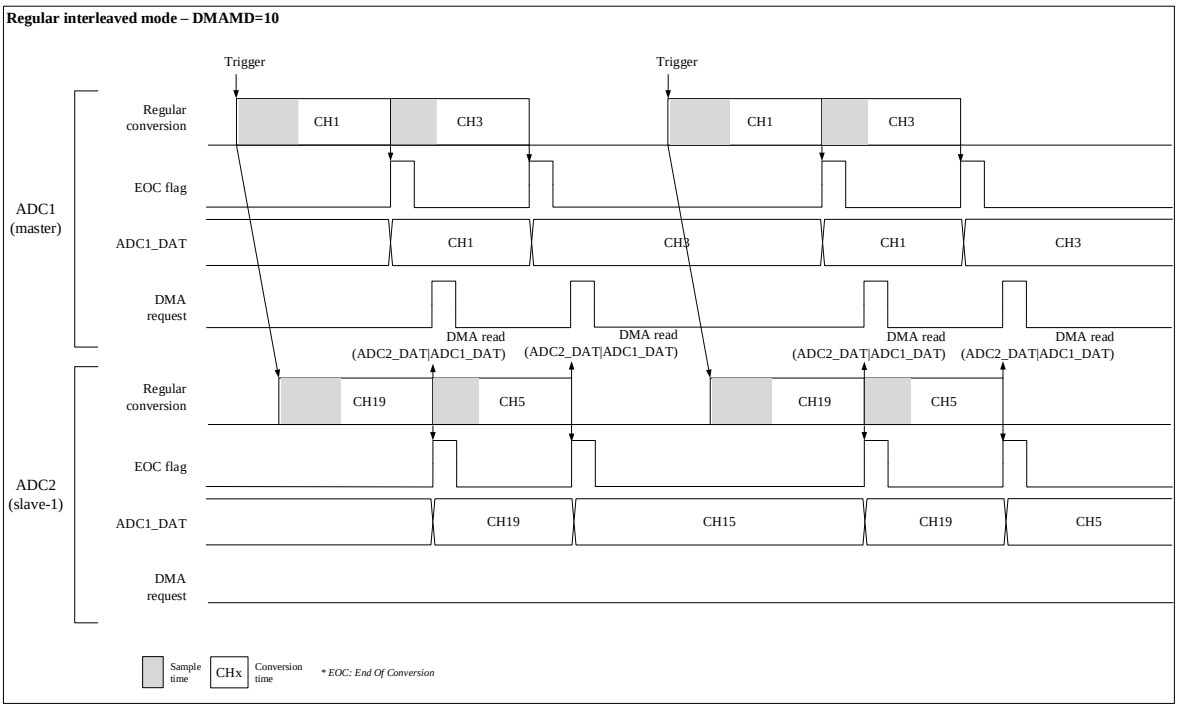


Figure 26-31 Dual ADC regular interleaved mode (DMAMD=10)



If DREGCH = 1, each “n” simultaneous conversions (“n” is defined by DCTU) of the regular sequence require a regular trigger event to occur.

In this mode, injected conversions are supported. When injection is done (either on master or on slave), both the master and the slave regular conversions are aborted and the sequence is restarted from the master.

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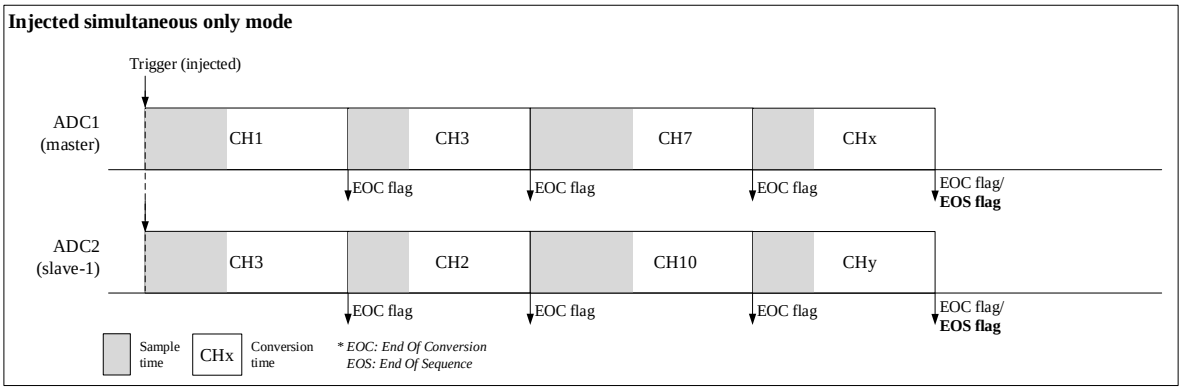
26.5.13.3 Injected simultaneous only

This mode is selected by programming bits MULTMODE[4:0] = 00101.

This mode converts an injected group of channels. The external trigger source comes from the injected group multiplexer of the master ADC (selected by the EXTJSEL bits).

Figure 26-32 Dual ADC injected simultaneous only mode



Note: Do not convert the same channel on the two ADCs (no overlapping sampling times for the two ADCs when converting the same channel).

In simultaneous mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the longer of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

Regular conversions can be performed on one or all ADCs. In that case, they are independent of each other and are interrupted when an injected event occurs. They are resumed at the end of the injected conversion group.

- At the end of injected sequence of conversion event (JENDC) on the master ADC, the converted data is stored into the master ADC_JDATy registers and a JENDC interrupt is generated (if enabled)
- At the end of injected sequence of conversion event (JENDC) on the slave ADC, the converted data is stored into the slave ADC_JDATy registers and a JENDC interrupt is generated (if enabled)
- If the duration of the master injected sequence is equal to the duration of the slave injected one, it is possible for the software to enable only one of the two JENDC interrupt (ex: master JENDC) and read both converted data (from master ADC_JDATy and slave ADC_JDATy registers).

If DJCH = 1, each simultaneous conversion of the injected sequence requires an injected trigger event to occur.

26.5.13.4 Injected alternate trigger only

This mode is selected by programming bits MULTMODE[4:0] = 01001.

This mode can be started only on an injected group. The source of external trigger comes from the injected group multiplexer of the master ADC.

This mode is only possible when selecting hardware triggers: EXTPJSEL[1:0] must not be 00.

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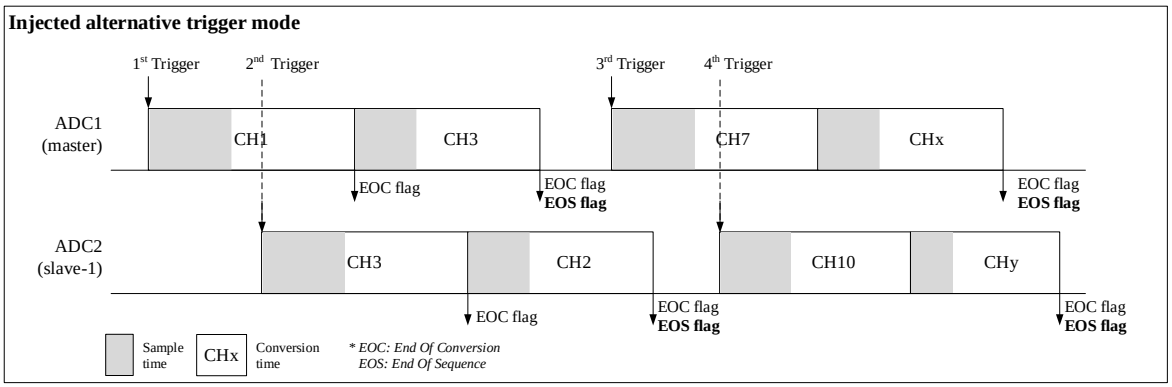
Figure 26-33 Dual ADC injected alternate trigger only mode



Injected discontinuous mode disabled (DJCH = 0 for all ADCs):

1. When the 1st trigger occurs, all injected master ADC channels in the group are converted.
2. When the 2nd trigger occurs, all injected slave ADC channels in the group are converted.
3. And so on.

A JENDC interrupt, if enabled, is generated after all injected channels of the master ADC in the group have been converted.

A JENDC interrupt, if enabled, is generated after all injected channels of the slave ADC in the group have been converted.

JENDCA interrupts, if enabled, can also be generated after each injected conversion.

If another external trigger occurs after all injected channels in the group have been converted then the alternate trigger process restarts by converting the injected channels of the master ADC in the group.

Note: Regular conversions can be enabled on one or all ADCs. In this case the regular conversions are independent of each other. A regular conversion is interrupted when the ADC has to perform an injected conversion. It is resumed when the injected conversion is finished.

The time interval between 2 trigger events must be greater than or equal to 1 ADC clock period. The minimum time interval between 2 trigger events that start conversions on the same ADC is the same as in the single ADC mode.

Injected discontinuous mode enabled (DJCH = 1 for all ADCs):

If the injected discontinuous mode is enabled for both master and slave ADCs:

1. When the 1st trigger occurs, the first injected channel of the master ADC is converted.
2. When the 2nd trigger occurs, the first injected channel of the slave ADC is converted.
3. And so on.

A JENDC interrupt, if enabled, is generated after all injected channels of the master ADC in the group have been converted.

A JENDC interrupt, if enabled, is generated after all injected channels of the slave ADC in the group have been converted.

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JENDCA interrupts, if enabled, can also be generated after each injected conversion.

If another external trigger occurs after all injected channels in the group have been converted then the alternate trigger process restarts.

26.5.13.5 Combined regular simultaneous + injected simultaneous

This mode is selected by programming bits MULTMODE[4:0] = 00001.

It is possible to interrupt the simultaneous conversion of a regular group to start the simultaneous conversion of an injected group.

Note: In combined regular/injected simultaneous mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the long conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

26.5.13.6 Combined regular simultaneous + injected alternate trigger

This mode is selected by programming bits MULTMODE[4:0] = 00010.

It is possible to interrupt the simultaneous conversion of a regular group to start the alternate trigger conversion of an injected group. Figure 26-34 shows the behavior of an alternate trigger interrupting a simultaneous regular conversion.

The injected alternate conversion is immediately started after the injected event. If a regular conversion is already running, in order to ensure synchronization after the injected conversion, the regular conversion of all (master/slave) ADCs is stopped and resumed synchronously at the end of the injected conversion.

Note: In combined regular simultaneous + alternate trigger mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the long conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

If a trigger occurs during an injected conversion that has interrupted a regular conversion, the alternate trigger is served. Figure 26-35 shows the behavior in this case (note that the 6th trigger is ignored because the associated alternate conversion is not complete).

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Figure 26-34 Combined regular simultaneous + injected alternate trigger

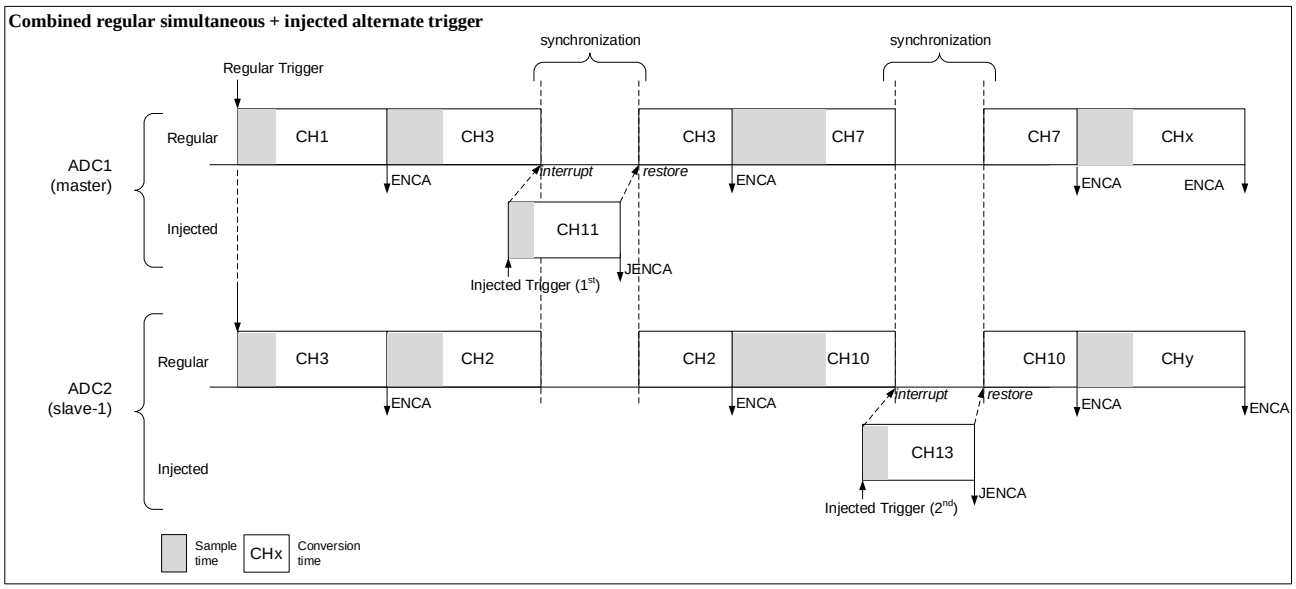
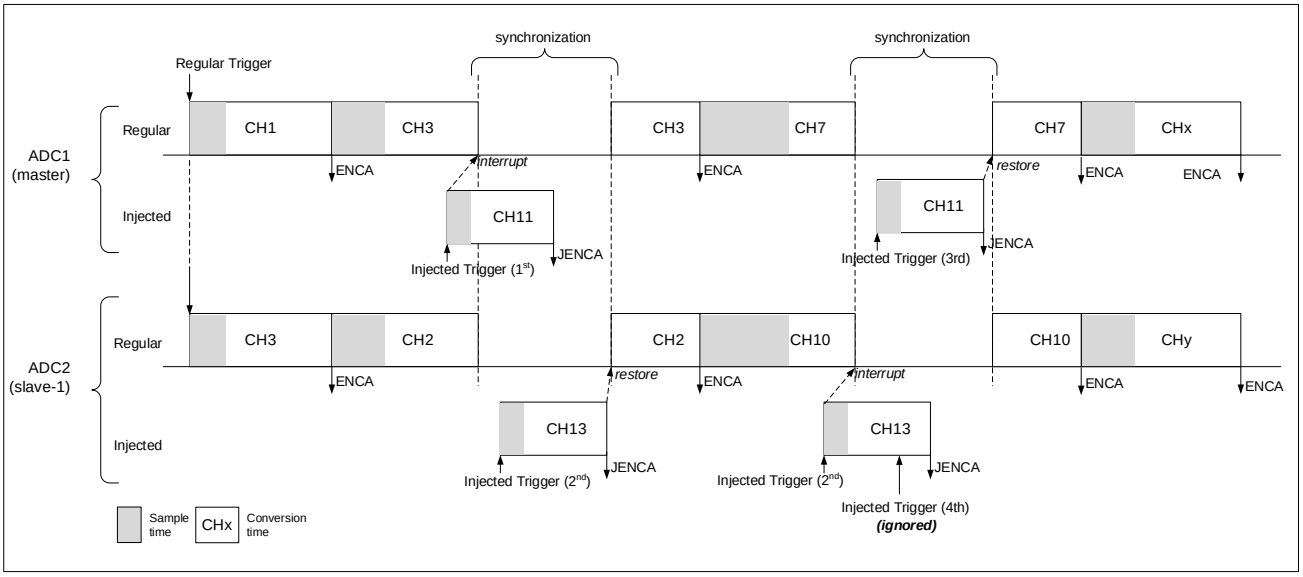


Figure 26-35 Case of trigger occurring during injected conversion



26.5.13.7 Combined regular interleaved + injected simultaneous

This mode is selected by programming bits MULTMODE[4:0] = 00011

It is possible to interrupt an interleaved conversion with a simultaneous injected event.

In this case the interleaved conversion is interrupted immediately and the simultaneous injected conversion starts. At the end of the injected sequence the interleaved conversion is resumed. When the interleaved regular conversion resumes, the first regular conversion which is performed is alway the master's one.

26.5.13.8 Stopping the conversions in dual ADC modes

The user must set the control bits SWRSTOP/SWJSTOP of the master ADC to stop the conversions of both ADC in dual ADC mode. The other SWRSTOP control bit of the slave ADC has no effect in dual ADC mode.

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Once both ADC are effectively stopped, the bits ADC_CTRL3.RSTART/ADC_CTRL3.JSTART of the master and slave ADCs are both cleared by hardware.

26.5.14 Triple ADC mode

In triple ADC mode the start of conversion is triggered alternately or simultaneously by the ADC1 master to the ADC2, ADC3 slaves depending on the mode selected by the bits MULTMODE[4:0] in the ADC_CTRL1 register.

Four possible modes are implemented:

- Injected simultaneous mode
- Regular simultaneous mode
- Interleaved mode
- Alternate trigger mode

It is also possible to use these modes combined in the following ways:

- Injected simultaneous mode + Regular simultaneous mode
- Regular simultaneous mode + Alternate trigger mode
- Injected simultaneous mode + Interleaved mode

In dual ADC mode, the following bits are only valid to set on master ADC (ADC1):

- SCANMD
- CTU
- DREGCH, DCTU, DJCH
- AUTOJC
- EXTPRSEL, EXTPJSEL
- DMNGT
- DMAMD
- MDSMU
- EN (applied only when DMNGT=11 and DMAMD=01 or 10)
- ADC_CTRL3.RSTART, ADC_CTRL3.JSTART
- SWRSTOP, SWJSTOP

Above bits in the slave ADC (ADC2, ADC3) are always equal to the corresponding bits of the master ADC.

To start a conversion in dual mode, the user must program the bits EXTPRSEL[1:0], EXTRSEL,EXTPJSEL[1:0], EXTJSEL of the master ADC only, to configure a software or hardware trigger, and a regular or injected trigger. (the bits EXTPRSEL[1:0] and EXTPJSEL[1:0] of the slave ADC are don’t care). Only trigger on master is allowed to use, the trigger on slave is prohibited.

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In regular simultaneous or interleaved modes: once the user sets bit ADC_CTRL3.RSTART or bit SWRSTOP of the master ADC, the corresponding bit of the slave ADC is also automatically set. However, bit ADC_CTRL3.RSTART or bit SWRSTOP of the slave ADC is not necessary cleared at the same time as the master ADC bit.

In injected simultaneous or alternate trigger modes: once the user sets bit ADC_CTRL3.JSTART or bit SWJSTOP of the master ADC, the corresponding bit of the slave ADC is also automatically set. However, bit ADC_CTRL3.JSTART or bit SWJSTOP of the slave ADC is not necessary cleared at the same time as the master ADC bit.

In triple ADC mode, the converted data of the master and slave ADC can be read in parallel, by reading the ADC1_DAT and ADC1_JDATy. These registers are in 32-bit: the upper 16-bit apart used for ADC2, the lower apart used for ADC1. Note that ADC2_DAT and ADC2_JDATy still store the converted data of ADC2 which can be read separately.

Note: In multi ADC mode, when configuring conversion trigger by an external event, the application must set trigger by the master only and disable trigger by slaves to prevent spurious triggers that would start unwanted slave conversions.

26.5.14.1 Regular simultaneous only

This mode is selected by programming bits MULTMODE[4:0] = 10110.

This mode is performed on a regular group of channels. The external trigger source comes from the regular group multiplexer of the master ADC (selected by the EXTRSEL bits). A simultaneous trigger is provided to the slave ADC.

In this mode, independent injected conversions are supported. An injection request (either on master or on the slave) aborts the current simultaneous conversions, which are restarted once the injected conversion is completed.

[Note]: *Do not convert the same channel on the three ADCs (no overlapping sampling times for the three ADCs when converting the same channel).*

In regular simultaneous mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the longer conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

Software is notified by interrupts when it can read the data:

- At the end of each conversion event (ENDCA) on the master ADC, a master EOC interrupt is generated (if ENDCAIEN is enabled) and software can read the ADC_DAT of the master ADC.
- At the end of each conversion event (ENDCA) on the slave ADC, a slave EOC interrupt is generated (if ENDCAIEN is enabled) and software can read the ADC_DAT of the slave ADC.
- It is also possible to read the regular data using the DMA.

  Using two DMA channels (one for the master and one for the slave):

  – Configure the DMA master ADC channel to read ADC_DAT from the master. DMA requests are generated at each EOC event of the master ADC.

  – Configure the DMA slave ADC channel to read ADC_DAT from the slave. DMA requests are generated at each EOC event of the slave ADC.

If DREGCH = 1 then each “n” simultaneous conversions of the regular sequence require a regular trigger event to

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occur (“n” is defined by DCTU).

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26.5.14.2 Regular interleaved only

This mode is selected by programming bits MULTMODE[4:0] = 10111.

This mode can be started only on a regular group (usually one channel). The external trigger source comes from the regular channel multiplexer of the master ADC.

After an external trigger occurs:

- The master ADC1 starts immediately.
- The slave ADC2 starts after a delay of several ADC clock cycles after the sampling phase of the master ADC1 has complete.
- The slave ADC3 starts after a delay of several ADC clock cycles after the sampling phase of the slave ADC2 has complete.

The minimum delay which separates two conversions in interleaved mode is configured in the INTLEADVAL bits in the ADC_DLYSMP register. User must properly calculate this delay to ensure that an ADC does not start a conversion while the other ADC is still sampling its input.

If the ADC_CTRL2.CTU bit is set on both master and slave ADCs, the selected regular channels of both ADCs are continuously converted.

The software is notified by interrupts when it can read the data at the end of each conversion event (ENDCA) on the slave ADC. A slave and master EOC interrupts are generated (if ENDCAIEN is enabled) and the software can read the ADC_DAT of the slave/master ADC.

It is also possible to have the regular data transferred by DMA.

If DREGCH = 1, each “n” simultaneous conversions (“n” is defined by DCTU) of the regular sequence require a regular trigger event to occur.

In this mode, injected conversions are supported. When injection is done (either on master or on slave), both the master and the slave regular conversions are aborted and the sequence is restarted from the master.

26.5.14.3 Injected simultaneous only

This mode is selected by programming bits MULTMODE[4:0] = 10101.

This mode converts an injected group of channels. The external trigger source comes from the injected group multiplexer of the master ADC (selected by the EXTJSEL bits).

Note: Do not convert the same channel on the two ADCs (no overlapping sampling times for the two ADCs when converting the same channel).

In simultaneous mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the longer of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

Regular conversions can be performed on one or all ADCs. In that case, they are independent of each other and are interrupted when an injected event occurs. They are resumed at the end of the injected conversion group.

- At the end of injected sequence of conversion event (JENDC) on the master ADC, the converted data is stored into the master ADC_JDATy registers and a JENDC interrupt is generated (if enabled)

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- At the end of injected sequence of conversion event (JENDC) on the slave ADC, the converted data is stored into the slave ADC_JDATy registers and a JENDC interrupt is generated (if enabled)
- If the duration of the master injected sequence is equal to the duration of the slave injected, it is possible for the software to enable only one of the two JENDC interrupt (ex: master JENDC) and read both converted data (from master ADC_JDATy and slave ADC_JDATy registers).

If DJCH = 1, each simultaneous conversion of the injected sequence requires an injected trigger event to occur.

26.5.14.4 Injected alternate trigger only

This mode is selected by programming bits MULTMODE[4:0] = 11001.

This mode can be started only on an injected group. The source of external trigger comes from the injected group multiplexer of the master ADC.

This mode is only possible when selecting hardware triggers: EXTPJSEL[1:0] must not be 00.

Injected discontinuous mode disabled (DJCH = 0 for all ADCs):

1. When the 1st trigger occurs, all injected master ADC1 channels in the group are converted.
2. When the 2nd trigger occurs, all injected slave ADC2 channels in the group are converted.
3. When the 3rd trigger occurs, all injected slave ADC3 channels in the group are converted.
4. And so on.

A JENDC interrupt, if enabled, is generated after all injected channels of the master ADC in the group have been converted.

A JENDC interrupt, if enabled, is generated after all injected channels of the slave ADC in the group have been converted.

JENDCA interrupts, if enabled, can also be generated after each injected conversion.

If another external trigger occurs after all injected channels in the group have been converted then the alternate trigger process restarts by converting the injected channels of the master ADC in the group.

Note: Regular conversions can be enabled on one or all ADCs. In this case the regular conversions are independent of each other. A regular conversion is interrupted when the ADC has to perform an injected conversion. It is resumed when the injected conversion is finished.

The time interval between 2 trigger events must be greater than or equal to 1 ADC clock period. The minimum time interval between 2 trigger events that start conversions on the same ADC is the same as in the single ADC mode.

Injected discontinuous mode enabled (DJCH = 1 for all ADCs):

If the injected discontinuous mode is enabled for both master and slave ADCs:

1. When the 1st trigger occurs, all injected master ADC1 channels in the group are converted.
2. When the 2nd trigger occurs, all injected slave ADC2 channels in the group are converted.
3. When the 3rd trigger occurs, all injected slave ADC3 channels in the group are converted.
4. And so on.

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A JENDC interrupt, if enabled, is generated after all injected channels of the master ADC in the group have been converted.

A JENDC interrupt, if enabled, is generated after all injected channels of the slave ADC in the group have been converted.

JENDCA interrupts, if enabled, can also be generated after each injected conversion.

If another external trigger occurs after all injected channels in the group have been converted then the alternate trigger process restarts.

26.5.14.5 Combined regular simultaneous + injected simultaneous

This mode is selected by programming bits MULTMODE[4:0] = 10001.

It is possible to interrupt the simultaneous conversion of a regular group to start the simultaneous conversion of an injected group.

Note: In combined regular/injected simultaneous mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the long conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

26.5.14.6 Combined regular simultaneous + injected alternate trigger

This mode is selected by programming bits MULTMODE[4:0] = 10010.

It is possible to interrupt the simultaneous conversion of a regular group to start the alternate trigger conversion of an injected group.

The injected alternate conversion is immediately started after the injected event. If a regular conversion is already running, in order to ensure synchronization after the injected conversion, the regular conversion of all (master/slave) ADCs is stopped and resumed synchronously at the end of the injected conversion.

Note: In combined regular simultaneous + alternate trigger mode, one must convert sequences with the same length or ensure that the interval between triggers is longer than the long conversion time of the 2 sequences. Otherwise, the ADC with the shortest sequence may restart while the ADC with the longest sequence is completing the previous conversions.

If a trigger occurs during an injected conversion that has interrupted a regular conversion, the alternate trigger is served.

26.5.14.7 Combined regular interleaved + injected simultaneous

This mode is selected by programming bits MULTMODE[4:0] = 10011

It is possible to interrupt an interleaved conversion with a simultaneous injected event.

In this case the interleaved conversion is interrupted immediately and the simultaneous injected conversion starts. At the end of the injected sequence the interleaved conversion is resumed. When the interleaved regular conversion resumes, the first regular conversion which is performed is alway the master’s one.

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

26.5.14.8 Stopping the conversions in triple ADC modes

The user must set the control bits SWRSTOP/SWJSTOP of the master ADC to stop the conversions of all ADCs in triple ADC mode. The other SWRSTOP control bit of the slave ADCs has no effect in dual ADC mode.

Once all ADCs are effectively stopped, the bits ADC_CTRL3.RSTART/ADC_CTRL3.JSTART of the master and slave ADCs are both cleared by hardware.

26.6 ADC calibration

26.6.1 ADC calibration timing

Figure 26-36 shows the calibration timing.

t_{CALADC}: calibration time. It can be configured by ADC_INTLRCFG register to write value to internal register of ADC IP (ADC_CALWIN – address 0x6, see section 26.6.2 for detail). It is calculated by following formula:

t_{CALADC} (ADC kernel clock cycle) = (((2 x ADC_CALWIN) + 2) x 4) + 2

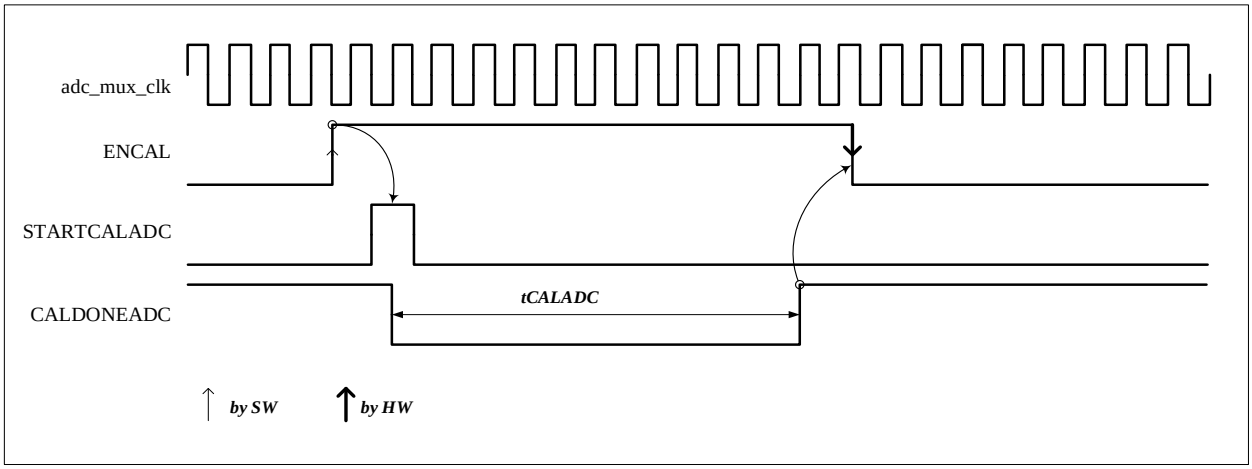
For example:

– ADC_CALWIN=0: t_{CALADC} = 14 cycles

– ADC_CALWIN=4: t_{CALADC} = 74 cycles. This is default value after reset.

In normal situation, the user does not need to change this register value but if there is a trade-off needed between calibration time and accuracy then this register can be changed.

Figure 26-36 Calibration timing



26.6.2 ADC calibration configuration

The ADC has the built-in calibration registers and allow to load/read/modify the coefficients for ADC.

These registers can also be used to read calibration data and upload it later, if there is any need to apply power gating on the digital supply of the ADC.

Table 26-8 shows the detail of the ADC internal registers.

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Table 26-8 ADC internal register for calibration

REGISTER ADDRESS	REG NAME	BITS								RESET VALUE	RW
		7	6	5	4	3	2	1	0		
0x00	ID	ID								0xAD	R
0x01	CONFIG0	ADC_OFFSET								0x80	R/W
0x02	CONFIG1	0								0x00	R
0x03	CONFIG2	0	ADC_DCAL[14:8]							0x00	R/W
0x04	CONFIG3	ADC_DCAL[7:0]								0xFF	R/W
0x05	CONFIG4	0	ADCCAL_DONE	CALCTRL_ADC	0	CALCTRL_DCAL	0			0x40	R/W (a)
0x06	CONFIG5	**0**					ADC_CALWIN			0x04	R/W
0x07	CONFIG6	**0**								0x00	R

(a) BIT 7 & 6 are read-only

REG FIELD NAME	PURPOSE
ID	ID of the ADC (0xAD returned as ID)
CALCTRL_ADC	Selection of external ADC offset bits
ADC_OFFSET	Externally applied 8-bit ADC offset bits
CALCTRL_DCAL	Selection of external Delay calibration bits
ADC_DCAL[14:0]	Externally applied 15-bit Delay calibration bits
ADC_CALWIN	Number of ADC conversions for averaging
ADCCAL_DONE	Flag to indicate ADC calibration is complete

These registers cannot be accessed directly but must use the ADC internal register configuration register (ADC_INTLRCFG) of controller. Below describes software procedure to access the ADC internal register:

Software procedure to read ADC internal register

1. Set ADC_CFG_RW_CTRL=0 (read)
2. Set ADC_CFG_ADDR=<*Internal register address*>
3. Set ADC_CFG_RW_START=1
4. Polling ADC_CFG_RW_DONE bit until it is 1
5. Read ADC_CFG_RDATA to get content of the internal register(8-bit data only)

Software procedure to write ADC internal register

1. Dummy Read: execute steps R1-R5 with ADC_CFG_ADDR=<*Internal register address*>

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2. Dummy Write:
   a) Set ADC_CFG_RW_CTRL=1 (write)
   b) Set ADC_CFG_ADDR=<*Internal register address*>
   c) Set ADC_CFG_WDATA=<*Expected value*>(8-bit data only)
   d) Set ADC_CFG_RW_START=1
   e) Polling ADC_CFG_RW_DONE bit until it is 1
3. Dummy Read: execute steps R1-R5 with ADC_CFG_ADDR=<*Internal register address*>
4. Main Write: Repeat steps 2.a-2.e
5. Dummy Write: execute steps R1-R5 with ADC_CFG_ADDR=<*Internal register address*>

Note: Dummy Read/Write for write procedure is needed to assure the hardware timing.

26.7 Offset compensation

An offset y (y = 1,2,3,4) can be applied to a channel by setting the bit OFFSCHyEN = 1 into ADC_OFFSETy register. The channel to which the offset is applied is programmed into the bits OFFSCHyCH[4:0] of ADC_OFFSETy register. In this case, the converted value is decreased by the user-defined offset written in the bits OFFSCHyDAT[11:0]. The result may be a negative value so the read data is signed and the SEXT bit represents the extended sign value.

When OFFSCHySATEN bit is set in ADC_OFFSETy register during offset operation, data are unsigned. All the offset data saturate at 0x000 (in 12-bit mode). When OFFSCHyDIR bit is set, the offsetdirection is positive and the data saturate at 0xFFF (in 12-bit mode). In 10-bit mode, data saturate at 0x00 and 0x3FF, respectively.

The analog watchdog comparison is performed on unsigned values, after offset and gain compensation. For correct watchdog operation, the data after offset compensation must be in unsigned format (OFFSCHySATEN bit set in ADC_OFFSETy register).

Note: Offset correction is not supported in oversampling mode. When OSRE and/or OSJE bit is set, the value of the OFFSCHyEN bit in ADC_OFFSETy register is ignored (considered as reset).

Table 26-9 Offset computation versus data resolution

RES bit	Raw converted data	Offset	Result	Note
1: 12-bit	DATA[11:0]	OFFSCHyDAT[11:0]	Signed 12-bit data	
0: 10-bit	DATA[11:2],00	OFFSCHyDAT[11:2]	Signed 10-bit data	OFFSCHyDAT[1:0] is not used. User should configure this to 00

26.8 Gain compensation

This function is to improve the dynamic range of the ADC even when the input range is not aligned with the reference voltage

- Applying a gain factor helps extend the signal range to map it to the full ADC range

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- It is applied on all converted data (all channels) after oversampling shift

When GCOMPEN bit is set in ADC_CTRL3 register, the gain compensation is activated on all the converted data. After each conversion, data is calculated with the following formula:

$$DATA = DATA(converted) \times GCOMPCOEFF[13:0] \div 4096$$

As GCOMPDAT can be programmed from 0 to 16383, the actual gain compensation factor can range from 0 to 3.999756. Gain factor = GCOMPDAT[13:0] ÷4096.

Since "÷4096" is equivalent to shifting 12-bit, before storing the resulting data in ADC_DAT or ADC_JRy registers, the 12-bit LSB value is evaluated to round up the data and minimize the error: if it higher than or equal to 2048 (12'h800) then plus 1, else plus 0. For example:

1. (Data x GCOMPDAT)= 24'h2F_A5A5
   → after shifting 12-bit: = 12'h2FA, left part = 12'h5A5 < 12'h800
   → final result keep 12'h2FA
2. (Data x GCOMPDAT)= 24'h2F_A9A5
   → after shifting 12-bit: = 12'h2FA, left part = 12'h9A5 > 12'h800
   → final result plus 1: 12'h2FB

The gain compensation is also effective for the oversampling. When the gain compensation is used for the oversampling mode, the gain calculation is performed after the accumulation and right-shift operations to minimize the power consumption (the gain calculation is done only once instead of at each conversion).

Note: Since GCOMPDAT is 14-bit and 4096 is 12-bit, the data after gain compensation can be up to 14-bit. However, only 12-bit LSBs are used for watchdog comparison. Therefore, user should set GCOMPDAT so that the result data is not over 12-bit in order to prevent wrong data comparison.

26.9 Alignment

The ALIG bit in the ADC_CTRL2 register selects the alignment of the data stored after conversion. Data can be right- or left-aligned as shown in section 26.10.1.

Note: Left-alignment is not supported in oversampling mode. When OSRE and/or OSJE bit is set, the ALIG bit value is ignored and the ADC only provides right-aligned data.

26.10 Data management

At the end of each regular conversion channel (when EOC event occurs), the result of the converted data is stored into the ADC_DAT data register which is 32 bits wide. CPU or other master (DMA) can read data directly from this register for further processing, or simply store to RAM and prevent from overrunning. It also has an interface to transfer the converted data directly to DSMU. If FIFO is used (EN=1), the converted result is stored to FIFO buffer. When CPU or other master read ADC_DAT register, it will read the 1st data valid from FIFO. Multi-adc modes and DMNGT mode affects to how the data arranged in ADC_DAT, refer to related section for more detail.

At the end of each injected conversion channel (when JEOC event occurs), the result of the converted data is stored into the corresponding ADC_JDATy data register which is 32 bits wide. CPU or other master can read directly these registers to get conversion data result for further processing, or simply store to RAM to prevent from overrunning.

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FIFO is not available for injected conversion. Multi-adc modes and DMNGT mode do not affect to how the data arranged in ADC_JDATy.

Figure 26-37 Figure 26-37 Regular conversion result data management flowand Figure 26-38 shows the flow to control the data after regular and injected conversion, respectively.

Figure 26-37 Regular conversion result data management flow

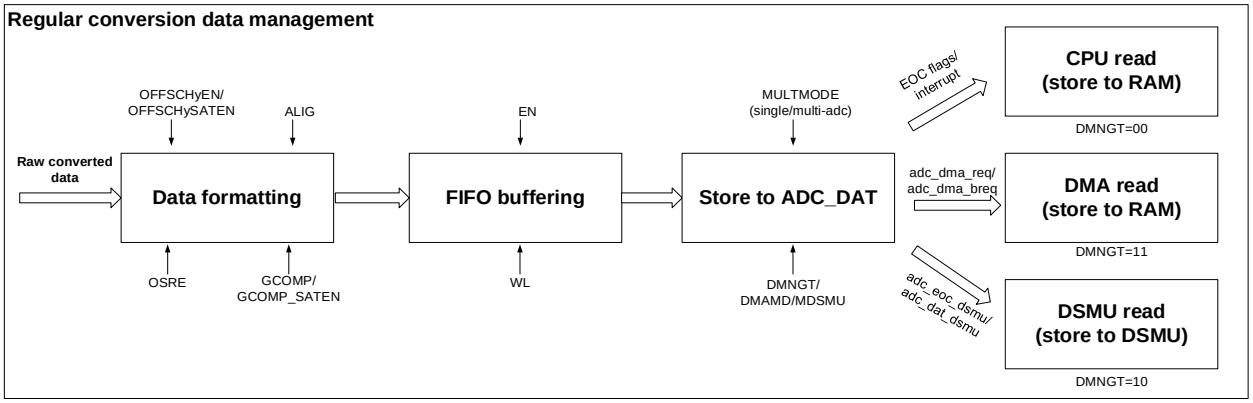
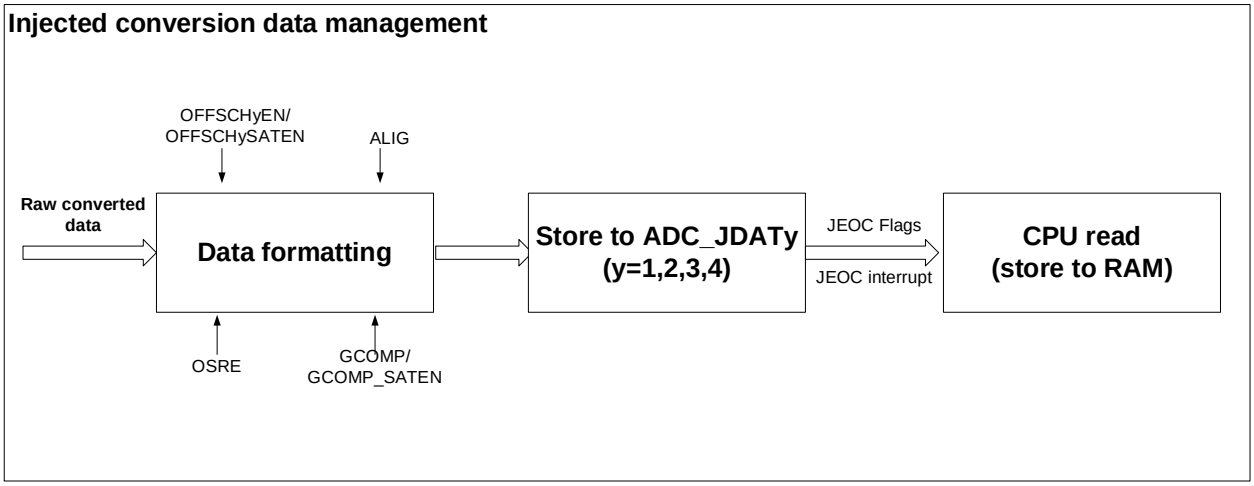


Figure 26-38 Injected conversion result data management flow



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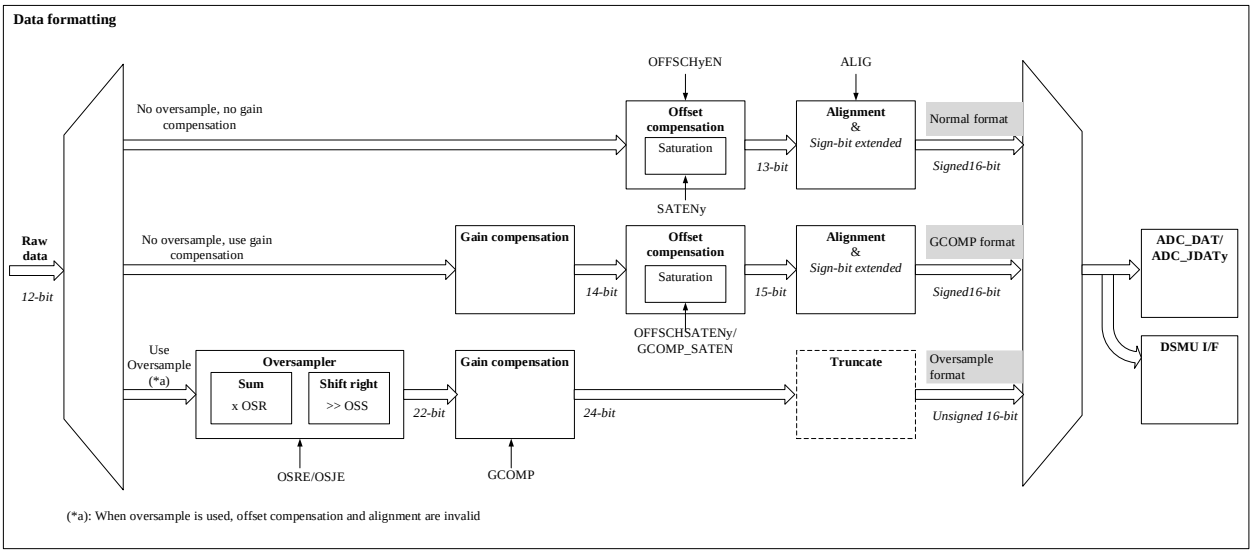
26.10.1 Data formatting

Figure 26-39 shows three possible types of data format, depended on offset/gain compensation and oversample.

Figure 26-39 Data formatting



26.10.1.1 Normal format

This format is used when both oversample and gain compensation are disable (OSRE/OSJE=0 and GCOMPEN=0). In this case, the data can be used directly from raw converted data (12-bit max). After offset compensation, the data can be negative or more than 12-bit (max 13-bit). Value range is from -0xFFF to +0x1FFE. Therefore, it is required to use 13-bit data (in case resolution is 12-bit) or 11-bit data (in case resolution is 10-bit) and extended to 16-bit before storing to registers. In case of OFFSCHySATEN=1, the data is always in 12-bit unsigned format: the value is saturated at 0x0 (if negative offset is used and the converted data less than offset) and saturated at 0xFFF. They are 10-bit unsigned format, saturated at 0x0 and 0x3FF in case of resolution 10-bit, respectively.

Table 26-10 Normal formatsummarizes all possible data format when normal format used.

Figure 26-40 Normal formatshows detail how data stored to 16-bit register in the normal format.

Table 26-10 Normal format

RES bit	OFFSCHyEN	OFFSCHyDIRy	OFFSCHySATEN	Data format	Note
1: 12-bit	0	x	x	12-bit unsigned	
	1	0	0	13-bit signed	
	1	1	0	13-bit unsigned	
	1	x	1	12-bit unsigned	saturation range: 0x0-0xFFF
0: 10-bit	0	x	x	10-bit unsigned	
	1	0	0	11-bit signed	
	1	1	0	11-bit unsigned	

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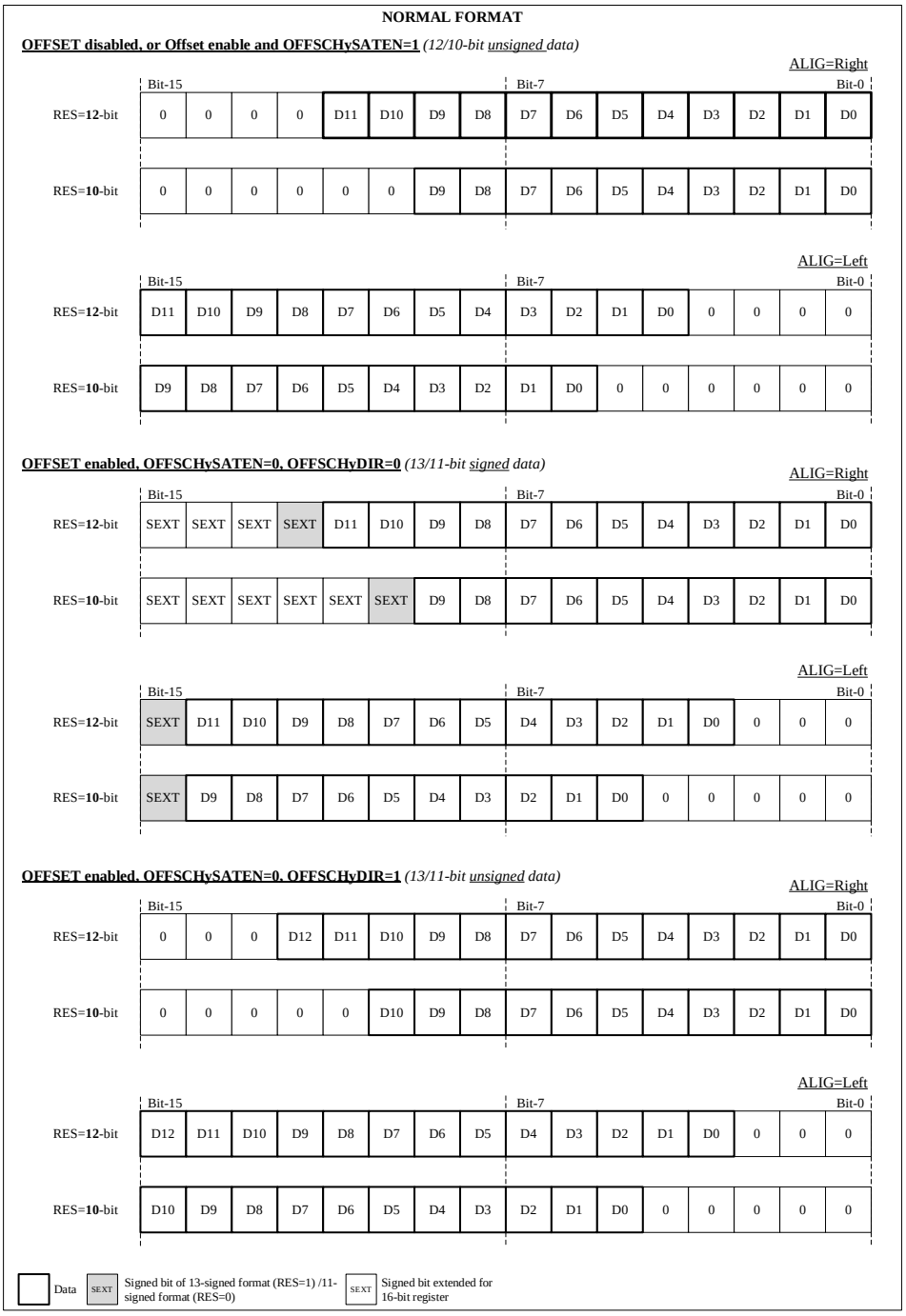
	1	x	1	10-bit unsigned	saturation range: 0x0-0x3FF

Figure 26-40 Normal format



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26.10.1.2 GCOMP format

This format is used when gain compensation are enabled (GCOMPEN=1), but oversample is not used (OSRE/OSJE=0). In this case, the data can be calculated as following formula:

$$DATA = (DATA(converted) \times GCOMPDAT \div 4096) \pm OFFSETy$$

By that, the data can be negative or more than 14-bit (max 15-bit). Therefore, it is required to use 15-bit signed data (in case resolution is 12-bit) or 13-bit signed data (in case resolution is 10-bit) and extended to 16-bit before storing to registers.

When Offset enable and OFFSCHySATEN=1:

- GCOMP_SATEN=1, the saturation range is extended: 0000-03FFF (RES=12-bit), and 0000-0FFF (RES=10-bit). The data is arranged in 14-bit unsigned (RES=12-bit), and 12-bit unsigned (RES=10-bit)
- GCOMP_SATEN=0, the saturation range is: 0000-00FFF (RES=12-bit), and 0000-03FF (RES=10-bit). However, the data is also arranged in 14-bit unsigned (RES=12-bit), and 12-bit unsigned (RES=10-bit)

GCOMP_SATEN is ignored when offset disable or OFFSCHySATEN=0.

Table 26-11 summarizes all possible data format when GCOMP format used.

Figure 26-41 shows detail how data stored to 16-bit register in the GCOMP format.

Table 26-11 GCOMP format

RES bit	OFFSCHyDAT_EN	OFFSCHyDIRy	OFFSCHySATEN	GCOMP_SATEN	Data format	Note
1: 12-bit	0	x	x	x	14-bit unsigned	-
	1	0	0	x	15-bit signed	-
	1	1	0	x	15-bit unsigned	-
	1	x	1	0	14-bit unsigned	saturation range: 0x0-0xFFF
	1	x	1	1	14-bit unsigned	saturation range: 0x0-0x3FFF
0: 10-bit	0	x	x	x	12-bit unsigned	-
	1	0	0	x	13-bit signed	-
	1	1	0	x	13-bit unsigned	-
	1	x	1	0	12-bit unsigned	saturation range: 0x0-0x3FF
	1	x	1	1	12-bit unsigned	saturation range: 0x0-0xFFF

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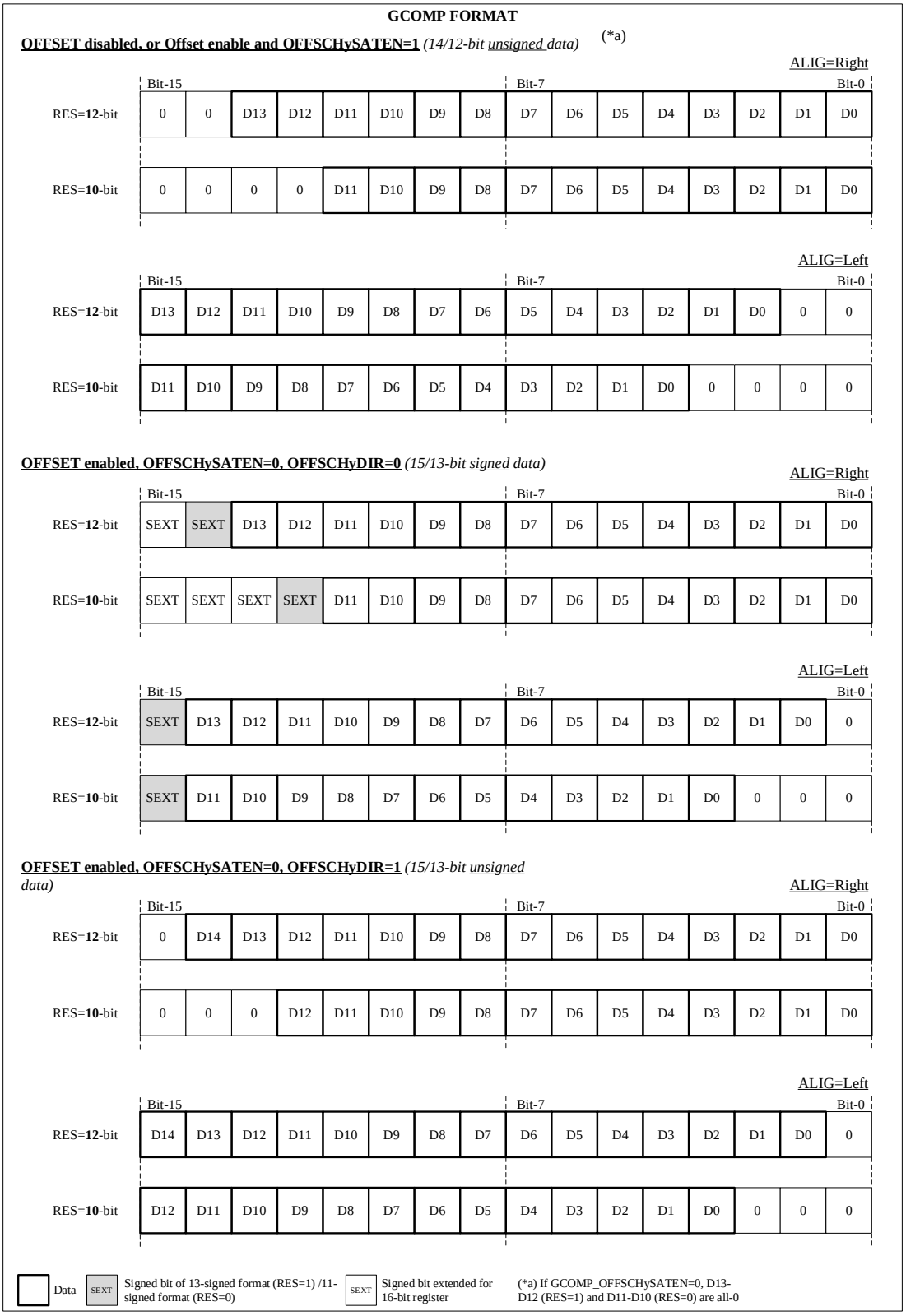
Figure 26-41 GCOMP format



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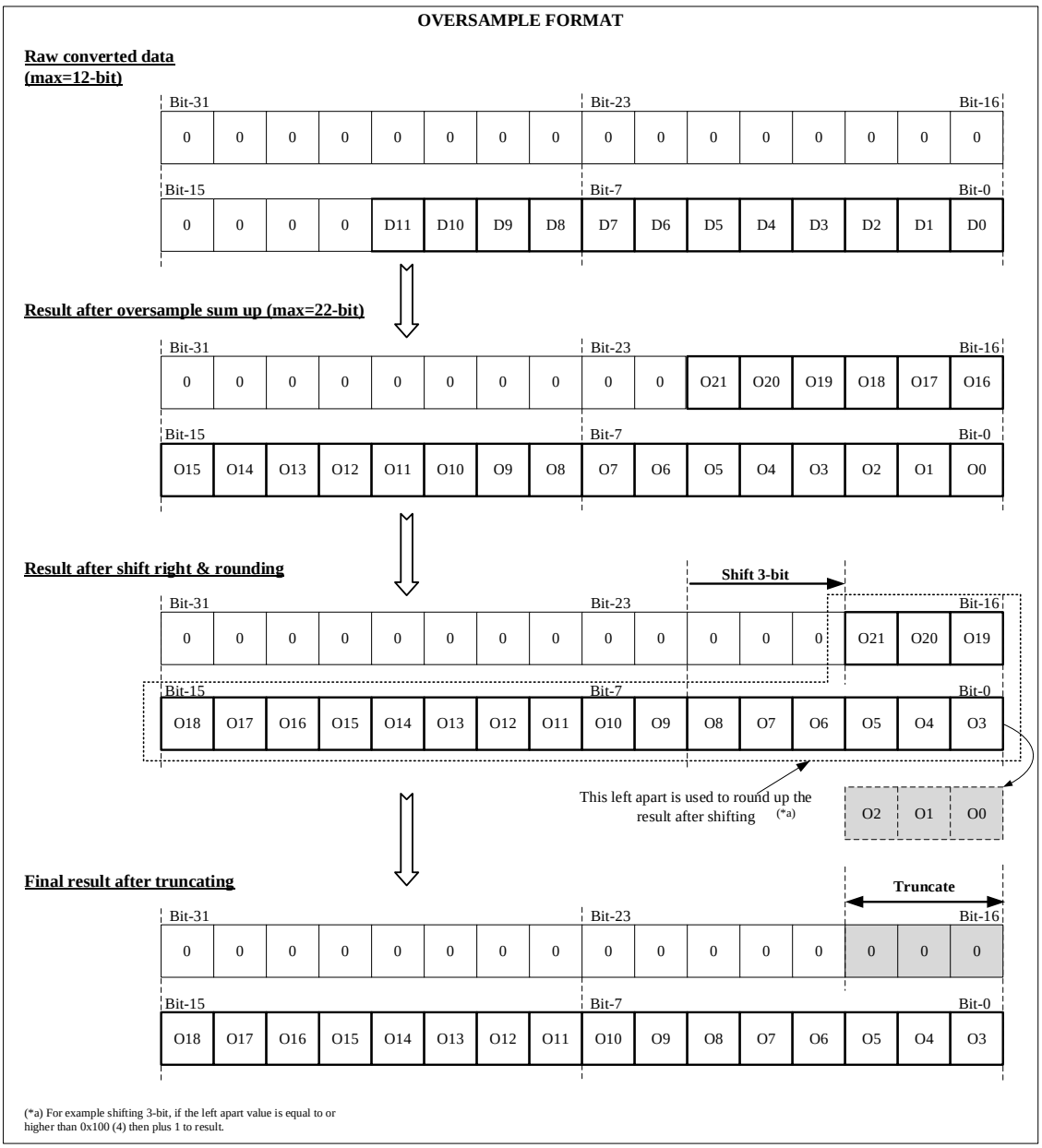
26.10.1.3 Oversample format

This format is used when oversample is used (OSRE=1 for regular conversion, and OSJE=1 for injected conversion).

In this case, offset compensation and alignment are invalid (related setting is ignored) and hence, the data is always in 16-bit unsigned format. However, since the result data can be yield up to 22 bits, it is rounded to the nearest value using the least significant bits left apart by the shifting, then it is truncated to the 16 least significant bits, before being finally transferred into the ADC_DAT or ADC_JDATy data registers.

Figure 26-42 shows detail how data stored to 16-bit register in the Oversample format. When user read the data in register with oversample format, it must be recognized as 16-bit unsigned data.

Figure 26-42 Oversample format (example: OSS=shift 3-bit)



Gain compensation if enabled (GCOMPEN=1) is performed to oversampling data after the step of shifting & rounding. Then it is also truncated in case the result data is over 16-bit.

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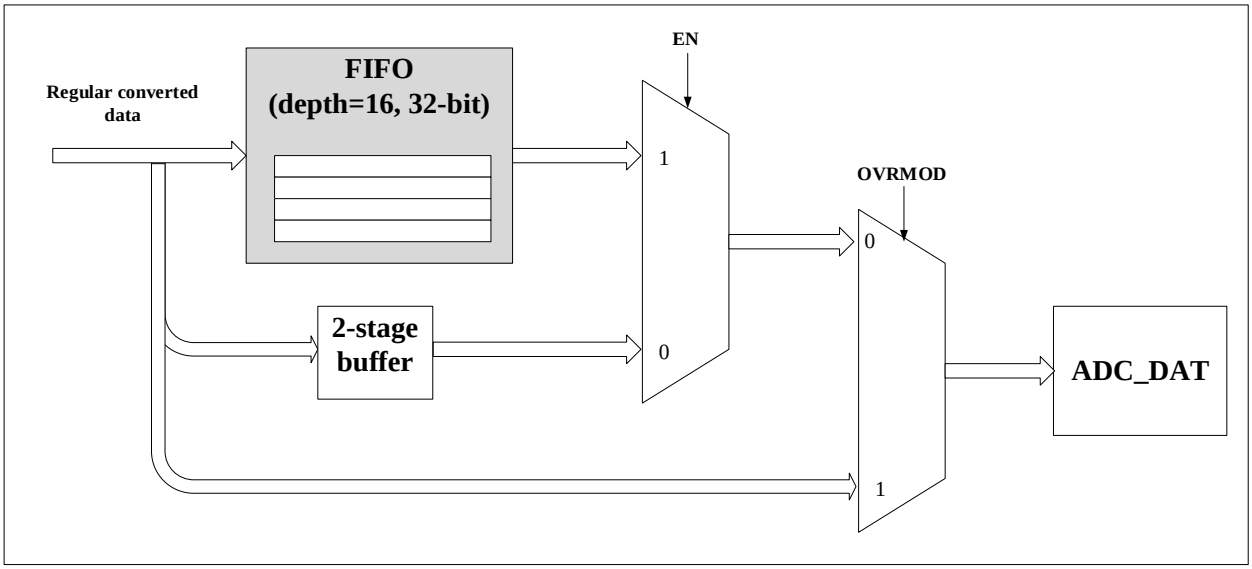
26.10.2 FIFO buffering (regular only)

For regular conversion data, there is a fifo for each ADC to store converted data. This FIFO is 16-stage depth, 32-bit data, and enabled to used when EN=1.

Figure 26-43 FIFO buffering



26.10.3 Manage data with DMA (regular only)

Since converted regular channel values are stored into a unique data register, it is useful to use DMA for conversion of more than one channel. This avoids the loss of the data already stored in the ADC_DAT register.

When the DMA mode is enabled (DMNGT=11), a DMA request is generated after each conversion of a channel. This allows the transfer of the converted data from the ADC_DAT register to the destination location selected by the software.

There are two DMA request signals used for single DMA transfer (adc_dma_req) and used for burst DMA transfer (adc_dma_breq). When FIFO is disable, adc_dma_req/adc_dma_breq are generated for each conversion, but only adc_dma_req are used by DMA. When FIFO is enable, adc_dma_breq are generated after FIFO reached the water mark level setting (WL); adc_dma_req are ignored. Both adc_dma_req and adc_dma_breq are de-asserted only after dma_ack_adc received.

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Figure 26-44 DMA request (FIFO disable)

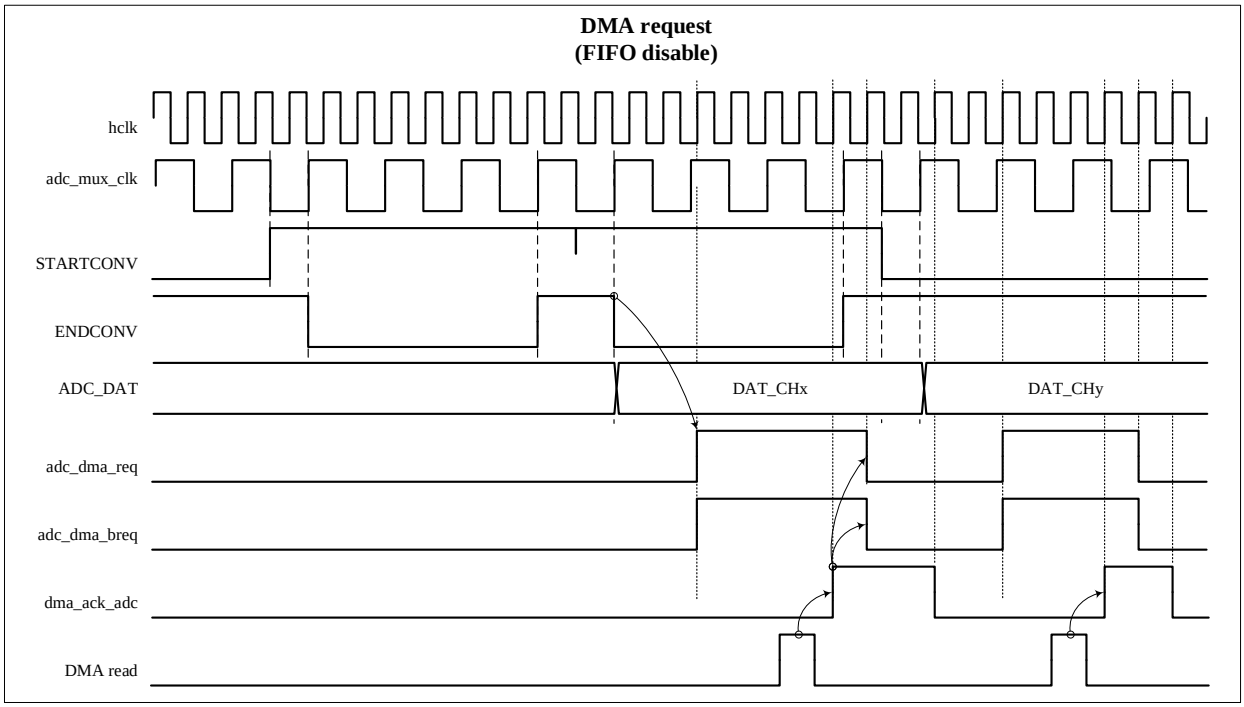
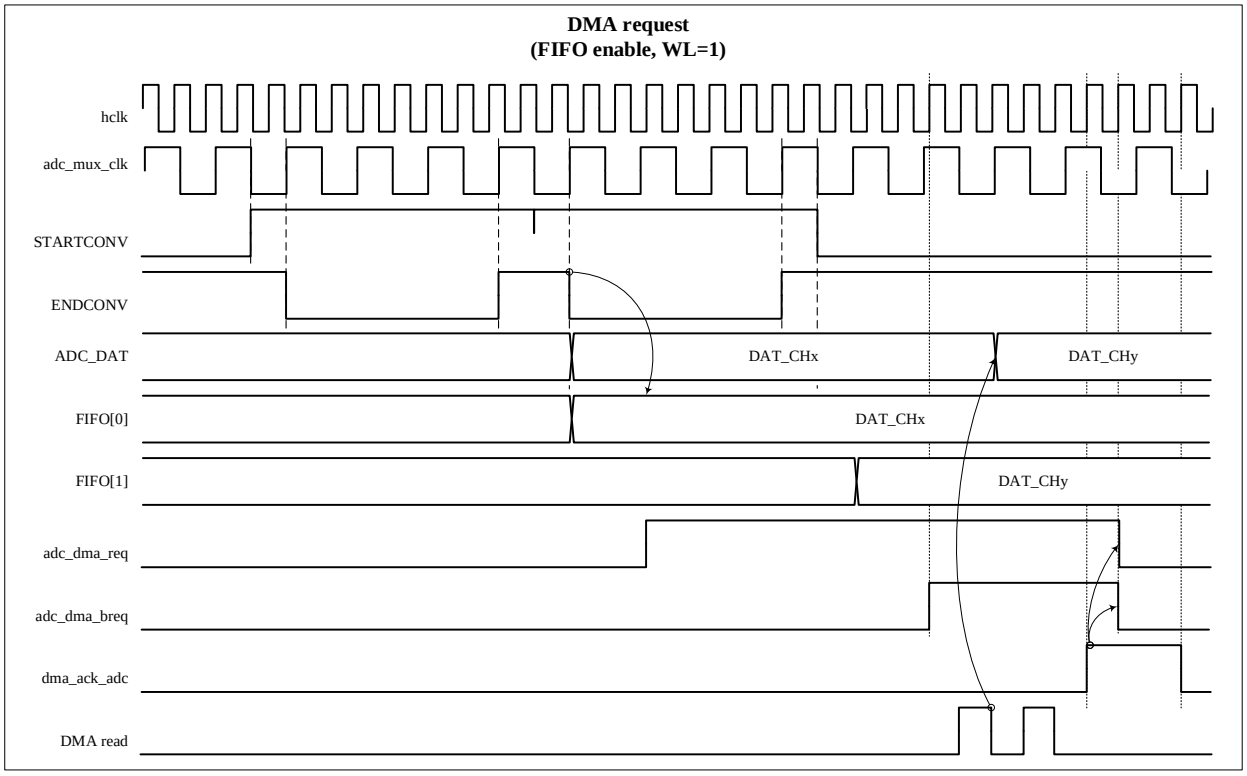


Figure 26-45 DMA request (FIFO enable)



Note:

1. DMA request signals (dma_req/breq) can be terminated when SWRSTOP=1, or ON=0, even the DMA acknowledge (dma_ack) has NOT returned.

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2. Use DMNGT and DMAMD(Multi-adc DMA) to enable and control DMA:

- DMNGT=11: enable DMA

- DMAMD=00: DMA request is generated on each separated ADC

DMAMD=01: DMA request is only on ADC1(master), after each one data item available (ADC1->ADC2->ADC3)

This mode is only used for modes: dual regular simultaneous, triple regular simultaneous (MULTMODE= 00110, 10110)

DMAMD=10: DMA request is only generated on ADC1(master), after each two data items available (ADC1+ADC2 -> ADC3+ADC1 -> ADC2+ADC3)

This mode is only used for modes: dual regular interleave, triple regular interleave, dual regular simultaneous (MULTMODE= 00111, 10111, 00110)

- In multi-adc mode:

+ DMNGT is valid on master only (ADC1). The DMNGT value on master is applied to slaves (DMNGT on slaves are don't care).

+ DMAMD is only valid on ADC1 (set DMAMD on ADC2,3 is not effective)

+ When DMAMD=01 or 10, user must set DMNGT=11 for both ADC1,2 (dual), or all ADC1,2,3 (triple)

+ When DMAMD=01 or 10, if using FIFO mode, only FIFO of ADC1 is used.

+ When DMAMD=01 or 10, user must take responsibility to calculate sample time/interleave delay value to ensure DMA have sufficient time to serve.

3. ENDCA flag is auto cleared after each DMA reading the ADC_DAT data.

In multi-adc mode, ENDCA flag of ADC2 or ADC3 can be also auto cleared when its corresponding data is read.

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26.10.3.1 DMA requests in multi-ADC mode

Figure 26-46 DMA request (DMAMD= 01)

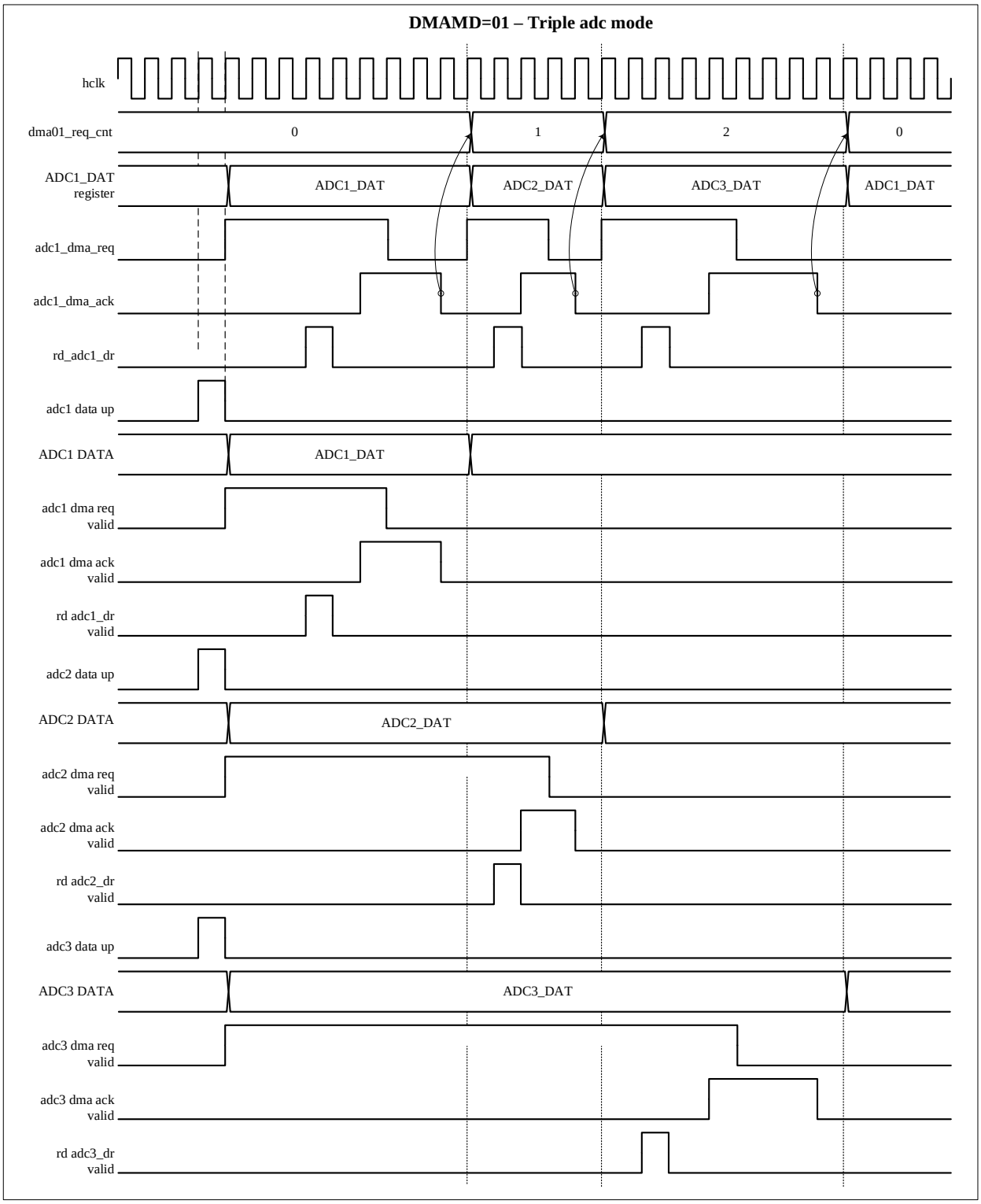

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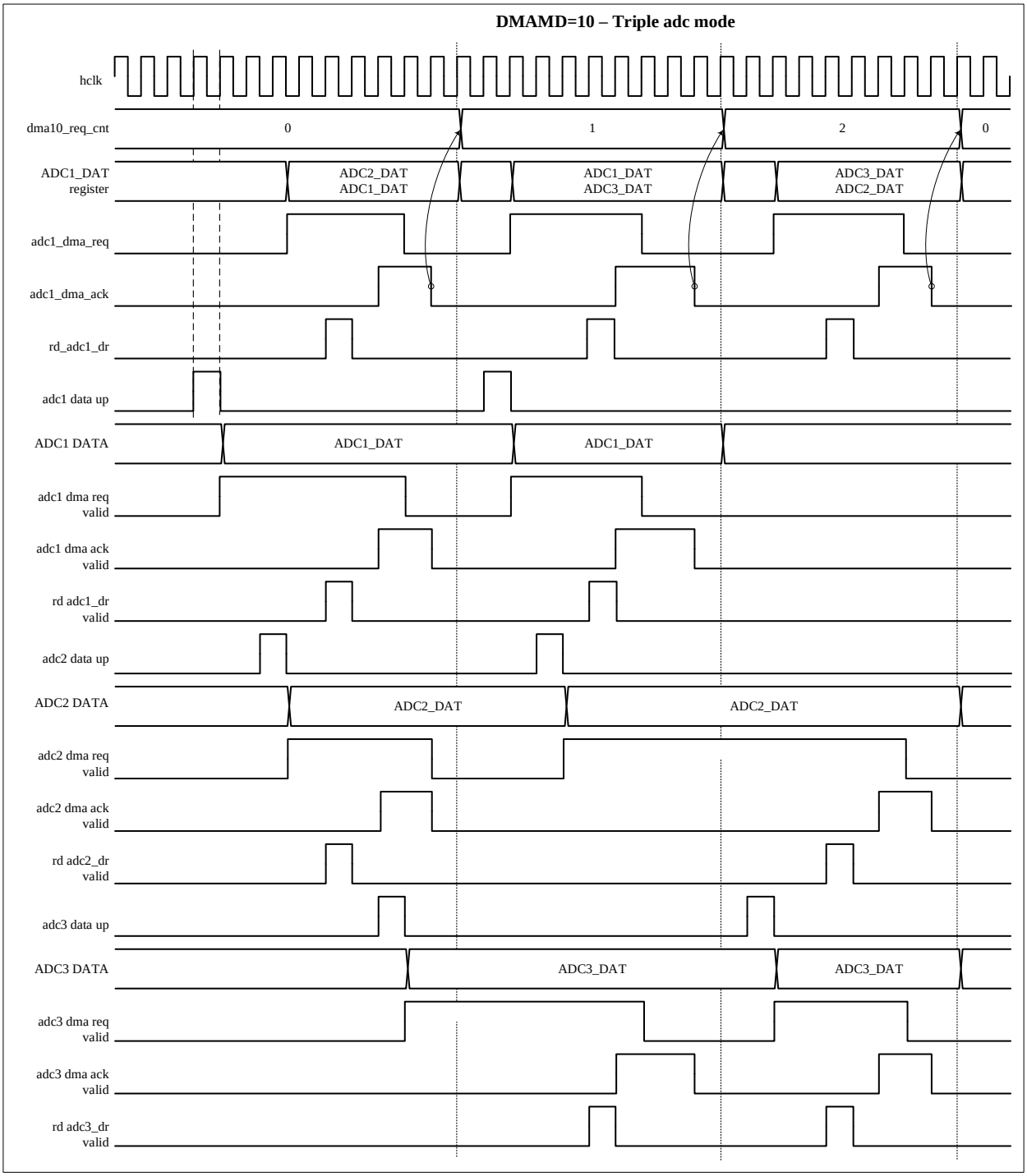
Figure 26-47 DMA request (DMAMD= 10)



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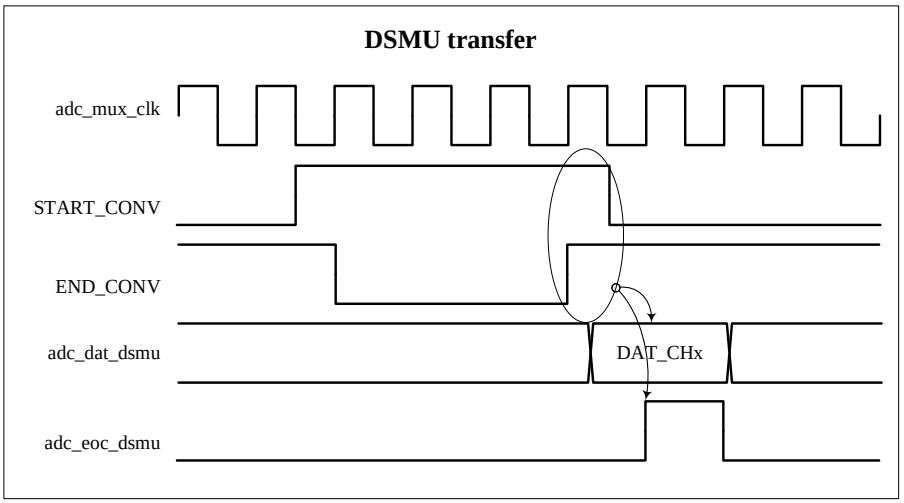
26.10.3.2 Manage data with DSMU (regular only)

Figure 26-48 DSMU transfer



Note:

1. Use DMNGT and MDSMU(Multi-adc DSMU) to enable and control DMA:

- DMNGT=10 => enable DSMU mode

- MDSMU=0: DSMU transfer is performed on each individual ADC

MDSMU=1: DSMU transfer is performed only on ADC1(master), after each one data item available (ADC1->ADC2->ADC3)

This mode is only used for modes: dual regular interleave, triple regular interleave (MULTMODE= 00111, 10111)

- In multi-adc mode:

+ DMNGT is valid on master only (ADC1). The DMNGT value on master is applied to slaves (DMNGT on slaves are don't care).

+ MDSMU is only valid on ADC1 (set DMAMD on ADC2,3 is not effective), and valid only for dual/triple mode

+ When MDSMU=1, user must set DMNGT=10 for both ADC1,2 (dual), or all ADC1,2,3 (triple)

+ When MDSMU=1, user must take responsibility to calculate sample time/interleave delay value to ensure DSMU transfer has sufficient time to process.

2. EOC flag is auto cleared after each adc_eoc_dsmu pulse.

In multi-adc mode, ENDCA flag of ADC2 or ADC3 can be also auto cleared when its data is transferred.

3. DSMU mode is used only for regular data conversion (i.e., injected data conversion if any will NOT be transferred to DSMU)

4. FIFO is NOT used for DSMU mode

5. To ensure the data format provided to DSMU is 16-bit signed, oversample must be disabled in DSMU mode.

7. When DSMU mode used (DMNGT=10), the data is still stored to ADC_DAT, however:

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- Not handle overrun/underrun when store data to ADC_DAT: Updating ADC_DAT or read ADC_DAT doens't assert WEFLAG/REFLAG flags

** WEFLAG/UNDRRUN is just used to indicate the data status which is transferred o DSMU*

- Not handle to clear ENDCA flag when read ADC_DAT

** ENDCA flag is auto-cleared only when the data was transfered to DSMU (adc_eoc_dsmu is asserted)*

- The data register is overwritten with the last conversion result and the previous unread data is lost.

ADC_DAT internal buffer or FIFO is disabled.

*Any further conversion is performed normally and the ADC_DAT register always contains the latest converted data. * This behavior is same as OVRMOD=1*

- Data is stored to each ADC_DAT separately, even when multi-adc mode and MDSMU=1.

8. When DSMU mode used (DMNGT=10), the analog watchdog functionality (AWD) is maintained as normal.

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26.10.3.3 DSMU transfer in multi-ADC mode

Figure 26-49 DSMU transfer in dual-ADC mode

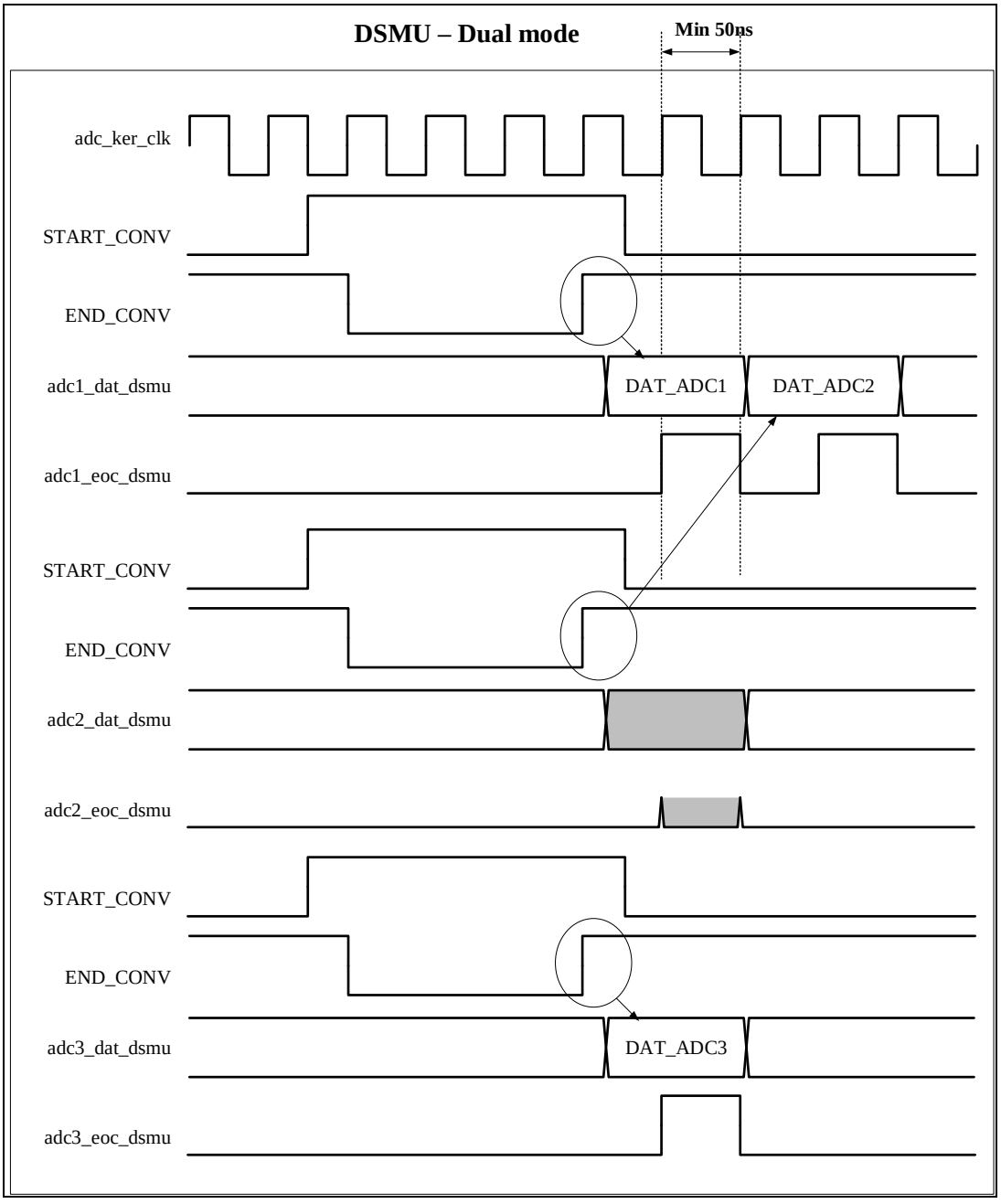

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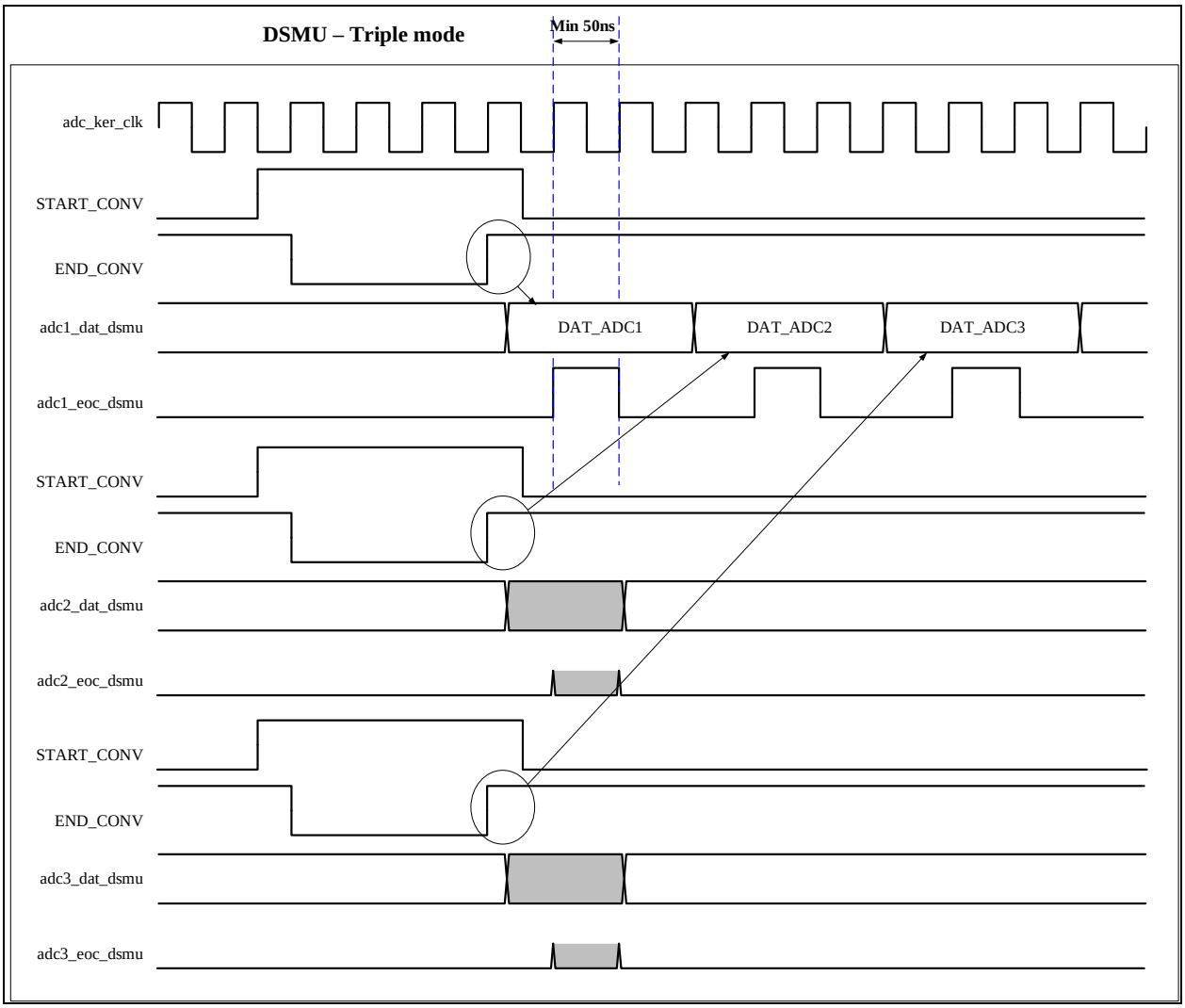
Figure 26-50 DSMU transfer in triple-ADC mode



26.10.4 Overrun/Underrun detection (regular only)

The overrun flag (WEFLAG) notifies of that a buffer overrun event occurred when the regular converted data has not been read (by the CPU or the DMA, or the DSMU) before new converted data became available. If this case occurs, the WEFLAG flag is set. An interrupt can be generated if bit WEIEN = 1.

The underrun flag (REFLAG) notifies of that there is a read (by the CPU or the DMA, or the DSMU) while data buffer is empty. If this case occurs, the REFLAG flag is set. An interrupt can be generated if bit REIEN = 1.

When an overrun condition occurs, the ADC is still operating and can continue converting unless the software decides to stop and reset the sequence by setting bit SWRSTOP = 1.

WEFLAG/REFLAG flags are cleared by software by writing 1 to each bit respectively.

It is possible to configure if data is preserved or overwritten when an overrun event occurs by programming the control bit OVRMOD:

- OVRMOD = 0:

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The overrun event preserves the data register from being overwritten: the old data is maintained up to ADC_DAT FIFO depth (if EN=1) and the new conversion is discarded and lost. If OVR remains at 1, any further conversion is be performed but the resulting data is also dicarded.

- OVRMOD = 1:

The data register is overwritten with the last conversion result and the previous unread data is lost. In this mode, ADC_DAT FIFO is disabled regardless of EN setting. If OVR remains at 1, any further conversion is performed normally and the ADC_DAT register always contains the latest converted data.

Note: There is no overrun detection on the injected channels since there is a dedicated data register for each of the four injected channels.

26.10.5 Clear data

The conversion data is cleared in one of below cases:

1. Read ADC_DAT register if DMNGT=00 or 1.

   If buffer or FIFO is used, it clears one element of data in order.

2. adc_dsmu_eoc is asserted (indicate DSMU transfer occurred) if DMNGT=10

   If buffer or FIFO is used, it clears one element of data in order.

3. Write 1 to CLR bit

   It clears all data buffer or FIFO.

4. Reset ADCCTRL (DMSU mode: adc kernel reset, other modes: AHB reset)

   It clears all data buffer or FIFO

5. Write 1 to ADC_CTRL3.RSTART to start new conversion sequence.

   It clears all data buffer or FIFO.

Note: Stop conversion (auto-clear or SWRSTOP command) does not clear data.

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26.11 Analog watchdog

The three AWD analog watchdogs monitor whether some channels remain within a configured voltage range.

26.11.1 AWDx flag and interrupt

An interrupt can be enabled for each of the 3 analog watchdogs by setting AWDxIE (x = 1,2,3).

AWDx (x = 1,2,3) flag is cleared by software by writing 1 to it.

The ADC conversion result is compared to the lower and higher thresholds beforealignment.

26.11.2 Analog watchdog 1

The AWD analog watchdog 1 is enabled by setting the AWD1ERCH bit. This watchdog monitors whether either one selected channel or all enabled channels (1) remain within a configured voltage range (window).

The AWD1 analog watchdog status bit is set if the analog voltage converted by the ADC is below a lower threshold or above a higher threshold.

Analog Watchdog Filter is used only in this case: AWD1ERCH/AWD1EJCH = 1, and AWD1SGLEN=1, user can use Single mode (one-shot) or SCANMD mode with LEN/JLEN=any.

When Analog Watchdog Filter is used, it just affects to AWDx flag. EOC flag, DMA request, ADC_DAT and AWDx_ADCy_OUT are NOT affected by this filter.

26.11.3 Analog watchdog 2,3

The second and third analog watchdogs are more flexible and can guard several selected channels by programming the corresponding bits in AWDxCH[18:0] (x=2,3).

The corresponding watchdog is enabled when any bit of AWDxCH[18:0] (x=2,3) is set.

26.11.4 ADCy_AWDx_OUT signal output generation

Each analog watchdog is associated to an internal hardware signal ADCy_AWDx_OUT (y=ADC number, x=watchdog number) which is directly connected to the external trigger input of some on-chip timers.

ADCy_AWDx_OUT is activated when the associated analog watchdog is enabled:

- ADCy_AWDx_OUT is set when a guarded conversion is outside the programmed thresholds.
- ADCy_AWDx_OUT is reset after the end of the next guarded conversion which is inside the programmed thresholds (It remains at 1 if the next guarded conversions are still outside the programmed thresholds).
- ADCy_AWDx_OUT is also reset when disabling the ADC (when setting ON = 0).

Note that stopping regular or injected conversions (setting SWRSTOP = 1 or SWJSTOP = 1) has no influence on the generation of ADCy_AWDx_OUT.

Note: AWDx flag is set by hardware and reset by software: AWDx flag has no influence on the generation of

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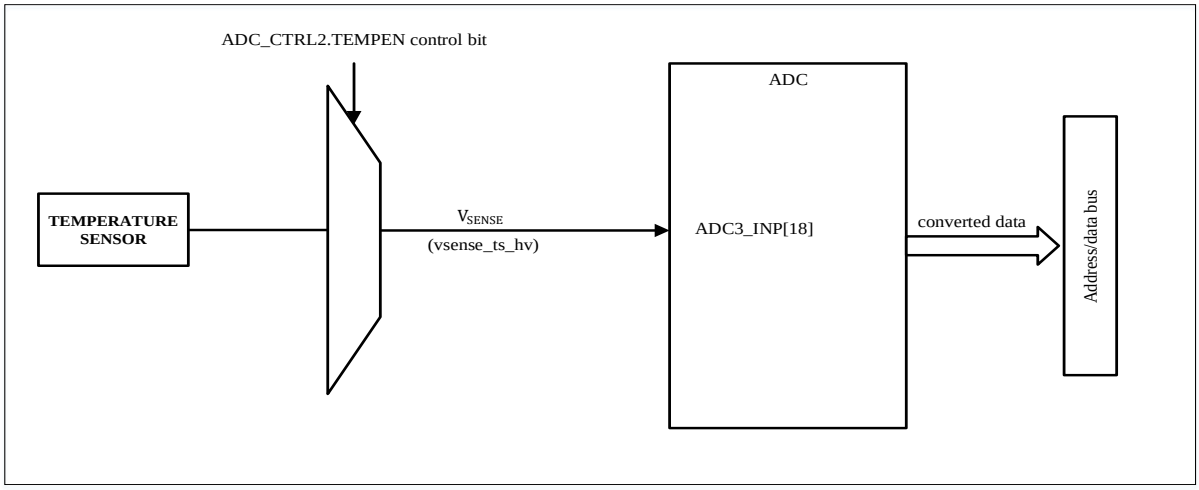
ADCy_AWDx_OUT (ex: ADCy_AWDx_OUT can toggle while AWDx flag remains at 1 if the software did not clear the flag).

26.12 Temperature Sensor

Set the ADC_CTRL2.TEMPEN bit to 1 to enable the temperature sensor, and use the temperature sensor to detect the ambient temperature when the device is operating. The output voltage sampled by the temperature sensor is converted into a digital value by the ADC3_INP[18] channel. When the temperature sensor is working, the ideal sampling time is 17.1us; when the temperature sensor is not working, the ADC_CTR2.TEMPEN bit can be cleared by software to reduce power consumption. As follows Figure 26-51 Temperature Sensor Channel Diagramis a block diagram of a temperature sensor.

The output voltage of the temperature sensor changes linearly with temperature. Different chips will have different offsets in the temperature curve due to different production processes. Through testing, it is found that the maximum offset is 3°C. This characteristic makes the internal temperature sensor more suitable for detecting temperature changes. Not suitable for measuring absolute temperature. When accurate temperature measurement is required, an external temperature sensor should be used.

Figure 26-51 Temperature Sensor Channel Diagram



26.12.1 Measure Temperature Values

1. Configure the channel (ADC3 INP[18]) and sampling time of the channel to be 17.1 us.
2. Set ADC_CTRL2.TEMPEN bit to 1 to enable temperature sensor.
3. Set ADC_CTRL2.ON bit to 1 to start ADC conversion (or through external trigger).
4. Read the temperature data in the ADC data register, and calculate the temperature value by the following formula：

$$Temperature(°C) = \{(V_{Temperature} - V_{SENSE}) / Avg_Slope\} + Temperature - T_{offset}$$

In which：

$V_{Temperature}$ = Temperature corresponding to the V_{SENSE}

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Avg_Slope ＝ temperature and Average slope of a V_{SENSE} curve (mV/°C or μV/°C)

T_{offset} = 1.25°C, Representation of empirical temperature error compensation（°C）

Temperature is the calibrated temperature.

The actual value of Avg_Slope in the electrical characteristics section of the reference data sheet.

Note：

1. *There is a settling time from power-down mode to the correct output VSENSE of the sensor; there is also a settling time after the ADC is powered on. Therefore, to reduce the delay, both the ADC_CTRL2.TEMPEN and ADC_CTRL2.ON bits should be set simultaneously.*
2. *This temperature is the junction temperature of the chip, which can differ significantly from the ambient temperature of the chip*

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26.13 Interrupt

For each ADC, an interrupt can be generated associated to a status register bit. Table 26-12 lists of supported interrupts. All they are level type. Separate interrupt enable bits are available for flexibility.

Table 26-12 List of interrupts

Interrupt description	Interrupt flag	Enable control bit
Regular data overrun	WEFLAG	WEIEN
Regular data underrun	REFLAG	REIEN
End of sampling	EOSAMP	EOSMPIEN
ADC Power-down ready	PDRDYFLAG	PDRDYIEN
ADC Ready	RDYFLAG	RDYIEN
Analog Watchdog 1 is set	AWDG1	AWD1IE
Analog Watchdog 2 is set	AWD2FLAG	AWD2INTEN
Analog Watchdog 3 is set	AWD3FLAG	AWD3INTEN
End of each conversion of injected group	JENDCA	JENDCAIEN
End of sequence of conversions of injected group	JENDC	JENDCIEN
End of each conversion of regular group	ENDCA	ENDCAIEN
End of sequence of conversions of regular group	ENDC	ENDCIEN
FIFO full (regular only)	FFLAG	FINTEN
FIFO half full (regular only)	HFFLAG	HFINTEN
FIFO not empty (regular only)	NEFLAG	NEINTEN
FIFO empty (regular only)	EFLAG	EINTEN

Some other flags are present in the ADC_STS register, but there is no interrupt associated with them:

- JSTR (Start of conversion of an injected group's sequence)
- STR (Start of conversion of a regular group's sequence)
- ROSOVFDSMU (Regular oversample overflow 15-bit data in DSMU mode)
- ROSOVF (Regular oversample overflow 16-bit data)
- JOSOVF (Injected oversample overflow 16-bit data)

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26.14 Registers

26.14.1.1 ADC Status Register (ADC_STS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														WEFLAG	REFLAG
														rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ROSOVFDSMU	JOSOVF	ROSOVF	EOSAMP	Reserved	PDRDYF	RDYF	Reserved	AWDG1	STR	JENDCA	JENDC	JSTR	ENDCA	ENDC
	rc_w1	rc_w1	rc_w1	rc_w1		rc_w1	rc_w1		rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	WEFLAG	FIFO write error status It is set to 1 by hardware, and writing 1 clears it by software. 0: No write error occurred 1: Write error occurred
16	REFLAG	FIFO read error status It is set to 1 by hardware, and writing 1 clears it by software. 0: No read error occurred 1: Read error occurred
15	Reserved	Reserved, the reset value must be maintained
14	ROSOVFDSMU	Regular oversample data overflow 15-bit in DSMU mode This bit is set by hardware when regular oversample is enabled (ADC_OSCFG.OSRE=1, DSMU mode (ADC_CTRL3.DMNGT=10) and calculated oversample data is over 15-bit 0: No overflow occurred 1: Overflow occurred
13	JOSOVF	Injected oversample data overflow 16-bit This bit is set by hardware when injected oversample is enabled (ADC_OSCFG.OSJE=1) and calculated oversample data is over 16-bit (the apart higher than 16-bit is truncated): 0: No overflow occurred 1: Overflow occurred

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12	ROSOVF	Regular oversample data overflow 16-bit This bit is set by hardware when regular oversample is enabled (ADC_OSCFG.OSRE=1) and calculated oversample data is over 16-bit (the apart higher than 16-bit is truncated): 0: No overflow occurred 1: Overflow occurred
11	EOSAMP	Regular channel sample end flag When the regular channel sampling is completed, this bit is set to 1 by hardware and cleared by software writing 1. 0: Regular channel sampling not completed； 1: Regular channel sampling completed.
10	Reserved	Reserved, the reset value must be maintained
9	PDRDYF	Power down ready This bit is set by hardware after ON=L and the controller has ended the operation. It is cleared by software. 0: ADC controller is in operation. 1: ADC controller is in power-down.
8	RDYF	ADC operation ready flag This bit is set by hardware after ON=H and the controller and ADC IP is ready. User can read this bit to start conversion. It is cleared by software. 0: ADC not ready 1: ADC ready.
7	Reserved	Reserved, the reset value must be maintained
6	AWDG1	Analog watchdog 1 flag When the converted voltage value exceeds the range defined by the ADC_AWD1HIGH.HTH and ADC_AWD1LOW.LTH registers, this bit is set to 1 by hardware and cleared by software writing 1. 0: No analog watchdog event occurred; 1: Analog watchdog event occurred.
5	STR	Regular channel start flag When the regular channel conversion starts, this bit is set to 1 by hardware and cleared by software writing 1. 0: Regular channel conversion not started; 1: Regular channel conversion started.
4	JENDCA	Any injected channel end of conversion Set to1 by hardware when the any injection channel sequence conversion ends, cleared by software writing 1. 0: Conversion not completed; 1: Conversion completed.

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3	JENDC	Injected channel end of conversion Set to 1 by hardware when the injection channel sequence conversion ends, cleared by software writing 1. 0: The injection channel sequence conversion not completed; 1: The injection channel sequence conversion completed.
2	JSTR	Inject channel start flag When the injection channel conversion starts, this bit is set to 1 by hardware and cleared by software writing 1. 0: Injection channel conversion not started; 1: Injection channel conversion started.
1	ENDCA	Any end of conversion flag Set to 1 by hardware when any regular channel conversion ends, cleared by software writing 1. 0: Conversion not completed; 1: Conversion completed.
0	ENDC	End of conversion Set to 1 by hardware when the regular channel sequence conversion ends, cleared by software writing 1. 0: Conversion not completed; 1: Conversion completed.

26.14.1.2 ADC Control Register 1 (ADC_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	WEIEN	REIEN	EOSMP IEN	PDRDY IEN	RDYIEN	Reserved	DJCH	DREGCH	AWD1 ERCH	AWD1 EJCH	AWD1CH[4:0]				
	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTMODE[4:0]					DCTU[2:0]			AUTOJC	AWD1 SGLEN	AWD1IEN	JENDC IEN	JENDCA IEN	ENDC IEN	ENDCA IEN	SCANMD
rw					rw			rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained
30	WEIEN	FIFO write error interrupt enable This bit is set and cleared by software. 0: Disable 1: Enable

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29	REIEN	FIFO read error interrupt enable This bit is set and cleared by software. 0: Disable 1: Enable
28	EOSMPIEN	ADC sample done interrupt enable This bit is set and cleared by software. 0: Disable ADC sampling complete interrupt; 1: Enable ADC sampling complete interrupt.
27	PDRDYIEN	ADC Power down ready interrupt enable This bit is set and cleared by software. 0: Disable ADC power down ready interrupt; 1: Enable ADC power down ready interrupt.
26	RDYIEN	ADC Ready interrupt enable This bit is set and cleared by software. 0: Disable ADC ready interrupt; 1: Enable ADC ready interrupt.
25	Reserved	Reserved, the reset value must be maintained
24	DJCH	Discontinuous mode on injected channels This bit is set and cleared by software to enable or disable discontinuous mode on the injection channel group 0: Disable discontinuous mode on the injection channel group； 1: Use discontinuous mode on the injection channel group.
23	DREGCH	Discontinuous mode on regular channels This bit is set and cleared by software to enable or disable discontinuous mode on the regular channel group. 0: Disable discontinuous mode on the regular channel group; 1: Use discontinuous mode on the regular channel group.
22	AWD1ERCH	Analog watchdog 1 enable on regular channels This bit is set and cleared by software. 0: Disable Analog Watchdog 1 on the regular channel; 1: Using Analog Watchdog 1 on the regular channel.
21	AWD1EJCH	Analog watchdog 1 enable on injected channels This bit is set and cleared by software. 0: Disable Analog Watchdog 1 on the injected channel; 1: Using Analog Watchdog 1 on the injected channel.

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20:16	AWD1CH[4:0]	Analog watchdog channel selection bits These bits are set and cleared by software to select the input channels protected by Analog Watchdog 1. 00000: ADC analog input channel 0; 00001: ADC analog input channel 1; …… 10000: ADC analog input channel 16; 10001: ADC analog input channel 17; 10010: ADC analog input channel 18; 10011: ADC analog input channel 19; Other: Reserved
15:11	MULTMODE[4:0]	Multi-ADC mode selection 00001 – 01001: Dual ADC operating mode (ADC1 and ADC2, ADC3 is independent) 00000: Independent mode 00001: Combined synchronous regular + synchronous injection mode 00010: Combined synchronous regular + alternate trigger mode 00011: Combined synchronous injection + interleaved mode 00100: Reserved 00101: Synchronous injection mode 00110: Synchronous regular mode 00111: Interleaved mode 01000: Reserved 01001: Alternate Trigger mode 10001 – 11001: Triple ADC operating mode(ADC1，ADC2 and ADC3) 10001: Combined synchronous regular + synchronous injection mode 10010: Combined synchronous regular + alternate trigger mode 10011: Combined synchronous injection + interleaved mode 10100: Reserved 10101: Synchronous injection mode 10110: Synchronous regular mode 10111: Interleaved mode 11000: Reserved 11001: Alternate Trigger mode *Note：* *1. In the slave ADC, these bits should be configured the same as ADC1;* *2. In dual ADC or triple ADC mode, changing the channel configuration will result in a condition that triggers a restart, causing synchronization loss. It is recommended to disable the dual ADC or triple ADC mode before making any configuration changes.*

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10:8	DCTU[2:0]	Discontinuous mode channel count Software defines the number of regular channel conversions to be performed after receiving an external trigger in discontinuous mode using these bits. 000: 1 channel 001: 2 channels …… 111: 8 channels
7	AUTOJC	Automatic injected group conversion This bit is set and cleared by software to enable or disable the injected channel sequence conversion after the regular channel sequence conversion ends. 0: Disable automatic injection channel sequence conversion； 1: Enable automatic injection channel sequence conversion.
6	AWD1SGLEN	Enable the watchdog 1 on a single channel in scan mode This bit is set and cleared by software to enable the Analog Watchdog 1 function on the channels specified by ADC_CTRL1_AWD1CH[4:0] or enable the Analog Watchdog 1 function on all channels. 0: Using Analog watchdog 1 on all channels; 1: Using Analog watchdog 1 on a single channel.
5	AWD1IEN	Analog watchdog 1 interrupt enable This bit is set and cleared by software to disable or enable the generation of an interrupt by Analog Watchdog 1. In scan mode, if Watchdog 1 detects an out-of-range value, the scan will be aborted only when this bit is set. 0: Disable Analog Watchdog 1 interrupt; 1: Enable Analog Watchdog 1 interrupt.
4	JENDCIEN	Interrupt enable for injection channels This bit is set and cleared by software to disable or enable the interrupt after all injection channel conversions are completed. 0: Disable ADC_STS.JENDC interrupt; 1: Enable ADC_STS.JENDC interrupt.
3	JENDCAIEN	Injected channel end of conversion Set to 1 by hardware when the injection channel sequence conversion ends, cleared by software writing 1. 0: The injection channel sequence conversion not completed; 1: The injection channel sequence conversion completed.
2	ENDCIEN	Interrupt enable for ENDC This bit is set and cleared by software to disable or enable the interrupt that occurs after a regular conversion sequence is completed. 0: Disable ADC_STS.ENDC interrupt; 1: Enable ADC_STS.ENDC interrupt.

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1	ENDCAIEN	Interrupt enable for any regular channels This bit is set and cleared by software to enable/disable the end of conversion interrupt for any regular channel. 0: Disable ADC_STS.ENDCA interrupt; 1: Enable ADC_STS.ENDCA interrupt.
0	SCANMD	Scan mode This bit is set and cleared by software to enable or disable scan mode. In scan mode, conversions are performed on the channels selected by the ADC_RSEQx or ADC_JSEQ registers. 0: Disable scan mode; 1: Enable scan mode. *Note: If only the ADC_CTRL1.ENDCIEN or ADC_CTRL1.JENDCIEN bit is set, the ADC_STS.ENDC or ADC_STS.JENDC interrupt occurs only after the last channel conversion.*

26.14.1.3 ADC Control Register 2 (ADC_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXTPRSEL[1:0]		EXTRSEL[5:0]						TEMPEN	SWSTRCH	SWSTRJCH	Reserved		EXTJSEL[5:3]		
rw		rw						rw	rw	rw			rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTJSEL[2:0]			Reserved	ALIG	EXTPJSEL[1:0]		DMAMD[1:0]		MDSMU	DMNGT[1:0]		Reserved	ENCAL	CTU	ON
rw				rw	rw		rw		rw	rw			rw	rw	rw

Bit field	Name	Description
31:30	EXTPRSEL[1:0]	External trigger enable and polarity selection for regular channels 00: External trigger detection disabled (user can only trigger ADC conversion through software) 01: Detection of rising edge of external trigger as a valid trigger 10: Detection of falling edge of external trigger as a valid trigger 11: Detection of both rising and falling edges of the external trigger as valid triggers
29:24	EXTRSEL[5:0]	External event select for regular group These bits select the external event used to trigger the regular sequence conversion. ADC trigger configuration: 000000: ATIM1 CC1 event 000001: ATIM1 CC2 event

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Bit field	Name	Description
		000010: ATIM1 CC3 event 000011: ATIM1 CC4 event 000100: ATIM1 TRGO event 000101: ATIM2 CC1 event 000110: ATIM2 CC2 event 000111: ATIM2 CC3 event 001000: ATIM1 TRGO2 event 001001: ATIM2 TRGO event 001010: ATIM3 CC1 event 001011: ATIM3 CC2 event 001100: ATIM3 CC3 event 001101: ATIM3 CC4 event 001110: ATIM2 TRGO2 event 001111: ATIM3 TRGO event 010000: ATIM4 TRGO2 event 010001: ATIM3 TRGO2 event 010010: ATIM4 TRGO event 010011: GTIMB1 TRGO event 010100: GTIMB2 TRGO event 010101: GTIMB3 TRGO event 010110: GTIMA1 TRGO event 010111: GTIMB1 CC2 event 011000: GTIMB2 CC4 event 011001: GTIMB3 CC2 event 011010: GTIMA1 CC4 event 011011: SHRTIM1 TRG1 event 011100: SHRTIM1 TRG3 event 011101: SHRTIM2 TRG1 event 011110: SHRTIM2 TRG3 event 011111: EXTI line 0~15 event
23	TEMPEN	Temperature sensor enable This bit is set and cleared by software to enable or disable the temperature sensor channel. This bit is available only in ADC1 and ignored in ADC2 and ADC3: 0: Disable temperature sensor channel measurement 1: Enable temperature sensor channel measurement
22	SWSTRRCH	Start conversion of regular channels This bit is set by software to start the conversion, and is cleared by hardware after the conversion begins. This bit is used to start a group of regular channel conversions. 0: Reset state; 1: Start conversion of regular channels.
21	SWSTRJCH	Start conversion of injection channels

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Bit field	Name	Description
		This bit is set by software to start the conversion and can be cleared immediately by software or hardware after the conversion begins. This bit is used to start a group of injection channel conversions. 0: Reset state; 1: Start conversion of injection channels.
20:19	Reserved	Reserved, the reset value must be maintained
18:13	EXTJSEL[5:0]	External event select for injected group These bits select the external event used to trigger the injection sequence conversion. ADC trigger configuration: 000000: ATIM1 CC1 event 000001: ATIM1 CC2 event 000010: ATIM1 CC3 event 000011: ATIM1 CC4 event 000100: ATIM1 TRGO event 000101: ATIM2 CC1 event 000110: ATIM2 CC2 event 000111: ATIM2 CC3 event 001000: ATIM1 TRGO2 event 001001: ATIM2 TRGO event 001010: ATIM3 CC1 event 001011: ATIM3 CC2 event 001100: ATIM3 CC3 event 001101: ATIM3 CC4 event 001110: ATIM2 TRGO2 event 001111: ATIM3 TRGO event 010000: ATIM4 TRGO2 event 010001: ATIM3 TRGO2 event 010010: ATIM4 TRGO event 010011: GTIMB1 TRGO event 010100: GTIMB2 TRGO event 010101: GTIMB3 TRGO event 010110: GTIMA1 TRGO event 010111: GTIMB1 CC1 event 011000: GTIMB2 CC4 event 011001: GTIMB3 CC1 event 011010: GTIMA1 CC3 event 011011: SHRTIM1 TRG2 event 011100: SHRTIM1 TRG4 event 011101: SHRTIM2 TRG2 event 011110: SHRTIM2 TRG4 event 011111: EXTI line 0~15 event
12	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
11	ALIG	Data alignment This bit is set and cleared by software. 0: Right-aligned; 1: Left-aligned.
10:9	EXTPJSEL[1:0]	External trigger enable and polarity selection for injected channels 00：External trigger detection disabled (the user can only trigger ADC conversion through software) 01: Detection of rising edge of external trigger as valid trigger 10: Detection of falling edge of external trigger as valid trigger 11: Detection of both rising and falling edges of external trigger as valid trigger
8:7	DMAMD[1:0]	DMA mode This bit is set and cleared by software to configure the DMA operating mode. 00: DMA mode 0, disable DMA 01: DMA mode 1 (transfers half a word per DMA request. The order of transfers for multiple ADCs is ADC1, ADC2, ADC3, ADC1, ADC2.....) 10: DMA mode 2 (transfers one word per DMA request. The sequence is ADC2|ADC1, ADC1& ADC3, ADC3& ADC2) 11: Reserved *Note：* *1. For single ADC, only DMA mode 0 and mode 1 are supported；* *2. For multiple ADCs, DMA mode 1, mode 2, and mode 3 are supported；* *3. Only ADC1 can generate DMA requests;* *4, This bit is valid only when ADC_CTRL2.DMNGT= 0b11*
6	MDSMU	Multi-adc DSMU mode These bits are set and cleared by software. These bits are valid only in master ADC1 when multi-adc mode (ADC2, ADC3: don't care). These bits are effective only when ADC_CTRL2.DMNGT[1:0] = 0b10. 0: Multi-adc DSMU mode disabled. DSMU data management can be independently performed on each individual ADC, if ADC_CTRL2.DMNGT[1:0] = 0b10 set on each ADC respectively. 1: Multi-adc DSMU mode enabled **Dual mode:** DSMU data management performed on ADC1 and ADC3, if ADC_CTRL2.DMNGT[1:0] = 0b10, set on ADC1 (ADC2: don't care) and ADC3 respectively. **Triple mode:** DSMU data management performed on ADC1 if ADC_CTRL2.DMNGT[1:0] = 0b10, set on ADC1 (ADC2,3: don't care) *Note:When multi-adc DSMU mode is enable in regular interleave, the ADC_DLYSMP.INTLEADVAL[3:0] must be set mininum delay 2-cycle.*
5:4	DMNGT	Data management configuration for regular conversion data This bit is set and cleared by software to select how ADC interface output data are managed. 00: Regular conversion data stored in ADC_DAT register only

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Bit field	Name	Description
		01: Reserved 10: DSMU mode selected 11: DMA Mode selected When multi-adc, only DMNGT[1:0] of master is valid.
3	Reserved	Reserved, the reset value must be maintained
2	ENCAL	A/D Calibration This bit is set by software to start calibration and is cleared by hardware when calibration is completed. 0: Calibration completed; 1: Start calibration.
1	CTU	Continuous conversion This bit is set and cleared by software. If this bit is set, the conversion will continue until the bit is cleared. 0: Single conversion mode; 1: Continuous conversion mode.
0	ON	A/D converter ON/OFF This bit is set and cleared by software. When this bit is '0', writing '1' will wake up the ADC from power-down mode, enabling the ADC. When RDY is '1', it indicates that the ADC conversion is ready. 0: Turn off ADC conversion and enter power-down mode; 1: Start ADC.

26.14.1.4 ADC Control Register 3 (ADC_CTRL3)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		GCOMPSATEN	GCOMPEN	SWJSTOP	SWRSTOP	JSTART	RSTART	Reserved							
		rw	rw	rs	rs	rs	rs								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						VBATMEN	VREFINTEN	BPCAL	PDRDY	RDY	CKMOD	Reserved		RES	Reserved
						rw	rw	rw	rc_w1	rc_w1	rw			rw	

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29	GCOMPSATEN	Gain compensation saturation enable This bit is set and cleared by software to extend the saturation range when gain compensation enabled.

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Bit field	Name	Description
		This bit is used only when gain, offset compensation enabled and SATEN=1: 0: Saturation range is max 0x0-0xFFF (12-bit) 1: Saturation range is max 0x0-0x3FFF (14-bit) Note: The software is allowed to write this bit only when ADC_CTRL3.RSTART = 0 (which ensures that no conversion is ongoing).
28	GCOMPEN	Gain compensation mode This bit is set and cleared by software to enable or disable the gain compensation mode. 0: Do not enable gain compensation mode; 1: Use gain compensation mode.
27	SWJSTOP	Stop conversion of injection channels This bit is set by software to stop the ongoing conversion of injection channels. After stopping, the user can reconfigure the conversion sequence, trigger source, etc. This bit is cleared by hardware. 0: Reset state; 1: Stop conversion of injection channels.
26	SWRSTOP	Stop conversion of regular channels This bit is set by software to stop the ongoing conversion of regular channels. After stopping, the user can reconfigure the conversion sequence, trigger source, etc. This bit is cleared by hardware. 0: Reset state; 1: Stop conversion of regular channels.
	JSTART	ADC start of injected conversion This bit is set by software to start ADC conversion of injected channels. It is cleared by hardware after the execution of the ADC_CTRL3.SWJSTOP command, at the same time that ADC_CTRL3.SWJSTOP is cleared by hardware. 0: No ADC injected conversion is ongoing. 1: Write 1 to start injected conversions. Read 1 means that the ADC is operating and eventually converting an injected channel. *Note:* *1. Only when ADC_CTRL2.ON= 1, the software is allowed to set ADC_CTRL3.SWJSTART;* *2.In auto-injection mode (ADC_CTRL2.JAUTO = 1), regular and auto-injected conversions are started by setting bit ADC_CTRL3.RSTART.*
	RSTART	ADC start of regular conversion This bit is set by software to start ADC conversion of regular channels. It is cleared by hardware after the execution of the ADC_CTRL3.SWRSTOP command 0: No ADC regular conversion is ongoing. 1: Write 1 to start regular conversions. Read 1 means that the ADC is operating and eventually converting a regular channel. *Note:* *1. Only when ADC_CTRL2.ON= 1, the software is allowed to set ADC_CTRL3.SWRSTART;*

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Bit field	Name	Description
		2.In auto-injection mode (ADC_CTRL2.JAUTO = 1), regular and auto-injected conversions are started by setting bit ADC_CTRL3.RSTART.
23:10	Reserved	Reserved, the reset value must be maintained
9	VBATMEN	Vbat monitor enable； This bit is available only in ADC1 and ignored in ADC2 and ADC3: 0: Disable 1: Enable
8	VREFINTEN	Internal voltage reference enable This bit is available only in ADC1 and ignored in ADC2 and ADC3: 0: Disable Internal voltage reference channel measurement 1: Enable Internal voltage reference channel measurement
7	BPCAL	Bypass calibration 0: Disable; 1: Enable.
6	PDRDY	Power down ready This bit is set to 1 by hardware and cleared by software writing 1. 0: Not ready; 1: Ready.
5	RDY	ADC Ready This bit is set to 1 by hardware and cleared by software writing 1. 0: Not Ready; 1: Ready.
4	CKMOD	Clock Mode 0: Select AHB as the synchronous clock; 1: PLL Select PLL as the asynchronous clock.
3:2	Reserved	Reserved, the reset value must be maintained
1	RES	Data resolution This bit is set and cleared by software to select the resolution of the conversion. 0: 10 bit; 1: 12 bit.
0	Reserved	Reserved, the reset value must be maintained

26.14.1.5 ADC Sampling Time Register 1 (ADC_SAMPT1)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAMP7[3:0]				SAMP6[3:0]				SAMP5[3:0]				SAMP4[3:0]			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMP3[3:0]				SAMP2[3:0]				SAMP1[3:0]				SAMP0[3:0]			

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rw rw rw rw

Bit field	Name	Description
31:0	SAMPx[3:0]	Channel Sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bits must remain unchanged during sampling. 0000: 1 cycle 0001: 2 cycle 0010: 3 cycle 0011: 4 cycle 0100: 5 cycle 0101: 6 cycle 0110: 7 cycle 0111: 10 cycle 1000: 13 cycle 1001: 17 cycle 1010: 24 cycle 1011: 32 cycle 1100: 83 cycle 1101: 93 cycle 1110: 215 cycle 1111: 397 cycle

26.14.1.6 ADC Sampling Time Register 2 (ADC_SAMPT2)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAMP15[3:0]				SAMP14[3:0]				SAMP13[3:0]				SAMP12[3:0]			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMP11[3:0]				SAMP10[3:0]				SAMP9[3:0]				SAMP8[3:0]			
rw				rw				rw				rw			

Bit field	Name	Description
31:0	SAMPx[3:0]	Channel Sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bits must remain unchanged during sampling. 0000: 1 cycle 0001: 2 cycle

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Bit field	Name	Description
		0010: 3 cycle 0011: 4 cycle 0100: 5 cycle 0101: 6 cycle 0110: 7 cycle 0111: 10 cycle 1000: 13 cycle 1001: 17 cycle 1010: 24 cycle 1011: 32 cycle 1100: 83 cycle 1101: 93 cycle 1110: 215 cycle 1111: 397 cycle

26.14.1.7 ADC Sampling Time Register 3 (ADC_SAMPT3)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMP19[3:0]				SAMP18[3:0]				SAMP17[3:0]				SAMP16[3:0]			
				rw				rw				rw			

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
15:0	SAMPx[3:0]	Channel Sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bits must remain unchanged during sampling. 0000: 1 cycle 0001: 2 cycle 0010: 3 cycle 0011: 4 cycle 0100: 5 cycle 0101: 6 cycle 0110: 7 cycle 0111: 10 cycle 1000: 13 cycle

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Bit field	Name	Description
		1001: 17 cycle 1010: 24 cycle 1011: 32 cycle 1100: 83 cycle 1101: 93 cycle 1110: 215 cycle 1111: 397 cycle

26.14.1.8 ADC Differential Mode Selection Register (ADC_DIFSEL)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												DIFSEL[18:15]			
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIFSEL[14:0]															Reserved
rw															

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:1	DIFSEL[18:0]	Differential mode for channels 19 to 1 DIFSEL[i] = 0: Configure ADC channel input i+1 in single-ended mode; DIFSEL[i] = 1: Configure ADC channel input i+1 in differential mode.
0	Reserved	Reserved, the reset value must be maintained

26.14.1.9 ADC Analog Watchdog Output Timer Register x(ADC_AWDOTIM)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													AWD3 TIMEN	AWD2 TIMEN	AWD1 TIMEN
													rw	rw	rw

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2	AWD3TIMEN	Analog watchdog 3 event to timer enable 0: Disable analog watchdog 3 event to timer;

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		1: Enable analog watchdog 3 event to timer;
1	AWD2TIMEN	Analog watchdog 2 event to timer enable 0: Disable analog watchdog 2 event to timer; 1: Enable analog watchdog 2 event to timer;
0	AWD1TIMEN	Analog watchdog 1 event to timer enable 0: Disable analog watchdog 1 event to timer; 1: Enable analog watchdog 1 event to timer;

26.14.1.10 ADC Data Offset Register x(ADC_OFFSETx) (x=1..4)

Address offset: 0x24-0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OFFSCHx EN	OFFSCHxCH[4:0]					OFFSCHx SATEN	OFFSCHx DIR	Reserved							
rw	rw					rw	rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OFFSCHxDAT[11:0]											
				rw											

Bit field	Name	Description
31	OFFSCHxEN	Offset channel x enable This bit can be written by software to enable offset compensation function. 0: Disable Offset Compensation Function 1: Enable Offset Compensation Function *Note: This bit should not be operated during ADC conversion*
30:26	OFFSCHxCH[4:0]	Offset channel x selection This bit can be written by software to select which channel to enable offset compensation. 00000: ADC analog input channel 0; 00001: ADC analog input channel 1; …… 10000: ADC analog input channel 16; 10001: ADC analog input channel 17; 10010: ADC analog input channel 18; 10011: ADC analog input channel 19;
25	OFFSCHxSATEN	Offset Saturation enable This bit can be written or cleared by software to enable saturation to 0x0000 and 0x0FFF. 0: Without saturation control, the offset data may be signed 1: Enabling saturation enables the offset data to be unsigned, with a range of 0x0000-0x0FFF

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Bit field	Name	Description
24	OFFSCHxDIR	Offset direction 0: Negative offset 1: Positive offset
23:12	Reserved	Reserved, the reset value must be maintained
11:0	OFFSCHxDAT[11:0]	Data offset for channel x These bits are defined to subtract from or add to the original conversion data when converting channel x (regular channel or injected channel), depending on the value of OFFSCHxDIR. The conversion result can be read in the ADC_DAT or ADC_JDATx register. If multiple offset channels are configured for the same channel, the offset channel 1 has the highest priority, followed by offset channel 2, offset channel 3, and offset channel 4. For example, if OFFSCH1CH[4:0] = 8, OFFSCH2CH[4:0] = 8, then only OFFSCH1DAT[11:0] will be used for calculations when converting channel 8.

26.14.1.11 ADC Watchdog 1 High Threshold Register (ADC_AWD1HIGH)

Address offset: 0x34

Reset value: 0x0000 0FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HLH[11:0]											
				rw											

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	HTH[11:0]	Analog watchdog 1 high threshold These bits define the high thresholds for analog watchdog 1.

26.14.1.12 ADC Watchdog 1 Low Threshold Register (ADC_AWD1LOW)

Address offset: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	AWDFIL[2:0]			LTH[11:0]											

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rw rw

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
14:12	AWDFIL[2:0]	Analog watchdog 1 filter value, can only act on a single channel of the watchdog, this bit can be written or cleared by software. 000: Do not enable filtering. 001: 2 consecutive detection results exceeding the threshold will generate an AWD1 flag or interrupt. 010: 3 consecutive detection results exceeding the threshold will generate an AWDx flag or interrupt. … 111: 8 consecutive detection results exceeding the threshold will generate an AWD1 flag or interrupt.
11:0	LTH[11:0]	Analog watchdog 1 low threshold These bits define the low thresholds for analog watchdog 1.

26.14.1.13 ADC Watchdog 2 High Threshold Register (ADC_AWD2HIGH)

Address offset: 0x3C

Reset value: 0x0000 0FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HLH[11:0]											

rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	HTH[11:0]	Analog watchdog 2 high threshold These bits define the high thresholds for analog watchdog 2.

26.14.1.14 ADC Watchdog 2 Low Threshold Register (ADC_AWD2LOW)

Address offset: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LTH[11:0]											
				rw											

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	LTH[11:0]	Analog watchdog 2 low threshold These bits define the low thresholds for analog watchdog 2.

26.14.1.15 ADC Watchdog 3 High Threshold Register (ADC_AWD3HIGH)

Address offset: 0x44

Reset value: 0x0000 0FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HLH[11:0]											
				rw											

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	HTH[11:0]	Analog watchdog 3 high threshold These bits define the high thresholds for analog watchdog 3.

26.14.1.16 ADC Watchdog 3 Low Threshold Register (ADC_AWD3LOW)

Address offset: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LTH[11:0]											
				rw											

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Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	LTH[11:0]	Analog watchdog 3 low threshold These bits define the low thresholds for analog watchdog 3.

26.14.1.17 ADC Analog Watchdog 2 Configuration Register (ADC_AWD2EN)

Address offset: 0x4C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												AWD2EN[19:16]			
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AWD2EN[15:0]															
rw															

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:0	AWD2EN[19:0]	Analog watchdog 2 channel selection These bits define the channels monitored by Analog Watchdog 2, and can be written or cleared by software. AWD2EN[x] = 0: Analog Watchdog 2 does not monitor ADC analog input channel x; AWD2EN[x] = 1: Analog Watchdog 2 monitors ADC analog input channel x; AWD2EN[19:0] = 0b000..00, Analog Watchdog 2 is not operational.

26.14.1.18 ADC Analog Watchdog 3 Configuration Register (ADC_AWD3EN)

Address offset: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												AWD3EN[19:16]			
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AWD3EN[15:0]															
rw															

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Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:0	AWD3EN[19:0]	Analog watchdog 3 channel selection These bits define the channels monitored by Analog Watchdog 3, and can be written or cleared by software. AWD3EN[x] = 0: Analog Watchdog 3 does not monitor ADC analog input channel x; AWD3EN[x] = 1: Analog Watchdog 3 monitors ADC analog input channel x; AWD3EN[19:0] = 0b000..00, Analog Watchdog 3 is not operational.

26.14.1.19 ADC Analog Watchdog 2 Interrupt Enable Register (ADC_AWD2INTEN)

Address offset: 0x54

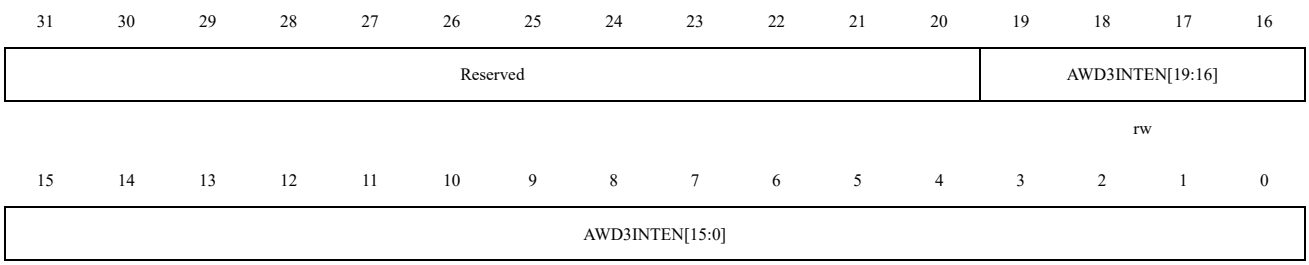
Reset value: 0x0000 0000

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:0	AWD2INTEN[19:0]	Analog watchdog 2 interrupt enable These bits define whether the interrupt for the channels monitored by Analog watchdog 2 is enabled, and can be written or cleared by software. AWD2INTEN[x] = 0: The interrupt for the channel x monitored by Analog watchdog 2 is not enabled; AWD2INTEN[x] = 1: The interrupt for the channel x monitored by Analog watchdog 2 is enabled;

26.14.1.20 ADC Analog Watchdog 3 Interrupt Enable Register (ADC_AWD3INTEN)

Address offset: 0x58

Reset value: 0x0000 0000



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rw

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:0	AWD3INTEN[19:0]	Analog watchdog 3 interrupt enable These bits define whether the interrupt for the channels monitored by Analog watchdog 3 is enabled, and can be written or cleared by software. AWD3INTEN[x] = 0: The interrupt for the channel x monitored by Analog watchdog 3 is not enabled; AWD3INTEN[x] = 1: The interrupt for the channel x monitored by Analog watchdog 3 is enabled;

26.14.1.21 ADC Analog Watchdog 2 Status Register (ADC_AWD2STS)

Address offset: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												AWD2FLAG [19:16]			
												rc-w1			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AWD2FLAG[15:0]															
rc-w1															

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:0	AWD2FLAG[19:0]	Analog watchdog 2 status flag AWD2FLAG[x] = 0: Indicates that the voltage value of the channel x conversion monitored by Analog Watchdog 2 has not exceeded the range defined by the ADC_AWD2HIGH.HTH [11:0] and ADC_AWD2LOW.LTH [11:0] registers； AWD2FLAG[x] = 1: Indicates that when the voltage value of the channel x conversion monitored by Analog Watchdog 2 exceeds the range defined by the ADC_AWD2HIGH.HTH[11:0] and ADC_AWD2LOW.LTH[11:0] registers, it is set to 1 by hardware, and writing 1 clears it by software.

26.14.1.22 ADC Analog Watchdog 3 Status Register (ADC_AWD3STS)

Address offset: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	AWD2FLAG[19:16]
	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AWD2FLAG[15:0]															
rc_w1															

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19:0	AWD3FLAG[19:0]	Analog watchdog 3 status flag AWD3FLAG[x] = 0: Indicates that the voltage value of the channel x conversion monitored by Analog Watchdog 2 has not exceeded the range defined by the ADC_AWD3HIGH.HTH [11:0] and ADC_AWD3LOW.LTH [11:0] registers； AWD3FLAG[x] = 1: Indicates that when the voltage value of the channel x conversion monitored by Analog Watchdog 3 exceeds the range defined by the ADC_AWD3HIGH.HTH[11:0] and ADC_AWD3LOW.LTH[11:0] registers, it is set to 1 by hardware, and writing 1 clears it by software.

26.14.1.23 ADC Regular Sequence Register 1 (ADC_RSEQ1)

Address offset: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LEN[4:0]					SEQ20[4:0]					SEQ19[4:0]				
	rw					rw					rw				

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
14:10	LEN[4:0]	Regular channel sequence length These bits are defined by software to specify the number of channels in the regular sequence conversion. 00000: 1 conversion 00001: 2 conversion ... 01111: 16 conversion 10000: 17 conversion

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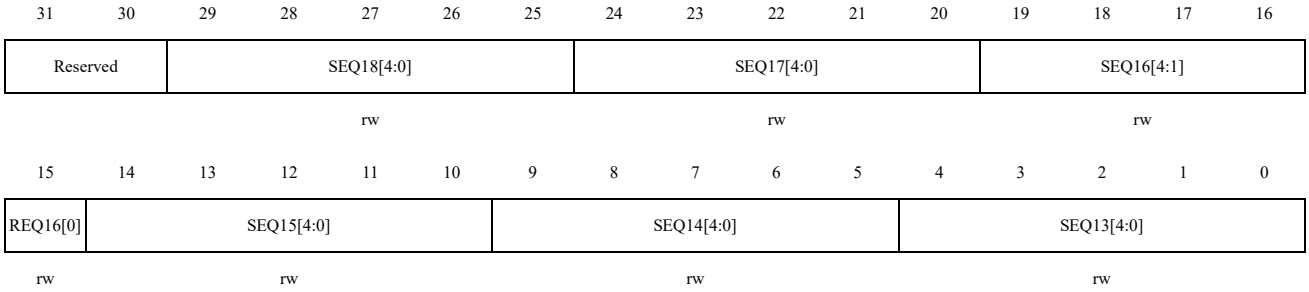
Bit field	Name	Description
		10001: 18 conversion 10010: 19 conversion 10011: 20 conversion.
9:5	SEQ20[4:0]	20th conversion in regular sequence
4:0	SEQ19[4:0]	19th conversion in regular sequence

26.14.1.24 ADC Regular Sequence Register 2 (ADC_RSEQ2)

Address offset: 0x68

Reset value: 0x0000 0000

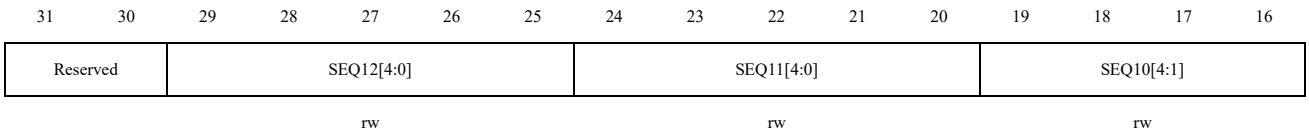


Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ18[4:0]	18th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 18th conversion channel in the conversion sequence.
24:20	SEQ17[4:0]	17th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 17th conversion channel in the conversion sequence.
19:15	SEQ16[4:0]	16th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 16th conversion channel in the conversion sequence.
14:10	SEQ15[4:0]	15th conversion in regular sequence
9:5	SEQ14[4:0]	14th conversion in regular sequence
4:0	SEQ13[4:0]	13th conversion in regular sequence

26.14.1.25 ADC Regular Sequence Register 3 (ADC_RSEQ3)

Address offset: 0x6C

Reset value: 0x0000 0000



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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ10[0]	SEQ9[4:0]					SEQ8[4:0]					SEQ7[4:0]				
rw	rw					rw					rw				

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ12[4:0]	12th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 12th conversion channel in the conversion sequence.
24:20	SEQ11[4:0]	11th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 11th conversion channel in the conversion sequence.
19:15	SEQ10[4:0]	10th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 10th conversion channel in the conversion sequence.
14:10	SEQ9[4:0]	9th conversion in regular sequence
9:5	SEQ8[4:0]	8th conversion in regular sequence
4:0	SEQ7[4:0]	7th conversion in regular sequence

26.14.1.26 ADC Regular Sequence Register 4 (ADC_RSEQ4)

Address offset: 0x70

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SEQ6[4:0]					SEQ5[4:0]					SEQ4[4:1]			
		rw					rw					rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQ4[0]	SEQ3[4:0]					SEQ2[4:0]					SEQ1[4:0]				
rw	rw					rw					rw				

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ6[4:0]	6th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 6th conversion channel in the conversion sequence.
24:20	SEQ5[4:0]	5th conversion in regular sequence These bits are defined by software to specify the number (0-19) of the 5th conversion channel in the conversion sequence.
19:15	SEQ4[4:0]	4th conversion in regular sequence

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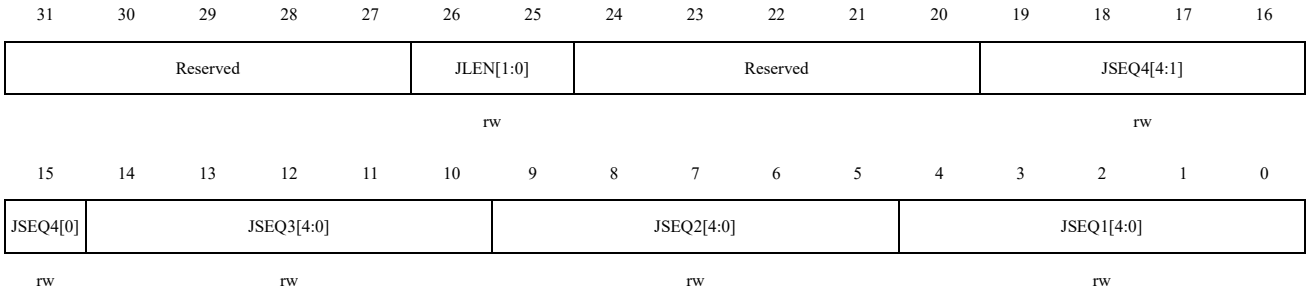
Bit field	Name	Description
		These bits are defined by software to specify the number (0-19) of the 4th conversion channel in the conversion sequence.
14:10	SEQ3[4:0]	3th conversion in regular sequence
9:5	SEQ2[4:0]	2nd conversion in regular sequence
4:0	SEQ1[4:0]	1st conversion in regular sequence

26.14.1.27 ADC Injected Sequence Register（ADC_JSEQ）

Offset address: 0x70

Reset value: 0x0000 0000



Bit Field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained
26:25	JLEN[1:0]	Injected sequence length These bits are software-defined as the number of channels in the injected channel conversion sequence. 00: 1 conversion; 01: 2 conversions; 10: 3 conversions; 11: 4 conversions.
24:20	Reserved	Reserved, the reset value must be maintained
19:15	JSEQ4[4:0]	4th conversion in injected sequence These bits are defined by software as the number (0-18) of the 4th conversion channel in the conversion sequence. *Note: Different from regular conversion sequences, if the length of ADC_JSEQ.JLEN[1:0] is less than 4, the sequence of conversion starts from (4-JLEN). For example, ADC_JSEQ[21:0] = 10 00011 00011 00111 00010 means that the scan conversion will be converted in the following channel order: 7, 3, 3 instead of 2, 7, 3.*
14:10	JSEQ3[4:0]	3rd conversion in injected sequence
9:5	JSEQ2[4:0]	2nd conversion in injected sequence
4:0	JSEQ1[4:0]	1st conversion in injected sequence

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26.14.1.28 ADC Injection Data Register x (ADC_JDATx)(x = 1..4)

Address offset: 0x78-0x84

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JDATx[15:0]															
r															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	JDAT[15:0]	Injected data These bits are read-only and contain the conversion results of the injected channel. The data is left-aligned or right-aligned

26.14.1.29 ADC Regular Data Register (ADC_DAT)

Address offset: 0x88

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAT2[15:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT1[15:0]															
r															

Bit field	Name	Description
31:16	DAT2[15:0]	2nd data item of a pair of regular conversions —In dual mode, these bits contain data from ADC2。 —In triple mode, these bits can also contain the regular data from ADC1, ADC2, and ADC3. These bits are read-only and contain the conversion results of the regular channels. Data can be left-aligned or right-aligned.
15:0	DAT1[15:0]	1st data item of a pair of regular conversions —In dual mode, these bits contain the regular data from the master ADC. —In triple mode, these bits can also contain the regular data from ADC1, ADC2, and

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Bit field	Name	Description
		ADC3. These bits are read-only and contain the conversion results of the regular channels. The data can be left-aligned or right-aligned.

26.14.1.30 ADC FIFO Configuration Register (ADC_FIFOCFG)

Address offset: 0x8C

Reset value: 0x0000 0180

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				NE INTEN	CLR	WL[3:0]				EN	HF INTEN	EINTEN	FINTEN	Reserved	
				rw	rw	rw				rw	rw	rw	rw		

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	NEINTEN	FIFO non-empty interrupt enable 0: Disable 1: Enable
10	CLR	FIFO clear signal 0: Disable 1: Enable
9:6	WL[3:0]	FIFO water level 0000: FIFO water level is 1; 0001: FIFO water level is 2; 0010: FIFO water level is 3; 0011: FIFO water level is 4; 0100: FIFO water level is 5; 0101: FIFO water level is 6; 0110: FIFO water level is 7; 0111: FIFO water level is 8; 1000: FIFO water level is 9; 1001: FIFO water level is 10; 1010: FIFO water level is 11; 1011: FIFO water level is 12; 1100: FIFO water level is 13; 1101: FIFO water level is 14; 1110: FIFO water level is 15; 1111: FIFO water level is 16;

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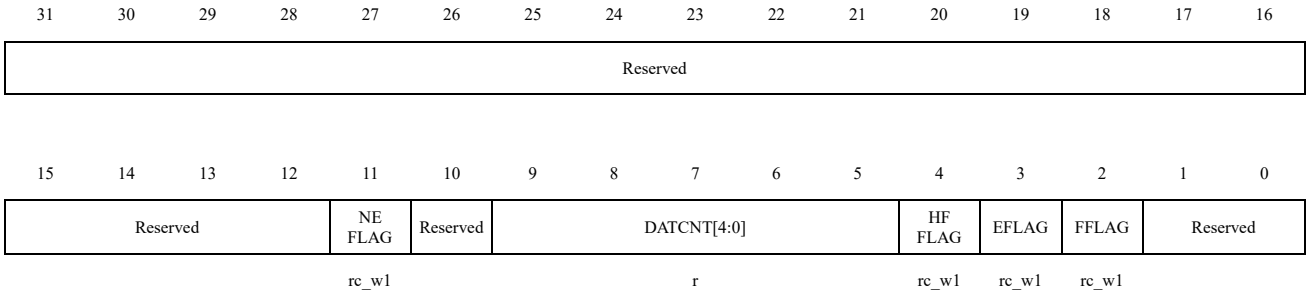
Bit Field	Name	Description
5	EN	FIFO enable 0: Disable 1: Enable
4	HFINTEN	FIFO half-full interrupt enable 0: Disable 1: Enable
3	EINTEN	FIFO empty interrupt enable 0: Disable 1: Enable
2	FINTEN	FIFO full interrupt enable 0: Disable 1: Enable
1:0	Reserved	Reserved, the reset value must be maintained

26.14.1.31 ADC FIFO Status Register (ADC_FIFOSTS)

Address offset: 0x90

Reset value: 0x0000 0008



Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	NEFLAG	FIFO non-empty status It is set to 1 by hardware, and writing 1 clears it by software
10	Reserved	Reserved, the reset value must be maintained
9:5	DATCNT[4:0]	FIFO valid data count 00000: Valid data is 0; 00001: Valid data is 1; 00010: Valid data is 2; 00011: Valid data is 3; 00100: Valid data is 4; 00101: Valid data is 5; 00110: Valid data is 6; 00111: Valid data is 7;

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Bit Field	Name	Description
		01000: Valid data is 8; 01001: Valid data is 9; 01010: Valid data is 10; 01011: Valid data is 11; 01100: Valid data is 12; Other: Reserved
4	HFFLAG	FIFO half-full status It is set to 1 by hardware, and writing 1 clears it by software.
3	EFLAG	FIFO empty status It is set to 1 by hardware, and writing 1 clears it by software.
2	FFLAG	FIFO full status It is set to 1 by hardware, and writing 1 clears it by software.
1:0	Reserved	Reserved, the reset value must be maintained

26.14.1.32 ADC Delay Sampling Register (ADC_DLYSMP)

Address offset: 0x94

Reset value: 0x7000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTLEADVAL[3:0]				DLYVAL[3:0]				DLY SAMPEN	Reserved						
rw				rw				rw	rw						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:28	INTLEADVAL[3:0]	Delayed sampling cycle configuration. These bits are set and cleared by software, and these bits are used for interleaved mode in dual ADC or triple ADC mode. 0000: 1 cycle delay 0001: 2 cycles delay 1111: 16 cycles delay *Note:* *1.This bit can only be used in interleaved mode with multiple ADCs, and does not apply beyond that.*
27:24	DLYVAL[3:0]	Delayed sampling cycle configuration in independent mode. These bits are set and cleared by software 0000: 1 cycle delay 0001: 2 cycles delay 1111: 16 cycles delay *Note:*

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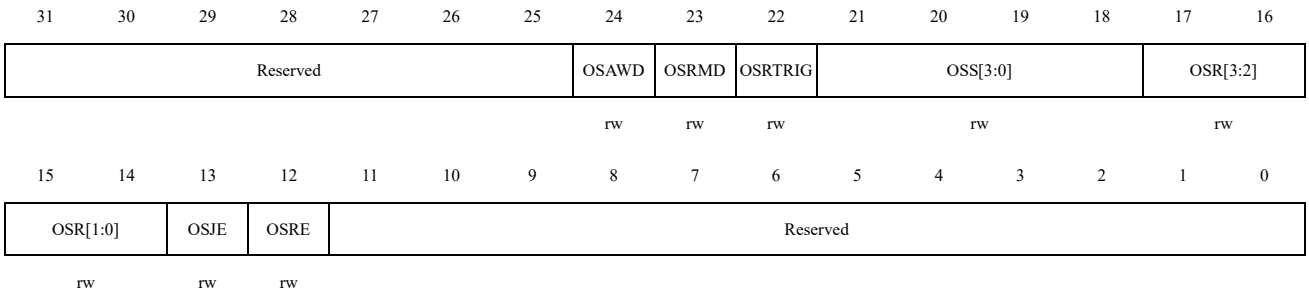
Bit Field	Name	Description
		1.This bit can only be used in indenpendent mode , and multiple ADCs do not apply beyond that.
23	DLYSAMPEN	Delayed sampling mode enable in independent mode. These bits are set and cleared by software. 0: disable delayed sampling mode; 1: enable delay sampling mode; *Note: This bit can only be used in indenpendent mode, and multiple ADCs do not apply beyond that.*
22:0	Reserved	Reserved, the reset value must be maintained

26.14.1.33 ADC Oversampling Register (ADC_OSCFG)

Address offset: 0x98

Reset value: 0x0000 0000



Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	OSAWD	Oversampling data for analog watchdog comparision 0: Oversampling result data DAT[15:4] is used for comparison with the watchdog threshold; 1: Oversampling result data DAT[11:0] is used for comparison with the watchdog threshold;
23	OSRMD	Regular channels oversample mode 0: Continuous mode. When the regular oversampling is triggered, oversampling temporarily stops. When triggered again, oversampling resumes. 1: Reset mode. When the regular oversampling is triggered, oversampling stops. When triggered again, oversampling restarts.
22	OSRTRIG	Regular channels oversample triagger 0: All oversampling conversions only require one trigger 1: Each oversampling conversion requires one trigger each time
21:18	OSS[3:0]	Oversample data right shift bit width 0000: right shift 0 bit 0001: right shift 1 bit 0010: right shift 2 bit 0011: right shift 3 bit 0100: right shift 4 bit 0101: right shift 5 bit 0110: right shift 6 bit

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Bit Field	Name	Description
		0111: right shift 7 bit 1000: right shift 8 bit 1001: right shift 9 bit 1010: right shift 10 bit Other: right shift 0 bit
17:14	OSR[3:0]	Oversample rate times configuration 0000: The number of oversampling is 1 0001: The number of oversampling is 2 0010: The number of oversampling is 4 0011: The number of oversampling is 8 0100: The number of oversampling is 16 0101: The number of oversampling is 32 0110: The number of oversampling is 64 0111: The number of oversampling is 128 1000: The number of oversampling is 256 1001: The number of oversampling is 512 1010: The number of oversampling is 1024 Other: The number of oversampling is 1
13	OSJE	Injection channels oversample enable 0: Disable 1: Enable
12	OSRE	Regular channels oversample enable 0: Disable 1: Enable
11:0	Reserved	Reserved, the reset value must be maintained.

26.14.1.34 ADC Internal Register Configuration Register (ADC_INTLRCFG)

Address offset: 0x9C

Reset value: 0x2000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WEN	RWSTART	DONE	ADDR[2:0]			WDATA[7:0]								RDAT[7:0]	
rw	w	r	rw			rw								r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDAT[5:0]						Reserved									
r															

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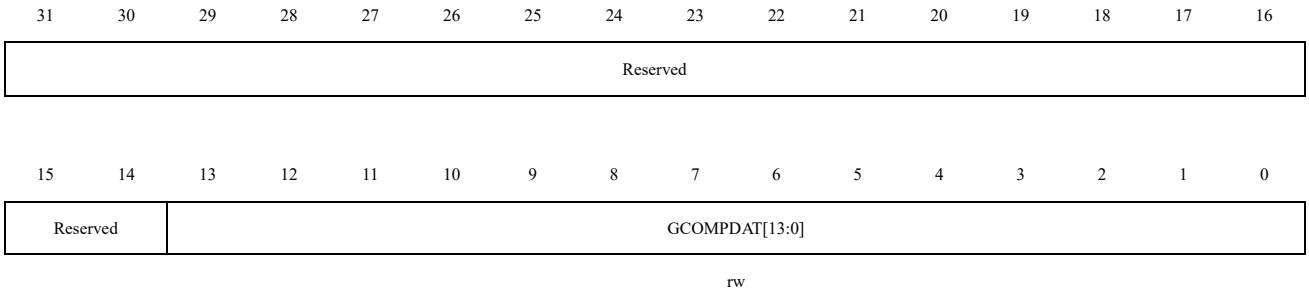
Bit Field	Name	Description
31	WEN	Write enable This bit is set by software to enable writing. 0: Enable reading; 1: Enable writing;
30	RWSTART	Start Read/ Write Internal Register This bit is set by software to start write/read internal register. And read always as 0; When this bit is set, ADC_INTLRCFG.DONE will be cleared immediately.
29	DONE	Write/Read Internal Register Finish Flag This bit is set by hardware to indicate the ready status of writing/reading internal register. This bit is cleared by setting WRSTART.
28:26	ADDR[2:0]	The address of internal registers, range from 3'b0 - 3'b111;
25:18	WDAT [7:0]	Data write into internal register.
17:10	RDAT [7:0]	Data read from internal register.
9:0	Reserved	Reserved, the reset value must be maintained.

26.14.1.35 ADC Gain Compensation Register (ADC_GCOMP)

Address offset: 0xA0

Reset value: 0x0000 0000



Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:0	GCOMPDAT[13:0]	Gain compensation coefficient This bit is set and cleared by software to set the gain compensation coefficient. 00 1000 0000 0000: The gain compensation coefficient is 0.5 ... 01 0000 0000 0000: The gain compensation coefficient is 1 10 0000 0000 0000: The gain compensation coefficient is 2 11 0000 0000 0000: The gain compensation coefficient is 3 ... The range of this gain coefficient is 0 to 3.999756, and the gain coefficient is the parameter divided by 4096.

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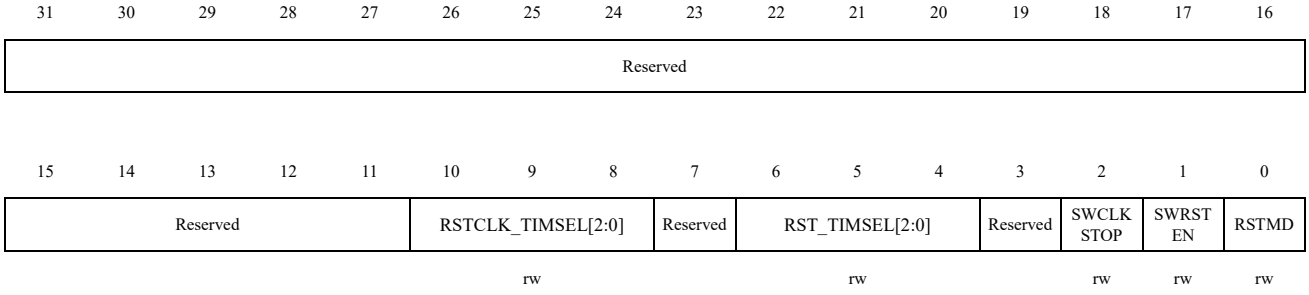
26.14.1.36 ADC Power up configuration Register (ADC_PUCFG)

Address offset: 0xA4

Reset value: 0x007D 2210



Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10:8	RSTCLK_TIMESEL	Time from ADC reset to clock start. 3'b000: 1-cycle 3'b001: 2-cycle 3'b010: 4-cycle … 3'b110: 64-cycle Others: Reserved Others: Reserved Valid only when RSTMD =0. Must set before setting ON
7	Reserved	Reserved, the reset value must be maintained.
6:4	RST_TIMESEL	ADC Reset cycles. 3'b000: 1-cycle 3'b001: 2-cycle 3'b010: 4-cycle … 3'b110: 64-cycle Others: Reserved Valid only when RSTMD =0. Must set before setting ON.
3	Reserved	Reserved, the reset value must be maintained.
2	SWCLKSTOP	Software clock enable for ADC. 0: Enable clock 1: Stop clock Valid only when RSTMD =1.
1	SWRSTEN	Software reset for ADC. 0: release the reset. 1: reset ADC

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Bit Field	Name	Description
		Valid only when RSTMD =1.
0	RSTMD	ADC RESET MODE 0: Reset ADC according to ADC ON 1: Reset ADC by software reset

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27 Digital-to-analog converter (DAC)

27.1 Introduction

DAC is a digital/analog converter, mainly digital input, voltage output. DAC data can be 8-bit or 12-bit and support DMA functionality. When the DAC is configured in 12-bit mode, the DAC data can be right-aligned or left-aligned. When the DAC is configured in 8-bit mode, the DAC data can be right-aligned. Each DAC has an independent converter and can perform conversions independently. In dual DAC mode, each DAC can perform conversions independently, or two DACs (DAC1 & DAC2, DAC3 & DAC4, DAC5 & DAC6 can each form a pair) can simultaneously perform conversions and updates.

VREF+ is input through the pin as the DAC reference voltage, which increases the precision of the DAC conversion data. The built-in VREFBUF can also serve as the DAC's reference voltage. For information about the voltage reference buffer (VREFBUF) section, please refer to the VREFBUF chapter.

When the DAC output is internally connected to external peripherals on the chip, the DACx_OUT pin can be used as a general-purpose input/output (GPIO). The DAC output buffer can be selectively enabled to achieve high driving output current.

27.1.1 Main Features

- Support for 6 DACs, each corresponding to an independent DAC converter.
- Support for 8-bit or 12-bit output, with data available in both right-aligned and left-aligned modes in 12-bit mode.
- Dual DAC supports synchronous or independent conversion.
- Each DAC supports DMA functionality and DMA underflow error detection.
- DMA double data mode can save bus bandwidth.
- Noise wave, triangular waveform, sawtooth wave generation.
- DAC output supports connection to on-chip peripherals (COMP).
- Buffer offset calibration.
- Input reference voltage supports VREF+ and built-in VREFBUF.
- External event-triggered conversion.

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27.2 DAC Overview

Table 27-1 DAC Features

DAC Features	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6
Output buffer	Support		-			
I/O connection	PA4 connected to DAC1_OUT	PA5 connected to DAC1_OUT	-			
External output	Support		-			
Internal output	Support		Support			
Maximum sampling rate	1MSPS		15MSPS			

DAC structural diagram and pin description are as follows

Figure 27-1 Block diagram of DAC

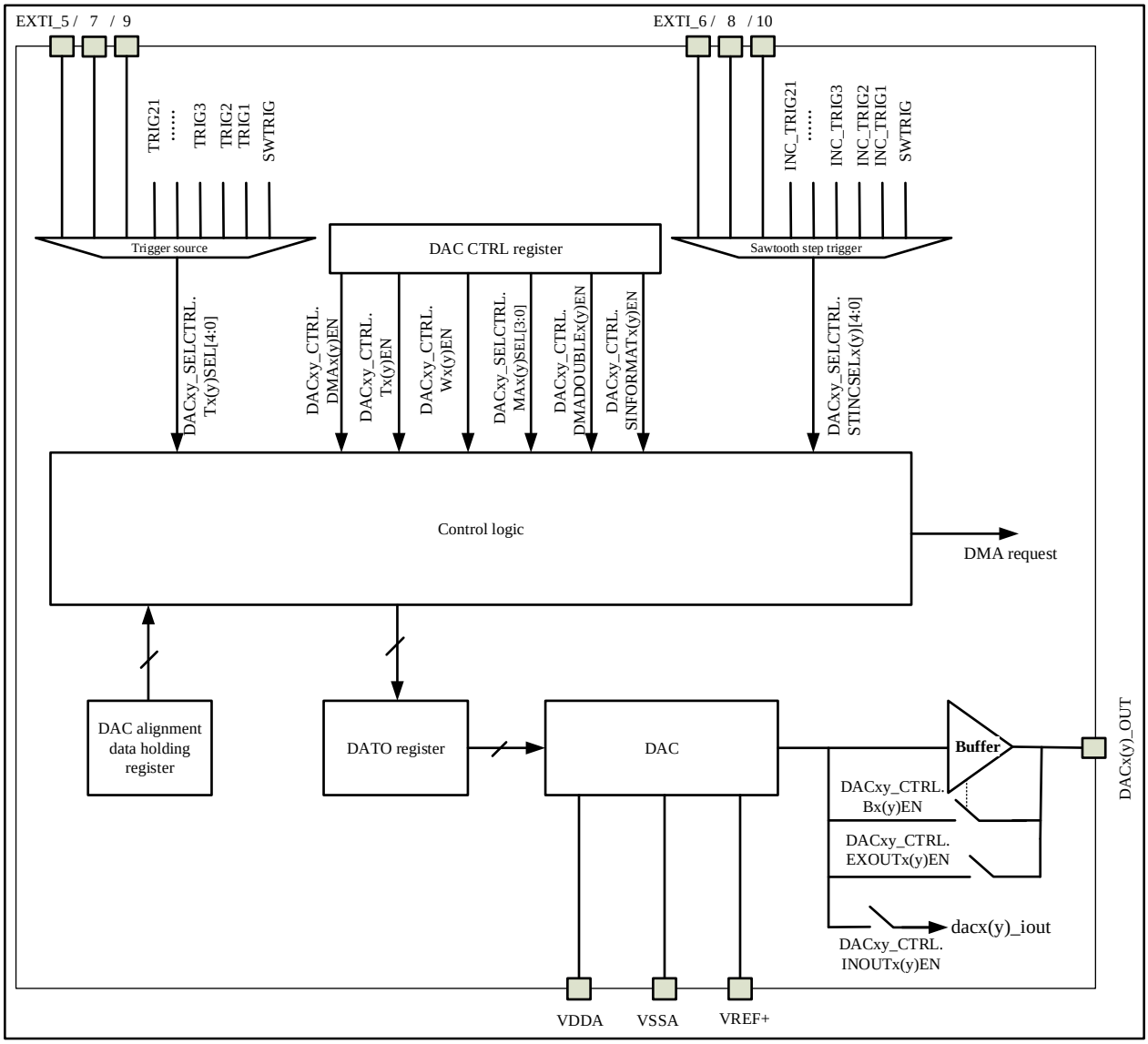

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Table 27-2 DAC Pins

Name	Description	Type
V_{REF+}	Positive reference voltage used by the DAC. $1.8V \leq V_{REF+} \leq V_{DDA}$（3.6V）	input: Positive analog reference voltage
V_{DDA}	Analog power	input: Analog power
V_{SSA}	Analog power ground	input: Analog power ground
DACx(y)_OUT	Analog output from DACx or DACy to external IO	output: Analog output signal
dacx(y)_iout	Analog output from DACx or DACy to internal peripherals	output: Analog output signal

27.3 DAC Function Description And Operation Description

27.3.1 DAC Enable

Powering on the DAC can be done by configuring DACxy_CTRL.DACx(y)EN = 1. It takes some time for t_{WAKEUP} to open the DAC.

27.3.2 DAC Output Buffer

By configuring DACxy_CTRL.Bx(y)EN to disable or enable the output buffer of DAC, if the output buffer is enable, the output impedance is reduced, the driving ability is enhanced, and the external load can be driven without the external operational amplifier.

Table 27-3 DAC1/2 output characteristics

Output type	DACxy_CTRL.INOUTx(y)EN	DACxy_CTRL.EXOUTx(y)EN	DACxy_CTRL.Bx(y)EN
Internal output	1	0	0
External output	0	1	0/1
Simultaneous internal and external output	1	1	1

Note: When using simultaneous internal and external output, the output buffer must be enabled (DACxy_CTRL.Bx(y)EN = 1).

27.3.3 DAC Data Format

27.3.3.1 Data aligned

When the configuration data is written to the DACx(y)_DR12 register, the data is written to DACx(y)_DR12[11:0], and the 12-bit data is right-aligned. (Actually stored in the register DACx(y)_DHR[11:0] bits, DACx(y)_DHR is the internal data storage register)

When the configuration data is written to the DACx(y)_DL12 register, the data is written to DACx(y)_DL12[15:4], and the 12-bit data is left-aligned. (Actually stored in the register DACx(y)_DHR[11:0] bits, DACx(y)_DHR is the internal data storage register)

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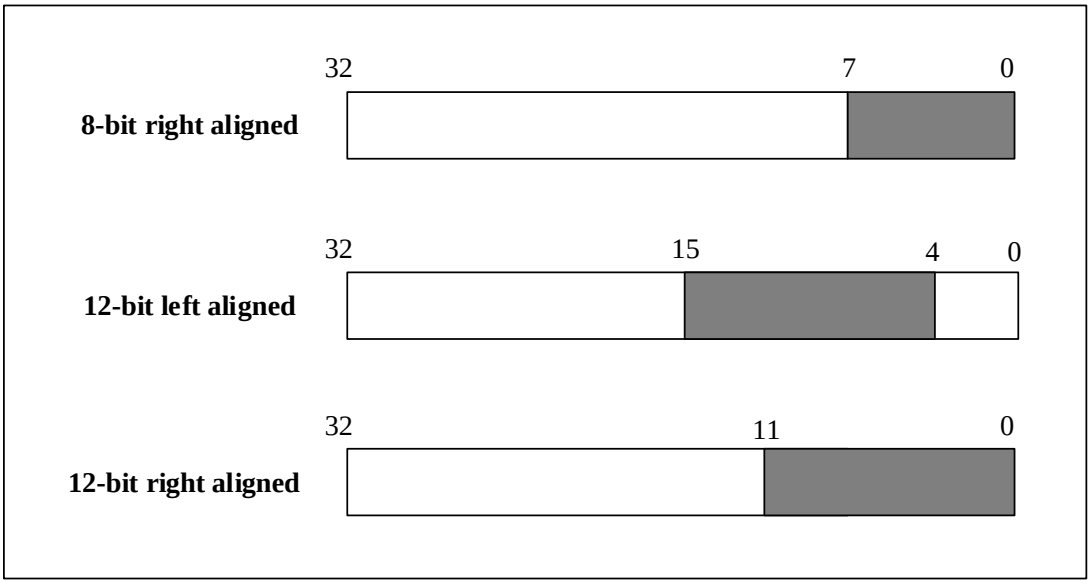
When the configuration data is written to the DACx(y)_DR8 register, the data is written to DACx(y)_DR8[7:0], and the 8-bit data is right-aligned. (Actually stored in the register DACx(y)_DHR[11:4] bits, DACx(y)_DHR[11:4] is the internal data storage register)

Figure 27-2 Data Register Of Single DAC Channel Mode



When DAC outputs are synchronized, there are 3 scenarios:

When configuring data writing to the DACxy_DR12D register, DACx data is written to DACxy_DR12D[11:0] (actually stored in the DACx_DHR[11:0] bits, DACx_DHR is the internal data holding register), and DACy data is written to DACxy_DR12D[27:16] (actually stored in the DACy_DHR[11:0] bits, DACy_DHR is the internal data holding register), with 12-bit data right-aligned.

When configuring data writing to the DACxy_DL12D register, DACx data is written to DACxy_DL12D[15:4] (actually stored in the DACx_DHR[11:0] bits, DACx_DHR is the internal data holding register), and DACy data is written to DACxy_DL12D[31:20] (actually stored in the DACy_DHR[11:0] bits, DACy_DHR is the internal data holding register), with 12-bit data left-aligned.

When configuring data writing to the DACxy_DR8D register, DACx data is written to DACxy_DR8D[7:0] (actually stored in the DACx_DHR[11:4] bits, DACx_DHR is the internal data holding register), and DACy data is written to DACxy_DR8D[15:8] (actually stored in the DACy_DHR[11:4] bits, DACy_DHR is the internal data holding register), with 8-bit data left-aligned.

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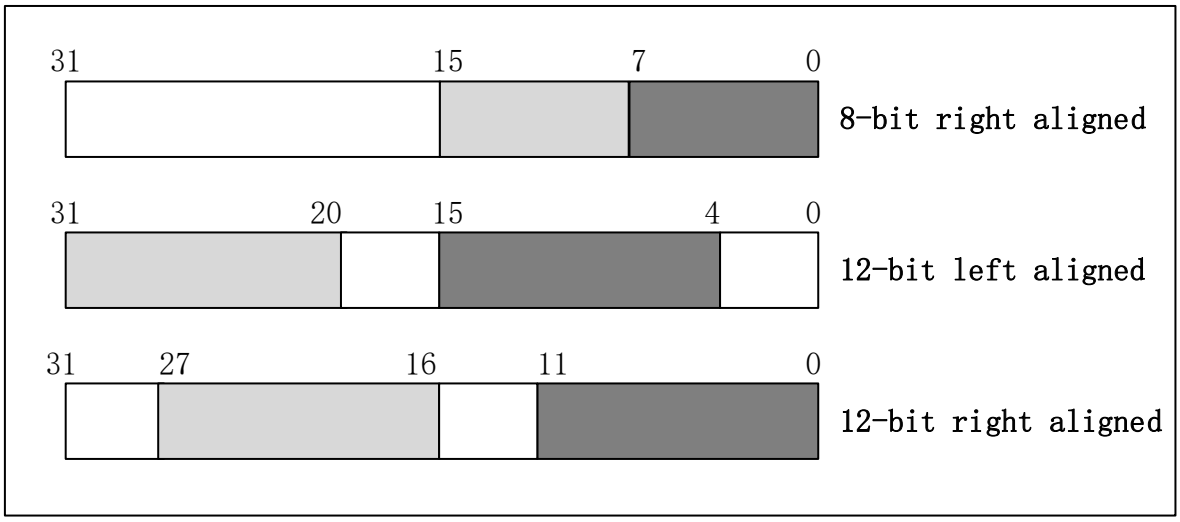
Figure 27-3 Data format when DAC outputs are synchronized



27.3.3.2 Signed/Unsigned Data

The DAC has an unsigned input data range of 0 to 0xFFF.

The DAC can also process signed input data in two's complement format. This is achieved by setting the DACxy_CTRL.SINFORMATx(y) bit. When DACxy_CTRL.SINFORMATx(y) is set to 1, the most significant bit (MSB) of the data written to the holding register is inverted when copied to the data output DACx(y)_DATO register.

Table 27-4 12-bit data format

SINFORMATx(y)-bit	DACx(y)D register value	DACx(y)_DATO register value
0	0x800	0x800
0	0x7FF	0x7FF
0	0xFFF	0xFFF
1	0x000	0x800
1	0x7FF	0xFFF
1	0x800	0x000
1	0xFFF	0x7FF

27.3.4 DAC Trigger

Enabling DAC external trigger can be achieved by configuring DACxy_CTRL.Tx(y)EN = 1, and selecting an external trigger event as the DAC's external trigger source by configuring DACxy_SELCTRL.Tx(y)SEL[4:0].

These events can also be software-triggered or hardware-triggered, as shown in the table below：

Table 27-5 DAC External Trigger

Trigger source	Type	Tx(y)SEL[4:0]
ATIM1 TRGO events	Internal signal from the on-chip timer	00001
ATIM2 TRGO events		00010
ATIM3 TRGO events		00011

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Trigger source	Type	Tx(y)SEL[4:0]
ATIM4 TRGO events		00100
GTIMA1 TRGO events		00101
GTIMA2 TRGO events		00110
GTIMA3 TRGO events		00111
GTIMA4 TRGO events		01000
GTIMA5 TRGO events		01001
GTIMA6 TRGO events		01010
GTIMA7 TRGO events		01011
GTIMB1 TRGO events		01100
GTIMB2 TRGO events		01101
GTIMB3 TRGO events		01110
EXTI line 5	External pins	01111
EXTI line 7		10000
EXTI line 9		10001
SHRTIM1 Reset_TRG1 events	Internal signal from the on-chip timer	10010
SHRTIM1 Reset_TRG2 events		10011
SHRTIM1 Reset_TRG3 events		10100
SHRTIM1 Reset_TRG4 events		10101
SHRTIM1 Reset_TRG5 events		10110
SHRTIM1 Reset_TRG6 events		10111
SHRTIM1 TRG1/2/3 events		11000
SHRTIM2 Reset_TRG1 events		11001
SHRTIM2 Reset_TRG2 events		11010
SHRTIM2 Reset_TRG3 events		11011
SHRTIM2 Reset_TRG4 events		11100
SHRTIM2 Reset_TRG5 events		11101
SHRTIM2 Reset_TRG6 events		11110
SHRTIM2 TRG1/2/3 events		11111
SWTRIG (Software Triggered)	Software control bit	00000

When the DAC's trigger source is a timer output or rising edge of an EXTI line, upon trigger generation, the data held in the alignment data holding register will be transferred to the DACx(y)_DATO register. This data transfer process requires (0.5*PCS) DAC_CLK cycles or 3/5/7 bus_clk cycles (depending on the value of DACxy_HFSEL[1:0]) clock cycles of time.

If the user selects software trigger as the trigger source, by configuring DACxy_SOTTR.TRx(y)EN = 1, the data held in the alignment data holding register will be transferred to the DACx(y)_DATO register. The DACxy_SOTTR.TRx(y)EN bit will automatically clear to 0 by hardware after data transfer.

The step trigger source for sawtooth wave generation can be selected using the DACxy_SELCTRL.STINCSELx(y)[4:0] control bits.

The specific trigger sources are shown in the table below:

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Table 27-6 DAC DAC sawtooth wave step trigger source signals

Trigger source	Type	STINCSELx(y)[4:0]
ATIM1 TRGO events	Internal signal from the on-chip timer	00001
ATIM2 TRGO events		00010
ATIM3 TRGO events		00011
ATIM4 TRGO events		00100
GTIMA1 TRGO events		00101
GTIMA2 TRGO events		00110
GTIMA3 TRGO events		00111
GTIMA4 TRGO events		01000
GTIMA5 TRGO events		01001
GTIMA6 TRGO events		01010
GTIMA7 TRGO events		01011
GTIMB1 TRGO events		01100
GTIMB2 TRGO events		01101
GTIMB3 TRGO events		01110
EXTI line 6	External pins	01111
EXTI line 8		10000
EXTI line 10		10001
SHRTIM1 Step_TRG1 events		10010
SHRTIM1 Step_TRG2 events		10011
SHRTIM1 Step_TRG3 events		10100
SHRTIM1 Step_TRG4 events		10101
SHRTIM1 Step_TRG5 events		10110
SHRTIM1 Step_TRG6 events		10111
Reserved		11000
SHRTIM2 Step_TRG1 events		11001
SHRTIM2 Step_TRG2 events		11010
SHRTIM2 Step_TRG3 events		11011
SHRTIM2 Step_TRG4 events		11100
SHRTIM2 Step_TRG5 events		11101
SHRTIM2 Step_TRG6 events		11110
SWTRIG (Software Triggered)	Software control bit	00000

Note:

1. *Changing the DACxy_SELCTRL.Tx(y)SEL[4:0] bits is prohibited while the DAC is enabled.*
2. *When using software trigger, the transfer of data from the alignment data holding register to the DACx(y)_DATO register takes 1 bus_clk (where bus_clk is either pclk or hclk depending on the clock bus the DAC is connected to) clock cycle.*
3. *SHRTIM, ATIM, GTIM, and DAC operate in different clock domains, crossing clock domains can lead to*

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metastability. If the DAC step trigger rate is too close to the DAC operating clock, metastability may occur, resulting in overshoot, and overshoot can cause the loss of step triggers at the overshoot point.

27.3.5 DAC Conversion

Users cannot directly operate the DACx(y)_DATO register; writing to the DHR (including DACx(y)_DR8, DACx(y)_DR12, DACx(y)_DL12, DACxy_DR8D, DACxy_DR12D, DACxy_DL12D) is required for the changes to take effect.

It takes time for the data to transfer from the DHR to the DACx(y)_DATO register (referred to as DATO), as detailed in the following table:

Table 27-7 DAC1-DAC2 Conversion Description

Tx(y)EN	Wx(y)EN	Tx(y)SEL[4:0]	DHR -> DATO(bus_clk)	From DATO to the time T1 for establishing
0	0b'000	00000	2	HFSEL = 0:T1 is (PCS[7:0]/2-1) bus_clk[1]; HFSEL = 1:T1 is 1 bus_clk; HFSEL = 2:T1 is 3 bus_clk; HFSEL = 3:T1 is 5 bus_clk;
1	0b'000	00000	4	
	0b'000	non-0b'000	4	
	non-0b'000	-	3	

Table 27-8 DAC3-DAC6 Conversion Description

Tx(y)EN	Wx(y)EN	Tx(y)SEL[4:0]	DHR -> DATO(bus_clk)	From DATO to the time T1 for establishing
0	0b'000	00000	2	T1 fixed 5 bus_clk.
1	0b'000	00000	4	
	0b'000	non-0b'000	4	
	non-0b'000	-	3	

Note: 1. bus_clk is the bus clock to which the DAC is attached, DAC1/2 are attached to the APB bus, and DAC3/4/5/6 are attached to the AHB bus.

As DAC1/2, When the bus_clk clock speed exceeds 80 MHz, the DACxy_HFSEL[1:0] bits must be set. This will add additional delay to the transfer from the DACx(y)_DHR register to the DACx(y)_DATO register.

If data is updated or a software/hardware trigger event occurs during a prohibited time period, the behavior of the peripheral will be affected. Updating data or triggering events during this period will lead to unpredictable behavior of the peripheral.

The effective output of the DAC needs to go through the following stages. Firstly, the DAC transfers data from the data holding register to the DACx(y)_DATO register. Then, after a delay of time T1, the analog output conversion is initiated from the DACx(y)_DATO register. Finally, the output becomes valid after a settling time $t_{SETTLING}$, which is related to the power supply voltage and the analog output load.

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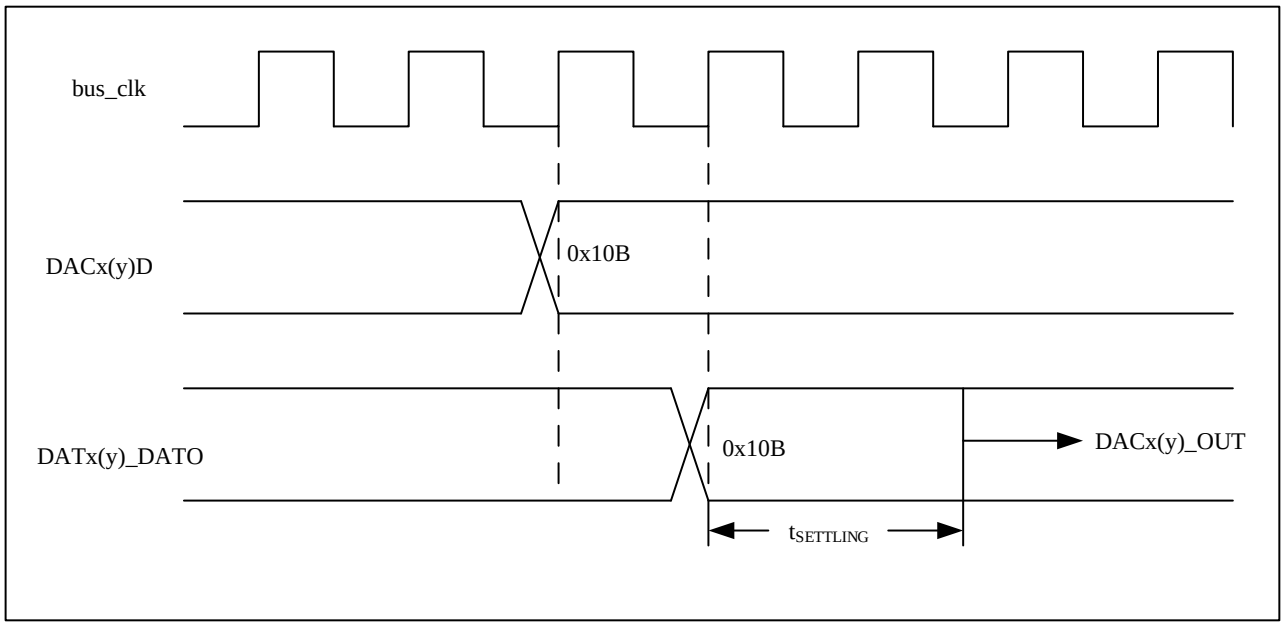
Figure 27-4 Timing diagram for conversion when trigger is disabled



27.3.6 DAC Output Voltage

The digital input is converted to analog voltage output by a DAC module in a linear relationship ranging from 0 to V_{REF+}. The output voltage of DAC is calculated as follows:

DAC output = V_{REF} X (DATO / 4095).

27.3.7 DMA Requests

To enable DMA functionality, configure DACxy_CTRL.DMAx(y)EN = 1. When an external trigger occurs (not a software trigger), a DMA request is generated, and subsequently, the data from the alignment data holding register is transferred to the DACx(y)_DATO register.

In dual DAC mode, if both DACxy_CTRL.DMAx(y)EN bits are set, two DMA requests will be generated. If only one DMA request is needed, then set the DMAxEN bit. This allows applications to manage two DACs using a single DMA request.

Since the DMA request occurs after the data is loaded into the data holding register and transferred to the DACx(y)_DATO register, users must first write data to the data holding register before triggering the DAC conversion.

27.3.7.1 DMA Underflow

DAC's DMA requests are not queued, so if a second external trigger arrives before the acknowledgment of the first external trigger (the first request), no new request will be issued. Instead, the DACxy_STS.DMAUDRx(y) flag will be set to report an error condition. The DAC continues to convert old data. Therefore, users must set an appropriate DAC trigger frequency to reduce the workload on DMA and avoid DMA underflow.

When a DMA underflow occurs, users can clear the DACxy_STS.DMAUDRx(y) flag by writing a 1, then disable DMA, and reinitialize both DMA and DAC to correctly restart the transfer.

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If the user sets the DACxy_CTRL.DMAUDRx(y)IEN bit, a DMA underflow interrupt will be generated when a DMA underflow event occurs.

27.3.7.2 DMA double data mode

During DMA operation, a single DMA request can only transfer 8-bit or 12-bit effective data due to the 32-bit AHB bandwidth, which greatly wastes DMA bandwidth. Therefore, it is possible to consider transmitting two 12-bit data simultaneously to save DMA transfer efficiency. Setting DACxy_CTRL.DMADOUBLEx(y) to 1 enables DMA double data mode.

When the DACxy_CTRL.DMAx(y)EN bit is set, a DAC DMA request is generated every two external triggers (except for software triggers).

1. When the first trigger event is detected, the value of the DACx(y)DB register will be transferred to the DACx(y)_DATO register. A DMA request is then generated, and new data is written into the DACx(y) D and DACx(y) DB data registers by DMA.
2. When the next trigger event is detected, the value of the DACx(y)D register will be transferred to the DACx(y)_DATO register. The second trigger event will not generate any DMA request.
3. When the next trigger event is detected, the value of the DACx(y)DB register will be transferred to the DACx(y)_DATO register. A DMA request is then generated, and new data is written into the DACx(y) D and DACx(y)DB data registers by DMA.

In DMA double data mode, the DAC also supports DMA underflow function.

In DMA double data mode, a DMA request can only handle one DAC. When using DMA double data mode in dual DAC mode, where both DACs are simultaneously using DMA double data, users need to separately configure two independent DMA channels.

To switch from double data mode to single data mode, or from single data mode to double data mode, the following conditions must be met:

- DAC must be in the off state. (DACxy_CTRL.DACx(y)EN = 0)
- DMA enable must be in the off state (DACxy_CTRL.DMAx(y)EN = 0)

27.3.8 Noise Generation

DAC can generate noise by configuring DACxy_CTRL.Wx(y)EN[2:0] as 3b’001 to enable the noise function. By configuring DACxy_SELCTRL.MAx(y)SEL[3:0] to select which bits of the linear feedback shift register (LFSR) to mask, the value of the LFSR register is added to the value of the aligned data hold register and then written to the DACx(y)_DATO register (overflow bits are discarded). The initial value of the LFSR is 0xAAA, and the value of the LFSR is updated three bus_clk clock cycles after the trigger event occurs.

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Figure 27-5 DAC LFSR Algorithm

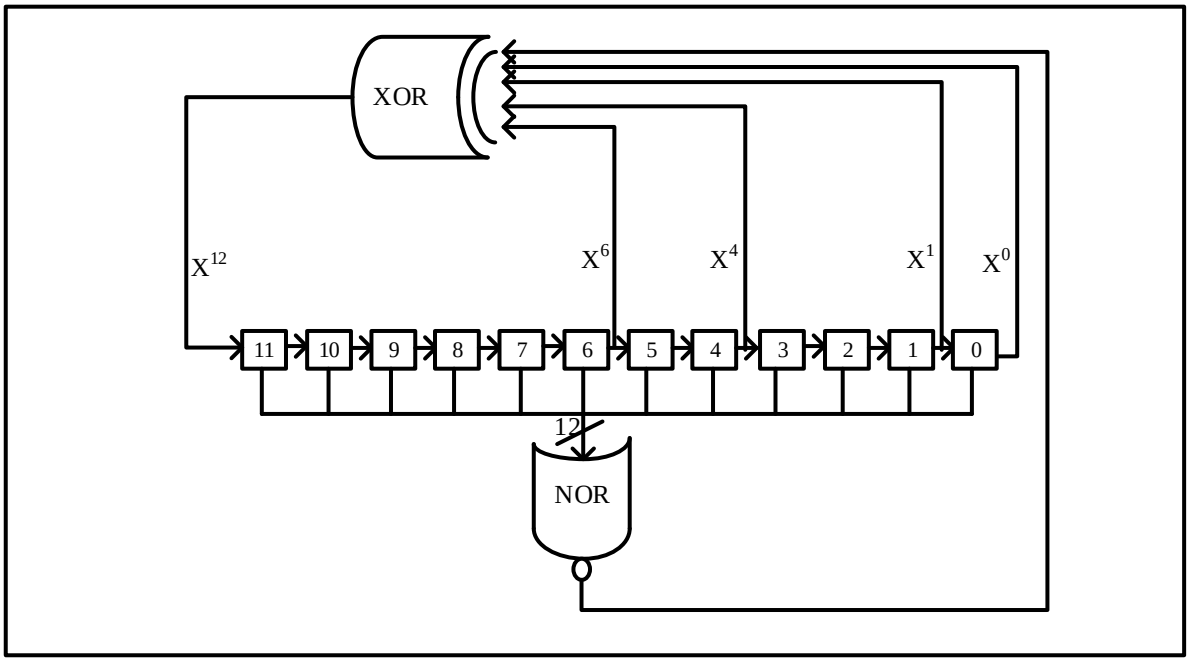
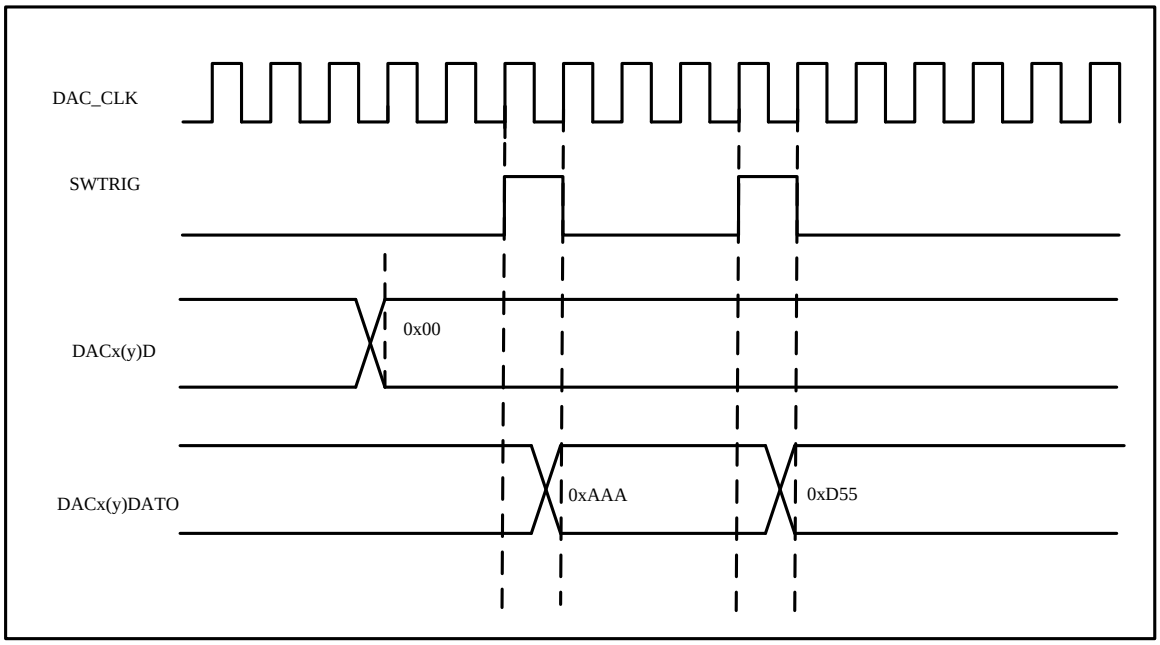


Figure 27-6 DAC Conversion with LFSR Waveform Generation (Enable Software Trigger)



Note: DAC must be configured for trigger enable (DACxy_CTRL.Tx(y)EN = 1) to generate noise.

27.3.9 Triangular Wave Generation

DAC can generate a triangular wave by configuring DACxy_CTRL.Wx(y)EN[2:0] as 3b'010 to enable the triangular wave function. By configuring DACxy_SELCTRL.MAx(y)SEL[3:0] to select the amplitude of the triangular wave, the internal triangular wave counter value is added to the value of the aligned data hold register and then written to the DACx(y)_DATO register (overflow bits are discarded). The triangular wave counter value is updated three

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bus_clk cycles after the trigger event occurs, and the triangular wave counter will accumulate to the set maximum amplitude, then decrement to 0, repeating this cycle.

Figure 27-7 DAC Triangular Wave Generation

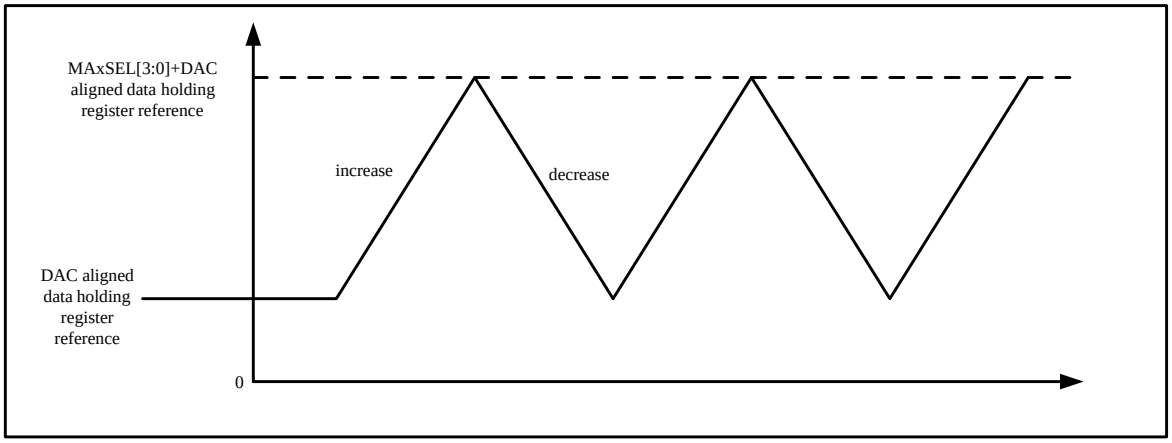
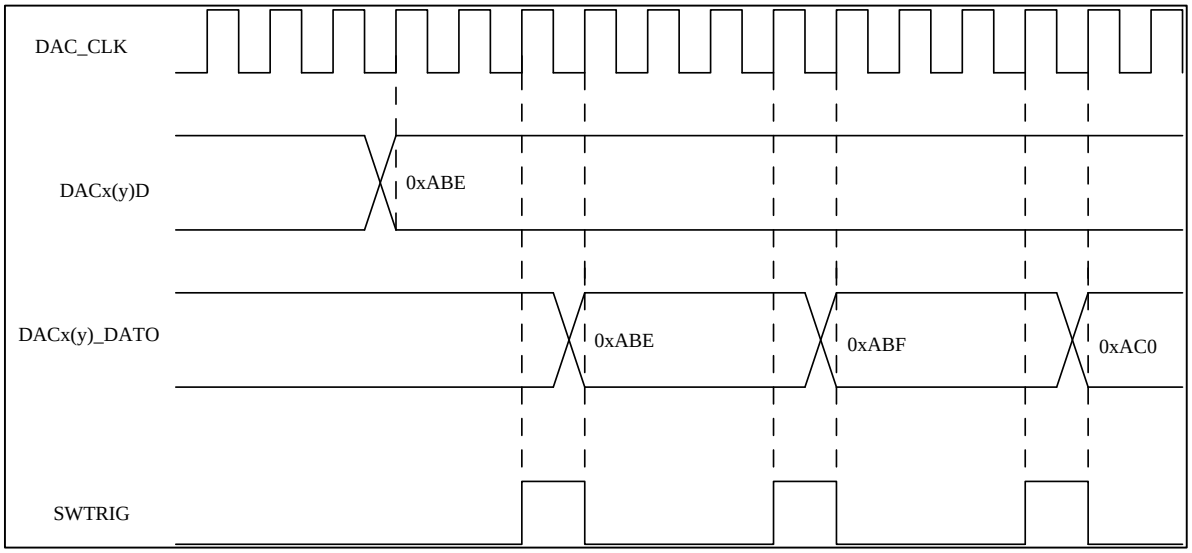


Figure 27-8 DAC Conversion with Triangular Wave Generation (Enable Software Trigger, HFSEL[1:0] = 0b'01)



Note:

1. *DAC must be configured for trigger enable (DACxy_CTRL.Tx(y)EN = 1) to generate a triangular wave;*
2. *It is not allowed to set DACxy_SELCTRL.MAx(y)SEL[3:0] after enabling the DAC.*

27.3.10 Sawtooth Wave Generation

The steps for generating a sawtooth wave are as follows:

1. Configure DACxy_CTRL.Wx(y)EN[2:0] as 3b'100 or 3b'110 to select either an increasing sawtooth wave or a decreasing sawtooth wave;
2. Set the values of DACxy_SELCTRL.Tx(y)SEL[4:0] and DACxy_SELCTRL.STINCSELx(y)[4:0] to configure the reset trigger source and step trigger source for the sawtooth wave respectively;

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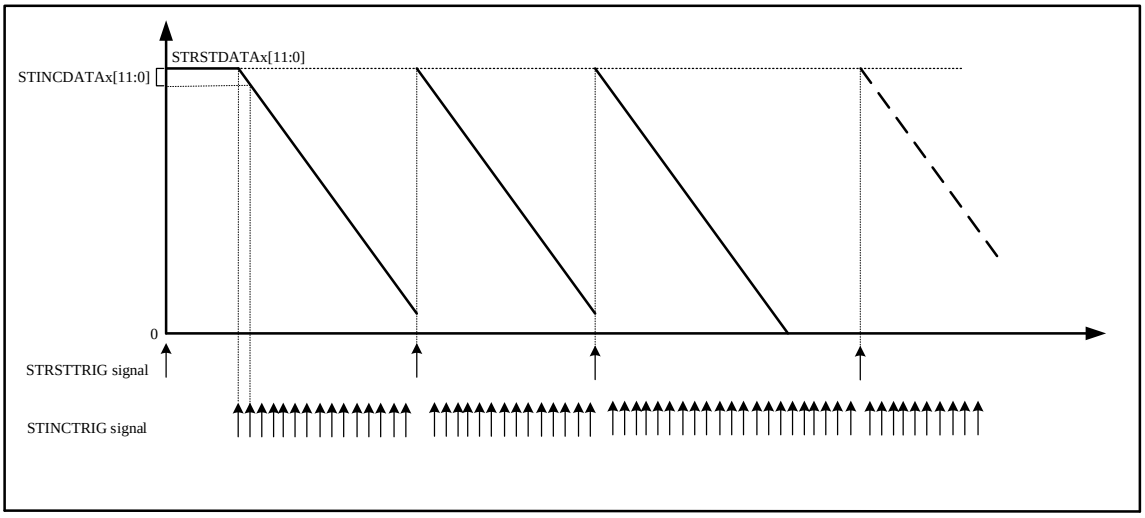
3. Configure the reset value of the sawtooth wave by setting DACxy_STRST.STRSTDATAx(y)[11:0];

4. Configure the step value of the sawtooth wave by setting DACxy_STRST.STINCDATAx(y)[11:0].

When configured as an increasing sawtooth wave, the sawtooth wave starts counting from DACxy_STRST.STRSTDATAx[11:0]. With each step trigger, the counter increases by DACxy_STRST.STINCDATAx(y)[11:0]. When the counter reaches the saturation value of 0xFFF, another step trigger will put the counter in a saturated state. Upon a reset trigger, the counter will reset to DACxy_STRST.STRSTDATAx(y)[11:0].

When configured as a decreasing sawtooth wave, the sawtooth wave starts counting from DACxy_STRST.STRSTDATAx(y)[11:0]. With each step trigger, the counter decreases by DACxy_STRST.STINCDATAx(y)[11:0]. When the counter reaches the saturation value of 0x000, another step trigger will put the counter in a saturated state. Upon a reset trigger, the counter will reset to DACxy_STRST.STRSTDATAx(y)[11:0].

Figure 27-9 Decreasing Sawtooth Wave Generation



The reset trigger signal STRSTTRIG for the sawtooth wave has higher priority than the step trigger signal STINCTRIG, and the external trigger rate for the sawtooth wave must not exceed the update rate of the DAC. If the step trigger signal DACxy_SELCTRL.STINCSELx(y)[4:0] is higher than the DAC's update rate, the trigger signal will be ignored. If a reset trigger signal STRSTTRIG is suddenly applied after responding to the step trigger signal STINCTRIG, STRSTTRIG will be paused. Then, a reset trigger will be immediately responded to after data increment or decrement.

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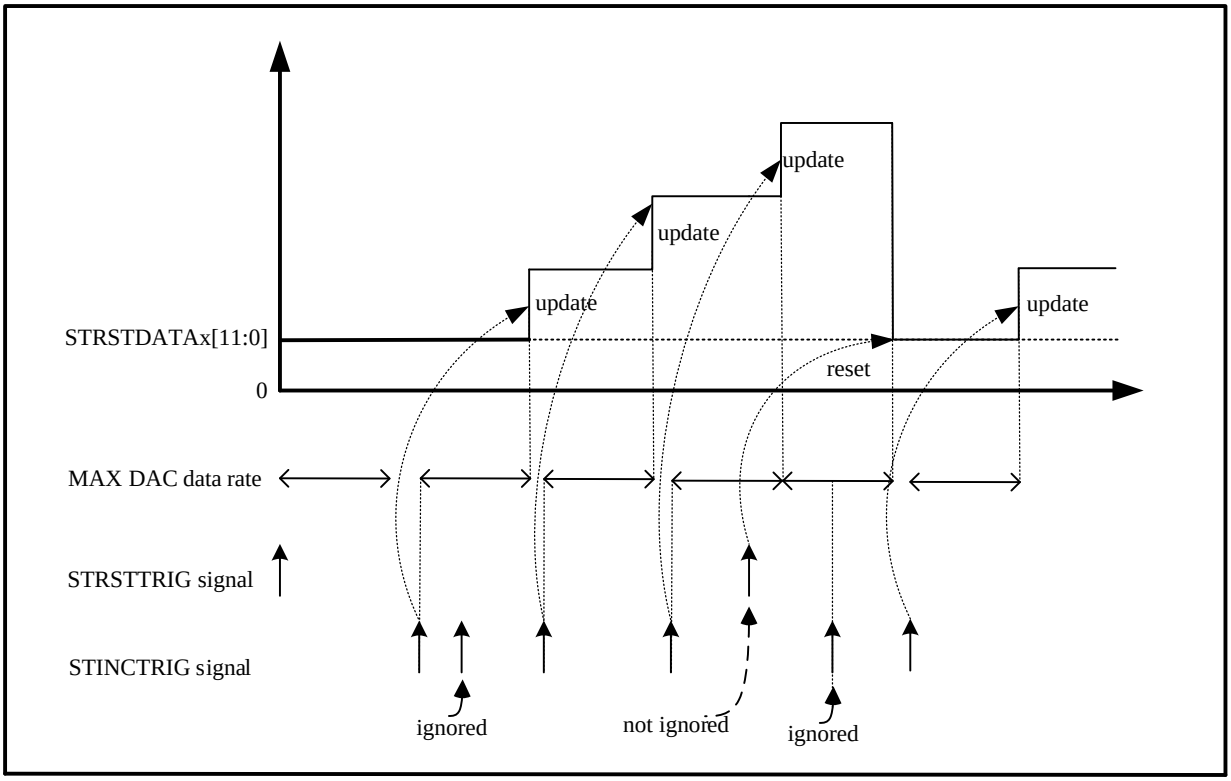
Figure 27-10 DAC Increasing Sawtooth Wave Reset Signal Trigger Priority over Step Trigger



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27.3.11 DAC Buffer Calibration

The formula for an N-bit DAC converter is as follows:

$$V_{OUT} = (\mathrm{Din}/2^N) \times \mathrm{Gain} \times V_{REF} + V_{OFFSET}$$

Where: VOUT is the analog voltage output, Din is the digital input, Gain is the gain error, VREF is the full-scale voltage, VOFFSET is the offset voltage. For an ideal DAC, Gain = 1, VOFFSET = 0.

Due to the output buffer characteristics, voltage offsets may differ between different components and introduce absolute offset errors on the analog output. To compensate for this voltage offset (VOFFSET), calibration is required through trimming techniques. Calibration is only effective when DACx is operating with the buffer enabled (BxEN = 0b'1). It is ineffective if applied in other modes with the buffer disabled. During the calibration process:

- Output disconnected from external pins or internal connections.
- Buffer acting as a comparator, sensing the mid-code value 0x800, and comparing it with the VREF+/2 signal through an internal bridge

Conducting a comparison, and then based on the comparison result (DACxy_STS.CALFLAGx(y) bit), switching its output signal to 0 or 1.

There are two calibration modes: factory calibration and user calibration, users can choose

1. Factory calibration:

   This calibration value is set during manufacturing, and upon DAC reset, it will be loaded into the DACxy_CALC.OTRIMx(y)[4:0] register.

2. User calibration:

   User trimming can be performed under operating conditions different from the nominal factory trimming conditions, especially when VDDA voltage, temperature, and VREF+ values change. User trimming can be done at any point in the application software. The factory calibration environment can be referenced in the datasheet.

The user calibration steps are as follows:

1） Enable DAC calibration (DACxy_CTRL.CALx(y)EN = 1)；

2） Enable the buffer mode for the DAC (DACxy_CTRL.Bx(y)EN = 1);

3）Enable the DAC (DACxy_CTRL.DAC(y)EN = 1)；

4）Apply calibration algorithm:

a) Write 00000b to DACxy_CALC.OTRIMx(y)[4:0];

b) Wait for at least 100us and check if the status register DACxy_STS.CALFLAGx(y) bit is set to 1?

c) If the status is set to 1, end the calibration; otherwise, write 00001b to DACxy_CALC.OTRIMx(y)[4:0] and repeat the above steps.

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Software algorithms can use successive approximation or binary search techniques to quickly calculate and set the contents of DACxy_CALC.OTRIMx(y)[4:0] bits. The toggling of the DACxy_STS.CALFLAGx(y) bit indicates that the offset has been correctly compensated, and the corresponding trim code must be retained in the DACxy_CALC.OTRIMx(y)[4:0] bits.

If during device operation VDDA, VREF+, and temperature conditions remain unchanged but it more frequently enters STANDBY or VBAT mode, the software can store the DACxy_CALC.OTRIMx(y)[4:0] bits found during the initial user calibration in flash or backup registers. Then, upon power recovery of the device, these bits can be directly loaded/written to avoid waiting for a new calibration time. When the DACxy_CTRL.CALx(y)EN bit is set, the DACxy_CTRL.DACx(y)EN bit must be set to enable the calibration function.

27.4 Dual DAC Conversion Operation

The two DACs can operate independently or simultaneously. In this mode, there are three registers available: DACxy_DR12D, DACxy_DL12D, and DACxy_DR8D, which can efficiently utilize the bus bandwidth, allowing simultaneous operation on both DAC channels with each register.

When both DACs are enabled for conversion simultaneously, there are a total of 15 modes available. In the case of using only one DAC for conversion, the other DAC can still operate independently. Please refer to the description in the following section for details.

27.4.1 Independent Trigger without Waveform Generator

Configuration process as follows:

- Enable DACx and DACy trigger by configuring DACxy_CTRL.TxEN and DACxy_CTRL.TyEN.
- Select different trigger sources by setting DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to different values.
- Choose not to use the waveform generator by setting DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] to "000".
- Place the desired data for conversion into the corresponding aligned data hold registers.

When a trigger event occurs for DACx, the value of the aligned data hold register will be transferred to the DACx_DATO register after a delay of 3 bus_clk clock cycles. When a trigger event occurs for DACy, the value of the aligned data hold register will be transferred to the DACy_DATO register after a delay of 3 bus_clk clock cycles.

27.4.2 Independent Trigger for Generating Identical Noise

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Configure DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] with different values to select different trigger sources.
- Configure DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "001" to enable noise generation.
- Configure DAC_SELCTRL.MAxSEL[3:0] and DAC_SELCTRL.MAySEL[3:0] with the same value to obtain

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the same LFSR register mask bit.

- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event is generated by DACx, the counter value of LFSR register 1 is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 1 is updated at this time. When a trigger event is generated by DACy, the counter value of LFSR register 2 is added to the value of the corresponding data holding register. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 2 is updated at this time.

27.4.3 Generating Independent Triggers for Different Noises

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Configure DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] with different values to select different trigger sources.
- Configure DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "001" to enable noise generation.
- Configure DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] with different values to obtain different LFSR register mask bits.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event is generated by DACx, the counter value of LFSR register 1 is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 1 is updated at this time. When a trigger event is generated by DACy, the counter value of LFSR register 2 is added to the value of the corresponding data holding register. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 2 is updated at this time.

27.4.4 Generating Independent Triggers for the Same Triangle Wave

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Configure DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] with different values to select different trigger sources.
- Configure DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "010" to enable triangle wave generation.
- Configure DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] with the same value to obtain the same triangle wave amplitude.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event is generated by DACx, the triangle wave amplitude is added to the value of the corresponding

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data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, and the counter value of DACx's triangle wave is updated at this time. When a trigger event is generated by DACy, the triangle wave amplitude is added to the value of the corresponding data holding register. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, and the counter value of DACy's triangle wave is updated at this time.

27.4.5 Generating Independent Triggers for Different Triangle Waves

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Configure DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] with different values to select different trigger sources.
- Configure DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "010" to enable triangle wave generation.
- Configure DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] with different values to obtain different triangle wave amplitudes.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event is generated by DACx, the triangle wave amplitude is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, and the counter value of DACx's triangle wave is updated at this time. When a trigger event is generated by DACy, the triangle wave amplitude is added to the value of the corresponding data holding register. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, and the counter value of DACy's triangle wave is updated at this time.

27.4.6 Generating Independent Triggers for the Same Sawtooth Wave

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Configure DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] with different values to select different reset trigger sources.
- Configure DAC_SELCTRL.STINCSELx[4:0] and DAC_SELCTRL.STINCSELy[4:0] with different values to select different increment trigger sources.
- Configure DAC_STINC.STINCDATAx[11:0] and DAC_STINC.STINCDATAy[11:0] with the same value as the step value for the sawtooth wave.
- Configure DAC_STRST.STRSTDATAx[11:0] and DAC_STRST.STRSTDATAy[11:0] with the same value as the reset value for the sawtooth wave.
- Configure DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "100" or "110" to enable sawtooth wave generation.
- Enable the corresponding external triggers.

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When a reset event is triggered by DACx, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAx[11:0] register to the DACx_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACx's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will increase or decrease by DAC_STINC.STINCDATAx[11:0], and the result of the operation will be passed to the DACx_DATO register after a delay of 3 bus_clk clock cycles. When a reset event is triggered by DACy, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAy[11:0] register to the DACy_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACy's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will increase or decrease by DAC_STINC.STINCDATAy[11:0], and the result of the operation will be passed to the DACy_DATO register after a delay of 3 bus_clk clock cycles.

27.4.7 Generating Independent Triggers for Different Sawtooth Waves

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Configure DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] with different values to select different reset trigger sources.
- Configure DAC_SELCTRL.STINCSELx [4:0] and DAC_SELCTRL.STINCSELy[4:0] with different values to select different increment trigger sources.
- Configure DAC_STINC.STINCDATAx [11:0] and DAC_STINC.STINCDATAy[11:0] with different values as the step value for the sawtooth wave.
- Configure DAC_STRST.STRSTDATAx[11:0] and DAC_STRST.STRSTDATAy[11:0] with different values as the reset value for the sawtooth wave.
- Configure DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "100" or "110" to enable sawtooth wave generation.
- Enable the corresponding external triggers.

When a reset event is triggered by DACx, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAx[11:0] register to the DACx_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACx's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will subtract DAC_STINC.STINCDATAx[11:0], and the result of the operation will be passed to the DACx_DATO register after a delay of 3 bus_clk clock cycles. When a reset event is triggered by DACy, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAy[11:0] register to the DACy_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACy's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will subtract DAC_STINC.STINCDATAy[11:0], and the result of the operation will be passed to the DACy_DATO register after a delay of 3 bus_clk clock cycles.

27.4.8 Simultaneous Software Startup

Configuration process as follows:

- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to "00000" to choose software as the

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trigger source.

- Enable DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to activate trigger enable for DACx and DACy.
- Place the required conversion data into the corresponding aligned data holding registers.
- Enable DAC_SOTTR.TRxEN and DAC_SOTTR.TRyEN to trigger software conversion.

The value of DACx's aligned data holding register will be passed to the DACx_DATO register after a delay of 1 bus_clk clock cycle.

The value of DACy's aligned data holding register will be passed to the DACy_DATO register after a delay of 1 bus_clk clock cycle.

27.4.9 Synchronous Trigger without Using Waveform Generators

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to the same value to select the same trigger source.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "000" to choose not to use waveform generators.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event occurs, the value of DACx's aligned data holding register will be passed to the DACx_DATO register after a delay of 3 bus_clk clock cycles; the value of DACy's aligned data holding register will be passed to the DACy_DATO register after a delay of 3 bus_clk clock cycles.

27.4.10 Generating Synchronous Triggers for the Same Noise

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to the same value to select the same trigger source.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "001" to enable noise generation.
- Set DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] to the same value to obtain the same LFSR register mask bits.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event occurs, the counter value of LFSR register 1 is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 1 is updated at this time. Similarly, the counter value of LFSR register 2 is added to the value of the corresponding data holding register when a trigger event occurs. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 2 is updated at

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Email: sales@nsing.com.sg

this time.

27.4.11 Generating Synchronous Triggers for Different Noises

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to different values to select the same trigger source.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "001" to enable noise generation.
- Set DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] to different values to obtain the same LFSR register mask bits.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event occurs, the counter value of LFSR register 1 is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 1 is updated at this time. Similarly, the counter value of LFSR register 2 is added to the value of the corresponding data holding register when a trigger event occurs. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, and the counter value of LFSR register 2 is updated at this time.

27.4.12 Generating Synchronous Triggers for the Same Triangle Wave

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to the same value to select the same trigger source.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "010" to enable triangle wave generation.
- Set DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] to the same value to obtain the same triangle wave amplitude.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event occurs, the triangle wave amplitude of DACx is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, updating the counter value of DACx's triangle wave at that time. Similarly, the triangle wave amplitude of DACy is added to the value of the corresponding data holding register when a trigger event occurs. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, updating the counter value of DACy's triangle wave at that time.

27.4.13 Generating Synchronous Triggers for Different Triangle Waves

Configuration process as follows:

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- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to the same value to select the same trigger source.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "010" to enable triangle wave generation.
- Set DACxy_SELCTRL.MAxSEL[3:0] and DACxy_SELCTRL.MAySEL[3:0] to different values to obtain different triangle wave amplitudes.
- Place the desired conversion data into the corresponding aligned data holding registers.

When a trigger event occurs, the triangle wave amplitude of DACx is added to the value of the corresponding data holding register. This sum is then passed to the register DACx_DATO after a delay of 3 bus_clk clock cycles, updating the counter value of DACx's triangle wave at that time. Similarly, the triangle wave amplitude of DACy is added to the value of the corresponding data holding register when a trigger event occurs. This sum is then passed to the register DACy_DATO after a delay of 3 bus_clk clock cycles, updating the counter value of DACy's triangle wave at that time.

27.4.14 Generating Synchronous Triggers for the Same Sawtooth Wave

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to the same value to select the same reset trigger source.
- Set DAC_SELCTRL.STINCSELx[4:0] and DAC_SELCTRL.STINCSELy[4:0] to the same value to select the same increment trigger source.
- Set DAC_STINC.STINCDATAx[11:0] and DAC_STINC.STINCDATAy[11:0] to the same value as the step value for the sawtooth wave.
- Set DAC_STRST.STRSTDATAx[11:0] and DAC_STRST.STRSTDATAy[11:0] to the same value as the reset value for the sawtooth wave.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "100" or "110" to enable sawtooth wave generation.
- Enable the corresponding external triggers.

When a reset event is triggered by DACx, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAx[11:0] register to the DACx_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACx's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will increase or decrease by DAC_STINC.STINCDATAx[11:0], and the result of the operation will be passed to the DACx_DATO register after a delay of 3 bus_clk clock cycles. When a reset event is triggered by DACy, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAy[11:0] register to the DACy_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACy's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will increase or decrease by DAC_STINC.STINCDATAy[11:0], and the result of the operation will be passed to the DACy_DATO register after

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a delay of 3 bus_clk clock cycles.

27.4.15 Generating Synchronous Triggers for Different Sawtooth Waves

Configuration process as follows:

- Configure DACxy_CTRL.TxEN and DACxy_CTRL.TyEN to enable DACx and DACy trigger.
- Set DAC_SELCTRL.TxSEL[4:0] and DAC_SELCTRL.TySEL[4:0] to the same value to select the same reset trigger source.
- Set DAC_SELCTRL.STINCSELx[4:0] and DAC_SELCTRL.STINCSELy[4:0] to the same value to select the same increment trigger source.
- Set DAC_STINC.STINCDATAx[11:0] and DAC_STINC.STINCDATAy[11:0] to different values as the step value for the sawtooth wave.
- Set DAC_STRST.STRSTDATAx[11:0] and DAC_STRST.STRSTDATAy[11:0] to different values as the reset value for the sawtooth wave.
- Set DACxy_CTRL.WxEN[2:0] and DACxy_CTRL.WyEN[2:0] as "100" or "110" to enable sawtooth wave generation.
- Enable the corresponding external triggers.

When a reset event is triggered by DACx, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAx[11:0] register to the DACx_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACx's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will increase or decrease by DAC_STINC.STINCDATAx[11:0], and the result of the operation will be passed to the DACx_DATO register after a delay of 3 bus_clk clock cycles. When a reset event is triggered by DACy, the sawtooth wave will pass the value of DAC_STRST.STRSTDATAy[11:0] register to the DACy_DATO register after a delay of 3 bus_clk clock cycles, updating the counter value of DACy's sawtooth wave at that time. When an increment event is triggered, the counter of the sawtooth wave will increase or decrease by DAC_STINC.STINCDATAy[11:0], and the result of the operation will be passed to the DACy_DATO register after a delay of 3 bus_clk clock cycles.

27.5 DAC Interrupt

If when the external trigger arrives for DAC, DMA has not yet responded to the previous external trigger request, then DAC will not issue a new request. Instead, it will set the DAC_STS.DMAUDRx(y) flag to report an error condition. This flag can be cleared by writing a 1 through software.

If the DACxy_CTRL.DMAUDRx(y)IEN bit is enabled, an interrupt will be generated at this time. This interrupt can wake the chip from SLEEP mode.

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27.6 Registers

27.6.1 DACxy Control Register（DACxy_CTRL）(xy = 12、34、56)

Offset address: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	TROVCyIEN	EXOUTDACy	INOUTDACy	CALyEN	WyEN			SINFROMATy	DMADOUBLEy	HDByEN	DMAUDRyIEN	TyEN	ByEN	DMAyEN	DACyEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TROVCxIEN	EXOUTDACx	INOUTDACx	CALxEN	WxEN			SINFROMATx	DMADOUBLEx	HDBxEN	DMAUDRxIEN	TxEN	BxEN	DMAxEN	DACxEN
	rw	rw	rw	rw	rw			rw	rw	rw	rw	rw	rw	rw	rw

Field offset	Register name	Description
31	Reserved	Reserved, the reset value must be maintained
30	TROVCyIEN	DACy trigger overclock interrrupt enable This bit is set and cleared by software. 0: DACy trigger interrrupt overclock interrupt disabled 1: DACy trigger interrrupt overclock interrupt enabled
29	EXOUTyEN	DACy external output channel enable. This bit set and cleared by software to enable/disable DACy external output channel. 0: DACy external output disabled 1: DACy external output enabled *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
28	INOUTyEN	DACy internal output channel enable. This bit set and cleared by software to enable/disable DACy internal output channel. 0: DACy internal output disabled 1: DACy internal output enabled *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
27	CALyEN	DACy calibration enable This bit is set and cleared by software to enable/disable DACy calibration, it can be written only if DACyEN bit is set to 0 into DACxy_CTRL(the calibration mode can be entered/exit only when the DAC channel is disabled)Otherwise, the write operation is ignored. 0: DACy in nomal operating mode 1: DACy in calibration mode *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3,*

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Field offset	Register name	Description
		DAC4, DAC5, and DAC6.
26:24	WyEN[2:0]	DACy noise/triangle wave/sawtooth wave generation enable These bits are set/reset by software. 000: wave generation disabled 001: Noise wave generation enabled 010: Triangle wave generation enabled 100: increase sawtooth wave generation enable 110: decrease sawtooth wave generation enable *Note: only used if bit TyEN = 1 (DACy trigger enabled)*
23	SINFORMATy	DACy signed format enable This bit is set and cleared by software. 0: DACy input data is in unsigned format 1: DACy input data is in signed format.The MSB bit represents the sign
22	DMADOUBLEy	DACy DMA double data mode This bit is set and cleared by software. 0: DACy DMA normal mode selected 1: DACy DMA double data mode selected
21	HDByEN	DACy drive buffer enable This bit is set and cleared by software. 0: DACy output normal drive 1: DACy output high drive *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
20	DMAUDRyIEN	DACy DMA Underrun Interrupt enable This bit is set and cleared by software. 0: DACy DMA Underrun Interrupt disabled 1: DACy DMA Underrun Interrupt enabled
19	TyEN	DACy trigger enable This bit set and cleared by software to enable/disable DACy trigger 0：DACy trigger disable 1：DACy trigger enable
18	ByEN	DACy output buffer enable This bit set and cleared by software to enable/disable DACy output buffer. 0: DACy output buffer disabled 1: DACy output buffer enabled *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
17	DMAyEN	DACy DMA enable This bit is set and cleared by software. 0: DACy DMA mode disabled 1: DACy DMA mode enabled
16	DACyEN	DACy enable

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Field offset	Register name	Description
		This bit set and cleared by software to enable/disable DACy. 0: DACy disabled 1: DACy enabled
15	Reserved	Reserved, the reset value must be maintained
14	TROVCxIEN	DACx trigger overclock interrrupt enable This bit is set and cleared by software. 0: DACx trigger interrrupt overclock interrupt disabled 1: DACx trigger interrrupt overclock interrupt enabled
13	EXOUTxEN	DACx external output channel enable. This bit set and cleared by software to enable/disable DACx external output channel. 0: DACx external output disabled 1: DACx external output enabled *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
12	INOUTxEN	DACx internal output channel enable. This bit set and cleared by software to enable/disable DACx internal output channel. 0: DACx internal output disabled 1: DACx internal output enabled *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
11	CALxEN	DACx calibration enable This bit is set and cleared by software to enable/disable DAC 1 calibration. 0: DAC1 in nomal operating mode 1: DAC1 in calibration mode *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
10:8	WEN[2:0]	DACx noise/triangle wave/sawtooth wave generation enable These bits are set/reset by software. 000: wave generation disabled 001: Noise wave generation enabled 010: Triangle wave generation enabled 100: increase sawtooth wave generation enable 110: decrease sawtooth wave generation enable *Note: only used if bit TxEN = 1 (DACx trigger enabled)*
7	SINFORMATx	DACx signed format enable This bit is set and cleared by software. 0: DACx input data is in unsigned format 1: DACx input data is in signed format.The MSB bit represents the sign
6	DMADOUBLEx	DACx DMA double data mode This bit is set and cleared by software. 0: DACx DMA normal mode selected

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Field offset	Register name	Description
		1: DACx DMA double data mode selected
5	HDBxEN	DACx drive buffer enable This bit is set and cleared by software. 0: normal drive 1: high drive *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
4	DMAUDRxIEN	DACx DMA Underrun Interrupt enable This bit is set and cleared by software. 0: DACx DMA Underrun Interrupt disabled 1: DACx DMA Underrun Interrupt enabled
3	TxEN	DACx trigger enable This bit set and cleared by software to enable/disable DACx trigger 0: DACx trigger disabled 1: DACx trigger enabled
2	BxEN	DACx output buffer enable This bit set and cleared by software to enable/disable DACx output buffer. 0: DACx output buffer disabled 1: DACx output buffer enabled *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
1	DMAxEN	DACx DMA enable This bit is set and cleared by software. 0: DACx DMA mode disabled 1: DACx DMA mode enabled
0	DACxEN	DACx enable This bit set and cleared by software to enable/disable DACx. 0: DACx disabled 1: DACx enabled

27.6.2 DACxy Software Trigger Register（DACxy_SOTTR）

Offset address:：0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														TRByEN	TRBxEN
														w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														TRyEN	TRxEN

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w w

Field offset	Register name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	TRByEN	Enable sawtooth wave step trigger for DACy. This bit is set to 1 by software to enable/disable software triggering. This signal is only used for the sawtooth wave step trigger signal. 0: Disable software triggering for DACy sawtooth wave step; 1: Enable software triggering for DACy sawtooth wave step.
16	TRBxEN	Enable sawtooth wave step trigger for DACx. This bit is set to 1 by software to enable/disable software triggering. This signal is only used for the sawtooth wave step trigger signal. 0: Disable software triggering for DACx sawtooth wave step; 1: Enable software triggering for DACx sawtooth wave step.
15:2	Reserved	Reserved, the reset value must be maintained
1	TRyEN	DACy software trigger enable. This bit is set to 1 by the software to enable/disable software triggering. This signal can be used as the trigger signal for triangle wave/noise wave, or as the reset trigger signal for sawtooth wave. 0: Disable DACy software trigger; 1: Enable DACy software trigger.
0	TRxEN	DACx software trigger enable. This bit is set to 1 by the software to enable/disable software triggering. This signal can be used as the trigger signal for triangle wave/noise wave, or as the reset trigger signal for sawtooth wave. 0: Disable DACx software trigger; 1: Enable DACx software trigger.

27.6.3 DACx Data Output Register（DACx_DATO）

Offset address: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DACxDO[11:0]											
				r											

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位域	名称	描述
31:12	Reserved	Reserved, the reset value must be maintained
11:0	DACxDO[11:0]	DACx data output These bits are read only, they contain data output for DACx

27.6.4 DACy Data Output Register（DACy_DATO）

Offset address: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DACyDO[11:0]											
				r											

Field offset	Register name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	DACyDO[11:0]	DACy data output These bits are read only, they contain data output for DACy

27.6.5 DACx 8-bit right-aligned data holding register（DACx_DR8）

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACxDB[7:0]								DACxD[7:0]							
rw								rw							

Field offset	Register name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	DACxDB[7:0]	DACx 8-bit right-aligned data B These bits are written by software.They specify 8-bit data for DACx when the DAC operates in double data mode

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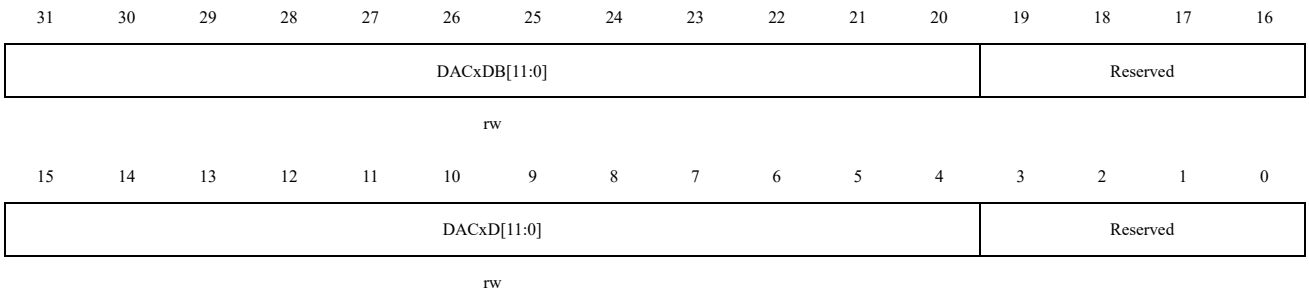
Field offset	Register name	Description
7:0	DACxD[7:0]	DACx 8-bit right-aligned data These bits are written by software.They specify 8-bit data for DACx.

27.6.6 DACx 12-bit left-aligned data holding register（DACx_DL12）

Offset address: 0x14

Reset value: 0x0000 0000

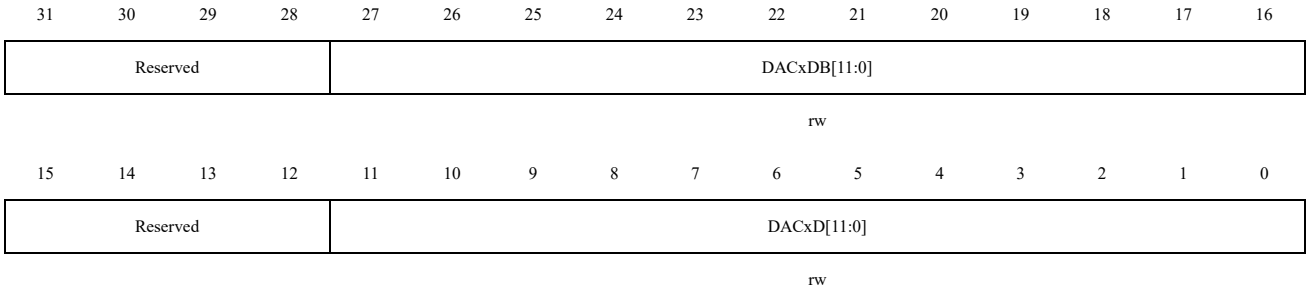


Field offset	Register name	Description
31:20	DACxDB[11:0]	DACx 12-bit left-aligned data B These bits are written by software.They specify 12-bit data for DACx when the DAC operates in double data mode
19:16	Reserved	Reserved, the reset value must be maintained
15:4	DACxD[11:0]	DACx 12-bit left-aligned data These bits are written by software.They specify 12-bit data for DACx.
3:0	Reserved	Reserved, the reset value must be maintained

27.6.7 DACx 12-bit right-aligned data holding register（DACx_DR12）

Offset address: 0x18

Reset value: 0x0000 0000



Field offset	Register name	Description
31:28	Reserved	Reserved, the reset value must be maintained

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Field offset	Register name	Description
27: 16	DACxDB[11:0]	DACx 12-bit right-aligned data B These bits are written by software.They specify 12-bit data for DACx when the DAC operates in double data mode
15:12	Reserved	Reserved, the reset value must be maintained
11:0	DACxD[11:0]	DACx 12-bit right-aligned data These bits are written by software.They specify 12-bit data for DACx.

27.6.8 DACy 8-bit right-aligned data holding register（DACy_DR8）

Offset address: 0x1C

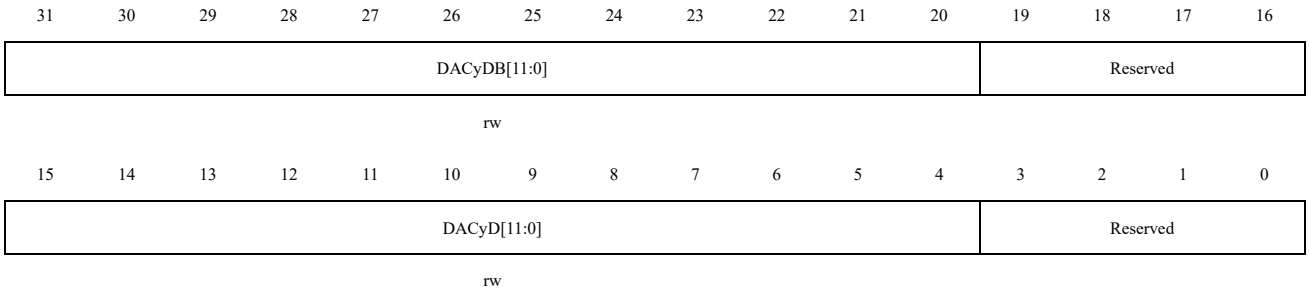
Reset value: 0x0000 0000

Field offset	Register name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	DACyDB[7:0]	DACy 8-bit right-aligned data B These bits are written by software.They specify 8-bit data for DACy when the DAC operates in double data mode
7:0	DACyD[7:0]	DACy 8-bit right-aligned data These bits are written by software.They specify 8-bit data for DACy.

27.6.9 DACy 12-bit left-aligned data holding register（DACy_DL12）

Offset address: 0x20

Reset value: 0x0000 0000



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Field offset	Register name	Description
31:20	DACyDB[11:0]	DACy 12-bit left-aligned data B These bits are written by software.They specify 12-bit data for DACy when the DAC operates in double data mode
19:16	Reserved	Reserved, the reset value must be maintained
15:4	DACyD[11:0]	DACy 12-bit left-aligned data These bits are written by software.They specify 12-bit data for DACy.
3:0	Reserved	Reserved, the reset value must be maintained

27.6.10 DACy 12-bit right-aligned data holding register（DACy_DR12）

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				DACyDB[11:0]											
				rw											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DACyD[11:0]											
				rw											

Field offset	Register name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:16	DACyDB[11:0]	DACy 12-bit right-aligned data B These bits are written by software.They specify 12-bit data for DACy when the DAC operates in double data mode
15:12	Reserved	Reserved, the reset value must be maintained
11:0	DACyD[11:0]	DACy 12-bit right-aligned data These bits are written by software.They specify 12-bit data for DACy.

27.6.11 Dual DACxy's 8-bit right-aligned data holding register（DACxy_DR8D）

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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DACyD [7:0]	DACxD[7:0]
rw	rw

Field offset	Register name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	DACyD[7:0]	DACy 8-bit right-aligned data B These bits are written by software.They specify 8-bit data for DACy when the DAC operates in double data mode
7:0	DACxD[7:0]	DACx 8-bit right-aligned data These bits are written by software.They specify 8-bit data for DACx.

27.6.12 Dual DACxy's 12-bit left-aligned data holding register（DACxy_DL12D）

Offset address: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DACyD[11:0]												Reserved			
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACxD[11:0]												Reserved			
rw															

Field offset	Register name	Description
31:20	DACyD[11:0]	DACy 12-bit left-aligned data These bits are written by software.They specify 12-bit data for DACy.
19:16	Reserved	Reserved, the reset value must be maintained
15:4	DACxD[11:0]	DACx 12-bit left-aligned data These bits are written by software.They specify 12-bit data for DACx.
3:0	Reserved	Reserved, the reset value must be maintained

27.6.13 Dual DACxy's 12-bit right-aligned data holding register（DACxy_DR12D）

Offset address: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				DACyD[11:0]											
				rw											

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DACxD[11:0]											
				rw											

Field offset	Register name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:16	DACyD[11:0]	DACy 12-bit right-aligned data These bits are written by software.They specify 12-bit data for DACy.
15:12	Reserved	Reserved, the reset value must be maintained
11:0	DACxD[11:0]	DACx 12-bit right-aligned data These bits are written by software.They specify 12-bit data for DACx.

27.6.14 DACxy selection control register（DACxy_SELCTRL）

Offset address: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TySEL[4:0]					Reserved	MAySEL[3:0]				STINCSELy[4:0]					Reserved
rw						rw				rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxSEL[4:0]					Reserved	MAxSEL[3:0]				STINCSELx[4:0]					Reserved
rw						rw				rw					

Field offset	Register name	Description
31:27	TySEL[4:0]	DACy trigger selection for LFSR/triangle/sawtooth reset These bits select the external event used to trigger DACy 00000: software_trgo 00001: atim1_trgo 00010: atim2_trgo 00011: atim3_trgo 00100: atim4_trgo 00101: gtima1_trgo 00110: gtima2_trgo 00111: gtima3_trgo 01000: gtima4_trgo 01001: gtima5_trgo 01010: gtima6_trgo 01011: gtima7_trgo

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Field offset	Register name	Description
		01100: gtimb1_trgo 01101: gtimb2_trgo 01110: gtimb3_trgo 01111: exti5 10000: exti7 10001: exti9 10010: shrtim1_dac_reset_trg1 10011: shrtim1_dac_reset_trg2 10100: shrtim1_dac_reset_trg3 10101: shrtim1_dac_reset_trg4 10110: shrtim1_dac_reset_trg5 10111: shrtim1_dac_reset_trg6 11000: shrtim1_dac_trg1/2/3 11001: shrtim2_dac_reset_trg1 11010: shrtim2_dac_reset_trg2 11011: shrtim2_dac_reset_trg3 11100: shrtim2_dac_reset_trg4 11101: shrtim2_dac_reset_trg5 11110: shrtim2_dac_reset_trg6 11111: shrtim2_dac_trg1/2/3 *Note:* ● *only used if bit TxEN = 1 (DACx trigger enabled)；* ● *when 0b11111 or 0b11000 is selected, it corresponds to shrtimx_dac_trg1 for DAC1/2; shrtimx_dac_trg2 for DAC3/4; andshrtimx_dac_trg3 for DAC5/6.*
26	Reserved	Reserved, the reset value must be maintained
25:22	MAySEL[3:0]	DACy mask/amplitude selector These bits are written by software to select mask in wave generation mode or amplitude in triangle generation mode. 0000: Unmask bit0 of LFSR/ Triangle Amplitude equal to 1 0001: Unmask bits[1:0] of LFSR/ Triangle Amplitude equal to 3 0010: Unmask bits[2:0] of LFSR/ Triangle Amplitude equal to 7 0011: Unmask bits[3:0] of LFSR/ Triangle Amplitude equal to 15 0100: Unmask bits[4:0] of LFSR/ Triangle Amplitude equal to 31 0101: Unmask bits[5:0] of LFSR/ Triangle Amplitude equal to 63 0110: Unmask bits[6:0] of LFSR/ Triangle Amplitude equal to 127 0111: Unmask bits[7:0] of LFSR/ Triangle Amplitude equal to 255 1000: Unmask bits[8:0] of LFSR/ Triangle Amplitude equal to 511 1001: Unmask bits[9:0] of LFSR/ Triangle Amplitude equal to 1023 1010: Unmask bits[10:0] of LFSR/ Triangle Amplitude equal to 2047 ≥ 1011: Unmask bits[11:0] of LFSR/ Triangle Amplitude equal to 4095
21:17	STINCSELy[4:0]	DACy sawtooth increment trigger selection.

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Field offset	Register name	Description
		00000 : software_trgo 00001 : atim1_trgo 00010 : atim2_trgo 00011 : atim3_trgo 00100 : reserved 00101 : gtima1_trgo 00110 : gtima2_trgo 00111 : gtima3_trgo 01000 : gtima4_trgo 01001 : gtima5_trgo 01010 : gtima6_trgo 01011 : gtima7_trgo 01100 : gtimb1_trgo 01101 : gtimb2_trgo 01110 : gtimb3_trgo 01111: exti6 10000: exti8 10001: exti10 10010: shrtim1_step_trg1 10011: shrtim1_step_trg2 10100: shrtim1_step_trg3 10101: shrtim1_step_trg4 10110: shrtim1_step_trg5 10111: shrtim1_step_trg6 11000: reserved 11001: shrtim1_step_trg1 11010: shrtim1_step_trg2 11011: shrtim1_step_trg3 11100: shrtim1_step_trg4 11101: shrtim1_step_trg5 11110: shrtim1_step_trg6 11111: reserved These bits are available only on dual-channel DACs.
16	Reserved	Reserved, the reset value must be maintained
15:11	TxSEL[4:0]	DACx trigger selection for LFSR/triangle/sawtooth reset These bits select the external event used to trigger DACx 00000 : software_trgo 00001 : atim1_trgo 00010 : atim2_trgo 00011 : atim3_trgo 00100 : atim4_trgo 00101: gtima1_trgo

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Field offset	Register name	Description
		00110: gtima2_trgo 00111: gtima3_trgo 01000: gtima4_trgo 01001: gtima5_trgo 01010: gtima6_trgo 01011: gtima7_trgo 01100: gtimb1_trgo 01101: gtimb2_trgo 01110: gtimb3_trgo 01111 : exti5 10000 : exti7 10001 : exti9 10010 : shrtim1_dac_reset_trg1 10011 : shrtim1_dac_reset_trg2 10100 : shrtim1_dac_reset_trg3 10101 : shrtim1_dac_reset_trg4 10110 : shrtim1_dac_reset_trg5 10111 : shrtim1_dac_reset_trg6 11000 : shrtim1_dac_trg1/2/3 11001 : shrtim2_dac_reset_trg1 11010 : shrtim2_dac_reset_trg2 11011 : shrtim2_dac_reset_trg3 11100 : shrtim2_dac_reset_trg4 11101 : shrtim2_dac_reset_trg5 11110 : shrtim2_dac_reset_trg6 11111 : shrtim2_dac_trg1/2/3 *Note:* ● *only used if bit TxEN = 1 (DACx trigger enabled)；* ● *when 0b11111 or 0b11000 is selected, it corresponds to shrtimx_dac_trg1 for DAC1/2; to shrtimx_dac_trg2 for DAC3/4; to shrtimx_dac_trg3 for DAC5/6.*
10	Reserved	Reserved, the reset value must be maintained
9:6	MAxSEL[3:0]	DACx mask/amplitude selector These bits are written by software to select mask in wave generation mode or amplitude in triangle generation mode. 0000: Unmask bit0 of LFSR/ Triangle Amplitude equal to 1 0001: Unmask bits[1:0] of LFSR/ Triangle Amplitude equal to 3 0010: Unmask bits[2:0] of LFSR/ Triangle Amplitude equal to 7 0011: Unmask bits[3:0] of LFSR/ Triangle Amplitude equal to 15 0100: Unmask bits[4:0] of LFSR/ Triangle Amplitude equal to 31 0101: Unmask bits[5:0] of LFSR/ Triangle Amplitude equal to 63 0110: Unmask bits[6:0] of LFSR/ Triangle Amplitude equal to 127 0111: Unmask bits[7:0] of LFSR/ Triangle Amplitude equal to 255

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Field offset	Register name	Description
		1000: Unmask bits[8:0] of LFSR/ Triangle Amplitude equal to 511 1001: Unmask bits[9:0] of LFSR/ Triangle Amplitude equal to 1023 1010: Unmask bits[10:0] of LFSR/ Triangle Amplitude equal to 2047 ≥ 1011: Unmask bits[11:0] of LFSR/ Triangle Amplitude equal to 4095
5:1	STINCSELx[4:0]	DACx sawtooth increment trigger selection. 00000 : software_trgo 00001 : atim1_trgo 00010 : atim2_trgo 00011 : atim3_trgo 00100 : reserved 00101: gtima1_trgo 00110: gtima2_trgo 00111: gtima3_trgo 01000: gtima4_trgo 01001: gtima5_trgo 01010: gtima6_trgo 01011: gtima7_trgo 01100: gtimb1_trgo 01101: gtimb2_trgo 01110: gtimb3_trgo 01111: exti6 10000: exti8 10001: exti10 10010: shrtim1_step_trg1 10011: shrtim1_step_trg2 10100: shrtim1_step_trg3 10101: shrtim1_step_trg4 10110: shrtim1_step_trg5 10111: shrtim1_step_trg6 11000: reserved 11001: shrtim1_step_trg1 11010: shrtim1_step_trg2 11011: shrtim1_step_trg3 11100: shrtim1_step_trg4 11101: shrtim1_step_trg5 11110: shrtim1_step_trg6 11111: reserved These bits are available only on dual-channel DACs.
0	Reserved	Reserved, the reset value must be maintained

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27.6.15 DACxy status register（DACxy_STS）

Offset address: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											VFLAGx COMP	TROVC FLAGy	DOR STATy	CAL FLAGy	DMA UDRy
											r	rc_w1	r	r	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											VFLAGx COMP	TROVC FLAGx	DOR STATx	CAL FLAGx	DMA UDRx
											r	rc_w1	r	r	rc_w1

Field offset	Register name	Description
31:21	Reserved	Reserved, the reset value must be maintained
20	VFLAGyCOMP	DACy signal stability indicator for the comparator. 0: The signal from DACy to the comparator is unprocessed and may be unstable; 1: The signal from DACy to the comparator is processed and stable. *Note: This bit is only configurable for DAC3, DAC4, DAC5, DAC6, It is reserved as 0 for DAC1 and DAC2.*
19	TROVCFLAGy	DACy trigger source overrun interrupt flag. This bit is set by hardware and cleared by software (cleared by writing 1). 0: No trigger source overrun situation for DACy; 1: Trigger source overrun situation for DACy: The frequency at which the selected trigger source drives DACy conversion is faster than the speed of data updates.
18	DORSTATy	DACy data output register status bit. This bit is set and cleared by hardware and is available when DACy is operating in dual data mode. 0: DACyD is being used for DACy output data. 1: DACyDB is being used for DACy output data.
17	CALFLAGy	DACy calibration offset status. This bit is set and cleared by hardware. 0: Calibration adjustment value is less than the offset calibration value. 1: Calibration adjustment value is greater than or equal to the offset calibration value.
16	DMAUDRy	DACy DMA underrun interrupt flag. This bit is set by hardware and cleared by software (cleared by writing 1). 0: No DMA underrun error occurred for DACy; 1: DMA underrun error occurred for DACy (the frequency at which the selected trigger source drives DACy conversion is faster than the rate provided by DMA).
15:5	Reserved	Reserved, the reset value must be maintained
4	VFLAGxCOMP	VFLAGxCOMP

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Field offset	Register name	Description
		DACx signal stability indicator. 0: The signal from DACx to the comparator is unprocessed and may be unstable; 1: The signal from DACx to the comparator is processed and stable. *Note: This bit is only configurable for DAC3, DAC4, DAC5, DAC6. It is reserved as 0 for DAC1 and DAC2..*
3	TROVCFLAGx	DACx trigger source overrun flag. This bit is set by hardware and cleared by software (cleared by writing 1). 0: No trigger source overrun situation for DACx; 1: Trigger source overrun situation for DACx: The frequency at which the selected trigger source drives DACx conversion is faster than the speed of data updates.
2	DORSTATx	DACx data output register status bit. This bit is set and cleared by hardware and is available when DACx is operating in dual data mode. 0: DACxD is being used for DACx output data. 1: DACxDB is being used for DACx output data.
1	CALFLAGx	DACx calibration offset status. This bit is set and cleared by hardware. 0: The calibration adjustment value is less than the offset calibration value. 1: The calibration adjustment value is greater than or equal to the offset calibration value.
0	DMAUDRx	DACx DMA underrun flag. This bit is set by hardware and cleared by software (cleared by writing 1). 0: No DMA underrun error occurred for DACx; 1: DMA underrun error occurred for DACx (the frequency at which the selected trigger source drives DACx conversion is faster than the rate provided by DMA).

27.6.16 DACxy general control register（DACxy_GCTRL）

Offset address: 0x40

Reset value: 0x0077 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								PCS[7:0]							
r								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													HFSEL[1:0]		Reserved
r													rw		

Field offset	Register name	Description
31:24	Reserved	Reserved, the reset value must be maintained

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Field offset	Register name	Description
23:16	PCS[7:0]	DACx clock divider coefficient. When operating DACx as DAC1~DAC2: the operating frequency range of DACx is 4MHz to APB1_CLKmax. Configure the corresponding divider coefficient to achieve a maximum of 1M for DACxy_PCS[7:0] (x = 1, 2). For example, if the operating frequency of DAC1~2 is 150MHz, the corresponding divider coefficient is 10010101. When operating DACx as DAC3~DAC6: PCS[7:5] reserved as 0; the operating frequency range of DACx is 60MHz to AHB2_CLKmax. Configure the corresponding divider coefficient to achieve a maximum of 15M for DACxy_PCS[4:0] (x =3, 4, 5, 6). For example, if the operating frequency of DAC3~6 is 300MHz, the corresponding divider coefficient is 10011. 0: No division 1：Division by 2 2：Division by 3 …: Division by (PCS[7:0] + 1) *Note: If it is necessary to configure the DAC operating frequency to exceed 1MHz (DAC1, DAC2) or 15MHz (DAC3,DAC4,DAC5, DAC6), it is important to consider the maximum operating frequency of the DAC.*
15:3	Reserved	Reserved, the reset value must be maintained
2:1	HFSEL[1:0]	DACx and DACy response speed selection 00: DAC_DATO update rate is (PCS[7:0]/2) DAC_CLK cycles; this selection is the default value. 01: DAC_DATO update rate is 3 bus_clk cycles; (Fbus_clk < 80MHz) 10: DAC_DATO update rate is 5 bus_clk cycles; (80MHz < Fbus_clk < 160MHz) 11: DAC_DATO update rate is 7 bus_clk cycles; (Fbus_clk > 160MHz). *Note: This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
0	Reserved	Reserved, the reset value must be maintained

27.6.17 DACxy sawtooth wave step register（DACxy_STINC）

Offset address: 0x44

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				STINCDATAy[11:0]											
				rw											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				STINCDATAx[11:0]											
				rw											

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Field offset	Register name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:16	STINCDATAy[11:0]	DACy sawtooth wave step value. Range from 0 to 0xfff.
15:12	Reserved	Reserved, the reset value must be maintained
11:0	STINCDATAx[11:0]	DACx sawtooth wave step value. Range from 0 to 0xfff.

27.6.18 DACxy sawtooth wave reset register（DACxy_STRST）

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				STRSTDATAy[11:0]											
				rw											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				STRSTDATAx[11:0]											
				rw											

Field offset	Register name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:16	STRSTDATAy[11:0]	DACy sawtooth wave reset value. Range from 0 to 0xfff.
15:12	Reserved	Reserved, the reset value must be maintained
11:0	STRSTDATAx[11:0]	DACx sawtooth wave reset value. Range from 0 to 0xfff.

27.6.19 DACxy calibration control register（DACxy_CALC）

Offset address: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											OTRIMy[4:0]				
											rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											OTRIMx[4:0]				
											rw				

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Field offset	Register name	Description
31:21	Reserved	Reserved, the reset value must be maintained
20:16	OTRIMy[4:0]	DACy offset calibration value. *Note：* *1. Can only be used when ByEN=1.* *2. This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*
15:5	Reserved	Reserved, the reset value must be maintained
4:0	OTRIMx[4:0]	DACx offset calibration value. *Note：* *1. Can only be used when BxEN=1.* *2. This bit is only configurable for DAC1, DAC2. It is reserved as 0 for DAC3, DAC4, DAC5, and DAC6.*

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28 Comparator (COMP)

The COMP module is used to compare the analog voltages of two inputs and output high/low levels based on the comparison result. When ‘INP’ input voltage is higher than ‘INM’ input voltage, the comparator outputs are high level, when ‘INP’ input voltage is lower than ‘INM’ input voltage, the comparator outputs are low level.

28.1 COMP System Connection Block Diagram

The COMP module supports 4 independent comparators, which are connected to the APB5 bus.

Figure 28-1 COMP1&COMP2 connection

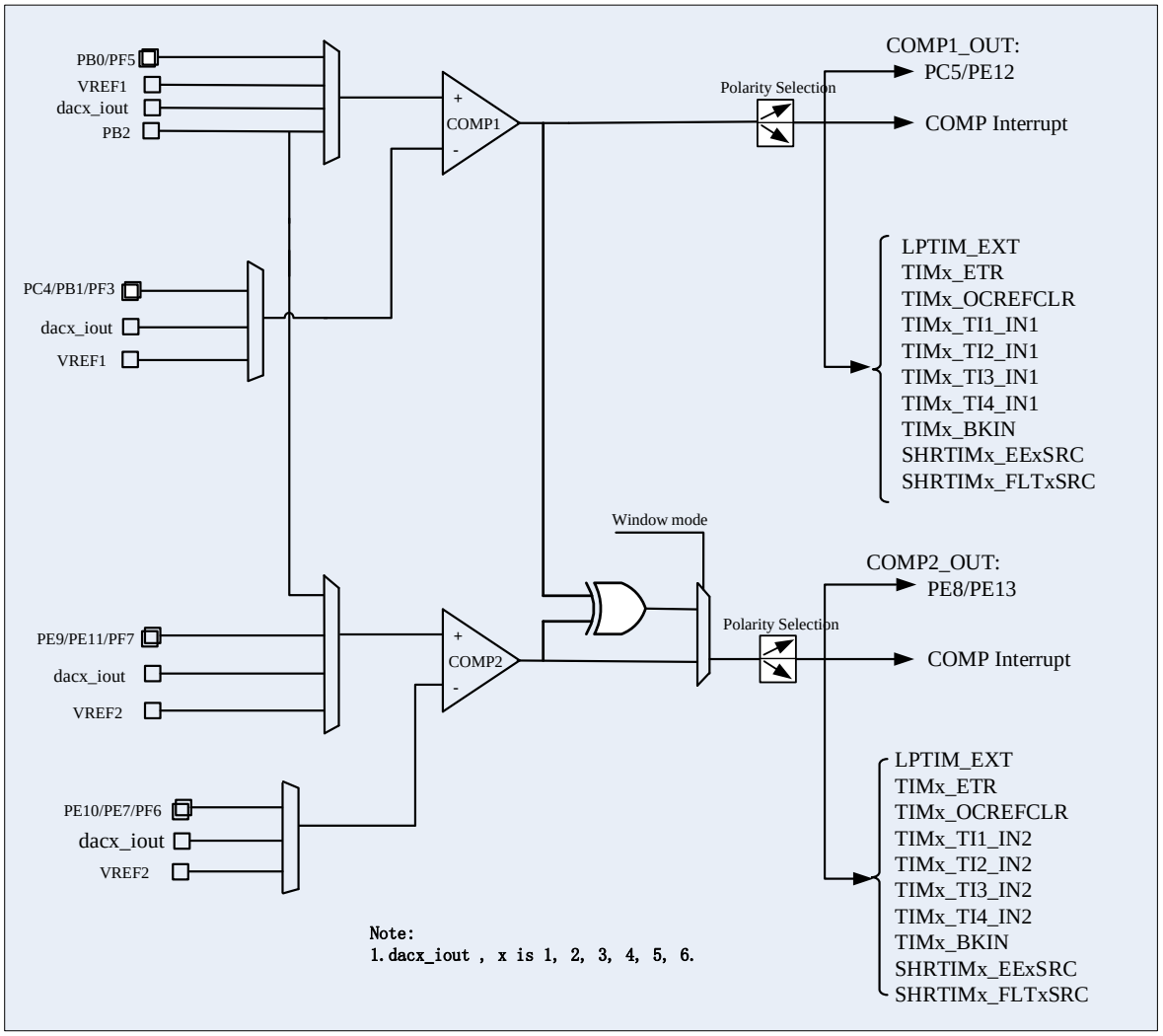

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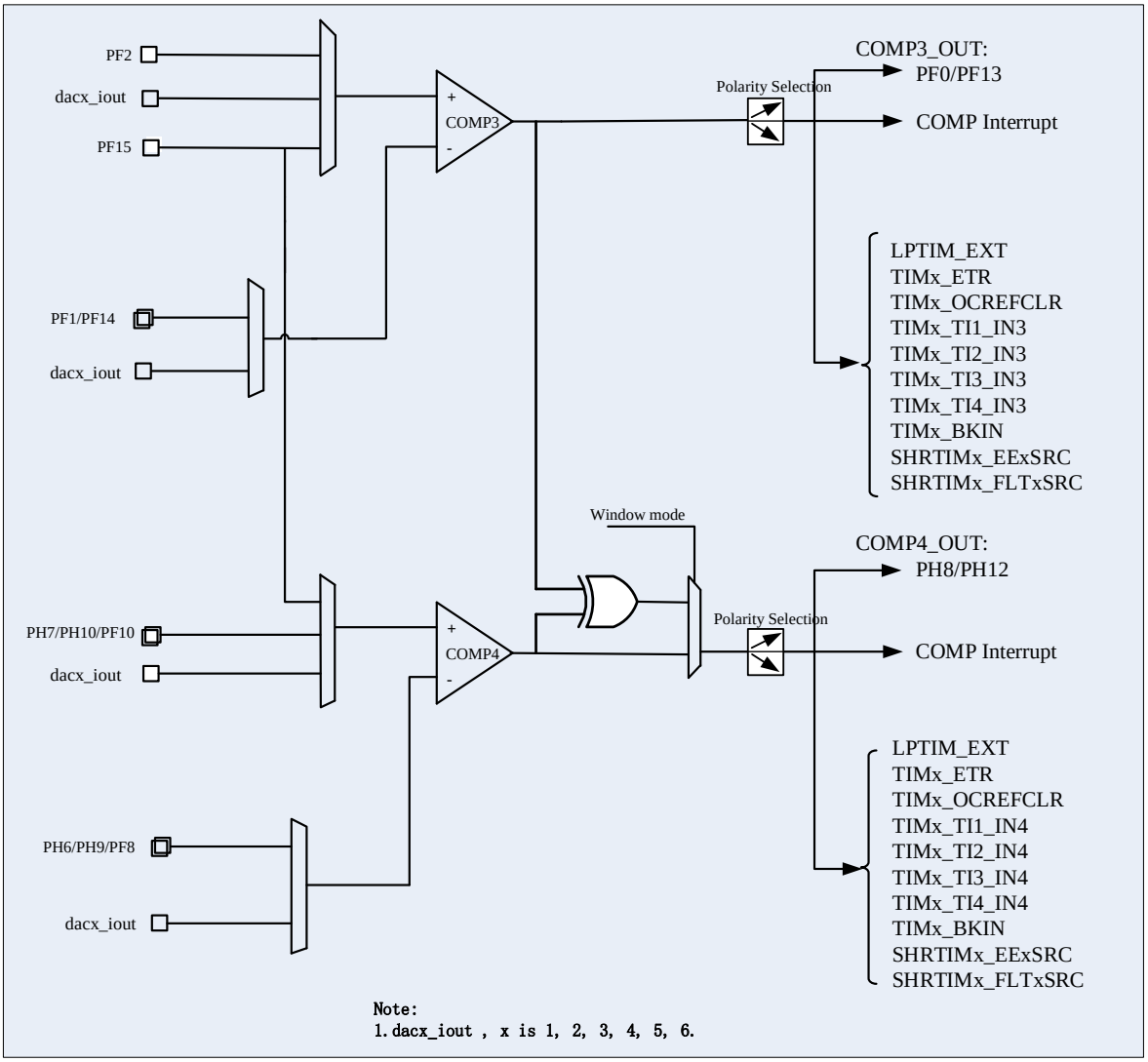
Figure 28-2 COMP3&COMP4 connection



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28.2 Main Feature

- Supports up to 4 independent comparators.
- Embedded three 64 level programmable comparison voltage reference sources VREF1, VREF2.
- Supports filter clock, filter reset.
- Output polarity can be configured high and low.
- Support 4 programmable hysteresis levels.
- The comparison result can be output to the I/O port or trigger timer, which is use to event capture, OCREF_CLR event, break event, and interrupt generation.
- The input channels can be selected from I/O ports, VREF1, VREF2, the general 12-bit DAC.
- It can be read-only or read-write, and can be unlocked only after a reset.
- Supports blanking, blanking source can be configurabled.
- COMP1/COMP2、COMP3/COMP4 can form window comparators.
- You can wake the system from Sleep mode by generating an interrupt.
- Filter window size can be configured.
- Filter threshold size can be configured.
- The sampling frequency for filtering can be configured.

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28.3 COMP Configuration Precedure

The complete configuration includes the following steps If the default configuration is used, skip the corresponding configuration items.

- Configurable hysteresis level COMPx_CTRL.HYST[2:0].
- Configure the output polarity COMPx_CTRL.POL.
- Configuration input selection, Comparator positive input COMPx_CTRL.INPSEL[3:0], negative input COMPx_CTRL.INMSEL[3:0].
- Enable output selection configuration COMPx_OTIMEN.
- Configure blanking source COMPx_CTRL.BLKINGEN and COMPx_CTRL.BLKING[3:0].
- Configure the filter sampling window COMPx_FILC.SAMPW[4:0].
- Configure the threshold COMPx_FILC.THRESH[4:0] (threshold should be greater than COMPx_FILC.SAMPW[4:0]/2).
- Configure the filter sampling frequency (for timer applications, sampling frequency should be greater than 5MHz).
- Enable COMPx_FILC.FILEN filter.
- Enable COMPx_CTRL.EN on the comparator.

Note: For the above steps, the filter should be enabled first and then the comparator should be enabled. The comparator should be enabled after the filtering (if enabled) is configured and enabled. In addition, when the comparator control register is locked, it can only be unlocked by reset.

28.4 COMP Operating Mode

28.4.1 Window Comparators

The comparators can be combined into 2 window comparators as follows:

- Comparator 1 and comparator 2 can be combined as window comparator and share PB2.
- Comparator 3 and comparator 4 can be combined as window comparator and share PF15.

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28.4.2 Independent Comparators

The seven comparators can be configured independently to complete the comparator function. The output of a comparator can be output to an I/O port. Each comparator has a different remapped port, Enable the comparator to output to the TIM port by configuring the corresponding bit of COMPx_OTIMEN.

The Comparator output, supports triggering events, such as configuring it as the break function of timer x or the OCREFCLEAR function of timer x.

Note: Refer to the comparator interconnection for specific configuration

28.5 Comparator Interconnection

For the interconnection of the output port of the comparator, please refer to the chapter on the multiplexing function of GPIO, which defines the value of the remapping of the comparator OUT.

The comparator OUT pin is as follows:

COMP1	COMP2	COMP3	COMP4
PC5	PE8	PF0	PH8
PE12	PE13	PF13	PH12

The comparator INP pin has the following configurations:

INPSEL	COMP1	COMP2	COMP3	COMP4
0000	PB0	PE9	PF2	PH10
0001	PB2	PE11	PF15	PH7
0010	DAC1_out	DAC1_out	DAC1_out	DAC1_out
0011	DAC2_out	DAC2_out	DAC2_out	DAC2_out
0100	DAC3_out	DAC3_out	DAC3_out	DAC3_out
0101	DAC4_out	DAC4_out	DAC4_out	DAC4_out
0110	DAC5_out	DAC5_out	DAC5_out	DAC5_out
0111	DAC6_out	DAC6_out	DAC6_out	DAC6_out
1000	VREF_VC1	VREF_VC2	-	PF15
1001	PF5	PB2	-	PF10
1010	-	PF7	-	-

The comparator INM pin has the following configurations:

INPSEL	COMP1	COMP2	COMP3	COMP4
0000	PB1	PE7	PF1	PH9
0001	PC4	PE10	PF14	PH6
0010	DAC1_out	DAC1_out	DAC1_out	DAC1_out
0011	DAC2_out	DAC2_out	DAC2_out	DAC2_out
0100	DAC3_out	DAC3_out	DAC3_out	DAC3_out
0101	DAC4_out	DAC4_out	DAC4_out	DAC4_out
0110	DAC5_out	DAC5_out	DAC5_out	DAC5_out

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INPSEL	COMP1	COMP2	COMP3	COMP4
0111	DAC6_out	DAC6_out	DAC6_out	DAC6_out
1000	VREF_VC1	VREF_VC2	-	PF8
1001	PF3	PF6	-	-

28.6 Interrupt

COMP supports interrupt response, COMP1 and COMP2 share one interrupt entry, COMP3 and COMP4 share one interrupt entry. There are two cases of interrupt generation as follows.

- The polarity of COMPx_CTRL.POL is not reversed, and the interrupt is enabled. When INPSEL > INMSEL, the comparator interrupt will be generated when COMPx_CTRL.OUT is set to 1 by hardware.
- The polarity of COMPx_CTRL.POL is reversed, and the interrupt is enabled. When INPSEL < INMSEL, the comparator interrupt is generated when COMPx_CTRL.OUT is set to 1 by hardware.

Note: COMP interrupt usage requires configuring the EXTI line first, refer to the NVIC section.

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28.7 Register

28.7.1 COMP1 Control Register (COMP1_CTRL)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			VV1TRM[5:0]						VV1EN	OUT	BLKING EN	BLKING[3:0]			
			rw						rw	r	rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HYST[1:0]		POL	Reserved				INPSEL[3:0]				INMSEL[3:0]				EN
rw		rw					rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28:23	VV1TRM[5:0]	Internal comparator 1 reference input voltage comparison VREF level selection 0~0b'111111 corresponds to an output voltage range of 0~VREF+, with a total of 64 levels. For example, 7 represents（7）* VREF+/63 = 1/9 * VREF+
22	VV1EN	Internal comparator 1 reference input voltage comparison enable, this bit is set and cleared by software: 0: Disable; 1: Enable.
21	OUT	The output state of the comparator output. 0: Output low level; 1: Output high level.
20	BLKINGEN	This bit is set and cleared by software to controls the enabling of COMP1 output blanking. 0: Disable 1: Enable
19:16	BLKING[3:0]	These bits select which timer output controls the comparator 1 output blanking. 0000: ATIM1 OC5 selected as blanking source; 0001: GTIMB1 OC5 selected as blanking source; 0010: GTIMB2 OC5 selected as blanking source; 0011: ATIM2 OC5 selected as blanking source; 0100: ATIM3 OC5 selected as blanking source; 0101: ATIM4 OC1 selected as blanking source; 0110: GTIMB3 OC5 selected as blanking source. 0111: GTIMA4 OC5 selected as blanking source. 1000: GTIMA2 OC3 selected as blanking source. 1001: GTIMA1 OC3 selected as blanking source.

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Bit field	Name	Description
		1010: GTIMA3 OC3 selected as blanking source. 1011: GTIMA5 OC3 selected as blanking source. 1100: GTIMA6 OC3 selected as blanking source. 1101: GTIMA7 OC3 selected as blanking source. Others: Reserved.
15:14	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis; 01: Low hysteresis; 10: Medium hysteresis; 11: High hysteresis;
13	POL	This bit is used to invert the comparator output. 0: Output is not inverted； 1: Output is inverted.
12:9	Reserved	Reserved, the reset value must be maintained.
8:5	INPSEL[3:0]	Comparator positive terminal selection bit: 0000: PB0 0001: PB2 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout 1000: VREF_VC1 1001: PF5 Other: Reserved
4:1	INMSEL[3:0]	Comparator negative terminal selection bit: 0000: PB1 0001: PC4 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout 1000: VREF_VC1 1001: PF3 Other: Reserved
0	EN	This bit switches COMP ON/OFF 0: Comparator disabled; 1: Comparator enable.

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28.7.2 COMP1 Filter Control Register（COMP1_FILC）

Offset address: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			VFPEN	VFNEN	SAMPW[4:0]					THRESH[4:0]					FILEN
			rw	rw	rw					rw					rw

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	VFNEN	VFLAG enable for COMP1 negative end; 0: Disable. The effsective flag bit for COMP1 negative end for DAC channel data (VFLAG) is not used, controlling the filter sampling; 1: Enable.The effsective flag bit for COMP1 negative end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP1_FILC.FILEN is set and 12-bit DAC channel is selected as COMP1 negative input.*
11	VFPEN	VFLAG enable for COMP1 positive end; 0: Disable. The effsective flag bit for COMP1 positive end for DAC channel data (VFLAG) is not used, controlling the filter sampling; 1: Enable.The effsective flag bit for COMP1 positive end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP1_FILC.FILEN is set and 12-bit DAC channel is selected as COMP1 positive input.*
10:6	SAMPW[4:0]	Low-pass filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The low-pass filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable. 0: Disable; 1: Enable.

28.7.3 COMP1 Filter Prescaler Register（COMP1_FILP）

Offset address: 0x18

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CLKPSC[15:0]	Low filter sample clock prescaler. Systerm clock divider = CLKPSC + 1。 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle … 65535: Every 65536 cycle

28.7.4 COMP2 Control Register (COMP2_CTRL)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			VV2TRM[5:0]						VV2EN	OUT	BLKING EN	BLKING[3:0]			
			rw						rw	r	rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HYST[1:0]		POL	Reserved				INPSEL[3:0]				INMSEL[3:0]				EN
rw		rw					rw				rw				rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28:23	VV2TRM[5:0]	Internal comparator 2 reference input voltage comparison VREF level selection 0~0b'111111 corresponds to an output voltage range of 0~VREF+, with a total of 64 levels. For example, 7 represents（7）* VREF+/63 = 1/9 * VREF+
22	VV2EN	Internal comparator 2 reference input voltage comparison enable: 0: Disable; 1: Enable.
21	OUT	The output state of the comparator output.

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Bit field	Name	Description
		0: Output low level; 1: Output high level.
20	BLKINGEN	This bit is set and cleared by software to controls the enabling of COMP2 output blanking. 0: Disable 1: Enable
19:16	BLKING[3:0]	These bits select which timer output controls the comparator 2 output blanking. 0000: ATIM1 OC5 selected as blanking source; 0001: GTIMB1 OC5 selected as blanking source; 0010: GTIMB2 OC5 selected as blanking source; 0011: ATIM2 OC5 selected as blanking source; 0100: ATIM3 OC5 selected as blanking source; 0101: ATIM4 OC1 selected as blanking source; 0110: GTIMB3 OC5 selected as blanking source. 0111: GTIMA4 OC5 selected as blanking source. 1000: GTIMA2 OC3 selected as blanking source. 1001: GTIMA1 OC3 selected as blanking source. 1010: GTIMA3 OC3 selected as blanking source. 1011: GTIMA5 OC3 selected as blanking source. 1100: GTIMA6 OC3 selected as blanking source. 1101: GTIMA7 OC3 selected as blanking source. Others: Reserved.
15:14	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis; 01: Low hysteresis; 10: Medium hysteresis; 11: High hysteresis;
13	POL	This bit is used to invert the comparator output. 0: Output is not inverted； 1: Output is inverted.
12:9	Reserved	Reserved, the reset value must be maintained.
8:5	INPSEL[3:0]	Comparator positive terminal selection bit: 0000: PE9 0001: PE11 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout 1000: VREF_VC2 1001: PB2(Forming window mode with COMP1) 1010: PF7

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Bit field	Name	Description
		Other: Reserved
4:1	INMSEL[3:0]	Comparator negative terminal selection bit: 0000: PE7 0001: PE10 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout 1000: VREF_VC2 1001: PF6 Other: Reserved
0	EN	This bit switches COMP ON/OFF 0: Comparator disabled; 1: Comparator enable.

28.7.5 COMP2 Filter Control Register（COMP2_FILC）

Offset address: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			VFPEN	VFNEN	SAMPW[4:0]					THRESH[4:0]					FILEN
			rw	rw	rw					rw					rw

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	VFNEN	VFLAG enable for COMP2 negative end; 0: Disable. The effsective flag bit for COMP2 negative end for DAC channel data (VFLAG) is not used, controlling the filter sampling; 1: Enable.The effsective flag bit for COMP2 negative end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP2_FILC.FILEN is set and 12-bit DAC channel is selected as COMP2 negative input.*
11	VFPEN	VFLAG enable for COMP2 positive end; 0: Disable. The effsective flag bit for COMP2 positive end for DAC channel data

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Bit Field	Name	Description
		(VFLAG) is not used, controlling the filter sampling; 1: Enable.The effsective flag bit for COMP2 positive end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP2_FILC.FILEN is set and 12-bit DAC channel is selected as COMP2 positive input.*
10:6	SAMPW[4:0]	Low-pass filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The low-pass filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable. 0: Disable; 1: Enable.

28.7.6 COMP2 Filter Prescaler Register（COMP2_FILP）

Offset address: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CLKPSC[15:0]	Low filter sample clock prescaler. Systerm clock divider = CLKPSC + 1。 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle … 65535: Every 65536 cycle

28.7.7 COMP3 Control Register (COMP3_CTRL)

Address offset: 0x30

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										OUT	BLKING EN	BLKING[3:0]			
										r	rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HYST[1:0]		POL	Reserved				INPSEL[3:0]				INMSEL[3:0]				EN
rw		rw					rw				rw				rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	OUT	The output state of the comparator output. 0: Output low level; 1: Output high level.
20	BLKINGEN	This bit is set and cleared by software to controls the enabling of COMP3 output blanking. 0: Disable 1: Enable
19:16	BLKING[3:0]	These bits select which timer output controls the comparator 3 output blanking. 0000: ATIM1 OC5 selected as blanking source; 0001: GTIMB1 OC5 selected as blanking source; 0010: GTIMB2 OC5 selected as blanking source; 0011: ATIM2 OC5 selected as blanking source; 0100: ATIM3 OC5 selected as blanking source; 0101: ATIM4 OC1 selected as blanking source; 0110: GTIMB3 OC5 selected as blanking source. 0111: GTIMA4 OC5 selected as blanking source. 1000: GTIMA2 OC3 selected as blanking source. 1001: GTIMA1 OC3 selected as blanking source. 1010: GTIMA3 OC3 selected as blanking source. 1011: GTIMA5 OC3 selected as blanking source. 1100: GTIMA6 OC3 selected as blanking source. 1101: GTIMA7 OC3 selected as blanking source. Others: Reserved.
15:14	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis; 01: Low hysteresis; 10: Medium hysteresis; 11: High hysteresis;
13	POL	This bit is used to invert the comparator output. 0: Output is not inverted； 1: Output is inverted.
12:9	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
8:5	INPSEL[3:0]	Comparator positive terminal selection bit: 0000: PF2 0001: PF15 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout Other: Reserved
4:1	INMSEL[3:0]	Comparator negative terminal selection bit: 0000: PF1 0001: PF14 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout Other: Reserved
0	EN	This bit switches COMP ON/OFF 0: Comparator disabled; 1: Comparator enable.

28.7.8 COMP3 Filter Control Register（COMP3_FILC）

Offset address: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			VFPEN	VFNEN	SAMPW[4:0]					THRESH[4:0]					FILEN
			rw	rw	rw					rw					rw

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	VFNEN	VFLAG enable for COMP3 negative end; 0: Disable. The effsective flag bit for COMP3 negative end for DAC channel data

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Bit Field	Name	Description
		(VFLAG) is not used, controlling the filter sampling; 1: Enable. The effsective flag bit for COMP3 negative end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP3_FILC.FILEN is set and 12-bit DAC channel is selected as COMP3 negative input.*
11	VFPEN	VFLAG enable for COMP3 positive end; 0: Disable. The effsective flag bit for COMP3 positive end for DAC channel data (VFLAG) is not used, controlling the filter sampling; 1: Enable. The effsective flag bit for COMP3 positive end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP3_FILC.FILEN is set and 12-bit DAC channel is selected as COMP3 positive input.*
10:6	SAMPW[4:0]	Low-pass filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The low-pass filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable. 0: Disable; 1: Enable.

28.7.9 COMP3 Filter Prescaler Register（COMP3_FILP）

Offset address: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CLKPSC[15:0]	Low filter sample clock prescaler. Systerm clock divider = CLKPSC + 1。 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle …

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Bit Field	Name	Description
		65535: Every 65536 cycle

28.7.10 COMP4 Control Register (COMP4_CTRL)

Address offset: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										OUT	BLKING EN	BLKING[3:0]			
										r	rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HYST[1:0]		POL	Reserved				INPSEL[3:0]				INMSEL[3:0]				EN
rw		rw					rw				rw				rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	OUT	The output state of the comparator output. 0: Output low level; 1: Output high level.
20	BLKINGEN	This bit is set and cleared by software to controls the enabling of COMP4 output blanking. 0: Disable 1: Enable
19:16	BLKING[3:0]	These bits select which timer output controls the comparator 4 output blanking. 0000: ATIM1 OC5 selected as blanking source; 0001: GTIMB1 OC5 selected as blanking source; 0010: GTIMB2 OC5 selected as blanking source; 0011: ATIM2 OC5 selected as blanking source; 0100: ATIM3 OC5 selected as blanking source; 0101: ATIM4 OC1 selected as blanking source; 0110: GTIMB3 OC5 selected as blanking source. 0111: GTIMA4 OC5 selected as blanking source. 1000: GTIMA2 OC3 selected as blanking source. 1001: GTIMA1 OC3 selected as blanking source. 1010: GTIMA3 OC3 selected as blanking source. 1011: GTIMA5 OC3 selected as blanking source. 1100: GTIMA6 OC3 selected as blanking source. 1101: GTIMA7 OC3 selected as blanking source. Others: Reserved.
15:14	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis;

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Bit field	Name	Description
		01: Low hysteresis; 10: Medium hysteresis; 11: High hysteresis;
13	POL	This bit is used to invert the comparator output. 0: Output is not inverted； 1: Output is inverted.
12:9	Reserved	Reserved, the reset value must be maintained.
8:5	INPSEL[3:0]	Comparator positive terminal selection bit: 0000: PH10 0001: PH7 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout 1000: PF15(Forming window mode with COMP3) 1001: PF10 Other: Reserved
4:1	INMSEL[3:0]	Comparator negative terminal selection bit: 0000: PH9 0001: PH6 0010: dac1_iout 0011: dac2_iout 0100: dac3_iout 0101: dac4_iout 0110: dac5_iout 0111: dac6_iout 1000: PF8 Other: Reserved
0	EN	This bit switches COMP ON/OFF 0: Comparator disabled; 1: Comparator enable.

28.7.11 COMP4 Filter Control Register（COMP4_FILC）

Offset address: 0x44

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			VFPEN	VFNEN	SAMPW[4:0]					THRESH[4:0]					FILEN
			rw	rw	rw					rw					rw

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12	VFNEN	VFLAG enable for COMP4 negative end; 0: Disable. The effsective flag bit for COMP4 negative end for DAC channel data (VFLAG) is not used, controlling the filter sampling; 1: Enable. The effsective flag bit for COMP4 negative end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP4_FILC.FILEN is set and 12-bit DAC channel is selected as COMP4 negative input.*
11	VFPEN	VFLAG enable for COMP4 positive end; 0: Disable. The effsective flag bit for COMP4 positive end for DAC channel data (VFLAG) is not used, controlling the filter sampling; 1: Enable. The effsective flag bit for COMP4 positive end for DAC channel data (VFLAG) is used, controlling the filter sampling. *Note: this bit is effective when the COMP4_FILC.FILEN is set and 12-bit DAC channel is selected as COMP4 positive input.*
10:6	SAMPW[4:0]	Low-pass filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The low-pass filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable. 0: Disable; 1: Enable.

28.7.12 COMP4 Filter Prescaler Register（COMP4_FILP）

Offset address: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKPSC[15:0]															
rw															

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Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CLKPSC[15:0]	Low filter sample clock prescaler. Systerm clock divider = CLKPSC + 1。 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle … 65535: Every 65536 cycle

28.7.13 COMP Low Power Mode Register（COMP_LPMODE）

Offset address: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															LPEN
															rw

Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	LPEN	This bit is set and cleared by software to enable low power mode. 0: Normal run mode. (The digital filter clock is from system clock.) 1: Low power mode(the digital filter clock is from LSE or LSI)

28.7.14 COMP Window Mode Register（COMP_WINMODE）

Offset address: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														CMP34 MD	CMP12 MD

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rw rw

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	CMP34MD	This bit selects window mode: the two non-inverting inputs of the comparator share the PF15 input. 0: Comparators 3 and 4 are not in window mode, the port output the result of COMP4; 1: Comparators 3 and 4 are in window mode, the port output the XOR result of COMP3 and COMP4.
0	CMP12MD	This bit selects window mode: the two non-inverting inputs of the comparator share the PB2 input. 0: Comparators 1 and 2 are not in window mode, the port output the result of COMP2; 1: Comparators 1 and 2 are in window mode, the port output the XOR result of COMP1 and COMP2。

28.7.15 COMP Lock Register（COMP_LOCK）

Offset address: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4LK	CMP3LK	CMP2LK	CMP1LK
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	CMP4LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP4_CTRL, COMP4_FILC, COMP4_FILP registers to be read-only. 0: COMP4_CTRL, COMP4_FILC, COMP4_FILP is read-write. 1: COMP4_CTRL, COMP4_FILC, COMP4_FILP is read-only.
2	CMP3LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP3_CTRL, COMP3_FILC, COMP3_FILP registers to be read-only. 0: COMP3_CTRL, COMP3_FILC, COMP3_FILP is read-write.

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Bit Field	Name	Description
		1: COMP3_CTRL, COMP3_FILC, COMP3_FILP is read-only.
1	CMP2LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP2_CTRL, COMP2_FILC, COMP2_FILP registers to be read-only. 0: COMP2_CTRL, COMP2_FILC, COMP2_FILP is read-write. 1: COMP2_CTRL, COMP2_FILC, COMP2_FILP is read-only.
0	CMP1LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP1_CTRL, COMP1_FILC, COMP1_FILP registers to be read-only. 0: COMP1_CTRL, COMP1_FILC, COMP1_FILP is read-write. 1: COMP1_CTRL, COMP1_FILC, COMP1_FILP is read-only.

28.7.16 COMP Interrupt Enable Register（COMP_INTEN）

Offset address: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4IEN	CMP3IEN	CMP2IEN	CMP1IEN
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	CMP4IEN	This bit controlled Interrupt enable of COMP4 0: Disable; 1: Enable.
2	CMP3IEN	This bit controlled Interrupt enable of COMP3 0: Disable; 1: Enable.
1	CMP2IEN	This bit controlled Interrupt enable of COMP2 0: Disable; 1: Enable.
0	CMP1IEN	This bit controlled Interrupt enable of COMP1 0: Disable; 1: Enable.

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28.7.17 COMP Interrupt Status Register（COMP_INTSTS）

Offset address: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4IS	CMP3IS	CMP2IS	CMP1IS
												rc_w0	rc_w0	rc_w0	rc_w0

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3	CMP4IS	This bit indicate the interrupt status of COMP4,write 0 to clear.
2	CMP3IS	This bit indicate the interrupt status of COMP3,write 0 to clear.
1	CMP2IS	This bit indicate the interrupt status of COMP2,write 0 to clear.
0	CMP1IS	This bit indicate the interrupt status of COMP1,write 0 to clear.

28.7.18 COMP Output to Timer Enable Register（COMP_OTIMEN）

Offset address: 0x68

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CMP4 OEN	CMP3 OEN	CMP2 OEN	CMP1 OEN
												rw	rw	rw	rw

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	CMP4OEN	This bit controls the enabling of COMP4 output to the timer function 0: Disable 1: Enable
2	CMP3OEN	This bit controls the enabling of COMP3 output to the timer function 0: Disable

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Bit Field	Name	Description
		1: Enable
1	CMP2OEN	This bit controls the enabling of COMP2 output to the timer function 0: Disable 1: Enable
0	CMP1OEN	This bit controls the enabling of COMP1 output to the timer function 0: Disable 1: Enable

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29 Voltage reference buffer (VREFBUF)

29.1 Introduction

The chip features an internal voltage reference buffer that can be used as the voltage reference for the ADC, 12-bit DAC, and internal 6-bit DAC of the COMP. It can also be used as an external component's voltage reference through the VREF+ pin. When the VREF+ pin is connected to the VDDA pin within the package (refer to the package pin description in the datasheet for details), the voltage reference buffer is not available, must remain disabled, and the VREFBUF_CTRL1.EN and VREFBUF_CTRL1.HIM bits must be set to 00.

29.2 Functional Description

29.2.1 VREFBUF level selection

The built-in voltage reference buffer supports four voltage levels: 2.5V, 2.048V, 1.8V and 1.5V. The voltage level can be selected by configuring the VREFBUF_CTRL2.VLSEL[1:0] register bits.

Table 29-1 Voltage Reference Buffer Level Selection

VLSEL[1:0]	Voltage Reference Buffer Level Selection
00	2.5V
01	2.048V
10	1.8V
11	1.5V

29.2.2 VREFBUF mode selection

The internal voltage reference can be set in four different modes based on the configuration of the EN and HIM bits. These modes are listed in the table below:

Table 29-2 Voltage Reference Buffer mode

VREFBUF_ CTRL1.EN	VREFBUF_ CTRL1.HIM	Voltage Reference Buffer configuration
0	0	VREFBUF output disabled, V_{REF+} pin pulled down to VSSA
0	1	VREFBUF output in high-impedance state, V_{REF+} pin in external input mode
1	0	VREFBUF output enabled, V_{REF+} pin connected to VREFBUF output
1	1	VREFBUF output in high-impedance state, V_{REF+} pin voltage maintained by an external capacitor

Users can enable the operation of VREFBUF by first setting the VREFBUF_CTRL1.HIM bit to 0 and then setting the VREFBUF_CTRL1.EN bit to 1. At this point, users must wait for the VREFBUF_STS.RDY bit to be set,

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indicating that the voltage reference output has reached 90% of the expected value[(1)].

Notes:

1. When VREFBUF is operational, VREF- is connected to VSSA by default;

2. The input voltage of VREF+ must not exceed VDDA;

3. After enabling VREFBUF, the VREF+ pin should not be externally connected to a voltage;

4. When using the VREFBUF output, configure VREFBUF_CTRL1.HIM = 0 first;

5. The 100nF filtering capacitor is crucial and should be placed as close as possible to the VREF+ pin in PCB design.

6. [(1)]Additional 250+ uS delay added to VREFBUF_STS.RDY rise edge to align at 100% settled VREFBUF output

29.2.3 VREFBUF trim

The output voltage of VREFBUF is calibrated by the chip during manufacturing. When restarting VREFBUF or each time the voltage level of VREFBUF is changed (VREFBUF_CTRL2.VLSEL[1:0]), the calibration data is automatically loaded the trimming registers. The VREFBUF_CTRL2.VLSEL[1:0] also selects the individual trim bit registers as follows: VREFBUF_TRIM1.TRIM0[5:0], VREFBUF_TRIM1.TRIM1[5:0], VREFBUF_TRIM2.TRIM2[5:0], VREFBUF_TRIM2.TRIM3[5:0] for the VREFBUF_CTRL2.VLSEL[1:0] values 00, 01, 10, and 11 respectively. Users can fine-tune the output voltage by directly changing the bits of the trimming registers. The fine-tuning the output voltage does not affect the ready signal VREFBUF_STS.RDY.

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29.3 Registers

29.3.1 VREFBUF Trim Register 1 (VREFBUF_TRIM1)

Address offset: 0x28

Reset value: 0x0820 00A8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				TRIM1[5:0]						TRIM0[5:0]					
				rw						rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:22	TRIM1[5:0]	VREFBUF Calibration VLSEL[1:0] = 01 (VREFBUF output 2.048V): Adjustment step size is 1mV
21:16	TRIM0[5:0]	VREFBUF Calibration VLSEL[1:0] = 00 (VREFBUF output 2.5V): Adjustment step size is 1.25mV
15:0	Reserved	Reserved, the reset value must be maintained.

29.3.2 VREFBUF Status Register (VREFBUF_STS)

Address offset: 0x34

Reset value: 0x0000 0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		RDY	Reserved												
		r													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	RDY	VREFBUF Ready Flag 0: VREFBUF output not completed

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Bit field	Name	Description
		1: VREFBUF output ready
28:0	Reserved	Reserved, the reset value must be maintained.

29.3.3 VREFBUF Control Register 1 (VREFBUF_CTRL1)

Address offset: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						HIM	Reserved	EN	Reserved						
						rw		rw							

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	HIM	High-Impedance Mode Enable 0: REF+ pin internally pulled down to VSSA 1: REF+ pin in high-impedance state.
8	Reserved	Reserved, the reset value must be maintained.
7	EN	VREFBUF Enable 0: Disable 1: Enable
6:0	Reserved	Reserved, the reset value must be maintained.

29.3.4 VREFBUF Control Register 2 (VREFBUF_CTRL2)

Address offset: 0xDC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														VLSEL[1:0]	
														rw	

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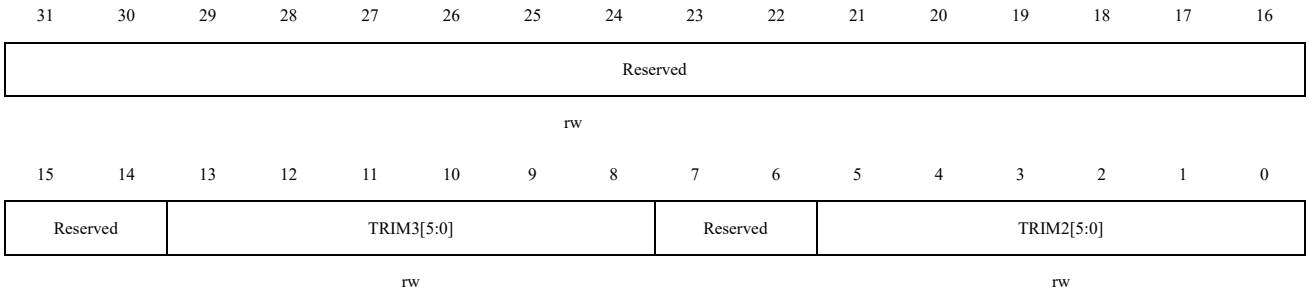
Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1:0	VLSEL[1:0]	VREFBUF Range Selection 00: VREFBUF output 2.5V 01: VREFBUF output 2.048V 10: VREFBUF output 1.8 V 11: VREFBUF output 1.5V

29.3.5 VREFBUF Trim Register 2 (VREFBUF_TRIM2)

Address offset: 0xE8

Reset value: 0x0010 2020



Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:8	TRIM3[5:0]	VREFBUF Calibration VLSEL[1:0] = 11 (VREFBUF output 1.5V): Adjustment step size is 0.75mV
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	TRIM2[5:0]	VREFBUF Calibration VLSEL[1:0] = 10 (VREFBUF output 1.8V): Adjustment step size is 0.9mV

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30 Filter Math Accelerator（FMAC）

30.1 FMAC Introduction

The mathematical acceleration unit of the filter performs arithmetic operations on vectors, including a multiplier, an accumulator, and address generation logic that allows indexing of vector elements in local memory. This unit supports input and output circular buffers to facilitate the implementation of digital filters such as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters.

This unit allows the processor to be freed from frequent or lengthy filtering operations, thereby enabling the processor to perform other tasks. In many cases, it can accelerate such calculations compared to software implementations, speeding up the processing of critical time tasks.

30.2 FMAC Main Features

- 16 x 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction capabilities
- 16-bit fixed-point input and output data
- 256 x 16-bit data buffer
- Up to three data buffers can be defined in memory (two inputs, one output), defined by programmable base address pointers and related size registers
- Input and output buffers can be recycled
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, correlation
- Supports DMA for reading and writing data

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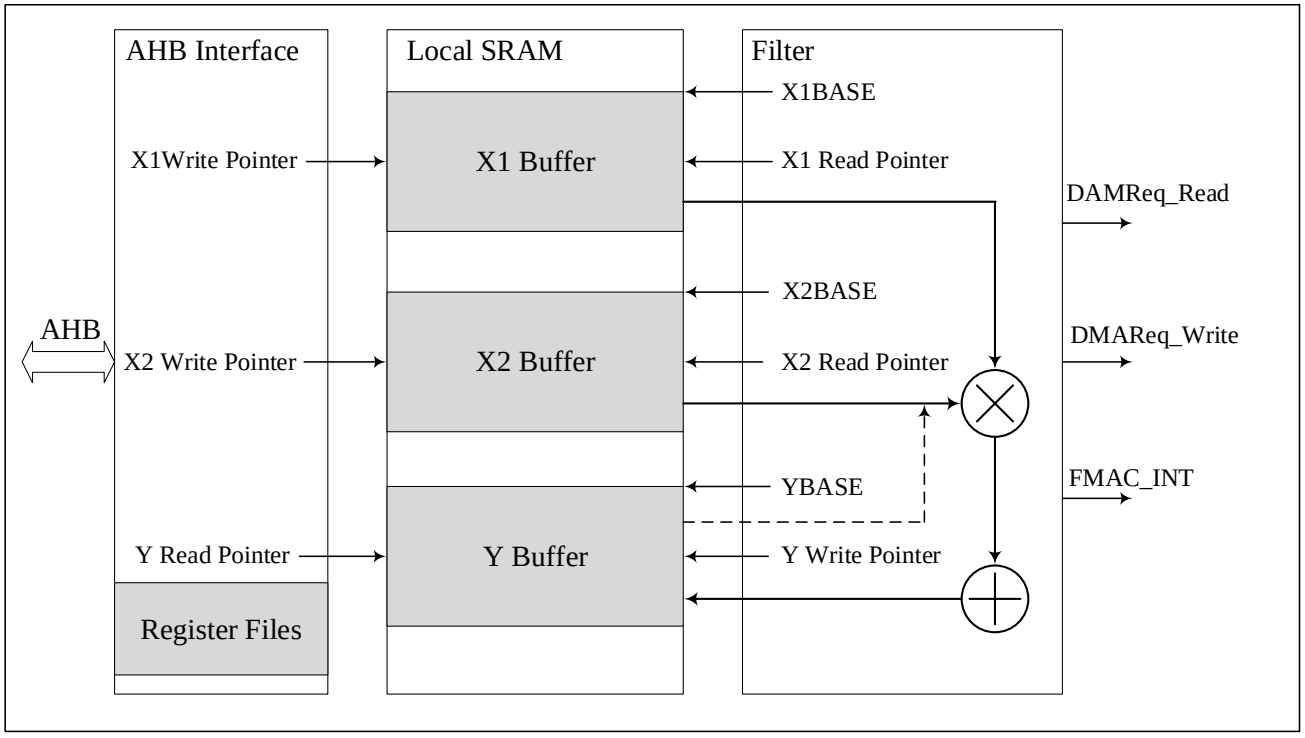
30.3 FMAC Function Description

30.3.1 General Description

Figure 30-1 FMAC Block Diagram



This unit consists of a fixed-point multiplier, accumulator, and buffer.

The two vector input data of the multiplier are loaded from the buffer by the core or DMA, and then multiplied by the multiplier using dot product computation.

The accumulator accumulates the output result of the multiplier, and after the calculation is completed, the output result in the accumulator is stored in the buffer for the core or DMA to read.

The module buffer can be divided into input data buffer (X1), coefficient buffer (X2), and output data buffer (Y). The coefficient buffer stores the feedforward and feedback filter coefficients of FIR and IIR filters, the input data buffer stores the input vector data, and the output data buffer stores the results calculated by FIR and IIR filters, as well as the pre-stored filter output data of the IIR filter.

The output result of the Finite Impulse Response (FIR) filter is the dot product of the input vector data and the feedforward filter coefficients. The input vector data is continuously updated, meaning the earliest sampled data is discarded, and a new sample data is added to form the new vector data.

The output result of the Infinite Impulse Response (IIR) filter is the product between the feedback filter coefficients and the previous filter output data, added to the convolution of FIR.

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30.3.2 Buffer

This unit contains a 256 x 16-bit read/write storage area: input values are stored in buffer X1 and buffer X2, while output values are stored in buffer Y. The addresses and sizes of the buffers are specifically described as follows:

- X1BASE: Base address of buffer X1.
- X2BASE: Base address of buffer X2.
- YBASE: Base address of buffer Y.

The length of the buffers is as follows:

- X1BUFSIZE: Number of 16-bit words allocated for buffer X1.
- X2BUFSIZE: Number of 16-bit words allocated for buffer X2.
- YBUFSIZE: Number of 16-bit words allocated for buffer Y.

The above parameters need to be configured into the corresponding FMAC_X1BUFCFG, FMAC_X2BUFCFG, FMAC_YBUFCFG registers before starting the FMAC module. The base addresses of the three buffers can be freely configured within the range of 0x00-0xFF, and the total length of the three buffers must be less than 256. There are no restrictions on the position and size of the buffers, which may lead to overlapping of the three buffer locations. To avoid abnormal operation, it is not recommended to overlap the buffers when configuring the base addresses and lengths of the buffers.

Prior to initiating the conversion in the FMAC module, corresponding data can be preloaded into the buffers. Buffer X1 preloads the input vector data, buffer X2 preloads the filter coefficients, and buffer Y preloads the previous filter output data (only required for IIR filters). Data loading into the target buffer indicated by the write pointer is accomplished by writing data to the FMAC_WDAT register. After completing a write operation, the write pointer is incremented. If the pointer reaches the end of the allocated buffer space, the write pointer returns to the base address.

If buffer recycling is required, an optional reserved area d can be added to the buffer. Additionally, to adjust the operation of the CPU or DMA, it is necessary to set the watermark threshold size. To meet the performance requirements of the application, the values of d and the watermark need to be configured reasonably. Typically, for higher data throughput, the input buffer should not be empty, so d should be slightly larger than the watermark to accommodate any interrupts or DMA delays. On the other hand, if the speed of incoming data is slower than the processing speed, the input buffer can be empty and wait for the next data to be written. In this case, d and the watermark can be set equal to ensure that the input buffer does not overflow.

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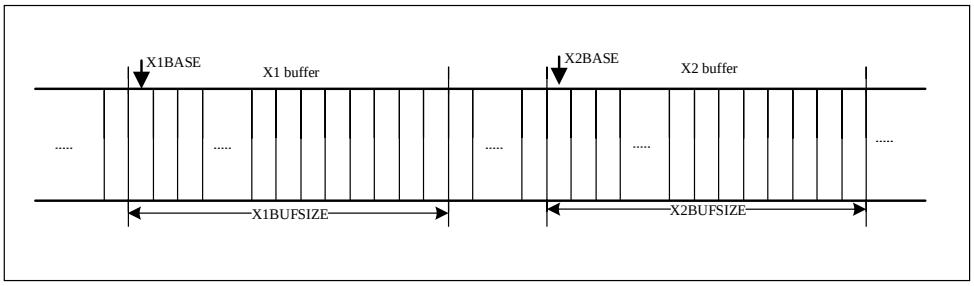
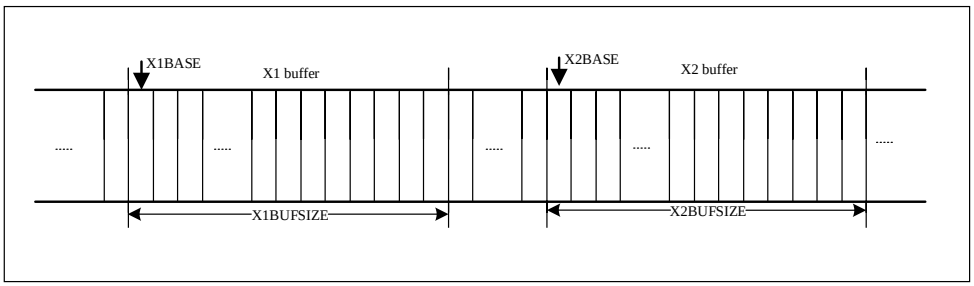
30.3.3 Input Buffer

Figure 30-1 Input Buffer Schematic



As shown in Figure 30-1, the X1 buffer and X2 buffer are used to store the data input to the multiplier in the FMAC module. For each multiplication operation, the multiplier extracts one data from the X1 buffer and one from the X2 buffer, and multiplies them. After each multiplication operation, the control unit generates a read pointer address offset based on the current function, which is relative to the buffer base address. The read pointer address offset is controlled by hardware and automatically performed.

Figure 30-2 Schematic of Circular Input Buffer



The X1 buffer can operate in circular mode, as shown in Figure 30-2. In the presence of available space, new data is continuously transferred to the input buffer. For digital filters, preloading the buffer is optional. When the filtering operation begins, if the input sample values have not been written to the X1 buffer, the buffer is marked as 'empty'. The FMAC module generates requests to load new sample data to the DMA or CPU, which continue until there is sufficient sample data for filtering calculations (FIR/IIR).

The X2 buffer only operates in non-circular mode and is used to store filter coefficients, which typically need to be preloaded.

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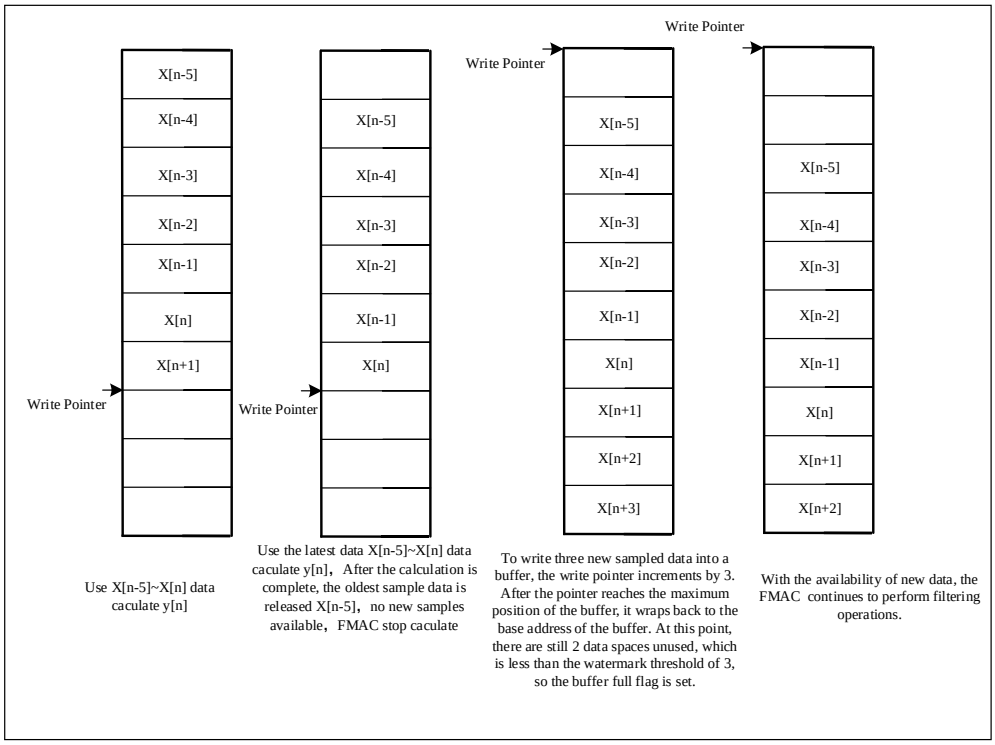
Figure 30-3 Schematic of Circular Input Buffer Operation



When the buffer operates in circular mode, its space (X1BUFSIZE) should be larger than the number of elements used by the current calculation function to ensure that there are new values available in the buffer for computation. The schematic of the circular input buffer operation during filtering is shown in . When computing the output y[n], the FMAC calls N+1 input samples from x[n-N] to x[n]. After computing y[n], it calls the input sample sequence from x[n-N+1] to x[n+1] to begin computing y[n+1]. The earliest input sample (x[n-N]) is discarded, and a new sample value (x[n+1]) is added.

When computing y[n+1], the CPU or DMA must ensure that the new sample data x[n+1] is available in the buffer space. If x[n+1] is not available, the hardware in the FMAC module automatically marks the buffer as 'empty', blocking the calculation of the current y[n+1] until the buffer is written with the new sample value. The X1 buffer will not generate an underflow signal. If the input data is sampled by a timer or other external device where the sampling data input rate is typically slower than the filtering processing speed, the buffer usually operates in an 'empty' state (no data involved in the computation).

The X1BUFWM[1:0] bits in FMAC_X1BUFCFG register configure the watermark threshold value. If the available free space in the buffer (free space refers to the space that does not contain data or has been used) is less than the watermark threshold, the buffer is considered 'full'. When an FMAC interrupt or DMA write enable is active, if the FMAC_STS.X1BUFFF bit is not set, an interrupt or DMA write data request is generated. Without considering the risk of overflow, when an interrupt or DMA write data request occurs, several data can be transferred to the buffer. However, in case of overflow, the FMAC_STS.OVF flag is set, the written data is ignored, and the write pointer does not increment. Figure 30-3 illustrates the changes in the X1 buffer during the operation of an FIR filter with a length of 8, with the watermark set to 4.

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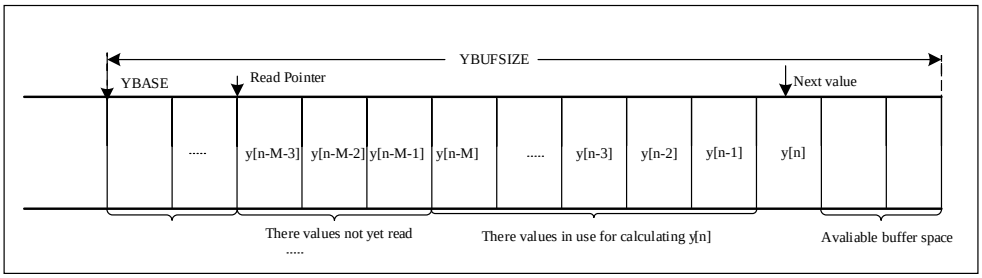
30.3.4 Output Buffer

The Y buffer is the output buffer used to store the accumulated results. The processor or DMA controller can read the output values, after which the buffer space will be released. Each time data is read from the register, data is obtained from the address indicated by the read pointer. The read pointer is then incremented, and when the pointer reaches the end of the allocated Y buffer space, it returns to the base address.

Figure 30-4 Loopback Buffer Diagram



The Y buffer can also function as a circular buffer. If the address of the next output value is the same as the address indicated by the read pointer (unread data), the buffer is marked as full, filtering is stopped until the output value is read.

In an IIR filter, M previous output sample values (y[n-M] to y[n-1]) are used to calculate the next output sample y[n]. When a new output sample value is generated, the earliest output sample value y[n-M] is discarded.

If the number of unread data in the buffer is less than the watermark threshold programmed in FMAC_YBUFCFG.YBUFWM[1:0] bit field, the buffer will be marked as empty. If the empty flag is not set to 1 (indicating that the output buffer is not empty, i.e., the number of unread data is greater than the watermark threshold), an interrupt or DMA request (if enabled) will be generated to read data from the buffer. The presence of the watermark allows for the transfer of multiple data under a single interrupt without the risk of data shortage. In case of data underflow, the FMAC_STS.UNF flag will be set to 1. In this scenario, the read pointer will not increment, and the read operation will return the content at the address pointed to by the read pointer.

Figure 30-4 llustrates the dynamic process of the Y buffer during filter operation. The filter is a 7-tap IIR filter with a watermark set to 4.

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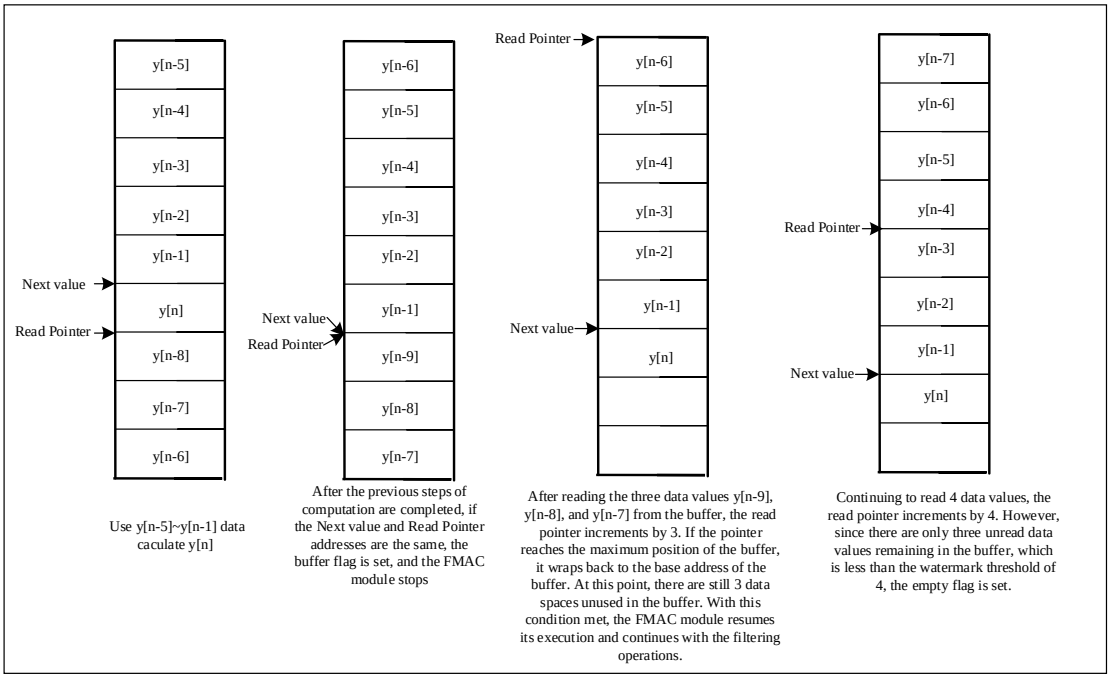
Figure 30-5 Circular Output Buffer Operation Diagram



30.3.5 Initialization Function

By writing the corresponding value in the FUNC field of the FMAC_PARAMCFG register and setting the START bit, the calculation of the corresponding function can be initiated. The P and Q bit fields must also contain the respective parameter values for each function, without using the R field. Once the function is completed, the START bit will be automatically reset.

During initialization, it is advisable to disable DMA requests and interrupts. Data transfer to the FMAC memory can be accomplished through software or DMA controller transfers.

Loading the X1 buffer

This function starts from the address in X1BASE and preloads N values for the X1 buffer. Continuous writes to the FMAC_WDAT register load the written data into the X1 buffer and increment the write pointer. Upon completion of the function, the write pointer points to the address X1BASE + N.

- Parameter P represents the number of data values loaded into the X1 buffer.
- Parameter Q and R are not used.

The X1 buffer loading operation is completed after N writes to the FMAC_WDAT register.

Loading the X2 buffer

This function starts from the address in X2BASE and preloads N + 1 + M values for the X2 buffer. Starting from the address in X2BASE, continuous writes to the FMAC_WDAT register load the written data into the X2 buffer and increment the write pointer.

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In an IIR filter, N+1 feedforward coefficients and M feedback coefficients are concatenated and loaded into the X2 buffer. The total number of coefficients is equal to N + 1 + M. For FIR filters, there are no feedback coefficients, so M = 0.

- Parameter P contains the number of feedforward filter coefficients, N+1, starts at the address X2BASE.
- Parameter Q contains the number of feedback filter coefficients, M, starts at the address X2BASE+N+1.
- Parameter R is not used.

The X2 buffer loading operation is completed after N + 1 + M writes to the FMAC_WDAT register.

Loading the Y buffer

This function starts from the address in YBASE, loads M written data from the FMAC_WDAT register into the Y buffer, increments the write pointer, and upon completion of the function, the read pointer points to the address YBASE + M.

This function can be used to preload the feedback storage parameters of an IIR filter.

- Parameter P containing the number of feedback storage parameters, M.
- Parameter Q and R are not used.

The Y buffer loading operation is completed after M writes to the FMAC_WDAT register.

30.3.6 Filter Function

By writing the corresponding value in the FUNC field of the FMAC_PARAMCFG register and setting the START bit, the corresponding function can be triggered, while the P, Q, and R bit fields must also contain the respective parameter values. Once configured, the filtering function will continue to operate until the START bit is reset by software.

FIR filter: Y = B*X

$$y[n] = 2^R \cdot \sum_{j=0}^{N} b[j] \cdot x[n-j]$$

This function is used to implement a Finite Impulse Response (FIR) filter, where vector B represents the coefficients of the FIR filter with a length of N+1. X is an infinite-length input sample vector data. The elements of Y are computed as the dot product $yn = B \cdot X_n$, where $Xn = [x_{n-N},...,x_n]$.

The FIR filter structure is shown in Figure 30-6.

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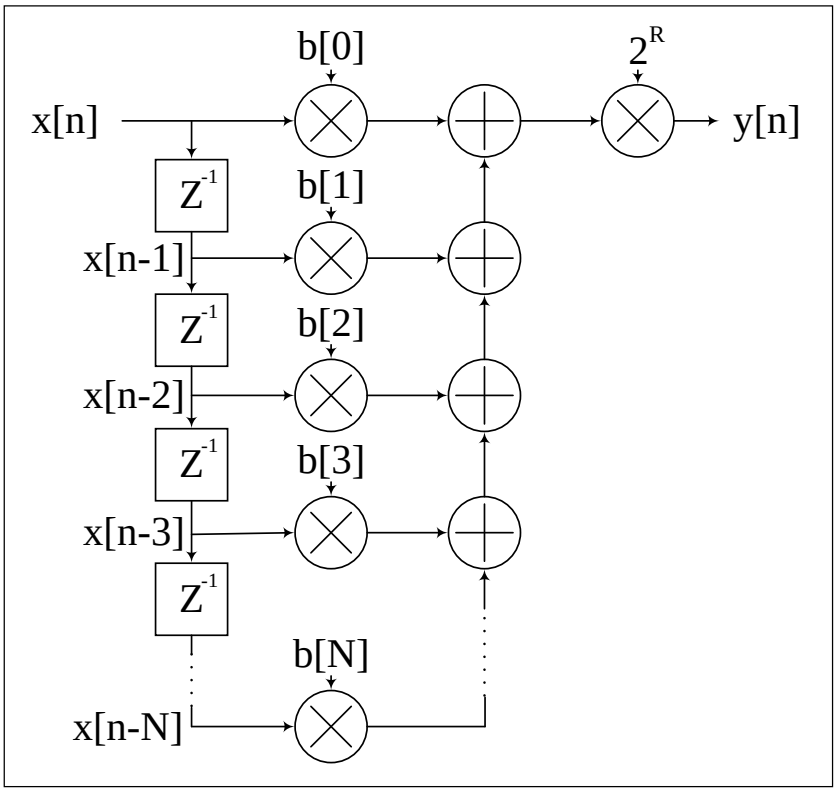
Figure 30-6 FIR Filter Structure Diagram



FIR filter input:

- The X1 buffer contains the elements of vector X, which is a circular buffer of length N + 1 + d.
- The X2 buffer contains the elements of vector B, which is a non-circular buffer of length N + 1.

FIR filter output:

- The Y buffer contains the output values y_n, which is a circular buffer of length d.

FIR filter parameters:

- Parameter P is the length of coefficient vector B, N+1, ranging from [2:127].
- Parameter R is the gain applied to the accumulator output. The value of the accumulator multiplied by 2^R is output to the Y buffer, where the range of R is [0:7].
- Parameter Q is not used.

The function ends when the FMAC_PARAMCFG.START bit is reset by software.

IIR filter: Y = B*X+A*Y

$$y[n] = 2^R \cdot (\sum_{j=0}^{N} b[j] \cdot x[n-j] + \sum_{j=1}^{M} a[j]y[n-j])$$

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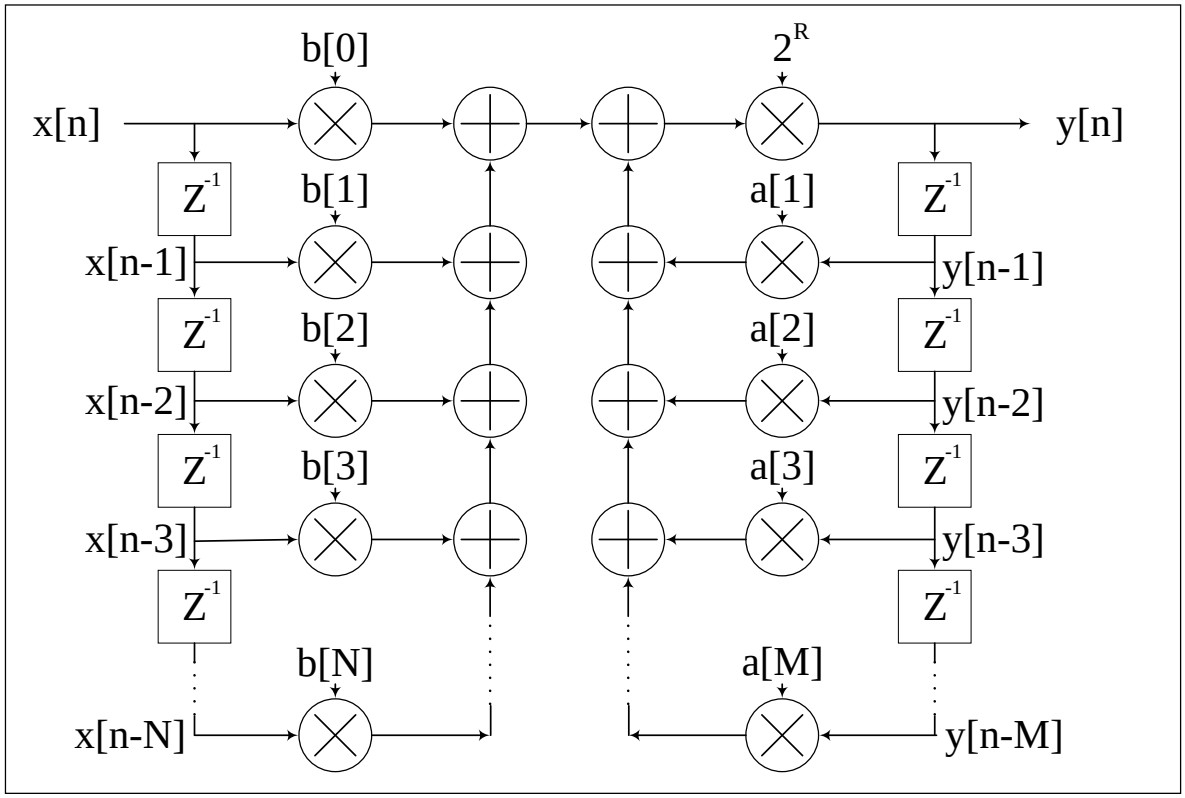
This function is used to implement an Infinite Impulse Response (IIR) filter, where the output vector Y is the convolution of the coefficient vector B (length N+1) with the infinite-length vector X, added to the convolution of the vector Y (previous output sequence) and the vector A (feedback filter coefficients). The elements of the output vector Y are calculated as yn = B·X_n + A·Y_{n-1}, where Xn = [x_{n-N}, ..., x_n] and Yn-1 = [y_{n-M}, ..., y_{n-1}].

The IIR filter structure is shown in Figure 30-7.

Figure 30-7 IIR Filter Structure Diagram



IIR filter input:

- The X1 buffer contains the elements of vector X, which is a circular buffer of length N + 1 + d.
- The X2 buffer contains the elements connected from coefficient vectors B and A (b0, b1, b2, ..., bN, aM, ..., a2, a1). This is a non-circular buffer of length M + N + 1.

IIR filter output:

- The Y buffer contains the output values yn. It is a circular buffer of length M + d.

IIR filter parameters:

- Parameter P is the length of coefficient vector B, N + 1, ranging from [2:64].
- Parameter Q is the length of coefficient vector A, M, ranging from [1:63].
- Parameter R is the gain applied to the accumulator output, where the value of the accumulator multiplied by 2^R is output to the Y buffer, and the range of R is [0:7].

When the FMAC_PARAMCFG.START bit is reset by software, the function ends.

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30.3.7 Fixed-Point Data Format

FMAC operates in signed fixed-point format, with input and output values in q1.15 format. In the q1.15 format, numbers consist of a sign bit and 15 fractional bits (binary decimal places), with a numerical range from -1 (0x8000) to 1 - 2^-15 (0x7FFF). The accumulator has 26 bits, with 22 bits for fractional parts and 4 bits for integer/sign bits (q4.22), supporting an accumulator result range from -8 (0x2000000) to +7.99999976 (0x1FFFFFF).

At the output of the accumulator, programmable gain from 0dB to 42dB can be used, with a step size of 6dB. Note that if the value exceeds the numerical range, greater than +7.99999976 or less than -8, the accumulator content wraps around. The wraparound triggered is harmless as subsequent accumulation operations will cancel out the wraparound. If a wraparound occurs, the FMAC_STS.SATF bit is set, and if the FMAC_CTRL.SATINTEN bit is set, an interrupt is generated. This aids in debugging the filter.

By setting the FMAC_CTRL.LIMITEN bit, after applying programmable gain, the data at the output of the accumulator can be optionally saturated. If LIMITEN is set to 1, any values exceeding the q1.15 output numerical range will be set to 1 - 2^-15 or -1. If LIMITEN is set to 0, any unused accumulator bits after applying gain will be simply truncated.

30.3.8 FIR Filter

FMAC can be configured as an FIR filter of length N, where N is the number of taps or filter coefficients. The minimum buffer required for an FIR filter of length N is 2N + 1, consisting of N sample data, 1 output sample, and N filter coefficients. Since the buffer size is 256, the maximum value for N is 127. For maximum throughout, a small additional space (d1 and d2) needs to be allocated for the input and output sample buffers to ensure that the filter does not stall while waiting for new input samples or reading output samples. In this scenario, the buffer requirement is 2N + d1 + d2

The FIR filter buffer can be configured as follows: X1BUFSIZE equals N + d1, X2BUFSIZE equals N, YBUFSIZE equals d2. If the output buffer does not require additional space, YBUFSIZE can be set to 1.

The base addresses of the buffers can be arbitrarily assigned, but the X2 buffer must not overlap with other buffers, as this would overwrite the coefficients. A configuration example is as follows: X2BASE equals N, X1BASE equals 0, YBASE equals 2N+d1. If storage space is limited, the X1 buffer and Y buffer can overlap, but ensure that X1BASE equals 0, X2BASE equals N, YBASE equals N. In this case, the latest output sample replaces the oldest input sample, maintaining the buffers in sync.

Note: The X1 buffer configuration register's X1BUFWM field must be configured as less than or equal to log2(d1). Otherwise, before all N input parameters are fully written (e.g., writing N-2), the buffer will be marked as full, indicating that the buffer space is full and no more input samples will be requested. Similarly, the Y buffer configuration register's YBUFWM field must be less than or equal to log2(d2), otherwise the output buffer will be marked as empty.

The X2 buffer must preload the FIR filter coefficients, while the X1 buffer can optionally preload any number of sample data, up to a maximum of N. Based on the FIR filter structure, preloading the Y buffer does not make sense.

There are three ways to read and write data in the FMAC memory: polling, interrupt, and DMA.

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Polling: No DMA or interrupt request is generated. Before writing to WDAT, software needs to ensure that the X1BUFFF flag is 0 (indicating the buffer is not full), and before reading from RDAT, software needs to ensure that the YBUFEF flag is 0 (indicating the buffer is not empty).

Interrupt: Write interrupt request is generated when X1BUFFF flag is low; read interrupt request is generated when YBUFEF flag is low.

DMA: DMA write request is generated when X1BUFFF flag is low; DMA read request is generated when YBUFEF flag is low.

Reading and writing can use different methods. However, it is not recommended to use interrupts and DMA requests simultaneously in the same operation. If interrupts and DMA requests are enabled simultaneously, only DMA can perform the transfer.

To start the filter, write the following bit field values to the FMAC_PARAMCFG register: FUNC = 8 (FIR filter); P = N (number of filter coefficients); Q = "any value"; R = gain; START = 1.

If the preloaded values in the X1 buffer are less than N + d1 - 2X1BUFWM, the X1BUFFF flag remains 0. If the FMAC_CTRL.WINTEN bit is set, an immediate write interrupt request is generated, requiring the processor to write 2X1BUFWM additional sample values into the buffer. The interrupt request remains pending until the FMAC_STS.X1BUFFF flag is set.

In the interrupt service function, the X1BUFFF flag should be checked after writing every 2X1BUFWM data until the X1BUFFF flag is set.

Similarly, if the FMAC_CTRL.DMAWEN bit is set to 1, DMA write channel requests will continue to be generated until the X1BUFFF flag is set.

The filter will only calculate the first output sample when at least N samples (including any preloaded samples) are written to the X1 buffer.

When $2^{X1BUFWM}$ output samples have been written to the Y buffer, the FMAC_STS.YBUFEF flag becomes 0.

If the FMAC_CTRL.RINTEN bit is set, an immediate read interrupt request is generated at this point, requiring the processor to read 2^{YBUFWM} samples from the buffer. The interrupt request remains pending until the FMAC_STS.YBUFEF flag is set.

In the interrupt service function, the FMAC_STS.YBUFEF flag should be checked after reading every 2^{YBUFWM} data until the FMAC_STS.YBUFEF flag is set.

Similarly, if the FMAC_CTRL.DMAREN bit is set, DMA read channel requests will continue to be generated until the FMAC_STS.YBUFEF flag is set.

The filter continues to operate in this manner until the software resets the FMAC_PARAMCFG.START bit, stopping the filter operation.

30.3.9 IIR Filter

FMAC can be configured as an IIR filter with a length of N+1 and M, where N+1 is the number of feedforward taps or coefficients, and M is the number of feedback filter coefficients, with values ranging from 1 to N.

The minimum buffer required for an IIR filter is 2N + 2M, consisting of N feedforward filter coefficients, M feedback

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filter coefficients, N input sample data, and M output sample values. Since the buffer size is 256, if M = N-1, the maximum length of the IIR filter is N = 64.

For maximum throughput, a small additional space (d1 and d2) needs to be allocated for the input and output sample buffers, in which case the buffer requirement is 2N + d1 + d2.

The IIR filter buffer can be configured as follows: X1BUFSIZE equals N + d1, X2BUFSIZE equals N+M (number of coefficients), YBUFSIZE equals M + d2.

The base addresses of the buffers can be arbitrarily assigned, but the buffers must not overlap. A configuration example is as follows: X2BASE equals 0, X1BASE equals N+M, YBASE equals 2N+M+d1.

Note: The X1 buffer configuration register's X1BUFWM field must be configured as less than or equal to log2(d1). Otherwise, before all N input parameters are fully written (e.g., writing N-2), the buffer will be marked as full, indicating that the buffer space is full and no more input samples will be requested. Similarly, the Y buffer configuration register's YBUFEF field must be less than or equal to log2(d2), otherwise the output buffer will be marked as empty.

The X2 buffer must preload the IIR filter coefficients (N feedforward, followed by M feedback), while the X1 buffer can optionally preload any number of sample data, up to a maximum of N. The Y buffer can optionally preload any number of values, with a maximum not exceeding M.

To start the IIR filter, write the following bit field values to the FMAC_PARAMCFG register: FUNC = 9 (IIR filter); P = N (number of feedforward filter coefficients); Q = M (number of feedback filter coefficients); R = gain; START = 1.

If the preloaded values in the X1 buffer are less than N + d1 - $2^{X1BUFWM}$, the X1BUFFF flag remains 0. If the FMAC_CTRL.WINTEN bit is set, an immediate write interrupt request is generated, requiring the processor to write $2^{X1BUFWM}$ additional sample values into the buffer. The interrupt request remains pending until the FMAC_STS.X1BUFFF flag is set.

In the interrupt service function, the X1BUFFF flag should be checked after writing every $2^{X1BUFWM}$ data until the X1BUFFF flag is set.

Similarly, if the FMAC_CTRL.DMAWEN bit is set, DMA write channel requests will continue to be generated until the X1BUFFF flag is set.

The filter will only calculate the first output sample when at least N samples (including any preloaded samples) are written into the X1 buffer. The calculation of the first output value uses the first N samples in the X1 buffer and the first M samples in the Y buffer (whether preloaded or not) to compute the first output sample. The first output sample is written to YBASE + M in the Y buffer.

When 2^{YBUFWM} output samples have been written to the Y buffer, the FMAC_STS.YBUFEF flag becomes 0.

At this point, if the FMAC_CTRL.RINTEN bit is set, an immediate read interrupt request is generated, requiring the processor to read 2^{YBUFWM} samples from the buffer. The interrupt request remains pending until the FMAC_STS.YBUFEF flag is set.

In the interrupt service function, the FMAC_STS.YBUFEF flag should be checked after reading every 2^{YBUFWM} data until the YBUFEF flag is set.

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Similarly, if the FMAC_CTRL.DMAREN bit is set, DMA read channel requests will continue to be generated until the YBUFEF flag is set. The filter continues to operate in this manner until the software resets the FMAC_PARAMCFG.START bit, stopping the filter operation.

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30.4 FMAC Register

30.4.1 FMAC Register Overview

Table 30-1 FMAC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	FMAC_X1BUFCFG	Reserved						X1BUFWM [1:0]		Reserved								X1BUFSIZE[7:0]								X1BASE[7:0]							
	Reset Value							0	0									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	FMAC_X2BUFCFG	Reserved																X2BUFSIZE[7:0]								X2BASE[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	FMAC_YBUFCFG	Reserved						YBUFWM [1:0]		Reserved								YBUFSIZE[7:0]								YBASE[7:0]							
	Reset Value							0	0									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	FMAC _PARAMCFG	START	FUNC[6:0]							R[7:0]								Q7:0]								P[7:0]							
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	FMAC _CTRL	Reserved															RESET	LIMITEN	Reserved					DMAWEN	DMAREN	Reserved				SATINTEN	UNINTEN	OVINTEN	WINTEN	RINTEN
	Reset Value																0	0						0	0					0	0	0	0	0
014h	FMAC _STS	Reserved																					SATF	UNF	OVF	Reserved							X1BUFFF	YBUFEF
	Reset Value																						0	0	0								0	1
018h	FMAC_WDAT	Reserved																WDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	FMAC_RDAT	Reserved																RDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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30.4.2 FMAC X1 Buffer Configuration Register (FMAC_X1BUFCFG)

Offset address: 0x00

Reset value: 0x0000 0000

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained
25:24	X1BUFWM [1:0]	Buffer watermark size Defined as the threshold set in circular mode to trigger the X1 buffer full flag. The corresponding flag will be set if the number of free spaces in the buffer is less than $2^{X1BUFWM}$. 00: Threshold is 1, 01: Threshold is 2, 10: Threshold is 4, 11: Threshold is 8 Setting a threshold greater than 1 allows multiple data transfers to the buffer in a single interrupt.If DMA write request is enabled (FMAC_CTRL.DMAWEN = 1), the threshold should be set to 1. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
23:16	Reserved	Reserved, the reset value must be maintained
15:8	X1BUFSIZE[7:0]	X1 buffer size. The X1 buffer size in 16-bit words, the minimum buffer size is the number of feedforward filter coefficients in the filter (+ watermark threshold - 1). This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
7:0	X1BASE[7:0]	X1 buffer base address. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.

30.4.3 FMAC X2 Buffer Configuration Register (FMAC_X2BUFCFG)

Offset address: 0x04

Reset value: 0x0000 0000

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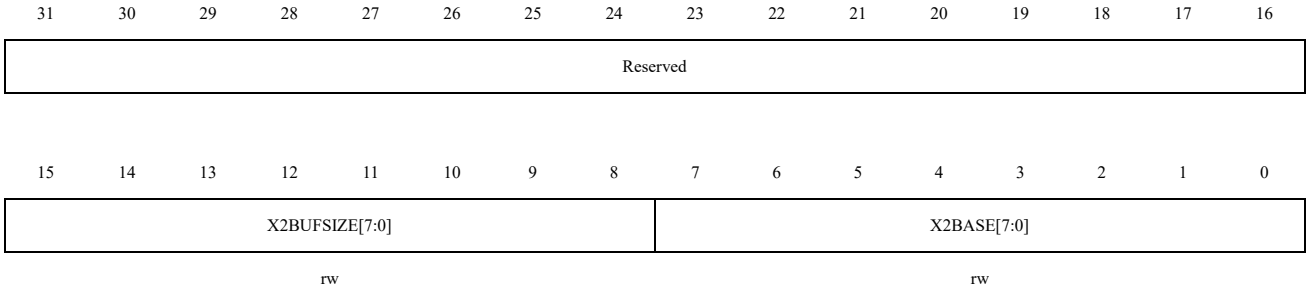
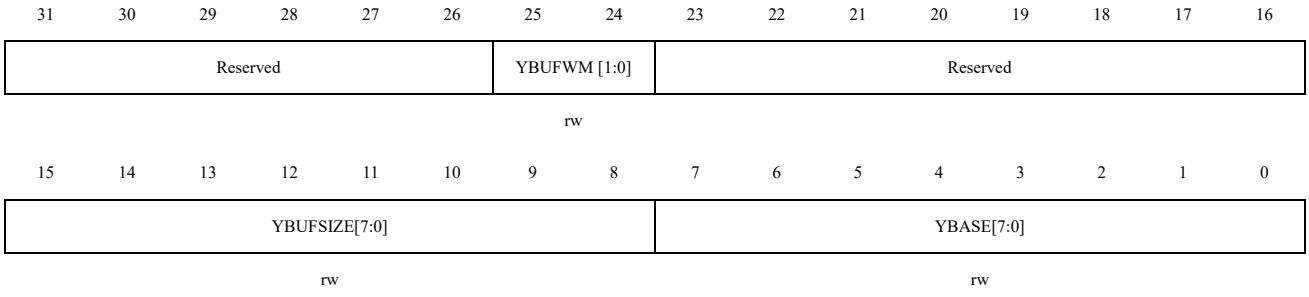


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	X2BUFSIZE[7:0]	X2 buffer size in 16-bit words. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
7:0	X2BASE[7:0]	X2 buffer base address. When START=1, the X2 buffer base address can be modified, for example when changing coefficient values. Since changing coefficients during computation can affect the results, the filter should be in a stopped state when performing this operation.

30.4.4 FMAC Y Buffer Configuration Register (FMAC_YBUFCFG)

Offset address: 0x08

Reset value: 0x0000 0000



Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained
25:24	YBUFWM [1:0]	Buffer watermark size Defined as the threshold set in circular mode to trigger the Y buffer empty flag. The corresponding flag will be set if the number of unread data in the buffer is less than

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Bit field	Name	Description
		$2^{Y1BUFWM}$. 00: Threshold is 1, 01: Threshold is 2, 10: Threshold is 4, 11: Threshold is 8 Setting a threshold greater than 1 allows multiple data transfers to the buffer in a single interrupt.If DMA read request is enabled (FMAC_CTRL.DMAREN = 1), the threshold should be set to 1.
23:16	Reserved	Reserved, the reset value must be maintained
15:8	YBUFSIZE[7:0]	Y buffer size. For FIR filters, the minimum buffer size is the watermark threshold. For IIR filters the minimum buffer size is the number of feedback taps (+ the watermark threshold).
7:0	YBASE[7:0]	Y buffer base address.

30.4.5 FMAC Parameter Configuration Register (FMAC _PARAMCFG)

Offset address: 0xC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START	FUNC[6:0]							R[7:0]							
rw	rw							rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q[7:0]								P[7:0]							
rw								rw							

Bit field	Name	Description
31	START	Enable execution. 0: Stop execution 1: Start execution Setting this bit will trigger the execution of the function selected in the FUNC bit field, but FMAC would not doing anything when FUNC is reserved. Resetting this bit by software can stop any ongoing function execution. For initialization functions, this bit is reset by hardware.
30:24	FUNC[6:0]	Function. 0: Reserved 1: Load X1 buffer 2: Load X2 buffer 3: Load Y buffer

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Bit field	Name	Description
		4 to 7: Reserved 8: FIR filter 9: IIR filter (direct form 1) 10 to 127: Reserved This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
23:16	R[7:0]	Input parameter R. The value of this parameter depends on the function. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
15:8	Q[7:0]	Input parameter Q. The value of this parameter depends on the function. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
7:0	P[7:0]	Input parameter P. The value of this parameter depends on the function. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.

30.4.6 FMAC Control Register (FMAC_CTRL)

Offset address: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															RESET
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITEN	Reserved					DMAW EN	DMAR EN	Reserved			SATINT EN	UNINT EN	OVINT EN	WINT EN	RINT EN
rw						rw	rw				rw	rw	rw	rw	rw

Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	RESET	Reset FMAC. Set this bit will reset the write and read pointers, internal control logic, FMAC_STS register, and FMAC_PARAMCFG register (if activated), including the START bit. Other register settings are not affected. This bit is reset by hardware. 0: Disable reset 1: Enable reset
15	LIMITEN	Clipping enable. 0: Clipping disabled, values exceeding the accumulator range are truncated. 1: Clipping enabled, values exceeding the accumulator range are clipped to the maximum

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Bit field	Name	Description
		positive value or minimum negative value (+1 or -1).
14:10	Reserved	Reserved, the reset value must be maintained
9	DMAWEN	Enable DMA write channel request. 0: Disabled. No DMA requests generated. 1: Enabled. DMA write requests are generated when X1 buffer is not full. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
8	DMAREN	Enable DMA read channel request. 0: Disabled. No DMA requests generated. 1: Enabled. DMA read requests are generated when Y buffer is not empty. This bit field cannot be modified when FMAC_PARAMCFG.START = 1.
7:5	Reserved	Reserved, the reset value must be maintained
4	SATINTEN	Saturation error interrupt enable. 0: Disabled. No interrupt generated when saturation is detected. 1: Enabled. Interrupt request generated if the SATF flag is set. This bit can be set and cleared by software. Reading returns the current status of this bit.
3	UNINTEN	Underflow error interrupt enable. 0: Disabled. No interrupt generated when underflow is detected. 1: Enabled. Interrupt request generated if the UNF flag is set. This bit can be set and cleared by software. Reading returns the current status of this bit.
2	OVINTEN	Overflow error interrupt enable. 0: Disabled. No interrupt generated when overflow is detected. 1: Enabled. Interrupt request generated if the OVF flag is set. This bit can be set and cleared by software. Reading returns the current status of this bit.
1	WINTEN	Write interrupt enable. 0: Disabled. No write interrupt requests generated. 1: Enabled. Interrupt request generated when the X1 buffer FULL flag is not set. This bit can be set and cleared by software. Reading returns the current status of this bit.
0	RINTEN	Read interrupt enable. 0: Disabled. No read interrupt requests generated. 1: Enabled. Interrupt request generated when the Y buffer EMPTY flag is not set. This bit can be set and cleared by software. Reading returns the current status of this bit.

30.4.7 FMAC Status Register (FMAC _STS)

Offset address: 0x14

Reset value: 0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SATF	UNF	OVF	Reserved						X1BUFFF	YBUFEF
					r	r	r							r	r

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	SATF	Saturation error flag. Saturation occurs when the accumulation result exceeds the range of the accumulator. 0: No saturation detected 1: Saturation detected. If the SATINTEN bit is set, an interrupt will be generated. This flag will be cleared after device reset.
9	UNF	Underflow error flag. When reading data from FMAC_RDAT, underflow error occurs if there is no valid data in the Y buffer. 0: No underflow detected 1: Underflow detected. If the UNINTEN bit is set, an interrupt will be generated. This flag will be cleared after device reset.
8	OVF	Overflow error flag. Overflow occurs when writing to FMAC_WDAT and there is no available space in the X1 buffer. 0: No overflow detected 1: Overflow detected. If the OVINTEN bit is set, an interrupt will be generated. This flag will be cleared after device reset.
7:2	Reserved	Reserved, the reset value must be maintained
1	X1BUFFF	X1 buffer full flag. If the available space count is less than the X1BUFWM threshold, the buffer will be marked as full. The available space count is the difference between the write pointer and the latest sample being used. 0: X1 buffer not full. If the WINTEN bit is set, interrupt requests will be generated until the flag is set. If DMAWEN is set, DMA write channel requests will be generated until this flag is set. 1: X1 buffer full. This flag is set and cleared by hardware or reset. *Note: After the last available space in the X1 buffer is filled, there will be a delay of 3 clock cycles before the X1BUFFF flag is cleared. To avoid any risk of overflow, it is recommended to insert a software delay after writing to the X1 buffer before reading FMAC_STS. Additionally, X1BUFWM=2 can be used to configure the threshold.*
0	YBUFEF	Y buffer empty flag. If the number of unread data is less than the YBUFWM threshold, the buffer will be marked as empty. The number of unread data is the difference between the read pointer and the current output target address. 0: Y buffer not empty. If the RINTEN bit is set, interrupt requests will be generated until the

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Bit field	Name	Description
		flag is set. If the DMAREN bit is set, DMA read channel requests will be generated until this flag is set." 1: Y buffer is empty. This flag is set and cleared by hardware or reset. *Note: After reading the last sample from the Y buffer, there will be a delay of 3 clock cycles before the YBUFEF flag is set. To avoid any risk of underflow, it is recommended to insert a software delay after reading data from the Y buffer before reading FMAC_STS. Additionally, YBUFWM=2 can be used to configure the threshold.*

30.4.8 FMAC Write Data Register (FMAC_WDAT)

Offset address: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDAT[15:0]															
w															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WDAT[15:0]	Write data. When accessing this register for writing, the written data will be transferred to the address offset indicated by the write pointer. After each write operation, the pointer address will automatically increment.

30.4.9 FMAC Read Data Register (FMAC_RDAT)

Offset address: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDAT[15:0]															
r															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	RDAT[15:0]	Read data. When accessing this register for reading, the data read is the content in the Y output buffer. After each read operation, the pointer address will automatically increment.

31 CORDIC Processors（CORDIC）

31.1 Introduction

CORDIC hardware computing units can accelerate mathematical functions (primarily trigonometric functions) in hardware. They are commonly used for accelerating mathematical function calculations in applications such as motor control, measurement, signal processing, and many other applications.

31.2 Main Features

- Supports rotation and vector calculation modes.
- Supports circular and hyperbolic coordinate systems.
- Once the calculation starts, any operation to read the result register will insert the bus into a waiting state until the calculation is completed, allowing the calculation result to be read out when completed without the need for polling or interrupts.
- Calculate 10 functions: sin, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm.
- Supports fixed-point(q1.31 or q1.15) and floating-point input/output modes.
- Supports interrupt, polling, and DMA request read/write modes.
- Programmable iteration precision.

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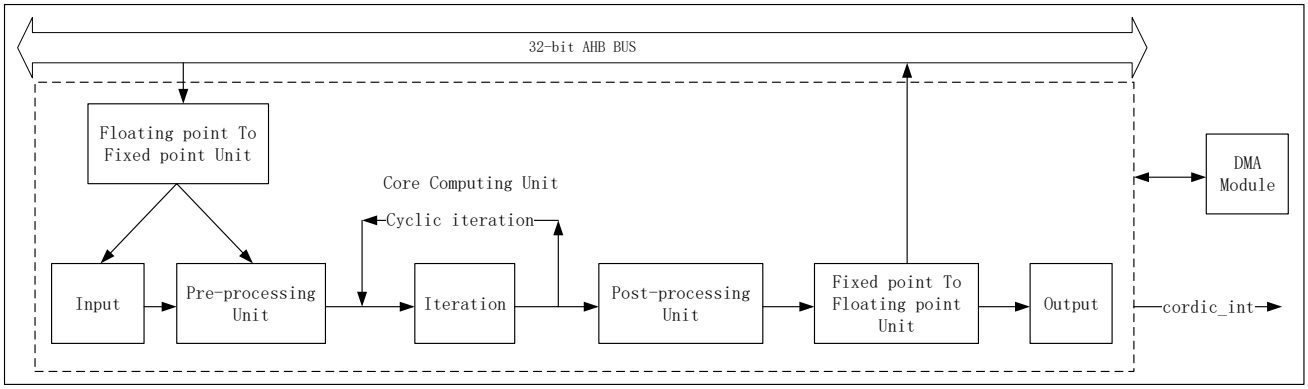
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

31.3 Block Diagram

Figure 31-1 CORDIC Block Diagram



The CORDIC hardware computing unit structural diagram above includes its main core computing unit, data preprocessing unit, data post-processing unit, floating-point to fixed-point unit, and fixed-point to floating-point unit.

Floating-point to fixed-point unit: The floating-point to fixed-point unit converts floating-point or half-precision data into corresponding q1.31 or q1.15 formats and stores them in the CORDIC_WDAT register. It is configured by the FLOATIN bit of the CORDIC_CTRLSTS register. The default is fixed-point input, and if the FLOATIN bit is configured as 1, it is set to floating-point input.

Data preprocessing unit: It processes the data in the CORDIC_WDAT register before sending it to the core computing unit of CORDIC.

Core computing unit: The processed input data is iteratively calculated to obtain the computed value, with the computational precision determined by the number of iterations which can be programmable. It supports circular and hyperbolic systems, with each system supporting rotation and vector modes.

Data post-processing unit: It processes the computed values from the core computing unit of CORDIC to obtain data in q1.31 or q1.15 format.

Fixed-point to floating-point unit: It converts q1.31 or q1.15 format data to the corresponding single-precision floating-point data or half-precision floating-point data.

31.4 Function Description

31.4.1 CORDIC Function

The functions supported by Cordic are shown in the following tables.

Table 31-1 CORDIC Function Overview

Function	Primary Parameter	Secondary Parameter	Primary Result	Secondary Result
Cosine	Angle θ	Modulus m	m * cos θ	m * sin θ
Sine	Angle θ	Modulus m	m * sin θ	m * cos θ

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Email: sales@nsing.com.sg

Function	Primary Parameter	Secondary Parameter	Primary Result	Secondary Result
Phase	x	y	atan2(y,x)	$\sqrt{x^2+y^2}$
Modulus	x	y	$\sqrt{x^2+y^2}$	atan2(y,x)
Arctangent	x	none	$\tan^{-1}x$	none
Hyperbolic cosine	x	none	cosh x	sinh x
Hyperbolic sine	x	none	sinh x	cosh x
Hyperbolic actangent	x	none	$\tanh^{-1}x$	none
Natural logarithm	x	none	ln x	none
Square root	x	none	$\sqrt{x}$	none

Through the above 10 functions, more functions can be indirectly obtained.

For example, $e^x = \sinh(x) + \cosh(x)$.

Cosine Function

Table 31-2 Cosine Parameters

Parameter	Range	Description
First input parameter (θ)	[-1, 1)	It is the angle value θ, measured in radians (rad), with the rangeθ∈[-π, π). When using it, first divide the target angle θ by π to convert it to the range [-1, 1), and then write it in signed fixed-point (q1.31 and q1.15 formats) or floating-point data (single-precision and half-precision) to the CORDIC_WDATA register.
Second input parameter (m)	[0, 1]	It represents the magnitude of the function. When m ≥ 1, the software scales m down to the [0, 1] range, and then writes it in signed fixed-point (q1.31 and q1.15 formats) or floating-point data (single-precision and half-precision) to the CORDIC_WDATA register.
First output result m * cos(θ)	[-1, 1)	If m has been scaled down by software before, the output data needs to be correspondingly scaled up to obtain the actual result.
Second output result m * sin(θ)	[-1, 1)	If m has been scaled down by software before, the output data needs to be correspondingly scaled up to obtain the actual result.
Scaling factor (n)	Unavailable	Configure SCALE[2:0] as 3'b000.

Note:

1. When the magnitude m > 1, the software can choose the scaling ratio.

Sine Function

Table 31-3 Sine **Parameters**

Parameter	Range	Description
First input parameter (θ)	[-1, 1)	It is the angle value θ, measured in radians (rad), with the rangeθ∈[-π, π).

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Parameter	Range	Description
		When using it, first divide the target angle θ by π to convert it to the range [-1, 1), and then write it in signed fixed-point (q1.31 and q1.15 formats) or floating-point data (single-precision and half-precision) to the CORDIC_WDATA register.
Second input parameter (m)	[0, 1]	It represents the magnitude of the function. When m ≥ 1, the software scales m down to the [0, 1] range, and then writes it in signed fixed-point (q1.31 and q1.15 formats) or floating-point data (single-precision and half-precision) to the CORDIC_WDATA register.
First output result m * sin (θ)	[-1, 1)	If m has been scaled down by software before, the output data needs to be correspondingly scaled up to obtain the actual result.
Second output result m * cos(θ)	[-1, 1)	If m has been scaled down by software before, the output data needs to be correspondingly scaled up to obtain the actual result.
Scaling factor (n)	Unavailable	Configure SCALE[2:0] as 3'b000.

Note:

1. When the magnitude m > 1, the software can choose the scaling ratio.

Phase(atan2(y, x)) Function

Table 31-4 Phase Parameters

Parameter	Range	Description
First input parameter (x)	[-1, 1)	x represents the abscissa value in the Cartesian coordinate system. If x ≥ 1 or x <-1, software scaling to the q1.31 range is required.
Second input parameter (y)	[-1, 1)	y represents the ordinate value in the Cartesian coordinate system. If y ≥ 1 or y <-1, software scaling to the q1.31 range is required.
First output result θ = atan2(y,x)	[-1, 1)	The angle corresponding to the coordinate position (x, y), [-1, 1) corresponds to [-π, π). Multiplying this output data by π gives the actual angle value. Note that, due to the nature of phase angles, values close to π may sometimes be calculated as -π.
Second output result $m=\sqrt{x^2+y^2}$	[0, 1)	If x and y have been scaled before, the magnitude needs to be proportionally enlarged.
Scaling factor (n)	Unavailable	Configure SCALE[2:0] as 3'b000.

Note:

1. *If either x or y exceeds the range [-1, 1), both x and y need to be proportionally scaled together, not just one. This ensures that the angle corresponding to the coordinates remains unchanged before and after scaling.*
2. *When $\sqrt{x^2+y^2} \geq 1$, the magnitude m can only be saturated to the maximum value of the fixed-point format ($1-2^{-15}$ or $1-2^{-31}$). Before proportionally scaling x and y, consider the magnitude of the scaling factor to avoid saturation of the magnitude as much as possible.*

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Modulus($\sqrt{x^2+y^2}$) Function

Table 31-5 Modulus Parameters

Parameter	Range	Description
First input parameter (x)	[-1, 1)	x represents the abscissa value in the Cartesian coordinate system. If the desired x value is not within the range, it needs to be scaled to the range [-1, 1).
Second input parameter (y)	[-1, 1)	y represents the abscissa value in the Cartesian coordinate system. If the desired y value is not within the range, it needs to be scaled to the range [-1, 1).
First output result $m=\sqrt{x^2+y^2}$	[0, 1)	If x and y have been scaled before, the magnitude needs to be proportionally enlarged.
Second output result θ = atan2(y,x)	[-1, 1)	The angle corresponding to the coordinate position (x, y) corresponds to [-1, 1) corresponding to [-π, π). Multiplying this output data by π gives the actual angle value. Note that, due to the nature of phase angles, values close to π may sometimes be calculated as -π.
Scaling factor (n)	Unavailable	Configure SCALE[2:0] as 3'b000.

Note:

1. *If either x or y exceeds the range [-1, 1), both x and y need to be proportionally scaled together, not just one. This ensures that the angle corresponding to the coordinates remains unchanged before and after scaling.*
2. *When $\sqrt{x^2+y^2} \geq 1$, the magnitude m can only be saturated to the maximum value of the fixed-point format ($1-2^{-15}$ or $1-2^{-31}$). Before proportionally scaling x and y, consider the magnitude of the scaling factor to avoid saturation of the magnitude as much as possible.*

Arctangent($\tan^{-1}(x)$) Function

This mode is used to calculate the $\tan^{-1}(x)$ function. It has only one input and one output.

Table 31-6 Arctangent Parameters

Parameter	Range	Description
First input parameter ($x * 2^{-n}$)	[-1, 1)	If |x| > 1, the software must scale it down by a factor of 2^(-n) to ensure x is within the range [-1, 1). The scaling factor n is written in the SCALE[10:8] bit field.
Second input parameter	-	Not applicable
First output result $\theta = \tan^{-1}x * 2^{-n}$	[-1, 1)	[-1, 1) corresponds to [-π, π), so the output result needs to be multiplied by π and 2^n to obtain the actual angle value.
Second output result	-	Not applicable
Scaling factor (n)	[0, 7]	Configure SCALE[2:0] as n.

Hyperbolic cosine (cosh (x)) Function

This mode is used to calculate the cosh(x) function. It has one input and two outputs.

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Table 31-7 Hyperbolic cosine Parameters

Parameter	Range	Description
First input parameter (x *2^{-n})	[-0.559, 0.559]	Only x values within the range of [-1.118, +1.118] are supported. The software scales x down by a factor of 2^(-n). The factor n=1 must be written into the SCALE[10:8] bit.
Second input parameter	-	Not applicable
First output result cosh (x) * 2^{-n}	[-0.5, 0.846]	Hyperbolic cosine value cosh (x). The first output result must be multiplied by 2^n to obtain the correct result.
Second output result sinh (x) * 2^{-n}	[-0.683, 0.683]	Hyperbolic sine value sinh (x). The second output result must also be multiplied by 2^n to obtain the correct result.
Scaling factor (n)	1	Can only be configured as 3'b001.

Hyperbolic sine (sinh(x)) Function

This mode is used to calculate the sinh(x) function. It has one input and two outputs

Table 31-8 Hyperbolic sine Parameters

Parameter	Range	Description
First input parameter (x *2^{-n})	[-0.559, 0.559]	Only x values within the range of [-1.118, +1.118] are supported. The software scales x down by a factor of 2^(-n). The factor n=1 must be written into the SCALE[10:8] bit.
Second input parameter	-	Not applicable
The first output result sinh (x) * 2^{-n}	[-0.683, 0.683]	Hyperbolic cosine value sinh (x). The first output result must be multiplied by 2^n to obtain the correct result.
The second output result cosh (x) * 2^{-n}	[-0.5, 0.846]	Hyperbolic sine value cosh (x). The second output result must also be multiplied by 2^n to obtain the correct result.
Scaling factor (n)	1	Configure SCALE[2:0] as 3'b001.

Hyperbolic arctangent (tanh^{-1}(x)) Function

This mode is used to calculate the tanh^{-1}(x) function. It has only one input and one output.

Table 31-9 Hyperbolic arctangent Parameters

Parameter	Range	Description
First input parameter (x *2^{-n})	[-0.403, 0.403]	Only x values within the range of [-0.806, 0.806] are supported. The software scales x down by a factor of 2^(-n). The factor n=1 must be written into the SCALE[10:8] bit.
Second input parameter	-	Not applicable
First output result	[-0.559, 0.559]	Multiplying the output data by 2^n yields the inverse hyperbolic tangent

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Parameter	Range	Description
$\tanh^{-1}(x) *2^{-n}$		$\tanh^{-1}(x)$.
Second output result	-	Not applicable
Scaling factor (n)	1	Configure SCALE[2:0] as 3'b001.

Natural logarithm (ln(x)) Function

This mode is used to calculate the ln(x) function. It has one input and one output

Table 31-10 Natural logarithm Parameters

Parameter	Range	Description
First input parameter $(x *2^{-n})$	[0.054, 0.875]	For x∈[0.107, 9.35], if not within the range, the software needs to scale x down by a factor of 2^(-n) to [0.054, 0.875]. Then write n into the SCALE[10:8] bit.
Second input parameter	-	Not applicable
First output result $\ln(x) * 2^{-(n+1)}$	[-0.279, 0.137]	Multiplying the output data by 2^(n+1) yields the natural logarithm ln(x).
Second output result	-	Not applicable
Scaling factor (n)	[1, 4]	Configure SCALE[2:0] as n.

To ensure calculation accuracy, it is recommended to use the scaling factors in the table below for different inputs:

n	x range	Input parameter range
1	$0.107 \le x < 1$	$0.0535 \le \frac{x}{2^n} < 0.5$
2	$1 \le x < 3$	$0.25 \le \frac{x}{2^n} < 0.75$
3	$3 \le x < 7$	$0.375 \le \frac{x}{2^n} < 0.875$
4	$7 \le x \le 9.35$	$0.4375 \le \frac{x}{2^n} < 0.584$

Square root ($\sqrt{x}$) Function

This function calculates the square root of the input parameter x, with one input and one output.

Table 31-11 Square root Parameters

Parameter	Range	Description
First input parameter $(x *2^{-n})$	[0.027, 0.875]	For x∈[0.027, 2.34], if not within the range, the software needs to scale x down by a factor of 2^(-n) to [0.054, 0.875]. Then write n into the SCALE[10:8] bit threshold.

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Parameter	Range	Description
Second input parameter	-	Not applicable
First output result $2^{-n} * \sqrt{x}$	[0.04, 1]	Multiplying the output data by 2^n yields √x.
Second output result	-	Not applicable
Scaling factor (n)	[0, 2]	Configure SCALE[2:0] as n.

To ensure calculation accuracy, it is recommended to use the scaling factors in the table below for different inputs.

n	x range	Input parameter range
0	$0.027 \leq x < 0.75$	$0.027 \leq （\frac{x}{2}） < 0.75$
1	$0.75 \leq x < 1.75$	$0.375 \leq （\frac{x}{2}） < 0.875$
2	$1.75 \leq x \leq 2.341$	$0.4375 \leq （\frac{x}{2}） \leq 0.585$

31.4.2 Data Format

The input and output data of the CORDIC module support signed integer fixed-point formats (q1.31 and q1.15) and floating-point data (single-precision and half-precision). Floating-point data needs to be converted according to the IEEE 754 standard before writting to the data register.

The FLOATIN bit of the CORDIC_CTRLSTS register configures the data input format, with the default being fixed-point format input. Setting the FLOATIN bit to 1 enables floating-point input.

The FLOATOUT bit of the CORDIC_CTRLSTS register configures the data output format, with the default being fixed-point format output. Setting the FLOATOUT bit to 1 enables floating-point output. The INSIZE bit of the CORDIC_CTRLSTS register is used to configure the width of the input data, with the default being 32 bits width.

If configured as 32-bit, the input data should be in q1.31 fixed-point format or single-precision floating point, meaning that the input data written to the CORDIC_WDAT register should be in q1.31 fixed-point format (FLOATIN = 0) or single-precision floating point (FLOATIN = 1) format.

If configured as 16-bit, the input data should be in q1.15 fixed-point format or half-precision floating-point format, that is, the input data written to the CORDIC_WDAT register is in q1.15 fixed-point format (FLOATIN = 0) or half-precision floating-point format (FLOATIN = 1).

The NUMWRITE bit of the CORDIC_CTRLSTS register is used to configure the number of input data, with the default setting being to input a single data parameter (NUMWRITE = 0).

If configured with NUMWRITE = 0, and if the data input width is set to 32-bit (INSIZE = 0), one can input a q1.31 fixed-point format or single-precision floating-point data; if the data input width is set to 16-bit (INSIZE = 1), two q1.15 fixed-point format or half-precision floating-point data can be input, with the first parameter placed in the lower 16 bits and the second parameter placed in the higher 16 bits.

If configured with NUMWRITE = 1, only two q1.31 fixed-point format or single-precision floating-point data can

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be input. The output data format remains the same as above.

31.4.3 Scaling Factor

The preceding functions specify a scaling factor SCALE. This allows the extended function input range to cover all values supported by CORDIC without causing input, output, or internal register saturation. If a scaling factor is required, it must be calculated in software and programmed into the SCALE field of the CORDIC_CTRLSTS register. When scaling down the value in the CORDIC_WDAT register and programming the scaling factor SCALE, the input parameters must also be correspondingly scaled down. Finally, the scaling down must be undone for the result read from the CORDIC_RDAT register, i.e., multiplied by 2^n to obtain the correct value.

Note: The scaling factor may result in loss of precision due to truncation of the scaling value.

31.4.4 Precision

Each clock cycle, CORDIC can perform four iterations.Table 31-2 lists the maximum error after every four iterations for each function and the number of clock cycles required to achieve that precision. Based on this table, the required number of cycles can be determined and programmed into the precision field of the CORDIC_CTRLSTS register. Once the programmed number of iterations is completed, the CORDIC processor stops immediately, and the results can be read instantly.

Table 31-12 CORDIC Precision

Iteration Cycle.	Maximum Residual Error			
	Normal	16-bit fixed-point output	16-bit floating-point output	16-bit floating-point input
COS，SIN				
1	2^{-3}	2^{-3}	2^{-2}	2^{-2}
2	2^{-7}	2^{-6}	2^{-6}	2^{-6}
3	2^{-10}	2^{-10}	2^{-9}	2^{-10}
4	2^{-14}	2^{-13}	2^{-10}	2^{-12}
5	2^{-18}	2^{-14}	2^{-10}	2^{-12}
6	2^{-18}	2^{-14}	2^{-10}	2^{-12}
PHASE，MODULUS				
1	2^{-3}	2^{-3}	2^{-3}	2^{-3}
2	2^{-7}	2^{-7}	2^{-7}	2^{-7}
3	2^{-12}	2^{-12}	2^{-9}	2^{-12}
4	2^{-13}	2^{-13}	2^{-9}	2^{-13}
5	2^{-13}	2^{-13}	2^{-9}	2^{-13}
6	2^{-13}	2^{-13}	2^{-9}	2^{-13}
ARCTAN				

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Email: sales@nsing.com.sg

Iteration Cycle.	Maximum Residual Error			
	Normal	16-bit fixed-point output	16-bit floating-point output	16-bit floating-point input
1	2^{-3}	2^{-3}	2^{-3}	2^{-3}
2	2^{-7}	2^{-7}	2^{-7}	2^{-7}
3	2^{-12}	2^{-12}	2^{-10}	2^{-12}
4	2^{-15}	2^{-14}	2^{-10}	2^{-16}
5	2^{-18}	2^{-14}	2^{-10}	2^{-16}
6	2^{-19}	2^{-14}	2^{-10}	2^{-16}
HB_COS，HB_SIN，HB_ARCT，LN				
1	2^{-3}	2^{-3}	2^{-3}	2^{-3}
2	2^{-7}	2^{-7}	2^{-7}	2^{-7}
3	2^{-11}	2^{-11}	2^{-9}	2^{-11}
4	2^{-14}	2^{-13}	2^{-10}	2^{-14}
5	2^{-17}	2^{-14}	2^{-10}	2^{-14}
6	2^{-18}	2^{-14}	2^{-10}	2^{-14}
SQRT				
1	2^{-7}	2^{-7}	2^{-7}	2^{-7}
2	2^{-14}	2^{-13}	2^{-10}	2^{-14}
3	2^{-18}	2^{-13}	2^{-10}	2^{-14}
4	2^{-18}	2^{-13}	2^{-10}	2^{-14}
5	2^{-18}	2^{-13}	2^{-10}	2^{-14}
6	2^{-18}	2^{-13}	2^{-10}	2^{-14}

Note:

1. *All other cases (32-bit fixed-point input, 32-bit fixed-point output, 32-bit floating-point input, 32-bit floating-point output, 16-bit fixed-point input) are categorized under normal mode. In Table 31-12, if there are multiple applicable modes, the maximum error is considered.*

2. *In PHASE and MODULUS modes, the precision of the resulting angle is limited by the precision of the input y and x ratios. x and y should be scaled synchronously. To ensure a precision of 10^{-4}, one of the input data x or y should be greater than 0.005 (0.125 for 16-bit input). The precision data in Table 31-12 is calculated under the condition that one of x or y is greater than 0.005 (0.125). For higher precision, optimal precision can be achieved when one of x or y is close to 1. When one of x or y is greater than 0.1, the number of iteration cycles is 5 or 6 (in 32-bit mode), and precision can reach 10^{-5}. Table 31-13 lists the precision of PHASE and MODULUS when the x and y ratios are larger.*

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Table 31-13 Supplementary Table for PHASE and MODULUS Precision

Iteration Cycle.	Maximum Residual Error			
	32-bit input		16-bit input	
	max(x,y) > 0.005 (able to achieve a precision of 10^{-4})	max(x,y) > 0.05 （optimal precision）	max(x,y) > 0.125 (able to achieve a precision of 10^{-4})	max(x,y) > 0.5 （optimal precision）
1	2^{-3}	2^{-3}	2^{-3}	2^{-3}
2	2^{-7}	2^{-7}	2^{-7}	2^{-7}
3	2^{-12}	2^{-12}	2^{-12}	2^{-12}
4	2^{-13}	2^{-15}	2^{-13}	2^{-14}
5	2^{-13}	2^{-18}	2^{-13}	2^{-14}
6	2^{-13}	2^{-18}	2^{-13}	2^{-14}

31.4.5 Operation Mode

CORDIC operation modes: Zero-Overhead Mode, Polling Mode, Interrupt Mode, and DMA Mode.

31.4.5.1 Zero-Overhead Mode

The fastest way to use the coprocessor is to pre-program the CORDIC_CTRLSTS register, which includes the desired function (FUNC), the required number of clock cycles (PRECISION), the number of bits for input and output values (INSIZE, OUTSIZE), the number of input parameters (NUMWRITE) and results (NUMREAD), and the scaling factor (SCALE) if applicable.

Subsequently, triggering the computation is done by writing the input parameters into the CORDIC_WDAT register. Once the correct number of input parameters is written (and any ongoing computation has completed), a new computation is initiated using these input parameters and the current CORDIC_CTRLSTS settings. If there are no changes, there is no need to reprogram the CORDIC_CTRLSTS register.

If dual 32-bit input parameters are required (INSIZE = 0, NUMWRITE = 1), the first input parameter must be written first, followed by the second input parameter. If the second parameter remains constant across a series of computations, it can be avoided to write it a second time by reprogramming the parameter count to one (INSIZE = 0) after the first calculation has started.

If using two 16-bit parameters (INSIZE = 1), they must be packed into a 32-bit word, with the primary parameter in the least significant half-word and the secondary parameter in the most significant half-word. The packed 32-bit word is then written into the CORDIC_WDAT register. In this scenario (NUMWRITE = 0), only one write operation is required.

For functions that only require one input parameter, it is recommended to set NUMWRITE = 0. If NUMWRITE = 1, a second write to CORDIC_WDAT must be performed to trigger the computation. In this case, the data for the second input is not used.

Once the computation begins, any attempt to read the CORDIC_RDAT register will result in a bus wait state until the computation is completed, and then the result will be returned. Therefore, software can write the input and

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

immediately read the result without polling to see if it is valid. Alternatively, the processor can wait for the appropriate number of clock cycles before reading the result. If needed, this time can be used to program the CORDIC_CTRLSTS register for the next computation and prepare the next input data. The CORDIC_CTRLSTS register can be reprogrammed during computation without affecting the results of the ongoing computation. Similarly, once the previous parameters start the computation, the CORDIC_WDAT register can be updated with the next parameters. The next parameters and settings remain pending until the previous computation is completed.

After the computation is completed, the result can be read from the CORDIC_RDAT register. If two 32-bit results are needed (OUTSIZE = 1, NUMWRITE = 0), the first result is read first, followed by the second result. If only one 32-bit result is needed (NUMWRITE = 0, OUTSIZE = 0), the first result is output during the first read.

If a 16-bit result is needed (OUTSIZE = 1), a single read of CORDIC_RDAT will pack both results into a single 32-bit word. The first result will be in the lower half-word, and the second result will be in the upper half-word. In this case, it is recommended to program NUMWRITE = 0. If NUMWRITE = 1, a second read of CORDIC_RDAT must be performed to release CORDIC for the next operation. The data from the second read must be discarded.

The next computation starts when the expected number of results has been read, provided that the expected number of parameters has been written. This means that at any given time, there may be one ongoing computation or waiting for result, and one pending operation. Any further access to CORDIC_WDAT while the operation is pending will cancel the pending operation and overwrite the data.

31.4.5.2 Polling Mode

When new results are available in the CORDIC_RDAT register, the RRF flag is set in the CORDIC_CTRLSTS register. This flag can be queried by reading the register, and reading the CORDIC_RDAT register once or twice (depending on the NUMWRITE field of the CORDIC_CTRLSTS register) will reset the RRF flag.

Polling the RRF flag takes slightly longer than directly reading the CORDIC_RDAT register because the results are not read immediately when available. However, the program and bus interface do not halt when reading the CORDIC_CTRLSTS register, so this mode might be a good choice if stopping the program is unacceptable (e.g., low-latency interrupt handling is required).

31.4.5.3 Interrupt Mode

By setting the interrupt enable (INTEN) bit in the CORDIC_CTRLSTS register, an interrupt is generated whenever the RRF flag is set. The interrupt is cleared when the RRF flag is reset. This mode allows reading the computation results under an interrupt service routine, giving it a priority over other tasks. However, due to the delay in interrupt handling, it is slower than directly reading the results or polling the flag.

31.4.5.4 DMA Mode

If the DMA write enable (DMAWEN) bit is set in the CORDIC_CTRLSTS register and there are no pending operations, a DMA write channel request is issued. The DMA controller can transfer the first input parameter from memory to the CORDIC_WDAT register. If NUMWRITE = 1 in the CORDIC_CTRLSTS register, a second DMA write channel request is issued to transfer the second input parameter to the CORDIC_WDAT register. Once all input parameters have been written and any ongoing computation has been completed (verified by reading the results), a new computation will be initiated, triggering another DMA write channel request.

If the DMA read enable (DMAREN) bit is set in the CORDIC_CTRLSTS register, the RRF flag being valid will generate a DMA read channel request. Subsequently, the DMA controller can transfer the first result from the

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CORDIC_RDAT register to memory. If NUMWRITE = 1 in the CORDIC_CTRLSTS register, a second DMA request is generated to read the second result. Once all results have been read, the RRF flag becomes invalid.

The DMA read and write channels can be enabled separately. If both channels are enabled, CORDIC can autonomously perform repetitive computations on the data buffer without processor intervention, allowing the program to execute other tasks. The DMA controller operates in memory-to-peripheral mode for the write channel and in peripheral-to-memory mode for the read channel. It is important to note that the timing is initiated by setting the DMAWEN flag in the program. Subsequently, the generation speed of DMA read and write requests can match the speed at which CORDIC processes data.

In some cases, input data may be stored in memory, and the output is periodically transferred to another peripheral device, such as a digital-to-analog converter. In this scenario, a DMA request is generated by the target peripheral every time new data is needed. The DMA controller can directly fetch the next sample from the CORDIC_RDAT register (in this case, the DMA controller operates in memory-to-peripheral mode, even if the source is a peripheral register). The behavior of reading results allows CORDIC to start a new computation, thereby generating a DMA write channel request for the DMA controller to transfer the next input value to the CORDIC_WDAT register. At this point, the DMA write channel is enabled (DMAWEN = 1), but the read channel is not enabled.

Similarly, data from another peripheral device (such as an ADC) can be directly transferred to the CORDIC_WDAT register in a similar manner (in peripheral-to-memory mode). The DMA write channel cannot be enabled in this case as well. If DMAREN = 1, CORDIC processes the input data and generates a DMA read request upon completion. The DMA controller then transfers the results from the CORDIC_RDAT register to memory (peripheral-to-memory mode)

Note:

1. *DMA requests are not generated to program the CORDIC_CTRLSTS register. Therefore, DMA mode is only useful when repeatedly executing the same function with the same settings. It is also important to note that the scaling factor cannot be changed during a series of DMA transfers.*
2. *For each DMA request, a response signal must be issued before the DMA can access the CORDIC_WDAT or CORDIC_RDAT registers. If unrelated accesses to the relevant registers occur before the DMA issues the response signal, it may block the DMA channel. Therefore, when the DMA read channel is enabled, CPU accesses to the CORDIC_RDAT register must be avoided. Similarly, when the DMA write channel is enabled, the program must avoid accessing the CORDIC_WDAT register.*

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31.5 CORDIC Registers

31.5.1 CORDIC Registers Overview

Table 31-14 Cordic Registers Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000h	CORDIC_CTRLSTS	RRF	INOVF	Reserved		INOVINTEN	CODINLIMIT	PHASELIMIT	FLOATOUT	FLOATIN	INSIZE	OUTSIZE	NUMWRITE	NUMREAD	DMAWEN	DMAREN	INTEN	Reserved					SCALE[2:0]			PRECISION[3:0]				FUNC[3:0]			
	Reset Value	0	0			0	0	0	0	0	0	0	0	0	0	0	0						0	0	0	0	1	0	1	0	0	0	0
0004h	CORDIC_WDAT	WDAT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0008h	CORDIC_RDAT	RDAT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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31.5.2 CORDIC Control Status Register (CORDIC_CTRLSTS)

Offset address: 0x00

Reset value: 0x0000 0050

Each time data is written to the control status register, any stored but unprocessed data is discarded to prevent previous data from being computed using the current control configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RRF	INOVF	Reserved		INOV INTEN	CODIN LIMIT	PHASE LIMIT	FLOAT OUT	FLOAT IN	INSIZE	OUTSIZE	NUM WRITE	NUM READ	DMAWEN	DMAREN	INTEN
r	rw			rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SCALE[2:0]			PRECISION[3:0]				FUNC[3:0]			
					rw			rw				rw			

Bit field	Name	Description
31	RRF	Result Ready Flag. 0: No new data in the CORDIC_RDAT register. 1: New data in the CORDIC_RDAT register. This bit is set by hardware when the CORDIC operation is completed. It is reset by hardware after reading the CORDIC_RDAT register (NUMREAD + 1) times. When this bit is set, if the INTEN bit is also set, the CORDIC generates a read interrupt. If the DMAREN bit is also set, a DMA read channel request is generated. When this bit is set, no new computation is initiated
30	INOVF	Input Overflow Flag. 0: No input overflow event has occurred or input overflow interrupt control is not enabled. 1: An input overflow event has occurred. *Note: Writing a 1 to this bit clears it to 0, writing a 0 has no effect.*
29:28	Reserved	Reserved, the reset value must be maintained.
27	INOVINTEN	Input Overflow Interrupt Control Bit. 0: Disabled 1: Enabled. Setting INOVF to 1 when an input overflow occurs.
26	CODINLIMIT	Coordinate Output Limit Control. 0: No restriction on coordinate output result 1: Limit coordinate output result to prevent overflow In some cases, outputs close to 1 may overflow to -1 or vice versa. If CODINLIMIT = 1, when an overflow occurs, the positive output is limited to 1, and the negative output is limited to -1.
25	PHASELIMIT	Phase Output Limit Control. 0: No restriction on phase output 1: Limit phase output

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Bit field	Name	Description
		If PHASELIMIT = 1, when an overflow occurs, the positive phase is limited to π, and the negative phase is limited to -π.
24	FLOATOUT	Floating-point Fixed-point Output Control. 0: Fixed-point output 1: Floating-point output
23	FLOATIN	Floating-point Fixed-point Input Control. 0: Fixed-point input 1: Floating-point input
22	INSIZE	Input Data Width. 0: 32-bit 1: 16-bit If configured as 32-bit, the data written to the CORDIC_WDAT register is in q1.31 fixed-point format or single-precision floating-point. If configured as 16-bit, the data written to the CORDIC_WDAT register is in q1.15 fixed-point format or half-precision floating-point.
21	OUTSIZE	Output Data Width. 0: 32-bit 1: 16-bit If configured as 32-bit, the data output from the CORDIC_RDAT register is in q1.31 fixed-point format or single-precision floating-point. If configured as 16-bit, the data output from the CORDIC_RDAT register is in q1.15 fixed-point format or half-precision floating-point.
20	NUMWRITE	CORDIC_WDAT Register Parameter Count. 0: Only one 32-bit value needs to be written for the next computation (or two 16-bit values if INSIZE = 1). 1: Two 32-bit values must be written to the CORDIC_WDAT register to trigger the next computation. In some condition with 2 arguments, the second argument remains unchanged for a series of calculations. It is allowable to set NUMWRITE =0 and only write the first argument. Reading will return the current state of the bit.
19	NUMREAD	Number of results that can be read from the CORDIC_RDAT register. 0: When the next computation is completed, only one 32-bit value (or two 16-bit values if OUTSIZE = 1) is transferred to the CORDIC_RDAT register. 1: Two 32-bit values are transferred to the CORDIC_RDAT register. When the next computation is completed, two 32-bit values are transferred to the CORDIC_RDAT register. It requires two reads of CORDIC_RDAT to reset the RRF flag. Some functions (such as PHASE) have two result outputs, and if the second result is not needed, it is allowed to set NUMREAD = 0.
18	DMAWEN	DMA Write Request Enable. 0: Disabled. No DMA write request is generated.

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Bit field	Name	Description
		1: Enabled. DMA write requests are generated when there is no operation is pending. This bit is set and cleared by software. The current state of this bit is returned when read.
17	DMAREN	DMA Read Request Enable. 0: Disabled. No DMA read request is generated. 1: Enabled. DMA read requests are generated when the RRF is set. This bit is set and cleared by software. The current state of this bit is returned when read.
16	INTEN	Interrupt Enable. 0: Disabled. No interrupt request is generated. 1: Enabled. An interrupt request is generated when the RRF flag is set. This bit is set and cleared by software. The current state of this bit is returned when read.
15:11	Reserved	Reserved, the reset value must be maintained.
10:8	SCALE[2:0]	Scaling Factor: $2^{SCALE[2:0]}$ 000：2^0 001：2^1 010：2^2 … 110：2^6 111：2^7 When the actual input parameters exceed the specified input data range [-1,1), the actual input parameters need to be divided by $2^{SCALE[2:0]}$ and the output data needs to be multiplied by $2^{SCALE[2:0]}$ to obtain the actual output result. For example: CORDIC_WDAT = actual input parameters / $2^{SCALE[2:0]}$ Actual output result = CORDIC_RDAT * $2^{SCALE[2:0]}$
7:4	PRECISION[3:0]	Iteration Count. 0: Reserved 1-15: Iteration count/4 Determines the number of iterations required for a specific precision. For most functions, the suggested range for this field is 3-6 iterations. Note: Higher iteration count results in higher precision.
3:0	FUNC[3:0]	Functions: 4'b0: COS 4'b1: SIN 4'b2: PHASE 4'b3: MODULUS 4'b4: ARCTANT 4'b5: HB_COS: Hyperbolic Cosine 4'b6: HB_SIN: Hyperbolic Sine 4'b7: HB_ARCT: Hyperbolic Arctangent 4'b8: NATL: Natural Logarithm

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Bit field	Name	Description
		4'b9: SQRT: Square Root 4'b10~4'b15: Reserved

31.5.3 CORDIC Write Data Register (CORDIC_WDAT)

Offset address: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WDAT[31:16]															
w															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDAT[15:0]															
w															

Bit field	Name	Description
31:0	WDAT[31:0]	Write Data. When a write access is made to this register, the write data is transferred to the address offset indicated by the write pointer. After each write, the pointer address automatically increments. This register is programmed based on the input parameters of the function selected in the FUNC field of the CORDIC_CTRLSTS register. If selecting the 32-bit format (INSIZE = 0) and requiring two input parameters (NUMWRITE = 1), then this register needs to be written to consecutively twice. The main parameter is written in the first instance, followed by the secondary parameter in the second instance. If selecting the 32-bit format and only needing one input parameter (NUMWRITE = 0), then writing to this register only once is required, containing the main parameter. If the selected format is 16-bit (INSIZE = 1), then writing to this register only once is needed, containing both parameters. The main parameter is located in WDAT[15:0], and the secondary parameter is located in WDAT[31:16]. In this case, NUMWRITE must be set to 0. For the parameters required for each function and their allowable ranges, please refer to section 31.4.1. After writing the required number of parameters, if the previous computation has been completed, CORDIC will evaluate the function specified in the FUNC field using the provided input parameters. If a computation is in progress, the values of the main parameter and secondary parameter remain pending until the computation is completed and the results are read. During this time, writes to the register will cancel the pending operation and overwrite the parameter data.

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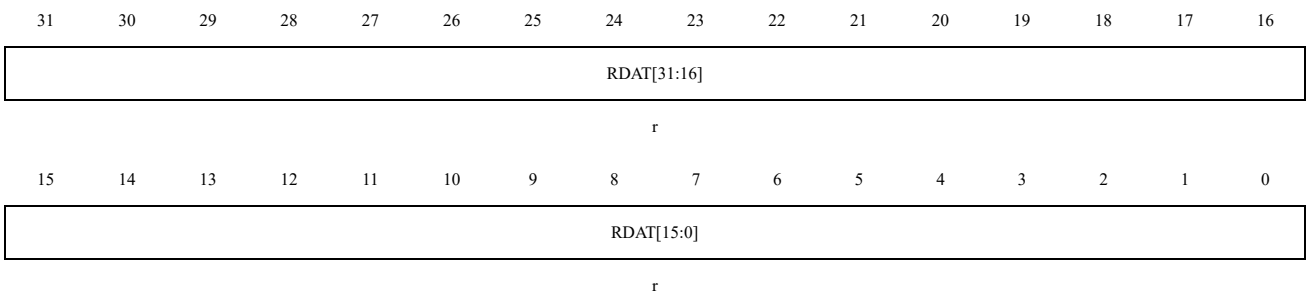
31.5.4 CORDIC Read Data Register (CORDIC_RDAT)

Offset address: 0x08

Reset value: 0x0000 0000



Bit field	Name	Description
31:0	RDAT[31:0]	Output Data. If the 32-bit format is selected (OUTSIZE = 0) and two output values are expected (NUMREAD = 1), this register must be read twice when setting the RRF flag. The first read retrieves the main result (the first output result). The second read retrieves the secondary result (the second output result) and resets the RRF. If the 16-bit format is selected (OUTSIZE = 1), the lower half of this register, RDAT[15:0], contains the main result (the first output result), and the upper half, RDAT[31:16], contains the secondary result (the second output result). In this case, NUMREAD must be set to 0, and only one read operation is required. Reading data from this register will reset the RRF flag in the CORDIC_CTRLSTS register.

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32 Digital filter for sigma delta modulators (DSMU)

32.1 Introduction

The DSMU module is designed to interface with external ΣΔ modulators. It supports up to 8 external digital serial interfaces (channels) and includes up to 4 digital filters. These filters offer flexible Sigma Delta stream digital processing options, enabling up to 24-bit final ADC resolution. Additionally, the DSMU can optionally accept parallel data stream input from internal ADC peripherals or device memory.

32.2 Main feature

- Supports up to 8 multiplexed digital serial input channels:
  - Customizable SPI interface for various ΣΔ modulators connection
  - Customizable Manchester coded 1-wire interface support
  - Clock signal output for ΣΔ modulator(s)
- Supports up to 8 internal digital parallel channels:
  - Each input supporting up to 16-bit resolution
  - Internal sources from ADCs data or CPU/DMA write(memory) data
- Configurable digital signal processing:
  - Sinc^x filter: Adjustable order/type (1 to 5) and oversampling ratio (1 to 1024)
  - Integrator: Adjustable oversampling ratio (1 to 256)
- Support up to 24-bit output data resolution:
  - Right bit-shifter for final data (0 to 31 bits)
- Signed filter output data
- Automatic data offset correction (user-stored offset in register)
- Continuous or single conversion
- Start-of-conversion synchronization with:
  - Software trigger
  - Internal timers trigger
  - External events trigger
  - Start-of-conversion synchronize with first DSMU filter (DSMU_FLT0)
- Analog watchdog feature:
  - Low and high value threshold registers
  - Configurable Sinc^x digital filter (order = 1 to 3, oversampling ratio = 1 to 32)

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- Input from filter output data register or from serial channels (1 to 8)
- Continuous monitoring independent of standard conversion

- Short-circuit detector for saturated analog input values (bottom and top ranges):
  - 8-bit counter to detect 1 to 256 consecutive 0's or 1's in the input data stream
  - Continuous monitoring of each channel (8 serial channel transceiver outputs)
- Break generation on analog watchdog or short-circuit detector event
- Extremes detector:
  - Store minimum and maximum output data values
  - Refreshed by software reading
- DMA support for reading converted data
- Interrupts: End of conversion, overrun, analog watchdog, short-circuit, channel clock absence
- Two types of conversions:
  - Regular: Triggred by lesser priority software only, can be requested anytime or in continuous mode without affecting the timing of injected conversions
  - Injected: Higher priority, multiple trigger sources and precise timing.

32.3 Implementation

Table 32-1 DSMU Function Overview

DSMU function	DSMU
Number of channels	8
Numbers of filters	4
Internal ADC bus	3
Supported trigger sources	32
Analog watchdog	4
Analog watchdog sinc filter	8

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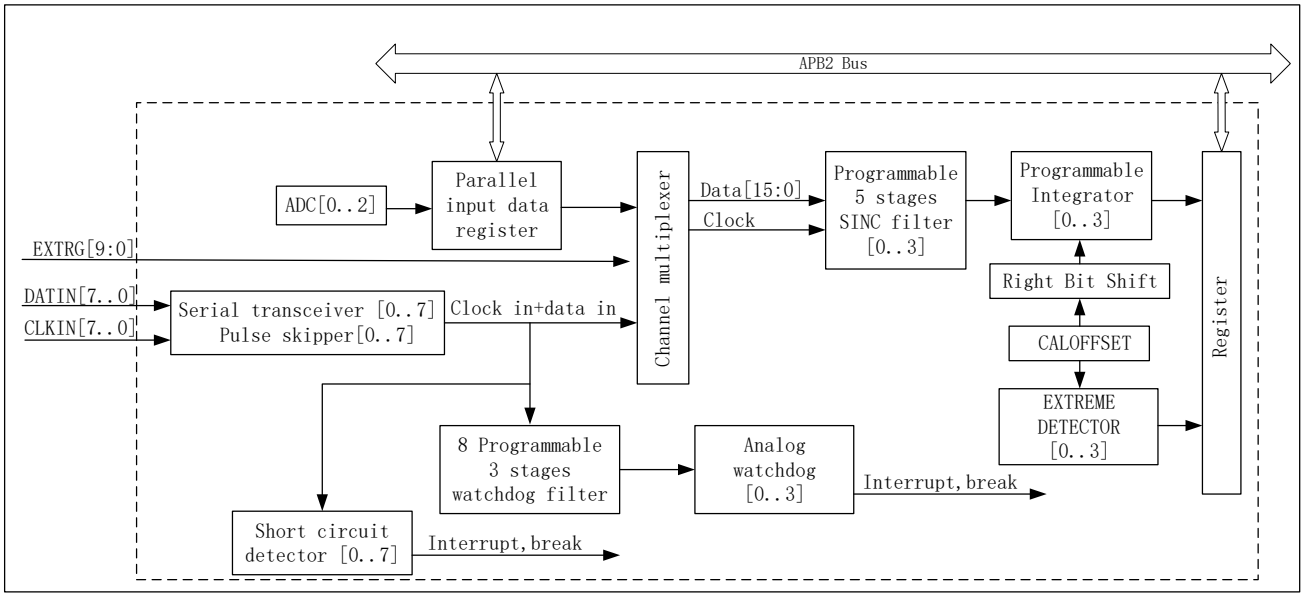
32.4 DSMU Function description

32.4.1 DSMU block diagram

Figure 32-1 DSMU block diagram



Note:

- APB2 clock frequency should be equal or smaller than DSMU clock.
- Audio clock should choose specific clock frequency, that after divided by 2-256, the generated clock frequency can be used for audio frequency, for example 44.1 kHz or 48.0 kHz.
- For serial transceiver, DSMU clock needs to be at least 4 times faster than SPI clock, or at least 6 times higher than Manchester data rate.
- For parallel transceiver, DSMU clock needs to be at least 2(4 if interleaved mode) times faster than the input data rate.
- ADC supports interleave mode, i.e. ADC1, ADC2 data arrives on ADC1 bus. It also supports triple mode, i.e. ADC1, ADC2, and ADC3 data arrive on ADC1 bus.
- If user want to use interleave mode (ADC1 ADC2) or triple mode (ADC1 ADC2 ADC3), the APB clock and DSMU clock both need to be at least 4 times higher than the ADC data rate.
- If Manchester coding is used, the user also needs to configure the CLKOUTDIV value for recovering Manchester coded data.

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32.4.2 DSMU signals

32.4.2.1 External connection

Table 32-2 DSMU external signals

Name	Singnal Type	Description
VDD	Power supply	Digital power supply.
VSS	Power supply	Digital ground power supply.
CKIN[7:0]	Clock input	Clock signal provided from external ΣΔ modulator.
DATIN[7:0]	Data input	Data signal provided from external ΣΔ modulator.
CKOUT	Clock output	Clock output to provide clock signal into external ΣΔ modulator.
EXTRG[9:0]	External trigger signal	Input trigger from EXTI signals to start analog conversion (from GPIOs: EXTI6~15).

32.4.2.2 Triggers connection

The trigger signals for injected conversions can be configured by JEXTSEL[4:0] bits in DSMU_FLTxCTRL1 register.

The signal sources are shown in the table below.

Table 32-3 DSMU trigger signal connection

Signals	Trigger signal sources
dsmu_jtrg0	ATIM1_TRGO
dsmu_jtrg1	ATIM2_TRGO
dsmu_jtrg2	ATM3_TRGO
dsmu_jtrg3	ATIM4_TRGO
dsmu_jtrg4	GTIMB1_TRGO
dsmu_jtrg5	GTIMB2_TRGO
dsmu_jtrg6	GTIMB3_TRGO
dsmu_jtrg7	GTIMA1_TRGO
dsmu_jtrg8	GTIMA2_TRGO
dsmu_jtrg9	GTIMA3_TRGO
dsmu_jtrg10	GTIMA4_TRGO
dsmu_jtrg11	GTIMA5_TRGO
dsmu_jtrg12	ATIM1_TRGO2
dsmu_jtrg13	ATIM3_TRGO2
dsmu_jtrg14	SHRTIM1_ADC_TRG1
dsmu_jtrg15	SHRTIM1_ADC_TRG2
dsmu_jtrg16	SHRTIM1_ADC_TRG3
dsmu_jtrg17	SHRTIM1_ADC_TRG4
dsmu_jtrg18	SHRTIM2_ADC_TRG1
dsmu_jtrg19	SHRTIM2_ADC_TRG2
dsmu_jtrg20	SHRTIM2_ADC_TRG3
dsmu_jtrg21	SHRTIM2_ADC_TRG4

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Signals	Trigger signal sources
dsmu_jtrg22	EXTI6
dsmu_jtrg23	EXTI7
dsmu_jtrg24	EXTI8
dsmu_jtrg25	EXTI9
dsmu_jtrg26	EXTI10
dsmu_jtrg27	EXTI11
dsmu_jtrg28	EXTI12
dsmu_jtrg29	EXTI13
dsmu_jtrg30	EXTI14
dsmu_jtrg31	EXTI15

Note: Trigger width should be at least 1 DSMU clock cycle long for DSMU to detect the active rising or falling edge.

32.4.2.3 Break connection

The break signal connections are shown in the table below.

Table 32-4 DSMU break signal connection

Signals	Connection
dsmu_brk0	ATIM1/ATIM2/ATIM3/GTIMB1 brkin5 SHRTIMx_FLT1/5
dsmu_ brk1	ATIM1/ATIM2/ATIM3 brk2in6 GTIMB2 brkin6 SHRTIMx_FLT2/6
dsmu_ brk2	ATIM1/ATIM3/ATIM4/GTIMB3 brkin7 SHRTIMx_FLT3
dsmu_ brk3	ATIM1/ATIM3/ATIM4 brk2in8 SHRTIMx_FLT4

32.4.3 DSMU reset and clocks

DSMU on-off control

DSMU has a global enable bit DSMUEN in DSMU_CH0CFG1 register. Once DSMUEN=1, all channels and digital filters start to work if their enable bits are set:

- For channels: CHEN bit in DSMU_CHyCFG1 register.
- For filters: DFLTEN bit in DSMU_FLTxCTRL1 register.

Once DFLTEN=1, both Sincx filter unit and integrator unit are reinitialized.

If clear DFLTEN, any conversion is immediately stop and filter goes to stop mode. All others register remain unchanged except filter status registers are reset (i.e. DSMU_FLTxAWDSTS and DSMU_FLTxSTS).

Once CHEN=1, the channel starts to receive serial data from external ΣΔ modulator or parallel internal data (ADCs or CPU/DMA from memory).

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Before stopping the system clock to enter the STOP mode, DSMU must be globally disabled (i.e. DSMUEN=0)

32.4.3.1 DSMU clocks

DSMU has clock domains as below.

1. PCLK2 domain: For configure/status/data registers under APB2 bus. PCLK2 can be up to 100 Mhz.
2. DSMU_CLK domain: For all DSMU internal blocks includes channel transceivers, digital processing blocks (digital filter, integrator), additional blocks (Analog watchdog, short-circuit detector, extremes detector, conversion control and channel multiplexer).

   DSMU_CLK can be selected from PCLK2(by default), PLL1, PLL2, PLL3, SYSCLK. Users need to make sure DSMU_CLK >= PCLK2 freq.

   For serial channel transceivers. DSMU_CLK should be at least 4 times faster than external serial clock for SPI standard or 6 times faster if Manchester coding is used.

   DSMU filter takes at least two DSMU_CLK cycles to process one sample data.

   The DSMU can generate an external output clock signal via CKOUT pin to control the clock input(s) of external ΣΔ modulator(s). The clock signal must fall within the range specified in the device datasheet. It is created from either the DSMU clock or the audio clock (as determined by the CLKOUTSRC bit in the DSMU_CH0CFG1 register) and can be adjusted using a programmable divider (CLKOUTDIV in the DSMU_ CH0CFG1 register). with the range of 2 to 256.
3. ACLK domain: The audio clock source comes from RCC. By properly configuration the clock source and division factors, the DSMU can produce an accurate audio clock frequency for audio application.

32.4.3.2 Generated clocks configure sequence

Turn on generated clock

1. Configure CLKOUTSRC and CLKOUTDIV in DSMU_CH0CFG1.
2. Set DSMUEN = 1 in DSMU_ CH0CFG1.
3. Set ACLK / DSMU_CLK from RCC.

Turn off generated clock

1. Turn off DSMUEN.
2. If DSMU_CLK is used, wait for 2 DSMU_CLK cycles. If ACLK is used, wait for 3 ACLK cycles.

32.4.4 Serial channel transceivers

There are 8 multiplexed serial data channels available for conversion by each filter, Analog watchdog, or Short-circuit detector. These channels receive data stream from external ΣΔ modulator. The data can be transmitted either in SPI format or Manchester coded format, as specified by the SITP[1:0] bits in DSMU_CHyCFG1 register.

To enable a channel, set CHEN=1 in DSMU_CHyCFG1 register.

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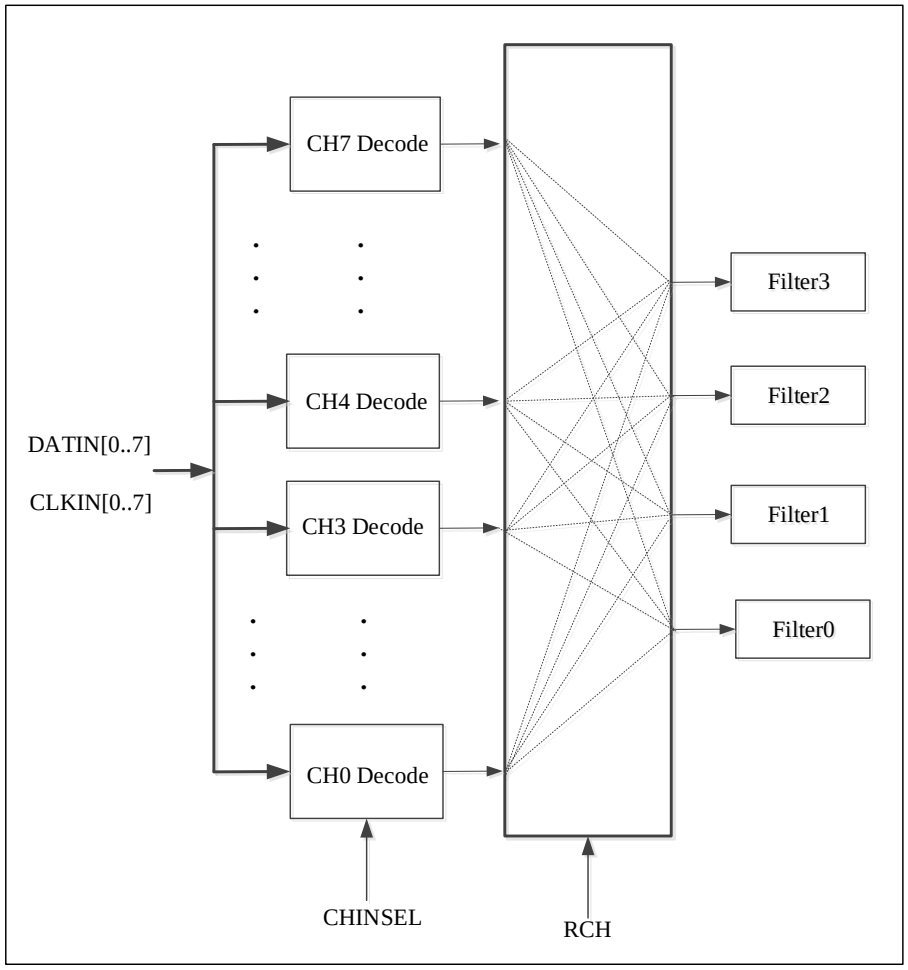
32.4.4.1 Channel input selection

Serial input pins for data and clock signals can be redirected from specific channel pins. This redirection is controlled by the CHINSEL bit in the DSMU_CHyCFG1 register. Channel redirection is used for collecting audio data from PDM (Pulse Density Modulation) stereo microphone. A PDM stereo microphone has one data signal and one clock signal. The data signal carries information for both left and right audio channel (the rising clock edge for the left channel while the falling clock edge for the right channel).

e.g. The PDM microphone input Serial channels configuration:

1. DSMU input serial channel y and CLKOUT connect to PDM microphone data and clock respectively.
2. For channel y: Set CHINSEL to 0 to use the pins DSMU_DATIN[y] and DSMU_CKIN[y].
3. For channel (y-1) (modulo 8): Set CHINSEL to 1 to use the pins DSMU_DATIN[y] and DSMU_CKIN[y].
4. For channel y: Set SITP[1:0] to 0 to sample data on the rising edge, which corresponds to the left audio channel.
5. For channel (y-1): Set SITP[1:0] to 1 to sample data on the falling edge, which corresponds to the right audio channel.
6. Assign two DSMU filters to channel y and channel (y-1) to filter left and right channels from the PDM microphone.

Figure 32-2 DSMU channel mux



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32.4.4.2 Output clock generation

The CKOUT pin can provide a clock signal for external ΣΔ modulators. This signal's frequency comes from either the DSMU clock or the audio clock, divided by a pre-scaler (set by CLKOUTDIV in the DSMU_CH0CFG1 register).

If the output clock stops, the CKOUT signal goes low. User can stop the clock by setting CLKOUTDIV to 0 or DSMUEN to 0 in the DSMU_CH0CFG1 register.

Before changing the clock source (CLKOUTSRC), ensure the CKOUT signal has stopped to avoid glitches. The output clock frequency should be between 0 and 20 MHz. The internal clock multiplexer is not glitch-free and cannot change the clock on the fly.

32.4.4.3 SPI data input format operation

The SPI data is sent serially using data and clock signals. The data signal always comes from the DSMU_DATIN[y] pin. The clock signal can come from either the DSMU_CKIN[y] pin (external) or be derived internally from the CKOUT source.

If using an external clock (SPICLKCFG[1:0]=0), the data on the DSMU_DATIN[y] pin is sampled on the rising or falling edge of the DSMU_CKIN[y] pin, as set by the SITP[1:0] bits in the DSMU_CHyCFG1 register.

The internal clock can only be used if the external ΣΔ modulator uses CKOUT as clock input to ensure synchronized operation. Using the internal clock saves pin connections for other uses.

The clock signal frequency must be between 0 to 20 MHz for SPI and less than $f_{DSMUCLK}/4$.

32.4.4.4 Manchester coded data input format operation

The Manchester data stream is sent serially through the DSMU_DATIN[y] pin. The decoded data and clock signals are recovered from this stream after Manchester decoding. There are two possible Manchester coding settings (configured by the SITP[1:0] bits in the DSMU_CHyCFG1 register):

- Rising edge = logic 0; Falling edge = logic 1
- Rising edge = logic 1; Falling edge = logic 0

The recovered clock signal frequency for Manchester coding must be between 0 and 10 MHz and less than fDSMUCLK/6.

To correctly receive Manchester coded data, the CLKOUTDIV divider (in the DSMU_CH0CFG1 register) must be set according to the expected Manchester data rate using the appropriate formula:

$((CLKOUTDIV + 1) * T_{DSMU_CLK}) < T_{Manchester\ clock} < (2 * CLKOUTDIV * T_{DSMU_CLK})$

32.4.4.5 Clock absence detection

The serial clock inputs for channels can be monitored to check if the clock is present or absence, ensuring correct conversion and error reporting. You can enable or disable clock absence detection for each input channel using the CLKABEN bit in the DSMU_CHyCFG1 register. When enabled, this detection runs continuously on the selected channel.

If a clock absence is detected, the CLKABF[y] flag is set to 1, and an interrupt can be triggered if CLKABIEN is set to 1. You can find the clock absence flags in the DSMU_FLT0STS register and enable detection in the DSMU_CHyCFG1 register. After clearing the clock absence flag using the CLRCLKABF bit in the

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DSMU_FLT0INTCLR register, the flag is refreshed.

The CLKABF[y] flag is also set by hardware when the corresponding channel is disabled (CHEN[y] = 0).

When a clock absence event occurs, data conversion, analog watchdog, and short-circuit detection may provide incorrect data. The user should handle this event and discard the affected data.

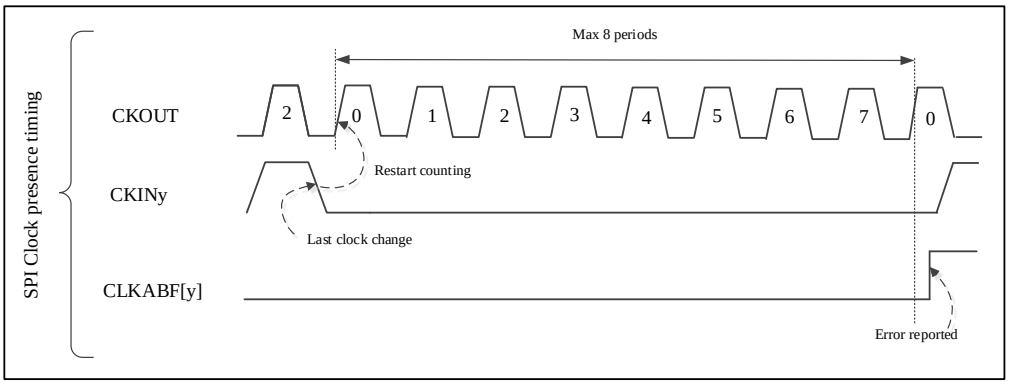
Clock absence detection is only available when the system clock is used for the CKOUT signal (CLKOUTSRC=0 in the DSMU_CH0CFG1 register).

If the transceiver is not synchronized, the clock absence flag is set and cannot be cleared using the CLRCLKABF[y] bit in the DSMU_FLT0INTCLR register. The software sequence for clock absence detection:

- Enable the channel by setting CHEN to 1
- Clear the clock absence flag by setting CLRCLKABF to 1. Repeat this until the flag is cleared (CLKABF = 0). This indicates the transceiver is synchronized and ready to receive data.
- Enable the clock absence detection feature by setting CLKABEN to 1 and the associated interrupt by setting CLKABIEN to 1. This will detect if the SPI clock is lost or if Manchester data edges are missing.

The SPI clock absence detection compares the external input clock with the output clock (CKOUT signal). The external input clock must change at least once every 8 periods of the CKOUT signal, which is controlled by the CLKOUTDIV field in the DSMU_CH0CFG1 register.

Figure 32-3 Clock absence timing diagram for SPI



The Manchester clock absence means the clock cannot be recovered from the Manchester coded signal. For correct clock recovery, the data must first transition from 1 to 0 or 0 to 1. After initial synchronization, clock absence detection compares changes in the coded serial data input signal with the output clock (CKOUT signal).

There must be a voltage level change on the DSMU_DATIN[y] pin within 2 periods of the CKOUT signal, controlled by the CLKOUTDIV bits in the DSMU_CH0CFG1 register. This condition sets the minimum data rate needed to correctly recover Manchester coded data and clock signals. The maximum data rate for Manchester coded data must be less than the CKOUT signal.

To correctly receive Manchester coded data, the CLKOUTDIV divider must be set according to the appropriate formula:

$((CLKOUTDIV + 1) * T_{DSMU_CLK}) < T_{Manchester\ clock} < (2 * CLKOUTDIV * T_{DSMU_CLK})$

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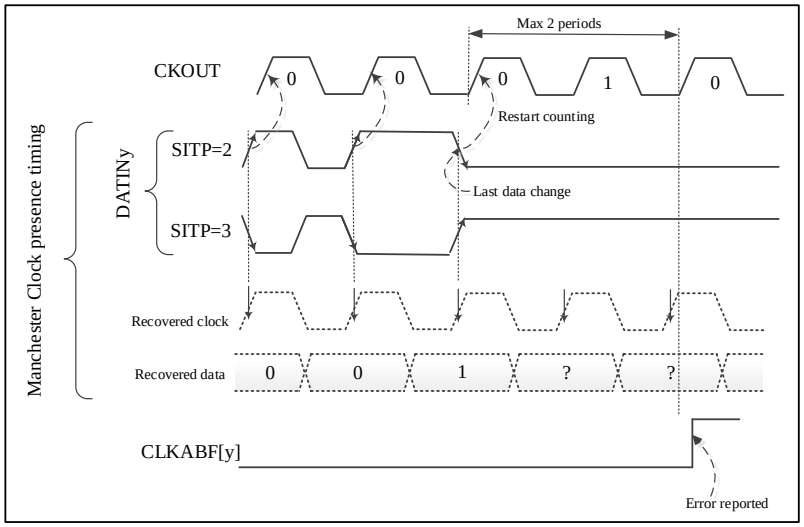
If an input clock recovery error occurs, a clock absence flag (CLKABF[y] = 1) is set, and an interrupt can be triggered if CLKABIEN is set to 1. You can find the clock absence flags in the DSMU_FLT0STS register and enable detection in the DSMU_CHyCFG1 register. After clearing the clock absence flag using the CLRCLKABF bit in the DSMU_FLT0INTCLR register, the flag is refreshed.

Figure 32-4 Clock absence timing diagram for Manchester coding



32.4.4.6 Manchester/SPI code synchronization

To synchronize the Manchester coded stream after enabling the channel (CHEN=1 in the DSMU_CHyCFG1 register), follow these steps:

1. Initial Synchronization: The stream must first detect a data transition from 0 to 1 or 1 to 0.
2. Check Synchronization: Poll the CLKABF[y] flag. If it is set, clear it by setting the CLRCLKABF[y] bit in the DSMU_FLT0INTCLR register.
3. Repeat if Necessary: If the channel is not yet synchronized, the hardware will immediately set the CLKABF[y] flag again. Continue clearing the flag and polling until the CLKABF[y] flag remains clear, indicating synchronization.
4. Set CLKOUTDIV: Ensure the CLKOUTDIV divider in the DSMU_CH0CFG1 register is set according to the expected Manchester data rate.

$$((CLKOUTDIV + 1) * T_{DSMU_CLK}) < T_{Manchester\ clock} < (2 * CLKOUTDIV * T_{DSMU_CLK})$$

SPI The SPI coded stream synchronizes after detecting the first valid rising or falling edge of the clock input signal.

If the transceiver is not yet synchronized, the clock absence flag will be set and cannot be cleared using the CLRCLKABF[y] bit in the DSMU_FLT0INTCLR register

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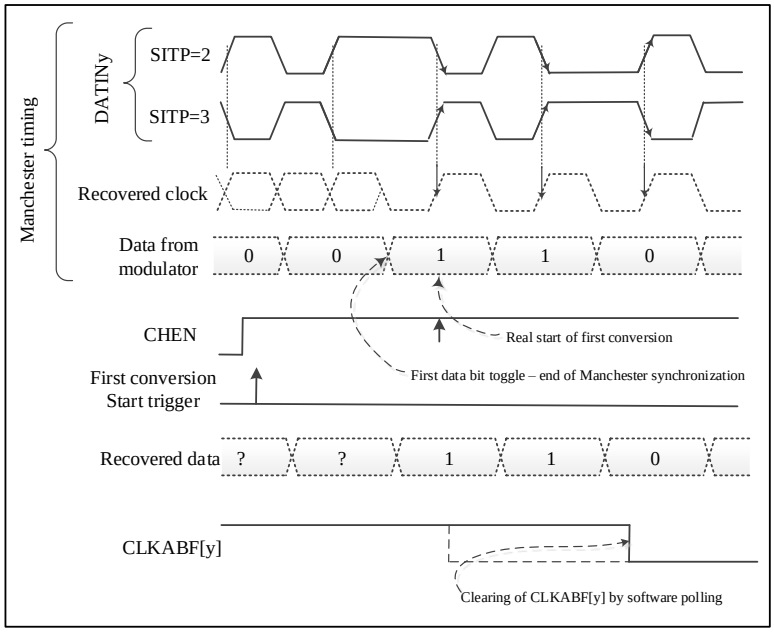
Figure 32-5 First conversion for Manchester coding (Manchester synchronization)



32.4.4.7 External serial clock frequency measurement

Measuring the serial clock input frequency of a channel provides the actual data rate from an external ΣΔ modulator, which is crucial for applications. This frequency can be measured by a timer that counts DSMU clocks (fDSMUCLK) during one conversion cycle. The counting starts with the first input data clock after a conversion trigger (regular or injected) and ends with the last input data clock before the conversion finishes (when the end of conversion flag is set).

Each conversion duration (time between the first and last serial sample) is recorded in the COVCNT[27:0] counter in the DSMU_FLTxCOVTIM register when the conversion is complete (JEOCF=1 or REOCF=1). The user can then calculate the data rate based on the digital filter settings (FORD, FOSR, IOSR, FAST). The external serial frequency measurement stops only if the filter is bypassed (FOSR=0, only the integrator is active, COVCNT[27:0]=0 in the DSMU_FLTxCOVTIMR register).

For parallel data input, the measured frequency is the average input data rate during one conversion.

If the conversion is interrupted (e.g., by disabling/enabling the selected channel), the interruption time is also counted in COVCNT[27:0]. Therefore, it is recommended not to interrupt the conversion to get an accurate conversion duration result.

32.4.4.8 Channel calibration offset setting

Each channel has its own offset setting, stored in a register, which is subtracted from each conversion result (injected or regular) for that channel. Offset calibration occurs after the data is right shifted. The offset is stored as a 24-bit signed value in the CALOFFSET[23:0] field in the DSMU_CHyCFG2 register.

32.4.4.9 Data right bit shift

To align the result to a 24-bit value, each channel specifies the number of right-bit shifts to apply to each conversion result (injected or regular). This bit shift number is stored in the DATRBS[4:0] bits in the DSMU_CHyCFG2 register.

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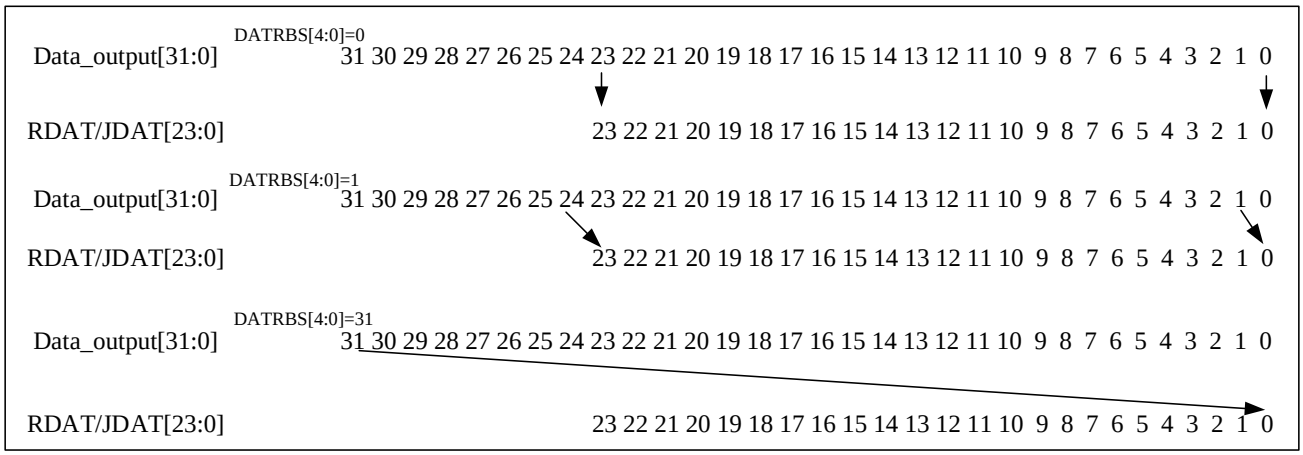
The right bit-shift rounds the result to the nearest integer while maintaining the sign, ensuring the result is in a valid 24-bit signed format.

Figure 32-6 Data right bit shift example



32.4.4.10 Configuration the input serial interface

To configure the input serial interface, set the following parameters:

- **Output Clock Predivider:** Use the CLKOUTDIV[7:0] bits in the DSMU_CH0CFG1 register to set a programmable predivider (range: 2 - 256) for generating the output clock from the DSMU clock.
- **Serial Interface Type and Input Clock Phase:** Select SPI or Manchester coding and the sampling edge of the input clock using the SITP[1:0] bits in the DSMU_CHyCFG1 register.
- **Input Clock Source:** Choose between an external source from the DSMU_CKIN[y] pin or an internal source from the CKOUT pin using the SPICLKCFG[1:0] field in the DSMU_CHyCFG1 register.
- **Final Data Right Bit-Shift:** Define the number of right bit shifts to align the result to a 24-bit value using the DATRBS[4:0] bits in the DSMU_CHyCFG2 register.
- **Channel Offset:** Set the analog offset for each serial channel (connected external ΣΔ modulator) using the CALOFFSET[23:0] bits in the DSMU_CHyCFG2register.
- **Short-Circuit Detector and Clock Absence Monitoring:** Enable or disable the short-circuit detector (SCDETEN bit) and clock absence monitoring (CLKABEN bit) for each serial channel in the DSMU_CHyCFG1 register.
- **Analog Watchdog Filter and Short-Circuit Detector Threshold:** Configure the analog watchdog filter parameters and short-circuit detector parameters in the DSMU_CHyAWDSCDET register.

32.4.5 Parallel channel transceivers

Each input channel has a register for 16-bit parallel data input, in addition to serial data input. The 16-bit parallel input can only come from internal sources:

- Internal ADC results
- Direct CPU/DMA writing

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The selection between serial or parallel data input for a channel is made using the DATMUX[1:0] field in the DSMU_CHyCFG1 register. This field also defines the parallel data source: either internal ADC or direct CPU/DMA write.

Each channel has a 32-bit data input register (DSMU_CHyDATIN) where 16-bit data can be written. The data is in a 16-bit signed format and can be used as input to the digital filter, which accepts 16-bit parallel data.

If serial data input is selected (DATMUX[1:0] = 0), the DSMU_CHyDATIN register is write-protected.

32.4.5.1 Input from internal ADC

Thear are three internal ADCs, the channel connection is fixed:

ADC1 – channel 0, ADC2 – channel 1, ADC3 – channel 2.

ADC1 and ADC2 support interleaved mode. Both ADC1 and ADC2 data will come on the ADC1 data bus.

ADC1, ADC2, ADC3 supports triple mode, the data will come on ADC1 data bus only.

When using ADC data parallel input (DATMUX[1:0]=1), the result from ADC[y+1] is assigned to channel y. An end-of-conversion event from ADC[y+1] updates the data for channel y, sending the parallel data from ADC[y+1] as the next sample to the digital filter. This data is written into the DSMU_CHyDATIN register (INDATA0[15:0]) when the end-of-conversion event occurs.

The data packing mode setting (DATPACK[1:0] in the DSMU_CHyCFG1 register) does not affect ADC data input.

If the internal ADC is configured in interleaved mode (e.g., ADC1 with ADC2), each result from ADC1 or ADC2 will be sent to the same 16-bit bus, which connects to DSMU channel 0. This results in a double input data rate for DSMU channel 0, as samples from both ADC1 and ADC2 are indicated by their respective end-of-conversion events. Channel 1, associated with ADC2, will be free.

32.4.5.2 Input from memory(direct CPU/DMA write)

When using direct data write into the DSMU_CHyDATIN register by CPU or DMA (DATMUX[1:0]=2), you can process digital data streams from memory or peripherals. Data Writing Methods:

1. CPU data write:

   The CPU writes input data directly into the DSMU_CHyDATIN register

2. DMA data write:

   Configure the DMA in memory-to-memory transfer mode (no request needed) to transfer data from a memory buffer into the DSMU_CHyDATIN register. The destination address is the DSMU_CHyDATIN register.

   Data is transferred at DMA speed from memory to the DSMU parallel input.

   This DMA transfer is different from the DMA used to read DSMU conversion results. Both DMAs can operate simultaneously: one DMA (configured for memory-to-memory transfer) writes input data, while the other DMA (configured for peripheral-to-memory transfer) reads conversion results

Accesses to the DSMU_CHyDATIN register can be either 16-bit or 32-bit wide, allowing you to load one or two samples in a single write operation. The 32-bit input data register (DSMU_CHyDATIN) can hold one or two 16-bit data samples, depending on the data packing mode set by the DATPACK[1:0] field in the DSMU_CHyCFG1 rregister:

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1. Standard mode (DATPACK[1:0]=0):

Only one sample is stored in the INDATA0[15:0] field of the DSMU_CHyDATIN register, which is used as input data for channel y. The upper 16 bits (INDATA1[15:0]) are ignored and write-protected. The digital filter must perform one input sampling from INDATA0[15:0] to empty the data register after it has been filled by the CPU/DMA. This mode is used with 16-bit CPU/DMA access to the DSMU_CHyDATIN register to load one sample per write operation. The DSMU clock (dsmu_clk) needs to be at least twice as fast as the input write rate.

2. Interleaved mode (DATPACK[1:0]=1):

The DSMU_CHyDATIN register can act as a two-sample buffer. The first sample is stored in INDATA0[15:0], and the second sample is stored in INDATA1[15:0]. The digital filter must perform two input samplings from channel y to empty the DSMU_CHyDATIN register. This mode is used with 32-bit CPU/DMA access to the DSMU_CHyDATIN register to load two samples per write operation.

The DSMU clock (dsmu_clk) needs to be at least 4 times faster than the input write rate. When writing 32-bit data (INDATA1[15:0] & INDATA0[15:0]) in a single 32-bit write, the write rate must be halved compared to the standard mode because the hardware reads only 16 bits sequentially at a time.

3. Dual mode (DATPACK[1:0]=2):

Both samples (INDATA0[15:0] for channel y and INDATA1[15:0] for channel y+1) are written into the DSMU_CHyDATIN register. The data in INDATA1[15:0] is automatically copied to INDATA0[15:0] of the next channel's data register (DSMU_CH$_{[y+1]}$DATIN). The digital filters perform two samplings: one from channel y and one from channel y+1 to clear the DSMU_CHyDATIN registers. Dual mode (DATPACK[1:0]=2) is only for even channel numbers (e.g., 0, 2, 4, 6). If an odd channel (e.g., 1, 3, 5, 7) is set to Dual mode, both INDATA0[15:0] and INDATA1[15:0] are write-protected for that channel. If an even channel is set to Dual mode, the subsequent odd channel must be set to Standard mode (DATPACK[1:0]=0) to function correctly with the even channels.

Table 32-5 DSMU_CHyDATIN registers operation modes and assignment

Standard mode		Interleave mode		Dual mode		y
bit[31:16]	bit[15:0]	bit[31:16]	bit[15:0]	bit[31:16]	bit[15:0]	
Unused	CH0(sample 0)	CH0(sample 1)	CH0(sample 0)	CH1(sample 0)	CH0(sample 0)	0
Unused	CH1(sample 0)	CH1(sample 1)	CH1(sample 0)	Unused	CH1(sample 0)	1
Unused	CH2(sample 0)	CH2(sample 1)	CH2(sample 0)	CH3sample 0)	CH2(sample 0)	2
Unused	CH3(sample 0)	CH3(sample 1)	CH3(sample 0)	Unused	CH3(sample 0)	3
Unused	CH4(sample 0)	CH4(sample 1)	CH4(sample 0)	CH5(sample 0)	CH4(sample 0)	4
Unused	CH5(sample 0)	CH5(sample 1)	CH5(sample 0)	Unused	CH5(sample 0)	5
Unused	CH6(sample 0)	CH6(sample 1)	CH6(sample 0)	CH7(sample 0)	CH6(sample 0)	6
Unused	CH7(sample 0)	CH7(sample 1)	CH7(sample 0)	Unused	CH7(sample 0)	7

Writing one or two samples into the DSMU_CHyDATIN register must be done after enabling the selected input channel (channel y) for data collection (starting conversion for channel y). Otherwise, the written data will be lost.

For example, in single conversion and interleaved mode, do not begin writing pairs of data samples into DSMU_CHyDATIN before starting the single conversion. Any data present in DSMU_CHyDATIN before starting a conversion will be discarded.

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32.4.6 Channel selection

There are 8 channels available for conversion, which can be selected using either the injected channel or the regular channel.

Injected Channel:

User can select any or all of the 8 channels. The channels are chosen using the JCHG[7:0] register, where JCHG[y]=1 means channel y is selected. Injected conversions can run in:

Scan mode (JSCAN=1): Converts each selected channel one by one, starting from the lowest channel.

Single mode (JSCAN=0): Converts only one selected channel at a time. Writing to JCHG[7:0] resets the selection to the lowest channel.

These conversions can be started by software or a trigger and are not interrupted by regular conversions.

Regular Channel:

Only one of the 8 channels can be selected.

The selected channel is indicated by RCH[2:0] in the DSMU_FLTxCTRL1 register.

Regular conversions can only be started by software and are temporarily interrupted by injected conversions.

If a conversion is performed on a disabled channel (CHEN=0), it will never end because no input data is provided. To fix this, enable the channel (CHEN=1) or stop the conversion by setting DFLTEN=0 in the DSMU_FLTxCTRL1 register.

32.4.7 Digital filter configuration

The DSMU includes a Sincx digital filter that processes incoming digital data. This filtering reduces the output data rate (decimation) and enhances the output data resolution. The Sincx filter can be configured to achieve the desired output data rates and resolutions. The adjustable parameters are:

- Filter order/type: (FORD[2:0] bits in DSMU_FLTxFCTRL register):
  - FastSinc
  - $Sinc^1$
  - $Sinc^2$
  - $Sinc^3$
  - $Sinc^4$
  - $Sinc^5$
- Filter oversampling/decimation ratio (FOSR[9:0] bits in DSMU_FLTxFCTRL register):
  - FOSR = 1 to 1024: Applicable for the FastSinc filter and $Sinc^x$ filter with FORD values from 1 to 3
  - FOSR = 1 to 215: Applicable for the $Sinc^x$ filter with a FORD value of 4
  - FOSR = 1to 73: Applicable for the $Sinc^x$ filter with a FORD value of 5

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The filter's transfer function (impulse response in the H domain) is as follows:

Sincx filter type:

$$H(z)= [\frac{1-z^{-FOSR}}{1-Z^{-1}}]^{X}$$

FastSinc filter type:

$$H(z)= [\frac{1-z^{-FOSR}}{1-Z^{-1}}]^{2} * (1 + z^{-(2*FOSR)})$$

Figure 32-7 Sinc^3 filter response example

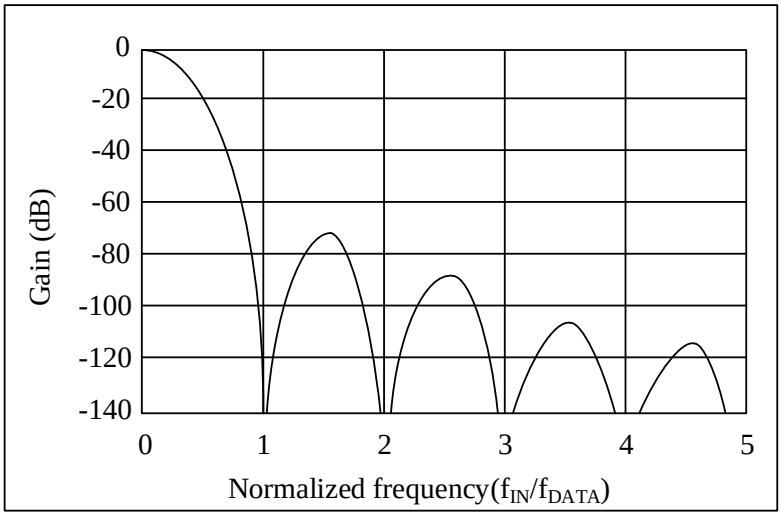

Table 32-6 Filter max resolution (output data values) for various FOSR

FOSR	Sinc^1	Sinc^2	FastSinc	Sinc^3	Sinc^4	Sinc^5
x	+/- x	+/- x^2	+/- 2x^2	+/- x^3	+/- x^4	+/- x^5
4	+/- 4	+/- 16	+/- 32	+/- 64	+/- 256	+/- 1024
8	+/- 8	+/- 64	+/- 128	+/- 512	+/- 4096	-
32	+/- 32	+/- 1024	+/- 2048	+/- 32768	+/- 1048576	+/- 33554432
64	+/- 64	+/- 4096	+/- 8192	+/- 262144	+/- 16777216	+/- 1073741824
128	+/- 128	+/- 16384	+/- 32768	+/- 2097152	+/- 268435456	
256	+/- 256	+/- 65536	+/- 131072	+/- 16777216	Result can overflow on full scale input	
1024	+/- 1024	+/- 1048576	+/- 2097152	+/-1073741824	(> 32-bit signed integer)	

32.4.8 Integrator unit

The integrator further decimates and increases the resolution of data from the digital filter by summing a specified number of data samples. The integrator oversampling ratio (IOSR) determines how many data samples are summed into one output. The IOSR can be set between 1 and 256, as described in the IOSR[7:0] bits of the DSMU_FLTxFCTRL register.

Table 32-7 Integrator max resolution (output data values) for various IOSR, FOSR = 256 with Sinc^3 filter

IOSR	Sinc^1	Sinc^2	FastSinc	Sinc^3	Sinc^4	Sinc^5

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x	+/-FOSR*x	+/-FOSR^2*x	+/-2FOSR^2*x	+/-FOSR^3*x	+/-FOSR^4*x	+/-FOSR^5*x
4	-	-	-	+/-67 108 864	-	-
32	-	-	-	+/-536 870 912	-	-
128	-	-	-	+/- 2 147 493 648	-	-
256	-	-	-	+/-2^{32}	-	-

32.4.9 Analog watchdog

The analog watchdog is used to trigger an external signal (break or interrupt) when an analog signal crosses specified maximum or minimum threshold values, initiating an interrupt event or break.

Each analog watchdog monitors serial data receiver outputs (post-filtering) or main filter data output registers (current injected or regular conversion results) based on the AWDFSEL bit setting in the DSMU_FLTxCTRL1 register. The channels to be monitored are selected using the AWDCH[7:0] bits in the DSMU_FLTxCTRL2 register.

Analog watchdog conversions operate independently from main conversions, using their own filters and signal processing for each input serial channel. These conversions run continuously on selected input channels, even when main injected or regular conversions are paused (RCIP = 0, JCIP = 0 in the DSMU_FLTxSTS register).

High and low threshold registers (AWDHT[23:0] and AWDLT[23:0] in the DSMU_FLTxAWDHT and DSMU_FLTxAWDLT registers, respectively) are used to compare against given data values.

Two options for comparing threshold and data:

- Option 1: Input data from the final output data register (AWDFSEL=0):
  - Up to 24-bits high input data resolution
  - Slow response time and not suitable for fast-response applications like overcurrent detection
  - The final data for comparison are used after bit shifting and offset data correction
  - Final data available after main regular or injected conversions
  - Suitable for parallel input data sources (DATMUX[1:0] ≠ 0 in the DSMU_CHyCFG1 register).

- Option 2: Input data from any serial data receiver's output (AWDFSEL=1):
  - Input serial data processed by dedicated analog watchdog Sincx filters with oversampling ratio (1 to 32) and filter order (1 to 3), (AWDFOSR[4:0] and AWDFORD[1:0] in the DSMU_CHyAWDSCDET register)
  - Up to 16-bits lower resolution
  - Fast response time and suitable for applications such as overcurrent or overvoltage detection.
  - Data are available in continuously and independently from main regular or injected conversions activity

When monitoring input channels (AWDFSEL=1), the data for threshold comparison is taken from channels selected by the AWDCH[7:0] field in the DSMU_FLTxCTRL2 register. Each selected channel's filter result is compared to a

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threshold value pair (AWDHT[23:0] / AWDLT[23:0]). In this scenario, only the higher 16 bits (AWDHT[23:8] / AWDLT[23:8]) are used to define the 16-bit threshold compared with the analog watchdog filter output, as the data from the analog watchdog filter has up to a 16-bit resolution. The lower 8 bits (AWDHT[7:0] / AWDLT[7:0]) are not used in the comparison.

The parameters for configuring the analog watchdog filter for each input channel are set in the DSMU_CHyAWDSCDET register. These parameters include the filter order (AWDFORD[1:0]) and the filter oversampling ratio (AWDFOSR[4:0]).

Each input channel has its own comparator which compares the analog watchdog data (from analog watchdog filter) with analog watchdog threshold values (AWDHT/AWDLT). When several channels are selected (field AWDCH[7:0] field of DSMU_FLTxCTRL2 register), several comparison requests may be received simultaneously. In this case, the channel request with the lowest number is managed first and then continuing to higher selected channels. For each channel, the result can be recorded in a separate flag (fields AWDHTF[7:0], AWDLTF[7:0] of DSMU_FLTxAWDSTS register). Each channel request is executed in 8 DSMU clock cycles. So, the bandwidth from each channel is limited to 8 DSMU clock cycles (if AWDCH[7:0] = 0xFF). Because the maximum input channel sampling clock frequency is the DSMU clock frequency divided by 4, the configuration AWDFOSR = 0 (analog watchdog filter is bypassed) cannot be used for analog watchdog feature at this input clock speed. Therefore user must properly configure the number of watched channels and analog watchdog filter parameters with respect to input sampling clock speed and DSMU frequency.

Each input channel has its own comparator that compares the analog watchdog data (from the analog watchdog filter) with the threshold values (AWDHT/AWDLT). When multiple channels are selected (using the AWDCH[7:0] field in the DSMU_FLTxCTRL2 register), several comparison requests may occur simultaneously. In such cases, the channel with the lowest number is processed first, followed by higher-numbered channels. The result for each channel can be recorded in separate flags (AWDHTF[7:0] and AWDLTF[7:0] in the DSMU_FLTxAWDSTS register).

Each channel request is executed in 8 DSMU clock cycles, limiting the bandwidth for each channel to 8 DSMU clock cycles (if AWDCH[7:0] = 0xFF). Since the maximum input channel sampling clock frequency is the DSMU clock frequency divided by 4, the configuration AWDFOSR = 0 (bypassing the analog watchdog filter) cannot be used at this input clock speed. Therefore, users must properly configure the number of monitored channels and the analog watchdog filter parameters according to the input sampling clock speed and DSMU frequency.

The analog watchdog filter data for a given channel y can be read by software from the AWDDAT[15:0] field in the DSMU_CHyAWDDAT register. This data is continuously converted (if CHEN=1 in the DSMU_CHyCFG1 register) at a rate determined by the analog watchdog filter settings and the channel input clock frequency.

The analog watchdog filter conversion operates similarly to a regular Fast Continuous Conversion but without the integrator. The number of serial samples required for one result from the analog watchdog filter output (at the channel input clock frequency fCKIN) is determined by the filter settings.

First conversion:

For Sincx filters (x=1 to 5): Number of samples = [FOSR * FORD + 2]

For FastSinc filter: Number of samples = [FOSR * 4 + 2]

Subsequent conversions:

For Sincx and FastSinc filters: Number of samples = [FOSR * IOSR]

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Where:

FOSR: Filter oversampling ratio: FOSR = AWDFOSR[4:0]+1 (refer DSMU_CHyAWDSCDET register)

FORD: Filter order: FORD = AWDFORD[1:0] (refer DSMU_CHyAWDSCDET register)

When monitoring the output data register (AWDFSEL=0), the comparison is performed after applying a right bit shift and an offset correction to the final data (refer to the CALOFFSET[23:0] and DATRBS[4:0] fields in the DSMU_CHyCFG2 register). This comparison occurs after each injected or regular end of conversion for the channels selected by the AWDCH[7:0] field in the DSMU_FLTxCTRL2 register.

The status of an analog watchdog event is indicated in the DSMU_FLTxAWDSTS register, where the event is latched. The AWDHTF[y]=1 flag indicates that the AWDHT[23:0] value was crossed on channel y. The AWDLTF[y]=1 flag indicates that the AWDLT[23:0] value was crossed on channel y. Latched events in the DSMU_FLTxAWDSTS register are cleared by writing '1' to the corresponding clearing bit (CLRAWDHTF[y] or CLRAWDLTF[y]) in the DSMU_FLTxAWDCLR register.

The global status of an analog watchdog is indicated by the AWDF flag bit in the DSMU_FLTxSTS register, which is used for quickly detecting an interrupt source. AWDF=1 indicates that at least one watchdog event occurred (AWDHTF[y]=1 or AWDLTF[y]=1 for at least one channel). The AWDF bit is cleared when all AWDHTF[7:0] and AWDLTF[7:0] flags are cleared.

An analog watchdog event can be assigned to a break output signal. There are four break outputs (dsmu_break[3:0]) that can be linked to a high or low threshold crossing event. The assignment of the break signal to a specific analog watchdog event is done using the BKAWDHT[3:0] and BKAWDLT[3:0] fields in the DSMU_FLTxAWDHT and DSMU_FLTxAWDLT registers.

Limitation of AWD is that the CPU must read the AWDDAT faster than the hardware updates it to avoid missing data, as there is no trigger flag, CPU read AWDDAT for debugging purposes only.

32.4.10 Short-circuit detector

The short-circuit detector quickly signals if an analog signal reaches and stays at saturated values (out of full-scale ranges), which can indicate short-circuit or open-circuit errors (e.g., overcurrent or overvoltage). This can trigger an interrupt, event, or break.

Input data comes from channel transceiver outputs. Each input channel has a counter that counts consecutive 0's or 1's on serial data receiver outputs. The counter resets if the data stream changes from 1 to 0 or 0 to 1.

If the counter reaches the short-circuit threshold (SCDETTH[7:0] in the DSMU_CHyAWDSCDET register), a short-circuit event is triggered. Each input channel has its own short-circuit detector.

Channels can be continuously monitored by setting the SCDETEN bit in the DSMU_CHyCFG1 register.

Each channel has its own settings for the short-circuit detector (threshold value in SCDETTH[7:0], status bit SCDETF[7:0], and status clearing bits CLRSCDETF[7:0]). The status flag SCDETF[y] is also cleared by hardware when the corresponding channel y is disabled (CHEN[y] = 0).

A short-circuit detector event on each channel can be assigned to one of four break output signals (dsmu_break[3:0]). The assignment is done using the BKSCDET[3:0] field in the DSMU_CHyAWDSCDET register.

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The short-circuit detector cannot be used if parallel input data channel selection is enabled (DATMUX[1:0] ≠ 0 in the DSMU_CHyCFG1 register). There are a total of four break outputs available, which are shared with the analog watchdog function.

32.4.11 Extreme detector

The extremes detector collects the minimum and maximum values of final output data words (peak-to-peak values).

If the output data word is higher than the current maximum value in the extremes detector (EXDETMAX[23:0] in DSMU_FLTxEXDETMAX register), the register is updated with the new value, and the channel is recorded in EXDETMAXCH[2:0].

If the output data word is lower than the current minimum value in the extremes detector (EXDETMIN[23:0] in DSMU_DFxEXDETMIN register), the register is updated with the new value, and the channel is recorded in EXDETMINCH[2:0].

The minimum and maximum register values can be refreshed by reading the DSMU_FLTxEXDETMAX or DSMU_DFxEXDETMIN registers.

After refreshing, the minimum register (DSMU_DFxEXDETMIN) is set to 0x7FFFFF (maximum positive value), and the maximum register (DSMU_FLTxEXDETMAX) is set to 0x800000 (minimum negative value).

The extremes detector performs comparisons after the right bit shift and offset data correction.

The input channels to be considered for computing the extremes value are selected using the EXDETCH[7:0] bits in the DSMU_FLTxCTRL2 register.

32.4.12 Data unit block

The data unit block is the final stage in the processing path: External ΣΔ modulators → Serial transceivers → Sinc filter → Integrator → Data unit block.

The output data rate depends on the serial data stream rate, as well as the filter and integrator settings. The maximum output data rate for (IOSR > 0) is:

Datarate[samples/s] = f_{DATAIN_RATE}/(FOSR * (IOSR + FORD) +1) , for FAST = 0, $Sinc^x$ filters FORD = 1 to 5

or

Datarate[samples/s] = f_{DATAIN_RATE}/(FOSR * (IOSR + 4) +1) , for FAST = 0, FastSinc filters FORD = 0

or

Datarate[samples/s] = f_{DATAIN_RATE}/(FOSR * IOSR), for FAST = 1

where f_{DATAIN_RATE} is the input data rate from external ΣΔ modulators, ADC or from CPU/DMA.

The maximum output data rate for (IOSR = 0) is:

Datarate[samples/s] = f_{DATAIN_RATE}/(FOSR * FORD +1) , for FAST = 0, $Sinc^x$ filters FORD = 1 to 5

Datarate[samples/s] = f_{DATAIN_RATE}/(FOSR * 4 +1) , for FAST = 0, FastSinc filters FORD = 0

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The final data is right bit-shifted in this module because the final data width is 24 bits, while the data from the processing path can be up to 32 bits. This right bit-shift can be configured from 0 to 31 bits for each selected input channel (see DATRBS[4:0] bits in the DSMU_CHyCFG2 register). The right bit-shift rounds the result to the nearest integer and maintains the sign to ensure a valid 24-bit signed format.

Next, an offset correction is applied. The offset correction value (CALOFFSET[23:0] in the DSMU_CHyCFG2 register) is subtracted from the output data for each channel. This value is set by software through a calibration routine.

Since all digital processing operations are performed on 32-bit signed registers, the following conditions must be met to avoid overflow:

- For $Sinc^x$ filters (x = 1 to 5): $FOSR^{FORD} * IOSR <= 2^{31}$
- For FastSinc filter: $2*FOSR^2 * IOSR <= 2^{31}$

The input data rate (f_{DATAIN_RATE}) must be limited to ensure all output data can be read: $f_{DATAIN_RATE} \leq f_{PCLK2}$ if both the integrator and filter are bypassed (IOSR[7:0]=0 and FOSR[9:0]=0).

32.4.13 Signed data format

Data is stored in a signed format in registers for final output data, analog watchdog, extremes detector, and offset correction. The most significant bit (MSB) of the output data word indicates the sign of the value (two's complement format).

Each DSMU input serial channel can connect to one external ΣΔ modulator. This modulator has two differential inputs (positive and negative) for measuring differential or single-ended signals. The output from the ΣΔ modulator is always in a signed format, where a stream of zeros and ones represents values of -1 and +1.

32.4.14 Launching conversions

32.4.14.1 Injected conversion

Injected conversions can be started using the following methods:

1. Software: By writing '1' to JSWSTART in the DSMU_FLTxCTRL1 register.
2. Trigger: JEXTSEL[4:0] selects the trigger signal, and JEXTEN activates the trigger and selects the active edge (see DSMU_FLTxCTRL1 register).
3. Synchronous with DSMU_FLT0 if JSYNC=1: For DSMU_DFx (x>0), an injected conversion starts automatically when initiated by software in DSMU_FLT0 (JSWSTART=1 in DSMU_FLTxCTRL2 register). Each injected conversion in DSMU_FLTx (x>0) follows its local settings (JSCAN, JCHG, etc.).

Scan Conversion Enabled (JSCAN=1): Each time an injected conversion is triggered, all selected channels in the injected group (JCHG[7:0] in DSMU_FLTxJCHG register) are converted sequentially, starting with the lowest channel (channel 0, if selected).

Scan Conversion Disabled (JSCAN=0): Each time an injected conversion is triggered, only one selected channel in the injected group is converted, then the selection moves to the next channel. Writing to JCHG[7:0] when JSCAN=0 resets the selection to the lowest selected channel.

Only one injected conversion can occur at a time. Any new request for an injected conversion is ignored if another is

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already in progress.

32.4.14.2 Regular conversion

Regular conversions can be started using the following methods:

1. Software: Write '1' to the RSWSTART field in the DSMU_FLTxCTRL1 register.
2. Synchronous with DSMU_DF0: If RSYNC=1, for DSMU_FLTx (where x > 0), a regular conversion starts automatically when DSMU_FLT0 begins. For DSMU_FLT0, start a regular conversion by writing '1' to RSWSTART in the DSMU_FLTxCTRL2 register. Each regular conversion in DSMU_FLTx (x > 0) follows its local settings (like RCONT, RCH, etc.).

At any moment, only one regular conversion can be either pending or in progress. If a new request for a regular conversion comes in while another one is still pending or ongoing, the new request will be ignored.

A regular conversion can be delayed if interrupted by an injected conversion or if it starts while an injected conversion is in progress. The pending conversion will resume after all injected conversions are finished. This is indicated by the RPEND bit in the DSMU_FLTxRDAT register.

If a regular conversion is ongoing and an injected conversion starts, the regular conversion will be discarded. After the injected conversion ends, the regular conversion will restart with fresh input data.

32.4.15 Continuous and fast modes

Continuous Mode for Regular Conversions in DSMU enabled by Set RCONT to 1 in the DSMU_FLTxCTRL1 register. The channel selected by RCH[2:0] will be converted repeatedly after writing '1' to RSWSTART. Stopping Continuous Mode by write '0' to RCONT to stop continuous conversions immediately.

Increasing Data Rate with fast mode is by setting the FAST bit in the DSMU_FLTxCTRL1 register. This allows the filter to use previously sampled data without needing new data for each conversion, speeding up the process. The speed increase depends on the filter order. The first conversion in fast mode takes the same time as normal mode, but subsequent conversions are faster.

If a continuous conversion is in progress (RCONT=1) and you write to the DSMU_FLTxCTRL1 register to request another continuous conversion, it will restart from the next cycle. This applies even if there is no change in the register settings.

For a quick restart by writing RCONT=1 when RCONT=1, it will only take effect if you are not writing to RSWSTART or JSWSTART at the same time. Resetting RCONT will not take effect if DFLTEN is set to 0.

Continuous mode is not available for injected conversions. Injected conversions can be started by a timer trigger to mimic continuous mode with precise timing.

32.4.16 Request precedence

Injected conversions have higher priority than regular conversions. If a regular conversion is in progress and an injected conversion is requested, the regular conversion is immediately interrupted and will restart after the injected conversion finishes.

An injected conversion cannot start if another injected conversion is already pending or in progress. Any new request

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will be ignored if the JCIP bit in the DSMU_FLTxSTS register is '1'.

Similarly, a regular conversion cannot start if another regular conversion is pending or in progress. Any new request will be ignored if the RCIP bit in the DSMU_FLTxSTS register is '1'.

If an injected conversion is requested while a regular conversion is in progress, the regular conversion is stopped and the injected conversion starts. The regular conversion will restart after the injected conversion finishes, indicated by the RPEND bit.

Injected conversions can interrupt a sequence of continuous regular conversions. Once the injected conversions finish, the continuous regular conversions will resume if RCONT is still set. The delayed restart of the regular conversion will be indicated by the RPEND bit.

Precedence also applies when multiple actions are initiated simultaneously or are pending. For example, if an injected conversion is in progress (JCIP=1) and a regular conversion is requested (RSWSTART=1), the regular conversion will start after the injected conversion finishes, with the delayed start indicated by the RPEND bit.

For quick restarts, writing RCONT=1 when RCONT=1 will only take effect if RSWSTART or JSWSTART are not written at the same time.

Resetting RCONT will not take effect if DFLTEN is set to 0.

32.4.17 DSMU interrupts

To boost CPU performance, a series of interrupts have been implemented to handle specific CPU events.

- End of injected conversion interrupt:
  - Enabled by setting JEOCIEN bit in DSMU_FLTxCTRL2 register.
  - The interrupt is indicated by JEOCF bit in DSMU_FLTxSTS register.
  - Read the DSMU_FLTxJDAT register (which contain injected data) to clear the interrupt.
  - The specific channel where the end of conversion occurred is indicated by the JDATCH[2:0] bits in the DSMU_FLTxJDAT register.
- End of regular conversion interrupt:
  - Enabled by setting REOCIEN bit in the DSMU_FLTxCTRL2 register.
  - The interrupt is indicated by the REOCF bit in the DSMU_FLTxSTS register.
  - Read the DSMU_FLTxRDAT register (which contains the regular data) to clear the interrupt.
  - The specific channel where the end of conversion occurred is indicated by the RDATCH[2:0] bits in the DSMU_FLTxRDAT register.
- Data overrun interrupt for injected conversions:
  - This interrupt happens when the injected converted data in the DSMU_FLTxJDAT register is not read by the CPU or DMA and gets overwritten by new injected conversion data
  - Enabled by setting JOVRIEN bit in DSMU_FLTxCTRL2 register
  - The interrupt is indicated by the JOVRF bit in the DSMU_FLTxSTS register.

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- Write '1' to the CLRJOVRF bit in the DSMU_FLTxINTCLR register to clear the interrupt.

- Data overrun interrupt for regular conversions:
  - This interrupt happens when the regular converted data in the DSMU_FLTxRDAT register is not read by the CPU or DMA and gets overwritten by new regular conversion data.
  - Enabled by setting ROVRIEN bit in DSMU_FLTxCTRL2 register.
  - The interrupt is indicated by the ROVRF bit in the DSMU_FLTxSTS register.
  - Write '1' to the CLRROVRF bit in the DSMU_FLTxINTCLR register to clear the interrupt.
- Analog watchdog interrupt:
  - This interrupt happens when the converted data (either output data or data from the analog watchdog filter, based on the AWDFSEL bit setting in the DSMU_FLTxCTRL1 register) crosses the high or low thresholds set in the DSMU_FLTxAWDHT or DSMU_FLTxAWDLT registers
  - Enabled by setting AWDIEN bit in DSMU_FLTxCTRL2 register (on selected channels AWDCH[7:0])
  - The interrupt is indicated by the AWDF bit in the DSMU_FLTxSTS register.
  - Separate indications for high or low analog watchdog threshold errors are provided by the AWDHTF[7:0] and AWTHLF[7:0] fields in the DSMU_FLTxAWDSTS register.
  - Write '1' to the corresponding CLRAWDHTF[7:0] / CLRAWDHLF[7:0] bits in the DSMU_FLTxAWDCLR register to clear the interrupt.
- Short-circuit detector interrupt:
  - This interrupt happens when the number of stable data points crosses the thresholds set in the DSMU_CHyAWDSCDET register.
  - Enabled by setting SCDETIEN bit in DSMU_FLTxCTRL2 register (Ensure the channel is selected by setting the SCDETEN bit in the DSMU_CHyCFG1)
  - The interrupt is indicated by the SCDETF[7:0] bits in the DSMU_FLTxSTS register, which also shows the channel where the short-circuit detector event occurred
  - Write '1' to the corresponding CLRSCDETF[7:0] bit in the DSMU_FLTxINTCLR register to clear the interrupt
- Channel clock absence interrupt:
  - This interrupt happens when there is no clock signal on the CKINy pin (refer to Clock Absence Detection in Section 35.4.4: Serial Channel Transceivers).
  - Enabled by setting CLKABIEN bit in the DSMU_FLTxCTRL2 register for channels selected by the CLKABEN bit in the DSMU_CHyCFG1 register
  - The interrupt is indicated by the CLKABF[y] bit in the DSMU_FLTxSTS register
  - Write '1' to the CLRCLKABF[y] bit in the DSMU_FLTxINTCLR register to clear the interrupt.

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Table 32-8 DSMU interrupt requests

Interrupt event	Event flag	Event/Interrupt clearing method	Interrupt enable control bit
End of injected conversion	JEOCF	reading DSMU_FLTxJDAT	JEOCIEN
End of regular conversion	REOCF	reading DSMU_FLTxRDAT	REOCIEN
Injected data overrun	JOVRF	writing CLRJOVRF= 1	JOVRIEN
Regular data overrun	ROVRF	writing CLRROVRF= 1	ROVRIEN
Analog watchdog	AWDF, AWDHTF[7:0], AWTHLF[7:0]	writing CLRAWDHTF[7:0] = 1 writing CLRAWDHLF[7:0] = 1	AWDIEN(AWDCH[7:0])
Short-circuit detector	SCDETF[7:0]	writing CLRSCDETF[7:0] = 1	SCDETIEN(SCDETEN)
Channel clock absence	CLKABF[7:0]	writing CLRCLKABF[7:0] = 1	CLKABIEN(CLKABEN)

32.4.18 DSMU DMA transfer

To reduce the CPU load, enabling the DMA Transfers:

For injected conversions: Set JDMAEN=1 in the DSMU_FLTxCTRL1 register.

For regular conversions: Set RDMAEN=1 in the DSMU_FLTxCTRL1 register.

The destination address is the JDATA address. Inside the DSMU, a read data multiplexer (mux) handle this.

The DMA request is automatically cleared when the DMA reads the data register, so there’s no need for the DMA to send an acknowledgment signal.

When using DMA transfers, the interrupt flag is automatically cleared at the end of the conversion (either JEOCF for injected or REOCF for regular) because the DMA reads the DSMU_FLTxJDAT or DSMU_FLTxRDAT register.

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32.5 DSMU registers

32.5.1 DSMU register map

Table 32-9 DSMU register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	DSMU_CH0CFG1	DSMUEN	CLKOUTSRC	Reserved						CLKOUTDIV[7:0]								DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value	0	0							0	0	0	0	0	0	0	0	0	0	0	0				0	0	0	0	0	0	0	0	0
0x04	DSMU_CH0CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0x08	DSMU_CH0 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0x0C	DSMU_CH0 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	DSMU_CH0 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	DSMU_CH1CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value																	0	0	0	0				0	0	0	0	0	0	0	0	0
0x24	DSMU_CH1CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0x28	DSMU_CH1 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0x2C	DSMU_CH1 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	DSMU_CH1 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	DSMU_CH2CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value																	0	0	0	0				0	0	0	0	0	0	0	0	0
0x44	DSMU_CH2CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0x48	DSMU_CH2 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0x4C	DSMU_CH2 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	DSMU_CH2 DATIN	INDAT1[15:0]																INDAT0[15:0]															

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x60	DSMU_CH3CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value																	0	0	0	0				0	0	0	0	0	0	0	0	0
0x64	DSMU_CH3CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0x68	DSMU_CH3 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0x6C	DSMU_CH3 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x70	DSMU_CH3 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x80	DSMU_CH4CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value																	0	0	0	0				0	0	0	0	0	0	0	0	0
0x84	DSMU_CH4CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0x88	DSMU_CH4 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0x8C	DSMU_CH4 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x90	DSMU_CH4 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA0	DSMU_CH5CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value																	0	0	0	0				0	0	0	0	0	0	0	0	0
0xA4	DSMU_CH5CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0xA8	DSMU_CH5 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0xAC	DSMU_CH5 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB0	DSMU_CH5 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xC0	DSMU_CH6CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
	Reset Value																	0	0	0	0				0	0	0	0	0	0	0	0	0
0xC4	DSMU_CH6CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		

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	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0xC8	DSMU_CH6 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0xCC	DSMU_CH6 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD0	DSMU_CH6 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xE0	DSMU_CH7CFG1	Reserved																DATPACK[1:0]		DATMUX[1:0]		Reserved		CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]		
	Reset Value																	0	0	0	0			0	0	0	0	0	0	0	0	0	0
0xE4	DSMU_CH7CFG2	CALOFFSET[23:0]																								DATRBS[4:0]					Reserved		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0xE8	DSMU_CH7 AWDSCDET	Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]					BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
	Reset Value									0	0		0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0xEC	DSMU_CH7 AWDDAT	Reserved																AWDDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xF0	DSMU_CH7 DATIN	INDAT1[15:0]																INDAT0[15:0]															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x100	DSMU_FLT0 CTRL1	Reserved	AWDFSEL	FAST	Reserved		RCH[2:0]			Reserved		RDMAEN	Reserved	RSYNC	RCONT	RSWSTART	Reserved		JEXTEN[1:0]			JEXTSEL[4:0]				Reserved		JDMAEN	JSCAN	JSYNC	Reserved	JSWSTART	DFLTEN
	Reset Value		0	0		0	0	0				0		0	0	0		0	0	0	0	0	0	0	0			0	0	0		0	0
0x104	DSMU_FLT0 CTRL2	Reserved								AWDCH[7:0]								EXDETCH[7:0]								Reserved	CLKABIEN	SCDETIEN	AWDIEN	ROVRIEN	JOVRIEN	REOCIEN	JEOCIEN
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
0x108	DSMU_FLT0STS	SCDETF[7:0]								CLKABF[7:0]								Reserved	RCIP	JCIP	Reserved								AWDF	ROVRF	JOVRF	REOCF	JEOCF
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0									0	0	0	0	0
0x10C	DSMU_FLT0 INTCLR	CLRSCDETF[7:0]								CLRCLKABF[7:0]								Reserved												CLRROVRF	CLRJOVRF	Reserved	
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0													0	0		
0x110	DSMU_FLT0 JCHG	Reserved																								JCHG[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
0x114	DSMU_FLT0 FCTRL	FORD[2:0]			Reserved					FOSR[9:0]								Reserved								IOSR[7:0]							
	Reset Value	0	0	0			0	0	0	0	0	0	0	0	0	0	0									0	0	0	0	0	0	0	0
0x118	DSMU_FLT0 JDAT	JDAT[23:0]																								Reserved					JDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x11C	DSMU_FLT0 RDAT	RDAT[23:0]																								Reserved		RPEND	Reserved		RDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0			0	0	0
0x120	DSMU_FLT0 AWDHT	AWDHT[23:0]																								Reserved					BKAWDHT[3:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x124	DSMU_FLT0 AWDLT	AWDLT[23:0]																								Reserved					BKAWDLT[3:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0

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0x128	DSMU_FLT0 AWDSTS	Reserved																AWDHTF[7:0]								AWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x12C	DSMU_FLT0 AWDCLR	Reserved																CLRAWDHTF[7:0]								CLRAWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x130	DSMU_FLT0 EXDETMAX	EXDETMAX[23:0]																								Reserved					EXDET MAXCH[2:0]		
	Reset Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x134	DSMU_FLT0 EXDETMIN	EXDETMIN[23:0]																								Reserved					EXDET MINCH[2:0]		
	Reset Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						0	0	0
0x138	DSMU_FLT0 COVTIM	COVCNT[27:0]																												Reserved			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
0x180	DSMU_FLT1 CTRL1	Reserved	AWDFSEL	FAST	Reserved		RCH[2:0]			Reserved		RDMAEN	Reserved	RSYNC	RCONT	RSWSTART	Reserved	JEXTEN[1:0]		JEXTSEL[4:0]					Reserved		JDMAEN	JSCAN	JSYNC	Reserved	JSWSTART	DFLTEN	
	Reset Value		0	0			0	0	0			0		0	0	0		0	0	0	0	0	0	0	0			0	0	0		0	0
0x184	DSMU_FLT1 CTRL2	Reserved								AWDCH[7:0]								EXDETCH[7:0]								Reserved		AWDIEN	ROVRIEN	JOVRIEN	REOCIEN	JEOCIEN	
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0
0x188	DSMU_FLT1STS	Reserved																	RCIP	JCIP	Reserved							AWDF	ROVRF	JOVRF	REOCF	JEOCF	
	Reset Value																		0	0								0	0	0	0	0	0
0x18C	DSMU_FLT1 INTCLR	Reserved																												CLRROVRF	CLRJOVRF	Reserved	
	Reset Value																													0	0		
0x190	DSMU_FLT1 JCHG	Reserved																								JCHG[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
0x194	DSMU_FLT1 FCTRL	FORD[2:0]			Reserved				FOSR[9:0]									Reserved								IOSR[7:0]							
	Reset Value	0	0	0			0	0	0	0	0	0	0	0	0	0	0									0	0	0	0	0	0	0	0
0x198	DSMU_FLT1 JDAT	JDAT[23:0]																								Reserved					JDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x19C	DSMU_FLT1 RDAT	RDAT[23:0]																								Reserved			RPEND	Reserved	RDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				0		0	0	0
0x1A0	DSMU_FLT1 AWDHT	AWDHT[23:0]																								Reserved					BKAWDHT[3:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x1A4	DSMU_FLT1 AWDLT	AWDLT[23:0]																								Reserved					BKAWDLT[3:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x1A8	DSMU_FLT1 AWDSTS	Reserved																AWDHTF[7:0]								AWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1AC	DSMU_FLT1 AWDCLR	Reserved																CLRAWDHTF[7:0]								CLRAWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1B0	DSMU_FLT1 EXDETMAX	EXDETMAX[23:0]																								Reserved					EXDET MAXCH[2:0]		
	Reset Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x1B4	DSMU_FLT1 EXDETMIN	EXDETMIN[23:0]																								Reserved					EXDET MINCH[2:0]		
	Reset Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						0	0	0
0x1B8	DSMU_FLT1 COVTIM	COVCNT[27:0]																												Reserved			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
0x200	DSMU_FLT2 CTRL1	Reserved	AWDFSEL	FAST	Reserved		RCH[2:0]			Reserved		RDMAEN	Reserved	RSYNC	RCONT	RSWSTART	Reserved	JEXTEN[1:0]		JEXTSEL[4:0]					Reserved		JDMAEN	JSCAN	JSYNC	Reserved	JSWSTART	DFLTEN	
	Reset Value		0	0			0	0	0			0		0	0	0		0	0	0	0	0	0	0	0			0	0	0		0	0

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0x204	DSMU_FLT2 CTRL2	Reserved								AWDCH[7:0]								EXDETCH[7:0]								Reserved			AWDIEN	ROVRIEN	JOVRIEN	REOCIEN	JEOCIEN
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				0	0	0	0	0
0x208	DSMU_FLT2STS	Reserved																	RCIP	JCIP	Reserved								AWDF	ROVRF	JOVRF	REOCF	JEOCF
	Reset Value																		0	0									0	0	0	0	0
0x20C	DSMU_FLT2 INTCLR	Reserved																												CLRROVRF	CLRJOVRF	Reserved	
	Reset Value																													0	0		
0x210	DSMU_FLT2 JCHG	Reserved																								JCHG[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
0x214	DSMU_FLT2 FCTRL	FORD[2:0]			Reserved			FOSR[9:0]										Reserved								IOSR[7:0]							
	Reset Value	0	0	0				0	0	0	0	0	0	0	0	0	0									0	0	0	0	0	0	0	0
0x218	DSMU_FLT2 JDAT	JDAT[23:0]																								Reserved					JDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x21C	DSMU_FLT2 RDAT	RDAT[23:0]																								Reserved			RPEND	Reserved	RDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				0		0	0	0
0x220	DSMU_FLT2 AWDHT	AWDHT[23:0]																								Reserved					BKAWDHT[3:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x224	DSMU_FLT2 AWDLT	AWDLT[23:0]																								Reserved					BKAWDLT[3:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x228	DSMU_FLT2 AWDSTS	Reserved																AWDHTF[7:0]								AWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x22C	DSMU_FLT2 AWDCLR	Reserved																CLRAWDHTF[7:0]								CLRAWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x230	DSMU_FLT2 EXDETMAX	EXDETMAX[23:0]																								Reserved					EXDET MAXCH[2:0]		
	Reset Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x234	DSMU_FLT2 EXDETMIN	EXDETMIN[23:0]																								Reserved					EXDET MINCH[2:0]		
	Reset Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						0	0	0
0x238	DSMU_FLT2 COVTIM	COVCNT[27:0]																												Reserved			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
0x280	DSMU_FLT3 CTRL1	Reserved	AWDFSEL	FAST	Reserved			RCH[2:0]		Reserved		RDMAEN	Reserved	RSYNC	RCONT	RSWSTART	Reserved	JEXTEN[1:0]		JEXTSEL[4:0]						Reserved		JDMAEN	JSCAN	JSYNC	Reserved	JSWSTART	DFLTEN
	Reset Value		0	0			0	0	0			0		0	0	0		0	0	0	0	0	0	0	0			0	0	0		0	0
0x284	DSMU_FLT3 CTRL2	Reserved								AWDCH[7:0]								EXDETCH[7:0]								Reserved			AWDIEN	ROVRIEN	JOVRIEN	REOCIEN	JEOCIEN
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				0	0	0	0	0
0x288	DSMU_FLT3STS	Reserved																	RCIP	JCIP	Reserved								AWDF	ROVRF	JOVRF	REOCF	JEOCF
	Reset Value																		0	0									0	0	0	0	0
0x28C	DSMU_FLT3 INTCLR	Reserved																												CLRROVRF	CLRJOVRF	Reserved	
	Reset Value																													0	0		
0x290	DSMU_FLT3 JCHG	Reserved																								JCHG[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
0x294	DSMU_FLT3 FCTRL	FORD[2:0]			Reserved			FOSR[9:0]										Reserved								IOSR[7:0]							
	Reset Value	0	0	0				0	0	0	0	0	0	0	0	0	0									0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x298	DSMU_FLT3 JDAT	JDAT[23:0]																								Reserved					JDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x29C	DSMU_FLT3 RDAT	RDAT[23:0]																								Reserved			RPEND	Reserved	RDATCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				0		0	0	0
0x2A0	DSMU_FLT3 AWDHT	AWDHT[23:0]																								Reserved				BKAWDHT[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0
0x2A4	DSMU_FLT3 AWDLT	AWDLT[23:0]																								Reserved				BKAWDLT[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0
0x2A8	DSMU_FLT3 AWDSTS	Reserved																AWDHTF[7:0]								AWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2AC	DSMU_FLT3 AWDCLR	Reserved																CLRAWDHTF[7:0]								CLRAWDLTF[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2B0	DSMU_FLT3 EXDETMAX	EXDETMAX[23:0]																								Reserved					EXDET MAXCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x2B4	DSMU_FLT3 EXDETMIN	EXDETMIN[23:0]																								Reserved					EXDET MINCH[2:0]		
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0
0x2B8	DSMU_FLT3 COVTIM	COVCNT[27:0]																												Reserved			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

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32.5.2 DSMU channel y configure register1 (DSMU_CHyCFG1)

Offset error：0x00 + 0x20 * y (y = 0 to 7)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSMUEN	CLKOUTSRC	Reserved						CLKOUTDIV[7:0]							
rw	rw							rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATPACK[1:0]		DATMUX[1:0]		Reserved			CHINSEL	CHEN	CLKABEN	SCDETEN	Reserved	SPICLKSEL[1:0]		SITP[1:0]	
rw		rw					rw	rw	rw	rw		rw		rw	

Bit field	Name	Description
31	DSMUEN	DSMU interface global enable 0: DSMU interface disabled 1: DSMU interface enabled If DSMU interface is enabled, then it is started to operate according to enabled y channels and enabled x filters settings (CHEN bit in DSMU_CHyCFG1 and DFLTEN bit in DSMU_FLTxCTRL1). When setting DSMUEN=0: all registers in DSMU_FLTxSTS are set to reset value (x = 0..3) all registers in DSMU_FLTxAWDSTS are set to reset value (x = 0..3) *Note: DSMUEN is present only in DSMU_CH0CFG1 register (channel y=0)*
30	CLKOUTSRC	Output serial clock source selection 0: Source for output serial clock is from system clock 1: Source for output serial clock is from audio clock This value can be modified only when DSMUEN=0 (in DSMU_CH0CFG1 register). *Note: CLKOUTSRC is present only in DSMU_CH0CFG1 register (channel y=0)*
29:24	Reserved	Reserved, the reset value must be maintained
23:16	CLKOUTDIV[7:0]	Output serial clock divider 0: Output clock generation is disabled (CKOUT signal is set to low state) 1- 255: Defines the division of system clock for the serial clock output for CKOUT signal in range 2 -256 (Divider = CLKOUTDIV+1). CLKOUTDIV also defines the threshold for a clock absence detection. CLKOUTDIV must be configured to follow below formula to receive manchester code. ((CLKOUTDIV + 1) × TSYSCLK) < TManchester clock < (2 × CLKOUTDIV × TSYSCLK) This value can only be modified when DSMUEN=0 (in DSMU_CH0CFG1 register). If DSMUEN=0 (in DSMU_CH0CFG1 register) then CKOUT signal is set to low state (setting is performed two DSMU clock cycle after DSMUEN=0).

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		Note: CLKOUTDIV is present only in DSMU_CH0CFG1 register (channel y=0)
15:14	DATPACK[1:0]	Data packing config in DSMU_CHyDATIN register. 0:Standard: input data in DSMU_CHyDATIN register are stored only in INDAT0[15:0]. Transceiver will generate one sample to the DSMU filter. 1: Interleaved: input data in DSMU_CHyDATIN register are stored as two samples: first sample in INDAT0[15:0] (assigned to channel y) second sample INDAT1[15:0] (assigned to channel y) Transceiver will generate two samples to DSMU filter(INDAT0[15:0] part is read as first sample and then INDAT1[15:0] part is read as next sample). 2: Dual: input data in DSMU_CHyDATIN register are stored as two samples: first sample INDAT0[15:0] (assigned to channel y) second sample INDAT1[15:0] (assigned to channel y+1) Transceiver will generate two samples to DSMU filter, one is from channel y and the other sample is from channel y+1. Dual mode is available only on even channel numbers (y = 0, 2, 4, 6), for odd channel numbers (y = 1, 3, 5, 7) DSMU_CHyDATIN is write protected. If an even channel is set to dual mode then the following odd channel must be set into standard mode (DATPACK[1:0]=0) for correct cooperation with even channel. 3: Reserved This value can be modified only when CHEN=0 (in DSMU_CHyCFG1 register).
13:12	DATMUX[1:0]	Data input multiplexer for channel y 0:Data to channel y are taken from external serial inputs as 1-bit values. DSMU_CHyDATIN register is write protected. 1: Data to channel y are taken from internal ADCy+1 output register update as 16-bit values (if ADCy+1 is available). Data from ADCs are written into INDAT0[15:0],part of DSMU_CHyDATIN register. 2: Data to channel y are taken from internal DSMU_CHyDATIN register by direct CPU/DMA write. There can be written one or two 16-bit data samples according DATPACK[1:0] bit field setting. 3:Reserved This value can be modified only when CHEN=0 (in DSMU_CHyCFG1 register).
11:9	Reserved	Reserved, the reset value must be maintained
8	CHINSEL	Channel inputs selection 0: Channel inputs are taken from pins of the channel y. 1: Channel inputs are taken from pins of the following channel (channel (y+1) modulo 8). This value can be modified only when CHEN=0 (in DSMU_CHyCFG1 register).
7	CHEN	channel y enable 0: channel y disabled 1: channel y enabled If channel y is enabled, then according channel serial data receiving is started.
6	CLKABEN	Clock absence detector enable on channel y

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		0: Clock absence detector disabled on channel y 1: Clock absence detector enabled on channel y
5	SCDETEN	Short-circuit detector enable on channel y 0: channel y serial input will not be monitored by the short-circuit detector 1: channel y serial input will be continuously monitored by the short-circuit detector
4	Reserved	Reserved, the reset value must be maintained
3:2	SPICLKSEL[1:0]	SPI clock source config for channel y 0:SPI clock coming from external CKINy input - sampling point according SITP[1:0] 1:SPI clock coming from internal CKOUT output - sampling point according SITP[1:0] 2:SPI clock coming from internal CKOUT - sampling point on each second CKOUT falling edge. Connected external ΣΔ modulator which divides its clock input (from CKOUT) by 2 to generate its output serial communication clock (and this output clock change is active on each clock input rising edge). 3:SPI clock coming from internal CKOUT output - sampling point on each second CKOUT rising edge. Connected external ΣΔ modulator which divides its clock input (from CKOUT) by 2 to generate its output serial communication clock (and this output clock change is active on each clock input falling edge). This value can be modified only when CHEN=0 (in DSMU_CHyCFG1 register).
1:0	SITP[1:0]	Serial interface type for channel y 00: SPI with rising edge to strobe data 01: SPI with falling edge to strobe data 10: Manchester coded input on DATINy pin: rising edge = logic 0, falling edge = logic 1 11: Manchester coded input on DATINy pin: rising edge = logic 1, falling edge = logic 0 This value can only be modified when CHEN=0 (in DSMU_CHyCFG1 register).

32.5.3 DSMU channel y configuration register2 (DSMU_CHyCFG2)

Offset error：0x04 + 0x20 * y (y = 0 to 7)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALOFFSET[23:8]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALOFFSET[7:0]								DATRBS[4:0]					Reserved		
rw								rw							

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Bit field	Name	Description
31:8	CALOFFSET[23:0]	channel y 24-bit calibration CALOFFSET value. For channel y, CALOFFSET is applied to each conversion result from this channel. This value is set by software.
7:3	DATRBS[4:0]	channel y data right bit-shift value 0-31: Defines how many bit shifts to the right for the result from integrator, will be performed to have final results. Bit-shift is performed before CALOFFSET correction. The data shift is rounding the result to nearest integer value. The sign of shifted result is maintained (to have valid 24-bit signed format of result data). This value can be modified only when CHEN=0 (in DSMU_CHyCFG1 register).
2:0	Reserved	Reserved, the reset value must be maintained

32.5.4 DSMU channel y short-circuit detector and analog watchdog register (DSMU_CHyAWDSCDET)

Offset error：0x08 + 0x20 * y (y = 0 to 7)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								AWDFORD[1:0]		Reserved	AWDFOSR[4:0]				
								rw			rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BKSCDET[3:0]				Reserved				SCDETTH[7:0]							
rw								rw							

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:22	AWDFORD[1:0]	Analog watchdog Sinc filter order on channel y 0: FastSinc filter type 1: Sinc^1 filter type 2: Sinc^2 filter type 3: Sinc^3 filter type Sincx filter type transfer function: $H(z)= [\frac{1-z^{-FOSR}}{1-Z^{-1}}]^X$ FastSinc filter type transfer function: $H(z)= [\frac{1-z^{-FOSR}}{1-Z^{-1}}]^2 * (1+z^{-(2*FOSR)})$ This bit can be modified only when CHEN=0 (in DSMU_CHyCFG1 register).
21	Reserved	Reserved, the reset value must be maintained

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20:16	AWDFOSR[4:0]	Analog watchdog filter oversampling ratio (decimation rate) on channel y 0 - 31: Defines the length of the Sinc type filter in the range 1 - 32 (AWDFOSR + 1). This number is also the decimation ratio of the analog data rate. This bit can be modified only when CHEN=0 (in DSMU_CHyCFG1 register). *Note: If AWDFOSR = 0 then the sinc filter has no effect (filter bypass).*
15:12	BKSCDET[3:0]	Break signal assignment for short-circuit detector on channel y BKSCDET[i] = 0: Break i signal not assigned to short-circuit detector on channel y BKSCDET[i] = 1: Break i signal assigned to short-circuit detector on channel y
11:8	Reserved	Reserved, the reset value must be maintained
7:0	SCDETTH[7:0]	short-circuit detector threshold value for channel y Software write these bits to define the threshold counter value for the short-circuit detector. If this value is reached, then a short-circuit event occurs on a given channel.

32.5.5 DSMU channel y watchdog filter data register(DSMU_CHyAWDDAT)

Offset error：0x0C + 0x20 * y (y = 0 to 7)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AWDDAT[15:0]															
r															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	AWDDAT[15:0]	Input channel y watchdog data Data converted by the analog watchdog filter for input channel y. This data is continuously converted (no trigger) for this channel, with a limited resolution (OSR=1..32/sinc order = 1..3). The rate of reading this AWD must be faster than the rate of continuously update of AWD to avoid missing data, as it don't have trigger flag, main purpose is for debugging only.

32.5.6 DSMU channel y input data register(DSMU_CHyDATIN)

Offset error：0x10 + 0x20 * y (y = 0 to 7)

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Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INDATAT1[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDATAT0[15:0]															
rw															

Bit field	Name	Description
31:16	INDATAT1[15:0]	Input data for channel y or channel y+1 Input parallel channel data to be processed by the digital filter if DATMUX[1:0]=1 or DATMUX[1:0]=2. Data can be written by CPU/DMA (if DATMUX[1:0]=2) or by internal ADC (if DATMUX[1:0]=1). If DATPACK[1:0]=0 (standard mode),INDAT1[15:0] is write protected (not used for input sample). If DATPACK[1:0]=1 (interleaved mode),Second channel y data sample is stored into DAT1IN[15:0]. First channel y data sample is stored into INDAT0[15:0]. Both samples are read sequentially by DSMU_FLTx filter as two channel y data samples. If DATPACK[1:0]=2 (dual mode) For even y channels: sample in INDAT1[15:0] is automatically copied into INDAT0[15:0] of channel (y+1). For odd y channels: INDAT1[15:0] is write protected. See Parallel data inputs section for more details. INDAT1[15:0] is in the16-bit signed format.
15:0	INDATAT0[15:0]	Input data for channel y Input parallel channel data to be processed by the digital filter if DATMUX[1:0]=1 or DATMUX[1:0]=2. Data can be written by CPU/DMA (if DATMUX[1:0]=2) or directly by internal ADC (if DATMUX[1:0]=1). If DATPACK[1:0]=0 (standard mode) Channel y data sample is stored into INDATAT0[15:0]. If DATPACK[1:0]=1 (interleaved mode) First channel y data sample is stored into INDATAT0[15:0]. Second channel y data sample is stored into INDATAT1[15:0]. Both samples are read sequentially by DSMU_FLTx filter as two channel y data samples. If DATPACK[1:0]=2 (dual mode). For even y channels: Channel y data sample is stored into INDATAT0[15:0]. For odd y channels: INDATAT0[15:0] is write protected. See Parallel data inputs section for more details.

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		INDATAT0[15:0] is in the16-bit signed format.

32.5.7 DSMU filter x control register 1 (DSMU_FLTxCTRL1)

Offset error： 0x100 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	AWDFSEL	FAST	Reserved		RCH[2:0]			Reserved		RDMAEN	Reserved	RSYNC	RCONT	RSWSTART	Reserved
	rw	rw			rw					rw		rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	JEXTEN[1:0]		JEXTSEL[4:0]					Reserved		JDMAEN	JSCAN	JSYNC	Reserved	JSWSTART	DFLTEN
	rw		rw							rw	rw	rw		rw	rw

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained
30	AWDFSEL	Analog watchdog input data selection 0: Analog watchdog on data output value (after the digital filter). The comparison is done after CALOFFSET calibration and right bit-shift 1: Analog watchdog on channel serial transceivers value (after watchdog filter)

29	FAST	Fast conversion mode selection for regular conversions
		0: Fast conversion mode disabled
		1: Fast conversion mode enabled
		When converting a regular conversion in continuous mode, having enabled the fast mode causes each conversion (except the first) to execute faster than in standard mode. This bit has no effect on conversions which are not continuous.
		This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1).
		if FAST=0 (or first conversion in continuous mode if FAST=1):
		t = [FOSR * (IOSR-1 + FORD) + FORD] / f_{CKIN}..... for $Sinc^x$ filters
		t = [FOSR * (IOSR-1 + 4) + 2] / f_{CKIN}..... for FastSinc filter
		if FAST=1 in continuous mode (except first conversion):
		t = [FOSR * IOSR] / f_{CKIN}
		in case if FOSR = FOSR[9:0]+1 = 1 (filter bypassed, active only integrator):
		t = IOSR / f_{CKIN} (... but COVCNT=0)
		where: f_{CKIN} is the channel input clock frequency (on given channel CKINy pin) or input data rate in case of parallel data input.

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28:27	Reserved	Reserved, the reset value must be maintained
26:24	RCH[2:0]	Regular conversion channel 0: Channel 0 is selected as the regular conversion channel 1: Channel 1 is selected as the regular conversion channel ... 7: Channel 7 is selected as the regular conversion channel Writing these bits when RCIP=1 takes effect when the next regular conversion begins. This is especially useful in continuous mode (RCONT=1). It also affects regular conversions which are pending (due to ongoing injected conversion).
23:22	Reserved	Reserved, the reset value must be maintained
21	RDMAEN	DMA channel enabled to read regular conversion data 0: The DMA channel is not enabled to read regular converison data 1: The DMA channel is enabled to read regular conversion data This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1).
20	Reserved	Reserved, the reset value must be maintained
19	RSYNC	Launch regular conversion synchronously with DSMU_FLT0 0: Do not launch a regular conversion synchronously with DSMU_FLT0 1: Launch a regular conversion in this DSMU_FLTx at the very moment when a regular conversion is launched in DSMU_FLT0. This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1).
18	RCONT	Continuous mode config for regular conversions 0: The regular channel is converted just once for each conversion request 1: The regular channel is converted repeatedly after each conversion request Writing ‘0’ to this bit while a continuous regular conversion is already in progress stops the continuous mode immediately.
17	RSWSTART	Software trigger of a conversion on the regular channel 0: Writing ‘0’ has no effect 1: Writing ‘1’ makes a trigger to start a conversion on the regular channel and causes RCIP to become ‘1’. If RCIP=1 already, writing to RSWSTART has no effect. Writing ‘1’ has no effect if RSYNC=1. This bit is always read as ‘0’.
16:15	Reserved	Reserved, the reset value must be maintained
14:13	JEXTEN[1:0]	External trigger enable and trigger active edge selection for injected conversions 00: Trigger detection is disabled 01: Each rising edge on the selected trigger makes a request to launch an injected conversion 10: Each falling edge on the selected trigger makes a request to launch an injected conversion 11: Both rising edges and falling edges on the selected trigger make requests to launch injected conversions This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1).

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12:8	JEXTSEL[4:0]	External trigger signal selection for launching injected conversions 0x0-0x1F: Trigger inputs selected by the following table (internal or external trigger). This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1). *Note: synchronous trigger has latency up to one DSMU clock cycle (with deterministic jitter), asynchronous trigger has latency 2-3 DSMUCLK clock cycles (with jitter up to 1 cycle).* DSMU_FLTx 0x00 DSMU_jtrg0 0x01 DSMU_jtrg1 ... 0x1E DSMU_jtrg30 0x1F DSMU_jtrg31 Refer to : DSMU triggers connection.
7:6	Reserved	Reserved, the reset value must be maintained
5	JDMAEN	DMA channel enabled to read data for the injected conversion 0: The DMA channel is not enabled to read injected data 1: The DMA channel is enabled to read injected data This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1).
4	JSCAN	Injected scanning conversion mode 0: One channel conversion is performed from the injected channel group and the next selected channel from this group is selected. 1: The series of conversions for the injected group channels is executed, starting over with the lowest selected channel. This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1). Writing JCHG if JSCAN=0 resets the channel selection to the lowest selected channel.
3	JSYNC	Launch an injected conversion synchronously with the DSMU_FLT0 JSWSTART event 0: Do not launch an injected conversion synchronously with DSMU_FLT0 1: Launch an injected conversion in this DSMU_FLTx at the very moment when an injected conversion is launched in DSMU_FLT0 by its JSWSTART trigger This bit can be modified only when DFLTEN=0 (DSMU_FLTxCTRL1).
2	Reserved	Reserved, the reset value must be maintained
1	JSWSTART	Start a conversion of the injected group of channels 0: Writing ‘0’ has no effect. 1: Writing ‘1’ makes a request to convert the channels in the injected conversion group, causing JCIP to become ‘1’ at the same time. If JCIP=1 already, then writing to JSWSTART has no effect. Writing ‘1’ has no effect if JSYNC=1. This bit is always read as ‘0’.

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0	DFLTEN	DSMU_FLTx enable 0: DSMU_FLTx is disabled. All conversions of given DSMU_FLTx are stopped immediately and all DSMU_FLTx functions are stopped. 1: DSMU_FLTx is enabled. If DSMU_FLTx is enabled, then DSMU_FLTx starts operating according to its setting. Data which are cleared by setting DFLTEN=0: DSMU_FLTxSTS registers are set to the reset state DSMU_FLTxAWDSTS registers are set to the reset state

32.5.8 DSMU filter x control register 2 (DSMU_FLTxCTRL2)

Offset error：0x104 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								AWDCH[7:0]							
								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXDETCH[7:0]								Reserved	CLKABIEN	SCDETIEN	AWDIEN	ROVRIEN	JOVRIEN	REOCIEN	JEOCIEN
rw									rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:16	AWDCH[7:0]	Analog watchdog channel selection These bits select the input channel to be guarded continuously by the analog watchdog. AWDCH[x] = 0: Analog watchdog is disabled on channel y AWDCH[x] = 1: Analog watchdog is enabled on channel y
15:8	EXDETCH[7:0]	Extremes detector channel selection These bits select the input channels to be taken by the Extremes detector. EXDETCH[x] = 0: Extremes detector does not accept data from channel y EXDETCH[x] = 1: Extremes detector accepts data from channel y
7	Reserved	Reserved, the reset value must be maintained

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6	CLKABIEN	Clock absence interrupt enable 0: Detection of channel input clock absence interrupt is disabled 1: Detection of channel input clock absence interrupt is enabled Please see the explanation of CLKABF[7:0] in DSMU_FLTxSTS. *Note: CLKABIEN is present only in DSMU_FLT0CTRL2 register (filter x=0)*
5	SCDETIEN	Short-circuit detector interrupt enable 0: short-circuit detector interrupt is disabled 1: short-circuit detector interrupt is enabled Please see the explanation of SCDETF[7:0] in DSMU_FLTxSTS. *Note: SCDETIEN is present only in DSMU_FLT0CTRL2 register (filter x=0)*
4	AWDIEN	Analog watchdog interrupt enable 0: Analog watchdog interrupt is disabled 1: Analog watchdog interrupt is enabled Please see the explanation of AWDF in DSMU_FLTxSTS.
3	ROVRIEN	Regular data overrun interrupt enable 0: Regular data overrun interrupt is disabled 1: Regular data overrun interrupt is enabled Please see the explanation of ROVRF in DSMU_FLTxSTS.
2	JOVRIEN	Injected data overrun interrupt enable 0: Injected data overrun interrupt is disabled 1: Injected data overrun interrupt is enabled Please see the explanation of JOVRF in DSMU_FLTxSTS.
1	REOCIEN	Regular conversion end interrupt enable 0: Regular conversion end interrupt is disabled 1: Regular conversion end interrupt is enabled Please see the explanation of REOCF in DSMU_FLTxSTS.
0	JEOCIEN	Injected conversion end interrupt enable 0: Injected conversion end interrupt is disabled 1: Injected conversion end interrupt is enabled Please see the explanation of JEOCF in DSMU_FLTxSTS.

32.5.9 DSMU filter x status register (DSMU_FLTxSTS)

Offset error：0x108 + 0x80 * x (x = 0 to 3)

Reset value：0x00FF 0000(x=0)　0x0000 0000(x= 1 to 3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCDETF[7:0]								CLKABF[7:0]							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	RCIP	JCIP	Reserved	AWDF	ROVRF	JOVRF	REOCF	JEOCF
r	r	r		r	r	r	r	r

For each of the flag bits, an interrupt can be enabled by setting the corresponding bit in DSMU_FLTxCTRL2. If an interrupt is called, the flag must be cleared before exiting the interrupt service routine.

All the bits of DSMU_FLTxSTS are automatically reset when DFLTEN=0.

Bit field	Name	Description
31:24	SCDETF[7:0]	short-circuit event flag SCDETF[y]=0: No short-circuit detector event occurred on channel y SCDETF[y]=1: The short-circuit detector counter reaches, on channel y, the value programmed in the DSMU_CHyAWDSCDET registers This bit is set by hardware. It can be cleared by software using the corresponding CLRSCDETF[y] bit in the DSMU_FLTxINTCLR register. SCDETF[y] is cleared also by hardware when CHEN[y] = 0 (given channel is disabled). *Note: SCDETF[7:0] is present only in DSMU_FLT0STS register (filter x=0)*
23:16	CLKABF[7:0]	Clock absence event flag CLKABF[y]=0: Clock signal on channel y is present. CLKABF[y]=1: Clock signal on channel y is not present. Given y bit is set by hardware when clock absence is detected on channel y. It is held at CLKABF[y]=1 state by hardware when CHEN=0 (see DSMU_CHyCFG1 register). It is held at CLKABF[y]=1 state by hardware when the transceiver is not yet synchronized. It can be cleared by software using the corresponding CLRCLKABF[y] bit in the DSMU_FLTxINTCLR register. *Note: CLKABF[7:0] is present only in DSMU_FLT0STS register (filter x=0)*
15	Reserved	Reserved, the reset value must be maintained
14	RCIP	Regular conversion active status 0: No request to convert the regular channel has been issued 1: The conversion of the regular channel is in progress or a request for a regular conversion is pending A request to start a regular conversion is ignored when RCIP=1.
13	JCIP	Injected conversion active status 0: No request to convert the injected channel group (neither by software nor by trigger) has been issued 1: The conversion of the injected channel group is in progress or a request for a injected conversion is pending, due either to '1' being written to JSWSTART or to a trigger detection A request to start an injected conversion is ignored when JCIP=1.
12:5	Reserved	Reserved, the reset value must be maintained

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4	AWDF	Analog watchdog event flag 0: No Analog watchdog event occurred 1: The analog watchdog block detected voltage which crosses the value programmed in the DSMU_FLTxAWDLT or DSMU_FLTxAWDHT registers. This bit is set by hardware. It is cleared by software by clearing all source flag bits AWDHTF[7:0] and AWDLTF[7:0] in DSMU_FLTxAWDSTS register (by writing '1' into the clear bits in DSMU_FLTxAWDCLR register).
3	ROVRF	Regular conversion overrun flag 0: No regular conversion overrun has occurred 1: A regular conversion overrun has occurred, which means that a regular conversion finished while REOCF was already '1'. RDAT is not affected by overruns This bit is set by hardware. It can be cleared by software using the CLRROVRF bit in the DSMU_FLTxINTCLR register.
2	JOVRF	Injected conversion overrun flag 0: No injected conversion overrun has occurred 1: An injected conversion overrun has occurred, which means that an injected conversion finished while JEOCF was already '1'. JDAT is not affected by overruns. This bit is set by hardware. It can be cleared by software using the CLRJOVRF bit in the DSMU_FLTxINTCLR register.
1	REOCF	Regular conversion end event flag 0: No regular conversion has completed 1: A regular conversion has completed and its data may be read This bit is set by hardware. It is cleared when the software or DMA reads DSMU_FLTxRDAT. *Note: In DMA mode, the destination address is set as DSMU_FLTxJDAT.*
0	JEOCF	Injected conversion end event flag 0: No injected conversion has completed 1: An injected conversion has completed and its data may be read This bit is set by hardware. It is cleared when the software or DMA reads DSMU_FLTxJDAT.

32.5.10 DSMU filter x interrupt flag clear register (DSMU_FLTxINTCLR)

Offset error：0x10C + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRSCDETF[7:0]								CLRCLKABF[7:0]							
w								w							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												CLRROVRF	CLRJOVRF	Reserved	
												w	w		

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The bits of DSMU_FLTxINTCLR are always read as ‘0’.

Bit field	Name	Description
31:24	CLRSCDETF[7:0]	Clear the short-circuit event flag CLRSCDETF[y]=0: Writing ‘0’ has no effect CLRSCDETF[y]=1: Writing ‘1’ to position y clears the corresponding SCDETF[x] bit in the DSMU_FLTxSTS register *Note: CLRSCDETF[7:0] is present only in DSMU_FLT0INTCLR register*
23:16	CLRCLKABF[7:0]	Clear the clock absence flag CLRCLKABF[y]=0: Writing ‘0’ has no effect CLRCLKABF[y]=1: Writing ‘1’ to position y clears the corresponding CLKABF[y] bit in the DSMU_FLTxSTS register. When the transceiver is not yet synchronized, the clock absence flag is set and cannot be cleared by CLRCLKABF[y]. *Note: CLRCLKABF[7:0] is present only in DSMU_FLT0INTCLR register*
15:4	Reserved	Reserved, the reset value must be maintained
3	CLRROVRF	Clear the regular conversion overrun flag 0: Writing ‘0’ has no effect 1: Writing ‘1’ clears the ROVRF bit in the DSMU_FLTxSTS register
2	CLRJOVRF	Clear the injected conversion overrun flag 0: Writing ‘0’ has no effect 1: Writing ‘1’ clears the JOVRF bit in the DSMU_FLTxSTS register
1:0	Reserved	Reserved, the reset value must be maintained

32.5.11 DSMU filter x injected channel group selection register (DSMU_FLTxJCHG)

Offset error：0x110 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								JCHG[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained

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7:0	JCHG[7:0]	Injected channel group selection JCHG[y]=0: channel y is not part of the injected group JCHG[y]=1: channel y is part of the injected group If JSCAN=1, each of the selected channels is converted, one after another. The lowest channel (channel 0, if selected) is converted first and the sequence ends at the highest selected channel. If JSCAN=0, then only one channel is converted from the selected channels, and the channel selection is moved to the next channel. Writing JCHG, if JSCAN=0, resets the channel selection to the lowest selected channel. At least one channel must always be selected for the injected group. Writes causing all JCHG bits to be zero are ignored.

32.5.12 DSMU filter x function control register (DSMU_FLTxFCTRL)

Offset error：0x114 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FORD[2:0]			Reserved			FOSR[9:0]									
rw						rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								IOSR[7:0]							
								rw							

Bit field	Name	Description
31:29	FORD[2:0]	Sinc filter order 0: FastSinc filter type 1: Sinc^1 filter type 2: Sinc^2 filter type 3: Sinc^3 filter type 4: Sinc^4 filter type 5: Sinc^5 filter type 6-7: Reserved Sinc^x filter type transfer function: $H(z)= [\frac{1-z^{-FOSR}}{1-Z^{-1}}]^X$ FastSinc filter type transfer function: $H(z)= [\frac{1-z^{-FOSR}}{1-Z^{-1}}]^2 * (1+z^{-(2*FOSR)})$ This bit can be modified only when DFLTEN=0 (in DSMU_FLTxCTRL1 register).
28:26	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
25:16	FOSR[9:0]	Sinc filter oversampling ratio (decimation rate) 0 - 1023: Defines the length of the Sinc type filter in the range 1 - 1024 (FOSR = FOSR[9:0] +1). This number is also the decimation ratio of the output data rate from filter. This bit can only be modified when DFLTEN=0 (DSMU_FLTxCTRL1) *Note: If FOSR = 0, then the filter has no effect (filter bypass).*
15:8	Reserved	Reserved, the reset value must be maintained
7:0	IOSR[7:0]	Integrator oversampling ratio (averaging length) 0- 255: The length of the Integrator in the range 1 - 256 (IOSR + 1). Defines how many samples from Sinc filter will be summed into one output data sample from the integrator. The output data rate from the integrator will be decreased by this number (additional data decimation ratio). This bit can only be modified when DFLTEN=0 (DSMU_FLTxCTRL1) Note: If IOSR = 0, then the Integrator has no effect (Integrator bypass).

32.5.13 DSMU filter x injected conversion data register (DSMU_FLTxJDAT)

Offset error：0x118 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
JDAT[23:8]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JDAT[7:0]								Reserved					JDATCH[2:0]		
r													r		

DMA may be used to read the data from this register. Half-word accesses may be used to read only the MSBs of conversion data.

Reading this register also clears JEOCF in DSMU_FLTxSTS. Thus, the firmware must not read this register if DMA is activated to read data from this register.

Bit field	Name	Description
31:8	JDAT[23:0]	Injected group conversion data When each conversion of a channel in the injected group finishes, its resulting data is stored in this field. The data is valid when JEOCF=1. Reading this register clears the corresponding JEOCF.
7:3	Reserved	Reserved, the reset value must be maintained

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2:0	JDATCH[2:0]	Injected channel most recently converted When each conversion of a channel in the injected group finishes, JDATCH[2:0] is updated to indicate which channel was converted. Thus, JDAT[23:0] holds the data that corresponds to the channel indicated by JDATCH[2:0].

32.5.14 DSMU filter x data register for the regular channel (DSMU_FLTxRDAT)

Offset error：0x11C + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDAT[23:8]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDAT[7:0]								Reserved			RPEND	Reserved	RDATCH[2:0]		
r											r	r	r		

Half-word accesses may be used to read only the MSBs of conversion data.

Reading this register also clears REOCF in DSMU_FLTxSTS.

Bit field	Name	Description
31:8	RDAT[23:0]	Regular channel conversion data When each regular conversion finishes, its data is stored in this register. The data is valid when REOCF=1. Reading this register clears the corresponding REOCF.
7:5	Reserved	Reserved, the reset value must be maintained
4	RPEND	Regular channel pending data Regular data in RDAT[23:0] was delayed due to an injected channel trigger during the conversion
3	Reserved	Reserved, the reset value must be maintained
2:0	RDATCH[2:0]	Regular channel most recently converted When each regular conversion finishes, RDATCH[2:0] is updated to indicate which channel was converted (because regular channel selection RDATCH[2:0] in DSMU_FLTxCTRL1 register can be updated during regular conversion). Thus RDAT[23:0] holds the data that corresponds to the channel indicated by RDATCH[2:0].

32.5.15 DSMU filter x analog watchdog high threshold register (DSMU_FLTxAWDHT)

Offset error：0x120 + 0x80 * x (x = 0 to 3)

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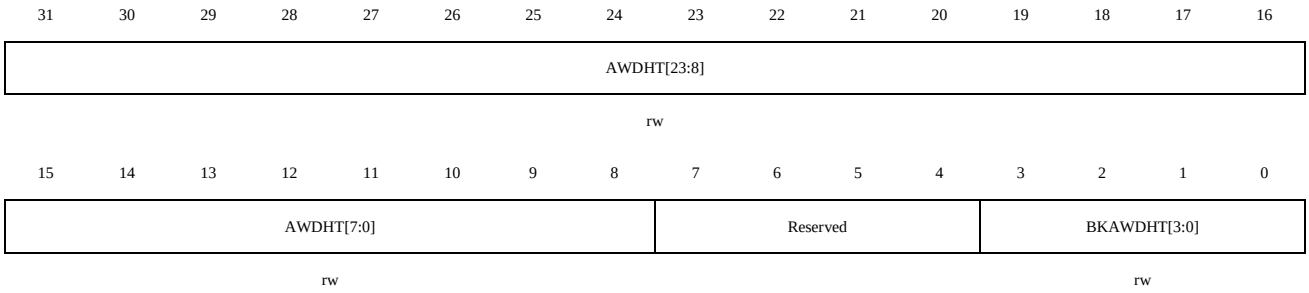
Reset value：0x0000 0000

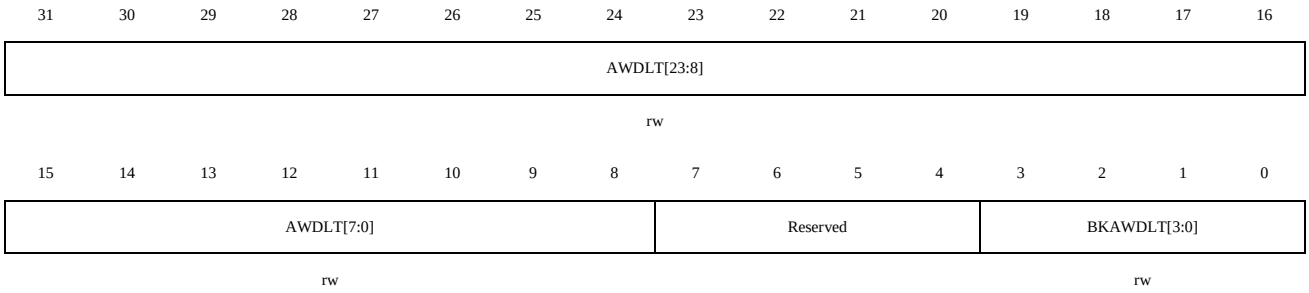


Bit field	Name	Description
31:8	AWDHT[23:0]	Analog watchdog threshold high These bits are written by software to define the high threshold for the analog watchdog. *Note: In case channel transceivers monitor (AWDFSEL=1), the higher 16 bits (AWDHT[23:8]) define the 16-bit threshold as compared with the analog watchdog filter output (because data coming from the analog watchdog filter are up to a 16-bit resolution). Bits AWDHT[7:0] are not taken into comparison in this case.*
7:4	Reserved	Reserved, the reset value must be maintained
3:0	BKAWDHT[3:0]	Break signal assignment to analog watchdog threshold high event BKAWDHT[i] = 0: Break i signal is not assigned to an analog watchdog high threshold event BKAWDHT[i] = 1: Break i signal is assigned to an analog watchdog high threshold event

32.5.16 DSMU filter x analog watchdog low threshold register (DSMU_FLTxAWDLT)

Offset error：0x124 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000



Bit field	Name	Description

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[31:8]	AWDLT[23:0]	Analog watchdog threshold low These bits are written by software to define the low threshold for the analog watchdog. *Note: In case channel transceivers monitor (AWDFSEL=1), only the higher 16 bits (AWDLT[23:8]) define the 16-bit threshold as compared with the analog watchdog filter output (because data coming from the analog watchdog filter are up to a 16-bit resolution). Bits AWDLT[7:0] are not taken into comparison in this case.*
[7:4]	Reserved	Reserved, the reset value must be maintained
[3:0]	BKAWDLT[3:0]	Break signal assignment to analog watchdog threshold low event BKAWDLT[i] = 0: Break i signal is not assigned to an analog watchdog low threshold event BKAWDLT[i] = 1: Break i signal is assigned to an analog watchdog low threshold event

32.5.17 DSMU filter x analog watchdog status register (DSMU_FLTxAWDSTS)

Offset error：0x128 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AWDHTF[7:0]								AWDLTF[7:0]							
r								r							

All the bits of DSMU_FLTxAWDSTS are automatically reset when DFLTEN=0.

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	AWDHTF[7:0]	Analog watchdog threshold high flag AWDHTF[y]=1 indicates a high threshold error on channel y. It is set by hardware. It can be cleared by software using the corresponding CLRAWDHTF[y] bit in the DSMU_FLTxAWDCLR register.
7:0	AWDLTF[7:0]	Analog watchdog threshold low flag AWDLTF[y]=1 indicates a low threshold error on channel y. It is set by hardware. It can be cleared by software using the corresponding CLRAWDLTF[y] bit in the DSMU_FLTxAWDCLR register.

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32.5.18 DSMU filter x analog watchdog clear flag register (DSMU_FLTxAWDCLR)

Offset error：0x12C + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRAWDHTF[7:0]								CLRAWDLTF[7:0]							
w								w							

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	CLRAWDHTF[7:0]	Clear the analog watchdog threshold high flag CLRAWDHTF[y]=0: Writing ‘0’ has no effect CLRAWDHTF[y]=1: Writing ‘1’ to position y clears the corresponding AWDHTF[y] bit in the DSMU_FLTxAWDSTS register
7:0	CLRAWDLTF[7:0]	Clear the analog watchdog threshold low flag CLRAWDLTF[y]=0: Writing ‘0’ has no effect CLRAWDLTF[y]=1: Writing ‘1’ to position y clears the corresponding AWDLTF[y] bit in the DSMU_FLTxAWDSTS register

32.5.19 DSMU filter x extremes detector maximum register (DSMU_FLTxEXDETMAX)

Offset error：0x130 + 0x80 * x (x = 0 to 3)

Reset value：0x8000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXDETMAX[23:8]															
rs_r	rc_r														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXDETMAX[7:0]								Reserved					EXDETMAXCH[2:0]		
rc_r													rc_r		

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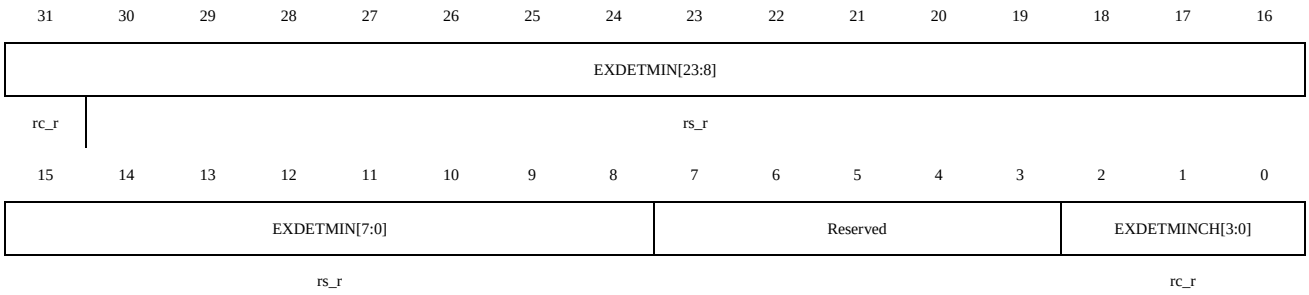
Bit field	Name	Description
31:8	EXDETMAX[23:0]	Extremes detector maximum value These bits are set by hardware and indicate the highest value converted by DSMU_FLTx. EXDETMAX[23:0] bits are reset to value (0x800000) by reading of this register.
7:3	Reserved	Reserved, the reset value must be maintained
2:0	EXDETMAXCH[2:0]	Extremes detector maximum data channel. These bits contains information about the channel on which the data is stored into EXDETMAX[23:0]. Bits are cleared by reading of this register.

32.5.20 DSMU filter x extremes detector minimum register (DSMU_FLTxEXDETMIN)

Offset error：0x134 + 0x80 * x (x = 0 to 3)

Reset value：0x7FFF FF00



Bit field	Name	Description
31:8	EXDETMIN[23:0]	Extremes detector minimum value These bits are set by hardware and indicate the lowest value converted by DSMU_FLTx. EXDETMIN[23:0] bits are reset to value (0x7FFFFF) by reading of this register.
7:3	Reserved	Reserved, the reset value must be maintained
2:0	EXDETMINCH[2:0]	Extremes detector minimum data channel These bits contain information about the channel on which the data is stored into EXDETMIN[23:0]. Bits are cleared by reading of this register.

32.5.21 DSMU filter x conversion timer register (DSMU_FLTxCOVTIM)

Offset error：0x138 + 0x80 * x (x = 0 to 3)

Reset value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COVCNT[27:12]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COVCNT[11:0]												Reserved			
r															

Bit field	Name	Description

31:4	COVCNT[27:0]	28-bit timer counting conversion time t = COVCNT[27:0] / $f_{DSMUCLK}$
		The timer has an input clock from DSMU clock ($f_{DSMUCLK}$). Conversion time measurement is started on each conversion start and stopped when conversion finishes (interval between first and last serial sample). Only in case of filter bypass (FOSR[9:0] = 0) is the conversion.Time measurement stopped and COVCNT[27:0] = 0. The counted time is:
		if FAST=0 (or first conversion in continuous mode if FAST=1):
		t = [FOSR * (IOSR-1 + FORD) + FORD] / f_{CKIN}..... for $Sinc^x$ filters
		t = [FOSR * (IOSR-1 + 4) + 2] / f_{CKIN}..... for FastSinc filter
		if FAST=1 in continuous mode (except first conversion):
		t = [FOSR * IOSR] / f_{CKIN}
		in case if FOSR = FOSR[9:0]+1 = 1 (filter bypassed, active only integrator):
		COVCNT = 0 (counting is stopped, conversion time: t = IOSR / f_{CKIN})
		where: f_{CKIN} is the channel input clock frequency (on given channel CKINy pin) or input data rate in case of parallel data input (from internal ADC or from CPU/DMA write)
		Note: When conversion is interrupted (e.g. by disable/enable selected channel) the timer counts also this interruption time.

3:0	Reserved	Reserved, the reset value must be maintained

33 Universal Synchronous Asynchronous Receiver Transmitter (USART)

33.1 Introduction

USART is a full-duplex universal synchronous/asynchronous serial transceiver module. This interface is a highly flexible serial communication device that can perform full-duplex data exchange with external devices.

The USART has programmable transmit and receive baud rates and can communicate continuously using DMA. It

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also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smartcard asynchronous protocol, IrDA SIR ENDEC function, and hardware flow control function.

33.2 Main Features

- Supports full-duplex, asynchronous communication
- Supports single-wire half-duplex communication
- Configurable baud rate, with a maximum baud rate of 37.5Mbit/s
- Supports 8x or 16x oversampling
- Supports 8-bit or 9-bit data frames
- Features two internal FIFOs for transmitting and receiving data
- Supports 1-bit or 2-bit stop bits
- Hardware generation of parity bits and parity check
- Hardware flow control: RTS, CTS
- Supports RS-485
- Supports DMA for both transmission and reception
- Supports multi-processor communication: enters silent mode if address does not match, can be woken up by idle bus detection or address identification
- Supports synchronous mode, allowing users to control bidirectional synchronous serial communication in master mode
- Supports smart card asynchronous protocol, compliant with ISO7816-3 standard
- Supports Serial Infrared (IrDA SIR) protocol encoding and decoding, providing normal and low-power operation modes
- Supports LIN mode
- Supports multi-clock error detection: data overflow error, frame error, noise error, parity error
- Supports multiple interrupt requests: transmit data register empty, CTS flag, transmission complete, data received, data overflow, bus idle, parity error, LIN mode break frame detection, and noise flag/overflow error/frame error in multi-buffer communication (DMA)

33.3 Functional Block Diagram

Figure 33-1 USART Block Diagram

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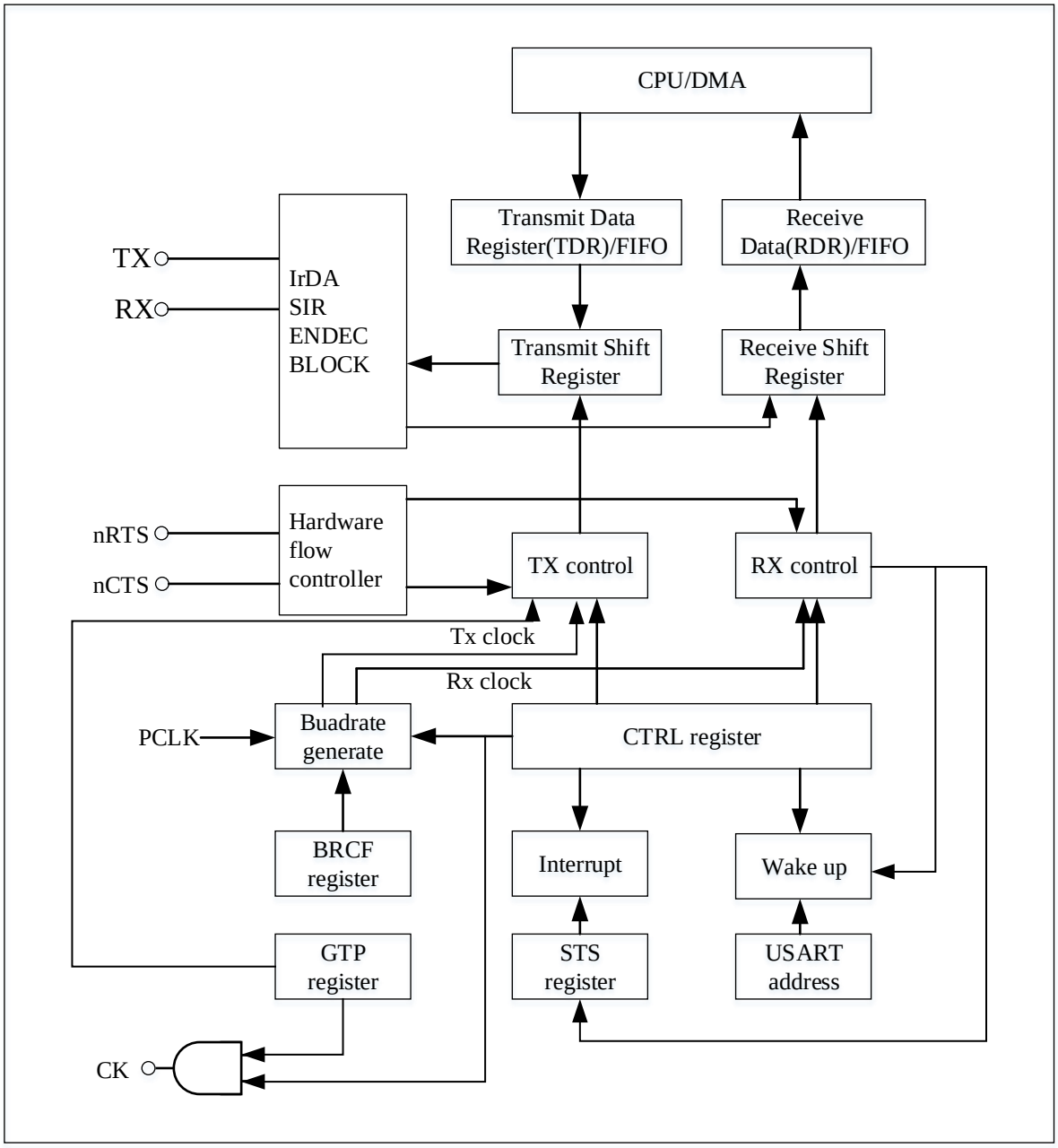

33.4 Function Description

As shown in the Figure 33-1, the bidirectional communications of any USART need to use the RX and TX pins of the external connection. Among them, TX is the output pin for serial data transmission. When the transmitter is active and not sending data, the TX pin is pulled high. When the transmitter is inactive, the TX pin reverts to the I/O port configuration. RX is an input pin for serial data reception, data is received by the oversampling technique.

The data packets of serial communication are transmitted from the sending device to the RX interface of the receiving device through its own TX interface, and the bus is in an idle state before transmitting or receiving. Frame format is: 1 start bit + 8 or 9 data bits (least significant bit first) + 1 parity bit (optional) + 0.5,1,1.5 or 2 stop bit.

Use the fractional baud rate generator to configure transmit and receive baud rates.

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According to the block diagram, when using the hardware flow control mode, the nRTS output and nCTS input pins are required. When the USART receiver is ready to receive new data, nRTS becomes low level. If nCTS is valid (pulled to a low level), the next data is sent, otherwise the next frame of data is not sent.

When using synchronous mode, the CK pin is required. The CK pin is used for clock output for synchronous transfers. Clock phase and polarity are software programmable. During the start and stop bits, the CK pin does not output clock pulses.The CK pin is also used when using smartcard mode.

33.4.1 USART Frame Format

Start bit: 1 bit, active low.

Data bits: Configurable via USART_CTRL1.WL as 8 or 9 bits, with the LSB first.

Stop bit: Active high.

Idle frame: A complete data frame consisting entirely of '1's, including the start bit. followed by the start bit of a data frame containing the data .

Break frame: A break frame is a complete data frame consisting of '0's, including the stop bit. at the end of the break frame, the transmitter inserts 1 or 2 more stop bits ('1') to acknowledge the start bit.

Figure 33-2 Word Length = 8 setting

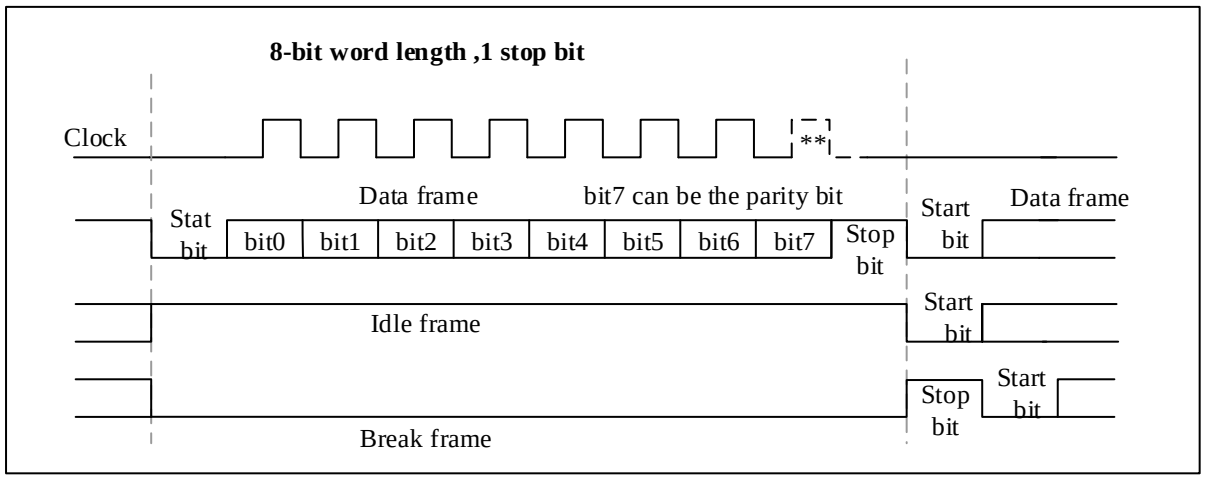

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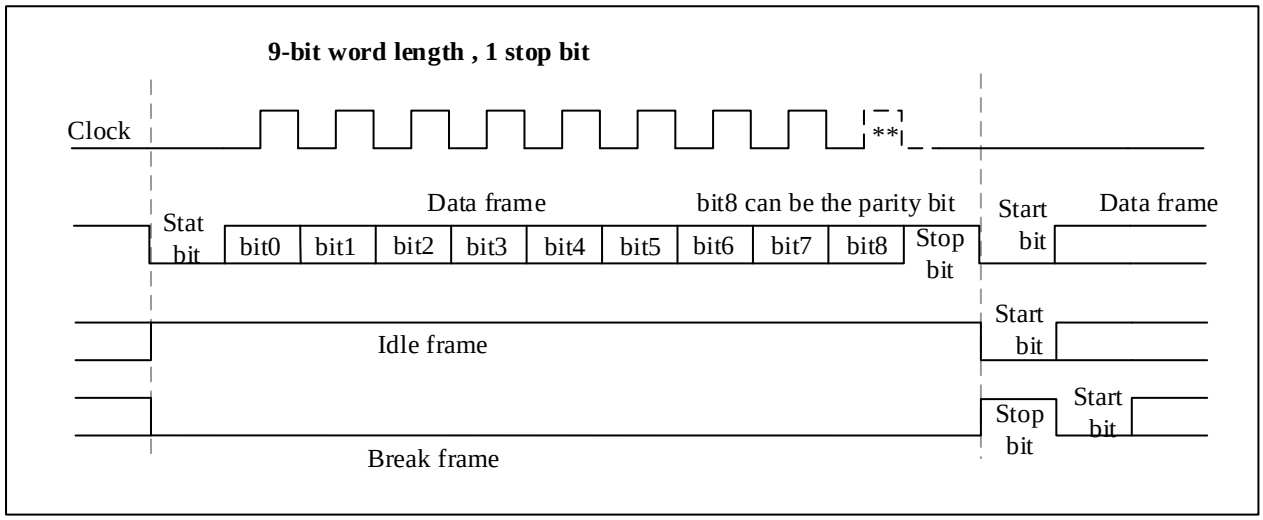
Figure 33-3 Word Length = 9 setting



33.4.2 USART FIFO and Threshold

USART can operate in FIFO mode.

USART has a transmit FIFO (TXFIFO) and a receive FIFO (RXFIFO). FIFO mode can be enabled by setting USART_FIFO.EN to 1.

The maximum data word length is 9 bits, so TXFIFO is 9 bits wide. However, the default width of RXFIFO is 12 bits. This is because the receiver not only stores data in the FIFO but also stores error flags associated with each character (parity error, noise error, and frame error flags).

Note:

Received data is stored together with the corresponding flags in RXFIFO, but only the data is read when reading USART_DAT. Status flags are located in the USART_STS register.

The TXFIFO and RXFIFO thresholds that trigger TX and RX interrupts can be configured. These thresholds are programmed through the RXFTCFG and TXFTCFG bit fields in the USART_FIFO control register.

In this case: When the amount of data received in the RXFIFO reaches the threshold programmed in the RXFTCFG bit field, an Rx interrupt is generated. At this point, the RXFT flag in the USART_STS register is set to 1. This indicates that RXFTCFG data has been received: there is 1 data in USART_DAT and (RXFTCFG-1) data in RXFIFO. For example, if RXFTCFG is programmed as "101", the RXFT flag will be set to 1 when the corresponding amount of data is received (1 data in USART_DAT and (FIFO size-1) data in RXFIFO). Since the RX FIFO is not full, the next received data will not set the overflow flag to 1.

When the number of empty slots in the TXFIFO reaches the threshold programmed in the TXFTCFG bit field, a Tx interrupt is generated.

There are internal registers available to view the number of data entries in the TXFIFO/RXFIFO.

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Recommended configuration process for USART RX/TX FIFO:

1. Enable USART_FIFO.CLR to clear TX/RX FIFO data when in use, or operate on the USART_FIFO.CLR bit when wanting to clear FIFO data.
2. Configure interrupt enable: TX interrupt/RX interrupt.
3. Configure FIFO waterline thresholds: USART_FIFO.RXFTCFG/USART_FIFO.RXFTCFG (do not configure as 2'b00).
4. Enable the FIFO module by setting USART_FIFO.EN.

33.4.3 Transmitter

After the transmitter is enabled, the data in the transmit shift register is sent out through the TX pin.

33.4.3.1 Idle frame

Setting USART_CTRL1.TXEN will cause the USART to transmit an idle frame before the first data frame.

33.4.3.2 Character transmission

Idle frames are followed by characters sent. Each character is preceded by a low start bit. The transmitter sends 8-bit or 9-bit data according to the configuration of the data bit length, with the least significant bit first. If USART_CTRL1.TXEN is reset during a data transfer, it will cause the baud rate counter to stop counting and the data being transferred will be corrupted.

33.4.3.3 Stop bit

The characters are followed by stop bits, the number of which can be configured by setting USART_CTRL2. STPB[1:0].

Table 33-1 Stop Bit Configuration

USART_CTRL2.STPB[1:0]	Stop Bit Length (Bits)	Functional Description
00	1	default
01	0.5	Receiving in Smartcard mode
10	2	General USART mode, single-wire mode and modem mode.
11	1.5	Transmitting and receiving in Smartcard mode

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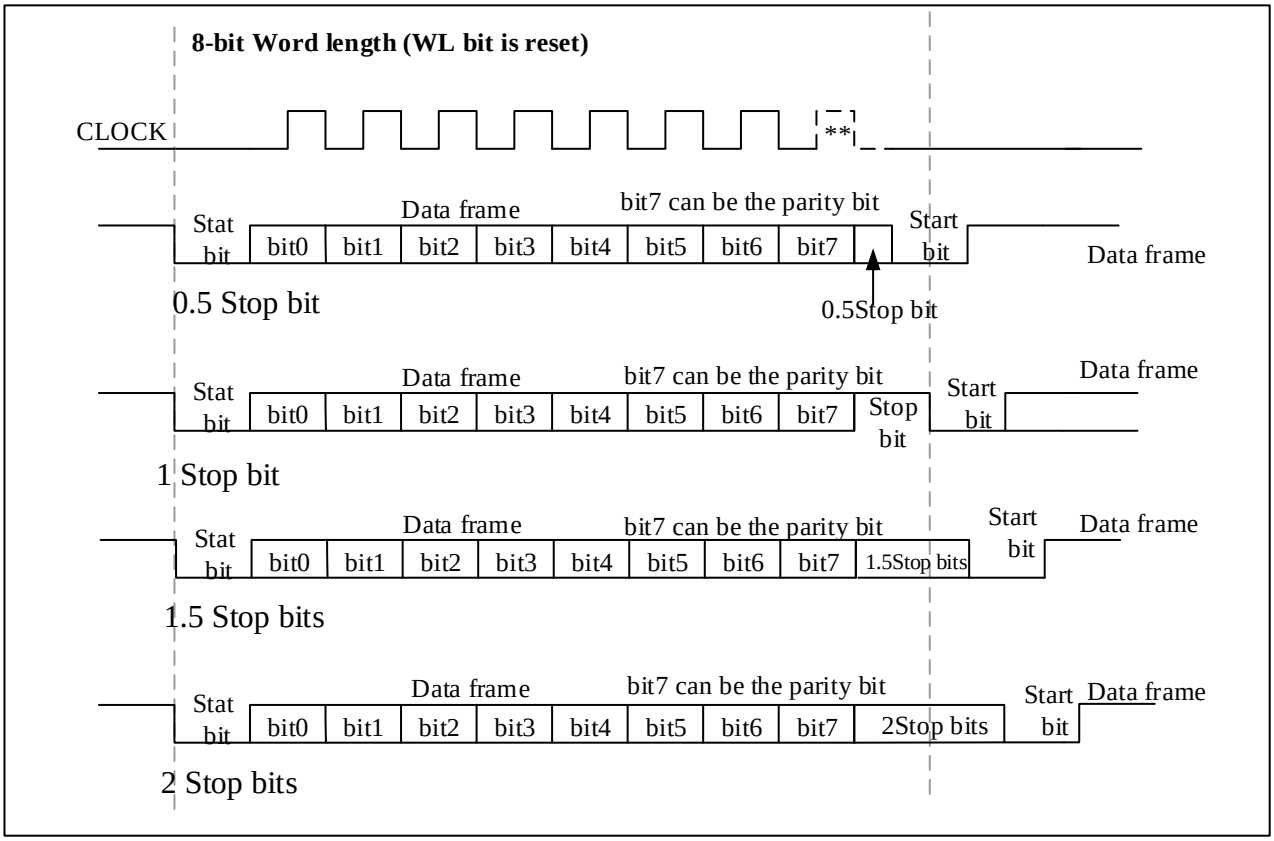
Figure 33-4 Configuration Stop Bit



33.4.3.4 Break frame

Use USART_CTRL1.SDBRK to send the break character. When there is 8-bit data, the break frame consists of 10 bits of low level, followed by a stop bit; when there is 9-bit data, the break frame consists of 11 bits of low level, followed by a stop bit.

After the break frame is sent, USART_CTRL1.SDBRK is cleared by hardware, and the stop bit of the break frame is automatically sent. Therefore, to send a second break frame, USART_CTRL1.SDBRK should be set after the stop bit of the previous break frame has been sent.

If software resets the USART_CTRL1.SDBRK bit before starting to send the break frame, the break frame will not be sent.

33.4.3.5 Transmitter process

1. Enable USART_CTRL1.UEN to activate USART;
2. Configure the transmitter's baud rate, data bit length, parity bit (optional), the number of stop bits or DMA configuration;
3. Activate the transmitter (USART_CTRL1.TXEN);
4. Send each data to be sent to the USART_DAT register through the CPU or DMA, and the write operation to the USART_DAT register will clear USART_STS.TXDE;
5. After writing the last data word in the USART_DAT register, wait for USART_STS.TXC =1, which indicates

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the end of the transmission of the last data frame.

33.4.3.6 Single Byte Communication

A write to the USART_DAT register clears the USART_STS.TXDE bit.

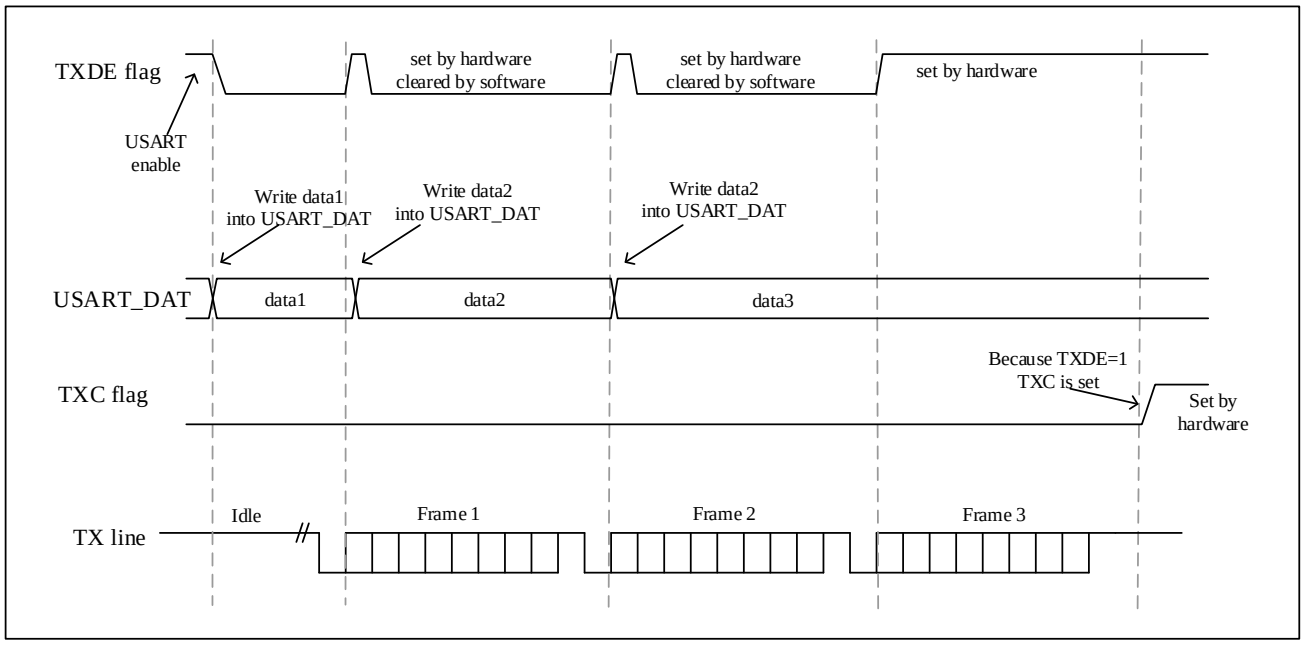
The USART_STS.TXDE bit is set by hardware when the data in the USART_DAT register is transferred to the transmit shift register (indicating that data is being transmitted). An interrupt will be generated if USART_CTRL1.TXDEIEN is set. At this point, the next data can be sent to the USART_DAT register because the USART_DAT register has been cleared and will not overwrite the previous data.

Write operation to USART_DAT register:

- When the transmit shift register is not sending data and is in an idle state, the data is directly put into the shift register for transmission, and the USART_STS.TXDE bit is set by hardware;
- When the transmit shift register is sending data, the data is stored in the USART_DAT register, and after the current transmission is completed, the data is put into the shift register.

When a frame containing data is sent and USART_STS.TXDE=1, the USART_STS.TXC bit is set to '1' by hardware. An interrupt is generated if USART_CTRL1.TXCIEN is '1'. USART_STS.TXC bit is cleared by a software sequence (read USART_STS register first, then write USART_DAT register).

Figure 33-5 TXC/TXDE Changes During Transmission



33.4.4 Receiver

33.4.4.1 Start bit detection

When the received sampling sequence is: 1 1 1 0 X 0 X 0 X 0 0 0 0, it is considered that a start bit is detected.

The samples at the 3rd, 5th, and 7th bits, and the samples at the 8th, 9th, and 10th bits are all '0' (that is, 6 '0'), then confirm the receipt of the start bit, the USART_STS.RXDNE flag bit is set, and if USART_CTRL1.RXDNEIEN=1,

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an interruption occurs and will not Set the NEF noise flag.

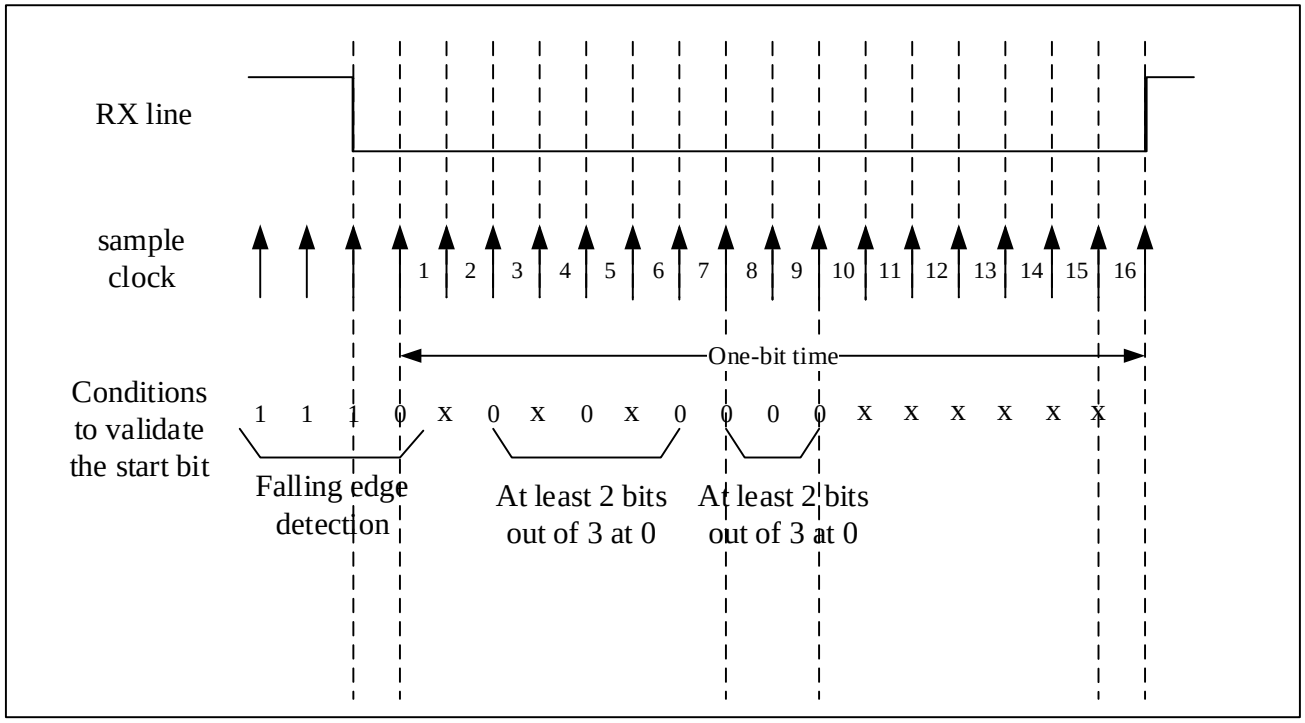
If there are six ‘0’ samples at the 3rd, 5th, 7th bits, and at the 8th, 9th, 10th bits, a start bit is confirmed to have been received, and USART_STS.RXDNE is set to 1, but the NEF noise flag will not be set. If USART_CTRL1.RXDNEIEN has been set to 1, an interrupt will be generated.

If there are two '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are two '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, but the NEF noise flag will be set.

If there are three '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are two '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, and the NEF noise flag will be set.

If there are two '0' samples at the 3rd, 5th, 7th bits, and at the same time, there are three '0' samples at the 8th, 9th, 10th bits, a start bit is also confirmed to have been received, and the NEF noise flag will be set.

Figure 33-6 Start Bit Detection



33.4.4.2 Stop bit description

During data reception, the number of data stop bits can be configured by the USART_CTRL2.STPB[1:0]. In normal mode, 1 or 2 stop bits can be selected. In Smartcard mode, 0.5 or 1.5 stop bits can be selected.

1. 0.5 stop bits (receive in smartcard mode): 0.5 stop bits are not sampled. Therefore, if 0.5 stop bits is selected, framing errors and broken frames cannot be detected.
2. 1 stop bit: sampling for 1 stop bit is done on the 8th, 9th and 10th samples.
3. 1.5 stop bits (Smartcard mode): when transmitting in Smartcard mode, the device must check whether the data is sent correctly. So the receiver function block must be activated (USART_CTRL1.RXEN=1) and sample the signal on the data line during the transmission of the stop bit. If a parity error occurs, the smartcard will pull down the data line when the transmitter samples the NACK signal, that is, within the time corresponding to the stop bit on the bus, indicating that a framing error has occurred. The USART_STS.FEF is set together with the

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USART_STS.RXDNE at the end of the 1.5th stop bit. The 1.5 stop bits are sampled at points 16, 17 and 18. The 1.5 stop bits can be divided into two parts: one is 0.5 clock cycles, during which nothing happens. This is followed by the stop bit of 1 clock cycle, which is sampled at the midpoint of this period of time. For details, see 33.4.17 Smartcard mode.

4. 2 stop bits: the sampling of the 2 stop bits is completed at the 8th, 9th and 10th sampling points of the first stop position. If a frame error is detected during the first stop bit, the frame error flag is set. The second stop bit does not detect framing error. The USART_STS.RXDNE flag will be set at the end of the first stop bit.

33.4.4.3 Receiver process

1. Enable USART_CTRL1.UEN to activate USART;
2. Configure the receiver's baud rate, data bit length, parity bit (optional), stop bit number or DMA configuration;
3. Activate the receiver (USART_CTRL1.RXEN) and start looking for the start bit;
4. The receiver receives 8-bit or 9-bit data according to the configuration of the data bit length, and the least significant bit of the data is first shifted from the RX pin into the receive shift register;
5. When the data of the received shift register is moved to the USART_DAT register, USART_STS.RXDNE is set, and the data can be read out. If USART_CTRL1.RXDNEIEN is 1, an interrupt will be generated;
6. When an overflow error, noise error, or frame error is detected in the received frame, the corresponding error flag status bit will be set. If USART_CTRL1.RXEN is reset during data transmission, the data being received will be lost;
7. USART_STS.RXDNE is set after receiving data, and a read operation of USART_DAT can clear this bit:

- During multi-buffer communication, the data register is cleared by the DMA read operation;
- During single-buffer communication, it is cleared by software reading the USART_DAT register.

33.4.4.4 Idle frame detection

The receiver of the USART can detect idle frames. An interrupt is generated if USART_CTRL1.IDLEIEN is '1'. USART_STS.IDLEF bit is cleared by a software sequence (read USART_STS register first, then read USART_DAT register).

33.4.4.5 Break frame detection

The frame error flag(USART_STS.FEF) is set by hardware when the receiver detects a break frame. It can be cleared by a software sequence (read USART_STS register first, then read USART_DAT register).

33.4.4.6 Framing error

A framing error occurs when a stop bit is not received and recognized at the expected time. At this time, the frame error flag USART_STS.FEF will be set by hardware, and the invalid data will be transferred from the shift register to the USART_DAT register. During single-byte communication, no interrupt framing error will be generated because it occurs with USART_STS.RXDNE and the hardware will generate an interrupt when the USART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt will be generated if the USART_CTRL3.ERRIEN bit is set.

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33.4.4.7 Overrun error

In non-FIFO mode: If USART_STS.RXDNE is set to 1 and there is data in the receive shift register that needs to be transferred to the data register, an overflow error occurs, and the USART_STS.OREF flag is set to 1.

In FIFO mode: If the RX FIFO is full and there is data in the receive shift register that needs to be transferred to the data register, an overflow error occurs, and the USART_STS.OREF flag is set to 1. The data in the data register will not be lost in this case, but the data in the shift register will be overwritten.

The USART_STS.OREF flag can be cleared through the following software operation: first read the USART_STS register, then read the USART_DAT register. When an overflow error occurs and USART_CTRL1.RXDNEIEN is set to 1, a receive interrupt will be generated. In multi-buffer communication mode (DMA), if USART_CTRL3.ERRIEN is set to 1, an error interrupt will be generated.

33.4.4.8 Noise error

USART_STS.NEF is set by hardware when noise is detected on a received frame. It is cleared by software sequence (read USART_STS register first, then write USART_DAT register). During single-byte communication, no noise interrupt generated because it occurs with USART_STS.RXDNE and the hardware will generate an interrupt when the USART_STS.RXDNE flag is set. In multi-buffer communication mode(DMA), an interrupt is generated when the USART_STS.NEF flag is set if the USART_CTRL3.ERRIEN bit is set.

Table 33-2 Data Sampling for Noise Detection

Sample value	NE status	Received bits	Data validity
000	0	0	Effective
001	1	0	be invalid
010	1	0	be invalid
011	1	1	be invalid
100	1	0	be invalid
101	1	1	be invalid
110	1	1	be invalid
111	0	1	Effective

33.4.5 Fractional Baud Rate Calculation

The baud rate is configured through the USART_BRCF register, which consists of integer and fractional parts of the divisor and is applicable to both the transmitter and receiver. After writing to the USART_BRCF register, the baud rate counter will be replaced by the new value of the baud rate register. Therefore, do not change the value of the baud rate register during communication.

Oversampling set to 8:

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$$\text{TX / RX baud rate} = f_{PCLK} / (8 * \text{USARTDIV})$$

Oversampling set to 16:

$$\text{TX / RX baud rate} = f_{PCLK} / (16 * \text{USARTDIV})$$

where f_{PCLK} is the clock provided to the peripheral:

- HCLK is used for USART1~USART2, up to 300MHz
- PCLK1 is used for USART3~USART4, UART9~UART12, up to 150MHz
- PCLK2 is used for USART5~USART8, UART13~UART15, up to 150MHz.

USARTDIV is an unsigned fixed-point number.

33.4.5.1 USARTDIV and USART_BRCF register configuration

Oversampling set to 16:

Example 1:

If USARTDIV = 27.75, then:

DIVDEC = 16*0.75 = 12 = 0x0C

DIVINT = 27=0x1B

So USART_BRCF = 0x1BC

Example 2:

If USARTDIV = 20.98, then:

DIVDEC = 16*0.98 = 15.68

Nearest integer: DIVDEC = 16 = 0x10, out of configurable range, so a carry to integer is required

So DIVINT = 20+1 = 21 = 0x15

DIVDEC = 0x0

So USART_BRCF = 0x150

Example 3:

If USART_BRCF = 0x19B：

DIVINT = 0x19 = 25

DIVDEC = 0x0B = 11

So USARTDIV = 25+11/16 = 25.6875

Oversampling set to 8:

Example 1:

If USARTDIV = 27.75, then:

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DIVDEC = 8*0.75 = 6 = 0x06

DIVINT = 27=0x1B

So USART_BRCF = 0x1B6

Example 2:

If USARTDIV = 20.98, then:

DIVDEC = 8*0.98 = 7.84

Nearest integer: DIVDEC = 8 = 0x08, out of configurable range, so a carry to integer is required

So DIVINT = 20+1 = 21 = 0x15

DIVDEC = 0x0

So USART_BRCF = 0x150

Example 3:

If USART_BRCF = 0x196：

DIVINT = 0x19 = 25

DIVDEC = 0x06 = 6

USARTDIV = 25+6/8 = 25.75

Table 33-3 Error Calculation When Setting Baud Rate

16x oversampling（USART_CTRL1.OSPM = 0）									
Baud rate		**f_{PCLK}=150MHz**				**f_{PCLK}=300MHz**			
serial number	Kbps	reality	Oversampling value	Set value in register	Error(%)	reality	Oversampling value	Set value in register	Error(%)
1	2.4	2.4	16	3906.25	0%	2.4	16	7812.5	0%
2	9.6	9.6	16	976.5625	0%	9.6	16	1953.125	0%
3	19.2	19.19	16	488.3125	0.05%	19.2	16	976.5625	0%
4	57.6	57.6	16	162.75	0%	57.603	16	325.5	0%
5	115.2	115.2	16	81.375	0%	115.207	16	162.75	0%
6	230.4	230.41	16	40.6875	0%	230.41	16	81.375	0.06%

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						4			
7	460.8	460.12	16	20.375	1.6%	460.82	16	40.6875	0.04%
8	921.6	920.2	16	10.1875	0.15%	920.24	16	20.375	0.15%
9	7500	7500	16	1.25	0%	7500	16	2.5	0%
10	15000	impossible	16	impossible	impossible	15000	16	1.25	0%
11	30000	impossible	16	impossible	impossible	30000	16	impossible	impossible

Table 33-4 Error Calculation When Setting Baud Rate

8x oversampling（USART_CTRL1.OSPM = 1）									
Baud rate		**f_{PCLK}=150MHz**				**f_{PCLK}=300MHz**			
serial number	Kbps	reality	Oversampling value	Set value in register	Error(%)	reality	Oversampling value	Set value in register	Error(%)
1	2.4	2.4	8	impossible	impossible	2.4	8	impossible	impossible
2	9.6	9.6	8	1953.125	0%	9.6	8	3906.25	0%
3	19.2	19.198	8	976.625	0.1%	19.2	8	1953.125	0%
4	57.6	57.603	8	325.5	0.005%	57.598	8	651.0625	0.03%
5	115.2	115.207	8	162.75	0.006%	115.207	8	325.5	0.006%
6	230.4	230.414	8	81.375	0.006%	230.414	8	162.75	0.006%
7	460.8	460.122	8	40.75	0.14%	460.122	8	81.5	0.14%
8	921.6	920.24	8	20.375	0.14%	923.076	8	40.625	0.16%

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9	7500	7500	8	2.5	0%	7500	8	5	0%
10	15000	15000	8	1.25	0%	15000	8	2.5	0%
11	30000	15000	8	impossible	impossible	30000	8	1.25	0%

Note: The lower the CPU clock frequency, the lower the error for a specific baud rate.

33.4.6 USART Receiver Tolerance to Clock Variations

In the application, there may be transmission errors (including changes in the transmitter clock), receiver baud rate errors and oscillator variations, and changes in transmission lines (usually caused by inconsistent data rising and falling edge timing). These factors will all affect the overall clock system variations. Only when the sum of the above four variations is less than the tolerance of the USART receiver, can the USART asynchronous receiver work properly.

During normal data reception, the tolerance of the USART receiver is the maximum allowable variation, depending on the choice of data bit length and whether fractional baud rate divider is used.

Table 33-5 When DIVDEC = 0, the tolerance of the USART receiver

WL bit	PCEN bit	Considering NEF as an error	Not considering NEF as an error
0	0	3.75%	4.375%
1	0	3.41%	3.97%
0	1	2.5%	3.75%
1	1	2.27%	3.41%

Table 33-6 When DIVDEC != 0, the tolerance of the USART receiver

WL bit	PCEN bit	Considering NEF as an error	Not considering NEF as an error
0	0	3.33%	4.0%
1	0	3.03%	3.63%
0	1	1.25%	2.5%
1	1	1.13%	2.27%

33.4.7 Parity Control

Parity can be enabled by configuring the USART_CTRL1.PCEN bit.

When the parity bit is enabled for transmission, a parity bit is generated, parity check is performed on reception.

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Table 33-7 Frame Format

WL bit	PCEN bit	USART frame
0	0	| Start bit | 8-bit data | Stop bit |
0	1	| Start bit | 7 bits of data | Parity bit | Stop bit |
1	0	| Start bit | 9-bit data | Stop bit |
1	1	| start bit | 8-bit data | parity bit | stop bit |

Even parity

Configure USART_CTRL1.PSEL to 0, and even parity can be selected.

Make the number of '1' in the transmitted data (including parity bit) be an even number. For example: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total). The receiver confirms the number of '1's in the data. If it is an even number, the check is passed, indicating that no errors occurred during the transmission process. If it is not even, it means that an error has occurred, the USART_STS.PEF flag is set to '1', and if USART_CTRL1.PEIEN is enabled, an interrupt is generated.

Odd parity

Configure USART_CTRL1.PSEL to 1, you can choose odd parity.

Make the number of '1' in the transmitted data (including parity bit) be an odd number. For example: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total). The receiver confirms the number of '1's in the data If it is an odd number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an odd number, it means that an error has occurred, the USART_STS.PEF flag is set to '1', and if USART_CTRL1.PEIEN is enabled, an interrupt is generated.

33.4.8 DMA Communication

The USART supports the DMA mode using multi-buffer configuration, which can realize high-speed data communication.

33.4.8.1 DMA transmission

Set USART_CTRL3.DMATXEN to enable DMA mode when transmitting. When the USART's transmit shift register is empty (USART_STS.TXDE=1), the DMA will transfer the data from the SRAM to the USART_DAT register of the USART.

When using DMA transmission, the process of configuring the DMA channel is as follows:

1. Set the address of the data memory. When a data transfer request occurs, the transferred data will be read from this address.
2. Set the address of the USART_DAT register. When a data transfer request occurs, this address will be the destination address of the data transfer.
3. Set the amount of data to transfer.

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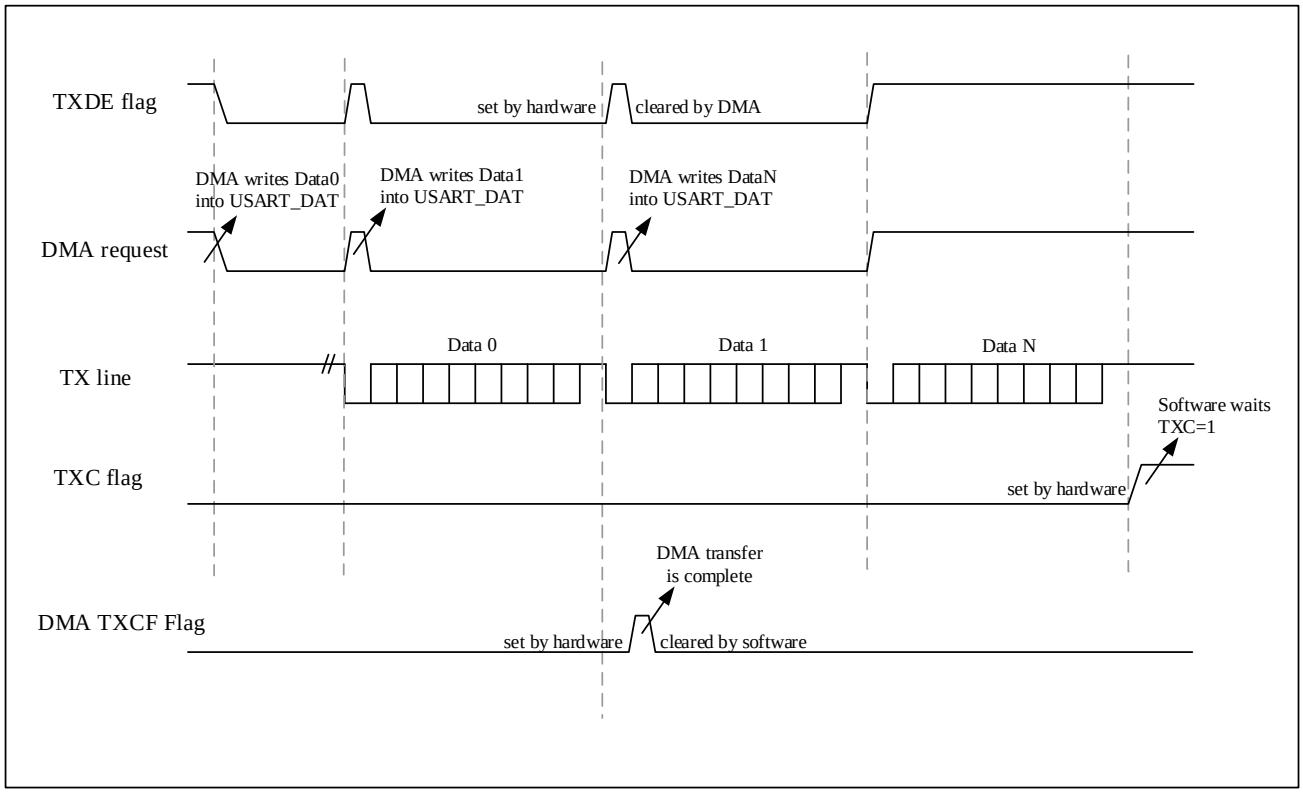
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the current DMA channel.
6. After the data transfer is completed, the transfer complete flag (DMA_TCINTSTS. CHn) is set to 1.

Figure 33-7 DMA Transmission



33.4.8.2 DMA reception

Set USART_CTRL3.DMARXEN to enable DMA mode when receiving. When a byte is received (USART_STS.RXDNE=1), the DMA will transfer the data from the USART_DAT register of the USART to the SRAM.

When using DMA reception, the process of configuring the DMA channel is as follows:

1. Set the address of the USART_DAT register. When a data transfer request occurs, this address will be the source address of the data transfer.
2. Set the address of the data memory. When a data transfer request occurs, the transferred data will be written to this address.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the current DMA channel.

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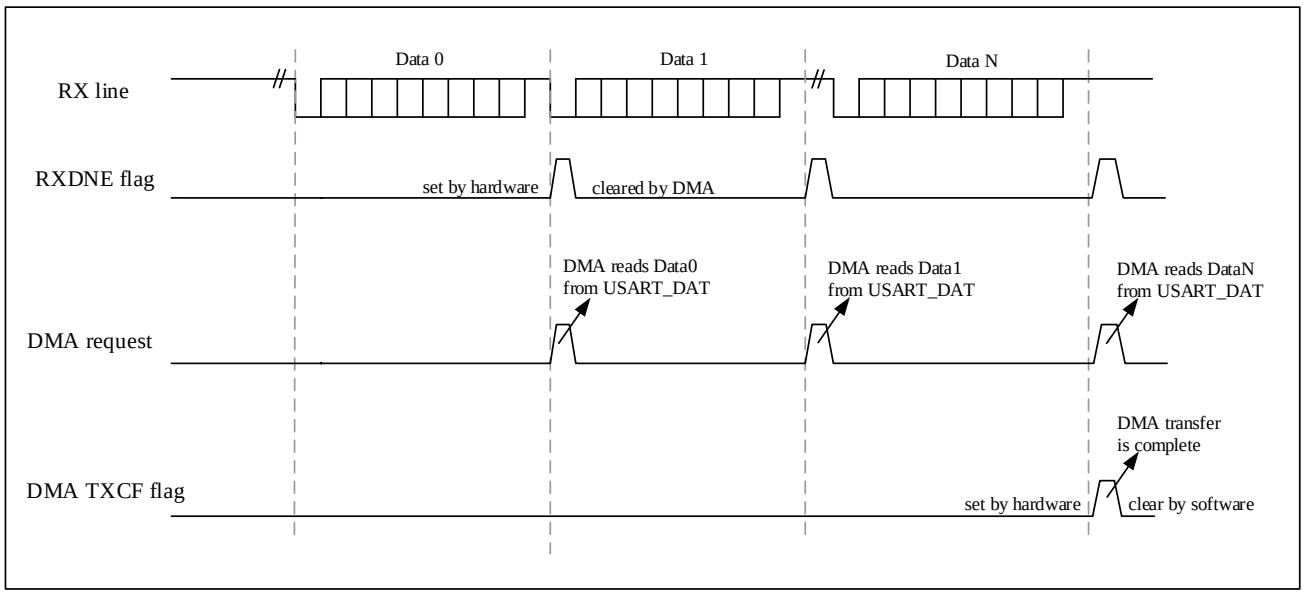
Figure 33-8 DMA Reception

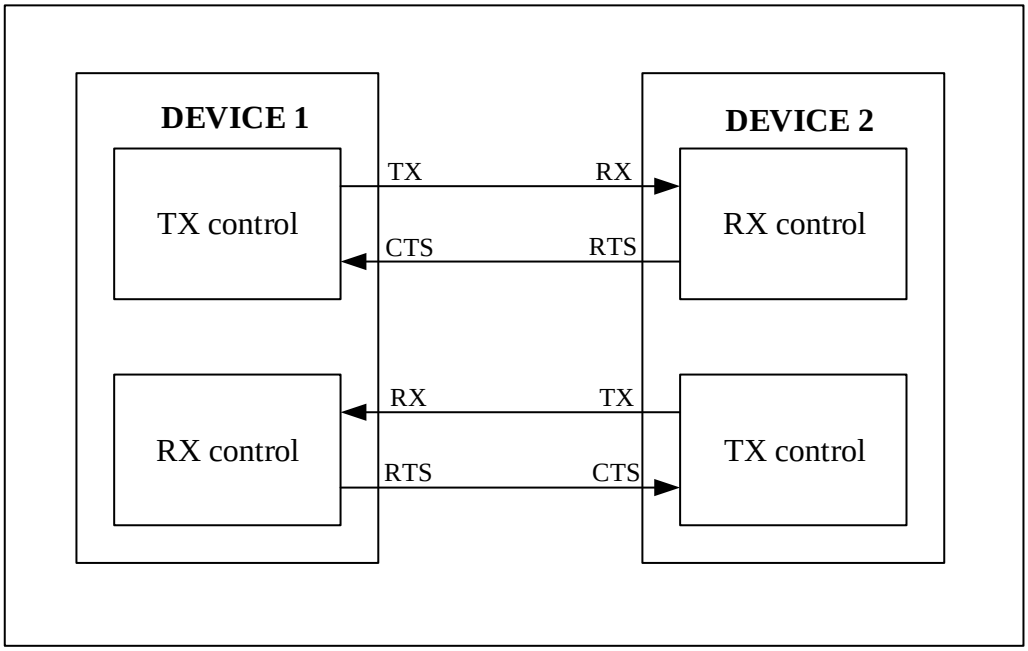


In multi-buffer communication mode, the error flag will be set when there is a frame error, overrun or noise error. An interrupt will be generated if the error interrupt is enabled (USART_CTRL3.ERRIEN=1).

33.4.9 Hardware Flow Control

USART supports hardware flow control. The purpose is to coordinate the transmitting and receiving parties so that the data will not be lost. The connection method is shown in the following figure.

Figure 33-9 Hardware Flow Control Between Two USART



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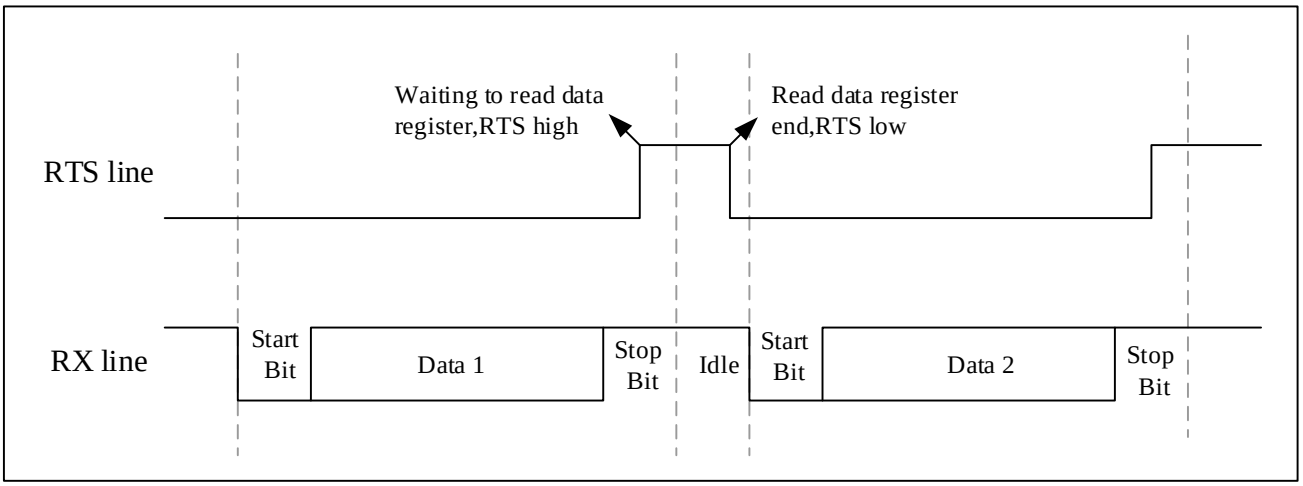
33.4.9.1 RTS flow control

Set USART_CTRL3.RTSEN to enable RTS. RTS is the output signal used to indicate that the receiver is ready. When data arrives in RDR, nRTS is asserted, notifying the sender to stop data transmission at the end of the current frame. When receiver is ready to receive new data, nRTS is deasserted.

Figure 33-10 RTS Flow Control



33.4.9.2 CTS flow control

Set USART_CTRL3.CTSEN to enable CTS. CTS is an input signal, used to judge whether data can be sent to the other device. The low level is valid, and the low level indicates that the device can send data to the other device. If the nCTS signal becomes invalid during data transmission, the transmission will stop after sending the data. If you write data to the data register when nCTS is invalid, the data will not be sent until nCTS is valid.

If the USART_CTRL3.CTSEN bit is set, the USART_STS.CTSF bit will be set high by hardware when the nCTS input changes state. An interrupt will be generated if USART_CTRL3.CTSIEN is enabled.

Figure 33-11 CTS CTS Flow Controls

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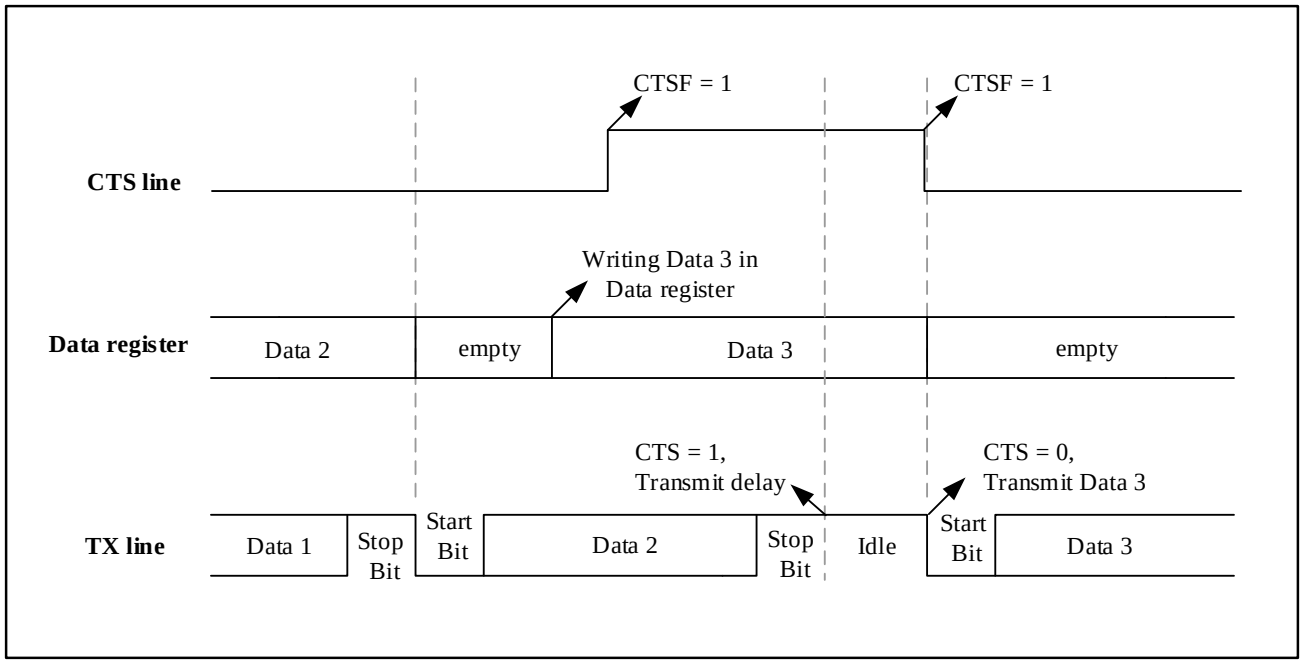

33.4.10 Multiprocessor Communication

USART allows multiprocessor communication. When multiple processors communicate through USART, it is necessary to determine who is the master device, and the remaining processors are all slave devices. The TX output of the master device is directly connected to the RX port of all slave device. The TX outputs of the slaves are logically AND together and connected to the RX inputs of the master.

When multi-processor communication is performed, the slave devices are all in mute mode, and the host uses a specific method to wake up a slave device to be communicated when needed, so that the slave device is in an active state and transmits data with the master device.

The USART can wake up from mute mode by idle line detection or address mark detection.

33.4.10.1 Idle line detection

The idle line detection configuration process is as follows:

1. Configure the USART_CTRL1.WUM bit to 0, and the USART performs idle line detection;
2. When USART_CTRL1.RCVWU is set (which can be automatically controlled by hardware or written by software under certain conditions), USART enters mute mode. In mute mode, none of the receive status bits are set, and all receive interrupts are disabled;
3. As shown in the Figure 33-12 below, when an idle frame is detected, USART is woken up, and then USART_CTRL1.RCVWU is cleared by hardware. At this time, USART_STS.IDLEF is not set.

Figure 33-12 Mute Mode Using Idle Line Detection

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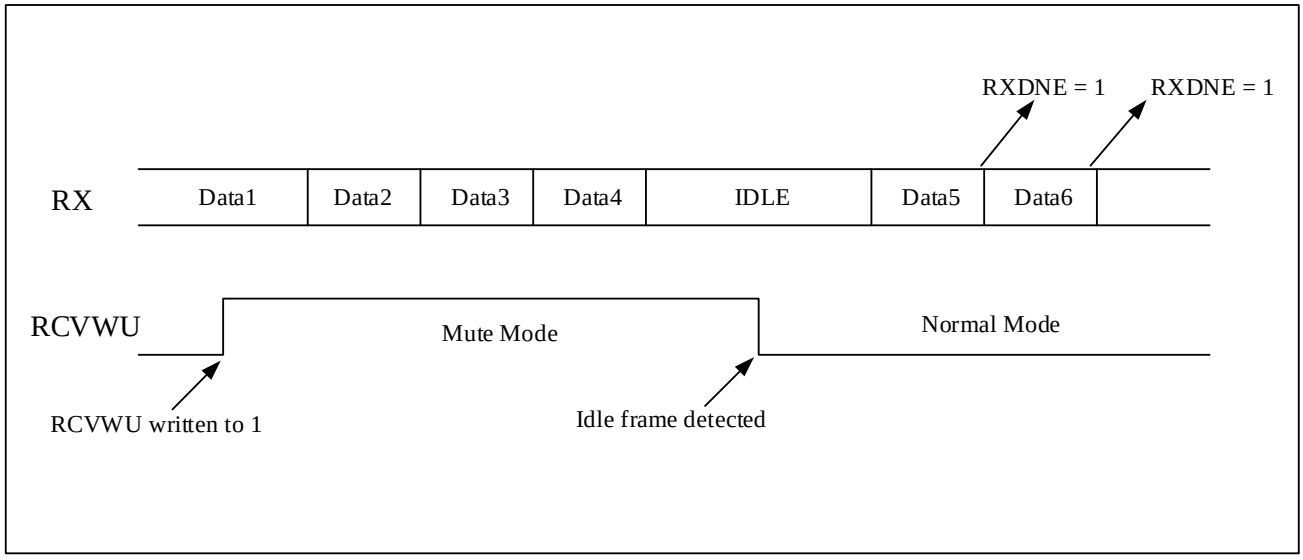

33.4.10.2 Address mark detection

By configuring the USART_CTRL1.WUM bit to 1, the USART performs address mark detection. The address of the receiver is programmable through the USART_CTRL2.ADDR[3:0] bits. If the MSB is 1, the byte is considered as an address, otherwise it is considered as data.

In this mode, the USART can enter mute mode by:

- When the receiver does not contain data, USART_CTRL1.RCVWU can be written to 1 by software, and USART enters mute mode;

  Note: When the receive buffer contains no data (RXNE=0 in USART_SR), the USART_CTRL1.RCVWU bit can be written to 0 or 1. Otherwise, the write operation is ignored.

- When the received address does not match the address of the USART_CTRL2.ADDR[3:0] bits, USART_CTRL1.RCVWU is written to 1 by hardware.

In mute mode, none of the receive status bits are set and all receive interrupts are disabled.

When the received address matches the address of the USART_CTRL2.ADDR[3:0] bits, the USART is woken up and USART_CTRL1.RCVWU is cleared. The USART_STS.RXDNE bit will be set when this matching address is received. Data can then be transmitted normally.

Figure 33-13 Mute Mode Detected Using Address Mark

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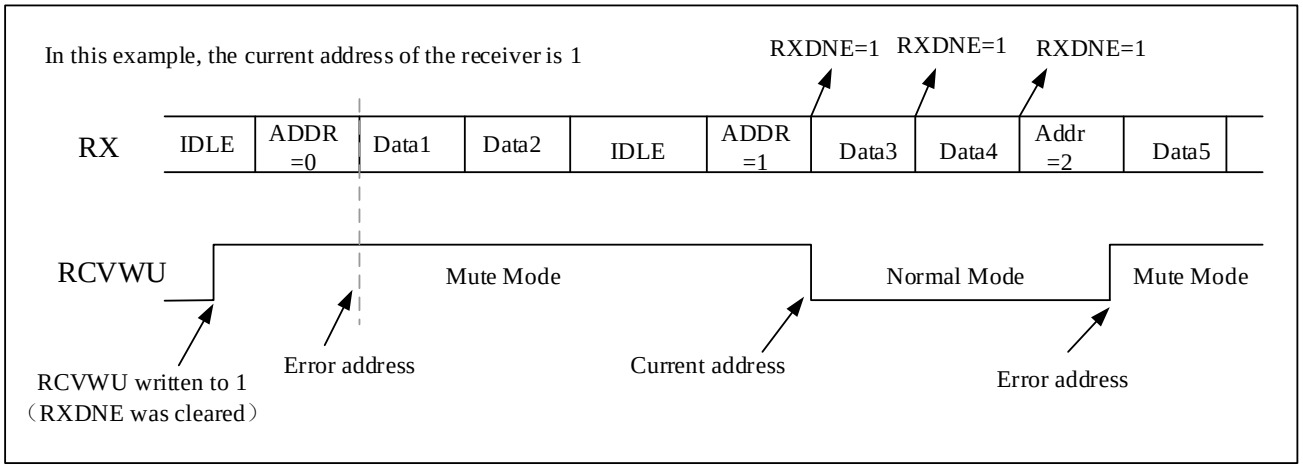

33.4.11 Synchronous Mode

USART supports synchronous serial communication. The USART only supports the master mode, and cannot use the input clock from other devices to receive and transmit data. Synchronous mode can be enabled by configuring the USART_CTRL2.CLKEN bit.

Note: When using synchronous mode, USART_CTRL2.LINMEN, USART_CTRL3.SCMEN, USART_CTRL3.HDMEN, USART_CTRL3. IRDAMEN, these bits need to be kept clear.

33.4.11.1 Synchronized clock

The CK pin is the output of the USART transmitter clock. During the bus idle period, before the actual data arrives and when the break symbol is sent, the clock not output.

Clock phase and polarity are software programmable and need to be configured when both the transmitter and receiver are disabled. When the clock polarity is 0 (USART_CTRL2.CLKPOL=0), the default level of CLK is low; when the clock polarity is 1 (USART_CTRL2.CLKPOL=1), the default level of CLK is high. When the phase polarity is 0 (USART_CTRL2.CLKPHA=0), the data is sampled on the first edge of the clock; when the phase polarity is 1 (USART_CTRL2.CLKPHA=1), the data is sampled on the second edge.

During the start and stop bits, the CK pin does not output clock pulses.

A sync data cannot be received when no data is sent. Because the clock is only available when the transmitter is activated and data is written to the USART_DAT register.

The USART_CTRL2.LBCLK bit controls whether to output the clock pulse corresponding to the last data byte (MSB) sent on the CK pin. This bit needs to be configured when both the transmitter and receiver are disabled. If USART_CTRL2.LBCLK is 1, the clock pulse of the last bit of data will be output from CK. If USART_CTRL2.LBCLK is 0, the clock pulse of the last bit of data is not output from CK.

33.4.11.2 Synchronous transmitting

The transmitter in synchronous mode works the same as in asynchronous mode. Data on the TX pin is sent out synchronously with CK.

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33.4.11.3 Synchronous receiving

The receiver in synchronous mode works differently than in asynchronous mode. Data is sampled on CK without any oversampling. But setup time and hold time (depending on baud rate, 1/16 bit time) must be considered.

Figure 33-14 USART Synchronous Transmission Example

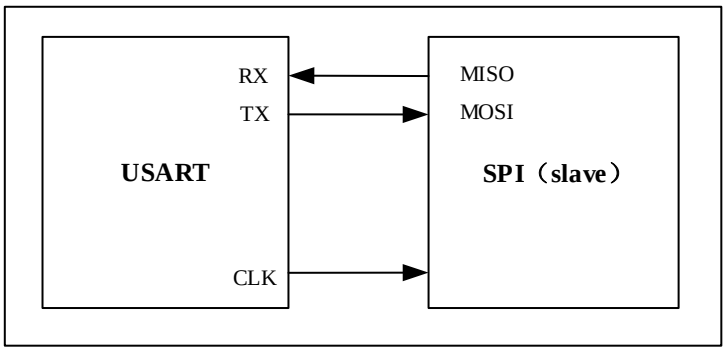

Figure 33-15 USART Data Clock Timing Example (WL=0)

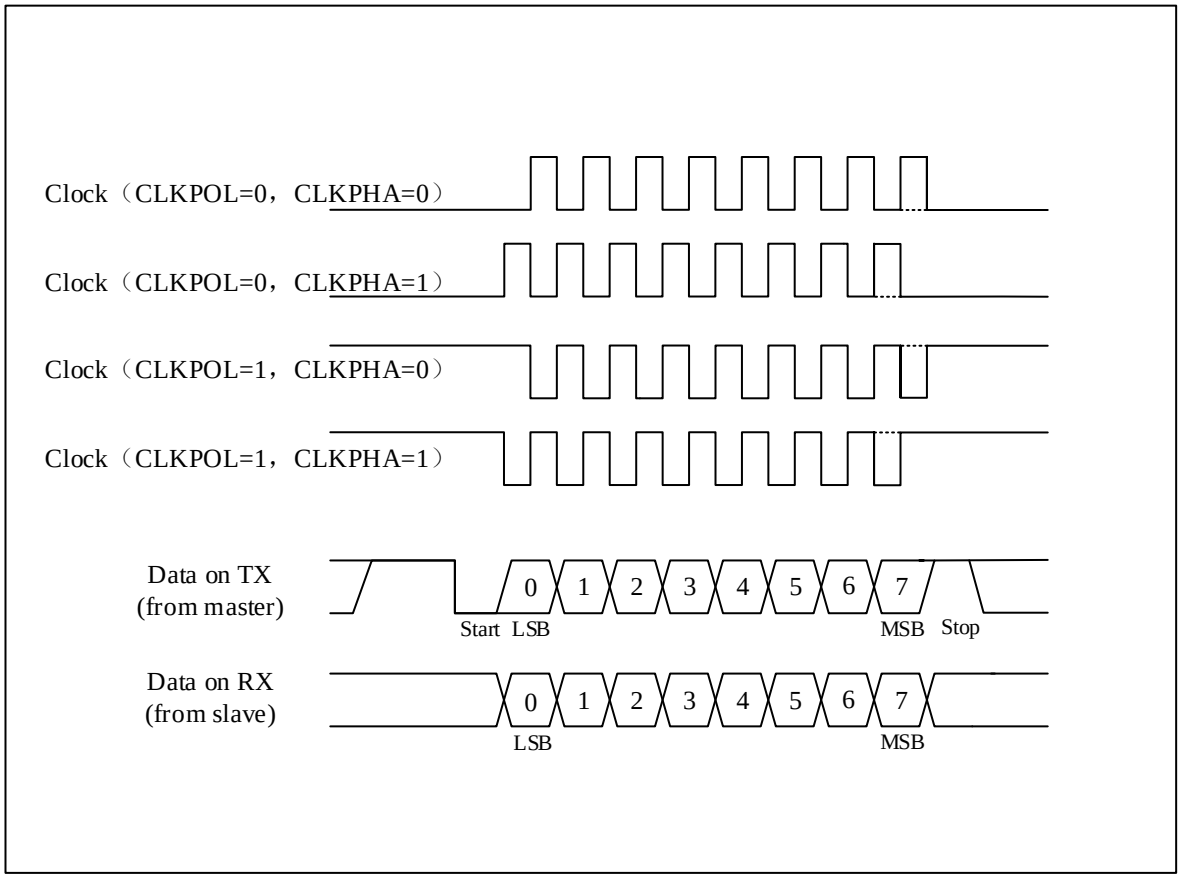

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Figure 33-16 USART Data Clock Timing Example (WL=1)

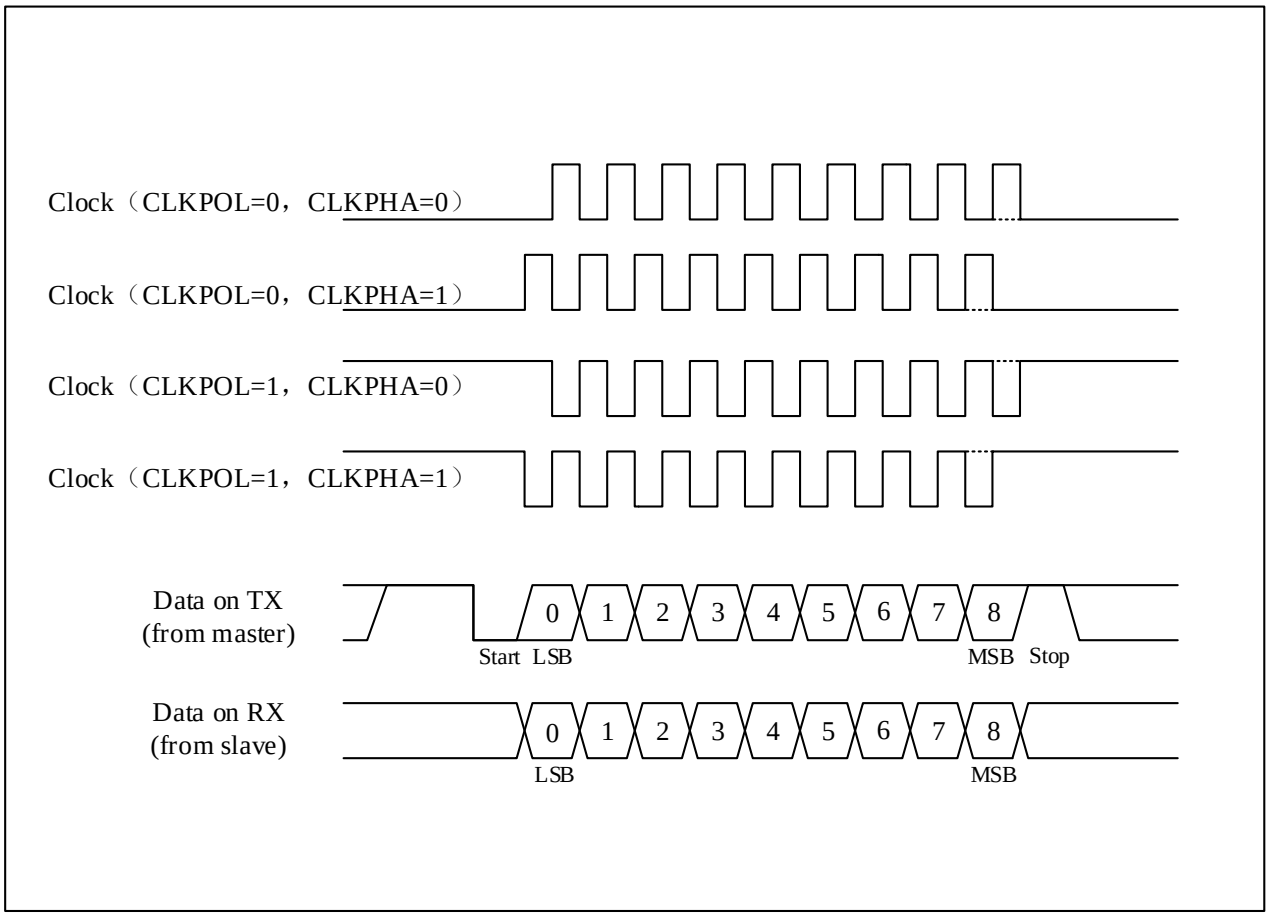
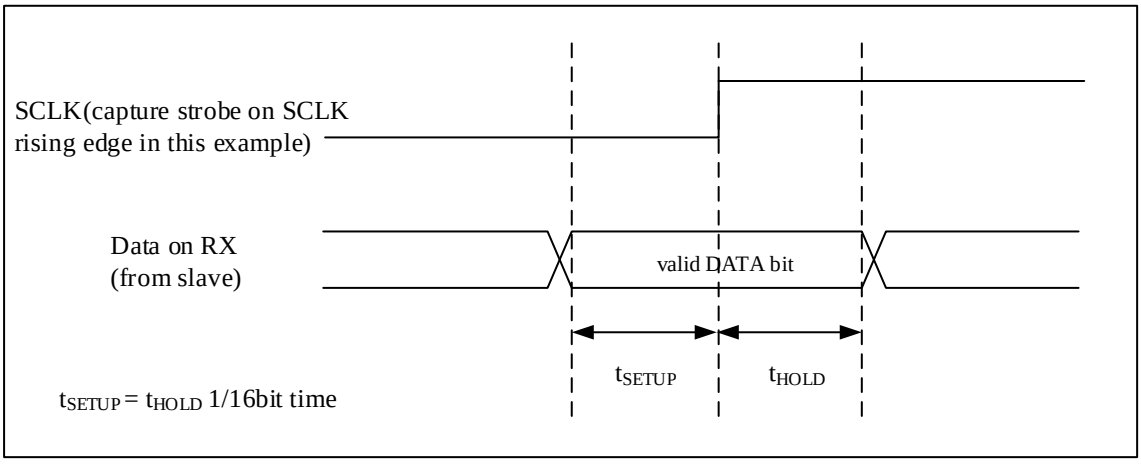


Figure 33-17 RX Data Sampling / Holding Time



Note: the function of CK is different in Smartcard mode, please refer to the Smartcard mode section for details.

33.4.12 Single-Wire Half-Duplex Mode

USART supports single-wire half-duplex communication, allowing data to be transmitted in both directions, but only allows data to be transmitted in one direction at the same time. Communication conflicts are managed by software.

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Through the USART_CTRL3.HDMEN bit, you can choose whether to enable half-duplex mode. When using single-wire half-duplex, USART_CTRL2.CLKEN,USART_CTRL2.LINMEN,USART_CTRL3.SCMEN, USART_CTRL3. IRDAMEN, these bits should be kept clear.

After the half-duplex mode is turned on, the TX pin and the RX pin are internally connected, and the RX pin is no longer used. When there is no data to be transmitted, TX is always released. Therefore, when not driven by the USART, the TX pin must be configured as a floating input or an open-drain output high.

33.4.13 Receiver Timeout

Receiver timeout function can be enabled by setting USART_CTRL2.RTOEN to 1.

The timeout interval is programmed through the USART_RTO.TIME field.

The receiver timeout counter starts counting following these rules: it begins counting from the end of the stop bit reception.

After the timeout interval elapses, the USART_STS.RTOF flag is set to 1. If USART_CTRL1.RTOIEN is set to 1, a timeout interrupt will be generated.

Note: After a receiver timeout, it is necessary to clear the timeout flag USART_STS.RTOF, otherwise, the timeout counting will not restart; after clearing the flag, the receiver timeout counting starts only after receiving the next data.

33.4.14 Data error discard function

USART has parity error flag (PEF), framing error flag (FEF), and noise error flag (NEF) for data checking on USART. Configuration of USART_CTRL2.PEFLOSE/FEFLOSE/NEFLOSE can be done on USART to check for data errors in the data written to the receive FIFO. If one of these errors occurs in the receive FIFO, the data will not be written into the FIFO. It is as if the data is directly discarded, and the USART_STS.PELOSEF/FELOSEF/NELOSEF three status bits indicate the occurrence of the respective errors in the previous data. This function is used under the condition of receiving data in FIFO mode.

Indicate error flag:

Set: Indicates the type of error that occurred when a data error occurs;

Clear: Write a 1 to USART_STS.PELOSEF/FELOSEF/NELOSEF to clear.

33.4.15 Serial IrDA Infrared Encoding/Decoding Mode

USART supports the IrDA (Infrared Data Association).

Through the USART_CTRL3. IRDAMEN bit, you can choose whether to enable the infrared mode. When using the infrared function, USART_CTRL2.CLKEN, USART_CTRL2.STPB[1:0], USART_CTRL2.LINMEN, USART_CTRL3.HDMEN, USART_CTRL3.SCMEN, these bits should be kept clear.

Through the USART_CTRL3. IRDALP bit, it can be used to select normal mode or low power infrared mode.

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33.4.15.1 IrDA normal mode

When USART_CTRL3.IRDALP=0, select normal infrared mode.

IrDA is a half-duplex communication protocol, so there should be a minimum delay of 10ms between sending and receiving.that uses a inverted return-to-zero modulation scheme (RZI), which uses an infrared light pulse to represent a logic '0', and the pulse width is specified as 3/16 of a bit period in normal mode, as shown in the Figure 33-19. USART only supports up to 115200bps.

The USART sends data to the SIR encoder, and the bit stream output by the USART will be modulated. A modulated stream of pulses is sent from the infrared transmitter and then received by the infrared receiver. The SIR receiver decoder demodulates it and outputs the data to the USART.

The transmit encoder output has opposite polarity to the decoder input. When idle, SIR transmit is low, while SIR receive is high. The high pulse sent by SIR is '0' and the low level is '1', while SIR reception is the opposite.

If the USART is sending data to the IrDA transmit encoder, then the IrDA receive decoder will ignore any data on the IrDA receive line. If the USART is receiving data sent from the SIR receiver decoder, the data sent by the USART to the IrDA transmitter encoder will not be encoded.

Pulse width is programmable. The IrDA specification requires pulses to be wider than 1.41us. For pulse widths less than 2 cycles, the receiver will filter them out. PSCV is the prescaler value programmed in the USART_GTP register.

33.4.15.2 IrDA low power mode

When USART_CTRL3.IRDALP=1, select low power infrared mode.

For the transmitter, when in low power mode, the pulse width is 3 times the low power baud rate, which is a minimum of 1.42MHz. Typically this value is 1.8432MHz (1.42 MHz < PSC < 2.12 MHz).

For the receiver, the requirement for a valid signal is that the duration of the low level signal must be greater than 2 cycles of the IrDA low power baud rate clock.

Figure 33-18 IrDA SIR ENDEC–Block Diagram

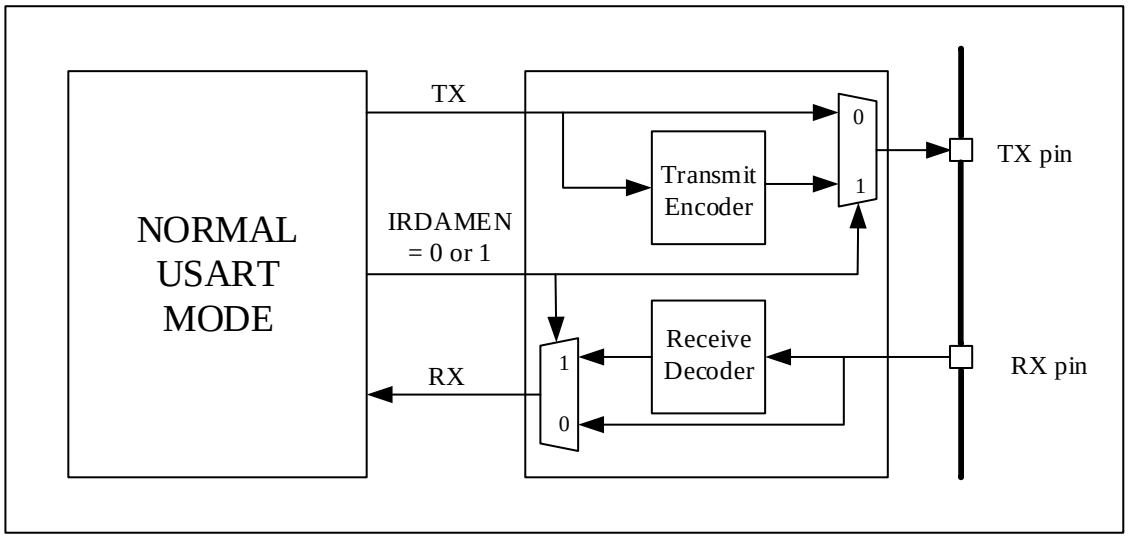

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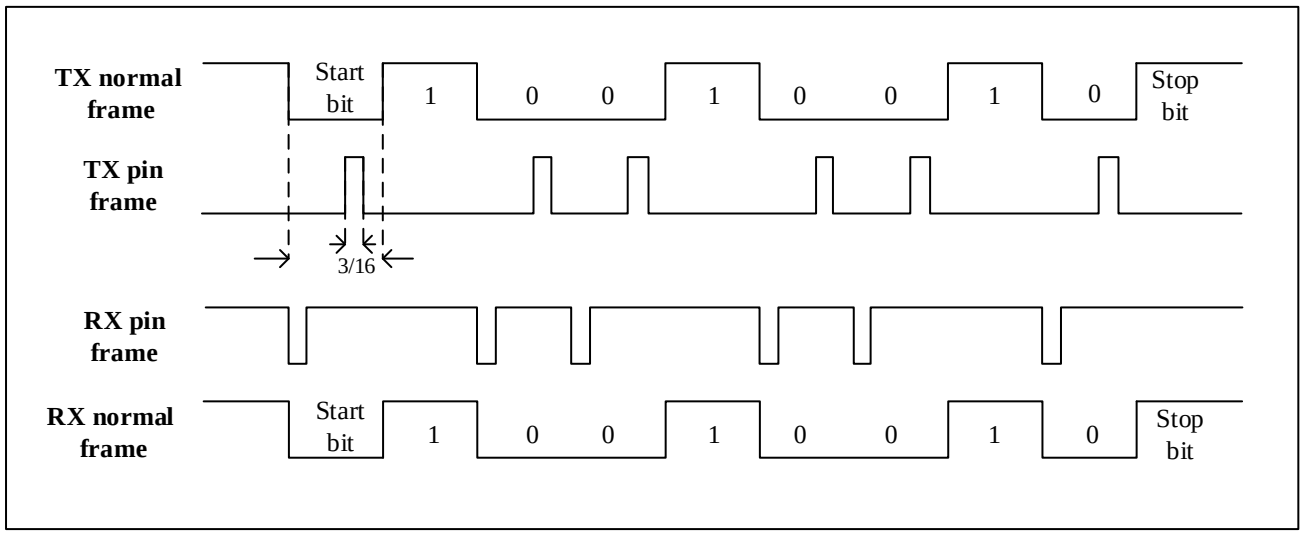
Figure 33-19 IrDA Data Modulation (3/16)-Normal Mode



33.4.16 LIN Mode

USART supports the ability of a LIN(Local interconnection Network) master to send a synchronization break and the ability of a LIN slave to detect a break. LIN mode can be enabled by configuring the USART_CTRL2.LINMEN bit.

Note: When using LIN mode, USART_CTRL2.STPB[1:0], USART_CTRL2.CLKEN, USART_CTRL3.SCMEN, USART_CTRL3.HDMEN, USART_CTRL3. IRDAMEN, these bits should be kept clear.

33.4.16.1 LIN transmission

When LIN is sent, the length of the data bits sent can only be 8 bits. By setting USART_CTRL1.SDBRK, a 13-bit '0' will be sent as the break symbol, and insert a stop bit.

33.4.16.2 LIN reception

Whether the bus is idle or during the transmission of a data frame, as long as the break frame appears, it can be detected. The break symbol detection is independent of the USART receiver.

By configuring the USART_CTRL2.LINBDL bit, 10-bit or 11-bit break character detection can be selected.

When the receiver detects the start bit, the circuit samples each subsequent bit at the 8th, 9th, and 10th oversampling clock points of each bit. When 10 or 11 consecutive bits are detected as '0' and followed by a delimiter, it means that a LIN break is detected, and USART_STS.LINBDF is set. Before confirming the break symbol, check the delimiter as it means the RX line has gone back to high level. An interrupt is generated if the LIN breaker detection interrupt (USART_CTRL2.LINBDIEN) is enabled.

If a '1' is sampled before the 10th or 11th sample point, the current detection is canceled and the start bit is searched again.

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Figure 33-20 LIN Break Detection In LIN Mode (11-bit break length-the LINBDL bit is set)

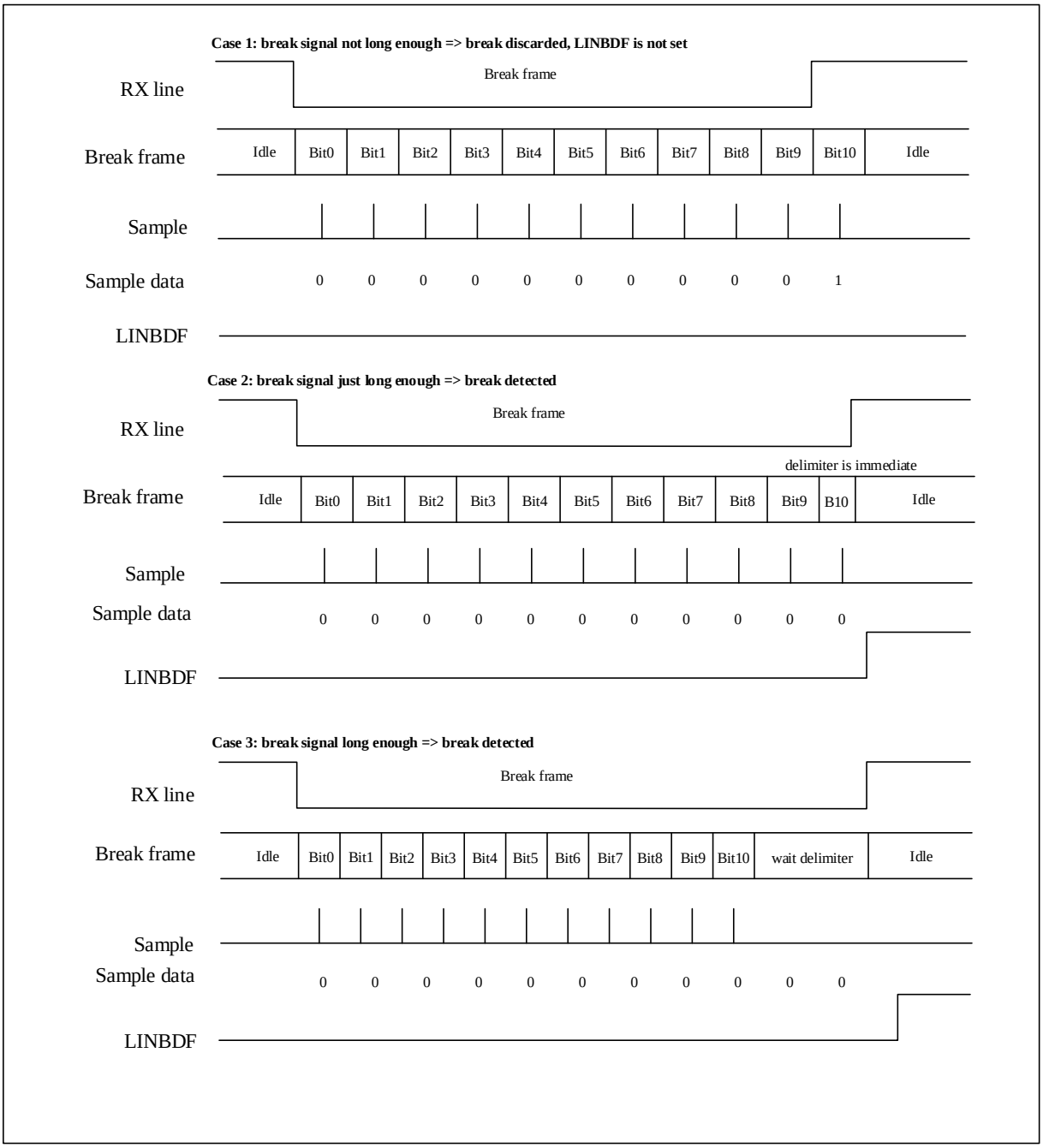

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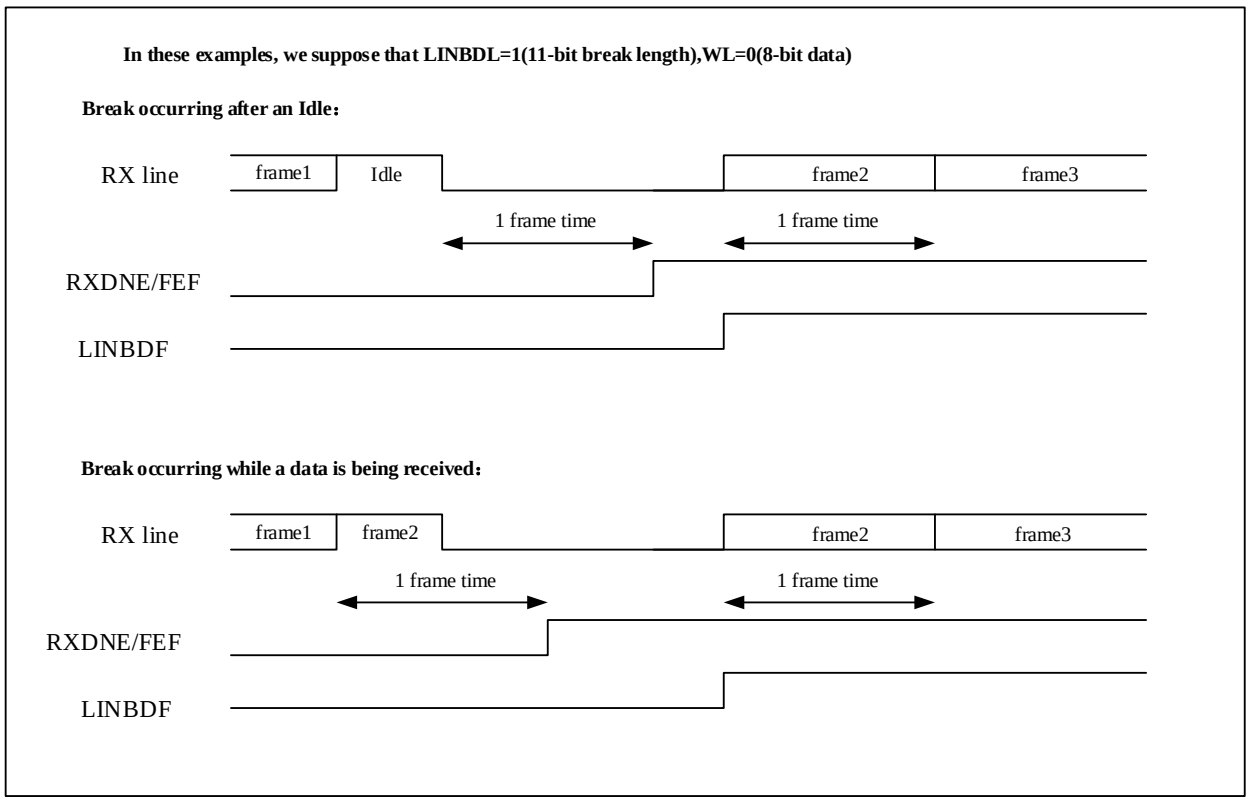
Figure 33-21 Break Detection And Framing Error Detection In LIN Mode



33.4.17 Smartcard Mode (ISO7816)

USART supports smartcard protocol. The smartcard interface supports the asynchronous smartcard protocol defined in the ISO7816-3 standard.

Through the USART_CTRL3.SCMEN bit, you can choose whether to enable smartcard mode. When using smartcard mode, USART_CTRL2.LINMEN, USART_CTRL3.HDMEN, USART_CTRL3.IRDAMEN, these bits should be kept clear.

In smartcard mode, the USART can provide a clock through the CK pin. The system clock is divided by the prescaler register to provide the clock to the smartcard. The CK frequency can be from $f_{CK}/2$ to $f_{CK}/62$, where f_{CK} is the peripheral input clock.

In smartcard mode, 0.5 and 1.5 stop bits can be used when receiving data, and only 1.5 stop bits can be used when transmitting data. So 1.5 stop bits are recommended as this avoids configuration transitions.

In smartcard mode, the data bits should be configured as 8 bits, and the parity bit should be configured.

When a parity error is detected by receiver, the transmit data line is pulled low for one baud clock cycle at the end of the stop bit as NACK signal(If USART_CTRL3.SCNACK is set). This NACK signal will generate a framing error on the transmitter side (transmitter side is configured with 1.5 stop bits).

When the transmitter receives a NACK signal (framing error) from the receiver, it does not detect the NACK as a start bit (according to the ISO protocol, the duration of the received NACK can be 1 or 2 baud clock cycles).

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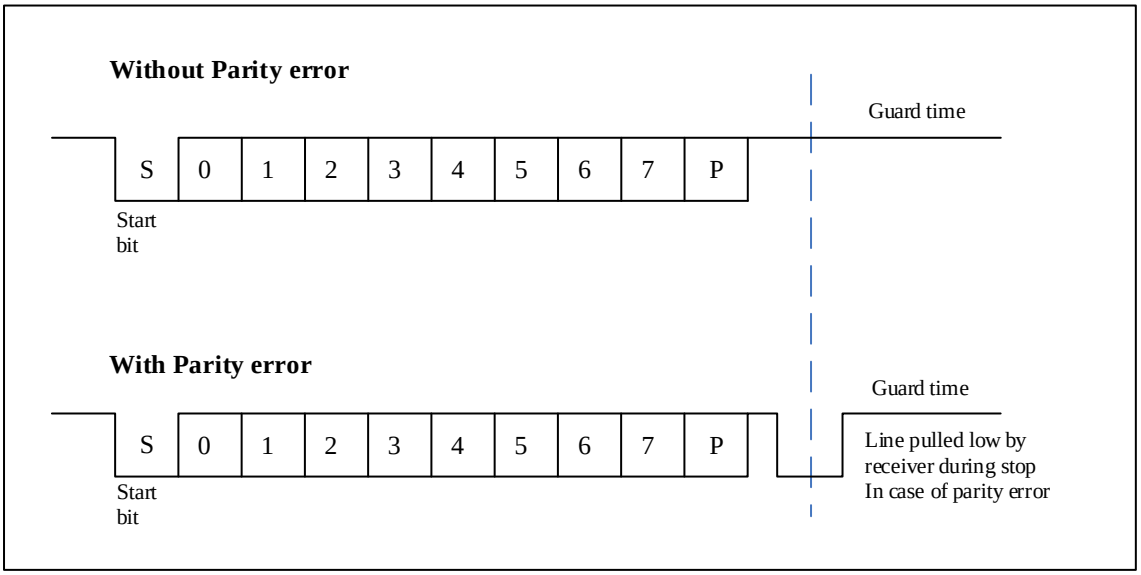
The example given in the following figure illustrates the signal on the data line with and without parity errors.

Figure 33-22 ISO7816-3 Asynchronous Protocol



The break frame has no meaning in smartcard mode. A 00h data with a framing error will be treated as data instead of a break symbol.

Under normal operation, data will be shifted out of the transmit shift register on the next baud clock. The smartcard mode is delayed by a minimum of 1/2 baud clock than normal operation.

In normal operation, USART_STS.TXC is set when a frame containing data is sent and USART_STS.TXDE=1.In smartcard mode, the transmission completion flag (USART_STS.TXC) is set high when the guard time counter reaches the value (USART_GTP.GTV[7:0]). The clearing of the USART_STS.TXC flag is not affected by the smartcard mode.

The following figure details how USART samples NACK signals.

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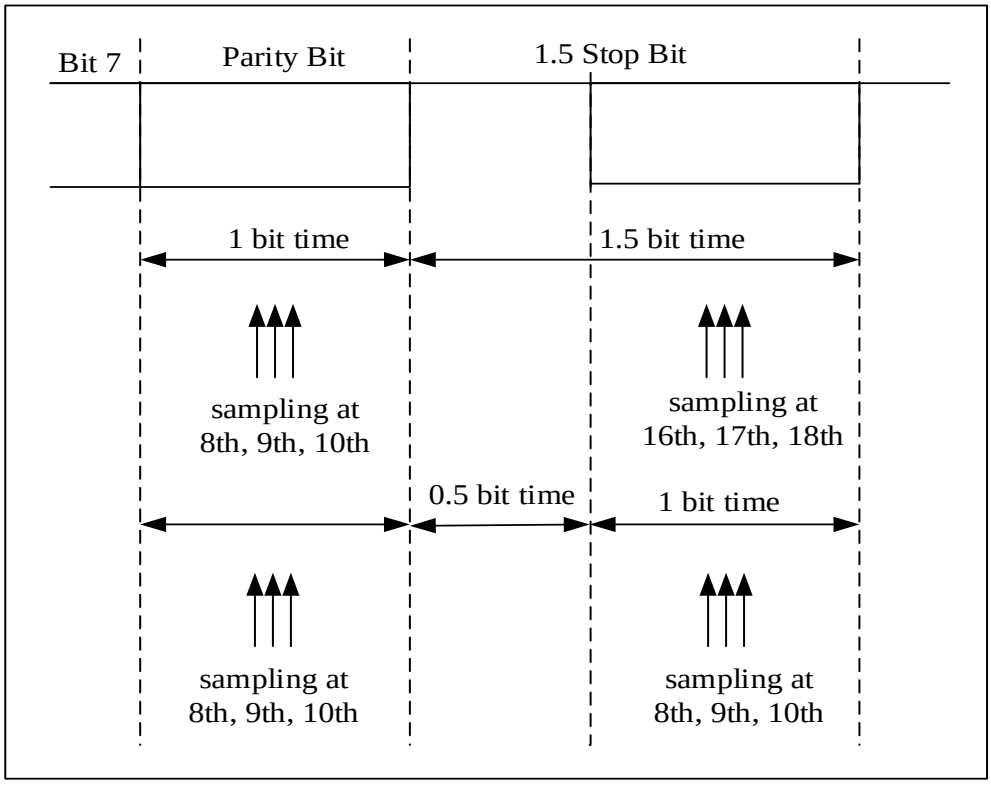
Figure 33-23 Use 1.5 Stop Bits To Detect Parity Errors



33.5 Interrupt Request

The various interrupt events of USART are logical OR relations, if the corresponding enable control bit is set, these events can generate their own interrupts, but only one interrupt request can be generated at the same time.

Table 33-8 USART Interrupt Request

Interrupt function	Interrupt event	Event flag	Enable bit
USART global interrupt	Transmission data register is empty.	TXDE	TXDEIEN
	CTS flag	CTSF	CTSIEN
	Transmission complete	TXC	TXCIEN
	Receive data ready to be read	RXDNE	RXDNEIEN
	Data overrun error detected.	OREF	
	Idle line detected	IDLEF	IDLEIEN
	Parity error	PEF	PEIEN
	Disconnect flag	LINBDF	LINBDIEN
	Noise Flag / Overflow Error in Multi-Buffer	NEF/OREF/FEF	ERRIEN(1)

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	Communication (DMA) / Frame Error(1)		
	Receiver Timeout	RTOF	RTOIEN
	RXFIFO Receive FIFO Interrupt	RXFE	RXFEIEN
		RXFF	RXFFIEN
		RXFT	RXFTIEN
	TXFIFO Transmit FIFO Interrupt	TXFE	TXFEIEN
		TXFF	TXFFIEN
		TXFT	TXFTIEN

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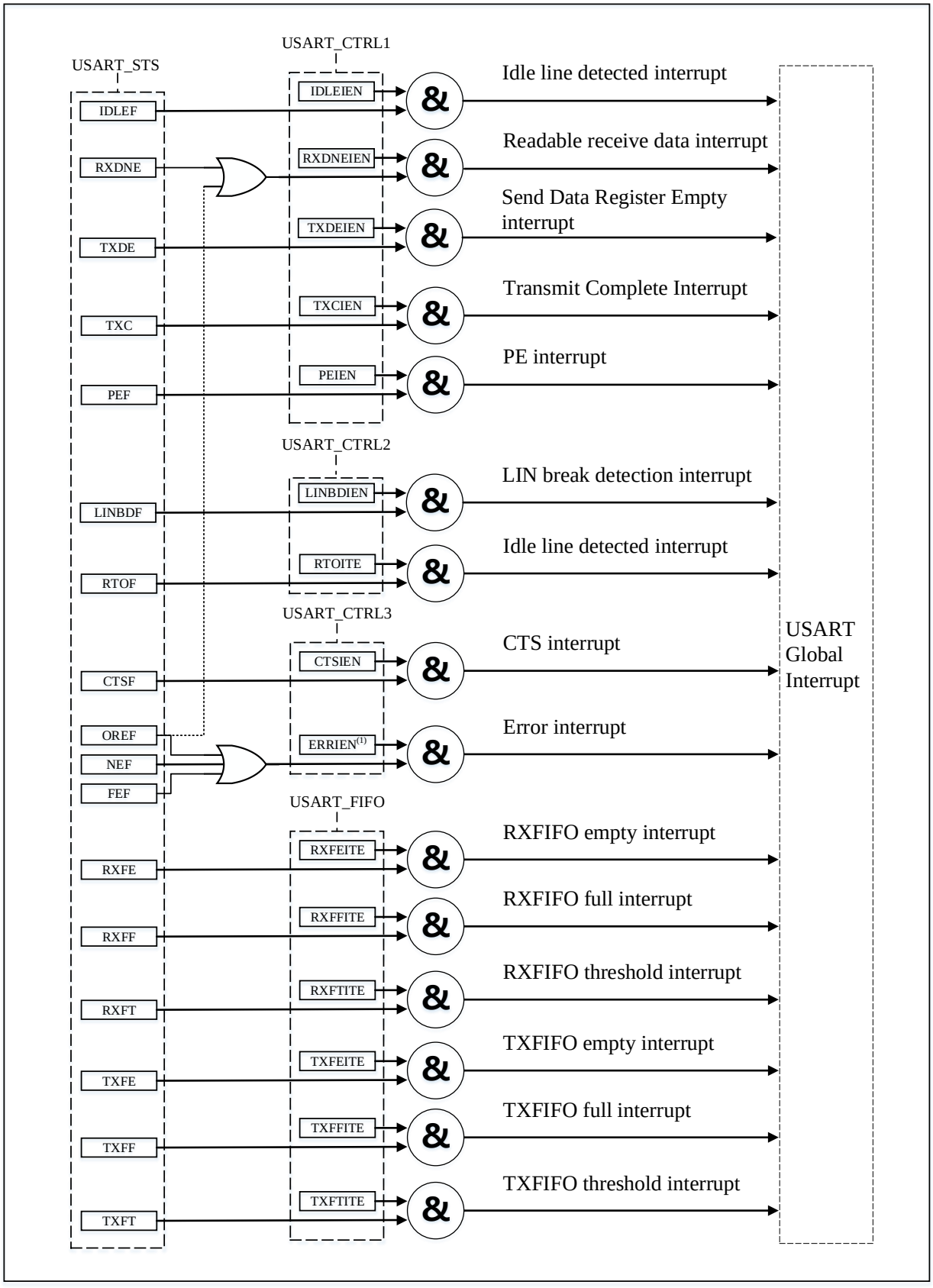
Figure 33-24 USART Interrupt Request



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(1) These flags will only generate an error interrupt when receiving data using DMA (USART_CTRL3.DMARXEN=1).

33.6 Mode Support

Table 33-9 USART Mode Setting (1)

Communication mode	USART1~USART8	UART9~UART15
Asynchronous mode	Y	Y
Multiprocessor	Y	Y
LIN	Y	Y
Synchronous mode	Y	N
Single-wire half duplex mode	Y	Y
Smartcard mode	Y	N
IrDA infrared mode	Y	Y
DMA communication mode	Y	Y
Hardware flow control mode	Y	Y

(1) Y = support this mode, N = do not support this mode.

33.7 USART Registers

33.7.1 USART Control Register 1 Register (USART_CTRL1)

Address offset : 0x00

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			IFCEN	SWAP	OSPM	DEAT					DEDT				
			rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEP	DEM	SDBRK	PEIEN	TXC IEN	TXDE IEN	RXDNE IEN	IDLE IEN	WUM	RCVWU	WL	PCEN	PSEL	TXEN	RXEN	UEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained
28	IFCEN	Idle frame controllable enable. 0: Disable idle frame controllable adjustment, idle frame length is consistent with the

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Bit Field	Name	Description
		number of data bits; 1: Enable idle frame controllable adjustment, idle frame length is controlled by USART_IFW. *Note: This bit can only be written when USART is disabled (UEN='0').*
27	SWAP	Swap TX/RX pins. This bit is set to 1 and cleared by software. 0: Use TX/RX pins as defined in standard pinout. 1: Swap the functions of TX and RX pins. Allows operation in cross-connection with another USART. *Note: This bit can only be written when USART is disabled (UEN='0').*
26	OSPM	Oversampling mode 0: x16 Oversampling 1: x8 Oversampling *Note: 1. This bit can only be written when USART is disabled (UEN='0').* *2.In LIN, IrDA, and smart card modes, this bit must remain cleared.*
25:21	DEAT	Driver Enable assertion time. These 5 bits are used to define the time between activating the DE (Driver Enable) signal and the start of the start bit. This time is represented in sampling time units (1/8 or 1/16 of a bit time, depending on the oversampling rate). This bit field can only be written when USART is disabled (UEN='0').
20:16	DEDT	Driver Enable deassertion time. These 5 bits are used to define the time between the end of the last stop bit in the transmitted message and the deactivation of the DE (Driver Enable) signal. This time is represented in sampling time units (1/8 or 1/16 of a bit time, depending on the oversampling rate). If a write operation is performed on the USART_DAT register within the DEDT time, the new data will only be sent after the DEDT and DEAT times have elapsed. *Note: This bit can only be written when USART is disabled (UEN='0').*
15	DEP	Driver enable polarity selection 0: DE signal active high. 1: DE signal active low. *Note: This bit can only be written when USART is disabled (UEN='0').*
14	DEM	Driver enable mode. This bit is used to activate external transceiver control via the DE signal (DE signal output on the RTS pin). 0: Disable DE function. 1: Enable DE function. *Note: This bit can only be written when USART is disabled (UEN='0').*
13	SDBRK	Send Break Character. The software transmits a break character by setting this bit to 1. This bit is cleared by hardware during stop bit of the break frame transmission. 0: No break character was sent.

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Bit Field	Name	Description
		1: Send a break character.
12	PEIEN	PE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.PEF bit is set. 0: Parity error interrupt is disabled. 1: Parity error interrupt is enabled.
11	TXCIEN	Transmit complete interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.TXC is set. 0: Transmission completion interrupt is disabled. 1: Transmission completion interrupt is enabled.
10	TXDEIEN	TXDE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.TXDE bit is set. 0: Send buffer empty interrupt is disabled. 1: Send buffer empty interrupt is enabled.
9	RXDNEIEN	RXDNE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.RXDNE or USART_STS.OREF is set. 0: Data buffer non-empty interrupt o and overrun error interrupt are disabled. 1: Data buffer non-empty interrupt o and overrun error interrupt are enabled.
8	IDLEIEN	IDLE interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.IDLEF is set. 0:IDLE line detection interrupt is disabled. 1: IDLE line detection interrupt is enabled.
7	WUM	Wake up mode from mute mode. 0: Idle frame wake up. 1: Address identifier wake up.
6	RCVWU	The receiver wakes up Software can set this bit to 1 to make USART enter mute mode, and clear this bit to 0 to wake up USART. In idle frame wake-up mode (USART_CTRL1.WUM=0), this bit is cleared by hardware when an idle frame is detected. In address wake-up mode (USART_CTRL1.WUM=1), when an address matching frame is received, this bit is cleared by hardware. Or when an address mismatch frame is received, it is set to 1 by hardware. 0: The receiver is in normal operation mode. 1: The receiver is in mute mode.
5	WL	Word length. 0:8 data bits. 1:9 data bits. *Note: If data is in transit, this bit cannot be configured.*
4	PCEN	Parity control enable 0: Parity control is disabled. 1: Parity control is enabled.
3	PSEL	Parity selection.

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Bit Field	Name	Description
		0: even check. 1: odd check.
2	TXEN	Transmitter enable. 0: The transmitter is disabled. 1: the transmitter is enabled.
1	RXEN	Receiver enable 0: The receiver is disabled. 1: the receiver is enabled.
0	UEN	USART enable When this bit is cleared, the divider and output of USART stop working after the current byte transmission is completed to reduce power consumption. Software can set or clear this bit. 0:USART is disabled. 1:USART is enabled.

33.7.2 USART Control Register 2 Register (USART_CTRL2)

Address offset : 0x04

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											FEFLOSE	NEFLOSE	PEFLOSE	RTOIEN	RTOCF
											rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTOEN	LINBDL	LINBDIEN	LINMEN	LBCLK	CLKPHA	CLKPOL	CLKEN	Reserved	STPB		Reserved	ADDR			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained
20	FEFLOSE	FEF Data Discard Enable Bit. Enabling this bit prevents data from being written into the FIFO when a framing error occurs during data reception in FIFO mode, and no FEF flag will be generated. 1: Enable 0: Disable
19	NEFLOSE	NEF Data Discard Enable Bit. Enabling this bit prevents data from being written into the FIFO when a noise error occurs during data reception in FIFO mode, and no NEF flag will be generated. 1: Enable 0: Disable
18	PEFLOSE	PEF Data Discard Enable Bit.

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Bit Field	Name	Description
		Enabling this bit prevents data from being written into the FIFO when a framing error occurs during data reception in FIFO mode, and no PEF flag will be generated. 1: Enable 0: Disable
17	RTOIEN	Receiver timeout interrupt enable. This bit is set to 1 and cleared by software. 0: Disable interrupt 1: Generate USART interrupt when RTOF bit in USART_STS register is set to 1.
16	RTOCF	Receiver timeout clear flag. When writing '1' to this bit, the RTOF flag in the USART_STS register will be cleared.
15	RTOEN	Receiver timeout enable. This bit is set to 1 and cleared by software. 0: Disable receiver timeout function. 1: Enable receiver timeout function. Upon enabling this function, if the RX line remains idle (no reception) for the programmed duration in RTOR (Receiver Timeout Register), the RTOF flag in the USART_STS register is set to 1.
14	LINBDL	LIN break detection length. This bit is used to set the length of the break frame. 0:10 bit break detection 1:11 bit break detection *Note: LINBDL can be used to control the detection length of Break Characters in LIN mode and other modes, and the detection length is the same as that in LIN mode.*
13	LINBDIEN	LIN break detection interrupt enable. If this bit is set to 1, an interrupt will be generated when USART_STS.LINBDF bit is set. 0: Disconnect signal detection interrupt is disabled. 1: Turn-off signal detection interrupt enabled
12	LINMEN	LIN mode enable 0:LIN mode is disabled 1:LIN mode enabled
11	LBCLK	The Last bit clock pulse. This bit is used to set whether the clock pulse corresponding to the last transmitted data byte (MSB) is output on CK pin in synchronous mode. 0: The clock pulse of the last bit of data is not output from CK. 1: The clock pulse of the last bit of data will be output from CK. *Note: This bit cannot be used for UART9~15.*
10	CLKPHA	Clock phase. This bit is used to set the phase of CK pin in synchronous mode. 0: Sample the first data at the first clock edge.

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Bit Field	Name	Description
		1: Sample the first data at the second clock edge. *Note: This bit cannot be used for UART9~15.*
9	CLKPOL	Clock polarity. This bit is used to set the polarity of CK pin in synchronous mode. 0: CK pin remains low when it is not transmitted to the outside. 1: CK pin remains high when it is not sent to the outside. *Note: This bit cannot be used for UART9~15.*
8	CLKEN	Clock enable 0:CK pin is disabled 1:CK pin enabled *Note: This bit cannot be used for UART9~15.*
7	Reserved	Reserved, the reset value must be maintained
6:5	STPB[1:0]	STOP bits. 00:1 stop bit. 01:0.5 stop bit. 10:2 stop bit. 11:1.5 stop bit. *Note: For UART9~15, only one stop bit and two stop bits are valid.*
4	Reserved	Reserved, the reset value must be maintained
3:0	ADDR[3:0]	USART address. Used in the mute mode of multiprocessor communication, using address identification to wake up a USART device. In address wake-up mode (USART_CTRL1.WUM=1), if the lower four bits of the received data frame are not equal to the ADDR[3:0] value, USART will enter the mute mode; If the lower four bits of the received data frame are equal to the ADDR[3:0] value, USART will be awakened.

33.7.3 USART Control Register 3 Register (USART_CTRL3)

Address offset : 0x08

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SCNACK	SCMEN	IRDALP	IRDAMEN	ERRIEN	DMARXEN	DMATXEN	HDMEN	RTSEN	CTSIEN	CTSEN
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	SCNACK	Smartcard NACK enable. This bit is used for Smartcard mode to enable transmitting NACK when parity error occurs. 0: Do not send NACK when there is a parity error. 1: send NACK when there is a parity error. *Note: This bit cannot be used for UART9~15*
9	SCMEN	Smartcard mode enable. This bit is used to enable Smartcard mode. 0: Smartcard mode is disabled. 1: Smartcard mode is enabled. *Note: This bit cannot be used for UART9~15*
8	IRDALP	IrDA low-power mode. This bit is used to select the low power consumption mode for IrDA mode. 0: Normal mode. 1: Low power mode.
7	IRDAMEN	IrDA mode enable. 0:IrDA is disabled. 1:IrDA is enabled.
6	ERRIEN	Error interrupt enable. When DMA receive mode (USART_CTRL3.DMARXEN=1) is enabled, an interrupt will be generated when USART_STS.FEF, USART_STS. OREF or USART_STS. NEF bit is set. 0: Error interrupt is disabled. 1: Error interrupt enabled.
5	DMARXEN	DMA receiver enable. 0:DMA receive mode is disabled. 1:DMA receive mode is enabled.
4	DMATXEN	DMA transmitter enable. 0:DMA transmission mode is disabled. 1:DMA transmission mode is enabled.
3	HDMEN	Half-duplex mode enable. This bit is used to enable half-duplex mode. 0: Half-duplex mode is disabled. 1: Half-duplex mode is enabled.
2	RTSEN	RTS enable. This bit is used to enable RTS hardware flow control function. 0:RTS hardware flow control is disabled. 1:RTS hardware flow control is enabled.
1	CTSIEN	CTS interrupt enable. If this bit is set to 1, an interrupt will be generated when USART_STS.CTSF bit is set. 0:CTS interrupt is disabled.

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Bit Field	Name	Description
		1:CTS interrupt is enabled.
0	CTSEN	CTS enable. This bit is used to enable the CTS hardware flow control function. 0:CTS hardware flow control is disabled. 1:CTS hardware flow control is enabled.

33.7.4 USART Status Register (USART_STS)

Address offset : 0x0C

Reset value : 0x0000 0180

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												FELOSEF	NELOSEF	PELOSEF	RTOF
												rc_w1	rc_w1	rc_w1	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEF	NEF	OREF	PEF	LINBDF	CTSF	RXDNE	TXC	TXDE	IDLEF	TXFT	RXFT	RXFE	TXFE	RXFF	TXFF
r	r	r	r	rc_w0	rc_w0	rc_w0	rc_w0	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	FELOSEF	Received Data FE Error Discard Flag. In the FIFO mode, when an FE error is received, indicating that erroneous data is discarded and not written into the FIFO. Writing a 1 to this bit clears it. In non-FIFO mode, this bit is 0. 1: Discard data with FE error; 0: No data FE error
18	NELOSEF	Received Data NE Error Discard Flag. In the FIFO mode, when an NE error is received, indicating that erroneous data is discarded and not written into the FIFO. Writing a 1 to this bit clears it. In non-FIFO mode, this bit is 0. 1: Discard data with NE error; 0: No data NE error
17	PELOSEF	Received Data PE Error Discard Flag Bit. In the FIFO mode, when a PE error is received, indicating that erroneous data is discarded and not written into the FIFO. Writing a 1 to this bit clears it. In non-FIFO mode, this bit is 0. 1: Discard data with PE error; 0: No data PE error
16	RTOF	Receiver Timeout. After the programmed timeout value in the RTOR register has elapsed and there is no

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Bit Field	Name	Description
		communication, this bit is set to 1 by hardware. This bit is cleared by software by writing a '1' to the USART_CTRL2.RTOCF bit. If RTOIEN in the USART_CTRL2 register is set to '1', an interrupt is generated. 0: Timeout value not reached, 1: Timeout value reached, no data received
15	FEF	Framing error. When the data is not synchronized or a large amount of noise is detected, and the stop bit is not received and recognized at the expected time, it will be judged that a framing error has been detected, and this bit will be set to 1. First read USART_STS, then read USART_DAT can cleared this bit. 0: No framing errors were detected. 1: A framing error or a Break Character is detected. *Note: this bit will not generate an interrupt because it appears with USART_STS.RXDNE, and the hardware will generate an interrupt when setting the USART_STS.RXDNE flag. If the currently transmitted data has both framing errors and overload errors, the hardware will continue to transmit the data and only set the USART_STS.OREF flag bit.* *In the multi-buffer communication mode, if the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the FEF flag is set.*
14	NEF	Noise error flag. When noise is detected in the received frame, this bit is set by hardware. It is cleared by the software sequence (read first USART_STS, read USART_DAT again). 0: No noise error detected. 1: Noise error detected. *Note: this bit will not generate an interrupt because it appears with USART_STS.RXDNE, and the hardware will generate an interrupt when setting the USART_STS.RXDNE flag. In the multi-buffer communication mode, if the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the NEF flag is set.*
13	OREF	Overrun error With RXDNE set, this bit is set if the USART_DAT register receives data from the shift register. When USART_CTRL3.ERRIEN bit is set, an interrupt will be generated. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No overrun error was detected. 1: Overflow error detected.
12	PEF	Parity error. This bit is set when the parity bit of the received data frame is different from the expected check value. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No parity error was detected.

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Bit Field	Name	Description
		1: Parity error detected.
11	LINBDF	LIN break detection flag. If USART_CTRL2.LINMEN bit is set, this bit is set by hardware when LIN disconnection is detected. If USART_CTRL2.LINBDIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0: LIN break character not detected. 1: LIN break character detected.
10	CTSF	CTS flag If USART_CTRL3.CTSEN bit is set, this bit is set by hardware when the nCTS input changes. If USART_CTRL3.CTSIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0:nCTS status line has not changed. 1:nCTS status line changes.
9	RXDNE	The Read data register not empty. This bit is set when the read data buffer receives data from the shift register. When USART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. Software can clear this bit by writing 0 to it or reading the USART_DAT register. 0: The read data buffer is empty. 1: The read data buffer is not empty.
8	TXC	Transmission complete. This bit is set to 1 after power-on reset. If USART_STS.TXDE is set, this bit is set when the current data transmission is completed. Setting USART_CTRL1.TXCIEN bit will generate an interrupt. This bit is cleared by software. 0: Transmitting did not complete. 1: Send completed.
7	TXDE	The Transmit data register empty. Set to 1 after power-on reset or data to be sent has been sent to the shift register. Setting USART_CTRL1.TXDEIEN will generate an interrupt. This bit is cleared to 0 when the software writes the data to be sent into USART_DAT. 0: Send data buffer is not empty. 1: The transmitting data buffer is empty.
6	IDLEF	IDLE line detected flag. Within one frame time, the idle state is detected at the RX pin, and this bit is set to 1. When USART_CTRL1.IDLEIEN bit is set, an interrupt will be generated. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No idle frame detected. 1: idle frame detected. *Note: IDLEF bit will not be set high again until USART_STS.RXDNE bit is set (that is, an idle line is detected again).*

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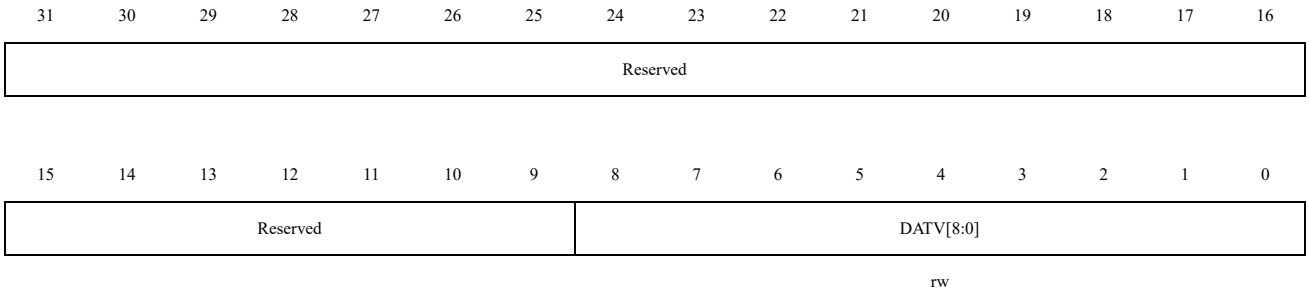
Bit Field	Name	Description
5	TXFT	TX FIFO threshold. 0: Number of data in the TX FIFO has not reached the threshold. 1: Number of data in the TX FIFO has reached the threshold.
4	RXFT	RX FIFO threshold 0: Number of data in the RX FIFO has not reached the threshold. 1: Number of data in the RX FIFO has reached the threshold.
3	RXFE	Receive FIFO empty 0: Receive FIFO data is not empty. 1: Receive FIFO data is empty.
2	TXFE	Send FIFO empty 0: Send FIFO data is not empty. 1: Send FIFO data is empty.
1	RXFF	Receive FIFO full 0: Receive FIFO data is not full. 1: Receive FIFO data is full.
0	TXFF	Send FIFO full 0: Send FIFO data is not full. 1: Send FIFO data is full.

33.7.5 USART Data Register (USART_DAT)

Address offset : 0x10

Reset value : undefined (uncertain value)



Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	DATV[8:0]	Data value Contains the data sent or received; Software can change the transmitted data by writing these bits, or read the values of these bits to obtain the received data. If parity is enabled, when the transmitted data is written into the register, the highest bit of the data (the 7th or 8th bit depends on USART_CTRL1.WL bit) will be replaced by the parity bit.

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33.7.6 USART Baud Rate Register (USART_BRCF)

Address offset : 0x14

Reset value : 0x0000 0000

Note: When USART_CTRL1.UEN=1, this register cannot be written.The baud counter stops counting if USART_CTRL1.TXEN or USART_CTRL1.RXEN are disabled respectively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIVINT[11:0]												DIVDEC[3:0]			
rw												rw			

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:4	DIVINT [11:0]	Integer part of baud rate divider.
3:0	DIVDEC[3:0]	Fractional part of baud rate divider. *Note: Under 8x oversampling, only the lower three bits of DIVDEC[3:0] are valid.*

33.7.7 USART Guard Time And Prescaler Register (USART_GTP)

Address offset : 0x18

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTV[7:0]								PSCV[7:0]							
rw								rw							

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	GTV[7:0]	Guard time value in Smartcard mode. This Bit Field specifies the guard time in baud clock. In Smartcard mode, this function is required. The setting time of USART_STS.TXC flag is delayed by GTV[7:0] baud clock cycles.

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Bit Field	Name	Description
		Note: This bit is invalid for UART9~15.
7:0	PSCV[7:0]	Prescaler value. In IrDA low power consumption mode: these bits are used to set the frequency division coefficient for dividing the peripheral clock (PCLK1/PCLK2) to generate low power consumption frequency. 00000000: reserved-do not write this value. 00000001: divide the source clock by 1. … 11111111: divide the source clock by 255. In IrDA normal mode: PSCV can only be set to 00000001. In Smartcard mode: PSCV[4:0] is used to set the frequency division of Smartcard clock generated by peripheral clock (PCLK1/ PCLK2). Coefficient. The actual frequency division coefficient of is twice the set value of PSCV[4:0]. 0000: reserved-do not write this value. 0001: Divide the source clock by 2. 0010: Divide the source clock by 4. … 1111: Divide the source clock by 62. In Smartcard mode, PSCV[7:5] is reserved.

33.7.8 USART FIFO Register (USART_FIFO)

Address offset : 0x1C

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										TXCNT				RXCNT	
										r				r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXCNT		TXFTIEN	RXFTIEN	RXFEIEN	TXFEIEN	RXFFIEN	TXFFIEN	RXFTCFG			TXFTCFG			CLR	EN
r		rw	rw	rw	rw	rw	rw	rw			rw			rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21:18	TXCNT	number of TXFIFO valid data
17:14	RXCNT	number of RXFIFO valid data
13	TXFTIEN	TXFIFO threshold interrupt enable

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Bit Field	Name	Description
		If this bit is set to 1, an interrupt is generated when USART_STS.TXFT is set. 0: Disable TXFT interrupt. 1: Enable TXFT interrupt.
12	RXFTIEN	RXFIFO threshold interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.RXFT is set. 0: Disable RXFT interrupt. 1: Enable RXFT interrupt.
11	RXFEIEN	RXFIFO empty interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.RXFE is set. 0: Disable RXFE interrupt. 1: Enable RXFE interrupt.
10	TXFEIEN	TXFIFO empty interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.TXFE is set. 0: Disable TXFE interrupt. 1: Enable TXFE interrupt.
9	RXFFIEN	RXFIFO full interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.TXFF is set. 0: Disable RXFF interrupt. 1: Enable RXFF interrupt.
8	TXFFIEN	TXFIFO full interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.TXFF is set. 0: Disable TXFF interrupt. 1: Enable TXFF interrupt.
7:5	RXFTCFG	RXFIFO threshold configuration. 000: Receive FIFO reaches 1/8 of its depth 001: Receive FIFO reaches 2/8 of its depth 010: Receive FIFO reaches 4/8 of its depth 011: Receive FIFO reaches 6/8 of its depth 100: Receive FIFO reaches 7/8 of its depth 101: Receive FIFO is full All other combinations: Reserved
4:2	TXFTCFG	TXFIFO threshold configuration. 000: TXFIFO reaches 1/8 of its depth 001: TXFIFO reaches 1/4 of its depth 010: TXFIFO reaches 1/2 of its depth 011: TXFIFO reaches 3/4 of its depth 100: TXFIFO reaches 7/8 of its depth 101: TXFIFO becomes empty All other combinations: Reserved
1	CLR	Clear data and pointers in the FIFO. This bit is a pulse signal, writing 1 clears it, and CLR is also automatically cleared. 0: No clear.

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Bit Field	Name	Description
		1: Clear.
0	EN	FIFO model enable. 0: FIFO mode disabled. 1: FIFO mode enabled.

33.7.9 USART Idle Frame Width Register (USART_IFW)

Address offset : 0x20

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIDTH															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WIDTH	Idle Frame Width *Note: In units of baud rate time*

33.7.10 USART Receive Timeout Width Register (USART_RTO)

Address offset : 0x24

Reset value : 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				TIME											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME															
rw															

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:0	TIME	Receiver Timeout Value *Note: In units of baud rate time*

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

34 Low power universal asynchronous receiver transmitter (LPUART)

34.1 Introduction

Low power universal asynchronous receiver transmitter (LPUART) is a low power, full duplex, asynchronous serial communication interface. The LPUART can be clock provided by LSE, HSE, HSI, MSI, SYSCLK . When 32.768kHz LSE is selected as the clock source, the LPUART can work in STOP0/2 low-power mode with a maximum communications up to 9600bps. LPUART supports receiving data wake-up. By configuring wake-up events, the CPU in STOP0/2 mode can be woken up.

At the same time, when MCU works in RUN mode, LPUART can also be used as a common asynchronous serial port. Users can switch the clock source to HSI, SYSCLK to obtain higher communication speed.

34.2 Main Features

- Full duplex asynchronous communication
- Selectable clock source of HSI, HSE, LSE, MSI, SYSCLK
- Fractional baud rate generator system: Programmable baud rate shared by sending and receiving up to 5Mbits/s; baud rates from 300bps to 9600bps when using 32.768 kHz clock source (LSE)
- Fixed 8-bit data word length, 1 stop bit and optional 1 parity bit
- Support DMA data transfer
- Support hardware flow control
- Transfer detection flag: Receive buffer full, Receive buffer half full, Receive buffer not empty, Receive buffer overrun, Transmission complete, Transmit buffer full, Transmit buffer half full, Transmit buffer not empty
- Parity control: Odd and even parity selection, Parity can be disable
- Error detection flag: Parity error, Overrun error, Noise error
- 32 byte receive buffer, 8 byte transmit buffer
- Baud rate error correction at low frequencies
- Configurable sampling method of 1 or 3 samples
- Noise detection
- Configurable flow control RTS threshold
- Support STOP0/2 mode Configurable source mode
- Start bit detection
- Receive buffer non-empty detection
- A configurable receive byte(1~32 byte)
- A programmable 8-byte frame

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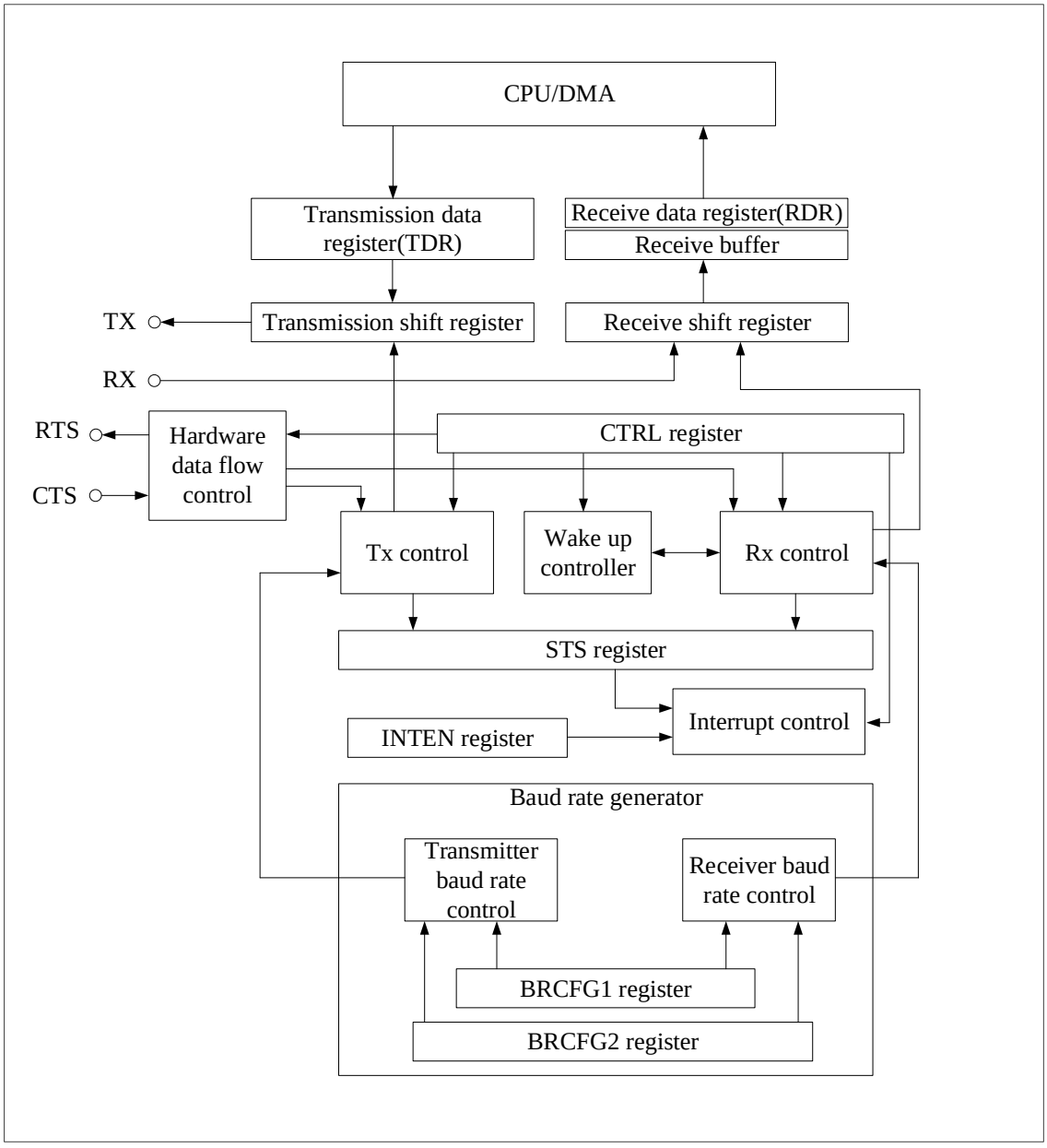
34.3 Functional block diagram

Figure 34-1 LPUART block diagram



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34.4 Function Description

As shown in Figure 34-1, LPUART bidirectional communication requires at least two pins: receiving data input (RX) and sending data output (TX).

RX: Serial data input. When the number of samples is 3, data and noise can be distinguished.

TX: Serial data output. When sending is enabled, the pin defaults to be high level.

The following pins are required in hardware flow control mode:

CTS (Clear To Send): When transmitter detects that CTS is valid (low level), the next data is sent.

RTS (Request To Send): When receiver is ready to receive new data, pull the RTS pin low.

LPUART has the following characteristics:

- Idle status without sending or receiving
- A start bit
- A data word (8 bits) with the least significant bits first
- A stop bit, indicating the end of a data frame
- A status register (LPUART_STS)
- Transmit Data register (LPUART_TXDAT)
- Receive Data register (LPUART_RXDAT)
- Two baud rate configuration registers (LPUART_BRCFG1 and LPUART_BRCFG2) using fractional baud rate generators:16-bit integer and 8-bit decimal representations

For specific definitions of each bit in the registers above, please refer to Section 34.6 of register Description.

34.4.1 LPUART frame format

The LPUART data word length is fixed at 8 bits (see Figure 34-2). During the start bit, TX pin is at a low level and during the stop bit it is at a high level. The parity bit follows the data word when enabled.

Both transmitting and receiving are driven by two different baud clock generators. When the LPUART_CTRL.TXEN of transmitter is set, the corresponding baud clock generator generates baud clock. When the start bit is received, the receiver's corresponding baud clock generator generates the clock.

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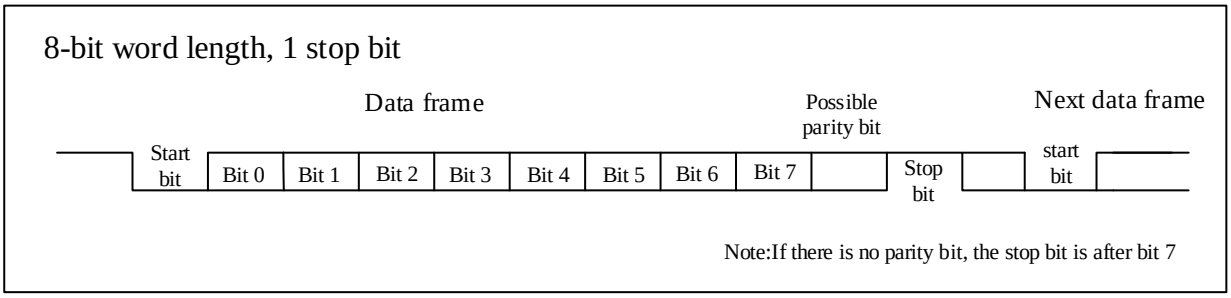
Figure 34-2 Frame format



Note: in this chapter, unless special instruction, setting means that a register is set to state '1', and resetting or clearing means that a register is set to state '0'. Hardware or programs may set or clear a register. Please refer to this chapter for details.

34.4.2 Transmitter

When the Transmit Enable bit (LPUART_CTRL.TXEN) is set and there is data in the buffer, the transmitter sends 8-bit data words. The data in the shift register is output on the TX pin.

34.4.2.1 Transmit process

During an LPUART transmission, the least significant bit of the data is shifted out on TX pin. In this mode, the LPUART_TXDAT register contains 8 byte buffer between the internal bus and the transmitter shift register (see Figure 34-1).

Each character is preceded by a low level starting bit; and is terminated by a stop bit.

Note: You cannot reset the LPUART_CTRL.TXEN bit during data transfer, otherwise the data on the TX pin will be corrupted because the baud rate counter stops counting. The current data being transferred will be lost.

The LPUART sends data as follows:

1. Configure baud rate, parity check, DMA, flow control, etc.
2. Set the LPUART_CTRL.TXEN bit to enable data transmission.
3. Write data to the LPUART_TXDAT register, it have 8 byte transmit buffer.
4. Check if the LPUART_STS.TXCF flag is set, it means the transmission is over. If the flag is set, write 1 to the LPUART_STS.TXCF bit to clear the flag.
5. Check the LPUART_STS.PCEF bit to confirm whether the parity is wrong.
6. Otherwise, go to Step 3 and send the next data.

Note: Be sure to initialize the LPUART module before using the transmitter.

LPUART initialization as follows:

1. Set all flag bits in the LPUART_STS register to clear the interrupt flag.
2. To enable the interrupt function, configure LPUART_INTEN.

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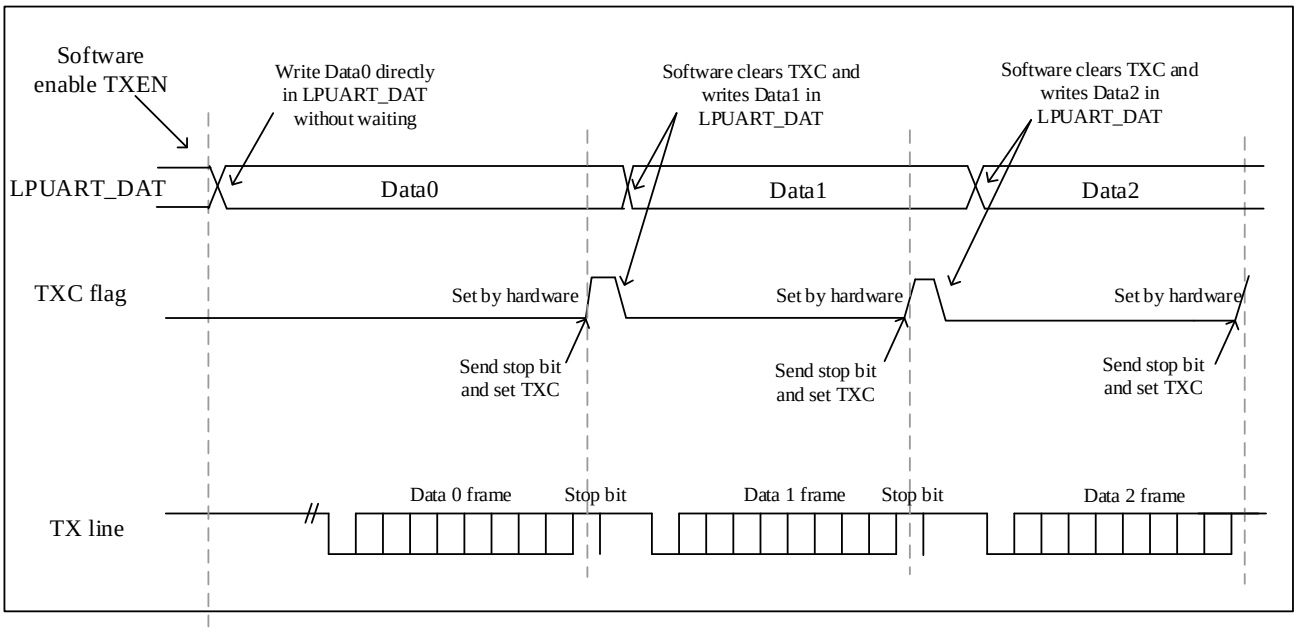
3. Set LPUART_CTRL.FRXF clear the RX buffer.

When send data:

- After configuring the baud rate and setting LPUART_CTRL.TXEN, the CPU can write directly to the LPUART_TXDAT register to send data.
- When a frame transmission is completed (after the stop bit is sent), the LPUART_STS.TXCF bit is set. If the LPUART_INTEN.TXCIE bit is set, an interrupt occurs immediately.
- After the last data byte is written to the LPUART_TXDAT register, you must wait for LPUART_STS.TXCF=1 before shutting down the LPUART module or setting the microcontroller into low-power mode.

Figure 34-3 TXC changes during transmission



34.4.3 Receiver

34.4.3.1 Start bit detection

If the LPUART_CTRL.SSM bit is 0, that is, the number of samples is 3, when there are at least two 0s in the three sample numbers, the start bit is valid. Otherwise it will be invalid.

Table 34-1 Start bit detection

Sampling values	NF state	Received bit value	Start bit validity
000	0	0	effective
001	1	0	effective
010	1	0	effective
011	1	1	invalid
100	1	0	effective
101	1	1	invalid

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110	1	1	invalid
111	0	1	invalid

34.4.3.2 Receive process

During LPUART reception, the least significant bits of data are first moved in from the RX pin. In this mode, the LPUART_RXDAT register contains 32 byte buffer between the internal APB bus and the receive shift register.

The steps for LPUART to receive data are as follows:

1. Configure baud rate, parity check, wake up event/enable, sampling mode, DMA, flow control, etc.
2. Check the interrupt flags of the LPUART_STS register: buffer is not empty, buffer is half full, buffer is full, buffer overrun;
3. Read the data by reading the LPUART_RXDAT register.
4. Return to Step 2 and continue receiving data.

Note: Please be sure to initialize the LPUART module before using the receiver.

When receiving a data frame:

- The LPUART_STS.RXFNEF bit is set, and the contents of the shift register are transferred to the RDR (Receiver Data Register). In other words, the data has been received and can be read (including its associated error flags).
- If the LPUART_INTEN.RXFNEIEN bit is set, an interrupt is generated.
- Frame errors (parity detection errors), noise or overrun errors are detected during reception, so the error flag will be set.
- In multi-buffer communication mode, the LPUART_STS.RXFNEF flag bit is placed after each byte received and cleared by DMA's read operation on the data register.
- In single buffer mode, the software can clear LPUART_STS.RXFNEF bits by reading the LPUART_RXDAT register or by writing 0.The LPUART_STS.RXFNEF bit must be cleared before the end of the next frame of data reception to avoid overrun errors.

34.4.3.3 Overrun error

The LPUART receiving data buffer has a total of 32 bytes. The LPUART_STS.RXFFF flag will be set after receiving 32 bytes of data. When the buffer data is not read out and causes LPUART_STS.RXFFF to be not reset in time, if next character is received, an overrun error occurs. This character will be discarded by the hardware. Data can only be transferred from the shift register to the receiving data buffer if the LPUART_STS.RXFFF bit is cleared. If the next data has been received or the previous DMA request has not been served, the LPUART_STS.RXFFF flag is still set and an overrun error occurs.

When an overrun error occurs:

- The LPUART_STS.RXFOF bit is set.
- The receiving data buffer content will not be lost. Reading the LPUART_RXDAT register still returns the previous data.

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- The contents of the shift register will be overwritten. Any subsequent data received will be lost.
- If the LPUART_INTEN.RXFOIEN bit is set, an interrupt is generated.
- LPUART_DAT register read operation, reset LPUART_STS.RXFOF.

34.4.3.4 Noise error

Noise errors use an over-sampling technique (if the LPUART_CTRL.SSM bit is 0, that is, the number of samples is 3) to recover data by distinguishing valid input data from noise.

Figure 34-4 Data sampling for noise detection

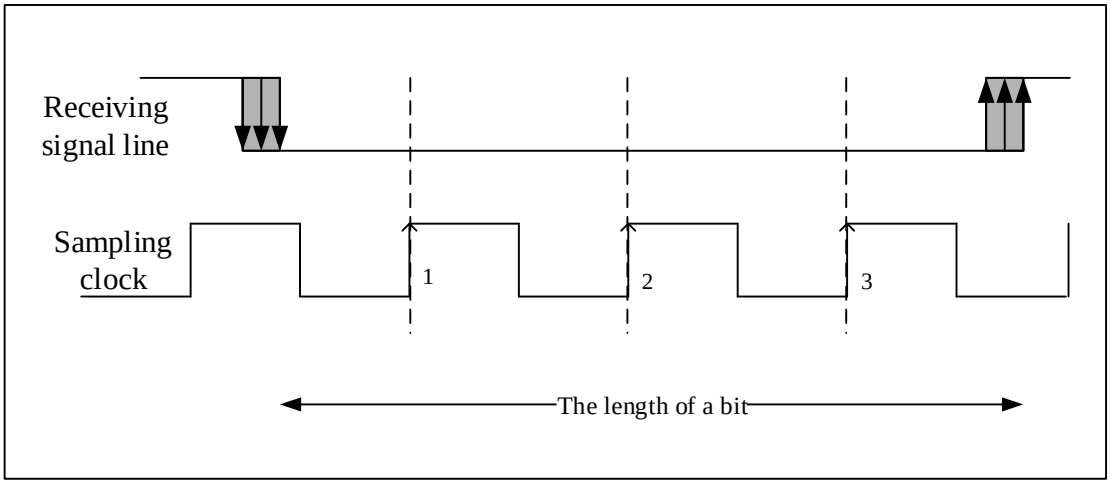

Table 34-2 Data sampling for noise detection

Sampling values	NEF state	Received bit value
000	0	0
001	1	0
010	1	0
011	1	1
100	1	0
101	1	1
110	1	1
111	0	1

When noise is detected in a receiving frame, you can do the following:

- If three sample values are inconsistent, set the LPUART_STS.NEF flag immediately.
- The received data is transferred from the shift register to the buffer.

- Software write 1 clears the LPUART_STS.NEF flag bit.

34.4.4 Fractional baud rate generation

Baud rate frequency division coefficient is divided into 16-bit integer part and 8-bit decimal part. The baud rate generator uses the value of the combination of these two parts to determine the baud rate. The fractional baud rate

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divider will enable the LPUART to generate all standard baud rates.

Baud rate frequency division coefficient (LPUARTDIV) has the following relationship with system clock :

$$\text{TX/RX baud rate} = f_{CLK} / (\text{LPUARTDIV})$$

Here the f_{CLK} is the clock for LPUART (the clock source of LPUART can be HSI, LSE, SYSCLK). The value of LPUARTDIV is set in the baud rate configuration registers LPUART_BRCFG1 and LPUART_BRCFG2

Note: After writing LPART_BRCFG1 and LPUART_BRCFG2, the baud rate counter is replaced with the new value of the baud rate register. Therefore, do not change the value of the baud rate register during communication.

34.4.4.1 Configure baud rates through LPUART_BRCFG1 and LPUART_BRRCFG2

For example, baud rate = 4800bps, clock frequency = 32768Hz.

LPUARTDIV = 32768/4800 = 6.82667.LPUART_BRCFG1 = 6 and the value of LPUART_BRCFG2 is calculated by adding fractions in the table below (the value of LPUART_BRCFG2 is 0xEFh).

Table 34-3 Calculation of LPUART_BRCFG1/2

Decimal addition	Carry to the next integer	Bit field	Value
0.82667 + 0.82667 = 1.65333	YES	DECIMAL0	1
1.65333 + 0.82667 = 2.48000	YES	DECIMAL1	1
2.48000 + 0.82667 = 3.30667	YES	DECIMAL2	1
3.30667 + 0.82667 = 4.13333	YES	DECIMAL3	1
4.13333 + 0.82667 = 4.96000	NO	DECIMAL4	0
4.96000 + 0.82667 = 5.78667	YES	DECIMAL5	1
5.78667 + 0.82667 = 6.61333	YES	DECIMAL6	1
6.61333 + 0.82667 = 7.44000	YES	DECIMAL7	1

When LSE clock (32.768KHz) is used, the values of baud rate configuration registers LPUART_BRCFG1 and LPUART_BRCFG2 with different baud rate Settings are as follows:

Table 34-4 Baud rate configuration of register LPUART_BRCFG1/2

Baud rate	Divisor	LPUART_BRCFG1	LPUART_BRCFG2
300	109.2267	6Dh	88h
600	54.6133	36h	ADh
1200	27.3067	1Bh	24h
2400	13.6533	0Dh	6Dh
4800	6.8267	06h	EFh

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9600	3.4133	03h	4Ah

Note: The lower the clock frequency of the CPU, the lower the accuracy of a particular baud rate.

If the MCU is powered by 3.3V, the LPUART baud rate should be within 1Mbps, and if the MCU is powered by 1.8V, the LPUART baud rate should be within 115200bps.

34.4.5 Parity control

Reset the LPUART_CTRL.PC bit, enable parity control (generate a parity bit when sending, parity check when receiving), set or reset the LPUART_CTRL.PEN bit selection to use odd or even check. LPUART frame formats are listed in the table below.

Table 34-5 Parity frame format

PCDIS bit	LPUART frame
0	| Start bit | 8-bit data | parity bit | stop bit |
1	| Start bit | 8 bits data | stop bit |

Transfer mode: Parity is enabled by resetting the LPUART_CTRL.PC bit. If parity fails, the LPUART_STS.PCEF flag is set to '1', and an interrupt occurs if LPUART_INTEN.PCEIEN is set.

Odd parity: LPUART_CTRL.PEN＝1.

Make the number of '1' in one frame data (including parity bit) be an odd number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total).

Even parity: LPUART_CTRL.PEN＝0.

Make the number of '1' in one frame data (including parity bit) be an even number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total).

34.4.6 DMA application

LPUART can access the transmit data register (TDR) and receive buffer respectively through DMA.

34.4.6.1 DMA transmission

The steps for assigning a DMA channel to the LPUART transmissions are as follows (x indicates the channel number) :

1. Configure the LPUART_TXDAT register address as the destination address for DMA transfer, and the memory address as the source address for DMA transfer.
2. Set the total number of bytes to be transmitted.
3. Set the channel priority.
4. Configure to generate DMA interrupts when the transfer is half or all complete.
5. Activate the channel.

Completing a DMA transfer will generate an interrupt on the corresponding DMA channel. In transmission mode, when the DMA has finished the data transfer, the DMA controller sets the DMA_TCINTSTS.CHn flag. The

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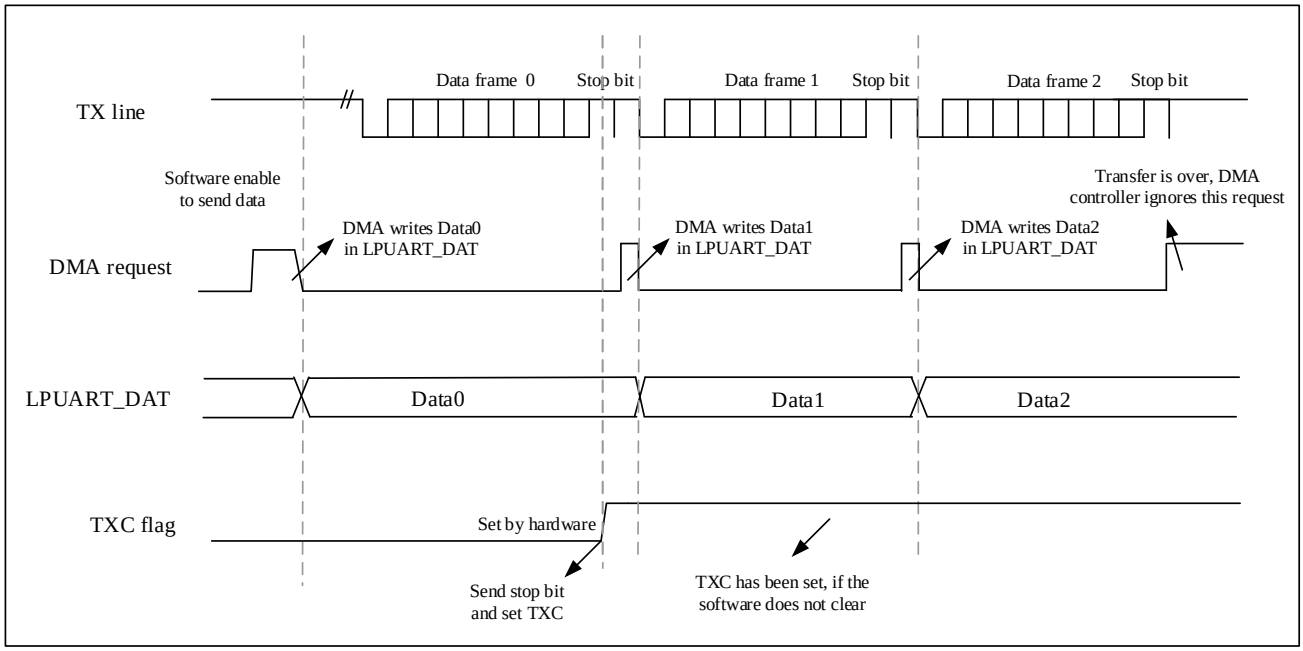
LPUART_STS.TXCF flag bit is asserted by the hardware to indicate that the transfer is completed. The software needs wait for LPUART_STS.TXCF=1.

Figure 34-5 Sending using DMA



34.4.6.2 DMA reception

The steps for assigning a DMA channel to the LPUART receiving are as follows (x indicates the channel number) :

1. Configure the LPUART_RXDAT register address as the source address for transmission and the memory address as the destination address for transmission through the DMA configuration register.
2. Configure the number of DMA bytes to be transferred.
3. Configure the channel priority on the DMA register for data transfer.
4. Configure interrupts to generate DMA interrupts when the transfer is half or all complete.
5. Activate the channel.

When completing the transfer specified by the DMA controller, the DMA controller generates an interrupt on the DMA channel's interrupt vector.

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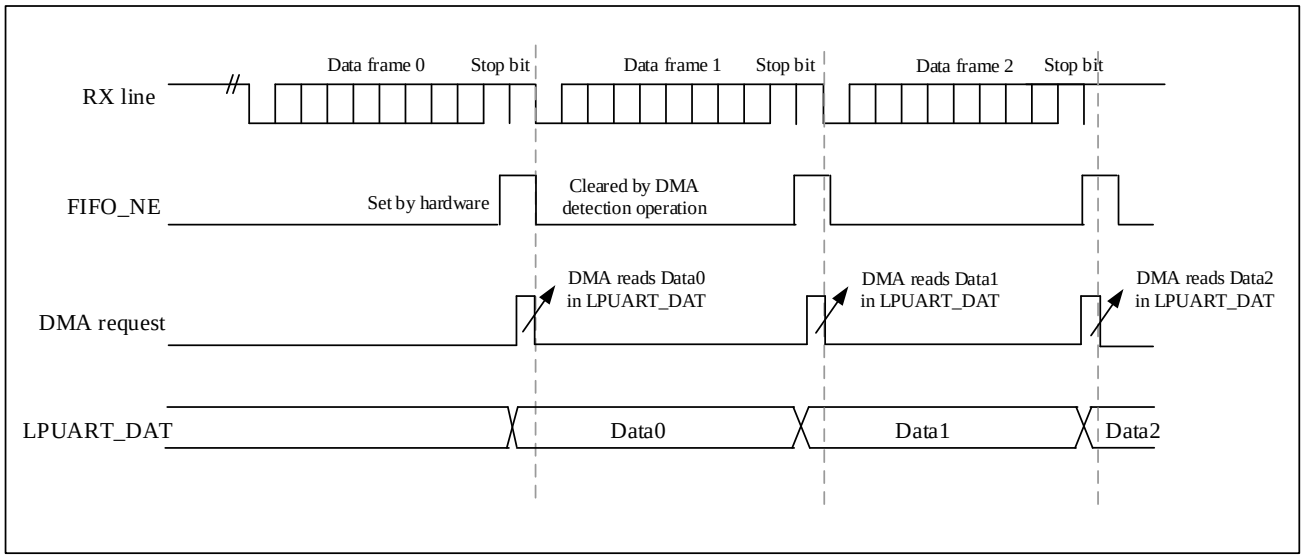
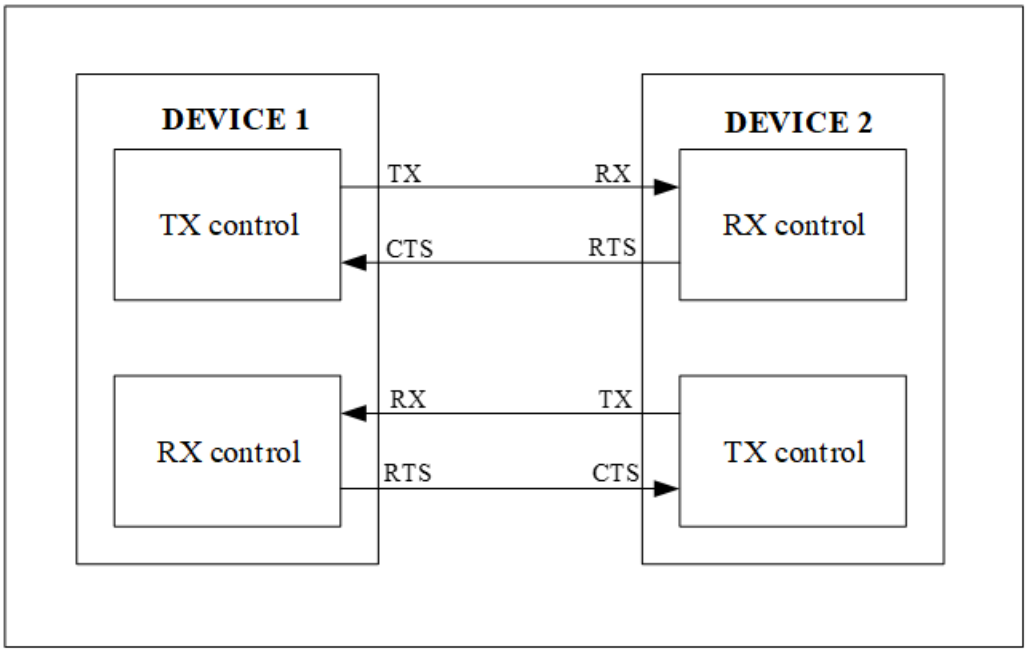
Figure 34-6 Receiving with DMA



34.4.7 Hardware flow control

Hardware flow control functions through CTS input and RTS output. The following figure shows how two devices are connected in this mode.

Figure 34-7 Hardware flow control between two LPUART



RTS and CTS flow control can be independently enabled by setting LPUART_CTRL.RTSEN and LPUART_CTRL.CTSEN.

34.4.7.1 RTS flow control

If RTS flow control is enabled (LPUART_CTRL.RTSEN =1), the RTS will be driven high (active) when the RTS

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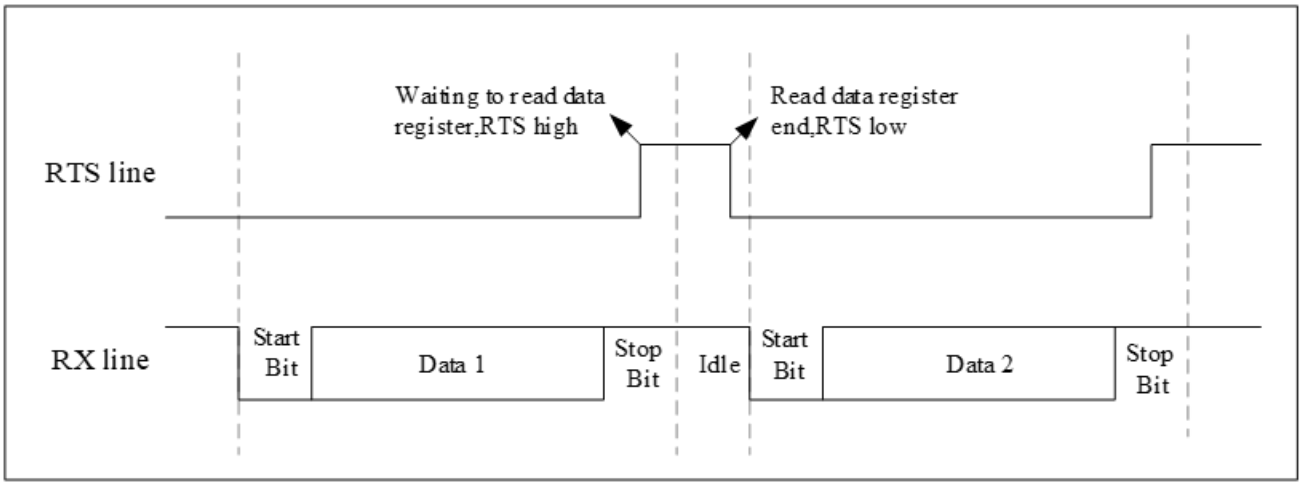
threshold condition is achieved, otherwise it will be driven low.How is the RTS valid can be selected by the LPUART_CTRL.RTST[1:0] bits. The RTS threshold can be selected to be effective when the FIFO is half full, 3/4 full, or full. Below is an example of communication with RTS flow control enabled.

Figure 34-8 RTS flow control



34.4.7.2 CTS flow control

If CTS flow control is enabled (LPUART_CTRL.CTSEN=1), the sender will check the CTS pin to decide whether or not send data before sending the next frame. If the CTS is pulled low (valid), the sender sends data (assuming that data is ready to be sent). If the CTS is pulled up during transmission, the transmission of the current data frame is stopped after transmission.

If CTS flow control is enabled (LPUART_CTRL.CTSEN=1), the signal of CTS pin will be changed. See Figure 34-9 for enabling CTS flow control.

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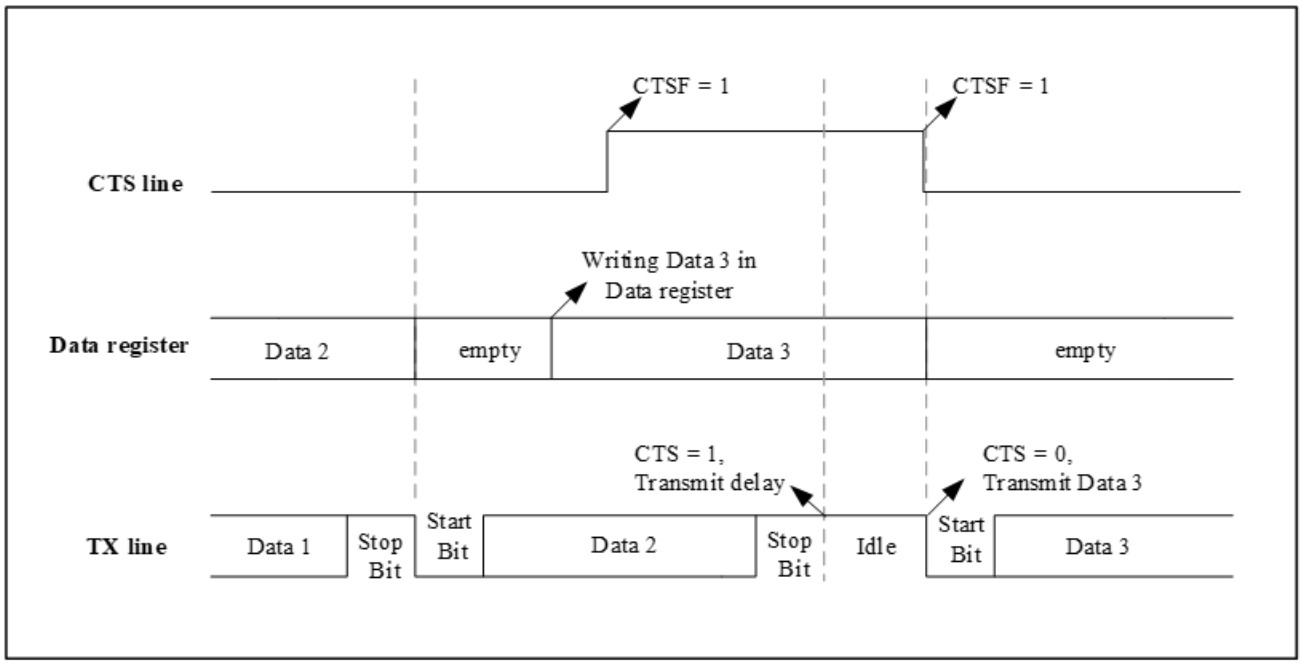
Figure 34-9 CTS flow control



34.4.8 Low power wake up

LPUART can work in STOP0/2 mode, if the LPUART_CTRL.WUSTPEN is set, it can wake up the system on EXTI when a specific waking up event occurs.

The LPUART waking up event can be handled in the following ways (through the LPUART_CTRL.WUS[5:0]) :

- A waking up event is generated when a start bit is detected
- A waking up event is generated when the receive buffer non-empty flag is set
- A waking up event is generated when data is received and the first byte matches LPUART_WUDAT1[7:0]
- A waking up event is generated when data is received and four bytes match LPUART_WUDAT1 [31:0]
- A waking up event is generated when data is received and four bytes match LPUART_WUDAT2[31:0]
- A waking up event is generated when data is received match Configurable Received Byte

When waking up event occurs, the LPUART_STS.WUF bit will be set.

34.5 Interrupt request

Table 34-6 LPUART interrupt requests

Interrupt	Interrupt event	Event flag	Enable bit
LPUART global interrupt	Parity check error	PCEF	PCEIEN
	TX complete	TXCF	TXCIEN
	Receive buffer overrun	RXFOF	RXFOIEN
	Receive buffer full	RXFFF	RXFFIEN

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	Receive buffer half full	RXFHFF	RXFHFIEN
	Receive buffer not empty	RXFNEF	RXFNEIEN
	Wake up in STOP mode	WUF	WUIEN
	Transmit buffer overrun	TXFOF	TXFOIEN
	Transmit buffer full	TXFFF	TXFFIEN
	Transmit buffer quarter Full	TXFQFF	TXFQFIEN
	Transmit buffer half full	TXFHFF	TXFHFIEN
	Transmit buffer not empty	TXFNEF	TXFNEIEN
	Idle frame detected	IDLEF	IDLEFIEN
	Frame error detected	FE	FEIEN
	Transmit buffer empty flag	TXFEF	TXFEIEN

LPUART interrupt events are logical OR. If the corresponding enable control bit is set, these events can generate their own interrupt, but only one interrupt request can be generated at the same time.

34.6 LPUART Registers

34.6.1 LPUART status register(LPUART_STS)

Address offset: 0x0000

Reset value: 0x0001 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															TXFEF
							r								r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEF	IDLEF	TXFNEF	TXFHFF	TXFQFF	TXFFF	TXFOF	NEF	WUF	CTSF	RXFNEF	RXFHFF	RXFFF	RXFOF	TXCF	PCEF
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	r	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	TXFEF	Transmit FIFO Empty Flag 0: FIFO is non-empty 1: FIFO is empty. TX Data is ready for transmitting note: when LPUART_CTRL. TXEN is 1 and writing LPUART_TXDAT register.
15	FE	Frame Error Detected 0:don't detect frame error 1:detect frame error
14	IDLEF	IDLE Frame Detected 0:don't detect idle frame 1:detect idle frame

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Bit field	Name	Description
13	TXFNEF	Transmit FIFO Non-Empty Flag 0: FIFO is empty 1: FIFO is non-empty. TX Data is ready for transmitting note: TXFNEF will clear to 0, when TLPUART_CTRL. FTXF register is 1.
12	TXFHFF	Transmit FIFO Half Full Flag 0: FIFO is not yet Half Full 1: FIFO is Half-Full. Should transmit TX Data Before It is Full note: TXFHFF will clear to 0, when TLPUART_CTRL. FTXF register is 1.
11	TXFQFF	Transmit FIFO quarter Full Flag 0: FIFO is not yet quarter Full 1: FIFO is three-QUAR-Full. Should transmit TX Data Before It is Full note: TXFQFF will clear to 0, when TLPUART_CTRL. FTXF register is 1.
10	TXFFF	Transmit FIFO Full Flag 0: FIFO is not yet Full 1: FIFO is Full. Should transmit TX Data to be ready for transmitting New Data note: TXFFF will clear to 0, when TLPUART_CTRL. FTXF register is 1.
9	TXFOF	Transmit FIFO Overflow Flag 0: FIFO is not overflow 1: FIFO is overflow note: TXFOF will clear to 0, when TLPUART_CTRL. FTXF register is 1.
8	NEF	Noise Error Flag This bit is set by hardware when noise is detected on a received frame. It is cleared by software, writing 1 to this bit 0: No noise is detected 1: Noise is detected
7	WUF	Wakeup From Stop2 mode Flag 0: No Wakeup Events Detected 1: Wakeup Events Detected
6	CTSF	CTS signal (hardware flow control) flag Ready to Receive Data once the transmitter requested to send data 0: CTS line is reset. 1: CTS line is set.
5	RXFNEF	Receive FIFO Non-Empty Flag 0: FIFO is empty 1: FIFO is non-empty. RX Data is ready for Reading note: RXFNEF will clear to 0, when LPUART_CTRL.FRXF register is 1, automatically cleared when FIFO is empty.
4	RXFHFF	Receive FIFO Half Full Flag 0: FIFO is not yet Half Full 1: FIFO is Half-Full. Should Read RX Data Before It is Full note: RXFHFF will clear to 0, when LPUART_CTRL.FRXF register is 1
3	RXFFF	Receive FIFO Full Flag

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Bit field	Name	Description
		0: FIFO is not yet Full 1: FIFO is Full. Should Read RX Data to be ready for Receiving New Data note: RXFFF will clear to 0, when LPUART_CTRL.FRXF register is 1
2	RXFOF	Receive FIFO Overflow Flag 0: FIFO is not overflow 1: FIFO is overflow note: RXFOF will clear to 0, when LPUART_CTRL.FRXF register is 1.
1	TXCF	TX Complete Flag 0: TX is not enabled or not yet completed 1: TX Transmission is Done
0	PCEF	Parity Check Error Flag 0: No parity error is detected 1: TX/RX Parity Error is Detected

34.6.2 LPUART interrupt enable register (LPUART_INTEN)

Address offset: 0x0004

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TXFEIEN	FEIEN	IDLEFIEN	TXFNEIEN	TXFHFIEN	TXFQFIEN	TXFFIEN	TXFOIEN	WUIEN	RXFNEIEN	RXFHFIEN	RXFFIEN	RXFOIEN	TXCIEN	PCEIEN
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	TXFEIEN	TXFIFO Empty Interrupt Enable 0: Disable TXFIFO Empty Interrupt 1: Enable TXFIFO Empty Interrupt
13	FEIEN	FRAME_ERROR Interrupt Enable 0: Disable FRAME_ERROR Interrupt 1: Enable FRAME_ERROR Interrupt
12	IDLEFIEN	IDLE_FRAMEIE Interrupt Enable 0: Disable IDLE_FRAMEIE Interrupt 1: Enable IDLE_FRAMEIE Interrupt
11	TXFNEIEN	TXFIFO Non-Empty Interrupt Enable 0: Disable TXFIFO Non-Empty Interrupt 1: Enable TXFIFO Non-Empty Interrupt

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Bit field	Name	Description
10	TXFHFIEN	TXFIFO Half Full Interrupt Enable 0: Disable TXFIFO Half-Full Interrupt 1: Enable TXFIFO Half-Full Interrupt
9	TXFQFIEN	TXFIFO QUAR Full Interrupt Enable 0: Disable TXFIFO three-QUAR-Full Interrupt 1: Enable TXFIFO three-QUAR-Full Interrupt
8	TXFFIEN	TXFIFO Full Interrupt Enable 0: Disable TXFIFO Full Interrupt 1: Enable TXFIFO Full Interrupt
7	TXFOIEN	TXFIFO Overflow Interrupt Enable 0: Disable TXFIFO Overflow Interrupt 1: Enable TXFIFO Overflow Interrupt
6	WUIEN	Wakeup Interrupt Enable 0: Disable Wakeup Interrupt 1: Enable Wakeup Interrupt
5	RXFNEIEN	Receive FIFO Non-Empty Interrupt Enable 0: Disable FIFO Non-Empty Interrupt 1: Enable FIFO Non-Empty Interrupt
4	RXFHFIEN	Receive FIFO Half Full Interrupt Enable 0: Disable FIFO Half-Full Interrupt 1: Enable FIFO Half-Full Interrupt
3	RXFFIEN	Receive FIFO Full Interrupt Enable 0: Disable FIFO Full Interrupt 1: Enable FIFO Full Interrupt
2	RXFOIEN	Receive FIFO Overflow Interrupt Enable 0: Disable FIFO Overflow Interrupt 1: Enable FIFO Overflow Interrupt
1	TXCIEN	TX Complete Interrupt Enable 0: Disable TX Complete Interrupt 1: Enable TX Complete Interrupt
0	PCEIEN	Parity Check Error Interrupt Enable 0: Disable Parity Error Interrupt 1: Enable Parity Error Interrupt

34.6.3 LPUART control register (LPUART_CTRL)

Address offset: 0x0008

Reset value: 0x0000 0200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							RXEN	RXNUMWU[4:0]					FTXF	IDLEFEN	SSM

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			r				rw			rw				rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
WUS[3:0]				RTSEN	CTSEN	RTST[1:0]		WUSTPEN	DMARXEN	DMATXEN	LB	PC	FRXF	TXEN	PEN	
rw				rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
24	RXEN	RX Enable 0: Disable 1: Enable RX
23:19	RXNUMWU[4:0]	A configurable receive byte means that there is a configuration byte, which can be configured to receive how many bytes of data to wakeup.NUM=(RXNUMWU +1)
18	FTXF	Flush Transmit TXFIFO 0: Disable 1: Enable to Flush TXFIFO Content
17	IDLEFEN	Idle Frame Detect Enable 0:disable 1:enable
16	SSM	Specify the Sampling Method 0: 3 Sample bit => Allow Noise Detection (LPUART_BRCFG1 should be large enough, e.g., >10) 1: 1 Sample => Disable Noise Detection
15:12	WUS[3:0]	Wakeup Event Selection. Specify the event which activates the WUF (wakeup from Stop2 mode flag) 0001: RXNE Detection 0010: A Configurable Received Byte 0011: A Programmed 2-Byte Frame 0100: A Programmed 3-Byte Frame 0101: A Programmed 4-Byte Frame 0110: A Programmed 5-Byte Frame 0111: A Programmed 6-Byte Frame 1000: A Programmed 7-Byte Frame 1001: A Programmed 8-Byte Frame 1010：Configure how many bytes to receive(1-32 Bytes) 1011: Start Bit Detection
11	RTSEN	Hardware Flow Control RX Enable 0: Disable 1: Enable
10	CTSEN	Hardware Flow Control TX Enable 0: Disable 1: Enable

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Bit field	Name	Description
9:8	RTST[1:0]	RTS Threshold 00: RTS = FIFO Half Full 10: RTS = FIFO Full x1: RTS = FIFO 3/4 Full
7	WUSTPEN	LPUART Wakeup Enable in Stop2 mode 0: Not able to Wakeup in Stop2 mode 1: Able to Wakeup in Stop2 mode
6	DMARXEN	DMA RX Request Enable
5	DMATXEN	DMA TX Request Enable
4	LB	LoopBack Self-Test 0: Normal 1: Loop Back Test (RXD connected to TXD)
3	PC	Parity Control 0: Enable Parity Bit 1: Disabled Parity Bit
2	FRXF	Flush Receiver FIFO 0: Disable 1: Enable to Flush FIFO Content
1	TXEN	TX Enable 0: Disable 1: Enable TX
0	PEN	Odd Parity Bit Enable 0: Even Parity Bit 1: Odd Parity Bit

34.6.4 LPUART baud rate configuration register 1 (LPUART_BRCFG1)

Address offset: 0x000C

Reset value: 0x0000 0174

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRP[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	BRP[15:0]	Baud Rate Parameter Register.

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Bit field	Name	Description
		Calculate Baud Rate Parameter Register as follows: Baud Rate 9600bps and Clock Frequency 32768Hz. BRP = 32768/9600 = 3.4133 Then BRP = 3. It is noted that in this case, the fraction part 0.4133 is significant compared to the integer part (3). The Modulation Control Register should be used for baud rate error correction. 1 bit sample method should also be employed to avoid sampling errors since BRP is not large enough for 3 bit sampling method with noise detection feature.

34.6.5 LPUART Transmit data register (LPUART_TXDAT)

Address offset: 0x0010

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DAT[7:0]							
r								rw							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DAT[7:0]	Write to Data Register for TXFIFO

34.6.6 LPUART baud rate configuration register 2 (LPUART_BRCFG2)

Address offset: 0x0014

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MCR[7:0]							
r								rw							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
7:0	MC[7:0]	Modulation Control Register For Baud Rate Error Correction at Low Frequency. For example: Baud Rate 4800bps and Clock Frequency 32768Hz. BRP = 32768/4800 = 6.8266 Then BRP = 6. The fraction part 0.8266 is significant compared to the integer part (6). To correct baud rate error, the Modulation Control Register should be used in this case

34.6.7 LPUART wake up data register 1 (LPUART_WUDAT1)

Address offset: 0x0018

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAT[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[31:0]															
rw															

Bit field	Name	Description
31:0	DAT[31:0]	Configure this register to detect byte or frame match for wakeup CPU from Stop2 mode First byte is used for byte match wakeup All 4 bytes are used for frame match wakeup {byte4,byte3,byte2,byte1}

34.6.8 LPUART wake up data register 2 (LPUART_WUDAT2)

Address offset: 0x001C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAT[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[31:0]															
rw															

Bit field	Name	Description
31:0	DAT[31:0]	Configure this register to detect byte or frame match for wakeup CPU from Stop2 mode

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Bit field	Name	Description
		First byte is used for byte match wakeup All 4 bytes are used for frame match wakeup {byte8,byte7,byte6,byte5}

34.6.9 LPUART Receive data register (LPUART_RXDAT)

Address offset: 0x0020

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DAT[7:0]							
r								r							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DAT[7:0]	Read this register to read RX data from RX FIFO

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35 Inter-Integrated Circuit Interface (I2C)

The I2C is a simple two-wire serial protocol used to communicate between two devices or chips in an embedded system. I2C has two lines SCL and SDA, SCL is used for clock and SDA is used for data.

35.1 Introduction

This I2C has multimaster capabilities, control I2C sequences, protocols, arbitration, interrupts and timing. It supports Standard-mode (Sm), Fast-mode (Fm), Fast-mode Plus (Fm+), and High-Speed (HS).

SMBus (system management bus) and PMBus (power management bus) are supported. DMA also used to reduce CPU load.

35.2 Main Features

The main features supported are shown below:

- I2C bus specification rev 3 compatibility:
  - Slave and master modes
  - Multi master
  - Standard-mode (up to 100 kHz)
  - Fast-mode (up to 400 kHz)
  - Fast-mode Plus (up to 1 MHz)
  - High speed mode (up to 3.4 MHz)
  - 7-bit and 10-bit addressing mode
  - Multiple 7-bit slave addresses (2 addresses, 1 with configurable mask)
  - All 7-bit addresses acknowledge mode
  - General call, Programmable setup and hold times
  - Interrupt & clock stretching
- SMBus specification rev 3.0 compatibility:
  - Hardware CRC (Packet Error Checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and Device support
  - SMBus alert
  - Timeouts and idle condition detection
  - PMBus rev 1.3 standard

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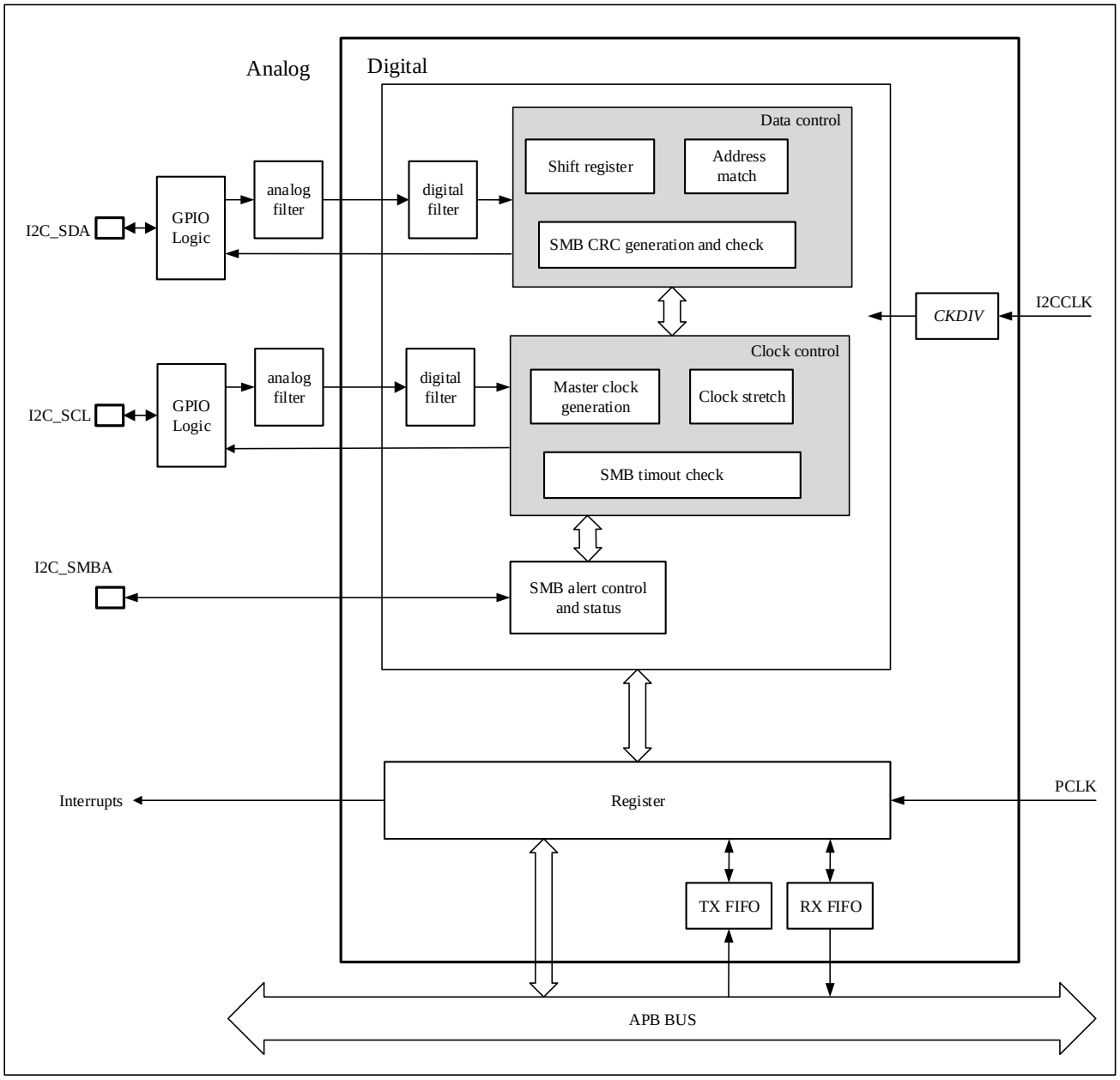
Others feature:

- Programmable up to 8-bytes buffer/burst with DMA
- Programmable analog and digital noise filters
- Independent clock sources allowing the I2C communication speed to be independent from the i2c_pclk reprogramming

35.3 Block Diagram

Figure 35-1 I2C Block Diagram



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35.4 Function Description

35.4.1 Clock requirements

PCLK: used to access I2C registers, I2C1\2\3 is PCLK1, I2C4\5\6 is PCLK2, I2C7\8\9\10 is PCLK5.

I2CCLK: used as the I2C kernel clock, and is independent of PCLK, This clock can be selected from the following four clock sources:

- Sys_bus_div_clk after divider clock (default)
- PLL3C clock
- HSI clock
- MSI clock

The I2CCLK can also be further divided by the I2C_BUSTM.CKDIV(high speed mode by I2C_HSBUSTM.CKDIV), the divided clock is fCKDIV.

Note: The max fCKDIV frequency is 8 MHz for SCL=100kHz to 1MHz, the max fCKDIV frequency is 48 MHz for SCL=3.4MHz.

35.4.2 I2C Mode & transfer flow

The I2C can operate in one of the modes:

- Slave transmitter
- Slave receiver
- Master transmitter
- Master receiver

By default, it is in slave mode. It switches to master when it generates a START condition, and from master to slave if an arbitration loss or a STOP generation occurs, allowing multimaster capability.

In Master mode, the I2C initiates data transfer and generates clock signal. A transfer always begins with a START condition and ends with a STOP condition, which are generated by software.

In Slave mode, the I2C ACK its own addresses (7 or 10-bit), and General Call address. The reserved SMBus addresses can also be enabled by software.

Data and addresses are transferred as 8-bit bytes, MSB first. The first byte(s) after the START condition is the address (one in 7-bit mode, two in 10-bit mode). Address is always send in Master mode.

A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter.

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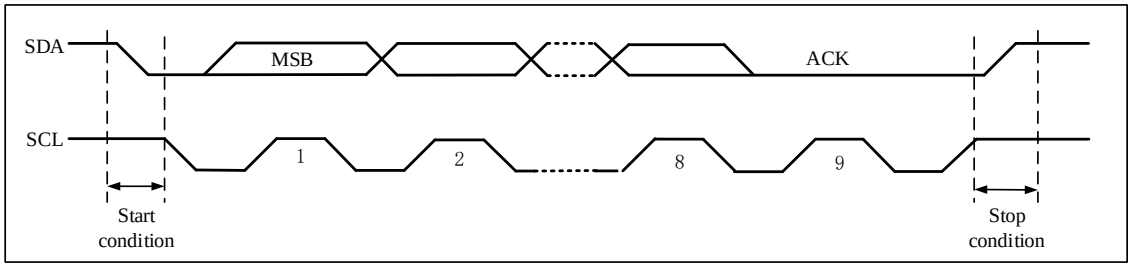
Figure 35-2 I2C Bus Protocol



35.4.2.1 I2C initialization

Enabling and disabling the peripheral

The I2C is enabled by setting the I2CEN bit in the I2C_CTRL1 register.

When the I2C is disabled (I2CEN=0), it performs a software reset.

Software reset

A software reset can be performed by clearing the I2CEN bit in the I2C_CTRL1 register, I2C lines SCL and SDA are released. communication control bits, status bits and states machines are reset. The configuration registers are not impacted. I2CEN need to be low for 3 pclk cycles or 3 fCKDIV cycles whichever is longer to be effective.

The following register bits are reset:

1. I2C_CTRL2 register: START, STOP, NAK

2. I2C_STSINT register: BUSY, WRE, WRAVL, RDAVL, ADR, NAKF, TFCR, TFC, STOPF, BSER, ABLO, OVF

and in addition when the SMBus feature is supported:

1. I2C_CTRL2 register: CRCBYTE

2. I2C_STSINT register: CRCERR, TMOUT, ALRT

I2C timings

The timings is configured to get correct data hold and setup time, used in master and slave modes. This is done by programming the CKDIV[3:0], DSCL[3:0] and DSDA[3:0] bits in the I2C_BUSTM register. Additional I2C_HSBUSTM setting also needed if using HS Mode.

Noise filters

The analog noise filter suppress glitch up to 35ns, controlled by AFOFF and GFLTRCTRL register.

If digital noise filter is enabled, the level of the SCL or the SDA line is internally changed only if it stable for more than DF10 x I2CCLK periods. This allows spikes with a programmable length of 1 to 15 I2CCLK periods to be suppressed.

35.4.2.2 Data transfer

Reception

The SDA input fills the shift register. After the 8th SCL pulse (when the complete data byte is received), the shift register is copied into I2C_RDR register if it is empty (RDAVL=0). If RDAVL=1, meaning that the previous received

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data byte has not yet been read, the SCL line is stretched low until I2C_RDR is read. The stretch is inserted between the 8th and 9th SCL pulse (before the Acknowledge pulse).

Transmission

If the I2C_WDR register is not empty (WRE=0), its content is copied into the shift register after the 9th SCL pulse (the Acknowledge pulse). Then the shift register content is shifted out on SDA line. If WRE=1, meaning that no data is written yet in I2C_WDR, SCL line is stretched low until I2C_WDR is written. The stretch is done after the 9th SCL pulse.

35.4.3 Hardware transfer management

The I2C has a byte counter in hardware to manage byte transfer and control functions such as:

- NAK, STOP and ReSTART generation in master mode
- ACK control in slave receiver mode
- CRC generation/checking for SMBus

The byte counter is always used in master mode, default it is disabled in slave mode, but can be enabled by setting the SBCTL (Slave Byte Control) bit in the I2C_CTRL2 register.

The number of bytes to be transferred is programmed in the BYTECNT[7:0] bit field in the I2C_CTRL2 register. If the number of bytes to be transferred (BYTECNT) is greater than 255, or if a receiver wants to control the acknowledge value of a received data byte, the refill mode must be selected by setting the REFILL bit in the I2C_CTRL2 register. In this mode, TFCR flag is set when the number of bytes programmed in BYTECNT has been transferred, and an interrupt is generated if TFCIE is set. SCL is stretched if TFCR flag is set. TFCR is cleared when BYTECNT is written to a non-zero value.

When the BYTECNT counter is refilled with the last number of bytes, REFILL bit must be cleared.

When REFILL=0 in master mode, the counter can be used in 2 modes:

Automatic stop mode (AUTOSTOP = '1' in the I2C_CTRL2 register). In this mode, the master automatically sends a STOP condition after the number of bytes in the BYTECNT[7:0] has been transferred.

Software stop mode (AUTOSTOP = '0' in the I2C_CTRL2 register). Once the number of bytes in the BYTECNT[7:0] has been transferred, software action is expected; the TFC flag is set and an interrupt is generated if the TFCIE bit is set. The SCL signal is stretched if the TFC flag is set. The TFC flag is cleared when the START or STOP bit is set in the I2C_CTRL2 register. This mode must be used when the master wants to send a RESTART.

35.4.4 I2C slave mode

35.4.4.1 I2C slave initialization

Minimum one slave address must be enabled. I2C_ADR1 and I2C_ADR2 are for the slave own addresses AD1 and AD2.

AD1 can be configured either in 7-bit mode or 10-bit addressing mode by with AD1MODE in I2C_ADR1 and set

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AD1EN bit.

If additional slave addresses are required, the 2nd slave address AD2 can be configured and set AD2EN.

Up to 7 AD2 LSB can be masked by configuring the AD2MSK[2:0] bits in the I2C_ADR2 register.

For AD2MSK = 1 to 6, only AD2[7:2], AD2[7:3], AD2[7:4], AD2[7:5], AD2[7:6] or AD2[7] are compared with the received address, excludes reserved addresses (0000 XXX and 1111 XXX).

If AD2MSK=7, all received 7-bit addresses are acknowledged (except reserved addresses).

These reserved addresses can be acknowledged if they are enabled by the specific enable bit, if they are programmed in the I2C_ADR1 or I2C_ADR2 register with AD2MSK=0.

The General Call address is enabled by setting the GENC bit in the I2C_CTRL1 register.

When the I2C is selected by one of its enabled addresses, the ADR interrupt status flag is set, and an interrupt is generated if the ADRIE bit is set.

By default, the slave stretches the SCL signal at low level when needed, in order to perform software actions. If the master does not support clock stretching, the I2C must be configured with NOSTRCH=1 in the I2C_CTRL1 register.

At ADR interrupt, if several addresses are enabled, read ADRRCV[6:0] bits in the I2C_STSINT register to check which address matched. DIR flag is the transfer direction.

Slave clock stretching (NOSTRCH = 0)

In default mode, the I2C slave stretches the SCL clock in this conditions:

When the ADR flag is set: the received address matches with one of the enabled slave addresses. This stretch is released when the ADR flag is cleared by setting ADRCLR bit.

In transmission, if the previous data transmission is completed and no new data is written in I2C_WDR register, or if the first data byte is not written when the ADR flag is cleared (WRE=1). This stretch is released when the data is written to the I2C_WDR register.

In reception when the I2C_RDR register is not read yet and a new data reception is completed. This stretch is released when I2C_RDR is read.

When TFCR = 1 in Slave Byte Control mode, refill mode (SBCTL=1 and REFILL=1), means last data byte transferred. This stretch is released when then TFCR is cleared by writing non-zero to BYTECNT[7:0].

After SCL falling edge detection, the I2C stretches SCL low.

Slave without clock stretching (NOSTRCH = 1)

When NOSTRCH = 1 in the I2C_CTRL1 register, the I2C slave does not stretch the SCL signal.

The SCL clock is not stretched while the ADR flag is set.

In transmission, the data must be written in the I2C_WDR register before the first SCL pulse corresponding to its transfer occurs. If not, an underrun occurs, the OVF flag is set in the I2C_STSINT register and an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register. The OVF flag is also set when the first data transmission starts and the STOPF bit is still set (has not been cleared). Therefore, if the user clears the STOPF flag of the previous transfer only after writing the first data to be transmitted in the next transfer, he ensures that the OVF status is provided,

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even for the first data to be transmitted.

In reception, the data must be read from the I2C_RDR register before the 9th SCL pulse (ACK pulse) of the next data byte occurs to prevent overrun.

35.4.4.2 Slave byte control mode

In order to allow byte ACK control in slave reception mode, Slave Byte Control mode must be enabled by setting the SBCTL bit in the I2C_CTRL1 register. This is required to be compliant with SMBus standards.

Refill mode must be selected in order to allow byte ACK control in slave reception mode (REFILL=1). To get control of each byte, BYTECNT must be initialized to 0x1 in the ADR interrupt subroutine, and refilled to 0x1 after each received byte. When the byte is received, the TFCR bit is set, stretching the SCL signal low between the 8th and 9th SCL pulses. The user can read the data from the I2C_RDR register, and then decide to acknowledge it or not by configuring the ACK bit in the I2C_CTRL2 register. The SCL stretch is released by programming BYTECNT to a non-zero value: the ACK or NAK is sent and next byte can be received.

BYTECNT can be loaded with a value greater than 0x1, and in this case, the reception flow is continuous during BYTECNT data reception.

Limitation:

Slave byte Ack control which require SCL stretch before ACK is not supported in high speed mode due to not allowed to stretch SCL at bit 9.

Also, it is only for Slow CPU which is late in clearing RDAVL/TFCR,

For fast CPU/pclk which can clear the RDAVL in less than 1 tCKDIV, this feature will not work.

35.4.4.3 Slave transmitter

A transmit interrupt status (WRAVL) is generated when the I2C_WDR register becomes empty. An interrupt is generated if the WDRIE bit is set in the I2C_CTRL1 register.

The WRAVL bit is cleared when the I2C_WDR register is written with the next data byte to be transmitted.

When a NAK is received, the NAKF bit is set in the I2C_STSINT register and an interrupt is generated if the NAKIE bit is set in the I2C_CTRL1 register. The slave automatically releases the SCL and SDA lines in order to let the master perform a STOP or a RESTART condition. The WRAVL bit is not set when a NAK is received.

When a STOP is received and the STOPIE bit is set in the I2C_CTRL1 register, the STOPF flag is set in the I2C_STSINT register and an interrupt is generated. In most applications, the SBCTL bit is usually programmed to '0'. In this case, If WRE = 0 when the slave address is received (ADR=1), the user can choose either to send the content of the I2C_WDR register as the first data byte, or to flush the I2C_WDR register by setting the WRE bit in order to program a new data byte.

In Slave Byte Control mode (SBCTL=1), the number of bytes to be transmitted must be programmed in BYTECNT in the address match interrupt subroutine (ADR=1). In this case, the number of WRAVL events during the transfer corresponds to the value programmed in BYTECNT.

When NOSTRCH=1, the SCL clock is not stretched while the ADR flag is set, so the user cannot flush the I2C_WDR

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register content in the ADR subroutine, in order to program the first data byte. The first data byte to be sent must be previously programmed in the I2C_WDR register:

This data can be the data written in the last WRAVL event of the previous transmission message.

If this data byte is not the one to be sent, the I2C_WDR register can be flushed by setting the WRE bit in order to program a new data byte. The STOPF bit must be cleared only after these actions, in order to guarantee that they are executed before the first data transmission starts, following the address acknowledge.

If STOPF is still set when the first data transmission starts, an underrun error is generated (the OVF flag is set).

If a WRAVL event is needed, (Transmit Interrupt or Transmit DMA request), the user must set the WRAVL bit in addition to the WRE bit, in order to generate a WRAVL event

35.4.4.3.1 Example sequence to transmit

For example: SCL=1MHz, I2CCLK=8MHz, transmit 4 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_CTRL1 write (h000100ff)**
   NOSTRCH=0; SBCTL=1; I2CEN=1; All interrupt Enable.
3. **I2C_CTRL2 write (h00040000)**
   BYTECNT=0x4; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
4. **I2C_ADR2 write (h00008066)**
   AD2MSK=000(No mask); 7 bits address enabled; I2C slave address=7'b0110011;
5. **Wait for interrupt, read I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
6. **Wait for interrupt, read I2C_STSINT**
   if WRAVL bit is set to 1, write 1st data to I2C_WDR
7. **Wait for interrupt, read I2C_STSINT**
   if WRAVL bit is set to 1, write 2nd data to I2C_WDR
8. **Repeat the same for 3rd and 4th last data**

35.4.4.3.2 Example sequence to transmit, no stretch

For example: SCL=1MHz, I2CCLK=8MHz, transmit 4 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_CTRL1 write (h000200ff)**
   NOSTRCH=1; SBCTL=0; I2CEN=1; All interrupt Enable.
3. **I2C_WDR write 1st data**

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When clock stretch is disabled, need to write 1st data before START condition or Slave address received/ACKed

4. **I2C_CTRL2 write (h00040000)**
   BYTECNT=0x4; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
5. **I2C_ADR2 write (h00008066)**
   AD2MSK=000(No mask); 7 bits address enabled; I2C slave address=7'b0110011;
6. **Wait for interrupt, read I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
7. **Wait for interrupt, read I2C_STSINT**
   if WRAVL bit is set to 1, write 2nd data to I2C_WDR
8. **Repeat the same for 3rd and 4th last data**
9. **Wait for interrupt, read I2C_STSINT**
   if WRAVL bit is set to 1, write 5th data to I2C_WDR
   Note: Since BYTECNT is configured as 4, WRAVL will be set 4 times("number of WRAVL" = BYTECNT). WRAVL will be set one more time but the extra 5th data written to I2C_WDR will not be send out if slave get NACKed at 4th data)

35.4.4.3.3 Example sequence to transmit via TX FIFO

For example: SCL=1MHz, I2CCLK=8MHz, transmit 4 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_CTRL1 write (hC00100ff)**
   NOSTRCH=0; SBCTL=1; I2CEN=1; All interrupt Enable(include FIFO interrupt).
3. **I2C_FIFOCSR write (hC8080000)**
   TFE=1; RFE=1; TXILEVEL=8; RXILEVEL=8.
4. **I2C_CTRL2 write (h00040000)**
   BYTECNT=0x4; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
5. **I2C_ADR2 write (h00008066)**
   AD2MSK=000(No mask); 7 bits address enabled; I2C slave address=7'b0110011;
6. **Wait for interrupt, read I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
7. **Wait for interrupt, read I2C_STSINT**
   if FTXIS bit is set to 1, write 1st data to I2C_WDR, write 2nd data to I2C_WDR, write 3rd data to I2C_WDR, write 4th data to I2C_WDR; Slave get NACKed at 4th data
   Note: FTXIS interrupt flag will be auto cleared

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35.4.4.3.4 Example sequence to transmit via TX FIFO, no stretch

For example: SCL=1MHz, I2CCLK=8MHz, transmit 4 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_CTRL1 write (hC00200ff)**
   NOSTRCH=1; SBCTL=0; I2CEN=1; All interrupt Enable(include FIFO interrupt).
3. **I2C_WDR write 1st data**
   When clock stretch is disabled, need to write 1st data before I2C_FIFOCSR.TFE set 1
4. **I2C_FIFOCSR write (hC8080000)**
   TFE=1; RFE=1; TXILEVEL=8; RXILEVEL=8.
5. **I2C_CTRL2 write (h00040000)**
   BYTECNT=0x4; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
6. **I2C_ADR2 write (h00008066)**
   AD2MSK=000(No mask); 7 bits address enabled; I2C slave address=7'b0110011;
7. **Wait for interrupt, read I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
8. **Wait for interrupt, read I2C_STSINT**
   if FTXIS bit is set to 1, write 2nd data to I2C_WDR, write 3rd data to I2C_WDR, write 4th data to I2C_WDR, write 5th data to I2C_WDR
   Note: This extra 5th byte will not send out if slave get NACKed at 4th data

35.4.4.4 Slave receiver

RDAVL is set in I2C_STSINT when the I2C_RDR is full, and generates an interrupt if RDRIE is set in I2C_CTRL1. RDAVL is cleared when I2C_RDR is read.

When a STOP is received and STOPIE is set in I2C_CTRL1, STOPF is set in I2C_STSINT and an interrupt is generated.

35.4.4.4.1 Example sequence to receive via DMA

For example: SCL=100kHz, I2CCLK=8MHz, receive 4 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00012526)**
   CKDIV=0; DSCL=0; DSDA=0x1; HSCL=0x25; LSCL=0x26;
2. **I2C_ADR1 write (h00008066)**
   7 bits address enabled; I2C slave address=7'b0110011;
3. **I2C_CTRL1 write (h0001C001)**
   NOSTRCH=0; SBCTL=1; DMARDEN=1; DMAWREN=1; I2CEN=1.

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4. **I2C_CTRL2 write (h00040000)**
   BYTECNT=0x4; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
5. **Wait for interrupt, read I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
6. **dma_rx_req & dma_rx_ack sequence start**
   Hardware start receive 1st bytes from I2C bus and send it to DMA, this repeat for 2nd, 3rd and 4th bytes; No need to use RDAVL interrupt in DMA mode

35.4.5 I2C master mode

35.4.5.1 I2C master initialization

I2C master clock is configured by HSCL and LSCL in I2C_BUSTM register.

To support multi-master clock synchronization:

The low level of the clock is counted by LSCL counter, starting from the SCL low level internal detection.

The high level of the clock is counted by HSCL counter, starting from the SCL high level internal detection.

The I2C detects its own SCL low level after synchronization delay on the SCL falling edge, SCL input noise filters. The I2C releases SCL to high once the LSCL counter reaches the value in the LSCL[7:0] bits in the I2C_BUSTM register.

The I2C detects its own SCL high level after synchronization delay on the SCL rising edge, SCL input noise filters. The I2C ties SCL to low level once the HSCL counter is reached reaches the value in the HSCL[7:0] bits in the I2C_BUSTM register.

master clock period is:

$$tSCL = SYNC\ delay + \{[(HSCL+1) + (LSCL+1)] \times (CKDIV+1) \times tI2CCLK\}$$

The duration of synchronization delay depends on these parameters:

- SCL falling & rising slope
- Input delay induced by the analog+digital filter if enabled.
- Delay due to SCL synchronization with I2CCLK clock

Master communication initialization (address phase)

To start transfer, program this for the addressed slave in the I2C_CTRL2 register:

- Addressing mode (7-bit or 10-bit): ADR10
- Slave address to be sent: SADR[9:0]
- Transfer direction: RWN
- For 10-bit address read: HDR10 bit. HDR10 must be configure to indicate if the complete address sequence must be sent, or only the header if direction change.
- The number of bytes to be transferred: BYTECNT[7:0]. If the number of bytes is equal to or greater than 255

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bytes, BYTECNT[7:0] must initially be filled with 0xFF.

Set the START bit in I2C_CTRL2, the master is then sends the START condition followed by the slave address if bus is free (BUSY = 0) and after a delay of tBUF.

If arbitration loss, the master switches back to slave mode and acknowledge its own address if it is addressed.

In 10-bit addressing mode, when the Slave Address first 7 bits is NACKed by the slave, the master auto resend slave address until ACK is received, if NACK continue, set ADDRCF to stop sending slave address.

Set STOP bit to send STOP, or START to restart after Address NACKed.

Master receiver addressing a 10-bit address slave initialization

If the slave address is in 10-bit format, can choose to send the complete read sequence by clearing the HDR10 bit in the I2C_CTRL2, then the master automatically sends the following complete sequence after the START bit is set: (Re)Start + Slave address 10-bit header Write + Slave address 2nd byte + ReStart + Slave address 10-bit header Read

If the master addresses a 10-bit address slave, transmits data to this slave and then reads data from the same slave, a master transmission flow must be done first. Then a repeated start is set with the 10 bit slave address configured with HDR10=1. In this case the master sends this sequence: ReStart + Slave address 10-bit header Read.

35.4.5.2 Master transmitter

For write transfer, the WRAVL flag is set after each byte transmission, after the 9th SCL pulse when an ACK is received.

A WRAVL event generates an interrupt if the WDRIE bit is set in the I2C_CTRL1 register. The flag is cleared when the I2C_WDR register is written with the next data byte to be transmitted.

The number of WRAVL events during the transfer corresponds to the value programmed in BYTECNT[7:0]. If the total number of data bytes to be sent is greater than 255, refill mode must be selected by setting the REFILL bit in the I2C_CTRL2 register. When BYTECNT data have been transferred, the TFCR flag is set and the SCL line is stretched low until BYTECNT[7:0] is written non-zero.

The WRAVL flag is not set when a NAK is received.

When REFILL=0 and BYTECNT data have been transferred:

- In automatic stop mode (AUTOSTOP=1), a STOP is automatically sent.
- In software stop mode (AUTOSTOP=0), the TFC flag is set and the SCL line is stretched low to perform software actions:

  A RESTART condition can be requested by setting the START bit in the I2C_CTRL2 register with the correct slave address configuration, and number of bytes to be transferred. Setting the START bit clears the TFC flag and the START condition is sent on the bus.

  A STOP condition is requested by setting the STOP bit in the I2C_CTRL2 register. Setting the STOP bit clears the TFC flag and the STOP condition is sent on the bus.

If a NAK is received: the WRAVL flag is not set, and a STOP condition is automatically sent after the NAK reception, the NAKF flag is set in the I2C_STSINT register, and an interrupt is generated if NAKIE bit is set.

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35.4.5.2.1 Example sequence to transmit via TX FIFO

For example: SCL=1MHz, I2CCLK=8MHz, transmit 16 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_FIFOCSR write (hC8080000)**
   TFE=1; RFE=1; TXILEVEL=8; RXILEVEL=8.
3. **I2C_CTRL1 write (hC00000ff)**
   NOSTRCH=0; SBCTL=0; I2CEN=1; All interrupt Enable(include FIFO interrupt).
4. **I2C_CTRL2 write (h02102066)**
   AUTOSTOP=1; BYTECNT=16;NAK=0; STOP=0; START=1; ADR10=0; RWN=0; SADR=0x066.
5. **Wait 10us for configuration to complete**
6. **Wait for interrupt, read I2C_STSINT**
   if FTXIS bit is set to 1, write 1st data to I2C_WDR, write 2nd data to I2C_WDR…write 8th data to I2C_WDR.
7. **Wait for interrupt, read I2C_STSINT**
   if FTXIS bit is set to 1, write 9th data to I2C_WDR, write 10th data to I2C_WDR…write 16th data to I2C_WDR.
   Note: FTXIS interrupt flag will be auto cleared

35.4.5.2.2 Example sequence to transmit via HS mode

For example: SCL=3.4MHz, I2CCLK=48MHz, transmit 8 bytes

The communication flow is as follows:

1. **I2C_GFLTRCTRL write (h00000000)**
   Set to lower analog noise filter setting;
2. **I2C_HSBUSTM write (h00010207)**
   HS mode SCL=3.4MHz: HSCKDIV=0; HSDSCL=0; HSDSDA=1; HSHSCL=2; HSLSCL=7;
   Note: for HS mode(3.4MHz) used only, SCL High to low ratio ≈ 104:187
3. **I2C_BUSTM write (h80330309)**
   Fast mode SCL=267kHz: CKDIV=0; DSCL=3; DSDA=3; HSCL=0x03; LSCL=0x9;
4. **Wait 50us for configuration to complete**
5. **I2C_CTRL1 write (h000000ff)**
   NOSTRCH=0; SBCTL=0; I2CEN=1; All interrupt Enable.
6. **I2C_CTRL2 write (h0008200C)**
   BYTECNT=0x8; NAK=0; STOP=0; START=1; ADR10=0; RWN=0; SADR=0x00C (master code=00001xxx).
7. **Wait 50us for configuration to complete**
8. **I2C_CTRL2 write (h00082066)**

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BYTECNT=0x8; NAK=0; STOP=0; START=1(Send START condition); ADR10=0; RWN=0; SADR=0x066.

9. **Wait for interrupt, read I2C_STSINT**

   if WRAVL bit is set to 1, write 1st data to I2C_WDR

10. **Wait for interrupt, read I2C_STSINT**

    if WRAVL bit is set to 1, write 2nd data to I2C_WDR

11. **Repeat the same for 3rd to 8th last data**
12. **I2C_CTRL2 write (h00084066)**
    STOP=1(Send STOP condition); START=0;
    Note: If AUTOSTOP is set, there is no need to send a STOP condition by software and this step can be ignored

35.4.5.3 Master receiver

In read transfer, the RDAVL flag is set after each byte received, after the 8th SCL pulse. An RDAVL event generates an interrupt if RDRIE bit is set in the I2C_CTRL1 register. The flag is cleared when I2C_RDR is read.

If the total number of data bytes to be received is greater than 255, refill mode must be selected by setting the REFILL bit in the I2C_CTRL2 register. In this case, when BYTECNT[7:0] data have been transferred, the TFCR flag is set and the SCL line is stretched low until BYTECNT[7:0] is written to a non-zero value.

When REFILL=0 and BYTECNT[7:0] data have been transferred:

- In automatic end mode (AUTOSTOP=1), a NAK and a STOP are automatically sent after the last received byte.
- In software stop mode (AUTOSTOP=0), a NAK is automatically sent after the last received byte, the TFC flag is set and the SCL line is stretched low to allow software actions:

  A RESTART condition is requested by setting the START bit in the I2C_CTRL2 register with the correct slave address configuration, and number of bytes to be transferred. Setting the START bit clears the TFC flag and the START condition, followed by slave address, are sent on the bus.

  A STOP condition can be requested by setting the STOP bit in the I2C_CTRL2 register. Setting the STOP bit clears the TFC flag and the STOP condition is sent on the bus.

35.4.5.3.1 Example sequence to receive via RESTART

For example: SCL=1MHz, I2CCLK=8MHz, receive 8 bytes, send restart to receive another 2 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_CTRL1 write (h000000ff)**

   NOSTRCH=0; SBCTL=0; I2CEN=1; All interrupt Enable;
3. **I2C_CTRL2 write (h00082467)**
   AUTOSTOP=0; REFILL=0; BYTECNT=8; NAK=0;STOP=0; START=1; ADR10=0; RWN=1; SADR=0x067.

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4. **Wait for interrupt, read I2C_STSINT**

   if RDAVL bit is set to 1, read 1st data from I2C_RDR

5. **Wait for interrupt, read I2C_STSINT**

   if RDAVL bit is set to 1, read 2nd data from I2C_RDR

6. **Repeat the same for 3rd, 4th…8th data**

7. **Wait for interrupt, read I2C_STSINT**

   if TFC bit is set to 1, means 8 data bytes received

8. **I2C_CTRL2 write (h00022467)**
   AUTOSTOP=0; REFILL=0; BYTECNT=2(another 2 bytes); NAK=0;STOP=0; START=1(Send a Restart to clear the TFC); ADR10=0; RWN=1; SADR=0x067.
   Note: Any delay of clearing TFC=1 will stretch the SCL low

9. **Wait for interrupt, read I2C_STSINT**

   if RDAVL bit is set to 1, read 9th data from I2C_RDR

10. **Wait for interrupt, read I2C_STSINT**

    if RDAVL bit is set to 1, read 10th data from I2C_RDR

11. **I2C_CTRL2 write (h00024467)**
    STOP=1(Send STOP condition); START=0;

35.4.5.3.2 Example sequence to receive via RX FIFO

For example: SCL=1MHz, I2CCLK=8MHz, receive 10 bytes

The communication flow is as follows:

1. **I2C_BUSTM write (h00000102)**
   CKDIV=0; DSCL=0; DSDA=0; HSCL=0x1; LSCL=0x2;
2. **I2C_FIFOCSR write (hC8080000)**
   TFE=1; RFE=1; TXILEVEL=8; RXILEVEL=8.
3. **I2C_CTRL1 write (hC00000ff)**

   NOSTRCH=0; SBCTL=0; I2CEN=1; All interrupt Enable(include FIFO interrupt);
4. **I2C_CTRL2 write (h000A2467)**
   AUTOSTOP=0; REFILL=0; BYTECNT=10; NAK=0;STOP=0; START=1; ADR10=0; RWN=1; SADR=0x067.
5. **Wait 1us for configuration to complete**
6. **Wait for interrupt, read I2C_STSINT**

   if FRXNE bit is set to 1, read 1st data from I2C_RDR, read 2nd data from I2C_RDR…, read 8th data from I2C_RDR

7. **Choose one of the following methods**

   METHOD1: Wait for interrupt, read I2C_STSINT

   if FRXNE bit is set to 1, read 9th data from I2C_RDR, read 10th data from I2C_RDR

   Note: Last remaining bytes which less than RXILEVEL=8(last 2 bytes) will also get FRXNE=1 interrupt

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METHOD2: Poll waiting RXFLEVEL[3:0]

if RXFLEVEL=2, read 9th data from I2C_RDR, read 10th data from I2C_RDR

Note: Do this only after finished reading previous 8 bytes

METHOD3: Wait for interrupt, read I2C_STSINT

if TFC bit is set to 1, then set STOP=1, BYTECNT=2. Wait for STOPF=1 then read 9th data from I2C_RDR, read 10th data from I2C_RDR

Note: Do this only AUTOSTOP=0

35.4.6 I2C_BUSTM and I2C_HSBUSTIM examples

Examples of program the I2C_BUSTM and I2C_HSBUSTM with fI2CCLK = 48MHz

Table 35-1 Timing settings example

Register	**Register bit**	**Standard-mode (Sm)**	**Fast-mode (Fm)**	**Fast-mode Plus (Fm+)**	**HS-mode(Hm)**
		100kHz	**400kHz**	**1MHz**	**3.4MHz**
fCKDIV		8M	8M	8M	48M(1)
I2C_BUSTM	CKDIV	0x5	0x5	0x5	0x8
	DSCL	0x0	0x2	0x0	0x3
	DSDA	0x1	0x1	0x0	0x3
	HSCL	0x25	0x6	0x1	0x3
	LSCL	0x26	0x7	0x2	0x9
I2C_HSBUSTM	HSCKDIV	ignore			0x0(1)
	HSDSCL				0x0
	HSDSDA				0x1
	HSHSCL				0x2
	HSLSCL				0x7

Note(1): In high speed mode, fCKDIV = fI2CCLK/(HSCKDIV+1)

35.4.7 SMBus features

35.4.7.1 Bus protocols

The protocols are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read Word, Process Call, Block Read, Block Write and Block Write-Block Read Process Call.

Address resolution protocol (ARP)

This peripheral supports the Address Resolution Protocol (ARP). The SMBus Device Default Address (0b1100 001) is enabled by setting SMBD bit in I2C_CTRL1 register. The ARP commands is implemented by the software.

Arbitration is also performed in slave mode for ARP support.

Received Command and Data acknowledge control

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A SMBus receiver must be able to NAK each received command or data. In order to allow the ACK control in slave mode, Slave Byte Control mode is enabled by SBCTL bit in I2C_CTRL1 register.

Host Notify protocol

This peripheral supports the Host Notify protocol by setting the SMBH bit in the I2C_CTRL1 register, the host then acknowledges the SMBus Host Address (0b0001 000).

When this protocol is used, the device acts as a master and the host as a slave.

SMBus alert

A slave-only device can signal the host through the SMBA pin that it wants to talk. The host processes the interrupt and simultaneously accesses all SMBA devices through the Alert Response Address (0b0001 100). Only the device(s) which pulled SMBA low acknowledges the Alert Response Address.

When configured as a slave device(SMBH=0), the SMBA pin is pulled low by setting the ALRTEN bit in the I2C_CTRL1 register. The Alert Response Address is enabled at the same time.

When configured as a host (SMBH=1), the ALRT flag is set in the I2C_STSINT register when a falling edge is detected on the SMBA pin and ALRTEN=1. An interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register. When ALRTEN=0, the ALRT line is considered high even if the external SMBA pin is low.

35.4.7.2 SMBus initialization

Received Command and Data Acknowledge control (Slave mode)

A SMBus receiver is able to NAK each received command or data. In order to allow ACK control in slave mode, the Slave Byte Control mode is enabled by SBCTL bit in the I2C_CTRL1 register.

Specific address (Slave mode)

- The SMBus Device Default Address (0b1100 001) is enabled by setting the SMBD bit in the I2C_CTRL1 register.
- The SMBus Host Address (0b0001 000) is enabled by setting the SMBH bit in the I2C_CTRL1 register.
- The Alert Response Address (0b0001100) is enabled by setting the ALRTEN bit in the I2C_CTRL1 register.

Packet error check

Packet Error Checking is implemented by adding a Packet Error Code (CRC) at the end of each transfer. The CRC using the C(x) = x8 + x2 + x + 1 CRC-8 polynomial on all bytes (including addresses and read/write bits).

The peripheral has hardware CRC calculator and allows NACK to be sent automatically when the received byte does not match with the hardware calculated CRC.

CRC calculation is enabled by setting the CRCEN bit in the I2C_CTRL1. CRC transfer is using byte counter: BYTECNT[7:0] in the I2C_CTRL2. The CRCEN bit is configured before enabling the I2C.

The SBCTL bit must be set when interfacing the SMBus in slave mode. The CRC is transferred after BYTECNT-1 data have been transferred when the CRCBYTE bit is set and the REFILL bit is cleared.

SMBus with CRC setting

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Table 35-2 I2C configuration

Mode	SBCTL bit	REFILL bit	AUTOSTOP bit	CRCBYTE bit
Master Tx/Rx BYTECNT + CRC+ STOP	x	0	1	1
Master Tx/Rx BYTECNT + CRC + ReSTART	x	0	0	1
Slave Tx/Rx with CRC	1	0	x	1

Timeout detection

This peripheral timers compliant with the 3 timeouts defined in SMBus specification.

The timeout detection is enabled by setting the TMOUTEN and TMEXTEN bits in the I2C_TMOUTR. The timers is programmed to detect a timeout before the maximum time in the SMBus specification.

- tTMOUT check

To enable the tTMOUT check, the 12-bit TMOUTA[11:0] bits is programmed with the timer refill value to check the tTMOUT parameter. The TMIDLE bit is set to '0' to detect the SCL low level timeout.

Then the timer is enabled by setting the TMOUTEN.

If SCL is tied low for a time larger than (TMOUTA+1) x 2048 x tI2CCLK, the TMOUT flag is set in the I2C_STSINT register.

- tLOW:SEXT and tLOW:MEXT check

The 12-bit TMOUTB timer is configured to check tLOW:SEXT for a slave and tLOW:MEXT for a master.

The timer is enabled by TMEXTEN.

If the SMBus peripheral performs a SCL stretch for a time greater than (TMOUTB+1) x 2048 x tI2CCLK, the TMOUT flag is set in the I2C_STSINT register.

Bus Idle detection

The peripheral supports a hardware bus idle detection.

To enable the tIDLE check, the 12-bit TMOUTA[11:0] field is fill with the timer refill value to obtain the tIDLE parameter. The TMIDLE bit is set to detect both SCL and SDA high level timeout. Timer is enabled by TMOUTEN.

If both the SCL and SDA lines remain high for a time larger than (TMOUTA+1) x 4 x tI2CCLK, the TMOUT flag is set in the I2C_STSINT register.

SMBus I2C_TMOUTR register examples

Examples of TMOUTA (max t_{IDLE} = 50 µs)

Table 35-3 TMOUTA TMIDLE=1

f_{I2CCLK}	TMOUTA[11:0] bits	TMIDLE bit	TMOUTEN bit	t_{TIDLE}
8 MHz	0x63	1	1	100 x 4 x 125 ns = 50 µs
48 MHz	0x257	1	1	600 x 4 x 20.08 ns = 50 µs
327 MHz	0xFFF	1	1	4095 x 4 x 3 ns = 50 us

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Examples of TMOUTB

Table 35-4 TMOUTB

f_{I2CCLK}	TMOUTB[11:0] bits	TMEXTEN bit	$t_{LOW:EXT}$
8 MHz	0x1F	1	32 x 2048 x 125 ns = 8 ms
48 MHz	0xBB	1	188 x 2048 x 20.08 ns = 8 ms
1048MHz	0xFFF	1	4095 x 2048 x 0.95ns = 8 ms

Examples of TMOUTA (max t_{TMOUT} = 25 ms)

Table 35-5 TMOUTA TMIDLE=0

f_{I2CCLK}	TMOUTA[11:0] bits	TMIDLE bit	TMOUTEN bit	t_{TMOUT}
8 MHz	0x61	0	1	98 x 2048 x 125 ns = 25 ms
48 MHz	0x249	0	1	586 x 2048 x 20.08 ns = 25 ms
335 MHz	0xFFF	0	1	4095 x 2048 x 3 ns = 25 ms

35.4.7.3 SMBus Slave transmitter

In SMB mode, SBCTL must be programmed to '1' in order to allow the CRC transmission. When the CRCBYTE bit is set, the number of bytes programmed in BYTECNT[7:0] includes the CRC. In that case the total number of WRAVL interrupts is BYTECNT-1 and the content of the I2C_CRCR register is automatically transmitted if the master requests an extra byte after the BYTECNT-1 data transfer.

35.4.7.3.1 Example sequence to transmit via CRC + DMA

For example: SCL=100kHz, I2CCLK=8MHz, transmit 4 bytes + 1 CRC

The communication flow is as follows:

1. **I2C_BUSTM write (h00012526)**
   CKDIV=0; DSCL=0; DSDA=1; HSCL=0x25; LSCL=0x26;
2. **I2C_ADR1 write (h00008066)**
   AD1EN=1; 7 bits address enabled; slave address=7'b0110011;
3. **I2C_CTRL1 write (h0081C001)**
   CRCEN=1; NOSTRCH=0; SBCTL=1; DMARDEN=1; DMAWREN=1; I2CEN=1;
4. **I2C_CTRL2 write (h04050000)**
   CRCBYTE=1; REFILL=0; BYTECNT=0x5; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
5. **Poll waiting I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
6. **I2C_CTRL1 write (h0081C001)**
   CRCEN=1; NOSTRCH=0; SBCTL=1; DMARDEN=1; DMAWREN=1; I2CEN=1;

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7. **I2C_CTRL2 write (h04050000)**
   CRCBYTE=1(reset after address match); REFILL=0; BYTECNT=0x5; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
8. **Poll waiting I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
9. **dma_tx_req & dma_tx_ack sequence start**
   Hardware start receive 1st bytes from DMA and send it to I2C bus, this repeat for 2nd, 3rd and 4th bytes, then send 1 CRC to I2C bus; No need to use WRAVL interrupt in DMA mode

35.4.7.4 SMBus Slave receiver

In SMB mode, SBCTL is programmed to '1' to allow the CRC checking. To allow the ACK control of each byte, the refill mode is set (REFILL=1).

To check the CRC byte, the REFILL bit is cleared and the CRCBYTE bit isset, after BYTECNT-1 data have been received, the next received byte is compared with the internal I2C_CRCR register. NAK is generated if the comparison mismatch, ACK is generated if the comparison matches, whatever the ACK bit value. CRC byte received is copied to I2C_RDR and RDAVL flag is set.

If CRC mismatch, the CRCERR flag is set and an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

35.4.7.4.1 Example sequence to receive via CRC + 10bit address

For example: SCL=100kHz, I2CCLK=8MHz, receive 4 bytes + 1 CRC

The communication flow is as follows:

1. **I2C_BUSTM write (h00012526)**
   CKDIV=0; DSCL=0; DSDA=1; HSCL=0x25; LSCL=0x26;
2. **I2C_CTRL1 write (h008100ff)**
   CRCEN=1; NOSTRCH=0; SBCTL=1; I2CEN=1; All interrupt Enable
3. **I2C_ADR1 write (h00008733)**
   AD1EN=1; 10 bits address enabled; slave address=10'b1100110011;
4. **Wait for interrupt, read I2C_STSINT**
   if ADR bit is set to 1, the Address matched. clear ADR bit by writing I2C_INTCLR.ADRCLR
5. **I2C_CTRL1 write (h008100ff)**
   CRCEN=1; NOSTRCH=0; SBCTL=1; I2CEN=1; All interrupt Enable
6. **I2C_CTRL2 write (h04050000)**
   CRCBYTE=1; REFILL=0; BYTECNT=0x5; NAK=0; STOP=0; START=0; ADR10=0; RWN=0; SADR=000.
7. **Wait for interrupt, read I2C_STSINT**
   if RDAVL bit is set to 1, read 1st data from I2C_RDR
8. **Repeat the same for 2nd, 3rd, 4th data and 1 CRC**

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9. **Wait for interrupt, read I2C_STSINT**

   if STOPF bit is set to 1, slave receives stop condition. clear STOPF bit by writing I2C_INTCLR.STOPCLR

35.4.7.5 SMBus Master transmitter

If SMB master wants to transmit the CRC, set the CRCBYTE and write the number of bytes in the BYTECNT[7:0] before setting the START bit, the total number of WRAVL interrupts is BYTECNT-1. If CRCBYTE bit is set when BYTECNT=0x1, the content of the I2C_CRCR register is transmitted.

If SMB master wants to send a STOP condition after the CRC, set automatic stop mode(AUTOSTOP=1), the STOP condition send after the CRC transmission.

When the SMB master wants to send a RESTART condition after the CRC, software mode is selected (AUTOSTOP=0). Once BYTECNT-1 have been transmitted, the I2C_CRCR content is transmitted and the TFC flag is set, stretching the SCL line low. The RESTART condition is programmed in the TFC interrupt subroutine.

35.4.7.5.1 Example sequence to transmit via CRC + DMA

For example: SCL=100kHz, I2CCLK=48MHz, transmit 1 byte + 1CRC

The communication flow is as follows:

1. **I2C_BUSTM write (h50012526)**
   CKDIV=5; DSCL=0; DSDA=1; HSCL=0x25; LSCL=0x26;
2. **I2C_CTRL1 write (h0082C0B9)**

   CRCEN=1; NOSTRCH=1; SBCTL=0; DMARDEN=1; DMAWREN=1; I2CEN=1; All interrupt Enable
3. **I2C_CTRL2 write (h6022066)**
   CRCBYTE=1; AUTOSTOP=1; REFILL=0; BYTECNT=0x2; NAK=0; STOP=0; START=1; ADR10=0; RWN=0; SADR=0x066.
4. **dma_tx_req & dma_tx_ack sequence start**

   Hardware start receive 1st bytes from DMA and send it to I2C bus, then send 1 CRC to I2C bus, final automatic sending STOP; No need to use WRAVL interrupt in DMA mode

35.4.7.6 SMBus Master receiver

When the SMB master wants to receive the CRC followed by a STOP at the end of the transfer, automatic stop mode can be selected (AUTOSTOP=1). The CRCBYTE bit is set and the slave address programmed before setting the START bit, after BYTECNT-1 data have been received, the next received byte is compare with I2C_CRCR content. NACK response is given to the CRC byte, followed by a STOP condition.

When the SMB master receiver wants to receive the CRC byte followed by a RESTART condition at the end of the transfer, use software mode (AUTOSTOP=0). The CRCBYTE bit is set and the slave address programmed before setting the START bit, after BYTECNT-1 data received, the next received byte is compared with I2C_CRCR content. The TFC flag is set after CRC byte reception, stretching the SCL line low. The RESTART condition is then programmed in the TFC interrupt subroutine.

The CRCBYTE bit has no effect when the REFILL bit is set.

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35.4.7.6.1 Example sequence to receive via CRC

For example: SCL=100kHz, I2CCLK=8MHz, receive 8 bytes + 1 CRC

The communication flow is as follows:

1. **I2C_BUSTM write (h00012526)**
   CKDIV=0; DSCL=0; DSDA=1; HSCL=0x25; LSCL=0x26;
2. **I2C_CTRL1 write (h008000ff)**
   CRCEN=1; NOSTRCH=0; SBCTL=0; I2CEN=1; All interrupt Enable
3. **I2C_CTRL2 write (h06092466)**
   CRCBYTE=1; AUTOSTOP=1; REFILL=0; BYTECNT=9; NAK=0; STOP=0; START=1; ADR10=0; RWN=1; SADR=0x066.
4. **Wait for interrupt, read I2C_STSINT**
   if RDAVL bit is set to 1, read 1st data from I2C_RDR
5. **Wait for interrupt, read I2C_STSINT**
   if RDAVL bit is set to 1, read 2nd data from I2C_RDR
6. **Repeat the same for 3rd, 4th…8th data and 1 CRC**

35.4.8 Error conditions

Bus error (BSER)

A bus error is detected when a START or a STOP condition is detected and is not located after a multiple of 9 SCL clock pulses. A START or a STOP condition is detected when a SDA edge occurs while SCL is high.

The bus error flag is set only if the I2C is involved in the transfer as master or addressed slave (i.e. not during the address phase in slave mode).

When a bus error is detected, the BSER flag is set in the I2C_STSINT register, and an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

Arbitration lost (ABLO)

An arbitration loss is detected when a high level is sent on the SDA line, but a low level is sampled on the SCL rising edge.

- In master mode, arbitration loss is detected during the address phase, data phase and data acknowledge phase. In this case, the SDA and SCL lines are released, the START control bit is cleared by hardware and the master switches automatically to slave mode.
- In slave mode, arbitration loss is detected during data phase and data acknowledge phase. In this case, the transfer is stopped, and the SCL and SDA lines are released.

When an arbitration loss is detected, the ABLO flag is set in the I2C_STSINT register, and an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

Overrun/underrun error (OVF)

An overrun or underrun error is detected in slave mode when NOSTRCH=1 and:

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In reception when a new byte is received and the RDR register has not been read yet. The new received byte is lost, and a NAK is sent as a response to the new byte.

In transmission: When STOPF=1 and the first data byte should be sent. The content of the I2C_WDR register is sent if WRE=0, 0xFF if not.

When a new byte must be sent and the I2C_WDR register has not been written yet, 0xFF is sent.

When an overrun or underrun error is detected, the OVF flag is set in the I2C_STSINT register, and an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

Packet Error Checking Error (CRCERR)

For SMBus, CRCERR set in the I2C_STSINT register when the received CRC byte does not match with the I2C_CRCR register content. A NAK is automatically sent, an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

Timeout Error (TMOUT)

For SMBus. A timeout error occurs if:

- TMIDLE=0 and SCL remained low for the time defined in the TMOUTA[11:0] bits: this is used to detect a SMBus timeout.
- TMIDLE=1 and both SDA and SCL remained high for the time defined in the TMOUTA [11:0] bits: this is used to detect a bus idle condition.
- Master cumulative clock low extend time reached the time defined in the TMOUTB[11:0] bits (SMBus tLOW:MEXT parameter)
- Slave cumulative clock low extend time reached the time defined in TMOUTB[11:0] bits (SMBus tLOW:SEXT parameter)

When a timeout violation is detected in master mode, a STOP condition is automatically sent.

When a timeout violation is detected in slave mode, SDA and SCL lines are automatically released.

When a timeout error is detected, the TMOUT flag is set in the I2C_STSINT register, and an interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

Alert (ALRT)

For SMBus. The ALRT flag is set when the I2C interface is configured as a Host (SMBH=1), the alert pin detection is enabled (ALRTEN=1) and a falling edge is detected on the SMBA pin. An interrupt is generated if the ERRIE bit is set in the I2C_CTRL1 register.

35.4.9 Transmission using DMA

DMA transmission is enabled by setting the DMAWREN in I2C_CTRL1. Data loaded from DMA to the I2C_WDR register whenever the WRAVL bit is set. Only data are transferred with DMA.

- In master mode: software program the initialization, slave address, direction, number of bytes and START bit, DMA is initialized before setting the START bit, the end of transfer is determined by BYTECNT counter.

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- In slave mode: DMA is initialized before the address match event or in ADR interrupt subroutine, before clearing ADR.

35.4.10 Reception using DMA

DMA reception is enabled by setting the DMARDEN bit in I2C_CTRL1. Data is loaded from the I2C_RDR register to DMA whenever the RDAVL bit is set. Only the data (including CRC) are transferred with DMA.

- In master mode: The Reception sequences is same as above (Transmission using DMA)
- In slave mode with NOSTRCH=0, the DMA must be initialized before the address match event, or in the ADR interrupt subroutine, before clearing the ADR.

The CRC transfer is managed with the BYTECNT counter.

35.4.11 FIFO controller limitation

When FIFO is enabled, internal burst counters depend on exact number of WRREG write or RDREG read to the I2C. So software should not read more than necessary or write more than necessary, i.e. write when TX FIFO is full(write WRREG when there is no more FTXIS interrupt) or read when RX FIFO is already empty(read RDREG when there is no more FRXNE interrupt).

In Slave NOSTRCH=1 transmitter mode, the first data need to be written before TX FIFO Enabled and before START condition, the extra last data is always not send out(WRE=0). So if want to redo the same after the first transaction completed, software need to do the following,

1. Disable TX FIFO Enable(TFE=0), wait 2 pclk cycles
2. Write WRE=1.
3. Write the first data.
4. Enable TX FIFO(TFE=1) again
5. Wait for ADR, FTXIS interrupt

35.4.12 I2C interrupts

Table 35-6 I2C interrupt requests

Interrupt event	Event flag	Event flag/Interrupt clearing method	Interrupt enable bit
Receive buffer not empty	RDAVL	Read I2C_RDR register	RDRIE
Transmit buffer interrupt status	WRAVL	Write I2C_WDR register	WDRIE
Stop detection interrupt flag	STOPF	Write STOPCLR=1	STOPIE
Transfer Complete Refill	TFCR	Write BYTECNT a non-zero value.	TFCIE
Transfer complete	TFC	Write START=1 or STOP=1	
Address matched	ADR	Write ADRCLR=1	ADRIE
NACK reception	NAKF	Write NAKCLR=1	NAKIE
Bus error	BSER	Write BSERCLR=1	ERRIE

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Arbitration loss	ABLO	Write ABLOCLR=1	
Overrun/Underrun	OVF	Write OVFCLR=1	
CRC error	CRCERR	Write CRCCLR=1	
Timeout/tLow error	TMOUT	Write TMOUTCLR=1	
SMBus Alert	ALRT	Write ALRTCLR=1	
Receive FIFO not empty	FRXNE	Read I2C_RDR register continuously until the RX FIFO is empty	FRXIE
Transmit FIFO interrupt status	FTXIS	Write I2C_WDR register N times (N = TXILEVEL or BYTECNT) continuously	FTXIE

35.4.13 I2C debug mode

When the microcontroller enters debug mode (core halted), the SMBus timeout either continues to work normally or stops, depending on the I2Cx_STOP configuration bits in the DBG module.

35.5 I2C Registers

35.5.1 I2C control register 1 (I2C_CTRL1)

Address offset: 0x0000

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FTXIE	FRXIE	DFX						CRCEN	ALRTEN	SMBD	SMBH	GENC	Reserved	NOSTRCH	SBCTL
rw	rw	rw						rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMARDEN	DMAWREN	Reserved	AFOFF	DF				ERRIE	TFCIE	STOPIE	NAKIE	ADRIE	RDRIE	WDRIE	I2CEN
rw	rw		rw	rw				rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	FTXIE	TX FIFO Interrupt enable 0: Transmit (FTXIS) interrupt disabled 1: Transmit (FTXIS) interrupt enabled
30	FRXIE	RX FIFO Interrupt enable 0: Receive (FRXNE) interrupt disabled 1: Receive (FRXNE) interrupt enabled
29:24	DFX	Digital noise filter This is the highest 6 bits of the10 bits Digital Noise Filter. DF10={DFX,DF}. These bits are used to configure the digital noise filter on SDA and SCL input. The digital filter, filters spikes with a length of up to DF10 * tI2CCLK

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		DF10=0000000000: Digital filter disabled DF10=0000000001: Digital filter enabled and filtering up to 1 cycle ... DF10=1111111111: Digital filter enabled and filtering up to 1023 cycles
23	CRCEN	CRC enable (Must set to 1 if CRCBYTE=1) 0: CRC calculation disabled 1: CRC calculation enabled If BYTECNT=1 and slave intend to send only 1 data instead of CRC, this bit need to be 0 before being addressed. If BYTECNT=1 and slave intend to send only CRC instead of 1 data, this bit need to be 1 before being addressed.
22	ALRTEN	SMBus alert enable 0: The SMBus alert pin (SMBA) is not supported 1: The SMBus alert pin is supported in host mode (SMBH=1). In device mode (SMBH=0), the SMBA pin is driven low and the Alert Response Address header is enabled (0001100x followed by ACK).
21	SMBD	SMBus Device Default Address enable 0: Device Default Address disabled. Address 0b1100001x is NAKed. 1: Device Default Address enabled. Address 0b1100001x is ACKed.
20	SMBH	SMBus Host Address enable 0: Host Address disabled. Address 0b0001000x is NAKed. 1: Host Address enabled. Address 0b0001000x is ACKed.
19	GENC	General call enable 0: General call disabled. Address 0b00000000 is NAKed. 1: General call enabled. Address 0b00000000 is ACKed.
18	Reserved	Reserved, the reset value must be maintained.
17	NOSTRCH	Clock stretching disable This bit is used to disable clock stretching in slave mode. It must be kept cleared in master mode. 0: Clock stretching enabled 1: Clock stretching disabled
16	SBCTL	Slave byte control This bit is used to enable hardware byte control in slave mode. 0: Slave byte control disabled 1: Slave byte control enabled
15	DMARDEN	DMA reception requests enable 0: DMA mode disabled for reception 1: DMA mode enabled for reception
14	DMAWREN	DMA transmission requests enable 0: DMA mode disabled for transmission 1: DMA mode enabled for transmission
13	Reserved	Reserved, the reset value must be maintained.
12	AFOFF	Analog noise filter main switch 0: Analog noise filter enable

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		1: Analog noise filter disable More SCL and SDA analog filter setting in register I2C_GFLTRCTRL
11:8	DF	Digital noise filter This is the lowest 4 bits of the10 bits Digital Noise Filter, DF10 = {DFX,DF}.. These bits are used to configure the digital noise filter on SDA and SCL input. The digital filter, filters spikes with a length of up to DF10 * tI2CCLK DF10=0000000000: Digital filter disabled DF10=0000000001: Digital filter enabled and filtering up to 1 cycle ... DF10=1111111111: Digital filter enabled and filtering up to 1023 cycles
7	ERRIE	Error interrupts enable 0: Error detection interrupts disabled 1: Error detection interrupts enabled
6	TFCIE	Transfer Complete interrupt enable 0: Transfer Complete interrupt disabled 1: Transfer Complete interrupt enabled
5	STOPIE	Stop detection Interrupt enable 0: Stop detection (STOPF) interrupt disabled 1: Stop detection (STOPF) interrupt enabled
4	NAKIE	Not acknowledge received Interrupt enable 0: Not acknowledge (NAKF) received interrupts disabled 1: Not acknowledge (NAKF) received interrupts enabled
3	ADRIE	Address match Interrupt enable (slave only) 0: Address match (ADR) interrupts disabled 1: Address match (ADR) interrupts enabled
2	RDRIE	RX Interrupt enable 0: Receive (RDAVL) interrupt disabled 1: Receive (RDAVL) interrupt enabled
1	WDRIE	TX Interrupt enable 0: Transmit (WRAVL) interrupt disabled 1: Transmit (WRAVL) interrupt enabled
0	I2CEN	Peripheral enable 0: Peripheral disable 1: Peripheral enable I2CEN need to be low for 3 pclk cycles or 3 fCKDIV cycles whichever is longer to be effective. Where tCKDIV = (CKDIV+1) x tI2CCLK

35.5.2 I2C control register 2 (I2C_CTRL2)

Address offset: 0x0004

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					CRCBYTE	AUTOSTOP	REFILL	BYTECNT[7:0]							
					rw	rw	rw	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAK	STOP	START	HDR10	ADR10	RWN	SADR[9:0]									
rw	rw	rw	rw	rw	rw	rw									

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	CRCBYTE	Packet error checking byte Set by software, and cleared by hardware when the CRC is transferred, or when a STOP condition or an Address matched is received, also when I2CEN=0. 0: No CRC transfer. 1: CRC transmission/reception is requested Writing '0' to this bit has no effect. This bit has no effect when REFILL is set. This bit has no effect is slave mode when SBCTL=0.
25	AUTOSTOP	Automatic stop mode (master mode) Set and cleared by software. 0: software stop mode: TFC flag is set when BYTECNT data are transferred, stretching SCL low. 1: Automatic stop mode: a STOP condition is automatically sent when BYTECNT data are transferred.
24	REFILL	BYTECNT refill mode This bit is set and cleared by software. 0: The transfer is completed after the BYTECNT data transfer (STOP or RESTART follows). 1: The transfer is not completed after the BYTECNT data transfer (BYTECNT is refilled). TFCR flag is set when BYTECNT data are transferred, stretching SCL low.
23:16	BYTECNT[7:0]	Number of bytes The number of bytes to be transmitted/received is programmed there. In non FIFO mode and slave mode with SBCTL=0, it is don't care. After x number of bytes transferred, if SMB software need to change or rewrite BYTECNT on the fly, need to rewrite with "number of remaining bytes + x".
15	NAK	NAK generation (slave mode) Set/Reset by software, cleared by hardware when the NAK is sent, or when a STOP condition or an Address matched received, or I2CEN=0. 0: an ACK is sent after current received byte. 1: a NAK is sent after current received byte.
14	STOP	Stop generation (master mode) Set by software, cleared by hardware when a STOP condition is detected, or I2CEN = 0. 0: No Stop generation.

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		1: Stop generation after current byte transfer.
13	START	Start generation Set by software and cleared by hardware after the Start followed by the address is sent, by an arbitration loss, by a timeout error detection, or I2CEN = 0. It can also be cleared by writing '1' to the ADRCLR bit in the I2C_INTCLR register. 0: No Start generation. 1: Restart/Start generation
12	HDR10	10-bit address header only read direction (master receiver mode) 0: The master sends the complete 10 bit slave address read sequence: Start + 2 bytes 10bit address in write direction + Restart + 1st 7 bits of the 10 bit address in read direction. 1: The master only sends the 1st 7 bits of the 10 bit address, followed by Read direction.
11	ADR10	10-bit addressing mode (master mode) 0: The master operates in 7-bit addressing mode, 1: The master operates in 10-bit addressing mode
10	RWN	Transfer direction (master mode) 0: Master requests a write transfer. 1: Master requests a read transfer.
9:0	SADR[9:0]	Slave address (master mode) In 7-bit addressing mode (ADR10 = 0): SADR[7:1] written with the 7-bit slave address to be sent. In 10-bit addressing mode (ADR10 = 1): SADR[9:0] written with the 10-bit slave address to be sent.

35.5.3 I2C own address 1 register (I2C_ADR1)

Address offset: 0x0008

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD1EN	Reserved				AD1MODE	AD1[9:0]									
rw					rw	rw									

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	AD1EN	Own Address 1 enable 0: Own address 1 disabled. The received slave address AD1 is NAKed. 1: Own address 1 enabled. The received slave address AD1 is ACKed.
14:11	Reserved	Reserved, the reset value must be maintained.

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10	AD1MODE	Own Address 1 10-bit mode 0: Own address 1 is a 7-bit address. 1: Own address 1 is a 10-bit address.
9:0	AD1[9:0]	Interface own slave address 7-bit addressing mode: AD1[6:0] contains the 7-bit own slave address. The bits AD1[9], AD1[8] and AD1[0] are don't care. 10-bit addressing mode: AD1[9:0] contains the 10-bit own slave address.

35.5.4 I2C own address 2 register (I2C_ADR2)

Address offset: 0x000C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD2EN	Reserved				AD2MSK[2:0]			AD2[6:0]							Reserved
rw					rw			rw							

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	AD2EN	Own Address 2 enable 0: Own address 2 disabled. The received slave address AD2 is NAKed. 1: Own address 2 enabled. The received slave address AD2 is ACKed.
14:11	Reserved	Reserved, the reset value must be maintained.
10:8	AD2MSK[2:0]	Own Address 2 masks 000: No mask 001: AD2[1] don’t care. Only AD2[7:2] are compared. 010: AD2[2:1] don’t care. Only AD2[7:3] are compared. 011: AD2[3:1] don’t care. Only AD2[7:4] are compared. 100: AD2[4:1] don’t care. Only AD2[7:5] are compared. 101: AD2[5:1] don’t care. Only AD2[7:6] are compared. 110: AD2[6:1] don’t care. Only AD2[7] is compared. 111: AD2[7:1] don’t care. No comparison is done, all (except reserved) 7-bit received addresses are acknowledged.
7:1	AD2[7:1]	Interface address 7-bit addressing mode: 7-bit address
0	Reserved	Reserved, the reset value must be maintained.

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35.5.5 I2C timing register (I2C_BUSTM)

Address offset: 0x0010

Reset value: 0x0000 0000

Bit field	Name	Description
31:28	CKDIV[3:0]	Timing prescaler prescale I2CCLK in order to generate the clock period tCKDIV used for data setup and hold counters and for SCL high and low level counters. tCKDIV = (CKDIV+1) x tI2CCLK Program CKDIV[3:0] to divide the I2CCLK down to the max internal fCKDIV frequency. The max fCKDIV frequency is 8 MHz for SCL=100kHz to 1MHz. The max fCKDIV frequency is 48 MHz for SCL=3.4MHz. eg. I2CCLK =128MHz, SCL=100kHz, use CKDIV[3:0]=0xF.
27:24	Reserved	Reserved, the reset value must be maintained.
23:20	DSCL[3:0]	Data setup time This field is used to generate a delay tDSCL between SDA edge and SCL rising edge. In master mode and in slave mode with NOSTRCH = 0, the SCL line is stretched low during tDSCL. tDSCL = (DSCL+1) x tCKDIV
19:16	DSDA[3:0]	Data hold time This field is used to generate the delay tDSDA between SCL falling edge and SDA edge. In master mode and in slave mode with NOSTRCH = 0, the SCL line is stretched low during tDSDA. tDSDA= DSDA x tCKDIV
15:8	HSCL[7:0]	SCL high period (master mode) This field is used to generate the SCL high period in master mode. tHSCL = (HSCL+1) x tCKDIV; Minimum value is 1.
7:0	LSCL[7:0]	SCL low period (master mode) This field is used to generate the SCL low period in master mode. tLSCL = (LSCL+1) x tCKDIV; Minimum value is 2.

35.5.6 I2C timeout register (I2C_TMOUTR)

Address offset: 0x0014

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TMEXTEN	Reserved			TMOUTB[11:0]											
rw				rw											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMOUTEN	Reserved		TMIDLE	TMOUTA[11:0]											
rw			rw	rw											

Bit field	Name	Description
31	TMEXTEN	Extended clock timeout enable 0: Extended clock timeout detection is disabled 1: Extended clock timeout detection is enabled. When a cumulative SCL stretch for more than tLOW:EXT is done by the I2C interface, a timeout error is detected (TMOUT=1).
30:28	Reserved	Reserved, the reset value must be maintained.
27:16	TMOUTB[11:0]	Bus timeout B This field is used to configure the cumulative clock extension timeout: In master mode, the master cumulative clock low extend time (tLOW:MEXT) is detected In slave mode, the slave cumulative clock low extend time (tLOW:SEXT) is detected tLOW:EXT= (TMOUTB+1) x 2048 x tI2CCLK
15	TMOUTEN	Clock timeout enable 0: SCL timeout detection is disabled 1: SCL timeout detection is enabled: when SCL is low for more than tTMOUT (TMIDLE=0) or high for more than tIDLE (TMIDLE=1), a timeout error is detected (TMOUT=1).
14:13	Reserved	Reserved, the reset value must be maintained.
12	TMIDLE	Idle clock timeout detection 0: TMOUTA is used to detect SCL low timeout 1: TMOUTA is used to detect both SCL and SDA high timeout (bus idle condition)
11:0	TMOUTA[11:0]	Bus Timeout A This field is used to configure: The SCL low timeout condition tTMOUT when TMIDLE=0 tTMOUT= (TMOUTA+1) x 2048 x tI2CCLK The bus idle condition (both SCL and SDA high) when TMIDLE=1 tIDLE= (TMOUTA+1) x 4 x tI2CCLK

35.5.7 I2C interrupt and status register (I2C_STSINT)

Address offset: 0x0018

Reset value: 0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FTXIS	FRXNE	Reserved						ADRRCV[6:0]							DIR

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r	r										r				r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUSY	QADR	ALRT	TMOUT	CRCERR	OVF	ABLO	BSER	TFCR	TFC	STOPF	NAKF	ADR	RDAVL	WRAVL	WRE
r	r	r	r	r	r	r	r	r	r	r	r	r	r	rw	rw

Bit field	Name	Description
31	FTXIS	Transmit FIFO interrupt status (transmitters) This bit is only valid if TX FIFO Enable (TFE) is set, purpose of FTXIS is reduce number of interrupt to CPU. FTXIS set by hardware when the number of empty bytes is available in TX FIFO equal TXILEVEL, and the number of data(TXILEVEL) to be transmitted can be written to I2C_WDR address continuously and data routed to TX FIFO. It is cleared when this number of bytes(TXILEVEL) is written or total number of bytes(BYTECNT, and BYTECNT is less than TXILEVEL) to be transmitted is written.
30	FRXNE	Receive FIFO not empty (receivers) This bit is only valid if RX FIFO Enable (RFE) is set, purpose of FRXNE is reduce number of interrupt to CPU. This bit is set by hardware when the number of bytes received in the RX FIFO equal RXILEVEL. It is also set if the final last few number of bytes(BYTECNT- RXILEVEL, and BYTECNT is greater than TXILEVEL) received is less than RXILEVEL. It is cleared when all bytes in RX FIFO are read from I2C_RDR.
29:24	Reserved	Reserved, the reset value must be maintained.
23:17	ADRRCV[6:0]	Address match received (Slave mode) These bits updated with the received address when an address match occurs (ADR = 1). If 10-bit address, ADRRCV provides the 10-bit header followed by the 2 MSBs of the address.
16	DIR	Transfer direction (Slave mode) This flag updated when address match event occurs (ADR=1). 0: Write transfer, slave enters receiver mode. 1: Read transfer, slave enters transmitter mode.
15	BUSY	Bus busy It is set when a START condition is detected. Cleared by hardware when a STOP condition is detected, or when I2CEN=0.
14	QADR	Quick command Address matched (slave mode) Set by hardware if received slave address matching Quick command Address (QCMDAD[7:1]) and QCMDEN=1. Cleared by setting ADRCLR bit.
13	ALRT	SMBus alert This flag is set by hardware when SMBH=1, ALRTEN=1 and a SMBALRT event (falling edge) is detected on SMBA pin. Cleared by setting the ALRTCLR bit.
12	TMOUT	Timeout or tLOW detection flag This flag is set by hardware when a timeout or extended clock timeout occurred. Cleared by setting the TMOUTCLR bit.

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11	CRCERR	CRC Error in reception This flag is set by hardware when the received CRC does not match with the CRC register content. A NAK is sent after the wrong CRC reception. Cleared by setting the CRCCLR bit.
10	OVF	Overrun/Underrun (slave mode) Set by hardware in slave mode with NOSTRCH=1, when an overrun/underrun error occurs. Cleared by setting the OVFCLR bit.
9	ABLO	Arbitration lost This flag is set by hardware if arbitration loss. Cleared by setting the ABLOCLR bit.
8	BSER	Bus error This flag is set by hardware when a misplaced Start or STOP condition is detected whereas the peripheral is involved in the transfer. The flag is not set during the address phase in slave mode. Cleared by setting BSERCLR bit.
7	TFCR	Transfer Complete Refill This flag is set by hardware when REFILL=1 and BYTECNT data have been transferred. Cleared when BYTECNT is written to a non-zero value. only for master mode, or for slave mode when the SBCTL bit is set.
6	TFC	Transfer Complete (master mode) This flag is set by hardware when REFILL=0, AUTOSTOP=0 and BYTECNT data have been transferred. Cleared when START bit or STOP bit is set.
5	STOPF	Stop detection flag This flag is set by hardware when a STOP condition is detected on the bus and the peripheral is involved in this transfer: either as a master, provided that the STOP condition is generated by the peripheral. or as a slave, provided that the peripheral has been addressed previously during this transfer. Cleared by setting the STOPCLR bit.
4	NAKF	Not Acknowledge received flag This flag is set by hardware when a NAK is received after a byte transmission. Cleared by setting the NAKCLR bit.
3	ADR	Address matched (slave mode) This bit is set by hardware as soon as the received slave address matched with one of the enabled slave addresses. Cleared by setting ADRCLR bit.
2	RDAVL	Receive data available (receivers) This bit is set by hardware when the received data is copied into the I2C_RDR register, and is ready to be read. Cleared when I2C_RDR is read
1	WRAVL	Write available (transmitters) Hardware set this bit when the I2C_WDR register is empty and new data can be written to I2C_WDR. Cleared when the next data to be sent is written to I2C_WDR register. This bit can be written to '1' when NOSTRCH=1 only, in order to generate a WRAVL event (interrupt if WDRIE=1 or DMA request if DMAWREN=1).
0	WRE	Write data register empty (transmitters) Set by hardware when the I2C_WDR register is empty. Cleared when the next data to be sent is written in the I2C_WDR register. Data not sent out to I2C bus from internal shift register means WRE is 0.

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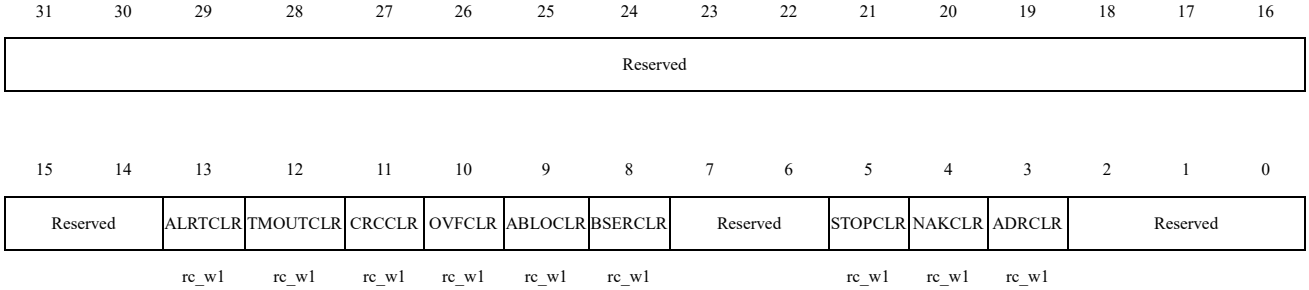
		When this bit is 0, I2C_WDR cannot be written, this bit can then be written to '1' by force to "flush", so data can be written again (eg. used in slave transmitter NOSTRCH=1 sequence).

35.5.8 I2C interrupt clear register (I2C_INTCLR)

Address offset: 0x001C

Reset value: 0x0000 0000



Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	ALRTCLR	Alert flag clear Writing 1 to this bit clears the ALRT flag in the I2C_INTR register
12	TMOUTCLR	Timeout detection flag clear Writing 1 to this bit clears the TMOUT flag in the I2C_INTR register.
11	CRCCLR	CRC Error flag clear Writing 1 to this bit clears the CRCERR flag in the I2C_INTR register.
10	OVFCLR	Overrun/Underrun flag clear Writing 1 to this bit clears the OVF flag in the I2C_INTR register.
9	ABLOCLR	Arbitration lost flag clear Writing 1 to this bit clears the ABLO flag in the I2C_INTR register.
8	BSERCLR	Bus error flag clear Writing 1 to this bit clears the BSERF flag in the I2C_INTR register.
7:6	Reserved	Reserved, the reset value must be maintained.
5	STOPCLR	STOP detection flag clear Writing 1 to this bit clears the STOPF flag in the I2C_INTR register.
4	NAKCLR	Not Acknowledge flag clear Writing 1 to this bit clears the NAKF flag in I2C_INTR register.
3	ADRCLR	Address matched flag clear Writing 1 to this bit clears the ADR flag in the I2C_INTR register. Writing 1 to this bit also clears the START bit in the I2C_CONF2 register.
2:0	Reserved	Reserved, the reset value must be maintained.

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35.5.9 I2C PEC register (I2C_CRCR)

Address offset: 0x0020

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CRC[7:0]							
								r							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CRC[7:0]	CRC or packet error checking register when CRCEN=1. Cleared when I2CEN=0. The time to read the final CRC is after CRCBYTE go low.

35.5.10 I2C receive data register (I2C_RDR)

Address offset: 0x0024

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RDREG [7:0]							
								r							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	RDAT[7:0]	Data byte received from the I2C bus

35.5.11 I2C transmit data register (I2C_WDR)

Address offset: 0x0028

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WRREG[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	WDAT[7:0]	Data byte to be transmitted to the I2C bus Written only when WRE=1.

35.5.12 I2C HS timing register (I2C_HSBUSTM)

Address offset: 0x002C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSCKDIV[3:0]				Reserved				HSDSCL[3:0]				HSDSDA[3:0]			
rw								rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSHSCL[7:0]								HSLSCL[7:0]							
rw								rw							

Bit field	Name	Description
31:28	HSCKDIV[3:0]	High speed mode timing prescaler This field is identical to CKDIV[3:0] but only used for HS Mode transfer
27:24	Reserved	Reserved, the reset value must be maintained.
23:20	HSDSCL[3:0]	High speed mode Data setup time this field is identical to DSCL[3:0] but only used for HS Mode transfer
19:16	HSDSDA[3:0]	High speed mode Data hold time This field is identical to DSDA[3:0] but only used for HS Mode transfer
15:8	HSHSCL[7:0]	High speed mode SCL high period (master mode) This field is identical to HSCL[7:0] but only used for HS Mode transfer
7:0	HSLSCL[7:0]	High speed mode SCL low period (master mode) This field is identical to LSCL[7:0] but only used for HS Mode transfer

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35.5.13 I2C FIFO Control & Status register (I2C_FIFOCSR)

Address offset: 0x0030

Reset value: 0x0800 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFE	RFE	Reserved		TXILEVEL[3:0]				Reserved				RXILEVEL[3:0]			
rw	rw			rw								rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXFLEVEL[3:0]				Reserved				RXFLEVEL[3:0]			
				r								r			

Bit field	Name	Description
31	TFE	Set TX FIFO active For transmitting data, when set, CPU may write data continuously up to the number indicated by TXILEVEL to I2C_WDR, data are redirect to the 8 bytes TX FIFO. WRAVL and WRE are not used externally and should be ignored. FTXIS is used.
30	RFE	Set RX FIFO active For receiving data, when RXFE set, data received are redirect to 8 bytes RX FIFO, CPU may read data continuously up to the number indicated by RXILEVEL from I2C_RDR. RDAVL is not used externally and should be ignored. FRXNE is used.
29:28	Reserved	Reserved, the reset value must be maintained.
27:24	TXILEVEL[3:0]	TX FIFO empty level (8 to 1) to generate FTXIS empty interrupt or assert i2c_dma_tx_req if DMAWREN=1. 8(default): interrupt after 8 empty space available; Also for DMA burst 8 when DMAWREN=1. 7: interrupt after 7 empty space available; Also for DMA burst 7 when DMAWREN=1. ... 2: interrupt after 2 empty space available; Also for DMA burst 2 when DMAWREN=1. 1: interrupt after 1 empty space available, Also for DMA single cycle when DMAWREN=1. 0: Invalid
23:20	Reserved	Reserved, the reset value must be maintained.
19:16	RXILEVEL[3:0]	RX FIFO filled level(1 to 8) to generate FRXNE not empty interrupt or for DMA burst value when DMARDEN=1, FRXNE is also set high if the final last few bytes received is less than RXILEVEL. 0: Invalid 1: interrupt after 1 data byte received,

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		Also for DMA single cycle when DMARDEN=1. 2: interrupt after 2 data bytes received, Also for DMA burst 2 when DMARDEN=1. … 7: interrupt after 7 data bytes received, Also for DMA burst 7 when DMARDEN=1. 8: interrupt after 8 data bytes received, Also for DMA burst 8 when DMARDEN=1.
15:12	Reserved	Reserved, the reset value must be maintained.
11:8	TXFLEVEL[3:0]	Number of bytes currently in the TX FIFO (0 to 8) This is the number of unsent bytes in TX FIFO. In normal condition, TXFLEVEL go 0 when all data transferred from TX FIFO to internal shift register, in the case of error, NAK, debug phase, etc, number of data not yet sent out to internal shift register are reflected in TXFLEVEL. Unsent data are cleared by TFE=0 or I2CEN=0.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	RXFLEVEL[3:0]	Number of bytes currently in the RX FIFO (0 to 8) This is the number of unread bytes in RX FIFO. Decreased by reading I2C_RDR. Cleared when RFE=0 or I2CEN=0.

35.5.14 I2C quick command address register (I2C_QCMD)

Address offset: 0x0034

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QCMDEN	Reserved							QCMDAD[6:0]							Reserved
rw								rw							

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	QCMDEN	For Master mode: 0: No quick command (No STOP condition generated after Address is ACKed) 1: STOP condition will be generated after slave address (SADR[7:1]) sent out and ACK received, (Set ADR10 = 0, Quick command bit = RWN), Quick command has higher priority than normal addressing. For Slave mode:

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		SMB Quick command own Address enable 0: Quick command Own address disabled. The received slave address that match QCMDAD is NAKed. 1: Quick command Own address enabled. The received slave address that match QCMDAD is ACKed, Quick command has higher priority than normal addressing.
14:8	Reserved	Reserved, the reset value must be maintained.
7:1	QCMDAD[6:0]	For Slave mode only: SMB Quick command address If QCMDEN = 1 and QCMDAD matched with the received slave address, the ADR and QADR are set and the receive command bit can be read from DIR bit.
0	Reserved	Reserved, the reset value must be maintained.

35.5.15 I2C Analog noise filter register (I2C_GFLTRCTRL)

Address offset: 0x0038

Reset value: 0x0000 2200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLAFENN	Reserved	SCLAFW[1:0]		SDAAFENN	Reserved	SDAAFW[1:0]		Reserved							
rw		rw		rw		rw									

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	SCLAFENN	SCL analog filter enable 0: SCL analog filter enable. (default) 1: SCL analog filter disable
14	Reserved	Reserved, the reset value must be maintained.
13:12	SCLAFW	SCL analog filter adjustment range control 2'b00: SCL filter up to 5ns glitch 2'b01: SCL filter up to 15ns glitch 2'b10: SCL filter up to 25ns glitch 2'b11: SCL filter up to 35ns glitch
11	SDAAFENN	SDA analog filter enable 0: SDA analog filter enable. (default) 1: SDA analog filter disable
10	Reserved	Reserved, the reset value must be maintained.
9:8	SDAAFW	SDA analog filter adjustment range control 2'b00: SDA filter up to 5ns glitch

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		2’b01: SDA filter up to 15ns glitch 2’b10: SDA filter up to 25ns glitch 2’b11: SDA filter up to 35ns glitch
7:0	Reserved	Reserved, the reset value must be maintained.

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36 Serial Peripheral Interface/Inter-IC Sound (SPI/ I2S)

36.1 Introduction

36.1.1 SPI Introduction

The serial peripheral interface (SPI) allows half/ full-duplex, synchronous, serial communication with external devices. The interface can be configured as the master and in this case it provides the communication clock (SCK) to the external slave device. The interface is also capable of operating in multimaster configuration.

It may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

36.1.2 I2S Introduction

I2S is a synchronous serial interface communication protocol. It supports four audio standards, including Philips standard, MSB alignment standard, LSB alignment standard, and PCM standard. It can operate in master and slave modes in half-duplex communication. When operating as a master device, it provides clock signals to external slave devices through the interface.

36.2 Main Features

36.2.1 SPI Features

- Full-duplex and half-duplex synchronous mode.
- Support master mode, slave mode and multi-master mode.
- Supports 8-bit or 16-bit data frame format.
- Data bit sequence programmable.
- NSS management by hardware or software.
- Clock polarity and phase programmable.
- Transmitting and receiving support hardware CRC calculation and check.
- DMA capability for transmission and reception
- Supports FIFO mode, with a depth of 8 for both the transmit FIFO and receive FIFO.
- The maximum communication frequency of the interface is 50Mbps.
- Programmable NSS polarity.

36.2.2 I^2S Features

- Full-duplex mode and half-duplex synchronous mode.

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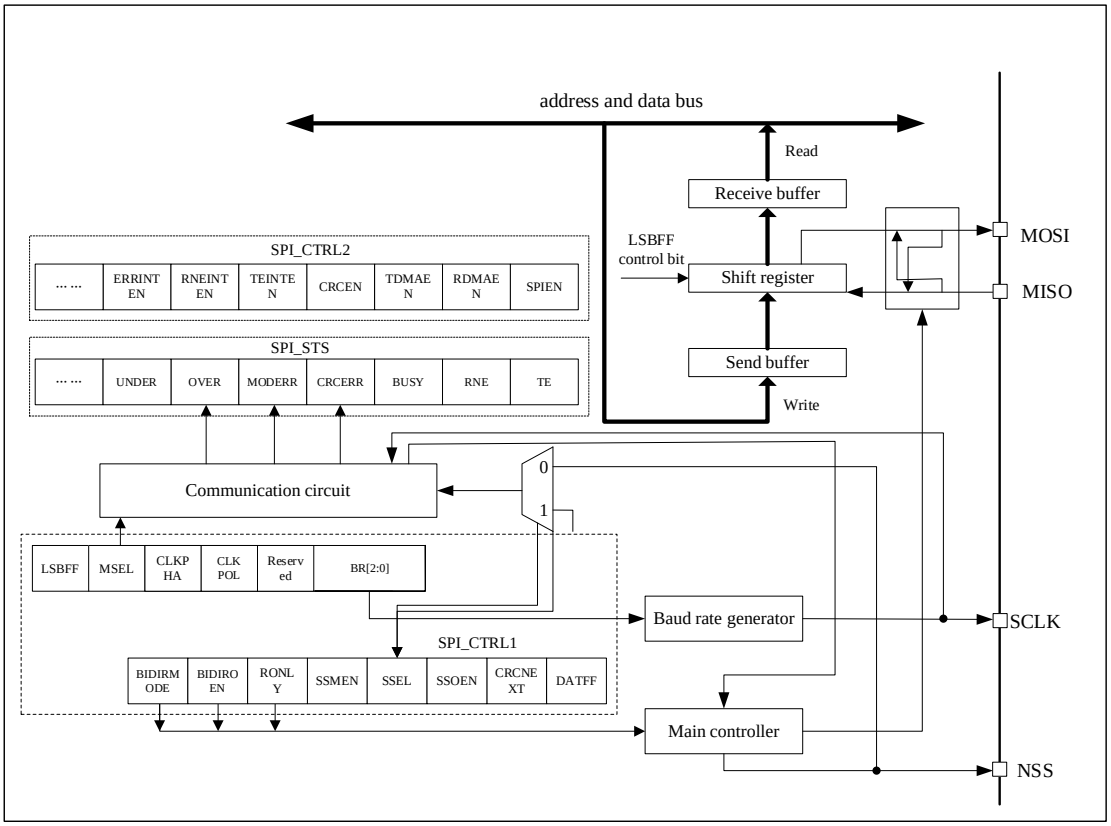
- Supports master mode and slave mode operation.
- Four audio standards are supported: Philips I2S standard, MSB alignment standard, LSB alignment standard and PCM standard.
- The audio sampling frequency from 8kHz to 192kHz can be configured.
- Supports 16-bit, 24-bit or 32-bit data length and data frame format (configured according to requirements).
- Steady state clock polarity programmable.
- The data direction is always MSB first.
- DMA capability for transmission and reception
- Supports PLL, HSI, SYSCLK, and external clock.

36.3 SPI Function Description

36.3.1 Principles of SPI

36.3.1.1 General Description

Figure 36-1 SPI Clock Diagram



Usually, the SPI is connected to external devices through four pins:

- SCLK: serial clock pin. Serial clock signal is output from the SCLK pin of master device and input to SCLK pin of slave device.

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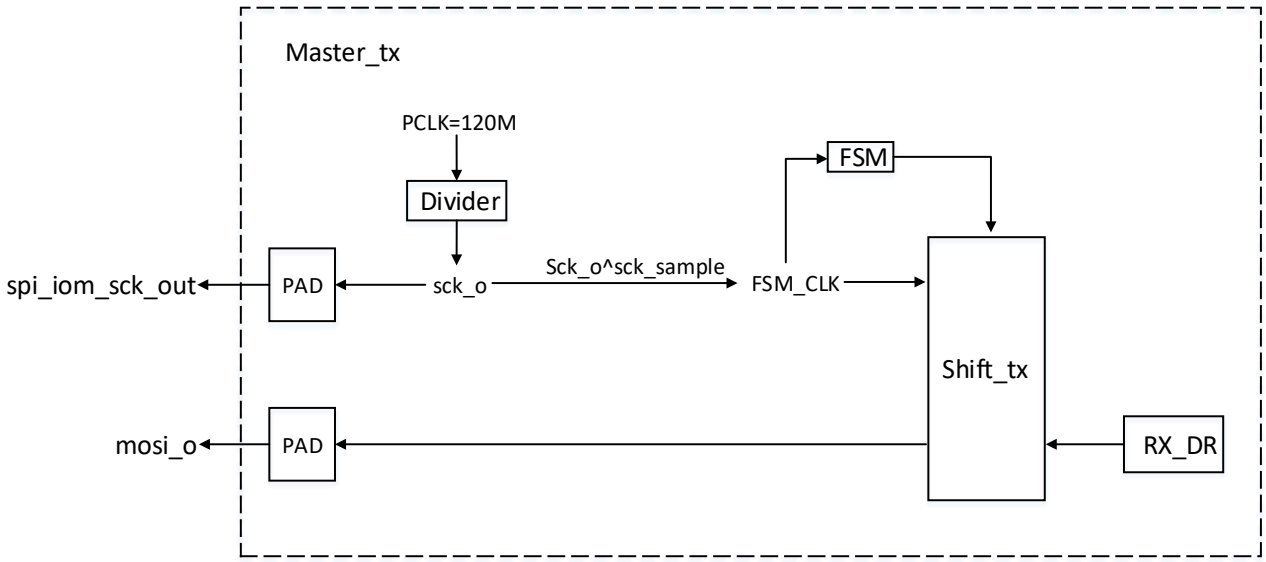
- MISO: master input/slave output pin. Data is received from the MISO pin of master device and send by the MISO pin of slave device.
- MOSI: master output/slave input pin. Data is transmitted by the MOSI pin of master device and received from the MOSI pin of slave device.
- NSS: Slave select. There are two types of NSS pin, internal pin and external pin. If the internal pin detects a high level, SPI works in the master mode. Conversely, SPI works in the slave mode. Users can use a standard I/O pin of the master device to control the NSS pin of the slave device.

Additional Information: In order to increase the maximum communication speed of SPI to 60M, adjustments were made to the internal clock architecture of SPI in N32xxx. The following Figure 36-2 shows the clock architecture diagram of the SPI transmission process.

Figure 36-2 SPI Transmission Process Clock Architecture Diagram



For the receive process, the clock generated by the master (sck_o) is internally sampled through registers (sampling clock is pclk) to generate a delayed clock sck_delay. The specific delay, controlled by software, can be up to 7 cycles (with a maximum delay of 29.16ns at pclk of 240M). sck_delay controls the receive state machine (state_rx), receive shift register (shift_rx), and the first-stage sampling data register (samp reg), as shown in Figure 36-3.

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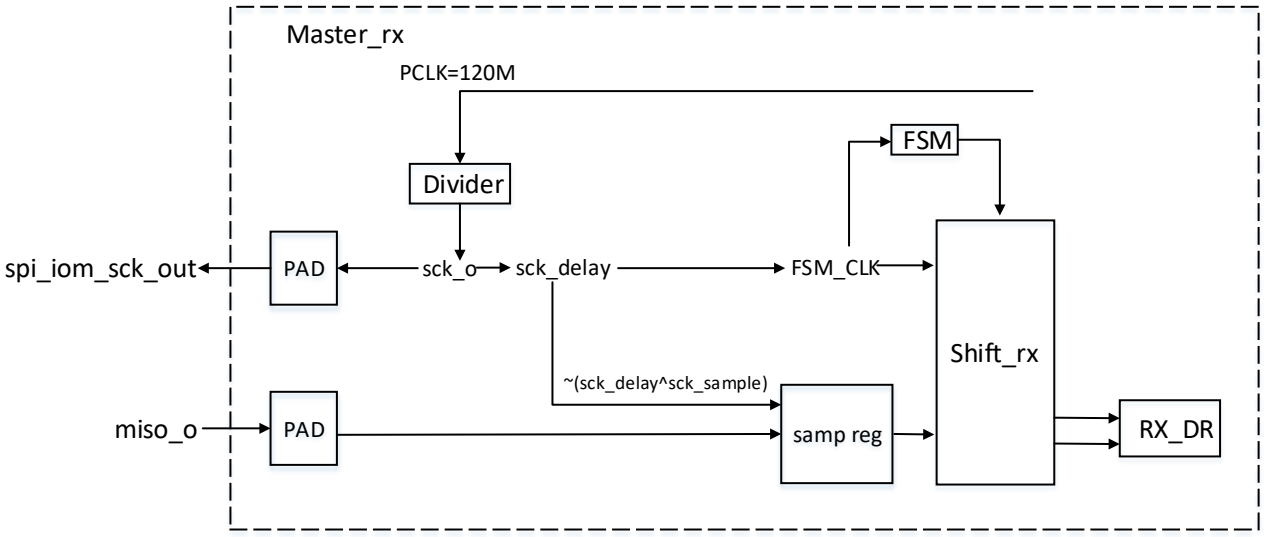
Figure 36-3 SPI Receive Process Clock Architecture Diagram



36.3.1.2 NSS Pin Management

- **Software NSS mode**

  The software slave device management is enabled when SPI_CTRL1.SSMEN = 1.

  The NSS pin remains free in software NSS mode. In this mode the internal NSS signal level is driven by writing the SPI_CTRL1.SSEL bit (set SPI_CTRL1.SSEL=1 in master mode and set SPI_CTRL1.SSEL = 0 in slave mode).

- **Hardware NSS mode**

  The software slave device management is disabled when SPI_CTRL1.SSMEN = 0.

  NSS input mode: The NSS output of the master device is disabled (SPI_CTRL1.MSEL = 1, SPI_CTRL1.SSOEN = 0), allowing operation in multi-master mode. The master should connect NSS pin to the high level and the slave should connect NSS pin to the low level during the entire data frame transfer. When configured in master mode with NSS configured as an input (SPI_CTRL1.MSEL = 1, SPI_CTRL1.SSOEN = 0) and if NSS is pulled low, the SPI enters the master mode fault state.

  NSS output mode: NSS output of the master device is enable (SPI_CTRL1.MSEL = 1, SPI_CTRL1.SSOEN = 1). SPI as the master device must pull the NSS pin to low level, all device which connected to the master device and set to NSS hardware mode, will detect low level and enter the slave mode automatically.

  Note: The choice of software mode or hardware mode depends on whether NSS control is needed in the communication protocol. If not, you can choose the software mode, and release a GPIO pin for other purposes.

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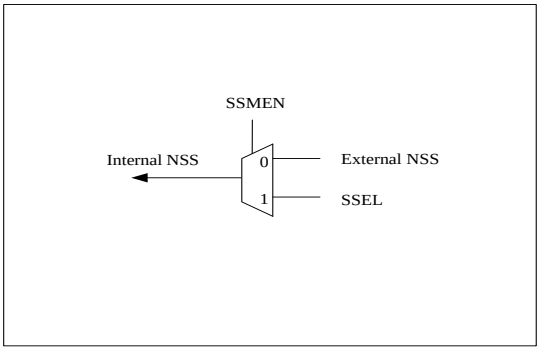
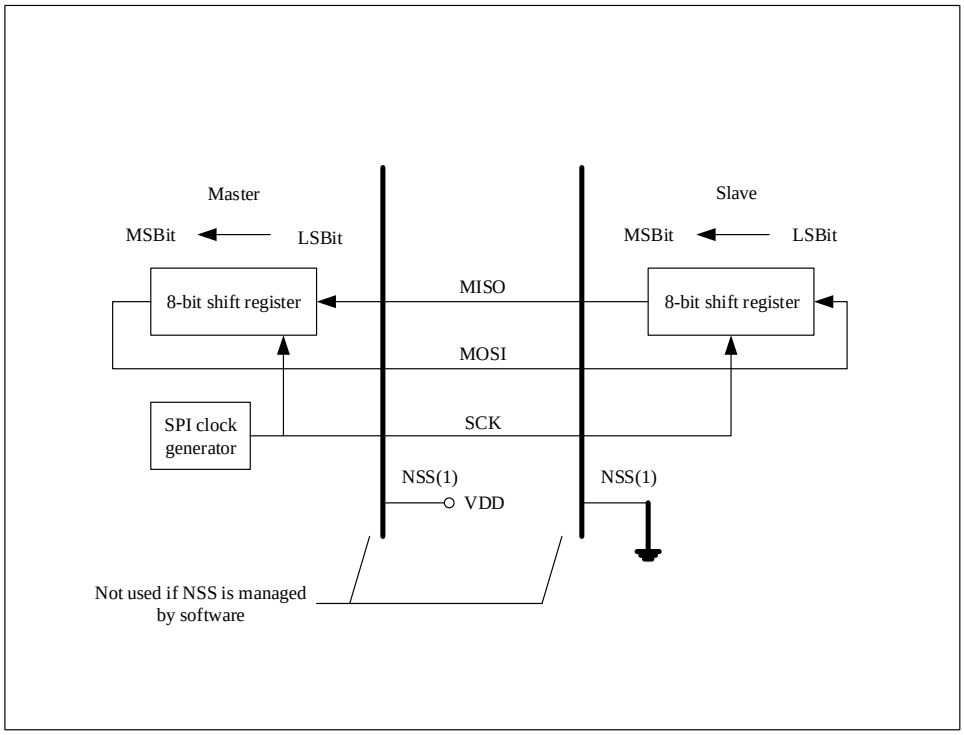
Figure 36-4 Selective Management of Hardware/Software



The following figure is an example of the interconnection of single master and single slave devices：

Figure 36-5 SPI Master and Slave Applications



Note: (1)NSS pin is set as input

SPI is a ring bus structure. The master device outputs a synchronous clock signal through the SCK pin, the MOSI pin of the master device is connected to the MOSI pin of the slave device, and the MISO pin of the master device is connected to the MISO pin of the slave device, so that data can be transferred between devices. Continuous data transfer between master and slave, sending data to slave through MOSI pin and slave sending data to master through MISO pin.

36.3.1.3 SPI timing mode

User can select the clock edge of data capture by setting SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit.

- When CLKPOL = 0, CLKPHA = 0, the SCLK pin will keep low in idle state, and the data will be sampled at the first edge, which is rising edge.

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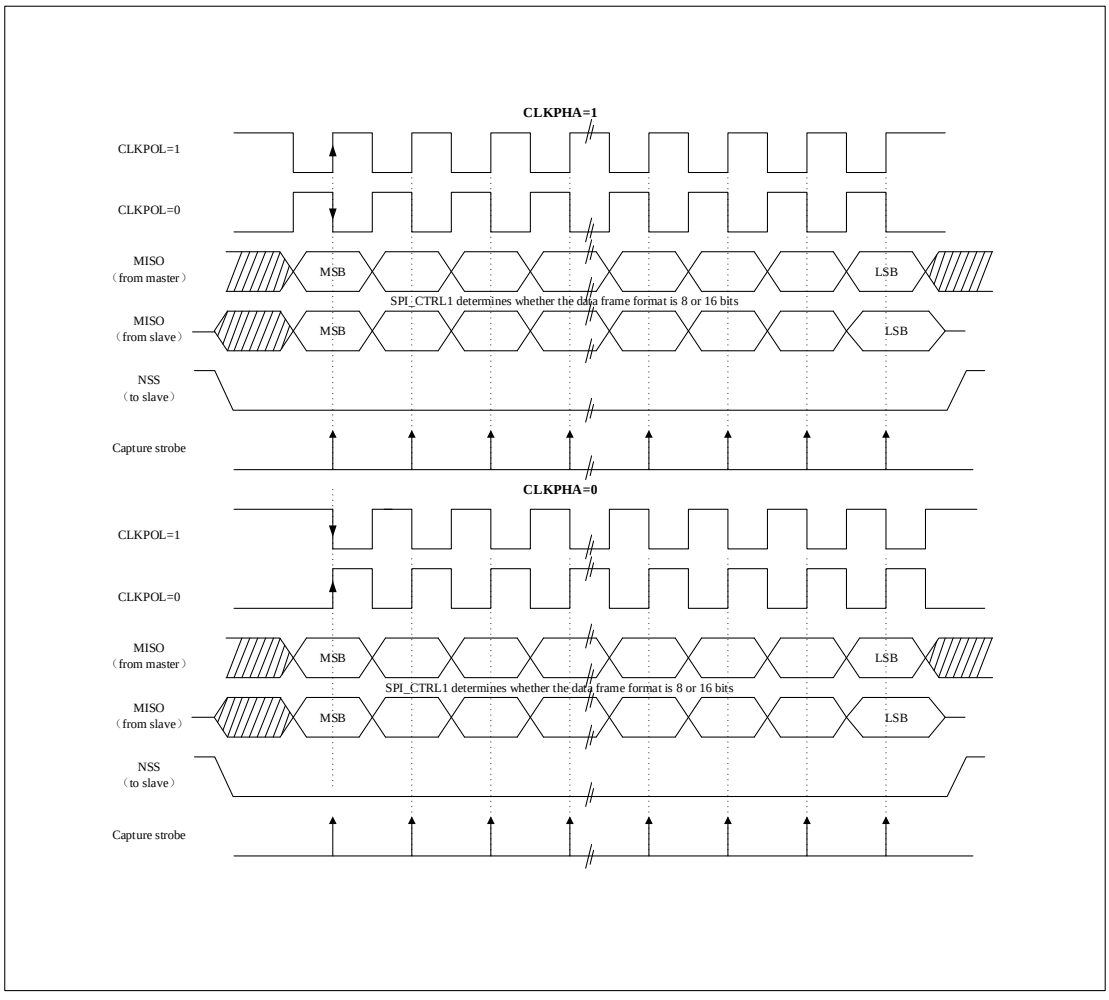
- When CLKPOL = 0, CLKPHA = 1, the SCLK pin will keep low in idle state, and the data will be sampled at the second edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 0, the SCLK pin will keep high in idle state, and the data will be sampled at the first edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 1, the SCLK pin will keep high in idle state, and the data will be sampled at the second edge, which is rising edge.

Regardless of the timing mode used, the master and slave configuration must be the same.

Figure 36-6 is the combination timing of four CLKPHA and CLKPOL bits transmitted by SPI when the SPI_CTRL1.LSBFF = 0.

Figure 36-6 Data Clock Timing Diagram



36.3.1.4 Data format

User can selects the data order by setting the SPI_CTRL1.LSBFF bit. When SPI_CTRL1.LSBFF = 0, SPI will send the high-order data (MSB) first; When SPI_CTRL1.LSBFF = 1, SPI will send low-order data (LSB) first.

User can selects the data frame by setting the SPI_CTRL1.DATFF bit.

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36.3.1.5 CRC Calculation

CRC check is used to ensure the reliability of full-duplex communication. Separate CRC calculators are used for data transmission and reception. The CRC is calculated by programmable polynomial operations on each received bit. The CRC calculation occurs on the sampling clock edges defined by the CLKPHA and CLKPOL bits in the SPI_CR1 register.

Note: The SPI interface provides two CRC calculation methods, depending on the selected data frame format for transmission and/or reception: CR8 for 8-bit data frames and CRC16 for 16-bit data frames. CRC calculation is enabled by setting the CRCEN bit in the SPI_CR2 register. When the CRCEN bit is set, the CRC registers (SPI_CRCTDAT and SPI_CRCTDAT) are reset. If the CRCNEXT bit in the SPI_CR1 register is set, the content of SPI_CRCTDAT is sent out after the current byte is transmitted. During the transmission of the SPI_CRCTDAT content, if the value received in the shift register does not match the content of SPI_CRCTDAT, the CRCERR flag in the SPI_STS register is set to 1. If there is still data in the TX buffer, the CRC value is only transmitted after the data byte transfer ends. The CRC calculator is disabled during CRC transmission, and the value in the registers remains unchanged.

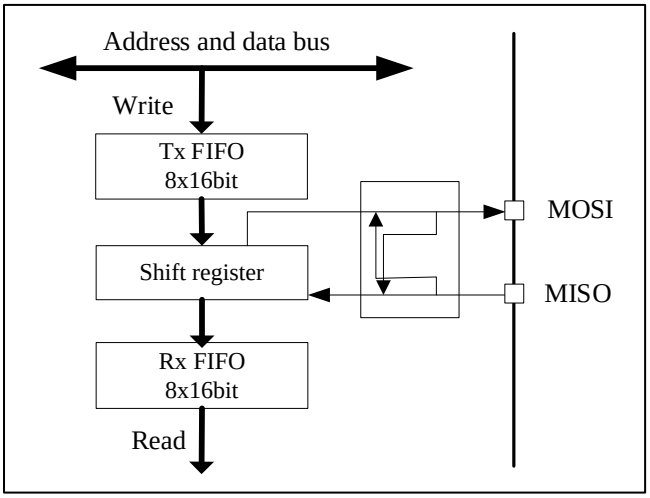
36.3.1.6 FIFO

Support FIFO function.

When the data frame format is configured as 8-bit, the TX_FIFO size is 8 x 8 bits, and the RX_FIFO size is 8x8 bits.

When the data frame format is configured as 16-bit, the TX_FIFO size is 8x16 bits, and the RX_FIFO size is 8x16 bits.

Figure 36-7 FIFO Diagram



When setting SPI_CTRL2.FIFOEN to '1', the SPI will enable the FIFO function.

Transmit: When the CPU writes data to the SPI_DAT register, the transmitted data will be written to the TX_FIFO, and serially output to the interface through TX_SHIFT.

Receive: Receive data serially from the interface and transfer it to the RX_FIFO through RX_SHIFT.

Note: In FIFO mode, data is read by accessing the SPI_RX_FIFO register, while in non-FIFO mode, data is read by accessing the SPI_DAT register. Both FIFO and non-FIFO modes involve writing data by accessing the SPI_DAT

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register.

To enhance data control flexibility, flags for TX_FIFO half-empty, TX_FIFO full, RX_FIFO half-full, and RX_FIFO full have been added. Users can access the SPI_FIFO_CNT register to view the effective number of data in the FIFO for better compatibility with various scenarios.

36.3.2 User Configuration Process

36.3.2.1 Configuring SPI as Slave Mode

In slave mode, the SCK pin is used to receive the serial clock from the master device. The setting of BR[2:0] in the SPI_CTRL1 register does not affect the data transfer rate.

Note: It is recommended to enable the SPI slave device before the master device sends the clock to avoid unexpected data transmission. The data register of the slave device must be ready before the arrival of the first edge of the communication clock or before the ongoing communication ends. The polarity of the communication clock must be at a stable value before enabling the slave device and the master device.

Follow the steps below to configure the SPI as a slave mode:

Configuration Process:

1. Set the SPI_CTRL1.DATFF bit to define the data frame format as 8-bit or 16-bit.
2. Choose the SPI_CTRL1.CLKPOL and SPI_CTRL1.CLKPHA bits to define the phase relationship between data transfer and the serial clock. To ensure correct data transmission, the CLKPOL and CLKPHA bits of the slave device and master device must be configured in the same manner.
3. The frame format ("MSB first" or "LSB first" defined by the LSBFF bit in the SPI_CTRL1 register) must be the same as the master device.
4. In hardware mode (refer to the NSS Pin Management section), the NSS pin must be low during the complete data frame (8-bit or 16-bit) transfer process. In NSS software mode, set the SSMEN bit in the SPI_CTRL1 register and clear the SSEL bit.
5. Clear the SPI_CTRL1.MSEL bit, set the SPI_CTRL2.SPIEN bit to operate the corresponding pins in SPI mode. In this configuration, the MOSI pin is the data input, and the MISO pin is the data output.

Data Transmission Process

In a write operation, data words are written in parallel to the transmit buffer. When the slave device receives the clock signal and the first data bit appears on the MOSI pin, the transmission process begins (note: at this point, the first bit is sent out). The remaining bits (7 bits for 8-bit data frame format, 15 bits for 16-bit data frame format) are loaded into the shift register. When the data from the transmit buffer is transferred to the shift register, the TE flag in the SPI_STS register is set, and if the TEINTEN bit in the SPI_CR2 register is set, an interrupt will be generated.

Data Reception Process

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For the receiver, when data reception is completed:

- The data from the shift register is transferred to the receive buffer, and the RNE flag in the SPI_STS register is set.
- If the RNEINTEN bit in the SPI_CTRL2 register is set, an interrupt will be generated.

After the last sampling clock edge, the RNE bit is set to '1', and the received data byte in the shift register is transferred to the receive buffer. When reading the SPI_DAT register, the SPI device returns the value from this receive buffer. The RNE bit is cleared when reading the SPI_DAT register.

36.3.2.2 Configuring SPI as Master Mode

Configuration Process:

1. Define the serial clock baud rate through the BR[2:0] bits of the SPI_CTRL1 register.
2. Choose the SPI_CTRL1.CLKPOL and SPI_CTRL1.CLKPHA bits to define the phase relationship between data transfer and the serial clock.
3. Set the SPI_CTRL1.DATFF bit to define the 8-bit or 16-bit data frame format.
4. Configure the LSBFF bit of the SPI_CTRL1 register to define the frame format.
5. If the NSS pin needs to operate in input mode, in hardware mode, the NSS pin should be connected to a high level during the entire data frame transmission; in software mode, set the SSMEN bit and SSEL bit in the SPI_CTRL1 register. If the NSS pin operates in output mode, only set the SPI_CTRL1.SSOEN bit.
6. The SPI_CTRL1.MSEL and SPI_CTRL2.SPIEN bits must be set (these bits can only remain set when the NSS pin is connected to a high level). In this configuration, the MOSI pin is the data output, and the MISO pin is the data input

Data Transmission Process

When writing data to the transmit buffer, the transmission process begins. When sending the first data bit, the data word is parallelly (via the internal bus) loaded into the shift register and then serially shifted out to the MOSI pin; whether the MSB comes first or the LSB comes first depends on the setting of the LSBFF bit in the SPI_CTRL1 register. The TE flag is set when the data is transferred from the transmit buffer to the shift register, and if the TEINTEN bit in the SPI_CTRL2 register is set, an interrupt will be generated.

Data Reception Process

For the receiver, when data transmission is complete:

- The data from the shift register is transferred to the receive buffer, and the RNE flag is set.
- If the RNEINTEN bit in the SPI_CTRL2 register is set, an interrupt will be generated.

After the last sampling clock edge, the RNE bit is set, and the received data byte in the shift register is transferred to the receive buffer. When reading the SPI_DAT register, the SPI device returns the data from the receive buffer.

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Reading the SPI_DAT register clears the RXNE bit. Once the transmission starts, a continuous flow of transmission can be maintained if the next data to be sent is placed in the transmit buffer. Before attempting to write to the transmit buffer, ensure that the TE flag is set to '1'.

Note: In NSS hardware mode, the NSS input of the slave device is controlled by the NSS pin or another GPIO pin driven by software.

36.3.2.3 Configuring SPI for Simplex Communication

The SPI module can operate in simplex mode in two configurations:

1. 1 clock line and 1 bidirectional data line;
2. 1 clock line and 1 data line (receive only or transmit only)

1 clock line and 1 bidirectional data line (BIDIRMODE=1)

Enable this mode by setting the BIDIRMODE bit in the SPI_CTRL1 register. In this mode, the SCK pin serves as the clock, with the master device using the MOSI pin and the slave device using the MISO pin for data communication. The direction of the transmission is controlled by the BIDIROEN in the SPI_CTRL1 register, where the data line is set as output when this bit is '1', otherwise it is set as input.

1 clock line and 1 unidirectional data line (BIDIRMODE=0)

In this mode, the SPI module can operate either as transmit only or receive only.

- Transmit only mode is similar to full-duplex mode (BIDIRMODE=0, RONLY=0): data is transmitted on the transmit pin (MOSI in master mode, MISO in slave mode), while the receive pin (MISO in master mode, MOSI in slave mode) can be used as a general-purpose I/O. In this case, the software does not need to be concerned with the data in the receive buffer (if the data register is read, it does not contain any received data).
- In receive only mode, the output function of the SPI can be disabled by setting the RONLY bit in the SPI_CTRL1 register; in this case, the transmit pin (MOSI in master mode, MISO in slave mode) is released and can be used for other functions. Configuring and enabling the SPI module in receive-only mode involves:
- In master mode, once the SPI is enabled, communication starts immediately, and the current reception stops when the SPIEN bit is cleared. In this mode, there is no need to read the BUSY flag, as it remains '1' throughout the SPI communication.

In slave mode, as long as the NSS is pulled low (or in NSS software mode, the SSI bit is '0') and there are clock pulses on the SCK, the SPI continues to receive.

36.3.3 Data Transmission and Reception Process

36.3.3.1 Receive and Transmit Buffers

During reception, the received data is stored in an internal receive buffer; during transmission, data is first stored in an internal transmit buffer before being sent. Reading from the SPI_DAT register returns the content of the receive buffer, while writing data to the SPI_DAT register writes the data into the transmit buffer.

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36.3.3.2 Initiating Transmission in Master Mode

- Full-Duplex Mode (BIDIRMODE=0 and RONLY=0)
  - Transmission begins after writing data to the SPI_DAT register (transmit buffer).
  - During the transmission of the first data bit, the data is parallelly transferred from the transmit buffer to an 8-bit shift register and then sequentially shifted out to the MOSI pin.
  - Simultaneously, the data received on the MISO pin is sequentially shifted into an 8-bit shift register and then parallelly transferred to the SPI_DAT register (receive buffer).
- Unidirectional Receive-Only Mode (BIDIRMODE=0 and RONLY=1)
  - Transmission starts when SPIEN=1.
  - Only the receiver is active, and the data received on the MISO pin is sequentially shifted into an 8-bit shift register and then parallelly transferred to the SPI_DAT register (receive buffer).
- Bidirectional Mode, Transmitting (BIDIRMODE=1 and BIDIROEN=1)
  - Transmission begins after writing data to the SPI_DAT register (transmit buffer).
  - During the transmission of the first data bit, the data is parallelly transferred from the transmit buffer to an 8-bit shift register and then sequentially shifted out to the MOSI pin.
  - No data is received.
- Bidirectional Mode, Receiving (BIDIRMODE=1 and BIDIROEN=0)
  - Transmission starts when SPIEN=1 and BIDIROEN=0.
  - The data received on the MOSI pin is sequentially shifted into an 8-bit shift register and then parallelly transferred to the SPI_DAT register (receive buffer).
  - The transmitter is not activated, and no data is sequentially shifted out to the MOSI pin.

36.3.3.3 Initiating Reception in Master Mode

- Full-Duplex Mode (BIDIRMODE=0 and RONLY=0)
  - Transmission begins when the slave device receives the clock signal and the first data bit appears on its MOSI, followed by the sequential movement of subsequent data bits into the shift register.
  - Simultaneously, during the transmission of the first data bit, the data from the transmit buffer is parallelly transferred to an 8-bit shift register and then serially sent to the MISO pin. The software must ensure that the data to be sent is written into the transmit buffer before the SPI master device starts data transmission.
- Unidirectional Receive-Only Mode (BIDIRMODE=0 and RONLY=1)
  - Transmission starts when the slave device receives the clock signal and the first data bit appears on its MOSI, followed by the sequential movement of subsequent data bits into the shift register.
  - The transmitter is not activated, and no data is serially sent to the MISO pin.
- Bidirectional Mode, Transmitting (BIDIRMODE=1 and BIDIROEN=1)
  - Transmission begins when the slave device receives the clock signal and the first data bit from the transmit buffer is sent to the MISO pin.

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- uring the transmission of the first data bit to the MISO pin, the data to be sent from the transmit buffer is parallelly transferred to an 8-bit shift register and then serially sent to the MISO pin. The software must ensure that the data to be sent is written into the transmit buffer before the SPI master device starts data transmission.
- No data is received.

- Bidirectional Mode, Receiving (BIDIRMODE=1 and BIDIROEN=0)

- Transmission starts when the slave device receives the clock signal and the first data bit appears on its MOSI.
- The data received on the MISO pin is serially transferred to an 8-bit shift register, then parallelly transferred to the SPI_DAT register (receive buffer).
- The transmitter is not activated, and no data is serially sent to the MISO pin.

36.3.3.4 Handling Data Transmission and Reception

When data is transferred from the transmit buffer to the shift register, the TE flag (transmit buffer empty) is set, indicating that the internal transmit buffer is ready to receive the next data; if the TEINTEN bit is set in the SPI_CTRL2 register, an interrupt will be generated at this point; writing to the SPI_DAT register clears the TE bit.

Note: Before writing to the transmit buffer, the software must ensure that the TE flag is '1', otherwise new data will overwrite the existing data in the transmit buffer.

At the last edge of the sampling clock, when the data is transferred from the shift register to the receive buffer, the RNE flag (receive buffer not empty) is set; it indicates that the data is ready to be read from the SPI_DAT register; if the RNEINTEN bit is set in the SPI_CTRL2 register, an interrupt will be generated at this point; reading from the SPI_DAT register clears the RNE flag. In some configurations, when transmitting the last data, the BUSY flag can be used to wait for the end of the data transmission.

36.3.3.5 Full-Duplex Transmission and Reception Process in Master or Slave Mode (BIDIRMODE=0 and RONLY=0)

➢ Master full duplex mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)

After the first data is written to the SPI_DAT register, the transmission will start. When the first bit of the data is sent, the data bytes are loaded from the data register into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the data bits follow the MSB or LSB order are serially shifted to the MOSI pin. At the same time, the data receives on the MISO pin is serially shifted into the shift register in the same order and then loaded into the SPI_DAT register in parallel. The software operation process is as follows:

- Set SPI_CTRL2.SPIEN = 1, Enable SPI module.
- Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
- Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Wait for SPI_STS.RNE bit to be set to '1', read SPI_DAT to get the first received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT. Repeat the above operation, sending subsequent data and receiving n-1 data at the same time;

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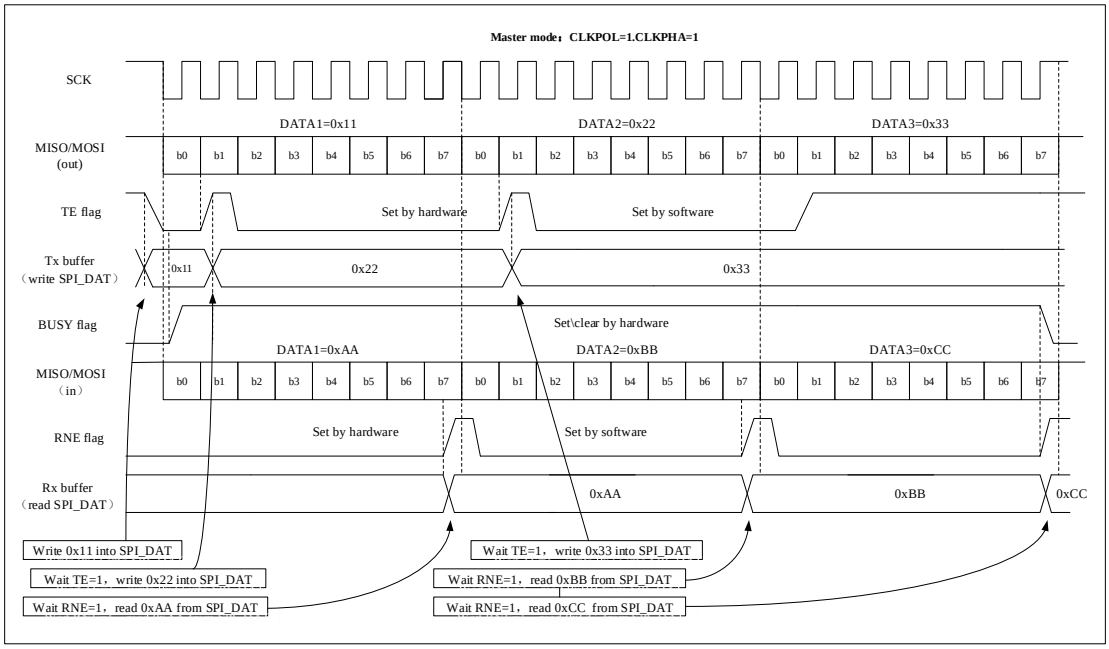
- Wait for SPI_STS.RNE bit to be set to '1' to receive the last data;
- Wait for SPI_STS.TE to be set to '1', then wait for SPI_STS.BUSY bit to be cleared and turn off SPI module.

The process of data transmitting and data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE or SPI_STS.TE flag.

Figure 36-8 TE/RNE/BUSY Behavior in Master / Full-Duplex Mode(BIDIRMODE = 0, RONLY = 0) during Continuous Transmission



- Slave full duplex mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)

The data transfer process begins when the slave device receives the first clock edge. The data serially moves into the shift register.

At the same time, while transmitting the first data bit, the data in the transmit buffer is parallel transferred to the shift register, and then serially sent out to the MISO pin. Software must ensure that the data to be transmitted is written into the slave transmit buffer before the SPI master device starts data transfer.

Figure 36-9 TE/RNE/BUSY Behavior in Slave / Full-Duplex Mode(BIDIRMODE = 0, RONLY = 0) during Continuous

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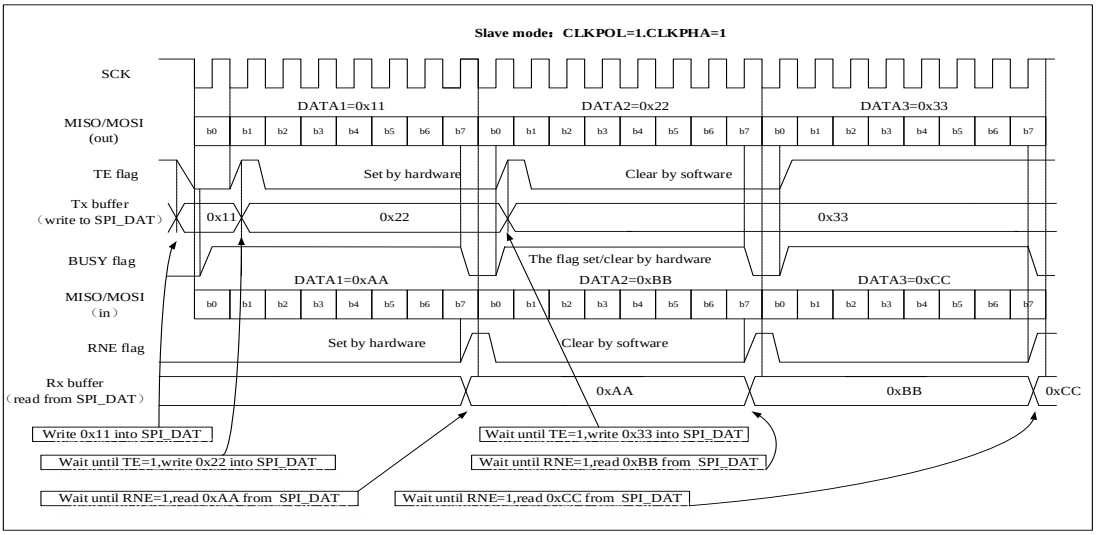
Transfers



- Master two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL=1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)

Master two-wire unidirectional transmit-only mode is similar to master full-duplex mode. The difference is that this mode will not read the received data, so the SPI_STS.OVER bit will be set to '1', and the software will ignore it. The software operation process is as follows:

- Set SPI_CTRL1.SPIEN = 1 to enable SPI module.
- Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
- Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Repeat this operation to send subsequent data;

After writing the last data to SPI_DAT, wait for SPI_STS.TE bit to set '1'; then wait for SPI_STS.BUSY bit to be cleared to complete the transmission of all data. This process can also be implemented in the interrupt handler triggered by the rising edge of the SPI_STS.TE flag.

Note:

1. *For discontinuous transmissions, there is a 2 APB clock cycle delay between writing to the SPI_DAT register and setting the BUSY bit. Therefore, in transmit-only mode, it is advisable to wait for TE=1 after writing the last data, and then wait for BUSY=0.*
2. *In transmit-only mode, after transmitting two data, the OVER bit in the SPI_STS register becomes '1' due to not reading the received data. (Note: Software does not need to worry about this OVR flag).*

Figure 36-10 **TXE/BSY Behavior in Master Transmit-Only Mode(BIDIRMODE = 0, RONLY = 0) during Continuous Transfers**

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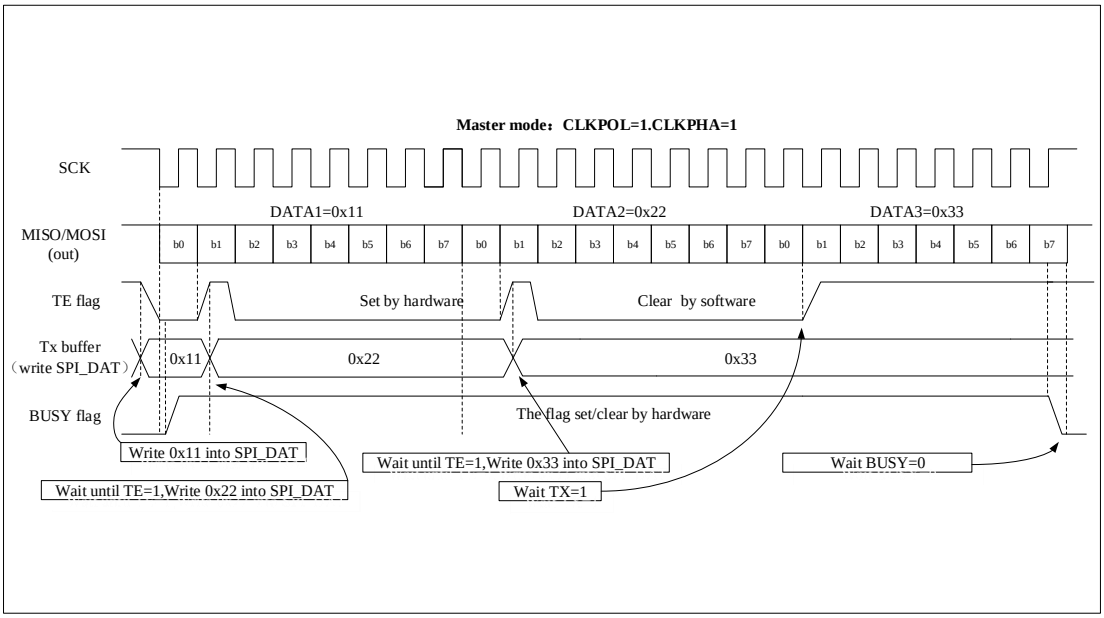
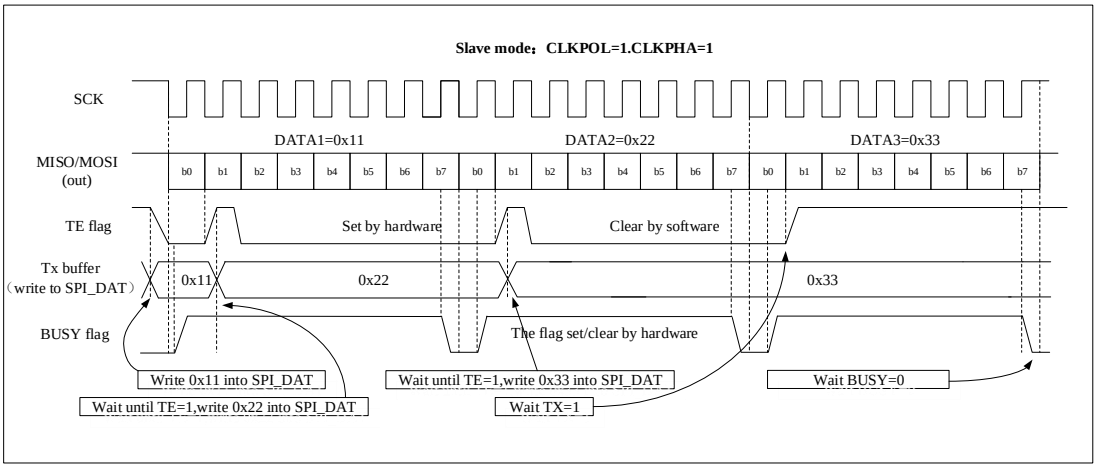


- Slave two-wire unidirectional transmit-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 0)

Figure 36-11 **TE/BUSY Behavior in Slave Transmit-Only Mode in Case of Continuous Transfers**



36.3.3.6 Bidirectional Transmission Process (BIDIRMODE=1 and BIDIROEN=1)

In this mode, the operation process is similar to the transmit-only mode, with the difference that before enabling the SPI module, both the BIDIRMODE and BIDIROEN bits in the SPI_CTRL1 register need to be set to '1'.

36.3.3.7 Unidirectional Receive-Only Mode (BIDIMODE=0 and RXONLY=1)

When SPI_CTRL1.SPIEN = 1, the receiving process starts. The data bits from the MISO pin are sequentially shifted into the shift register and then loaded into the SPI_DAT register(receive buffer) in parallel. The software operation process is as follows:

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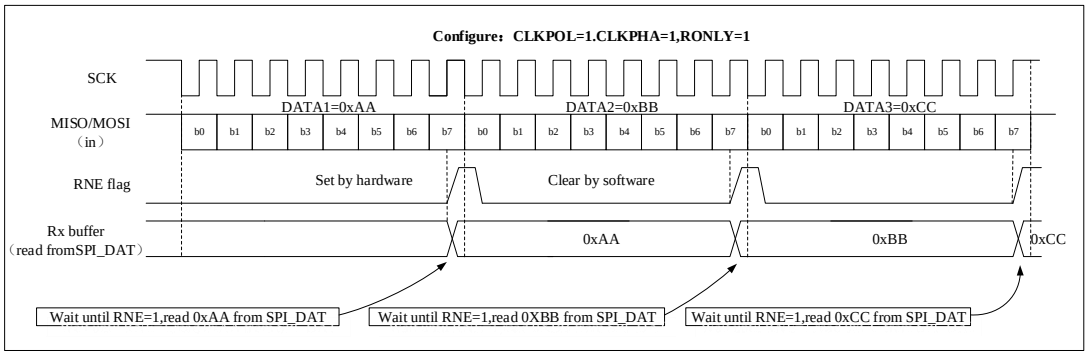
- Set SPI_CTRL1.RONLY = 1 to enable the receive-only mode.
- In master mode, setting the SPI_CTRL2.SPIEN bit to 1 enables the SPI module, and the SCLK signal is generated immediately. Data is continuously received until the SPI is disabled (SPI_CTRL2.SPIEN = 0). In slave mode, when the master device drives the NSS signal low and generates SCLK, data is continuously received.
- Wait for SPI_STS.RNE bit to be set to '1', read the SPI_DAT register to get the received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT register. Repeat this operation to receive all data.The process of data receiving can also be implemented in the interrupt handler generated by the rising edge of the RNE flag (SPI_STS.RNE).

Figure 36-12 **RNE Behavior in Receive-Only Mode in Case of Continuous Transfers (BIDIRMODE = 0 , RONLY = 1)**



36.3.3.8 Bidirectional Reception Process (BIDIMODE=1 and BIDIOE=0)

In this mode, the operation process is similar to the receive-only mode, with the difference that before enabling the SPI module, the BIDIRMODE bit in the SPI_CTRL2 register needs to be set to '1' and the BIDIROEN bit needs to be cleared to '0'.

36.3.3.9 Continous and discontinous transmission

When sending data in master mode, if the software is fast enough to detect each TE (SPI_STS.TE) rising edge (or TE interrupt), and the data is written to the SPI_DAT register immediately before the end of the ongoing transmission. At this time, the SPI clock remains continuous between the transmission of data items, and the SPI_STS.BUSY bit will not be cleared, continuous communication can be achieved.

If the software is not fast enough, it will result in discontinuous communication; in this case, the SPI_STS.BUSY bit is cleared between the transmission of each data items.

In master receive-only mode (SPI_CTRL1.RONLY = 1), communication is always continuous and the BUSY flag (SPI_STS.BUSY) is always high.

In slave mode, the continuity of communication is determined by the SPI master device. However, even if the communication is continuous, the BUSY flag (SPI_STS.BUSY) will be low for at least one SPI clock cycle between each data item.

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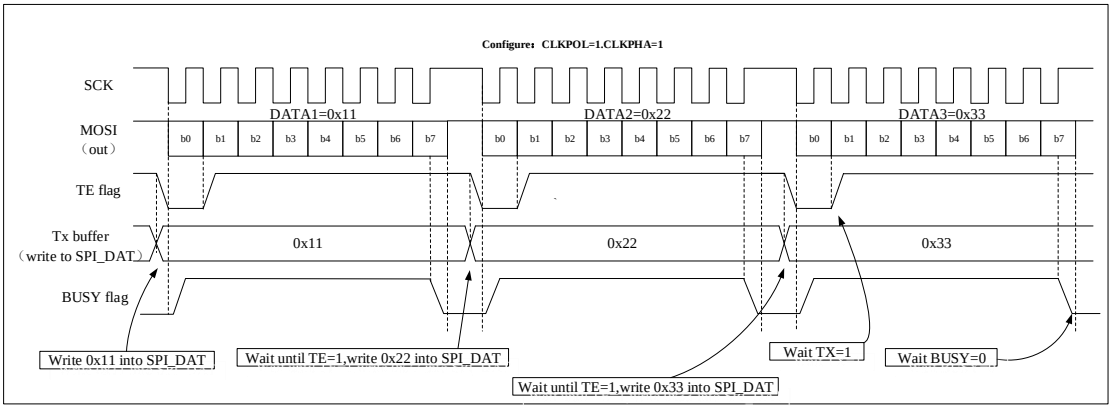
Note: If you want the NSS to toggle with each frame of data, i.e., pulled low during frame transmission and pulled high after frame transmission, the user can enable the SPI before frame transmission and disable it after transmission is completed.

Figure 36-13 **TE/BUSY Behavior in Non-Continuous Transmission (BIDIRMODE = 0 and RONLY = 0)**



36.3.3.10 SPI initialization process

1) The baud rate of serial clock is defined by the SPI_CTRL1.BR[2:0] bits (this step is ignored if it is working in slave mode).
2) Select SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit to define the phase relationship between data transmission and serial clock.
3) Set SPI_CTRL1.DATFF bit to define 8-bit or 16-bit data frame format.
4) Configure the SPI_CTRL1.LSBFF bit to define the frame format.
5) Configure the NSS mode as described above for the NSS function.
6) Run mode is configured by SPI_CTRL1.MSEL bit, SPI_CTRL1.BIDIRMODE bit, SPI_CTRL1.BIDIROEN bit and SPI_CTRL1.RONLY bit.
7) Set the SPI_CTRL1.SPIEN = 1 to enable SPI.

36.3.3.11 Basic SPI send and receive processing

When SPI sends a data frame, it firstly loads the data frame from the data buffer into the shift register, and then starts to send the loaded data. When the data is transferred from the transmit buffer to the shift register, the transmit buffer empty flag is set (SPI_STS.TE = 1), and the next data can be loaded into the send buffer; if the TEINTEN bit is set (SPI_CTRL2.TEINTEN = 1), an interrupt will be generated; writing data to the SPI_DAT register will clear the SPI_STS.TE bit.

At the last edge of the sampling clock, when the data is transferred from the shift register to the receive buffer, the receive buffer non-empty flag is set (SPI_STS.RNE = 1), at this time the data is ready and can be read from the SPI_DAT register; if the receive buffer non-empty interrupt is enabled (SPI_CTRL2.RNEINTEN = 1), an interrupt will be generated; the SPI_STS.RNE bit can be cleared by reading the SPI_DAT register data.

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In master mode, the transmitting process starts when data is written to the send buffer. If the next data has been written into the SPI_DAT register before the current data frame sending is completed, the continuous sending function can be achieved.

In slave mode, the NSS pin is low, and when the first clock edge arrives, the transmission process begins. In order to avoid accidental data transmission, software must write data to the transmit buffer before data transmission (it is recommended to enable the SPI module before the master sends the clock).

In some configurations, when the last data is sent, the BUSY flag (SPI_STS.BUSY) can be used to wait for the end of the data sending.

36.3.4 CRC Calculation

SPI can enable CRC calculation through follow steps:

- Write the polynomial into the SPI_CRCPOLY register.
- Enable CRC calculation by setting the SPI_CTRL2.CRCEN bit, which will also clear the SPI_CRCRDAT and SPI_CRCTDAT registers.
- Set the SPI_CTRL2.SPIEN bit to enable the SPI module.
- Start and continue transmitting data until only the last byte or half-word remains in the current communication.
- After the last data is written into the transmit buffer, set the SPI_CTRL1.CRCNEXT = 1, which indicates that the hardware will start transmitting the CRC value (SPI_CRCTDAT value) after transmitting the data. When the CRC is sent, the CRC calculation will stop.
- When the last byte or half-word is sent, the SPI sends the CRC value, and the SPI_CTRL1.CRCNEXT bit is cleared. Similarly, the received CRC is compared with the SPI_CRCRDAT value. If they do not match, the SPI_STS.CRCERR flag is set. If SPI_CTRL2.ERRINTEN is set, an interrupt is generated.

Note: When the SPI module is in slave mode, please ensure that CRC calculation is enabled only after the clock is stable to avoid incorrect CRC calculation results. As long as the SPI_CTRL2.CRCEN bit is set and there is an input clock on the SCK pin, CRC calculation will be performed regardless of the state of the SPI_CTRL2.SPIEN bit.

When the SPI clock frequency is high, users must be cautious when sending CRC. During CRC transmission, the CPU usage should be minimized as much as possible. To avoid errors when receiving the final data and CRC, function calls should be disabled during the CRC sending process. Setting the CRCNEXT bit must be completed before sending/receiving the last piece of data.

When the SPI clock frequency is high, as CPU operations can impact the SPI bandwidth, it is recommended to use DMA mode to avoid slowing down the SPI frequency.

When the SPI is configured as a slave and NSS hardware mode is used, the NSS pin should remain low during both data and CRC transmission. When the SPI is configured as a slave and using CRC functionality, the CRC calculation will still be performed even if the NSS pin is high (CRC calculation will continue if there are clock pulses on the SCK pin while the NSS signal is high. For example, this can occur when the master device alternates communication between multiple slave devices. Setting the SPI_CTRL2[13] bit can prevent incorrect CRC operation in this scenario).

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In order to keep the synchronization of the next CRC calculation results between the master and slave devices when transitioning from deselecting one slave device (NSS signal high) to selecting a slave device (NSS signal low), the CRC values at both ends (master and slave) should be cleared.

Clear the CRC values according to the following steps:

1) Disable the SPI module (SPI_CTRL2.SPIEN=0)
2) Clear the SPI_CTRL2.CRCEN bit to '0'
3) Set the SPI_CTRL2.CRCEN bit to '1'
4) Enable the SPI module (SPI_CTRL2.SPIEN=1)

Transmit the CRC

In non-FIFO mode:

- In CPU mode, the user needs to set the SPI_CTRL1.CRCNEXT bit to 1 before transmitting the last frame of data.
- In DMA mode, the hardware automatically transmits the CRC check value.

In FIFO mode:

- In CPU mode, if it is receive-only mode, the CRC will automatically be transmitted based on the value configured in the SPI_TRANS_NUM register by the user.
- In CPU mode, except for receive-only mode, the user needs to configure the SPI_CTRL1.CRCNEXT bit to 1 before transmitting the last data to transmit the CRC value.
- In DMA mode, the hardware automatically transmits the CRC check value.

Note: In practical applications, if software-calculated CRC needs to match the hardware-calculated result, the following settings need to be correctly configured:

CRC8/CRC16

- width:8/16
- Polynomial (POLY): Configurable through the SPI_CRCPOLY register.
- Initial value (INIT): 0x0000
- Input data reverse (REFIN): No
- Output data reverse (REFOUT): No

36.3.5 Status Flag

The SPI_STS register has 3 flag bits to monitor the status of the SPI:

Send buffer empty flag bit (TE)

When the send buffer is empty, the TE flag (SPI_STS.TE) is set to 1, which means that new data can be written into the SPI_DAT register. When the send buffer is not empty, the hardware will clear this flag to 0.

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Receive buffer non-empty flag bit (RNE)

When the receive buffer is not empty, the RNE flag (SPI_STS.RNE) is set to 1, so the user knows that there is data in the receive buffer. After reading the SPI_DAT register, the hardware will set this flag to 0.

BUSY flag bit (BUSY)

When the transmission starts, the hardware sets the BUSY flag (SPI_STS.BUSY) to 1, and after the transmission ends, the hardware sets the BUSY flag to 0.

Only when the device is in the master one-wire bidirectional receive mode, the BUSY flag (SPI_STS.BUSY) will be set to 0 when the communication is in progress.

The BUSY flag (SPI_STS.BUSY) will be cleared to 0 in the following cases:

- End of transmission (except for continuous communication in master mode);
- Disable the SPI module (SPI_CTRL1.SPIEN = 0);
- The master mode error occurs (SPI_STS.MODERR = 1)

In non-continuous communication, the BUSY flag is low between the transmission of each data item.

In continuous communication:

- In master mode: the BUSY flag remains high throughout the entire transmission process
- In slave mode: the BUSY flag is low for one SPI clock cycle between the transmission of each data item.

Note: It is not recommended to use the BUSY flag to handle the transmission and reception of each data item; it is better to use the TE and RNE flags.

36.3.6 Disabling SPI

When communication is complete, it is possible to terminate the communication by closing the SPI module. Closing the SPI can be achieved by clearing the SPIEN bit. In certain configurations, prematurely closing the SPI module and entering standby mode before the transmission is complete can result in the current transmission being disrupted, and the BUSY flag becoming unreliable. To avoid such situations, it is recommended to follow the steps below when closing the SPI module:

- **Master or slave full duplex mode(SPI_CTRL1.BIDIMODE=0，SPI_CTRL1.RONLY=0)**
  1) Wait for the RNE flag (SPI_STS.RNE) to be set to 1 and the last byte to be received;
  2) Wait for the TE flag (SPI_STS.TE) to be set to 1;
  3) Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
  4) Turn off the SPI module (SPI_CTRL1.SPIEN = 0).
- **Two-wire unidirectional transmit-only mode(SPI_CTRL1.BIDIMODE=0，SPI_CTRL1.RONLY=0) or one-wire bidirectional transmit mode(SPI_CTRL1.BIDIMODE=1， SPI_CTRL1.BIDIROEN=1) for master or slave**
  1) After writing the last byte to the SPI_DAT register, wait for the TE flag (SPI_STS.TE) to be set to 1;
  2) Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;

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3) Disable the SPI module (SPI_CTRL1.SPIEN = 0).

Note: In master mode with unidirectional transmit-only mode, the SPI_STS.BUSY flag remains low during the transmission process.

- **Two-wire unidirectional receive-only mode(SPI_CTRL1.MSEL=1， SPI_CTRL1.BIDIMODE=0，SPI_CTRL1.RONLY=1) or one-wire bidirectional receive mode(SPI_CTRL1.MSEL=1 ，SPI_CTRL1.BIDIMODE=1，SPI_CTRL1.BIDIROEN=0) for master**

  This scenario needs to be handled specifically to ensure that the SPI does not initiate a new transmission:

  1) Wait for the penultimate RNE (SPI_STS.RNE) to be set to 1;
  2) Before closing the SPI module (SPI_CTRL1.SPIEN = 0), wait for 1 SPI clock cycle (using software delay);
  3) Wait for the last RNE (SPI_STS.RNE) to be set before entering shutdown mode (or disabling the SPI module clock).

- **Two-wire unidirectional receive-only mode(SPI_CTRL1.MSEL=0， SPI_CTRL1.BIDIMODE=0，SPI_CTRL1.RONLY=1) or one-wire bidirectional receive mode(SPI_CTRL1.MSEL=0 ，SPI_CTRL1.BIDIMODE=1，SPI_CTRL1.BIDIROEN=0) for slave**

  1) The SPI module can be disabled at any time (SPI_CTRL1.SPIEN = 0), and after the current transfer is over, the SPI module will be disabled;
  2) If you want to enter the shutdown mode, you must wait for the BUSY flag (SPI_STS.BUSY) to be set to 0 before entering the shutdown mode (or disable the SPI module clock).

36.3.7 SPI Communication Using DMA

To achieve maximum communication speed, it is necessary to promptly fill the SPI transmit buffer with data and also read data from the receive buffer in a timely manner to prevent overflow. To facilitate high-speed data transfer, SPI implements a simple request/response DMA mechanism.

When the corresponding enable bit on the SPI_CTRL2 register is set, the SPI module can issue DMA transfer requests. The transmit buffer and receive buffer also have their own DMA requests.

- When the send buffer DMA is enabled (SPI_CTRL2.TDMAEN = 1), each time the TE flag (SPI_STS.TE) bit is 1, a DMA request will be generated, and the DMA will automatically write the data to the SPI_DAT register, which will clear the TE flag (SPI_STS.TE) bit.
- When the receive buffer DMA is enabled (SPI_CTRL2.RDMAEN = 1), each time the RNE flag (SPI_STS.RNE) bit is set to 1, a DMA request will be generated, and the DMA will automatically read the SPI_DAT register, which will clear the RNE flag (SPI_STS.RNE) bit.

When the SPI is only used for transmitting data, only the transmit DMA channel of the SPI needs to be enabled (SPI_CTRL2.TDMAEN = 1). At this time, since the received data has not been read, the OVER flag is set to '1' (software does not need to pay attention to this flag).

When the SPI is only used for receiving data, only the receive DMA channel of the SPI needs to be enabled (SPI_CTRL2.RDMAEN = 1).

In transmit mode, after DMA has sent all the data to be sent (DMA_INTSTS.TXCF = 1), BUSY flag (SPI_STS.BUSY)

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can monitor to confirm whether SPI communication is over, which can avoid destroying the transmission of the last data when the SPI is turned off or enters the shutdown mode. Therefore, the software needs to wait for the TE flag (SPI_STS.TE) bit to be set to 1, and wait for the BUSY flag (SPI_STS.BUSY) bit to be set to 0.

Note: In discontinuous transfers, there is a delay of 2 APB clock cycles between writing data to the SPI_DAT register and the SPI_STS.BUSY bit being set to '1'. Therefore, after writing the last data, it is necessary to wait for TE=1 first and then wait for SPI_STS.BUSY=0.

Figure 36-14 Transmition Using DMA

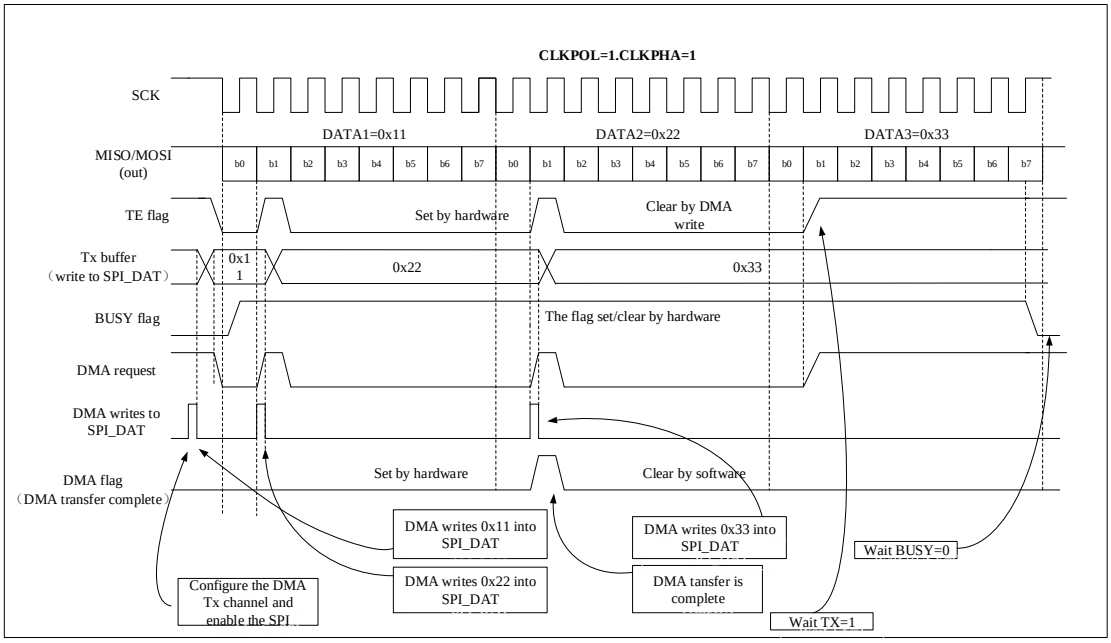
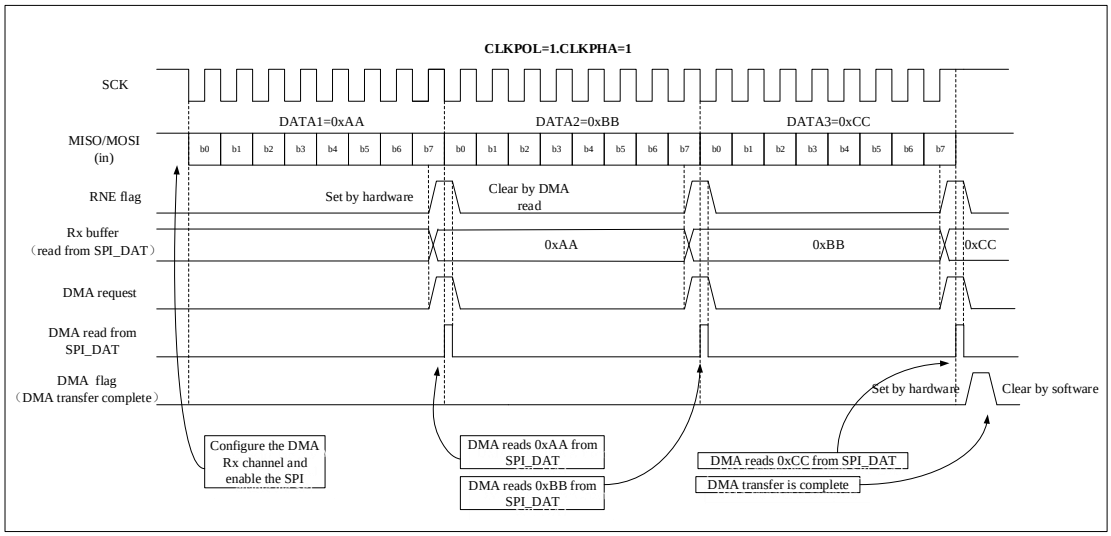


Figure 36-15 Reception Using DMA



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36.3.8 Error Flag

Master mode fault (MODERR)

The following two conditions will cause the master mode fault:

- In NSS pin hardware management mode, the master device NSS pin is pulled low;
- In NSS pin software management mode, the SPI_CTRL1.SSEL bit is set to 0.

The master mode fault has the following impacts on the SPI device:

- When a master mode failure error occurs, the SPI_STS.MODERR bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1).
- The SPI_CTRL1.SPIEN bit and SPI_CTRL1.MSEL bit will be write protected and both are cleared by hardware. SPI is disabled and forced into slave mode
- The SPI_CTRL1.MSEL bit is cleared to '0', forcing the device into slave mode.

The following steps are used to clear the SPI_STS.MODERR bit:

1) Perform a read or write operation to the SPI_STS register
2) Writes to the SPI_CTRL1 register.

In systems with multiple MCUs, to avoid conflicts with multiple slave devices, the NSS pin of the master device must be pulled high before clearing the SPI_STS.MODERR bit. After clearing it, the SPI_CTRL2.SPIEN and SPI_CTRL1.MSEL bits can be restored to their reset state.

Forsecurity reasons, when the SPI_STS.MODERR bit is '1', the hardware does not allow the setting of the SPI_CTRL2.SPIEN and SPI_CTRL1.MSEL bits.

Normally, the SPI_STS.MODERR bit of the slave cannot be set to 1. However, in a multi-master configuration, the slave's SPI_STS.MODERR bit may be set to 1. In this case, the SPI_STS.MODERR bit indicates that there is a multi-master collision. The interrupt routine can perform a reset or return to the default state to recover from an error state.

Overflow Error (OVER)

In SPI non-FIFO mode, When the SPI_STS.RNE bit is set to 1, but there is still data sent into the receive buffer, an overflow error will occur. In SPI FIFO mode, if data is written to the TX FIFO when it is already full, this flag will be set to 1.

When an overflow error occurs:

- The OVER bit is set to "1", when the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated.

For SPI1/SPI2/SPI3/SPI4/SPI5/SPI6/SPI7, when OVER is 1, reading the SPI_DAT register (twice) and then reading the SPI_STS register will clear OVER. For I2S1/I2S2/I2S3/I2S4, when OVER is 1, reading the SPI_DAT register (once) and then the SPI_STS register will clear OVER.

Underflow Error (UNDER)

In SPI non-FIFO mode, this flag is not used; in SPI FIFO mode, attempting to read the RX FIFO when it is empty

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Email: sales@nsing.com.sg

will cause this flag to be set to 1. Reading the SPI_STS status register in software will clear this bit.

CRC Error (CRCERR)

The CRC error flag is used to check the validity of the received data. A CRC error occurs when the received CRC value does not match the SPI_CRCRDAT value. At this time, the SPI_STS.CRCERR flag bit is set to '1', and an interrupt will be generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1).

36.3.9 SPI Interrupt

Table 36-1 SPI Interrupt Request

Interrupt event	Event flag	Enable Control bit
transmit buffer empty flag	TE	TEINTEN
receive buffer not empty flag	RNE	RNEINTEN
master mode fault event	MODERR	ERRINTEN
Overflow error	OVER	
CRC error	CRCERR	
transmit FIFO half-empty flag	TXFIFHE	TXFHEINTEN
receive FIFO half-full flag	RXFIFHF	RXFHFINTEN
receive FIFO full flag	RXFIFFU	RXFFUINTEN
transfer completion flag (receive-only mode)	RXTSCP	RXCPINTEN

36.4 IntroductionI2S Function Description

The block diagram of I2S is shown in the figure below:

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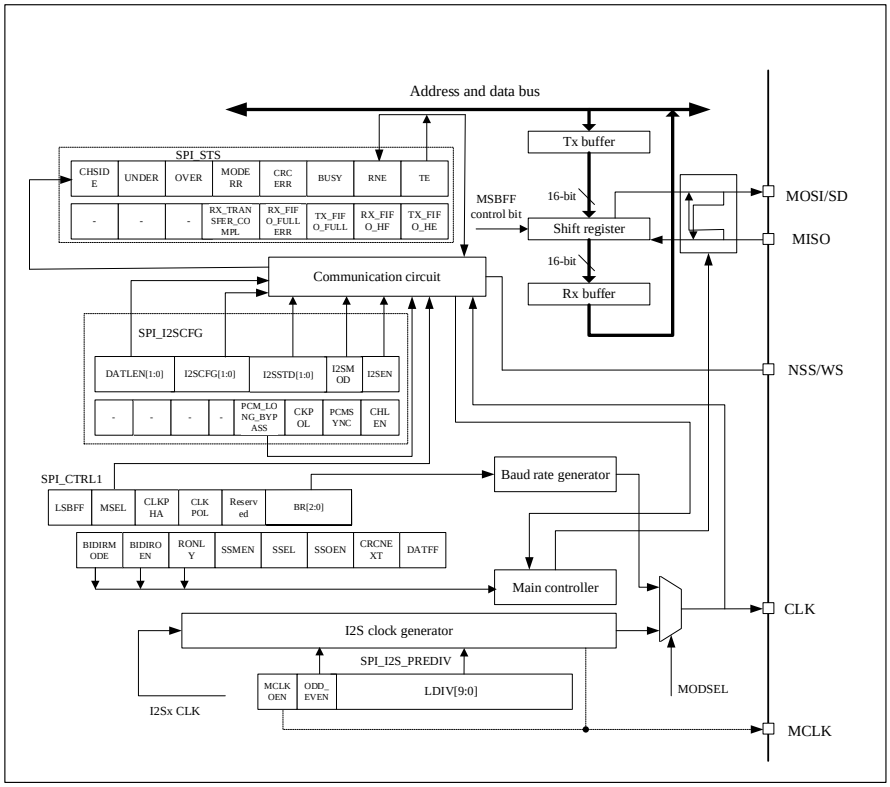
Figure 36-16 I2S Block Diagram



The I2S interface uses the same pins, flags and interrupts as the SPI interface. Setting the SPI_I2S_CFGR. I2SMOD= 1 selects the I2S audio interface.

I2S has a total of 4 pins, 3 of which are shared with SPI:

- SD: serial data (shared with MOSI pin), used for data send and receive (independently mapped).
- SD_1: used only in I2S full-duplex mode for data transmission and reception.
- SCK: serial clock (mapped to the CLK pin), acts as a clock signal output in master mode and as an input in slave mode. In some external audio devices that require a master clock, an additional pin can be used to output the clock.
- WS: Word Select (mapped to the NSS pin), used as a data control signal output in master mode and as an input in slave mode.
- MCK: Master Clock (independently mapped), when I2S is configured as master mode, it is used as an additional clock signal output pin when the MCLKOEN bit of the SPI_I2SPR register is set to '1'. The frequency of the output clock signal is preset to 256 × Fs, where Fs is the sampling frequency of the audio signal.

In master mode, I2S uses its own clock generator to generate clock signals for communication, and this clock generator is also the clock source of the master clock output

36.4.1 I2S Full-dDuplex Function

I2S can be combined with the I2SEXT module to support I2S full-duplex mode. When the I2S and I2SEXT are combined to achieve full-duplex functionality, the I2S can be configured as master or slave mode, while the I2SEXT

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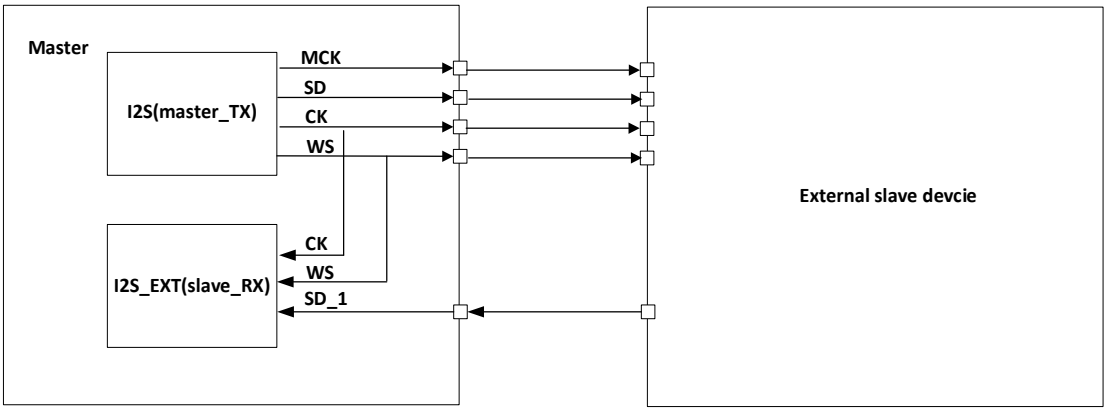
Email: sales@nsing.com.sg

can only be configured as slave mode. I2SEXT shares the CK and WS of I2S, and there are several corresponding configurations:

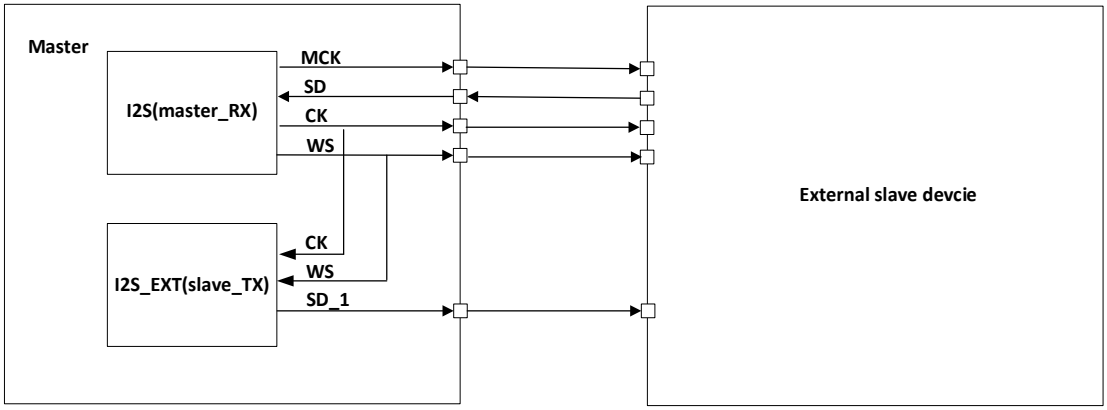
1) I2S configured as master transmit mode (I2SCFG=10), I2S_EXT configured as slave receive mode (I2SCFG=01):

Figure 36-17 I2S master transmit (I2SCFG=10), I2S_EXT slave receive (I2SCFG=01)



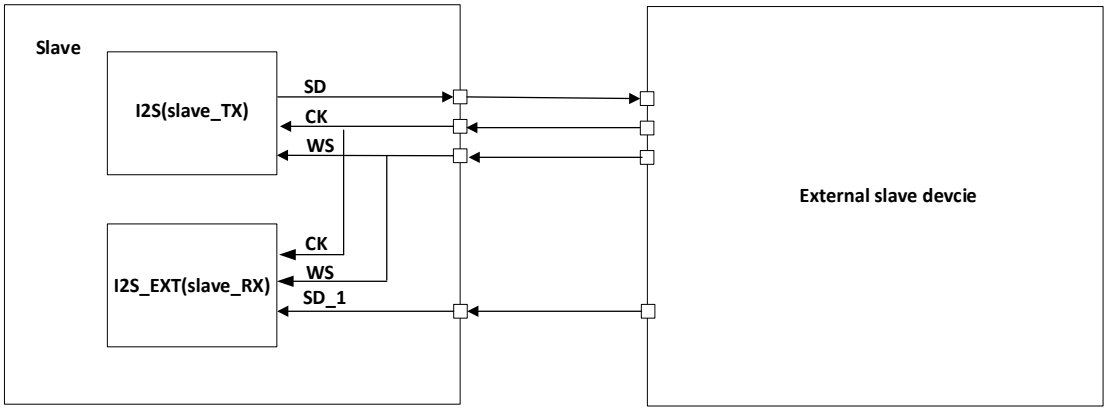
2) I2S configured as master receive mode (I2SCFG=11), I2S_EXT configured as slave transmit mode (I2SCFG=00):

Figure 36-18 I2S master receive (I2SCFG=11), I2S_EXT slave transmit (I2SCFG=00)



3) I2S configured as slave transmit mode (I2SCFG=00), I2S_EXT configured as slave receive mode (I2SCFG=01):

Figure 36-19 I2S slave transmit mode (I2SCFG=00), I2S_EXT slave receive (I2SCFG=01)



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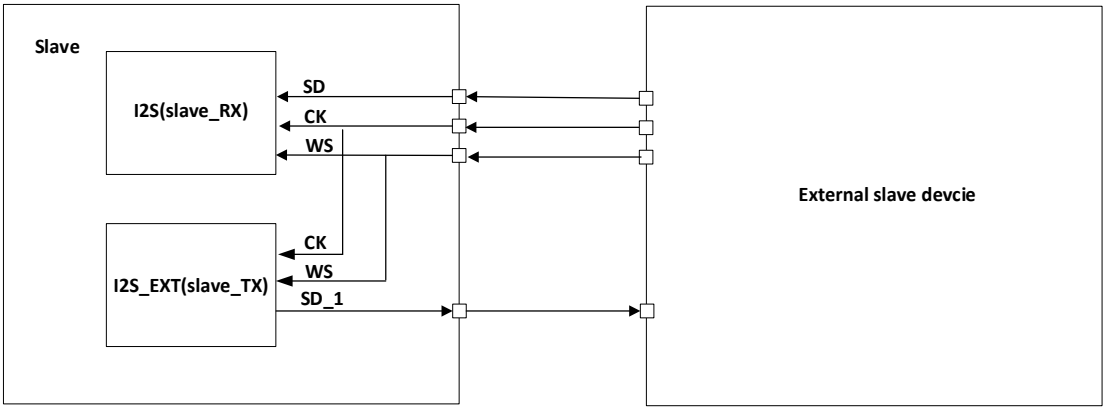
4) I2S configured as slave receive mode (I2SCFG=01), I2S_EXT configured as slave transmit mode (I2SCFG=00):

Figure 36-20 I2S slave receive (I2SCFG=01), I2S_EXT slave transmit (I2SCFG=00)



36.4.2 Supported Audio Protocols

Both the I2S and I2S_EXT modules have a 16-bit data register for transmitting or receiving data. When software writes data to the data register, it writes the corresponding data based on the current channel in the transmission. Similarly, when reading from the register, the received data can be identified for each channel by checking the CHSIDE bit in the register. The left channel always transmit data before the right channel (the CHSIDE bit is not meaningful in PCM protocol).

By setting the SPI_I2SCFG.TDATLEN bits, the user can set the length of the data to be transmitted, and set the data bit width of the channel by setting the SPI_I2SCFG.CHBITS bits. There are 4 data formats for sending data as follows:

- 16-bit data is packed into 16-bit data frame
- 16-bit data is packed into 32-bit data frame(The first 16 bits are valid data, and the last 16 bits are set to 0 by hardware).
- 24-bit data is packed into 32-bit data frame(The first 24 bits are valid data, and the last 8 bits are set to 0 by hardware).
- 32-bit data is packed into 32-bit data frame

I2S uses the same SPI_DAT register as SPI to transmit and receive 16-bit wide data. If I2S needs to transmit or receive 24-bit or 32-bit wide data, the CPU needs to read or write the SPI_DAT register twice. On the other hand, when I2S transmits or receives 16-bit wide data, the CPU only needs to read or write the SPI_DAT register once.

Regardless of which data format and communication standard is used, I2S always sends the data high-order bit (MSB) first.

36.4.2.1 I2S Philips standard

Using the I2S Philips standard, the device that transmits data on the falling edge of the clock, and the device that receives data on the rising edge of the clock. The WS signal should be valid one clock before the first data bit (MSB) is sent and will change on the falling edge of the clock signal.

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Figure 36-21 I2S Philips Protocol Waveform (16/32-Bit Full Precision, CLKPOL = 0)

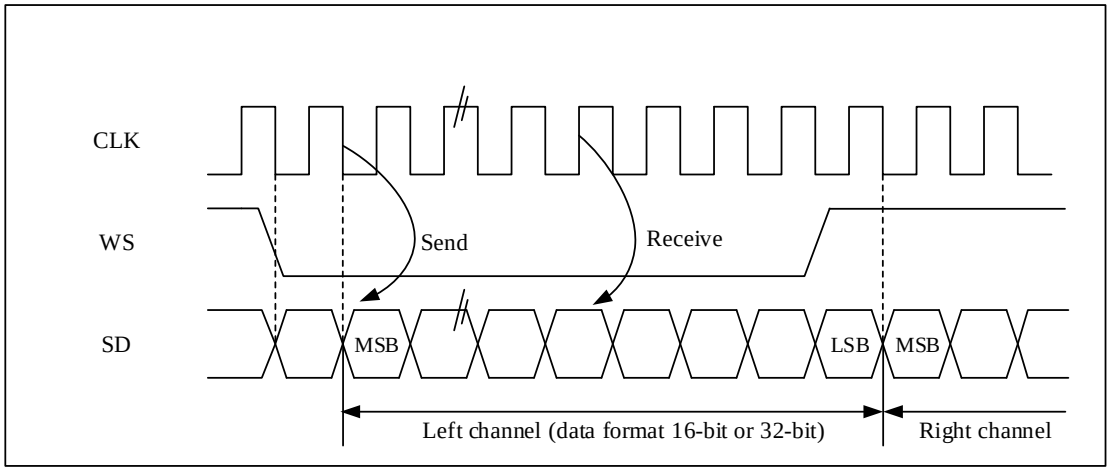
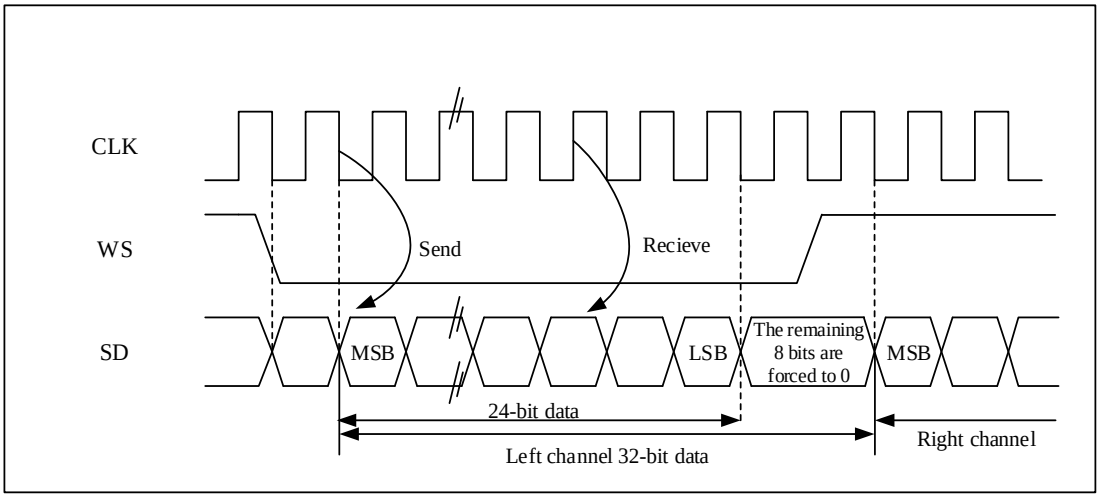


Figure 36-22 I2S Philips Protocol Standard Waveform (24-Bit Frame, CLKPOL = 0)



If the 24-bit data needs to be packaged into 32-bit data frame format, the CPU needs to read or write the SPI_DAT register twice during each frame of data transmission. For example, if the user sends 24-bit data 0x95AA66, the CPU will first write 0x95AA into the SPI_DAT register, and then write 0x66XX into the SPI_DAT register (only the upper 8-bit data is valid, the lower 8-bit data is meaningless and can be any value); if the user receives 24-bit data 0x95AA66, the CPU will first read the SPI_DAT register to get 0x95AA, and then read the SPI_DAT register to get 0x6600 (only the upper 8-bit data is valid, and the lower 8-bit data is always 0).

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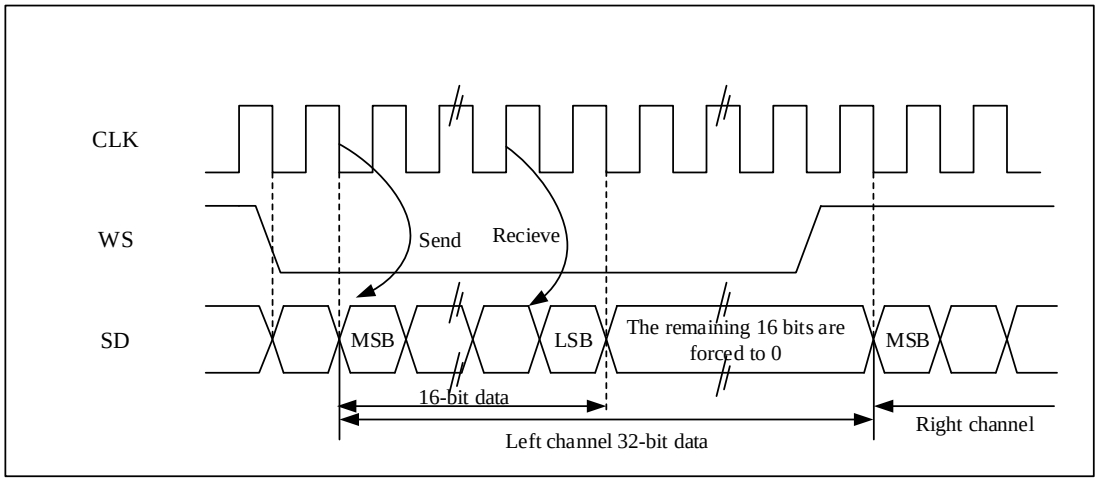
Figure 36-23 I2S Philips Protocol Standard Waveform (16-Bit Extended to 32-Bit Packet Frame, CLKPOL = 0)



If 16-bit data needs to be packed into 32-bit data frame format, the CPU only needs to read or write the SPI_DAT register once for each frame of data transmission. The lower 16 bits of data for expansion to 32 bits are always set to 0x0000. For example, if the user sends or receives 16-bit data 0x89C1 (extended to 32-bit data is 0x89C10000). In the process of sending data, the upper 16-bit half word (0x89C1) needs to be written into the SPI_DAT register; the user can write new data until the SPI_STS.TE bit is set. An interrupt is generated if the user enables the corresponding interrupt. The sending is performed by hardware, even if the last 16 bits (0x0000) are not sent, the hardware will set the TE (SPI_STS.TE) bit to 1 and the corresponding interrupt will be generated. In the process of receiving data, the RNE flag (SPI_STS.RNE) will be set to 1 after each time the device receives the upper 16-bit halfword (0x89C1). An interrupt is generated if the user enables the corresponding interrupt. In this way, there is more time between 2 reads and writes, which can prevent underflow or overflow from happening.

36.4.2.2 MSB alignment standard

In the MSB alignment standard, the device transmits the data on the falling edge of the clock, and the device receives the data on the rising edge of the clock. The WS signal and the first data bit (MSB) are generated simultaneously.

The standard data receiving and transmitting processing mode is the same as I2S Philips standard.

Figure 36-24 The MSB is Aligned With 16-Bit or 32-Bit Full Precision, CLKPOL = 0

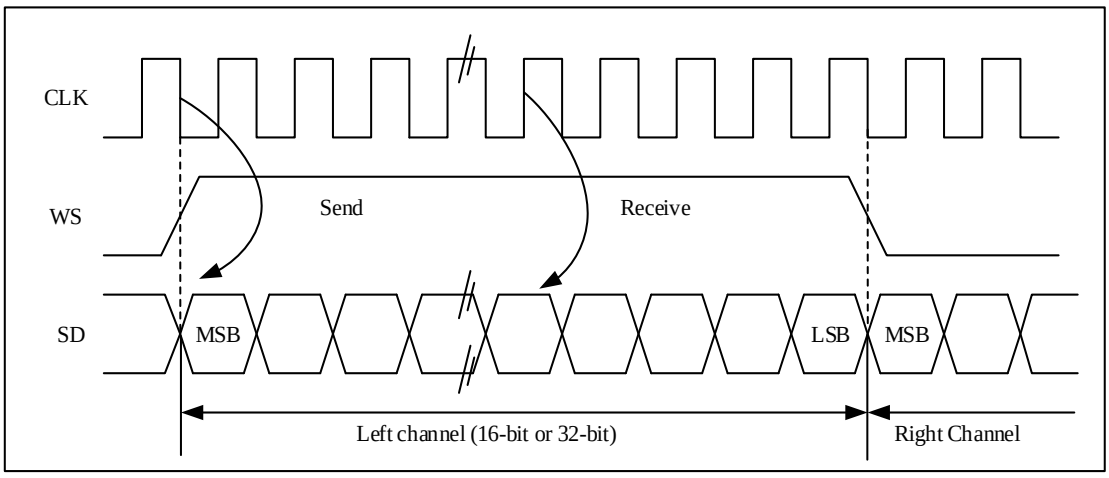


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Figure 36-25 MSB Aligns 24-Bit Data, CLKPOL = 0

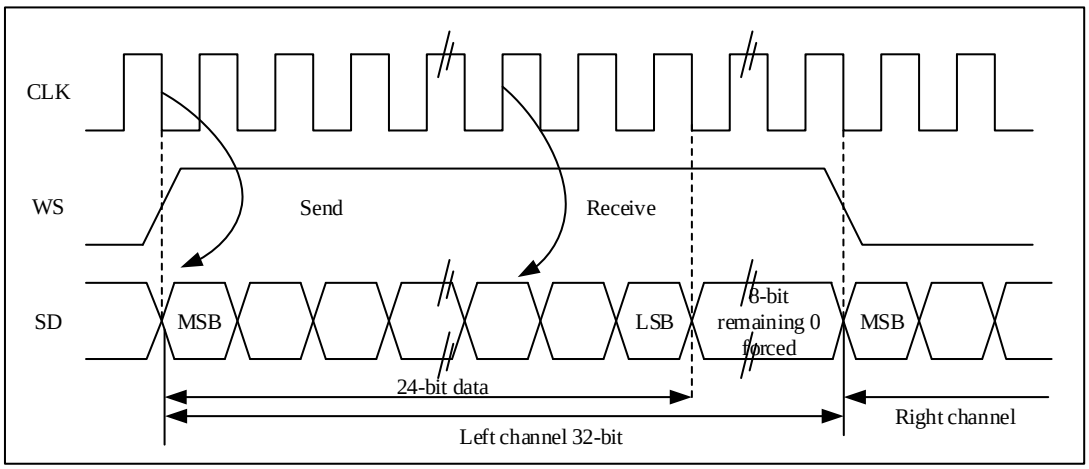
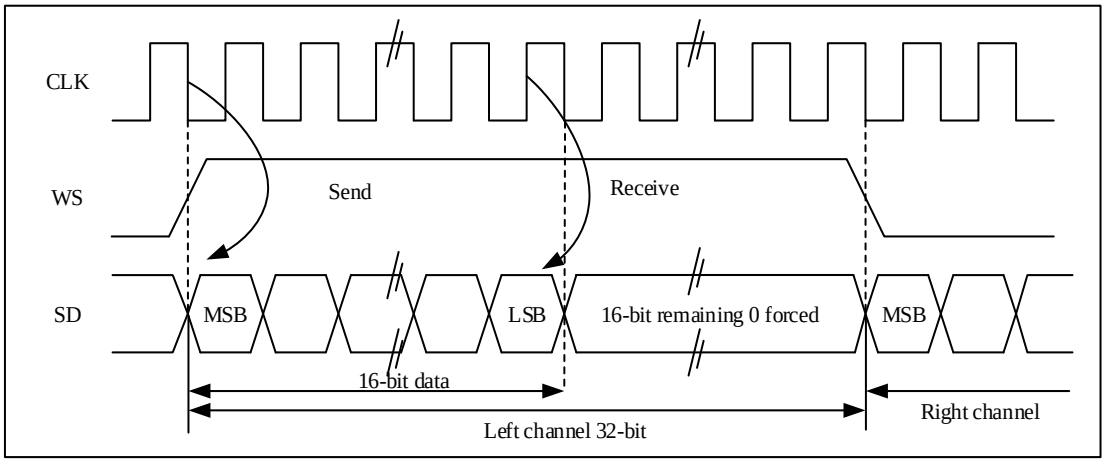


Figure 36-26 MSB-Aligned 16-Bit Data Is Extended to 32-Bit Packet Frame, CLKPOL = 0



36.4.2.3 LSB alignment standard

In 16-bit or 32-bit full-precision frame format, LSB alignment standard is the same as MSB alignment standard.

Figure 36-27 LSB Alignment 16-Bit or 32-Bit Full Precision, CLKPOL = 0

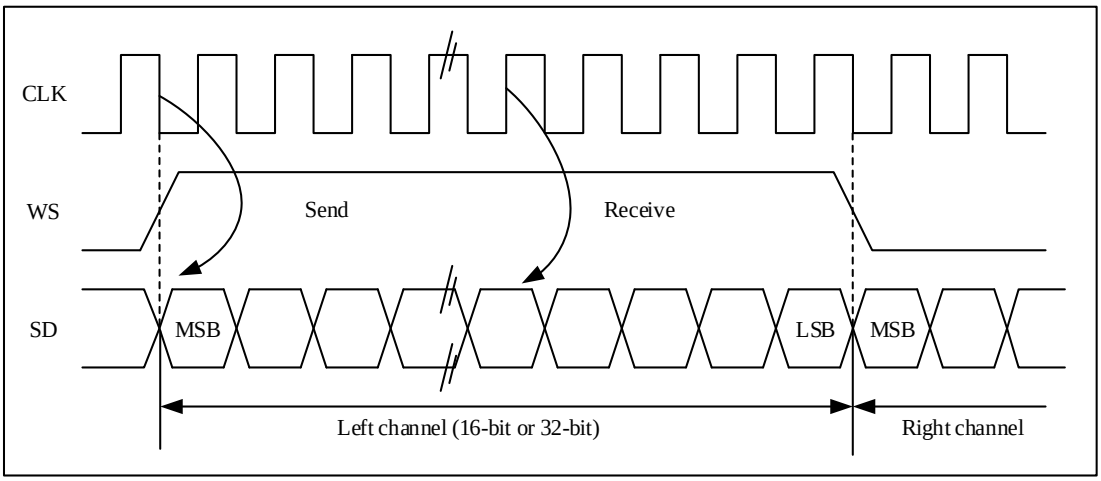


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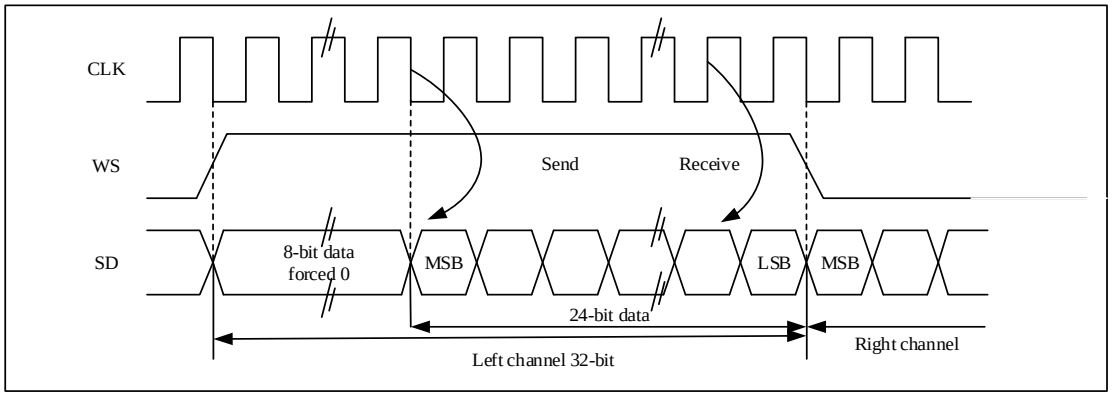
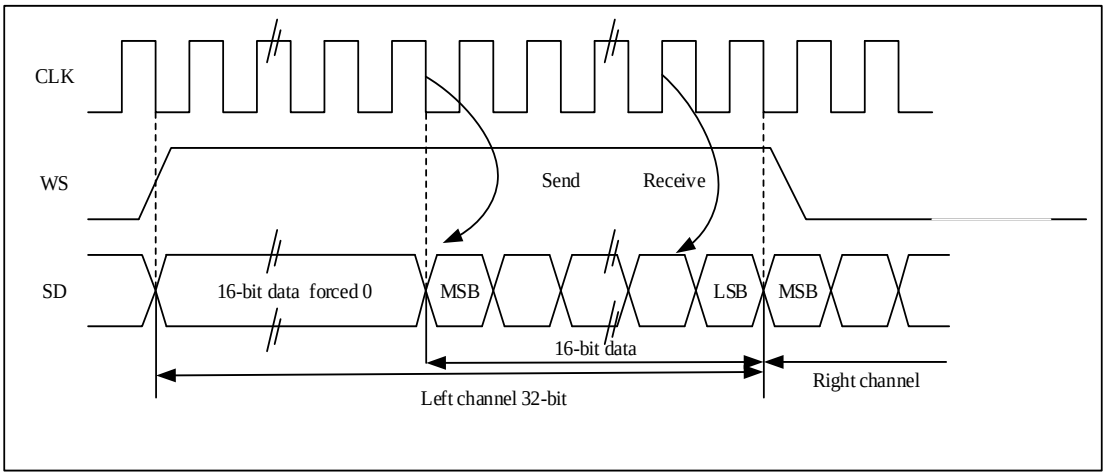
Figure 36-28 LSB Aligns 24-Bit Data, CLKPOL = 0



If the 24-bit data needs to be packed into the 32-bit data frame format, the CPU needs to read or write the SPI_DAT register twice during each frame of data transmission. For example, if the user sends 24-bit data 0x95AA66, the CPU will first write 0xXX95 (only the lower 8-bit data is valid, the upper 8-bit data is meaningless and can be any value) into the SPI_DAT register, and then write 0xAA66 into the SPI_DAT register. If the user receives 24-bit data 0x95AA66, the CPU will first read the SPI_DAT register to get 0x0095 (only the lower 8 bits are valid, the upper 8 bits are always 0), and then read the SPI_DAT register to get 0xAA66.

Figure 36-29 LSB Aligned 16-Bit Data Is Extended to 32-Bit Packet Frame, CLKPOL = 0



If the 16-bit data needs to be packaged into a 32-bit data frame format, the CPU only needs to read or write the SPI_DAT register once for each frame of data transmission. The upper 16 bits of extended to 32 bits data are set to 0x0000 by hardware, if the user sends or receives 16-bit data 0x89C1 (extended to 32-bit data is 0x000089C1). In the process of sending data, the upper 16-bit halfword (0x0000) needs to be written to the SPI_DAT register first; once the valid data starts to be send, the next TE (SPI_STS.TE) event will be generated. In the process of receiving data, once the device receives valid data, the RNE (SPI_STS.RNE) event will be generated. In this way, there is more time between 2 reads and writes, which can prevent underflow or overflow from happening.

36.4.2.4 PCM standard

In the PCM standard, there are two frame structures, short frame and long frame. The user can select the frame structure by setting the SPI_I2SCFG.PCMFSYNC bits. The WS signal indicates frame synchronization information.

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The WS signal for synchronizing long frames is 13 bits effective; the WS signal length for synchronizing short frames is 1 bit.

The standard data receiving and transmitting processing mode is the same as I²S Philips standard.

Figure 36-30 PCM Standard Waveform (16 Bits)

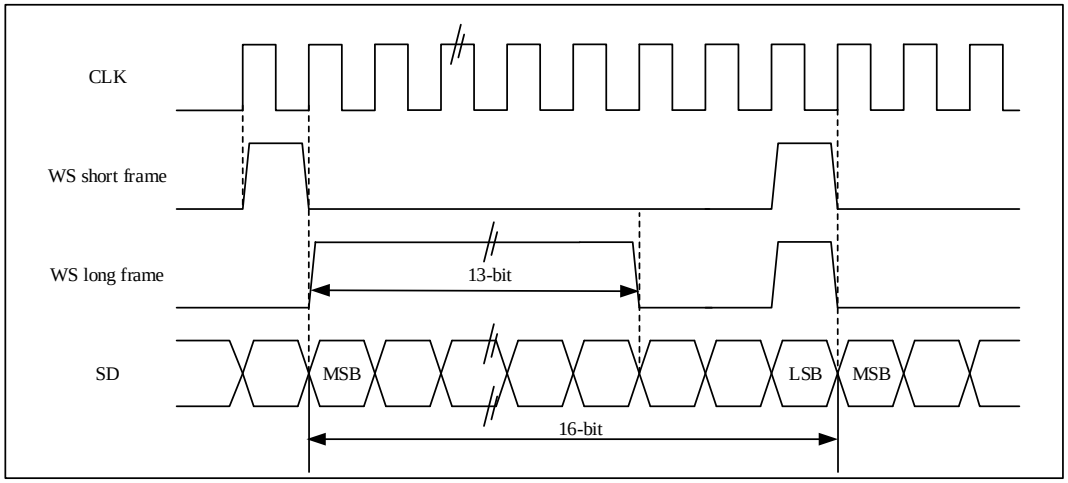
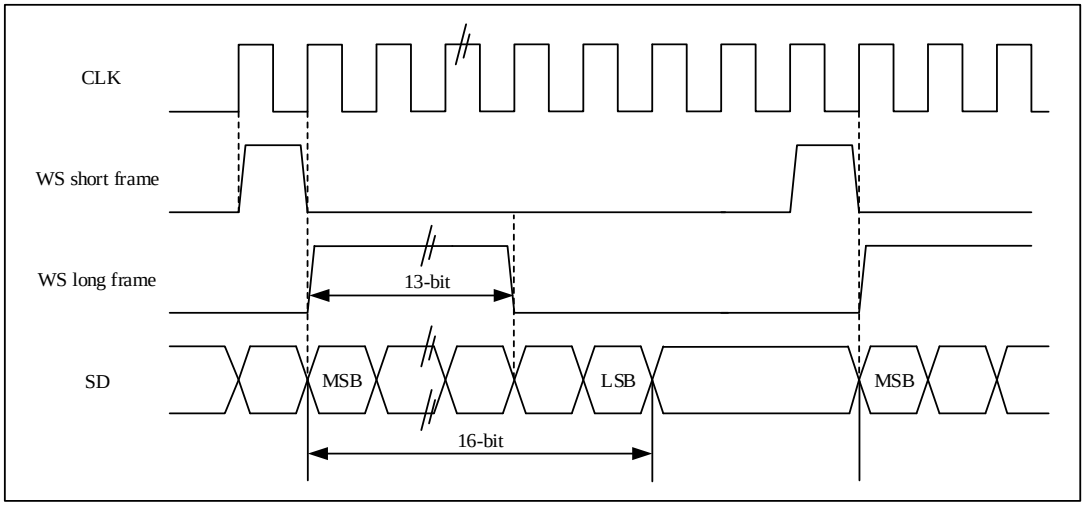


Figure 36-31 PCM Standard Waveform (16-Bit Extended to 32-Bit Packet Frame)



36.4.3 Clock Generator

In the master mode, the linear divider needs to be set correctly in order to obtain the desired audio frequency.

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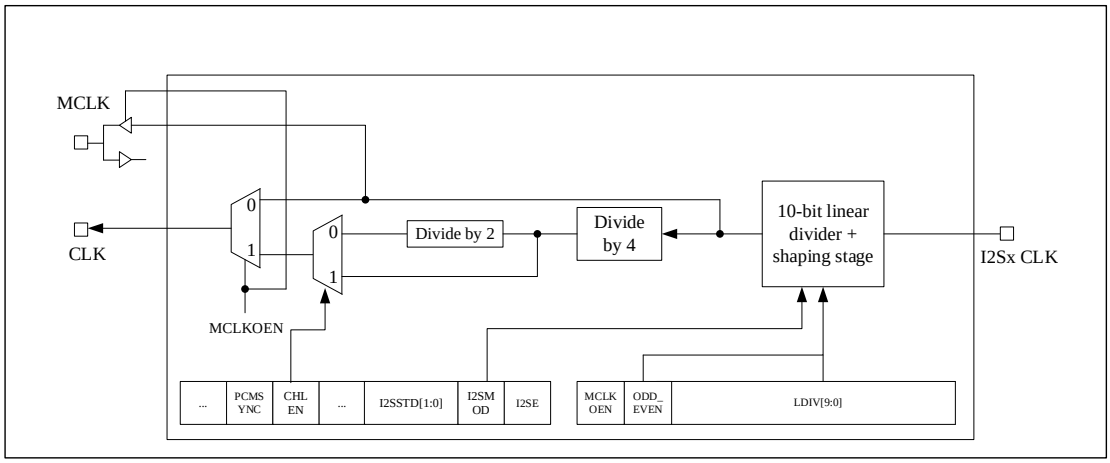
Figure 36-32 I2S Clock Generator Structure



Note: The clock source for I2SxCLK can be an independent s_i2s(n)_ker_gated_clk(130MHz), s_i2s(n)_gated_pclk(150MHz), or an external clock input.

The bit rate of I2S determines the data flow on the I2S data line and the frequency of the I2S clock signal.

I2S bit rate = number of bits per channel × number of channels × audio sampling frequency

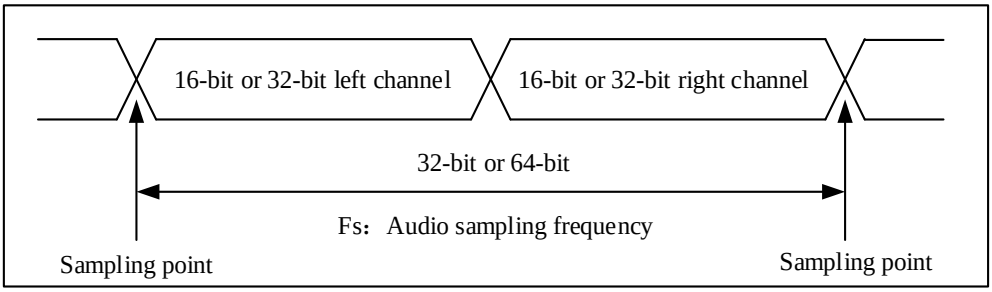
For a signal with left and right channels and 16-bit audio, the I2S bit rate is calculated as:

I2S bit rate = 16 × 2 × FS

If the packet length is 32 bits, there are:

I2S bit rate = 32 × 2 × FS

Figure 36-33 Audio Sampling Frequency Definition



The sampling signal frequency of the audio can be set by setting the SPI_I2SPREDIV.ODD_EVEN bit and the SPI_I2SPREDIV.LDIV[7:0] bits. Audio can be sampled at 96kHz, 48kHz, 44.1kHz, 32kHz, 22.05kHz, 16kHz, 11.025kHz, or 8kHz (or any value within this range). Set the linear divider according to the following formula:

When MCLKOEN = 1 and CHBITS= 0, $F_S = I^2Sx\ \ CLK/[(16 \times 2) \times ((2 \times LDIV) + ODD_EVEN) \times 8]$

When MCLKOEN = 1 and CHBITS = 1, $F_S = I^2Sx\ \ CLK/[(32 \times 2) \times ((2 \times LDIV) + ODD_EVEN) \times 4]$

When MCLKOEN = 0 and CHBITS = 0, $F_S = I^2Sx\ \ CLK/[(16 \times 2) \times ((2 \times LDIV) + ODD_EVEN)]$

When MCLKOEN = 0 and CHBITS = 1, $F_S = I^2Sx\ \ CLK/[(32 \times 2) \times ((2 \times LDIV) + ODD_EVEN)]$

The exact audio frequency can be obtained by referring to the clock configuration in the table below.

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Table 36-2 Use The Standard 8mhz HSE Clock to Get Accurate Audio Frequency

SYSCLK (MHz)	I²S_LDIV		I²S_ODDEVEN		MCLK	Target F_S(Hz)	Real FS (Hz)		Error	
	16 bits	32 bits	16 bits	32 bits			16 bits	32 bits	16 bits	32 bits
240	19	10	1	0	without	192000	192307.7	187500	0.16%	2.34%
240	39	19	0	1	without	96000	96153.85	96153.85	0.16%	0.16%
240	78	39	0	0	without	48000	48076.92	48076.92	0.16%	0.16%
240	85	42	0	1	without	44100	44117.65	44117.65	0.04%	0.04%
240	117	58	0	1	without	32000	32051.28	32051.28	0.16%	0.16%
240	170	85	0	0	without	22050	22058.82	22058.82	0.04%	0.04%
240	234	117	1	0	without	16000	15991.47	16025.64	0.05%	0.16%
240	340	170	0	0	without	11025	11029.41	11029.41	0.04%	0.04%
240	469	234	0	1	yes	8000	7995.736	7995.736	0.05%	0.05%
240	2	2	1	1	yes	192000	187500	187500	2.34%	2.34%
240	5	5	0	0	yes	96000	93750	93750	2.34%	2.34%
240	10	10	0	0	yes	48000	46875	46875	2.34%	2.34%
240	10	10	1	1	yes	44100	44642.86	44642.86	1.23%	1.23%
240	14	14	1	1	yes	32000	32327.59	32327.59	1.02%	1.02%
240	21	21	1	1	yes	22050	21802.33	21802.33	1.12%	1.12%
240	29	29	1	1	yes	16000	15889.83	15889.83	0.69%	0.69%
240	42	42	1	1	yes	11025	11029.41	11029.41	0.04%	0.04%
240	58	58	1	1	yes	8000	8012.821	8012.821	0.16%	0.16%

Note: Using SHRPLL as the clock source can achieve higher precision.

36.4.4 I²S Transmission And Reception Sequence

There are several configuration modes corresponding to master full-duplex mode:

- I2S configured as master transmit mode (I2SCFG=10), I2S_EXT configured as slave receive mode (I2SCFG=01)
- I2S configured as master receive mode (I2SCFG=10), I2S_EXT configured as slave transmit mode (I2SCFG=01)

Setting I2S to operate in master mode, the serial clock is output by the CK pin, and the word select signal is generated by the WS pin. The output of the master clock (MCK) can be selected or deselected by setting the SPI_I2SPR.MCLKOEN register bit.

I²S initialization sequences:

1) Set the SPI_I2SPR.LDIV[9:0] and SPI_I2SPR.ODDEVEN to define the serial clock baud rate that matches the audio sampling frequency.

2) The user can set the CLKPOL bit to define the polarity of the communication clock when idle.If the user needs the master device to provide the main clock MCLK to the external DAC/ADC audio device, set the SPI_I2SPR.MCLKOEN = 1.

3) Set the SPI_I2SCFGR.I2SMOD bit to '1' to enable the I2S function, set the SPI_I2SCFGR.I2SSTD[1:0] and SPI_I2SCFGR.PCMSYNC bits to select the I2S standard to be used, set the SPI_I2SCFGR.CHLEN to choose

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the data bit length for each channel. Also, set the SPI_I2SCFGR.I2SCFG[1:0] to select the I2S master mode and direction (transmit or receive).

4) If needed, the desired interrupt and DMA functions can be enabled by setting the SPI_CTRL2 register.

5) Set the SPI_I2SCFGR.I2SE register bit to '1'.

6) The WS and CK pins need to be configured as output mode. If the SPI_I2SPR.MCLKOEN bit is set to '1', the MCK pin also needs to be configured as output mode.

36.4.5 I2S Master Mode

36.4.5.1 Transmission Process in Master Mode

When writing one half-word (16 bits) of data to the transmit buffer, the transmission process begins.

Assuming the first data written to the transmit buffer corresponds to the left channel data. When the data is moved from the transmit buffer to the shift register, the TE flag is set to '1'. At this point, the corresponding right channel data needs to be written to the transmit buffer. The CHSIDE flag indicates which channel the current data to be transmitted corresponds to. The value of the CHSIDE flag is updated when TE is '1', so it is meaningful when TE is '1'. A complete data frame is considered complete only after both left and right channel data have been transmitted. It is not permissible to transmit only part of a data frame, such as data from only the left channel.

As the first bit of data is sent out, the half-word data is transmitted in parallel to the 16-bit shift register, and the subsequent bits are then sent out from the I2S_SD/I2S_EXT_SD pins in order, starting with the most significant bit. Each time data is transferred from the transmit buffer to the shift register, the TE flag is set to '1', and if the SPI_CTRL2.TEINTEN bit is set to '1', an interrupt is generated.

To ensure continuous audio data transmission, it is recommended to write the next data to be transmitted to the SPI_DAT register before the current transmission is completed. It is recommended to wait for the SPI_STS.TE=1 and SPI_STS.BUSY=0 flags before disabling the I2S function, and then clear the SPI_I2S_CFGR.I2SE bit to '0'.

36.4.5.2 Reception Process in Master Mode

Select the master receive mode by configuring SPI_I2S_CFGR[1:0].

Regardless of the data and channel length, audio data is always received in packets of 16 bits. When the data is transferred from the shift register to the receive buffer, the RNE flag bit is set to 1, at this time, the data is ready and can be read from the SPI_DAT register. If the SPI_CTRL2.RNEINTEN bit is set to 1, an interrupt will be generated. According to the configured data and channel length, the received audio data will need to be transferred to the receive buffer once or twice.

Reading the SPI_DAT register to clear the RNE flag. The CHSIDE is updated after each reception. Its value depends on the WS signal generated by the I2S unit. If the previously received data is not read, new data is received again, an overflow occurs, and the SPI_STS.OVER flag is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated to indicate that an error has occurred.

To disable the I2S module, special operations need to be performed to ensure that the I2S module can complete the transmission cycle properly without starting new data transfers. The operation process is related to data configuration, channel length, and the audio protocol:

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Email: sales@nsing.com.sg

- Data length is 16 bits, channel length is 32 bits (DATLEN=00, CHLEN=1), LSB alignment standard (I2SSTD=10).

  1) Wait for the penultimate RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2) Software delay, waiting for 17 I2S clock cycles.
  3) Disable I2S (SPI_I2S_CFGR.I2SEN = 0).

- Data length is 16 bits, the channel length is 32 bits (DATLEN=00, CHLEN=1), the MSB alignment standard (I2SSTD=01), I2S Philips standard (I2SSTD=00) or PCM standard (I2SSTD= = 11)

  1) Wait for the last RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2) Software delay, waiting for 1 I2S clock cycle.
  3) Turn off I2S (SPI_I2S_CFGR.I2SEN = 0).

- For all other combinations of DATLEN and CHLEN, and any audio mode selected by I2SSTD, the I2S can be disabled in the following steps:

  1) Wait for the penultimate RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2) Software delay, waiting for 1 I2S clock cycle.
  3) Disable I2S (SPI_I2S_CFGR.I2SEN = 0).

36.4.6 I2S Slave Mode(Full Duplex)

There are several configuration modes corresponding to slave full-duplex mode:

1) I2S configured as slave transmit mode (SPI_I2S_CFGR.I2SCFG=00), I2S_EXT configured as slave receive mode (I2S_CFGR.I2SCFG=01).
2) I2S configured as slave receive mode (SPI_I2S_CFGR I2SCFG=01), I2S_EXT configured as slave transmit mode (I2S_CFGR.I2SCFG=00).

In slave mode, I2S/I2S_EXT can be set to transmit and receive modes. The configuration process for slave mode is similar to that of master mode. In slave mode, there is no need for the I2S interface to provide a clock. The clock signal and WS signal are provided by the external master I2S device, connected to the respective pins. Therefore, the user does not need to configure the clock.

The configuration steps are as follows:

1) Set the SPI_I2SCFGR.I2SMOD bit to 1 to enable the I2S module. Select the I2S standard by configuring I2SSTD[1:0]. Choose the length of the data to betransferred by configuring DATLEN[1:0]. Configure CHLEN to select the data bit length for each channel. Configure the SPI_I2SCFGR.I2SCFG[1:0] to choose the data direction (transmit or receive) for the I2S slave mode.
2) If needed, the desired interrupt and DMA functions can be enabled by setting the SPI_CTRL2 register.
3) The SPI_I2SCFGR.I2SE bit must be set to '1'.

36.4.6.1 Transmission Process in Slave Mode

The transmitting process begins when an external master sends a clock signal, and when a WS signal requires data

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transmission. Only when the slave device is enabled and the data has been written to the I2S data register, the external master device can start communication.

For I2S MSB alignment and LSB alignment modes, the first data item written to the data register corresponds to the left channel data. When communication begins, the data is transferred from the transmit buffer to the shift register, and then the TE flag is set to '1'; at this point, the corresponding data item for the right channel should be written to the I2S data register.

The SPI_STS.CHSIDE flag indicates which channel the currently transmitted data corresponds to. Compared with the master mode transmitting process, in the slave mode, CHSIDE depends on the WS signal of the external master I2S device (WS signal is 1 means the left channel). This means that the I2S slave needs to be ready with the first data to be sent before receiving the clock signal generated by the master.

As the first bit of data is transmitted, the half-word data is transmitted in parallel through the I2S internal bus to the 16-bit shift register, and then the remaining bits are sent out from the I2S_SD/I2S_EXT_SD pins in order, starting with the most significant bit. Each time data is transferred from the transmit buffer to the shift register, the TE flag is set to '1', and if the SPI_CTRL2.TEINTEN bit is set to '1', an interrupt is generated.

Before writing data to the transmit buffer, ensure that the TE flag is set to '1'. To ensure continuous audio data transmission, it is recommended to write the next data to be transmitted to the SPI_DAT register before the current transmission is completed.

Before writing data to the transmit buffer, ensure that the TE flag is set to '1'. To ensure continuous audio data transmission, it is recommended to write the next data to be transmitted to the SPI_DAT register before the current transmission is completed. If the new data is not written to the SPI_DAT register before the first clock edge representing the next data transfer arrives, the underrun flag will be set to '1'. It indicates a software data transmission error. If the SPI_CTRL2.ERRINTEN bit is set to '1', an interrupt will be generated when the UNDER flag in the SPI_STS register is high. It is recommended to close the I2S at this point, and then restart sending data from the left channel.

36.4.6.2 Reception Process in Slave Mode

Select the slave receive mode by configuring I2SCFG[1:0].

Regardless of the data and channel length, audio data is always received in packets of 16 bits. When the data is transferred from the shift register to the receive buffer, the RNE flag bit is set to 1, at this time, the data is ready and can be read from the SPI_DAT register. If the SPI_CTRL2.RNEINTEN bit is set to 1, an interrupt will be generated. According to the configured data and channel length, the received audio data will need to be transferred to the receive buffer once or twice.

The CHSIDE is updated after each reception. Its value depends on the WS signal generated by the master device. Reading the SPI_DAT register to clear the RNE flag. If the previously received data is not read, new data is received again, an overflow occurs, and the SPI_STS.OVER flag is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated to indicate that an error has occurred. When disabling the I2S function, the SPI_I2S_CFGR.I2SE bit should be cleared to 0 at the last RNE=1.

36.4.7 Status Flag

There are the following 4 flag bits in the SPI_STS register for monitoring the status of the I2S bus.

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BUSY flag (BUSY)

The SPI_STS.BUSY flag is set and cleared by hardware (writing to this bit has no effect), indicating the status of the I2S communication. When this bit is '1', it indicates that I2S communication is in progress, with one exception: in master receive mode (I2SCFG=11), the SPI_STS.BUSY flag is always low during reception.

Before disabling the I2S module in software, you can use the SPI_STS.BUSY flag to check if the transmission has ended. This can help avoid disrupting the final transmission.

When the transmission starts, the SPI_STS.BUSY flag is set to '1', unless the I2S module is in master receive mode.

The flag is cleared under the following conditions:

- When the transmission ends (except in master transmit mode, where communication is continuous).
- When the I2S module is disabled.

When communication is continuous:

- In master transmit mode, the SPI_STS.BUSY flag remains high throughout the entire transmission.
- In slave mode, the SPI_STS.BUSY flag transitions low for one I2S clock cycle between each data item transfer.

TX buffer empty flag (TE)

When the send buffer is empty, this flag is set to 1, indicating that new data can be written into the SPI_DAT register. When the send buffer is not empty, this flag is cleared to 0.

RX buffer not empty flag (RNE)

When the receive buffer is not empty, this flag is set to 1, indicating that valid data has been received into the receive buffer. When reading the SPI_DAT register, this flag is set to 0.

Channel Side flag (CHSIDE)

In transmit mode, the flag is updated when the TE flag (SPI_STS.TE) is set, indicating the channel where the data sent on the I2S_SD/I2S_EXT_SD pin is located. If an underflow error occurs in transmit mode, the value of this flag is invalid, and the I2S needs to be disabled and enabled before communication can resume. In receive mode, the flag is updated when the RNE flag (SPI_STS.RNE) is set. If an overflow (SPI_STS.OVER) error occurs in receive mode, this flag is invalid, and the I2S needs to be disabled and enabled before communication can resume Under the PCM standard, this flag has no meaning.

36.4.8 Error Flag

The SPI_STS register has 2 error flag bits.

Overflow flag (OVER)

If new data is received before the previous data is read, causing an overflow, the flag is set to '1'. If the SPI_CTRL2.ERRINTEN bit is set to '1', an interrupt is generated to indicate an error has occurred. In this case, the contents of the receive buffer are not updated with the new data from the transmitting device. Reading the SPI_DAT register will return the last correctly received data. All other 16-bit data sent by the transmitting device after the overflow occurred will be lost. Reading the SPI_DAT register first and then the SPI_STS register can clear this flag.

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Underflow flag (UDER)

In slave send mode, when the first clock edge of sending data arrives, if the transmit buffer is still empty, the UNDER flag (SPI_STS.UNDER) is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to '1', an interrupt will be generated. This flag can be cleared by reading the SPI_STS register.

36.4.9 I²S Interrupt

The following table lists all I²S interrupts.

Table 36-3 I2S Interrupt Request

Interrupt Event	Event Flag Bit	Enable Control Bit
Send buffer empty flag	TE	TEINTEN
Receive buffer non empty flag	RNE	RNEINTEN
Underflow flag bit	UNDER	ERRINTEN

36.4.10 DMA Function

To achieve the maximum communication frequency, it is necessary to promptly write data to the I2S transmit buffer and also read the data from the receive buffer in a timely manner to prevent overflow. To facilitate high-speed data transfer, I2S has implemented a simple request/response DMA mechanism.

When the corresponding enable bit on the SPI_CTRL2 register is set, the I2S module can generate DMA transfer requests. Both the transmit buffer and receive buffer also have their own DMA requests.

- During transmission, a DMA request is generated each time TE is set to '1', and the DMA controller writes data to the SPI_DAT register, clearing the TE flag in the process.
- During reception, a DMA request is generated each time RNE is set to '1', and the DMA controller reads data from the SPI_DAT register, clearing the RNE flag in the process.

When only using I2S/I2S_EXT to transmit data, only the transmit DMA channel of I2S/I2S_EXT needs to be enabled. In this case, since no received data is being read, OVER is set to '1'. When only using I2S/I2S_EXT to receive data, only the receive DMA channel of I2S/I2S_EXT needs to be enabled.

36.5 SPI and I2S Register

36.5.1 SPI Control Register 1 (SPI_CTRL1) (Not Used in I2S Mode)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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BIDIRMODE	BIDIROEN	RONLY	SSMEN	SSEL	SSOEN	CRCNEXT	DATFF	LSBFF	MSEL	CLKPHA	CLKPOL	Reserved	BR[2:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	BIDIRMODE	Bidirectional data mode enable 0: Select the "two-wire one-way" mode. 1: Select the "one-wire bidirectional " mode. *Note: Not used in I²S mode.*
14	BIDIROEN	Output enable in bidirectional mode 0: Output disable (receive-only mode). 1: Output enabled (send-only mode). In master mode, the "one-wire" data line is the MOSI pin, and in slave mode, the "one-wire" data line is the MISO pin. *Note: Not used in I²S mode.*
13	RONLY	Only receive mode This bit, together with the SPI_CTRL1.BIDIRMODE bit, determines the transfer direction in two-wire one-way mode. In the application scenario of multiple slave devices, this bit is only set to 1 by the unaccessed slave device, and only the accessed slave device can output, so as to avoid data line conflicts. 0: Full duplex (sending mode and receiving mode). 1: Disable output (receive-only mode). *Note: Not used in I²S mode.*
12	SSMEN	Software slave device management When the SPI_CTRL1.SSMEN bit is set to 1, the NSS pin level is determined by the value of the SPI_CTRL1.SSEL bit. 0: Disable software slave device management. 1: Enable software slave device management. *Note: Not used in I²S mode.*
11	SSEL	Internal slave device selection This bit only has meaning when the SPI_CTRL1.SSMEN bit is set. It determines the NSS level, and I/O operations on the NSS pin have no effect. *Note: Not used in I²S mode.*
10	SSOEN	NSS output enable 0: Disable NSS output in master mode, the device can work in multi-master mode. 1: When the device is enabled, enable NSS output in the master mode, the device cannot work in the multi-master device mode. *Note: Not used in I²S mode.*
9	CRCNEXT	Send CRC next 0: The next sent value comes from the send buffer. 1: The next send value comes from the CRC register. *Note: This bit should be set immediately after the last data is written in SPI_DAT*

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Bit field	Name	Description
		register during transmission. This bit should be set immediately after receiving the second-to-last data during reception. *Note: Not used in I²S mode.*
8	DATFF	Data frame format 0: 8-bit data frame format is used for sending/receiving. 1: 16-bit data frame format is used for sending/receiving. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* *Note: Not used in I²S mode.*
7	LSBFF	Frame format 0: Send MSB first. 1: Send LSB first. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
6	MSEL	Master device selection 0: Configure as the slave device. 1: Configure as the master device. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
5	CLKPHA	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
4	CLKPOL	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
3	Reserved	Reserved, the reset value must be maintained.
2:0	BR[2:0]	Baud rate control 000: fPCLK/2 001: fPCLK/4 010: fPCLK/8 011: fPCLK/16 100: fPCLK/32 101: fPCLK/64 110: fPCLK/128 111: fPCLK/256 *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*

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36.5.2 SPI Control Register 2 (SPI_CTRL2)

Address offset: 0x04

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RNEDMABYPASS	RXCPINTEN	CRCNMISEN	RXFFUINTEN	RXFHFINTEN	TXFHEINTEN	FIFOCLR	FIFOEN	SS_POL	ERRINTEN	RNEINTEN	TEINTEN	CRCEN	TDMAEN	RDMAEN	SPIEN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	RNEDMABYPASS	rxne for dma is bypass.
14	RXCPINTEN	In receive-only mode, enable the transfer complete interrupt. 0：enable the transfer complete interrupt 1：disable the transfer complete interrupt
13	CRCNMISEN	When NSS becomes invalid, whether the CRC stop calculating immediately 0：As long as there is a clock, the CRC calculation continues. 1：CRC stop calculating immediately when NSS becomes invalid
12	RXFFUINTEN	Enable RX FIFO full interrupt. This bit is only used in FIFO mode. 0：disable RX FIFO full interrupt 1：enable RX FIFO full interrupt
11	RXFHFINTEN	Enable RX FIFO half-full interrupt. This bit is only used in FIFO mode. 0：disable RX FIFO half-full interrupt 1：enable RX FIFO half-full interrupt
10	TXFHEINTEN	Enable TX FIFO half-empty interrupt. This bit is only used in FIFO mode. 0：disable TX FIFO half-empty interrupt. 1：Enable TX FIFO half-empty interrupt.
9	FIFOCLR	FIFO clear bit This bit is only used in FIFO mode. 0：not clear FIFO 1：clear FIFO

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Bit field	Name	Description
8	FIFOEN	Enable FIFO 0：disable FIFO 1：enable FIFO
7	SS_POL	NSS polarity control 0：NSS valid level is low. 1：NSS valid level is high.
6	ERRINTEN	Error interrupt enable When an error (SPI_STS.CRCERR, SPI_STS.OVER, SPI_STS.UNDER, SPI_STS.MODERR) is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
5	RNEINTEN	Receive buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when RNE flag (SPI_STS.RNE) is set to ‘1’.
4	TEINTEN	Transmit buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when TE flag (SPI_STS.TE) is set to '1'.
3	CRCEN	Hardware CRC check enable 0: Disable CRC calculation. 1: Enable CRC calculation. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* This bit can only be used in full duplex mode. *Note: Not used in I^2S mode.*
2	TDMAEN	Transmit buffer DMA enable When this bit is set, a DMA request is issued as soon as the TE flag (SPI_STS.TE) is set 0: Disable send buffer DMA 1: Enable send buffer DMA
1	RDMAEN	Receive buffer DMA enable When this bit is set, a DMA request is issued as soon as the RNE flag (SPI_STS.RNE) is set 0: Disable receive buffer DMA. 1: Enable receive buffer DMA.
0	SPIEN	SPI enable 0: Disable SPI device. 1: Enable the SPI device. *Note: Not used in I^2S mode.*

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Bit field	Name	Description
		Note: When turning off the SPI device, please follow paragraph 36.3.6 Section's procedure operation.

36.5.3 SPI Status Register (SPI_STS)

Address offset: 0x08

Reset value: 0x0101

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RXTSCP	RXFIFFU	TXFIFFU	RXFIFHF	TXFIFHE	CHSIDE	UNDER	OVER	MODERR	CRCERR	BUSY	RNE	TE
			rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained.
12	RXTSCP	In receive-only mode, the transfer completion status. 0：The current transfer is not yet completed. 1：The current transfer has been completed.
11	RXFIFFU	RX FIFO full flag This bit is only used in FIFO mode. 0：RX FIFO is not full. 1：RX FIFO is full.
10	TXFIFFU	TX FIFO full flag This bit is only used in FIFO mode. 0：TX FIFO is not full 1：TX FIFO is full
9	RXFIFHF	RX FIFO half-full flag This bit is only used in FIFO mode. 0：RX FIFO is not half-full 1：RX FIFO is half-full
8	TXFIFHE	TX FIFO half-empty flag This bit is only used in FIFO mode. 0：TX FIFO is not half-empty 1：TX FIFO is half-empty

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Bit field	Name	Description
7	CHSIDE	Channel 0: The left channel needs to be sent or received. 1: The right channel needs to be sent or received. *Note: not used in SPI mode. No meaning in PCM mode.*
6	UNDER	Underflow flag 0: No underflow occurred. 1: Underflow occurred. *Note: This bit is set by hardware and cleared according to the sequence of software operations. In non-FIFO mode of SPI, this flag is not used. In FIFO mode of SPI, attempting to read the RX FIFO when it is empty will set this flag.* *In I2S slave transmit mode, if the first clock edge of data transfer arrives and new data has not been written to the SPI_DR register, this flag will be set to '1'.*
5	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. This bit is set by hardware, and reading the data register first and then reading the status register will clear it. Note: In SPI non-FIFO mode/I2S mode, this flag being set to 1 indicates an overflow in the receive data register. In SPI FIFO mode, attempting to write data to the TX FIFO when it is already full will set this flag.
4	MODERR	Mode error 0: No mode error. 1: A mode error occurred. *Note: This bit is set by hardware and cleared according to the sequence of software operations.* For detailed information on software sequences, refer to the error flag section. *It is not used in I2S mode.*
3	CRCERR	CRC error flag 0: The received CRC value matches the value the SPI_CRCRDAT register value. 1: The received CRC value does not match the SPI_CRCRDAT register value. *Note: this bit is set by hardware and cleared by software by writing 0.* *Note: Not used in I^2S mode.*
2	BUSY	Busy flag 0: SPI is not busy. 1: SPI is busy communicating or the send buffer is not empty.

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Bit field	Name	Description
		This bit is set or reset by hardware.
1	RNE	Receive buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.
0	TE	The send buffer is empty 0: The send buffer is not empty. 1: The send buffer is empty.

36.5.4 SPI Data Register (SPI_DAT)

Address offset: 0x0C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
rw															

Bit field	Name	Description
15:0	DAT[15:0]	Data register Data to be sent or received In FIFO mode, this register is the transmit data register. In non-FIFO mode, this register is the transmit/receive data register. The data register corresponds to two buffers: one for write (transmit buffer); The other is for read (receive buffer). Write operation writes data to transmit buffer; The read operation will return the data in the receive buffer. Note on SPI mode: According to the selection of the data frame format by the SPI_CTRL1.DATFF bit, the data transmitting and receiving can be 8-bit or 16-bit. To ensure correct operation, the data frame format needs to be determined before enabling the SPI. For 8-bit data, the buffer is 8-bit, and only SPI_DAT[7:0] is used when transmitting and receiving. When receiving, SPI_DAT[15:8] is forced to 0. For 16-bit data, the buffer is 16-bit, and the entire data register is used when transmitting and receiving, that is, SPI_DAT[15:0].

36.5.5 SPI Transmit CRC Register (SPI_CRCTDAT)

Address offset：0x10

Reset value：0x0000

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCTDAT[15:0]															
r															

Bit field	Name	Description
15:0	CRCTDAT[15:0]	Transmit CRC register When CRC calculation is enabled, CRCTDAT[15:0] contains the CRC value calculated by the bytes sent subsequently. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.* *Note: not used in I^2s mode.*

36.5.6 SPI Receive CRC Register (SPI_CRCRDAT)

Address offset: 0x14

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCRDAT[15:0]															
ro															

Bit field	Name	Description
15:0	CRCRDAT[15:0]	Receive CRC register When CRC calculation is enabled, CRCRDAT[15:0] will contain the calculated CRC value of subsequent received bytes. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.* *Note: not used in I^2s mode.*

36.5.7 SPI CRC Polynomial Register (SPI_CRCPOLY)

Address offset：0x18

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Reset value：0x0007

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCPOLY[15:0]															
rw															

Bit field	Name	Description
15:0	CRCPOLY[15:0]	CRC polynomial register This register contains the polynomial used for the CRC calculation. The reset value is 0x0007, other values can be set according to the application. *Note: not used in I^2s mode.*

36.5.8 SPI_I2S Configuration Register (SPI_I2S_CFGR)

Address offset：0x1C

Reset value：0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PCMBYPASS	CLKPOL	PCMSYNC	CHLEN	DATLEN[1:0]		I2SCFG[1:0]		I2SSTD[1:0]		I2SMOD	I2SE
				rw	rw	rw	rw	rw		rw		rw		rw	rw

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	PCMBYPASS	pcm long for 13bit is bypass 1:no bypass 0:bypass
10	CLKPOL	Static clock polarity 0: I2S clock static state is low level. 1: I2S clock static state is high level. *Note: For correct operation, this bit can only be set when I^2S is disabledf.* *Note: not used in SPI mode.*
9	PCMSYNC	PCM frame synchronization 0: Short frame synchronization 1: Long frame synchronization. *Note: This bit is only valid when I2SSTD = 11 (used by the PCM standard)。* *Note: not used in SPI mode.*
8	CHLEN	Channel length (number of data bits per audio channel) 0: 16 bits wide;

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Bit field	Name	Description
		1: 32 bits wide. *Note: This bit is only valid when* DATLEN = 00，otherwise the channel length is fixed to 32 bits by hardware. *Note: For correct operation, this bit can only be set when I²S is disabled.* *Note: not used in SPI mode.*
7:6	DATLEN[1:0]	Length of data to be transmitted 00: 16-bit data length. 01: 24-bit data length; 10: 32-bit data length; 11: Not allowed. *Note: For correct operation, this bit can only be set when I²S is disabled.*
5:4	I2SCFG[1:0]	I²S mode setting 00: Configured as slave transmit mode. 01: Configured as slave receive mode. 10: Configured as Master transmit mode. 11: Configured as Master receive mode. *Note: This bit can only be set when I²S is turned off.* *Note: not used in SPI mode.*
3:2	I2SSTD[1:0]	Selection of I²S standard 00: I²S Philips standard. 01: High byte alignment standard (left alignment). 10: Low byte alignment standard (right alignment). 11: PCM standard. *Note: For correct operation, this bit can only be set when I²S is disabled.* *Not used in SPI mode.*
1	I2SMOD	I²S mode selection 0: Select SPI mode. 1: Select I²S mode. *Note: this bit can only be set when SPI or* I²S *is disabled.*
0	I2SEN	I²S enable 0: Disable I²S. 1: Enable I²S. *Note: not used in SPI mode.*

36.5.9 SPI_I2S Prescaler Register (SPI_I2S_PREDIV)

Address offset：0x20

Reset value：0x0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				MCLKOEN	ODDEVEN	LDIV[9:0]									

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rw rw rw

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	MCLKOEN	Master clock output enable 0: Disable master clock output. 1: Enable master clock output. *Note: For correct operation, this bit can only be set when I²S is disabled* *Note: not used in SPI mode.*
10	ODDEVEN	Coefficient prescaler 0: actual frequency division coefficient = LDIV ×2. 1: actual frequency division coefficient = (LDIV × 2) + 1. See Section 36.4.3 for details. *Note: For correct operation, this bit can only be set when I²S is disabled. Use this bit only in I²S master mode.* *Not used in SPI mode.*
9:0	LDIV[9:0]	I²S linear prescaler Setting LDIV [9:0] = 0 or LDIV [9:0] = 1 is prohibited. *Note: For correct operation, this bit can only be set when I²S is disabled. Use this bit only in I²S master mode.* *Not used in SPI mode.*

36.5.10 SPI Receive FIFO (SPI_RX_FIFO)

Address offset：0x24

Reset value：0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFIFDAT[15:0]															
rw															

Bit field	Name	Description
15:0	RXFIFDAT[15:0]	In FIFO mode, it is the receive FIFO (read receive FIFO data by accessing this register). In non-FIFO mode, this register is not used.

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36.5.11 SPI FIFO Configuration register (SPI_FIFO_NUM)

Address offset：0x28

Reset value：0x0044

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									RXFBSNUM[2:0]			Reserved	TXFBSNUM[2:0]		
									rw				rw		

Bit field	Name	Description
15:7	Reserved	Reserved, the reset value must be maintained.
6:4	RXFBSNUM[2:0]	In FIFO mode, configuration of the RX FIFO half-full threshold When the number of valid data entries in the RX FIFO reaches this configured value, SPI_STS.RXFIFHF will be set to 1. When conducting DMA communication, the number of data items per burst should match the value in this register. This register is not used in non-FIFFO mode.
3	Reserved	Reserved, the reset value must be maintained.
2:0	TXFBSNUM[2:0]	In FIFO mode, configuration of the TX FIFO half-empty threshold When the number of valid data entries in the TX FIFO reaches this configured value, SPI_STS.TXFIFHE will be set to 1. When conducting DMA communication, the number of data items per burst should match the value in this register. This register is not used in non-FIFFO mode.

36.5.12 SPI FIFO Count Register (SPI_FIFO_CNT)

Address offset：0x30

Reset value：0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RXFIFCNT[3:0]				TXFIFCNT[3:0]			
								r				r			

Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:4	RXFIFCNT[3:0]	In FIFO mode, the number of valid data entries in the RX FIFO

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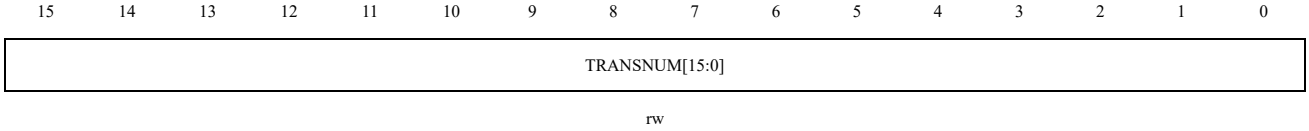
Bit field	Name	Description
3:0	TXFIFCNT[3:0]	In FIFO mode, the number of valid data entries in the TX FIFO

36.5.13 SPI Transfer Number Configuration Register (SPI_TRANS_NUM)

Address offset：0x34

Reset value：0x0000

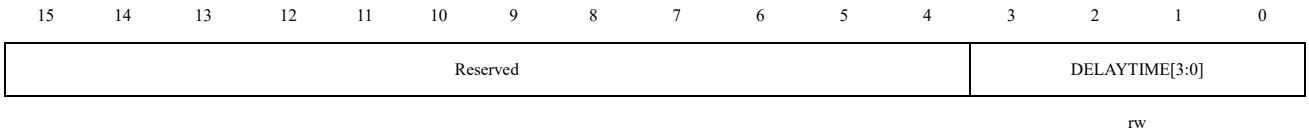


Bit field	Name	Description
15:0	TRANSNUM[15:0]	When in FIFO mode and CRC function is enabled, this register is configured for the total number of data to be transferred. In CPU mode, if the receive-only mode is enabled, by configuring this register, the user does not need to set the CRCNEXT bit by software, as this operation is performed by hardware.

36.5.14 SPI RX Sample Delay Register (SPI_CR3)

Address offset：0x38

Reset value：0x0000



Bit field	Name	Description
15:4	Reserved	Reserved, the reset value must be maintained.
3:0	DELAYTIME[3:0]	Configuration of SPI master sampling delay time, after setting the value of this register, the received data will be sampled using the delayed clock. 4'b0000: bypass, no delay processing for the sampling clock. 4'b0001: Sample the data on the MISO port after a delay of 1/2 Tapb_clk cycle. 4'b0010: Sample the data on the MISO port after a delay of 1 Tapb_clk cycle. 4'b0011: Sample the data on the MISO port after a delay of 3/2 Tapb_clk cycle. 4'b0100: Sample the data on the MISO port after a delay of 2 Tapb_clk cycle. 4'b0101: Sample the data on the MISO port after a delay of 5/2 Tapb_clk cycle.

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Bit field	Name	Description
		4'b0110: Sample the data on the MISO port after a delay of 3 Tapb_clk cycle. 4'b0111: Sample the data on the MISO port after a delay of 7/2 Tapb_clk cycle. 4'1000: Sample the data on the MISO port after a delay of 4 Tapb_clk cycle. 4'b1001: Sample the data on the MISO port after a delay of 9/2 Tapb_clk cycle. 4'b1010: Sample the data on the MISO port after a delay of 5 Tapb_clk cycle. 4'b1011: Sample the data on the MISO port after a delay of 11/2 Tapb_clk cycle. 4'b1100: Sample the data on the MISO port after a delay of 6 Tapb_clk cycle. 4'b1101: Sample the data on the MISO port after a delay of 13/2 Tapb_clk cycle. 4'b1110: Sample the data on the MISO port after a delay of 7 Tapb_clk cycle. 4'b1111: Sample the data on the MISO port after a delay of 1 Tapb_clk cycle. Note: Tapb_clk is the APB clock cycle. This register can only be configured in SPI master full-duplex and SPI master receive modes. Configuring this bit in other SPI modes is invalid; this register is not used in I2S mode.

36.5.15 I2S_EXT Control Register（I2S_CTRL2）

Address offset：0x204

Reset value：0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXNEDMABYPASS	Reserved								ERRINTEN	RNEINTEN	TEINTEN	Reserved	TDMAEN	RDMAEN	Reserved
									rw	rw	rw		rw	rw	rw

Bit field	Name	Description
15	RXNEDMABYPASS	rxne for dma is bypass
14:7	Reserved	Reserved, the reset value must be maintained.
6	ERRINTEN	Error interrupt enable When an error is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
5	RNEINTEN	Receive buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when RNE flag is set to ‘1’.
4	TEINTEN	Transmit buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when TE flag is set to '1'.
3	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
2	TDMAEN	Transmit buffer DMA enable When this bit is set, a DMA request is issued as soon as the TE flag is set 0: Disable Transmi buffer DMA. 1: Enable Transmibuffer DMA.
1	RDMAEN	Receive buffer DMA enable When this bit is set, a DMA request is issued as soon as the RNE flag is set 0: Disable receive buffer DMA. 1: Enable receive buffer DMA.
0	Reserved	Reserved, the reset value must be maintained.

36.5.16 I2S_EXT Status Register (I2S_STS)

Address offset：0x208

Reset value：0x0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CHSIDE	UNDER	OVER	Reserved		BUSY	RNE	TE
								r	r	r			r	r	r

Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7	CHSIDE	Channel 0: The left channel needs to be sent or received. 1: The right channel needs to be sent or received. *Note: not used in SPI mode. No meaning in PCM mode.*
6	UNDER	Underflow flag 0: No underflow occurred. 1: Underflow occurred. In I2S_EXT slave transmit mode, if the first clock edge of data transfer arrives before new data is written to the data register, this bit will be set to 1. This flag is set to 1 by hardware, and reading the I2S_STS status register in software will clear it to 0.
5	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. This bit is set by hardware, and software must first read the data register, then read the I2S_STS status register to clear it.

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Bit field	Name	Description
4:3	Reserved	Reserved, the reset value must be maintained.
2	BUSY	Busy flag 0: I2S is not busy. 1: I2S is busy communicating or the transmit buffer is not empty. This bit is set or reset by hardware.
1	RNE	Receive buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.
0	TE	The transmit buffer is empty 0: The transmit buffer is not empty. 1: The transmit buffer is empty.

36.5.17 I2S_EXT Data Register (I2S_DAT)

Address offset：0x20C

Reset value：0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
rw															

Bit field	Name	Description
15:0	DAT[15:0]	Data register Data to be sent or received The data register corresponds to two buffers: one for write (transmit buffer); The other is for read (receive buffer).Write operation writes data to transmit buffer; The read operation will return the data in the receive buffer.

36.5.18 I2S_EXT Configuration Register (I2S_CFGR)

Address offset：0x21C

Reset value：0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PCMLBYPASS	CLKPOL	PCMSYNC	CHLEN	DATLEN[1:0]		I2SCFG[1:0]		I2SSTD[1:0]		I2SMOD	I2SE
				rw	rw	rw	rw	rw		rw		rw		rw	rw

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
11	PCMLBYPASS	pcm long for 13bit is bypass 1:no bypass 0:bypass
10	CLKPOL	Static clock polarity 0: I2S clock static state is low level. 1: I2S clock static state is high level. *Note: For correct operation, this bit can only be set when I2S_CFGR.I2SE=0.* *Note: not used in SPI mode.*
9	PCMSYNC	PCM frame synchronization 0: Short frame synchronization. 1: Long frame synchronization. *Note: This bit is only valid when I2S_CFGR.I2SSTD = 11 (used by the PCM standard).* *Note: not used in SPI mode.*
8	CHLEN	Channel length (number of data bits per audio channel) 0: 16 bits wide; 1: 32 bits wide. Writing to this bit is valid only when I2S_CFGR.DATLEN = 00, otherwise the channel length is fixed to 32 bits by hardware. *Note: For correct operation, this bit can only be set when I2S_CFGR.I2SE=0.* *Note: not used in SPI mode.*
7:6	DATLEN[1:0]	Length of data to be transmitted 00: 16-bit data length. 01: 24-bit data length; 10: 32-bit data length; 11: Not allowed. *Note: For correct operation, this bit can only be set when I2S_CFGR.I2SE=0.*
5:4	I2SCFG[1:0]	I^2S mode setting 00: Configured as slave transmit mode. 01: Configured as slave receive mode. 10: Configured as Master transmit mode. 11: Configured as Master receive mode. *Note: this bit can only be configured as 2'b00 or 2'b01.This bit can only be set when I2S_CFGR.I2SE=0.* *Note: not used in SPI mode.*
3:2	I2SSTD[1:0]	Selection of I^2S standard 00: I^2S Philips standard. 01: High byte alignment standard (left alignment). 10: Low byte alignment standard (right alignment). 11: PCM standard. *Note: this bit can only be set when I2S_CFGR.I2SE=0.* *Note: not used in SPI mode.*
1	I2SMOD	I^2S mode selection

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Bit field	Name	Description
		0: Select SPI mode. 1: Select I²S mode. *Note: this bit can only be configured as 1'b1. This bit can only be set when I2S_CFGR.I2SE=0.*
0	I2SE	I²S enable 0: Disable I²S. 1: Enable I²S. *Note: not used in SPI mode.*

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37 Expanded Serial Peripheral Interface（xSPI）

37.1 Introduction

xSPI can be used as a single/dual/quad/octal SPI peripheral communication interface. It can operate in two following modes.

- Indirect mode: Perform all operations using xSPI registers, could be known as FIFO mode. All the operations are performed through the setting of configuration register. Transmit data goes through the data register (which is a TX FIFO). Data exchanges are driven by software or by the DMA. Received data is returned by reading the data register (which is a RX FIFO).
- Memory-mapped mode: External flash is mapped to the microcontroller's address space, and the system treats it as internal storage space, could be known as eXecute In Place-XIP mode. AHB Read operation will be transformed into SPI flash read and write operation.

37.2 Main Features

The following list highlights the features of the xSPI Synchronous Serial Interface component:

- Data communication supports single/dual/quad/octal mode
- Supports Single SPI/Normal SPI, DUAL SPI, QUAD SPI, OCTAL SPI modes
- Bus max speed 133Mhz
- Supports Motorola SPI: Standard/Dual/Quad/Octal SPI
- Supports Single Data Rate (SDR) and Double Data Rate (DDR) modes
- Supports read data strobe feature
- Supports clock stretching feature
- In indirect mode and memory-mapped mode, the frame format and opcodes can be configured through software
- Internally integrated FIFO for transmitting and receiving data
- Supports 8/16/32-bit data access
- Dedicated 32x32bit TX FIFO and 32x32bit RX FIFO
- DMA capability for transmission and reception
- Supports only XIP read, not support XIP Write
    - Supports continuous transmission in XIP mode
    - Supports data prefetch operation in XIP mode
- Supports automatic decryption when executing code through XSPI peripheral, i.e., storing code in cipher text in XSPI peripheral, reading cipher text during code execution and automatically decrypting into plaintext for CPU execution, without affecting the access speed to external storage. Decryption can be enabled/disabled by software control, with the root key stored in the NVR area, inaccessible to the user

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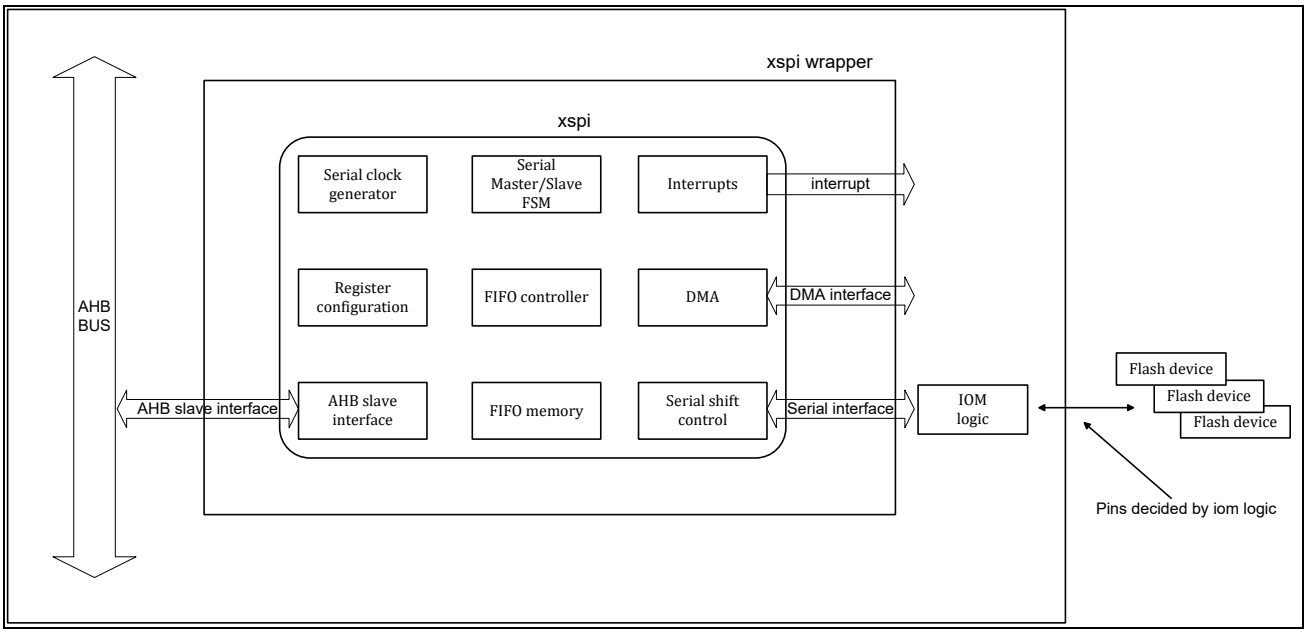
- Supports communication with serial NAND, NOR FLASH and PSRAM
- In master mode, it supports four external chip select output controls. In slave mode, it supports one chip select input. In master mode, all IOs multiplexed as chip select outputs can be multiplexed as chip select inputs in slave mode

37.3 Block diagram

Figure 37-1 xSPI Block Diagram



37.4 Function description

37.4.1 xSPI command sequence

XSPI_clk is derived from the AHB clock, BAUDR is the divisor, and SCK is the xSPI output clock. xSPI communicates with external devices through commands. Each command includes five phases: Instruction phase, Address phase, Mode bits phase, Wait cycles phase, and Data phase. Any phase can be skipped, but at least one of the Instruction phase, Address phase, Mode bits phase, or Data phase must be retained.

Figure 37-2 Octal spi command sequence

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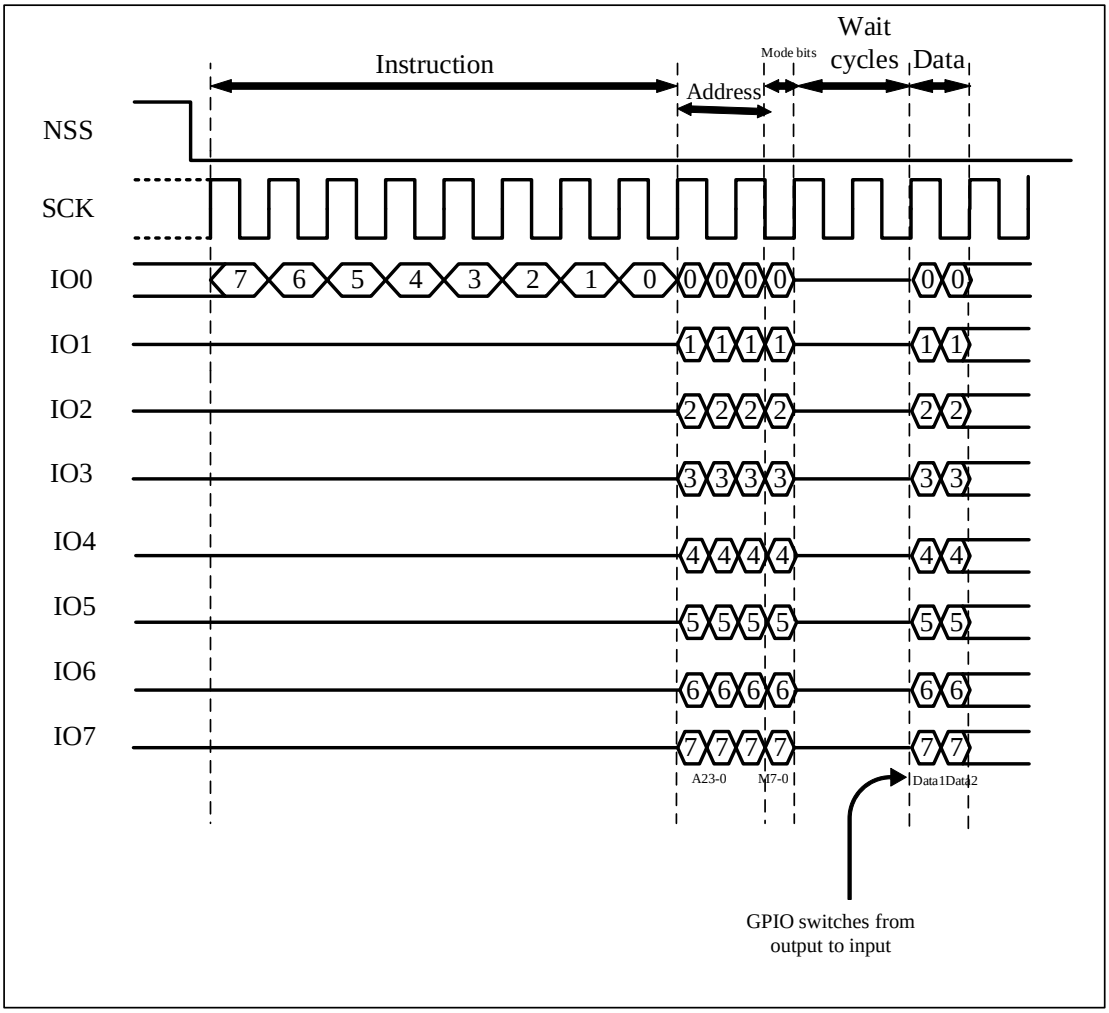

37.4.2 xSPI Programming guide

Before moving to XSPI register for its operation, ensure AHB_clk for registers configuration and xspi_core_clk (gated by xSPI sleep output signal) are already supported. In addition, some of MMU registers relative to xSPI FLASH also need to be configured as below:

NOTE: Before any registers are configured, make sure that XSPI_EN. XSPIEN was disable, at this time, Transmit and receive FIFO buffers are cleared, the xSPI sleep output is set (after delay) to inform the system that it is safe to remove the xSPI_ clk, thus saving power consumption in the system. When all required registers are configured, enable XSPI_EN. XSPIEN for xSPI operations.

Following configurations are settings for a basic transfer in indirect mode,DMA mode and xip mode.

37.4.2.1 Indirect mode

In indirect mode, commands are transferred by configuring xSPI registers, address and data is transferred through read and write data registers, following the same manner as with other communication peripherals.

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37.4.2.1.1 CTRL0 register

1) When XSPI_CTRL0.TMOD[1:0] 00, it is in transmit & receive mode, where both transmitting and receiving data are valid. The data transfer process continues until the transmit FIFO is empty. Data received from external devices is stored in the Receive FIFO, which can be accessed by the master processor.

   Note: transmit & receive mode can only be used in standard SPI mode (XSPI_CTRL0. SPIFRF [1:0] = 00)

2) When XSPI_CTRL0.TMOD[1:0] = 01, the xSPI is in indirect transmit mode, where the data to be transmitted is written to the XSPI_DATx register, and it is sent to the flash memory during the data transmission phase.

3) When XSPI_CTRL0.TMOD[1:0] = 10, the xSPI is in indirect receive mode, where data is received from the flash memory during the data reception phase, and the received data is obtained by reading the XSPI_DATx register.

4) When XSPI_CTRL0.TMOD[1:0] = 11, the xSPI is in EEPROM read mode, and can transmit the opcode/address to the EEPROM device.

   Note: EEPROM read mode is only supported in standard SPI mode (XSPI_CTRL0. SPIFRF [1:0] = 00). The number of bytes to be read is configured in XSPI_CTRL1.NDF[15:0]

- Select selects if xSPI is working in Master (default) or Slave mode by XSPI_CTRL0. MST (optional).

  Values:

  - 0x1 (MASTER): XSPI is Master
  - 0x0 (SLAVE): XSPI is Slave

  Because we only used Master Mode, so it is read only as zero（reserved）

- Select operation mode by XSPI_CTRL0.SRL (optional).

  Values:

  - 0x1 (TESTING_MODE): Test Mode Operation
  - 0x0 (NORMAL_MODE): Normal mode Operation-Default

- Enables or disables the setting of the xSPI output from the XSPI serial slave by XSPI_CTRL0.SLVOE (optional). Relevant only when the XSPI is configured as a serial-slave device. When configured as a serial master, this bit field has no functionality.

  Values:

  - 0x1 (DISABLED): Slave Output is disabled
  - 0x0 (ENABLED): Slave Output is enabled

- Selects clock phase and polarity by XSPI_CTRL0.SCPOL& XSPI_CTRL0.SCPH (optional).

  Values (SCPOL):

  - 0x0 (INACTIVE_HIGH): Inactive state of serial clock is low – Default SCPOL
  - 0x1 (INACTIVE_LOW): Inactive state of serial clock is high

  Values (SCPH):

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- 0x1 (START_BIT): Serial clock toggles at start of first bit
- 0x0 (MIDDLE_BIT): Serial clock toggles in middle of first bit– Default SCPH

- Selects data frame format for Transmitting/Receiving the data by XSPI_CTRL0.SPIFRF

  Values:

  - 0x0 (SPI_STANDARD): Standard SPI Format
  - 0x1 (SPI_DUAL): Dual SPI Format
  - 0x2 (SPI_QUAD): Quad SPI Format
  - 0x3 (SPI_OCTAL): Octal SPI Format

- Selects the data frame length by XSPI_CTRL0.DFS. When the data frame size is programmed to be less than 32 bits, the receive data is automatically right justified by the receive logic, with the upper bits of the receive FIFO zero-padded.
- Slave Select Toggle Enable by XSPI_CTRL0.SSTE (optional). While operating in SPI mode with clock phase (SCPH) set to zero, this register controls the behavior of the slave select line (NSS) between data frames. Values:

  - 0x1 (TOGGLE_EN): NSS line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while NSS is high
  - 0x0 (TOGGLE_DISABLE): NSS will stay low and sclk will run continuously for the duration of the transfer

  NOTE: A Slave select toggle is not supported when XSPI_CTRL0.SCPH parameter is set to one.

37.4.2.1.2 CTRL1 register

Selects Number of Data Frames by XSPI_CTRL1.NDF[15:0]. When XSPI_CTRL0.TMOD[1:0] = 10 or XSPI_CTRL0.TMOD[1:0] = 11, this register field sets the number of data frames to be continuously received by the XSPI. The XSPI continues to receive serial data until the number of data frames received is equal to this register value plus one, which enables you to receive up to 64 KB of data in a continuous transfer. When XSPI_ENH_CTRL0. CLKSTREN =1 and XSPI_CTRL0.TMOD[1:0] = 01, this register field sets the number of data frames to be continuously transmitted by XSPI. If the Transmit FIFO goes empty in-between, XSPI masks the serial clock (sclk_out) and wait for rest of the data until the programmed amount of frames are transferred successfully.

37.4.2.1.3 BAUDR register

Selects baud rate by XSPI_BAUD.CLKDIV. The LSB for this field is always set to zero (XSPI_BAUD[0]) and is unaffected by a write operation, which ensures an even value is held in this register. If the value is zero, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation:

Fsclk_out = Fssi_clk/BAUDR

where BAUDR is any even value between 2 and 65534 (BAUDR = {CLKDIV [14:0]*2}).

For example: for Fssi_clk = 3.6864MHz and BAUDR =2 Fsclk_out = 3.6864/2 = 1.8432MHz

37.4.2.1.4 TXFT register

Selects TX FIFO threshold value by XSPI_TXFT. TXFTST. Used to control the level of entries in transmit FIFO

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above which transfer will start on serial line. This register can be used to ensure that sufficient data is present in transmit FIFO before starting a write operation on serial line. In Internal DMA mode, this field sets the minimum amount of data frames present in the FIFO after which XSPI starts the transfer.

37.4.2.1.5 RXFT register

Selects RX FIFO threshold value by XSPI_RXFT. RXFTTFI. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 8-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + one, the receive FIFO full interrupt is triggered.

37.4.2.1.6 ENH_CTRL0 register

- Enables clock stretching capability in SPI transfers by XSPI_ENH_CTRL0. CLKSTREN (optional).

  In case of write, if the FIFO becomes empty XSPI will stretch the clock until FIFO has enough data to continue the transfer.

  In case of read, if the receive FIFO becomes full XSPI will stop the clock until data has been read from the FIFO.

- Selects Dual/Quad/Octal mode instruction length in bits by XSPI_ENH_CTRL0. INSTL

  Values:

  - 0x0 (INST_L0): No Instruction
  - 0x1 (INST_L4): 4 bit Instruction length
  - 0x2 (INST_L8): 8 bit Instruction length
  - 0x3 (INST_L16): 16 bit Instruction length

- Selects length of Address to be transmitted by XSPI_ENH_CTRL0.ADDRLEN. Only after this much bits are programmed in to the FIFO the transfer can begin.

- Selects whether XSPI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in XSPI_CTRL0.SPIFRF field by ADDRLEN. TRANSTYPE

  Values:

  - 0x0 (TT0): Instruction and Address will be sent in Standard SPI Mode.
  - 0x1 (TT1): Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by XSPI_CTRL0.SPIFRF.
  - 0x2 (TT2): Both Instruction and Address will be sent in the mode specified by XSPI_CTRL0.SPIFRF.
  - 0x3 (TT3): Reserved.

- Selects wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception by XSPI_ENH_CTRL0.WAITCYCLES.

- Enables SPI data mask by XSPI_ENH_CTRL0. SPIRXDSEN (optional). When this bit is enabled, the txd_dm signal is used to mask the data on the txd data line. This bit is enabled only when the SSIC_DM_EN parameter

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is set to one.

- Enables read data strobe enable by XSPI_ENH_CTRL0. SPIDMEN (optional). Once this bit is set to one XSPI will use Read data strobe (rxds) to capture read data in DDR mode
- Enables Instruction DDR by XSPI_ENH_CTRL0. WRINDDREN (optional). This will enable Dual-data rate transfer for Instruction phase.

37.4.2.1.7 SLAVE_EN register

Selects Slave enable by XSPI_SLAVE_EN.SEN[3:0]. Each bit in this register corresponds to a slave select line from the XSPI master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to • the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

37.4.2.1.8 STS register

Tracking the status of TX/RX FIFO by polling/reading fields of XSPI_STS (Status register).

- XSPI_STS.DCERR: Data Collision Error.
- XSPI_STS.TXE: Transmission Error.
- XSPI_STS.RXFF: Receive FIFO Full.
- XSPI_STS.RXFNE: Receive FIFO Not Empty.
- XSPI_STS.TXFE: Transmit FIFO Empty.
- XSPI_STS.TXFNF: Transmit FIFO Not Full.
- XSPI_STS.BUSY: SSI Busy Flag.

37.4.2.1.9 DATx register

Access TX/RX FIFO by writing/reading these registers. When writing to this register, you must right-justify the data. Read data are automatically right justified.

37.4.2.2 DMA mode

Configurations with DMA transfer as follows:

Step1, need to configure required registers for read/write operation mentioned in above (Indirect mode).

Step2, configure registers required for DMA transfer as following:

37.4.2.2.1 DMA_CTRL register

- If execute write transaction, enables the transmit FIFO DMA channel by XSPI_DMA_CTRL.TXDMAEN

  Values:

  - 0x1 (ENABLED): Transmit DMA enabled
  - 0x0 (DISABLE): Transmit DMA disabled

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- If execute read transaction, enables the receive FIFO DMA channel by XSPI_DMA_CTRL.RXDMAEN

  Values:

  - 0x1 (ENABLED): Receive DMA enabled
  - 0x0 (DISABLE): Receive DMA disabled

37.4.2.2.2 DMATDL_CTRL register

Selects Transmit Data Level by XSPI_DMATDL_CTRL. DMATDL. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and XSPI_DMA_CTRL.TXDMAEN = 1.

37.4.2.2.3 DMARDL_CTRL register

Selects receive Data Level by XSPI_DMARDL_CTRL. DMARDL. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and XSPI_DMA_CTRL. RXDMAEN =1.

Step3, configure DMA for operations with source/destination address, numbers of data frame (BLK_TS), data width, numbers of data beat per burst (MSIZE).

Step4, start read/write command by XSPI.

37.4.2.3 eXecute In Place (XIP) mode

NOTE: At N32xxx, only XIP READ is supported, so only registers related to XIP READ are configured.

37.4.2.3.1 XIP_INCR_TOC register

Selects instruction op-code to be used in XIP READ INCR transactions by XSPI_XIP_WRITE_INCR_INST. INCRWRINST[15:0]. When XSPI_XIP_CTRL. XIPINSTEN bit is set to one, XSPI sends instruction for all XIP transfers, this register field stores the instruction op-code to be sent when an INCR type transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by XSPI_ENH_CTRL0. INSTL field.

37.4.2.3.2 XIP_WRAP_TOC register

Selects instruction op-code to be used in XIP READ WRAP transactions by XSPI_XIP_WRAP_TOC. WTOC [15:0]. When XSPI_XIP_CTRL. XIPINSTEN bit is set to one, XSPI sends instruction for all XIP transfers, this register field stores the instruction op-code to be sent when a WRAP type transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by XSPI_ENH_CTRL0. INSTL field.

37.4.2.3.3 XIP_CTRL register

- Enables XIP pre-fetch functionality in XSPI by XSPI_XIP_CTRL.XIPPREEN (optional). Once enabled XSPI will pre-fetch data frames from next contiguous location, to reduce the latency for the upcoming contiguous transfer. If the next XIP request is not contiguous then pre-fetched bits will be discarded.
- Selects XIP Mode bits length by XSPI_XIP_CTRL.XIPMBL(optional). These bits are valid only when XSPI_XIP_CTRL.MDBITSEN is set to one.
- Enable continuous transfer in XIP mode by XSPI_XIP_CTRL. XIPCTEN (optional). If this bit is set to 1 then

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continuous transfer mode in XIP will be enabled, in this mode XSPI will keep slave selected until a non-XIP transfer is detected on the AHB interface.

- Selects XIP instruction enable bit by XSPI_XIP_CTRL. XIPINSTEN. If this bit is set to 1 then XIP transfers will also have instruction phase. The instruction op-codes will be chosen from XSPI_XIP_INCR_TOC or XSPI_XIP_WRAP_TOC registers bases on AHB transfer type.
- Enables read data strobe enable bit by XSPI_XIP_CTRL. RXDSEN (optional). Once this bit is set to 1 XSPI will use Read data strobe (rxds) to capture read data in DDR mode
- Enables instruction DDR Enable bit by XSPI_XIP_CTRL.WRINDDREN (optional). This will enable Dual-data rate transfer for Instruction phase
- Enables SPI DDR Enable bit by XSPI_XIP_CTRL.DDREN (optional). This will enable Dual-data rate transfers in Dual/Quad/Octal frame formats of SPI.
- Selects fix DFS for XIP transfers by XSPI_XIP_CTRL.DFSHC (optional). If this bit is set to one then data, frame size for XIP transfers will be fixed to the programmed value in CTRLR0.DFS. The number of data frames to fetch will be determined by HSIZE and HBURST signals. If this bit is set to zero then data, frame size and number of data frames to fetch will be determined by HSIZE and HBURST signals
- Selects wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception by XSPI_XIP_CTRL.WAITCYCLES. Specified as number of SPI clock cycles.
- Selects Dual/Quad/Octal mode instruction length in bits by XSPI_XIP_CTRL.INSTL.
- Selects length of Address to be transmitted by XSPI_XIP_CTRL.ADDRL. Only after this much bits are programmed in to the FIFO the transfer can begin.
- Selects address and instruction transfer format by XSPI_XIP_CTRL. TRANSTYPE. Selects whether XSPI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in XSPI_CTRL0.SPIFRF field.
- Selects data frame format for Transmitting/Receiving the data by XSPI_XIP_CTRL.FRF.

37.4.2.3.4 XIP_SLAVE_EN register

Selects slave enable by XSPI_XIP_SLAVE_EN. SEN[3:0]. Each bit in this register corresponds to a slave select line (nss) from the XSPI master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a XIP transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a XIP transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

37.4.3 Big-Little endian

At this feature, we will only consider for XIP read transmission because XIP write is not supported in N32Hxx. For non-XIP, xspi also sample afio_xspi_endian signal which is software configuration to determine if write data was in little endian (default) or big endian.

The SPI flash memory is byte addressable memory. For read and write (programming) it takes the start address and

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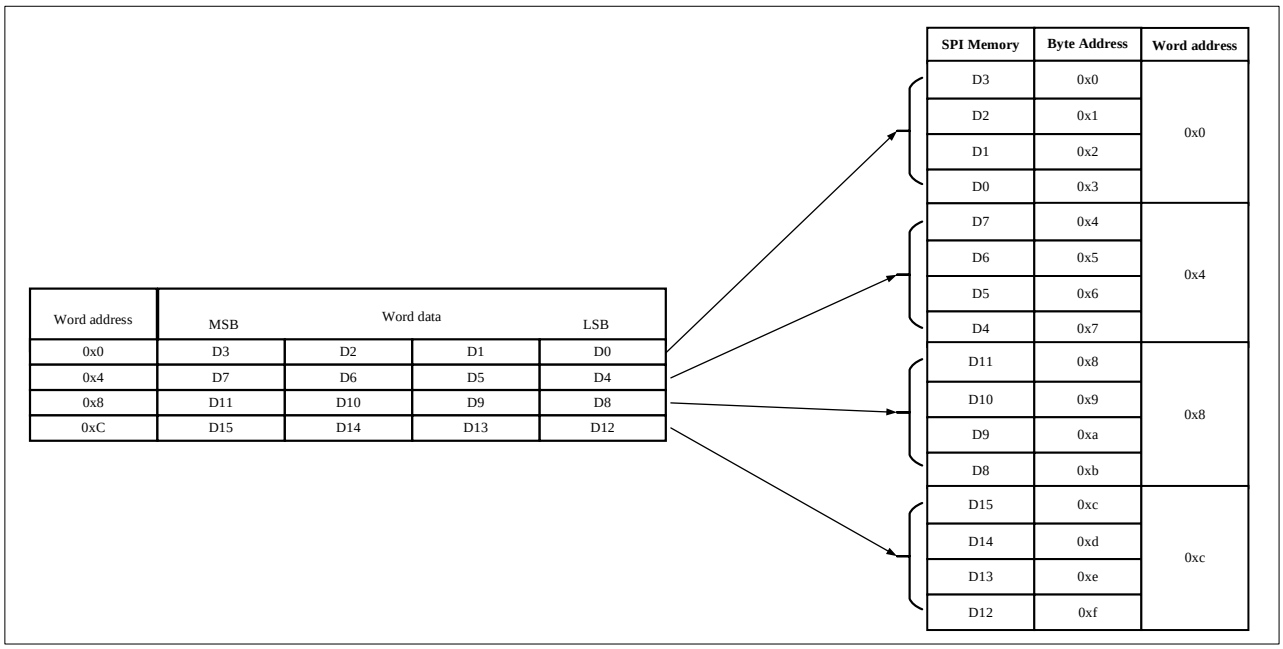
write serially the data and increments the address for the subsequent read or write access. Since the N32Hxx CPU is 32-bit and the AHB bus is 32-bit, we will discuss the memory organization for 32-bit data.

Let's consider, we write 4 Words (32-bit data) to the SPI flash as AHB incremental burst (INCR4) with HSIZE=32-bit. The xSPI controller transmit the first address of the AHB burst in the address phase and transmit data serially in the data phase. Data will be transmitted from Most Significant Bit (MSB) to Least Significant Bit (LSB), i.e., MSB will be transmitted first and LSB at last. How this AHB burst data will be stored in the SPI flash is shown as below.

Figure 37-3 32-bit write-read format



From this figure we can see that the data is stored in the flash can be seen as 32-bit big endian format. Now reading the memory content as Word will produce the same data output as the data has been written. If the Byte or Half word data is read back from the SPI flash memory the result, will be inconsistent to the write data. For example, if we read half word (16-bit) on address 0x4, the controller will issue the read command at address 0x4 and receive 16-bit serial transmission from MSB to LSB. As shown as below the output data will be wrong.

Figure 37-4 Wrong read 16-bit format

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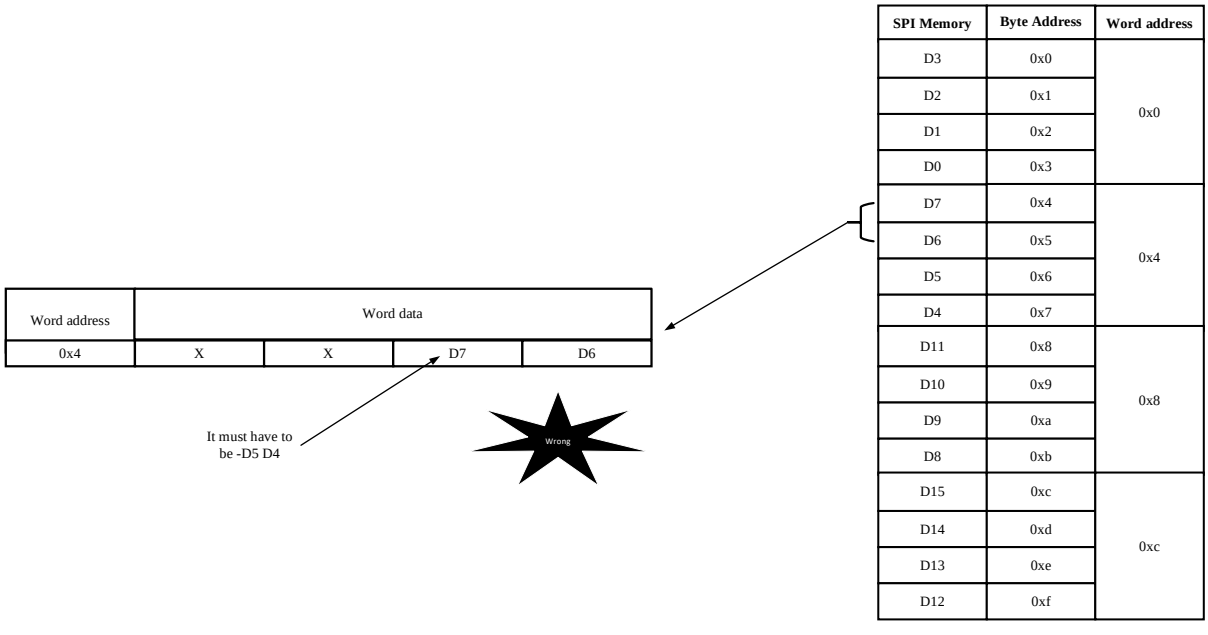
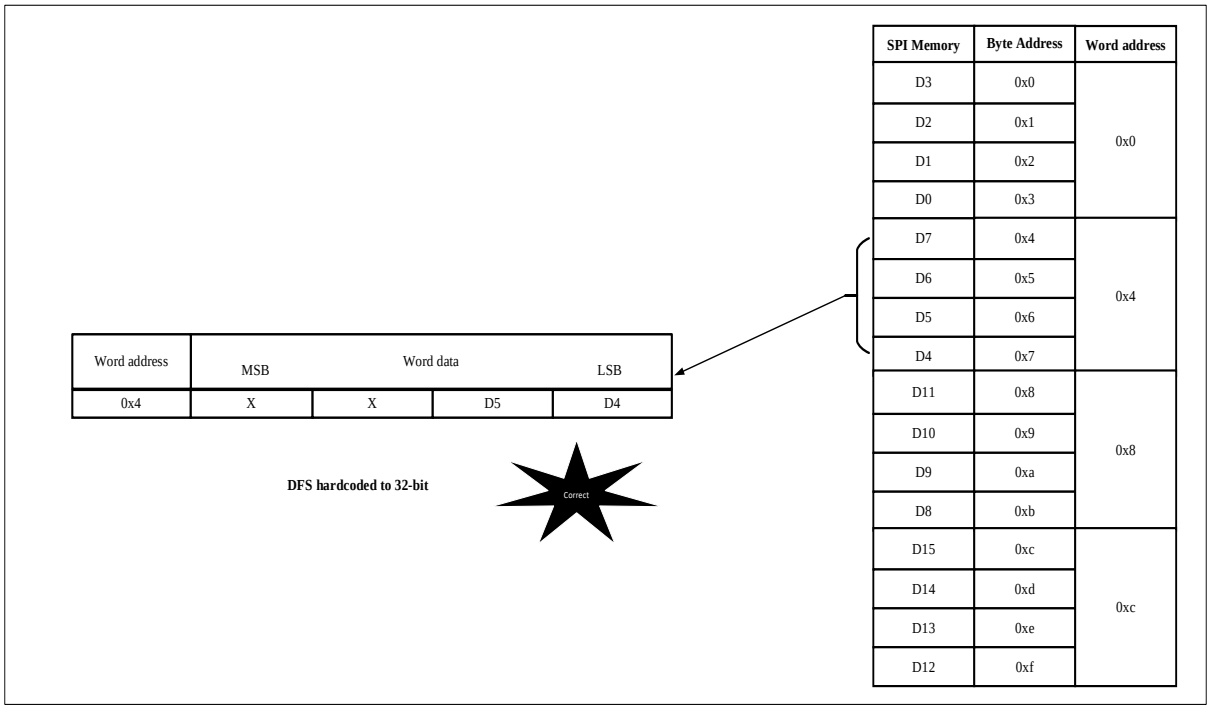


To solve that read transfer issue the xSPI controller have a register to specify the data frame size (DFS) which should be hardcoded to 32-bit as we have written the data into 32-bit format. Below shows the same AHB half word read with the DFS is hardcoded to 32-bit returns the correct value. When the DFS is hardcoded to 32-bit the xSPI controller reads the whole word and then pass the required 16-bit to the AHB bus.

Figure 37-5 Correct read 16-bit format with DFS-HC enable



Once the DFS is hardcoded to 32-bit, the read will always return the correct value for 8/16/32-bit read.

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37.4.4 Data transfer

Data transfers are started by the serial-master device when:

- XSPI is enabled (XSPIEN = 1) and
- Serial-slave device is enabled (SEN=1)
- Number of data entries in transmit FIFO is its threshold (XSPI_TXFT register)

While actively transferring the data, the busy flag (BUSY) in the status register (XSPI_STS) is set. You must wait until the busy flag is cleared before attempting a new serial transfer.

37.4.5 Clock ratios

37.4.5.1 Master

For the master mode of operation, the peripheral clock (sclk_out) period is a multiple of the internal core clock (ssi_clk). In the slave mode of operation, a synchronized peripheral clock is used by xSPI to receive or transmit the data.

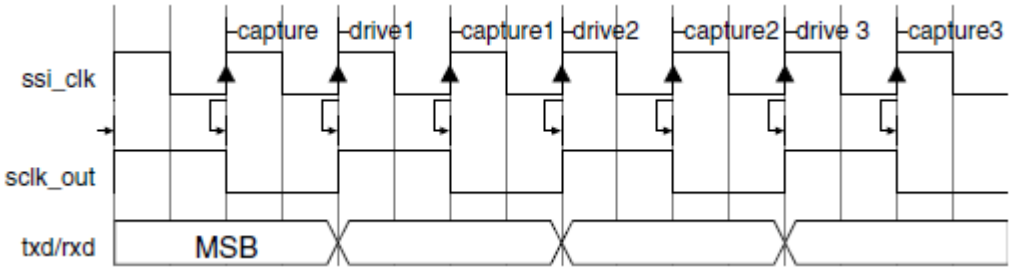
When the xSPI macro cell is configured as a master device, the maximum frequency of the bit-rate clock (sclk_out) is one-half the frequency of ssi_clk signal.

The frequency of sclk_out signal can be derived from the following equation.

Fsclk_out = Fssi_clk/SCKDV

Where, SCKDV is a programmable register holding any even value in the range 0 – 65,534. If SCKDV = 0, sclk_out is disabled.

Figure 37-6 Maximum sclk_out/ssi_clk ratio



37.4.5.2 Slave

When the xSPI macro cell is configured as a slave device the minimum frequency of the ssi_clk signal depends on the SSIC_ENH_CLK_RATIO configuration parameter and the operation of the slave peripheral.

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the xSPI peripheral clock (ssi_clk) are as follows:

- Slave SSIC_ENH_CLK_RATIO = 0
  - Receive only: Fssi_clk >= 8× (maximum Fsclk_in)
  - Transmit and Receive: Fssi_clk >= 10 × (maximum Fsclk_in)

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- Slave SSIC_ENH_CLK_RATIO = 1

- Fssi_clk >= 4 × (maximum Fsclk_in)

37.4.6 Receive and Transmit FIFO

In N32xxx, xSPI supports 32x32bit TX FIFO and 32x32-bit RX FIFO. Data frames that are less than 32 bits in size must be right justified when written into the transmit FIFO buffer. The shift control logic automatically right-justifies receive data in the receive FIFO buffer.

NOTE: The transmit and receive FIFO buffers are cleared when the xSPI is disabled (XSPIEN = 0) or when it is reset (hresetn).

The transmit FIFO is loaded by AHB write commands to the xSPI data register (XSPI_DATx). Data are popped (removed) from the transmit FIFO by the shift control logic into the transmit shift register. In addition, interrupts are asserted when transmit FIFO encounters below cases:

- Transmit FIFO Empty Interrupt (XSPI_ISTS.TXFEIS) – Set when the transmit FIFO is equal to or below its threshold value and requires service to prevent an under-run. The threshold value, set through a software-programmable register, determines the level of transmit FIFO entries at which an interrupt is generated. This interrupt is cleared by hardware when data are written into the transmit FIFO buffer, bringing it over the threshold level.

- Transmit FIFO Overflow Interrupt (XSPI_ISTS.TXFOIS) – Set when an AHB access attempts to write into the transmit FIFO after it has been completely filled. When set, data written from the AHB is discarded. This interrupt remains set until you read the transmit FIFO error interrupt clear register (XSPI_TXEICR_CLR.TXEICR).

Data are popped from the receive FIFO by AHB read commands to the XSPI data register (XSPI_DATx). The receive FIFO is loaded from the receive shift register by the shift control logic. In addition, interrupts are asserted when receive FIFO encounters below cases:

- Receive FIFO Full Interrupt (XSPI_ISTS.RXFFIS) – Set when the receive FIFO is equal to or above its threshold value plus 1 and requires service to prevent an overflow. The threshold value, set through a software-programmable register, determines the level of receive FIFO entries at which an interrupt is generated. This interrupt is cleared by hardware when data are read from the receive FIFO buffer, bringing it below the threshold level.

- Receive FIFO Overflow Interrupt (XSPI_ISTS.RXFOIS) – Set when the receive logic attempts to place data into the receive FIFO after it has been completely filled. When set, newly received data are discarded. This interrupt remains set until you read the receive FIFO overflow interrupt clear register (XSPI_RXFOI_CLR.RXFOIC).

- Receive FIFO Underflow Interrupt (XSPI_ISTS.RXFUIS) – Set when an AHB access attempts to read from the receive FIFO when it is empty. When set, zeros are read back from the receive FIFO. This interrupt remains set until you read the receive FIFO underflow interrupt clear register (XSPI_RXFUI_CLR.RXFUIC).

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37.4.7 Enhanced SPI

xSPI supports the dual, quad, and octal modes of SPI using the xSPI_MODE configuration parameter. When dual, quad, or octal mode is selected for this parameter, the width of txd, rxd and ssi_oe_n signals change to 2, 4, or 8, respectively. Hence, the data is shifted out/in on more than one line, increasing the overall throughput. The mode of operation (write/read) can be selected using the XSPI_CTRL0.TMOD field.

All four combinations of the serial clock's polarity and phase are valid in this mode and it works same as in normal SPI mode. However, need to check which modes (polarity, phase) that Flash devices support.

37.4.7.1 Enhanced write operation

Dual, Quad, or Octal SPI write operations can be divided into three parts:

Instruction phase -Address phase -Data phase

The following register fields are used for a write operation:

- XSPI_CTRL0.SPIFRF - Specifies the format in which the transmission happens for the frame.
- XSPI_ENH_CTRL0 (xSPI Control Register 0 register) – Specifies length of instruction, address, and data.
- XSPI_ENH_CTRL0.INSTL – Specifies length of an instruction (possible values for instruction length are 0, 4, 8, or 16 bits.)
- XSPI_ENH_CTRL0.ADDRLEN – Specifies address length
- XSPI_CTRL0.DFS – Specifies data length.

An instruction takes one FIFO location and address can take more than one FIFO locations. Both the instruction and address must be programmed in the data register (XSPI_DATx). xSPI waits until both have been programmed to start the write operation. The instruction, address and data can be programmed to send in dual mode/quad mode/octal mode, which can be selected from the XSPI_ENH_CTRL0.TRANSTYPE and XSPI_CTRL0.SPIFRF fields.

NOTE: If XSPI_CTRL0.SPIFRF is selected to be Standard SPI Format, everything is sent in Standard SPI mode and XSPI_ENH_CTRL0.TRANSTYPE field is ignored. In addition, XSPI_CTRL0.SPIFRF is only applicable if XSPI_CTRL0.SPIFRF is programmed to 00.

Typical write operation is showed as below:

Figure 37-7 Typical write operation

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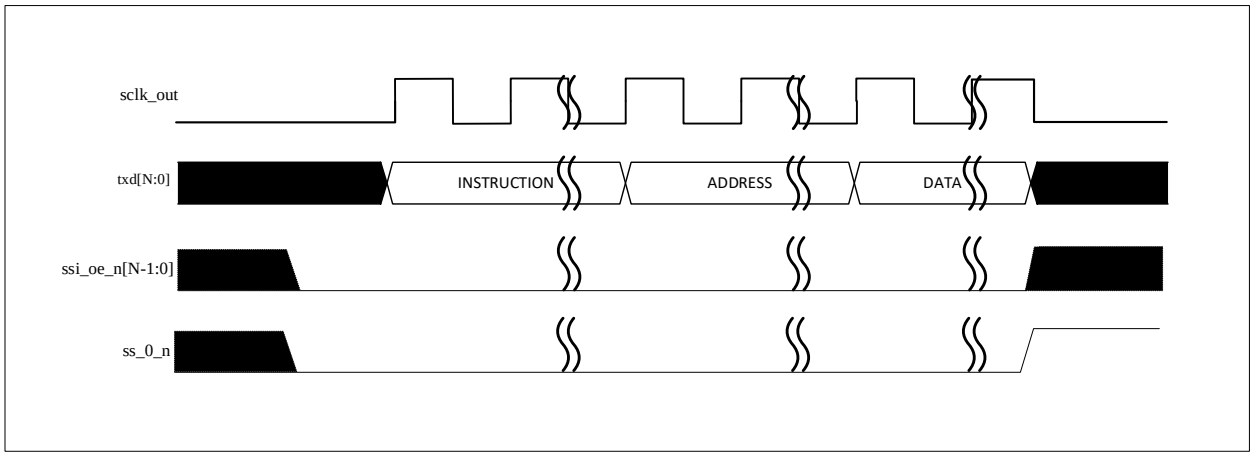
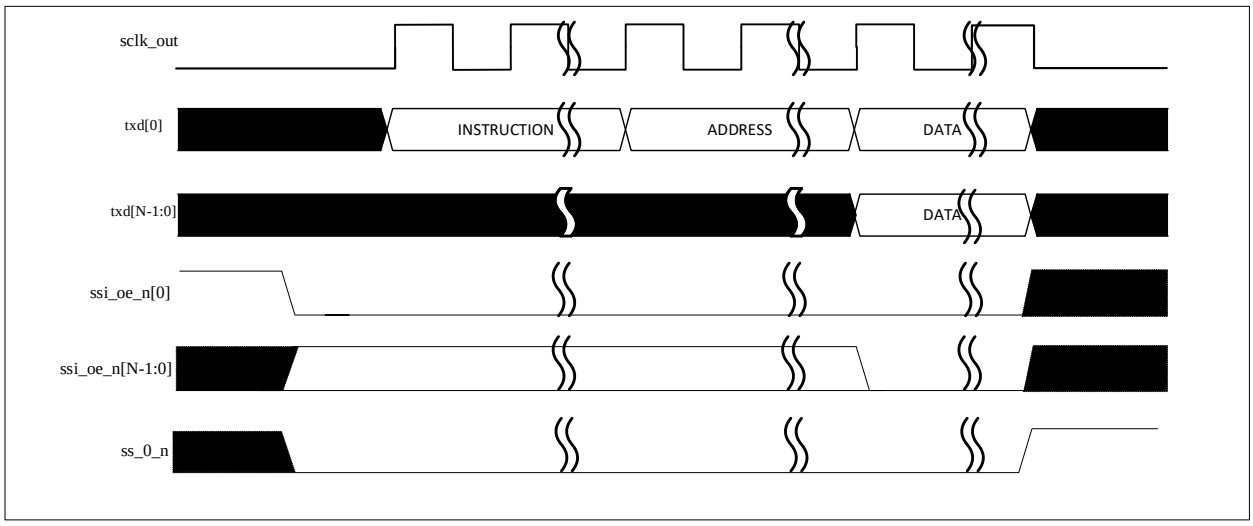


- Case A: Instruction and address both transmitted in standard SPI format

  For this, XSPI_ENH_CTRL0.TRANSTYPE field must be set to 00

Figure 37-8 Instruction and address both transmitted in standard SPI format



- Case B: Instruction transmitted in standard and address transmitted in Enhanced SPI format

  For this, XSPI_ENH_CTRL0.TRANSTYPE field must be set to 01.

Figure 37-9 Instruction transmitted in standard and address transmitted in Enhanced SPI format

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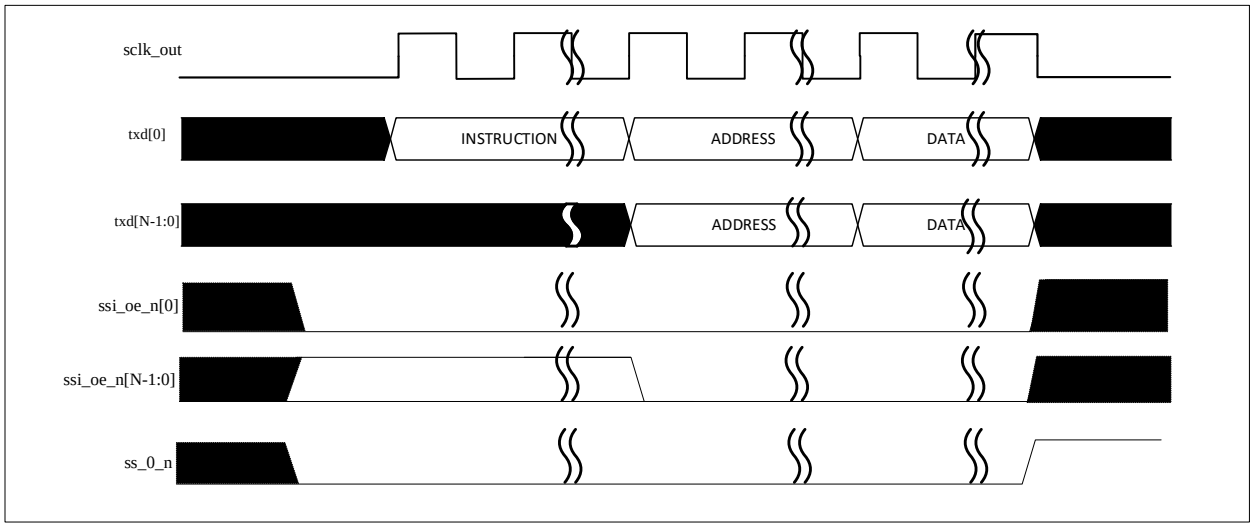
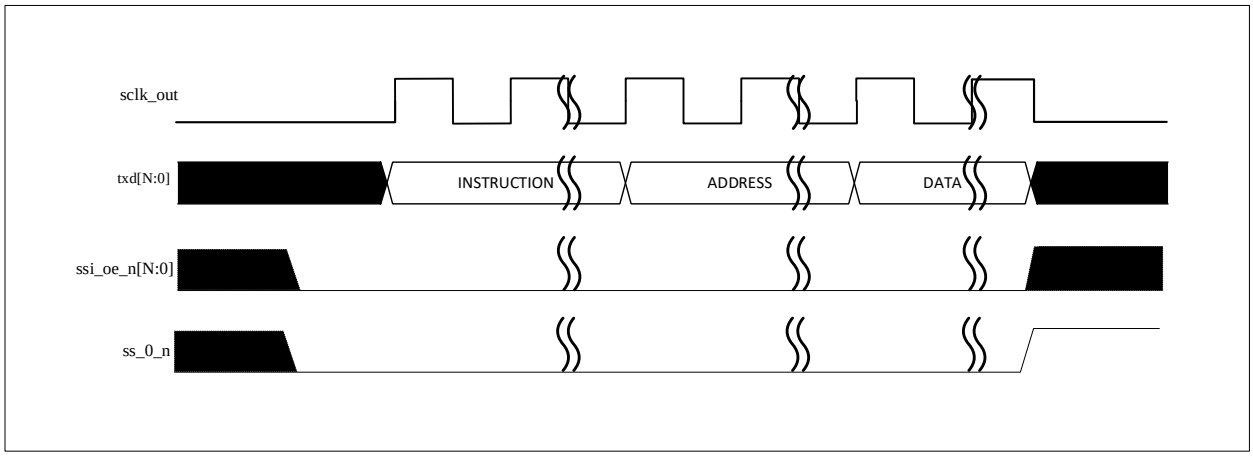


- Case C: Instruction and Address both transmitted in Enhanced SPI format

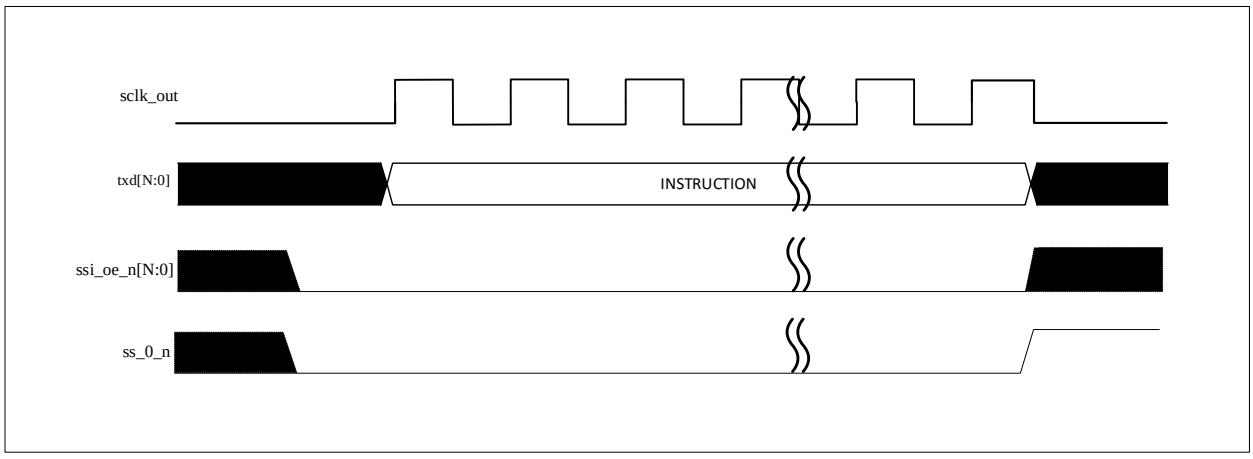
  For this, XSPI_ENH_CTRL0.TRANSTYPE field must be set to 10.

Figure 37-10 Instruction and Address both transmitted in Enhanced SPI format



- Case D: Instruction only transfer in enhanced SPI format

Figure 37-11 Instruction only transfer in enhanced SPI format



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37.4.7.2 Enhanced read operation

A Dual, Quad, or Octal SPI read operation could be divided into four phases:

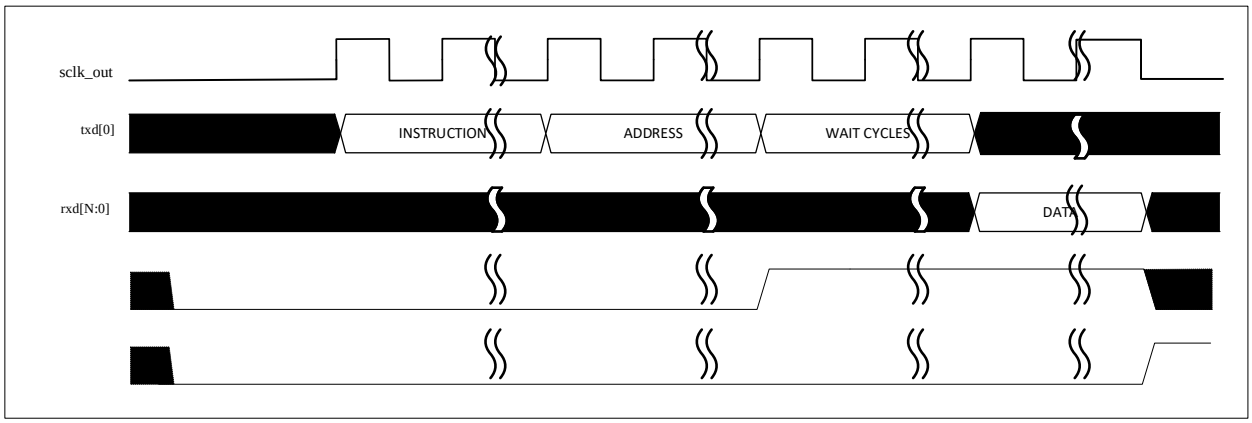
Instruction phase - Address phase -Wait cycles - Data phase

Wait Cycles can be programmed using XSPI_ENH_CTRL0.WAITCYCLES field. The wait cycles are introduced for target slave to change their mode from input to output and the wait cycles can vary for different devices.

For a READ operation, xSPI sends instruction and control data once and waits until it receives NDF (XSPI_CTRL1 register) number of data frames and then de-asserts slave select signal.

Typical read operation is showed as below:

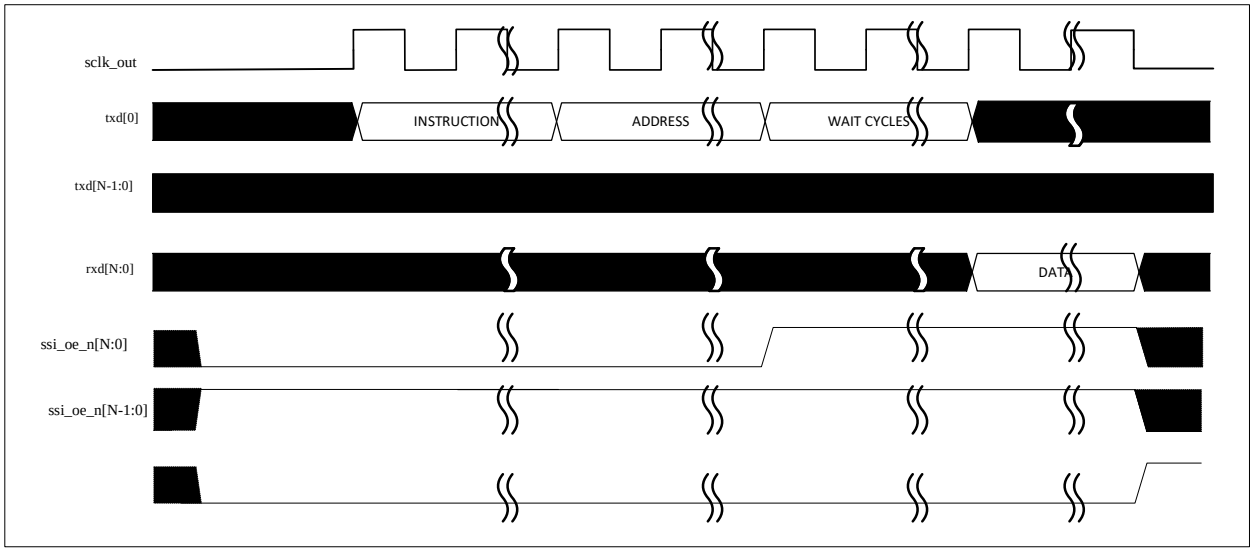
Figure 37-12 Typical read operation



- Case A: Instruction and address both transmitted in standard SPI format

For this, XSPI_ENH_CTRL0.TRANSTYPE field should be set to 00

Figure 37-13 Instruction and address both transmitted in standard SPI format



- Case B: Instruction transmitted in standard and address transmitted in Enhanced SPI format

  For this, XSPI_ENH_CTRL0.TRANSTYPE field should be set to 01

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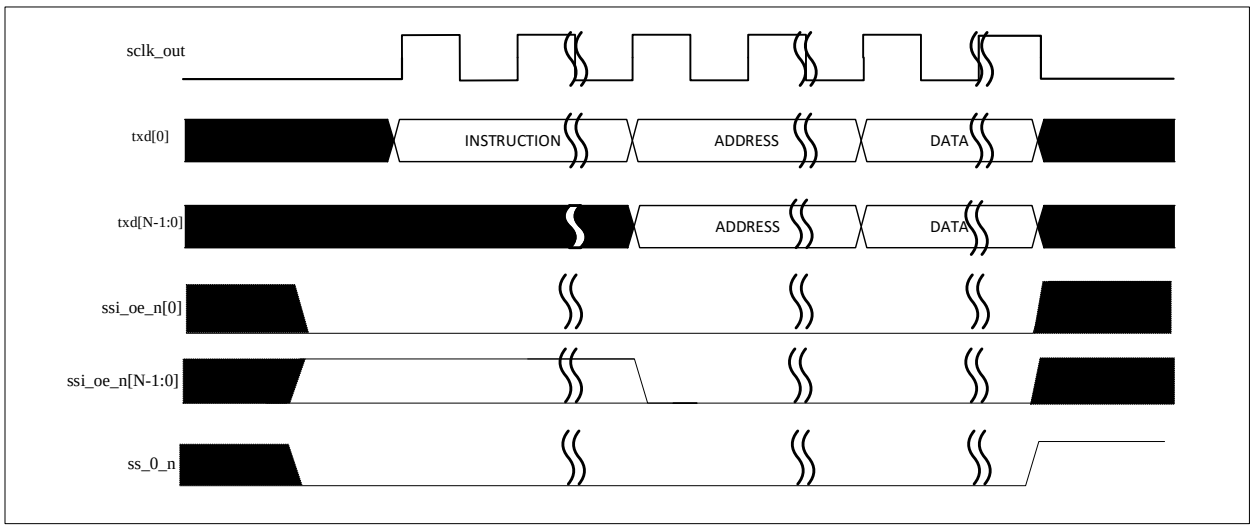
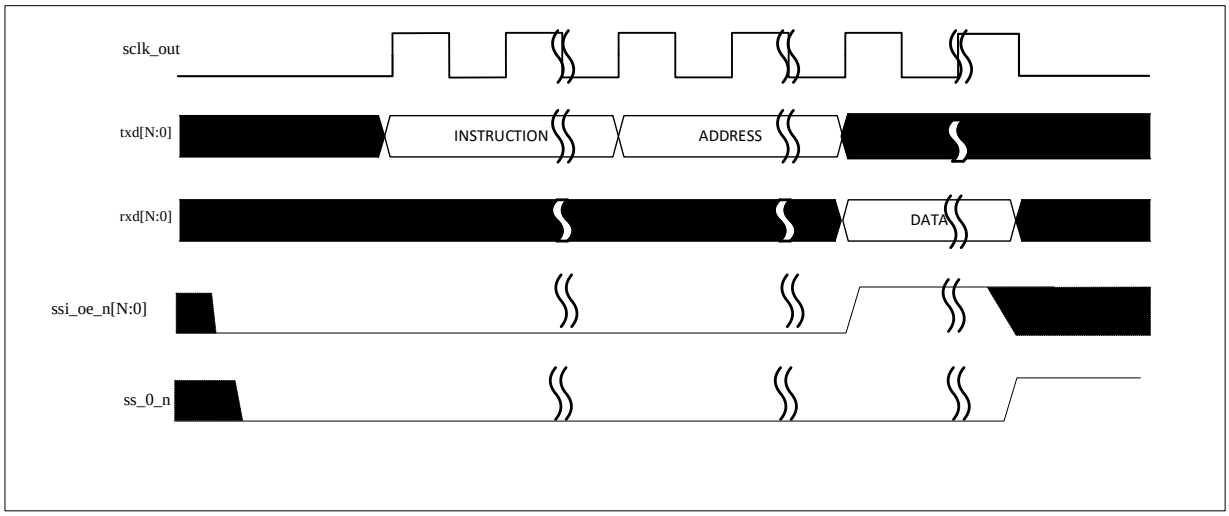
Figure 37-14 Instruction transmitted in standard and address transmitted in Enhanced SPI format



- Case C: Instruction and Address both transmitted in Enhanced SPI format

  For this, XSPI_ENH_CTRL0.TRANSTYPE field must be set to 10.

Figure 37-15 Instruction and Address both transmitted in Enhanced SPI format



- Case D: No Instruction, No Address READ transfer

  For this, XSPI_ENH_CTRL0.ADDRLEN and XSPI_ENH_CTRL0.INSTL must be set to 0 and XSPI_ENH_CTRL0.WAITCYCLES must be set to a non-zero value.

Figure 37-16 No Instruction, No Address READ transfer

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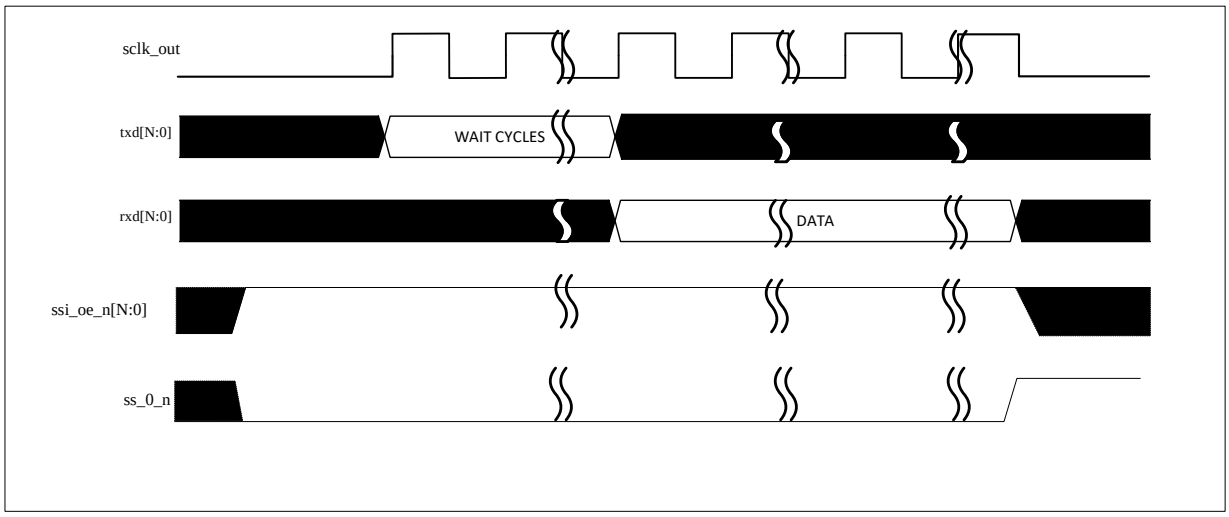
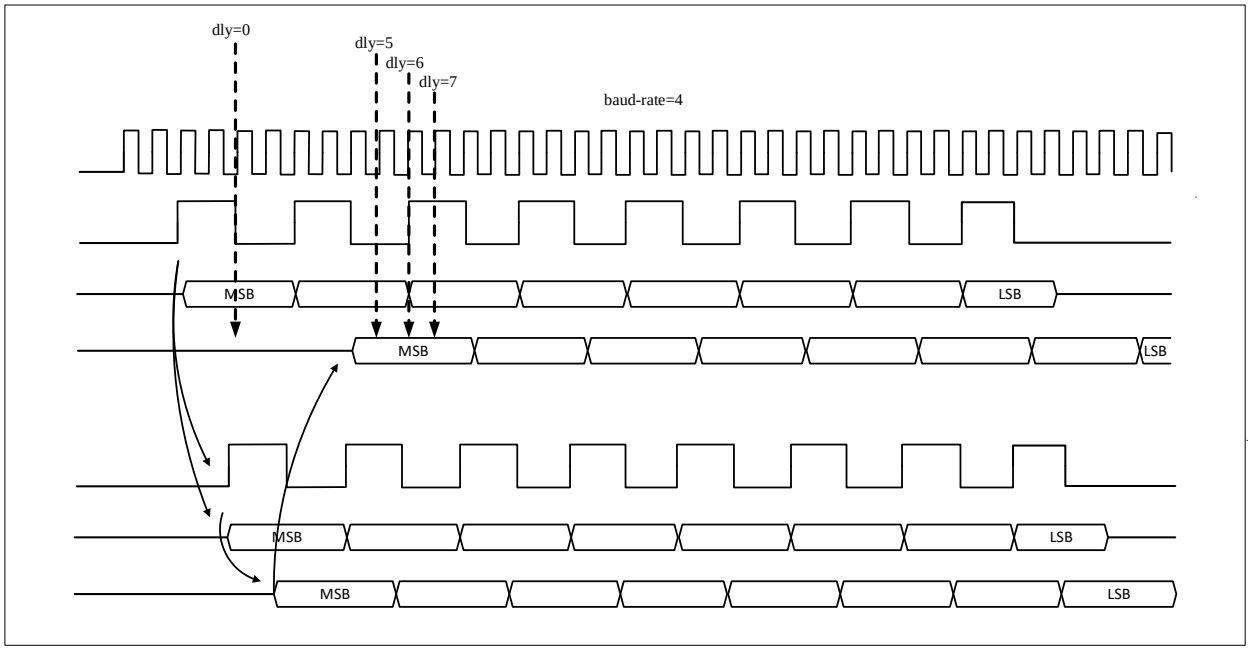


37.4.8 RXD sample delay

When xSPI is configured as a master, additional logic can be included in the design in order to delay the default sample time of the rxd signal. This additional logic can help to increase the maximum achievable frequency on the serial bus.

Figure 37-17 Round-trip delay



Round trip routing delays on the sclk_out signal from the master and the rxd signal from the slave can mean that the timing of the rxd signal—as seen by the master—has moved away from the normal sampling time. xSPI uses XSPI_RX_DELAY register to change the sampling point of rxd signal.

- If XSPI_RX_DELAY field of the SE register is set to zero, then XSPI delays the sampling point by the programmed number of ssi_clk cycles.

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- If XSPI_RX_DELAY field of the SE register is set to 1, then XSPI delays sampling point by programmed number of ssi_clk cycles + 0.5 * (ssi_clk period). Thus, the sampling is done on negative edge of ssi_clk signal. This gives user more sampling points within single sclk_out clock period.

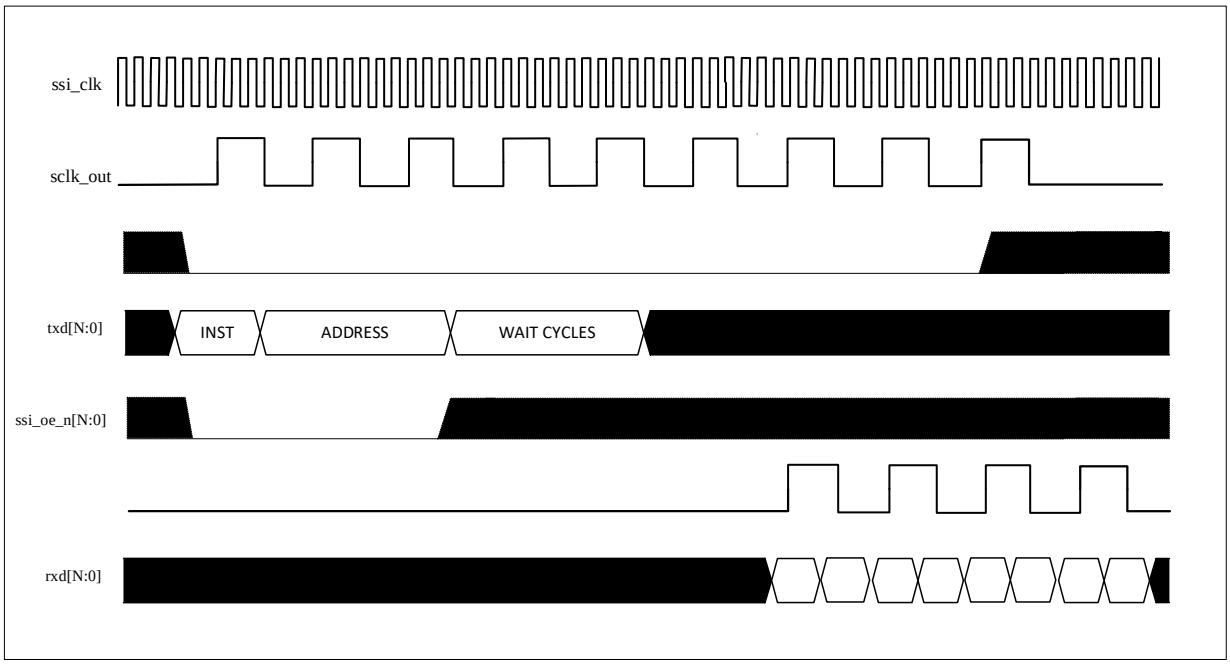
37.4.9 Read data strobe signal

To achieve high frequency, data strobe signaling is used in read operations. The device provides a data strobe (known as read data strobe (rxds), signal along with read data, which determines the output data valid window. The device provides data edge-aligned with respect to data strobe which need to be phase shifted and given to XSPI.

You must program the XSPI_ENH_CTRL0 field of the SPIRXDSEN register to one to sample incoming data with respect to the read data strobe signal.

NOTE: The data must be stable around the clock edge of the data strobe signal while sampling on both edges.

Figure 37-18 Read data strobe signal while reading from flash



Only the SPI mode 0 is supported in this mode, that is when SCPH= 0 and SCPOL= 0.

37.4.10 Clock stretching

While XSPI is transmitting or receiving the data from SPI device, the software may not be able to keep up with the transfer rate due to the bandwidth issues on the slave interface. To avoid data corruption, CPU must discard the current operation and start a new transfer. This process is time consuming and inefficient. To handle such scenarios, clock-stretching support has been added in XSPI.

Clock stretching feature can be used to prevent FIFO underflow and overflow conditions while transmitting or receiving the data respectively.

- For write transactions, If TX FIFO becomes empty before the transfer is complete, then XSPI master does not de-select the slave, instead it masks the sclk_out and then resumes the clock when TX FIFO becomes non-empty.

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While transmitting, you should program the number of data frames in the XSPI_CTRL1 register. The clock stretching only happens in the data phase of enhanced SPI transfers, to ensure that at least one data (apart from instruction and address) is present in transmit FIFO. Set the minimum threshold value in the XSPI_TXFT. TXFTST register to achieve that.

- In case of receive transaction, when RX FIFO becomes full, then XSPI masks sclk_out until the data is read from receive FIFO (the data level goes below the RX threshold programmed in the XSPI_RXFT register). If XSPI_RX_DELAY register is enabled, XSPI estimates the time when RX FIFO may become full and masks sclk_out accordingly.

XSPI provides a programming bit (CLKSTREN) in XSPI_ENH_CTRL0 register to enable clock-stretching feature.

NOTE: Clock stretching feature is applicable only for enhanced SPI transfers except XIP transfers.

37.4.11 Dual-Data rate (DDR)

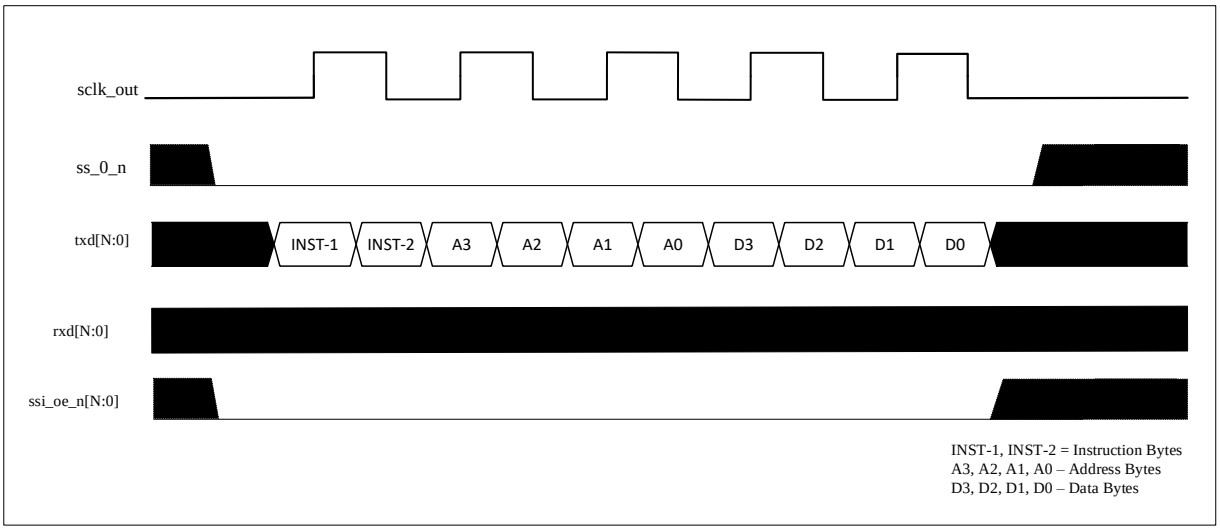
Enabling the DDR mode bit will enable double-rate transmission for the corresponding communication phases in 2/4/8-wire mode of SPI, which can improve throughput. Data is transferred on both the positive and negative edges of the clock.

The DDR mode supports the following modes of the SPI protocol:

- Mode0: When the default serial clock phase and default serial clock polarity are not enabled (XSPI_CTRL0.SCPH= 0 & XSPI_CTRL0.SCPOL = 0)
- Mode3: When the default serial clock phase and default serial clock polarity are enabled (XSPI_CTRL0.SCPH = 1& XSPI_CTRL0.SCPOL = 1)

The WRSPIDDREN (XSPI_ENH_CTRL0[16]) bit is used to determine if the Address and data have to be transferred in DDR mode and WRINDDREN (XSPI_ENH_CTRL0[16][17]) bit is used to determine if Instruction must be transferred in DDR format. These bits are only valid when the XSPI_CTRL0.SPIFRF bit is set to be in Dual, Quad or Octal mode.

Figure 37-19 Instruction, address and data in DDR format



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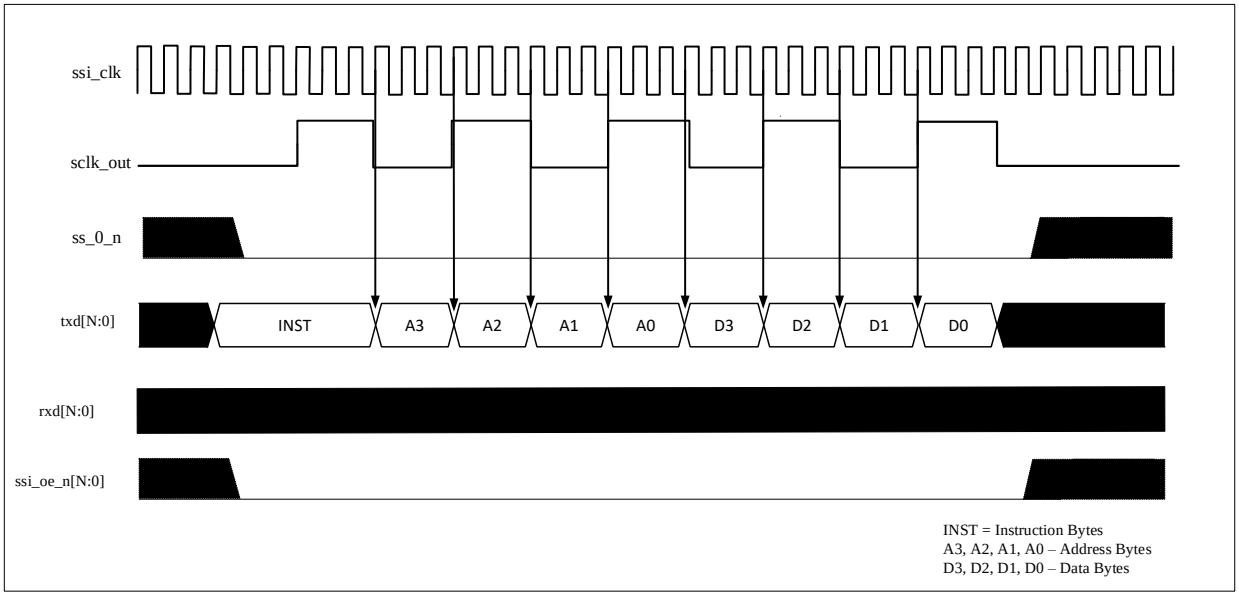
NOTE: In the DDR transfer, address and instruction cannot be programmed to a value of 0. The number of wait cycles cannot be 0 in a DDR read operation.

In DDR mode, data is transmitted on both edges so that it is difficult to sample data correctly. XSPI uses an internal register to determine the edge on which the data should be transmitted. This ensures that the receiver is able to get a stable data while sampling. The internal register (XSPI_DDR_TXDE) determines the edge on which the data is transmitted. XSPI sends data with respect to baud clock, which is an integral multiple of the internal clock (ssi_clk * BAUDR). The data needs to be transmitted within half clock cycle (BAUDR/2), therefore the maximum value for XSPI_DDR_TXDE register is equal to [(BAUDR/2)-1].

- XSPI_DDR_TXDE=0

Figure 37-20 DDR transfer while XSPI_DDR_TXDE=0



- XSPI_DDR_TXDE=1

Figure 37-21 DDR transfer while XSPI_DDR_TXDE=1

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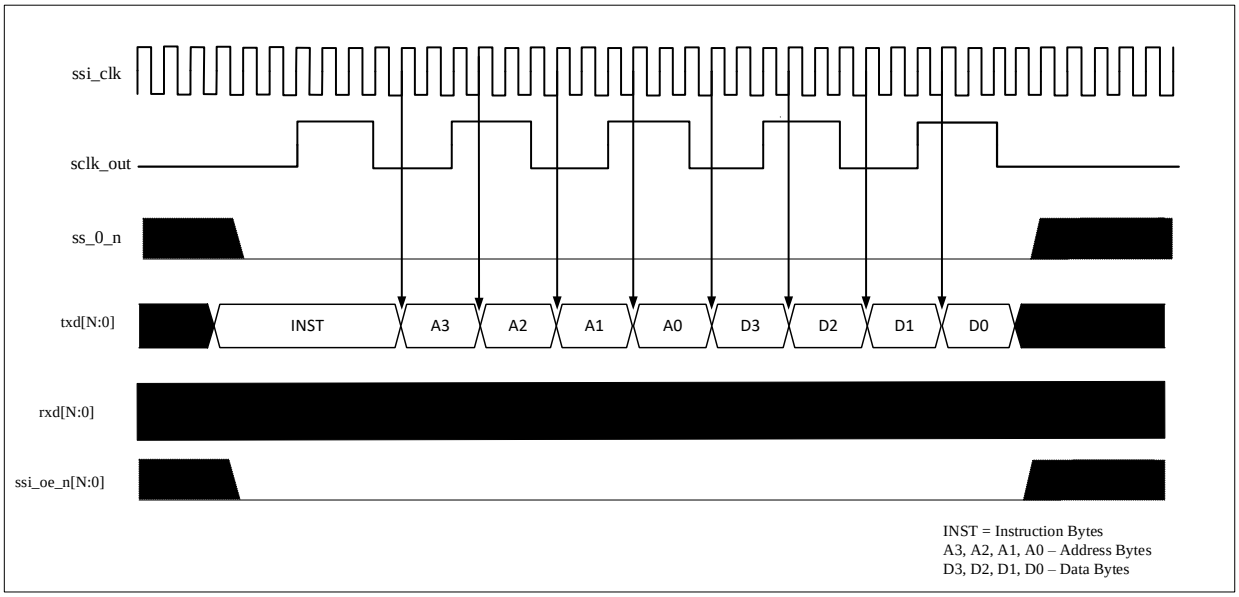

37.4.12 Hyperbus protocol support

HyperBus is an interface that supports both parallel and serial interface memories, while enhancing system performance, ease of design, and system cost reduction. A read or write transaction on a HyperBus interface consists of a sequential series of 16-bit, one-clock cycle, data transfers through two corresponding 8-bit width, one-half-clock cycle data transfers, one on each single-ended clock edge or differential clock crossing.

XSPI supports the Hyperbus protocol that works on the principle of the SPI DDR interface. The DDR protocol transfers two data bytes per clock cycle on the input/output (I/O) signals. You can enable the Hyperbus feature in XSPI using the XSPI_CTRL0.SPIHYPEEN configuration parameter.

The Hyperbus uses 48-bit command-address (CA) to convey the instruction and address information.

Table 37-1 Hyperbus CA format

CA Bit	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. ■ 1 – Indicates Read transaction. ■ 0 – Indicates a Write Transaction.
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. ■ 0 – Indicates memory space. ■ 1 – Indicates the register space. The register space is used to the access device ID and configuration registers.

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45	Burst Type	Indicates whether the burst is linear or wrapped. ■ 0 – Indicates a wrapped burst. ■ 1 – Indicates a linear burst.
44-16	Row & Upper Column Address	Row and Upper Column component of the target address: System word address bits A31-A3 If a particular device density does not use upper Row address bits, the Host controller master interface must set it to 0. The size of Rows and therefore the address bit boundary between Row and Column address is dependent on the slave device.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are do not care in current HyperBus devices but the Host controller must be set it to for future compatibility.
2-0	Lower Column address	Lower Column component of the target address: System word address bits A2-0 selecting the starting word within a half-page.

When the Hyperbus feature is enabled (XSPI_CTRL0.SPIHYPEEN=1) in XSPI, the XSPI_CTRL0. SPIHYPEEN register bit is set to program XSPI as a Hyperbus master. As the Hyperbus interface has a fixed frame format, the following fields are fixed when XSPI is programmed into Hyperbus mode:

- XSPI_CTRL0.SPIFRF – 2'b11 (Octal Frame format)
- XSPI_ENH_CTRL0.TRANSTYPE – 2'b10 (Address to be sent in Octal format)
- XSPI_ENH_CTRL0.ADDRLEN – 4'b1100 (Address length of 48 bits)
- XSPI_ENH_CTRL0.INSTL – 2'b00 (No Instruction phase)
- XSPI_ENH_CTRL0.WRSPIDDREN – 1 (Address to be sent on Octal-DDR format)
- XSPI_ENH_CTRL0.SPIRXDSEN – 1 (Enable read data strobe to sample incoming data)

You can configure Wait cycles using the XSPI_ENH_CTRL0.WAITCYCLES field, depending on memory requirement. As the Hyperbus protocol counts the Wait cycles from the third CA cycle, XSPI sends XSPI_ENH_CTRL0.WAITCYCLES - 1 wait cycles after the CA phase is complete. The remaining fields in the XSPI_ENH_CTRL0 register are not used for a Hyperbus transfer.

You can set the type of transaction (read/write) and data frame size in XSPI_CTRL0.TMOD and XSPI_CTRL0.DFS fields, respectively. The read back value of fixed fields is same as the register value but internally the hardware ignores those when XSPI_CTRL0. SPIHYPEEN bit is set to 1.

37.4.12.1 Read transaction

The HyperBus master begins a transaction by driving the ss_x_n signal to Low while the clock is idle. Then, the clock starts toggling while CA words are transferred. The HyperBus master then continues clocking for a number of

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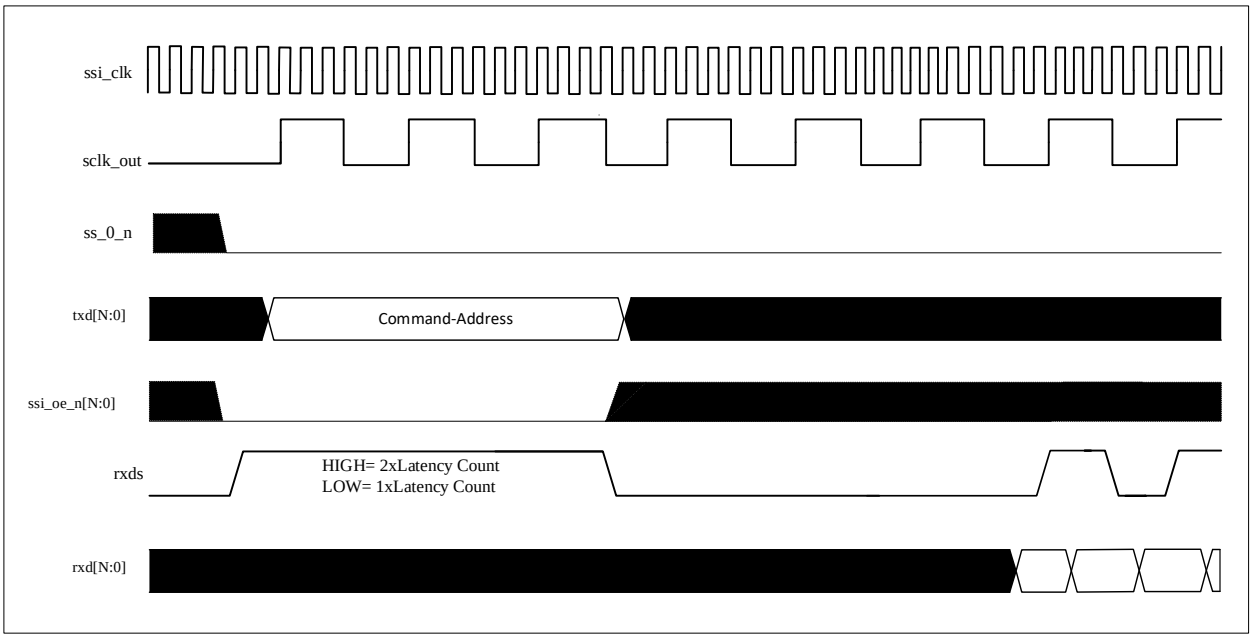
cycles defined by the latency count setting in a configuration register. If the Read-Write Data Strobe (RWDS) is low during the CA cycles, one latency count is inserted. If RWDS is high during the CA cycles, an additional latency count is inserted. After these latency clocks are completed, the memory transitions the RWDS and outputs the target data.

Figure 37-22 Hyperbus Read command



37.4.12.2 Write transaction

The HyperBus master begins a transaction by driving the ss_x_n signal to Low while the clock is idle. Then, the clock starts toggling while CA words are transferred. Further, the Hyperbus master continues clocking for a number of cycles defined by the latency count setting in a configuration register. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is high during the CA cycles, an additional latency count is inserted. After these latency clocks are completed, the Hyperbus master starts to output the target data. The Write data is center aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of sclk_out signal and the second byte is captured on the falling edge of sclk_out signal. The latency count can also be zero for a write transaction that is device dependent.

Figure 37-23 Hyperbus Write command

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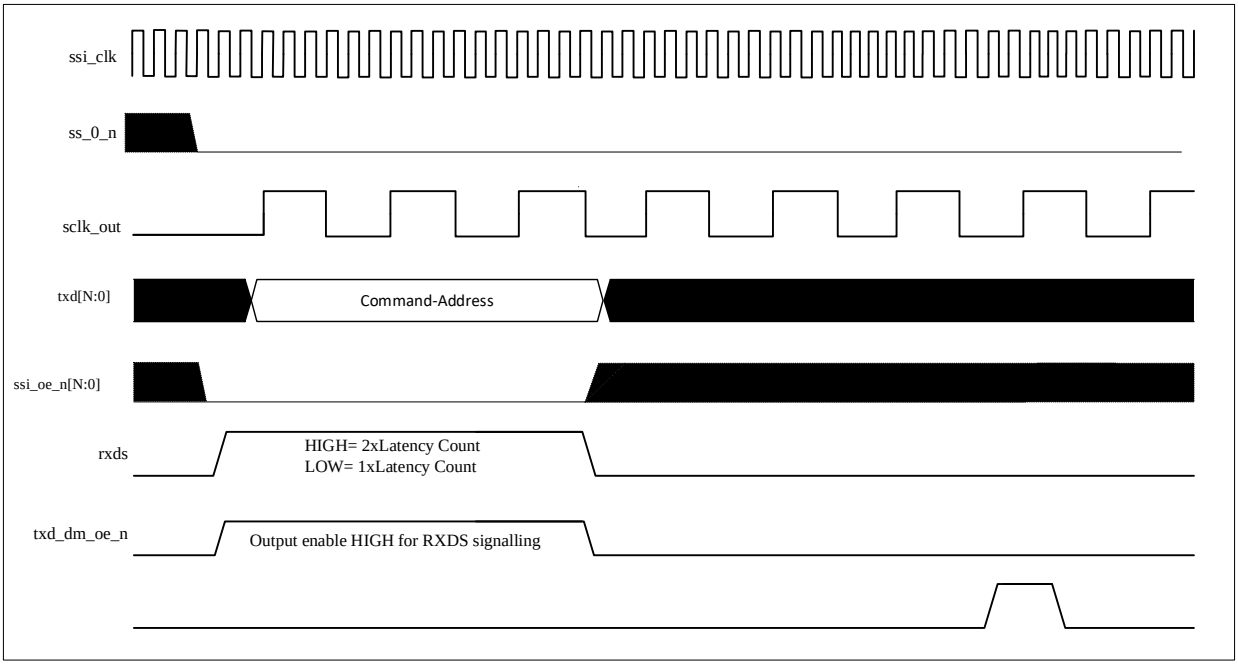

37.4.13 eXecute in Place (XIP) mode

NOTE: N32xxx, XSPI only support XIP READ.

XSPI provides a function to directly perform memory read operation from AHB transaction. This is called execute in place mode, in which XSPI acts as memory mapped interface to an SPI memory.

XIP operations are supported in only in Dual, Quad, or Octal enhanced SPI modes of operation, and so, the XSPI_CTRL0.SPIFRF bit must not be programmed to zero. Typically, an XIP operation consists of an address phase and a data phase.

When XSPI_XIP_CTRL field of the DFSHC register is set to zero, AHB control signals are used to derive the values of the data frame size and the number of data frames to be fetched by the device. hsize signal is used to get the value of data frame size for the transfer. Table 37-2 shows the data frame size mapping from the HSIZE value.

Table 37-2 HSIZE to Data Frame Size Decode

HSIZE	Data frame Size (DFS)
3’b000	8
3’b001	16
>=3’b010	32

The number of data frames to be fetched is derived from the HBURST signal. Table 37-3 shows the decode for the number for data frames decoded from the HBURST value.

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Table 37-3 HBURST to Number of Data Frames (XSPI_XIP_CTRL.DFSHC=0)

HBURST	Type	Number of Data Frames (NDF)
000	Single	1
001	INCR	Data is fetched until the burst completes
010	WRAP4	4
011	INCR4	4
100	WRAP8	8
101	INCR8	8
110	WRAP16	16
111	INCR16	16

NOTE: XSPI_XIP_CTRL field of the DFSHC register should to be set as one for XIP READ to ensure correct read behavior as explained in Big-Little endian section.

37.4.13.1 XIP transfer

Once the XSPI_CTRL0 and XSPI_ENH_CTRL0 registers are programmed with correct values for transfer, and then XIP transfer can be initiated by driving the xip_en signal to 1 and by performing a read operation on the AHB bus.

There are two types for AHB transfers that are handled differently by XSPI. The following sections describe the behavior of XSPI for each AHB transfer.

- Case A: Fixed INCR/WRAP Burst Transfer

  When XSPI receives a FIXED burst request, it fetches only fixed amount of data from SPI device. The number of data frames (NDF) field is determined by HBURST and data frame size is derived from the hsize signal. For the WRAP request, the device must send the correct data and XSPI forwards the data on the AHB interface.

- Case B: Undefined Incrementing Burst (INCR)

  In this case, XSPI continues to fetch the data from the device unless end of burst (IDLE transfer) is detected on slave interface. XSPI fetches s maximum of 1 KB data from SPI device for this transfer type.

37.4.13.2 AHB wait transfer

During XIP transfers, AHB master may insert wait states in the transfer. In this condition, XSPI does not break the transfer on SPI interface and continues to fetch the data from SPI slave until all the required data frames are fetched for the ongoing burst. This intermediate data is stored in XSPI receive FIFO and is transmitted to AHB interface after WAIT cycles are completed.

37.4.13.3 Early Burst Termination

Early burst termination (EBT) can occur in an ongoing AHB transfer. When IDLE transfer is detected on AHB

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interface, XSPI gracefully completes the ongoing transfer on the SPI line, and returns the last fetched data to the AHB device. AHB master can resume the burst from the last address and XSPI treats it as a new transfer and again transmit address to the SPI slave.

NOTE: XSPI does not support early burst termination while AHB Master is BUSY, in the XIP mode

37.4.13.4 Mode bits support

During a serial transfer, certain devices have the capability to send additional bits that are referred to as Mode bits. The mode bits setting as followings:

- XSPI_XIP_CTRL.MDBITSEN–enable mode bit.
- XSPI_XIP_CTRL.XIPMBL–set mode bits length.
- XSPI_XIP_MODE. XIPMDBITS-set mode bits value

Mode bits occur immediately after the address phase is completed and follow the same rules as for the address bits. Therefore, serial transfers consist of following phases when mode bit support is enabled:

Instruction Phase > Address Phase > Mode Bits > Wait cycles > Data Phase

NOTE: need software intervention to skip instruction phase in subsequent read commands after first XIP READ by setting XSPI_XIP_CTRL.XIPINSTEN=0.

37.4.14 Continuous transfer in XIP

When XSPI receives an XIP request, address from the AHB interface is transmitted onto the SPI interface directly. Each new transfer (XIP Read) on the AHB interface is treated in the same manner. Therefore, for every request, a new address must be sent to the device thereby contributing to the latency of the system. If a memory device allows the stretching of slave select signal in between the XIP read transfers, then XSPI can be programmed for continuous XIP mode to achieve higher performance. In this mode, the host fuses two or more AHB burst requests into a single SPI command by ensuring that the command and address are not retransmitted and the host controller need not wait for any dummy cycles in between these bursts.

XSPI can be enabled for continuous XIP mode by programming the XSPI_XIP_CTRL. XIPCTEN bit to one. When this bit is set to one, then XSPI functions in continuous XIP mode as soon as first XIP command is received. For the first XIP transfer, the address (and instruction if XSPI_XIP_CTR. XIPINSTEN = 1) is sent on the SPI interface. After reception of requested data, XSPI continues to keep the slave selected and the clock (sclk_out) remains in the default state. For subsequent XIP transfers on the AHB interface, XSPI resumes the clock (sclk_out) and neither the command nor the address is transmitted onto the SPI interface and the data to be fetched from the device immediately (no dummy cycles).

XSPI moves out of the continuous mode due to either of the following conditions:

- A non-XIP command is received on an XIP interface (effectively any AHB transaction with xip_en driven to 0).
- When the AHB transaction is to a non-consecutive address, the slave select is removed and then XSPI initiates a new XIP request.

NOTE: In continuous transfer mode, if XSPI_XIP_CTRL.DFSHC is set to one then the XIP address must always be aligned with the DFS value programmed in the XSPI_CTRL0.DFS bit.

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Continuous Incremental Transfer

A transfer is defined as continuous incremental when the first command received in the continuous XIP (XSPI_XIP_CTRL.XIPCTEN = 1) mode is INCR (hburst = 011/101/111). In this mode, when the transfer is completed, the next command must also be incremental, and the address must be a contiguous address of the last burst.

Continuous WRAP Transfer

A transfer is defined as continuous WRAP when the first command received in continuous XIP mode is WRAP (hburst = 010/100/110). In this mode, when the transfer is completed, the next command must start from the address of last-burst address boundary.

37.4.15 Data prefetch in XIP

For each XIP request on the AHB interface, XSPI sends instruction (if XSPI_XIP_CTRL.XIPINSTEN = 1) and address to the end device. The device responds with the data after some time, which is then sent to the AHB interface. In order to read a big chunk of data from the slave, which is divided into multiple bursts, each of them takes the same amount of time to complete. Since XSPI needs to send the address and data for each request, the controller must wait until the instruction and address phase is completed before getting the data.

Using the data pre-fetch feature in XSPI, the controller pre-fetches the data for the successive burst during the current XIP transaction. If the next transaction request is made to the successive address, the data can be read directly from the RX FIFO instead of waiting for a new address and data to be sent to the device. This improves the overall performance of the system

The amount of the data to be pre-fetched should be equal to the burst length of the last AHB request or the FIFO depth (whichever is lower).

NOTE: The HSIZE should be kept constant for all transfers in the Prefetch mode.

Case A: Transfer Request for the Contiguous Address

In this case, XSPI returns the number of beats available in the FIFO, and then fetches the rest of the beats to complete the current transfer. After the current transfer is complete, XSPI extends the same transfer to pre-fetch the data for the next transfer.

Case B: Transfer Request for the Non-Contiguous Address

In this case, the current serial transfer ends gracefully, receive FIFO gets flushed and a new serial transfer is initiated on serial lane to complete the current request.

NOTE: If XIP pre-fetching is enabled, AHB request for incremental transfer of undefined length (hburst = 3'b001) is not allowed.

37.4.16 DMA controller interface

The XSPI uses the following handshaking signals to interface with the DMA controller.

- dma_tx_req
- dma_rx_req

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- dma_tx_ack
- dma_rx_ack
- dma_tx_single
- dma_rx_single

To enable the DMA Controller interface on the XSPI, you must write the DMA Control Register (XSPI_DMA_CTRL). Writing one into the TXDMAEN bit field of XSPI_DMA_CTRL register enables the XSPI transmit handshaking interface. Writing a one into the RXDMAEN bit field of the XSPI_DMA_CTRL register enables the XSPI receive handshaking interface.

Transmit Watermark Level and Transmit FIFO Underflow:

During XSPI serial transfers, transmit FIFO requests are made to the DW_ahb_dmac whenever the number of entries in the transmit FIFO is less than or equal to the DMA Transmit Data Level Register (XSPI_DMATDL_CTRL) value; this is known as the watermark level. The DW_ahb_dmac responds by writing a burst of data to the transmit FIFO buffer, of length CTLx.DEST_MSIZE. Data should be fetched from the DMA often enough for the transmit FIFO to perform serial transfers continuously; that is, when the FIFO begins to empty another DMA request should be triggered. Otherwise, the FIFO runs out of data (underflow). To prevent this condition, you must set the watermark level correctly.

Receive Watermark Level and Receive FIFO Overflow

During XSPI serial transfers, receive FIFO requests are made to the DW_ahb_dmac whenever the number of entries in the receive FIFO is at or above the DMA Receive Data Level Register; that is, XSPI_DMARDL_CTRL+1. This is known as the watermark level. The DW_ahb_dmac responds by fetching a burst of data from the receive FIFO buffer of length CTLx.SRC_MSIZE.

Data should be fetched by the DMA often enough for the receive FIFO to accept serial transfers continuously; that is, when the FIFO begins to fill, another DMA transfer is requested. Otherwise, the FIFO l fills with data (overflow). To prevent this condition, you must correctly set the watermark level.

Two things to keep in mind:

- The burst request lines, dma_tx_req signal/dma_rx_req, once asserted remain asserted until their corresponding dma_tx_ack/dma_rx_ack signal is received even if the respective FIFO's drop below their watermark levels during the burst transaction.
- The dma_tx_req/dma_rx_req signals are de-asserted when their corresponding dma_tx_ack/dma_rx_ack signals are asserted, even if the respective FIFOs exceed their watermark levels.

dma_tx_single, dma_rx_single

- The dma_tx_single signal is asserted when there is at least one free entry in the transmit FIFO, and is cleared when the dma_tx_ack signal is active. The dma_tx_single signal is re-asserted when the dma_tx_ack signal is de-asserted, if the condition for setting still holds true.
- The dma_rx_single signal is asserted when there is at least one valid data entry in the receive FIFO, and is cleared when the dma_rx_ack signal is active. The dma_rx_single signal is re-asserted when the dma_rx_ack signal is de-asserted, if the condition for setting still holds true.

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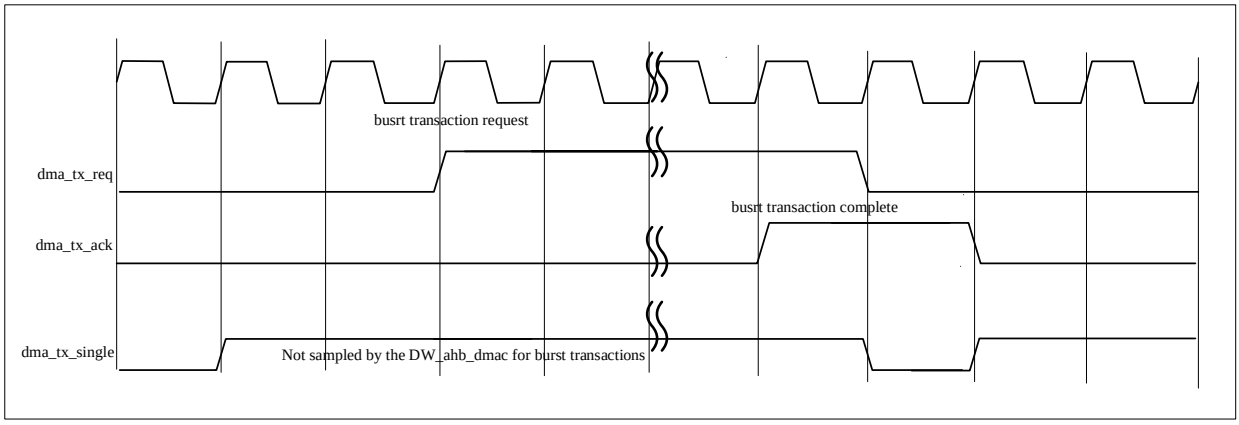
Figure 37-24 DMA handshaking



37.4.17 Error responses

XSPI provides an error response on the programming interface when any of the following conditions are met:

- Invalid Read or Write access on configuration registers
- If transmit FIFO is full, and a write operation is attempted in the Data Register (XSPI_DATx)
- If receive FIFO is empty, and a read operation is attempted in the Data Register (XSPI_DATx)
- If read or write operation is attempted in the Data Register when XSPI is not enabled (XSPI_EN register set to 0)
- Under XIP operation (xip_en == 1) the following conditions result in error response:
  - If SSIC_XIP_WRITE_EN parameter is set to 0, and any write operation occurs
  - If an XIP read operation is attempted while another master is active on the SPI bus (Master contention)
  - If XSPI is disabled and XIP transaction is attempted
  - If XIP transfer is attempted and the transmit FIFO is not empty
  - The Transmit FIFO underflow interrupt is set and XIP write transfer is attempted

37.5 Registers

37.5.1 xSPI Control Register 0 (XSPI_CTRL0)

This register controls the serial data transfer. It is impossible to write to this register when the DWC_ssi is enabled

Address offset: 0x0000

Reset value: 0x80804407

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MST	Reserved					DWSEN	SPIHYPEEN	SPIFRF[1:0]		Reserved		CFS[3:0]			

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rw						r	r	rw						rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SSTE	SRL	SLVOE	TMOD[1:0]		SCPOL	SCPH	FRF[1:0]		Reserved	DFS[4:0]				
	rw	rw	rw	rw		rw	rw	rw			rw				

Bit field	Name	Description
31	MST	This field selects if xspi is working in Master or Slave mode Values: • 0x1 (MASTER): xspi is Master • 0x0 (SLAVE): xspi is Slave because we only used Master mode，so it's read only as zero（reserved
30:26	Reserved	Reserved, the reset value must be maintained.
25	DWSEN	Enable Dynamic wait states in SPI mode of operation. This field is only applicable when XSPI_CTRL0.FRF is set to 0 (Motorola SPI Frame Format). Values: • 0x0 (DISABLE): Disable SPI Dynamic Wait State • 0x1 (ENABLE): Enable SPI Dynamic Wait State
24	SPIHYPEEN	SPI Hyperbus Frame format enable. Selects if data frame format for Transmitting/Receiving the data is in Hyperbus mode. This field is effective only when XSPI_CTRL0.FRF is set to SPI frame format. Values: • 0x0 (DISABLE): Disable Hyperbus Format • 0x1 (ENABLE): Enable Hyperbus Format
23:22	SPIFRF[1:0]	SPI Frame Format Selects data frame format for Transmitting/Receiving the data. Bits only valid when SSIC_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode. Values: • 0x0 (SPI_STANDARD): Standard SPI Format • 0x1 (SPI_DUAL): Dual SPI Format • 0x2 (SPI_QUAD): Quad SPI Format • 0x3 (SPI_OCTAL): Octal SPI Format
21:20	Reserved	Reserved, the reset value must be maintained.
19:16	CFS[3:0]	Control Frame Size. Selects the length of the control word for the Microwire frame format. Values: • 0x0 (SIZE_01_BIT): 01-bit Control Word • 0x1 (SIZE_02_BIT): 02-bit Control Word • 0x2 (SIZE_03_BIT): 03-bit Control Word • 0x3 (SIZE_04_BIT): 04-bit Control Word • 0x4 (SIZE_05_BIT): 05-bit Control Word • 0x5 (SIZE_06_BIT): 06-bit Control Word

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Bit field	Name	Description
		• 0x6 (SIZE_07_BIT): 07-bit Control Word • 0x7 (SIZE_08_BIT): 08-bit Control Word • 0x8 (SIZE_09_BIT): 09-bit Control Word • 0x9 (SIZE_10_BIT): 10-bit Control Word • 0xa (SIZE_11_BIT): 11-bit Control Word • 0xb (SIZE_12_BIT): 12-bit Control Word • 0xc (SIZE_13_BIT): 13-bit Control Word • 0xd (SIZE_14_BIT): 14-bit Control Word • 0xe (SIZE_15_BIT): 15-bit Control Word • 0xf (SIZE_16_BIT): 16-bit Control Word
15	Reserved	Reserved, the reset value must be maintained.
14	SSTE	Slave Select Toggle Enable. While operating in SPI mode with clock phase (XSPI_CTRL0.SCPH) set to 0, this register controls the behavior of the slave select line (NSS) between data frames Values: • 0x1 (TOGGLE_EN): NSS line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while NSS is high • 0x0 (TOGGLE_DISABLE): NSS will stay low and sclk will run continuously for the duration of the transfer
13	SRL	Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the xSPI is configured as a slave in loopback mode, the NSS and sclk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back. Values: • 0x1 (TESTING_MODE): Test Mode Operation • 0x0 (NORMAL_MODE): Normal mode operation
12	SLVOE	Slave Output Enable. Relevant only when the xSPI is configured as a serial-slave device. When configured as a serial master, this bit field has no functionality. This bit enables or disables the setting of the xspi_oe_n output from the xSPI serial slave. When SLVOE = 1, the xspi_oe_n output can never be active. When the xspi_oe_n output controls the tri-state buffer on the txd output from the slave, a high impedance state is always present on the slave txd output when SLVOE = 1. This is useful when the master transmits in broadcast mode (master transmits data to all slave devices). Only one slave may respond with data on the master rxd line. This bit is enabled after reset and must be disabled by software (when broadcast mode is used), if you do not want this device to respond with data. When XSPI_SLV_SPI_MODE is set to 1 and SPI is programmed to work in Enhanced SPI mode, then for correct operation this bit should be programmed to 0. Values:

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Bit field	Name	Description
		• 0x1 (DISABLED): Slave Output is disabled • 0x0 (ENABLED): Slave Output is enabled
11:10	TMOD[1:0]	Transfer Mode. Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. Values: • 0x0 (TX_AND_RX): Transmit & Receive; Not Applicable in enhanced SPI operating mode or when SSIC_HAS_TX_RX_EN is set to 0 • 0x1 (TX_ONLY): Transmit only mode; Or Write in enhanced SPI operating mode • 0x2 (RX_ONLY): Receive only mode; Or Read in enhanced SPI operating mode • 0x3 (EEPROM_READ): EEPROM Read mode; Not Applicable in enhanced SPI operating mode
9	SCPOL	Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the xSPI master is not actively transferring data on the serial bus. Values: • 0x0 (INACTIVE_HIGH): Inactive state of serial clock is low • 0x1 (INACTIVE_LOW): Inactive state of serial clock is high
8	SCPH	Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock. Values: • 0x1 (START_BIT): Serial clock toggles at start of first bit • 0x0 (MIDDLE_BIT): Serial clock toggles in middle of first bit
7:6	FRF[1:0]	Frame Format. Selects which serial protocol transfers the data. Values: • 0x0 (SPI): Motorola SPI Frame Format • 0x1 (SSP): Texas Instruments SSP Frame Format • 0x2 (MICROWIRE): National Semiconductors Microwire Frame Format • 0x3 (RESERVED): Reserved

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Bit field	Name	Description
5	Reserved	Reserved, the reset value must be maintained.
4:0	DFS[4:0]	Data Frame Size. Selects the data frame length. When the data frame size is programmed to be less than 32 bits, the receive data is automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. Note: When SSIC_SPI_MODE is set to "Dual", "Quad" or "Octal" mode and SPI_FRF is not set to 2'b00: • DFS value must be a multiple of 2 if SPI_FRF = 01 • DFS value must be multiple of 4 if SPI_FRF = 10 • DFS value must be multiple of 8 if SPI_FRF = 11 Values: • 0x0 (DFS_01_BIT): Reserved • 0x1 (DFS_02_BIT): Reserved • 0x2 (DFS_03_BIT): Reserved • 0x3 (DFS_04_BIT): 04-bit serial data transfer • 0x4 (DFS_05_BIT): 05-bit serial data transfer • 0x5 (DFS_06_BIT): 06-bit serial data transfer • 0x6 (DFS_07_BIT): 07-bit serial data transfer • 0x7 (DFS_08_BIT): 08-bit serial data transfer • 0x8 (DFS_09_BIT): 09-bit serial data transfer • 0x9 (DFS_10_BIT): 10-bit serial data transfer • 0xa (DFS_11_BIT): 11-bit serial data transfer • 0xb (DFS_12_BIT): 12-bit serial data transfer • 0xc (DFS_13_BIT): 13-bit serial data transfer • 0xd (DFS_14_BIT): 14-bit serial data transfer • 0xe (DFS_15_BIT): 15-bit serial data transfer • 0xf (DFS_16_BIT): 16-bit serial data transfer • 0x10 (DFS_17_BIT): 17-bit serial data transfer • 0x11 (DFS_18_BIT): 18-bit serial data transfer • 0x12 (DFS_19_BIT): 19-bit serial data transfer • 0x13 (DFS_20_BIT): 20-bit serial data transfer • 0x14 (DFS_21_BIT): 21-bit serial data transfer • 0x15 (DFS_22_BIT): 22-bit serial data transfer • 0x16 (DFS_23_BIT): 23-bit serial data transfer • 0x17 (DFS_24_BIT): 24-bit serial data transfer • 0x18 (DFS_25_BIT): 25-bit serial data transfer • 0x19 (DFS_26_BIT): 26-bit serial data transfer • 0x1a (DFS_27_BIT): 27-bit serial data transfer • 0x1b (DFS_28_BIT): 28-bit serial data transfer • 0x1c (DFS_29_BIT): 29-bit serial data transfer

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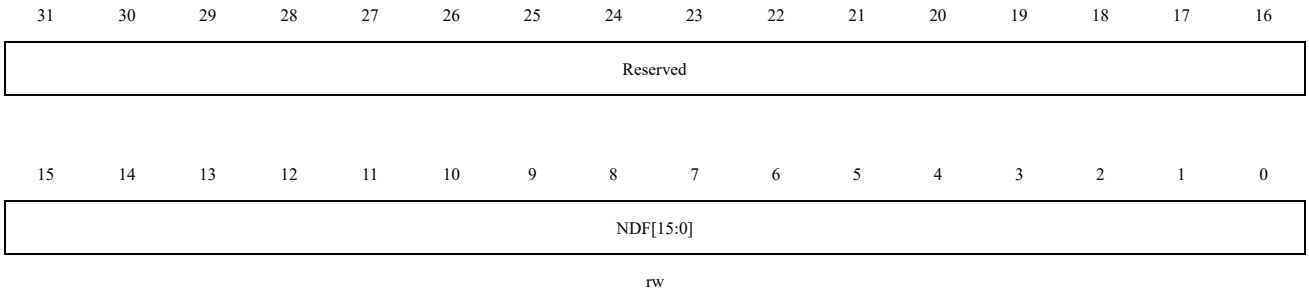
Bit field	Name	Description
		• 0x1d (DFS_30_BIT): 30-bit serial data transfer • 0x1e (DFS_31_BIT): 31-bit serial data transfer • 0x1f (DFS_32_BIT): 32-bit serial data transfer

37.5.2 xSPI Control Register 1 (XSPI_CTRL1)

This register exists only when the xSPI is configured as a master device. When the xSPI is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the xSPI is enabled.

Address offset: 0x0004

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	NDF[15:0]	Number of Data Frames. When xSPI_CTRL0.TMOD[1:0] = 10 or xSPI_CTRL0.TMOD = 11, this register field sets the number of data frames to be continuously received by the xSPI. The xSPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer. When xSPI_ENH_CTRL0.CLKSTREN=1 and xSPI_CTRL0.TMOD[1:0] = 01, this register field sets the number of data frames to be continously transmitted by xSPI. If the Transmit FIFO goes empty in-between, xSPI masks the serial clock (sclk_out) and wait for rest of the data until the programmed amount of frames are transferred successfully. When the xSPI is configured as a serial slave, the transfer continues for as long as the slave is selected. Therefore, this register serves no purpose and is not present when the xSPI is configured as a serial slave.

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37.5.3 xSPI Enable Register (XSPI_EN)

This register enables and disables the xSPI.

Address offset: 0x0008

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															XSPIEN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	XSPIEN	xSPI Enable. Enables and disables all xSPI operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the xSPI control registers when enabled. When disabled, the spi sleep output is set (after delay) to inform the system that it is safe to remove the sclk, thus saving power consumption in the system. Values: • 0x1 (ENABLED): Enables xSPI • 0x0 (DISABLE): Disables xSPI

37.5.4 Microwire Control Register (XSPI_MW_CTRL)

This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the xSPI is enabled.

Address offset: 0x000C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													MHSEN	MCDIR	MWMOD
													rw	rw	rw

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Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	MHSEN	Microwire Handshaking. Relevant only when the xSPI is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the xSPI checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register. Values: • 0x1 (ENABLED): handshaking interface is enabled • 0x0 (DISABLE): handshaking interface is disabled
1	MCDIR	Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the xSPI MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the xSPI MacroCell to the external serial device. Values: • 0x1 (TRANSMIT): SPI transmits data • 0x0 (RECEIVE): SPI receives data
0	MWMOD	Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received. Values: • 0x1 (SEQUENTIAL): Sequential Transfer • 0x0 (NON_SEQUENTIAL): Non-Sequential Transfer

37.5.5 Slave Enable Register (XSPI_SLAVE_EN)

This register is valid only when the xSPI is configured as a master device. When the xSPI is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the xSPI master. Up to 16 slave-select output pins are available on the xSPI master. You cannot write to this register when xSPI is busy and when XSPI_EN.XSPIEN = 1.

Address offset: 0x0010

Reset value: 0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												SEN[3:0]			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	SEN[3:0]	Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (nss) from the xSPI master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

37.5.6 Baud Rate Select Register (XSPI_BAUD)

This register is valid only when the xSPI is configured as a master device. When the xSPI is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the sclk divider value. It is impossible to write to this register when the xSPI is enabled.

Address offset: 0x0014

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKDIV[14:0]															Reserved
rw															

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
15:1	CLKDIV[14:0]	SPI Clock Divider. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/BAUDR

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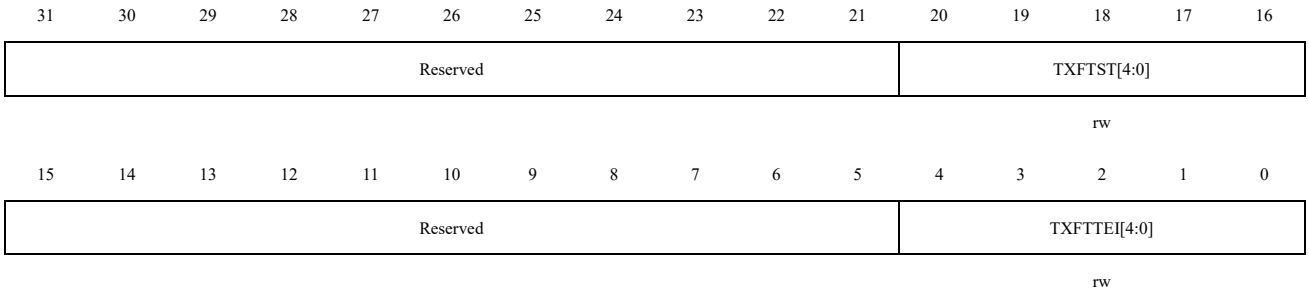
Bit field	Name	Description
		where BAUDR is any even value between 2 and 65534 (BAUDR = { CLKDIV [14:0] *2}). For example: for Fspi_clk = 3.6864MHz and BAUDR =2 Fsclk_out = 3.6864/2 = 1.8432MHz
0	Reserved	Reserved, the reset value must be maintained.

37.5.7 Transmit FIFO Threshold Level (XSPI_TXFT)

This register controls the threshold value for the transmit FIFO memory.

Address offset: 0x0018

Reset value: 0x0000 0000



Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:16	TXFTST[4:0]	Transfer start FIFO level. Used to control the level of entries in transmit FIFO above which transfer will start on serial line. This register can be used to ensure that sufficient data is present in transmit FIFO before starting a write operation on serial line. In Internal DMA mode, this field sets the minimum amount of data frames present in the FIFO after which xSPI starts the transfer. This field is valid only for Master mode of operation
15:5	Reserved	Reserved, the reset value must be maintained.
4:0	TXFTTEI[4:0]	Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 8-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

37.5.8 Receive FIFO Threshold Level (XSPI_RXFT)

This register controls the threshold value for the receive FIFO memory.

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Address offset: 0x001C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											RXFTTFI[4:0]				
											rw				

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4:0	RXFTTFI[4:0]	Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 8-256. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered

37.5.9 Transmit FIFO Level Register (XSPI_TXFN)

This register contains the number of valid data entries in the transmit FIFO memory.

Address offset: 0x0020

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											TXFN[5:0]				
											r				

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	TXFN[5:0]	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO

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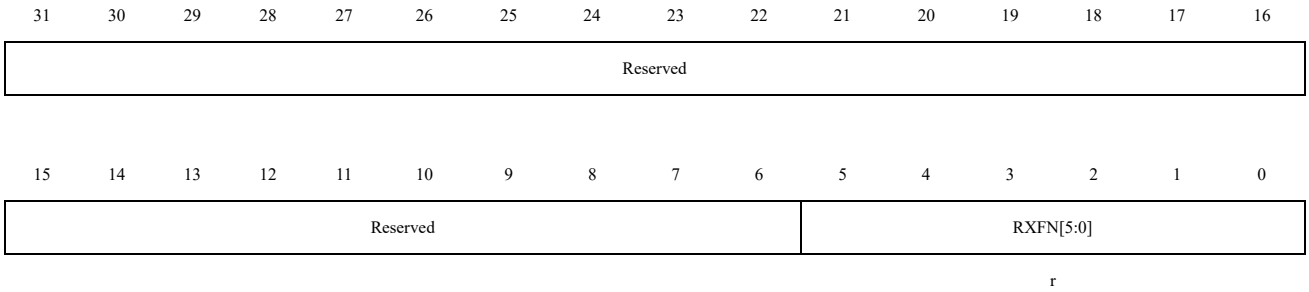
37.5.10 Receive FIFO Level Register (XSPI_RXFN)

This register contains the number of valid data entries in the receive FIFO memory.

Address offset: 0x0024

Reset value: 0x0000 0000



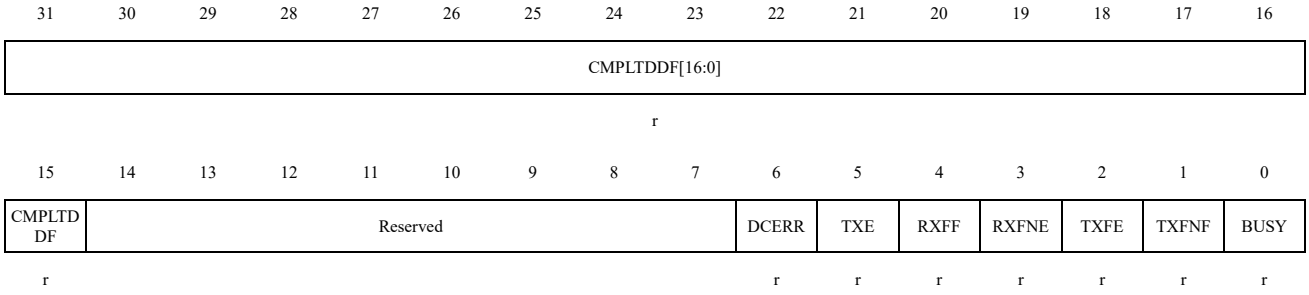
Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	RXFN[5:0]	receive FIFO Level. Contains the number of valid data entries in the receive FIFO

37.5.11 Status Register (XSPI_STS)

This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt.

Address offset: 0x0028

Reset value: 0x0000 0006



Bit field	Name	Description
31:15	CMPLTDDF[16:0]	Completed Data frames This field indicates total data frames transferred in the previous internal DMA transfer
14:7	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
6	DCERR	Data Collision Error. Relevant only when the xSPI is configured as a master device. This bit will be set if input is asserted by other master, when the xSPI master is in the middle of the transfer. This informs the processor that the last data transfer was halted before completion. This bit is cleared when read Values: • 0x1 (TX_COLLISION_ERROR): Transmit Data Collision Error • 0x0 (NO_ERROR_CONDITION): No Error
5	TXE	Transmission Error. Set if the transmit FIFO is empty when a transfer is started. This bit can be set only when the xSPI is configured as a slave device. Data from the previous transmission is resent on the txd line. This bit is cleared when read. Values: • 0x1 (TX_ERROR): Transmission Error • 0x0 (NO_ERROR): No Error
4	RXFF	Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. Values: • 0x1 (FULL): Receive FIFO is full • 0x0 (NOT_FULL): Receive FIFO is not full
3	RXFNE	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO. Values: • 0x1 (NOT_EMPTY): Receive FIFO is not empty • 0x0 (EMPTY): Receive FIFO is empty
2	TXFE	Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. Values: • 0x1 (EMPTY): Transmit FIFO is empty • 0x0 (NOT_EMPTY): Transmit FIFO is not empty
1	TXFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. Values: • 0x1 (NOT_FULL): Tx FIFO is not Full • 0x0 (FULL): Tx FIFO is full
0	BUSY	SPI Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the

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Bit field	Name	Description
		xSPI is idle or disabled. Values: • 0x1 (ACTIVE): xSPI is actively transferring data • 0x0 (INACTIVE): xSPI is idle or disabled

37.5.12 Interrupt Mask Register (XSPI_IMASK)

This read/write register masks or enables all interrupts generated by the xSPI. When the xSPI is configured as a slave device, the MSTIM bit field is not present. This changes the reset value from 0x3F for serial-master configurations to 0x1F for serial-slave configurations.

Address offset: 0x002C

Reset value: 0x0000 00FE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DONEM	SPITEM	Reserved	AXIEM	TXUIM	XRXOIM	MSTIM	RXFIM	RXOIM	RXUIM	TXOIM	TXEIM
				r	r		r	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	DONEM	SPI Done Interrupt Mask Values: • 0x1 (UNMASKED): spi_done_intr interrupt is not masked • 0x0 (MASKED): spi_done_intr interrupt is masked
10	SPITEM	SPI Transmit Error Interrupt Mask Values: • 0x1 (UNMASKED): spi_spite_intr interrupt is not masked • 0x0 (MASKED): spi_spite_intr interrupt is masked
9	Reserved	Reserved, the reset value must be maintained.
8	AXIEM	AXI Error Interrupt Mask Values: • 0x1 (UNMASKED): spi_axie_intr interrupt is not masked • 0x0 (MASKED): spi_axie_intr interrupt is masked
7	TXUIM	Transmit FIFO Underflow Interrupt Mask Values: • 0x1 (UNMASKED): spi_txu_intr interrupt is not masked • 0x0 (MASKED): spi_txu_intr interrupt is masked

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Bit field	Name	Description
6	XRXOIM	XIP Receive FIFO Overflow Interrupt Mask Values: • 0x1 (UNMASKED): spi_xrxo_intr interrupt is not masked • 0x0 (MASKED): spi_xrxo_intr interrupt is masked
5	MSTIM	Multi-Master Contention Interrupt Mask. This bit field is not present if the xSPI is configured as a serial-master device. Values: • 0x1 (UNMASKED): spi_mst_intr interrupt is not masked • 0x0 (MASKED): spi_mst_intr interrupt is masked
4	RXFIM	Receive FIFO Full Interrupt Mask 0 - spi_rxf_intr interrupt is masked 1 - spi_rxf_intr interrupt is not masked Values: • 0x1 (UNMASKED): spi_rxf_intr interrupt is not masked • 0x0 (MASKED): spi_rxf_intr interrupt is masked
3	RXOIM	Receive FIFO Overflow Interrupt Mask Values: • 0x1 (UNMASKED): spi_rxo_intr interrupt is not masked • 0x0 (MASKED): spi_rxo_intr interrupt is masked
2	RXUIM	Receive FIFO Underflow Interrupt Mask Values: • 0x1 (UNMASKED): spi_rxu_intr interrupt is not masked • 0x0 (MASKED): spi_rxu_intr interrupt is masked
1	TXOIM	Transmit FIFO Overflow Interrupt Mask Values: • 0x1 (UNMASKED): spi_txo_intr interrupt is not masked • 0x0 (MASKED): spi_txo_intr interrupt is masked
0	TXEIM	Transmit FIFO Empty Interrupt Mask Values: • 0x1 (UNMASKED): spi_txe_intr interrupt is not masked • 0x0 (MASKED): spi_txe_intr interrupt is masked

37.5.13 Interrupt Status Register (XSPI_ISTS)

This register reports the status of the xSPI interrupts after they have been masked.

Address offset: 0x0030

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	DONEIS	SPITEIS	Reserved	AXIEIS	TXUIS	XRXOIS	MMCIS	RXFFIS	RXFOIS	RXFUIS	TXFOIS	TXFEIS
	r	r		r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	DONEIS	SPI Done Interrupt Status Values: • 0x1 (ACTIVE): spi_done_intr interrupt is active after masking • 0x0 (INACTIVE): spi_done_intr interrupt is not active after masking
10	SPITEIS	SPI Transmit Error Interrupt Values: • 0x1 (ACTIVE): spi_spite_intr interrupt is active after masking • 0x0 (INACTIVE): spi_spite_intr interrupt is not active after masking
9	Reserved	Reserved, the reset value must be maintained.
8	AXIEIS	AXI Error Interrupt Status Values: • 0x1 (ACTIVE): spi_axie_intr interrupt is active after masking • 0x0 (INACTIVE): spi_axie_intr interrupt is not active after masking
7	TXUIS	Transmit FIFO Underflow Interrupt Status Values: • 0x1 (ACTIVE): spi_txu_intr interrupt is active after masking • 0x0 (INACTIVE): spi_txu_intr interrupt is not active after masking
6	XRXOIS	XIP Receive FIFO Overflow Interrupt Status Values: • 0x1 (ACTIVE): spi_xrxo_intr interrupt is active after masking • 0x0 (INACTIVE): spi_xrxo_intr interrupt is not active after masking
5	MMCIS	Multi-Master Contention Interrupt Status. This bit field is not present if the xSPI is configured as a serial-slave device. Values: • 0x1 (ACTIVE): spi_mst_intr interrupt is active after masking • 0x0 (INACTIVE): spi_mst_intr interrupt is not active after masking
4	RXFFIS	Receive FIFO Full Interrupt Status Values: • 0x1 (ACTIVE): spi_rxf_intr interrupt is active after masking • 0x0 (INACTIVE): spi_rxf_intr interrupt is not active after masking
3	RXFOIS	Receive FIFO Overflow Interrupt Status Values: • 0x1 (ACTIVE): spi_rxo_intr interrupt is active after masking • 0x0 (INACTIVE): spi_rxo_intr interrupt is not active after masking
2	RXFUIS	Receive FIFO Underflow Interrupt Status Values:

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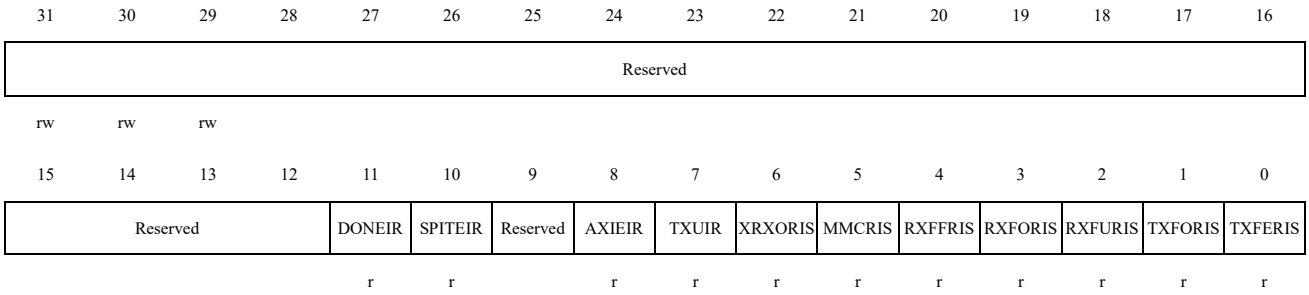
Bit field	Name	Description
		• 0x1 (ACTIVE): spi_rxu_intr interrupt is active after masking • 0x0 (INACTIVE): spi_rxu_intr interrupt is not active after masking
1	TXFOIS	Transmit FIFO Overflow Interrupt Status Values: • 0x1 (ACTIVE): spi_txo_intr interrupt is active after masking • 0x0 (INACTIVE): spi_txo_intr interrupt is not active after masking
0	TXFEIS	Transmit FIFO Empty Interrupt Status Values: • 0x1 (ACTIVE): spi_txe_intr interrupt is active after masking • 0x0 (INACTIVE): spi_txe_intr interrupt is not active after masking

37.5.14 Raw Interrupt Status Register (XSPI_RISTS)

Raw Interrupt Status Register.

Address offset: 0x0034

Reset value: 0x0000 0000



Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	DONEIR	SPI Done Interrupt Raw Status Values: • 0x1 (ACTIVE): spi_done_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_done_intr interrupt is not active prior masking
10	SPITEIR	SPI Transmit Error Interrupt status. This bit gets set, If SPI Master fails to get a READY status from the slave, then it will stop the SPI transfer and the FIFO is flushed (in case of write operation). Values: • 0x1 (ACTIVE): spi_spite_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_spite_intr interrupt is not active prior to masking
9	Reserved	Reserved, the reset value must be maintained.
8	AXIEIR	AXI Error Interrupt Raw Status Values:

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Bit field	Name	Description
		• 0x1 (ACTIVE): spi_axie_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_axie_intr interrupt is not active prior masking
7	TXUIR	Transmit FIFO Underflow Interrupt Raw Status Values: • 0x1 (ACTIVE): spi_txu_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_txu_intr interrupt is not active prior masking
6	XRXORIS	XIP Receive FIFO Overflow Raw Interrupt Status Values: • 0x1 (ACTIVE): spi_xrxo_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_xrxo_intr interrupt is not active prior masking
5	MMCRIS	Multi-Master Contention Raw Interrupt Status. This bit field is not present if the xSPI is configured as a serial-slave device. Values: • 0x1 (ACTIVE): spi_mst_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_mst_intr interrupt is not active prior masking
4	RXFFRIS	Receive FIFO Full Raw Interrupt Status Values: • 0x1 (ACTIVE): spi_rxf_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_rxf_intr interrupt is not active prior masking
3	RXFORIS	Receive FIFO Overflow Raw Interrupt Status Values: • 0x1 (ACTIVE): spi_rxo_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_rxo_intr interrupt is not active prior masking
2	RXFURIS	Receive FIFO Underflow Raw Interrupt Status Values: • 0x1 (ACTIVE): spi_rxu_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_rxu_intr interrupt is not active prior masking
1	TXFORIS	Transmit FIFO Overflow Raw Interrupt Status Values: • 0x1 (ACTIVE): spi_txo_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_txo_intr interrupt is not active prior masking
0	TXFERIS	Transmit FIFO Empty Raw Interrupt Status Values: • 0x1 (ACTIVE): spi_txe_intr interrupt is active prior to masking • 0x0 (INACTIVE): spi_txe_intr interrupt is not active prior masking

37.5.15 Transmit FIFO Error Interrupt Clear Registers (XSPI_TXEICR_CLR)

Transmit FIFO Error Interrupt Clear Register.

Address offset: 0x0038

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TXEICR
															rc_r

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	TXEICR	Clear Transmit FIFO Overflow/Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the spi_txo_intr/spi_txu_intr interrupt; writing has no effect

37.5.16 Receive FIFO Overflow Interrupt Clear Register (XSPI_RXFOI_CLR)

Receive FIFO Overflow Interrupt Clear Register.

Address offset: 0x003C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															RXFOIC
															rc_r

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	RXFOIC	Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the spi_rxo_intr interrupt; writing has no effect

37.5.17 Receive FIFO Underflow Interrupt Clear Register (XSPI_RXFUI_CLR)

Receive FIFO Underflow Interrupt Clear Register.

Address offset: 0x0040

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															RXFUIC
															rc_r

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	RXFUIC	Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the spi_rxu_intr interrupt; writing has no effect

37.5.18 Multi-Master Interrupt Clear Register (XSPI_MMC_CLR)

Multi-Master Interrupt Clear Register.

Address offset: 0x0044

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															MMCIC
															rc_r

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	MMCIC	Clear Multi-Master Contention Interrupt. This register reflects the status of the interrupt. A read from this register clears the spi_mst_intr interrupt; writing has no effect.

37.5.19 Interrupt Clear Register (XSPI_ICLR)

Interrupt Clear Register.

Address offset: 0x0048

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															INTC
															rc_r

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	INTC	Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the spi_txo_intr, spi_rxu_intr, spi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

37.5.20 DMA Control Register (XSPI_DMA_CTRL)

This register is only valid when xSPI is configured with a set of DMA Controller interface signals (SSIC_HAS_DMA = 1) or Internal DMA operation (SSIC_HAS_DMA = 2). When xSPI is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero.

Address offset: 0x004C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											AID[5:0]				
													r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AID	APROT[2:0]			ACACHE[3:0]				Reserved	AINC	Reserved	ATW[1:0]		IDMAE	TXDMAEN	INTC
r	r			r				r		r			r	rw	rw

Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:15	AID[5:0]	AXI awid/arid signal value
14:12	APROT[2:0]	AXI arprot/awprot signal value
11:8	ACACHE[3:0]	AXI arcache/awcache signal value
7	Reserved	Reserved, the reset value must be maintained.
6	AINC	Address Increment. Indicates whether to increment the AXI address on every transfer. 1 = Increment 0 = No Change Note: Increment aligns the address to the next

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Bit field	Name	Description
		XSPI_DMA_CTRL.ATW boundary
5	Reserved	Reserved, the reset value must be maintained.
4:3	ATW[1:0]	AXI transfer width for DMA transfers mapped to arsize/awsize. This value must be less than or equal to SSIC_AXI_DW. 0x0: 1 byte 0x1: 2 bytes 0x2: 4 bytes 0x3: 8 bytes Note: When SSIC_AXI_DW is set to 32 bits, if user programs this field to 0x8(3 bytes). xSPI will use 4 bytes as transfer size for the AXI transfers
2	IDMAE	Internal DMA Enable. This bit should be enabled only when XSPI_CTRL0.FRF = 0 (Motorola SPI) and XSPI_CTRL.SPIFRF > 0
1	TXDMAEN	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. Values: • 0x1 (ENABLED): Transmit DMA enabled • 0x0 (DISABLE): Transmit DMA disabled
0	RXDMAEN	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. Values: • 0x1 (ENABLED): Receive DMA enabled • 0x0 (DISABLE): Receive DMA disabled.

37.5.21 DMA Transmit Data Level (XSPI_DMATDL_CTRL)

This register is only valid when the xSPI is configured with a set of DMA interface signals (SSIC_HAS_DMA = 1). When xSPI is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero.

Address offset: 0x0050

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											DMATDL[4:0]				
											rw				

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4:0	DMATDL[4:0]	Transmit Data Level. This bit field controls the level at which a DMA request is made

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Bit field	Name	Description
		by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and XSPI_DMA_CTRL.TXDMAEN = 1

37.5.22 DMA Receive Data Level (XSPI_DMARDL_CTRL)

This register is only valid when xSPI is configured with a set of DMA interface signals (SSIC_HAS_DMA = 1). When xSPI is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero.

Address offset: 0x0054

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											DMARDL[4:0]				
											rw				

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4:0	DMARDL[4:0]	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and XSPI_DMA_CTRL.RXDMAEN=1

37.5.23 Identification Register (XSPI_IDR)

This register contains the peripherals identification code, which is written into the register at configuration time using coreConsultant.

Address offset: 0x0058

Reset value: 0xFFFF 3610

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDCODE[31:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDCODE[31:0]															

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r

Bit field	Name	Description
31:0	IDCODE[31:0]	Identification code. The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant

37.5.24 XSPI component version (XSPI_VERSION_ID)

This read-only register stores the specific xSPI component version.

Address offset: 0x005C

Reset value: 0x3130 332A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERSION[31:0]															

r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERSION[31:0]															

r

Bit field	Name	Description
31:0	VERSION[31:0]	Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 31_30_33_2A represents the version 1.03*

37.5.25 XSPI Data Register (XSPI_DATx)

The xSPI data register is a 32-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when XSPIEN = 1. FIFOs are reset when XSPIEN = 0. NoteThe DR register in the xSPI occupies thirty-six 32-bit address locations of the memory map to facilitate AHB burst transfers. Writing to any of these address locations has the same effect as pushing the data from the pwdata bus into the transmit FIFO. Reading from any of these locations has the same effect as popping data from the receive FIFO onto the hrdata bus. The FIFO buffers on the xSPI are not addressable.

Address offset: 0x0060+(0~35)*0x4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATx[31:0]															

rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATx[31:0]															
rw															

Bit field	Name	Description
31:0	DATx[31:0]	Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer Note: 36 registers with addresses: 0x60+(0~35)*0x4

37.5.26 RX Sample Delay Register (XSPI_RX_DELAY)

This register is only valid when the xSPI is configured with rxd sample delay logic (SSIC_HAS_RX_SAMPLE_DELAY==1). When the xSPI is not configured with rxd sample delay logic, this register will not exist and writing to its address location will have no effect; reading from its address will return zero. This register control the number of sclk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the xSPI is enabled.

Address offset: 0x00F0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															SES
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								SDCN[7:0]							
								rw							

Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	SES	Receive Data (rxd) Sampling Edge. This register is used to decide the sampling edge for RXD signal with sclk. Then this bit is set to 1 then negative edge of sclk will be used to sample the incoming data, otherwise positive edge will be used for sampling
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	SDCN[7:0]	Receive Data (rxd) Sample Delay. This register is used to delay the sample of the rxd input port. Each value represents a single sclk delay on the sample of rxd. Note; If this register is programmed with a value that exceeds the depth of the internal shift registers ,zero delay will be applied to the rxd sample

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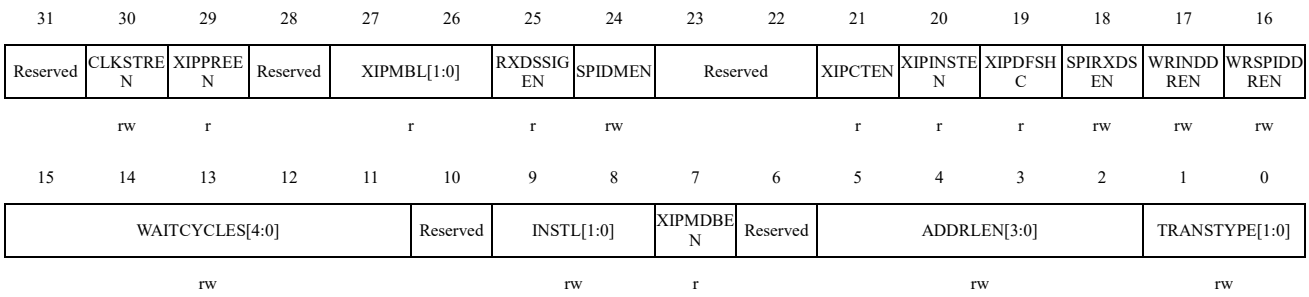
37.5.27 XSPI Control Register (XSPI_ENH_CTRL0)

This register is used to control the serial data transfer in enhanced SPI mode of operation. The register is relevant only when either XSPI_CTRL0.DWSEN is set to 1 or XSPI_CTRL0. SPIFRF is set to either 01 or 10 or 11. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

Address offset: 0x00F4

Reset value: 0x0000 0200



Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	CLKSTREN	Enables clock stretching capability in SPI transfers. In case of write, if the FIFO becomes empty xSPI will stretch the clock until FIFO has enough data to continue the transfer. In case of read, if the receive FIFO becomes full xSPI will stop the clock until data has been read from the FIFO
29	XIPPREEN	Enables XIP pre-fetch functionality in xSPI. Once enabled, xSPI will pre-fetch data frames from next contigous location, to reduce the latency for the upcoming contiguous transfer. If the next XIP request is not contigous then pre-fetched bits will be discarded
28	Reserved	Reserved, the reset value must be maintained.
27:26	XIPMBL[1:0]	XIP Mode bits length. Sets the length of mode bits in XIP mode of operation. These bits are valid only when XSPI_ENH_CTRL0.XIPMDBEN is set to 1. Values: • 0x0 (MBL_2): Mode bits length equal to 2 • 0x1 (MBL_4): Mode bits length equal to 4 • 0x2 (MBL_8): Mode bits length equal to 8 • 0x3 (MBL_16): Mode bits length equal to 16
25	RXDSSIGEN	Enable rxds signaling during address and command phase of Hypebus transfer. This bit enables rxds signaling by Hyperbus slave devices during Command-Address (CA) phase. If the rxds signal is set to 1 during the CA phase of transfer, xSPI transmits (2* XSPI_CTRL0.WAITCYCLES-1) wait cycles after the address phase is complete
24	SPIDMEN	SPI data mask enable bit. When this bit is enabled, the txd_dm signal is used to mask the data on the txd data line. This bit is enabled only when the SPIDMEN parameter is set to 1

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Bit field	Name	Description
23:22	Reserved	Reserved, the reset value must be maintained.
21	XIPCTEN	Enable continuous transfer in XIP mode. If this bit is set to 1 then continuous transfer mode in XIP will be enabled, in this mode xSPI will keep slave selected until a non-XIP transfer is detected on the AHB interface
20	XIPINSTEN	XIP instruction enable bit. If this bit is set to 1 then XIP transfers will also have instruction phase. The instruction op-codes will be chosen from XSPI_XIP_INCR_TOC or XSPI_XIP_WRAP_TOC registers bases on AHB transfer type
19	XIPDFSHC	Fix DFS for XIP transfers. If this bit is set to 1 then data frame size for XIP transfers will be fixed to the programmed value in XSPI_CTRL0.DFS. The number of data frames to fetch will be determined by HSIZE and HBURST signals. If this bit is set to 0 then data frame size and number of data frames to fetch will be determined by HSIZE and HBURST signals
18	SPIRXDSEN	Read data strobe enable bit. Once this bit is set to 1 xSPI will use Read data strobe (rxds) to capture read data in DDR mode
17	WRINDDREN	Instruction DDR Enable bit. This will enable Dual-data rate transfer for Instruction phase
16	WRSPIDDREN	SPI DDR Enable bit. This will enable Dual-data rate transfers in Dual/Quad/Octal frame formats of SPI
15:11	WAITCYCLES[4:0]	Wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception. Specified as number of SPI clock cycles
10	Reserved	Reserved, the reset value must be maintained.
9:8	INSTL[1:0]	Dual/Quad/Octal mode instruction length in bits. Values: • 0x0 (INST_L0): No Instruction • 0x1 (INST_L4): 4-bit Instruction length • 0x2 (INST_L8): 8-bit Instruction length • 0x3 (INST_L16): 16-bit Instruction length
7	XIPMDBEN	Mode bits enable in XIP mode. If this bit is set to 1, then in XIP mode of operation xSPI will insert mode bits after the address phase. These bits are set in register XSPI_XIP_MODE register. The length of mode bits is always set to 8 bits
6	Reserved	Reserved, the reset value must be maintained.
5:2	ADDRLEN[3:0]	This bit defines Length of Address to be transmitted. Only after this much bits are programmed in to the FIFO the transfer can begin. Values: • 0x0 (ADDR_L0): No Address • 0x1 (ADDR_L4): 4-bit Address length • 0x2 (ADDR_L8): 8-bit Address length • 0x3 (ADDR_L12): 12-bit Address length • 0x4 (ADDR_L16): 16-bit Address length • 0x5 (ADDR_L20): 20-bit Address length • 0x6 (ADDR_L24): 24-bit Address length • 0x7 (ADDR_L28): 28-bit Address length

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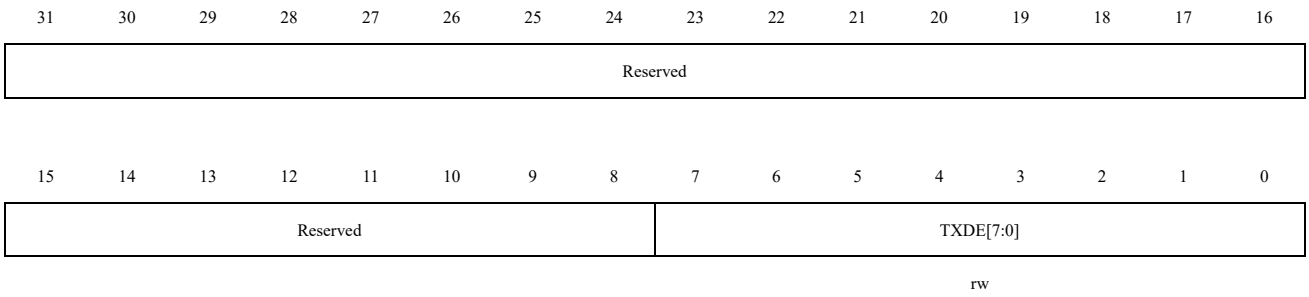
Bit field	Name	Description
		• 0x8 (ADDR_L32): 32-bit Address length • 0x9 (ADDR_L36): 36-bit Address length • 0xa (ADDR_L40): 40-bit Address length • 0xb (ADDR_L44): 44-bit Address length • 0xc (ADDR_L48): 48-bit Address length • 0xd (ADDR_L52): 52-bit Address length • 0xe (ADDR_L56): 56-bit Address length • 0xf (ADDR_L60): 60-bit Address length
1:0	TRANSTYPE[1:0]	Address and instruction transfer format. Selects whether xSPI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in XSPI_CTRL0.SPIFRF field. Values: • 0x0 (TT0): Instruction and Address will be sent in Standard SPI Mode. • 0x1 (TT1): Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by XSPI_CTRL0.SPIFRF. • 0x2 (TT2): Both Instruction and Address will be sent in the mode specified by XSPI_CTRL0.SPIFRF. • 0x3 (TT3): Reserved

37.5.28 Transmit Drive Edge Register (XSPI_DDR_TXDE)

This Register is valid only when SSIC_HAS_DDR is equal to 1(Dual Data Rate Support). This register is used to control the driving edge of TXD register in DDR mode. It is not possible to write to this register when the xSPI is enabled (XSPIEN =1).

Address offset: 0x00F8

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	TXDE[7:0]	TXD Drive edge register which decided the driving edge of transmit data. The maximum value of this register is = (BAUDR/2) -1 BAUDR= CLKDIV *2

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37.5.29 eXecute in Place - Mode bits (XSPI_XIP_MODE)

This register carries the mode bits which are sent in the XIP mode of operation after address phase. This is a 8 bit register and can only be written when XSPI_EN register is set to 0.

Address offset: 0x00FC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XIPMDBITS[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	XIPMDBITS[15:0]	XIP mode bits to be sent after address phase of XIP transfer.

37.5.30 XIP INCR transfer opcode (XSPI_XIP_INCR_TOC)

This Register is valid only when SSIC_XIP_EN is equal to 1. This register is used to store the instruction op-code to be used in INCR transactions when the same is requested on AHB interface. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

Address offset: 0x0100

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ITOC[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	ITOC[15:0]	XIP INCR transfer opcode. When XSPI_ENH_CTRL0.XIPINSTEN bit is set to 1, xSPI sends instruction for all XIP transfers, this register field stores the instruction op-code to

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Bit field	Name	Description
		be sent when an INCR type transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by XSPI_ENH_CTRL0.INSTL field

37.5.31 XIP WRAP transfer opcode (XSPI_XIP_WRAP_TOC)

This Register is valid only when SSIC_XIP_EN is equal to 1. This register is used to store the instruction op-code to be used in WRAP transactions when the same is requested on AHB interface. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

Address offset: 0x0104

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTOC[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	WTOC[15:0]	XIP WRAP transfer opcode. When XSPI_ENH_CTRL0.XIPINSTEN bit is set to 1, xSPI sends instruction for all XIP transfers, this register field stores the instruction op-code to be sent when an WRAP type transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by XSPI_ENH_CTRL0.INSTL field

37.5.32 XIP Control Register (XSPI_XIP_CTRL)

This Register is valid only when SSIC_CONCURRENT_XIP_EN is equal to 1. This register is used to store the control information that the XIP transfer will be using in the concurrent mode. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

Address offset: 0x0108

Reset value: 0x0800 0402

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		XIPPREEN	Reserved	XIPMBL[1:0]		RXDSSIGEN	XIPHYPEEN	XIPCTEN	XIPINSTEN	RXDSEN	WRINDDREN	DDREN	DFSHC	WAITCYCLES[4:0]	
		rw		rw		r	r	rw	rw	rw	rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WAITCYCLES[4:0]			MDBITSEN	Reserved	INSTL[1:0]		Reserved	ADDRL[3:0]				TRANSTYPE[1:0]		FRF[1:0]	

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rw rw rw rw rw rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	XIPPREEN	Enables XIP pre-fetch functionality in xSPI. Once enabled xSPI will pre-fetch data frames from next contigous location, to reduce the latency for the upcoming contiguous transfer. If the next XIP request is not contigous then pre-fetched bits will be discarded
28	Reserved	Reserved, the reset value must be maintained.
27:26	XIPMBL[1:0]	XIP Mode bits' length. Sets the length of mode bits in XIP mode of operation. These bits are valid only when XSPI_ENH_CTRL0.XIPMDBEN is set to 1. Values: 0x0 (MBL_2): Mode bits' length equal to 2 0x1 (MBL_4): Mode bits' length equal to 4 0x2 (MBL_8): Mode bits' length equal to 8 0x3 (MBL_16): Mode bits' length equal to 16
25	RXDSSIGEN	Enable rxds signaling during address and command phase of Hyperbus transfer. This bit enables rxds signaling by Hyperbus slave devices during Command-Address (CA) phase. If the rxds signal is set to 1 during the CA phase of transfer, xSPI transmits (2* WAITCYCLES-1) wait cycles after the address phase is complete
24	XIPHYPEEN	SPI Hyperbus Frame format enable for XIP transfers. Selects if data frame format for XIP transfers is in Hyperbus mode. This field is effective only when XSPI_CTRL0.FRF is set to SPI frame format
23	XIPCTEN	Enable continuous transfer in XIP mode. If this bit is set to 1 then continuous transfer mode in XIP will be enabled, in this mode xSPI will keep slave selected until a non-XIP transfer is detected on the AHB interface
22	XIPINSTEN	XIP instruction enable bit. If this bit is set to 1 then XIP transfers will also have instruction phase. The instruction op-codes will be chosen from XSPI_XIP_INCR_TOC or XSPI_XIP_WRAP_TOC registers bases on AHB transfer type
21	RXDSEN	Read data strobe enable bit. Once this bit is set to 1 xSPI will use Read data strobe (rxds) to capture read data in DDR mode
20	WRINDDREN	Instruction DDR Enable bit. This will enable Dual-data rate transfer for Instruction phase
19	DDREN	SPI DDR Enable bit. This will enable Dual-data rate transfers in Dual/Quad/Octal frame formats of SPI
18	DFSHC	Fix DFS for XIP transfers. If this bit is set to 1 then data frame size for XIP transfers will be fixed to the programmed value in XSPI_CTRL0.DFS. The number of data frames to fetch will be determined by HSIZE and HBURST signals. If this bit is set to 0 then data frame size and number of data frames to fetch will be determined by HSIZE and HBURST signals
17:13	WAITCYCLES[4:0]	Wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception. Specified as number of SPI clock cycles
12	MDBITSEN	Mode bits enable in XIP mode. If this bit is set to 1, then in XIP mode of operation xSPI

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Bit field	Name	Description
		will insert mode bits after the address phase. These bits are set in register XSPI_XIP_MODE register. The length of mode bits is always set to 8 bits
11	Reserved	Reserved, the reset value must be maintained.
10:9	INSTL[1:0]	Dual/Quad/Octal mode instruction length in bits. Values: 0x0 (INST_L0): No Instruction 0x1 (INST_L4): 4-bit Instruction length 0x2 (INST_L8): 8-bit Instruction length 0x3 (INST_L16): 16-bit Instruction length
8	Reserved	Reserved, the reset value must be maintained.
7:4	ADDRL[3:0]	This bit defines Length of Address to be transmitted. Only after this much bits are programmed in to the FIFO the transfer can begin. Values: 0x0 (ADDR_L0): No Address 0x1 (ADDR_L4): 4-bit Address length 0x2 (ADDR_L8): 8-bit Address length 0x3 (ADDR_L12): 12-bit Address length 0x4 (ADDR_L16): 16-bit Address length 0x5 (ADDR_L20): 20-bit Address length 0x6 (ADDR_L24): 24-bit Address length 0x7 (ADDR_L28): 28-bit Address length 0x8 (ADDR_L32): 32-bit Address length 0x9 (ADDR_L36): 36-bit Address length 0xa (ADDR_L40): 40-bit Address length 0xb (ADDR_L44): 44-bit Address length 0xc (ADDR_L48): 48-bit Address length 0xd (ADDR_L52): 52-bit Address length 0xe (ADDR_L56): 56-bit Address length 0xf (ADDR_L60): 60-bit Address length
3:2	TRANSTYPE[1:0]	Address and instruction transfer format. Selects whether xSPI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in CTRLR0.SPI_FRF field. Values: 0x0 (TT0): Instruction and Address will be sent in Standard SPI Mode. 0x1 (TT1): Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by XSPI_XIP_CTRL.FRF. 0x2 (TT2): Both Instruction and Address will be sent in the mode specified by XSPI_XIP_CTRL.FRF. 0x3 (TT3): Reserved
1:0	FRF[1:0]	SPI Frame Format Selects data frame format for Transmitting/Receiving the data. Values:

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Bit field	Name	Description
		0x0 (RSVD): Reserved 0x1 (SPI_DUAL): Dual SPI Format 0x2 (SPI_QUAD): Quad SPI Format 0x3 (SPI_OCTAL): Octal SPI Format

37.5.33 Slave Enable Register (XSPI_XIP_SLAVE_EN)

This register is valid only when the SSIC_CONCURRENT_XIP_EN is equal to 1 and SSIC_XIP_WRITE_EN is equal to 0. The register enables the individual slave select output lines from the xSPI master for XIP mode of operation. Up to 16 slave-select output pins are available on the xSPI master. You cannot write to this register when xSPI is busy or when XSPIEN = 1.

Address offset: 0x010C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												SEN[3:0]			
												rw			

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	SEN[3:0]	Slave Select Enable Flag. Each bit in this register corresponds to a slave select line (nss) from the xSPI master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a XIP transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a XIP transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set

37.5.34 XIP Receive FIFO Overflow Interrupt Clear Register (XSPI_XIP_RXFOI_CLR)

XIP Receive FIFO Overflow Interrupt Clear Register.

Address offset: 0x0110

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															XRXFOIC
															rc_r

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	XRXFOIC	Clear XIP Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_xrxo_intr(_n)interrupt; writing has no effect

37.5.35 XIP time out register for continuous transfers (XSPI_XIP_TOUT)

XIP count down register for continuous mode. The counter is used to de-select the slave during continuous transfer mode. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

Address offset: 0x0114

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								XTOUT[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	XTOUT[7:0]	XIP time out value in terms of hclk. Once slave is selected in continuous XIP mode this counter will be used to de-select the slave if there is no request for the time specified in the counter

37.5.36 XIP Write INCR transfer opcode (XSPI_XIP_WRITE_INCR_INST)

This Register is valid only when both SSIC_XIP_WRITE_REG_EN is set to 1. This register is used to store the instruction op-code to be used in INCR transactions for XIP Write when the same is requested on AHB interface. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

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Address offset: 0x0140

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INCRWRINST[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	INCRWRINST[15:0]	XIP Write INCR transfer opcode. When XIP_WRITE_CTRL.WRINSTL is not equal to 0, xSPI sends instruction for all XIP write transfers, this register field stores the instruction op-code to be sent when an INCR type XIP Write transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by XIP_WRITE_CTRL.WRINSTL field

37.5.37 XIP Write WRAP transfer opcode (XSPI_XIP_WRITE_WRAP_INST)

This Register is valid only when both SSIC_XIP_WRITE_REG_EN is set to 1. This register is used to store the instruction op-code to be used in WRAP transactions for XIP Write when the same is requested on AHB interface. It is not possible to write to this register when the xSPI is enabled (XSPIEN=1).

Address offset: 0x0144

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRAPWRINST[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	WRAPWRINST[15:0]	XIP Write WRAP transfer opcode. When XIP_WRITE_CTRL.WRINSTL is not equal to 0, DWC_ssi sends instruction for all XIP write transfers, this register field stores the instruction op-code to be sent when an WRAP type XIP Write transfer is requested

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Bit field	Name	Description
		on AHB bus. The number of bits to be send in instruction phase is determined by XIP_WRITE_CTRL.WRINSTL field

37.5.38 XIP Write Control Register (XSPI_XIP_WRITE_CTRL)

This Register is valid only when SSIC_XIP_WRITE_REG_EN is equal to 1. This register is used to store the control information that the XIP write transfer will be using in the xip mode. It is not possible to write to this register when the xSPI is enabled(XSPIEN=1).

Address offset: 0x0148

Reset value: 0x0000 0072

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											XIPWRWCY[4:0]				
											r				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		XIPWRRXDSSIGEN	XIPWRHYPEEN	WRINDDREN	WRSPIDDREN	WRINSTL[1:0]		WRADDRL[3:0]				WRTRTYPE[1:0]		WRFRF[1:0]	
		r	r	rw	rw	rw		rw				rw		rw	

Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:16	XIPWRWCY[4:0]	Wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception. Specified as number of SPI clock cycles
15:14	Reserved	Reserved, the reset value must be maintained.
13	XIPWRRXDSSIGEN	Enable rxds signaling during address and command phase of Hyperbus transfer. This bit enables rxds signaling by Hyperbus slave devices during Command-Address (CA) phase. If the rxds signal is set to 1 during the CA phase of transfer, xSPI transmits (2* XSPI_XIP_WRITE_CTRL.XIPWRWCY -1) wait cycles after the address phase is complete
12	XIPWRHYPEEN	SPI Hyperbus Frame format enable for XIP Write transfers. Selects if data frame format for XIP Write transfers is in Hyperbus mode. This field is effective only when XSPI_CTRL0.FRF is set to SPI frame format
11	WRINDDREN	Instruction DDR Enable bit. This will enable Dual-data rate transfer for Instruction phase
10	WRSPIDDREN	SPI DDR Enable bit. This will enable Dual-data rate transfers in Dual/Quad/Octal frame formats of SPI
9:8	WRINSTL[1:0]	Dual/Quad/Octal mode instruction length in bits. Values: 0x0 (INST_L0): No Instruction 0x1 (INST_L4): 4-bit Instruction length

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Bit field	Name	Description
		0x2 (INST_L8): 8-bit Instruction length 0x3 (INST_L16): 16-bit Instruction length
7:4	WRADDRL[3:0]	This bit defines Length of Address to be transmitted. Only after this much bits are programmed in to the FIFO the transfer can begin Values: 0x0 (ADDR_L0): Reserved 0x1 (ADDR_L4): 4-bit Address length 0x2 (ADDR_L8): 8-bit Address length 0x3 (ADDR_L12): 12-bit Address length 0x4 (ADDR_L16): 16-bit Address length 0x5 (ADDR_L20): 20-bit Address length 0x6 (ADDR_L24): 24-bit Address length 0x7 (ADDR_L28): 28-bit Address length 0x8 (ADDR_L32): 32-bit Address length
3:2	WRTRTYPE[1:0]	Address and instruction transfer format. Selects whether xSPI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in XIP_WRITE_CTRL.WRFRF field. Values: 0x0 (TT0): Instruction and Address will be sent in Standard SPI Mode. 0x1 (TT1): Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by XIP_WRITE_CTRL.WRFRF. 0x2 (TT2): Both Instruction and Address will be sent in the mode specified by XIP_WRITE_CTRL.WRFRF. 0x3 (TT3): Reserved
1:0	WRFRF[1:0]	SPI Frame Format Selects data frame format for Transmitting the data. Values: 0x0 (RSVD): Reserved 0x1 (SPI_DUAL): Dual SPI Format 0x2 (SPI_QUAD): Quad SPI Format 0x3 (SPI_OCTAL): Octal SPI Forma

37.5.39 XIP Write Timing Register (XSPI_XIP_WRITE_TIMING)

XIP Write Timing Register

Address offset: 0x0180

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TPP[31:0]															
rw															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPP[31:0]															
rw															

Bit field	Name	Description
31:0	TPP[31:0]	The timing register indicates the flash memory page programming time (tpp) This value must be set with respect to the frequency of tpp_clk clock. For example, if tpp_clk frequency is 16MHz (that is period is 62.5ns) and page programming time is 1,250 mico second the TPP register value should be 20,000 (32'h4E20). TPP register value must be set before performing any XIP write operation. For XIP write burst the xSPI will check for the write burst termination. For the last beat of the write burst the xSPI will insert the WAIT state in the AHB bus until the flash page proamming time is elapsed.

37.5.40 RXDS Delay line control (XSPI_RXDS_DELAY_CTRL)

RXDS Delay line control

Address offset: 0x0184

Reset value: 0x0000 0017

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											RXDSDELAYEN	RXDSTAPDELAY[3:0]			
											rw	rw			

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	RXDSDELAYEN	1 = Enable the RXDS delay line 0 = Bypass the RXDS delay line When enabled, the input signal RXDS will go through the delay line. The RXDS is delayed to approximately center alingned to the DDR input data. When disabled, the input RXDS signal will be directly used to capture the DDR input data. In such case the board should have appropiate delay in some extent to center align the DDR input data.
3:0	RXDSTAPDELAY[3:0]	RXDS Delay line is a 16 tapped delay consisting of delay cells. For each tap the delay cell can delays a range from 0.4ns to 0.6ns. Based on the DDR input timing the user should select appropiate delay to nearly center align the RXDS signal to capture the

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Bit field	Name	Description
		data. If RXDSDELAYENis 1, the RXDSTAPDELAY=0 will produce 1 tap delay.

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38 Flexible External Memory Controller（FEMC）

The FEMC uses a Core Link FEMC-353 AXI Static Memory Controller (SMC) IP core made by ARM Limited, England. More information about this controller can be found on the ARM Limited website (http://www.arm.com).

38.1 Introduction

The Flexible External Memory Controller (FEMC) is used to access various external memories, allowing for the convenient expansion of different types of high-capacity static memories based on application requirements. It can simultaneously expand multiple types of static memories without adding external interfaces. All external memories share the addresses, data, and control signals output by the FEMC controller, and FEMC distinguishes between different external devices using a unique chip-select signal.

38.2 Main Features

The main features supported by FEMC are shown below:

General

- 26 bit external address line
- 8-bit ,16-bit or 32 bit external data width is configurable
- Up to 100MHz clock frequency
- Supports two memory interface: SRAM Interface (4 chip selects) and NAND Interface (2 chip selects)
- Timing is programmable to support different devices
- External asynchronous wait control.
- Supports DMA access
- Supports software reset
- Write FIFO with 16x32-bit depth
- Read FIFO with 16x72-bit depth

SRAM Interface

- Supports 1 memory area, up to 256MB, and contains 4Block x 512-bit(64MB)
- Supports the expansion of the following devices:
  - SRAM
  - PSRAM
  - ROM
  - NOR Flash
  - LCD(8080/6800)
- 16-bit or 32-bit external data width is configurable
- Each bank has a dedicated chip selection signal line
- Each bank can be configured independently
- Supports burst mode for faster access to synchronous device such as NOR Flash, PSRAM
- Timing programmable to support different devices
- Write enable and byte channel select output, can be used with PSRAM, SRAM devices
- External asynchronous wait control

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- Asynchronous mode
- Synchronous burst mode
- Address/data bus reuse is configurable

NAND Interface

- Supports 2 memory areas, each area is 256MB
- 8-bit or 16-bit external data width is configurable
- Each memory area has independent device selection signals
- The parameter of each memory area can be configured independently
- Read and write timing can be configured independently
- External asynchronous wait control
- Supports hardware 1bit ECC. The ECC page size can be configured up to 2K bytes

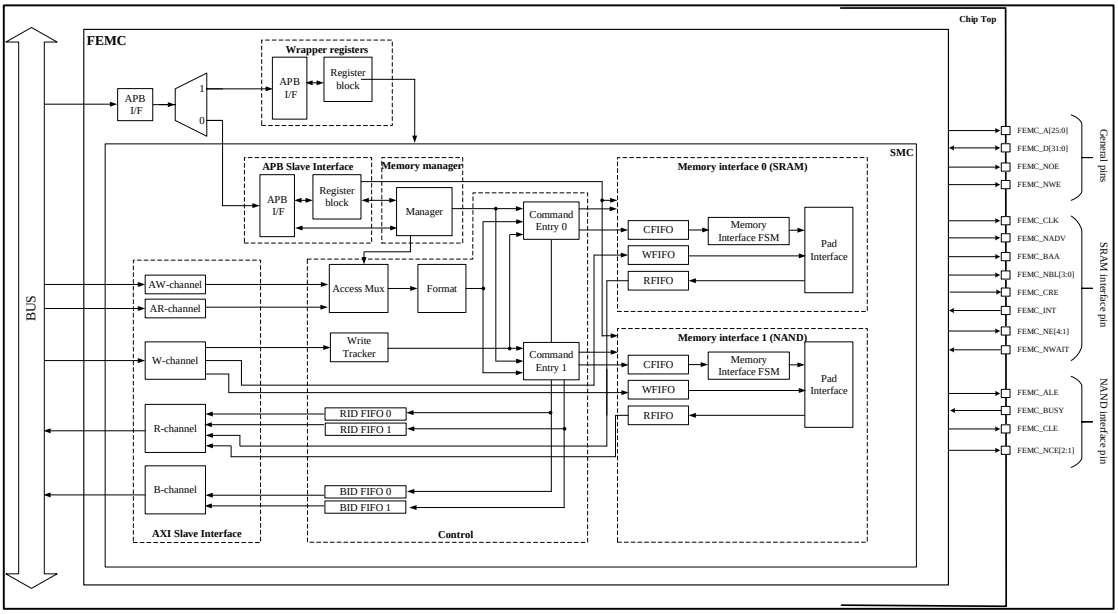
38.3 FEMC Block Diagram

FEMC consists of five parts:

- AXI interface
- FEMC configuration register
- NOR Flash and SRAM controller
- NAND Flash controller
- External device interface

The FEMC block diagram is as follows:

Figure 38-1 FEMC Block Diagram



38.4 Pin Definitions

Table 39-1 shows the pins used by SRAM and NAND, and their corresponding functions.

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Table 38-1 FEMC Pin Definitions

Pin Name	IO type	Interface type	Description
FEMC_A[25:0]	Output	General	Address
FEMC_D[31:0]	IN/OUT	General	Bidirectional Data
FEMC_NOE	Output	General	Output enable
FEMC_NWE	Output	General	Write enable
FEMC_CLK	Output	SRAM	Memory clock output
FEMC_NADV	Output	SRAM	Address valid
FEMC_BAA	Output	SRAM	Burst address advance
FEMC_NBL[3:0]	Output	SRAM	Byte lane strobe
FEMC_CRE	Output	SRAM	Configuration register write
FEMC_INT	Input	SRAM	Interrupt input
FEMC_NE[4:1]	Output	SRAM	Chip Enable (4 devices)
FEMC_NWAIT	Input	SRAM	Wait signal
FEMC_ALE	Output	NAND	Address latch enable
FEMC_BUSY	Input	NAND	Busy signal
FEMC_CLE	Output	NAND	Command latch enable
FEMC_NCE[2:1]	Output	NAND	Chip Enable (2 devices)

38.5 Function Description

38.5.1 Clock and Reset

There are 4 clock domains:

1. APB Bus domain: It is used for APB register configuration. Maximum clock frequency is 150Mhz.
2. AXI Bus domain: It is used for AXI transfer access. Maximum clock frequency is 300Mhz.
3. SRAM Interface domain: It is used for memory access on memory interface 0 (SRAM/ PSRAM/ NOR Flash). Maximum clock frequency is 100Mhz.

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This domain includes an inverted version of memory clock, an output clock provided to external memory device and a feedback clock from the pad.

4. NAND Interface domain: It is used for memory access on memory interface 0 (NAND Flash). Maximum clock frequency is 100Mhz.

   This domain includes an inverted version of memory clock.

It is programmable to configure synchronous or asynchronous between memory clocks and AXI clock.

Synchronous clocking

The benefit of synchronous clocking is that you can reduce the read and write latency by removing the synchronization registers between clock domains. However, because of the integer relationship of the clocks, you might not be able to get the maximum performance from the system because of constraints placed on the bus frequency by the external memory clock speed.

In synchronous mode, the handshaking between the aclk and mclk<x> domains enables synchronous operation of the two clocks at multiples of each other, that is, ratios of n:1 and 1:m. Synchronous operation of the clocks can be 1:1, n:1, or 1:n.

Asynchronous clocking

The main benefit of asynchronous clocking is that you can maximize the system performance, while running the memory interface at a fixed system frequency. Additionally, in sleep-mode situations when the system is not required to do much work, you can lower the frequency to reduce power consumption.

38.5.2 Memory control operation

38.5.2.1 Chip configuration registers

The FEMC provides a mechanism for synchronizing the switching of operating modes with that of the memory device.

The **FEMC Timing Configuration Register** and **FEMC Operate Mode Configuration Register** act as holding registers for new operating parameters until the FEMC detects the memory device has switched modes. This enables a memory device to be made to change its operating mode while still being accessed.

Figure 38-1 shows the memory manager containing a bank of registers for each memory chip supported by the FEMC configuration. The manager register bank consists of all the timing parameters, and operation modes. These are required for the FEMC to correctly time any type of access to a supported memory type.

The APB registers FEMC Timing Configuration Register and FEMC Operate Mode Configuration Register act as holding registers, the configuration registers within the manager are only updated if either:

- The FEMC Control Register indicates only a register update is taking place
- The FEMC Control Register indicates a mode register access either using the FEMC Control Register or using the AXI interface and the command has completed.

The chip configuration registers are available as read-only registers in the address map of the APB interface.

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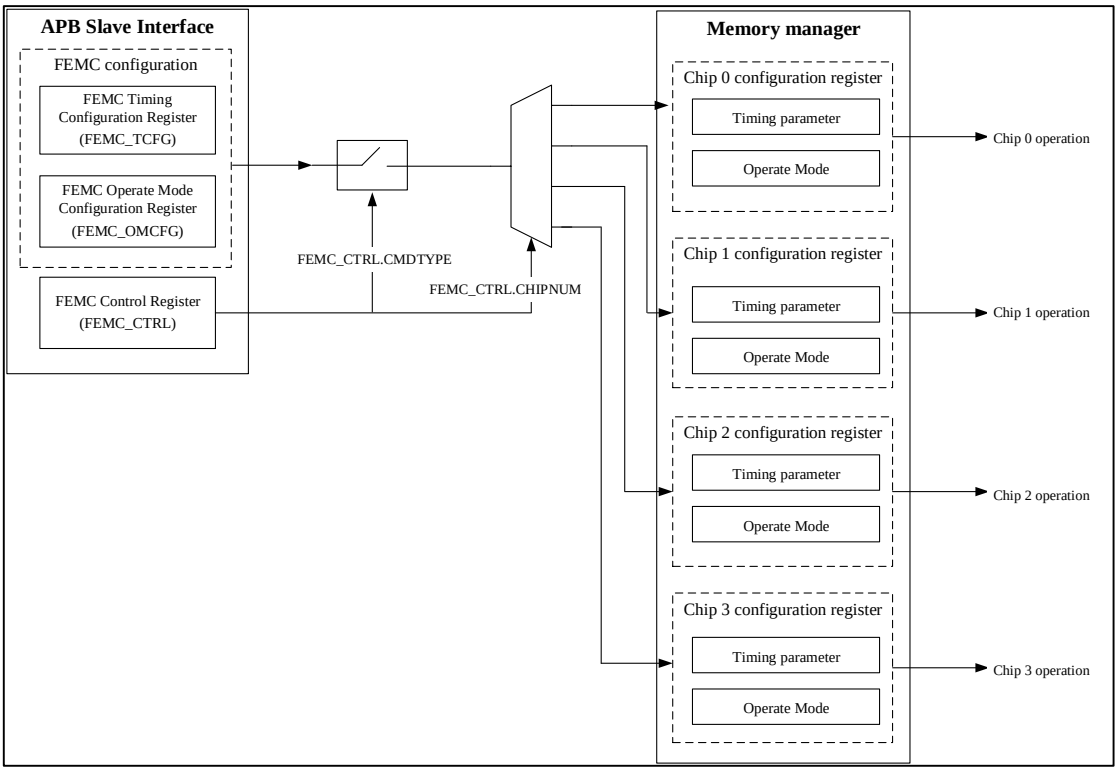
Figure 38-1 Chip configuration registers



38.5.2.2 Control commands

The FEMC enables code to be executed from the memory while simultaneously, from the software perspective, moving the same chip to a different operating mode. This is achieved by synchronizing the update of the chip configuration registers from the holding registers with the dispatch of the memory configuration register write.

The FEMC provides two mechanisms for simultaneously updating the controller and memory configuration registers. These are:

38.5.2.2.1 Device pin mechanism

For memories that use an input pin to indicate that a write is intended for the configuration register, for example some PSRAM devices, the write mechanism can be implemented using the FEMC Control Register. Figure 38-2 shows the sequence of events.

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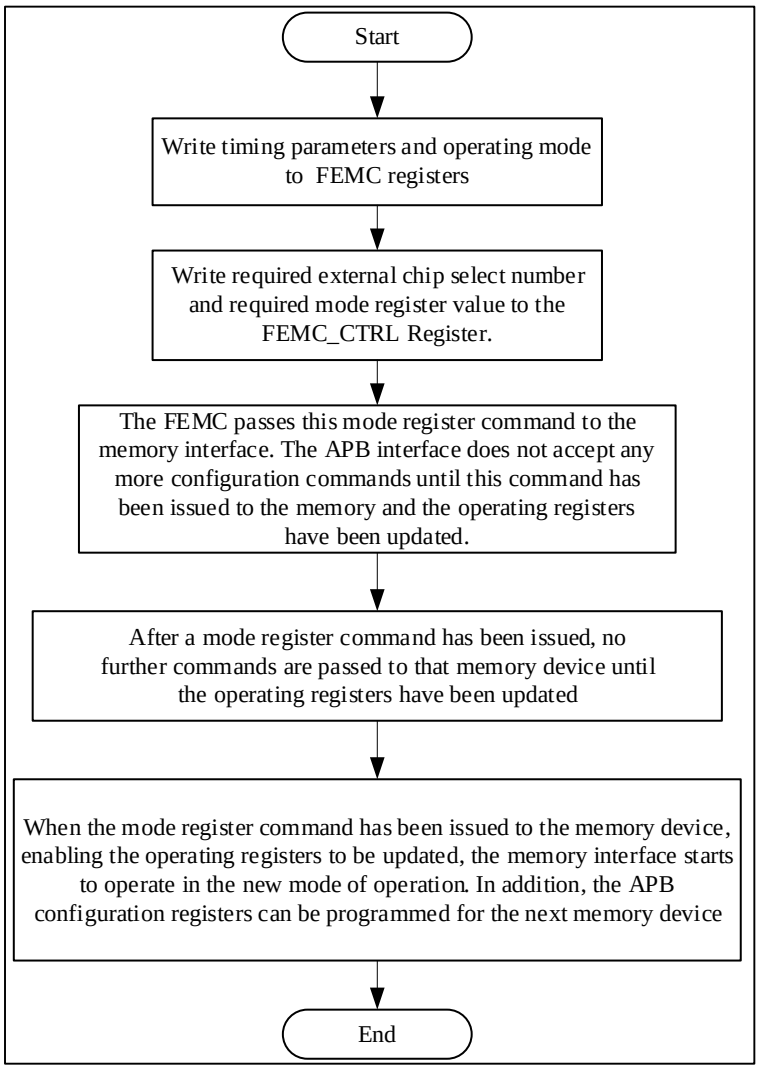
Figure 38-2 Device pin mechanism



38.5.2.2.2 Software mechanism

For memories that require a sequence of read and write commands, for example, most NOR flash devices use the AXI interface, with the write data bus used to indicate when the last transfer has completed and when it is safe for the FEMC to update the chip configuration registers. Figure 38-3 shows the sequence of events.

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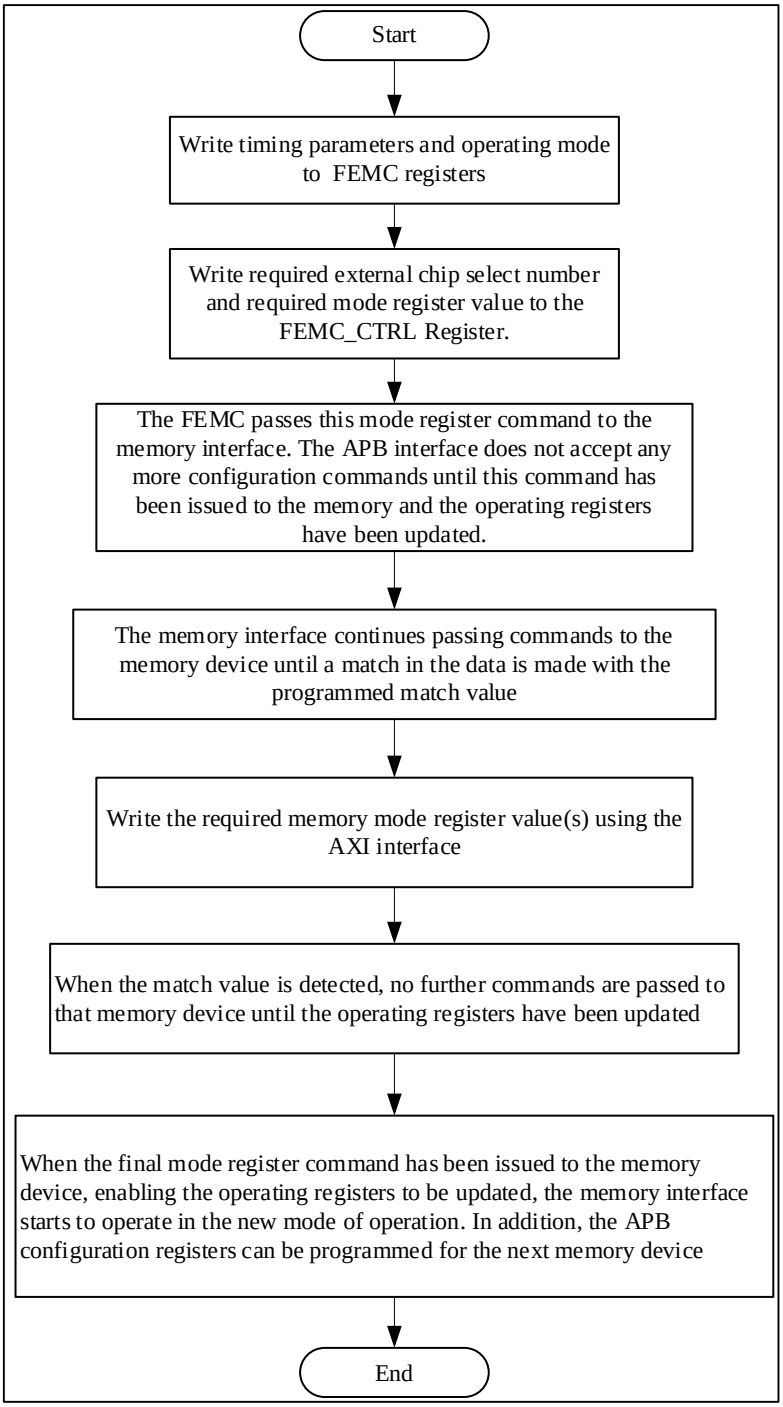
Figure 38-3 Software mechanism



38.5.3 SRAM interface memory access

38.5.3.1 Standard SRAM accesses

The FEMC programmer's view is a flat area of memory. The upper byte of the address read or write bus, **Address[31:24]** and the value of the **ADDRMCH[7:0]** and **ADDRMSK[7:0]** bits of the **Set Address Registers** determine the chip select being accessed, based on following formula:

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- **Address[31:24]** & **ADDRMSK[7:0]** must equal **ADDRMCH[7:0]**

The values for the **ADDRMCH** and **ADDRMSK** buses must be set so that no address maps onto more than one chip, otherwise the behavior of the FEMC is undefined. If an access does not map to any memory device then the FEMC performs an asynchronous transfer on memory interface 0 with all chip selects de-asserted. After the transfer completes, the FEMC provides an OKAY response. In addition to reads and writes, exclusive reads and writes are supported in accordance with the *AMBA AXI Protocol Specification*. Successful exclusive accesses have an EXOKAY response. All other accesses, including exclusive fail accesses, receive an OKAY response.

38.5.3.2 Memory address shifting

To produce the address presented to the memory device, the AXI address is aligned to the memory width. This is done because the AXI address is a byte-aligned address, whereas the memory address is a memory-width-aligned address.

NOTE: During initial configuration of a memory device, the memory mode register can be accessed with a sequence of transfers to specific addresses. You must take into consideration the shifting performance by the FEMC when accessing memory mode registers.

38.5.3.3 Memory burst alignment

The FEMC provides a programmable option for controlling the formatting of memory transfers with respect to memory burst boundaries, through the burst_align bit of the opmode registers.

When set, the burst_align bit causes memory bursts to be aligned to a memory burst boundary. This setting is intended for use with memories that use the concept of internal pages. This can be an asynchronous page mode memory, or a synchronous PSRAM. If an AXI burst crosses a memory burst boundary, the FEMC partitions the AXI transfer into multiple memory bursts, terminating a memory transfer at the burst boundary. Ensure the page size is an integer multiple of the burst length, to avoid a memory burst crossing a page boundary.

When the burst_align bit is not set, the FEMC ignores the memory burst boundary when mapping AXI commands onto memory commands. This setting is intended for use with devices such as NOR flash. These devices have no concept of pages.

38.5.3.4 Memory burst length

The FEMC enables you to program the memory burst length on an individual chip basis, from length 1 to 32 beats, or a continuous burst. The length of memory bursts are however automatically limited by the size of the read or write data FIFOs.

For read transfers, the maximum memory burst length on the memory interface is the depth of the read data FIFO. For writes, the maximum burst length is dependent on:

- The beat size of the AXI transfer
- The memory data bus width, mw
- The depth of the write data FIFO depth, wfifo_depth.

The formula to determine the maximum memory write burst length is:

Memory write burst length = ((1<<AXI burst size) x wfifo_depth) / (1<<mw)

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38.5.3.5 SRAM interface timing diagrams

This section describe the timing diagrams of the accesses occurs on SRAM interface (SRAM/PSRAM/NOR Flash). For the diagrams in this section, below signal notations are applied:

- *mclk* – SRAM interface memory clock (equal *FEMC_CLK*)
- *fbclk* – Fed-back clock, a delay version of mclk that compensate the delay of mclk on the pad
- *cs_n* – Chip Select (equal *FEMC_NE*)
- *oe_n* – Output Enable (equal *FEMC_NOE*)
- *add/address* – Address (equal *FEMC_A*)
- *adv* – Address valid (equal *FEMC_NADV*)
- *we_n* – Write enable (equal *FEMC_NWE*)
- *wait* – Wait signal (equal *FEMC_NWAIT*)
- *wait_reg_fbclk* – Wait signal is sampled by fbclk, which is used for FEMC internal logic
- *wait_reg_mclk* – Wait signal is sampled by mclk, which is used for FEMC internal logic
- *data* – Bidirectional data (equal *FEMC_D*)
- *data_en* – Data output enable (0: data in 1: data out)
- *data_in* – Data input to FEMC (used for read data)
- *data_out* – Data output from FEMC (use for write data, or address in multiplexed mode)
- *read_data* – Read data sampled by mclk and used for FEMC internal logic

38.5.3.5.1 Asynchronous read

Table 38-2 shows an example of register settings for the asynchronous read:

Table 38-2 Asynchronous read register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	--	--	b000	0	<data width>	--	--	--	--	b001	--	b0011

Figure 38-4 shows a single asynchronous read transfer with an initial access time, t_{RC}, of 3 cycles and an output enable assertion delay, t_{CEOE}, of one cycle.

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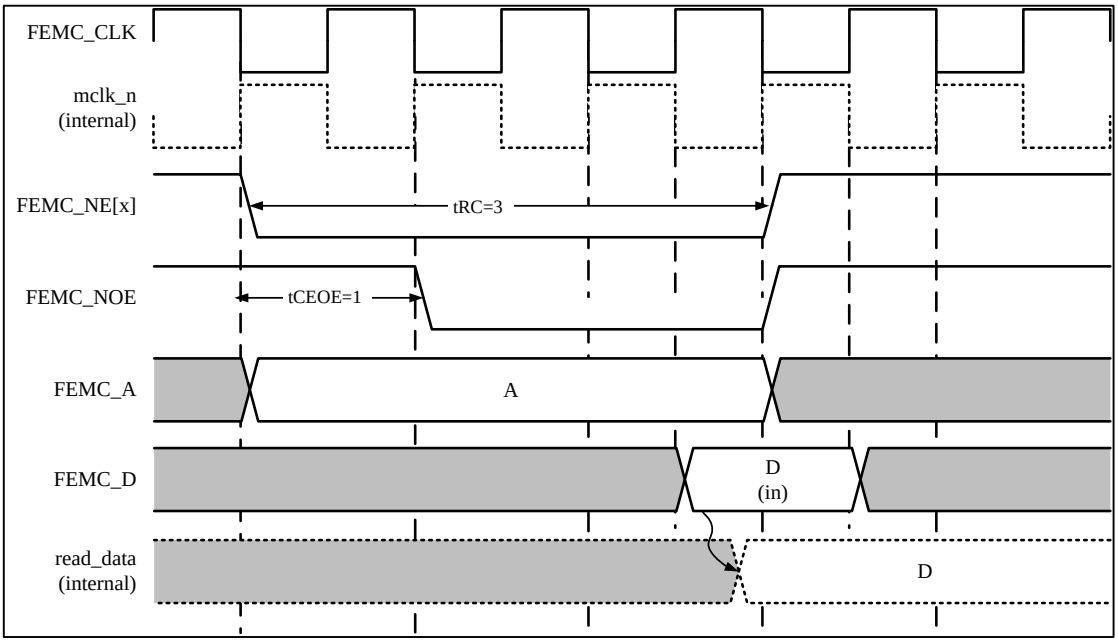
Figure 38-4 Asynchronous read



38.5.3.5.2 Asynchronous read in multiplexed mode

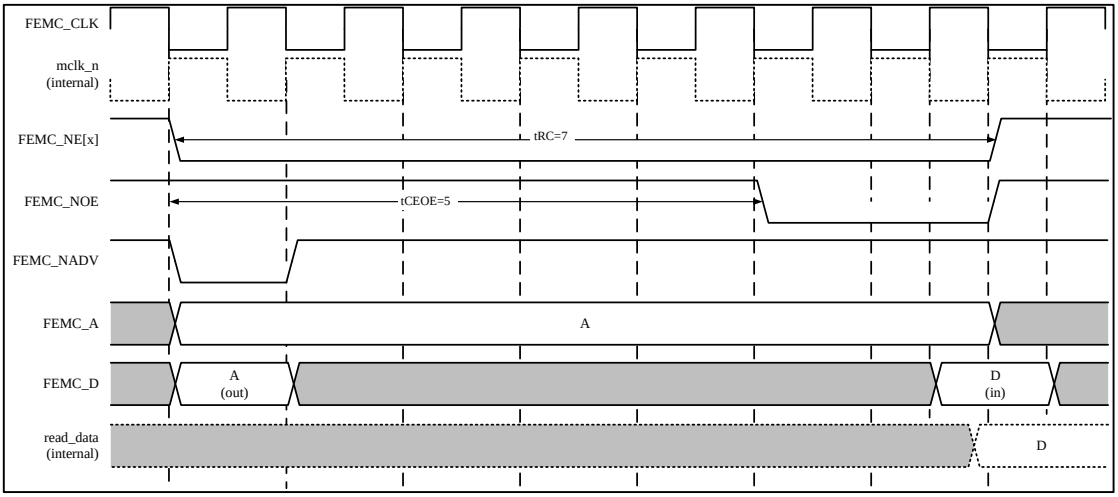
Table 38-3 shows an example of register settings for the asynchronous read in multiplexed mode:

Table 38-3 Asynchronous read (multiplexed mode) register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	1	--	--	--	b000	0	<data width>	--	--	--	--	b101	--	b0111

Figure 38-5 shows a single asynchronous read transfer in multiplexed SRAM mode, with t_{RC}=7, and t_{CEOE}=5.

Figure 38-5 Asynchronous read in multiplexed mode



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*NOTE: In multiplexed mode, both address and data are output by the FEMC on the **data_out** bus. Read data is accepted on the **data_in** bus. The address is still driven onto the address bus in multiplexed mode. This enables you to use the upper address bits for memories that require more address bits than data bits.*

38.5.3.5.3 Asynchronous write

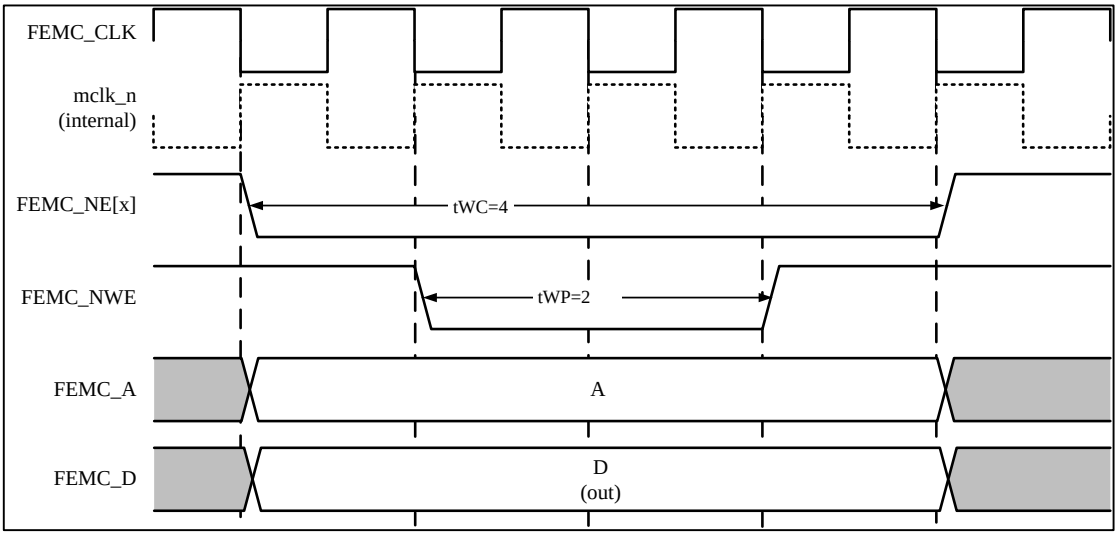
Table 38-4 shows an example of register settings for the asynchronous write:

Table 38-4 Asynchronous write register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	b000	0	--	--	<data width>	0	--	--	b010	--	b0100	--

Figure 38-6 shows an asynchronous write with a write cycle time t_{WC} of four cycles and a **we_n** assertion duration, t_{WP}, of two cycles.

Figure 38-6 Asynchronous write



*NOTE: The timing parameter t_{WP} controls the deassertion of **we_n**. You can use it to vary the hold time of **cs_n**, **addr** and **data**. This differs from the read case where the timing parameter t_{CEOE} controls the delay in the assertion of **oe_n**. Additionally, **we_n** is always asserted one cycle after **cs_n** to ensure the address bus is valid.*

38.5.3.5.4 Asynchronous write in multiplexed mode

Table 38-5 shows an example of register settings for the asynchronous write in multiplexed mode:

Table 38-5 Asynchronous write (multiplexed mode) register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC

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FEMC_OMCFG									FEMC_TCFG						
--	--	0	0	b000	0	--	--	<data width>	0, see Figure 38-7 1, see Figure 38-8	--	--	b100	--	b0111	--

Figure 38-7 shows an asynchronous write in multiplexed mode when the WECS bit is 0. t_{WC} is seven cycles, t_{WP} is four cycles, and the WECS bit programs the assertion of **we_n** to occur two clock cycles after **cs_n** goes LOW.

Figure 38-7 Asynchronous write in multiplexed mode when WECS is zero

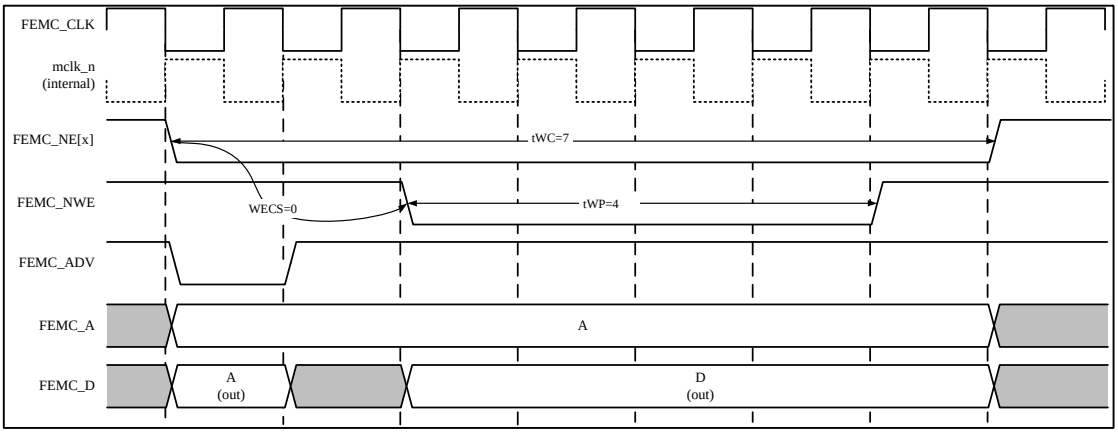
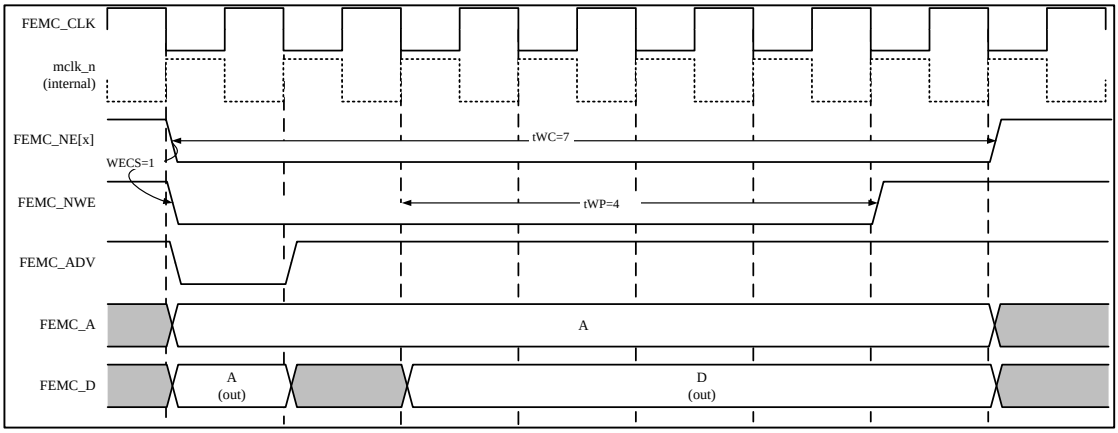


Figure 38-8 shows an asynchronous write in multiplexed mode when the WECS bit is 1. t_{WC} is seven cycles, t_{WP} is four cycles, and the WECS bit programs the assertion of **we_n** to occur when **cs_n** goes LOW.

Figure 38-8 Asynchronous write in multiplexed mode when WECS is one



38.5.3.5.5 Asynchronous page mode read

Table 38-6 shows an example of register settings for the asynchronous page mode read:

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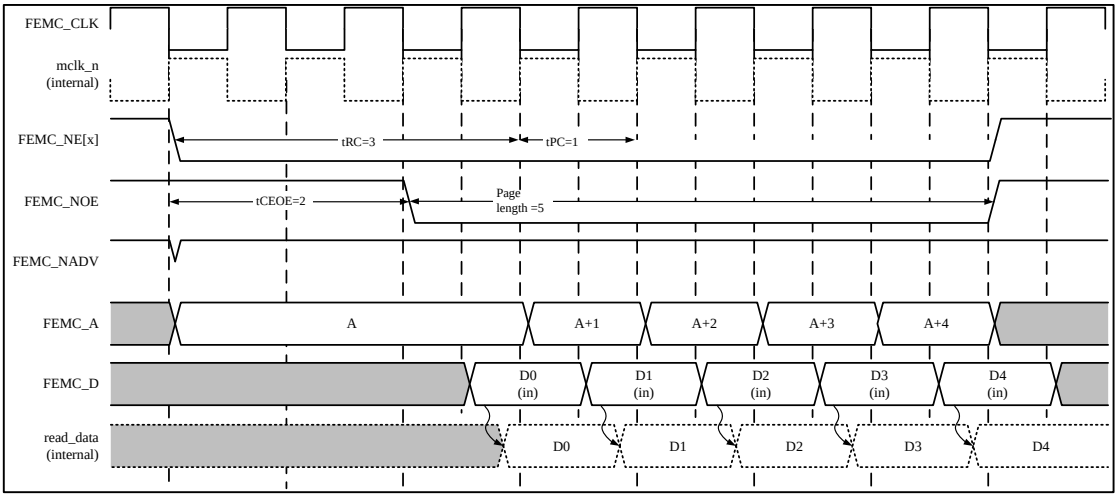
Table 38-6 Asynchronous page mode read register setting

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
1	--	--	--	--	--	<page length>	0	<data width>	--	--	b001	--	b010	--	b0011

Figure 38-9 shows a page read access, with an initial access time, t_{RC}, of three cycles, an output enable assertion delay, t_{CEOE}, of two cycles, and a page access time, t_{PC}, of one cycle.

User enables Page mode in the FEMC by setting the opmode Register for the relevant chip to asynchronous reads, and the burst length to the page size.

Figure 38-9 Asynchronous page mode read



NOTE: Multiplexed mode page accesses are not supported.

38.5.3.5.6 Synchronous burst read

Table 38-7 shows an example of register settings for the synchronous burst read:

Table 38-7 Synchronous burst read register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	1	--	--	--	<burst length>	1	<data width>	--	--	--	--	b010	--	b0100

Figure 38-10 shows a burst read with the **wait** output of the memory used to delay the transfer.

NOTE:

*Synchronous memories have a configuration register enabling **wait** to be asserted either on the same clock cycle as the delayed data, or a cycle early. The FEMC only supports **wait** being asserted one cycle early, enabling **wait** to be initially sampled with the fed-back clock and then with **mclk** before being used by the FSM. This enables the easiest*

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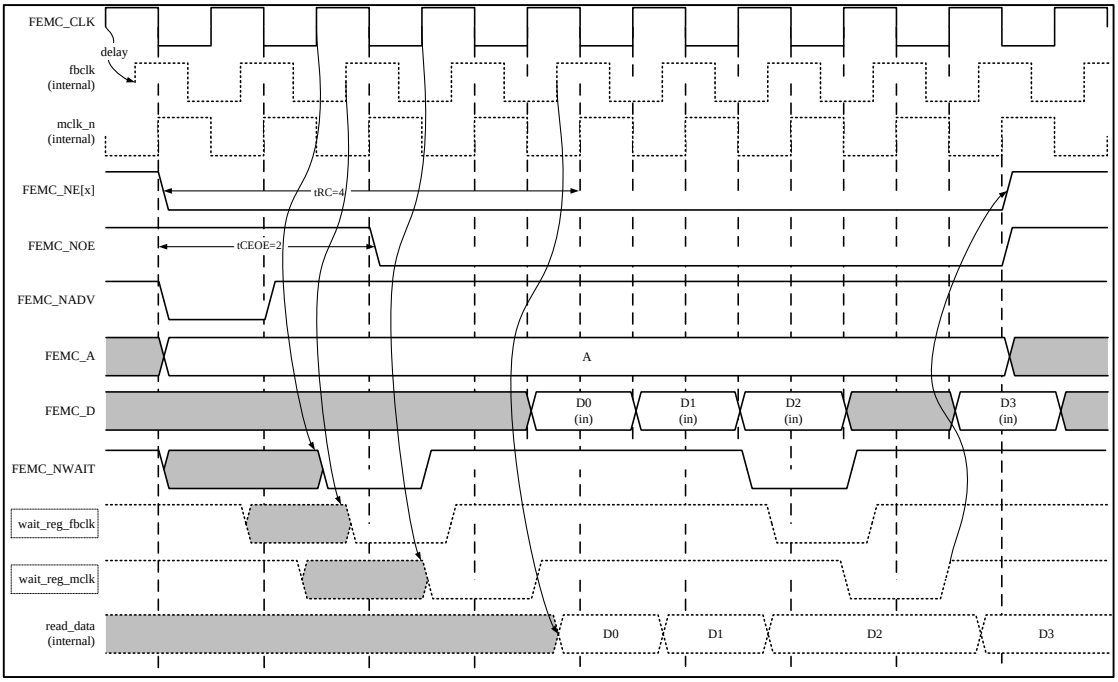
*timing closure. Additionally, you must configure the memory for **wait** to be active LOW.*

*In synchronous operation, the FEMC relies on the **wait** signal being deasserted HIGH to indicate that the memory can finish the transfer. When in synchronous mode, some memories do not deassert the **wait** signal during non-array read transfers. Non-array read transfers are typically status register reads. To avoid stalling the system with these memories, in synchronous mode you must not perform non-array read transfers with the memory and FEMC.*

*You must set t_{RC} to a value that enables **wait_reg_mclk** to stabilize.*

Figure 38-10 Synchronous burst read



38.5.3.5.7 Synchronous burst read in multiplexed mode

Table 38-8 shows an example of register settings for the synchronous burst read in multiplexed mode:

Table 38-8 Synchronous burst read (multiplexed mode) register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	--	--	<burst length>	1	<data width>	--	--	--	--	b010	--	b0100

Figure 38-11 shows the same synchronous read burst transfer as Figure 38-10, but in multiplexed mode.

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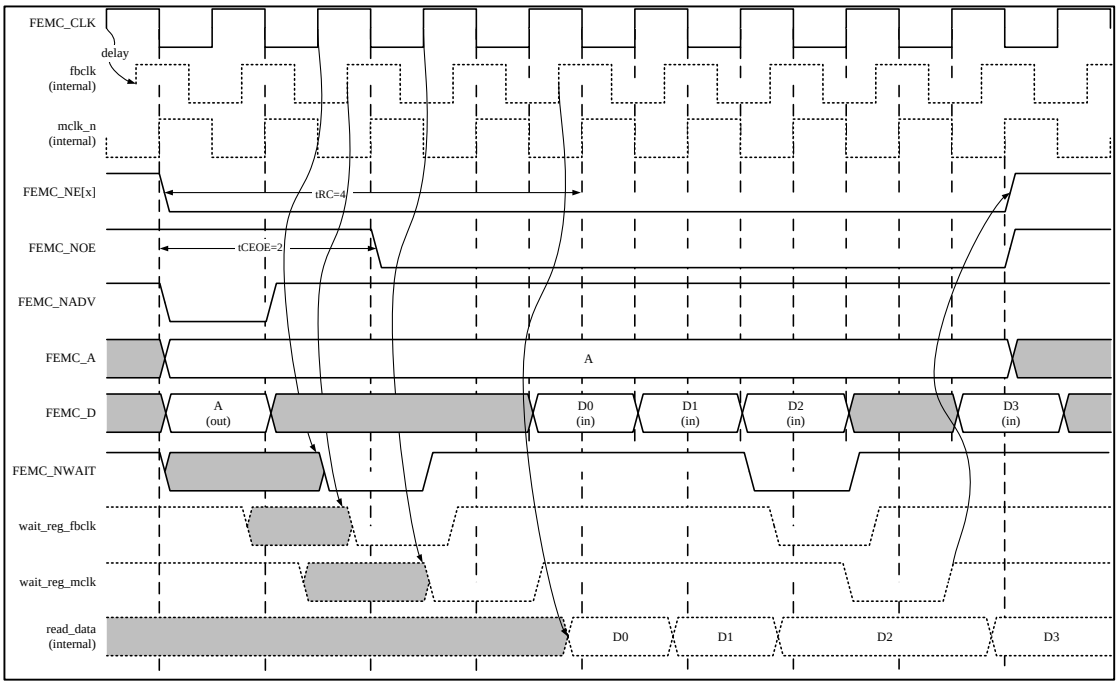
Figure 38-11 Synchronous burst read in multiplexed mode



38.5.3.5.8 Synchronous burst write

Table 38-9 shows an example of register settings for the synchronous burst write:

Table 38-9 Synchronous burst write register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	<burst length>	1	--	--	<data width>	0	--	--	b001	--	b0100	--

Figure 38-12 shows a synchronous burst write transfer that is delayed by the **wait** signal. You must configure the memory to assert **wait** one cycle early and with an active LOW priority. The **wait** signal is again registered with the fed-back clock and **mclk** before being used. The **wait** signal is used in the **mclk** domain to the memory interface FSM.

NOTE:

*Synchronous memories have a configuration register enabling **wait** to be asserted either on the same clock cycle as the delayed data, or a cycle early. The FEMC only supports **wait** being asserted one cycle early, enabling **wait** to be initially sampled with the fed-back clock and then with **mclk** before being used by the FSM. This enables the easiest timing closure. Additionally, you must configure the memory for **wait** to be active LOW.*

*You must set t_{WC} to a value that enables **wait_reg_mclk** to stabilize.*

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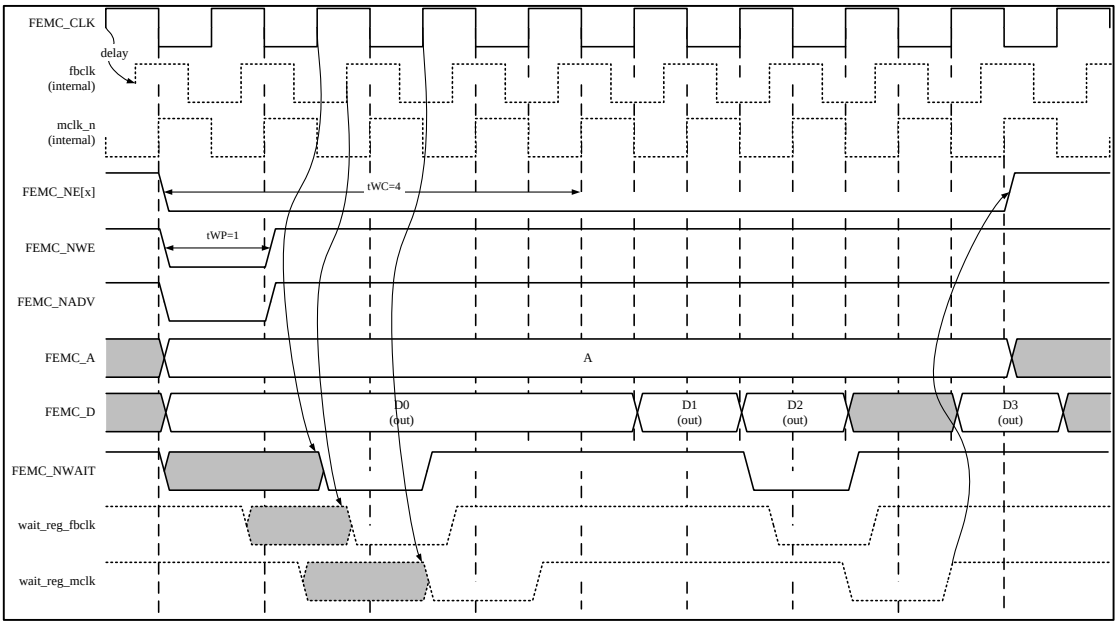
Figure 38-12 Synchronous burst write



38.5.3.5.9 Synchronous burst write in multiplexed mode

Table 38-10 shows an example of register settings for the synchronous burst write in multiplexed mode:

Table 38-10 Synchronous burst write (multiplexed mode) register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	1	--	<burst length>	1	--	--	<data width>	0	--	--	b001	--	b0100	--

Figure 38-13 shows the same synchronous burst write as Figure 38-12, but in multiplexed mode.

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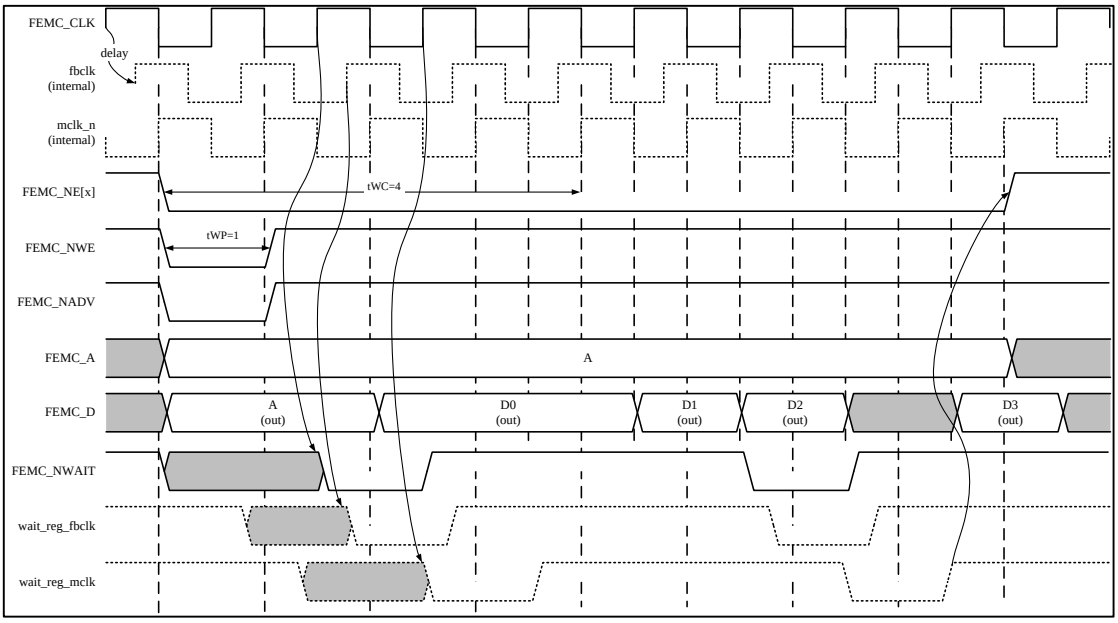
Figure 38-13 Synchronous burst write in multiplexed mode



38.5.3.5.10 Synchronous read and asynchronous write

Table 38-11 shows an example of register settings for the synchronous read and asynchronous write:

Table 38-11 Synchronous read and asynchronous write register settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	0	1	0	b000	0	b001	1	<data width>	--	b001	--	b001	b010	b0110	b0100

Figure 38-14 shows the turnaround time t_{TR}, enforced between synchronous read and asynchronous write. The turnaround time is enforced between:

- Reads followed by writes
- Writes followed by reads
- Read following a read from a different chip select
- Any two consecutive accesses in multiplexed address/data mode.

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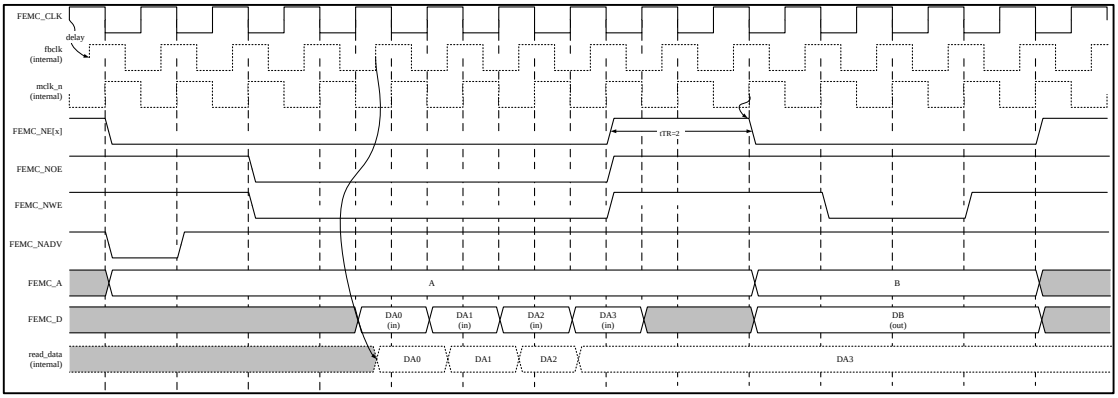
Figure 38-14 Synchronous read and asynchronous write



38.5.3.5.11 Programming t_{RC} and t_{WC} when the controller operates in synchronous mode

For t_{RC}:

- When using memory devices that are not wait-enabled, you must program t_{RC} to be the number of clock cycles required before valid data is available following the assertion of **cs_n**
- When using memory devices that are wait-enabled, you must program t_{RC} to be the number of clock cycles required before **wait** is active and stable, following the assertion of **cs_n**. That is: t_RC = 3 + t_CEOE

*NOTE: t_CEOE is only required if **wait** is asserted when **oe_n** goes LOW.*

For t_{WC}:

- When using memory devices that are not wait-enabled, you must program t_{WC} to be the number of clock cycles required before the first data is written, following the assertion of **cs_n**
- When using memory devices that are wait-enabled, you must program t_{WC} to be the number of clock cycles required before **wait** is active and stable, following the assertion of **cs_n**. That is: t_WC = 3

*NOTE: If a memory device is configured so that there are two or less clock cycles between the assertion of **wait** and data being required then you must program t_{WC} as if the memory device is not wait-enabled.*

38.5.3.5.12 Chip select assertion for SRAM memory interfaces

During repeated access to the same chip, the FEMC can keep chip select asserted. To support memories (e.g. PSRAM) that require chip select to be de-asserted periodically, you can program the REFPRD bit of FEMC Refresh Period Register to set a maximum number of consecutive memory bursts. You can set the number of consecutive bursts from one to 15, inclusive. See FEMC_RPE register.

38.5.4 NAND interface memory access

38.5.4.1 Two phase NAND accesses

The FEMC defines two phases of commands when transferring data to or from NAND flash:

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- **Command phase** : Commands and optional address information are written to the NAND flash. The command and address can be associated with either a data phase operation to write to or read from the array, or a status/ID register transfer.
- **Data phase:** Data is either written to or read from the NAND flash. This data can be either data transferred to or from the array, or status/ID register information.

The FEMC uses information contained in the AXI address bus, either **awaddr[ ]** or **araddr[ ]** signals, to determine whether the AXI transfer is a command or data phase access.

This information contained in the address bus additionally determines:

- The value of the command
- The number of address cycles
- The chip select to be accessed.

During a command phase transfer, the address to be written to the NAND memory is transferred to the FEMC using the AXI write channel.

NOTE: The size of the AXI transfer for data phase transfers must be larger than the width of the memory interface.

Table 38-12 shows the fields of **awaddr[ ]** and **araddr[ ]** signals that control a NAND flash transfer.

Table 38-12 NAND AXI address setup

AXI address	Command phase	Data phase
[31:24]	Chip address	Chip address
[23]	NoOfAddCycles_2	Reserved
[22]	NoOfAddCycles_1	Reserved
[21]	NoOfAddCycles_0	ClearCS
[20]	End command valid	End command valid(1)
[19]	0	1
[18:11]	End command	End command(2)
[10:3]	Start command	[10] ECC Last [9:3] Reserved
[2:0]	Reserved(3)	Reserved(3)

NOTE:

1. *For a read data phase transaction, the end command valid must be 0.*
2. *End command data is ignored if end command valid is not true.*
3. *The bottom three bits of a NAND access determine the valid data byte lanes, in the same way as for a standard AXI access.*

38.5.4.1.1 NAND command phase transfers

A command phase transfer is always performed as an AXI write. The AXI **awaddr[ ]** bus, and Table 38-12 contain

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the following information:

- **Address cycles:** The number of address cycles can be any value from zero to seven. Generally, up to five cycles are used during an array read or write, but a maximum of seven enables support for future devices.
- **Start command:** The start command is used to initiate the required operation, for example:
  - Page read
  - Page program
  - Random page read
  - Status or ID register read.
- **End command:** The value of the second command, if required. This command is executed when all address cycles have completed. For example, some NAND memories require an additional command, following the address cycles, for a page read.
- **End command valid:** Indicates whether the end command must be issued to the NAND flash.

Each address cycle consumes eight bits of address information. This is transferred to the FEMC through the AXI write channel.

NOTE: To ease system integration, the FEMC supports the use of multiple AXI write transactions to transfer address information. The following restrictions apply in this case:

1. *The AXI address [31:3] bits must not change between transactions. The first transaction must be double word aligned.*
2. *All other address information must be the same, with the exception of transaction length.*
3. *Data must be transferred in incrementing, consecutive accesses, that is, not wrapping, fixed, or sparse.*
4. *Extra or unused beats in the last transaction must have write strobes disabled.*
5. *Total number of beats must be less than the write FIFO depth.*

38.5.4.1.2 NAND data phase transfers

Transfers data to or from the NAND flash, and can be performed as either an AXI read or write, depending on the required operation. The **araddr[ ]** or **awaddr[ ]** bus, and Table 38-12 contain this information:

- **End command:** The value of a command that is issued following the data transfer. This is required by some memories to indicate a page program following input of write data.

NOTE: End commands are not supported for read data phase transfers.

- **End command valid:** Indicates whether the end command must be issued to NAND flash.
- **ClearCS:** When set, the chip select for a NAND flash is deasserted on completion of this command. When not set, the chip select remains asserted.
- **ECC Last:** When set, this bit indicates to the ECC block that the current command is the last access to the NAND page. It is ignored if the ECC block is not enabled.

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A NAND flash data phase program or read operation is expected to require multiple AXI transfers because of the large page size of NAND memories. Some memory devices require the chip select to remain asserted for the duration of a page access. The FEMC keeps the chip select asserted for the:

- **Command phase to data phase transition**
  - When the bit CSL of FEMC NAND Mode Register is set to HIGH.
- **Data phase to data phase transitions**
  - When the ClearCS is not set. The FEMC asserts the chip select while multiple AXI transfers transfer data to or from the NAND flash internal page. On the last AXI transfer, you can deassert the chip select by setting the ClearCS bit.

Figure 38-15 and Figure 38-16 show the steps taken to perform NAND flash page read and page program operations respectively.

Figure 38-15 NAND flash page read operations

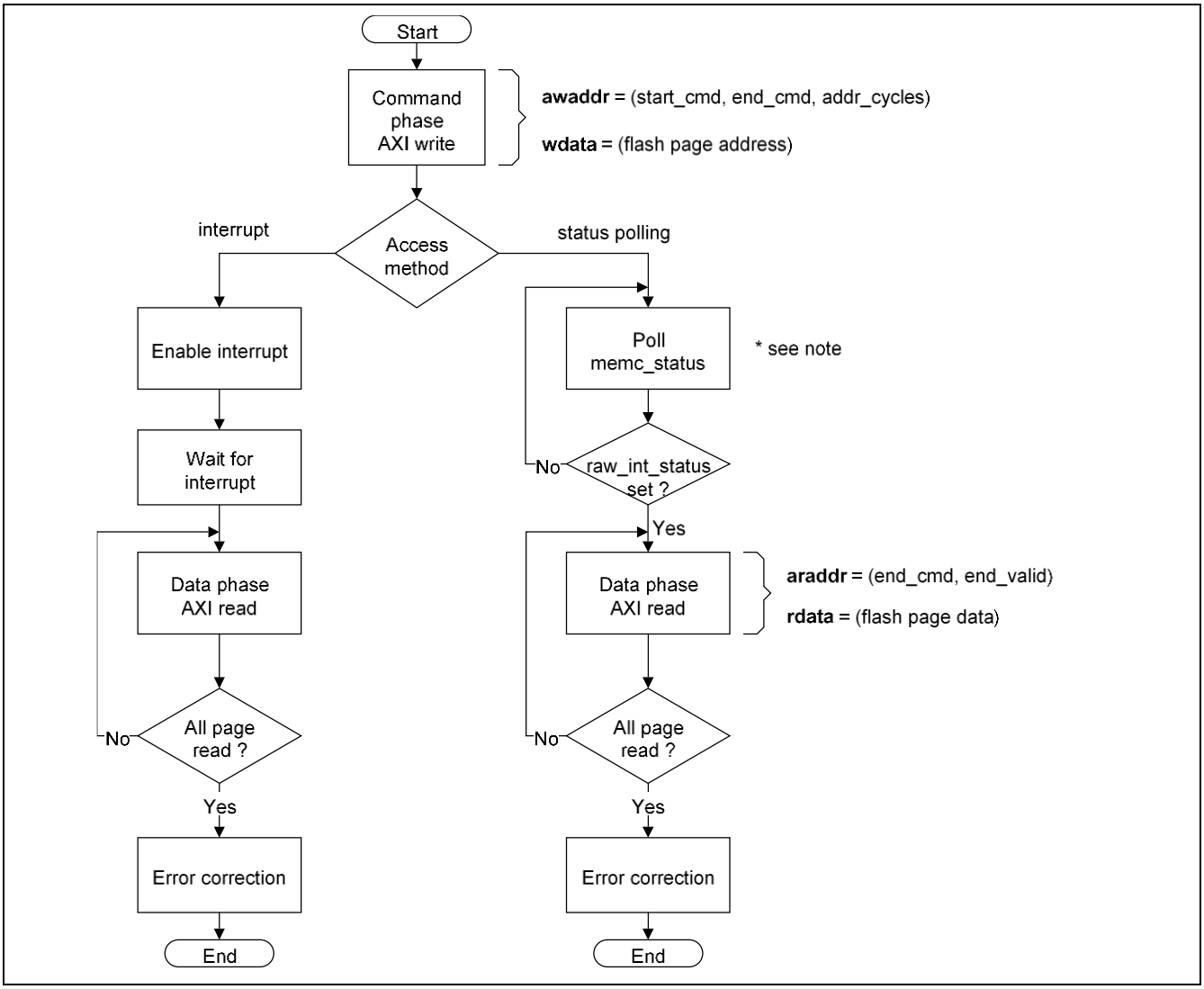

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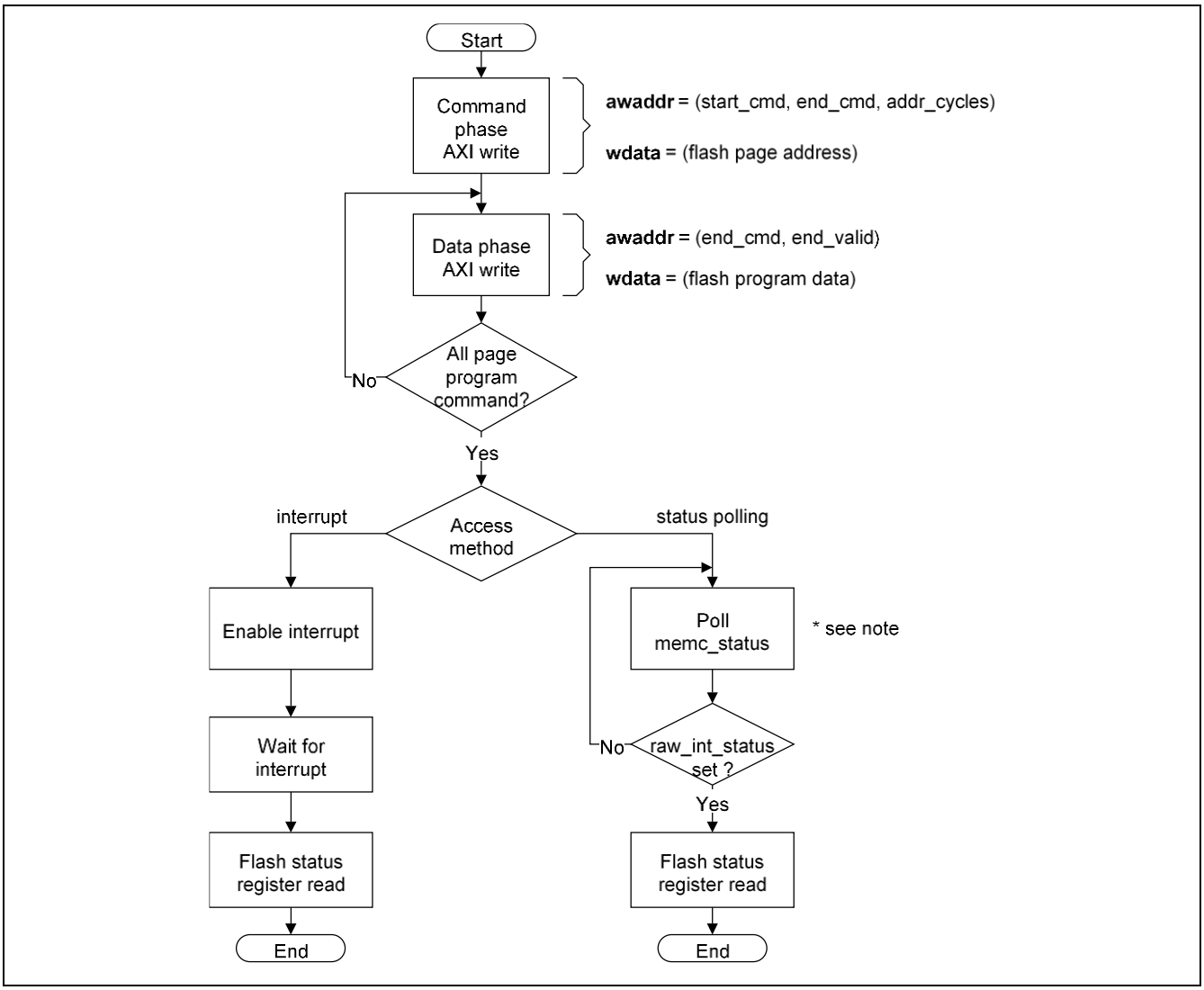
Figure 38-16 NAND flash page program operations



NOTE: You can poll for either a page program or page read completion in two ways:

1. *Poll the raw_int_status bit in the memc_status Register to determine when the memory **busy_<x>** output has gone HIGH, indicating a page program completion or read data ready.*
2. *In a system with multiple NAND flash devices connected to the FEMC. The **busy** outputs are wire-ANDed to produce the single **busy_<x>** input to the FEMC, that only transitions HIGH when all devices have completed. You can determine the status register of each NAND chip by reading the individual device status register.*

Figure 38-17 shows the steps taken to perform a NAND flash status register read.

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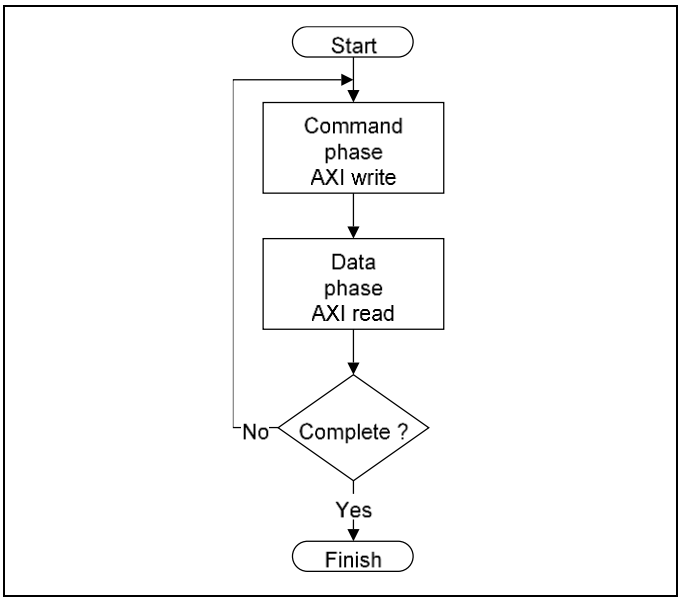
Figure 38-17 NAND flash status register read



The process boxes that Figure 38-17 shows are defined as:

- **Command phase AXI write**

  awaddr = (start_cmd = STATUS_READ_CMD,

  end_cmd = 0x0,

  end_valid = 0x0,

  addr_cycles = 0x0)

  NOTE: Ensure burst length is 1, ***awlen*** *= 0x0.*

  wdata = (don't care).

- **Data phase AXI read**

  araddr = (ClearCS = 0x1).

  NOTE: Ensure burst length is 1, arlen = 0x0. The transfer size is eight or sixteen, arsize = 0x0 or 0x1.

  rdata = NAND flash status output.

NOTE:Certain NAND flash devices can support multiple status register reads without reissuing the STATUS_READ_CMD. In this case, you can modify the flow that NAND flash status register read describes to include multiple data phase transfers for each command phase transfer.

Similar to SRAM interface memory access, the upper byte of the address read or write bus, **Address[31:24]** and the value of the **ADDRMCH[7:0]** and **ADDRMSK[7:0]** bits of the **Set Address Registers** determine the chip select being accessed, based on following formula:

– **Address[31:24]** & **ADDRMSK[7:0]** must equal **ADDRMCH[7:0]**

The values for the **ADDRMCH** and **ADDRMSK** buses must be set so that no address maps onto more than one chip,

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otherwise the behavior of the FEMC is undefined. If an AXI access does not map to any memory device then the FEMC performs an asynchronous transfer on memory interface 1 with all chip selects deasserted. After the transfer completes, the FEMC provides an OKAY response.

38.5.4.2 NAND interface timing diagrams

All NAND control and data outputs are registered on the rising edge of **mclkn**, which is equivalent to the falling edge of **mclk**. Additionally, read data from the memory device is registered by the FEMC on the rising edge of **mclkn** before being pushed onto the read data FIFO.

NOTE: This section does not describe the settings for the FEMC_OMCFG register, because for NAND devices you can only program the memory width field.

The following apply to NAND accesses:

- **Command phases:** When issuing a command phase access with address cycles = 0, you must always enable at least one byte lane.
- **Data phases:** Read data phases cannot have end commands associated with them.

*NOTE: The internal signal **read_data** is included in the read transfer waveforms to indicate the clock edge on which data is registered by the FEMC*

38.5.4.2.1 Command phase access

Table 38-13 shows an example of register settings for NAND flash address input:

Table 38-13 NAND flash address input settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	--	--	--	--	<data width>	--	--	--	b001	--	b0010	--

Figure 38-18 shows an address input phase. The cycle time t_wc is set to two, and the **we_n** assertion duration, t_wp, is set to one. The address consists of three cycles, and the second command is also required.

Figure 38-18 NAND flash address input

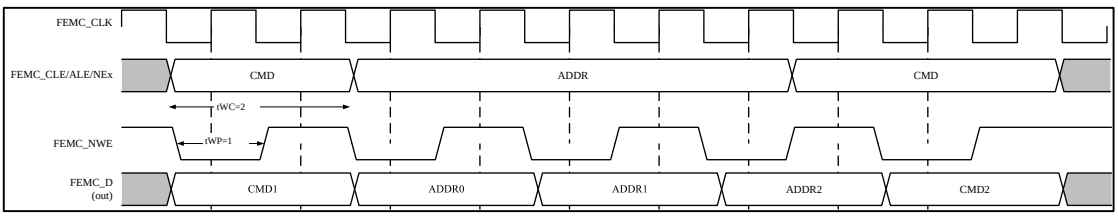

Table 38-14 shows example **awaddr** fields for NAND flash address input.

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Table 38-14 NAND flash address input example awaddr fields

awaddr bits	Value	Description
[31:24]	Chip select	-
[23:21]	b011	Three address cycles
[20]	1	End command required
[19]	0	Command phase transfer
[18:11]	CMD2	-
[10:3]	CMD1	-
[2:0]	b000	Address alignment

38.5.4.2.2 Data phase access

Table 38-15 shows an example of register settings for NAND flash read:

Table 38-15 NAND flash read settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	--	--	--	--	<data width>	--	--	--	--	b010	--	b0011

Figure 38-19 shows a read from NAND flash. The cycle time is set to three and the **re_n** assertion delay to two cycles. Three data items are read.

Figure 38-19 NAND flash read

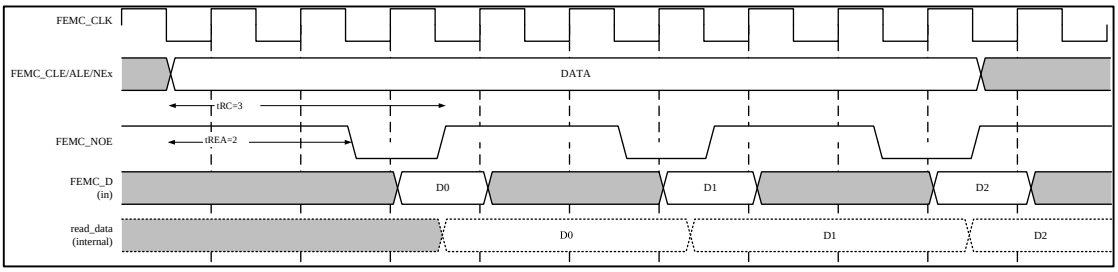

Table 38-16 shows example **araddr** fields for NAND flash page read.

Table 38-16 NAND flash page read example araddr fields

araddr bits	Value	Description

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[31:24]	Chip select	-
[23:22]	b00	Reserved
[21]	1	Last transfer, deassert chip select when complete
[20]	0	End command required
[19]	1	Data phase transfer
[18:11]	CMD2	-
[10]	0	ECC Last
[9:3]	b000_0000	Reserved
[2:0]	b000	Address alignment

38.5.4.2.3 Command-to-data phase access timing

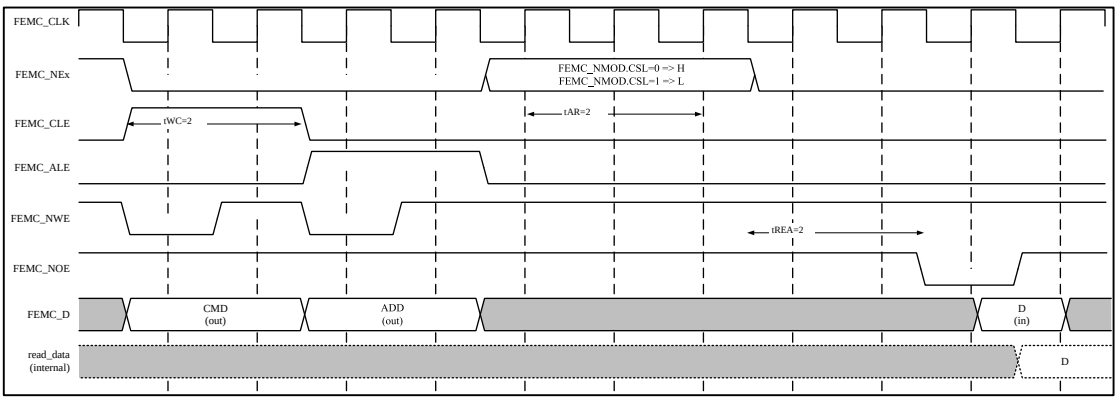
Table 38-17 shows an example of register settings for the address latch to data phase:

Table 38-17 Address latch to data phase settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	--	--	--	--	<data width>	--	b010	--	b001	b010	b0010	b0011

Figure 38-20 shows that t_{AR} is the number of extra cycles delay between address latch (**ale**) falling and the start of a new data phase command.

Figure 38-20 Address latch to data phase command



When booting from NAND with **BOOTEN** bit of FEMC NAND Mode register set to HIGH, t_{RR} is the number of extra cycles delay between the synchronization of the **busy** signal and the start of the next data phase command as

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Figure 38-21 shows.

Figure 38-21 Busy synchronization to data phase command

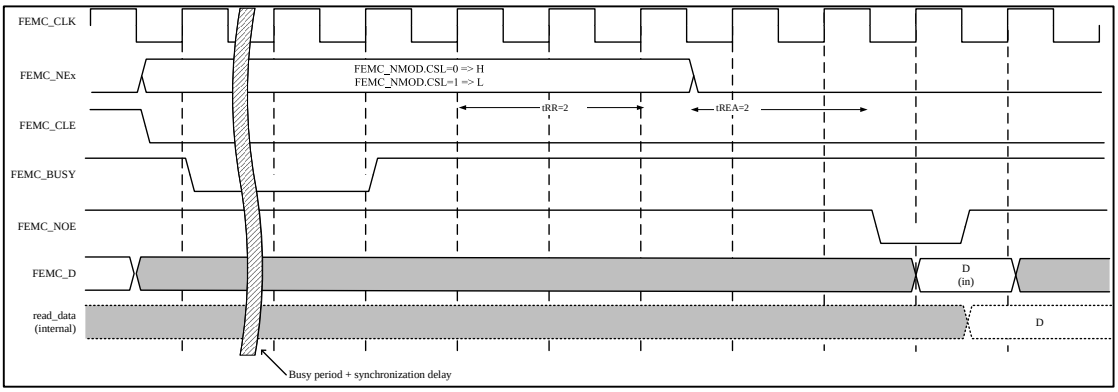
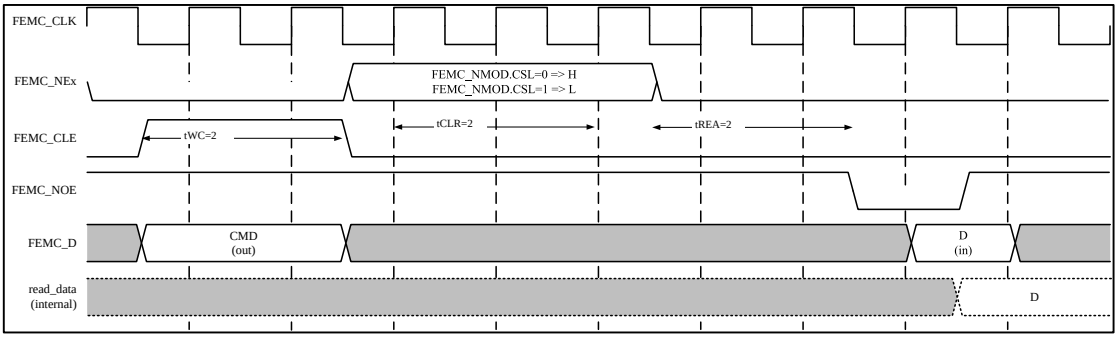


Figure 38-22 shows the t_{CLR} delay that is the number of extra cycles delay between a command being latched, **cle** HIGH, and the start, **CS** asserted, of a data phase command.

Figure 38-22 Command latched to data phase command



NOTE: The t_{CLR} delay is applied before both read and write data phase commands.

38.5.4.2.4 Data-to-command phase access timing

Table 38-18 shows an example of register settings for the data phase to command phase:

Table 38-18 Data phase to command phase settings

FEMC_OMCFG									FEMC_TCFG						
BSTAGN	BLSS	ADV	BAA	WRBL	WRSYN	RDBL	RDSYN	MDBW	WERR	TRAR	PCCLR	WP	CERE	WC	RC
--	--	--	--	--	--	--	--	<data width>	b0010	--	--	b001	b001	b0010	b0010

The FEMC also uses t_{RR} for the number of cycles delay between the data phase command and the assertion of the other data strobe, that is, either between:

- A write data phase and the next assertion of **re_n**

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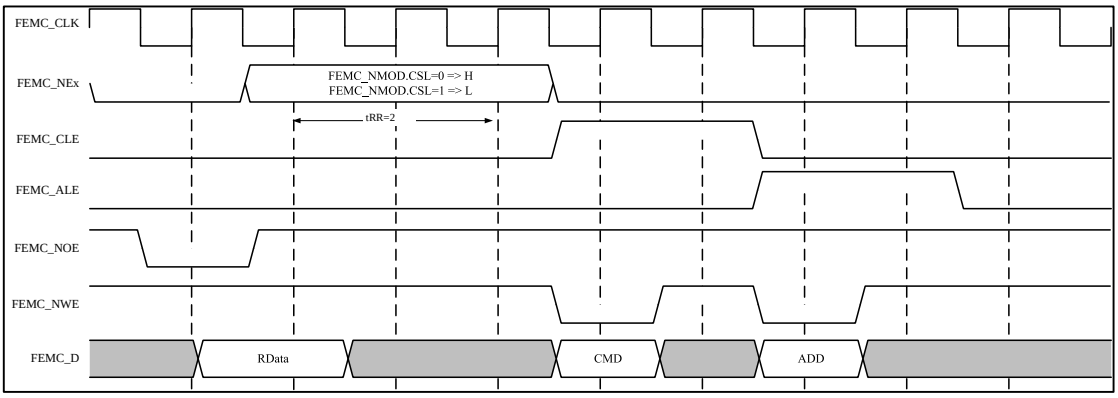
– A read data phase and the next assertion of **we_n** as Figure 38-23 shows.

Figure 38-23 Read data phase to command phase



NOTE: Figure 38-21 and Figure 38-23 show that the FEMC uses t_{RR} in two different ways. After you determine both values for t_{RR} you must program t_{RR} with the larger of the two values.

38.5.4.3 NAND transaction format

The transactions for NAND devices require some specific manipulation to format the transaction into the correct format for the FEMC to map the transaction correctly to the NAND device.

Figure 38-24 to Figure 38-27 show how a device driver is required to format the NAND command for the FEMC:

For a command phase access, the NAND memory address is passed as data, see Table 38-12 for a definition of how the address must be formatted. For a data phase access, the data is passed on the data bus.

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Figure 38-24 NAND read format example (1/2)

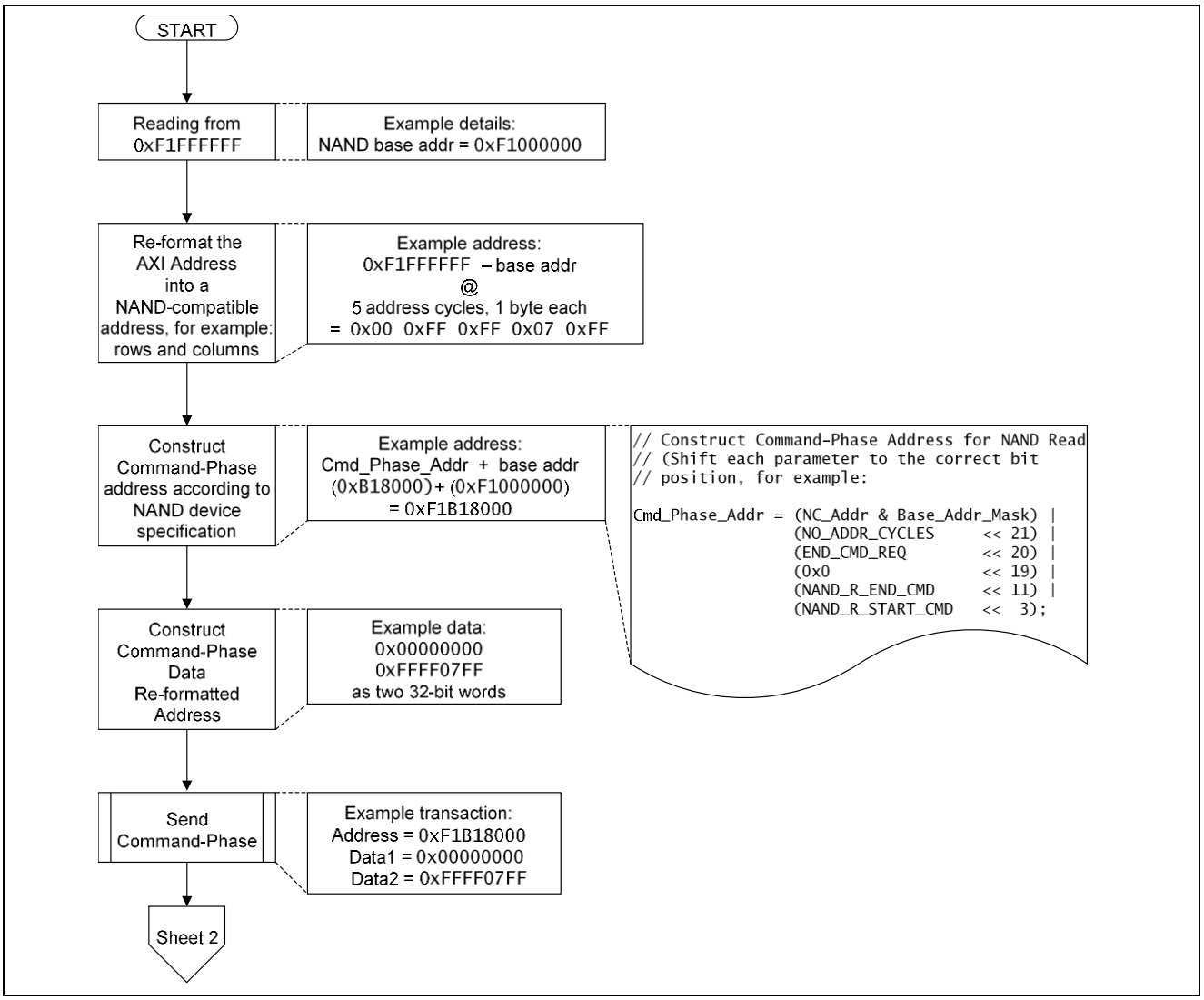

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Figure 38-25 NAND read format example (2/2)

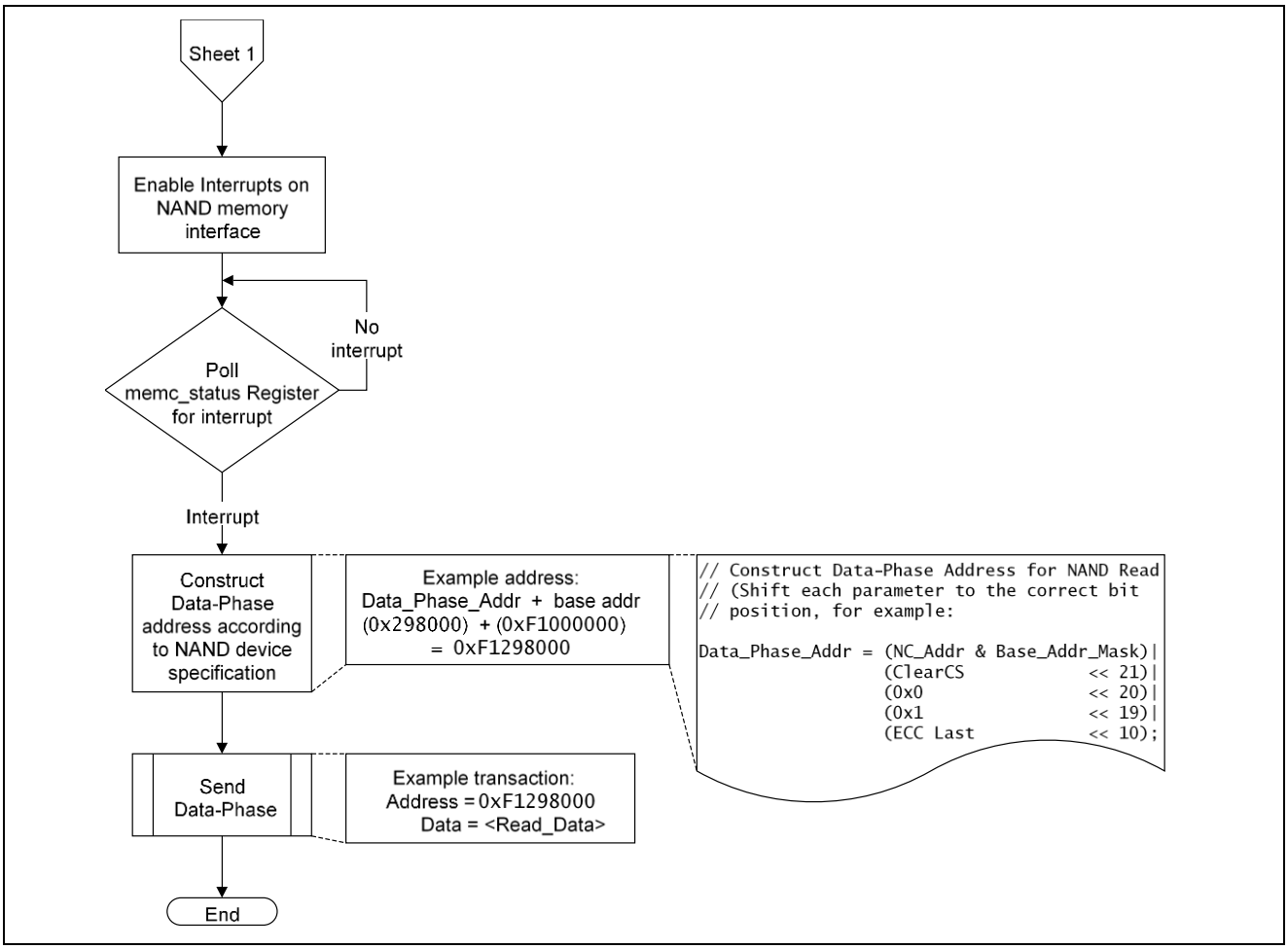

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Figure 38-26 NAND write format example (1/2)

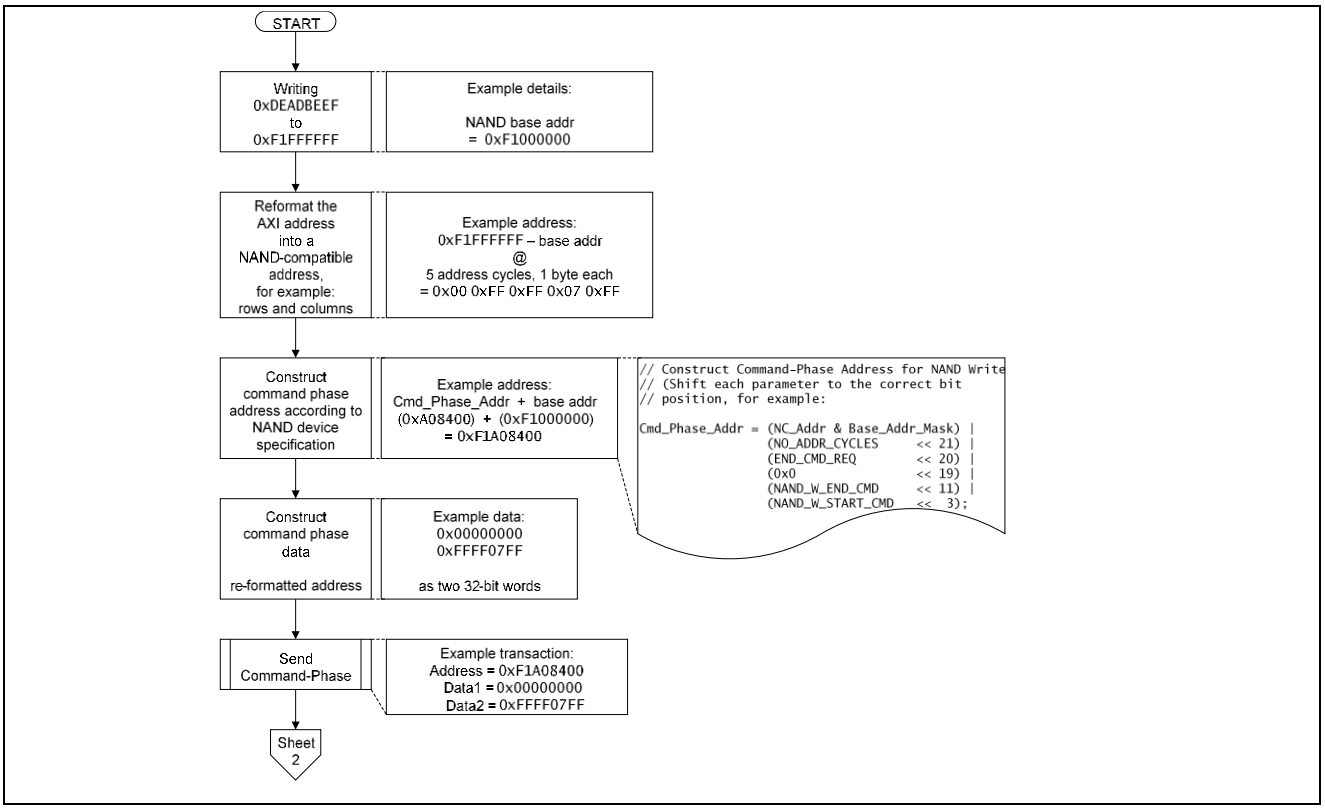

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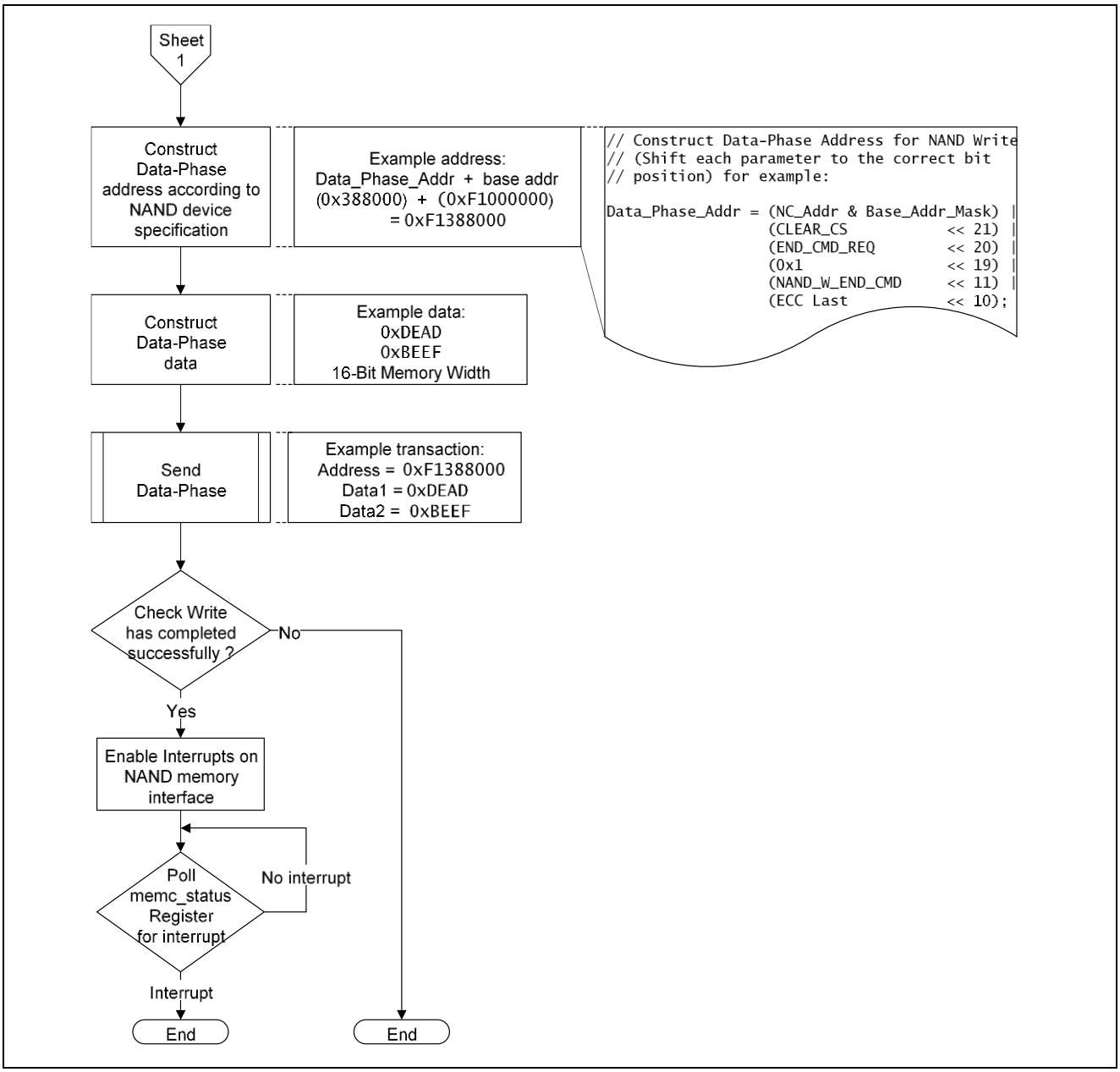
Figure 38-27 NAND read format example (2/2)



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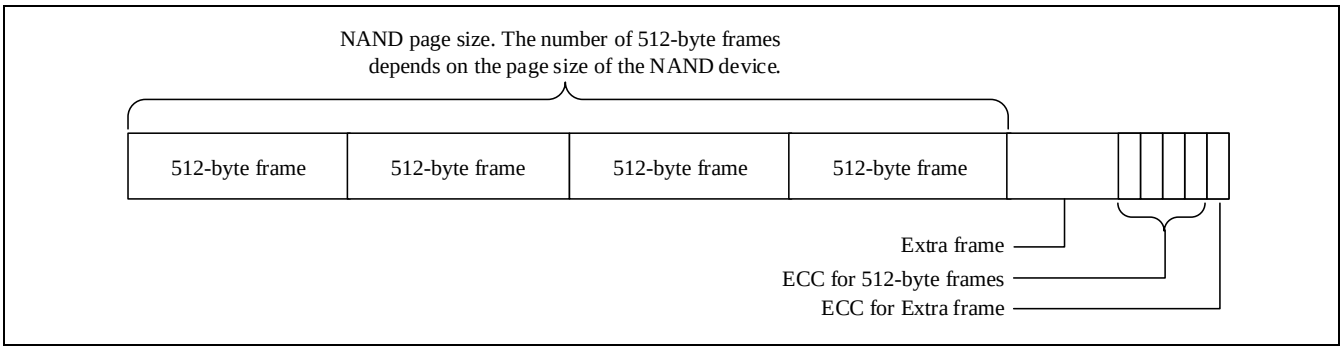
38.5.5 Error Correction Code (ECC)

An ECC block can be included for each NAND interface at the configuration stage. It operates on a number of 512-byte frames of NAND memory and can be programmed to store the ECC codes after the data in memory. For writes, the ECC is written to the spare area of the page. For reads, the result of a frame ECC check are made available to the device driver.

NOTE: Because there is no standard interface for NAND memory devices, it is important to know the characteristics of a particular memory type, before you enable the FEMC to use ECC functionality.

A configuration option enables an extra frame of 4, 8, 16, or 32 bytes to be included at the end of the page, before the start of the ECC data. Figure 38-28 shows the ECC block structure in memory.

Figure 38-28 ECC block structure



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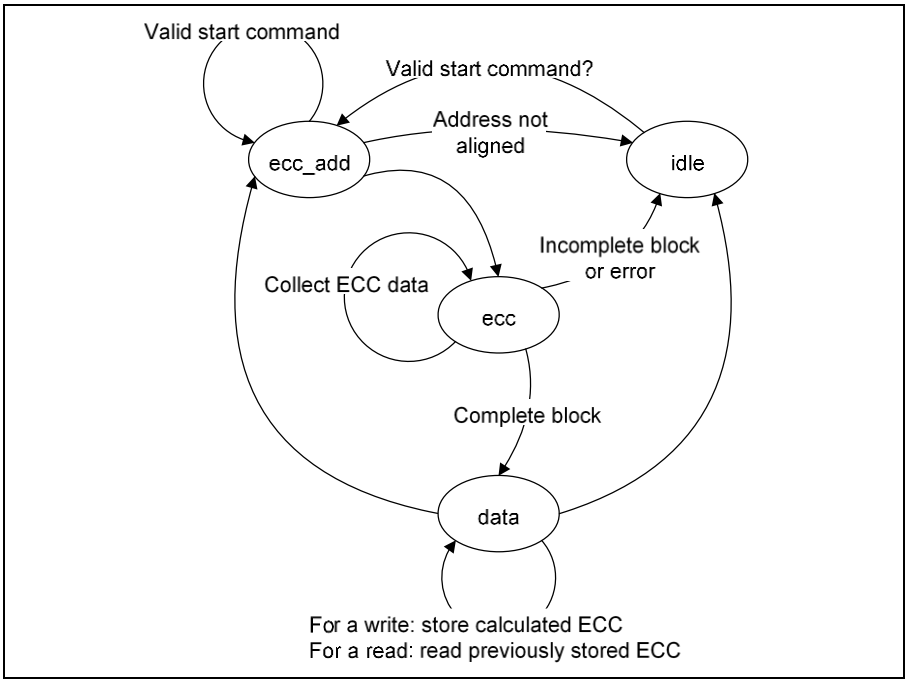
38.5.5.1 Operation

The ECC calculation uses a simple *Hamming* code, using 1-bit correction 2-bit detection. It starts when a valid read or write command with a 512-byte aligned address is detected on the memory interface, and the block is enabled using the NAND ECC Configuration Register. Values stored in the NAND ECC Command0 Register and the NAND ECC Command1 Register are used to detect the start of an address phase access.

Figure 38-29 shows an overview of how the ECC operates.

Figure 38-29 ECC state diagram



A 24-bit ECC value is generated for each 512-byte frame and a shorter code between 10 and 16 bits for the extra frame.

NOTE: For a 16-bit interface, ECC values are written to memory aligned to 16-bit boundaries.

Figure 38-30 shows the basic operation with no reading ECC values between blocks.

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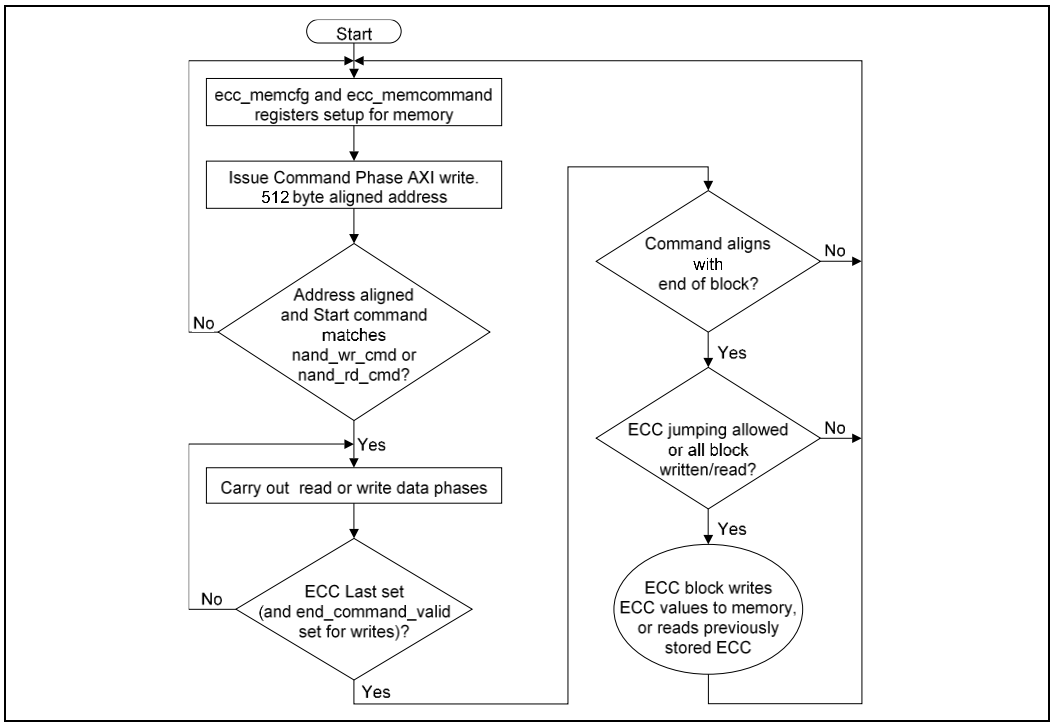
Figure 38-30 ECC Basic operation



38.5.5.2 Addressing

The ECC block supports two addressing modes. This must be set correctly for the type of memory in use, because it is used when generating addresses to move around the NAND page, and for detecting 512-byte aligned addresses.

38.5.5.2.1 Normal mode addressing

The normal mode, setting the ecc_ignore_add_eight bit to 0, expects the first two bytes to contain just the column address bits as Table 38-19 shows.

Table 38-19 Normal mode addressing

Cycle	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	L_a	L_a	L_a	L_a	A11[b]/L	A10	A9	A8
3rd-7th				Don’t care				

a. These bits must be LOW; otherwise, the behavior is undefined.

b. A11 might be present, depending on the memory width.

This mode supports all random access, column change commands, and up to four 512-byte frames. See 38.5.5.4 Address jumping.

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38.5.5.2.2 Secondary mode addressing

The secondary mode, setting the ecc_ignore_add_eight bit to 1, supports memories with 512 bits where the address formatting is as Table 38-20 Secondary mode addressing shows.

Table 38-20 Secondary mode addressing

Cycle	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	Don't care							
3rd-7th	Don't care							

NOTE: In this mode, A8 is passed as part of the start command and is not present in the data.

In this mode, random accesses are not possible. The nand_rd_col_change field in the *NAND ECC Command1 Register* can be used as an alternative read start command. This enables ECC calculation on just the extra frame at the end of the page.

For writes, issuing a zero address cycle, pointer change command, that matches the *nand_rd_col_change* command, tells the ECC block that the next write command is to the extra bits. This only applies to the subsequent write command, even if the memory only requires one pointer access for multiple writes.

38.5.5.3 Data

When a valid start address has been sent, data can be read or written using a series of NAND data phase commands. See 38.5.4.1.2 NAND data phase transfers. The last access must align with the end of a 512-byte frame, or the extra frame if it is enabled. You must set ECC Last on the last data phase access, to tell the ECC block not to expect any more data.

If an access to a different chip is received during an ECC operation, the ECC block aborts and sets the ecc_last_status field in the *NAND ECC Configuration Register* to indicate *Data stop after incomplete block*. No more ECC data is read or written to memory.

38.5.5.4 Address jumping

To enable you to write individual 512-byte frames, or the ECC extra frame, the FEMC can issue address phase commands to move around the NAND page.

The ecc_jump field in the *NAND ECC Configuration Register* controls how the FEMC jumps to the correct place in memory. You can program ecc_jump to:

38.5.5.4.1 Jump using full command

The FEMC uses the commands stored in the ecc_memcommand1 Register to control the NAND address pointer. It also uses these commands to detect the start of a NAND read or write. See NAND ECC Command 0 Register.

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38.5.5.4.2 Jump using column change commands

The FEMC uses the commands stored in the ecc_memcommand2 Register. The value used as the end command for a write access is taken directly from the previous AXI command that had the end_command_valid bit asserted. See NAND ECC Command 1 Register.

38.5.5.4.3 No jumping

The FEMC only reads or writes ECC data at the end of a page.

The ECC values for writes are only written to memory after the end command is received. For reads, the ecc_read_end bit setting can be used to read ECC data from memory between every frame.

38.5.5.5 Address modes

The following sections describe the different methods used to control the address pointer, when writing ECC values:

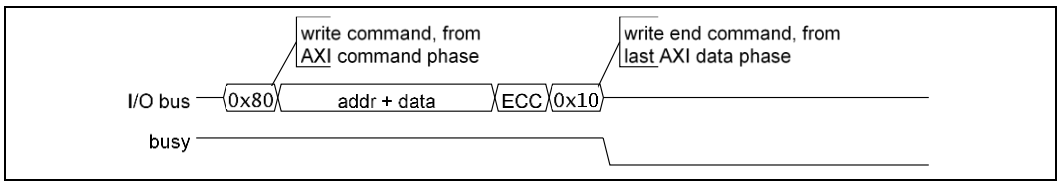
- *ecc_jump = no jumping*
- *ecc_jump = column change*
- *ecc_jump = full command* on page 2-47
- *ignore_add_8 and ecc_jump is not no_jump* on page 2-47.

NOTE: The same methods can be applied to reads, except that end commands may be output after the address, if enabled in the NAND ECC Command n Registers, but never after a data transfer.

38.5.5.5.1 ecc_jump = no jumping

If the ecc_jump field is set to no jumping, and not all frames in a page are read or written, then an error is generated. However, the calculated ECC values are available in the *NAND ECC Block Register*. If required, you can then use software to write them to memory. See Figure 38-31.

Figure 38-31 Every block is written



NOTE: The command values shown in these diagrams, for example 0x80, 0x10, or 0x15, are representative and may not match your particular NAND device.

38.5.5.5.2 ecc_jump = column change

If the ecc_jump field is set to column change commands, the FEMC issues a col_change command, with two address cycles. See Figure 38-32.

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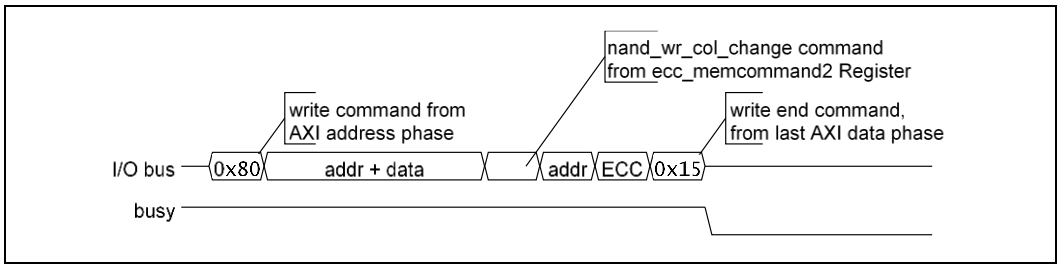
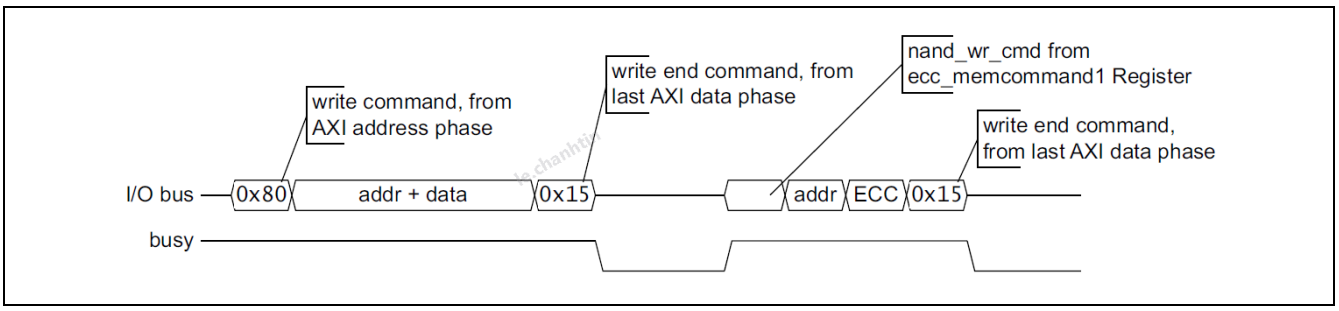
Figure 38-32 Not every block written, random access



38.5.5.5.3 ecc_jump = full command

If a full command is used, the FEMC issues an entire new command phase access with the same number of address cycles as the initial write. See Figure 38-33.

Figure 38-33 Full jumping



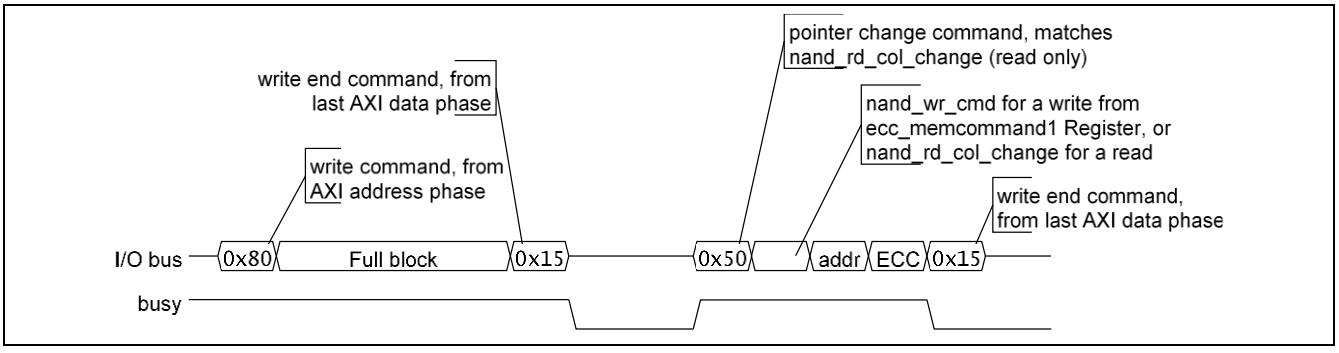
NOTE:

- *If the ecc_jump field is set to use full commands, this counts against the maximum number of program operations before a NAND page must be erased.*
- *If the ecc_read_end bit is set to read between frames, then each boundary must be aligned with the end of a data phase access. Otherwise, data phases accesses can cross boundaries between frames.*

38.5.5.5.4 ignore_add_8 and ecc_jump is not no_jump

If not all frames are written, the FEMC issues a pointer change command using the value in the nand_rd_col_change field of the *NAND ECC Command1 Register*. For reads, the nand_rd_col_change field is used instead of the standard read command, to access the extra bits at the end of the page. See Figure 38-34.

Figure 38-34 addressing mode ignore_add_8 with extra blocks



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NOTE: After writing or reading ECC values in the secondary addressing mode, see Secondary mode addressing*, the ECC block does not return the pointer to its previous state. Software might have to correct the pointer, depending on the memory and if the ECC block was forced to jump into the extra data area.*

38.5.5.6 Cache mode accesses

If performing cache mode reads, the entire page must be read and ECC Last only issued on the last data phase access of the last page. Undefined behavior occurs if you attempt to read data beyond the page size.

NOTE:

- *The ecc_jump field must be set to no jump to prevent the FEMC from attempting to move the address pointer around the cache register.*
- *If multiple pages are read, then the software must maintain a count of the number of pages. All block valid and read flags* are cleared when the first frame of a new page is read.

38.5.5.7 Error codes

The error code available from the NAND ECC Status Register applies to the previous ECC operation. It must only be considered valid when the ECC block is not busy.

38.5.5.8 ECC Interrupts

Interrupts can be generated:

- When the ECC block detects an error on a read.
- When the ECC data is read from memory, if the ecc_int_pass bit is set in the NAND ECC Configuration Register.
- When an error occurs, if the ecc_int_abort bit is set in the NAND ECC Configuration Register.

Interrupts can be cleared by:

- Writing to the interrupt flag in the NAND ECC Status Register.
- Writing any value to the appropriate NAND ECC Block Register.

NOTE: To enable the external interrupt, the ecc_int_enable0 or ecc_int_enable1 bits must be set using the FEMC Configuration Register.

38.5.5.9 Correcting errors

The FEMC identifies the occurrence and location of errors so that software can correct those errors.

If an error occurs, the ecc_fail bit for that frame is set in the FEMC Status Register 1. If the error is correctable, then the ecc_correct bit is set in the corresponding NAND ECC Block Register and the ecc_value field provides the location of the bit that must be corrected.

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Table 38-21 shows the decoded meaning of the ecc_fail bit and the ecc_correct bit.

Table 38-21 ecc_fail bit and ecc_correct bit encoding

ecc_fail bit	ecc_correct bit	Meaning
0	0	No error
0	1	Parity error
1	0	Multiple error
1	1	Single error

The bottom three bits in the ecc_value field provide the bit number, and the remaining 21 bits indicate which byte contains an error. For example, an ecc_value of 0x101 indicates that bit 1 of byte 32 is incorrect.

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38.5.6 Interrupts

This IP has only one interrupt signal (femc_int) which is combined of each memory interface interrupt and ECC interrupt.

The interrupt is triggered on the rising edge of:

1. the **int** input for the SRAM memory interface type, or
2. the **busy** input for the NAND memory interface type, or
3. ECC interrupt (only NAND memory interface)

It is clear when all interrupt sources are clear:

1. For interrupt generated by **int** input: it is clear when there is next AXI Read issued to SRAM memory interface type, or write to the appropriate bit in the Clear Configuration Register.
2. For interrupt generated by **busy** input: it is clear when there is next AXI Read issued to NAND memory interface type, or write to the appropriate bit in the Clear Configuration Register.
3. ECC interrupt is clear by writing to corresponding register bit

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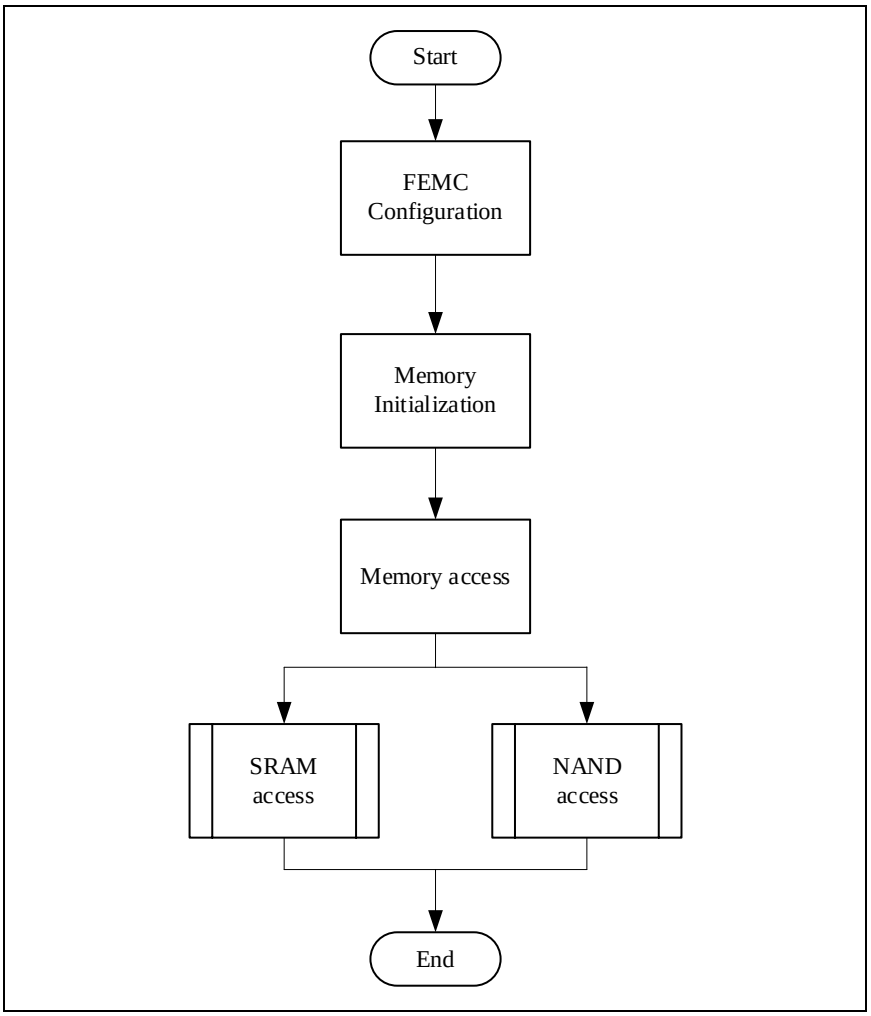
38.5.7 Programming Guide

This controller provides a large number of registers to allow user configure the FEMC, internal SMC core, external memory, timing operation mode of memory accesses. General programming flow of user setting for memory access operation is shown at Figure 38-35.

Figure 38-35 General programming flow



38.5.7.1 FEMC Configuration

User can change the following FEMC configuration:

- Address map of each external memory banks

  User can set the **ADDRMCH** and **ADDRMSK** bits of FEMC SRAM/NOR Set Address Register and FEMC NAND Set Address Register to re-define the actual address map range of each device.

  NOTE: It must be changed address map to sub-range of original system memory map for the bank only. If not, the access to external memory will not be decoded properly.

- Synchronization between AXI clock and memory clock

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This controller allows the memory clocks are synchronous or asynchronous with AXI clock. User can set the bit **SYNC** of FEMC SRAM/NOR Mode Register or FEMC NAND Mode Register to select it.

- SRAM interface mode (remap, multiplexed address/data)
- NAND interface mode (remap, booting function, chip select timing)

Since these settings take effective to the initial values and further operation of SMC core and therefore, operation of FEMC, it must be only changed during SMC core reset. Using the AXI reset signal to reset SMC core while FEMC wrapper reset pin is H to configure those registers. See the section of RCC for more detail on resets of FEMC.

38.5.7.2 Memory Initialization

Use the registers settings to initialize FEMC and memory device to make sure they are synchronized and compatible before accessing memory.

Figure 38-36 and Figure 38-37 show the sequence of events that a device driver must carry out to initialize the FEMC and a memory device to ensure the configuration of both is synchronized.

Typically, PSRAM devices can have the mode register programmed using the address bus only. NOR flash memory devices are examples of memory that require mode register accesses to be carried out using a sequence of accesses using the address and data buses. Check the data sheet for the specific memory device you are configuring to determine the configuration method.

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Figure 38-36 FEMC and memory initialization flow (1/2)

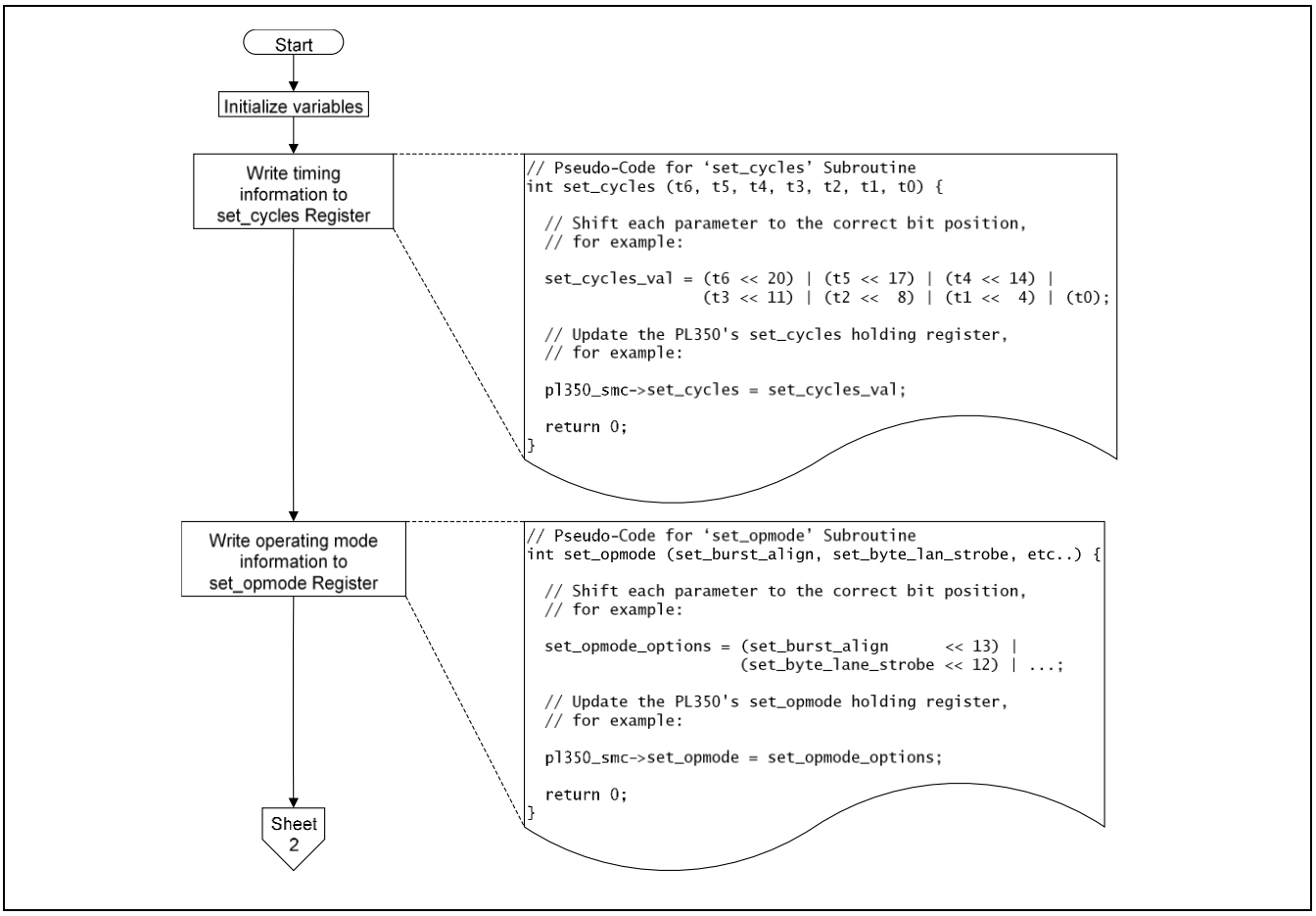

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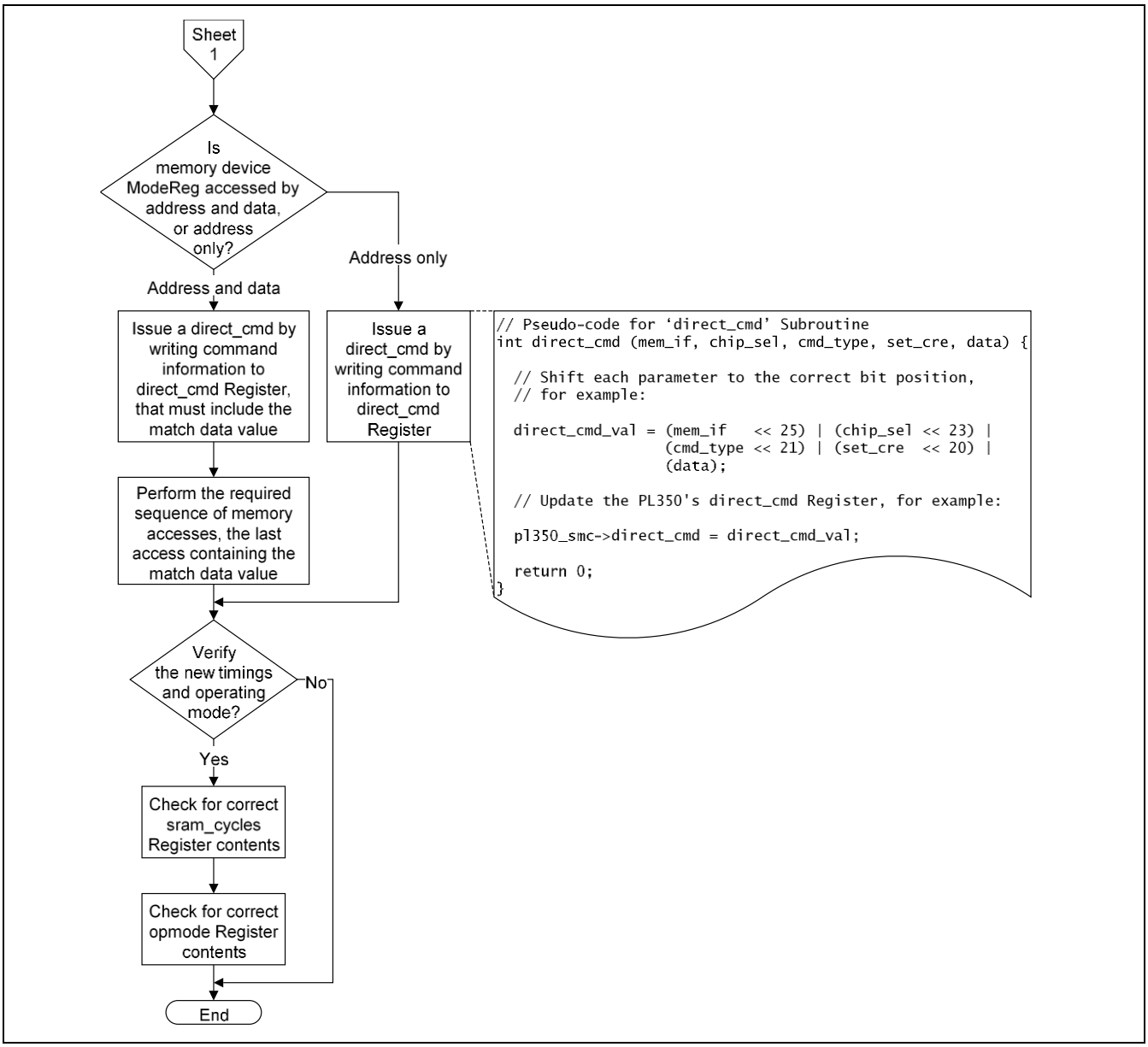
Figure 38-37 FEMC and memory initialization flow (2/2)



38.5.7.3 Memory Access

Use AXI transaction to access the memory. This IP converts the AXI transaction to corresponding memory access.

For SRAM access, there is no special limitation on AXI burst attributes as long as the memory initialization performed correctly. Note that although it is possible to issue the outstanding parallel AXI bursts, the converted memory accesses are issued in serial. See section 38.5.2 for more detail of SRAM interface accesses.

For NAND access, it requires some specific manipulation to format the transaction into the correct format for the FEMC to map the transaction correctly to the NAND device. See section 38.5.4 for more detail of NAND interface accesses.

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38.6 FEMC Register

FEMC Base Address: 0xA000 0000

38.6.1 FEMC Register Overview

38.6.2 FEFEMC Status Register（FEMC_STS）

Address Offset：0x000

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RECC INTF	Reserved	ECC INTF	Reserved	ECCINTE NF	Reserved	RINT1F	RINT0F	INT1F	INT0F	INT1 ENF	INT0 ENF	Reserved
			r		r		r		r	r	r	r	r	r	

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	RECCINTF	Raw status of the ECC interrupt signal.
11	Reserved	Reserved, the reset value must be maintained.
10	ECCINTF	Interrupt status for ECC:
9	Reserved	Reserved, the reset value must be maintained.
8	ECCINTENF	Interrupt enable status for ECC: 0 = Interrupt is disabled 1 = Interrupt is enabled.
7	Reserved	Reserved, the reset value must be maintained
6	RINT1F	Raw status of the INT1 interrupt signal.
5	RINT0F	Raw status of the INT0 (SRAM) interrupt signal.
4	INT1F	Status of the INT1 (SRAM)interrupt signal.

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Bit Field	Name	Description
3	INT0F	Status of the INT0 (SRAM) interrupt signal.
2	INT1ENF	Interrupt enable status for INT1(NAND): 0: Interrupt is disabled. 1: Interrupt is enabled.
1	INT0ENF	Interrupt enable status for INT0(SRAM): 0: Disabled INT0. 1: Enabled INT0.
0	Reserved	Reserved, the reset value must be maintained.

38.6.3 FEMC Status Register1（FEMC_STS1）

Address Offset：0x004

Reset Value：0x0000 162D

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														M0TYPE[1:0]	
														r	

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained
1:0	M0TYPE[1:0]	Returns the memory interface 0 type: 00 = reserved 01 = SRAM non-multiplexed 10 = reserved 11 = SRAM multiplexed.

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38.6.4 FEMC Configuration Register（FEMC_CFG）

Address Offset: 0x008

Default Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							ASYNC ADV	Reserved	ECCINT EN	Reserved				INT1EN	INT0EN
							w		w					w	w

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	ASYNCADV	0 = No effect. 1 = ASYNC Mode ADV signal same as Multiplexed Mode.
7	Reserved	Reserved, the reset value must be maintained.
6	ECCINTEN	0 = No effect. 1 = Enables the ECC interrupt.
5:2	Reserved	Reserved, the reset value must be maintained.
1	INT1EN	0 = No effect. 1 = Enables the INT1 (NAND) interrupt.
0	INT0EN	0 = No effect. 1 = Enables the INT0 (SRAM) interrupt.

38.6.5 FEMC Configuration Clear Register（FEMC_CCFG）

Address Offset: 0x00C

Default Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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rw	rw	rw													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							ASYNC ADVDIS	Reserved	ECCINT DIS	Reserved	INT1 CLR	INT0 CLR	Reserved	INT1DIS	INT0DIS
							w		w		w	w		w	w

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	ASYNCADVDIS	0 = No effect. 1 = ASYNC Mode no ADV signal.
7	Reserved	Reserved, the reset value must be maintained.
6	ECCINTDIS	0 = No effect. 1 = Disable the ECC interrupt.
5	Reserved	Reserved, the reset value must be maintained.
4	INT1CLR	0 = No effect. 1 = Clear INT1 flag.
3	INT0CLR	0 = No effect. 1 = Clear INT0 flag.
2	Reserved	Reserved, the reset value must be maintained.
1	INT1DIS	0 = No effect. 1 = Disable the INT1 (NAND) interrupt.
0	INT0DIS	0 = No effect. 1 = Disable the INT0 (SRAM) interrupt.

38.6.6 FEMC Control Register（FEMC_CTRL）

Address Offset: 0x010

Default Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						CHIPNUM[2:0]			CMDTYPE[1:0]		CREPOL	ADDR[19:16]			

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Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained
25:23	CHIPNUM[2:0]	Selects chip configuration register bank to update, and enables chip mode register access depending on cmd_type. The encoding is: 000~011: Chip selects 1-4 on memory interface 0 100~110: Chip selects 1-2 on memory interface 1.
22:21	CMDTYPE[1:0]	Selects the command type: 00: UpdateRegs and AXI 01: ModeReg 10: UpdateRegs(Set FEMC_OMCFG or FEMC_TCFG register to correspondence status register) 11: ModeReg and UpdateRegs.
20	CREPOL	Maps to the configuration register enable signal CRE, when a ModeReg command is issued. The encoding is: 0: CRE is LOW 1: CRE is HIGH when ModeReg write occurs.
19:0	ADDR[19:0]	When CMDTYPE[1:0] = 00, then: • bits [15:0] are used to match wdata[15:0] • bits [19:16] are reserved. Write as zero. When CMDTYPE[1:0] = 01 or 11, these bits map to the external memory address bits [19:0]. When CMDTYPE[1:0] = 10, these bits are reserved. Write as zero.

38.6.7 FEMC Timing Configuration Register（FEMC_TCFG）

Address Offset: 0x014

Default Value: 0x0000 0000

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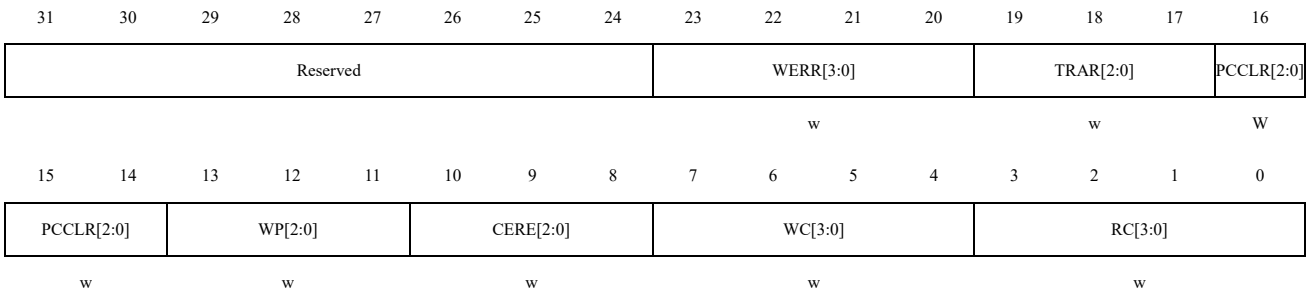

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	WERR[3:0]	Contains the value to be written to either the: • we_time bit of the SRAM Cycles Register • t_rr field of the NAND Cycles Register
19:17	TRAR[2:0]	Contains the value to be written to either the: • t_tr field of the SRAM Cycles Register • t_ar field of the NAND Cycles Register
16:14	PCCLR[2:0]	Contains the value to be written to either the: • t_pc field of the SRAM Cycles Register • t_clr field of the NAND Cycles Register
13:11	WP[2:0]	Contains the value to be written to the t_wp field in either the: • SRAM Cycles Register • NAND Cycles Register
10:8	CERE[2:0]	Contains the value to be written to either the: • t_ceoe field of the SRAM Cycles Register • t_rea field of the NAND Cycles Register
7:4	WC[3:0]	Contains the value to be written to the t_wc field in either the: • SRAM Cycles Register • NAND Cycles Register
3:0	RC[3:0]	Contains the value to be written to the t_rc field in either the: • SRAM Cycles Register • NAND Cycles Register

38.6.8 FEMC Operate Mode Configuration Register（FEMC_OMCFG）

Address Offset: 0x018

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Default Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSTAGN[2:0]			BLSS	ADV	BAA	WRBL[2:0]			WRSYN	RDBL[2:0]			RDSYN	MDBW[1:0]	
w			w	w	w	w			w	w			w	w	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:13	BSTAGN[2:0]	Burst align set in synchronous mode. When memory perform synchronous transfersa, these bits control if memory bursts are split on memory burst boundaries: 000 = bursts can cross any address boundary 001 = burst split on memory burst boundary, that is, 32 beats for continuous 010 = burst split on 64 beat boundary 011 = burst split on 128 beat boundary 100 = burst split on 256 beat boundary Other values: Reserved Only SRAM memory interface used.
12	BLSS	BLS signal synchronous set bit. 0: The status of BLS signal and CS signal changes synchronously 1: The status of BLS signal and WE signal changes synchronously. Only SRAM memory interface used.
11	ADV	The memory uses the address advance signal ADV set bit. 0: ADV signal is invalid. 1: ADV signal is valid. Only SRAM memory interface used.
10	BAA	BAA signal set bit. 0: BAA signal is invalid. 1: BAA signal is valid. Only SRAM memory interface used.
9:7	WRBL[2:0]	The memory write burst length: 000 = 1 beat 001 = 4 beats

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		010 = 8 beats 011 = 16 beats 100 = 32 beats 101 = continuous 110-b111 = reserved. Only SRAM memory interface used.
6	WRSYN	Write synchronous enable bit: 0: Disable synchronous write. 1: Enable synchronous write. Only SRAM memory interface used.
5:3	RDBL[2:0]	The memory read burst length: b000 = 1 beat b001 = 4 beats b010 = 8 beats b011 = 16 beats b100 = 32 beats b101 = continuous b110-b111 = reserved. Only SRAM memory interface used.
2	RDSYN	Read synchronous enable bit: 0: Disable synchronous read. 1: Enable synchronous read. Only SRAM memory interface used.
1:0	MDBW[1:0]	The memory data bus width: b00 = 8 bits b01 = 16 bits b10 = 32 bits b11 = reserved.

38.6.9 FEMC Refresh Period Register（FEMC_RPE）

Address Offset：0x020

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												REFPRD[3:0]			
												rw			

Bit Field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3:0	REFPRD[3:0]	Refresh period set. 0000 = disables the insertion of idle cycles between consecutive bursts 0001 = an idle cycle occurs after each burst 0010 = an idle cycle occurs after 2 consecutive bursts 0011 = an idle cycle occurs after 3 consecutive bursts 0100 = an idle cycle occurs after 4 consecutive bursts … 1111 = an idle cycle occurs after 15 consecutive bursts. *Note: In continuous mode the memory bursts are limited to 32 beats.* Only SRAM memory interface used.

38.6.10 SRAM/NOR Flash Timing Status Register（FEMC_SNTSTS1/2/3/4）

Address Offset: 0x100 + 0x20 * (x-1), (x=1,2,3,4)

Reset Value: 0x0002 B3CC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											WECS	TR[2:0]			PC[2]
											r	r			r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC[1:0]		WP[2:0]			CERE[2:0]			WC[3:0]				RC[3:0]			
r		r			r			r				r			

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained

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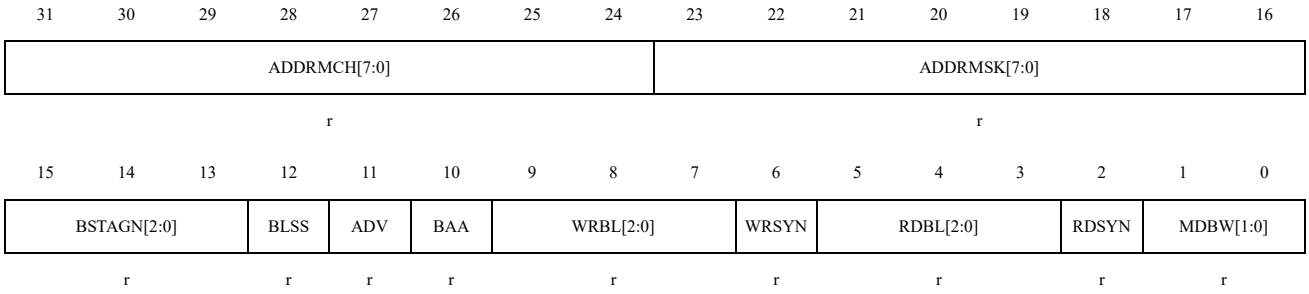
Bit Field	Name	Description
20	WECS	For asynchronous multiplexed transfers this bit returns when asserts we_n: 0: asserts we_n two mclk cycles after asserting cs_n. 1: asserts we_n and cs_n together.
19:17	TR[2:0]	Returns the t_tr turnaround time.
16:14	PC[2:0]	Returns the t_pc page cycle time.
13:11	WP[2:0]	Returns the t_wp assertion delay.
10:8	CEOE[2:0]	Returns the t_ceoe assertion delay..
7:4	WC[3:0]	Returns the t_wc write cycle time.
3:0	RC[3:0]	Returns the t_rc read cycle time.

38.6.11 SRAM/NOR Flash Operate Mode Status Register （FEMC_SNOMSTS1/2/3/4）

Address Offset: 0x104+ 0x20 * (x-1), (x=1,2,3,4)

Reset Value: 0x60FC 0802



Bit Field	Name	Description
31:24	ADDRMCH[7:0]	Returns the value of the address match which is the comparison value for address bits [31:24] to determine the chip 0 that is selected. *Note: Chip 0 is selected when araddr/awaddr[31:24] & addr_mask0 = addr_match0
23:16	ADDRMSK[7:0]	Returns the value of the address mask whic is the mask for address bits

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Bit Field	Name	Description
		[31:24]. A logic 1 indicates the bit is used for comparison. *Note: Chip 0 is selected when araddr/awaddr[31:24] & addr_mask0 = addr_match0
15:13	BSTAGN[2:0]	Return the memory burst operating mode in synchronous transfer: 000: Bursts can cross any address boundary. This is the default setting. 001: Burst split on memory burst boundary, that is, 32 beats for continuous. 010: Burst split on 64 beat boundary. 011: Burst split on 128 beat boundary. 100: Burst split on 256 beat boundary. Other values: Reserved.
12	BLSS	Returns the byte lane strobe operating mode for an SRAM memory interface: 0: BLS signal and CS signal changes synchronously 0: BLS signal and WE signal changes synchronously
11	ADV	Returns the address advance signal operating mode for an SRAM memory interface: 0: ADV signal is HIGH. 1: ADV signal is LOW.
10	BAA	Returns the burst address advance signal operating mode for an SRAM memory interface: 0: BAA signal is HIGH. 1: BAA signal is LOW.
9:7	WRBL[2:0]	Returns the memory burst length for writes on an SRAM memory interface: 000 = 1 beat. This is the default setting. 001 = 4 beats 010 = 8 beats 011 = 16 beats 100 = 32 beats 101 = Continuous Other values: Reserved.
6	WRSYN	Returns the write operating mode for an SRAM memory interface: 0 = FEMC performs asynchronous writes. 1 = FEMC performs synchronous writes.
5:3	RDBL[2:0]	Returns the memory burst length for reads on an SRAM memory interface: 000: 1 beat. This is the default setting.

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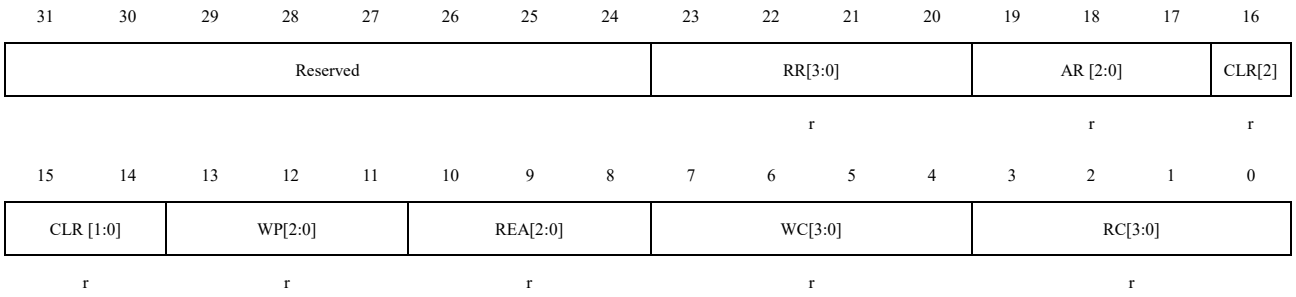
Bit Field	Name	Description
		001: 4 beats 010: 8 beats 011: 16 beats 100: 32 beats 101: Continuous Other values: Reserved.
2	RDSYN	Returns the read operating mode for an SRAM memory interface: 0: FEMC performs asynchronous reads. 1: FEMC performs synchronous reads.
1:0	MDBW[1:0]	Returns the memory data bus width: 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved.

38.6.12 NAND Flash Timing Status Register（FEMC_NTSTS1/2）

Address Offset: 0x180 + 0x20 * (x-1), (x=1,2)

Reset Value: 0x0024 ABCC



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	RR[3:0]	Returns the busy to re_n time.
19:17	AR[2:0]	Returns the ID read time.
16:14	CLR[2:0]	Returns the status read time.

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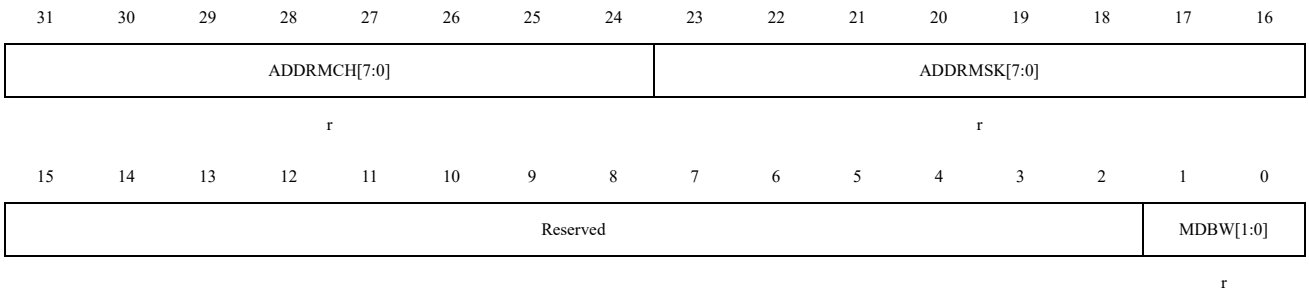
Bit Field	Name	Description
13:11	WP[2:0]	Returns the we_n assertion delay.
10:8	REA[2:0]	Returns the re_n assertion delay.
7:4	WC[3:0]	Returns the t_wc write cycle time.
3:0	RC[3:0]	Returns the t_rc read cycle time.

38.6.13 NAND Flash Operating Mode Status Register（FEMC_NOMSTS1/2）

Address Offset: 0x184 + 0x20 * (x-1), (x=1,2)

Reset Value: 0xA0F0 0001 (x=1)

Reset Value: 0xB0F0 0001 (x=2)



Bit Field	Name	Description
31:24	ADDRMCH[7:0]	Returns the value of the address match which is the comparison value for address bits [31:24] to determine the chip 1 that is selected. *Note: Chip 1 is selected when araddr/awaddr[31:24] & addr_mask0 = addr_match0
23:16	ADDRMSK[7:0]	Returns the value of the address mask whic is the mask for address bits[31:24]. A logic 1 indicates the bit is used for comparison. *Note: Chip 1 is selected when araddr/awaddr[31:24] & addr_mask0 = addr_match0
15:2	Reserved	Reserved, the reset value must be maintained
1:0	MDBW[1:0]	Returns the memory data bus width: b00 = 8 bits b01 = 16 bits b10 = 32 bits

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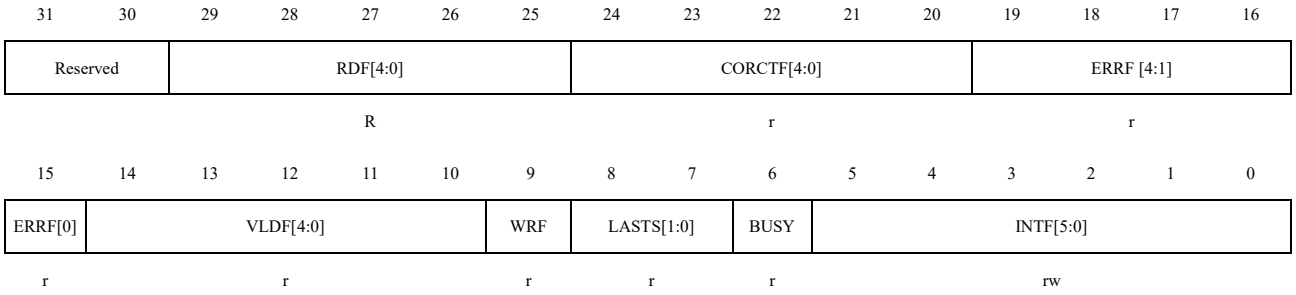
Bit Field	Name	Description
		b11 = reserved.

38.6.14 NAND ECC Status Register（FEMC_ECCSTS）

Address Offset: 0x400

Reset Value: 0x0000 0000



Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	RDF[4:0]	Read flags for ECC blocks. Indicates whether the stored ECC value for each block has been read from memory: 0 = not read 1 = read. [29]: ECC Block Extra. [28]: ECC Block 3. [27]: ECC Block 2. [26]: ECC Block 1. [25]: ECC Block 0.
24:20	CORCTF[4:0]	Correctable flag for each ECC block. Indicates if the detected error is correctable: 0 = not correctable 1 = correctable. [24]: ECC Block Extra. [23]: ECC Block 3.

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Bit Field	Name	Description
		[22]: ECC Block 2. [21]: ECC Block 1. [20]: ECC Block 0.
19:15	FAILF[4:0]	Pass, fail flag for each ECC block: 0 = pass 1 = fail. [19]: ECC Block Extra. [18]: ECC Block 3. [17]: ECC Block 2. [16]: ECC Block 1. [15]: ECC Block 0.
14:10	VLDF[4:0]	Valid flag for each ECC block. [14]: ECC Block Extra. [13]: ECC Block 3. [12]: ECC Block 2. [11]: ECC Block 1. [10]: ECC Block 0.
9	WRF	ECC write read flag: 0: write 1: read.
8:7	LASTS[1:0]	ECC last status 00: Completed successfully 01: Unaligned address, or out-of-range 10: Data stop after incomplete block 11: Data stopped but values not read/written because of ecc_jump value. *Note: The LASTS[1:0] bits are only updated at the completion of an ECC calculation.*
6	BUSY	ECC block status: 0: idle 1: busy.
5:0	INTF[5:0]	ECC block interrupts flag:

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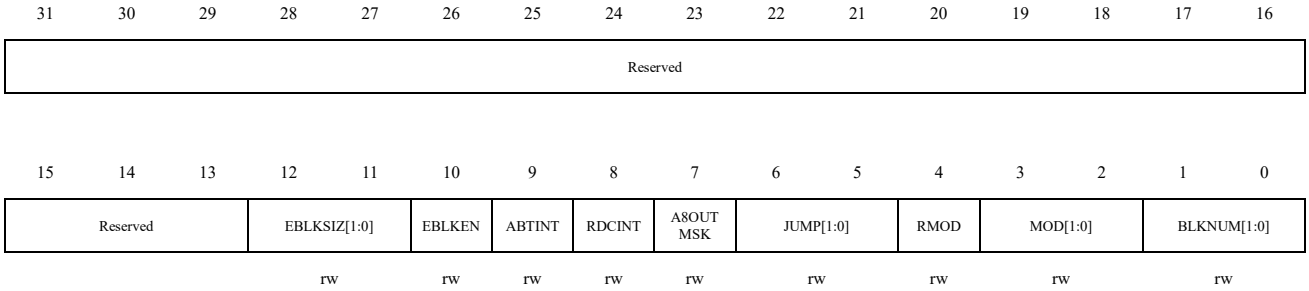
Bit Field	Name	Description
		[5]: Abort. [4]: Extra block (if used). [3]: Block 3. [2]: Block 2. [1]: Block 1. [0]: Block 0. To clear an interrupt, write 1 to the appropriate bit.

38.6.15 NAND ECC Configuration Register（FEMC_ECCCFG）

Address Offset: 0x404

Reset Value: 0x0000 0043



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained
12:11	EBLKSIZ[1:0]	The size of the extra block in memory after the last 512-byte block: b00 = 4 bytes b01 = 8 bytes b10 = 16 bytes b11 = 32 bytes.
10	EBLKEN	Enables a small block for extra information after the last 512 bytes block in the page. 0: Disable. 1: Enable.
9	ABTINT	Interrupt flag on ECC abort.
8	RDCINT	Interrupt flag when a correct ECC value is read from memory.

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Bit Field	Name	Description
7	A8OUTMSK	This bit is used to indicate if A8 is output with the address, required to find the aligned start of blocks: 0: A8 is output 1: A8 is not output.
6:5	JUMP[1:0]	Indicates that the memory supports column change address commands: 00: no jumping, reads and writes only occur at end of page 01: jump using column change commands 10: jump using full command 11: Reserved.
4	RMOD	Indicates when ECC values are read from memory: 0: the ECC value for a block must be read immediately after the block. Data access must stop on a 512 byte boundary. 1: ECC values for all blocks are read at the end of the page.
3:2	MOD[1:0]	This specifies the mode of the ECC block: 00: bypassed. 01: ECC values are calculated and made available on the APB interface, but they are not read from or written to memory. 10: ECC values and calculated and read/written to memory. For a read, the ECC value is checked and the result of the check is made available on the APB interface. 11: Reserved.
1:0	BLKNUM[1:0]	The number of 512 byte blocks in a page: 00： No 512 byte blocks. Reserved if an ecc_extra_block is not configured, or if an ecc_extra_block is configured but is not enabled. 01: One 512 byte block. 10: Two 512 byte blocks. 11: Four 512 byte blocks.

38.6.16 AND ECC Command0 Register（FEMC_ECCMD0）

Address Offset: 0x408

Reset Value: 0x0130 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	UEND	RDEND[7:0]
	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD [7:0]								WR[7:0]							
rw								rw							

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	UEND	Use end command
23:16	RDEND[7:0]	The NAND command to indicate the end of a read (0x30)
15:8	RD[7:0]	The NAND command to initiate a read (0x00)
7:0	WR[7:0]	The NAND command to initiate a write (0x80)

38.6.17 NAND ECC Command1 Register（FEMC_ECCMD1）

Address Offset: 0x40C

Reset Value: 0x01E00585

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							UEND	RDCOLEND[7:0]							
							rw	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDCOL [7:0]								WRCOL[7:0]							
rw								rw							

Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	UEND	Use end command
23:16	RDCOLEND[7:0]	The NAND command to indicate the end of a column change read (0xE0)

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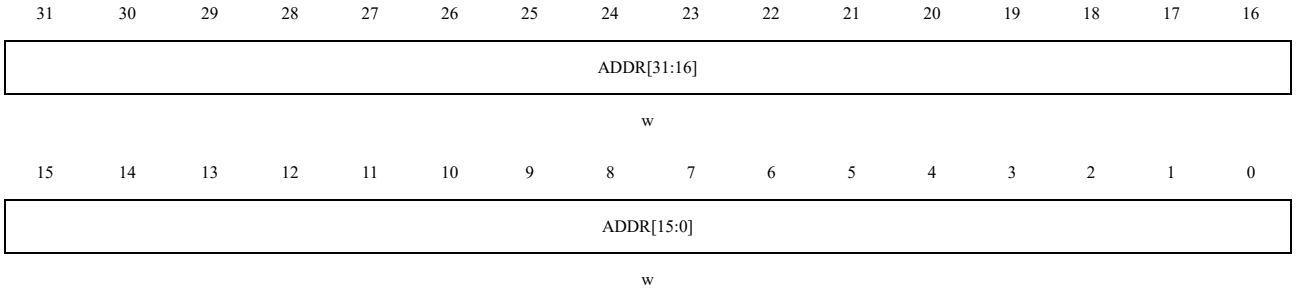
Bit Field	Name	Description
15:8	RDCOL[7:0]	The NAND command (0x05) that is either: • a command to initiate a column change read • a spare bits pointer command.
7:0	WRCOL[7:0]	The NAND command to initiate a column change write (0x85)

38.6.18 NAND ECC Address0 Register（FEMC_ECCADDR0）

Address Offset: 0x410

Reset Value: 0x0000 0000

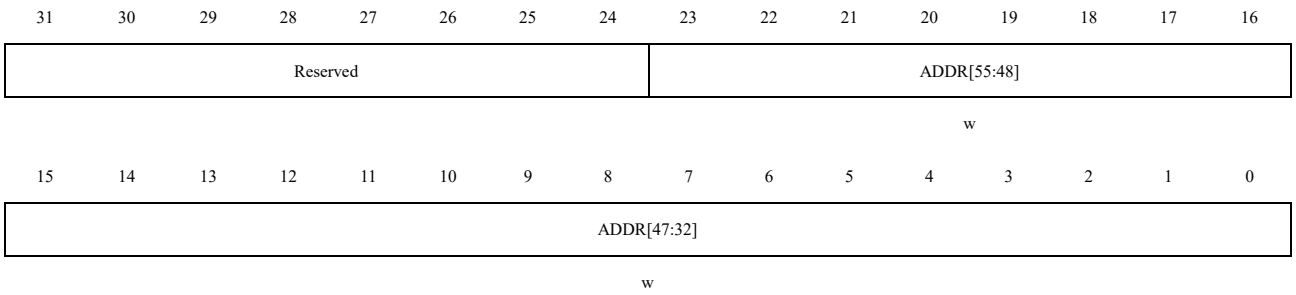


Bit Field	Name	Description
31:0	ADDR[31:0]	Address bits 31 to 0 for NAND

38.6.19 NAND ECC Address1 Register（FEMC_ECCADDR1）

Address Offset: 0x414

Reset Value: 0x0000 0000



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Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:0	ADDR[55:32]	Address bits [55:32] for NAND

38.6.20 NAND ECC Block Register（FEMC_ECCBLK0/1/2/3）

Address Offset: 0x418+ 4* x, (x=0,1,2,3)

Reset Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTF	VALDF	RDF	ERRF	CRTF	Reserved			VAL[23:16]							
rw	rw	rw	rw	rw				rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL[15:0]															
rw															

Bit Field	Name	Description
31	INTF	Interrupt flag for this block. To clear this bit, write any value to the register.
30	VALDF	Indicates if the ECC value for this block is valid.
29	RDF	Indicates if the ECC value for this block has been read from memory.
28	ERRF	Indicates if the ECC value for this block has failed.
27	CRTF	Indicates if this block is correctable.
26:24	Reserved	Reserved, the reset value must be maintained
23:0	VAL[23:0]	ECC value of check result for this block.

38.6.21 NAND ECC Extra Block Register（FEMC_ECCEBLK）

Address Offset: 0x428

Reset Value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTF	VALDF	RDF	ERRF	CRTF	Reserved			VAL[23:16]							

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rw	rw	rw	rw	rw											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL[15:0]															
rw															

Bit Field	Name	Description
31	INTF	Interrupt flag for this block. To clear this bit, write any value to the register.
30	VALDF	Indicates if the ECC value for this block is valid.
29	RDF	Indicates if the ECC value for this block has been read from memory.
28	ERRF	Indicates if the ECC value for this block has failed.
27	CRTF	Indicates if this block is correctable.
26:24	Reserved	Reserved, the reset value must be maintained
23:0	VAL[23:0]	ECC value of check result for this block.

38.6.22 FEMC SRAM/NOR Set Address Register（FEMC_SNADDR1/2/3/4）

Address Offset: 0x500 + 4 * (x-1), (x=1,2,3,4)

Reset Value: 0x60FC 0000(x=1)

Reset Value: 0x64FC 0000(x=2)

Reset Value: 0x68FC 0000(x=3)

Reset Value: 0x6CFC 0000(x=4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDRMCH[7:0]								ADDRMSK[7:0]							
rw								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

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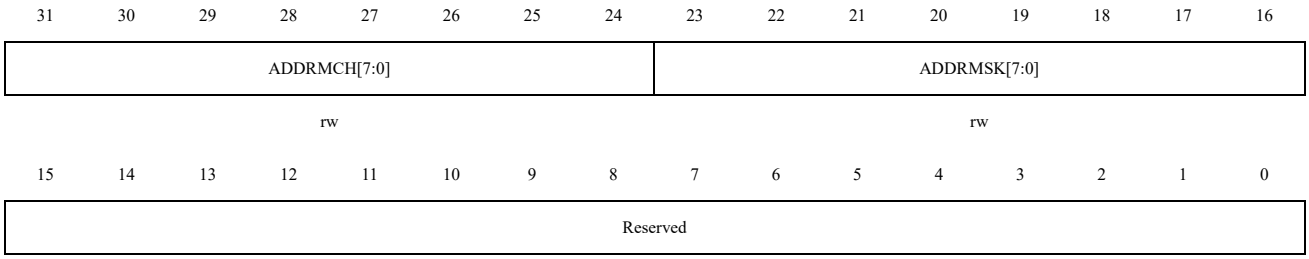
Bit Field	Name	Description
31:24	ADDRMCH[7:0]	Set address match for chip select of memory interface 0 (SRAM). The comparison value that determines the chip select base address.
23:16	ADDRMSK[7:0]	Set address mask for chip select of memory interface 0 (SRAM). A mask applied to the AXI address bits [31:24] before the comparison with the corresponding address match value.
15:0	Reserved	Reserved, the reset value must be maintained

38.6.23 FEMC NAND Set Address Register（FEMC_NADDR1/2）

Address Offset: 0x510 + 4 * (x-1), (x=1,2)

Reset Value: 0xA0F00000 (x=1)

Reset Value: 0xB0F00000 (x=2)



Bit Field	Name	Description
31:24	ADDRMCH[7:0]	Set address match for chip select 0 of memory interface 1 (NAND). The comparison value that determines the chip select base address.
23:16	ADDRMSK[7:0]	Set address mask for chip select 0 of memory interface 1 (NAND). A mask applied to the AXI address bits [31:24] before the comparison with the corresponding address match value.
15:0	Reserved	Reserved, the reset value must be maintained

38.6.24 FEMC SRAM/NOR Mode Register（FEMC_SNMOD）

Address Offset: 0x520

Reset Value: 0x0000 0019

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										MUXEN	AGTM	SYNC	Reserved		
										rw	rw	rw			

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5	MUXEN	Address/Data multiplexing enable, when this bit is set, the low 16 bits of the address and data will share the data bus. This bit is only valid for NOR and PSRM memory. 0: Address/data not multiplexed. 1: Address/data multiplexed on the data bus.
4	AGTM	When HIGH, it indicates that aclk is faster than, and synchronous to, mclk0. When LOW, it indicates that aclk is slower than or same, and synchronous to mclk0. It is valid only when SYNC = 1.
3	SYNC	When HIGH, indicates mclk0 is synchronous to aclk. Otherwise, they are asynchronous. 0: Asynchronous mode. 1: Synchronous mode.
2:0	Reserved	Reserved, the reset value must be maintained

38.6.25 FEMC NAND Mode Register（FEMC_NMOD）

Address Offset: 0x524

Reset Value: 0x0000 0018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	CSL	Reserved	AGTM	SYNC	Reserved
	rw		rw	rw	

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	CSL	When HIGH, the chip select remains asserted between the address phase and data phase of a transfer on the NAND interface.
5	Reserved	Reserved, the reset value must be maintained
4	AGTM	When HIGH, it indicates that aclk is faster than, and synchronous to mclk1. When LOW, it indicates that aclk is slower than or same, and synchronous to mclk1. It is valid only when SYNC=H.
3	SYNC	When HIGH, it indicates that mclk0 is synchronous to aclk, otherwise, they are asynchronous. 0: Asynchronous mode. 1: Synchronous mode.
2:0	Reserved	Reserved, the reset value must be maintained

38.6.26 FEMC Remap Register（FEMC_REMAP）

Address Offset: 0x528

Reset Value: 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															REMAP
															rw

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Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	REMAP	When HIGH, it indicates FEMC memory map is remapped. Note: only SRAM memory area can be remapped to SDRAM1 area. NAND memory area is not remapped.

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39 Secure Digital MultiMedia Card (SDMMC)

39.1 Introduction

SDMMC provides a host interface for SD memory cards, SDIO cards, and MMC devices.Only SD/SDIO/MMC cards with one protocol stack version are supported at a time.

The basic transaction of bus communication is command/response, and these types of bus transactions transfer their information directly in the command or response structure.Data transmission includes block mode, SDIO multi-byte mode and MMC continuous data flow mode.

HC: Host controller, i.e. SDMMC

HD: Host Driver, i.e., User Configuration

39.2 Main Features

- Compatible with SD master controller standard specification V3.00
- Compatible with SD physical layer interface specification V3.00
- Compatible with SDIO standard specification V3.00
- Compatible with eMMC standard specification V4.51
- Support 1 bit /4 bit SD card and SDIO mode
- Support UHS-I interface, need a level shift when the external device is powered by 1.8V
- Supports DS, HS, SDR12, SDR25, SDR50, DDR50, and SDR104 transmission modes
- Supports the 1-bit, 4-bit, and 8-bit MMC mode and BOOT mode
- Supports single block/multi-block read and write
- SD & SDIO modes support a maximum block size of 512 bytes, eMMC mode supports a maximum block size of 2048 bytes
- EMMC maximum clock frequency 200MHz (limited to maximum I/O frequency), maximum transmission rate up to 1.6Gbps (HS200 mode, 8-bit)
- Fully configurable 2048 * 2 bytes read-write FIFO
- Support internal dedicated DMA functionality

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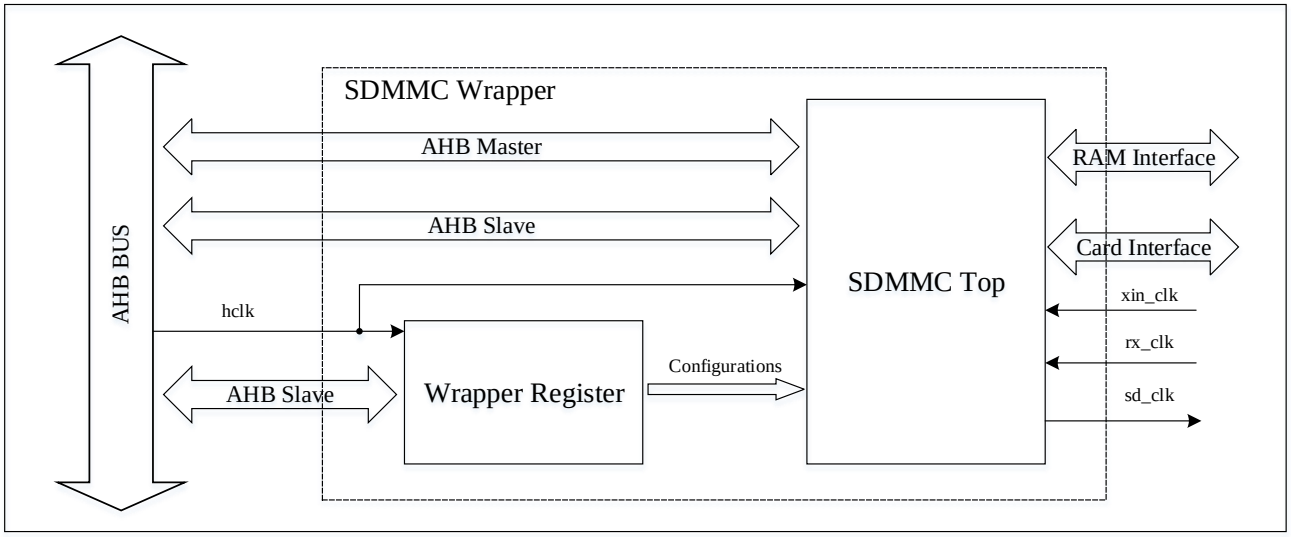
39.3 Block Diagram

Figure 39-1 SDMMC Top Level Diagram



Wrapper Register

Contains the configuration for the SDMMC with a separate AHB Slave interface.

SDMMC Top

The Host Controller Top. Block diagram of SDMMC Top is described as below

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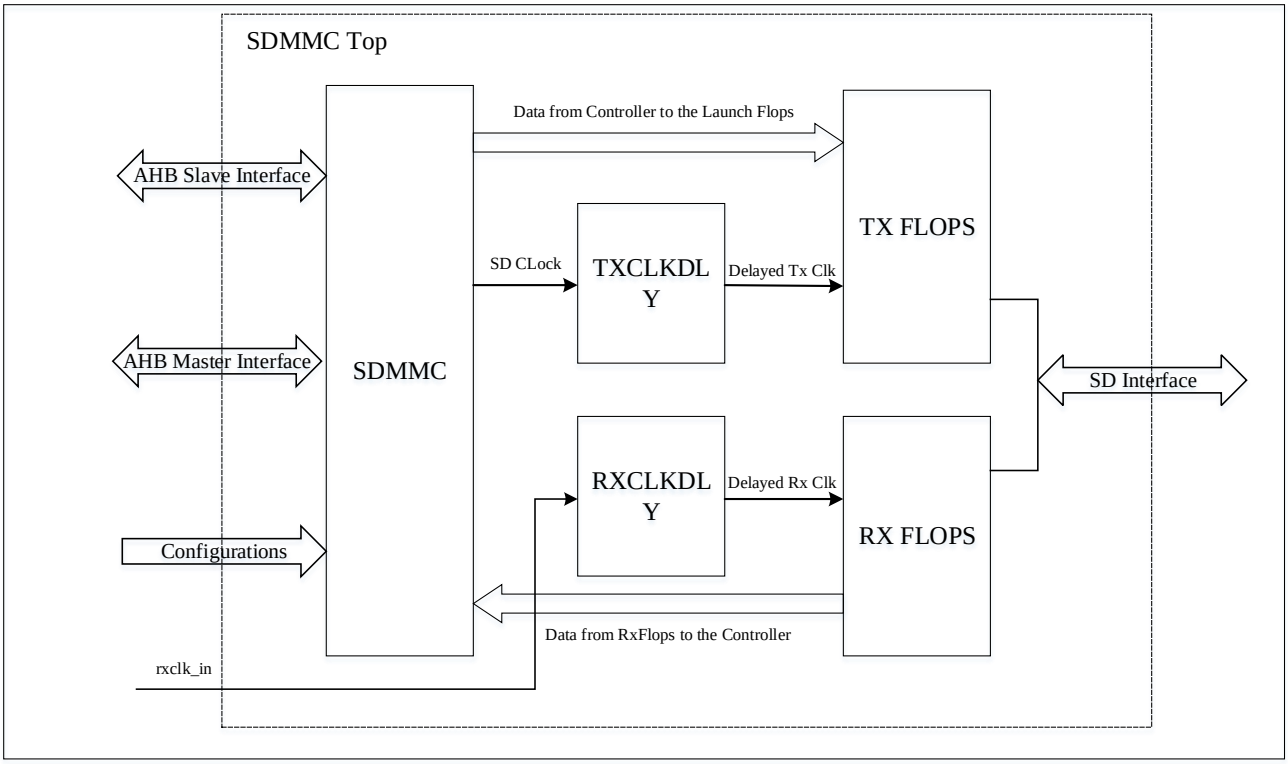
Figure 39-2 SDMMC Top Block Diagram



RxClk Delay Module

The RxClk Delay Module is used to support Receive Clock tuning to center align the receive data to the receive clock. There are two modes of Delaying the Receive Clock. First one is the Automatic Tuning of the Receive Clock when operating in SDR104 modes or optionally in SDR50 modes when the Tuning is implemented. The second one is under manual controls to offset for hardware delays etc. The manual control is implemented for HS mode and SDR25/SDR50/DDR50 modes using the SDMMC_DLYCTRL.ITDS[4:0] (input tap delay select) and SDMMC_DLYCTRL.ITDE (input tap delay enable) signals. This module is implemented with Tap Delay Lines for generating various phases of clock and selecting one of the phases of the clock. The Maximum number of Tap Delay (phases of the clock) is 32. A typical implementation will use either 4 or 8 Tap Delay lines (phases of clock).

Rx Flops Module

The RX Flops Module is a where the CMD/DAT lines from the SD Interface are flopped on the output of the RxClk Delay Module. To Support both DDR Mode of operation, the signals are latched on both positive edge of the Receive clock and the negative edge of the receive clock. The outputs from these flops are passed onto to SDMMC core for further processing.

TxClk Delay Module

The CMD and DAT outputs need to delayed with respect to the to the output SD_CLK signal to meet the hold time requirements in various modes of operation. The out going SD Clock is delayed and the delayed clock is used to flop the CMD/DAT lines and use this output to drive the SD Interface. The SD_CLK output itself is not delayed.

Tx Flops Module

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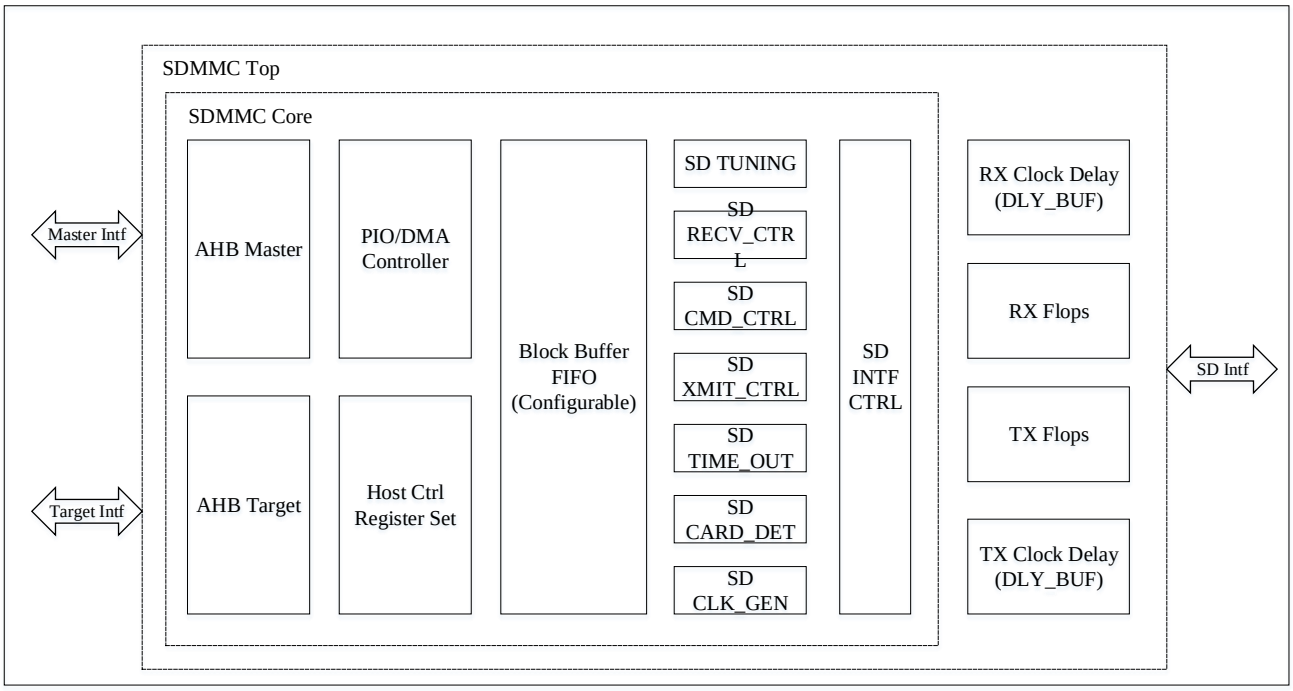
Email: sales@nsing.com.sg

The SD Outputs from the SDMMC Core are flopped on the Delayed Tx Clock. Also to support the DDR Mode of operation, the separate set of outputs are received from the Core to be driven on positive and negative edge of the Delayed Clock.

SDMMC (Host Controller) diagram is shown as below

Figure 39-3 SDMMC Block Diagram



AHB Master Interface

The Master Bus is used by the DMA Controller (when using DMA or ADMA2 Modes). The DMA Controller uses the Master DMA Interfaces to transfer data between the internal Block Buffer and the System Memory and vice-versa. The DMA Controller also uses the Master Interface to fetch the Descriptors while operating in ADMA2 mode.

AHB Target Interface

The Target Bus is used to access the Registers inside the Host controller. Also when operating in PIO mode, the Driver can access the SDHOST buffer Data Port Register (SDHOST_BUFDAT) through this Interface. This is the PIO method in which the Host Driver transfers data using the Buffer Data Port Register. The Target Bus supports only single Transfer access (no Burst Support).

Host Controller Register Set

The Host Controller Register set inside SDMMC core implements the Registers defined by the SD Host Controller Specification (Version 3.00). The Registers are accessible from the Target Interface. The Host Controller Register Set also implements the Data Port Registers for the PIO Mode transfers. The Register Set provides the Control Signals to rest of the Blocks in design and monitors the status signals from the blocks to set Interrupt Status Bits and eventually generate Interrupt signal to the System. The Host Controller Register Set acts as the bridge between CPU

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

and SDMMC. The SD/SDIO controller registers are programmed by the CPU through AHB Target interface. Interrupts are generated to the CPU based on the values set in the Interrupt status register and Interrupt enable registers.

PIO/DMA Controller

The PIO/DMA Controller Module implements the SDMA and ADMA2 Engines as defined in the SD Host Controller Specification and maintains the block transfer counts for PIO operation. It interacts with the Registers Set and starts the DMA Engine when a Command with Data Transfer is involved. The DMA Controller interfaces to the AHB Master Module to generate transfers and on the other side it interfaces with the Block Buffer to store/fetch block data. The DMA Controller implements a separate DMA for SDMA Operation and Separate DMA for the ADMA2 Operation. In addition it implements Host Transaction Generator that generates controls for the AHB Master Interface Module.

Block Buffer

SDMMC uses a Dual Port Block Buffer (read/write on both ports) that is used to store the Block Data during SD Transfers. The size of the Block Buffer is Configurable and has to be a minimum of 1 Block. The Block buffer size is 4KB, which is twice compares to the maximum Block Size supported by SDMMC (2KB). The Block Buffer uses Circular Buffer Architecture. One side of the Block Buffer is interfaced with the DMA Controller and operates on the system clock. The other side of the Block Buffer interfaces with SD Control Logic and operates on SD Clock. During a write transaction (data transferred from CPU to SD3.0 / SDIO3.0 / eMMC4.51 card), the data is fetched from the System Memory and is stored in the Block Buffer. When a Block of data is available, the SD Control logic will transfer it onto the SD Interface. The DMA Controller continues to fetch additional block of data when the Block Buffer has space. During a read transaction (data transferred from card to CPU), the data from card will be written in to block buffer and at the end when the CRC of the Block is valid, the data is committed. When a block of data is available, then the DMA Controller transfers this data to the System Memory. The SD Control logic meanwhile receives the next block of data provided there is space in the Block Buffer. If the SDMMC cannot accept any data from the card, then it will issue read wait (if card supports read wait mechanism) to stop the data transfer from card or by stopping the clock.

SD Clock Generator

The SD Clock Generator module generates the SD Clock from the Reference Clock (xin_clk), based on the controls programmed in the SDHOST_CTRL2 register. These include the Clock Divide Value, SD Clock Enable etc. The outputs from this module are the SD_CLK and the SD_CARD Clock. The SD_CLK is used by the SD Control Logic and connected to the “CLK” Pin on the SD Interface. This module also generates system resets to various clock domains.

SD Card Detect

The SD Card detect logic monitors the SD_CD# pin for card insertion/removal events. It implements the debouncing logic to filter the false transitions on the SD_CD# Pin. The card insertion & removal Events are reported to the SD Host Register set from which the Interrupt is eventually generated.

SD Timeout Control

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The SD Timeout Control logic implements the timeout check between block transfers. It uses the contents of the Data Timeout Counter Value in the SDHOST Control 2 Register (SDHOST_CTRL2) to implement timeout between Blocks.
This module operates under the control of the Transmit Control and Receive Control Modules (based on direction). When the timeout is detected, the event is reported to Transmit Control or Receive Control module.

SD Command Control

The SD Command control module generates the command sequence on the CMD line of the SD Interface for every new command programmed by the Software. The Command Control module also implements the response reception and checking the validity of the response. It uses the response type field to determine the length of the response and the presence of CRC7 field. The response is received on the receive clock (which is either the looped back clock or the tuned clock). Once the response is received the contents of the response (Start Bit, Command Index, CRC7, End Bit) are verified and response status is forwarded to the Register set module for setting various status bits. It also implements the timeout check on the response reception to make sure that the response is received with in the defined time (5 or 64 Clocks based on command type). The received response is then stored into appropriate bit position in the Response Register. The SD Command Control module generates controls to the SD Transmit Control and SD Receive Control based on the Transfer Direction The SD Command Control module also generates Auto Command (AutoCMD12 or AutoCMD23) when enabled.

SD Transmit Control

The SD Transmit control Module is used for write transfers for transferring data to the Card. Once the Command is issued, this module waits for the Block of data to be available in the Block Buffer and transfers this onto the SD DAT lines. Based on the configuration of data lines, the (1-bit, 4-bit or 8-bits or SPI), the data from Block Buffer is appropriately routed. The CRC16 is individually calculated on per lane basis and is attached at the end of block transfer before the END Bit. In case of DDR operation, it implements separate CRC16 for each edge of the clock.
At the end of Block transfer, it waits for the CRC Response on DAT0 line and reports the result of the CRC check to the Register Set.
Also this module checks for the Write Busy indication (DAT0 Line) before transferring next block of data. The Timeout Check is implemented to make sure that the Write Busy is asserted no more than the required limit.

SD Receive Control

The SD Receive control Module is used for read transfers for receiving data from the Card. Once the Command is issued, this module waits for the Block of data to be received from the Card. Based on the configuration of data lines, the (1-bit, 4-bit or 8-bits or SPI), the data from SD interface is assembled into byte and eventually into 32-bit word before it is being written into Block Buffer. The CRC16 is individually calculated on per lane basis and is checked against the received CRC16 at the end of block transfer before the END Bit. In case of DDR operation, it implements separate CRC16 checker for each edge of the clock. The data is received on the receive clock. This receive clock is either the Looped back Clock (SDCARD_CLK from IO) or the Tuned Clock using delay elements. The Timeout Check is implemented to make sure that the gap between the block no more than the required limit.

SD Tuning Block

The SD Tuning Block is used for SDR104 or SDR50 (optionally when enabled) and eMMC Hs200 modes to tune the receive clock. The Tuning block generates the Delay Controls to the external Delay Controller module. The

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Tuning modules receives the 64-byte Tuning Block (SD Mode) or 128-byte Tuning Block (eMMC Mode) and maintains a Tuning vector to determine the optimal Delay. The Tuning Block can be configured with number of Delay Taps (maximum 32) that are supported. Using this the Tuning Block performs Tuning and selects the optimal Tap Point for the Receive Clock.

SD Interface Control

The SD Interface Control block maps the internal signals to the External SD Interface and vice versa. Based on the Bus Width (1/4/8) the internal signals are driven out appropriately. In case of DS, the outputs are driven on the negative edge of the sd_clk.

The inputs from Rx Flops module are latched on the rx_clk (looped back or tuned clock) and is output to the Receive Control Module for further processing.

39.4 Pin Definition

Table 39-1 shows the pins used by SDMMC1 and their corresponding functions.

Table 39-1 SDMMC1 Pin Definitions

Pin Name	Function Name	Description
PB13_AF2 PC8_AF0	Bidirectional Data 0 Pin	Data 0 Input/Output. Used in SD/SDIO/MMC mode.
PC9_AF1	Bidirectional Data 1 Pin	Data 1 Input/Output. Used in SD/SDIO/MMC mode.
PC10_AF1	Bidirectional Data 2 Pin	Data 2 Input/Output. Used in SD/SDIO/MMC mode.
PC11_AF1	Bidirectional Data 3 Pin	Data 3 Input/Output. Used in SD/SDIO/MMC mode.
PB8_AF2 PD14_AF3	Bidirectional Data 4 Pin	Data 4 Input/Output. Used in MMC 8 bit mode.
PB9_AF1 PD15_AF3	Bidirectional Data 5 Pin	Data 5 Input/Output. Used in MMC 8 bit mode.
PB6_AF2 PC6_AF1	Bidirectional Data 6 Pin	Data 6 Input/Output. Used in MMC 8 bit mode.
PB7_AF1 PC7_AF1	Bidirectional Data 7 Pin	Data 7 Input/Output. Used in MMC 8 bit mode.
PD2_AF2	Bidirectional Command Pin	Command Input/Output to send command or receive response from card.
PD0_AF2	Write Protection Input Pin	Active High. SD Card write protect. 0: Card is not write protected 1: Card is write protected.
PD1_AF2	Card Detection Input Pin	Active Low. This pin is for the card insert detection. 0: Card is inserted 1: Card is not inserted
PB8_AF1	Looped-Back Clock Input Pin	Clock looped back from PAD
PC12_AF1	SD Clock Output Pin	SD/SDIO/MMC clock to card
PB9_AF0	Command Direction Output Pin	0: Command pin is input 1: Command pin is output

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Pin Name	Function Name	Description
PC6_AF0	Data 0 Direction Output Pin	0: Data 0 is input 1: data 0 in output
PC7_AF0	Data 1/2/3 Direction Output Pin	0: Data 1/2/3 is input 1: Data 1/2/3 is output
PE8_AF4 PF9_AF3 PI1_AF1	LED CTRL Output Pin	LED output indication 0 (LED OFF): no function 1 (LED ON): To Caution the user not to remove the card while the SD card is being accessed.
PA11_AF0 PI8_AF1 PJ12_AF0	1.8V Switching Enable Output Pin	1.8V signaling enable 0: 1.8V switching is disabled 1: 1.8V switching is enabled
PD3_AF0	EMMC Hardware Reset Output Pin	Active low. EMMC hardware reset 0: reset is active 1: reset is not active

Table 39-1 shows the pins used by SDMMC2 and their corresponding functions.

Table 39-2 SDMMC2 Pin Definitions

Pin Name	Function Name	Description
PB14_AF1 PG9_AF2	Bidirectional Data 0 Pin	Data 0 Input/Output. Used in SD/SDIO/MMC mode.
PB15_AF1 PG10_AF3	Bidirectional Data 1 Pin	Data 1 Input/Output. Used in SD/SDIO/MMC mode.
PB3_AF0 PG11_AF3	Bidirectional Data 2 Pin	Data 2 Input/Output. Used in SD/SDIO/MMC mode.
PB4_AF1 PG12_AF2	Bidirectional Data 3 Pin	Data 3 Input/Output. Used in SD/SDIO/MMC mode.
PB8_AF3 PG4_AF3	Bidirectional Data 4 Pin	Data 4 Input/Output. Used in MMC 8 bit mode.
PB9_AF2 PG5_AF4	Bidirectional Data 5 Pin	Data 5 Input/Output. Used in MMC 8 bit mode.
PC6_AF2 PG13_AF2	Bidirectional Data 6 Pin	Data 6 Input/Output. Used in MMC 8 bit mode.
PC7_AF2 PG14_AF3	Bidirectional Data 7 Pin	Data 7 Input/Output. Used in MMC 8 bit mode.
PA0_AF1 PD7_AF1	Bidirectional Command Pin	Command Input/Output to send command or receive response from card.
PD4_AF1	Write Protection Input Pin	Active High. SD Card write protect. 0: Card is not write protected 1: Card is write protected.
PD5_AF1 PG5_AF3	Card Detection Input Pin	Active Low. This pin is for the card insert detection. 0: Card is inserted

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Pin Name	Function Name	Description
		1: Card is not inserted
PC4_AF2 PG4_AF2	Looped-Back Clock Input Pin	Clock looped back from PAD
PC1_AF2 PD6_AF1	SD Clock Output Pin	SD/SDIO/MMC clock to card
PG5_AF3	Command Direction Output Pin	0: Command pin is input 1: Command pin is output
PG13_AF1	Data 0 Direction Output Pin	0: Data 0 is input 1: data 0 in output
PG14_AF2	Data 1/2/3 Direction Output Pin	0: Data 1/2/3 is input 1: Data 1/2/3 is output
PE9_AF4 PF8_AF3 PI1_AF2	LED CTRL Output Pin	LED output indication 0 (LED OFF): no function 1 (LED ON): To Caution the user not to remove the card while the SD card is being accessed.
PC5_AF8 PI8_AF2 PJ13_AF0	1.8V Switching Enable Output Pin	1.8V signaling enable 0: 1.8V switching is disabled 1: 1.8V switching is enabled
PG15_AF3	EMMC Hardware Reset Output Pin	Active low. EMMC hardware reset 0: reset is active 1: reset is not active

39.5 Function Description

39.5.1 Clocks

The following descriptions describe clocks for SDMMC

xin_clk

This is the main clock used for the SD Interface side of the SDMMC Core. This clock input is used to generate SD Clock based on the divisor value programmed by the user configurations. For maximum efficiency this should be around 104Mhz (maximum IO frequency) (for SD3.0 and eMMC4.51)/52Mhz (for eMMC 4.54.5) and 50Mhz (for SD2.0).

hclk

This is the system bus clock. This clock is used for AHB Slave and Master modules. The SD Register Set and the DMA Controller also operate on this Clock.

sd_clk

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This clock is generated internally. It is derived from xin_clk based on the control register (SDHOST_CTRL2) value programmed by the user settings. This Clock is used by the most of the SD control logic (SD Command Control, SD Transmit Control, SD Tuning Module and 2nd side of the Block Buffer).

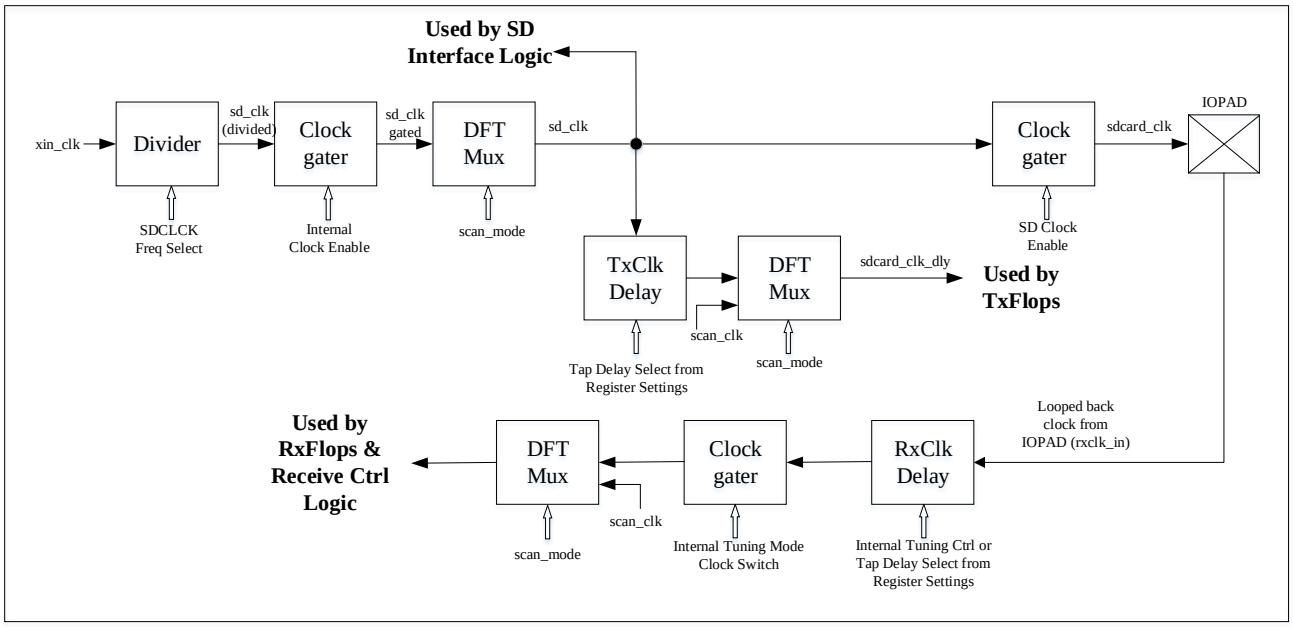
sdcard_clk

Same as sd_clk, except that this is available only when SD Clock Enable is set by the user settings. This is the clock supplied to the SD Card. The SDMMC supports both full speed and high speed card. For high speed card, SDMMC clocks out the data at rising edge of sd_clk and for full speed card, SDMMC clocks out the data at falling edge of sd_clk. During read transaction when the read FIFOs are full, there is no space to accept one block of data from card SDMMC will stop the clock to card so overrun condition will not occur on SD side.

rxclk_in

This is the Looped back clock from the sdcard_clk PAD (CLK). This will account for the delay on the CLK being driven onto the SD Interface through the Chip and the IO PAD.

Figure 39-4 SDMMC Clock architecture



39.5.2 Resets

SDMMC uses asynchronous reset to reset, even though the reset itself is synchronous to the corresponding clock domain. Reset from system bus domain is the primary reset input and is synchronized with hclk. Internally the independent reset signal is generated for each of the Clock domain. Also When the SD Clock Enable is set, the Reset is generated to make sure that the logic operating on sd_clk is properly reset. Similarly, when the SDCARD Clock Enable is set, the Reset is generated to make sure that the logic operating on the rx_clk is properly reset. It is expected that the system bus reset is asserted for a minimum of 16 Clocks. Any internally generated Reset Signals are generated for at least 16 Clocks to make sure that all the flops are in reset state at the de-assertion of the reset. In addition, the software generated reset events can also be used to reset the Flops/Logic in the design.

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39.5.3 Frequency Range

Frequency for system bus clock depends on the system configuration.

Frequency range for sd_clk is 400 KHz to 104 MHz. In case of SD2.0, the Maximum frequency is 50 MHz.

39.5.4 FIFO Overrun And Underrun Conditions In DMA And Non-DMA Transfers

Write

During write transaction, SDMMC will transmit data to card only when a block of data is ready to transmit and also the card is not driving busy. So underrun condition will not occur on SD side. In DMA mode SDMMC initiates DMA READ from SDMMC's memory only if space is available to accept a block of data. In non-DMA mode, SDMMC will assert buffer write ready interrupt only if space is available to accept a block of data.

Read

During read transaction, when the internal Block Buffer is full it can not accept any more data from the card. In these circumstances, SDMMC will stop the clock to card in order to avoid Buffer Overrun condition. In case of SDIO mode and Read wait is enabled, the Read Wait signal is asserted to block the Card from sending any more data. In DMA mode Host controller initiates DMA WRITE to SDMMC's memory only on reception of block of data from card. In non-DMA mode, SDMCC will assert buffer read ready interrupt only on reception of block of data from card.

39.5.5 Transmit CMD/DAT delay

TX CMD/DAT Delay is used to delay the CMD/DAT lines to avoid the hold time violation in the card due to board layout timing issues. In some cases, the board layout may not be optimal and the CMD/DAT lines may have hold time violations on the card as the CLK and CMD/DAT are source synchronous for the card.
SDMMC implements the delay chain to delay the internal sd_clk that is being sent out on the CLK line (as sdcard_clk), and use this delayed clock to flop out the CMD/DAT lines. The TXClkDly Module impalements the Delay Buffers to generate a phase shifted clock. The variable delay output, the user can program the tap delay by settings to delay control register (SDMMC_DLYCTRL) in SDMMC Wrapper Register.

- OTDS[3:0]: used to select the optimum Delay from 1-16 tap delay lines.
- OTDE: used to enable Output Tap Delay.

The TxFlops Module implements the final stage registers using this delayed clock. The TxFlops also implements two sets of registers for each CMD/DAT lines (one for positive edge output and another one negative edge output). In case of DDR we use both the flops and in SDR mode we use only the positive edge only (DS mode uses the negative edge outputs though)
When operating in Default DS, the outputs are driven on the falling edge of the Clock so that the card can have enough setup/hold time when latching the data. In this case the Output Tap Delay Control is not necessary and should

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

be disabled. When operating in HS modes and other SDR modes the output Data is driven on the rising edge of the Clock. The same clock is also output to the Card (SD Interface). Based on the Post silicon board layout, the Card might see Hold time violations for CMD/DAT lines. To avoid this, the output Tap Delay lines can be programmed under User Control.

39.5.6 Receive Clock Tap Delay

RX Clock Delay is used for the tuning/delaying the receive clock so as to align the clock in the center of data window. This is used in both auto tuning (in SDR50 and SDR104 mode) and optional manual tuning (for the high speed modes like DDR).

During read operation, SDMMC acts as a receiver and the data may not be exactly aligned with respect to the clock. The Clock signal can be delayed either by Auto Tuning or Manual Tuning so that the clock is center aligned to receive data.

For SDR104 mode or for SDR50(optional) automatic tuning is performed. SDMMC has an algorithm to correctly find the center of the eye for better timing. The Tuning Procedure selects one of the Phase of the Clock (rxclk_in) for each iteration. At the end of tuning, the right phase of the Clock is selected that is in the center of the Data.

In other modes (ex: DDR50) the manual tuning of the sdcard_clk (rxclk_in) can be performed using the user configurations in the delay control register (SDMMC_DLYCTRL) in SDMMC Wrapper Register.

- ITDS[4:0]: used to select the optimum Delay from 1-32 tap delay lines.
- ITDE: used to enable Input Tap Delay.

The Clock delay is implemented using Tap Delay that generates multiple phases of the clock. The Maximum number of phases (Tap Delay) supported is 32, even though the typical number of phases (Tap Delay) is 4 or 8.

For Auto Tuning the tuning count configuration (SDMMC_CFG1.TCNT[5:0]) should be programmed with the number of phases of the Clock being generated.

For example, when the Number of phases of clock is 4, then the four phases of the clocks are, clk_00, clk_90, clk_180, clk_270. Similarly, when the number of phases of clock is 8, the eight phases of the clocks are clk_00, clk_45, clk_90 and so on. When using all 32-phases the different between the two phases of clock will be 1/32 of the rxclk_in.

39.5.7 Advanced DMA (ADMA)

SD Host Controller Standard Specification Version 2.00 defines the ADMA (Advanced DMA) Transfer algorithm. The DMA algorithm defined in the SD Host Controller Standard Specification Version 1.00 is called SDMA (Single Operation DMA). SDMA had disadvantage that DMA Interrupt generated at every page boundary disturbs CPU to reprogram the new system address. This SDMA algorithm forms a performance bottleneck by interruption at every page boundary. ADMA adopts scatter gather DMA algorithm so that higher data transfer speed is available. The User Program can program a list of data transfers between system memory and SD card to the Descriptor Table before executing ADMA. It enables ADMA to operate without interrupting the CPU.

There are two types of ADMA; ADMA1 and ADMA2. ADMA1 can support data transfer of only 4KB aligned data in system memory. ADMA2 improves the restriction so that data of any location and any size can be transferred in system memory. The format of Descriptor Table is different between them. The Host Controller Specification Ver2.00 defines ADMA2 as standard ADMA and recommends supporting ADMA2 rather than ADMA1. DMA mode ADMA1 is not supported in Standard Host Controller versions 3.0 and latter. When the term "ADMA" is used in this document, it means ADMA2.

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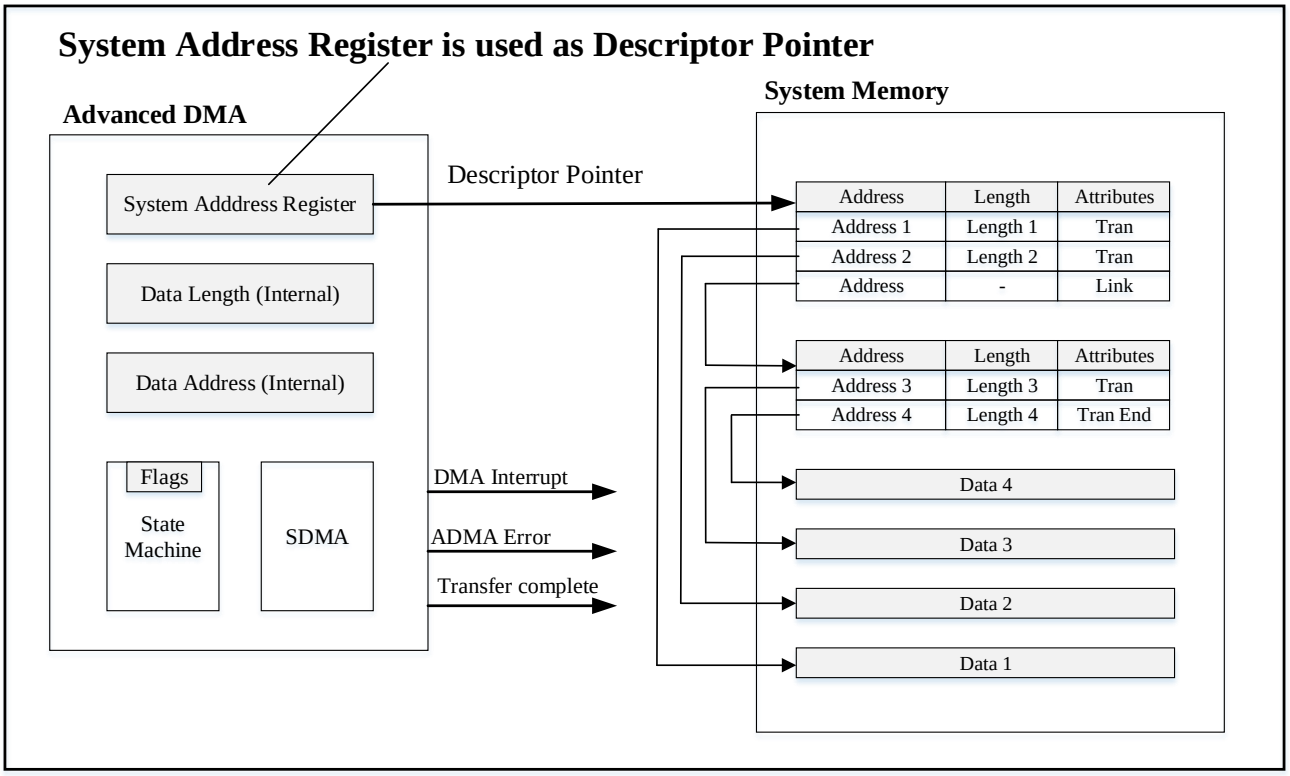
39.5.7.1 Block Diagram of ADMA2

Figure 39-5 Block Diagram of ADMA2



The 32-bit Descriptor Table is created in system memory by the User Program. Each descriptor line (one executable unit) consists with address, length and attribute field. The attribute specifies operation of the descriptor line. ADMA2 includes SDMA, State Machine and Registers circuits. ADMA2 does not use 32-bit SDMA System Address Register (SDHOST_DSADD – offset 00h) but uses the 64-bit Advanced DMA System Address register (SDHOST_ASADD0/1 offset 058h) for descriptor pointer. Writing Command register triggers off ADMA2 transfer. ADMA2 fetches one descriptor line and execute it. This procedure is repeated until end of descriptor is found (End=1 in attribute).

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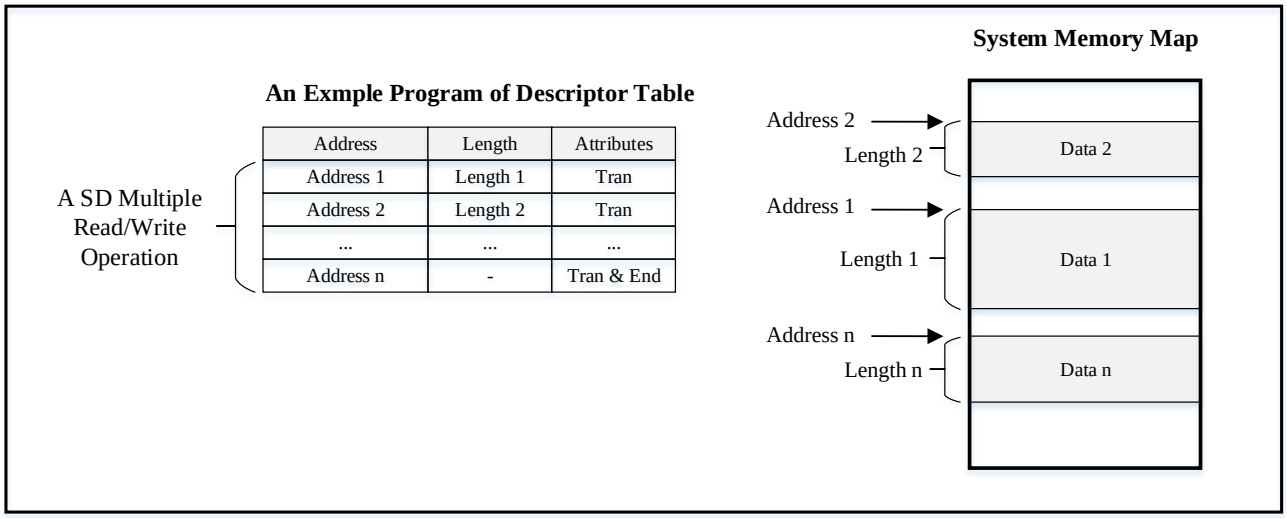
39.5.7.2 An Example of AMDA2 Programming

Figure 39-6 An Example of ADMA2 Data Transfer



The above figure shows a typical ADMA2 descriptor program. The User Program describes the Descriptor Table with each slice is placed somewhere in contiguous system memory. It describes the Descriptor Table with set of address, length and attributes. Each sliced data is transferred in turns as programmed in descriptor.

39.5.7.3 Data Address And Data Length Requirements

There are 3 requirements to program the descriptor.

The minimum unit of address is 4 bytes.

The maximum data length of each descriptor line is less than 64KB.

Total Length = Length 1 + Length 2 + Length 3 + ... + Length n = multiple of Block Size

If total length of a descriptor were not multiple of block size, ADMA2 transfer might not be terminated. In this case, the transfer should be aborted by data timeout.

Block Count settings in SDHOST Block Count and Size Configure Register (SDHOST_BLKCFG) limits the maximum of 65535 blocks transfer. If ADMA2 operation is less than or equal 65535 blocks transfer, Block Count setting can be used. In this case, total length of Descriptor Table shall be equivalent to multiply block size and block count. If ADMA2 operation is more than 65535 blocks transfer, Block Count setting shall be disabled by setting 0 to Block Count Enable in the Transfer Mode Register (SDHOST_TMODE). In this case, length of data transfer is not designated by block count but Descriptor Table. Therefore, the timing of detecting the last block on SD bus may be different and it affects the control of Read Transfer Active, Write Transfer Active and DAT line Active in the Present State register (SDHOST_PRESTS). In case of read operation, several blocks may be read more than required. The User Program shall ignore out of range error if the read operation is for the last block of memory area.

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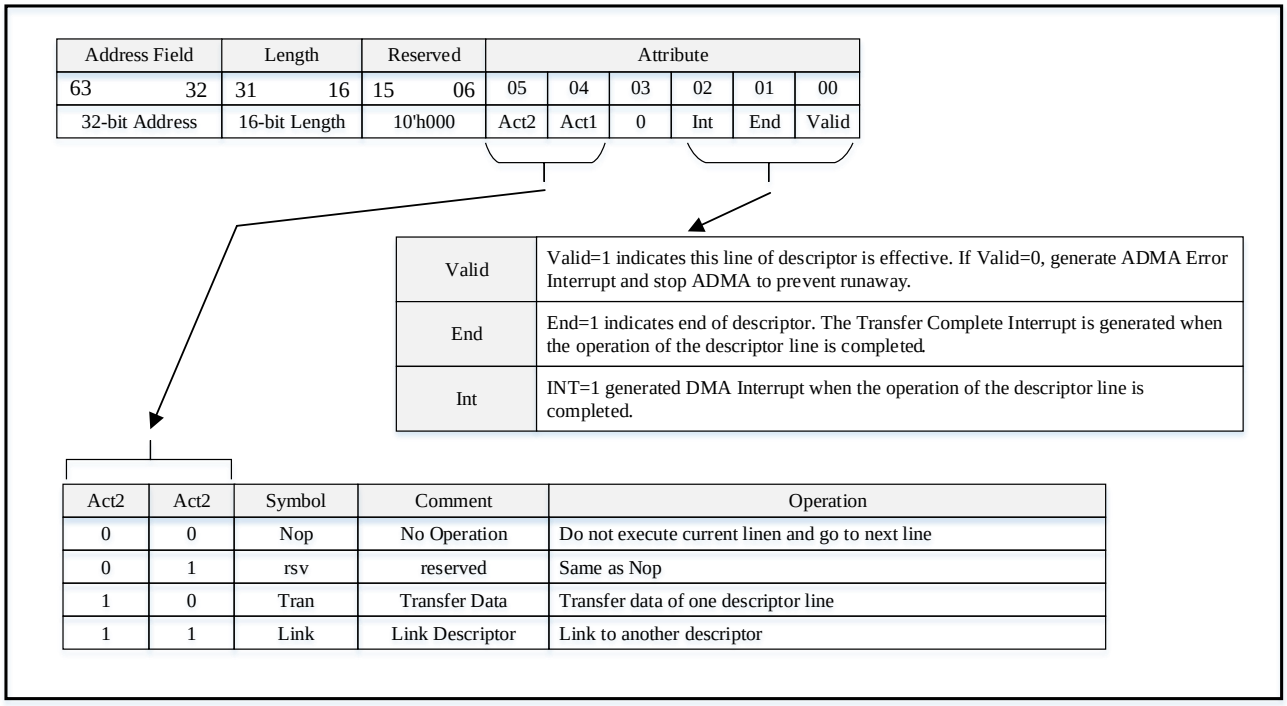
Email: sales@nsing.com.sg

39.5.7.4 Descriptor Table

Figure 39-7 32-bit Descriptor Table



The above figure shows the definition of 32-bit Address Descriptor Table. One descriptor line consumes 64-bit (8-byte) memory space. Attribute is used to control descriptor. 3 action symbols are specified. "Nop" operation skips current descriptor line and fetches next one. "Tran" operation transfers data designated by address and length field. "Link" operation is used to connect separated two descriptors. The address field of link points to next Descriptor Table. The combination of Act2=0 and Act1=1 is reserved and defined the same operation as “Nop”. A future version of SDMMC may use this field and redefine a new operation. 32-bit address is stored in the lower 32-bit of 64-bit address registers. Address field shall be set on 32-bit boundary (Lower 2-bit is always set to 0) for 32-bit address descriptor table.

The below table shows the definition of length field in the Descriptor Table.

Table 39-3 ADMA Length Field

Length Field	Value of Length
0x0000	65536 bytes
0x0001	1 byte
0x0002	2 bytes
……	……
0xFFFF	65535 bytes

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39.5.7.5 ADMA2 States

Below figure shows state diagram of ADMA2. 4 states are defined; Fetch Descriptor state, Change Address state, Transfer Data state, and Stop ADMA state. Operation of each state is explained in the later table.

Figure 39-8 State Diagram of the ADMA2

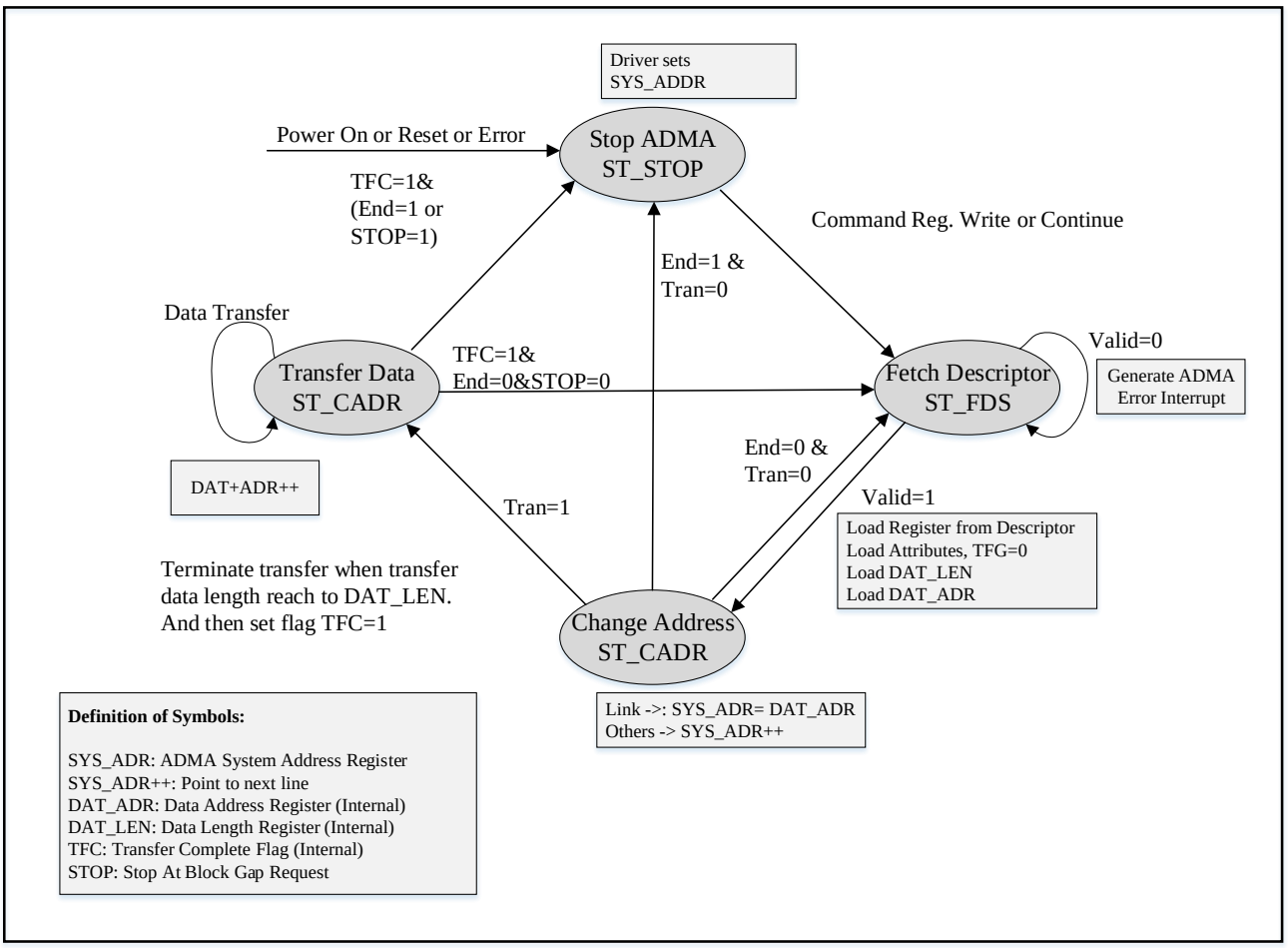

Table 39-4 ADMA2 States

State Name	Operation
ST_FDS (Fetch Descriptor)	ADMA2 fetches a descriptor line and set parameters in internal registers. Next go to ST_CADR state
ST_CADR (Change Address)	Link operation loads another Descriptor address to ADMA System Address register. In other operations, ADMA System Address register is incremented to point next descriptor line. If End=0, go to ST_TFR state. ADMA2 shall not be stopped at this state even if some errors occur.
ST_TFR	Data transfer of one descriptor line is executed between system memory and SD card. If data transfer continues (End=0) go to ST_FDS state. If data transfer completes, go to ST_STOP state.

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(Transfer Data)	
ST_STOP (Stop DMA)	ADMA2 stays in this state in following cases: (1) After Power on reset or software reset. (2) All descriptor data transfers are completed If a new ADMA2 operation is started by writing Command register, go to ST_FDS state.

ADMA2 does not support suspend / resume function but stop and continue are available. When the Stop At Block Gap Request in the SDHOST Control 1 register (SDHOST_CTRL1.SABGREQ) is set during the ADMA2 operation, the Block Gap Event Interrupt is generated when ADMA2 is stopped at block gap. SDMMC shall stop ADMA2 read operation by using Read Wait or stopping SD Clock. While stopping ADMA2, any SD commands cannot be issued. Error occurrence during ADMA2 transfer may stop ADMA2 operation and generate an ADMA Error Interrupt. The ADMA Error State field in the ADMA Error Status register (SDHOST_ADMAESTS) holds state of ADMA2 stopped. User Program can identify the error descriptor location by the following method: If ADMA stopped at ST_FDS state, the ADMA System Address Register points the error descriptor line. If ADMA stopped at ST_TFR or ST_STOP state, the ADMA System Address Register points the next location of error descriptor line. By this reason, ADMA2 shall not stop at ST_CADR state.

39.5.8 Programming Sequence

39.5.8.1 Non-DMA Transaction

The sequence non-using DMA is shown below

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Figure 39-9 Data Transfer Using DAT Line Sequence (Not Using DMA)

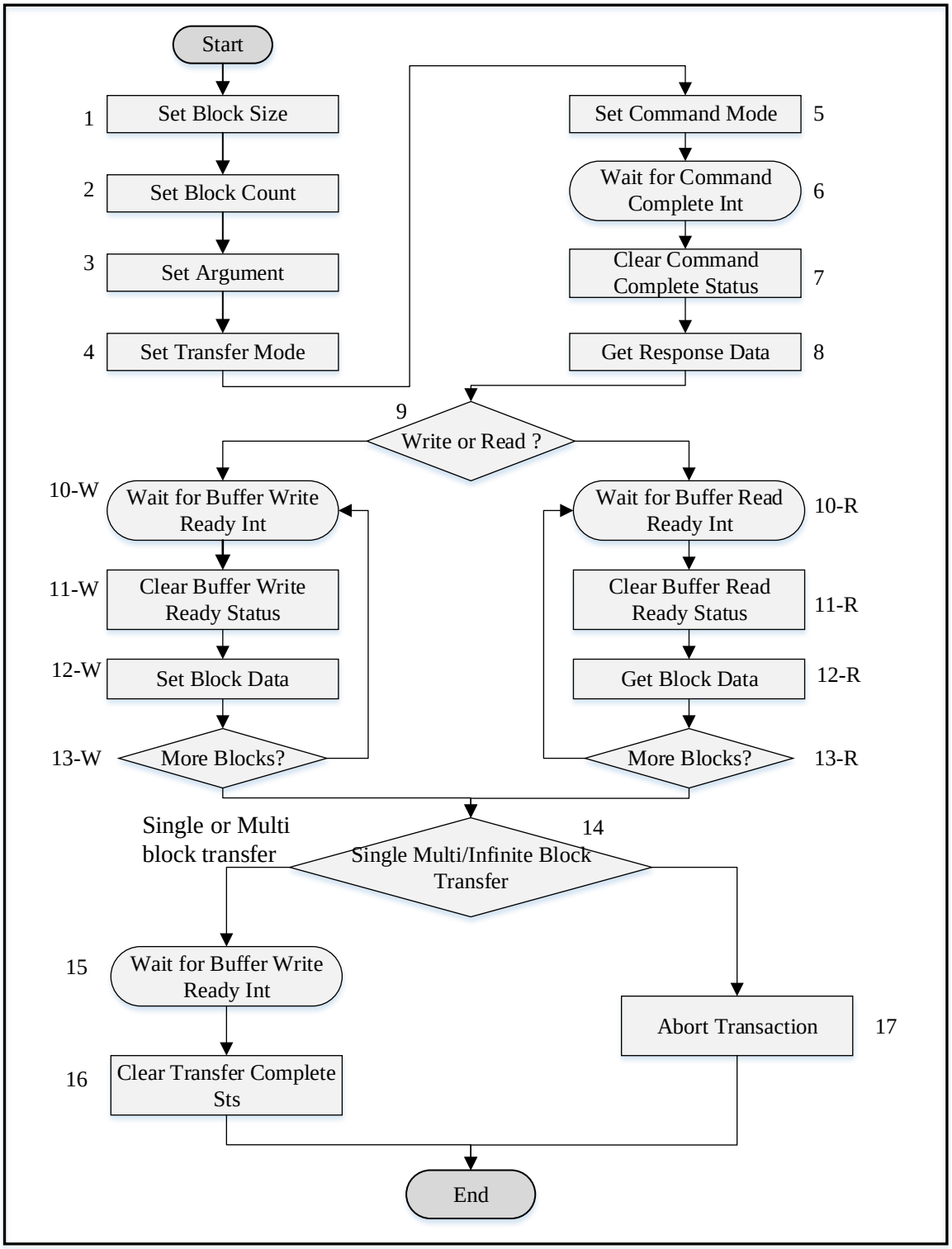

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Table 39-5 Non-DMA transaction

Step	Description
1	Set the value corresponding to SDHOST_BLKCFG.SIZE[11:0].
2	Set the value corresponding to SDHOST_BLKCFG.CNT[15:0].
3	Set the value corresponding to the issued command to Argument 1 register (SDHOST_CMDARG1).
4	Set the value to SDHOST_TMODE.BLKSEL and SDHOST_TMODE.NCNTE. Set the value corresponding to the issued command to Data Transfer Direction, Auto CMD12 Enable in the Transfer Mode Register (SDHOST_TMODE).
5	Set the value corresponding to the issued command to Transfer Mode Register (SDHOST_TMODE). When writing to the Command Index field (CMDX[5:0]) of this register , SD command is issued.
6	Wait for SDHOST_INTSTS.CMDC to be set.
7	Write 1 to SDHOST_INTSTS.CMDC bit for clearing this bit.
8	Read Response register (SDHOST_CMDRSP0/1/2/3) and get necessary information in accordance with the issued command.
9	In the case where this sequence is for write to a card, go to step (10-W). In case of read from a card, go to step (10-R).
10-W	Wait for Buffer Write Ready Interrupt in Interrupt Status Register (SDHOST_INTSTS). **Non DMA Write Transfer** On receiving the Buffer Write Ready interrupt, the CPU will act as a master and start transferring the data via Buffer Data Port Register (SDHOST_BUFDAT). Transmitter starts sending the data in SD bus when a block of data is ready in Buffer Data Port Register. While transmitting the data in SD bus the Buffer Write Ready interrupt is sent to the CPU for the second block of data. The CPU will act as a master and start sending the second block of data via Buffer Data Port Register. SDHOST_INTSTS.BUFWRDY bit will be asserted only when an internal FIFO is empty to receive a block of data.
11-W	Write 1 to SDHOST_INTSTS.BUFWRDY bit for clearing this bit.
12-W	Write block data (in according to the number of bytes specified at the step (1)) to Buffer Data Port register.
13-W	Repeat until all blocks are sent and then go to step (14).
10-R	**Non DMA Read Transfer** Buffer Read Ready interrupt is asserted whenever a block of data is ready in one of the internal FIFO. On receiving the Buffer Read Ready interrupt the CPU will act as a master and start reading the data via Buffer data port register. Receiver starts reading the data from SD bus only when a FIFO is empty to receive a block of data. When the FIFO is full, SDMMC will stop the data coming from the card through read wait mechanism (if card supports read wait) or through clock stopping.

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	Wait for Buffer Read Ready Interrupt
11-R	Write 1 to SDHOST_INTSTS.BUFRRDY for clearing this bit.
12-R	Read block data (in according to the number of bytes specified at the step (1)) from the Buffer Data Port register(SDHOST_BUFDAT).
13-R	Repeat until all blocks are received and then go to step (14).
14	If this sequence is for Single or Multiple Block Transfer, go to step (15). In case of Infinite Block Transfer, go to step (17).
15	Wait for SDHOST_INTSTS.TC to be set.
16	Write 1 to SDHOST_INTSTS.TC for clearing this bit.
17	Perform the sequence for Abort Transaction.

Note: Step 1 & 2 can be executed at the same time. Step 4 & 5 can be executed at the same time.

39.5.8.2 DMA Transaction

The sequence for Using DMA is shown below:

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Figure 39-10 Data Transfer Using DAT Line Sequence (Using DMA)

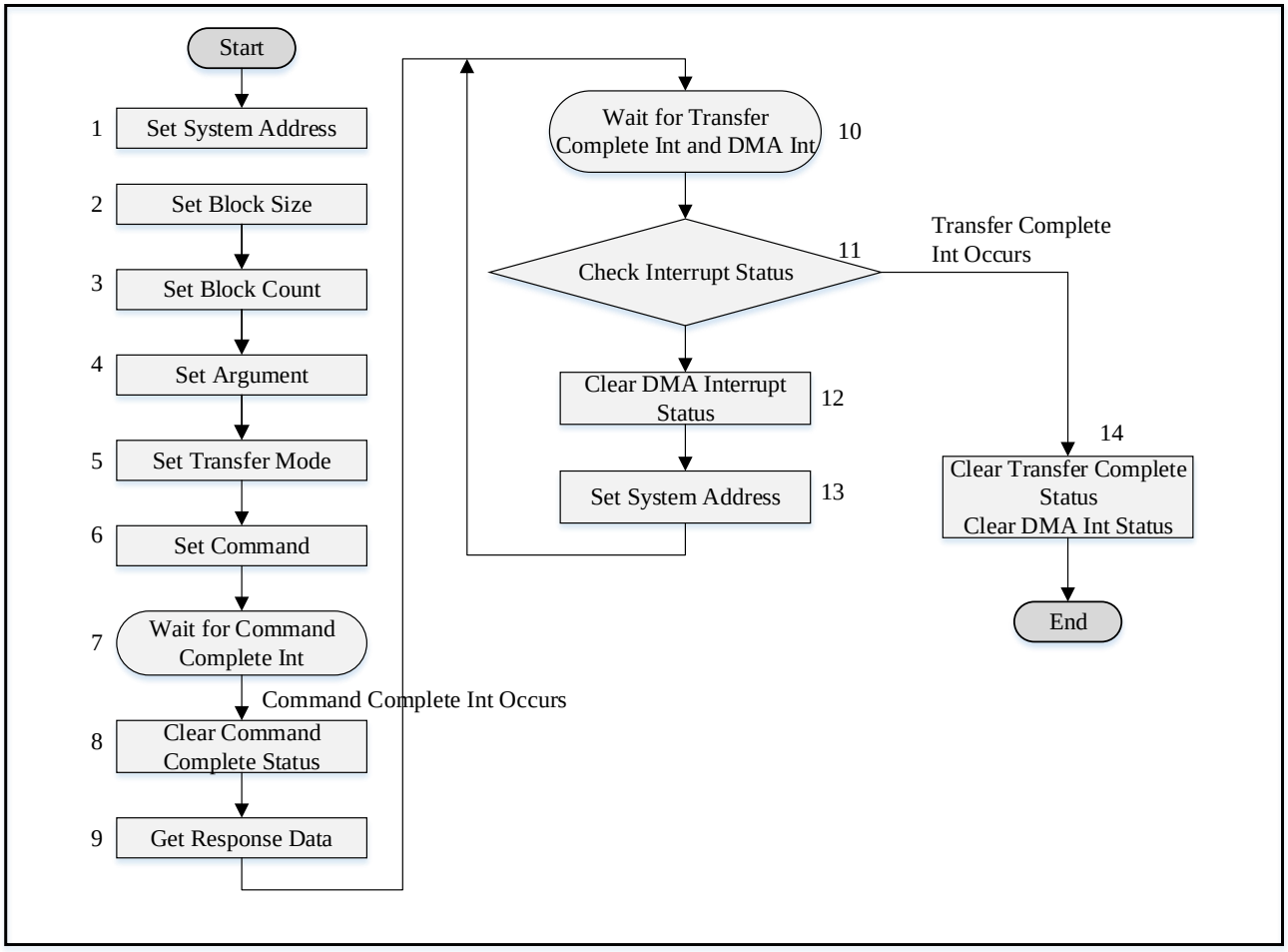

Table 39-6 DMA Transfer Sequence

Step	Description
1	Set the system address for DMA in SDHOST_DSADD register.
2	Set the value corresponding to SDHOST_BLKCFG.SIZE[11:0].
3	Set the value corresponding to SDHOST_BLKCFG.CNT[15:0].
4	Set the value corresponding to the issued command to Argument 1 register (SDHOST_CMDARG1).
5	Set the value to SDHOST_TMODE.BLKSEL and SDHOST_TMODE.NCNTE. Set the value corresponding to the issued command to Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the Transfer Mode Register (SDHOST_TMODE).
6	Set the value corresponding to the issued command to Transfer Mode Register (SDHOST_TMODE). When writing to the Command Index field (CMDX[5:0]) of this register , SD command is issued.
7	Wait for SDHOST_INTSTS.CMDC to be set.

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8	Write 1 to SDHOST_INTSTS.CMDC bit for clearing this bit.
9	Read Response register and get necessary information in accordance with the issued command. **DMA read transfer** On receiving the response end bit from the card for the write command (data flowing from SDMMC to Card), SDMMC will act as the master and request the System bus. After receiving the grant SDMMC will start reading a block of data from the system memory and fills the first FIFO. Whenever a block of data is ready the transmitter will start sending the data in SD bus. While transmitting the data in SD bus, SDMMC requests the bus to fill the second block in second FIFO. Ping Pong FIFOs are used to increase the throughput. Similarly, SDMMC reads a block of data from the system memory whenever a FIFO is empty. This will continue till all the blocks are read from the System memory. Transfer complete Interrupt will be set only after transferring all the blocks of data to the card. **DMA write transfer** The block of data received from the Card (data flowing from Card to Host) is stored in first half of the FIFO. Whenever a block of data is ready, SDMMC will act as the master and request the System bus. After receiving the grant, the host controller will start writing a block of data into the system memory from the first FIFO. While transmitting the data into System memory, SDMMC will receive the second block of data and store in second FIFO. Similarly, SDMMC writes a block of data into the system memory whenever data is ready. This will continue till all the blocks are transferred to the System memory. Transfer complete Interrupt will be set only after transferring all the blocks of data to the System memory. *Note: SDMMC will receive a block of data from the card only when it has room to store a block of data in FIFO. When both the FIFOs are full, SDMMC will stop the data coming from the card through read wait mechanism (if card supports read wait) or through clock stopping.*
10	Wait for SDHOST_INTSTS.TC and SDHOST_INTSTS.DMAINT to be set.
11	If SDHOST_INTSTS.TC is set 1, go to Step (14) else if SDHOST_INTSTS.DMAINT is set to 1, go to Step (12). SDHOST_INTSTS.TC is higher priority than SDHOST_INTSTS.DMAINT.
12	Write 1 to SDHOST_INTSTS.DMAINT to clear this bit.
13	Set the next system address of the next data position to the System Address register and go to Step (10).
14	Write 1 to SDHOST_INTSTS.TC and SDHOST_INTSTS.DMAINT to clear this bit.

Note: Step 2 & 3 can be executed at the same time. Step 5 & 6 can be executed at the same time

For example, if SDMMC wants to transfer 4KB of data to the Card. Assume the maximum block size is 512 bytes, then user need to program the block size as 512 and block count with the value 8.

The AHB Master and Transmitter residing inside the SDMMC will get the information (how much data to transfer) from these registers. Using the above information, the AHB master will act as a master and initiate a data read transaction (to read a block of data -512 bytes from the system memory). Whenever a block of data is ready in FIFO, the transmitter will start transmitting the block of data (512) in SD bus. After transmitting the entire block of data to the card, the transmitter will wait for a status response from the card. Transmitter will send the next block of data

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only, when it receives a good status response from the card for the previous block of data otherwise the transaction will be aborted and the host will go for a fresh transaction.

39.5.8.3 ADMA Transaction

The following figure and table describe the ADMA transaction sequence.

Figure 39-11 ADMA Transaction Flow

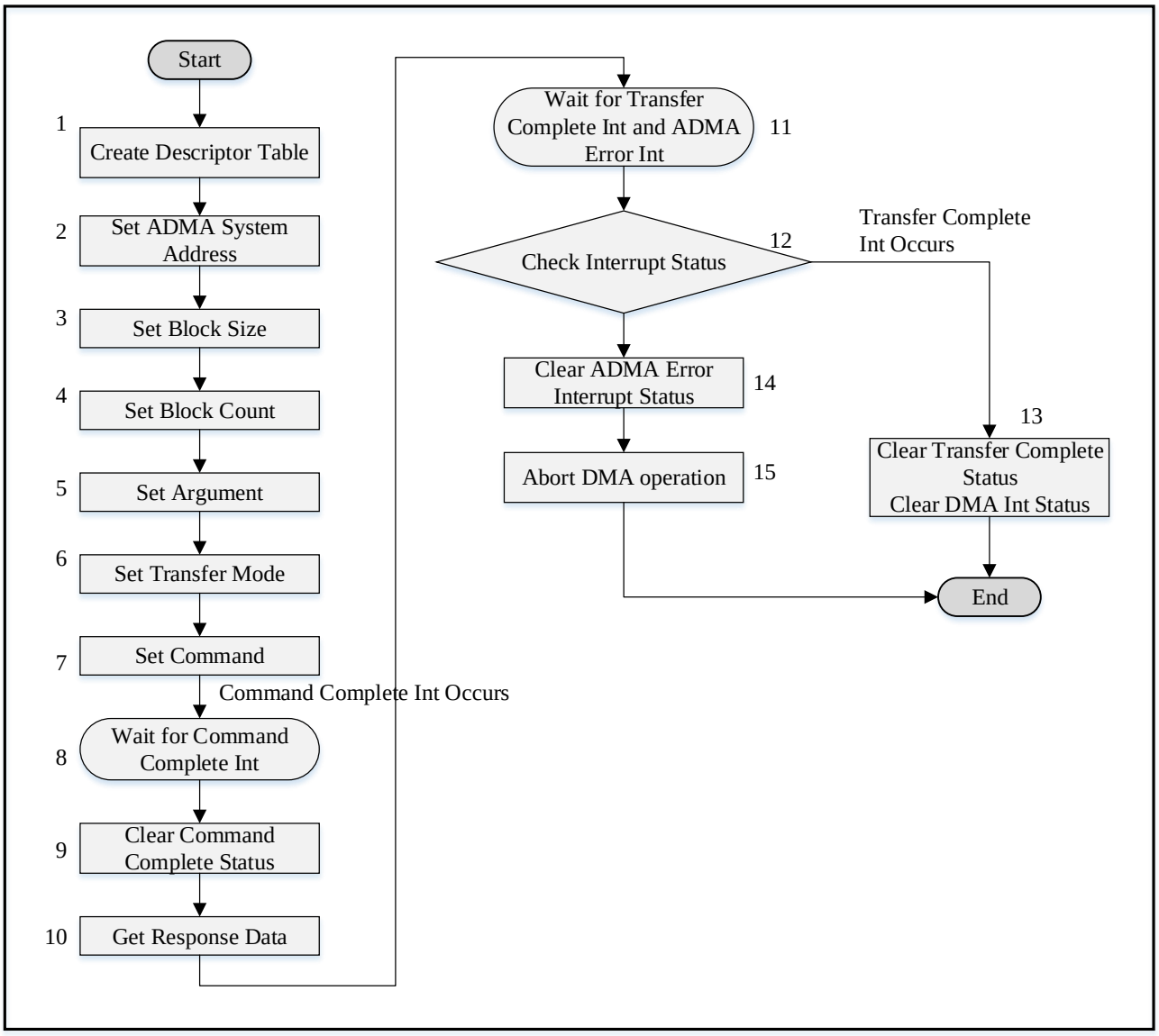

Table 39-7 ADMA Transaction Flow

Step	Description
1	Create Descriptor table for ADMA in the system memory

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2	Set the Descriptor address for ADMA in the ADMA System Address register.
3	Set the value corresponding to SDHOST_BLKCFG.SIZE[11:0].
4	Set the value corresponding to SDHOST_BLKCFG.CNT[15:0]. If SDHOST_TMODE.BCNTE is set to 1, total data length can be designated by the Block Count and the Descriptor Table. These two parameters shall indicate same data length. However, transfer length is limited by the 16-bit Block Count. If SDHOST_TMODE.BCNTE is set to 0, total data length is designated by not Block Count but the Descriptor Table. In this case, ADMA reads more data than length programmed in descriptor from SD card. Too much read operation is aborted asynchronously and extra read data is discarded when the ADMA is completed
5	Set the value corresponding to the issued command to Argument 1 register (SDHOST_CMDARG1).
6	Set the value to SDHOST_TMODE.BLKSEL and SDHOST_TMODE.NCNTE. Set the value corresponding to the issued command to Data Transfer Direction, Auto CMD12 Enable and DMA Enable in the Transfer Mode Register (SDHOST_TMODE).
7	Set the value corresponding to the issued command to Transfer Mode Register (SDHOST_TMODE). When writing to the Command Index field (CMDX[5:0]) of this register , SD command is issued.
8	Wait for SDHOST_INTSTS.CMDC to be set.
9	Write 1 to SDHOST_INTSTS.CMDC bit for clearing this bit.
10	Read Response register and get necessary information in accordance with the issued command.
11	Wait for SDHOST_INTSTS.TC and SDHOST_INTSTS.ADMAERR to be set.
12	If SDHOST_INTSTS.TC is set 1, go to Step (13) else if SDHOST_INTSTS.ADMAERR is set to 1, go to Step 14
13	Write 1 to SDHOST_INTSTS.TC to clear this bit.
14	Write 1 to SDHOST_INTSTS.ADMAERR to clear this bit.
15	Abort ADMA operation. SD card operation should be stopped by issuing abort command. If necessary, User Program checks ADMA Error Status register to detect why ADMA error is generated.

Note: Step 3 & 4 can be executed at the same time. Step 6 & 7 can be executed at the same time

39.5.8.4 Abort Transaction

An Abort transaction is performed using CMD12 for a SD Memory Card and by using CMD52 for a SDIO Card. There are two cases where the HD needs to do an Abort Transaction.

(1) When the User Program stops infinite block transfers.

(2) When the User Program stops transfers while a multiple block transfer is exacting.

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There are two ways to issue an Abort command. The first is an Asynchronous abort. The second is a Synchronous Abort. In an Asynchronous Abort sequence, the User Program can issue an Abort Command at anytime unless Command Inhibit (CMD) in the Present State Register (SDHOST_PRESTS) is set to 1. In a Synchronous Abort, the User Program shall issue an Abort command after the data transfer stopped by using Stop At Block Gap Request in the SDHOST Control 1 register (SDHOST_CTRL1.SABGREQ)

39.5.8.4.1 Synchronous Abort

The flow of synchronous Abort is as below:

Figure 39-12 Synchronous Abort Transaction

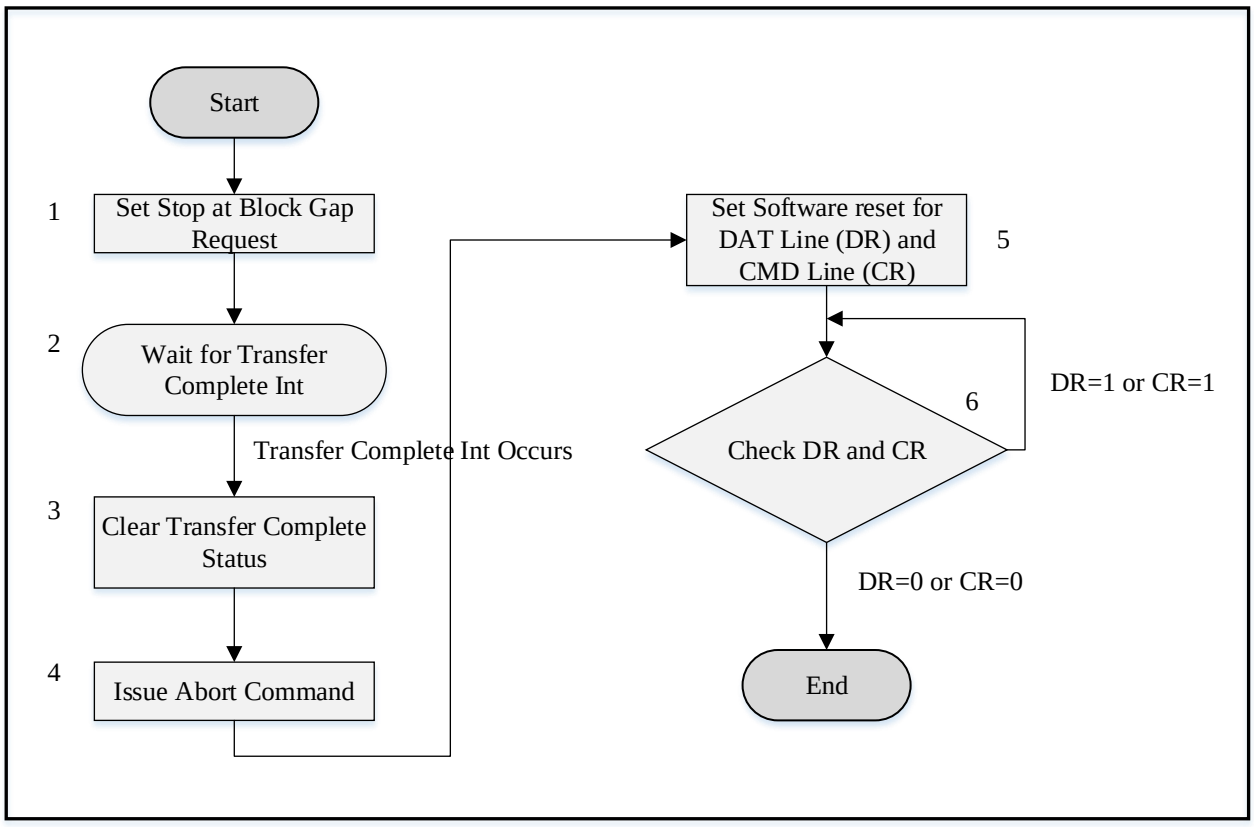

Table 39-8 Synchronous Abort Flow

Step	Description
1	Set SDHOST_CTRL1.SABGREQ to 1 to stop SD transactions.
2	Wait for SDHOST_INTSTS.TC to be set.
3	Write 1 to SDHOST_INTSTS.TC for clearing this bit.
4	Issue Abort Command
5	Set both SDHOST_CTRL2.SWRSTDL and SDHOST_CTRL2.SWRSTCL to 1 to do software reset.

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6	Check SDHOST_CTRL2.SWRSTDL and SDHOST_CTRL2.SWRSTCL. If both SDHOST_CTRL2.SWRSTDL and SDHOST_CTRL2.SWRSTCL are 0, go to “END”. If either SDHOST_CTRL2.SWRSTDL OR SDHOST_CTRL2.SWRSTCL is 1, repeat step(6).

39.5.8.4.2 Asynchronous Abort

The flow for asynchronous abort is shown below:

Figure 39-13 Asynchronous Abort Flow

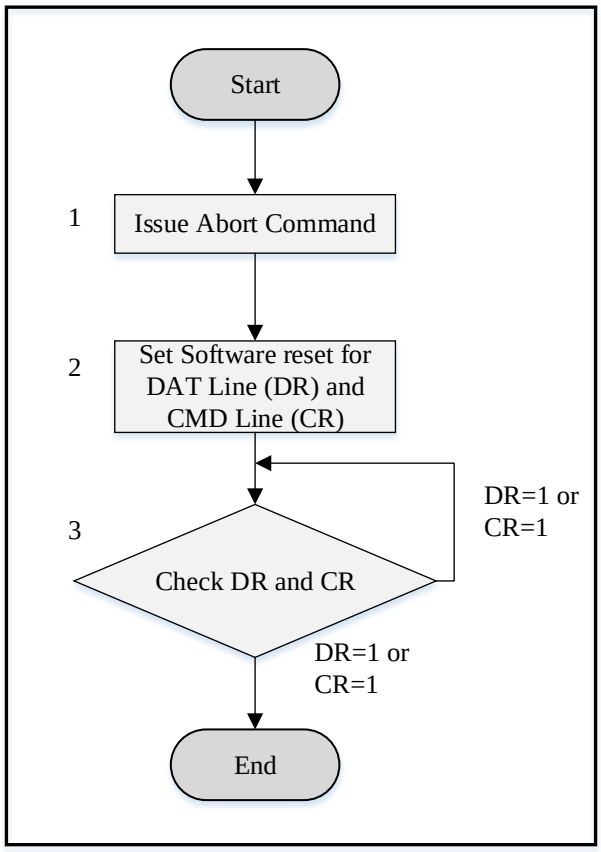

Table 39-9 Asynchronous Abort Flow

Step	Description
1	Issue Abort Command.
2	Set both SDHOST_CTRL2.SWRSTDL and SDHOST_CTRL2.SWRSTCL to 1 to do software reset.
3	Check SDHOST_CTRL2.SWRSTDL and SDHOST_CTRL2.SWRSTCL. If both SDHOST_CTRL2.SWRSTDL and SDHOST_CTRL2.SWRSTCL are 0, go to “END”. If either SDHOST_CTRL2.SWRSTDL OR SDHOST_CTRL2.SWRSTCL is 1, repeat step(3).

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39.5.8.5 Boot Operation

The boot operation is described as below

39.5.8.5.1 Normal Boot Operation

User Program writes the boot timeout value into Boot Timeout Control Register (SDHOST_BOOTTCTRL) as per the eMMC4.3+ spec. When User Program sets the "BOOTEN" bit to 1 in Control 1 Register (SDHOST_CTRL1) and Data Transfer Direction Select (DATDIR) bit to "1" in Transfer Mode Register (SDHOST_TMODE), SDMMC drives the CMD line to "0" for boot operation.
If SDMMC is configured to wait for boot acknowledge from the eMMC4.3+ device, it receives the boot acknowledgement and asserts the Boot Acknowledge interrupt to the CPU.

If SDMMC doesn't receive the boot acknowledgement from the device within the timeout value, it will assert the Data Timeout Error interrupt.
After servicing the boot acknowledge interrupt or data timeout error interrupt, User programs the Boot Timeout Control Register with boot data timeout value.

The eMMC4.3+ device starts sending the boot data on the data line and SDMMC sends the same to system whenever a block of data is received from device.
SDMMC terminates the boot operation when the programmed number of blocks is transferred to the System. User Program can write " SDHOST_CTRL1.BOOTEN" as "0" and then it shall wait for Boot Terminate Interrupt. After the Boot Termination Interrupt comes, the User Program issues soft reset for DATA line to SDMMC to reset the data state machines to idle state.

The boot operation can also be terminated in between the boot transfer. Program SDHOST_CTRL1.SABGREQ while transfer is going on and then wait for Transfer Complete interrupt. Once User Program receives the Transfer Complete Interrupt, it shall clear the Boot Enable and then issues soft reset for DATA line to SDMMC to reset the data state machines to idle state.

There is no need to perform error recovery sequence in case data timeout interrupt occurs during boot operation (i.e. ignore sending abort command, soft reset and just clear the Timeout Interrupt and proceed with the boot flow).

If the device sends wrong acknowledgement to SDMMC, it will assert Data CRC Error Interrupt to CPU. In this case, User Program has to stop the boot mode operation by setting BOOTEN as "0" and write soft reset for CMD and data line.
If the device sends end bit as "0" in acknowledgement to SDMMC, it will assert Data End Bit Error Interrupt to the CPU.
User Program stops the boot mode operation by setting BOOTEN as "0" in Control 1 Register and write soft reset for CMD and data line.

Note: Enable SDHOST_CTRL1.BOOTACKC bit during boot operation. If failed, SDMMC will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledge first and followed by boot data.

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39.5.8.5.2 Alternate Boot Operation

User Program writes the boot timeout value as per the eMMC4.3+ spec into Boot Timeout Control register (SDHOST_BOOTTCTRL).
If the SDHOST_CTRL1.BOOTINALT (Boot in Alternative mode) and SDHOST_CTRL1.BOOTEN are set to 1 and Data Transfer Direction Select (SDHOST_TMODE.DATDIR) bit is set to "1", SDMMC drives the CMD0 (0xFFFFFFFA) on the CMD line.
The system shall wait for Command Complete Interrupt before Boot Acknowledge Receive (BOOTACKR) interrupt.
If SDMMC is configured to wait for boot acknowledge from the eMMC4.3+ device, it receives the boot acknowledgement and asserts the Boot Acknowledge interrupt to the CPU.

The eMMC4.3+ device starts sending the boot data on the data line and SDMMC sends the same to system whenever a block of data is received from device.
SDMMC terminates the boot operation when the programmed number of blocks is transferred to the System. User Program can write "BOOTEN" and “BOOTINALT” as "0" in Control 1 Register and then it shall wait for Boot Terminate Interrupt. Once the CPU receives the Boot Termination Interrupt. It needs to program SDMMC to send CMD0 to inform the device about the boot operation complete. It shall program the Transfer Mode Register (SDHOST_TMODE) with argument "0x00000000" for the cmd0 (CMD type as ABORT) and waits for command complete. After that the User Program needs to issues the soft reset for data to SDMMC to reset the data state machines to idle state.

The boot operation can be terminated at any time. Program the Stop At Block Gap request while transfer is going on and then wait for Transfer Complete Interrupt. Once the CPU receives the transfer complete interrupt, it shall clear the BOOTEN, BOOTINALT and then the User Program needs to send CMD0 to inform the device about the boot operation complete. User Program shall program the Transfer Mode register with argument "0x00000000" for the cmd0 (CMD type as ABORT) and waits for Command Complete. After that the driver need to issues the soft reset for data to SDMMC to reset the data state machines to idle state.
If SDMMC doesn't receive the acknowledgement from the device with in timeout value, it will assert the Data Timeout Error interrupt. User programs the Boot Timeout Control Register with boot data timeout value.
There is no need to perform error recovery sequence in case of data timeout interrupt as mentioned above.
If the device sends wrong acknowledgement to SDMMC, it will assert Data CRC Error Interrupt to CPU. In this case, User Program has to stop the boot mode operation by setting BOOTEN and BOOTINALT as "0" and write soft reset for CMD and data line.

If the device sends end bit as "0" in acknowledgement to SDMMC, it will assert Data End Bit Error Interrupt to the CPU.
User Program stops the boot mode operation by setting BOOTEN and BOOTINALT as "0" in Control 1 Register and write soft reset for CMD and data line.

Note: Enable the Boot Acknowledge Check (BOOTACKC) bit in Control 1 Register during boot operation. If failed, SDMMC will not wait for boot acknowledge from the card and send out data CRC error when the card sends boot acknowledge first and followed by boot data.

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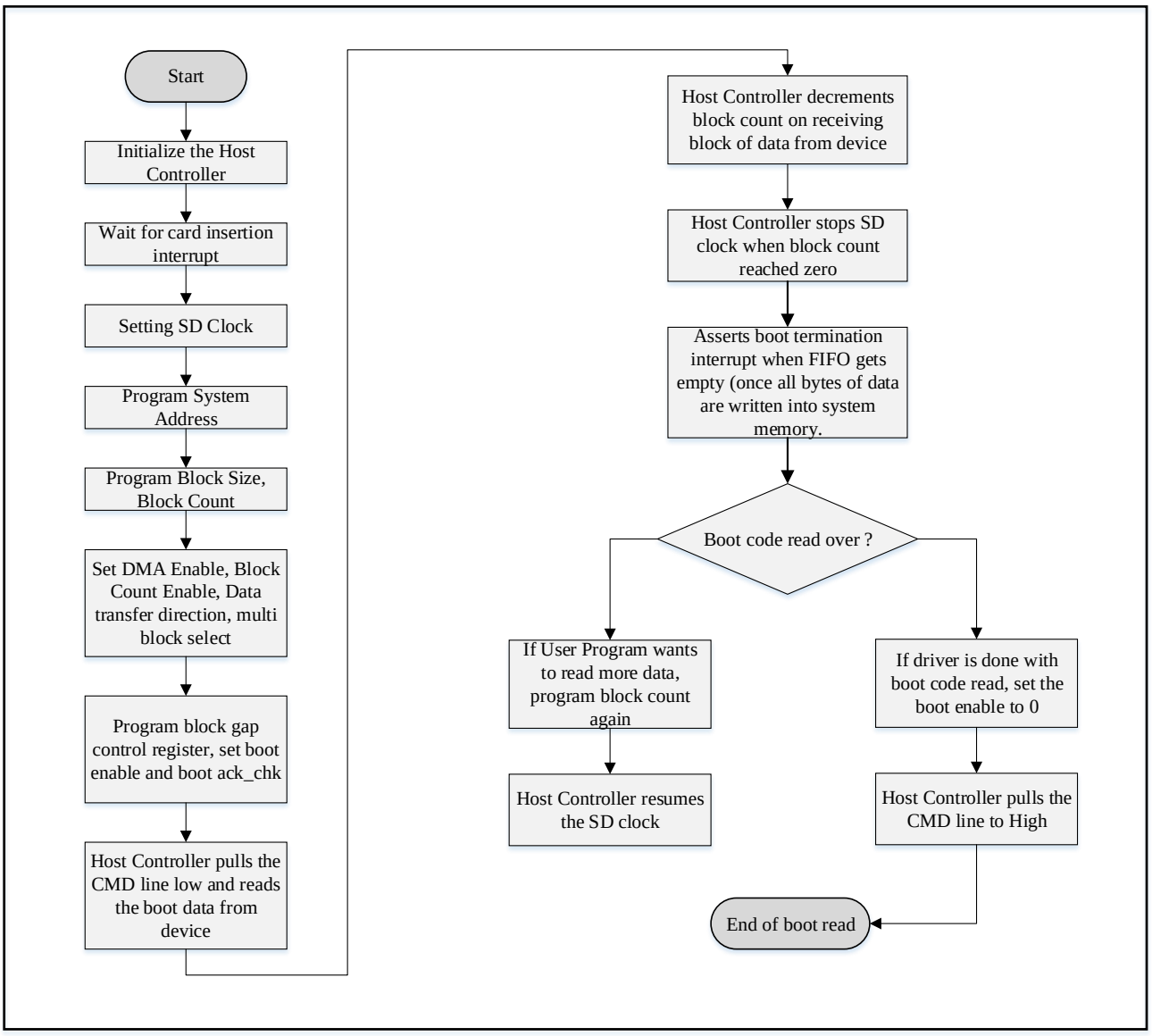
39.5.8.5.3 Boot Code Chunk Read Operation

The following figure explains the boot code read done as chunks of data (i.e., the User Program can read the boot data as 2K, 4K, 1K and 8K etc. instead of 128K at a time

Figure 39-14 Boot Code Access Flow Diagram



- After Power On Reset, Initialize the SDMMC (Host Controller)
- Wait for Card Insertion Interrupt
- Setting SD Clock in SD Host Control 2 Register
- Program System Address Register
- Program Block Size, Block Count in Block Count and Size Configure Register
- Set SDHOST_TMDE.DMAE,SDHOST_TMDE.BCNTE,SDHOST_TMDE.DATDIR adn SDHOST_TMDE.BLKSEL.
- Program SDHOST_CTRL1.BOOTEN, SDHOST_CTRL1.BOOTACKC bits.
- SDMMC pulls the CMD line low and read the boot data from device.

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- SDMMC decrements block count on receiving block of data from device (*).
- SDMMC stops SD clock when block count reaches zero.
- SDMMC asserts Boot Termination interrupt when FIFO gets empty once all bytes of data are written into system memory.
- If User Program wants to read more data, program the block count again. Then SDMMC resumes the SD clock and repeat step (*).
- If User Program is done with boot code read, set SDHOST_CTRL1.BOOTEN to “0”.
- SDMMC pulls the CMD line to High and finishes the process.

39.5.8.6 Voltage Switching Sequence

The voltage switching sequence is described below:

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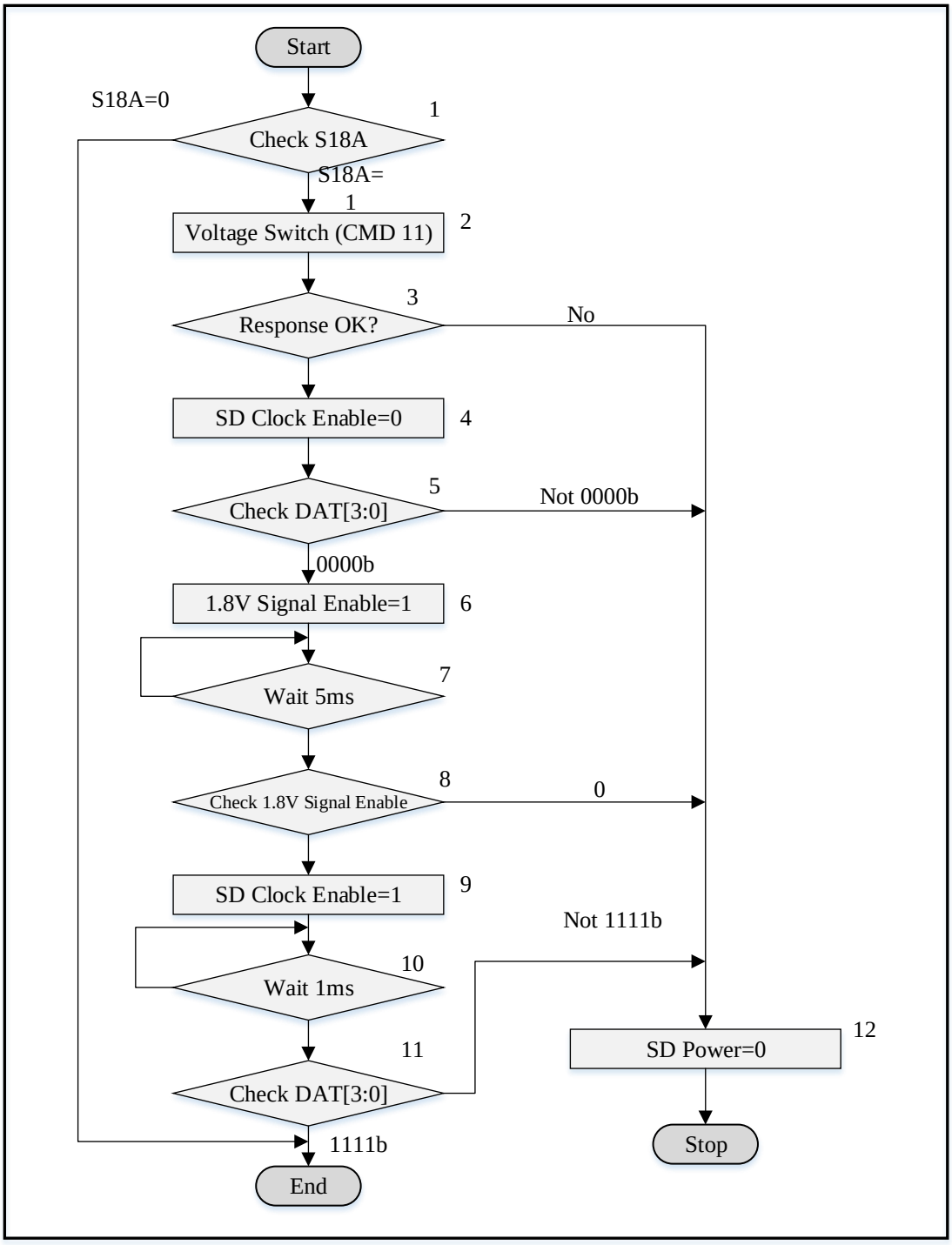
Figure 39-15 Voltage Switching Sequence



If S18A of CMD5 or S18A of ACMD41 is set to 1, signal voltage switch is performed according to the following steps. Otherwise, exists from this procedure.

Table 39-10 Voltage Switching Sequence

Step	Description

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1	Issue CMD11
2	Check response and if an error is detected, go to step (12)
3	Stop providing SD clock to the card.
4	Check DAT[3:0] level. If the level is 0000b, the card is ready to start voltage switch sequence. Otherwise, go to (12) to quit the sequence.
5	Set SDHOST_CTRLSTS.V18SE
6	Wait 5ms. 1.8V voltage regulator shall be stable within this period.
7	If SDHOST_CTRLSTS.V18SE is cleared by SDMMC, go to step (12).
8	Provide SD Clock to the card again
9	Wait 1ms.
10	Check DAT[3:0] level. If the level is 1111b, switch to 1.8V signal level is completed successfully. Otherwise, go to (12).
11	If an error occurs during voltage switch procedure, go to step 12
12	Stop providing the power to the card.

39.5.8.7 Retuning Procedure

The retuning procedure is described as below:

39.5.8.7.1 Sampling Clock Tuning

The SD bus can be operating in high clock frequency mode and then the data window from the card on CMD and DAT[3:0] lines gets smaller. The position of the data window will vary depending on the card and host system implementation. Therefore, SDMMC shall support a tuning circuit when SDR104 or SDR50 (if SDHOST_CAP1STS.UTFSDR50 is set to 1) by executing the tuning procedure and adjusting the sampling clock. Execute Tuning (ETUN) and Sampling Clock Select (SCS) bits in the SD Host Control Status register (SDHOST_CTRLSTS) are used to control the tuning circuit.

39.5.8.7.2 Tuning Modes

The expiration of a re-tuning timer prepared by User Program.
(1) Re-Tuning Mode 1 (this mode is only supported by SDMMC)
SDMMC does not have any internal logic to detect when the re-tuning needs to be performed. In this case, User Program should maintain all re-tuning timings by using a Re-Tuning Timer. To enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4MB.

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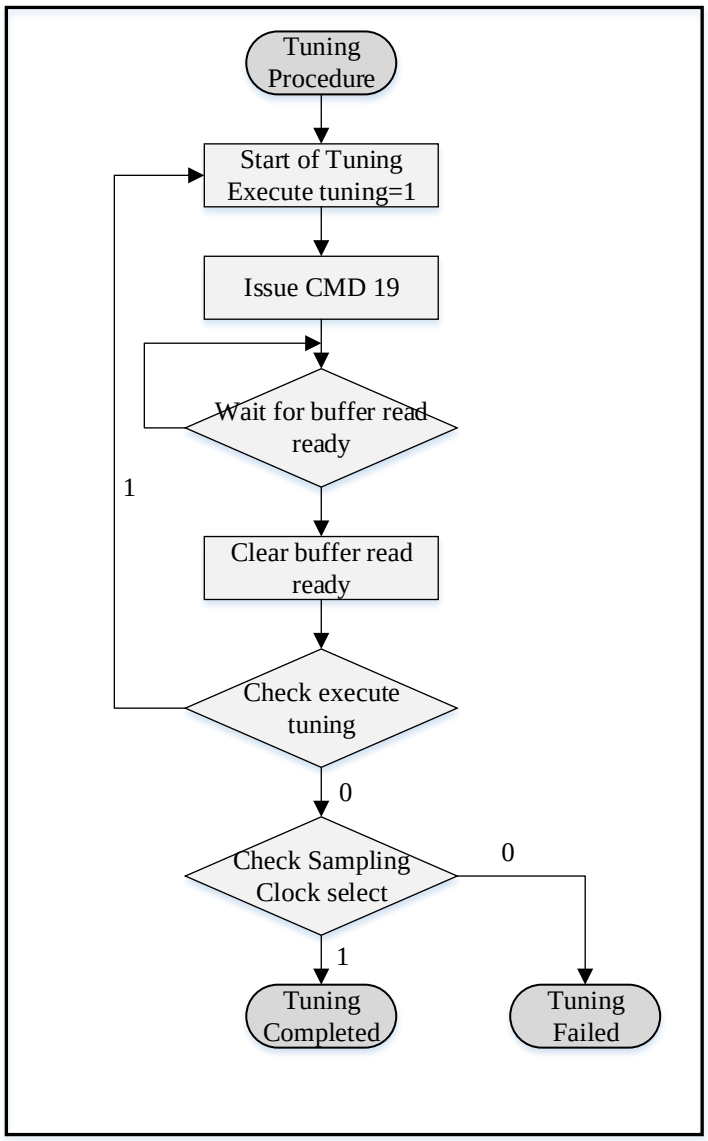
39.5.8.7.3 Clock Tuning Procedure

Figure 39-16 Clock Tuning Process



The above figure defines sampling clock tuning procedure supported by SDMMC. In default, for lower frequency operation, fixed sampling clock is used to receive signals on CMD and DAT[3:0]. Before using SDR104, sampling clock tuning is required. Start of sampling clock tuning is requested by setting Execute Tuning to 1 and Sampling Clock Select to 0.

User Program issue CMD19 repeatedly until SDMMC resets Execute Tuning to 0. SDMMC resets Execute Tuning to 0 when tuning is completed or tuning is not completed within 40 times. User Program can abort this loop by 40 times CMD19 issue or 150ms time-out.

If tuning is completed successfully, SDMMC set Sampling Clock Select to 1 and this means it starts to use tuned sampling clock. If tuning is failed, SDMMC keeps Sampling Clock Select to 0. By writing Sampling Clock Select to 0, sampling clock is switched from tuned sampling clock to fixed sampling clock. Re-tuning time would be smaller than the first tuning time. CMD19 response errors are not indicated while tuning is performed.

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The clock tuning tap delay values are selected using Variable sampling point detection. Fixed tap delay value is used for fixed tuning clock method.

39.5.9 Timing Diagram

Various timing diagrams are listed below

Figure 39-17 SD/SDIO Write Interrupt Cycle

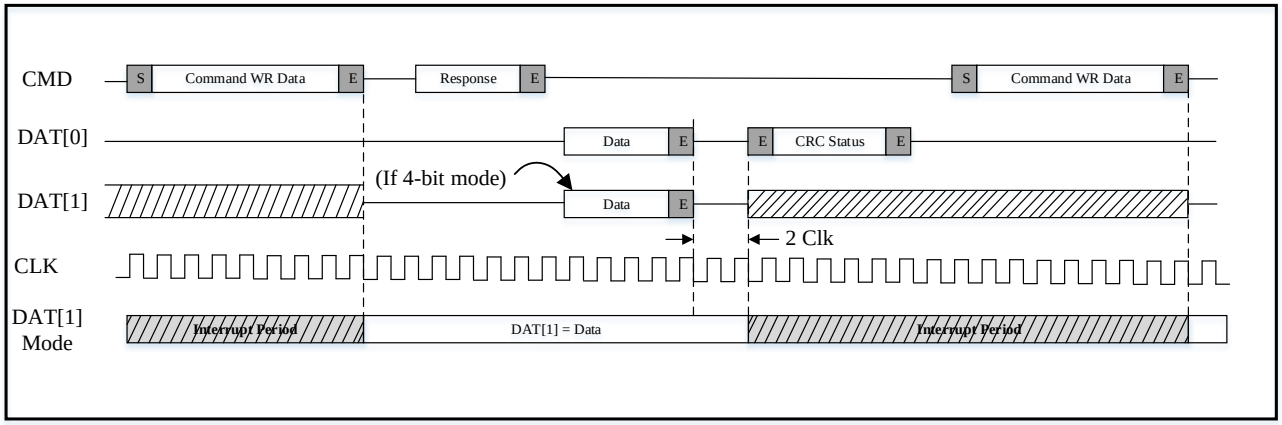

Figure 39-18 SD/SDIO Read Interrupt Cycle

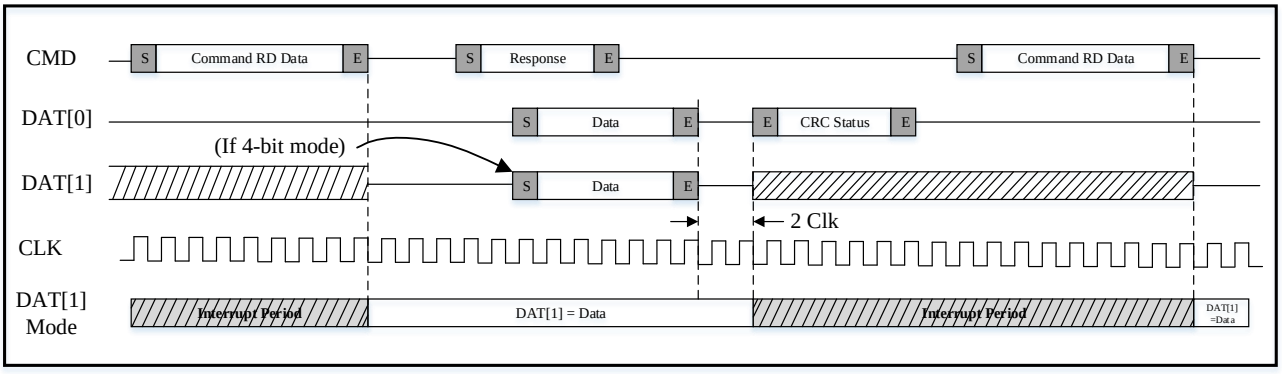

Figure 39-19 SD/SDIO suspend/resume timing

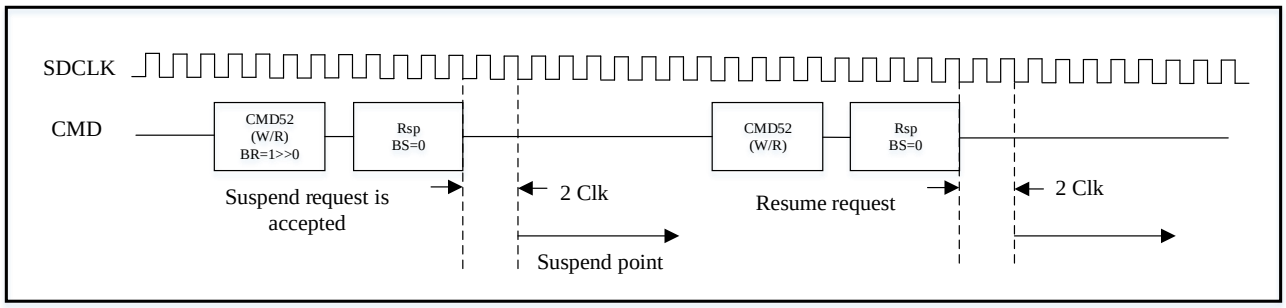

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Figure 39-20 Boot Operation Timing with Termination Between Consecutive Data Blocks

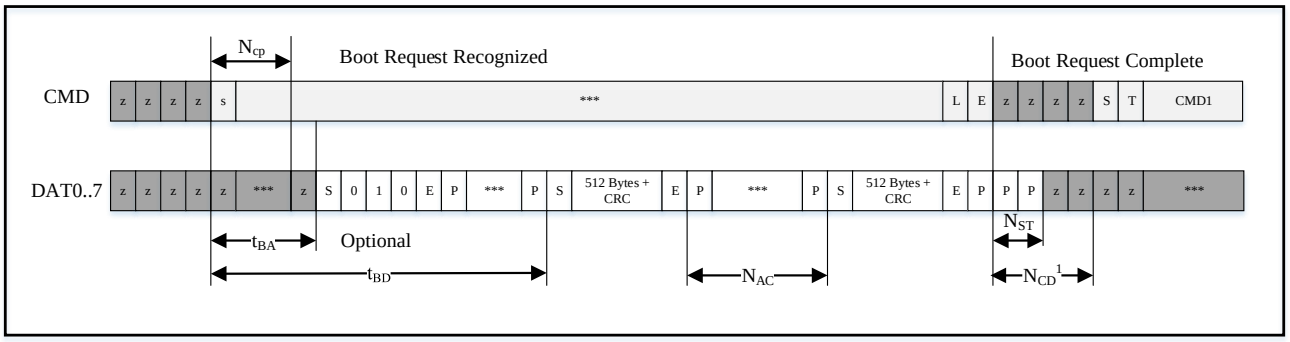


Figure 39-21 Boot Operation Timing with Termination During Transfer

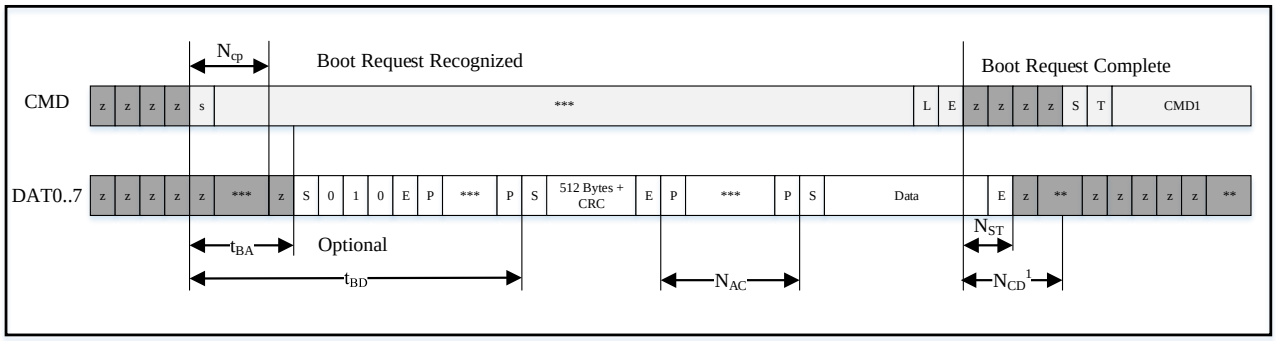
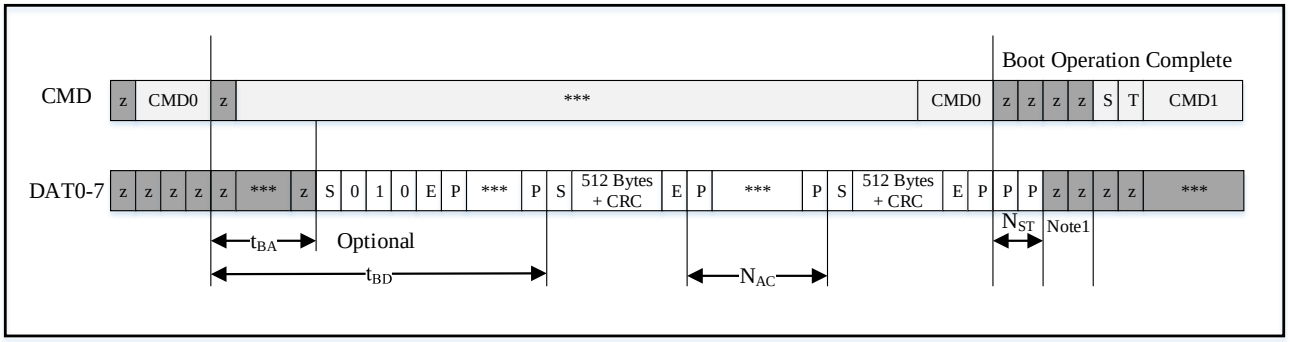


Figure 39-22 Alternative boot operation, termination between consecutive data blocks



Note 1: CMD0 with argument 0xFFFFF_FFFA

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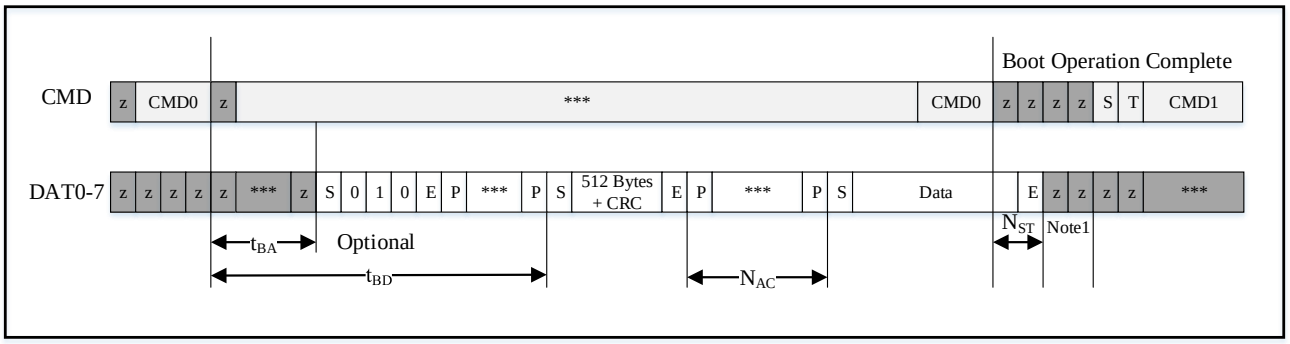
Figure 39-23 Alternative boot operation, termination during transfer



Note 1: CMD0 with argument 0xFFFFF_FFFA

Figure 39-24 Data Packet Format in DDR50 mode – Usual Data

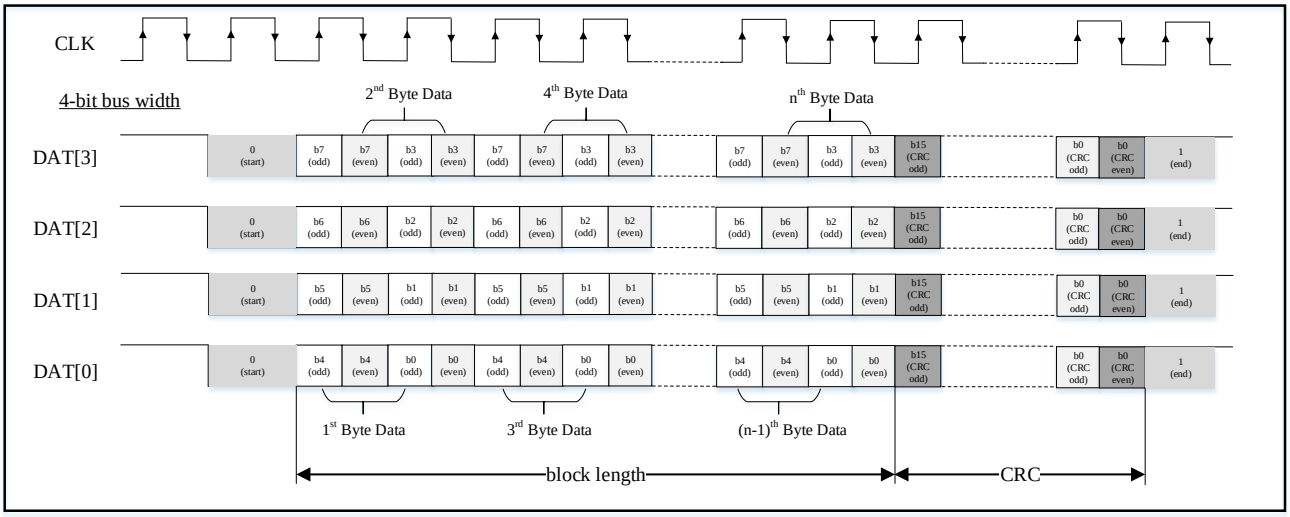


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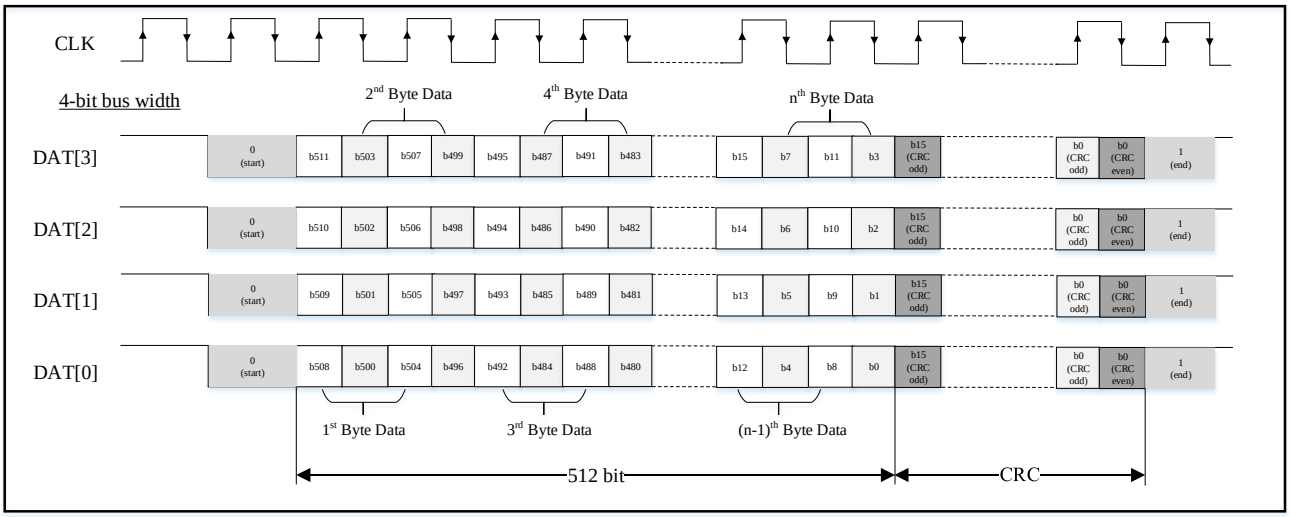
Figure 39-25 Data Packet Format in DDR50 mode – Wide Width Data



39.6 SDMMC Wrapper Registers

SDMMC1 base address：0x51107000

SDMMC2 base address：0x4004A000

39.6.1 SDMMC Configuration 1 Register (SDMMC_CFG1)

Address offset: 0x00

Reset value: 0x0034 00C1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								MBL[1:0]		BCLKF[7:2]					
								rw		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCLKF[1:0]		TCLKU	Reserved							TCNT[5:0]					WSGM
rw		rw								rw					rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:22	MBL[1:0]	Maximum Block Length supported by the Core/Device 00: 512 byte 01: 1024 byte 10: 2048 byte 11: Reserved
21:14	BCLKF[7:0]	Base Clock Frequency for SD Clock.

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Bit field	Name	Description
		This is the frequency of the xin_clk 8-bit Base Clock Frequency, Unit values are 1 MHz. The supported clock range is 10 MHz to 104 MHz. 0x69 - 0xFF: reserved, configuration not allowed 0x68: 104MHz ... 0x0A: 10 MHz 0x09 - 0x00: Reserved, configuration is not allowed. *Note 1: This value is the actual value of xin_clk given to the SDMMC after the RCC frequency division* *Note 2: If the real frequency is 16.5 MHz, the lager value shall be set 0x11 (17 MHz) because HD use this value to calculate the clock divider value (SDHOST_CTRL2.SDCLKSEL[9:0]) and it shall not exceed upper limit of the SD Clock frequency.*
13	TCLKU	Timeout Clock Unit Suggested Value is 0 (KHz) This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0: KHz 1: MHz
12:7	Reserved	Reserved, the reset value must be maintained.
6:1	TCNT[5:0]	Tuning Count Configures the number of delay taps that are supported for tuning the rxclk_in. The Tuning State Machine selects appropriate number of delay taps during Tuning Procedure within this configured number. Clock is used for tuning: rxclk_in 0x00: no tap is used 0x01: maximum 1 tap is used ... 0x20: maximum 32 taps are used 0x21 - 0x3F: Reserved, configuration not allowed.
0	WSGM	Wakeup Signal Generation Mode. This configuration is to determine how the wakeup event is generated. Wakeup event is the interrupt when card insertion or removal. 0: wakeup event is synchronized with controller clock (xin_clk). Xin_clk need to be supplied. System clock (ahb_clock) can be shut off. 1: wakeup event are asynchronous with xin_clk and can be generated without any clock (in standby mode).

39.6.2 SDMMC Configuration 2 Register (SDMMC_CFG2)

Address offset: 0x04

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Reset value: 0x0003 F2EE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												SPIBMOD	SPIMOD	Reserved	
												rw	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DDR50	SDR104	SDR50	STYP[1:0]		ASYNC INT	Reserved			VS33	SRS	SDMA	HS	ADMA2	EMBUS
	rw	rw	rw	rw		rw				rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19	SPIBMOD	SPI Block Mode 0: Not supported 1: Supported
18	SPIMOD	SPI Mode 0: Not supported 1: Supported
17:15	Reserved	Reserved, the reset value must be maintained.
14	DDR50	DDR50 Support 0: DDR50 is not supported 1: DDR50 is supported
13	SDR104	SDR104 Support 0: SDR104 is not supported 1: SDR104 is supported Note: SDR104 requires tuning.
12	SDR50	SDR50 Support 0: SDR50 is not supported 1: SDR50 is supported Note: If SDR104 is supported, this bit shall be set to 1. Bit UTFSDR50 indicates whether SDR50 requires tuning or not.
11:10	STYP[1:0]	Slot Type The Standard HD controls only a removable card or one embedded device is connected to a SD bus slot. 00: Removable card slot (SD/SDIO/MMC) 01: Embedded slot for one Device (eMMC) 10: Reserved 11: Reserved
9	ASYNCINT	Asynchronous Interrupt Refer to SDIO Specification Version 3.00 about asynchronous interrupt. 0: Asynchronous interrupt is not supported 1: Asynchronous interrupt is supported

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Bit field	Name	Description
8:6	Reserved	Reserved, the reset value must be maintained.
5	VS33	3.3V Support 0: 3.3V is not supported 1: 3.3V is supported Note: Must be configured as 1
4	SRS	Suspend/Resume Support This bit indicates whether the HC supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend/Resume commands. 0: Suspend/Resume is not supported 1: Suspend/Resume is supported
3	SDMA	SDMA Support This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. 0: SDMA is not supported 1: SDMA is supported.
2	HS	High Speed Support This bit indicates whether the HC and MCU support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz (for SD)/ 20 MHz to 52 MHz (for MMC). 0: High Speed is not supported 1: High Speed is supported
1	ADMA2	ADMA2 Mode 0: ADMA2 is not supported 1: ADMA2 is supported
0	EMBUS	8-bit Support for Embedded Device This bit indicates whether the HC is capable of using 8-bit bus width mode. 0: Extended Media Bus is not supported 1: Extended Media Bus is not supported

39.6.3 SDMMC Configuration 3 Register (SDMMC_CFG3)

Address offset: 0x08

Reset value: 0x0000 0013

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											UTF SDR50	Reserved			

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rw

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	UTFSDR50	Use Tuning for SDR50 This bit should be set if the application wants tuning be used for SDR50 mode. The HC operates with or without tuning for SDR50 mode as long as the clock can be manually tuned using tap delay. 0: SDR50 does not require tuning 1: SDR50 requires tuning
3:0	Reserved	Reserved, the reset value must be maintained.

39.6.4 SDMMC Preset Values 0 Control Register (SDMMC_PV0CTRL)

Address offset: 0x0C

Reset value: 0x0000 8000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									CLKFS_DS[9:3]						
									rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKFS_DS[2:0]			Reserved			CLKFS_INIT[9:0]									
rw						rw									

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:13	CLKFS_DS [9:0]	SDCLK Frequency Select Value for default speed 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
12:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_INIT [9:0]	SDCLK Frequency Select Value for Initialization 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system.

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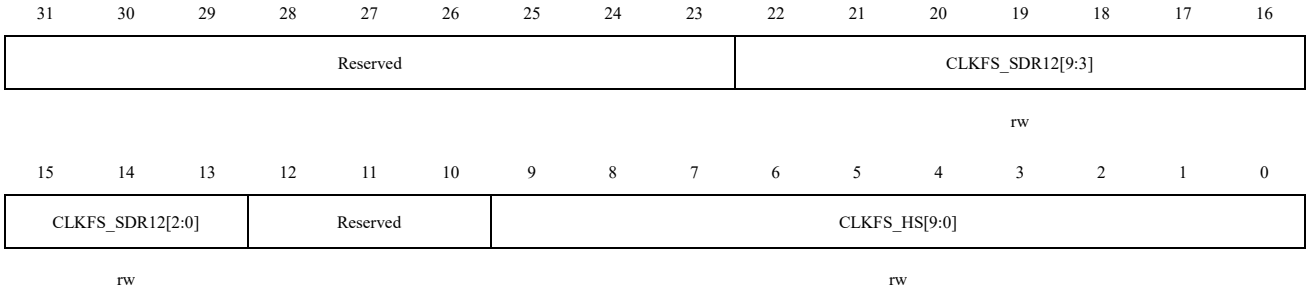
Bit field	Name	Description
		0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.6.5 SDMMC Preset Values 1 Control Register (SDMMC_PV1CTRL)

Address offset: 0x10

Reset value: 0x0000 8002



Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:13	CLKFS_SDR12 [9:0]	SDCLK Frequency Select Value for SDR12 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
12:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_HS [9:0]	SDCLK Frequency Select Value for High Speed 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock …

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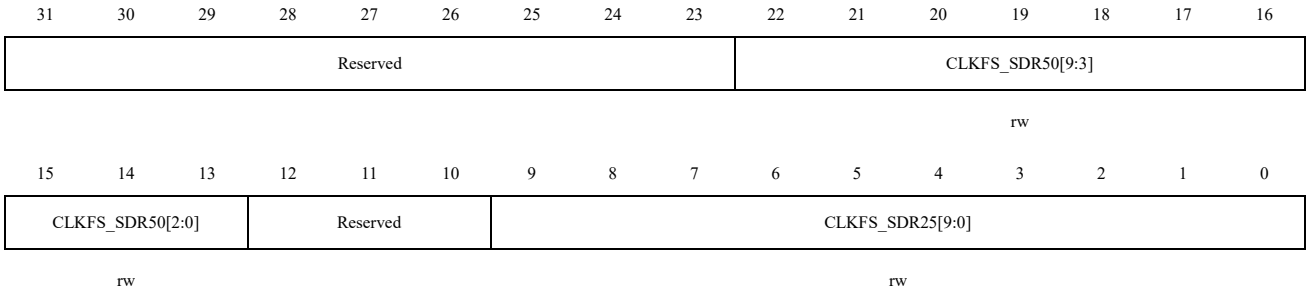
Bit field	Name	Description
		N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.6.6 SDMMC Preset Values 2 Control Register (SDMMC_PV2CTRL)

Address offset: 0x14

Reset value: 0x0000 2002



Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:13	CLKFS_SDR50 [9:0]	SDCLK Frequency Select Value for SDR50 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
12:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_SDR25 [9:0]	SDCLK Frequency Select Value for SDR25 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

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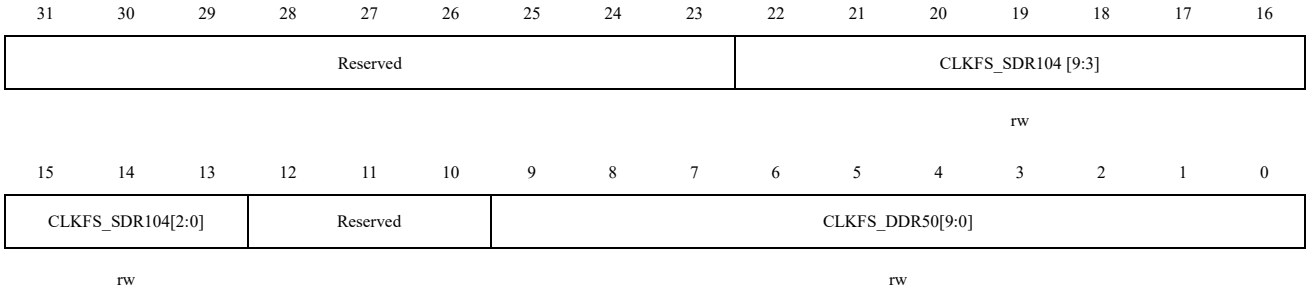
39.6.7 SDMMC Preset Values 3 Control Register (SDMMC_PV3CTRL)

Address offset: 0x18

Reset value: 0x0000 0002



Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:13	CLKFS_SDR104[9:0]	SDCLK Frequency Select Value for SDR104 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
12:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_DDR50[9:0]	SDCLK Frequency Select Value for DDR50 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.6.8 SDMMC TX and RX Delay Control Register (SDMMC_DLYCTRL)

Address offset: 0x20

Reset value: 0x0000 0000

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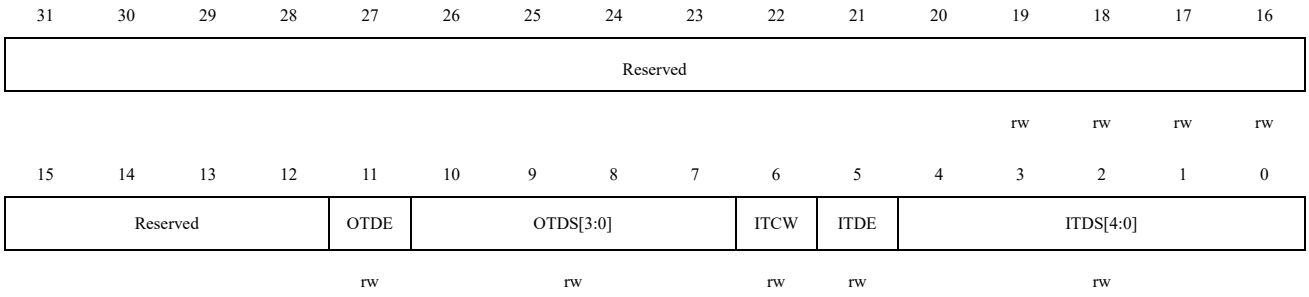

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	OTDE	Output Tap Delay Enable. This is used for the manual control of the txclk tap delay 0: Disable 1: Enable
10:7	OTDS[3:0]	Output Tap Delay Select. This is used for the manual control of the txclk tap delay, for flopping the final stage flops for maintaining hold requirements on eMMC interface. Tap Delay clk: txclk 0x00: use 1 delay tap ... 0x0F: use 16 delay taps
6	ITCW	Input Tap Change Window. After this bit set to 0, ITDS[4:0] may not be changed. This is used to gate of the rxclk to avoid clock glitches while the tap is changing 0: rxclk is not gated 1: rxclk is gated
5	ITDE	Input Tap Delay Enable. This is used for the manual control of the rxclk tap delay in non SDR104 mode. 0: Disable 1: Enable
4:0	ITDS[4:0]	Input Tap Delay Select. This is used for the manual control of the rxclk tap delay in non SDR104 mode. Rxclk is used for the tap delay clock. 0x00: use 1 delay tap ... 0x1F: use 32 delay taps

39.7 SDHOST Registers

SDHOST1 base address：0x51110000

SDHOST2 base address：0x40050000

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39.7.1 SDHOST SDMA System Address / Argument 2 Register (SDHOST_DSADD)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADD[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD[15:0]															
rw															

Bit field	Name	Description
31:0	ADD[31:0]	This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23 (1) SDMA System Address This register contains the system memory address for a SDMA transfer. When the HC stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The HD shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at every boundary specified by SDHOST_BLKCFG.HDBS[2:0] bits. The HC generates DMA Interrupt to request the HD to update this register. The HD sets the next system address of the next data position to this register. When the most upper byte of this register ([31:24]) is written, the HC restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting SDHOST_CTRL1.CONTREQ bit, the HC shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. (2) Argument 2 This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by SDHOST_BLKCFG. CNT[15:0] bits. 65535 blocks is the maximum value in this case.

39.7.2 SDHOST Block Count and Size Configure Register (SDHOST_BLKCFG)

Address offset: 0x04

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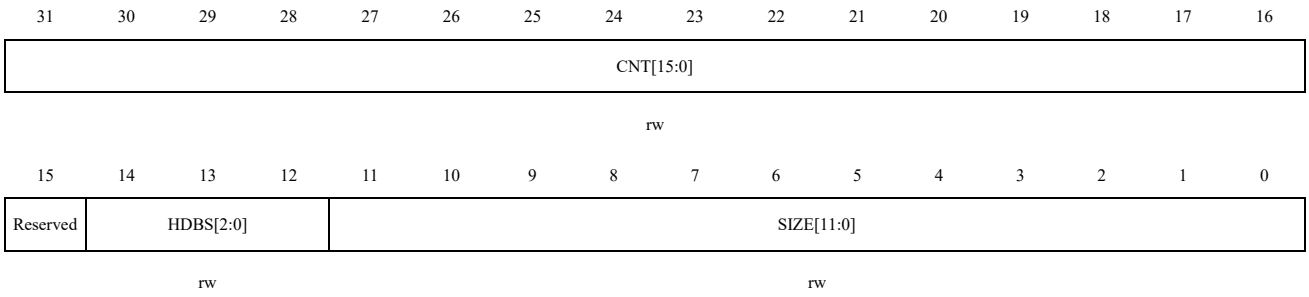
Reset value: 0x0000 000



Bit field	Name	Description
31:16	CNT[15:0]	Blocks Count for Current Transfer This register is enabled when SDHOST_TMODE.BCNTE bit is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero. It can be accessed only if no transaction is executing (i.e. after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. When saving transfer context as a result of Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously save block count. 0x0000: Stop Count 0x0001: 1 block 0x0002: 2 blocks … 0xFFFF: 65535 blocks
15	Reserved	Reserved, the reset value must be maintained.
14:12	HDBS[2:0]	Host SDMA Buffer Size To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at every boundary specified by these fields and the HC generates the DMA interrupt to request the HD to update the SDHOST_DSADD register. These bits shall support when SDMMC_CFG2.SDMA bit is set to 1 and this function is active when SDHOST_TMODE.DMAE bit is set to 1. 000: 4KB (detects A11 carry out) 001: 8KB (detects A12 carry out) 010: 16KB (detects A13 carry out) 011: 32KB (detects A14 carry out) 100: 64KB (detects A15 carry out) 101: 128KB (detects A16 carry out) 110: 256KB (detects A17 carry out) 111: 512KB (detects A18 carry out)

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Bit field	Name	Description
11:0	SIZE[11:0]	Transfer Block Size This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing (i.e. after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0x0000h - No Data Transfer 0x0001: 1 Byte 0x0002: 2 Bytes 0x0003: 3 Bytes 0x0004: 4 Bytes … 0x01FF: 511 Bytes 0x0200: 512 Bytes … 0x0800: 2048 Bytes

39.7.3 SDHOST Argument 1 Register (SDHOST_CMDARG1)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ARG1[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARG1[15:0]															
rw															

Bit field	Name	Description
31:0	ARG1[31:0]	The SD Command Argument is specified as bit39-8 of Command-Format.

39.7.4 SDHOST Transfer Mode Register (SDHOST_TMODE)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		CMDX[5:0]						TYPE[1:0]		DPRESEL	CMDXCK	CRCCK	Reserved	RTYPES[1:0]	
		rw						rw		rw	rw	rw		rw	

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										BLKSEL	DATDIR	ACMDE[1:0]		BCNTE	DMAE
										rw	rw	rw		rw	rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:24	CMDX[5:0]	Command Index This bit shall be set to the command number (CMD0-63, ACMD0-63).
23:22	TYPE[1:0]	Command Type There are three types of special commands. Suspend, Resume and Abort. These bits shall bet set to 00b for all other commands. **Suspend Command** If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting SDHOST_CTRL1.CONTREQ bit. **Resume Command** The HD re-starts the data transfer by restoring the registers in the range of 000-00Dh. The HC shall check for busy before starting write transfers. **Abort Command** If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset 00: Normal 01: Suspend 10: Resume 11: Abort
21	DPRESEL	Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. Set to 0 indicates the following: 1. Commands using only CMD line (ex. CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) 3. Resume Command 0: No Data Present 1: Data Present
20	CMDXCK	Command Index Check Enable If this bit is set to 1, the HC shall check the index field in the response to see if it has

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Bit field	Name	Description
		the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 0: Disable 1: Enable
19	CRCCK	Command CRC Check Enable If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 0: Disable 1: Enable
18	Reserved	Reserved, the reset value must be maintained.
17:16	RTYPES[1:0]	Response Type Select 00: No Response 01: Response length 136 10: Response length 48 11: Response length 48 check Busy after response
15:6	Reserved	Reserved, the reset value must be maintained.
5	BLKSEL	Multi / Single Block Select This bit enables multiple block data transfers. 0: Single Block 1: Multiple Block
4	DATDIR	Data Transfer Direction Select This bit defines the direction of data transfers. 0: Write (Host to Card) 1: Read (Card to Host)
3:2	ACMDE[1:0]	Auto CMD Enable This field determines use of auto command functions 00: Auto Command Disabled 01: Auto CMD12 Enable 10: Auto CMD23 Enable 11: Reserved There are two methods to stop Multiple-block read and write operation. (1) Auto CMD12 Enable Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 01b, the HC issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The HD shall not set this bit if the command does not require CMD12. (2) Auto CMD23 Enable When this bit field is set to 10b, the HC issues a CMD23 automatically before issuing a command specified in the Command Register The following conditions are required to use the Auto CMD23.

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Bit field	Name	Description
		• Auto CMD23 Supported • A memory card that supports CMD23 (SCR[33]=1) • If DMA is used, it shall be ADMA. • Only when CMD18 or CMD25 is issued By writing the Command register, the HC issues a CMD23 first and then issues a command specified by the Command Index in Command register 32-bit block count value for CMD23 is set to SDMA System Address / Argument 2 register
1	BCNTE	Block Count Enable This bit is used to enable SDHOST_BLKCFG.CNT[15:0] bits, which is only relevant for multiple block transfers. When this bit is 0, SDHOST_BLKCFG.CNT[15:0] is disabled, which is useful in executing an infinite transfer. 0: Disable 1: Enable
0	DMAE	DMA Enable DMA can be enabled only if SDMMC_CFG2.SDMA/SDMMC_CFG2.ADMA2 Support bit is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to SDHOST_BLKCFG.TMODE[5:0] bits. 0: Disable 1: Enable

39.7.5 SDHOST Command Response 0 Register (SDHOST_CMDRSP0)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESP[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESP[15:0]															
r															

Bit field	Name	Description
31:0	RESP0[31:0]	Command response bit 31:0

39.7.6 SDHOST Command Response 1 Register (SDHOST_CMDRSP1)

Address offset: 0x14

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESP[63:48]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESP[47:32]															
r															

Bit field	Name	Description
31:0	RESP1[31:0]	Command response bit 63:32

39.7.7 SDHOST Command Response 2 Register (SDHOST_CMDRSP2)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESP[95:80]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESP[79:64]															
r															

Bit field	Name	Description
31:0	RESP2[31:0]	Command response bit 95:64

39.7.8 SDHOST Command Response 3 Register (SDHOST_CMDRSP3)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESP[127:112]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESP[111:96]															
r															

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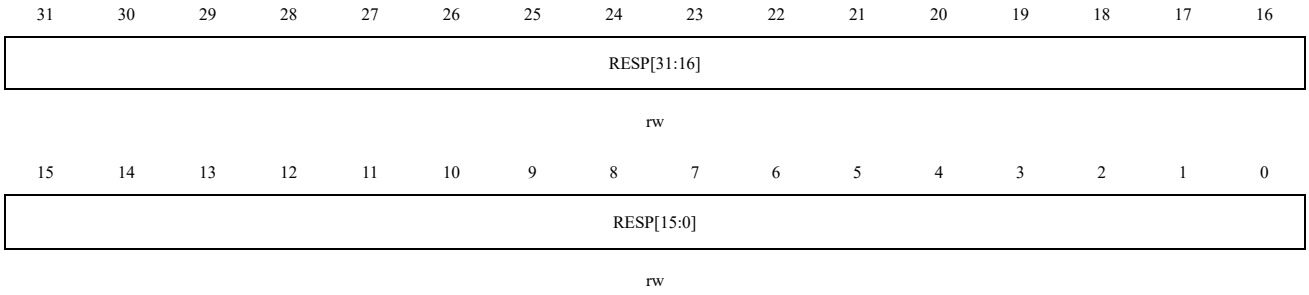
Bit field	Name	Description
31:0	RESP[31:0]	Command response bit 127:96

39.7.9 SDHOST Buffer Data Port Register (SDHOST_BUFDAT)

Address offset: 0x20

Reset value: 0x0000 0000

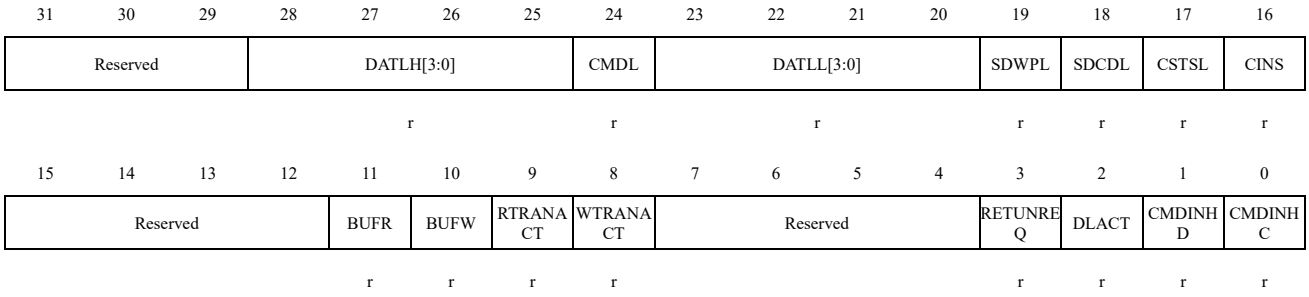


Bit field	Name	Description
31:0	DAT[31:0]	Data content This field is used to access the internal buffer.

39.7.10 SDHOST Present State Register (SDHOST_PRESTS)

Address offset: 0x24

Reset value: 0x000C 0000



Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28:25	DATLH[3:0]	DAT[7:4] Line Signal Level This status is used to check DAT line level to recover from errors, and for debugging. D28: DAT[7] D27: DAT[6] D26: DAT[5] D25: DAT[4]

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Bit field	Name	Description
24	CMDL	CMD Line Signal Level This status is used to check CMD line level to recover from errors, and for debugging.
23:20	DATLL[3:0]	DAT[3:0] Line Signal Level This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23: DAT[3] D22: DAT[2] D21: DAT[1] D20: DAT[0]
19	SDWPL	Write Protect Switch Pin Level The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. 0: Write protected (SDWP# = 0) 1: Write enabled (SDWP# = 1)
18	SDCDL	Card Detect Pin Level This bit reflects the inverse value of the SDCD# pin. 0: No Card present (SDCD# = 1) 1: Card present (SDCD# = 0)
17	CSTSL	Card State Stable This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. SDHOST_CTRL2.SWRSTALL bit shall not affect this bit. 0: Reset of Debouncing 1: No Card or Inserted
16	CINS	Card Inserted This bit indicates whether a card has been inserted. A change from 0 to 1 sets the Card Insertion Interrupt Status (SDHOST_INTSTS.CINS) to 1, while a change from 1 to 0 sets the Card Removal Interrupt Status (SDHOST_INTSTS.CRMV) to 1. TSDHOST_CTRL2.SWRSTALL bit shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear SDHOST_CTRL1.SDPWR bit and SDHOST_CTRL2.SDCLK bit. In addition, the HD should clear the HC by SDHOST_CTRL2.SWRSTALL bit. The card detect is active regardless of the SDHOST_CTRL1.SDPWR bit 0: Reset or Debouncing or No Card 1: Card Inserted
15:12	Reserved	Reserved, the reset value must be maintained.
11	BUFR	Buffer Read Enable This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt (SDHOST_INTSTS.BUFRRDY).

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Bit field	Name	Description
		0: Read Disable 1: Read Enable.
10	BUFW	Buffer Write Enable This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt (SDHOST_INTSTS.BUFWRDY). 0: Write Disable 1: Write Enable.
9	RTRANACT	Read Transfer Active This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: • After the end bit of the read command • When writing a 1 to SDHOST_CTRL1.CONTREQ bit to restart a read transfer This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the system. • When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the SDHOST_CTRL1.SABGBEQ bit set to 1. A transfer complete interrupt (SDHOST_INTSTS.TC) is generated when this bit changes to 0. 0: No valid data 1: Transferring data
8	WTRANACT	Write Transfer Active This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: • After the end bit of the write command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple) • After getting a CRC status of any block where data transmission is about to be stopped by set SDHOST_CTRL1.SABGBEQ bit. During a write transaction, a Block Gap Event interrupt(SDHOST_INTSTS.BLKGAPE) is generated when this bit is changed to 0, as a result of the SDHOST_CTRL1.SABGBEQ bit being set. This status is useful for the HD in determining when to issue commands during write busy. 0: No valid data 1: transferring data
7:4	Reserved	Reserved, the reset value must be maintained.
3	RETUNREQ	Re-Tuning Request Re-Tuning Request HC may request HD to execute re-tuning sequence by setting this

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Bit field	Name	Description
		bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting SDHOST_CTRLSTS.ETUN bit. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to SDHOST_INTSTS registers for more detail. This bit isn't set to 1 if SDHOST_CTRLSTS.SCS bit is set to 0 (using fixed sampling clock). 0: Fixed or well tuned sampling clock 1: Sampling clock needs re-tuning
2	DLACT	DAT Line Active This bit indicates whether one of the DAT line on SD bus is in use. 0: DAT line inactive 1: DAT line active
1	CMDINHD	Command Inhibit (DAT) This status bit is generated if either the DLACT bit or the RTRANACT bit is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt (SHOST_INTSTS.TC) in the SHOST_INTSTS register. Note: The SD HD can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. 0: Can issue command which uses the DAT line 1: cannot issue command which uses the DAT line
0	CMDINHC	Command Inhibit (CMD) If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after SDHOST_TMODE.CMDX[5:0] bit is written. This bit is cleared when the command response is received. Even if the CMDINHD bit is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt (SHOST_INTSTS.CMDC) in the SDHOST_INTSTS register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued by Auto CMD12 Error, this bit shall remain 1 and the SHOST_INTSTS.CMDC bit is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, HC shall manage to issue two commands: CMD12 and a command set by Command register.

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39.7.11 SDHOST Control 1 Register (SDHOST_CTRL1)

Address offset: 0x28

Reset value: 0x0080 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					RMVWKUP	INSTWKUP	INTWKUP	BOOTACKC	BOOTINALT	BOOTEN	SPIMODE	INTATBG	RWAITCTRL	CONTREQ	SABGREQ
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			HWRST	SDBVSEL[2:0]			SDPWR	CDSD	CDTL	EDTWIDTH	DMASEL[1:0]		HSEN	DTWIDTH	LEDCTRL
			rw	rw			rw	rw	rw	rw	rw		rw	rw	rw

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	RMVWKUP	Wakeup Event Enable On SD Card Removal This bit enables wakeup event via SDHOST_INTSTS.CRMV assertion. 0: Disable 1: Enable
25	INSTWKUP	Wakeup Event Enable On SD Card Insertion This bit enables wakeup event via SDHOST_INTSTS.CINS bit assertion. 0: Disable 1: Enable
24	INTWKUP	Wakeup Event Enable On Card Interrupt This bit enables wakeup event via SDHOST_INTSTS.CINT bit assertion. 0: Disable 1: Enable
23	BOOTACKC	Boot Ack Check To check for the boot acknowledge in boot operation. 0: Will not wait for boot ack from eMMC card 1: wait for boot ack from eMMC card
22	BOOTINALT	To start boot code access in alternative mode. 0: To stop alternate boot mode access 1: To start alternate boot mode access
21	BOOTEN	To start boot code access 0: To stop boot code access 1: To start boot code access
20	SPIMODE	SPI mode enable 0: SD mode 1: SPI mode
19	INTATBG	Interrupt At Block Gap

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Bit field	Name	Description
		This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.
18	RWAITCTRL	Read Wait Control The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported 0: Disable Read Wait Control 1: Enable Read Wait Control
17	CONTREQ	Continue Request This bit is used to restart a transaction which was stopped using the SABGREQ bit. To cancel stop at the block gap, set SABGREQ bit to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts. Therefore, it is not necessary for HD to set this bit to 0. If SABGREQ bit is set to 1, any write to this bit is ignored. 0: Ignored 1: Restart
16	SABGREQ	Stop At Block Gap Request This bit is used to stop executing a transaction at the next block gap for non- DMA, SDMA and ADMA transfers. Until theSDHOST_INTSTS.TC is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the SABGREQ and CONTREQ shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honor Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore, the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set RWAITCTRL bit to 1. In case of write transfers in which the HD writes data to the SDHOST_BUFDAT register, the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to SDHOST_BUFDAT register. This bit affects RTRANACT, WTRANACT, DLACT and CMDINHD bits in the SDHOST_PRESTS register. 0: Transfer 1: Stop

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Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained.
12	HWRST	Hardware reset Hardware reset signal is generated for eMMC card when this bit is set 0: De-assert the hardware reset pin 1: Drives the hardware reset pin as ZERO (Active LOW to eMMC card)
11:9	SDBVSEL[2:0]	SD Bus Voltage Select. 111b: 3.3V, must be configured as 3.3V Others: reserve
8	SDPWR	SD Bus Power Before setting this bit, the HD shall set SDBVSEL[2:0]. If the HC detects the No Card State, this bit shall be cleared. 0: Power off 1: Power on
7	CDSD	Card detect signal detection This bit selects source for card detection. 0: SDCD# is selected (for normal use) 1: The card detect test level is selected
6	CDTL	Card Detect Test Level This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the SDHOST_IE bit is set. 0: No Card 1: Card Inserted
5	EDTWIDTH	Extended Data Transfer Width This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in SDMMC_CFG.EMBUS bit. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by DTWIDTH bit. 0: Bus Width is Selected by DTWIDTH bit 1: 8-bit Bus Width
4:3	DMASEL[1:0]	DMA Select One of supported DMA modes can be selected. The HD shall check support of DMA modes by referring the SDMMC_CFG2 register. 00: SDMA is selected 01: Reserved 10: 32-bit address ADMA2 is selected 11: Reserved
2	HSEN	High Speed Enable This bit is optional. Before setting this bit, the HD shall check the SDMMC_CFG.HS in the capabilities register. If this bit is set to 0 (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/20 MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52 MHz for MMC)/208 MHz (for SD3.0).

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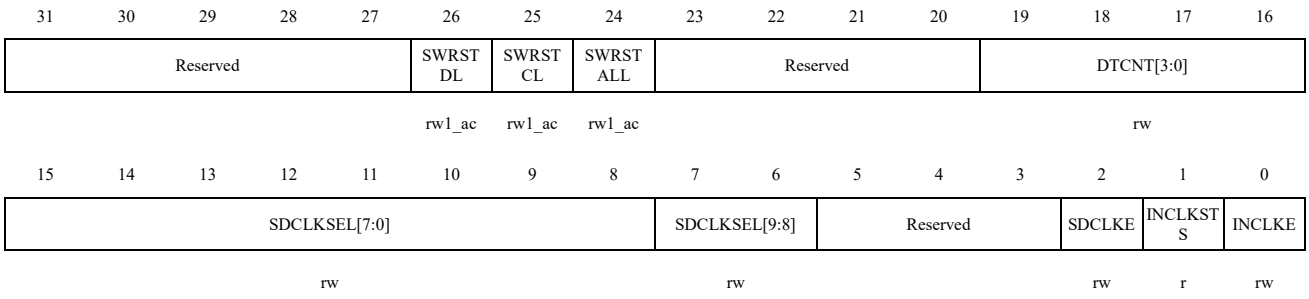
Bit field	Name	Description
		If SDHOST_CTRLSTS.PREVE bit is set to 1, HD needs to reset SDHOST_CTRL2.SDCLKE before changing this field to avoid generating clock glitches. After setting this field, the HD sets SDHOST_CTRL2.SDCLKE again 0: Normal Speed Mode 1: High Speed Mode
1	DTWIDTH	Data Transfer Width This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 0: 1 bit mode 1: 4 bit mode
0	LEDCTRL	LED Control This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 0: LED off 1: LED on

39.7.12 SDHOST Control 2 Register (SDHOST_CTRL2)

Address offset: 0x2C

Reset value: 0x0000 0000



Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	SWRSTDL	Software Reset for DAT Line Only part of data circuit is reset. The following registers and bits are cleared by this bit: **SDHOST_BUFDAT Register:** Buffer is cleared and Initialized. **SDHOST_PRESTS register:** BUFR/ BUFW/ RTRANACT/ WTRANACT/ DLACT/ CMDINHD bits **SDHOST_CTRL1 register:** CONTREQ / SABGREQ bits **SDHOST_INTSTS register:**

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Email: sales@nsing.com.sg

Bit field	Name	Description
		BUFRRDY / BUFWRDY/ BLKGAPE/ TC bits 0: Work 1: Reset
25	SWRSTCL	Software Reset for CMD Line Only part of command circuit is reset. The following registers and bits are cleared by this bit: **SDHOST_PRESTS register:** CMDINHC bit **SDHOST_INTSTS register:** CMDC bit 1: Reset 0: Work
24	SWRSTALL	Software Reset for All This reset affects the entire SDHOST registers except for the card detection circuitry. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. 1: Reset 0: Work
23:20	Reserved	Reserved, the reset value must be maintained.
19:16	DTCNT[3:0]	Data Timeout Counter Value This value determines the interval by which DAT line time-outs are detected. Refer to the SDHOST_INTSTS.DTERR bit for information on factors that dictate time-out generation. When setting this register, prevent inadvertent time-out events by clearing the SDHOST_IE.DTEE bit. TMCLK: SDMMC_CFG1.TCLKU bit determine 1 KHz or 1MHz. 1111: Reserved 1110: TMCLK * 2^27 … 0001: TMCLK * 2^14 0000: TMCLK * 2^13
15:8	SDCLKSEL [7:0]	SDCLK Frequency Select This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather these bits holds the divisor of SDMMC_CFG1.BCLKF[7:0]. Only the following settings are allowed. The length of divider is extended to 10 bits and all divider values shall be supported. This bit depends on the setting of SDHOST_CTRLSTS.PREVE bit. If the SDHOST_CTRLSTS.PREVE = 0, this bit is set by HD.

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Bit field	Name	Description
		If the SDHOST_CTRLSTS.PREVE = 1, this bit is automatically set to a value specified in one of SDMMC_PVxCTRL registers. 0x000: Base clock (10 MHz – 104MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
7:6	SDCLKSEL [9:8]	SDCLK Frequency Select Used in conjunction with SDCLKSEL [7:0]
5:3	Reserved	Reserved, the reset value must be maintained.
2	SDCLKE	SD Clock Enable The HC shall stop SDCLK when writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until SDCLK is stopped. If the HC detects the No Card state, this bit shall be cleared. 0: Disable 1: Enable
1	INCLKSTS	Internal Clock Stable This bit is set to 1 when SD clock is stable after writing to INCLKE bit to 1. The SD HD shall wait to set SDCLKE bit until this bit is set to 1. *Note: This is useful when using PLL for a clock oscillator that requires setup time.* 0: Not Ready 1: Ready
0	INCLKE	Internal Clock Enable This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set INCLKSTS bit in this register to 1. This bit shall not affect card detection. 0: Stop 1: Oscillate

39.7.13 SDHOST Interrupt Status Register (SDHOST_INTSTS)

Address offset: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			TRGR ERR	Reserved		ADMA ERR	ACMD ERR	Reserved	DEND ERR	DCRC ERR	DTERR	CINX ERR	CENDB ERR	CCRC ERR	CTERR
			rc_w1			rc_w1	rc_w1		rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALLERR	BOOTTER	BOOTACKR	RETUNE	Reserved			CINT	CRMV	CINS	BUFRRDY	BUFWRDY	DMAINT	BLKGAPE	TC	CMDC
r	rc_w1	rc_w1	r				r	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	TRGRERR	Target Response error Occurs when detecting ERROR in DMA transaction 0: no error 1: error
27:26	Reserved	Reserved, the reset value must be maintained.
25	ADMAERR	ADMA Error This bit is set when the HC detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 0: No error 1: Error
24	ACMDERR	Auto CMD Error Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. 0: No Error 1: Error
23	Reserved	Reserved, the reset value must be maintained.
22	DENDERR	Data End Bit Error Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0: No Error 1: Error
21	DCRCERR	Data CRC Error Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than “010”. 0: No Error 1: Error
20	DTERR	Data Timeout Error Occurs when detecting one of following timeout conditions. 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout

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Bit field	Name	Description
		0: No Error 1: Timeout
19	CINXERR	Command Index Error Occurs if a Command Index error occurs in the Command Response. 0: No Error 1: Error
18	CENDBERR	Command End Bit Error Occurs when detecting that the end bit of a command response is 0. 0: No Error 1: End Bit Error Generated
17	CCRCERR	Command CRC Error Command CRC Error is generated in two cases. 1. If a response is returned and the Command Time-out Error is set to 0, this bit is set to 1 when detecting a CRT error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 0: No Error 1: CRC Error Generated
16	CTERR	Command Timeout Error Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case Command CRC Error shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 0: No Error 1: Timeout
15	ALLERR	Error Interrupt Any error status bit (bit 28, bit 25 to bit 16) is set, then this bit is set. Therefore the HD can test for an error by checking this bit first. 0: No Error. 1: Error.
14	BOOTTER	Boot terminate Interrupt This status is set if the boot operation get terminated 0: Boot operation is not terminated. 1: Boot operation is terminated
13	BOOTACKR	Boot ack rcv This status is set if the boot acknowledge is received from device. 0: Boot ack is not received. 1: Boot ack is received.
12	RETUNE	Re-Tuning Event

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Bit field	Name	Description
		This status is set if SDHOST_PRESTS.RETUNREQ bit changes from 0 to 1. HC requests HD to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. 0: Re-Tuning is not required 1: Re-Tuning should be performed
11:9	Reserved	Reserved, the reset value must be maintained.
8	CINT	Card Interrupt Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. when this status has been set and the HD needs to start this interrupt service, SDHOST_IE.CINTE bit shall be set to 0 in order to clear the card interrupt statuses latched in the HC and stop driving the Host System. After completion of the card interrupt service (the reset factor in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of shared bus, interrupt pins are used to detect interrupts. 0: No Card Interrupt 1: Generate Card Interrupt
7	CRMV	Card Removal This status is set if SDHOST_PRESTS.CINS bit changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of SDHOST_PRESTS.CINS bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0: Card State Stable or Debouncing 1: Card Removed
6	CINS	Card Insertion This status is set if the Card Inserted in the Present State register changes from 0 to 1. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0: Card State Stable or Debouncing 1: Card Inserted
5	BUFRRDY	Buffer Read Ready This status is set if the SDHOST_PRESTS.BUFR bit changes from 0 to 1. BUFRRDY is set to 1 for every CMD19 execution in tuning procedure. 0: Not Ready to read Buffer. 1: Ready to read Buffer.

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Email: sales@nsing.com.sg

Bit field	Name	Description
4	BUFWRDY	Buffer Write Ready This status is set if the SDHOST_PRESTS.BUFW bit changes from 0 to 1. 0: Not Ready to Write Buffer. 1: Ready to Write Buffer.
3	DMAINT	DMA Interrupt This status is set If the HC detects the boundary set by SDHOST_BLKCFG.HDBS[2:0] . 0: No DMA Interrupt 1: DMA Interrupt is Generated
2	BLKGAPE	Block Gap Event If the SDHOST_CTRL1.SABGREQ bit is set, this bit is set. Read Transaction: This bit is set at the falling edge of the SDHOST_PRESTS.DLACT bit Status (When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function). Write Transaction: This bit is set at the falling edge of SDHOST_PRESTS.WTRANACT bit Status (After getting CRC status at SD Bus timing). 0: No Block Gap Event 1: Transaction stopped at Block Gap
1	TC	Transfer Complete This bit is set when a read / write transaction is completed. Read Transaction: This bit is set at the falling edge of SDHOST_PRESTS.RTRANACT bit Status. There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting theSDHOST_CTRL1.SABGREQ bit (After valid data has been read to the Host System). Write Transaction: This bit is set at the falling edge of the SDHOST_PRESTS.DLACT bit Status. There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting SDHOST_CTRL1.SABGREQ bit and data transfers completed. (After valid data is written to the SD card and the busy signal is released). Note: Transfer Complete has higher priority than Data Time-out Error. If both bits are set to 1, the data transfer can be considered complete Note: While performing tuning procedure (SDHOST_CTRLSTS.ETUN bit is set to 1), Transfer Complete is not set to 1 0: No Data Transfer Complete 1: Data Transfer Complete

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Email: sales@nsing.com.sg

Bit field	Name	Description
0	CMDC	Command Complete This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23) Note: Command Time-out Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. 0: No Command Complete 1: Command Complete

39.7.14 SDHOST Interrupt Status Enable Register (SDHOST_IE)

Address offset: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			TRGREE	Reserved		ADMAEE	ACMDEE	Reserved	DENDEE	DCRCEE	DTEE	CINXEE	CENDBEE	CCRCEE	CTEE
			rw			rw	rw		rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	BOOTTIE	BOOTACKRE	RTUNE	Reserved			CINTE	CRMVE	CINSE	BUFRRDYE	BUFWRDYE	DMAINTE	BLKGAPEE	TCE	CMDCE
	rw	rw	rw				rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	TRGREE	Target Response Error /Host Error Status Enable 0: Masked 1: Enabled
27:26	Reserved	Reserved, the reset value must be maintained.
25	ADMAEE	ADMA Error Status Enable 0: Masked 1: Enabled
24	ACMDEE	Auto CMD12 Error Status Enable 0: Masked 1: Enabled
23	Reserved	Reserved, the reset value must be maintained.
22	DENDEE	Data End Bit Error Status Enable 0: Masked 1: Enabled
21	DCRCEE	Data CRC Error Status Enable 0: Masked 1: Enabled
20	DTEE	Data Timeout Error Status Enable

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Bit field	Name	Description
		0: Masked 1: Enabled
19	CINXEE	Command Index Error Status Enable 0: Masked 1: Enabled
18	CENDBEE	Command End Bit Error Status Enable 0: Masked 1: Enabled
17	CCRCEE	Command CRC Error Status Enable 0: Masked 1: Enabled
16	CTEE	Command Timeout Error Status Enable 0: Masked 1: Enabled
15	Reserved	Reserved, the reset value must be maintained.
14	BOOTTIE	Boot terminate Interrupt enable 0: Masked 1: Enabled
13	BOOTACKRE	Boot ack rcv enable 0: Masked 1: Enabled
12	RTUNE	Re-Tuning Event Status Enable 0: Masked 1: Enabled
11:9	Reserved	Reserved, the reset value must be maintained.
8	CINTE	Card Interrupt Status Enable If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. 0: Masked 1: Enabled
7	CRMVE	Card Removal Status Enable 0: Masked 1: Enabled
6	CINSE	Card Insertion Status Enable 0: Masked 1: Enabled
5	BUFRRDYE	Buffer Read Ready Status Enable 0: Masked

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Bit field	Name	Description
		1: Enabled
4	BUFWRDYE	Buffer Write Ready Status Enable 0: Masked 1: Enabled
3	DMAINTE	DMA Interrupt Status Enable 0: Masked 1: Enabled
2	BLKGAPEE	Block Gap Event Status Enable 0: Masked 1: Enabled
1	TCE	Transfer Complete Status Enable 0: Masked 1: Enabled
0	CMDCE	Command Complete Status Enable 0: Masked 1: Enabled

39.7.15 SDHOST Interrupt Signal Enable Register (SDHOST_ISE)

Address offset: 0x38

Reset value: 0x0000 0000

This register is used to select which interrupt status is indicated to the host system as the interrupt. These status fields all share the same interrupt lines. Setting any of these fields to 1 enables interrupt generation. The corresponding Status register field generates an interrupt when the corresponding interrupt signal enable field is set.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			TRGRESE	Reserved		ADMAESE	ACMDESE	Reserved	DENDESE	DCRCESE	DTESE	CINXESE	CENDBESE	CCRCESE	CTESE
			rw			rw	rw		rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	BOOTTISE	BOOTACKRSE	RTUNSE	Reserved			CINTSE	CRMVSE	CINSSE	BUFRDYSE	BUFWRDYSE	DMAINTSE	BLKGAPESE	TCSE	CMDCSE
	rw	rw	rw				rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	TRGRESE	Target Response Error /Host Error Signal Enable 0: Masked 1: Enabled
27:26	Reserved	Reserved, the reset value must be maintained.
25	ADMAESE	ADMA Error Signal Enable

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Email: sales@nsing.com.sg

Bit field	Name	Description
		0: Masked 1: Enabled
24	ACMDESE	Auto CMD12 Error Signal Enable 0: Masked 1: Enabled
23	Reserved	Reserved, the reset value must be maintained.
22	DENDESE	Data End Bit Error Signal Enable 0: Masked 1: Enabled
21	DCRCESE	Data CRC Error Signal Enable 0: Masked 1: Enabled
20	DTESE	Data Timeout Error Signal Enable 0: Masked 1: Enabled
19	CINXESE	Command Index Error Signal Enable 0: Masked 1: Enabled
18	CENDBESE	Command End Bit Error Signal Enable 0: Masked 1: Enabled
17	CCRCESE	Command CRC Error Signal Enable 0: Masked 1: Enabled
16	CTESE	Command Timeout Error Signal Enable 0: Masked 1: Enabled
15	Reserved	Reserved, the reset value must be maintained.
14	BOOTTISE	Boot terminate Interrupt signal enable 0: Masked 1: Enabled
13	BOOTACKRSE	Boot ack rcv Signal Enable 0: Masked 1: Enabled
12	RTUNSE	Re-Tuning Event Signal Enable 0: Masked 1: Enabled
11:9	Reserved	Reserved, the reset value must be maintained.
8	CINTSE	Card Interrupt Signal Enable 0: Masked 1: Enabled

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Bit field	Name	Description
7	CRMVSE	Card Removal Signal Enable 0: Masked 1: Enabled
6	CINSSE	Card Insertion Signal Enable 0: Masked 1: Enabled
5	BUFRRDYSE	Buffer Read Ready Signal Enable 0: Masked 1: Enabled
4	BUFWRDYSE	Buffer Write Ready Signal Enable 0: Masked 1: Enabled
3	DMAINTSE	DMA Interrupt Signal Enable 0: Masked 1: Enabled
2	BLKGAPESE	Block Gap Event Signal Enable 0: Masked 1: Enabled
1	TCSE	Transfer Complete Signal Enable 0: Masked 1: Enabled
0	CMDCSE	Command Complete Signal Enable 0: Masked 1: Enabled

39.7.16 SDHOST Control Status Register (SDHOST_CTRLSTS)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PREVE	ASYNCIE	Reserved						SCS	ETUN	Reserved		V18SE	UHSMOD[2:0]		
rw	rw							rw	rw			rw	rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ACMD12E	Reserved		ACMDINXE	ACMDEBE	ACMDCRCE	ACMDTE	ACMD12NE
								r			r	r	r	r	r

Bit field	Name	Description
31	PREVE	Preset Value Enable As the operating SDCLK frequency and I/O driver strength depend on MCU

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Bit field	Name	Description
		implementation, it is difficult to determine these parameters in the Standard HD. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. 0 SDCLK and Driver Strength are controlled by HD 1 Automatic Selection by Preset Value is Enabled If this bit is set to 0, SDHOST_CTRL2.SDCLKSEL[9:0] are set by HD. If this bit is set to 1, SDHOST_CTRL2.SDCLKSEL[9:0] are set by HC as specified in the Preset Value registers.
30	ASYNCIE	Asynchronous Interrupt Enable This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode. If this bit is set to 1, the HD can stop the SDCLK during asynchronous interrupt period to save power. During this period, the HC continues to deliver Card Interrupt to the host when it is asserted by the Card. 0: Disabled 1: Enabled
29:24	Reserved	Reserved, the reset value must be maintained.
23	SCS	Sampling Clock Select This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. HC uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0. Change of this bit is not allowed while the HC is receiving response or a read data block. 0 Fixed clock is used to sample data 1 Tuned clock is used to sample data
22	ETUN	Execute Tuning This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0. 0: Not Tuned or Tuning Completed 1: Execute Tuning
21:20	Reserved	Reserved, the reset value must be maintained.
19	V18SE	1.8V Signaling Enable This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. HC clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. HD can set this bit to 1 when HC supports 1.8V signaling (One of support bits is set to

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Email: sales@nsing.com.sg

Bit field	Name	Description
		1: SDR50, SDR104 or DDR50 in the Capabilities register) and the card or device supports UHS-I 0: 3.3V Signaling 1: 1.8V Signaling
18:16	UHSMOD[2:0]	UHS Mode Select This field is used to select one of UHS-I modes and effective when V18SE bit is set to 1. If Preset Value Enable in the Host Control 2 register is set to 1, HC sets SDHOST_CTRL2.SDCLKSEL[9:0], SDHOST_CTRL2.CLKGSEL, SDHOST_CTRLSTS.DSS[1:0] according to Preset Value registers. In this case, one of preset value registers is selected by this field. HD needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, HD sets SD Clock Enable again. 000: SDR12 001: SDR25 010: SDR50(SD card)/SDR(eMMC card) 011: SDR104(SD card)/HS200(eMMC card) 100: DDR50(SD card)/DDR(eMMC card) 101 – 111: Reserved When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail.
15:8	Reserved	Reserved, the reset value must be maintained.
7	ACMD12E	Setting this bit to 1 means CMD is not executed due to an Auto CMD12 error (D04 - D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD12 0: No Error 1: Not Issued
6:5	Reserved	Reserved, the reset value must be maintained.
4	ACMDINXE	Auto CMD Index Error Occurs if the Command Index error occurs in response to a command. 0: No Error 1: Error
3	ACMDEBE	Auto CMD End Bit Error Occurs when detecting that the end bit of command response is 0. 0: No Error 1 :End Bit Error Generated
2	ACMDCRCE	Auto CMD CRC Error Occurs when detecting a CRC error in the command response. 0: No Error 1: CRC Error Generated
1	ACMDTE	Auto CMD Timeout Error

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Bit field	Name	Description
		Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, the other error status bits (D04 - D02) are meaningless. 0: No Error 1: Timeout
0	ACMD12NE	Auto CMD12 not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1, other error status bits (D04 - D01) are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 0: Executed 1: Not Executed

39.7.17 SDHOST Capabilities 0 Status Register (SDHOST_CAP0STS)

Address offset: 0x40

Reset value: 0x2768 D001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STYP[1:0]		ASYNC INT	Reserved				VS33	SRS	SDMA	HS	Reserved	ADMA2	EMBUS	MBL[1:0]	
r		r					r	r	r	r		r	r	r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCLKF[7:0]								TCLKU	Reserved						
r								r							

Bit field	Name	Description
31:30	STYP[1:0]	Slot Type The Standard HD controls only a removable card or one embedded device is connected to a SD bus slot. 00: Removable Card Slot 01: Embedded Slot for One Device 10: Reserved 11: Reserved
29	ASYNCINT	Asynchronous Interrupt Support Refer to SDIO Specification Version 3.00 about asynchronous interrupt. 0: Asynchronous Interrupt Not Supported 1: Asynchronous Interrupt Supported
28:25	Reserved	Reserved, the reset value must be maintained.
24	VS33	Voltage Support 3.3V

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Bit field	Name	Description
		0: 3.3 V Not Supported 1: 3.3 V Supported
23	SRS	Suspend / Resume Support This bit indicates whether the HC supports Suspend / Resume functionality. If this bit is 0, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend / Resume commands. 0: Not Supported 1: Supported
22	SDMA	SDMA Support This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. 0: SDMA Not Supported 1: SDMA Supported.
21	HS	High Speed Support This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz (for SD)/ 20MHz to 52 MHz (for MMC). 0: High Speed Not Supported 1: High Speed Supported
20	Reserved	Reserved, the reset value must be maintained.
19	ADMA2	0: ADMA2 not support 1: ADMA2 support.
18	EMBUS	Extended Media Bus Support This bit indicates whether the HC is capable of using 8-bit bus width mode. 0: Extended Media Bus Not Supported 1: Extended Media Bus Supported
17:16	MBL[1:0]	Max Block Length This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 00: 512 byte 01: 1024 byte 10: 2048 byte 11: Reserved
15:8	BCLKF[7:0]	Base Clock Frequency for SD Clock This mode is supported by the HC Version 3.00. Unit values are 1 MHz. The supported clock range is 10MHz to 255MHz. 0xFF: 255 MHz ... 0x0A: 10 MHz 0x09h - 0x00h: Reserved, configuration not allowed

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Bit field	Name	Description
		If the real frequency is 16.5 MHz, the lager value shall be set to 0x11 (17 MHz) because the HD use this value to calculate the clock divider value (Refer to SDHOST_CTRL2.SDCLKSEL[9:0] bits) and it shall not exceed upper limit of the SD Clock frequency.
7	TCLKU	Timeout Clock Unit This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0: KHz 1: MHz
6:0	Reserved	Reserved, the reset value must be maintained.

39.7.18 SDHOST Capabilities 1 Status Register (SDHOST_CAP1STS)

Address offset: 0x44

Reset value: 0x0000 2377

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						SPIBMOD	SPIMOD	Reserved							
						r	r								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		UTFSDR50	Reserved										DDR50	SDR104	SDR50
		r											r	r	r

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	SPIBMOD	SPI block mode 0: Not Supported 1: Supported
24	SPIMOD	SPI mode 0: Not Supported 1: Supported
23:14	Reserved	Reserved, the reset value must be maintained.
13	UTFSDR50	Use Tuning for SDR50 This bit should be set if the Application wants tuning be used for SDR50 Modes. The HC operates with or without tuning for SDR50 mode as long as the clock can be manually tuned using tap delay. 0: SDR50 does not require tuning 1: SDR50 requires tuning
12:3	Reserved	Reserved, the reset value must be maintained.
2	DDR50	DDR50 Support 0: DDR50 is Not Supported

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Bit field	Name	Description
		1: DDR50 is Supported
1	SDR104	SDR104 Support 0: SDR104 is Not Supported 1: SDR104 is Supported Note: SDR104 requires tuning.
0	SDR50	SDR50 Support 0: SDR50 is not Supported 1: SDR50 is Supported Note: If SDR104 is supported, this bit shall be set to 1. Bit UTFSDR50 indicates whether SDR50 requires tuning or not.

39.7.19 SDHOST Force Event Status Register (SDHOST_STSFE)

Address offset: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						ADMAE	ACMDE	Reserved	DEBE	DCRCE	DTE	CINXE	CEBE	CCRCE	CTE
						w	w		w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ACMD12E	Reserved		ACMDINXE	ACMDEBE	ACMDCRCE	ACMDTE	ACMD12NE
								w			w	w	w	w	w

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	ADMAE	Force Event for ADMA Error 0: No interrupt 1: Interrupt is generated
24	ACMDE	Force Event for Auto CMD Error 0: No interrupt 1: Interrupt is generated
23	Reserved	Reserved, the reset value must be maintained.
22	DEBE	Force Event for Data End Bit Error 0: No interrupt 1: Interrupt is generated
21	DCRCE	Force Event for Data CRC Error 0: No interrupt 1: Interrupt is generated
20	DTE	Force Event for Data Timeout Error 0: No interrupt

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Bit field	Name	Description
		1: Interrupt is generated
19	CINXE	Force Event for Command Index Error 0: No interrupt 1: Interrupt is generated
18	CEBE	Force Event for Command End Bit Error 0: No interrupt 1: Interrupt is generated
17	CCRCE	Force Event for Command CRC Error 0: No interrupt 1: Interrupt is generated
16	CTE	Force Event for Command Timeout Error 0: No interrupt 1: Interrupt is generated
15:8	Reserved	Reserved, the reset value must be maintained.
7	ACMD12E	Force Event for command not issued by Auto CMD12 Error 0: no interrupt 1: Interrupt is generated
6:5	Reserved	Reserved, the reset value must be maintained.
4	ACMDINXE	Force Event for Auto CMD Index Error 0: no interrupt 1: Interrupt is generated
3	ACMDEBE	Force Event for Auto CMD End Bit Error 0: no interrupt 1: Interrupt is generated
2	ACMDCRCE	Force Event for Auto CMD CRC Error 0: no interrupt 1: Interrupt is generated
1	ACMDTE	Force Event for Auto CMD timeout Error 0: no interrupt 1: Interrupt is generated
0	ACMD12NE	Force Event for Auto CMD12 NOT Executed 0: no interrupt 1: Interrupt is generated

39.7.20 SDHOST ADMA Error Status Register (SDHOST_ADMAESTS)

Address offset: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													ADMALME	ADMAE[1:0]	
													r	r	

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	ADMALME	ADMA Length Mismatch Error This error occurs in the following 2 cases. While SDHOST_TMODE.BCNTE being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 0: No error 1: Error
1:0	ADMAE[1:0]	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. 00: ST_STOP (Stop DMA) Points to next of the error descriptor 01: ST_FDS (Fetch Descriptor) Points to the error descriptor 10: Never set this state (Not used) 11: ST_TFR (Transfer Data) Points to the next of the error descriptor

39.7.21 SDHOST ADMA System Address 0 Register (SDHOST_ASADD0)

Address offset: 0x58

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADD[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD[15:0]															
rw															

Bit field	Name	Description
31:0	ADD[31:0]	ADMA System Address This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the HD shall set start address of the Descriptor table. The ADMA increments this register

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Bit field	Name	Description
		address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The HD shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b. 32-bit Address ADMA Register Value 32-bit System Address xxxxxxxx 0x00000000 0x00000000 xxxxxxxx 0x00000004 0x00000004 …. xxxxxxxx 0xFFFFFFFC 0xFFFFFFFC

39.7.22 SDHOST ADMA System Address 1 Register (SDHOST_ASADD1)

Address offset: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADD[63:48]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD[47:32]															
rw															

Bit field	Name	Description
31:0	ADD[63:32]	ADMA System Address This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the HD shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The HD shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b. 32-bit Address ADMA Register Value 32-bit System Address xxxxxxxx 0x00000000 0x00000000 xxxxxxxx 0x00000004 0x00000004 …. xxxxxxxx 0xFFFFFFFC 0xFFFFFFFC

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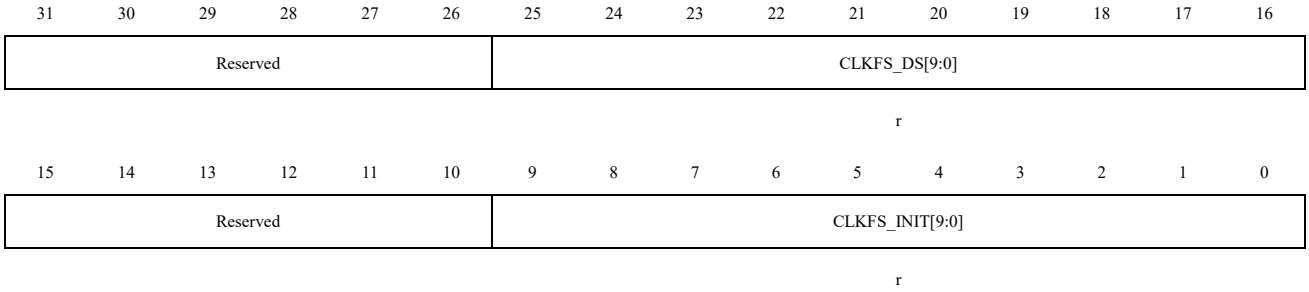
39.7.23 SDHOST Preset Values 0 Status Register (SDHOST_PV0STS)

Address offset: 0x60

Reset value: 0x0004 0000



Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	CLKFS_DS [9:0]	SDCLK Frequency Select Value for Default Speed 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_INIT [9:0]	SDCLK Frequency Select Value for Initialization 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz -104MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.7.24 SDHOST Preset Values 1 Status Register (SDHOST_PV1STS)

Address offset: 0x64

Reset value: 0x0004 0002

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						CLKFS_SDR12 [9:0]									
						r									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CLKFS_HS[9:0]									
						r									

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	CLKFS_SDR12 [9:0]	SDCLK Frequency Select Value for SDR12 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_HS [9:0]	SDCLK Frequency Select Value for High Speed 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.7.25 SDHOST Preset Values 2 Status Register (SDHOST_PV2STS)

Address offset: 0x68

Reset value: 0x0001 0002

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						CLKFS_SDR50[9:0]									
						r									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	CLKFS_SDR25[9:0]

r

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	CLKFS_SDR50 [9:0]	SDCLK Frequency Select Value for SDR50 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_SDR25 [9:0]	SDCLK Frequency Select Value for SDR25 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.7.26 SDHOST Preset Values 3 Status Register (SDHOST_PV3STS)

Address offset: 0x6C

Reset value: 0x0002 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						CLKFS_DDR50[9:0]									
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CLKFS_SDR104[9:0]									
r															

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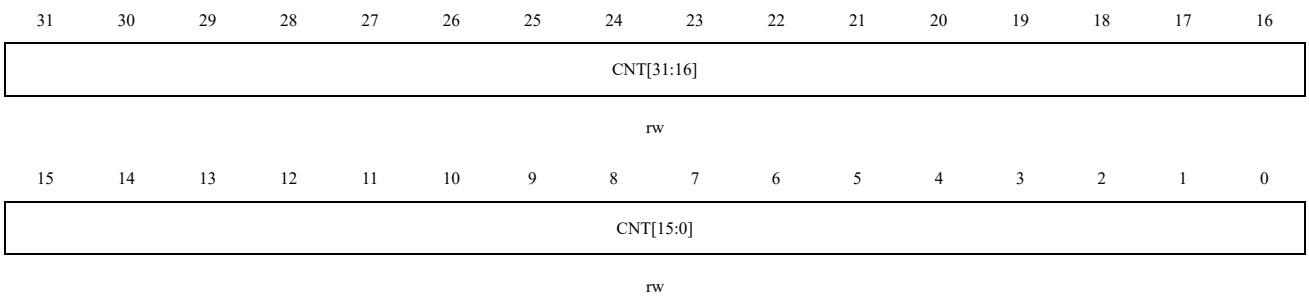
Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	CLKFS_DDR50[9:0]	SDCLK Frequency Select Value for DDR50 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	CLKFS_SDR104[9:0]	SDCLK Frequency Select Value for SDR104 10-bit preset value to set SDCLK Frequency Select in the SDHOST_CTRL2.SDCLKSEL[9:0] is described by a host system. 0x000: Base clock (10 MHz - 104 MHz) 0x001: 1/2 divided clock 0x002: 1/4 divided clock … N: 1/2N divided clock (duty 50%) … 0x3FF: 1/2046 divided clock

39.7.27 SDHOST Boot Timeout Control Register (SDHOST_BOOTTCTRL)

Address offset: 0x70

Reset value: 0x0000 0000



Bit field	Name	Description
31:0	CNT[31:0]	Boot Data Timeout Counter Value This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC card. The value is in number of SD clock.

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40 Universal Serial Bus High-speed Device Dual-role Interfaces （USB_HS_DualRole）

40.1 Introduction

Universal Serial Bus High-speed Device Dual-role Interfaces（USB HS Dual Role）is USBHS for short. The USBHS controller is designed to provide a standard interface for high-speed data transfer and connecting external devices. USBHS supports Host and Device. USBHS includes an internal high-speed PHY. The PHY can be configured as high-speed or full-speed, eliminating the need for an external PHY chip. USBHS can support all four transfer types defined by the USB 2.0 protocol (control transfer, bulk transfer, interrupt transfer, and isochronous transfer). In addition, there is a DMA inside the USBHS, which can act as an AHB bus master to accelerate data transfer between the USBHS and the system.

40.2 Main Features

- Supports USB2.0 high speed(480Mb/s) /full speed(12Mb/s)/low speed(1.5Mb/s) in host mode
- Supports USB2.0 high speed(480Mb/s) /full speed(12Mb/s) in device mode
- Supports Each endpoint supports four transfer types:
  - Control transfer
  - Bulk transfer
  - Interrupt transfer
  - Isochronous transfer
- Built-in high-speed PHY
- Supports the Keep-Alive in Low-Speed mode and SOFs in High/Full-Speed modes
- The SOF pulse can be output through the PAD.
- The SOF pulse is internally connected to the TIMx.
- support for A-B device identification (ID line)
- USBHS embeds an internal DMA with thresholding support and software selectable AHB burst type in DMA mode
- It has power-saving functions, such as system stop during USB suspend, turning off clock domains internal to the digital core, PHY and DFIFO power management
- It features 4 KB of dedicated RAM
- It is up to 16 channels in host mode: each channel is dynamically reconfigurable to allocate any type of USB transfer
- Built-in hardware scheduler holding in host mode:
  - Up to 16 interrupt plus isochronous transfer requests in the periodic hardware queue
  - Up to 16 control plus bulk transfer requests in the non-periodic hardware queue
- There are Rx FIFO, a periodic Tx FIFO and a nonperiodic Tx FIFO in host mode
- Contain 1 bidirectional control endpoint0, and 8 IN/OUT endpoints configurable to support bulk, interrupt or isochronous transfers in device mode
- There are a shared Rx FIFO, a Tx-OUT FIFO and up to 9 dedicated Tx-IN FIFOs in device mode
- Support for the soft disconnect feature

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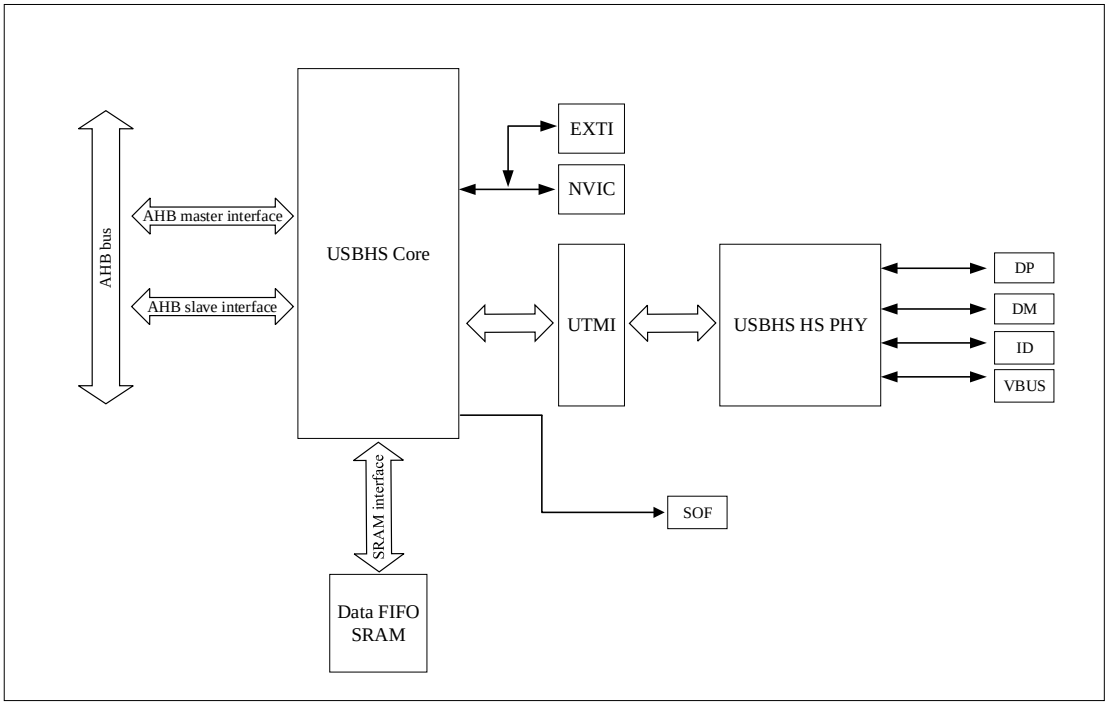
Note: The USB_HS_DM/USB_HS_DP pins of N32H760xxxx do not support high-speed USB, but support full-speed USB and other multiplexed functions. The USB_HS_DM/USB_HS_DP pins of N32H788xxxx support high-speed USB, but do not support functions other than USB (including GPIO functions).

40.3 Functional Description

40.3.1 USBHS System-Level Block Diagram

Figure 40-1 USBHS System-Level Block Diagram



40.3.2 USBHS Pins and Signals

Table 40-1 USBHS Input/Output Signal

Name	Type	Description
VBUS	input	power supply
DM	input/output	negative differential signal line
DP	input/output	positive differential signal line
ID	input	specifies whether the core is a host or device

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40.3.3 Embedded High-speed PHY

The USBHS embeds high-speed PHY, supporting high-speed, full-speed, and low-speed without the need for an external PHY. Integrated pull-up resistor on the ID line for sampling, to configure the USBHS into Host mode or Device mode. The DP/DM controlled by the USBHS module have integrated pull-up and pull-down resistors, with the specific enablement depending on the current mode.

40.4 USBHS Dual-role Device

40.4.1 ID line detection

The host or device(the default) role is assumed depending on the ID input pin.

If the B-side of the USB cable is connected with a floating ID wire, the integrated pullup resistor detects a high ID level and the default device role is confirmed.

If the A-side of the USB cable is connected with a grounded ID, the USBHS issues an ID line status change interrupt (CIDSCHG bit in OTG_GINTSTS) for host software initialization, and automatically switches to the host role.

40.5 USB Device

This section introduces the features of USBHS in device mode. In the following scenarios, the USBHS is used as a device:

- B-side of USB cable is plugged in
- Set the forced device mode bit (USBHS_GCFG.FDMODE) in the USBHS configuration register to 1, thereby forcing the USBHS core to be only a USB device. In this case, even if the ID line is present on the USB connector, it will be ignored.

40.5.1 Device State

40.5.1.1 Powered state

In the powered state, the USBHS expects to receive some reset signaling from the host.
No other USB operation is possible. When a reset signaling is received the reset detected interrupt (USBHS_GINTSTS.USBRSTIF) is generated. When the reset signaling is complete, the enumeration done interrupt (USBHS_GINTSTS. ENUMDIF) is generated and the USBHS enters the Default state.

40.5.1.1.1 Default state

In the Default state the USBHS expects to receive a SET_ADDRESS command from the host. No other USB operation is possible. When a valid SET_ADDRESS command is decoded on the USB, the application writes the corresponding number into the device address field in the device configuration register (USBHS_DCFG.DEVADD[6:0]). The USBHS
then enters the address state and is ready to answer host transactions at the configured USB address.

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40.5.1.1.2 Soft disconnect

The powered state can be exited by software with the soft disconnect feature. The DP pullup resistor is removed by setting the soft disconnect bit in the device control register (USBHS_DCTRL. SFTDIS), causing a device disconnect detection interrupt on the host side even though the USB cable was not really removed from the host port.

40.5.1.1.3 Suspended state

The USBHS device constantly monitors the USB activity. After counting 3 ms of USB idleness, the early suspend interrupt (USBHS_GINTSTS. ESUSPIF) is issued, and confirmed 3 ms later, if appropriate, by the suspend interrupt (USBHS_GINTSTS. USBSUSPIF). The device suspend bit is then automatically set in the device status register (USBHS_DSTS. SUSPF) and the USBHS enters the suspended state.
The suspended state may optionally be exited by the device itself. In this case the application sets the remote wakeup signaling bit in the device control register (USBHS_DCTRL. RMWKUP) and clears it after 1 to 15 ms. When a resume signaling is detected from the host, the resume interrupt (USBHS_GINTSTS.WKUPIF) is generated and the device suspend bit is automatically cleared.

40.5.2 USB Device Endpoint

There are a total of 1 control endpoint 0, 8 IN endpoints, and 8 OUT endpoints for the device. Control endpoint 0 is bidirectional and handles control messages only. IN and OUT endpoints can be configured to support the isochronous, bulk or interrupt transfer type.

Each endpoint of the device has independent control registers, interrupt status registers, transfer size registers, and DMA address registers. The control registers and transfer size registers of endpoint 0 may slightly differ from those of other endpoints, please refer to the register description for specific details.

40.5.2.1 Endpoint control

The following endpoint controls are available to the application through the device endpoint-*x* IN/OUT control register (USBHS_DIEPxCTRL/USBHS_DOEPxCTRL):
– Endpoint enable/disable
– Endpoint activate in current configuration
– Program USB transfer type (isochronous, bulk, interrupt)
– Program supported packet size
– Program Tx FIFO number associated with the IN endpoint
– Program the expected or transmitted data0/data1 PID (bulk/interrupt only)
– Program the even/odd frame during which the transaction is received or transmitted (isochronous only)
– Optionally program the NAK bit to always negative-acknowledge the host regardless of the FIFO status
– Optionally program the STALL bit to always stall host tokens to that endpoint
– Optionally program the SNOOP mode for OUT endpoint not to check the CRC field of received data

40.5.2.2 Endpoint transfer

The device endpoint-*x* transfer size registers (USBHS_DINEPxTSIZ/USBHS_DOUTEPxTSIZ) allow the application to program the transfer size parameters and read the transfer status. Programming must be done before

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setting the endpoint enable bit in the endpoint control register. Once the endpoint is enabled, these fields are read-only as the USBHS core updates them with the current transfer status. The following transfer parameters can be programmed:

- Transfer size in bytes
- Number of packets that constitute the overall transfer size

40.5.2.3 Endpoint status/interrupt

The device endpoint-*x* interrupt registers (USBHS_DINEPxINT/USBHS_DOUTPEPxINT*)* indicate the status of an endpoint with respect to USB- and AHB-related events. The application must read these registers when the OUT endpoint interrupt bit or the IN endpoint interrupt bit in the core interrupt register (USBHS_GINTSTS.OUTEPIF or USBHS_GINTSTS. INEPIF) is set. Before the application can read these registers, it must first read the device all endpoints interrupt (USBHS_DAINT) register to get the exact endpoint number for the device endpoint-*x* interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the USBHS_DAEPINTSTS and USBHS_GINTSTS registers.

40.6 USB Host

This section gives the functional description of the USBHS in the USB host mode. The USBHS works as a USB host in the following circumstances:
– OTG A-device default state when the A-side of the USB cable is plugged in
– Set the forced host mode bit (USBHS_GCFG.FHMODE) in the USBHS configuration register to 0, thereby configuring the USBHS core in normal mode. In this case, the USB switches between host mode and device mode based on the ID line status. When the ID line is grounded, the USBHS is in host mode.

40.6.1 USB Host States

40.6.1.1 Host port power

On-chip 5 V VBUS generation is not supported. For this reason, a charge pump or, if 5 V are available on the application board, a basic power switch, must be added externally to drive the 5 V VBUS line. When the application decides to power on VBUS, it must also set the port power bit in the host port control and status register (USBHS_HPCS.PPWR).

40.6.1.2 Host detection of a peripheral connection

The USB device or B device will be detected immediately after connection. The OTG_HS core issues a host port interrupt triggered by the device connected bit in the host port control and status register (USBHS_HPCS. PCDET).

40.6.1.3 Host detection of peripheral a disconnection

The peripheral disconnection event triggers the disconnect detected interrupt (USBHS_GINTSTS. DISCIF).

40.6.1.4 Host enumeration

After detecting a device connection, if a new device is connected, the host must initiate the enumeration process by sending USB reset and configuration commands to the new device.
The application drives a USB reset signaling (single-ended zero) over the USB by keeping the port reset bit set in the host port control and status register (USBHS_HPCS. PRST) for a minimum of 10 ms and a maximum of 20 ms.

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The application takes care of the timing count and then of clearing the port reset bit.
Once the USB reset sequence has completed, the host port interrupt is triggered by the port enable/disable change bit (PENCHNG bit in OTG_HPRT). This informs the application that the speed of the enumerated peripheral can be read from the port speed field in the host port control and status register (PSPD bit in OTG_HPRT) and that the host is starting to drive SOFs (FS) or Keep alives (LS). The host is now ready to complete the peripheral enumeration by sending peripheral configuration commands.

40.6.1.5 Host suspend

The application decides to suspend the USB activity by setting the port suspend bit in the host port control and status register (USBHS_HPCS.PSUSP). The USBHS core stops sending SOFs and enters the suspended state.
The suspended state can be optionally exited on the remote device's initiative (remote wakeup). In this case the remote wakeup interrupt (USBHS_GINTSTS.WKUPIF) is generated upon detection of a remote wakeup signaling, the port resume bit in the host port control and status register (USBHS_HPCS. PRST) self-sets, and resume signaling is automatically driven over the USB. The application must time the resume window and then clear the port resume bit to exit the suspended state and restart the SOF. If the suspended state is exited on the host initiative, the application must set the port resume bit to start resume signaling on the host port, time the resume window and finally clear the port resume bit.

40.6.2 Host Channels

The USBHS core instantiates 16 host channels. Each host channel supports an USB host transfer (USB pipe). The host is not able to support more than 16 transfer requests at the same time. If more than 16 transfer requests are pending from the application, the host controller driver (HCD) must re-allocate channels when they become available from previous duty, that is, after receiving the transfer completed and channel halted interrupts.
Each host channel can be configured to support in/out and any type of periodic/nonperiodic transaction. Each host channel makes us of proper control (USBHS_HCHxCTRL), transfer configuration (USBHS_HCHxSIZ) and status/interrupt (USBHS_HCHxINTSTS) registers with associated mask (USBHS_HCHxINTEN) registers.

40.6.2.1 Host channel control

The following host channel controls are available to the application through the host channel-*x* characteristics register (USBHS_HCHxCTRL):
– Channel enable/disable
– Program the HS/FS/LS speed of target USB peripheral
– Program the address of target USB peripheral
– Program the endpoint number of target USB peripheral
– Program the transfer IN/OUT direction
– Program the USB transfer type (control, bulk, interrupt, isochronous)
– Program the maximum packet size (MPS)
– Program the periodic transfer to be executed during odd/even frames

40.6.2.2 Host channel transfer

The host channel transfer size registers (USBHS_HCHxSIZ) allow the application to program the transfer size parameters, and read the transfer status. Programming must be done before setting the channel enable bit in the host channel characteristics register. Once the endpoint is enabled the packet count field is read-only as the USBHS core

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updates it according to the current transfer status.
The following transfer parameters can be programmed:
– transfer size in bytes
– number of packets making up the overall transfer size
– initial data PID

40.6.2.3 Host channel status/interrupt

The host channel-x interrupt register (USBHS_HCHxINTSTS) indicates the status of an endpoint with respect to USB- and AHB-related events. The application must read these register when the host channels interrupt bit in the core interrupt register (USBHS_GINTSTS. HCHIF) is set. Before the application can read these registers, it must first read the host all channels interrupt (USBHS_HACHINT) register to get the exact channel number for the host channel-x interrupt register. The application must clear the appropriate bit in this register to clear the corresponding bits in the USBHS_HACHINT and USBHS_GINTSTS registers. The mask bits for each interrupt source of each channel are also available in the USBHS_HCHxINTEN register.
The host core provides the following status checks and interrupt generation:
– Transfer completed interrupt, indicating that the data transfer is complete on both
the application (AHB) and USB sides
– Channel has stopped due to transfer completed, USB transaction error or disable
command from the application
– Associated transmit FIFO is half or completely empty (IN endpoints)
– ACK response received
– NAK response received
– STALL response received
– USB transaction error due to CRC failure, timeout, bit stuff error, false EOP
– Babble error
– frame overrun
– data toggle error

40.6.3 Host scheduler

The host core features a built-in hardware scheduler which is able to autonomously re-order and manage the USB transaction requests posted by the application. At the beginning of each frame the host executes the periodic (isochronous and interrupt) transactions first, followed by the nonperiodic (control and bulk) transactions to achieve the higher level of priority granted to the isochronous and interrupt transfer types by the USB specification.

The host processes the USB transactions through request queues (one for periodic and one for nonperiodic). Each request queue can hold up to 8 entries. Each entry represents a pending transaction request from the application, and holds the IN or OUT channel number along with other information to perform a transaction on the USB. The order in which the requests are written to the queue determines the sequence of the transactions on the USB interface.

At the beginning of each frame, the host processes the periodic request queue first, followed by the nonperiodic request queue. The host issues an incomplete periodic transfer interrupt (USBHS_GINTSTS.PTNCIF) if an isochronous or interrupt transaction scheduled for the

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current frame is still pending at the end of the current frame. The USBHS core is fully responsible for the management of the periodic and nonperiodic request queues.The periodic transmit FIFO and queue status register (USBHS_HPTXFQSTS) and nonperiodic transmit FIFO and queue status register (USBHS_GNPTXFSTS) are read-only registers which can be used by the application to read the status of each request queue.
They contain:

- The number of free entries currently available in the periodic (nonperiodic) request queue (8 max)
- Free space currently available in the periodic (nonperiodic) Tx FIFO (out-transactions)
- IN/OUT token, host channel number and other status information.

As request queues can hold a maximum of 8 entries each, the application can push to schedule host transactions in advance with respect to the moment they physically reach the SB for a maximum of 8 pending periodic transactions plus 8 pending non-periodic transactions.
To post a transaction request to the host scheduler (queue) the application must check that there is at least 1 entry available in the periodic (nonperiodic) request queue by reading the USBHS_HPTXFQSTS.PTXRQSAVL[6:0] or USBHS_GNPTXFSTS.NPTXRQSAV[7:0].

40.7 SOF Trigger

The USBHS core provides means to monitor, track and configure SOF framing in the host and peripheral, as well as an SOF pulse output connectivity feature.

40.7.1 Host SOFs

In host mode the number of PHY clocks occurring between the generation of two consecutive SOF (HS/FS) or Keep-alive (LS) tokens is programmable in the host frame interval register (HFIR), thus providing application control over the SOF framing period. An interrupt is generated at any start of frame (USBHS_GINTSTS.SOFIF). The current frame number and the time remaining until the next SOF are tracked in the host frame number register (USBHS_HFNUM).
A SOF pulse signal, is generated at any SOF starting token and with a width of 20 HCLK cycles. The SOF pulse is also internally connected to the input trigger of the timer, so that the input capture feature, the output compare feature and the timer can be triggered by the SOF pulse.

40.7.2 Device SOFs

In device mode, the start of frame interrupt is generated each time an SOF token is received on the USB (OTH_GINTSTS.SOFIF). The corresponding frame number can be read from the device status register (USBHS_DSTS.SOFFN[13:0]). A SOF pulse signal with a width of 12 system-clock cycles is also generated. The SOF pulse signal is also internally connected to the TIM input trigger, so that the input capture feature, the output compare feature and the timer can be triggered by the SOF pulse.

The end of periodic frame interrupt (USBHS_GINTSTS. EOPFIF) is used to notify the application when 80%, 85%, 90% or 95% of the time frame interval elapsed depending on the periodic frame interval field in the device configuration register (USBHS_DCFG. PFRITVL[1:0]). This feature can be used to determine if all of the isochronous traffic for that frame is complete.

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40.7.3 Dynamic Update of The USBHS_HFRI Register

The USBHS core embeds a dynamic trimming capability of micro-SOF framing period in host mode allowing to synchronize an external device with the micro-SOF frames. When the USBHS_HFRI register is changed within a current micro-SOF frame, the SOF period correction is applied in the next frame

40.8 Power Options

The power consumption of the USBHS PHY is controlled by two bits in the General Module Configuration Register:

The power consumption of the USBHS PHY is controlled by two bits in the general

core configuration register:

- Stop PHY clock（USBHS_PWRCTRL. PHYSTP）

  Setting the stop PHY clock bit in the clock gating control register to 1 will save power by reducing the dynamic power consumption caused by clock signal toggling in the module. Most of the transceiver is also disabled, and only the part in charge of detecting the asynchronous resume or remote wakeup event is kept alive.

- Gate HCLK （USBHS_PWRCTRL.GATEHCLK）

  When setting the Gate HCLK bit in the clock gating control register, most of the system clock domain internal to the USBHS core is switched off by clock gating. Only the register read and write interface is kept alive. The dynamic power consumption due to the USB clock switching activity is cut even if the system clock is kept running by the application for other purposes.

- USB system stop

  When the USBHS is in the USB suspended state, the application may decide to drastically reduce the overall power consumption by a complete shut down of all the clock sources in the system. USB System Stop is activated by first setting the Stop PHY clock bit and then configuring the system deep sleep mode in the power control system module (PWR).

The USBHS core automatically reactivates both system and USB clocks by asynchronous detection of remote wakeup (as an host) or resume (as a device) signaling on the USB.

To save dynamic power, the USB data FIFO is clocked only when accessed by the OTG_HS core.

40.9 USBHS Data FIFO

The USBHS system features 4 Kbytes of dedicated RAM with a sophisticated FIFO control mechanism. The packet FIFO controller module in the OTG_HS core organizes RAM space into Tx FIFOs into which the application pushes the data to be temporarily stored before the USB transmission, and into a single Rx FIFO where the data received from the USB are temporarily stored before retrieval (popped) by the application. The number of instructed FIFOs and how these are organized inside the RAM depends on the device's role. In peripheral mode an additional Tx FIFO is instructed for each active IN endpoint. Any FIFO size is software configured to better meet the application requirements.

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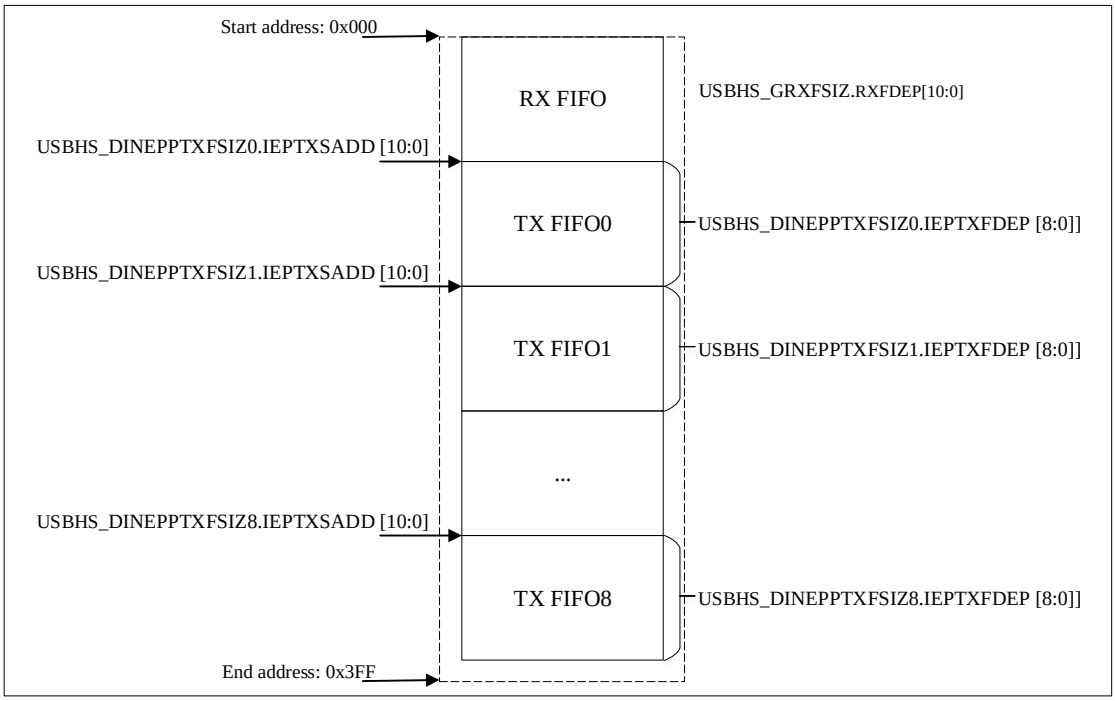
40.9.1 Device FIFO Architecture

Figure40-2 Device-mode FIFO Address Mapping and AHB FIFO Access Mapping



40.9.1.1 Device Rx FIFO

The USBHS peripheral uses a single receive FIFO that receives the data directed to all OUT endpoints. Received packets are stacked back-to-back until free space is available in the Rx FIFO. The status of the received packet (which contains the OUT endpoint destination number, the byte count, the data PID and the validity of the received data) is also stored by the core on top of the data payload. When no more space is available, host transactions are NACKed and an interrupt is received on the addressed endpoint. The size of the receive FIFO is configured in the receive FIFO size register (USBHS_GRXFSIZ).

The single receive FIFO architecture makes it more efficient for the USB peripheral to fill in the receive RAM buffer:

• All OUT endpoints share the same RAM buffer (shared FIFO)

• The OTG_HS core can fill in the receive FIFO up to the limit for any host sequence of OUT tokens

The application keeps receiving the Rx FIFO non-empty interrupt (USBHS_GINTSTS. RXFNEIF) as long as there is at least one packet available for download. It reads the packet information from the receive status read and pop register (USBHS_GRXSTSP) and finally pops data off the receive FIFO by reading from the endpoint-related pop address.

40.9.1.2 Device Tx FIFO

The core has a dedicated FIFO for each IN endpoint. The application configures FIFO sizes by writing the endpoint 0 transmit FIFO size register (USBHS_DIEP0TXFSIZ) for IN endpoint0 and the device IN endpoint transmit FIFOx registers (USBHS_DIEPxTXFSIZ) for IN endpoint-x.

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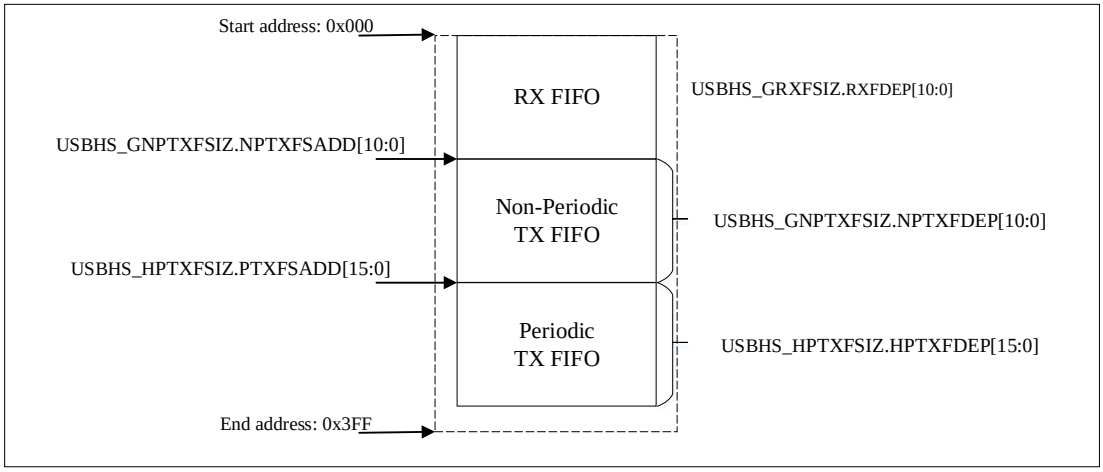
40.9.2 Host FIFO architecture

Figure40-3 Host-mode FIFO Address Mapping and AHB FIFO Access Mapping



40.9.2.1 Host Rx FIFO

The host uses one receiver FIFO for all periodic and nonperiodic transactions. The FIFO is used as a receive buffer to hold the received data (payload of the received packet) from the USB until it is transferred to the system memory. Packets received from any remote IN endpoint are stacked back-to-back until free space is available. The status of each received packet with the host channel destination, byte count, data PID and validity of the received data are also stored into the FIFO. The size of the receive FIFO is configured in the receive FIFO size register (USBHS_GRXFSIZ).

The single receive FIFO architecture makes it highly efficient for the USB host to fill in the

receive data buffer:

- All IN configured host channels share the same RAM buffer (shared FIFO)
- The USBHS core can fill in the receive FIFO up to the limit for any sequence of IN tokens driven by the host software The application receives the Rx FIFO not-empty interrupt as long as there is at least one packet available for download. It reads the packet information from the receive status read and pop register and finally pops the data off the receive FIFO.

40.9.2.2 Host Tx FIFO

The host uses one transmit FIFO for all non-periodic (control and bulk) OUT transactions and one transmit FIFO for all periodic (isochronous and interrupt) OUT transactions. FIFOs are used as transmit buffers to hold the data (payload of the transmit packet) to be transmitted over the USB. The size of the periodic (nonperiodic) Tx FIFO is configured in the host periodic (nonperiodic) transmit FIFO size (USBHS_HPTXFSIZ/USBHS_GNPTXFSIZ)

register.

The two Tx FIFO implementation derives from the higher priority granted to the periodic type of traffic over the USB frame. At the beginning of each frame, the built-in host scheduler processes the periodic request queue first, followed by the nonperiodic request queue.

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The two transmit FIFO architecture provides the USB host with separate optimization for periodic and nonperiodic transmit data buffer management:

- All host channels configured to support periodic (nonperiodic) transactions in the OUT direction share the same RAM buffer (shared FIFOs)
- The USBHS core can fill in the periodic (nonperiodic) transmit FIFO up to the limit for any sequence of OUT tokens driven by the host software

The USBHS core issues the periodic Tx FIFO empty interrupt (USBHS_GINTSTS.PTXFEI) as long as the periodic Tx FIFO is half or completely empty, depending on the value of the periodic Tx FIFO empty level bit in the AHB configuration register USBHS_GAHBCFG.PTXFETH). The application can push the transmission data in advance as long as free space is available in both the periodic Tx FIFO and the periodic request queue. The host periodic transmit FIFO and queue status register (USBHS_HPTXFQSTS) can be read to know how much space is available in both.

The USBHS core issues the non periodic Tx FIFO empty interrupt (USBHS_GINTSTS.NPTXFEIF) as long as the nonperiodic Tx FIFO is half or completely empty depending on the non periodic Tx FIFO empty level bit in the AHB configuration register (USBHS_GAHBCFG. NPTXFETH). The application can push the transmission data as long as free space is available in both the nonperiodic Tx FIFO and nonperiodic request queue. The host nonperiodic transmit FIFO and queue status register (USBHS_GNPTXFSTS) can be read to know how much space is available in both.

40.9.3 FIFO RAM Allocation

40.9.3.1 Device mode

Receive FIFO RAM allocation: the application should allocate RAM for SETUP packets:

- 10 locations must be reserved in the receive FIFO to receive SETUP packets on control endpoint. The core does not use these locations, which are reserved for SETUP packets, to write any other data.
- One location is to be allocated for Global OUT NAK.
- Status information is written to the FIFO along with each received packet. Therefore, a minimum space of (largest packet size / 4) + 1 must be allocated to receive packets. If multiple isochronous endpoints are enabled, then at least two (largest packet size / 4) + 1 spaces must be allocated to receive back-to-back packets. Typically, two (largest packet size / 4) + 1 spaces are recommended so that when the previous packet is being transferred to the CPU, the USB can receive the subsequent packet.
- Along with the last packet for each endpoint, transfer complete status information is also pushed to the FIFO. One location for each OUT endpoint is recommended.

  Device RxFIFO = (5 * number of control endpoints + 8) + ((largest USB packet used / 4) + 1 for status information) + (2 * number of OUT endpoints) + 1 for Global NAK

  Example: The MPS is 1,024 bytes for a periodic USB packet and 512 bytes for a nonperiodic USB packet. There are three OUT endpoints, three IN endpoints, one control endpoint, and three host channels.

  Device RxFIFO = (5 * 1 + 8) + ((1,024 / 4) +1) + (2 * 4) + 1 = 279

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Transmit FIFO RAM allocation: the minimum RAM space required for each IN endpoint. Transmit FIFO is the maximum packet size for that particular IN endpoint.

Note: More space allocated in the transmit IN endpoint FIFO results in better performance on the USB.

40.9.3.2 Host mode

Receive FIFO RAM allocation:

Status information is written to the FIFO along with each received packet. Therefore, a minimum space of (largest packet size / 4) + 1 must be allocated to receive packets. If multiple isochronous channels are enabled, then at least two (largest packet size / 4) + 1 spaces must be allocated to receive back-to-back packets. Typically, two (largest packet size / 4) + 1 spaces are recommended so that when the previous packet is being transferred to the CPU, the USB can receive the subsequent packet.

Along with the last packet in the host channel, transfer complete status information is also pushed to the FIFO. So one location must be allocated for this.

Host RxFIFO = (largest USB packet used / 4) + 1 for status information + 1 transfer complete

Example: Host RxFIFO = ((1,024 / 4) + 1) + 1 = 258

Transmit FIFO RAM allocation:

The minimum amount of RAM required for the host Non-periodic Transmit FIFO is the largest maximum packet size among all supported non-periodic OUT channels.

Typically, two largest packet sizes worth of space is recommended, so that when the current packet is under transfer to the USB, the CPU can get the next packet.

Non-Periodic TxFIFO = largest non-periodic USB packet used / 4

Example: Non-Periodic TxFIFO = (512 / 4) = 128

The minimum amount of RAM required for host periodic Transmit FIFO is the largest maximum packet size out of all the supported periodic OUT channels. If there is at least one isochronous OUT endpoint, then the space must be at least two times the maximum packet size of that channel.

Host Periodic TxFIFO = largest periodic USB packet used / 4

Example: Host Periodic TxFIFO = (1,024 / 4) = 256

Note: More space allocated in the Transmit Non-periodic FIFO results in better performance on the USB.

40.10 USBHS Programming Process

40.10.1 Core Initialization

The application must perform the core initialization sequence. If the cable is connected during power-up, the current

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mode of operation bit in the USBHS_GINTSTS (USBHS_GINTSTS. CMODE) reflects the mode. The USBHS controller enters host mode when an “A” plug is connected or device mode when a “B” plug is connected.

This section explains the initialization of the USBHS controller after power-on. The application must follow the initialization sequence irrespective of host or device mode operation. All core global registers are initialized according to the core’s configuration:

1. Program the following fields in the USBHS_GAHBCFG register:
   – Global interrupt mask bit GINTEN = 1
   – RX FIFO non-empty（USBHS_GINTSTS.RXFNEIF）
   – Periodic Tx FIFO empty level
2. Program the following fields in the USBHS_GCFG register:
   – USBHS timeout calibration field
   – USBHS turnaround time field
3. The software must enable the following bits in the USBHS_GINTEN register:
   – USBHS enable interrupt
4. The software can read the USBHS_GINTSTS.CMODE to determine whether the USBHS controller is operating in host or device mode.

40.10.2 Host initialization

To initialize the core as host, the application must perform the following steps:

1. Program the USBHS_GINTEN. HPIEN register to unmask.
2. Program the USBHS_HCFG register to select host mode (high speed, full speed, low speed).
3. Program the USBHS_HPCS. PPWR to 1. This drives VBUS on the USB.
4. Wait for the USBHS_HPCS. PCDET. This indicates that a device is connecting to the port.
5. Program the USBHS_HPCS.PRST to 1. This starts the reset process.
6. Wait at least 10ms for the reset process to complete.
7. Program the USBHS_HPCS. PRST to 0.
8. Wait for the PENCHNG interrupt in the USBHS_HPCS .PENC register.
9. Read the USBHS_HPCS.PSPD bits to get the enumerated speed.
10. Program the USBHS_HFRI.FRI[15:0] bits with a value corresponding to the selected PHY clock.
11. Program the USBHS_GRXFSIZ register to select the size of the receive FIFO.
12. Program the USBHS_GNPTXFSIZ register to select the size and the start address of the Non-periodic transmit FIFO for non-periodic transactions.
13. Program the USBHS_HPTXFSIZ register to select the size and start address of the periodic transmit FIFO for periodic transactions.

To communicate with devices, the system software must initialize and enable at least one channel.

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40.10.3 Device initialization

The application must perform the following steps to initialize the core as a device on power up or after a mode change from host to device.

1. Program the following fields in the USBHS_DCFG register:
   - Device speed
   - Non-zero-length status OUT handshake
2. Program the USBHS_ GINTEN register to unmask the following interrupts:
   - USB reset
   - Enumeration done
   - Early suspend
   - USB suspend
   - SOF
3. Wait for the USBRSTIF interrupt in USBHS_GINTSTS. It indicates that a reset has been detected on the USB that lasts for about 10ms on receiving this interrupt.
4. Wait for the ENUMDIF interrupt in USBHS_GINTSTS. This interrupt indicates the end of reset on the USB. On receiving this interrupt, the application must read the USBHS_DSTS register to determine the enumeration speed and perform the steps.

At this point, the device is ready to accept SOF packets and perform control transfers on control endpoint 0.

40.11 USBHS Registers

These registers are available in both host mode and device mode, and do not need to be reprogrammed when switching between these two modes. Unless otherwise specified, the bit values in the register descriptions are represented in binary.

USB base address: 0x4004 0000

40.11.1 USBHS Register Overview

40.11.2 USBHS global control and status registers

USBHS1 global control and status register base address: 0x4010 0000

USBHS2 global control and status register base address: 0x4060 0000

40.11.2.1 USBHS global control and status registers（USBHS_GCTRLSTS）

Address offset：0x0000

Reset value: 0x000D 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										CMODE	Reserved				IDSTS

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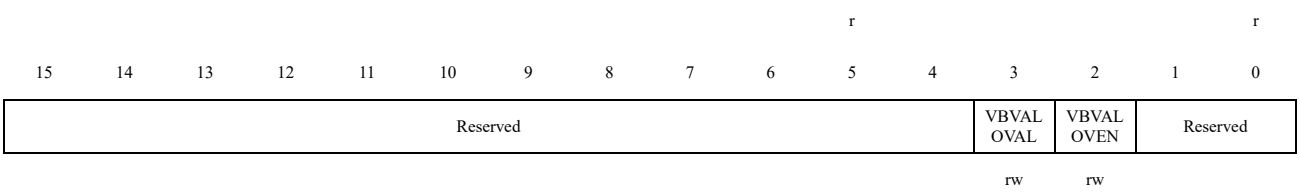

Bit Field	Name	Description
31:22	Reserved	Reserved, must be kept at reset value
21	CMODE	Current mode of operation 0：Device mode 1：Host mode *Note: Indicates the current mode (host or device).*
20:17	Reserved	Reserved, must be kept at reset value
16	IDSTS	Connector ID status 0: The USBHS controller is in A-device mode 1: The USBHS controller is in B-device mode
15:4	Reserved	Reserved, must be kept at reset value
3	VBVALOVAL	VBUS valid override value. This bit is used to set override value for vbusvalid signal when VBVALOEN bit is set. 0: vbusvalid value is '0' when VBVALOEN = 1 1: vbusvalid value is '1' when VBVALOEN = 1 Note: Only accessible in host mode.
2	VBVALOVEN	VBUS valid override enable. This bit is used to enable/disable the software to override the vbusvalid signal using the VBVALOVAL bit. 0: Override is disabled and vbusvalid signal from the respective PHY selected is used internally by the core 1: Internally vbusvalid received from the PHY is overridden with VBVALOVAL bit value Note: Only accessible in host mode

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Bit Field	Name	Description
1:0	Reserved	Reserved, must be kept at reset value

40.11.2.2 USBHS Global AHB Cnfiguration Register（USBHS_GAHBCFG）

Address offset：0x0008

Reset value : 0x0000 0000

Bit Field	Name	Description
31:9	Reserved	Reserved, must be kept at reset value
8	PTXFETH	Periodic Tx FIFO empty level 0: PTXFEIF (in USBHS_GINTSTS) interrupt indicates that the Periodic Tx FIFO is half empty 1: PTXFEIF (in USBHS_GINTSTS) interrupt indicates that the Periodic Tx FIFO is completely empty *Note: Only accessible in host mode.*
7	NPTXFETH	Nonperiodic Tx FIFO empty level Host mode: 0: The NPTXFEIF (in USBHS_GINTSTS) interrupt indicates that the nonperiodic Tx FIFO is half empty 1: The NPTXFEIF (in USBHS_GINTSTS) interrupt indicates that the nonperiodic Tx FIFO is completely empty Device mode: 0:The TXFE (in USBHS_DINTPxINTSTS) interrupt indicates that the IN endpoint Tx FIFO is half empty 1: The TXFE (in USBHS_DINTPxINTSTS) interrupt indicates that the IN

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Bit Field	Name	Description
		endpoint Tx FIFO is completely empty *Note: Accessible in host and device mode.*
6	Reserved	Reserved, must be kept at reset value
5	DMAEN	DMA enabled 0：DMA disabled 1：DMA enabled *Note: Accessible in host and device mode.*
4:1	BURSTTYP [3:0]	Burst bype 0000：single 0001：INCR 0011：INCR4 0101：INCR8 0111：INCR16 Others: Reserved *Note: Accessible in host and device mode.*
0	GINTEN	Global interrupt enable 0：disabled 1：enabled *Note: Accessible in host and device mode.*

40.11.2.3 USBHS Global Configuration Register（USBHS_GCFG）

Address offset：0x000C

Reset value：0x0000 1400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	FDMODE	FHMODE	Reserved												
	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		TRDTIM[3:0]				Reserved			PHYSEL	Reserved		PHYIF	TOCAL[2:0]		
		rw							rw			rw	rw		

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Bit Field	Name	Description
31	Reserved	Reserved, must be kept at reset value
30	FDMODE	Force device mode Writing a 1 to this bit, forces the core to device mode irrespective of the OTG_ID input pin. 0: Normal mode 1: Force device mode After setting the force bit, the application must wait at least 25 ms before the change takes effect. Note: Accessible in device and host modes.
29	FHMODE	Force host mode Writing a 1 to this bit, forces the core to host mode irrespective of the OTG_ID input pin. 0: Normal mode 1: Force host mode After setting the force bit, the application must wait at least 25 ms before the change takes effect. Note: Accessible in device and host modes.
28:14	Reserved	Reserved, must be kept at reset value
13:10	TRDTIM[3:0]	USB turnaround time These bits allows to set the turnaround time in PHY clocks. They must be configured according to or Table 34-2: TRDT values (HS), depending on the application AHB frequency. Higher TRDT values allow stretching the USB response time to IN tokens in order to compensate for longer AHB read access latency to the data FIFO. Note: Only accessible in device mode.
9:7	Reserved	Reserved, must be kept at reset value
6	PHYSEL	PHY select 0: USB 2.0 external ULPI high-speed PHY. 1: USB 1.1 full-speed serial transceiver.

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Bit Field	Name	Description
		Note: Accessible in device and host modes.
5:4	Reserved	Reserved, must be kept at reset value
3	PHYIF	PHY type 0：8bit 1：16bit Note: Accessible in device and host modes.
2:0	TOCAL[2:0]	FS timeout calibration The additional delay introduced by the PHY includes the number of PHY clock cycles set in this field by the application, as well as the inter-packet gap between high-speed/full-speed data packets in the module. The impact of the delay introduced by different PHYs on the data line status varies. The application can use TOC[2:0] to increase this value (in terms of PHY clocks). In the USB standard, the timeout for high-speed operation is 736 to 816 bit times, and for full-speed operation, it is 16 to 18 bit times. The number of bit times added per PHY clock is as follows: High speed: 30MHz PHY clock = 16bit times 60MHz PHY clock = 8bit times Full speed: 30MHz PHY clock = 0.4bit times 60MHz PHY clock = 0.2bit times 000：increase 0 PHY clock 001：increase 1 PHY clock … 111：increase 7 PHY clock Note: Accessible in device and host modes.

Table 40-2 TRDTIM Values（FS）

AHB Frequency Range (MHz)		TRDTIM Minimum Value
Min	Max	

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14.2	15	0xF
15	16	0xE
16	17.2	0xD
17.2	18.5	0xC
18.5	20	0xB
20	21.8	0xA
21.8	24	0x9
24	27.5	0x8
27.5	32	0x7
32	-	0x6

Table 40-3 TRDTIM Values（HS）

AHB Frequency Range (MHz)		**TRDTIM Minimum Value**
Min	**Max**	
30	15	0x9

40.11.2.4 USBHS Global Reset Register（USBHS_GRSTCTRL）

Address offset：0x0010

Reset value：0x8000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AHBIDLE	DMAREQ	SRSTDNE	Reserved												
r	r	rc_w1													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TXFNUM[4:0]					TXFFLSH	RXFFLSH	Reserved	HFCRST	PFSSRST	CSRST
							rw			rs	rs		rs	rs	rs

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Bit Field	Name	Description
31	AHBIDLE	AHB idle state 0：AHB is busy 1：AHB is idle Note: Accessible in device and host modes.
30	DMAREQ	DMA request 0：disable DMA 1：enable DMA Note: Accessible in device and host modes.
29	SRSTDNE	Core Soft Reset Done 0： No reset 1： Core Soft Reset is done Note: Accessible in device and host modes.
28:11	Reserved	Reserved, must be kept at reset value
10:6	TXFNUM[4:0]	TX FIFO Number This is the FIFO number that must be flushed using the TxFIFO Flush bit. This field must not be changed until the core clears the TxFIFO Flush bit. Host mode: 00000：Non-periodic TxFIFO flush 00001：Periodic TxFIFO flush 10000：Flush all the transmit FIFOs Device mode： 00000：Periodic TxFIFO flush 00001：Periodic TxFIF1 flush … 01111：Periodic TxFIF15 flush 10000：Flush all the transmit FIFOs
5	TXFFLSH	TX FIFO Flush

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Bit Field	Name	Description
		The application uses this bit to refresh the TX FIFO data, with TXFNUM[4:0] determining the FIFO number to be refreshed. However, this operation cannot be executed while the module is processing communication transactions. Once the refresh is complete, the hardware automatically clears this bit. After setting this bit, the application needs to wait for it to be cleared, which takes eight clocks to reset (using the slower PHY_CLK or HCLK clock), and no other operations should be performed by the USBHS before this. Read-NAK valid interrupt ensures that the module has not performed a read operation on the FIFO. Write-AHBIDLE ensures that the module has not performed a write operation on the FIFO. It is recommended to refresh the TX FIFO when reconfiguring it, and to refresh the TX FIFO during device endpoint disablement. Note: Accessible in device and host modes.
4	RXFFLSH	RX FIFO Flush The application refreshes the RX FIFO data by setting this control bit. However, this operation cannot be executed while the module is processing communication transactions. Once the refresh is complete, the hardware automatically clears this bit. After setting this bit, the application needs to wait for it to be cleared, which takes eight clocks to reset (using the slower PHY_CLK or HCLK clock), and no other operations should be performed by the USBHS before this. Note: Accessible in device and host modes.
3	Reserved	Reserved, must be kept at reset value
2	HFCRST	Host Frame Counter Reset The application writes this bit to reset the (micro)Frame number counter inside the USBHS. When the (micro)Frame counter is reset, the subsequent SOF sent out by the core has a (micro)Frame number of 0. After the reset operation is completed, the hardware automatically clears this bit. The application needs to wait for this bit to be cleared, and no other operations should be performed by the USBHS before this.

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Bit Field	Name	Description
		Note: Accessible in host modes.
1	PFSSRST	PIU FS Dedicated Controller Soft Reset All module state machines in FS Dedicated Controller of PIU are reset to the IDLE state. Used to reset the FS Dedicated controller in PIU in case of any PHY Errors like Loss of activity or Babble Error resulting in the PHY remaining in RX state for more than one frame boundary. Note: Accessible in device and host modes.
0	CSRST	USB Core Soft Reset Reset AHB and USB clock domain circuits, as well as most of the registers. The following registers or register bits will not be cleared: USBHS_GCFG USBHS_PWRCLKCTRL.PDMRST USBHS_PWRCLKCTRL.GATECLK USBHS_PWRCLKCTRL.PHYSTP Note: Accessible in device and host modes.

40.11.2.5 USBHS Global Interrupt Status Register（USBHS_GINTSTS）

Address offset：0x0014

Reset value：0x0400 0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WKUPIF	Reserved	DISCIF	IDSTSCIF	Reserved	PTXFEIF	HCHIF	HPIF	RSTDIF	FET SUSPIF	PTNCIFISO UTNCIF	ISOINCIF	OUTEPIF	INEPIF	Reserved	
rc_w1		rc_w1	rc_w1		r	r	r	rc_w1	rc_w1	rc_w1	rc_w1	r	r		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOPFIF	ISOUT PDIF	ENUMDIF	USB RSTIF	USB SUSPIF	ESUSPIF	Reserved		GOUT NAKEIF	GINNP NAKEIF	NPTXF EIF	RXFNEIF	SOFIF	Reserved	MOD MISIF	CMODE
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1			r	r	r	r	rc_w1		rc_w1	r

Bit Field	Name	Description
31	WKUPIF	Resume/Remote Wakeup Detected Interrupt flag： Detected the host sending a resume signal, this flag is set.

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Bit Field	Name	Description
		Host mode： Detected the device sending a remote wakeup signal, this flag is set. Note: Accessible in device and host modes.
30	Reserved	Reserved, must be kept at reset value
29	DISCIF	Disconnect Detected Interrupt flag Asserted when a device disconnect is detected. Note: Accessible in host modes.
28	IDSTSCIF	Connector ID Status Change The core sets this bit when there is a change in connector ID status. Note: Accessible in device and host modes.
27	Reserved	Reserved, must be kept at reset value
26	PTXFEIF	Periodic TxFIFO Empty Interrupt flag When the periodic TX FIFO is half-empty or completely empty, and there is at least one entry to be written in the periodic request queue, this flag is set. The TX FIFO empty threshold is determined by USBHS_GAHBCFG.PTXFETH. Note: Accessible in host modes.
25	HCHIF	Host Channels Interrupt flag When an interrupt is suspended on any channel in host mode, this flag is set. Software needs to first read the USBHS_HACHINT register to obtain the corresponding channel number, and then read the corresponding USBHS_HCHxINTSTS register to obtain the specific flag that caused the interrupt on the corresponding channel. The corresponding channel interrupt flag can be cleared by the USBHS_HCHxINTSTS register, and after the interrupt flag of the corresponding channel is cleared, the flag will be automatically cleared. Note: Accessible in host modes.
24	HPIF	Host Port Interrupt flag When the USBHS detects a change in the port status in host mode, this flag is set. Software needs to first read the USBHS_HPCS

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Bit Field	Name	Description
		register to obtain the interrupt source. The corresponding interrupt flag can be cleared by the USBHS_HPCS register, and after the flag causing the port interrupt is cleared, the flag will be automatically cleared. Note: Accessible in host modes.
23	RSTDIF	Reset detected Interrupt flag When the device is in suspend mode and a reset is detected, this flag is set. Note: Accessible in device modes.
22	FETSUSPIF	Data Fetch Suspended Interrupt flag This interrupt is only valid in DMA mode. This interrupt indicates that the module has stopped acquiring data for the IN endpoint due to unavailable space in the TX FIFO or request queue. This interrupt is used when the application endpoint does not match. For example, after detecting an endpoint mismatch, the application will perform the following actions: Sets a Global non-periodic IN NAK handshake ■ Disables IN endpoints ■ Flushes the FIFO ■ Determines the token sequence from the IN Token Sequence Learning Queue ■ Re-enables the endpoints ■ Clears the Global non-periodic IN NAK handshake If the Global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received. The core generates an 'IN token received when FIFO empty' interrupt. It then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a Global NAK handshake. Alternatively, the application can mask the IN token received when FIFO empty interrupt when clearing a Global IN NAK

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Bit Field	Name	Description
		handshake.Note: Accessible in device modes.
21	PTNCIF	Incomplete Periodic Transfer Interrupt flag In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current microframe.
	ISOUTNCIF	Incomplete Isochronous OUT Transfer Interrupt flag The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.
20	ISOINCIF	Incomplete Isochronous IN Transfer Interrupt flag Incomplete Isochronous IN Transfer (incompISOIN) The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register Accessible in device modes.
19	OUTEPIF	OUT Endpoints Interrupt flag When an interrupt is suspended on any OUT endpoint, this flag is set. The corresponding OUT endpoint needs to be read first by reading the USBHS_DAEPINTSTS register, and then the corresponding USBHS_DOUTEPxINTSTS register should be read to obtain the flag that caused the interrupt. Once the flag of the corresponding endpoint that caused the interrupt is cleared, this interrupt flag will be automatically cleared. Accessible in device modes.
18	INEPIF	IN Endpoints Interrupt flag When an interrupt is suspended on any IN endpoint in device mode, this flag is set. Software should first read the USBHS_DAEPINT register to obtain the corresponding IN endpoint, and then read the corresponding USBHS_DINEPxINSTS register to obtain the flag that caused the interrupt. Once the flag of the corresponding endpoint

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Bit Field	Name	Description
		that caused the interrupt is cleared, this interrupt flag will be automatically cleared. Accessible in device modes.
17:16	Reserved	Reserved, must be kept at reset value
15	EOPFIF	End of Periodic Frame Interrupt flag When the USB bus time within one frame reaches the value defined by USBHS_DCFG.PFRITVL, the USBHS sets this interrupt flag. Accessible in device modes.
14	ISOUTPDIF	Isochronous OUT Packet Dropped Interrupt flag The controller sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint. Accessible in device modes.
13	ENUMDIF	Enumeration Done Interrupt flag The core sets this bit to indicate that speed enumeration is complete. The application can read USBHS_DSTS.ENUMSPD[1:0] to obtain the current device speed. Accessible in device modes.
12	USBRSTIF	USB Reset Interrupt flag The controller sets this bit to indicate that a reset is detected on the USB. Accessible in device modes.
11	USBSUSPIF	USB Suspend Interrupt flag The controller sets this bit to indicate that a suspend was detected on the USB. The controller enters the Suspended state when there is no activity on the linestate signal for an extended period of time. Accessible in device modes.
10	ESUSPIF	Early Suspend Interrupt flag The controller sets this bit to indicate that an Idle state has been detected

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Bit Field	Name	Description
		on the USB for 3 ms. Accessible in device modes.
9:8	Reserved	Reserved, must be kept at reset value
7	GOUTNAKEIF	Global OUT NAK Effective flag When USBHS_DCTRL.SGONAK is set to 1, and after the global OUT NAK takes effect, this flag is set. Software can clear this flag by writing 1 to USBHS_DCTRT.CGONAK. Accessible in device modes.
6	GINNPNAKEIF	Global IN Non-periodic NAK Effective flag When USBHS_DCTRL.SGINAK is set to 1, and after the global IN NAK takes effect, this flag is set. Software can clear this flag by writing 1 to USBHS_DCTRT.CGINAK. This interrupt does not necessarily indicate that a NAK handshake signal has been sent on the USB. The STALL bit takes precedence over the NAK bit. Accessible in device modes.
5	NPTXFEIF	Non-periodic TxFIFO Empty Interrupt flag When the non-periodic TX FIFO is half-empty or completely empty, and there is at least one entry to be written in the non-periodic request queue, this flag is set. The TX FIFO empty threshold is determined by USBHS_GAHBCFG.NPTXFETH. Note: Accessible in device and host modes.
4	RXFNEIF	RxFIFO Non-Empty Interrupt flag Indicates that there is at least one packet pending to be read from the RxFIFO. Note: Accessible in device and host modes.
3	SOFIF	Start of (micro)Frame (SOF) Interrupt flag In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, the controller sets this bit to indicate that an SOF token has been received on the USB. The application can read the

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Bit Field	Name	Description
		Device Status register to get the current (micro)Frame number. This interrupt is seen only when the core is operating at either HS or FS. This bit can be set only by the core and the application must write 1 to clear it. Note: Accessible in device and host modes.
2	Reserved	Reserved, must be kept at reset value
1	MODMISIF	Mode Mismatch Interrupt Flag The core sets this bit when the application is trying to access: ■ A Host mode register, when the controller is operating in Device mode ■ A Device mode register, when the controller is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the controller internally and does not affect the operation of the controller. This bit can be set only by the core and the application must write 1 to clear it. Note: Accessible in device and host modes.
0	CMODE	Current Mode of Operation Indicates the current mode. ■ 0: Device mode ■ 1: Host mode Note: Accessible in device and host modes.

40.11.2.6 USBHS Global Interrupt enable Register（USBHS_GINTEN）

Address offset：0x0018

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WKUPIEN	Reserved	DISCIEN	IDSTSCIEN	Reserved	PTXFEIEN	HCHIEN	HPIEN	RSTDIEN	FETSUSP	PTNCIENISOUTNCIEN	ISOINCIEN	OUTEPIEN	INEPIEN	Reserved	
rw		rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw		

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOPFIEN	ISOUTPDIEN	ENUMDIEN	USBRSTIEN	USBSUSPIEN	ESUSPIEN	Reserved		GOUTNAKEIEN	GINNPNAKEIEN	NPTXFEIEN	RXFNEIEN	SOFIEN	USBHSIEN	MODMISIEN	Reserved
rw	rw	rw	rw	rw	rw			rw	rw	rw	rw	rw	rw	rw	

Bit Field	Name	Description
31	WKUPIEN	Resume/Remote Wakeup Detected Interrupt enable 0：disable Resume or Remote Wakeup Detected Interrupt 1：enable Resume or Remote Wakeup Detected Interrupt Note: Accessible in device and host modes.
30	Reserved	Reserved, must be kept at reset value
29	DISCIEN	Disconnect Detected Interrupt enable 0：disable 1：enable Note: Accessible in host modes.
28	IDSTSCIEN	Connector ID Status Change interrupt enable 0：disable 1：enable Note: Accessible in device and host modes.
27	Reserved	Reserved, must be kept at reset value
26	PTXFEIEN	Periodic TxFIFO Empty interrupt enable 0：disable 1：enable Note: Accessible in host modes.
25	HCHIEN	Host Channels Interrupt enable 0：disable 1：enable Note: Accessible in host modes.
24	HPIEN	Host Port Interrupt enable

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Bit Field	Name	Description
		0：disable 1：enable Note: Accessible in host modes.
23	RSTDIEN	Reset detected Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
22	FETSUSPIEN	Data Fetch Suspended Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
21	PTNCIEN	**Incomplete Periodic Transfer** Interrupt enable Host mode： 0：disable 1：enable
	ISOUTNCIEN	**Incomplete Isochronous OUT Transfer Interrupt enable** Device mode： 0：disable 1：enable
20	ISOINCIEN	Incomplete Isochronous IN Transfer enable 0：disable 1：enable Note: Accessible in device modes.
19	OUTEPIEN	OUT Endpoints Interrupt enable 0：disable 1：enable Note: Accessible in device modes.

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Bit Field	Name	Description
18	INEPIEN	IN Endpoints Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
17:16	Reserved	Reserved, must be kept at reset value
15	EOPFIEN	End of Periodic Frame Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
14	ISOUTPDIEN	Isochronous OUT Packet Dropped Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
13	ENUMDIEN	Enumeration Done Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
12	USBRSTIEN	USB reset Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
11	USBSUSPIEN	USB suspend Interrupt enable 0：disable 1：enable Note: Accessible in device modes.
10	ESUSPIEN	Early suspend Interrupt enable 0：disable

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Bit Field	Name	Description
		1：enable Note: Accessible in device modes.
9:8	Reserved	Reserved, must be kept at reset value
7	GOUTNAKEIEN	Global OUT NAK Effective enable 0：disable 1：enable Note: Accessible in device modes.
6	GINNPNAKEIEN	Global Non-periodic IN NAK Effective enable 0：disable 1：enable Note: Accessible in device modes.
5	NPTXFEIEN	Non-periodic TxFIFO Empty Interrupt enable 0：disable 1：enable Note: Accessible in device and host modes.
4	RXFNEIEN	Receive FIFO Non-Empty Interrupt enable 0：disable 1：enable Note: Accessible in device and host modes.
3	SOFIEN	Start of (micro)Frame Interrupt enable 0：disable 1：enable Note: Accessible in device and host modes.
2	USBHSIEN	USBHS Interrupt enable 0：disable 1：enable Note: Accessible in device and host modes.
1	MODMISIEN	Mode Mismatch Interrupt enable

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Bit Field	Name	Description
		0：disable 1：enable Note: Accessible in device and host modes.
0	Reserved	Reserved, must be kept at reset value

40.11.2.7 USBHS Global Receive Status Debug Read Register （USBHS_GRXSTS/USBHS_GRXSTSP）

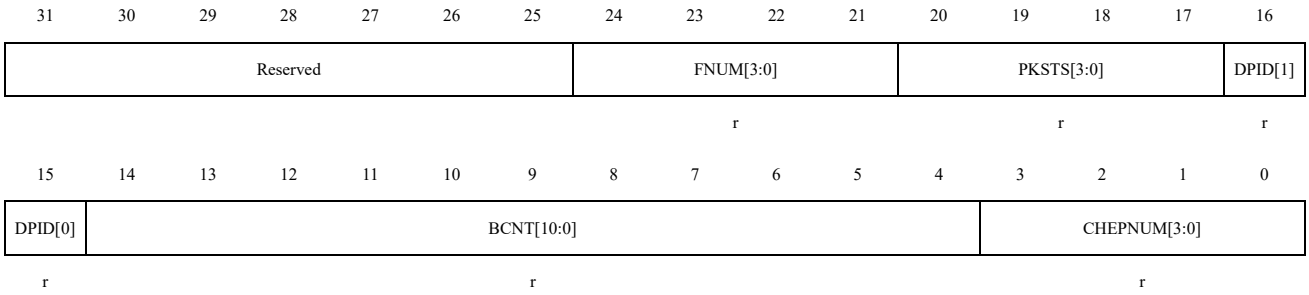
Read Address offset：0x001C

Pop Address offset：0x0020

Reset value：0x0000 0000

Reading the USBHS_GRXSTS register will return the content at the top of the receive FIFO. Reading the USBHS_GRXSTSP register will additionally pop the top data from the RX FIFO.

It is necessary to distinguish the receive status content in Host mode and Device mode. When the receive FIFO is empty, the USBHS will ignore USBHS_GRXSTSP. After the RX FIFO not empty interrupt flag USBHS_GINTSTS.RXFNEIF is set, the application can only read the USBHS_GRXSTS register.



Bit Field	Name	Description
31:25	Reserved	Reserved, must be kept at reset value
24:21	FNUM[3:0]	Frame Number This is the least significant 4 bits of the (micro)Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported. Note: Accessible in device modes.
20:17	PKTSTS[3:0]	Packet Status (PktSts) indicates the status of the received packet. In host mode,

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Bit Field	Name	Description
		■ 4'b0010: IN data packet received ■ 4'b0011: IN transfer completed (triggers an interrupt) ■ 4'b0101: Data toggle error (triggers an interrupt) ■ 4'b0111: Channel halted (triggers an interrupt) ■ Others: Reserved Reset:4'b0 In device mode, ■ 4'b0001: Global OUT NAK (triggers an interrupt) ■ 4'b0010: OUT data packet received ■ 4'b0011: OUT transfer completed (triggers an interrupt) ■ 4'b0100: SETUP transaction completed (triggers an interrupt) ■ 4'b0110: SETUP data packet received ■ Others: Reserved Reset:4'h0
16:15	DPID[1:0]	Data PID In host mode, indicates the Data PID of the received packet. In device mode, indicates the Data PID of the received OUT data packet. ■ 2'b00: DATA0 ■ 2'b10: DATA1 ■ 2'b01: DATA2 ■ 2'b11: MDATA Reset: 2'h0
14:4	BCNT[10:0]	Bytes count In host mode, indicates the byte count of the received IN data packet. In device mode, indicates the byte count of the received data packet.
3:0	CHEPNUM[3:0]	**Channel /Endpoint number:**

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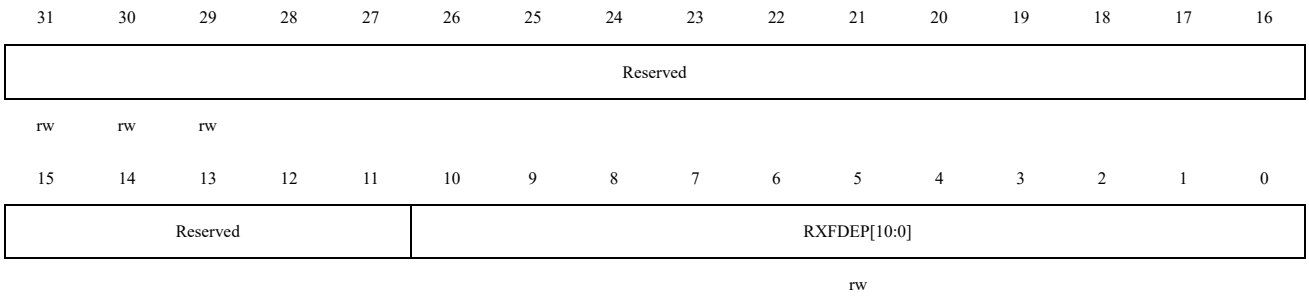
Bit Field	Name	Description
		Mode: Host only Indicates the channel number to which the current received packet belongs. Mode: Device only Indicates the endpoint number to which the current received packet belongs.

40.11.2.8 USBHS Global Receive FIFO Size Register（USBHS_GRXFSIZ）

Address offset：0x0024

Reset value：0x0000 0400

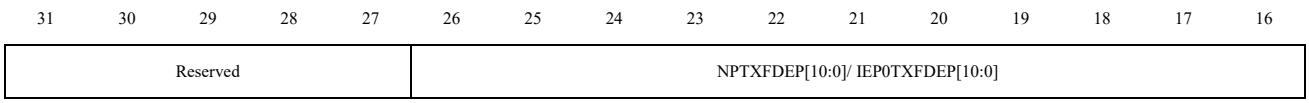


Bit Field	Name	Description
31:11	Reserved	Reserved, must be kept at reset value
10:0	RXFDEP[10:0]	RxFIFO Depth This value is in terms of 32-bit words. ■ Minimum value is 16 ■ Maximum value is 32,768

40.11.2.9 USBHS Global Non-periodic Transmit FIFO Size Register（USBHS_GNPTXFSIZ）/ Device IN endpoint 0 transmit FIFO size register（USBHS_DINEP0TXFSIZ）

Address offset：0x0028

Reset value：0x0400 0400



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										rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					NPTXFSADD[10:0]/ IEP0TXFSADD[10:0]										
					rw										

Host mode

Bit Field	Name	Description
31:27	Reserved	Reserved, must be kept at reset value
26:16	NPTXFDEP[10:0]	Host Non-periodic TxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16, Maximum value is 32,768, Must not exceed the reset value
15:11	Reserved	Reserved, must be kept at reset value
10:0	NPTXFSADD[10:0]	Host non-periodic TX FIFO start address Non-periodic TX FIFO start address

Device mode

Bit Field	Name	Description
31:27	Reserved	Reserved, must be kept at reset value
26:16	IEP0TXFDEP[10:0]	IN endpoint 0 TX FIFO depth This value is in terms of 32-bit words. Minimum value is 16, Maximum value is 1024, Must not exceed the reset value
15:11	Reserved	Reserved, must be kept at reset value
10:0	IEP0TXFRSADD[10:0]	IN endpoint 0 TX RAM start address Endpoint 0 TX FIFO RAM start address

40.11.2.10 USBHS Global Non-periodic Transmit FIFO/Queue Status Register （USBHS_GNPTXFSTS）

Address offset：0x002C

Reset value：0x0000 0400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	NPTXRQTOP[6:0]							NPTXRQSAV[7:0]							

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r															r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPTXFSAV[15:0]															
r															

Bit Field	Name	Description
31	Reserved	Reserved, must be kept at reset value
30:24	NPTXRQTOP[6:0]	Top of the Non-periodic Transmit Request Queue Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. ■ Bits [30:27]: Channel/endpoint number ■ Bits [26:25]: ■ 2'b00: IN/OUT token - 2'b01: Zero-length transmit packet (device IN/host OUT) - 2'b10: PING/CSPLIT token - 2'b11: Channel halt command ■ Bit [24]: Terminate (last Entry for selected channel/endpoint)
23:16	NPTXRQSAV[7:0]	Non-periodic Transmit Request Queue Space Available Indicates the amount of free space available in the Non-periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. ■ 8'h0: Non-periodic Transmit Request Queue is full ■ 8'h1: 1 location available ■ 8'h2: 2 locations available ■ n: n locations available (0 <= n <= 8) ■ Others: Reserved Reset: Configurable
15:0	NPTXFSAV[15:0]	Non-periodic TxFIFO Space Avail (NPTxFSpcAvail) Indicates the amount of free space available in the Non-periodic

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Bit Field	Name	Description
		TxFIFO. Values are in terms of 32-bit words. ■ 16'h0: Non-periodic TxFIFO is full ■ 16'h1: 1 word available ■ 16'h2: 2 words available ■ 16'hn: n words available (where 0 <= n <= 512) ■ Others: Reserved

40.11.2.11 USBHS User ID Register（USBHS_CID）

Address offset：0x003C

Reset value：0x0000 3608

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CID[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CID[15:0]															
rw															

Bit Field	Name	Description
31:0	CID	User ID (UserID) Application-programmable ID field. Reset value is configurable. Value After Reset: 0x12345678

40.11.2.12 USBHS Global Power Down Register（USBHS_GPD）

Address offset：0x0058

Reset value：0x0000 0010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										IDDIG	LINSTS		STSCHNGINTEN	STSCHNGINTSTS	Reserved
										r	r		rw	rc_w1	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CONNDETINTEN	CONNDETSTS	DISCONNDETINTEN	DISCONNDETSTS	RESTDETINTEN	RESTDETSTS	LINSTSCHNGINTEN	LINSTSCHNGSTS	Reserved						

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rw rc_w1 rw rc_w1 rw rc_w1 rw rc_w1

Bit Field	Name	Description
31:22	Reserved	Reserved, must be kept at reset value
21	IDDIG	This bit indicates the status of the signal IDDIG. The application must read this bit after receiving GPWRDN.StsChngInt and decode based on the previous value stored by the application. Indicates the current mode. ■ 0: Host mode ■ 1: Device mode
20:19	LINSTS[0:1]	LineState. ■ 2'b00: DM = 0, DP = 0. ■ 2'b01: DM = 0, DP = 1. ■ 2'b10: DM = 1, DP = 0. ■ 2'b11: Not-defined.
18	STSCHNGINTEN	Mask for StsChng Interrupt ■ 0 (NOMASK): No Status Change Interrupt Mask ■ 1 (MASK): Mask for Status Change Interrupt
17	STSCHNGINTSTS	Status Change Interrupt (StsChngInt) ■ 0: No Status change ■ 1: Status change detected
16:15	Reserved	Reserved, must be kept at reset value
14	CONNDETINTEN	Mask for ConnectDet interrupt ■ 0 (NOMASK): No ConnectDet Interrupt Mask ■ 1 (MASK): Mask for ConnectDet Interrupt
13	CONNDETSTS	This field indicates that a new connect has been detected ■ 0: Connect not detected ■ 1: Connect detected

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Bit Field	Name	Description
12	DISCONNDETINTEN	Mask For DisconnectDetect Interrupt ■ 0 (NOMASK): No DisconnectDetect Interrupt Mask ■ 1 (MASK): Mask for DisconnectDetect Interrupt
11	DISCONNDETSTS	This field generates an interrupt. After detecting disconnect during hibernation the application must not restore the core, but instead start the initialization process. ■ 0: Disconnect not detected ■ 1: Disconnect detected
10	RESTDETINTEN	Mask for ResetDetected interrupt ■ 0 (NOMASK): No ResetDetect Interrupt Mask ■ 1 (MASK): Mask for ResetDetect Interrupt
9	RESTDETSTS	This field indicates that Reset has been detected by the PMU module. This field generates an interrupt. ■ 0: Reset Not Detected ■ 1: Reset Detected
8	LINSTSCHNGINTEN	Mask for LineStateChange interrupt. ■ 0 (NOMASK): No LineStateChange Interrupt Mask ■ 1 (MASK): Mask for LineStateChange Interrupt
7	LINSTSCHNGSTS	This interrupt is asserted when there is a Linestate Change detected by the PMU. The application must read GPWRDN.Linestate to determine the current linestate on USB. ■ 0: No LineState change on USB ■ 1: LineState change on USB
6:0	Reserved	Reserved, must be kept at reset value

40.11.2.13 USBHS Host Periodic Transmit FIFO Size Register（USBHS_HPTXFSIZ）

Address offset：0x00100

Reset value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HPTXFDEP[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HPTXFSADD[15:0]															
rw															

Bit Field	Name	Description
31:16	HPTXFDEP[15:0]	Host Periodic TxFIFO Depth This value is in terms of 32-bit words. ■ Minimum value is 16 ■ Maximum value is 1024
15:0	HPTXFSADD[15:0]	Host Periodic TxFIFO Start Address

40.11.2.14 USBHS Device IN Endpoint/Periodic Transmit FIFO-x Size Register （USBHS_DINEPPTXFSIZx）(x=[1..8])

Address offset：0x00104 + (x-1)×4

Reset value：0x0100 0500

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						DPTXFDEP [9:0]									
						rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DPTXSADD [11:0]											
				rw											

Device Periodic Transmit FIFO size register

Bit Field	Name	Description
31:26	Reserved	Reserved, must be kept at reset value
25:16	DPTXFDEP [9:0]	Device Periodic TxFIFO Size This value is in terms of 32-bit words. ■ Minimum value is 4

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Bit Field	Name	Description
		■ Maximum value is 768
15:11	Reserved	Reserved, must be kept at reset value
11:0	DPTXSADD [11:0]	Device Periodic TxFIFO RAM Start Address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					INEPTXFDEP [10:0]										
					rw										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					INEPTXSADD [10:0]										
					rw										

Device IN Endpoint Transmit FIFO size register

Bit Field	Name	Description
31:27	Reserved	Reserved, must be kept at reset value
26:16	INEPTXFDEP [10:0]	IN Endpoint TxFIFO Size This value is in terms of 32-bit words. ■ Minimum value is 16 ■ Maximum value is 1024
15:11	Reserved	Reserved, must be kept at reset value
10:0	INEPTXSADD [10:0]	IN Endpoint TxFIFO RAM Start Address

40.11.3 USBHSHost control and status register

40.11.3.1 USBHS Host Configuration Register（USBHS_HCFG）

Address offset：0x0400

Reset value：0x0000 0200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	SPSEL	Reserved
	rw	

Bit Field	Name	Description
31:3	Reserved	Reserved, must be kept at reset value
2	SPSEL	The application uses this bit to control the core's enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even If the connected device supports HS traffic. Do not make changes to this field after initial programming. ■ 0: HS/FS/LS, based on the maximum speed supported by the connected device ■ 1: FS/LS-only, even If the connected device can support HS
1:0	Reserved	Reserved, must be kept at reset value

40.11.3.2 USBHS Host Frame Interval Register（USBHS_HFRI）

Address offset：0x0404

Reset value：0x0000 EA60

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															DRLDEN
															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRI[15:0]															
rw															

Bit Field	Name	Description
31:17	Reserved	Reserved, must be kept at reset value
16	DRLDEN	Reload Control This bit allows dynamic reloading of the HFIR register during run

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Bit Field	Name	Description
		time. ■ 0 : The HFIR cannot be reloaded dynamically ■ 1: the HFIR can be dynamically reloaded during runtime. This bit needs to be programmed during initial configuration and its value must not be changed during runtime.
15:0	FRI[15:0]	Frame Interval (FrInt) The value that the application programs to this field specifies the interval between two consecutive SOFs (FS) or micro- SOFs (HS) or Keep-Alive tokens (HS). This field contains the number of PHY clocks that constitute the required frame interval. The Default value set in this field is for FS operation when the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been Set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select field of the Host Configuration register (HCFG.FSLSPclkSel). Do not change the value of this field after the initial configuration. ■ 125 us * (PHY clock frequency for HS) ■ 1 ms * (PHY clock frequency for FS/LS)

40.11.3.3 USBHS Host Frame Number/Frame Time Remaining Register（USBHS_HFNUM）

Address offset：0x0408

Reset value：0x0000 3FFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRT[15:0]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRNUM[15:0]															
r															

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Bit Field	Name	Description
31:16	FRT[15:0]	Frame Remaining Time It indicates the remaining time of the current frame (in PHY clock cycles). This field decrements by 1 for each PHY clock cycle. When the value reaches zero, this field reloads the value of the frame interval register (USBHS_HFRI.FRI[15:0]) and the module sends a new SOF on the USB.
15:0	FRNUM[15:0]	Frame Number This field increments when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF. ■ 0 (INACTIVE): No SOF is transmitted ■ 1 (ACTIVE): SOF is transmitted

40.11.3.4 USBHS Host Periodic Transmit FIFO/Queue Status Register（USBHS_HPTXFQSTS）

Address offset：0x0410

Reset value：0x0008 0400

Bit Field	Name	Description
31:23	PTXRQTOP[8:0]	Top of the Periodic Transmit Request Queue This indicates the Entry in the Periodic Tx Request Queue that is currently being processed by the MAC. This register is used for debugging. ■ Bit [31]: Odd/Even (micro)Frame - 1'b0: send in even (micro)Frame - 1'b1: send in odd (micro)Frame

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		■ Bits [30:27]: Channel/endpoint number ■ Bits [26:25]: Type - 2'b00: IN/OUT - 2'b01: Zero-length packet - 2'b10: CSPLIT - 2'b11: Disable channel command ■ Bit [24]: Last Periodic Entry for the selected periodic channel/endpoint ■ Bit [23]: Terminate (last Entry for the selected channel/endpoint)
22:16	PTXRQSAVL[6:0]	Periodic Transmit Request Queue Space Available Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. ■ 7'h0: Periodic Transmit Request Queue is full ■ 7'h1: 1 location available ■ 7'h2: 2 locations available ■ n: n locations available (0 <= n <= 16) ■ Others: Reserved
15:0	PTXFSAVL[15:0]	Periodic Transmit Data FIFO Space Available Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words ■ 16'h0 : Periodic TxFIFO is full ■ 16'h1 : 1 word available ■ 16'h2 : 2 words available ■ 16'hn : n words available (where0 ≤ n ≤USBHS_HPTXFSIZ.HPTXFDEP[15:0]) ■ Others : Reserved

40.11.3.5 USBHSHost All Channels Interrupt Register（USBHS_HACHINT）

Address offset：0x0414

Reset value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HACHINT[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value
15:0	HACHINT[15:0]	Channel Interrupt for channel no. One bit for each channel: CH0 corresponds to bit 0, CH15 corresponds to bit 15.

40.11.3.6 USBHS Host All Channels Interrupt Mask Register（USBHS_HACHINTEN）

Address offset：0x0418

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HACHINTEN[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value
15:0	HACHINTEN[15:0]	Channel Interrupt Mask (HAINTMsk) One bit per channel: Bit 0 for channel 0, bit 15 for channel 15 ■ 0x0 (UNMASK): Unmask Channel interrupt ■ 0x1 (MASK): Mask Channel interrupt

40.11.3.7 USBHS Host Port Control and Status Register（USBHS_HPCS）

Address offset：0x0440

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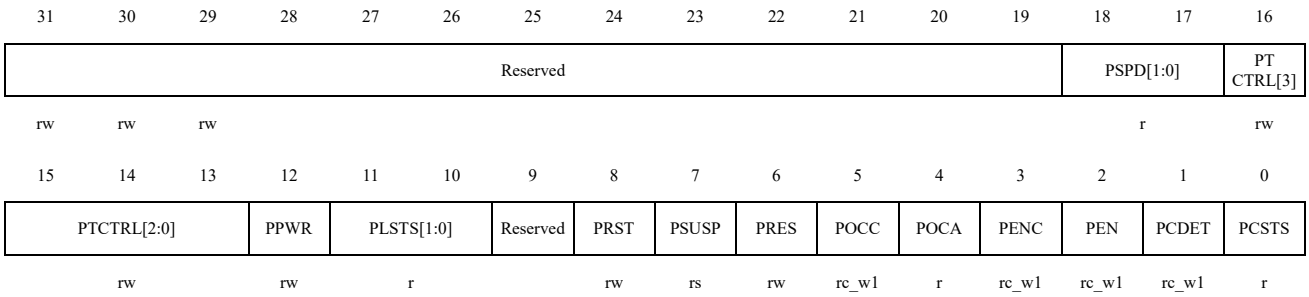
Reset value：0x0000 0000



Bit Field	Name	Description
31:19	Reserved	Reserved, must be kept at reset value
18:17	PSPD[1:0]	Port Speed (PrtSpd) Indicates the speed of the device attached to this port. ■ 2'b00: High speed ■ 2'b01: Full speed ■ 2'b10: Low speed ■ 2'b11: Reserved
16:13	PTCTRL[3:0]	Port Test Control The application writes a nonzero value to this field to put the port into a Test mode, and the corresponding pattern is signaled on the port. ■ 4'b0000: Test mode disabled ■ 4'b0001: Test_J mode ■ 4'b0010: Test_K mode ■ 4'b0011: Test_SE0_NAK mode ■ 4'b0100: Test_Packet mode ■ 4'b0101: Test_Force_Enable ■ Others: Reserved
12	PPWR	Port Power The application uses this field to control power to this port (write 1'b1 to set to 1'b1 and write 1'b0 to set to 1'b0), and the core can

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Bit Field	Name	Description
		clear this bit on an over current condition. ■ 0: Power off ■ 1: Power on
11:10	PLSTS[1:0]	Port Line Status Indicates the current logic level USB data lines ■ Bit [10]: Logic level of D+ ■ Bit [11]: Logic level of D
9	Reserved	Reserved, must be kept at reset value
8	PRST	Port Reset When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. ■ 0: Port not in reset ■ 1: Port in reset The application must leave this bit set for at least a minimum duration mentioned below to start a reset on the port. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit Set by the USB standard.This bit is cleared by the core even if there is no device connected to the Host.
7	PSUSP	Port Suspend The core only stops sending SOFs when this is Set. Once this control bit is set, it can only be cleared through the following operations. – set USBHS_HPCS.PRST – set USBHS_HPCS.PRES –Detected a remote wakeup signal –Detected a device disconnect

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Bit Field	Name	Description
		▪ 0: Port not in Suspend mode ▪ 1: Port in Suspend mode
6	PRES	Port Resume The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (USBHS_GINTSTS. WKUPIF), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. ■ 0: No resume driven ■ 1: Resume driven
5	POCC	Port Overcurrent Change The core sets this bit when the status of the Port Overcurrent Active bit (bit 4) in this register changes.This bit can be set only by the core and the application must write 1 to clear it
4	POCA	Port Overcurrent Active Indicates the overcurrent condition of the port. ■ 0: No overcurrent condition ■ 1: Overcurrent condition
3	PENC	Port Enable/Disable Change The core sets this bit when the status of the Port Enable bit [2] of this register changes.This bit can be set only by the core and the application must write 1 to clear it.
2	PEN	Port Enable

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Bit Field	Name	Description
		A port is enabled only by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot Set this bit by a register write. It can only clear it to disable the port by writing 1. This bit does not trigger any interrupt to the application. ■ 0: Port disabled ■ 1: Port enabled
1	PCDET	Port Connect Detected The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt).This bit can be set only by the core and the application must write 1 to clear it.The application must write a 1 to this bit to clear the interrupt.
0	PCSTS	Port Connect Status ■ 0: No device is attached to the port. ■ 1: A device is attached to the port.

40.11.3.8 USBHS Host Channel Characteristics Register（USBHS_HCHxCTRL）(x=[0..15])

Address offset：0x0500 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHEN	CHDIS	ODDFRM	DEVADDR[6:0]							MCNT[1:0]		EPTYPE[1:0]		LSPDDEV	Reserved
rs	rs	rw	rw							rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPDIR	EPNUM[3:0]				MPS[10:0]										
rw	rw				rw										

Bit Field	Name	Description
31	CHEN	Channel Enable

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Bit Field	Name	Description
		This field is set to 1 by the application software and cleared by hardware. ■ 1'b0: Channel disabled ■ 1'b1: Channel enabled
30	CHDIS	Channel Disable The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled. ■ 0x0 (INACTIVE): Transmit/Recieve normal ■ 0x1 (ACTIVE): Stop transmitting/receiving data on channel
29	ODDFRM	Odd Frame This field is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro)Frame. This field is applicable for only periodic (isochronous and interrupt) transactions. ■ 0: Even (micro)Frame ■ 1: Odd (micro)Frame
28:22	DEVADDR[6:0]	Device Address This field selects the specific device serving as the data source or sink.
21:20	MCNT[1:0]	Multi Count For periodic transfers, this Bit Field specifies the number of transactions the host must perform in each microframe. For non periodic transfers, this field is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes arbitration. ■ 2'b00: Reserved This field yields undefined results. ■ 2'b01: 1 transaction

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Bit Field	Name	Description
		■ 2'b10: 2 transactions to be issued for this endpoint per microframe ■ 2'b11: 3 transactions to be issued for this endpoint per microframe
19:18	EPTYPE[1:0]	Endpoint Type Indicates the transfer type selected. ■ 2'b00: Control ■ 2'b01: Isochronous ■ 2'b10: Bulk ■ 2'b11: Interrupt
17	LSPDDEV	Low-Speed Device This field is Set by the application to indicate that this channel is communicating to a low-speed device.
16	Reserved	Reserved, must be kept at reset value
15	EPDIR	Endpoint Direction (EPDir) Indicates whether the transaction is IN or OUT. ■ 0: OUT ■ 1: IN
14:11	EPNUM[3:0]	Endpoint Number Indicates the endpoint number on the device serving as the data source or sink.
10:0	MPS[10:0]	Maximum Packet Size Indicates the maximum packet size of the associated endpoint.

40.11.3.9 USBHS Host Channel Split Control Register（USBHS_HCHxSCTRL）(x=[0..15])

Address offset：0x0504 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPLEN	Reserved														COMP SPLF
rw															rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRANPOS[1:0]		HUBADDR[6:0]							PRTADD[6:0]						
rw		rw							rw						

Bit Field	Name	Description
31	SPLEN	Split Enable (SpltEna) The application sets this field to indicate that this channel is enabled to perform split transactions.
30:17	Reserved	Reserved, must be kept at reset value
16	COMPSPLF	Do Complete Split The application sets this field to request the OTG host to perform a complete split transaction.
15:14	TRANPOS[1:0]	Transaction Position This field is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. ■ 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). ■ 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). ■ 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188 bytes). ■ 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes).
13:7	HUBADD[6:0]	Hub Address This field holds the device address of the transaction translator's hub.
6:0	PRTADD[6:0]	Port Address This field is the port number of the recipient transaction translator.

40.11.3.10 USBHS Host Channel Interrupt Register（USBHS_HCHxINTSTS）(x=[0..15])

Address offset：0x0508 + x×20

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Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DTERRIF	FOVRIF	BBERRIF	TXERRIF	NYETIF	ACKIF	NAKIF	STALLIF	AHB ERRIF	CHHTDIF	TXCFIF
					rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31:11	Reserved	Reserved, must be kept at reset value
10	DTERRIF	Data Toggle Error ■ 0 (INACTIVE): No Data Toggle Error ■ 1 (ACTIVE): Data Toggle Error
9	FOVRIF	Frame Overrun : ■ 0 (INACTIVE): No Frame Overrun ■ 1 (ACTIVE): Frame Overrun
8	BBERRIF	Babble Error ■ 0 (INACTIVE): No Babble Error ■ 1 (ACTIVE): Babble Error
7	TXERRIF	Transaction Error Indicates one of the following errors occurred on the USB. ■ CRC check failure ■ Timeout ■ Bit stuff error ■ False EOP In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application must write 1 to clear it. ■ 0 (INACTIVE): No Transaction Error

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Bit Field	Name	Description
		■ 1 (ACTIVE): Transaction Error
6	NYETIF	NYET Response Received Interrupt (NYET) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application must write 1 to clear it. ■ 0 (INACTIVE): No NYET Response Received Interrupt ■ 1 (ACTIVE): NYET Response Received Interrupt
5	ACKIF	ACK Response Received/Transmitted Interrupt (ACK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application must write 1 to clear it. ■ 0 (INACTIVE): No ACK Response Received or Transmitted Interrupt ■ 1 (ACTIVE): ACK Response Received or Transmitted Interrup
4	NAKIF	NAK Response Received Interrupt (NAK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application must write 1 to clear it. ■ 0 (INACTIVE): No NAK Response Received Interrupt ■ 1 (ACTIVE): NAK Response Received Interrupt
3	STALLIF	STALL Response Received Interrupt (STALL) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.This bit can be set only by the core and the application must write 1 to clear it. ■ 0 (INACTIVE): No Stall Response Received Interrupt ■ 1 (ACTIVE): Stall Response Received Interrupt
2	AHBERRIF	AHB Error This is generated only in Internal DMA mode when there is an AHB

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Bit Field	Name	Description
		error during AHB read/write. The application can read the corresponding channel's DMA address register to get the error address. For details, see "AHB Error Handling" in the Programming Guide. ■ 0 (INACTIVE): No AHB error ■ 1 (ACTIVE): AHB error during AHB read/write
1	CHHTDIF	Channel Halted When DMA is not enabled: It indicates abnormal completion of the transfer, possibly due to any USB transaction error, application disable request, or completed transfer. When DMA is enabled: This indicates abnormal termination of the transfer due to any USB transaction error or in response to an application disable request. ■ 0 (INACTIVE): Channel not halted ■ 1 (ACTIVE): Channel Halted
0	TXCFIF	Transfer Completed ■ 0 (INACTIVE): Transfer in progress or No Active Transfer ■ 1 (ACTIVE): Transfer completed normally without any errors

40.11.3.11 USBHS Host Channel Interrupt Mask Register（USBHS_HCHxINTEN）(x=[0..15])

Address offset：0x050C + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DTERR IEN	FOVRIEN	BBERR IEN	TXERR IEN	NYETIEN	ACKIEN	NAKIEN	STALL IEN	AHBERR IEN	CHHLTD IEN	TXCIEN
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:11	Reserved	Reserved, must be kept at reset value

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Bit Field	Name	Description
10	DTERRIEN	Data Toggle Error Mask ■ 0 (MASK): Mask Data Toggle Error ■ 1 (NOMASK): No Data Toggle Error Mask
9	FOVRIEN	Frame Overrun Mask ■ 0 (MASK): Mask Overrun Mask ■ 1 (NOMASK): No Frame Overrun Mask
8	BBERRIEN	Babble Error Mask ■ 0 (MASK): Mask Babble Error ■ 1 (NOMASK): No Babble Error Mask
7	TXERRIEN	Transaction Error Mask ■ 0 (MASK): Mask Transaction Error ■ 1 (NOMASK): No Transaction Error Mask
6	NYETIEN	NYET Response Received Interrupt Mask ■ 0 (MASK): Mask NYET Response Received Interrupt ■ 1 (NOMASK): No NYET Response Received Interrupt Mask
5	ACKIEN	ACK Response Received/Transmitted Interrupt Mask ■ 0 (MASK): Mask ACK Response Received/Transmitted Interrupt ■ 1 (NOMASK): No ACK Response Received/Transmitted Interrupt Mask
4	NAKIEN	NAK Response Received Interrupt Mask ■ 0 (MASK): Mask NAK Response Received Interrupt ■ 1 (NOMASK): No NAK Response Received Interrupt Mask
3	STALLIEN	STALL Response Received Interrupt Mask ■ 0 (MASK): Mask STALL Response Received Interrupt ■ 1 (NOMASK): No STALL Response Received Interrupt Mask
2	AHBERRIEN	AHB Error Mask ■ 0 (MASK): AHB Error Mask

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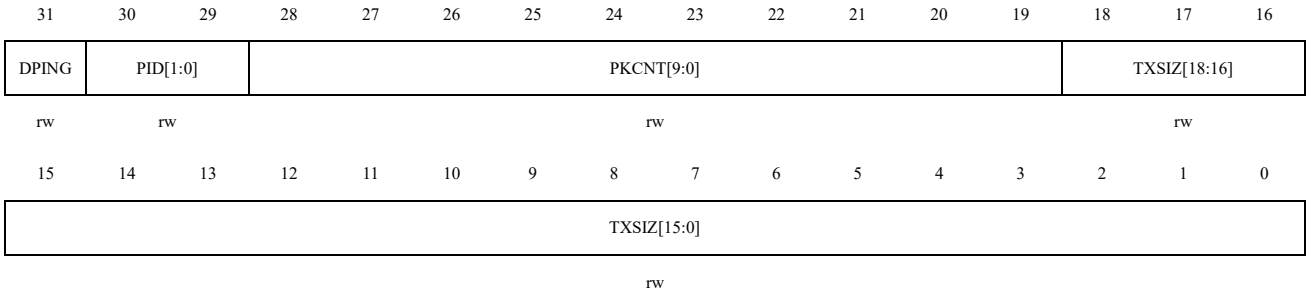
Bit Field	Name	Description
		■ 1 (NOMASK): No AHB Error Mask
1	CHHTDIEN	Channel Halted Mask ■ 0 (MASK): Channel Halted Mask ■ 1 (NOMASK): No Channel Halted Mask
0	TXCIEN	Transfer Completed Mask ■ 0 (MASK): Transfer Completed Mask ■ 1 (NOMASK): No Transfer Completed Mask

40.11.3.12 USBHS Host Channel Transfer Size Register（USBHS_HCHxTXSIZ）(x=[0..15])

Address offset：0x0510 + x×20

Reset value：0x0000 0000



Bit Field	Name	Description
31	DPING	Token Request This bit is only valid for OUT transfers. If set by software, the USBHS will perform the PING protocol. When an OUT transaction receives a NAK or NYET handshake packet, the USBHS will automatically set this control bit. Do not set this bit for IN transfers.
30:29	PID[1:0]	PID Software should write this Bit Field before the start of the transfer. For OUT transfers, this Bit Field contains the data PID of the first transfer packet. For IN transfers, this Bit Field contains the data PID of the first received packet. After the transfer begins, the USBHS automatically changes and switches this Bit Field according to the USB protocol.

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Bit Field	Name	Description
		00： DATA0 01： DATA2 10： DATA1 11： MDATA (non-control)/SETUP (control)
28:19	PKCNT[9:0]	Packet Count This field is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion.
18:0	TXSIZ[18:0]	Transfer Size For an OUT, this field is the number of data bytes the host sends during the transfer. For an IN, this field is the buffer size that the application has Reserved for the transfer. The application is expected to program this field as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic).

40.11.3.13 USBHS Host Channel DMA Address Register（USBHS_HCHxDMADD）(x=[0..15])

Address offset：0x0514 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMADD[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMADD[31:0]															
rw															

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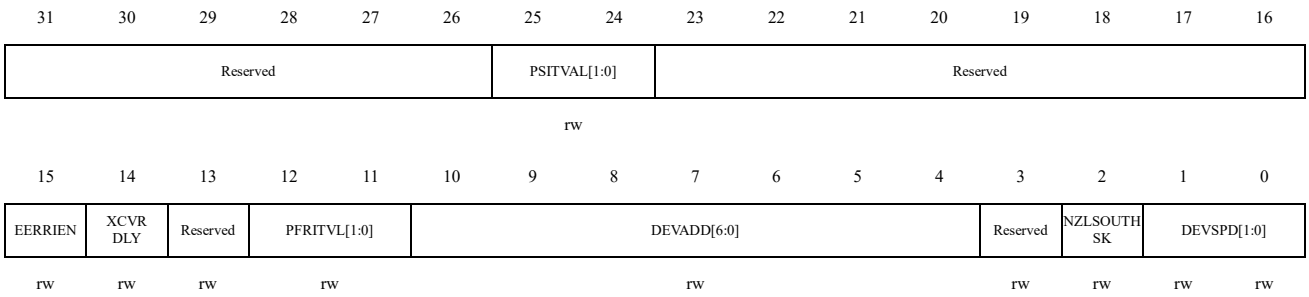
Bit Field	Name	Description
31:0	DMADD[31:0]	DMA Address This field stores the starting address of the memory used by the host to fetch data from a device endpoint or send data to a device endpoint. This register is incremented with each DMA transfer.

40.11.4 USBHS Device control and status register

40.11.4.1 USBHS Device Configuration Register（USBHS_DCFG）

Address offset：0x0800

Reset value：0x0802 0000



Bit Field	Name	Description
31:26	Reserved	Reserved, must be kept at reset value
25:24	PSITVL[1:0]	Periodic Scheduling Interval PerSchIntvl must be programmed for Scatter/Gather DMA mode. This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)Frame. ■ When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data . ■ When no periodic endpoints are active, Then the internal DMA

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Bit Field	Name	Description
		engine services non-periodic endpoints, ignoring this field. ■ After the specified time within a (micro)Frame, the DMA switches to fetching for non-periodic endpoints. - 2'b00: 25% of (micro)Frame. - 2'b01: 50% of (micro)Frame. - 2'b10: 75% of (micro)Frame. - 2'b11: Reserved
23:16	Reserved	Reserved, must be kept at reset value
15	EERRAIEN	Erratic Error Interrupt Mask ■ 0 (NOMASK): Early suspend interrupt is generated on erratic error ■ 1 (MASK): Mask early suspend interrupt on erratic error
14	XCVRDLY	Transceiver delay Enable or disable the delay of PHY timing during device chirping. 0：Disable delay (use default timing) 1：Enable default timing delay
13	Reserved	Reserved, must be kept at reset value
12:11	PFRITVL[1:0]	Periodic Frame Interval Indicates the time within a (micro)Frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine If all the isochronous traffic for that (micro)Frame is complete. ■ 2'b00: 80% of the (micro)Frame interval ■ 2'b01: 85% of the (micro)Frame interval ■ 2'b10: 90% of the (micro)Frame interval ■ 2'b11: 95% of the (micro)Frame interval
10:4	DEVARR[6:0]	Device Address The application must program this field after every SetAddress

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Bit Field	Name	Description
		control command.
3	Reserved	Reserved, must be kept at reset value
2	NZLSOUTHSK	Non-Zero-Length Status OUT Handshake The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. ■ 1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. ■ 0: Send the received OUT packet to the application (zerolength or nonzero-length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.
1:0	DEVSPD[1:0]	Device Speed Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the connect sequence is completed, and is based on the speed of the USB host to which the core is connected. Values: ■ 0x0 (USBHS20): High speed USB 2.0 PHY clock is 30 MHz or 60 MHz ■ 0x1 (USBFS20): Full speed USB 2.0 PHY clock is 30 MHz or 60 MHz ■ Others: Reserved

40.11.4.2 USBHSDevice Control Register（USBHS_DCTRL）

Address offset：0x0804

Reset value：0x0000 0002

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															NAKOBBLE
rw	rw	rw													rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				POPDNE	CGONAK	SGONAK	CGNPINAK	SGINAK	TSCTRL[2:0]			GONAKSTS	GINAKSTS	SFTDIS	RMWKUP
				rw	w	w	w	w	rw			r	r	rw	rw

Bit Field	Name	Description
31:17	Reserved	Reserved, must be kept at reset value
16	NAKOBBLE	NAK on Babble Error Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received.
15:12	Reserved	Reserved, must be kept at reset value
11	POPDNE	Power-On Programming Done The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.
10	CGONAK	Clear Global OUT NAK A write to this field clears the Global OUT NAK.
9	SGONAK	Set Global OUT NAK Writing to this bit will set the global OUT NAK to 1. The application sends NAK handshake signals to all OUT endpoints. The application can set this bit to 1 only when it has ensured that the global OUT NAK valid bit in the module interrupt register (USBHS_GINTSTS.GOUTNAKEIF) has been cleared.
8	CGNPINAK	Clear Global Non-periodic IN NAK A write to this field clears the Global Non-periodic IN NAK.
7	SGINAK	Set Global Non-periodic IN NAK A write to this field sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all nonperiodic

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Bit Field	Name	Description
		IN endpoints. The core can also Set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application can set this bit to 1 only when it has ensured that the global IN NAK valid bit in the module interrupt register (USBHS_GINTSTS.GINNPNAKEIF) has been cleared.
6:4	TSCTRL[2:]	Test Control ■ 3'b000: Test mode disabled ■ 3'b001: Test_J mode ■ 3'b010: Test_K mode ■ 3'b011: Test_SE0_NAK mode ■ 3'b100: Test_Packet mode ■ 3'b101: Test_Force_Enable ■ Others: Reserved
3	GONAKSTS	Global OUT NAK Status (GOUTNakSts) ■ 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. ■ 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.
2	GINAKSTS	Global Non-periodic IN NAK Status ■ 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. ■ 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.
1	SFTDIS	Soft Disconnect The application uses this bit to signal the controller to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the

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Bit Field	Name	Description
		USB. The core stays in the disconnected state until the application clears this bit. ■ 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. ■ 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host.
0	RMWKUP	Remote Wakeup Signaling (RmtWkUpSig) When the application sets this bit, the core initiates remote signaling to wake up the USB host. The application must Set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it. ■ 0x0 (DISABLEDRMWKUP): Core does not send Remote Wakeup Signaling ■ 0x1 (ENABLERMWKUP): Core sends Remote Wakeup Signaling

40.11.4.3 USBHS Device Status Register（USBHS_DSTS）

Address offset：0x0808

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								DEVLINSTS[1:0]		SOFFN[13:8]					
								r		r					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOFFN[7:0]								Reserved				ERERRF	ENUMSPD[1:0]		SUSPF
r												r	r		r

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Bit Field	Name	Description
31:24	Reserved	Reserved, must be kept at reset value
23:22	DEVLINSTS[1:0]	Device Line Status Indicates the current logic level USB data lines ■ DevLnSts[1]: Logic level of D+ ■ DevLnSts[0]: Logic level of DValue
21:8	SOFFN[13:0]	Frame or Microframe Number of the Received SOF The USBHS will update this field upon receipt of a SOF token.
7:4	Reserved	Reserved, must be kept at reset value
3	ERERRF	Erratic Error The module sets this bit to 1 to report any undefined error. Due to the undefined error, the USBHS controller will enter a suspended state, and an interrupt will be generated for the application with the early suspend bit (USBHS_GINTSTS.ESUSPIF) of the USBHS_GINTSTS register. If the early suspend interrupt is triggered by an undefined error, the application can only perform a soft disconnect to recover communication.
2:1	ENUMSPD[1:0]	Enumerated Speed (EnumSpd) Indicates the speed at which the controller has come up after speed detection through a connect or reset sequence. ■ 2'b00: High speed (PHY clock is running at 30 or 60 MHz) ■ 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) ■ Others: Reserved
0	SUSPF	Suspend Status In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspend state when there is no activity on the phy_line_state_i signal for an extended period of time. The core comes out of the suspend under the following conditions : –There is activity on the USB data line. –The application writes to the remote wakeup bit

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Bit Field	Name	Description
		(USBHS_DCTRL.RMWKUP) in the USBHS_DCTRL register.

40.11.4.4 USBHS Device IN Endpoint Common Interrupt Mask Register （USBHS_DINEPINTEN）

Address offset：0x0810

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		NAKIEN	Reserved				TXFUDIEN	Reserved	INEPNAKEIEN	INTREPMSIEN	TXFERINTKIEN	TOIEN	AHBERRIEN	EPDISIEN	TXCIEN
		rw					rw		rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, must be kept at reset value
13	NAKIEN	NAK interrupt Mask ■ 0 (MASK): Mask NAK Interrupt ■ 1 (NOMASK): No Mask NAK Interrupt
12:9	Reserved	Reserved, must be kept at reset value
8	TXFUDIEN	Fifo Underrun Mask Values: ■ 0 (MASK): Mask Fifo Underrun Interrupt ■ 1 (NOMASK): No Fifo Underrun Interrupt Mask
7	Reserved	Reserved, must be kept at reset value
6	INEPNAKEIEN	IN Endpoint NAK Effective Mask ■ 0 (MASK): Mask IN Endpoint NAK Effective Interrupt ■ 1 (NOMASK): No IN Endpoint NAK Effective Interrupt Mask

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Bit Field	Name	Description
5	INTREPMISIEN	IN Token received with EP Mismatch Mask ■ 0 (MASK): Mask IN Token received with EP Mismatch Interrupt ■ 1 (NOMASK): No Mask IN Token received with EP Mismatch Interrupt
4	TXFERINTKIEN	IN Token Received When TxFIFO Empty Mask ■ 0 (MASK): Mask IN Token Received When TxFIFO Empty Interrupt ■ 1 (NOMASK): No IN Token Received When TxFIFO Empty Interrupt
3	TOIEN	Timeout Condition Mask (Non-isochronous endpoints) ■ 0 (MASK): Mask Timeout Condition Interrupt ■ 1 (NOMASK): No Timeout Condition Interrupt Mask
2	AHBERRIEN	AHB Error Mask (AHBErrMsk) ■ 0 (MASK): Mask AHB Error Interrupt ■ 1 (NOMASK): No AHB Error Interrupt Mask
1	EPDISIEN	Endpoint Disabled Interrupt Mask ■ 0 (MASK): Mask Endpoint Disabled Interrupt ■ 1 (NOMASK): No Endpoint Disabled Interrupt Mask
0	TXCIEN	Transfer Completed Interrupt Mask ■ 0 (MASK): Mask Transfer Completed Interrupt ■ 1 (NOMASK): No Transfer Completed Interrupt Mask

40.11.4.5 USBHS Device OUT Endpoint Common Interrupt Mask Register （USBHS_DOUTEPINTEN）

Address offset：0x0814

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	NYETIEN	NAKIEN	BERRIEN	Reserved			OPERRIEN	Reserved	B2BSTUPIEN	Reserved	EPDISROTIEN	STUPDNEIEN	AHBERRIEN	EPDISIEN	TXCIEN
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, must be kept at reset value
14	NYETIEN	NYET interrupt Mask ■ 0 (MASK): Mask NYET Interrupt ■ 1 (NOMASK): No NYET Interrupt Mask
13	NAKIEN	NAK interrupt Mask ■ 0 (MASK): Mask NAK Interrupt ■ 1 (NOMASK): No NAK Interrupt Mask
12	BERRIEN	Babble Error interrupt Mask ■ 0 (MASK): Mask Babble Error Interrupt ■ 1 (NOMASK): No Babble Error Interrupt Mask
11:9	Reserved	Reserved, must be kept at reset value
8	OPERRIEN	OUT Packet Error Mask ■ 0 (MASK): Mask OUT Packet Error Interrupt ■ 1 (NOMASK): No OUT Packet Error Interrupt Mask
7	Reserved	Reserved, must be kept at reset value
6	B2BSTUPIEN	Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only. ■ 0 (MASK): Mask Back-to-Back SETUP Packets Received Interrupt ■ 1 (NOMAS
5	Reserved	Reserved, must be kept at reset value
4	EPDISROTIEN	OUT Token Received when Endpoint Disabled Mask Applies to control OUT endpoints only.

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Bit Field	Name	Description
		■ 0 (MASK): Mask OUT Token Received when Endpoint Disabled Interrupt ■ 1 (NOMASK): No OUT Token Received when Endpoint Disabled Interrupt Mask
3	STUPDNEIEN	SETUP Phase Done Mask Applies to control endpoints only. ■ 0 (MASK): Mask SETUP Phase Done Interrupt ■ 1 (NOMASK): No SETUP Phase Done Interrupt Mask
2	AHBERRIEN	AHB Error ■ 0 (MASK): Mask AHB Error Interrupt ■ 1 (NOMASK): No AHB Error Interrupt Mask
1	EPDIEN	Endpoint Disabled Interrupt Mask ■ 0 (MASK): Mask Endpoint Disabled Interrupt ■ 1 (NOMASK): No Endpoint Disabled Interrupt Mask
0	TXCIEN	Transfer Completed Interrupt Mask ■ 0 (MASK): Mask Transfer Completed Interrupt ■ 1 (NOMASK): No Transfer Completed Interrupt Mask

40.11.4.6 USBHS Device All Endpoints Interrupt Register（USBHS_DAEPINTSTS）

Address offset：0x0818

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							OUTEP INT8	OUTEP INT7	OUTEP INT6	OUTEP INT5	OUTEP INT4	OUTEP INT3	OUTEP INT2	OUTEP INT1	OUTEP INT0
							r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							INEPINT8	INEPINT7	INEPINT6	INEPINT5	INEPINT4	INEPINT3	INEPINT2	INEPINT1	INEPINT0
							r	r	r	r	r	r	r	r	r

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Bit Field	Name	Description
31:25	Reserved	Reserved, must be kept at reset value
24:16	OUTEPINT[8:0]	Device OUT Endpoint Interrupt state Each bit represents an OUT endpoint: Bit 16 represents OUT endpoint 0 Bit 24 represents OUT endpoint 8。
15:8	Reserved	Reserved, must be kept at reset value
7:0	INEPINT[8:0]	Device IN Endpoint Interrupt state Each bit represents an IN endpoint: Bit 0 represents IN endpoint 0, Bit 8 represents IN endpoint 8.

40.11.4.7 USBHS Device All Endpoints Interrupt Mask Register（USBHS_DAEPINTEN）

Address offset：0x081C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							OUTEPIEN8	OUTEPIEN7	OUTEPIEN6	OUTEPIEN5	OUTEPIEN4	OUTEPIEN3	OUTEPIEN2	OUTEPIEN1	OUTEPIEN0
							rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							INEPIEN8	INEPIEN7	INEPIEN6	INEPIEN5	INEPIEN4	INEPIEN3	INEPIEN2	INEPIEN1	INEPIEN0
							rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:25	Reserved	Reserved, must be kept at reset value
24:16	OUTEPIEN[8:0]	Device OUT Endpoint Interrupt Enable Each bit represents an OUT endpoint: Bit 16 represents OUT endpoint 0, Bit 24 represents OUT endpoint 8. The interrupt entry when an interrupt occurs is USB_HS_IRQn.
15:8	Reserved	Reserved, must be kept at reset value
7:0	INEPIEN [8:0]	Device IN Endpoint Interrupt Enable Translation: Each bit represents an IN endpoint: Bit0 represents IN endpoint 0, Bit8 represents IN endpoint 8.

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Bit Field	Name	Description
		The interrupt entry for generating interrupts is USB_HS_IRQn.

40.11.4.8 USBHS Device Threshold Control Register（USBHS_DTHRCTRL）

Address offset：0x0830

Reset value：0x0000 0000

Bit Field	Name	Description
31:28	Reserved	Reserved, must be kept at reset value
27	ARPEN	Arbiter Parking Enable This bit controls internal DMA arbiter parking for IN endpoints. If thresholding is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into underrun conditions. By default, arbiter parking is enabled. ■ 0 (DISABLED): Disable DMA arbiter parking ■ 1 (ENABLED): Enable DMA arbiter parking for IN endpoints
26	Reserved	Reserved, must be kept at reset value
25:17	RXTHRLEN[8:0]	Receive Threshold Length (RxThrLen) This field specifies Receive thresholding size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for

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Bit Field	Name	Description
		ThrLen is to be the same as the programmed AHB Burst Length（ USBHS_GAHBCFG. BURSTTYP [3:0]）。
16	RXTHREN	Receive Threshold Enable When this bit is set, the core enables thresholding in the receive direction.
15:11	Reserved	Reserved, must be kept at reset value
10:2	TXTHRLEN[8:0]	Transmit Threshold Length This field specifies Transmit thresholding size in DWORDS. This also forms the MAC threshold and specifies the amount of data in bytes to be in the corresponding endpoint transmit FIFO, before the core can start transmit on the USB. The threshold length has to be at least eight DWORDS when the value of AHBThrRatio is 2'h00. In case the AHBThrRatio is non zero the application needs to ensure that the AHB Threshold value does not go below the recommended eight DWORD. This field controls both isochronous and nonisochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length（USBHS_GAHBCFG. BURSTTYP [3:0]）.
1	ISOINEPTHREN	ISO IN Endpoints Threshold Enable. (ISOThrEn) When this bit is Set, the core enables thresholding for isochronous IN endpoints. ■ 0 (DISABLED): No thresholding ■ 1 (ENABLED): Enables thresholding for isochronous IN endpoints
0	NISOINEPTHREN	Non-ISO IN Endpoints Threshold Enable. When this bit is Set, the core enables thresholding for Non Isochronous IN endpoints. ■ 0 (DISABLED): No thresholding ■ 1 (ENABLED): Enable thresholding for non-isochronous IN

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Bit Field	Name	Description
		endpoints

40.11.4.9 USBHS Device IN Endpoint FIFO Empty Interrupt Mask Register （USBHS_DINEPFEINTEN）

Address offset：0x0834

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INEPTXFEIEN[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value
15:0	INEPTXFEIEN [15:0]	IN EP Tx FIFO Empty Interrupt Mask Bits (InEpTxfEmpMsk) These bits acts as mask bits for DIEPINTn.TxFEmp interrupt, one bit per IN Endpoint: Bit 0 for IN EP 0, bit 7 for IN EP 7 0：mask 1：nomask

40.11.4.10 USBHS Device Each Endpoints Interrupt Register（USBHS_DEEPINTSTS）

Address offset：0x0838

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								OUTEP INT7	OUTEP INT6	OUTEP INT5	OUTEP INT4	OUTEP INT3	OUTEP INT2	OUTEP INT1	OUTEP INT0
								r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								INEPINT7	INEPINT6	INEPINT5	INEPINT4	INEPINT3	INEPINT2	INEPINT1	INEPINT0
								r	r	r	r	r	r	r	r

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Bit Field	Name	Description
31:25	Reserved	Reserved, must be kept at reset value
24:16	OUTEPINT[8:0]	Device OUT endpoint interrupt status Each bit represents an OUT endpoint: Bit16 represents OUT endpoint 0, Bit24 represents OUT endpoint 8.
15:8	Reserved	Reserved, must be kept at reset value
7:0	INEPINT[8:0]	Device IN endpoint interrupt status. Each bit represents an IN endpoint: Bit0 represents IN endpoint 0, Bit8 represents IN endpoint 8.

40.11.4.11 USBHS Device Each Endpoints Interrupt Enable Register（USBHS_DEEPINTEN）

Address offset：0x083C

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								OUTEP IEN7	OUTEP IEN6	OUTEP IEN5	OUTEP IEN4	OUTEP IEN3	OUTEP IEN2	OUTEP IEN1	OUTEP IEN0
								rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								INEPIEN7	INEPIEN6	INEPIEN5	INEPIEN4	INEPIEN3	INEPIEN2	INEPIEN1	INEPIEN0
								rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:25	Reserved	Reserved, must be kept at reset value
24:16	OUTEPIEN[15:9]	Device OUT endpoint interrupt enable. Each bit represents an OUT endpoint: Bit16 represents OUT endpoint 0, Bit24 represents OUT endpoint 15. The interrupt entry for generating interrupts is USBHS_EP_OUT.
15:8	Reserved	Reserved, must be kept at reset value
7:0	INEPIEN [8:0]	Device IN endpoint interrupt enable.

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Bit Field	Name	Description
		Each bit represents an IN endpoint: Bit0 represents IN endpoint 0, Bit8 represents IN endpoint 8. The interrupt entry for generating interrupts is USBHS_EP_OUT.

40.11.4.12 USBHS Device Each IN Endpoint Interrupt Register（USBHS_DINEPxINTEN）(x=[0..8])

Address offset：0x0840 + x×4

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		NAKIEN	Reserved				TXFUDIEN	Reserved	INEPNAKEIEN	INTREPMSIEN	TXFERINTKIEN	TOIEN	AHBERRIEN	EPDISIEN	TXCIEN
		rw					rw		rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, must be kept at reset value
13	NAKIEN	NAK interrupt Mask ■ 0 (MASK): Mask NAK Interrupt ■ 1 (NOMASK): No NAK Interrupt Mask
12:9	Reserved	Reserved, must be kept at reset value
8	TXFUDIEN	Fifo Underrun Mask ■ 0 (MASK): Mask Fifo Underrun Interrupt ■ 1 (NOMASK): No Fifo Underrun Interrupt Mask
7	Reserved	Reserved, must be kept at reset value
6	INEPNAKEIEN	IN Endpoint NAK Effective Mask ■ 0(MASK): Mask IN Endpoint NAK Effective ■ 1 (NOMASK): No IN Endpoint NAK Effective Mask

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Bit Field	Name	Description
5	INTREPMISIEN	IN Token received with EP Mismatch Mask ■ 0 (MASK): Mask IN Token received with EP Mismatch Interrupt ■ 1 (NOMASK): No Mask IN Token received with EP Mismatch Interrupt
4	TXFERINTKIEN	IN Token Received When TxFIFO Empty Mask ■ 0 (MASK): Mask IN Token Received When TxFIFO Empty Interrupt ■ 1 (NOMASK): No IN Token Received When TxFIFO Empty Interrupt
3	TOIEN	Timeout Condition Mask (Non-isochronous endpoints) ■ 0 (MASK): Mask Timeout Condition Interrupt ■ 1 (NOMASK): No Timeout Condition Interrupt Mask
2	AHBERRIEN	AHB Error Mask ■ 0 (MASK): Mask AHB Error ■ 1 (NOMASK): No AHB Error Mask
1	EPDISIEN	Endpoint Disabled Interrupt Mask ■ 0 (MASK): Mask Endpoint Disabled Interrupt ■ 1 (NOMASK): No Endpoint Disabled Interrupt Mask
0	TXCIEN	Transfer Completed Interrupt Mask ■ 0 (MASK): Mask Transfer Completed Interrupt ■ 1 (NOMASK): No Transfer Completed Interrupt Mask

40.11.4.13 USBHS Device Each OUT Endpoint Interrupt Register（USBHS_DOUTEPxINTEN）(x=[0..8])

Address offset：0x0880 + x×4

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	NYETIEN	NAKIEN	BERRIEN	Reserved	OPERRIEN	Reserved	B2BSTUPIEN	Reserved	EPDISROTIEN	STUPDNEIEN	AHBERRIEN	EPDISIEN	TXCIEN
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:14	Reserved	Reserved, must be kept at reset value
14	NYETIEN	NYET interrupt Mask ■ 0 (MASK): Mask NYET Interrupt ■ 1 (NOMASK): No NYET Interrupt Mask
13	NAKIEN	NAK interrupt Mask ■ 0 (MASK): Mask NAK Response Received Interrupt ■ 1 (NOMASK): No NAK Response Received Interrupt Mask
12	BERRIEN	Babble Error interrupt Mask ■ 0 (MASK): Mask Babble Error Interrupt ■ 1 (NOMASK): No Babble Error Interrupt Mask
11:9	Reserved	Reserved, must be kept at reset value
8	OPERRIEN	OUT Packet Error Mask ■ 0 (MASK): Mask OUT Packet Error Interrupt ■ 1 (NOMASK): No OUT Packet Error Interrupt Mask
7	Reserved	Reserved, must be kept at reset value
6	B2BSTUPIEN	Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only. ■ 0 (MASK): Mask Back-to-Back SETUP Packets Received ■ 1 (NOMASK): No Back-to-Back SETUP Packets Received Mask
5	Reserved	Reserved, must be kept at reset value
4	EPDISROTIEN	OUT Token Received when Endpoint Disabled Mask Applies to control OUT endpoints only. ■ 0 (MASK): Mask OUT Token Received when Endpoint Disabled Interrupt

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Bit Field	Name	Description
		■ 1 (NOMASK): No OUT Token Received when Endpoint Disabled Interrupt Mask
3	STUPDNEIEN	SETUP Phase Done Mask Applies to control endpoints only. ■ 0 (MASK): Mask SETUP Phase Done Interrupt ■ 1 (NOMASK): No SETUP Phase Done Interrupt Mask
2	AHBERRIEN	AHB Error ■ 0 (MASK): AHB Error Mask ■ 1 (NOMASK): No AHB Error Mask
1	EPDISIEN	Endpoint Disabled Interrupt Mask ■ 0 (MASK): Mask Endpoint Disabled Interrupt ■ 1 (NOMASK): No Endpoint Disabled Interrupt Mask
0	TXCIEN	Transfer Completed Interrupt Mask ■ 0 (MASK): Transfer Completed Mask ■ 1 (NOMASK): No Transfer Completed Mask

40.11.4.14 USBHS Device Control IN Endpoint 0 Control Register（USBHS_DINEP0CTRL）

Address offset：0x0900

Reset value：0x0000 8000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPEN	EPDIS	Reserved		SNAK	CNAK	TXFNUM[3:0]				STALL	Reserved	EPTYPE[1:0]		NAKSTS	Reserved
rs	Rs			w	w	rw				rs		r		r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPACT	Reserved													MPLEN[1:0]	
r														rw	

Bit Field	Name	Description
31	EPEN	Endpoint Enable The application sets this bit to 1 to initiate data transmission on the

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Bit Field	Name	Description
		endpoint. The module clears this bit before triggering any of the following interrupts on this endpoint: – SETUP completed –Endpoint Disabled –Transfer Completed ■ 0 (INACTIVE): No action ■ 1 (ACTIVE): Enable Endpoint
30	EPDIS	Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must Set this bit only if Endpoint Enable is already set for this endpoint. ■ 0 (INACTIVE): No action ■ 1 (ACTIVE): Disabled Endpoint
29:28	Reserved	Reserved, must be kept at reset value
27	SNAK	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.
26	CNAK	Clear NAK A write to this bit clears the NAK bit for the endpoint.
25:22	TXFNUM[3:0]	TxFIFO Number Define the TX FIFO number for the IN endpoint.
21	STALL	STALL Handshake The application can only set this bit, and the core clears it, when a

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Bit Field	Name	Description
		SETUP token is received for this endpoint. If a NAK bit, Global Nonperiodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.
20	Reserved	Reserved, must be kept at reset value
19:18	EPTYPE[1:0]	Endpoint Type（For endpoint 0, this bit field is fixed at 00.） 00：control 01：Synchronization 10：Bulk 11：interruupt
17	NAKSTS	NAK Status Indicates the following: ■ 0: The core is transmitting non-NAK handshakes based on the FIFO status ■ 1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core: - Stop receiving any data on the OUT endpoint - For asynchronous IN endpoints: Even if there is available data in the TX FIFO, the module will stop sending any data through the IN endpoint. - For synchronous IN endpoints: Even if there is available data in the TX FIFO, the module will send data packets with zero length. Regardless of how this bit is set, the module always responds to SETUP data packets with an ACK handshake.
16	Reserved	Reserved, must be kept at reset value
15	EPACT	USB Active Endpoint This bit is always SET to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.
14:2	Reserved	Reserved, must be kept at reset value
1:0	MPLEN[1:0]	Maximum Packet Size

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Bit Field	Name	Description
		Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. ■ 2'b00: 64 bytes ■ 2'b01: 32 bytes ■ 2'b10: 16 bytes ■ 2'b11: 8 bytes

40.11.4.15 USBHS Device Each IN Endpoint Interrupt Register（USBHS_DINEPxCTRL）(x=[1..8])

Address offset：0x0900 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPEN	EPDIS	Reserved		SNAK	CNAK	TXFNUM[3:0]				STALL	Reserved	EPTYPE[1:0]		NAKSTS	Reserved
rs	rs			w	w	rw				rs		rw		r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPACT	Reserved					MPLEN[10:0]									
rw						rw									

Bit Field	Name	Description
31	EPEN	Endpoint Enable The application sets this bit to 1 to initiate data transmission on the endpoint. The module clears this bit before triggering any of the following interrupts on this endpoint: – SETUP completed –Endpoint Disabled –Transfer Completed ■ 0 (INACTIVE): No action ■ 1 (ACTIVE): Enable Endpoint

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Bit Field	Name	Description
30	EPDIS	Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must Set this bit only if Endpoint Enable is already set for this endpoint. ■ 0 (INACTIVE): No action ■ 1 (ACTIVE): Disabled Endpoint
29	SD1PID	Set DATA1 PID (applicable to interrupt and bulk IN endpoints) Software sets this bit to set the DPID bit of the register.
	SODDFRM	Set odd frame (applicable to synchronous IN endpoints) Software sets this bit to set the EOFRM bit of the register.
28	SD0PID	Set DATA0 PID (applicable to interrupt and bulk IN endpoints) Software sets this bit to clear the DPID bit of the register.
	SEVNFRM	Set even frame (applicable to synchronous IN endpoints) Software sets this bit to clear the EOFRM bit of the register.
27	SNAK	Set NAK. The application sets this bit to control the transmission of NAK handshake signal on the endpoint. After receiving a SETUP on the endpoint, the module will also set this bit to 1.
26	CNAK	Clear NAK. Writing to this bit will clear the NAK bit of the endpoint.
25:22	TXFNUM[3:0]	Tx FIFO number. Define the TX FIFO number for the IN endpoint.
21	STALL	STALL handshake When used for non-control, non-synchronous IN endpoints (access type rw): The application sets this bit to 1 to make the device respond

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Bit Field	Name	Description
		with STALL to all tokens from the USB host. If the NAK bit, global IN NAK, or global OUT NAK are set simultaneously with this bit, the STALL bit takes priority. When used for control endpoints (access type rs): The application can only write to this bit, and after receiving a SETUP token, USBHS clears this bit. If the NAK bit, global IN NAK, or global OUT NAK are set simultaneously with this bit, the STALL bit takes priority. Regardless of how this bit is set, the module always responds to SETUP data packets with an ACK handshake.
20	Reserved	Reserved, must be kept at reset value
19:18	EPTYPE[1:0]	Endpoint Type（For endpoint 0, this bit field is fixed at 00.） 00：control 01：Synchronization 10：Bulk 11：interruupt
17	NAKSTS	NAK Status Indicates the following: ■ 0: The core is transmitting non-NAK handshakes based on the FIFO status ■ 1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core: Stop receiving any data on the OUT endpoint For asynchronous IN endpoints: Even if there is available data in the TX FIFO, the module will stop sending any data through the IN endpoint. For synchronous IN endpoints: Even if there is available data in the TX FIFO, the module will send data packets with zero length. Regardless of how this bit is set, the module always responds to SETUP data packets with an ACK handshake.
16	EOFRM	Odd/Even frame (applicable to synchronous OUT endpoints) For synchronous transfers, software controls USBHS to send data packets to OUT transactions only in odd or even frames by using this

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Bit Field	Name	Description
		bit. If the parity of the current frame number does not match this bit, USBHS does not store the data packet. 0：Send data only in even frames. 1：Send data only in odd frames.
	DPID	Endpoint data PID (applicable to interrupt or bulk endpoints) In endpoint or bulk transfers, there is a data PID flipping mechanism. Before the transfer starts, software sets this bit by setting SD0PID. According to the data PID flipping mechanism described in the USB protocol, USBHS maintains this bit during the transfer process.。 0：The data packet PID is DATA0. 1：The data packet PID is DATA1.
15	EPACT	USB active endpoint It indicates whether this endpoint is active in the current configuration and interface. After detecting a USB reset, the module clears this bit for all endpoints (except endpoint 0). Upon receiving SetConfiguration and SetInterface commands, the application must program the endpoint registers accordingly and set this bit to 1.
14:11	Reserved	Reserved, must be kept at reset value
10:0	MPLEN	Maximum packet length It defines the maximum packet length of the current logical endpoint data packets, this value is in bytes.

40.11.4.16 USBHS Device Each IN Endpoint Interrupt Register（USBHS_DINEPxINTSTS）(x=[0..8])

Address offset：0x0908 + x×20

Reset value：0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	NYETIF	NAKIF	BBERRIF	PKDRPSTS	Reserved		TXFUDRIF	TXFEIF	INEPNAKEIF	INEPMISIF	TXFERINTIF	TOUTIF	AHBERRIF	EPDISIF	TXCIF
	rc_w1	rc_w1	rc_w1	rc_w1			rc_w1	r	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

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Bit Field	Name	Description
31:15	Reserved	Reserved, must be kept at reset value
14	NYETIF	NYET Interrupt The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. ■ 0 (INACTIVE): No interrupt ■ 1 (ACTIVE): NYET Interrupt
13	NAKIF	NAK Interrupt The core generates this interrupt when a NAK is transmitted or received by the device. <brIn case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. ■ 0 (INACTIVE): No interrupt ■ 1 (ACTIVE): NAK Interrupt
12	BBERRIF	NAK Interrupt The core generates this interrupt when babble is received for the endpoint.
11	PKDRPSTS	Packet Drop Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt.
10:9	Reserved	Reserved, must be kept at reset value
8	TXFUDRIF	Fifo Underrun Applies to IN endpoints only. The core generates this interrupt when it detects a transmit FIFO underrun condition in threshold mode for this endpoint.

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Bit Field	Name	Description
		■ 0 (INACTIVE): No Fifo Underrun interrupt ■ 1 (ACTIVE): Fifo Underrun interrupt
7	TXFEIF	Transmit FIFO Empty When the TX FIFO is half-empty or completely empty, this flag is set. The TX FIFO empty threshold is determined by USBHS_GAHBCFG.NPTXFETH.
6	INEPNAKEIF	IN Endpoint NAK Effective Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.
5	INEPMISIF	IN Token Received with EP Mismatch Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.
4	TXFERINTIF	IN Token Received When TxFIFO is Empty Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. ■ 0 (INACTIVE): No IN Token Received when TxFIFO Empty interrupt

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Bit Field	Name	Description
		■ 1 (ACTIVE): IN Token Received when TxFIFO Empty Interrupt
3	TOUTIF	Timeout Condition ■ In shared TX FIFO mode, applies to non-isochronous IN endpoints only. ■ In dedicated FIFO mode, applies only to Control IN endpoints. ■ In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.
2	AHBERRIF	AHB Error ■ 0 (INACTIVE): No AHB Error Interrupt ■ 1 (ACTIVE): AHB Error interrupt
1	EPDISIF	Endpoint Disabled Interrupt Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.
0	TXCIF	Transfer Completed Interrupt ■ 0 (INACTIVE): No Transfer Complete Interrupt ■ 1 (ACTIVE): Transfer Completed Interrupt

40.11.4.17 USBHS Device IN Endpoint 0 Transfer Size Register（USBHS_DINEP0TXSIZ）

Address offset：0x0910

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											PKTCNT[1:0]		Reserved		
											rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									TLEN[6:0]						
									rw						

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Bit Field	Name	Description
31:21	Reserved	Reserved, must be kept at reset value
20:19	PKTCNT[1:0]	Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. ■ IN Endpoints : This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. ■ OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.
18:7	Reserved	Reserved, must be kept at reset value
6:0	TLEN[6:0]	Transfer Size This field contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet.

40.11.4.18 USBHS Device Each IN Endpoint Transfer Size Register（USBHS_DINEPxTXSIZ） (x=[1..8])

Address offset：0x0910 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	MCNT[1:0]		PKTCNT[9:0]										TLEN[18:16]		
	rw		rw										rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLEN[15:0]															
rw															

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Bit Field	Name	Description
31:21	Reserved	Reserved, must be kept at reset value
30:29	MCNT[1:0]	Multi-packet count. This field describes the number of packets that need to be transmitted within one frame. 01: 1 packet 10: 2 packets 11: 3 packets
28:19	PKTCNT[9:0]	Packet count It indicates the number of data packets included in one data transfer of endpoint x. This field will decrement each time a data packet (maximum size packet or short packet) is read from the TX FIFO.
18:0	TLEN[18:0]	Transfer size It indicates the amount of data included in one data transfer of endpoint x, in bytes. The module interrupts the application only after the application has transmitted this data. The transfer size can be set to the maximum data packet size of the endpoint, interrupting at the end of each data packet. The module decrements this field each time a data packet from external memory is written to the TX FIFO.

40.11.4.19 USBHS Device Each IN Endpoint DMA Address Register（USBHS_DINEPxDMADD）(x=[0..8])

Address offset：0x0914 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMADD[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMADD[15:0]															
rw															

Bit Field	Name	Description
31:0	DMADD	DMAAddr

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Bit Field	Name	Description
		This field holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten.

40.11.4.20 USBHS Device Each IN Endpoint Transmit FIFO Status Register（USBHS_DINEPxTXFSTS）(x=[0..8])

Address offset：0x0918 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INEPTXFSPCAVL[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value
15:0	TXFSPCAVL[15:0]	IN Endpoint TxFIFO Space Avail Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. ■ 16'h0: Endpoint TxFIFO is full ■ 16'h1: 1 word available ■ 16'h2: 2 words available ■ 16'hn: n words available

40.11.4.21 USBHS Device Control OUT Endpoint 0 Control Register（USBHS_DOUTEP0CTRL）

Address offset：0x0B00

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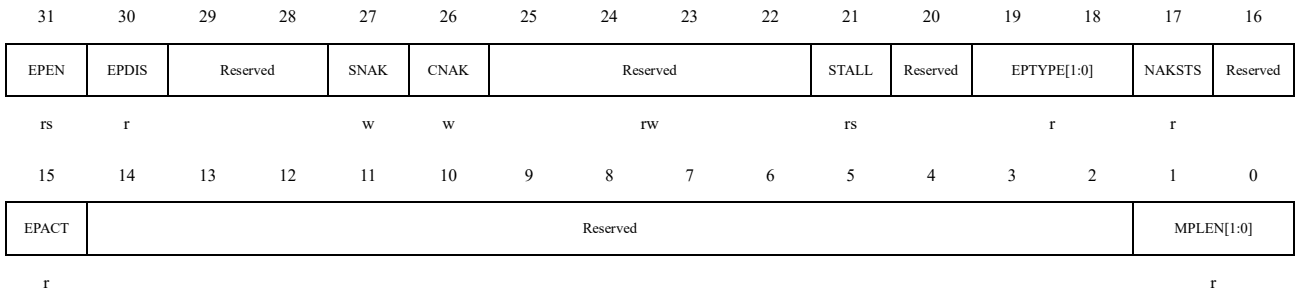
Reset value：0x0000 8000



Bit Field	Name	Description
31	EPEN	Endpoint Enable The application sets this bit to 1 to initiate data transmission on the endpoint. The module clears this bit before triggering any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Complete ■ 0 (INACTIVE): No action ■ 1 (ACTIVE): Enable Endpoint
30	EPDIS	Endpoint Disable The application cannot disable control OUT endpoint 0.
29:28	Reserved	Reserved, must be kept at reset value
27	SNAK	Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	CNAK	Clear NAK A write to this bit clears the NAK bit for the endpoint.
25:22	Reserved	Reserved, must be kept at reset value

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Bit Field	Name	Description
21	STALL	STALL Handshake The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is Set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
20	Reserved	Reserved, must be kept at reset value
19:18	EPTYPE[1:0]	Endpoint Type (EPType)（Hardcoded to 2'b00 for control.） 00：control 01：Synchronization 10：Bulk 11：interruupt
17	NAKSTS	NAK Status Indicates the following: ■ 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. ■ 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even If there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	Reserved	Reserved, must be kept at reset value
15	EPACT	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.
14:2	Reserved	Reserved, must be kept at reset value

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Bit Field	Name	Description
1:0	MPLEN[1:0]	Maximum Packet Size The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. ■ 2'b00: 64 bytes ■ 2'b01: 32 bytes ■ 2'b10: 16 bytes ■ 2'b11: 8 bytes

40.11.4.22 USBHS Device Each OUT Endpoint Control Register（USBHS_DOUTEPxCTRL）(x=[1..8])

Address offset：0x0B00 + x×20

Reset value：0x0000 8000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EPEN	EPDIS	SD1PID/ SODDFRM	SD0PID/ SEVNFRM	SNAK	CNAK	Reserved				STALL	Reserved	EPTYPE[1:0]		NAKSTS	EPDPID/ EPEOFRM
rs	rs	w	w	w	w					rs		rw		r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPACT	Reserved					MPLEN[10:0]									
rw						rw									

Bit Field	Name	Description
31	EPEN	Endpoint Enable The application sets this bit to 1 to initiate data transmission on the endpoint. The module clears this bit before triggering any of the following interrupts on this endpoint: - SETUP Phase Done - Endpoint Disabled - Transfer Complete ■ 0 (INACTIVE): No action ■ 1 (ACTIVE): Enable Endpoint
30	EPDIS	Endpoint Disable

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Bit Field	Name	Description
		The application cannot disable control OUT endpoint 0.
29	SD1PID	Set DATA1 PID Applicable to interrupt/bulk IN and OUT endpoints, writing to this bit will set the endpoint data PID (DPID) field in this register to DATA1.
	SODDFRM	Set odd frame Applicable only to synchronous IN and OUT endpoints. Software sets this bit to set the EPEOFRM bit of this register, setting it to an odd frame.
28	SD0PID	Set DATA0 PID Applicable to interrupt/bulk IN and OUT endpoints, writing to this bit will set the endpoint data PID (DPID) field in this register to DATA0.
	SEVNFRM	Set even frame Applicable only to synchronous IN and OUT endpoints. Software sets this bit to clear the EPEOF bit of this register, setting it to an even frame.
27	SNAK	Set NAK. The application sets this bit to control the transmission of NAK handshake signal on the endpoint. The module will also set this bit to 1 after receiving a SETUP on the endpoint.
26	CNAK	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.
25:22	Reserved	Reserved, must be kept at reset value
21	STALL	STALL Handshake The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is Set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake
20	Reserved	Reserved, must be kept at reset value

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Bit Field	Name	Description
19:18	EPTYPE[1:0]	Endpoint Type (EPType)（Hardcoded to 2'b00 for control.） 00：control 01：Synchronization 10：Bulk 11：interruupt
17	NAKSTS	NAK Status Indicates the following: ■ 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. ■ 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even If there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	EPDPID	Endpoint data packet PID Applicable to interrupt/bulk IN and OUT endpoints, indicates the data packet PID currently received/transmitted by the endpoint. The application needs to program bit 29 and bit 28 of this register to set the PID of the first received/transmitted data packet.。 0：DATA0 1：DATA1
	EPEOFRM	Endpoint odd/even frame Applicable to synchronous IN and OUT endpoints, indicates the frame number of the data packet currently received/transmitted by the endpoint. The application needs to program bit 29 and bit 28 of this register to set the frame number of the first received/transmitted data packet. 0：even frame 1：Odd frame

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Bit Field	Name	Description
15	EPACT	USB active endpoint It indicates whether this endpoint is active in the current configuration and interface. Upon detecting a USB reset, the module clears this bit for all endpoints (except endpoint 0). After receiving SetConfiguration and SetInterface commands, the application must programmatically configure the endpoint registers accordingly and set this bit to 1.
14:11	Reserved	Reserved, must be kept at reset value
10:0	MPLEN	Maximum packet length It defines the maximum packet length of the current logical endpoint data packets, this value is in bytes.

40.11.4.23 USBHS Device Each OUT Endpoint Interrupt Register（USBHS_DOUTEPxINTSTS）(x=[0..8])

Address offset：0x0B08 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STUPPRXIF	NYETIF	NAKIF	BBERRIF	PKDRPSTS	Reserved		OUTPCKERRIF	Reserved	B2BSTUPRIF	STSPRXIF	OUTTRXEPDISIF	STUPPDNEIF	AHBERRIF	EPDISIF	TXCIF
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1			rc_w1		rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value
15	STUPPRXIF	Setup Packet Received Applicable for Control OUT Endpoints in only in the Buffer DMA Mode Set by the controller, this bit indicates that this buffer holds 8 bytes

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Bit Field	Name	Description
		of setup data. There is only one Setup packet per buffer. On receiving a Setup packet, the controller closes the buffer and disables the corresponding endpoint. The application has to reenable the endpoint to receive any OUT data for the Control Transfer and reprogram the buffer start address. Note: Because of the above behavior, the controller can receive any number of back to back setup packets and one buffer for every setup packet is used. ■ 0: No Setup packet received ■ 1: Setup packet received
14	NYETIF	NYET Interrupt The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint. ■ 0 (INACTIVE): No NYET interrupt ■ 1 (ACTIVE): NYET Interrupt
13	NAKIF	NAK Interrupt The core generates this interrupt when a NAK is transmitted or received by the device. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo. ■ 0 (INACTIVE): No NAK interrupt ■ 1 (ACTIVE): NAK Interrupt
12	BBERRIF	NAK Interrupt The core generates this interrupt when babble is received for the endpoint.
11	PKDRPSTS	Packet Drop Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and

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Bit Field	Name	Description
		does not generate an interrupt
10:9	Reserved	Reserved, must be kept at reset value
8	OUTPCKERRIF	OUT Packet Error Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error for non-Isochronous OUT packet.
7	Reserved	Reserved, must be kept at reset value
6	B2BSTUPRIF	Back-to-Back SETUP Packets Received Applies to Control OUT endpoints only. This bit indicates that the core has received more than three backto-back SETUP packets for this particular endpoint. For information about handling this interrupt,
5	STSPRXIF	Status Phase Received for Control Write This interrupt is valid only for Control OUT endpoints. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase.
4	OUTTRXEPDISIF	OUT Token Received When Endpoint Disabled Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.

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Bit Field	Name	Description
3	STUPPDNEIF	SETUP Phase Done Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
2	AHBERRIF	AHB Error ■ 0 (INACTIVE): No AHB Error Interrupt ■ 1 (ACTIVE): AHB Error interrupt
1	EPDISIF	Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request. ■ 0 (INACTIVE): No Endpoint Disabled Interrupt ■ 1 (ACTIVE): Endpoint Disabled Interrupt
0	TXCIF	Transfer Completed Interrupt Applies to IN and OUT endpoints. Values: ■ 0 (INACTIVE): No Transfer Complete Interrupt ■ 1 (ACTIVE): Transfer Complete Interrupt

40.11.4.24 USBHS Device OUT Endpoint 0 Transfer Size Register（USBHS_DOUTEP0TXSIZ）

Address offset：0x0B10

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	STUPPCNT[1:0]		Reserved									PKTCNT	Reserved		
	rw														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									TLEN[6:0]						
									rw						

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Bit Field	Name	Description
31	Reserved	Reserved, must be kept at reset value
30:29	STUPPCNT[1:0]	SETUP Packet Count This field specifies the number of back-to-back SETUP data packets the endpoint can receive. ■ 2'b01: 1 packet ■ 2'b10: 2 packets ■ 2'b11: 3 packets
28:20	Reserved	Reserved, must be kept at reset value
19	PKTCNT[1:0]	Packet Count (PktCnt) This field is decremented to zero after a packet is written into the RxFIFO.
18:7	Reserved	Reserved, must be kept at reset value
6:0	TLEN[6:0]	Transfer Size Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

40.11.4.25 USBHS Device Each OUT Endpoint Transfer Size Registe （USBHS_DOUTEPxTXSIZ）(x=[1..8])

Address offset：0x0B10 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	RXDPID[1:0]/ STUPPCNT[1:0]		PKTCNT[9:0]										TLEN[18:16]		
	rw		rw										rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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TLEN[15:0]

rw

Bit Field	Name	Description
31:21	Reserved	Reserved, must be kept at reset value
30:29	RXDPID[1:0]	Received data PID Applicable to synchronous OUT endpoints. This is the PID of the last data packet received by this endpoint. 00：DATA0 01：DATA2 10：DATA1 11：MDATA
	STUPPCNT[1:0]	SETUP Packet Count This field specifies the number of back-to-back SETUP data packets the endpoint can receive. ■ 2'b01: 1 packet ■ 2'b10: 2 packets ■ 2'b11: 3 packets
28:19	PKTCNT[9:0]	Packet count It indicates the number of data packets included in one data transfer of endpoint x. This field will decrement each time a data packet (maximum size packet or short packet) is written to the RX FIFO.
18:0	TLEN[18:0]	Transfer size It indicates the amount of data included in one data transfer of endpoint x, in bytes. The module interrupts the application only after the application has transmitted this data. The transfer size can be set to the maximum data packet size of the endpoint, interrupting at the end of each data packet. This field decrements each time data is read from the RX FIFO and written to external memory.

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40.11.4.26 USBHS Device OUT Endpoint 0 DMA Address Register （USBHS_DOUTEPxDMADD）(x=[0..8])

Address offset：0x0B14 + x×20

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMADD[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMADD[15:0]															
rw															

Bit Field	Name	Description
31:0	DMADD	DMA address This field defines the DMA start address for the endpoint. DMA uses this address to fetch packet data for IN endpoints or write packet data for OUT endpoints.

40.11.5 USBHS Power control register

40.11.5.1 USBHS Power and Clock Gating Control Register（USBHS_PWRCTRL）

Address offset：0x0E00

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DSLEEP	PHY SLEEP	Reserved		PDMRST	Reserved	GATE HCLK	PHYSTP
								r	r			rw	rw	rw	rw

Bit Field	Name	Description
31:8	Reserved	Reserved, must be kept at reset value

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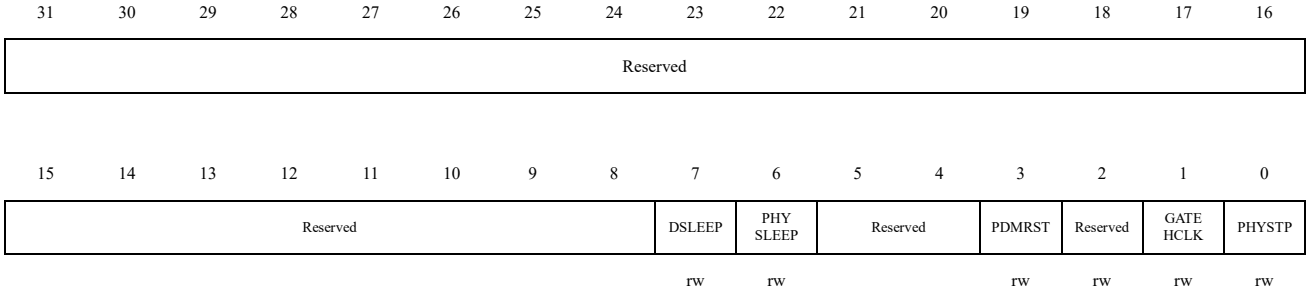
Bit Field	Name	Description
7	DSLEEP	Deep Sleep Indicates that the PHY is in deep sleep when in L1 state.
6	PHYSLEEP	PHY In Sleep Indicates that the PHY is in Sleep State.
5:4	Reserved	Reserved, must be kept at reset value
3	PDMRST	Reset Power-Down Modules This bit is valid only in Partial Power-Down mode. ■ 0 (ON): Power is turned on ■ 1 (OFF): Power is turned off
2	Reserved	Reserved, must be kept at reset value
1	GATEHCLK	Stop Gate HCLK When USBHS is in suspend or session invalid state, the application can set this bit to 1 to stop providing clock to modules other than the AHB bus interface, host interface, and wakeup logic. When USBHS resumes communication or a new session starts, the application clears this bit.
0	PHYSTP	Stop PHY clock When USBHS is in suspend state, session invalid state, or the device is disconnected, the application can set this bit to 1 to stop the PHY clock. When USB resumes or a new session starts, the application clears this bit.

40.11.5.2 USBHS Power and Clock Gating Control Register1（USBHS_PWRCTRL1）

Address offset：0x0E04

Reset value：0x0000 0000



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Bit Field	Name	Description
31:4	Reserved	Reserved, must be kept at reset value
3	RAMCLKEN	RAM Clock Gating Enable The application programs this bit to enable RAM Clock Gating in the ACG feature. ■ 0: Disable RAM Clock Gating (Default) ■ 1: Enable RAM Clock Gating
2:1	CNT[1:0]	Count to Gate Clock Gate clock count indicates to the Controller how many PHY Clock cycles and AHB Clock cycles of 'IDLE' (no activity) the Controller wait for before Gating the respective PHY and AHB clocks internal to the Controller. 00: 64 clocks (Default). 01: 128 clocks
0	GATEN	Enable Active Clock Gating The application programs this bit to enable Active Clock Gating feature for the PHY and AHB clocks. 0: Disable Active Clock Gating (Default) 1: Enable Active Clock Gating

40.11.6 USBHS Wrapper control register

USBHS1 Wrapper control register base address: 0x4014 0000

USBHS2 Wrapper control register base address: 0x400A 0000

40.11.6.1 USBHS Wrapper Control Register（USBHS_WRPCTRL）

Address offset：0x0000

Reset value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										LSCHGEN	SUSPWKEN	IDDETEN	HDISCEN	VBRM DETEN	PINDET EN
										rw	rw	rw	rw	rw	rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bit Field	Name	Description
31:22	Reserved	Reserved, must be kept at reset value
21	LSCHGEN	LineState Change Detection Enable This bit is to enable LineState Change Detection as one of waking up the SCLK clock sources. When the PHY is in Suspend state, and before the system turns off the SCLK, setting this bit to "1" enables the detection. The wakeup signal is asserted when the event is detected, so that it wakes up the SCLK. Once the SCLK is restored this bit should be set back to "0".
20	SUSPWKEN	Suspend De-assert Detect Enable This bit is to enable Suspend De-assertion Detection as one of waking up the SCLK clock sources. When the controller is in Suspend state, and before the system turns off the SCLK, setting this bit to "1" enables the detection. The wakeup signal is asserted when the event is detected, so that it wakes up the SCLK clock. Once the SCLK is restored this bit should be set back to "0". Note: This function will only work if the de-assertion of suspend does not require the SCLK present. Otherwise, this function will not work.
19	IDDETEN	Host Role ID Detect Enable This bit is to enable Host Role Detection on the ID PAD as one of waking up the SCLK clock sources. When the system is going to enter Low Power mode, and before the system turns off the SCLK, setting this bit to "1" enables the detection. Once the SCLK is restored this bit should be set back to "0".
18	HDISCEN	Host Disconnect Detection Enable This bit is to enable Host Disconnect Detection as one of waking up the SCLK clock sources. It has to be in HOST mode, and it is in suspend state. When the system is going to enter Low Power mode, and before the system turns off the SCLK, setting this bit to "1" enables the detection. Once the SCLK is restored this bit should be set back to "0".

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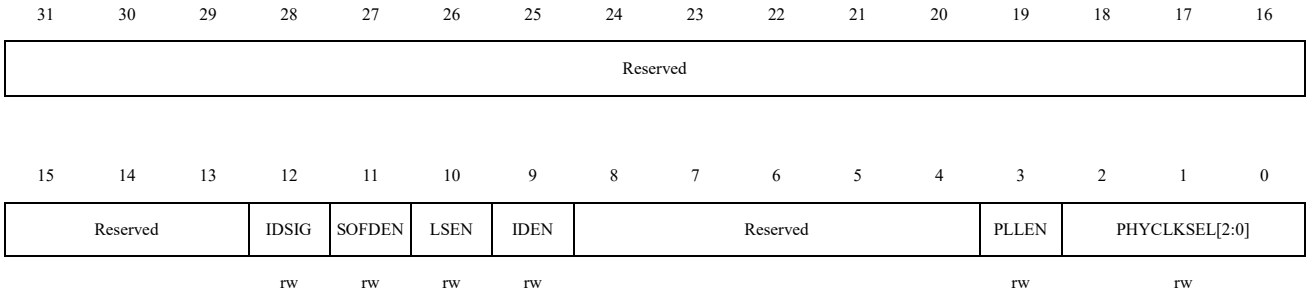
Bit Field	Name	Description
17	VBRMDETEN	VBUS Removal Detection Enable This bit is to enable VBUS Removal Detection as one of waking up the SCLK clock sources. When the system is going to enter Low Power mode, and before the system turns off the SCLK, setting this bit to "1" enables the detection. Once the SCLK is restored this bit should be set back to "0".
16	PINDETEN	Host Plug-In Detection Enable This bit is to enable Host Plug-In Detection as one of waking up the SCLK clock sources. When the system is going to enter Low Power mode, and before the system turns off the SCLK, setting this bit to "1" enables the detection. Once the SCLK is restored this bit should be set back to "0".
15:0	Reserved	Reserved

40.11.6.2 USBHS Wrapper Configuration Register（USBHS_WRPCFG）

Address offset：0x0004

Reset value：0x0000 0000



Bit Field	Name	Description
31:13	Reserved	Reserved
12	IDSIG	When IDEN=0, this register is used, else unused. 1: Set Internal id digital signal = 1 0: Set Internal id digital signal = 0
11	SOFDEN	USB SOF detection enable bit. 1: To enable SOF detection and its output. SOF pulse is output to USB_SOF port, and its pulse width is 20 hclk period.

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Bit Field	Name	Description
		0: SOF detection is disabled.
10	LSEN	Low Swing Control for USB2.0 Loopback Mode 0: Normal Swing (400mV) 1: Small Swing (355mV)
9	IDEN	ID Pin Enable This is ID Pin Enable bit. 1: ID Pin module is enabled. 0: ID Pin module is disabled.
8:4	Reserved	Reserved
3	PLLEN	Enable USB PHY PLL. Keeps the clock source alive in suspend mode. 0: PLLCK120 and PLLCK480 are inactive. 1: CLK48M, PLLCK120 and PLLCK480 are active.
2:0	PHYCLKSEL	PHY Source Clock Frequency Selection 000: 10Mhz 001: 12Mhz 010: 25Mhz 011: 30Mhz 100: 19.2Mhz 101: 24Mhz 110: 27Mhz 111: 40Mhz

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41 Flexible Data-rate Controller Area Network (FDCAN)

41.1 Introduction

Provide 8 FDCAN modules, compliant with ISO 11898-1:2015 standard, supporting CAN 2.0A/B and CAN FD protocols, compatible with Bosch protocol not based on ISO standard.

In addition, the CAN module FDCAN1&2&3&4 support time triggered CAN (TTCAN), specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1&2&3&4 contains additional registers, specific to the time triggered feature. The CANFD option can be used together with event-triggered and time-triggered CAN communication.

The 8 FDCAN modules share 2 message RAM areas, each FDCAN can freely select SRAM5 BANK1 or SRAM5 BANK2 used for receiving message filters, receive FIFO, receive buffer, transmit buffer, transmit event FIFO (and triggers for TTCAN). The message RAM is located in the internal SRAM of the MCU, with a configurable starting address and a maximum allocation of 4480 words (32-bit) to a single FDCAN.

41.2 Main Features

- Compliant with ISO 11898-1:2015 and ISO 11898-4 standards
- Support for CAN FD with up to 64 bytes of data
- Supports TTCAN Level 1 and Level 2 fully realized in hardware (FDCAN1/2/3/4 support only)
- Support for CAN error logging
- Support for AUTOSAR standard
- Support for SAE J1939 standard
- Enhanced receive filtering functionality
- Two configurable receive FIFOs
- Separate signaling for receiving high-priority messages
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO or queue
- Configurable transmit event FIFO
- Support for configurable message RAM shared by 8 FDCAN controllers
- Programmable loopback test mode
- Maskable module interrupts
- Two clock domains: CAN core clock and APB bus clock
- Support for Power-down mode

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

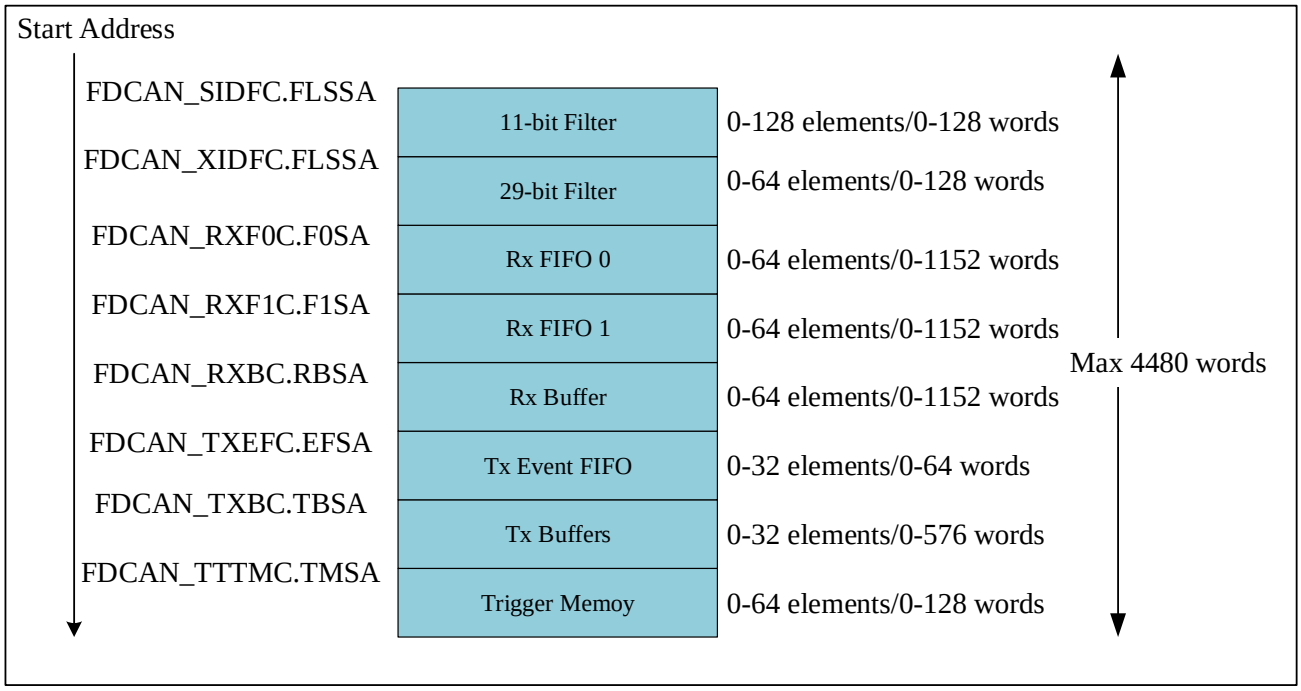
41.3 Message RAM

41.3.1 Message RAM Configuration

FDCAN supports a 32-bit Message RAM area, which includes receive filters, receive FIFOs, dedicated receive buffers, transmit buffer, transmit event FIFO (and triggers for TTCAN). Message RAM is located in general-purpose SRAM, with a configurable baseline address (FDCAN_TTSS.RAMSEL bit), supports per-word (32bit) access only, does not support byte access, up to 4,480 words can be allocated to a single FDCAN module, and 8 FDCAN modules share 2 message RAM areas(A single SRAM can be configured up to 4096 words, so in reality, a single FDCAN can be configured up to 4096 words). The structure of the Message RAM can be referred to in the following diagram.

Note: Message RAM is equipped with ECC functionality, it is recommended to initialize the Message RAM after hardware reset by writing e.g. 0x00000000 to each Message RAM word to create valid ECC checksums. This avoids that reading from uninitialized Message RAM sections will activate interrupt FDCAN_IR.BEC (Bit Error Corrected) or FDCAN_IR.BEU (Bit Error Uncorrected).

Figure 41-1 Example diagram of FDCAN Message RAM allocation



The various segments in the Message RAM are not mandatory, and there are no restrictions on their placement order. Users can configure them as needed. When operated in CAN FD mode the required Message RAM size strongly depends on the element size configured for Rx FIFO0, Rx FIFO1, Rx Buffers, and Tx Buffers via FDCAN_RXESC.F0DS, FDCAN_RXESC.F1DS, FDCAN_RXESC.RBDS, and FDCAN_TXESC.TBDS. The starting addresses configured in the registers are in word addresses, with the actual values written to the registers being the offsets of the starting addresses of each segment from the starting address of the Message RAM area.

Note: FDCAN does not check for errors in the configuration of the Message RAM. Therefore, extra caution must be taken when configuring the starting addresses and element counts of each segment to avoid data corruption or loss.

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41.3.2 Dedicated Receive Buffers and Receive FIFO

Each FDCAN module can configure up to 64 dedicated receive buffers and 2 receive FIFO areas in the Message RAM. The size of each receive FIFO can also be configured separately, with each able to store up to 64 received messages. The data field size of dedicated receive buffers and receive FIFO elements can be configured using the FDCAN_RXESC register, with a maximum of 64 bytes.

The data structure of receive buffers and FIFO elements is shown in the table below.

Table 41-1 Data Structure of Receive Buffers and Receive FIFO

word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	ESI	XTD	RTR	ID[28:0]																												
R1	ANMF	FIDX[6:0]							Reserved	FDF	BRS	DLC[3:0]					RXTS[15:0]															
R2	DB3[7:0]								DB2[7:0]								DB1[7:0]								DB0[7:0]							
R3	DB7[7:0]								DB6[7:0]								DB5[7:0]								DB4[7:0]							
...	...								...								...								...							
Rn	DBm[7:0]								DBm-1[7:0]								DBm-2[7:0]								DBm-3[7:0]							

Bit Field	Name	Description
R0 bit 31	ESI	Error State Indicator. 0: The sending node is in an active error state 1: The sending node is in a passive error state
R0 bit 30	XTD	Extended Identifier, indicating the received frame ID type. 0: 11-bit standard ID 1: 29-bit extended ID
R0 bit 29	RTR	Remote Transmission Request, indicating the received frame type. 0: Received frame is a data frame 1: Received frame is a remote frame Note: There are no remote frames in CAN FD format. In CAN FD frames (FDF = 1), the explicit bit RRS (Remote Request Substitute) replaces the RTR (Remote Transmission Request) bit.
R0 bit 28:0	ID[28:0]	Remote Transmission Request (Identifier (Identifier) standard ID or extended ID, depending on the XTD bit. When it is an 11-bit standard ID, store it left-aligned (ID[28:18]).
R1 bit 31	ANMF	Accept Non-matching Frame. can be enabled to accept non-matching frames by FDCAN_GFC.ANFS and FDCAN_GFC.ANFE. 0: Received frame matches filter index FIDX 1: Received frame does not match any receive filter elements
R1 bit 30:24	FIDX[6:0]	Filter Index. 0-127: Index of the receive filter element that matches the received frame (invalid when

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Bit Field	Name	Description
		ANMF = 1). Actual range is from 0 to FDCAN_SIDFC.LSS - 1 (standard frame) or FDCAN_XIDFC.LSE - 1 (extended frame).
R1 bit 21	FDF	FD Format 0: Typical CAN frame format 1: FDCAN frame format (new DLC encoding and CRC)
R1 bit 20	BRS	Bit Rate Switch 0: Do not switch bit rate when receiving frame 1: Switch bit rate when receiving frame
R1 bit 19:16	DLC[3:0]	Data Length Code. 0-8: CAN + CAN FD: Received frame contains 0-8 data bytes 9-15: CAN: Received frame contains 8 data bytes 9-15: CAN FD: Received frame contains 12/16/20/24/32/48/64 data bytes
R1 bit 15:0	RXTS[15:0]	Rx Timestamp Timestamp counter value captured at the start of receiving the frame. The resolution depends on the configuration of the timestamp counter pre-scaler FDCAN_TSCC.TCP.
R2 bit 31:24	DB3[7:0]	Data Byte 3 (Data Byte 3)
R2 bit 23:16	DB2[7:0]	Data Byte 2 (Data Byte 2)
R2 bit 15:8	DB1[7:0]	Data Byte 1 (Data Byte 1)
R2 bit 7:0	DB0[7:0]	Data Byte 0 (Data Byte 0)
R3 bit 31:24	DB7[7:0]	Data Byte 7 (Data Byte 7)
R3 bit 23:16	DB6[7:0]	Data Byte 6 (Data Byte 6)
R3 bit 15:8	DB5[7:0]	Data Byte 5 (Data Byte 5)
R3 bit 7:0	DB4[7:0]	Data Byte 4 (Data Byte 4)
…	…	…
Rn bit 31:24	DBm[7:0]	Data Byte m (Data Byte m)
Rn bit 23:16	DBm-1[7:0]	Data Byte m-1 (Data Byte m-1)
Rn bit 15:8	DBm-2[7:0]	Data Byte m-2 (Data Byte m-2)
Rn bit 7:0	DBm-3[7:0]	Data Byte m-3 (Data Byte m-3)

Note: Depending on the configuration of FDCAN_RXESC, the data field can occupy 2 to 16 bytes (Rn= 2..17).

41.3.3 Transmission Buffer

The transmission buffer can be configured as dedicated transmission buffer as well as transmission FIFO/transmission queue. If the transmission buffer is shared by dedicated transmission buffer and transmission FIFO/transmission queue, the dedicated transmission buffer is allocated first from the start address of the transmission buffer, and the remaining part is allocated to the transmission FIFO/transmission queue. The transmission processing unit distinguishes between dedicated transmission buffer and transmission FIFO/transmission queue based on the values of FDCAN_TXBC.TFQS and FDCAN_TXBC.NDTB. The size of transmission buffer and transmission FIFO/transmission queue elements can be configured, depending on the data field size, which can be configured up to 64 bytes using register FDCAN_TXESC.

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The data structure of dedicated transmission buffer and transmission FIFO/transmission queue elements is shown in the following table.

Table 41-2 Data Structure of Dedicated Transmission Buffer and Transmission FIFO/Queue

word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T0	ESI	XTD	RTR	ID[28:0]																												
T1	MM[7:0]								EFC	Reserved	FDF	BRS	DLC[3:0]				Reserved															
T2	DB3[7:0]								DB2[7:0]								DB1[7:0]								DB0[7:0]							
T3	DB7[7:0]								DB6[7:0]								DB5[7:0]								DB4[7:0]							
...	...								...								...								...							
Tn	DBm[7:0]								DBm-1[7:0]								DBm-2[7:0]								DBm-3[7:0]							

Bit Field	Name	Description
T0 bit 31	ESI	Error State Indicator. 0: In CAN FD frames, the ESI bit is solely dependent on the passive error flag 1: In CAN FD frames, the ESI bit will be sent recessive Note: The actual ESI bit sent is the result of a logical OR operation between the ESI written into the transmit buffer and the passive error flag. As per the requirements of the CAN FD protocol specification, active error nodes may choose to send the ESI bit recessive, but passive error nodes will always send the ESI bit recessive.
T0 bit 30	XTD	Extended Identifier. 0: 11-bit standard ID 1: 29-bit extended ID
T0 bit 29	RTR	Remote Transmission Request. 0: Send data frame 1: Send remote frame Note: When RTR = 1, even if CCCR.FDOE enables CAN FD format transmission, FDCAN will still send remote frames according to the ISO 11898-1:2015 standard.
T0 bit 28:0	ID[28:0]	Identifier. Standard ID or extended ID, depending on the XTD bit. When it is an 11-bit standard ID, store it left-aligned (ID[28:18]).
T1 bit 31:24	MM[7:0]	Message Marker. Written by the CPU when configuring the transmission buffer. Copied to the transmission event FIFO element to identify the transmission message status.
T1 bit 23	EFC	Event FIFO Control. 0: Do not store transmission events 1: Store transmission events
T1 bit 21	FDF	FD Format. 0: Send in typical CAN frame format 1: Send in CAN FD frame format
T1 bit 20	BRS	Bit Rate Switching.

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Bit Field	Name	Description
		0: Do not switch bit rate when sending CAN FD frames 1: Switch bit rate when sending CAN FD frames Note: ESI, FDF, and BRS bits are only valid when CAN FD is enabled (FDCAN_CCCR.FDOE = 1). Furthermore, BRS is only valid when FDCAN_CCCR.BRSE = 1.
T1 位 19:16	DLC[3:0]	Data Length Code. 0-8: CAN + CAN FD: Received frame contains 0-8 data bytes 9-15: CAN: Received frame contains 8 data bytes 9-15: CAN FD: Received frame contains 12/16/20/24/32/48/64 data bytes
T2 bit 31:24	DB3[7:0]	Data Byte 3 (Data Byte 3)
T2 bit 23:16	DB2[7:0]	Data Byte 2 (Data Byte 2)
T2 bit 15:8	DB1[7:0]	Data Byte 1 (Data Byte 1)
T2 bit 7:0	DB0[7:0]	Data Byte 0 (Data Byte 0)
T3 bit 31:24	DB7[7:0]	Data Byte 7 (Data Byte 7)
T3 bit 23:16	DB6[7:0]	Data Byte 6 (Data Byte 6)
T3 bit 15:8	DB5[7:0]	Data Byte 5 (Data Byte 5)
T3 bit 7:0	DB4[7:0]	Data Byte 4 (Data Byte 4)
…	…	…
Tn bit 31:24	DBm[7:0]	Data Byte m (Data Byte m)
Tn bit 23:16	DBm-1[7:0]	Data Byte m-1 (Data Byte m-1)
Tn bit 15:8	DBm-2[7:0]	Data Byte m-2 (Data Byte m-2)
Tn bit 7:0	DBm-3[7:0]	Data Byte m-3 (Data Byte m-3)

Note: Depending on the configuration of FDCAN_RXESC, the data field can occupy 2 to 16 bytes (Rn= 2..17).

41.3.4 Transmission Events FIFO

Each element stores information related to a sent message. By reading the transmission event FIFO, the host CPU can retrieve relevant information in the order of message transmission. The status information of the transmission event FIFO can be obtained from register FDCAN_TXEFS.

The data structure of transmission event FIFO elements is shown in the following table.

Table 41-3 Transmission Event FIFO Data Structure

word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E0	ESI	XTD	RTR	ID[28:0]																												
E1	MM[7:0]								ET[1:0]		FDF	BRS	DLC[3:0]				TXTS[15:0]															

Bit Field	Name	Description
E0 bit 31	ESI	Error State Indicator. 0: Sending node is in active error state 1: Sending node is in passive error state

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Bit Field	Name	Description
E0 bit 30	XTD	Extended Identifier. 0: 11-bit standard ID 1: 29-bit extended ID
E0 bit 29	RTR	Remote Transmission Request. 0: Send data frame 1: Send remote frame
E0 bit 28:0	ID[28:0]	Identifier. Standard ID or extended ID, depending on the XTD bit. When it is an 11-bit standard ID, store it left-aligned (ID[28:18]).
E1A/B bit 31:24	MM[7:0]	Message Marker. Copied from the transmission buffer to the transmission event FIFO element to identify the transmission message status.
E1A/B bit 23:22	ET[1:0]	Event Type. 00: Reserved 01: Transmission event 10: Transmit even after cancellation (must be set to this value when sending in DAR mode) 11: Reserve
E1A/B bit 21	FDF	FD Format. 0: Typical CAN frame format 1: FDCAN frame format (new DLC encoding and CRC
E1A/B bit 20	BRS	Bit Rate Switching. 0: Do not switch bit rate when sending CAN FD frames 1: Switch bit rate when sending CAN FD frames
E1A/B bit 19:16	DLC[3:0]	Data Length Code. 0-8: CAN + CAN FD: Received frame contains 0-8 data bytes 9-15: CAN: Received frame contains 8 data bytes 9-15: CAN FD: Received frame contains 12/16/20/24/32/48/64 data bytes
E1A bit 15:0	TXTS[15:0]	Tx Timestamp. Timestamp counter value captured at the start of sending the frame. The resolution depends on the configuration of the timestamp counter pre-scaler FDCAN_TSCC.TCP.

41.3.5 Standard Message ID Filter

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing standard message ID filter elements, the address is the start address of the standard filter list FDCAN_SIDFC.FLSSA plus the filter element index (0…127).

The data structure of standard message ID filter elements is shown in the following table.

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Table 41-4 Data Structure of Standard Message ID Filter

word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S0	SFT[1:0]		SFEC[2:0]			SFID1[10:0]											Reserved					SFID2[0:0]									

Bit Field	Name	Description
31:30	SFT[1:0]	Standard Filter Type 00: Range filter from SFID1 to SFID2 01: Dual ID filter: Filter ID is SFID1 or SFID2 10: Typical filter: SFID1 is the filter ID, SFID2 is the mask 11: Disable current filter Note: When SFT=11b, disable the filter element, but receive filtering remains active (same behavior as SFEC=00b).
29:27	SFEC[2:0]	Standard Filter Element Configuration All enabled filter elements are used for receiving filtering of standard frames. When the first matching enabled filter element is found, or when the end of the filter list is reached, the receive filtering stops. If SFEC = 100b, 101b, or 110b, when a match is found, the interrupt flag FDCAN_IR.HPM is set to 1 and an interrupt is generated (if enabled). In this case, register FDCAN_HPMS is updated to reflect the priority matching state. 000: Disable current filter 001: Store in receive FIFO 0 if matched by filter 010: Store in receive FIFO 1 if matched by filter 011: Reject reception if matched by filter, not suitable for use with synchronous messages 100: Set priority if matched by filter but do not store, not suitable for use with synchronous messages 101: Set priority if matched by filter and store in FIFO 0 110: Set priority if matched by filter and store in FIFO 1 111: Store in receive buffer or as a debug message, disregarding the configuration of SFT[1:0]
26:16	SFID1[10:0]	Standard Filter ID 1. The first ID of the standard ID filter element. When used for receive buffer, synchronous messages, or debug messages, this field is the message ID to be stored. In this case, the message ID must match exactly, and no mask mechanism is used.
10:0	SFID2[10:0]	Standard Filter ID 2. The definition of this field varies depending on the configuration of SFEC. 1) SFEC = 001b...110b: The second ID of the standard ID filter element 2) SFEC = 111b: Filter configuration used for receive buffer or debug messages, defined as follows: - 10:9: Defines the location where the received message is stored, processed in the

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Bit Field	Name	Description
		receive buffer, or as message A, B, or C in the debug message sequence 00: Store the message in the receive buffer 01: Debug message A 10: Debug message B 11: Debug message C - 8:6: Reserved - 5:0: Offset of the received message storage location in the receive buffer from the start address FDCAN_RXBC.RBSA.

41.3.6 Extended Message ID Filter

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing extended message ID filter elements, the address is FDCAN_XIDFC.FLESA plus twice the index of the filter element (0…63).

The data structure of extended message ID filter elements is shown in the following table.

Table 41-5 Data Structure of Extended Message ID Filter

word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0	EFEC[2:0]			EFID1[28:0]																												
F1	EFT[1:0]		Reserved	EFID2[28:0]																												

Bit Field	Name	Description
F0 bit 31:29	EFEC[2:0]	Extended Filter Element Configuration. All enabled filter elements are used for receiving filtering of extended frames. When the first matching enabled filter element is found, or when the end of the filter list is reached, the receive filtering stops. If EFEC = 100b, 101b, or 110b, when a match is found, the interrupt flag FDCAN_IR.HPM is set to 1 and an interrupt is generated (if enabled). In this case, register FDCAN.HPMS is updated to reflect the priority matching state. 000: Disable current filter 001: Store in receive FIFO 0 if matched by filter 010: Store in receive FIFO 1 if matched by filter 011: Reject reception if matched by filter, not suitable for use with synchronous messages 100: Set priority if matched by filter but do not store, not suitable for use with synchronous messages 101: Set priority if matched by filter and store in FIFO 0 110: Set priority if matched by filter and store in FIFO 1 111: Store in receive buffer or as a debug message, disregarding the configuration of

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Bit Field	Name	Description
		EFT[1:0]
F0 bit 28:0	EFID1[28:0]	Extended Filter ID 1. The first ID of the extended ID filter element. When used for receive buffer, synchronous messages, or debug messages, this field is the message ID to be stored. In this case, the message ID must match exactly, and only the XIDAM masking mechanism is used.
F1 bit 31:30	EFT[1:0]	Extended Filter Type. 00: Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) 01: Dual ID filter: Filter ID is EFID1 or EFID2 10: Typical filter: EFID1 is the filter ID, EFID2 is the mask 11: Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), ignoring XIDAM masking
F1 bit 28:0	EFID2[28:0]	Extended Filter ID 2. Depending on the different configurations of EFEC, the definition of this field also varies. 1) EFEC = 001b...110b: The second ID of the extended ID filter element 2) EFEC = 111b: Filter configuration used for receive buffer or debug messages, defined as follows: - 10:9: Defines the location where the received message is stored, processed in the receive buffer, or as message A, B, or C in the debug message sequence 00: Store the message in the receive buffer 01: Debug message A 10: Debug message B 11: Debug message C - 8:6: Reserved - 5:0: Offset of the received message storage location in the receive buffer from the start address FDCAN_RXBC.RBSA.

41.3.7 Trigger Memory

Up to 64 trigger memory elements can be configured. When accessing a Trigger Memory element, its address is the Trigger Memory Start Address FDCAN_TTTMC.TMSA plus the index of the trigger memory element (0…63).

Table 41-6 Data Structure of Trigger Memory

word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T0	TM[15:0]																Reserved	CC[6:0]							Reserved		TMIN	TMEX	TYPE[3:0]			
T1	Reserved								FTYPE	MNR[6:0]							Reserved														MSC[2:0]		

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Bit Field	Name	Description
T0 bit 31:16	TM[15:0]	Time Mark Cycle time for which the trigger becomes active.
T0 bit 14:8	CC[6:0]	Cycle code: Cycle count for which the trigger is valid. Ignored for trigger types Tx_Ref_Trigger, Tx_Ref_Trigger_Gap, Watch_Trigger, Watch_Trigger_Gap, End_of_List. 0b000000x valid for all cycles 0b000001c valid every 2nd cycle at cycle count mod2 = c 0b00001cc valid every 4th cycle at cycle count mod4 = cc 0b0001ccc valid every 8th cycle at cycle count mod8 = ccc 0b001cccc valid every 16th cycle at cycle count mod16 = cccc 0b01ccccc valid every 32nd cycle at cycle count mod32 = ccccc 0b1cccccc valid every 64th cycle at cycle count mod64 = cccccc
T0 bit 5	TMIN	Time mark event internal: 0: No action 1: FDCAN_TTIR.TTMI is set when trigger memory element becomes active
T0 bit 4	TMEX	Time mark event external: 0: No action 1: Pulse at output fdcan_tmp for more than one instance and fdcan_tmp if only one instance with the length of one period is generated when the time arc of the trigger memory element becomes active and FDCAN_TTOCN.TTMIE = 1
T0 bit 3:0	TYPE[3:0]	Trigger type: 0000 Tx_Ref_Trigger - valid when not in Gap 0001 Tx_Ref_Trigger_Gap - valid when in Gap 0010 Tx_Trigger_Single - starts a single transmission in an exclusive time window 0011 Tx_Trigger_Continuous - starts continuous transmission in an exclusive time window 0100 Tx_Trigger_Arbitration - starts a transmission in an arbitrating time window 0101 Tx_Trigger_Merged - starts a merged arbitration window 0110 Watch_Trigger - valid when not in Gap 0111 Watch_Trigger_Gap - valid when in Gap 1000 Rx_Trigger - check for reception 1001 Time_Base_Trigger - only control TMIN, TMEX 1010 … 1111=End_of_List - illegal type, causes configuration error
T1 bit 23	FTYPE	Filter type: 0: 11-bit standard message ID 1: 29-bit extended message ID
T1 bit 22:16	MNR[6:0]	Message Number Transmission: trigger is valid for configured Tx buffer number. Valid values are 0 to 31. Reception: trigger is valid for standard/extended message ID filter element number. Valid values are, respectively 0 to 63 and 0 to 127.
T1 bit 2:0	MSC[2:0]	Message status count Counts scheduling errors for periodic messages in exclusive time windows. It has no

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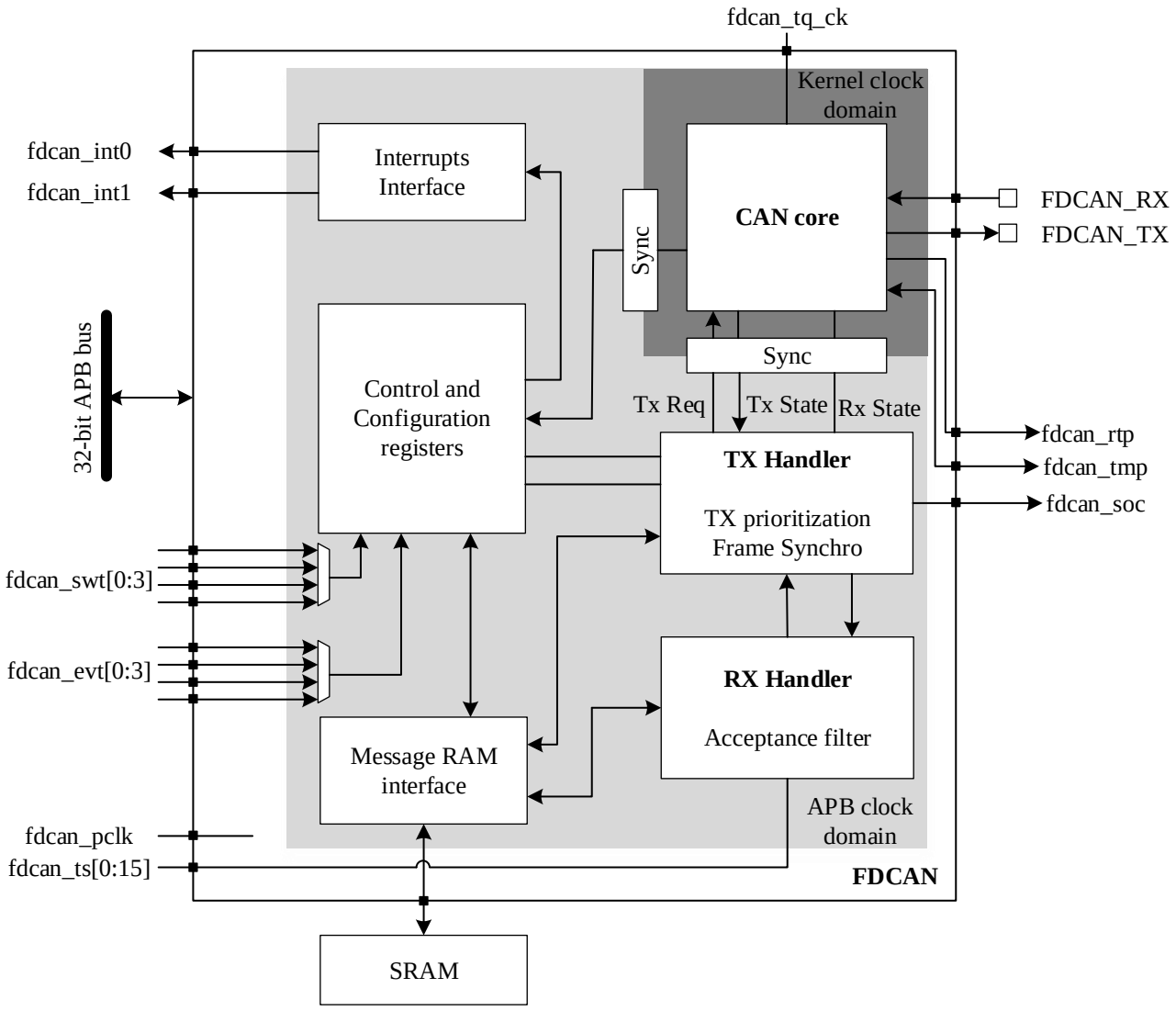
Email: sales@nsing.com.sg

Bit Field	Name	Description
		function for arbitrating messages and in event-driven CAN communication (ISO11898-1). 0-7= Actual status

Note: The trigger memory elements have to be written when the FDCAN is in INIT state. Write access to the trigger memory elements outside INIT state is not allowed. There is an exception for TMIN and TMEX when they are defined as part of a trigger memory element of TYPE Tx_Ref_Trigger. In this case they become active at the time mark modified by the actual reference trigger offset (FDCAN_TTOST.RTO).

41.4 Basic Function Description

Figure 41-2 FDCAN Functional Block Diagram



Interrupt Interface

The FDCAN module supports 2 interrupt lines output, fdcan_int0 and fdcan_int1, which can be enabled or disabled

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separately. All internal interrupts of the module can be connected to fdcan_int0 or fdcan_int1 and can be independently configured. By default, all interrupts are connected to the interrupt line fdcan_int0.

CAN Core

The CAN core comprises a CAN protocol controller and receive/transmit shift registers, providing all ISO 11898-1:2015 protocol functionalities, supporting both 11-bit and 29-bit identifiers.

Synchronization Unit

The synchronization unit synchronizes signals from the APB clock domain to the CAN core clock domain, or synchronizes signals from the CAN core clock domain to the APB clock domain.

Timestamp

Can receive an external 16-bit vector as a substitute for the internal 16-bit CAN time counter to generate receive and send timestamps.

Transmission Processing

The transmission processing unit controls the data transfer from message RAM to the CAN core. Up to 32 transmission buffers can be configured, which can be used as dedicated transmission buffers, transmission FIFO/queues, or a combination of dedicated transmission buffers and transmission FIFO/queues, with support for transmission cancellation. At any given time, the user can only select either a transmission queue or a transmission FIFO. Additionally, the configuration can include the generation of a transmission event FIFO during transmission, which includes transmission timestamps and associated message IDs.

The transmission processing unit also implements the Frame Synchronization Entity FSE which controls timetriggered communication according to ISO11898-4. It synchronizes itself to the reference messages on the CAN bus, controls cycle time and global time, and handles transmissions according to the predefined message schedule, the system matrix. It also handles the time marks of the system matrix that are linked to the messages in the Message RAM. Stop Watch Trigger, Event Trigger, and Time Mark Interrupt are synchronization interfaces.

Reception Processing

The receive processing unit controls the transfer of messages received from the CAN core to external message RAM. The receive processing unit supports two receive FIFOs, each with independently configurable sizes, and up to 64 dedicated receive buffers for storing all messages passing through the receive filters. Additionally, the receive processing unit supports dedicated receive buffers that store messages matching specific identifiers (IDs), different from receive FIFOs. All messages include receive timestamps. Up to 128 receive filters can be defined when using 11-bit IDs, and up to 64 filters can be defined for 29-bit IDs.

Message RAM Interface

The message RAM interface connects the FDCAN module to external 32-bit message RAM for message control and

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Email: sales@nsing.com.sg

arbitration, shared by eight FDCAN modules, supporting a maximum of 32K words (32-bit).

41.4.1 Operating Modes

41.4.1.1 Software Initialization

When FDCAN_CCCR.INIT is set to 1, the module enters the software initialization state. At this point, both incoming and outgoing messages from the CAN bus will stop, and the state of the CAN bus output pin FDCAN_TX will be recessive (high level). The Error Management Logic (EML) counters remain unchanged, and no configuration register values will be altered. The FDCAN_CCCR.INIT bit can be set to 1 by software or automatically set to 1 when a hardware reset occurs or when entering the Bus_Off state. Clearing the FDCAN_CCCR.INIT bit will end the software initialization, and the module's Bit Stream Processor (BSP) will wait for an 11-bit recessive (Bus_Idle) sequence to synchronize with data transmission on the CAN bus before participating in bus activities and message transmission.

Write operations to the FDCAN configuration registers are only allowed when both the FDCAN_CCCR.INIT bit and FDCAN_CCCR.CCE bit are set to 1.

The FDCAN_CCCR.CCE bit can only be set to 1 or cleared when the FDCAN_CCCR.INIT bit is set to 1, and it is automatically cleared when the FDCAN_CCCR.INIT bit is cleared."

When FDCAN_CCCR.CCE is set to 1, the following registers will be reset:

- FDCAN_HPMS - High Priority Message Status
- FDCAN_RXF0S - Receive FIFO 0 Status
- FDCAN_RXF1S - Receive FIFO 1 Status
- FDCAN_TXFQS - Transmit FIFO/Queue Status
- FDCAN_TXBRP - Transmit Buffer Request Pending
- FDCAN_TXBTO - Transmit Buffer Transmission Occurred
- FDCAN_TXBCF - Transmit Buffer Cancellation Finished
- FDCAN_TXEFS - Transmit Event FIFO Status
- FDCAN_TTOST - TT Operation Status
- FDCAN_TTLGT - TT local and global time, only global time FDCAN_TTLGT.GT is reset
- FDCAN_TTCTC - TT cycle time and count
- FDCAN_TTCSM - TT cycle sync mark

When FDCAN_CCCR.CCE is set to 1, the FDCAN_TOCV.TOC bit is preset to the configuration value of FDCAN_TOCC.TOP. At this point, both the transmission processing unit and the reception processing unit state machines remain in idle state.

Write operations to the following registers are only allowed when the FDCAN_CCCR.CCE bit is cleared:

- FDCAN_TXBAR - Transmit Buffer Add Request
- FDCAN_TXBCR - Transmit Buffer Cancellation Request

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The FDCAN_CCCR.TEST and FDCAN_CCCR.MON bits can only be set to 1 by software when both the FDCAN_CCCR.INIT and FDCAN_CCCR.CCE bits are set to 1, but can be cleared at any time.

The FDCAN_CCCR.DAR bit can only be set to 1 or cleared when both the FDCAN_CCCR.INIT and FDCAN_CCCR.CCE bits are set to 1.

41.4.1.2 Normal Operating Mode

After initialization is completed and the FDCAN_CCCR.INIT bit is cleared, FDCAN will synchronize with the CAN bus and prepare for communication.

Received messages (including message ID and DLC) filtered by the receive filters will be stored in Receive FIFO 0, Receive FIFO 1, or dedicated receive buffers.

Messages can be sent by initializing or updating dedicated transmission buffers and transmission FIFO/queues. Automatic transmission is not supported after receiving a remote frame.

41.4.1.3 CAN FD Operating Mode

The CAN FD protocol supports two frame modes. The first is the Extended Data Length (EDL) mode, in which the data field in a message frame can exceed eight bytes. The second is the Fast Frame Mode (FFM), where the bit rate of the control field, data field, and CRC field during message frame transmission is higher than that of the start and end fields. Fast Frame Mode can be used in conjunction with Extended Data Length mode.

The reserved bit in a CAN message frame with an 11-bit identifier and the first reserved bit in a CAN message frame with a 29-bit identifier are now used as the FDF bit. When FDF is recessive, it indicates a CAN FD message frame, while it indicates a typical CAN message frame when dominant. In a CAN FD message frame, the additional two bits after the FDF bit, res and BRS, determine whether a bit rate switch should occur. If res is dominant and BRS is recessive, it indicates that the current frame has a bit rate switch. If res is recessive, the functionality is undefined and reserved for future protocol extensions. If both FDF and res are recessive in a received frame, a protocol exception event occurs, setting the FDCAN_PSR.PXE bit to 1. If the protocol exception handling function is enabled (FDCAN_CCCR.PXHD = 0b), the module's operational state will transition from receiver (FDCAN_PSR.ACT = 10b) to synchronization (FDCAN_PSR.ACT = 00b) at the next sample point. If the protocol exception handling function is disabled (FDCAN_CCCR.PXHD = 1b), FDCAN will consider the recessive res bit as a formatting error and send an error frame.

By programming FDCAN_CCCR.FDOE, the CAN FD operating mode can be enabled, allowing the module to send and receive CAN FD message frames while also supporting the sending and receiving of typical CAN message frames. During transmission, the frame type (CAN FD message frame or typical CAN message frame) can be configured by setting the FDF bit in the corresponding transmission buffer. When FDCAN_CCCR.FDOE = 0b, received message frames are treated as typical CAN message frames, and if a CAN FD message frame is received, an error frame is sent. If the CAN FD functionality is disabled, even if the FDF bit in the transmission buffer is set to 1, CAN FD message frames will not be sent. Changes to FDCAN_CCCR.FDOE and FDCAN_CCCR.BRSE bits can only be made when both FDCAN_CCCR.INIT and FDCAN_CCCR.CCE are set to 1.

If FDCAN_CCCR.FDOE = 0b, the FDF and BRS bits are ignored, and only typical CAN message frames are sent. If FDCAN_CCCR.FDOE = 1b and FDCAN_CCCR.BRSE = 0b, the FDF bit is valid, allowing for the transmission of CAN FD message frames. When FDCAN_CCCR.FDOE = 1b and FDCAN_CCCR.BRSE = 1b, bit rate switching is supported when sending CAN FD message frames. For a transmission buffer where both the FDF and BRS bits

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

are set to 1, the message is sent as a CAN FD message frame with bit rate switching enabled.

It is recommended to switch modes only when the following conditions are met:

- The error rate of the CAN FD data field is significantly higher than that of the CAN FD arbitration field. In this case, the bitrate switching function should be disabled.
- After system startup, all nodes only send typical CAN message frames. Only after confirming that the current bus can communicate via CAN FD message frames, all nodes switch to CAN FD mode.
- Wake-up messages in the CAN local network must be sent in the format of typical CAN message frames.
- During the vehicle offline programming process, not all nodes support CAN FD. Non-CAN FD nodes will remain in silent mode until programming is completed. Subsequently, all nodes will switch back to typical CAN communication.

In CAN FD mode, when the DLC value ranges from 0 to 8, the data field length definition is the same as in typical CAN. When the DLC value ranges from 9 to 15 (where the data field in typical CAN is always 8 bytes), the data field length definition is based on the following table.

Table 41-7 CAN FD data field length definition

DLC	9	10	11	12	13	14	15
Number of data bytes	12	16	20	24	32	48	64

In CAN FD fast frame mode, if the BRS bit is recessive, the bit timing will automatically switch after the BRS bit. Before the BRS bit, the CAN FD arbitration field uses the standard bit timing defined by the nominal bit time and the prescaler register FDCAN_NBTP. In the subsequent CAN FD data field, the fast bit timing defined by the data bit time and the prescaler register FDCAN_DBTP is used. Finally, it switches back to standard bit timing at the CRC delimiter or when an error is detected (whichever event occurs first).

The maximum configurable bitrate of the CAN FD data field depends on the FDCAN core clock frequency. For example, if the FDCAN core clock frequency is 20MHz and the shortest configurable bit time is four time quanta (tq), then the bitrate of the data field is 5Mb/s.

In both the CAN FD long frame and fast frame data frame formats, the value of the ESI (Error State Indicator) bit is determined by the transmitter error state at the start of transmission. If the transmitter is in a passive error state, an recessive ESI bit occurs, otherwise, an dominant bit is sent. In CAN FD remote frames, the ESI bit is always dominant, regardless of the transmitter error state, and the data field length is 0.

41.4.1.4 Transceiver Delay Compensation

When sending data in the CAN FD data field, only one node is transmitting data, while all other nodes are in the receiver state. When the FDCAN transmitter sends data via the FDCAN_TX pin, the receiver simultaneously receives the data being sent via the FDCAN_RX pin. There is a delay in receiving the data relative to the transmission (transceiver loop delay). If the delay time is greater than TSEG1 (time segment before the sampling point in a single bit), bit errors occur. Without transceiver delay compensation, the data field bitrate will be limited by the loop delay.

FDCAN adopts a delay compensation mechanism to compensate for the transceiver loop delay, enabling stable transmission of the CAN FD data field at high bit rates without being affected by the loop delay.

To check for bit errors in the data field of the sending node, the delayed transmitted data is compared with the received

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data at the second sampling point SSP. If a bit error is detected, the transmitter will respond to the bit error at the next regular sampling point. Delay compensation is disabled in the arbitration field.

When the data bit time is less than the transmitter delay, FDCAN_DBTP.TDC can be set to 1 to enable transmitter delay compensation, which is detailed in the new version of the ISO11898-1 standard.

Received data bits are compared with the transmitted data bits at the SSP. SSP is defined as the sum of the delay time measured from the FDCAN transmit pin FDCAN_TX to the receive pin FDCAN_RX and the transmitter delay compensation offset value (configured by FDCAN_TDCR.TDCO). Transmitter delay compensation is used to adjust the position of the SSP in the received bit (e.g., half a data field bit time). The position of the second sampling point is rounded down to the next mtq (minimum time quanta, which is one fdcan_tq_ck clock cycle).

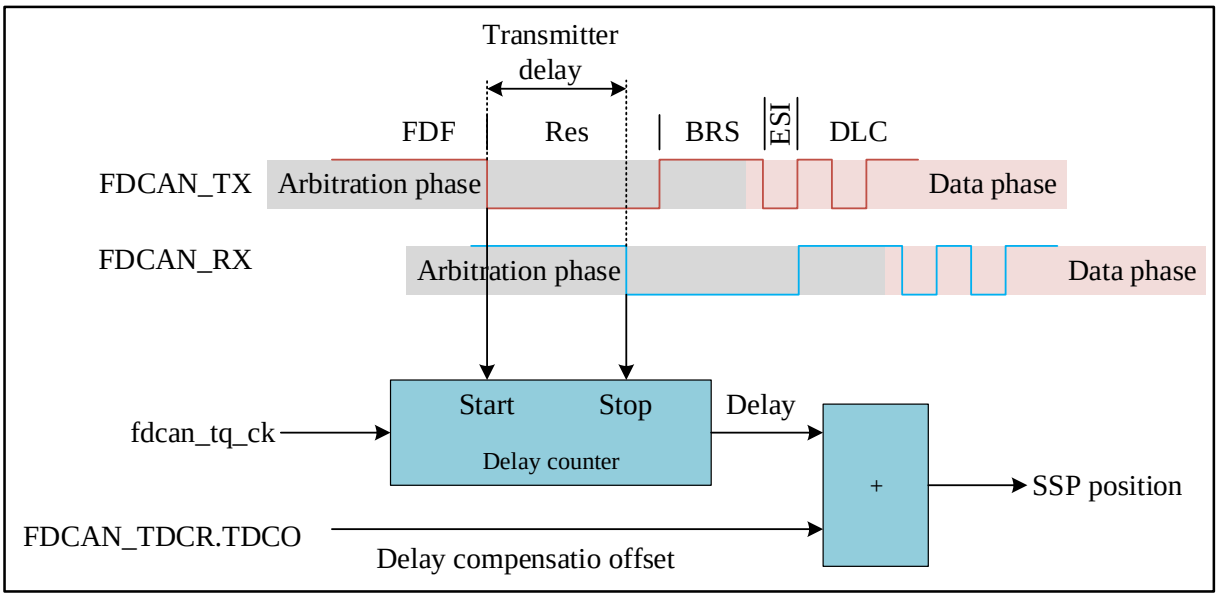
FDCAN_PSR.TDCV is the actual transmitter delay compensation value. When FDCAN_CCCR.INIT is set to 1, the FDCAN_PSR.TDCV value is cleared to zero. If FDCAN_DBTP.TDC is set to 1, the FDCAN_PSR.TDCV value is updated each time a CAN FD message frame is transmitted.

When using transmitter delay compensation in FDCAN, the following boundary conditions must be considered:

- The sum of the delay time measured between FDCAN_TX and FDCAN_RX and the transmitter delay compensation offset value FDCAN_TDCR.TDCO must be less than 6 bit times of the data field.
- The sum of the delay time measured between FDCAN_TX and FDCAN_RX and the transmitter delay compensation offset value FDCAN_TDCR.TDCO must be less than or equal to 127 mtq. If the sum exceeds 127 mtq, the transmitter delay compensation uses the maximum value (127 mtq).
- The data field ends at the sampling point of the CRC delimiter, at which point the reception of data bits stops at the SSP.

When FDCAN_DBTP.TDC is set to 1, the transmitter delay compensation is enabled. At this time, the measurement starts at the falling edge between the FDF bit and the res bit in each transmitted CAN FD message frame, and stops when this falling edge is observed on the receive pin FDCAN-RX. This measurement is in units of mtq.

Figure 41-3 FDCAN Transceiver Delay Measurement



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If there is a dominant glitch signal in the received FDF bit, it may cause an abnormal termination of the delay compensation measurement before the falling edge is received (resulting in an early SSP position). In this case, FDCAN_TDCR.TDCF can be set to 1 to enable the transmitter delay compensation filter window. The delay compensation filter window defines the minimum value of the SSP position, where the transmitter delay measurement will ignore the dominant edges received by FDCAN_RX that cause the SSP position to advance. The measurement stops when the SSP position is not less than the FDCAN_TDCR.TDCF value, and FDCAN_RX is at a low level.

41.4.1.5 Restricted Operating Mode

In Restricted Operating Mode, a node can receive data frames and remote frames, acknowledge valid frames, but will not transmit data frames, remote frames, active error frames, or overload frames. In case of an error or overload, the node will not send dominant bits but will wait for the bus to become idle to resynchronize with the CAN bus. The error counters (FDCAN_ECR.REC, FDCAN_ECR.TEC) are frozen, and the error log (FDCAN_ECR.CEL) remains active. When the FDCAN_CCCR.ASM bit is set to 1 by software, the FDCAN enters Restricted Operating Mode. The FDCAN_CCCR.ASM can only be set to 1 when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to "1", but it can be cleared at any time by software.

When the transmit processing unit fails to read data from the message RAM in a timely manner, it will automatically enter Restricted Operating Mode. Software must reset the FDCAN_CCCR.ASM bit to exit Restricted Operating Mode.

Restricted Operating Mode can be used for adaptive CAN bitrate applications. In this mode, the application tests different bitrates and exits Restricted Operating Mode upon receiving valid frames.

Note: Restricted Operating Mode cannot be combined with loopback mode (internal or external).

41.4.1.6 Bus Monitoring Mode (Silent Mode)

When FDCAN_CCCR.MON is set to 1, the FDCAN enters Bus Monitoring Mode. In Bus Monitoring Mode (for more detailed information, please refer to ISO11898-1, 10.12 Bus Monitoring), the FDCAN is able to receive valid data frames and valid remote frames, but cannot transmit. In this mode, the FDCAN will only send recessive bits on the CAN bus. If the FDCAN needs to send dominant bits (such as ACK bits, overload flags, active error flags), they are only sent internally within the module so that the FDCAN can monitor the dominant bit, while the CAN bus remains in the recessive state. In Bus Monitoring Mode, the FDCAN_TXBRP register will remain in the reset state.

Bus Monitoring Mode can be used to analyze the traffic on the CAN bus without causing interference by sending dominant bits. The connection of FDCAN_TX and FDCAN_RX signals to the FDCAN in Bus Monitoring Mode is shown in the diagram below.

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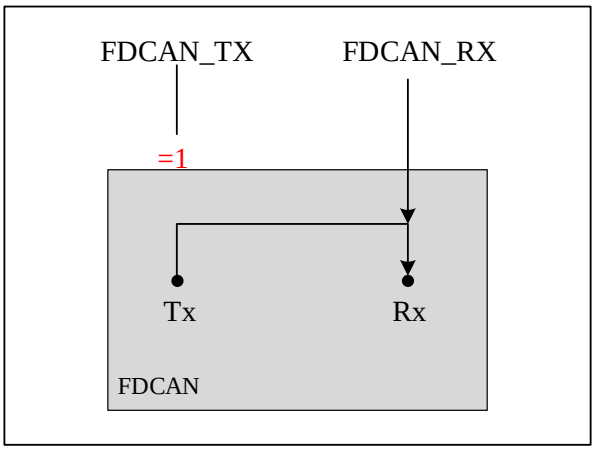
Figure 41-4 FDCAN Bus Monitoring Mode Pin Control



41.4.1.7 Disable Automatic Retransmission (DAR) Mode

According to the CAN specification (see ISO 11898-1:2015, 8.3.4 Recovery Management), FDCAN supports automatic retransmission of message frames in case of arbitration failure or error disturbance during transmission. Automatic retransmission is enabled by default, but can be disabled by setting FDCAN_CCCR.DAR to disable automatic retransmission.

According to the CAN specification, in DAR (Disable Automatic Retransmission) mode, all retransmission operations are automatically canceled once the CAN bus is started. The transmit buffer request pending bit FDCAN_TXBRP.TRPx is automatically reset after a successful transmission, and it is also reset if the transmission has not started when canceled, is aborted due to arbitration loss, or encounters an error during transmission.

- Successful Transmission:
  - The transmit start bit corresponding to the transmit buffer is set to 1 in FDCAN_TXBTO.TOx
  - The cancel complete bit corresponding to the transmit buffer in FDCAN_TXBCF.CFx is not set to 1
- Transmission Canceled but Still Successful:
  - The transmit start bit corresponding to the transmit buffer is set to 1
  - The cancel complete bit corresponding to the transmit buffer in FDCAN_TXBCF.CFx is set to 1
- Arbitration Loss or Frame Transmission Disturbance:
  - The transmit start bit corresponding to the transmit buffer is not set to 1
  - The cancel complete bit corresponding to the transmit buffer in FDCAN_TXBCF.CFx is set to 1

When a message frame is successfully transmitted, if the transmit event storage is enabled, a transmit event FIFO entry of event type ET=10b (even if the transmission is canceled) will be written.

41.4.1.8 Power-down (Sleep) Mode

FDCAN can enter Power-down mode by setting the Clock Stop Request bit FDCAN_CCCR.CSR. Once the clock stop request is effective, reading the FDCAN_CCCR.CSR bit will return a value of 1.

After all transmit requests are completed, FDCAN will wait until it detects bus idle state. Then, FDCAN_CCCR.INIT is set to 1 to prevent further CAN transmissions. FDCAN_CCCR.CSA is then set to 1 to confirm readiness to enter

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Power-down mode, and the module clock can be turned off. In this mode, if the module clock is not turned off, register access can still continue, but write operations to FDCAN_CCCR.INIT are ineffective.

Note: In case of severe disturbances on the CAN bus, it may not be possible to detect bus idle state, causing FDCAN not to set the FDCAN_CCCR.INIT bit. This situation can be detected by polling FDCAN_PSR.ACT. In this case, software can set FDCAN_CCCR.INIT to 1 to immediately stop CAN communication, regardless of any ongoing transmit/receive operations.

To exit Power-down mode, the application must first enable the module clock, then reset the FDCAN_CCCR.CSR bit. Next, check the FDCAN_CCCR.CSA bit; if it has been reset, confirm that the clock is enabled. The application can then restart CAN communication by resetting the FDCAN_CCCR.INIT bit.

41.4.1.9 Test Mode

To write access the FDCAN_TEST register, FDCAN_CCCR.TEST must be set to 1 first. This allows configuration of the test mode and functions.

By configuring FDCAN_TEST.TX, four output functions can be implemented on the FDCAN transmit pin FDCAN_TX. In addition to the default serial data output function, the bit time can be monitored using CAN sampling point signals, and the output can hold either the dominant or recessive value. The actual status of the FDCAN_RX pin can be read from FDCAN_TEST.RX. Both functions can be used to check the CAN bus physical layer.)

Due to the synchronization mechanism between the CAN core clock domain and the host clock domain, there may be a delay of several APB clock cycles between the new configuration output on the FDCAN_TX output pin and the write operation to FDCAN_TEST.TX. This delay also applies when reading the FDCAN_RX input pin status via FDCAN_TEST.RX.

Note: The test mode is only intended for production testing or self-testing. Software control of the FDCAN_TX pin will disrupt all CAN protocol functions. It is not recommended to use the test mode in actual applications.

41.4.1.10 External Loopback Mode

Setting FDCAN_TEST.LBCK to 1 enables the FDCAN to be in External Loopback Mode. In this mode, the FDCAN processes its own transmitted messages as received messages and stores the messages (if they pass through the receive filters) in the receive FIFO. The connection of FDCAN_TX and FDCAN_RX signals to the FDCAN in External Loopback Mode is shown in the diagram below.

External Loopback Mode is used for hardware self-testing. To avoid external simulation interference, the FDCAN ignores ACK errors in loopback mode (ACK is recessive in data/remote frames). In this mode, the FDCAN achieves internal feedback from transmit output to receive input. The actual value on the FDCAN_RX input pin is disregarded. The transmitted messages can be monitored on the FDCAN_TX transmit pin. The pin control in External Loopback Mode is shown in the diagram below.

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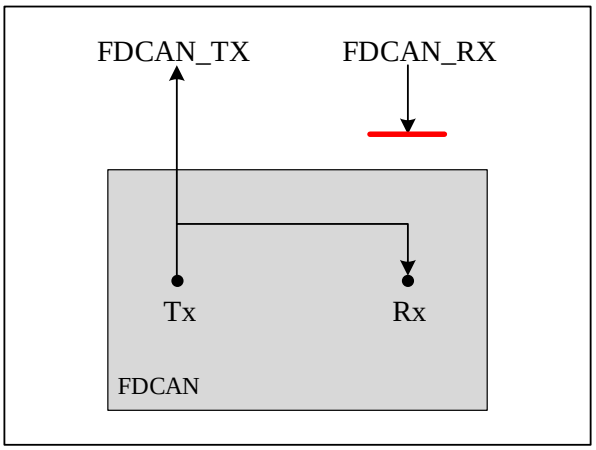
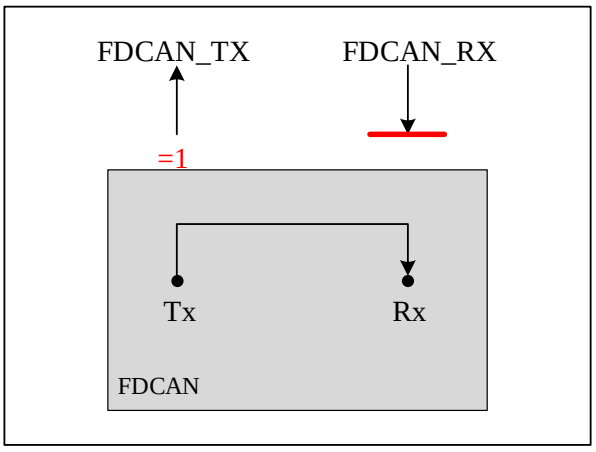
Figure 41-5 FDCAN External Loopback Mode Pin Control



41.4.1.11 Internal Loopback Mode

Setting both FDCAN_TEST.LBCK and FDCAN_CCCR.MON to 1 puts the FDCAN in Internal Loopback Mode. This mode can be used for "hot self-testing," allowing the FDCAN to perform diagnostics without affecting the CAN bus system connected to the FDCAN_TX and FDCAN_RX pins. In this mode, the FDCAN_RX pin is disconnected from the FDCAN, and the FDCAN_TX pin remains recessive. The pin control in Internal Loopback Mode is shown in the diagram below.

Figure 41-6 FDCAN Internal Loopback Mode Pin Control



41.4.1.12 Application Watchdog

The application watchdog is served by reading register FDCAN_TTOST. When the application watchdog is not served in time, bit FDCAN_TTOST.AWE is set, all TTCAN communication is stopped, and the FDCAN is set into bus monitoring mode.

The TT application watchdog can be disabled by programming the application watchdog limit FDCAN_TTOCF.AWL to 0x00. The TT application watchdog should not be disabled in a TTCAN application program.

41.4.1.13 Timestamp Generation

FDCAN provides a 16-bit loopback counter for timestamp generation. The counter clock source is the FDCAN bit

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Email: sales@nsing.com.sg

time, and can be configured with clock pre-scaling (1...16) using FDCAN_TSCC.TCP. The counter value can be read from FDCAN_TSCV.TCV. Writing to the FDCAN_TSCV register resets the counter value to 0. When the counter loops, FDCAN_IR.TSW is set to 1.

When a message frame starts to be received/transmitted, the counter value is captured and stored in the timestamp of the Rx buffer, Rx FIFO, or Tx event FIFO. The 16-bit timestamp can be enabled by configuring the FDCAN_TSCC.TSS bit.

41.4.1.14 Timeout Counter

FDCAN provides a 16-bit timeout counter to indicate timeout conditions for Receive FIFO 0, Receive FIFO 1, and the Tx Event FIFO. The timeout counter is a decrementing counter, with its clock prescaling controlled by FDCAN_TSCC.TCP, similar to the timestamp counter. The timeout counter can be configured using the FDCAN_TOCC register. The counter value can be read from FDCAN_TOCV.TOC. The timeout counter can only be started when FDCAN_CCCR.INIT=0. When FDCAN_CCCR.INIT=1, the timeout counter stops counting, for example when FDCAN enters Bus_Off state.

The operation mode of the timeout counter is selected by FDCAN_TOCC.TOS. When configured in continuous mode, the counter starts counting once FDCAN_CCCR.INIT is reset. Writing to FDCAN_TOCV presets the counter value to FDCAN_TOCC.TOP and continues decrementing the count.

When the timeout counter is controlled by one of the FIFOs, the counter is preset to the FDCAN_TOCC.TOP value when the FIFO is empty. The decrementing count starts when the first element is written to the FIFO. Writing to FDCAN_TOCV does not affect the count value at this time.

When the counter value decrements to zero, FDCAN_IR.TOO is set to 1. If operating in continuous mode, the counter immediately restarts with the initial value set to FDCAN_TOCC.TOP.

Note: The clock signal of the timeout counter is derived from the sampling point signal of the CAN core. Therefore, due to the synchronization/resynchronization mechanism of the CAN core, the timing of the timeout counter decrement may vary. If bitrate switching is used in CAN FD, the clock of the timeout counter in the arbitration field and data field may differ.

41.4.2 Receive Processing

The receive processing unit controls the receive filters, transfers the received messages to dedicated receive buffers or specified receive FIFOs, and updates the write and fetch indexes of the receive FIFOs.

41.4.2.1 Receive Filters

FDCAN can configure two sets of receive filters, one for standard identifiers and the other for extended identifiers. These filters can be assigned to dedicated receive buffers or receive FIFO 0/1. When receiving a message, each filter list is checked starting from element 0 until the first matching element is found. Once a matching element is found, the check stops and subsequent filter elements are ignored.

Main features include:

- Each filter element can be configured as
  - Range filter

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- Single or dual specific ID match filter
- Classic bit mask filter

- Each filter element can be configured to receive matched messages or reject matched messages
- Each filter element can be individually enabled/disabled
- Filters are checked one by one in list order, and the check stops after the first matching filter element is found.)

Relevant configuration registers include:

- Global Filter Configuration FDCAN_GFC
- Standard ID Filter Configuration FDCAN_SIDFC
- Extended ID Filter Configuration FDCAN_XIDFC
- Extended ID and Mask FDCAN_XIDAM

Based on the context of digital chip design, the translation of the content within parentheses into English is: (Based on the configuration of the filter element (SFEC/EFEC), one of the following actions will be triggered after a match:

- Store the received frame in Receive FIFO 0 or FIFO 1
- Store the received frame in a dedicated receive buffer
- Store the received frame in a dedicated receive buffer and generate a pulse on the filter event pin
- Reject the received frame
- Set the high priority message interrupt flag FDCAN_IR.HPM
- Set the high priority message interrupt flag FDCAN_IR.HPM and store the received frame in Receive FIFO 0 or FIFO 1)

After the complete ID reception, the receive filtering begins execution. Upon completion of the receive filtering, if a matching dedicated receive buffer or receive FIFO is found, the message processing unit will write the received message data in 32-bit form to the matching dedicated receive buffer or receive FIFO. If the CAN protocol controller detects an error condition (such as CRC error), the message will be discarded, resulting in the following effects:

- Dedicated Receive Buffer

The new message flag of the matching dedicated receive buffer will not be set to 1, but the newly received data will overwrite a portion of it. Error types refer to FDCAN_PSR.LEC or FDCAN_PSR.DLEC.

- Receive FIFO

The write index of the matching receive FIFO will not be updated, but the newly received data will overwrite a portion of it. Error types refer to FDCAN_PSR.LEC or FDCAN_PSR.DLEC. If the matching receive FIFO operates in overwrite mode, the boundary conditions described in the receive FIFO overwrite mode must be considered.

Note: When a received message is written to the receive FIFO or dedicated receive buffer, the unaltered receive ID will be stored, regardless of the filter used. The outcome of receive filtering largely depends on the order of configured

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filter elements.

41.4.2.1.1 Range Filtering

When using range filtering, the filter matches all message IDs within the range defined by SF1ID/SF2ID or EF1ID/EF2ID. For extended frames using range filtering, there are two possibilities:

- EFT=00b: Before applying range filtering, the received message ID is first ANDed with the extended ID mask (FDCAN_XIDAM).
- EFT=11b: Range filtering is directly performed, ignoring the extended ID mask (FDCAN_XIDAM).)

41.4.2.1.2 Specific ID Filtering

The filter can be configured to filter one or two specific message IDs. If filtering for a single specific message ID is required, the filter element must be configured as SFID1=SFID2 or EFID1=EFID2.

41.4.2.1.3 Classic Bit Mask Filtering

Classic bit mask filtering is used to mask certain bits of the received message ID to filter specific message groups. In this case, SFID1/EFID1 is used as the filter ID, while SFID2/EFID2 is used as the mask.

Bit positions in the mask that are 0 will mask the corresponding bit positions of the filter ID, disregarding the message ID's relevant bit positions during filtering, and only checking the receive message ID bit positions corresponding to the bit positions that are 1 in the mask.

If all mask bit positions are 1, a match will only occur when the receive message ID is identical to the filter ID. If all mask bit positions are 0, it matches all message IDs.

41.4.2.1.4 Standard Message ID Filtering

The process of filtering Standard Message IDs (11-bit IDs) is illustrated in the following figure.

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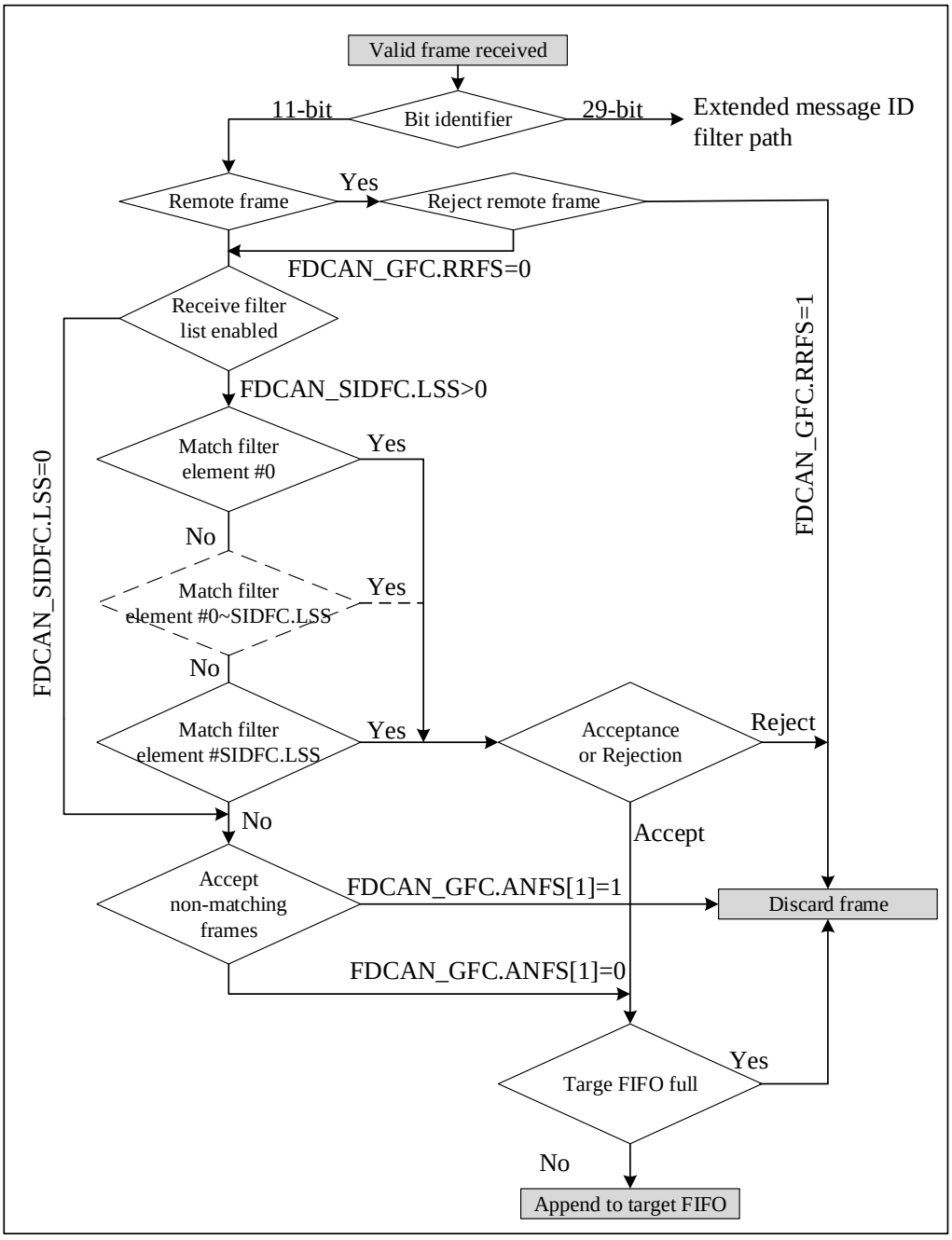
Figure 41-7 FDCAN Standard Message ID Filtering Process



By using the Global Filter Configuration FDCAN_GFC and the Standard ID Filter Configuration FDCAN_SIDFC, it is possible to compare and check the message ID, Remote Transmission Request bit (RTR), and Identifier Extension bit (IDE) of received message frames.

41.4.2.1.5 Extended Message ID Filtering

The process of filtering Extended Message IDs (29-bit IDs) is illustrated in the following diagram.

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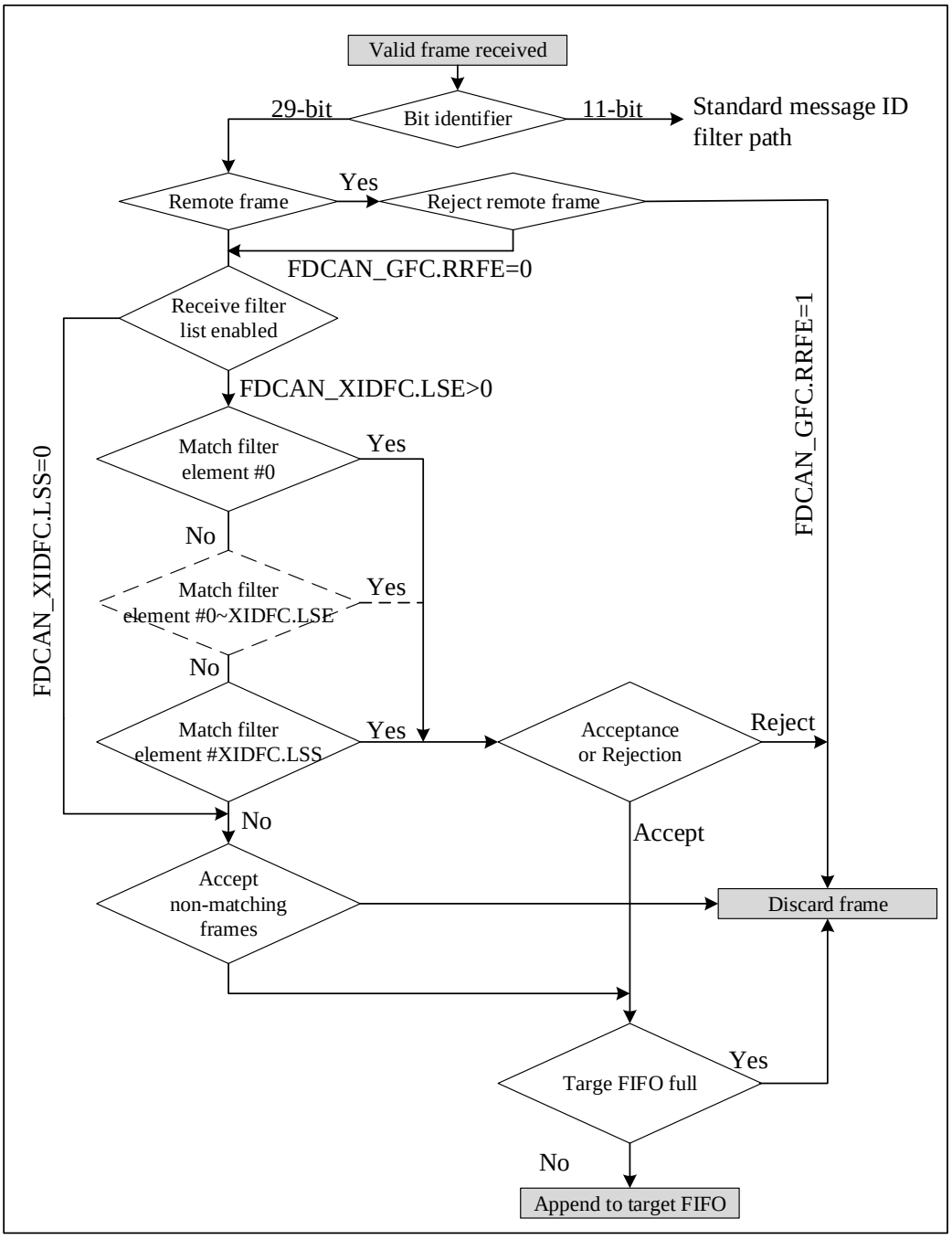
Figure 41-8 FDCAN Extended Message ID Filtering Process



By using the Global Filter Configuration FDCAN_GFC and the Extended ID Filter Configuration FDCAN_XIDFC, it is possible to compare and check the message ID, Remote Transmission Request bit (RTR), and Identifier Extension bit (IDE) of received message frames. However, before the filter check, the message's extended ID will be ANDed with the mask FDCAN_XIDAM.)

41.4.2.2 Receive FIFO

Receive FIFO 0 and Receive FIFO 1 can be configured individually using the registers FDCAN_RXF0C and FDCAN_RXF1C, with each FIFO capable of holding up to 64 elements.

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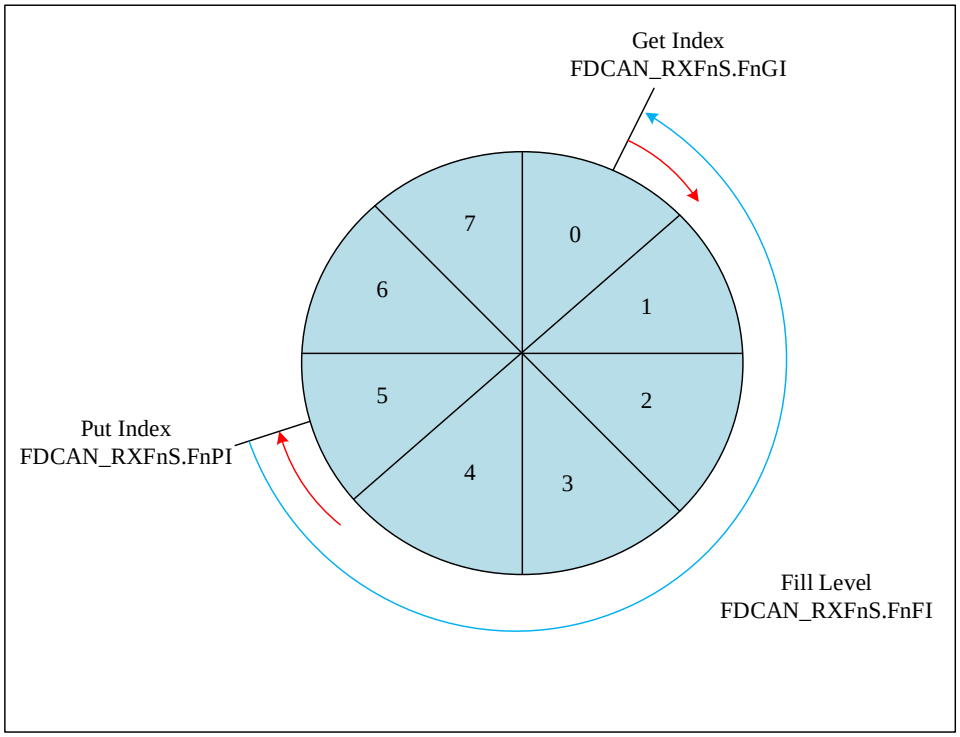
Messages that have passed through receive filtering will be transmitted to the corresponding receive FIFO based on the matched filter element configuration. In the default mode, when the receive FIFO is full (FDCAN_RXFnS.FnF=1b), new information cannot be written. This continues until at least one message is read out and the index is incremented.

When the receive FIFO is full, any new incoming information is discarded, and the FDCAN_IR.RFnL flag is set to 1.

The receive FIFO watermark flag can be used to prevent receive FIFO overflow. When the fill level of the receive FIFO reaches the receive FIFO watermark configured by FDCAN_RXFnC.FnWM, the FDCAN_IR.RFnW flag is set to 1.

The receive FIFO status is shown in the following diagram.

Figure 41-9 FDCAN Rx FIFO Status Diagram



When reading information from the receive FIFO, the actual address of the FIFO element is calculated by multiplying the get index (FDCAN_RXFnS.FnGI) by the element size and adding the current FIFO start address (FDCAN_RXFnC.FnSA).

The relationship between FIFO element size and register configuration is shown in the following table.

Table 41-8 CAN FD Data Field Length Definition

RXESC.RBDS[2:0] RXESC.FnDS[2:0]	Data Field (Bytes)	Element Size (RAM Words)
000	8	4
001	12	5
010	16	6

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011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

41.4.2.2.1 Receive FIFO Blocking Mode

Enabling the receive FIFO Blocking Mode is done by configuring FDCAN_RXFnC.FnOM=0b, which is also the default operating mode of the receive FIFO.

In this mode, when the receive FIFO is full (FDCAN_RXFnS.FnPI = FDCAN_RXFnS.FnGI), new messages cannot be written to the current FIFO until at least one message is read out and the get index is incremented. When the receive FIFO is full, FDCAN_RXFnS.FnF is set to 1. Additionally, the interrupt flag FDCAN_IR.RFnF is also set to 1.

If a message is received while the corresponding receive FIFO is full, the message will be discarded, and the situation of message loss will be indicated by FDCAN_RXFnS.RFnL = '1'. Additionally, the interrupt flag FDCAN_IR.RFnL will also be set to 1.

41.4.2.2.2 Receive FIFO Overwrite Mode

By configuring FDCAN_RXFnC.FnOM=1b, the receive FIFO overwrite mode is enabled.

When the receive FIFO is full, the next new message to be stored in the FIFO will overwrite the oldest message in the FIFO. Both the write index and get index will be incremented by 1.

In overwrite mode, when the FIFO is full, reading receive FIFO elements should start at least from the read get index + 1. This is because when the CPU reads messages from the message RAM via the get index, there may be new messages written to the message RAM via the write index. At this point, inconsistent data may be read from the corresponding receive FIFO elements. Adding an offset to the get index when reading data from the receive FIFO can avoid this issue. The offset depends on the speed at which the CPU accesses the receive FIFO. As shown in the diagram below, when reading the receive FIFO, an offset of 2 is added relative to the get index. At this point, the two messages stored in elements 1 and 2 will be lost.

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Figure 41-10 FDCAN Rx FIFO Full

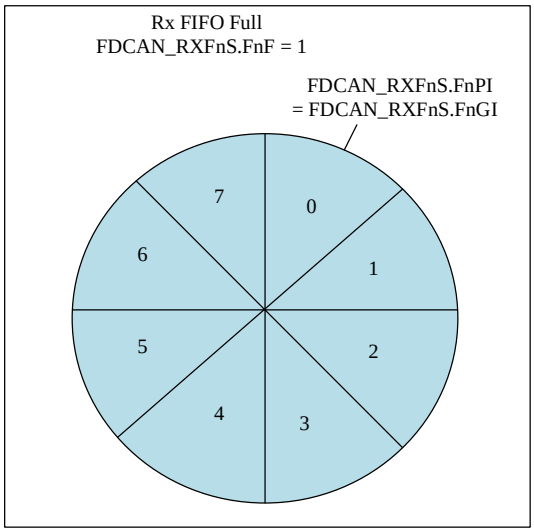
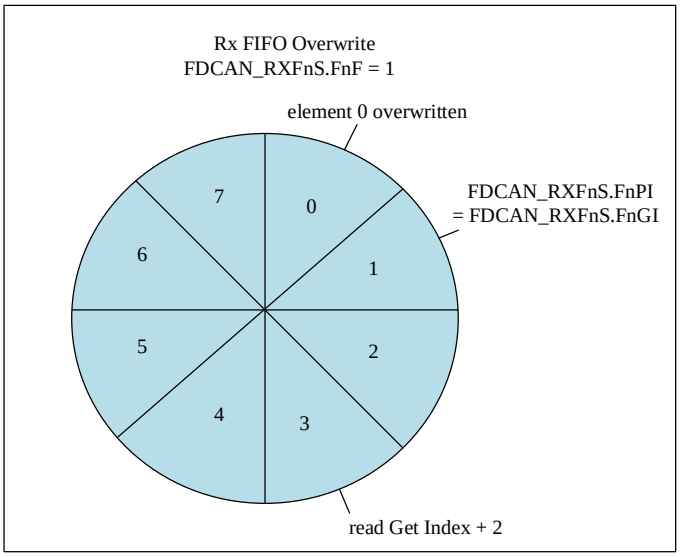


Figure 41-11 FDCAN Rx FIFO Overwrite Example



After reading data from the receive FIFO, the index of the last read element must be written to the receive FIFO acknowledgment index FDCAN_RXFnA.FnA. This will cause the get index to increment to that element index. If the write index has not yet advanced to this receive FIFO element, the FIFO full flag (FDCAN_RXFnS.FnF = '0') will be reset.

41.4.2.3 Dedicated Receive Buffer

FDCAN supports up to 64 dedicated receive buffers. The start address of the dedicated receive buffer area is configured by FDCAN_RXBC.RBSA.

For each dedicated receive buffer, a standard or extended message ID filter must be configured with SFEC/EFEC = 111b and SFID2/EFID2 [10:9] = 00b.

After a message is received through the filter, it will be stored in the dedicated receive buffer indicated by the filter element. The data format is the same as that of the receive FIFO elements. Additionally, the interrupt flag

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FDCAN_IR.DRX flag (message stored in dedicated receive buffer) is set to 1.

Table 41-9 Dedicated Receive Buffer Filter Configuration Example

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last byte of the matched received message is written to the message RAM, the corresponding new message flag in registers FDCAN_NDAT1 and FDCAN_NDAT2 is set to 1. Once the new message flag is set to 1, the corresponding dedicated receive buffer will be locked to prevent it from being updated by subsequent received messages. The host must write a "1" to the corresponding flag bit to reset the new message flag.

When the new message flag of a dedicated receive buffer is set to 1, the filter element referencing the message ID of this dedicated receive buffer will be ignored, and the receive filtering will continue to check the filter list. This may result in subsequent messages with the same ID as the dedicated buffer being stored in another dedicated receive buffer, stored in the receive FIFO, or rejected, depending on the filter configuration.

The processing flow of the dedicated receive buffer is as follows:

- Reset the interrupt flag FDCAN_IR.DRX
- Read the new message flag register
- Read the message from the message RAM
- Reset the new data flag of the processed message

41.4.2.4 Debug Message Filtering

Debug messages are stored in dedicated receive buffers. To use them, three consecutive dedicated receive buffers need to be allocated (for example, #61, #62, #63) to store debug messages A, B, and C. Their format is the same as that of dedicated receive buffer or receive FIFO elements.

To filter debug messages, a standard/extended message ID filter element needs to be configured for each debug message, with the standard/extended filter element set to SFEC/EFEC=111b. Messages matching these filter elements will be stored in the dedicated receive buffer specified by SFID2 / EFID2[5:0].

When a debug message is stored in a dedicated receive buffer, neither the new message flag nor the interrupt will be set. The status can be queried through FDCAN_RXF1S.DMS.

Table 41-10 Debug Message Filter Configuration Example

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID message 1	01	11 1101
1	ID message 2	10	11 1110
2	ID message 3	11	11 1111

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41.4.3 Transmission Processing

The transmission processing unit is responsible for handling the transmission requests of dedicated transmit buffers, transmit FIFOs, and transmit queues. It controls the transfer of messages to the CAN core, write index and get index management, and the transmission event FIFO. Up to 32 transmit buffers can be configured for message transmission, and each transmit buffer element can be individually configured for communication mode (Classical CAN or CAN FD). Depending on the different configurations of FDCAN_RXESC, the data field size of transmit buffer elements ranges from 2 to 16 bytes. The possible configurations for sending message frames are shown in the table below.

Table 41-11 Transmission Message Frame Configuration

FDCAN_CCCR		Transmit Buffer Element		Frame Transmit
BRSE	FDOE	FDF	BRS	
ignore	0	ignore	ignore	Classical CAN
0	1	0	ignore	Classical CAN
0	1	1	ignore	FD CAN without baud rate switching
1	1	0	ignore	Classical CAN
1	1	1	0	FD CAN without baud rate switching
1	1	1	1	FD CAN with baud rate switching

Note: AUTOSAR requires at least three transmit queues and supports transmit cancellation.

When the transmit buffer request pending register FDCAN_TXBRP is updated, the transmission processing unit will initiate a scan of the message RAM to find the highest priority transmission request (the transmit buffer with the smallest message ID). The FDCAN_TXBRP register is updated after the transmission is completed, or when the host writes a transmit request, or when the host writes a cancel transmit request through FDCAN_TXBCR.

41.4.3.1 Transmission Pause

The transmission pause function is suitable for CAN applications where the message ID is permanently set to a specific value and is difficult to change easily. These message IDs have a higher arbitration priority than other messages, but in specific applications, their arbitration priority should be the opposite. This can lead to a situation where one node sends a series of CAN messages, causing delays in the CAN messages of another node due to their lower arbitration priority.

For example, if CAN node 1 enables the transmission pause function and needs to send four messages based on application requirements, after the successful transmission of the first message, it will wait for a bus idle time of two CAN bit periods before allowing the transmission of the next message. If there are other pending messages from other nodes, they will be sent during the idle time without needing to arbitrate with the next message from node 1. Upon receiving messages from other nodes, node 1 can start the next transmission immediately after the CAN bus is released from receiving messages.

The transmission pause function is controlled by FDCAN_CCCR.TXP. When this bit is set to 1, after successfully sending a message, the FDCAN will pause for two CAN bit times before starting the next transmission. This allows other CAN nodes in the network to send messages with lower priority IDs. The transmission pause is disabled by default (FDCAN_CCCR.TXP = 0b).

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This feature can make burst transmissions from a single node more relaxed, preventing situations where the application erroneously requests excessive transmissions.

41.4.3.2 Dedicated Transmit Buffer

Dedicated transmit buffers are used for message transmission fully controlled by the host CPU. Each dedicated transmit buffer is configured with a specific message ID. If multiple transmit buffers are configured with the same message ID, the one with the lowest number will transmit first.

If the data section has been updated, a transmission request can be issued using FDCAN_TXBAR.ARn. The requested message will internally arbitrate with the messages in the configurable transmit FIFO/transmit queue and externally arbitrate with the messages on the CAN bus, and then be transmitted based on its message ID.

The size of dedicated transmit buffer elements is in words (32 bits). The starting address of the dedicated transmit buffer in the message RAM can be calculated by multiplying the transmit buffer index FDCAN_TXFQS.TFQPI (0…31) by the element size and then adding it to the transmit buffer start address FDCAN_TXBC.TBSA.

Table 41-12 Dedicated Transmit Buffer, Transmit FIFO/Queue Element Size

TXESC.TBDS[2:0]	Element Size (RAM Words)	Element Size (RAM Words)
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

41.4.3.3 Transmit FIFO

The transmission FIFO function can be enabled by clearing FDCAN_TXBC.TFQM. Messages stored in the transmit FIFO are sent starting from the message referenced by the get index FDCAN_TXFQS.TFGI. After each transmission, the get index is incremented cyclically until the transmit FIFO is empty. The transmit FIFO allows messages with the same ID to be sent from different transmit buffers in the order they were written into the transmit FIFO. FDCAN calculates the transmit FIFO fill level FDCAN_TXFQS.TFFL by the difference between the get index and the write index, indicating the number of available (idle) transmit FIFO elements.

New transmit messages must be written to the transmit buffer referenced by the write index FDCAN_TXFQS.TFQPI. Adding a request will increment the write index to the next available transmit FIFO element. When the write index reaches the get index, the transmit FIFO full flag (FDCAN_TXFQS.TFQF) is set to 1. At this point, do not continue writing messages to the transmit FIFO until the next message has been sent and the get index has been incremented.

When a message is added to the transmit FIFO, a request for transmission is made by writing a 1 to the FDCAN_TXBAR bit corresponding to the transmit buffer referenced by the transmit FIFO write index.

When multiple (n) messages are added to the transmit FIFO, they will be written into n consecutive transmit buffers

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starting from the write index. The transmit request can be made through FDCAN_TXBAR. Subsequently, the write index will increment cyclically n times. The number of requested transmit buffers should not exceed the number of available idle transmit buffers indicated by the transmit FIFO fill level.

When a transmission request from the transmit buffer referenced by the get index is canceled, the get index will increment to the next transmit buffer with a pending transmission request, and the transmit FIFO fill level will be recalculated.

If other transmit buffers' transmissions are canceled, the get index and FIFO fill level remain unchanged. The transmit FIFO element size is in words. The starting address of the next available (idle) transmit FIFO can be calculated by multiplying the transmit FIFO write index FDCAN_TXFQS.TFQPI (0…31) by the element size and then adding it to the transmit buffer start address FDCAN_TXBC.TBSA.

41.4.3.4 Transmission Queue

To enable the transmission queue function, set FDCAN_TXBC.TFQM to 1. Messages stored in the transmission queue will be sent starting from the message with the smallest message ID (highest priority).

If multiple queue buffers are configured with the same message ID, the buffer with the lowest number will transmit first. New messages must be written to the transmit buffer referenced by the write index FDCAN_TXFQS.TFQPI. Adding a transmission request will cyclically increment the write index to the next available transmit buffer. If the transmission queue is full (FDCAN_TXFQS.TFQF=1b), the write index is invalid, and new messages should not be written to the transmission queue until at least one message has been sent or a transmission request has been canceled.

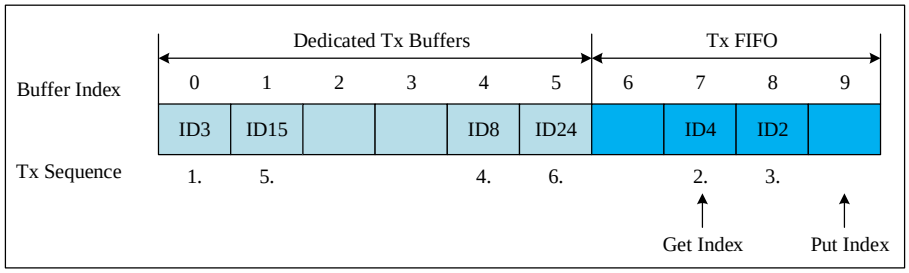
In the application, the register FDCAN_TXBRP can be used instead of the write index, allowing new messages to be written to any transmit buffer that does not have a pending request.

The transmission queue element size is in words. The starting address of the next available (idle) transmission queue can be calculated by multiplying the transmit queue write index FDCAN_TXFQS.TFQPI (0…31) by the element size and then adding it to the transmit buffer start address FDCAN_TXBC.TBSA.

41.4.3.5 Hybrid Use of Dedicated Transmit Buffers and Transmit FIFO

At this point, the transmit buffers in the message RAM are divided into a group of dedicated transmit buffers and a transmit FIFO. The number of dedicated transmit buffers is configured by FDCAN_TXBC.NDTB. The number of transmit buffers allocated to the transmit FIFO is configured by FDCAN_TXBC.TFQS. If TXBC.TFQS is 0, only dedicated transmit buffers are used.

Figure 41-12 FDCAN dedicated Tx Buffer and Tx FIFO Hybrid Configuration Example Diagram



The priority for transmission is as follows:

- Scan the dedicated transmit buffers and the earliest pending transmit FIFO buffer (the transmit buffer referenced

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Email: sales@nsing.com.sg

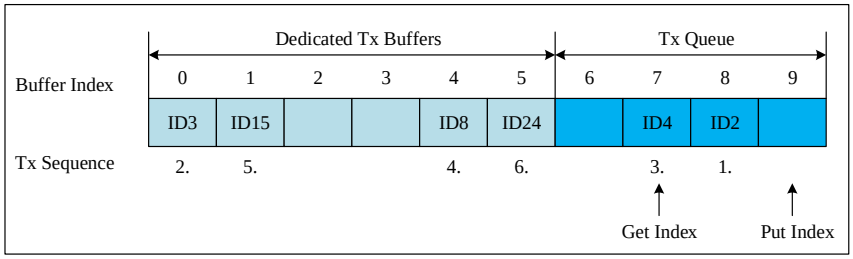
by FDCAN_TXFS.TFGI)

- The transmit buffer with the smallest ID has the highest priority and will be sent as the next message to transmit.

41.4.3.6 Hybrid Use of Dedicated Transmit Buffers and Transmit Queue

At this point, the transmit buffers in the message RAM are divided into a group of dedicated transmit buffers and a transmit queue. The number of dedicated transmit buffers is configured by FDCAN_TXBC.NDTB. The number of transmit buffers allocated to the transmit queue is configured by FDCAN_TXBC.TFQS. If TXBC.TFQS is set to zero, only dedicated transmit buffers are used.

Figure 41-13 FDCAN dedicated Tx Buffer and Tx Queue Hybrid Configuration Example Diagram



The priority for transmission is as follows:

- Scan all pending transmit buffers
- The transmit buffer with the smallest message ID has the highest priority and will be sent in the next transmission.

41.4.3.7 Transmission Cancellation

FDCAN supports transmission cancellation function. The host must write a 1 to the corresponding bit in the FDCAN_TXBCR register to cancel the transmission request from dedicated transmit buffers or transmit queue buffers. The transmission cancellation function does not apply to the transmit FIFO.

Upon successful cancellation, the corresponding positions in the FDCAN_TXBCF register are set to 1.

When canceling a message that is currently being sent, the corresponding FDCAN_TXBRP bit remains set to 1 until the transmission is completed or fails. If the transmission is successful, both the corresponding FDCAN_TXBTO and FDCAN_TXBCF bits will be set to 1. If the transmission fails, the message will not be retransmitted, and only the corresponding position in FDCAN_TXBCF will be set to 1.

Note: If a message is canceled immediately before starting transmission, a short idle window will occur, during which even if another message is waiting to be sent at that node, transmission will not start. This allows another node to send a message with lower priority than the second message in that node.

41.4.3.8 Transmission Event FIFO

FDCAN provides a Transmission Event FIFO to support transmission event handling. After sending a message on the CAN bus, the message ID and timestamp are stored in a Transmission Event FIFO element. To associate the transmission event with the Transmission Event FIFO element, the message tag from the sent message buffer is copied to the Transmission Event FIFO element. The Transmission Event FIFO can be configured with up to 32 elements.

The purpose of the Transmission Event FIFO is to separate the transmission status from the sent messages, where the

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transmit buffer only stores the messages to be sent, while the transmission status is stored separately in the Transmission Event FIFO. The advantage of this approach is that when handling dynamically managed transmission queues, the transmit buffer can be immediately used for new messages after a successful transmission. There is no need to retain the transmission status information of the transmit buffer before it is overwritten by a new message.

When the transmit event FIFO is full (FDCAN_IR.TEFF=1b), it is not possible to continue writing elements to the transmit event FIFO until at least one element is read out and the retrieval index of the transmit event FIFO has been incremented. If a transmit event occurs while the transmit event FIFO is full, this event will be discarded, and the interrupt flag FDCAN_IR.TEFL will be set to 1.

To prevent transmit event FIFO overflow, the transmit event FIFO watermark flag can be used. When the fill level of the transmit event FIFO reaches the transmit event FIFO watermark configured by FDCAN_TXEFC.EFWM, the interrupt flag FDCAN_IR.TEFW is set to 1.

When reading data from the transmit event FIFO, the starting address is obtained by multiplying the transmit event FIFO retrieval index FDCAN_TXEFS.EFGI by 2 and then adding it to the transmit event FIFO starting address FDCAN_TXEFC.EFSA.

41.4.4 FIFO acknowledgment

The retrieval indexes of Receive FIFO 0, Receive FIFO 1, and the Transmit Event FIFO are controlled by writing the corresponding FIFO acknowledgment indexes. After writing the FIFO acknowledgment index, the FIFO retrieval index will be set to the FIFO acknowledgment index value plus 1, and the FIFO fill level will be updated. Two scenarios may occur:

- When only a single element is read from the FIFO (i.e., the element pointed to by the retrieval index), this retrieval index value is written to the FIFO acknowledgment index.
- When a series of elements is read from the FIFO, simply write the FIFO acknowledgment index once at the end of the read sequence (the acknowledgment index value is the index of the last element read) to update the FIFO retrieval index.

Due to the CPU's unrestricted access to FDCAN's message RAM, special attention is required when reading FIFO elements in any order (without considering the retrieval index). This operation may be particularly useful when reading high-priority messages from one of the two Receive FIFOs. In this scenario, do not write the FIFO acknowledgment index, as doing so would set the retrieval index to an incorrect position and alter the FIFO fill level, resulting in the loss of some earlier FIFO elements.

Note: The application must ensure that the written FIFO acknowledgment index value is valid. FDCAN will not check whether the written value is correct.

41.4.5 Bit Timing

The bit timing logic monitors the serial bus, performs data sampling, and adjusts the sampling point by synchronizing at the start bit edge and resynchronizing at subsequent bit edges. Its operation can be simplified by dividing the bit time into three time segments, as follows:

- Synchronization Segment (SYNC_SEG): The time segment expected to have bit transitions, with a fixed length

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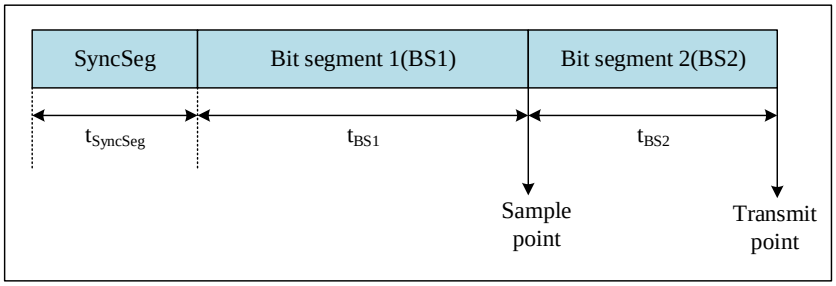
Email: sales@nsing.com.sg

of one time quantum (1×tq).

- Bit Segment 1 (BS1): Defines the position of the sampling point, including the PROP_SEG and PHASE_SEG1 as defined in the CAN standard, with a configurable duration between 1 to 16 time quanta, automatically extended to compensate for positive phase drift caused by frequency differences between nodes.
- Bit Segment 2 (BS2): Defines the position of the transmission point, namely the PHASE_SEG2 as defined in the CAN standard, with a configurable duration between 1 to 8 time quanta, automatically shortened to compensate for negative phase drift.

Figure 41-14 FDCAN Bit Timing



The baud rate is the reciprocal of the bit time (baud rate = 1/bit time), and the bit time is the sum of three time segments. As shown in the figure above, the bit time = $t_{SyncSeg} + t_{BS1} + t_{BS2}$, where:

- Nominal Bit Time
  - tq = (FDCAN_NBTP.NBRP[8:0] + 1) * $t_{fdcan_tq_ck}$
  - $t_{SyncSeg}$ = 1*tq
  - t_{BS1} = tq * (FDCAN_NBTP.NTSEG1[7:0] + 1)
  - t_{BS2} = tq * (FDCAN_NBTP.NTSEG2[6:0] + 1)
- Data Bit Time
  - tq = (FDCAN_DBTP. DBRP [4:0] + 1) * tfdcan_tq_ck
  - tSyncSeg = 1*tq
  - tBS1 = tq * (FDCAN_DBTP. DTSEG1 [4:0] + 1)
  - tBS2 = tq * (FDCAN_DBTP. DTSEG2 [3:0] + 1)

The (re)Synchronization Jump Width (SJW) defines the upper limit for extending or shortening time segments and can be configured between 1 to 128 time quanta.

An effective edge is defined as the first transition of the bus from a recessive level to a dominant level within one bit time, provided that the node itself does not transmit a dominant bit.

If an effective edge is detected in BS1 instead of in SYNC_SEG, BS1 can extend up to SJW at most, causing a delay in the sampling point. Conversely, if an effective edge is detected in BS2, BS2 can shorten SJW at most, advancing the transmission point.

To prevent programming errors, the bit timing registers can only be configured when the device is in standby mode. The FDCAN_DBTP and FDCAN_NBTP registers (dedicated to data and nominal bit timing, respectively) can only

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

be accessed when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

Note: For detailed information on CAN bit timing and resynchronization mechanisms, please refer to the ISO 11898-1 standard.

41.5 TTCAN Function Description

41.5.1 Reference message

A reference message is a data frame characterized by a specific CAN identifier. It is received and accepted by all nodes except the time master (sender of the reference message).

For level 1 the data length must be at least one; for level 0, 2 the data length must be at least four; otherwise, the message is not accepted as reference message. The reference message may be extended by other data up to the sum of eight CAN data bytes. All bits of the identifier except the three LSBs characterize the message as a reference message. The last three bits specify the priorities of up to eight potential time masters. Reserved bits are transmitted as logical 0 and are ignored by the receivers. The reference message is configured via register FDCAN_TTRMC.

The time master transmits the reference message. If the reference message is disturbed by an error, it is retransmitted immediately. In case of a retransmission, the transmitted Master_Ref_Mark is updated. The reference message is sent periodically, but is allowed to stop the periodic transmission (Next_is_Gap bit) and to initiate transmission eventsynchronized at the start of the next basic cycle by the current time master or by one of the other potential time masters.

The node transmitting the reference message is the current time master. The time master is allowed to transmit other messages. If the current time master fails, its function is replicated by the potential time master with the highest priority. Nodes that are neither time master nor potential time master are time-receiving nodes.

41.5.1.1 Level 1

Level 1 operation is configured via FDCAN_TTOCF.OM = 01 and FDCAN_TTOCF.GEN. External clock synchronization is not available in level 1. The information related to the reference message is stored in the first data byte as shown in Table 41-13. Cycle_Count is optional.

Table 41-13 First byte of level 1 reference message

Bits	0	1	2	3	4	5	6	7
First byte	Next_is_Gap	Reserved	Cycle_Count[5:0]					

41.5.1.2 Level 2

Level 2 operation is configured via FDCAN_TTOCF.OM = 10 and FDCAN_TTOCF.GEN. The information related to the reference message is stored in the first four data bytes as shown in Table 41-14. Cycle_Count and the lower four bits of NTU_Res are optional. The TTCAN does not evaluate NTU_Res[3:0] from received reference messages, it always transmits these bits as 0.

Table 41-14 First four bytes of level 2 reference message

Bits	0	1	2	3	4	5	6	7
First byte	Next_is_Gap	Reserved	Cycle_Count[5:0]					

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Second byte	NTU_Res[6:4]	NTU_Res[3:0]	Disc_Bit
Third byte	Master_Ref_Mark[7:0]		
Fourth byte	Master_Ref_Mark[15:8]		

41.5.1.3 Level 0

Level 0 operation is configured via FDCAN_TTOCF.OM = 11. External event-synchronized time-triggered operation is not available in level 0. The information related to the reference message is stored in the first four data bytes as shown in the table below. In level 0 Next_is_Gap is always 0. Cycle_Count and the lower four bits of NTU_Res are optional. The TTCAN does not evaluate NTU_Res[3:0] from received reference messages, it always transmits these bits as 0.

Table 41-15 First four bytes of level 0 reference message

Bits	0	1	2	3	4	5	6	7
First byte	Next_is_Gap	Reserved	Cycle_Count[5:0]					
Second byte	NTU_Res[6:4]			NTU_Res[3:0]				Disc_Bit
Third byte	Master_Ref_Mark[7:0]							
Fourth byte	Master_Ref_Mark[15:8]							

41.5.2 TTCAN configuration

41.5.2.1 TTCAN timing

The network time unit (NTU) is the unit in which all times are measured. The NTU is a constant of the whole network and is defined as a priority by the network system designer. In TTCAN level 1 the NTU is the nominal CAN bit time. In TTCAN level 0 and level 2 the NTU is a fraction of the physical second.

The NTU is the time base for the local time. The integer part of the local time (16-bit value) is incremented once each NTU. Cycle time and global time are both derived from local time. The fractional part (3-bit value) of local time, cycle time, and global time is not readable.

In TTCAN level 0 and level 2 the length of the NTU is defined by the time unit Ratio TUR. The TUR is in general a non-integer number, given by

TUR = FDCAN_TURNA.NAV / FDCAN_TURCF.DC.

The NTU length is given by

NTU = CAN clock period x TUR.

The TUR numerator configuration NC is an 18-bit number, FDCAN_TURCF.NCL[15:0] can be programmed in the range 0x0000–0xFFFF. FDCAN_TURCF.NCH[17:16] is hard wired to 0b01. When 0xnnnn is written to FDCAN_TURCF.NCL[15:0], FDCAN_TURNA.NAV starts with the value 0x10000 + 0x0nnnn = 0x1nnnn. The TUR denominator configuration FDCAN_TURCF.DC is a 14-bit number. FDCAN_TURCF.DC may be programmed in the range 0x0001 - 0x3FFF (0x0000 is an illegal value).

In level 1, NC must be equal or higher than 4 x FDCAN_TURCF.DC. In level 0 and level 2 NC must be equal or higher than 8 x FDCAN_TURCF.DC to get the 3-bit resolution for the internal fractional part of the NTU.

A hardware reset presets FDCAN_TURCF.DC to 0x1000 and FDCAN_TURCF.NCL to 0x10000, resulting in an

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

NTU consisting of sixteen CAN clock periods. Local time and application watchdog are not started before either the FDCAN_CCCR.INIT is reset, or FDCAN_TURCF.ELT is set. FDCAN_TURCF.ELT may not be set before the NTU is configured. Setting FDCAN_TURCF.ELT to 1 also locks the write access to register FDCAN_TURCF.

At startup FDCAN_TURNA.NAV is updated from NC (= FDCAN_TURCF.NCL + 0x10000) when FDCAN_TURCF.ELT is set. In TTCAN level 1 there is no drift compensation. FDCAN_TURNA.NAV does not change during operation, it is always equal to NC.

In TTCAN level 0 and level 2 there are two possibilities for FDCAN_TURNA.NAV to change. When operating as time slave or backup time master, and when FDCAN_TTOCF.ECC is set, FDCAN_TURNA.NAV is updated automatically to the value calculated from the monitored global time speed, as long as the TTCAN is in synchronization state In_Schedule or In_Gap. When it loses synchronization, it returns to NC. When operating as the actual time master, and when FDCAN_TTOCF.EECS is set, the Host may update FDCAN_TURCF.NCL. When the Host sets FDCAN_TTOCN.ECS, FDCAN_TURNA.NAV will be updated from the new value of NC at the next reference message. The status flag FDCAN_TTOST.WECS as is set when FDCAN_TTOCN.ECS is set and is cleared when FDCAN_TURNA.NAV is updated. FDCAN_TURCF.NCL is write locked while FDCAN_TTOST.WECS is set.

In TTCAN level 0 and level 2 the clock calibration process adapts FDCAN_TURNA.NAV in the range of the synchronization deviation limit SDL of NC ± 2^(FDCAN_TTOCF.LDSDL + 5). FDCAN_TURCF.NCL should be programmed to the largest applicable numerical value in order to achieve the best accuracy in the calculation of FDCAN_TURNA.NAV.

The synchronization deviation SD is the difference between NC and FDCAN_TURNA.NAV (SD = |NC - FDCAN_TURNA.NAV|). It is limited by the synchronization deviation limit SDL, which is configured by its dual logarithm FDCAN_TTOCF.LDSDL (SDL = 2^ (FDCAN_TTOCF.LDSDL + 5)) and should not exceed the clock tolerance given by the CAN bit timing configuration. SD is calculated at each new basic cycle. When the calculated FDCAN_TURNA.NAV deviates by more than SDL from NC, or if the Disc_Bit in the reference message is set, the drift compensation is suspended and FDCAN_TTIR.GTE is set and FDCAN_TTOSC.QCS is reset, or in case of the Disc_Bit = 1, FDCAN_TTIR.GTD is set.

Table 41-16 TUR configuration example

TUR	8	10	24	50	510	125000	32.5	100/12	529/17
NC	0x1FFF8	0x1FFFE	0x1FFF8	0x1FFEA	0x1FFFE	0x1E848	0x1FFE0	0x19000	0x10880
FDCAN_TURCF.DC	0x3FFF	0x3333	0x1555	0x0A3D	0x0101	0x0001	0x0FC0	0x3000	0x0880

FDCAN_TTOCN.ECS schedules NC for activation by the next reference message. FDCAN_TTOCN.SGT schedules FDCAN_TTGTP.TP for activation by the next reference message. Setting FDCAN_TTOCN.ECS and FDCAN_TTOCN.SGT requires FDCAN_TTOCF.EECS to be set (external clock synchronization enabled) while the FDCAN is actual time master.

The TTCAN module provides an application watchdog to verity the function of the application program. The Host has to serve this watchdog regularly, else all CAN bus activity is stopped. The application watchdog limit FDCAN_TTOCF.AWL specifies the number of NTUs between two times the watchdog has to be served. The maximum number of NTUs is 256. The application watchdog is served by reading register FDCAN_TTOST.

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Email: sales@nsing.com.sg

FDCAN_TTOST.AWE indicates whether the watchdog has been served in time. In case the application failed to serve the application watchdog, interrupt flag FDCAN_TTIR.AW is set. For software development, the application watchdog may be disabled by programming FDCAN_TTOCF.AWL to 0x00, see section 41.6.49.

41.5.2.1.1 Timing of interface signals

The timing events that cause a pulse at output FDCAN trigger time mark interrupt pulse fdcan1_tmp for more than one instance and fdcan_tmp if only one instance; FDCAN register time mark interrupt pulse fdcan1_rtp for more than one instance and fdcan_rtp if only one instance are generated in the CAN clock domain.

There is a clock domain crossing delay to be considered before the same event is visible in the APB clock domain (when FDCAN_TTIR.TTMI is set or FDCAN_TTIR.RTMI is set). As an example, the signals can be connected to the timing input(s) of another FDCAN node (fdcan_swt/fdcan_evt), in order to automatically synchronize two TTCAN networks.

Output fdcan_soc gets active whenever a reference message is completed (either transmitted or received). The output is controlled in the Host cloc k domain.

41.5.2.2 Message scheduling

FDCAN_TTOCF.TM controls whether the TTCAN operates as potential time master or as a time slave. If it is a potential time master, the three LSBs of the reference message identifier FDCAN_TTRMC.RID define the master priority, 0 giving the highest and 7 giving the lowest. There cannot be two nodes in the network using the same master priority. FDCAN_TTRMC.RID is used for recognition of reference messages. FDCAN_TTRMC.RMPS is not relevant for time slaves.

The initial reference trigger offset FDCAN_TTOCF.IRTO is a 7-bit-value that defines (in NTUs) how long a backup time master waits before it starts the transmission of a reference message when a reference message is expected but the bus remains idle. The recommended value for FDCAN_TTOCF.IRTO is the master priority multiplied with a factor depending on the expected clock drift between the potential time masters in the network. The sequential order of the backup time masters, when one of them starts the reference message in case the current time master fails, should correspond to their master priority, even with maximum clock drift.

FDCAN_TTOCF.OM decides whether the node operates in TTCAN level 0, level 1, or level 2. In one network, all potential time masters have to operate on the same level. Time slaves may operate on level 1 in a level 2 network, but not vice versa. The configuration of the TTCAN operation mode via FDCAN_TTOCF.OM is the last step in the setup. With FDCAN_TTOCF.OM = 00 (event-driven CAN communication), the FDCAN operates according to ISO 11898-1: 2015, without time triggers.With FDCAN_TTOCF.OM = 01 (level 1), the FDCAN operates according to ISO 11898-4, but without the possibility to synchronize the basic cycles to external events, the Next_is_Gap bit in the reference message is ignored. With FDCAN_TTOCF.OM = 10 (level 2), the TTCAN operates according to ISO 11898-4, including the event-synchronized start of a basic cycle. With FDCAN_TTOCF.OM = 11 (level 0), the FDCAN operates as event-driven CAN but maintains a calibrated global time base as in level 2.

FDCAN_TTOCF.EECS enables the external clock synchronization, allowing the application program of the current time master to update the TUR configuration during time-triggered operation, to adapt the clock speed and (in levels 0 and level 2 only) the global clock phase to an external reference.

FDCAN_TTMLM.ENTT in the TT matrix limits register specifies the number of expected Tx_Triggers in the system matrix. This is the sum of Tx_Triggers for exclusive, single arbitrating and merged arbitrating windows, excluding

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

the Tx_Ref_Triggers. Note that this is usually not the number of Tx_Trigger memory elements; the number of basic cycles in the system matrix and the trigger repeat factors have to be taken into account.

An inaccurate configuration of FDCAN_TTMLM.ENTT will result either in a TxCount Underflow (FDCAN_TTIR.TXU = 1 and FDCAN_TTOST.EL = 01, severity 1), or in a Tx count Overflow (FDCAN_TTIR.TXO = 1 and FDCAN_TTOST.EL = 10, severity 2).

Note: In case the first reference message seen by a node does not have Cycle_Count 0, this node may finish its first matrix cycle with its Tx count resulting in a Tx count underflow condition. As long as a node is in state Synchronizing its Tx_Triggers will not lead to transmissions.

FDCAN_TTMLM.CCM specifies the number of the last basic cycle in the system matrix. The counting of basic cycles starts at 0. In a system matrix consisting of eight basic cycles FDCAN_TTMLM.CCM would be 7. FDCAN_TTMLM.CCM is ignored by time slaves, a receiver of a reference message considers the received cycle count as the valid cycle count for the actual basic cycle.

FDCAN_TTMLM.TXEW specifies the length of the Tx enable window in NTUs. The Tx enable window is that period of time at the beginning of a time window where a transmission may be started. If a transmission of a message cannot be started inside the Tx enable window because of for example, a slight overlap from the previous time window message, the transmission cannot be started in that time window at all. FDCAN_TTMLM.TXEW has to be chosen with respect to the network synchronization quality and with respect to the relation between the length of the time windows and the length of the messages.

41.5.2.3 Trigger memory

The trigger memory is part of the external message RAM to which the TTCAN is connected to (see Section 41.6.26). It stores up to 64 trigger elements. A trigger memory element consists of time mark TM, cycle code CC, trigger type TYPE, filter type FTYPE, message Number MNR, message status count MSC, time mark event internal TMIN, time mark event external TMEX (see Section 41.3.7).

The time mark defines at which cycle time a trigger becomes active. The triggers in the trigger memory have to be sorted by their time marks. The trigger element with the lowest time mark is written to the first trigger memory word. Message number and cycle code are ignored for triggers of type Tx_Ref_Trigger, Tx_Ref_Trigger_Gap, Watch_Trigger, Watch_Trigger_Gap, and End_of_List.

When the cycle time reaches the time mark of the actual trigger, the FSE switches to the next trigger and starts to read the following trigger from the trigger memory. In case of a transmit trigger, the Tx handler starts to read the message from the message RAM as soon as the FSE switches to its trigger. The RAM access speed defines the minimum time step between a transmit trigger and its preceding trigger, the Tx handler has to be able to prepare the transmission before the transmit trigger time mark is reached. The RAM access speed also limits the number of non-matching (with regard to their cycle code) triggers between two matching triggers, the next matching trigger must be read before its time mar k is reached. If the reference message is n NTU long, a trigger with a time mark lower than n will never become active and will be treated as a configuration error.

Starting point of the cycle time is the sample point of the reference message start of frame bit. The next reference message is requested when cycle time reaches the Tx_Ref_Trigger time mark. The FDCAN reacts on the transmission request at the next sample point. A new Sync_Mark is captured at the start of frame bit, but the cycle time is incremented until the reference message is successfully transmitted (or received) and the Sync_Mark is taken as the new Ref_Mark. At that point in time, cycle time is restarted. As a consequence, cycle time can never (with the

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

exception of initialization) be seen at a value lower than n, with n being the length of the reference message measured in NTU.

Length of a basic cycle: Tx_Ref_Trigger time mark + 1 NTU + 1 CAN bit time.

The trigger list will be different for all nodes in the FDCAN network. Each node knows only the Tx_Triggers for its own transmit messages, the Rx_Triggers for those receive messages that are processed by this node, and the triggers concerning the reference messages.

41.5.2.3.1 Trigger types

Tx_Ref_Trigger (TYPE = 0000) and Tx_Ref_Trigger_Gap (TYPE = 0001) cause the transmission of a reference message by a time master. A configuration error (FDCAN_TTOST.EL = 11, severity 3) is detected when a time slave encounters a Tx_Ref_Trigger(_Gap) in its trigger memory. Tx_Ref_Trigger_Gap is only used in external event-synchronized time-triggered operation mode. In that mode, Tx_Ref_Trigger is ignored when the FDCAN synchronization state is In_Gap (FDCAN_TTOST.SYS = 10).

Tx_Trigger_Single (TYPE = 0010), Tx_Trigger_Continuous (TYPE = 0011), Tx_Trigger_Arbitration (TYPE = 0100), and Tx_Trigger_Merged (TYPE = 0101) cause the start of a transmission. They define the start of a time window.

Tx_Trigger_Single starts a single transmission in an exclusive time window when the message buffer transmission request pending bit is set. After successful transmission the transmission request pending bit is reset.

Tx_Trigger_Continuous starts a transmission in an exclusive time window when the message buffer transmission request pending bit is set. After successful transmission the transmission request pending bit remains set, and the message buffer is transmitted again in the next matching time window.

Tx_Trigger_Arbitration starts an arbitrating time window, Tx_Trigger_Merged a merged arbitrating time window. The last Tx_Trigger of a merged arbitrating time window must be of type Tx_Trigger_Arbitration. A configuration error (FDCAN_TTOST.EL = 11, severity 3) is detected when a trigger of type Tx_Trigger_Merged is followed by any other Tx_Trigger than one of type Tx_Trigger_Merged or Tx_Trigger_Arbitration. Several Tx_Triggers may be defined for the same Tx message buffer. Depending on their cycle code, they may be ignored in some basic cycles. The cycle code has to be considered when the expected number of Tx_Triggers (FDCAN_TTMLM.ENTT) is calculated.

Watch_Trigger (TYPE = 0110) and Watch_Trigger_Gap (TYPE = 0111) check for missing reference messages. They are used by both time masters and time slaves.

Watch_Trigger_Gap is only used in external event-synchronized time-triggered operation mode. In that mode, a Watch_Trigger is ignored when the FDCAN synchronization state is In_Gap (FDCAN_TTOST.SYS = 10).

Rx_Trigger (TYPE = 1000) is used to check for the reception of periodic messages in exclusive time windows. Rx_Triggers are not active until state In_Schedule or In_Gap is reached. The time mark of an Rx_Trigger shall be placed after the end of that message transmission, independent of time window boundaries. Depending on their cycle code, Rx_Triggers may be ignored in some basic cycles. At the time mark of the Rx_Trigger, it is checked whether the last received message before this time mark and after start of cycle or previous Rx_Trigger had matched the acceptance filter element referenced by MNR. Accepted messages are stored in one of the two receive FIFOs, according to the acceptance filtering, independent of the Rx_Trigger. Acceptance filter elements referenced by Rx_Triggers should be placed at the beginning of the filter list to ensure that the filtering is finished before the

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Email: sales@nsing.com.sg

Rx_Trigger time mark is reached.

Time_Base_Trigger (TYPE = 1001) are used to generate internal/external events depending on the configuration of TMIN and TMEX.

End_of_List (TYPE = 1010 … 1111) is an illegal trigger type, a configuration error (FDCAN_TTOST.EL = 11, severity 3) is detected when an End_of_List trigger is encountered in the trigger memory before the Watch_Trigger and Watch_Trigger_Gap.

41.5.2.3.2 Restrictions for the node trigger list

There may not be two triggers that are active at the same cycle time and cycle count, but triggers that are active in different basic cycles (different cycle code) may share the same time mark.

Rx_Triggers and Time_Base_Triggers may not be placed inside the Tx enable windows of Tx_Trigger_Single/Continuous/Arbitration, but they may be placed after Tx_Trigger_Merged.

Triggers that are placed after the Watch_Trigger (or the Watch_Trigger_Gap when FDCAN_TTOST.SYS = 10) will never become active. The watch triggers themselves will not become active when the reference messages are transmitted on time.

All unused trigger memory words (after the Watch_Trigger or after the Watch_Trigger_Gap when FDCAN_TTOST.SYS = 10) must be set to trigger type End_of_List.

A typical trigger list for a potential time master will begin with a number of Tx_Triggers and Rx_Triggers followed by the Tx_Ref_Trigger and the Watch_Trigger. For networks with external event- synchronized time-triggered communication, this is followed by the Tx_Ref_Trigger_Gap and the Watch_Trigger_Gap. The trigger list for a time slave will be the same but without the Tx_Ref_Trigger and the Tx_Ref_Trigger_Gap.

At the beginning of each basic cycle, that is at each reception or transmission of a reference message, the trigger list is processed starting with the first trigger memory element. The FSE looks for the first trigger with a cycle code that matches the current cycle count. The FSE waits until cycle time reaches the trigger time mark and activates the trigger.

Afterwards the FSE looks for the next trigger in the list with a cycle code that matches the current cycle count.

Special consideration is needed for the time around Tx_Ref_Trigger and Tx_Ref_Trigger_Gap. In a time master competing for master ship, the effective time mark of a Tx_Ref_Trigger may be decremented in order to be the first node to start a reference message. In backup time masters the effective time mark of a Tx_Ref_Trigger or Tx_Ref_Trigger_Gap is the sum of its configured time mark and the reference trigger offset FDCAN_TTOCF.IRTO. In case error level 2 is reached (FDCAN_TTOST.EL = 10), the effective time mark is the sum of its time mark and 0x127. No other trigger elements should be placed in this range otherwise it may happen that the time marks appear out of order and are flagged as a configuration error. Trigger elements which are coming after Tx_Ref_Trigger may never become active as long as the reference messages come in time.

There are interdependencies between the following parameters:

- APB clock frequency
- Speed and waiting time for trigger RAM accesses
- Length of the acceptance filter list
- Number of trigger elements

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

- Complexity of cycle code filtering in the trigger elements
- Offset between time marks of the trigger elements

41.5.2.3.3 Example for trigger handling

The example shows how the trigger list is derived from a node system matrix. Assumption is that node A is first time master and has knowledge of the section of the system matrix shown in Table 41-17.

Table 41-17 System matrix, Node A

Cycle count	Time mark						
	1	2	3	4	5	6	7
0	Tx7	-	-	-	-	TxRef	Error
1	Rx3	-	Tx2, Tx4		-	TxRef	Error
2	-	-	-	-	-	TxRef	Error
3	Tx7	-	Rx5	-	-	TxRef	Error
4	Tx7	-	-	Rx6	-	TxRef	Error

The cycle count starts with 0 and runs until 0, 1, 3, 7, 15, 31, 63 (the corresponding number of basic cycles in the system matrix is, respectively, 1, 2, 4, 8, 16, 32, 64). The maximum cycle count is configured by FDCAN_TTMLM.CCM. The cycle code CC is composed of repeat factor (= value of most significant 1) and the number of the first basic cycle in the system matrix (= bit field after most significant 1).

As an example, with a cycle code of 0b0010011 (repeat factor = 16, first basic cycle = 3) and a maximum cycle count of FDCAN_TTMLM.CCM = 0x3F matches occur at cycle counts 3, 19, 35 and 51.

A trigger element consists of time mark TM, cycle code CC, trigger type TYPE, and message Number MNR. For transmission MNR references the Tx buffer number (0 ... 31). For reception MNR references the number of the filter element (0 ... 127) that matched during acceptance filtering. Depending on the configuration of the filter type FTYPE, the 11-bit or 29-bit message ID filter list is referenced.

Table 41-18 Trigger list, Node A

Trigger	Time mark TM[15:0]	Cycle code CC [6:0]	Trigger type TYPE [3:0]	Mess No. MNR [6:0]
0	Mark 1	0b0000100	Tx_Trigger_Single	7
1	Mark 1	0b1000000	Rx_Trigger	3
2	Mark 1	0b1000011	Tx_Trigger_Single	7
3	Mark 3	0b1000001	Tx_Trigger_Merged	2
4	Mark 3	0b1000011	Rx_Trigger	5
5	Mark 4	0b1000001	Tx_Trigger_Arbitration	4
6	Mark 4	0b1000100	Rx_Trigger	6
7	Mark 6	N/A	Tx_Ref_Trigger	0(Ref)
8	Mark 7	N/A	Watch_Trigger	N/A

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9	N/A	N/A	End_of_List	N/A

Tx_Trigger_Single, Tx_Trigger_Continuous, Tx_Trigger_Merged, Tx_Trigger_Arbitration, Rx_Trigger, and Time_Base_Trigger are only valid for the specified cycle code. For all other trigger types the cycle code is ignored.

The FSE starts the basic cycle with scanning the trigger list starting from 0 until a trigger with time mark higher than cycle time and with its cycle code CC matching the actual cycle count is reached, or a trigger of type Tx_Ref_Trigger, Tx_Ref_Trigger_Gap, Watch_Trigger, or Watch_Trigger_Gap is encountered.

When the cycle time reached the time mark TM, the action defined by trigger type TYPE and message Number MNR is started. There is an error in the configuration when End_of_List is reached.

At mark 6 the reference message (always TxRef) is transmitted. After transmission of the reference message the FSE returns to the beginning of the trigger list. When the watch trigger at mark 7 is reached, the node was not able to transmit the reference message; error treatment is started.

41.5.2.3.4 Detection of configuration errors

A configuration error is signaled via FDCAN_TTOST.EL = 11 (severity 3) when:

- The FSE comes to a trigger in the list with a cycle code that matches the current cycle count but with a time mark that is less than the cycle time.
- The previous active trigger was a Tx_Trigger_Merged and the FSE comes to a trigger in the list with a cycle code that matches the current cycle count but that is neither a Tx_Trigger_Merged nor a Tx_Trigger_Arbitration nor a Time_Base_Trigger nor an Rx_Trigger.
- The FSE of a node with FDCAN_TTOCF.TM=0 (time slave) encounters a Tx_Ref_Trigger or a Tx_Ref_Trigger_Gap.
- Any time mark placed inside the Tx enable window (defined by FDCAN_TTMLM.TXEW) of a Tx_Trigger with a matching cycle code.
- A time mark is placed near the time mark of a Tx_Ref_Trigger and the reference trigger offset FDCAN_TTOST.RTO causes a reversal of their sequential order measured in cycle time.

41.5.2.4 Schedule initialization

The synchronization to the TTCAN message schedule starts when FDCAN_CCCR.INIT is reset. The TTCAN can operate strictly time-triggered (FDCAN_TTOCF.GEN = 0) or external event-synchronized time-triggered (FDCAN_TTOCF.GEN = 1). All nodes start with cycle time 0 at the beginning of their trigger list with FDCAN_TTOST.SYS = 00 (out of synchronization), no transmission is enabled with the exception of the reference message. Nodes in external event-synchronized time-triggered operation mode will ignore Tx_Ref_Trigger and Watch_Trigger and will use instead Tx_Ref_Trigger_Gap and Watch_Trigger_Gap until the first reference message decides whether a Gap is active.

41.5.2.4.1 Time slaves

After configuration, a time slave will ignore its Watch_Trigger and Watch_Trigger_Gap when it did not receive any message before reaching the Watch_Triggers. When it reaches Init_Watch_Trigger, interrupt flag FDCAN_TTIR.IWT is set, the FSE is frozen, and the cycle time will become invalid, but the node will still be able to take part in CAN bus communication (to acknowledge or to send error flags). The first received reference message

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

will restart the FSE and the cycle time.

Note: Init_Watch_Trigger is not part of the trigger list. It is implemented as an internal counter that counts up to 0xFFFF = maximum cycle time.

When a time slave has received any message but the reference message before reaching the Watch_Triggers, it will assume a fatal error (FDCAN_TTOST.EL = 11, severity 3), set interrupt flag FDCAN_TTIR.WT, switch off its CAN bus output, and enter the bus monitoring mode (FDCAN_CCCR.MON set to 1). In the bus monitoring mode it is still able to receive messages, but it cannot send any dominant bits and therefore cannot give acknowledge.

Note: To leave the fatal error state, the Host has to set FDCAN_CCCR.INIT = 1. After reset of FDCAN_CCCR.INIT, the node restarts TTCAN communication.

When no error is encountered during synchronization, the first reference message sets FDCAN_TTOST.SYS = 01 (Synchronizing), the second sets the FDCAN synchronization state (depending on its Next_is_Gap bit) to FDCAN_TTOST.SYS = 11 (In_Schedule) or FDCAN_TTOST.SYS = 10 (In_Gap), enabling all Tx_Triggers and Rx_Triggers.

41.5.2.4.2 Potential time masters

After configuration, a potential time master will start the transmission of a reference message when it reaches its Tx_Ref_Trigger (or its Tx_Ref_Trigger_Gap when in external event-synchronized time-triggered operation). It will ignore its Watch_Trigger and Watch_Trigger_Gap when it did not receive any message or transmit the reference message successfully before reaching the Watch_Triggers (assumed reason: all other nodes still in reset or configuration, giving no acknowledge). When it reaches Init_Watch_Trigger, the attempted transmission is aborted, interrupt flag FDCAN_TTIR.IWT is set, the FSE is frozen, and the cycle time will become invalid, but the node will still be able to take part in CAN bus communication (to give acknowledge or to send error flags). Resetting FDCAN_TTIR.IWT will re-enable the transmission of reference messages until next time the Init_Watch_Trigger condition is met, or another CAN message is received. The FSE will not be restarted by the reception of a reference message.

When a potential time master reaches the Watch_Triggers after it has received any message but the reference message, it will assume a fatal error (FDCAN_TTOST.EL = 11, severity 3), set interrupt flag FDCAN_TTIR.WT, switch off its CAN bus output, and enter the bus monitoring mode (FDCAN_CCCR.MON set to 1). In bus monitoring mode, it is still able to receive messages, but cannot send any dominant bits and therefore cannot give acknowledge.

When no error is detected during initialization, the first reference message sets FDCAN_TTOST.SYS = 01 (synchronizing), the second sets the FDCAN synchronization state (depending on its Next_is_Gap bit) to FDCAN_TTOST.SYS = 11 (In_Schedule) or FDCAN_TTOST.SYS = 10 (In_Gap), enabling all Tx_Triggers and Rx_Triggers.

A potential time master is current time master (FDCAN_TTOST.MS = 11) when it was the transmitter of the last reference message, else it is backup time master (FDCAN_TTOST.MS = 10).

When all potential time masters have finished configuration, the node with the highest time master priority in the network will become the current time master.

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Email: sales@nsing.com.sg

41.5.3 TTCAN gap control

All functions related to Gap control apply only when the FDCAN is operated in external event synchronized time-triggered mode (FDCAN_TTOCF.GEN = 1). In this operation mode the FDCAN message schedule may be interrupted by inserting Gaps between the basic cycles of the system matrix. All nodes connected to the CAN network have to be configured for external event- synchronized time-triggered operation.

During a Gap, all transmissions are stopped and the CAN bus remains idle. A Gap is finished when the next reference message starts a new basic cycle. A Gap starts at the end of a basic cycle that itself was started by a reference message with bit Next_is_Gap = 1 e.g. Gaps are initiated by the current time master.

The current time master has two options to initiate a Gap. A Gap can be initiated under software control when the application program writes FDCAN_TTOCN.NIG = 1. The Next_is_Gap bit will be transmitted as 1 with the next reference message. A Gap can also be initiated under hardware control when the application program enables the event trigger input pin fdcan_evt by writing FDCAN_TTOCN.GCS = 1. When a reference message is started and FDCAN_TTOCN.GCS is set, a HIGH level at event trigger pin fdcan_evt will set Next_is_Gap = 1.

As soon as that reference message is completed, the FDCAN_TTOST.WFE bit will announce the Gap to the time master as well as to the time slaves. The current basic cycle will continue until its last time window. The time after the last time window is the Gap time.

For the actual time master and the potential time masters, FDCAN_TTOST.GSI will be set when the last basic cycle has finished and the Gap time starts. In nodes that are time slaves, bit FDCAN_TTOST.GSI will remain at 0.

When a potential time master is in synchronization state In_Gap (FDCAN_TTOST.SYS = 10), it has four options to intentionally finish a Gap:

1. Under software control by writing FDCAN_TTOCN.FGP = 1.

2. Under hardware control (FDCAN_TTOCN.GCS = 1) an edge from HIGH to LOW at the event-trigger input pin fdcan_evt sets FDCAN_TTOCN.FGP and restarts the schedule.

3. The third option is a time-triggered restart. When FDCAN_TTOCN.TMG = 1, the next register time mark interrupt (FDCAN_TTIR.RTMI = 1) will set FDCAN_TTOCN.FGP and start the reference message.

4. Finally any potential time master will finish a Gap when it reaches its Tx_Ref_Trigger_Gap, assuming that the event to synchronize on did not occur in time.

None of these options can cause a basic cycle to be interrupted with a reference message.

Setting of FDCAN_TTOCN.FGP after the Gap time has started will start the transmission of a reference message immediately and will thereby synchronize the message schedule. When FDCAN_TTOCN.FGP is set before the Gap time has started (while the basic cycle is still in progress), the next reference message is started at the end of the basic cycle, at the Tx_Ref_Trigger – there will be no Gap time in the message schedule.

In strictly time-triggered operation, bit Next_is_Gap = 1 in the reference message will be ignored, as well as the event-trigger input pin fdcan_evt and the bits FDCAN_TTOCN.NIG, FDCAN_TTOCN.FGP, and FDCAN_TTOCN.TMG.

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

41.5.4 Stop watch

The stop watch function enables capturing of FDCAN internal time values (local time, cycle time, or global time) triggered by an external event.

To enable the stop watch function, the application program first has to define local time, cycle time, or global time as stop watch source via FDCAN_TTOCN.SWS. When FDCAN_TTOCN.SWS is different from 00 and TT interrupt register flag FDCAN_TTIR.SWE is 0, the actual value of the time selected by FDCAN_TTTOCN.SWS will be copied into FDCAN_TTCPT.SWV on the next rising / falling edge (as configured via FDCAN_TTOCN.SWP) on stop watch trigger pin fdcan_swt. This will set interrupt flag FDCAN_TTIR.SWE. After the application program has read FDCAN_TTCPT.SWV, it may enable the next stop watch event by resetting FDCAN_TTIR.SWE to 0.

41.5.5 Local time, cycle time, global time, and external clock synchronization

There are two possible levels in time-triggered CAN:

1. Level 1 only provides time-triggered operation using cycle time.

2. Level 2 additionally provides increased synchronization quality, global time and external clock synchronization. In both levels, all timing features are based on a local time base - the local time.

The local time is a 16-bit cyclic counter, it is incremented once each NTU. Internally the NTU is represented by a 3-bit counter which can be regarded as a fractional part (three binary digits) of the local time. Generally, the 3-bit NTU counter is incremented eight times each NTU. If the length of the NTU is shorter than eight CAN clock periods (as may be configured in level 1, or as a result of clock calibration in level 2), the length of the NTU fraction is adapted, and the NTU counter is incremented only four times each NTU.

Figure 41-15 describes the synchronization of the cycle time and global time, performed in the same manner by all FDCAN nodes, including the time master. Any message received or transmitted invokes a capture of the local time taken at the message is frame synchronization event. This frame synchronization event occurs at the sample point of each start of frame (SoF) bit and causes the local time to be stored as Sync_Mark. Sync_Marks and Ref_Marks are captured including the 3-bit fractional part.

Whenever a valid reference message is transmitted or received, the internal Ref_Mark is updated from the Sync_Mark. The difference between Ref_Mark and Sync_Mark is the cycle sync mark (cycle sync mark = Sync_Mark - Ref_Mark) stored in register FDCAN_TTCSM. The most significant 16 bits of the difference between Ref_Mark and the actual value of the local time is the cycle time (cycle time = local time - Ref_Mark).

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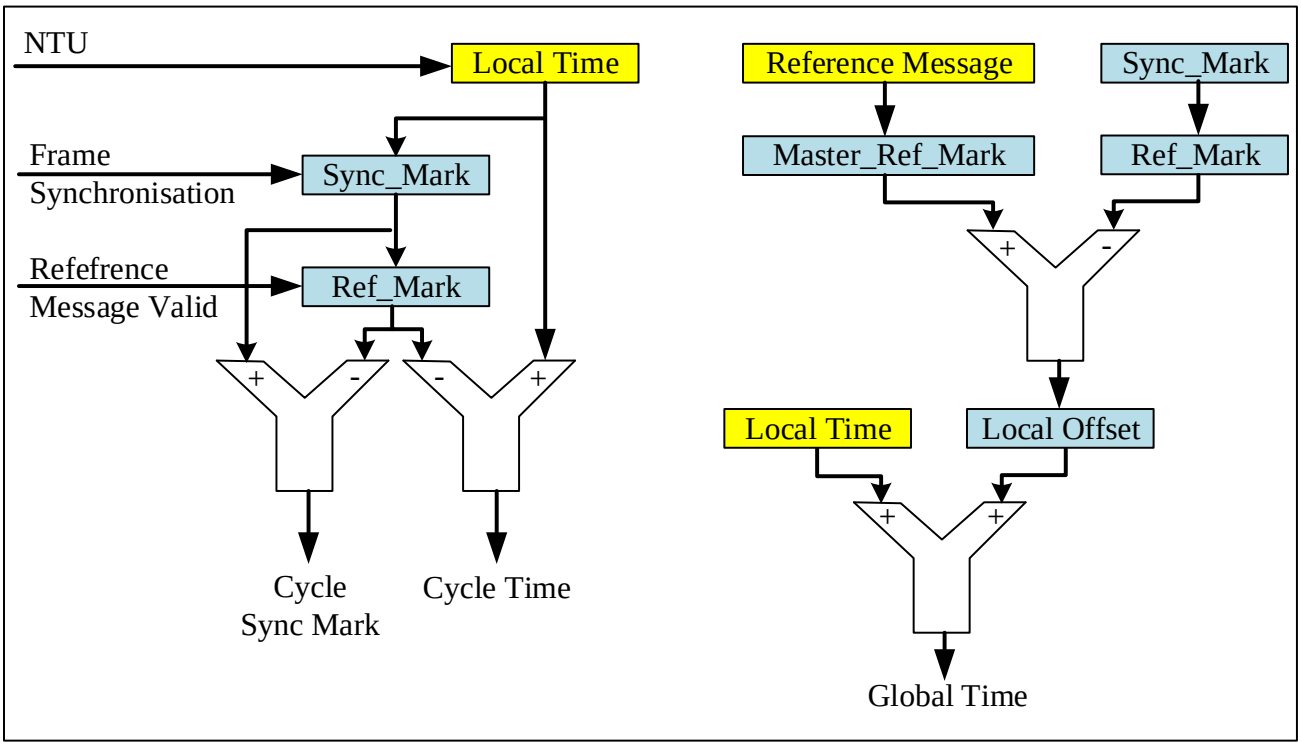
Figure 41-15 Cycle time and global time synchronization



The cycle time that can be read from FDCAN_TTCTC.CT is the difference of the node local time and Ref_Mark, both synchronized into the APB clock domain and truncated to 16 bit.

The global time exists for TTCAN level 0 and level 2 only, in level 1 it is invalid. The node view of the global time is the local image of the global time in (local) NTUs. After configuration, a potential time master will use its own local time as global time. The time master establishes its own local time as global time by transmitting its own Ref_Marks as Master_Ref_Marks in the reference message (bytes 3 and 4). The global time that can be read from FDCAN_TTLGT.GT is the sum of the node local time and its local offset, both synchronized into the APB clock domain and truncated to 16 bit. The fractional part is used for clock synchronization only.

A node that receives a reference message calculates its local offset to the global time by comparing its local Ref_Mark with the received Master_Ref_Mark (see Figure 41-16). The node view of the global time is local time plus local offset. In a potential time master that has never received another time master reference message, Local_Offset will be 0. When a node becomes the current time master after first having received other reference messages, Local_Offset will be frozen at its last value. In the time receiving nodes, Local_Offset may be subject to small adjustments, due to clock drift, when another node becomes time master, or when there is a global time discontinuity, signaled by Disc_Bit in the reference message. With the exception of global time discontinuity, the global time provided to the application program by register FDCAN_TTLGT is smoothed by a low-pass filtering to have a continuous monotonic value.

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Email: sales@nsing.com.sg

Figure 41-16 TTCAN level 0 and level 2 drift compensation

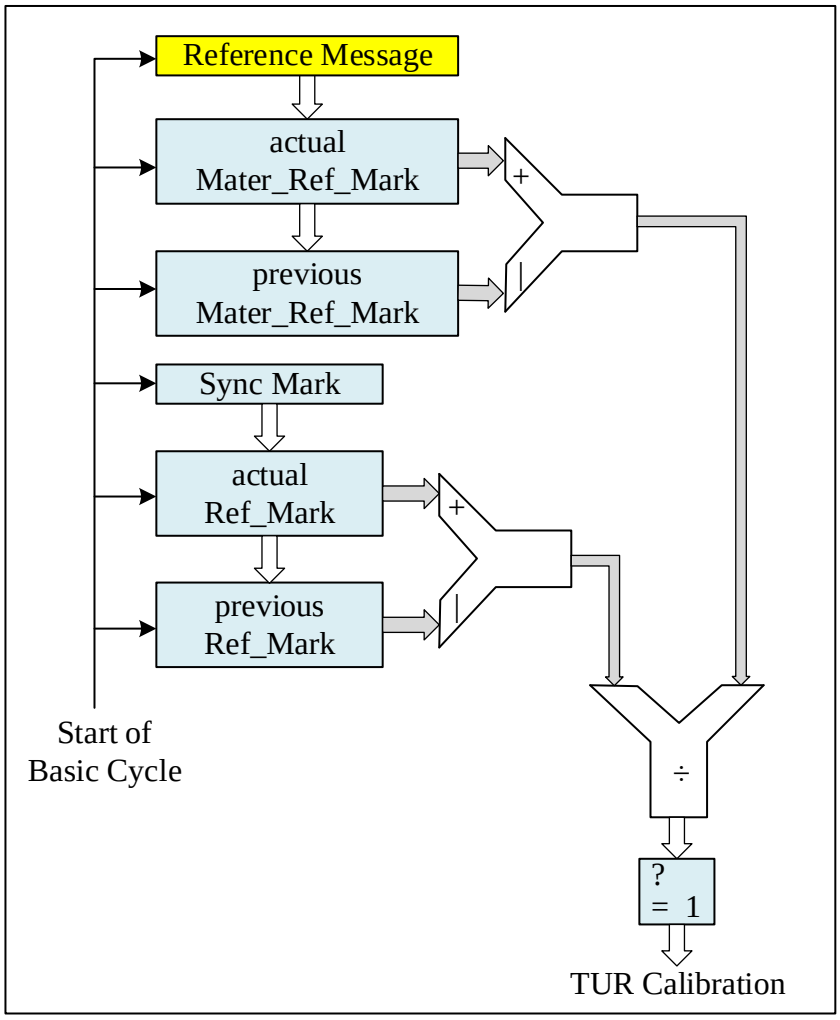

Figure 41-16 describes how in TTCAN levels 0 and 2 each time receiving node compensates the drift between its own local clock and the time master clock by comparing the length of a basic cycle in local time and in global time. If there is a difference between the two values and the Disc_Bit in the reference message is not set, a new value for FDCAN_TURNA.NAV is calculated. If the synchronization deviation SD = | NC - FDCAN_TURNA.NAV | ≤ SDL(synchronization deviation limit), the new value for FDCAN_TURNA.NAV takes effect. Else the automatic drift compensation is suspended.

In TTCAN level 0 and level 2, FDCAN_TTOST.QCS indicates whether the automatic drift compensation is active or suspended. In TTCAN level 1, FDCAN_TOST.QCS is always 1.

The current time master may synchronize its local clock speed and the global time phase to an external clock source. This is enabled by bit FDCAN_TTOCF.EECS.

The stop watch function (see Section 41.5.4: Stop watch) may be used to measure the difference in clock speed between the local clock and the external clock. The local clock speed is adjusted by first writing the newly calculated numerator configuration low to FDCAN_TURCF.NCL (FDCAN_TURCF.DC cannot be updated during operation). The new value takes effect by writing FDCAN_TTOCN.ECS to 1.

The global time phase is adjusted by first writing the phase offset into the TT global time Preset register

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Email: sales@nsing.com.sg

FDCAN_TTGTP. The new value takes effect by writing FDCAN_TTOCN.SGT to 1. The first reference message transmitted after the global time phase adjustment will have the Disc_Bit set to 1.

FDCAN_TTOST.QGTP shows whether the node global time is in phase with the time master global time. FDCAN_TTOST.QGTP is permanently 0 in TTCAN level 1 and when the synchronization deviation limit is exceeded in TTCAN level 0, 2 (FDCAN_TTOST.QCS = 0). It is temporarily 0 while the global time is low-pass filtered to supply the application with a continuous monotonic value. There is no low-pass filtering when the last reference message contained a Disc_Bit = 1 or when FDCAN_TTOST.QCS = 0.

41.5.6 TTCAN error level

The ISO 11898-4 specifies four levels of error severity:

1. S0 - No error

2. S1 - Warning - Only notification of application, reaction application-specific.

3. S2 error - Notification of application. All transmissions in exclusive or arbitrating time windows are disabled (i.e. no data or remote frames may be started). Potential time masters still transmit reference messages with the reference trigger offset FDCAN_TTOST.RTO set to the maximum value of 127.

4. S3 - Severe error - Notification of application. All CAN bus operations are stopped, i.e. transmission of dominant bits is not allowed, and FDCAN_CCCR.MON is set. The S3 error condition remains active until the application updates the configuration (set FDCAN_CCCR.CCE).

If several errors are detected at the same time, the highest severity prevails. When an error is detected, the application is notified by FDCAN_TTIR.ELC. The error level is monitored by FDCAN_TTOST.EL.

The TTCAN signals the following error conditions as required by ISO 11898-4:

- Config_error (S3)

  – Sets error level FDCAN_TTOST.EL to 11 when a merged arbitrating time window is not properly closed or when there is a Tx_Trigger with a time mark beyond the Tx_Ref_Trigger.

- Watch_Trigger_Reached (S3)

  – Sets error level FDCAN_TTOST.EL to 11 when a watch trigger was reached because the reference message is missing.

- Application_Watchdog (S3)

  – Sets error level FDCAN_TTOST.EL to 11 when the application failed to serve the application watchdog.The application watchdog is configured via FDCAN_TTOCF.AWL. It is served by reading register FDCAN_TTOST. When the watchdog is not served in time, bit FDCAN_TTOST.AWE and interrupt flag FDCAN_TTIR.AW are set, all FDCAN communication is stopped, and the FDCAN is set into bus monitoring mode (FDCAN_CCCR.MON set to 1).

- CAN_Bus_Off (S3)

  – Entering CAN_Bus_Off state sets error level FDCAN_TTOST.EL to 11. CAN_Bus_Off state is signaled by FDCAN_PSR.BO = 1 and FDCAN_CCCR.INIT = 1.

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- Scheduling_Error_2 (S2)

– Sets error level FDCAN_TTOST.EL to 10 if the MSC of one Tx_Trigger has reached 7. In addition interrupt flag FDCAN_TTIR.SE2 is set. The error level FDCAN_TTOST.EL is reset to 00 at the beginning of a matrix cycle when no Tx_Trigger has an MSC of 7 in the preceding matrix cycle.

- Tx_Overflow (S2)

– Sets error level FDCAN_TTOST.EL to 10 when the Tx count is equal or higher than the expected number of Tx_T riggers FDCAN_TTMLM.ENTT and a Tx_Trigger event occurs. In addition interrupt flag FDCAN_TTIR.TXO is set. The error level FDCAN_TTOST.EL is reset to 00 when the Tx count is no more than FDCAN_TTMLM.ENTT at the start of a new matrix cycle.

- Scheduling_Error_1 (S1)

– Sets error level FDCAN_TTOST.EL to 01 if within one matrix cycle the difference between the maximum MSC and the minimum MSC for all trigger memory elements (of exclusive time windows) is larger than two, or if one of the MSCs of an exclusive Rx_Trigger has reached seven. In addition interrupt flag FDCAN_TTIR.SE1 is set. If within one matrix cycle none of these conditions is valid, the error level FDCAN_TTOST.EL is reset to 00.

- Tx_Underflow (S1)

– Sets error level FDCAN_TTOST.EL to 01 when the Tx count is less than the expected number of Tx_Triggers FDCAN_TTMLM.ENTT at the start of a new matrix cycle. In addition interrupt flag FDCAN_TTIR.TXU is set. The error level FDCAN_TTOST.EL is reset to 00 when the Tx count is at least FDCAN_TTMLM.ENTT at the start of a new matrix cycle.

41.5.7 TTCAN message handling

41.5.7.1 Reference message

For potential time masters the identifier of the reference message is configured via FDCAN_TTRMC.RID. No dedicated Tx buffer is required for transmission of the reference message. When a reference message is transmitted, the first data byte for TTCAN level 1 (that is, the first four data bytes for TTCAN level 0 and the first four data bytes for TTCAN level 2) will be provided by the FSE.

In case the reference message Payload select FDCAN_TTRMC.RMPS is set, the rest of the reference message payload (level 1: bytes 2-8, level 0, 2: bytes 5-6) is taken from Tx buffer 0. In this case the data length DLC code from message buffer 0 is used.

Table 41-19 Number of data bytes transmitted with a reference message

FDCAN_TTRMC.RMPS	FDCAN_TXBRP.TRP0	Level 0	Level 1	Level 2
0	0	4	1	4
0	1	4	1	4
1	0	4	1	4
1	1	4+MBO	1+MBO	4+MBO

To send additional payload with the reference message in level 1 a DLC > 1 has to be configured, for level 0 and

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Email: sales@nsing.com.sg

level 2 a DLC > 4 is required. In addition the transmission request pending bit FDCAN_TXBRP.TRP0 of message buffer 0 must be set (see Table 41-19). In case bit FDCAN_TXBRP.TRP0 is not set when a reference message is started, the reference message is transmitted with the data bytes supplied by the FSE only.

For acceptance filtering of reference messages the reference identifier FDCAN_TTRMC.RID is used.

41.5.7.2 Message reception

Message reception is done via the two Rx FIFOs in the same way as for event-driven CAN communication (see Section 41.4.2).

The message status count MSC is part of the corresponding trigger memory element and has to be initialized to 0 during configuration. It is updated while the TTCAN is in synchronization states In_Gap or In_Schedule. The update happens at the message Rx_Trigger. At this point in time it is checked at which acceptance filter element the latest message received in this basic cycle had matched. The matching filter number is stored as the acceptance filter result. If this is the same the filter number as defined in this trigger memory element, the MSC is decremented by one. If the acceptance filter result is not the same filter number as defined for this filter element, or if the acceptance filter result is cleared, the MSC is incremented by one. At each Rx_Trigger and at each start of cycle, the last acceptance filter result is cleared.

The time mark of an Rx_Trigger should be set to a value where it is ensured that reception and acceptance filtering for the targeted message has completed. This has to take into consideration the RAM access time and the order of the filter list. It is recommended, that filters which are used for Rx_Triggers are placed at the beginning of the filter list. It is not recommended to use an Rx_Trigger for the reference message.

41.5.7.3 Message transmission

For time-triggered message transmission the TTCAN supplies 32 dedicated Tx buffers (see 41.4.3). A Tx FIFO or Tx queue is not available when the FDCAN is configured for time-triggered operation (FDCAN_TTOCF.OM = 01 or 10).

Each Tx_Trigger in the trigger memory points to a particular Tx buffer containing a specific message. There may be more than one Tx_Trigger for a given Tx buffer if that Tx buffer contains a message that is to be transmitted more than once in a basic cycle or matrix cycle.

The application program has to update the data regularly and on time, synchronized to the cycle time. The Host CPU is responsible that no partially updated messages are transmitted. To assure this the Host has to proceed in the following way:

Tx_Trigger_Single / Tx_Trigger_Merged / Tx_Trigger_Arbitration

- Check whether the previous transmission has completed by reading FDCAN_TXBTO
- Update the Tx buffer configuration and/or payload
- Issue an add request to set the Tx buffer request pending bit

Tx_Trigger_Continous

- Issue a cancellation request to reset the Tx buffer request pending bit
- Check whether the cancellation has finished by reading FDCAN_TXBCF
- Update Tx buffer configuration and/or payload

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Email: sales@nsing.com.sg

- Issue an add request to set the Tx buffer request pending bit

The message MSC stored with the corresponding Tx_Trigger provides information on the success of the transmission.

The MSC is incremented by one when the transmission could not be started because the CAN bus was not idle within the corresponding transmit enable window or when the message was started and could not be completed successfully. The MSC is decremented by one when the message was transmitted successfully or when the message could have been started within its transmit enable window but was not started because transmission was disabled (TTCAN in error level S2 or Host has disabled this particular message).

The Tx buffers may be managed dynamically, i.e. several messages with different identifiers may share the same Tx buffer element. In this case the Host has to assure that no transmission request is pending for the Tx buffer element to be reconfigured by checking FDCAN_TXBRP.

If a Tx buffer with pending transmission request should be updated, the Host first has to issue a cancellation request and check whether the cancellation has completed by reading FDCAN_TXBCF before it starts updating.

The Tx handler will transfer a message from the message RAM to its intermediate output buffer at the trigger element which becomes active immediately before the Tx_Trigger element which defines the beginning of the transmit window. During and after the transfer time the transmit message may not be updated and its FDCAN_TXBRP bit may not be changed. To control this transfer time, an additional trigger element may be placed before the Tx_Trigger. This may be example of a Time_Base_Trigger which need not cause any other action. The difference in time marks between the Tx_Trigger and the preceding trigger has to be large enough to guarantee that the Tx handler can read four words from the message RAM even at high RAM access load from other modules.

41.5.7.3.1 Transmission in exclusive time windows

A transmission is started time-triggered when the cycle time reaches the time mark of a Tx_Trigger_Single or Tx_Trigger_Continuous. There is no arbitration on the bus with messages from other nodes. The MSC is updated according the result of the transmission attempt. After successful transmission started by a Tx_Trigger_Single the respective Tx buffer request pending bit is reset. After successful transmission started by a Tx_Trigger_Continuous the respective Tx buffer request pending remains set. When the transmission was not successful due to disturbances, it will be repeated next time (one of) its Tx_Trigger(s) become(s) active.

41.5.7.3.2 Transmission in arbitrating time windows

A transmission is started time-triggered when the cycle time reaches the time mark of a Tx_Trigger_Arbitration. Several nodes may start to transmit at the same time. In this case the message has to arbitrate with the messages from other nodes. The MSC is not updated. When the transmission was not successful (lost arbitration or disturbance), it will be repeated next time (one of) its Tx_Trigger(s) become(s) active.

41.5.7.3.3 Transmission in merged arbitrating time windows

The purpose of a merged arbitrating time window is, to enable multiple nodes to send a limited number of frames which are transmitted in immediate sequence, the order given by CAN arbitration. It is not intended for burst transmission by a node. Since the node does not have exclusive access within this time window, it may happen that not all requested transmissions are successful.

Messages which have lost arbitration or were disturbed by an error, may be re-transmitted inside the same merged arbitrating time window. The re-transmission will not be started if the corresponding transmission request pending

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flag was reset by a successful Tx cancellation.

In single transmit windows, the Tx handler transmits the message indicated by the message number of the trigger element. In merged arbitrating time windows, it can handle up to three message numbers from the trigger list. Their transmissions will be attempted in the sequence defined by the trigger list. If the time mark of a fourth message is reached before the first is transmitted (or canceled by the Host), the four the request will be ignored.

The transmission inside a merged arbitrating time window is not time-triggered. The transmission of a message may start before its time mark, or after the time mark if the bus was not idle.

The messages transmitted by a specific node inside a merged arbitrating time window will be started in the order of their Tx_Triggers, so a message with low CAN priority may prevent the successful transmission of a following message with higher priority, if their is compelling bus traffic. This has to be considered for the configuration of the trigger list. Time_Base_Triggers may be placed between consecutive Tx_Triggers to define the time until the data of the corresponding Tx buffer needs to be updated.

41.5.8 TTCAN interrupt and error handling

The TT interrupt register FDCAN_TTIR consists off our segments. Each interrupt can be enabled separately by the corresponding bit in the TT interrupt enable register FDCAN_TTIE. The flags remain set until the Host clears them. A flag is cleared by writing a 1 to the corresponding bit position.

The first segment consists of flags CER, AW, WT, and IWT. Each flag indicates a fatal error condition where the CAN communication is stopped. With the exception of IWT, these error conditions require a re-configuration of the FDCAN module before the communication can be restarted.

The second segment consists of flags ELC, SE1, SE2, TXO, TXU, and GTE. Each flag indicates an error condition where the CAN communication is disturbed. If they are caused by a transient failure, e.g. by disturbances on the CAN bus, they will be handled by the FDCAN protocol failure handling and do not require intervention by the application program.

The third segment consists of flags GTD, GTW, SWE, TTMI, and RTMI. The first two flags are controlled by global time events (level 0, 2 only) that require a reaction by the application program. With a stop watch event triggered by a rising edge on pin fdcan_swt internal time values are captured. The trigger time mark interrupt notifies the application that a specific Time_Base_Trigger is reached. The register time mark interrupt signals that the time referenced by FDCAN_TTOCN.TMC (cycle, local, or global) equals time mark FDCAN_TTTMK.TM. It can also be used to finish a Gap.

The fourth segment consists of flags SOG, CSM, SMC, and SBC. These flags provide a means to synchronize the application program to the communication schedule.

41.5.9 Level 0

TTCAN level 0 is not part of ISO11898-4. This operation mode makes the hardware, that in TTCAN level 2 maintains the calibrated global time base, also available for event-driven CAN according to ISO11898-1.

Level 0 operation is configured via FDCAN_TTOCF.OM = 11. In this mode the FDCAN operates in event driven CAN communication, there is no fixed schedule, the configuration of FDCAN_TTOCF.GEN is ignored. External

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event-synchronized operation is not available in level 0. A synchronized time base is maintained by transmission of reference messages.

In level 0 the trigger memory is not active and therefore needs not to be configured. The time mark interrupt flag (FDCAN_TTIR.TTMI) is set when the cycle time has reached FDCAN_TTOCF.IRTO*0x200, it reminds the Host to set a transmission request for message buffer 0. The Watch_Trigger interrupt flag (FDCAN_TTIR.WT) is set when the cycle time has reached 0xFF00. These values were chosen to have enough margin for a stable clock calibration. There are no further TT-error-checks.

Register time mark interrupts (FDCAN_TTIR.RTMI) are also possible.

The reference message is configured as for level 2 operation. Received reference messages are recognized by the identifier configured in register FDCAN_TTRMC. For the transmission of reference messages only message buffer 0 may be used. The node transmits reference messages any time the Host sets a transmission request for message buffer 0, there is no reference trigger offset.

Level 0 operation is configured via:

- FDCAN_TTRMC
- FDCAN_TTOCF except EVTP, AWL, GEN
- FDCAN_TTMLM except ENTT, TXEW
- FDCAN_TURCF

Level 0 operation is controlled via:

- FDCAN_TTOCN except NIG, TMG, FGP, GCS, TTMIE
- FDCAN_TTGTP
- FDCAN_TTTMK
- FDCAN_TTIR excluding bits CER, AW, IWT SE2, SE1, TXO, TXU, SOG (no function)
- FDCAN_TTIR the following bits have changed function
  - TTMI not defined by trigger memory - activated at cycle time FDCAN_TTOCF.IRTO 0x200
  - WT not defined by trigger memory - activated at cycle time 0xFF00

Level 0 operation is signaled via:

- TTOST excluding bits AWE, WFE, GSI, GFI, RTO (no function)

41.5.9.1 Synchronizing

Figure 41-17 describes the states and the state transitions in TTCAN level 0 operation. Level 0 has no In_Gap state.

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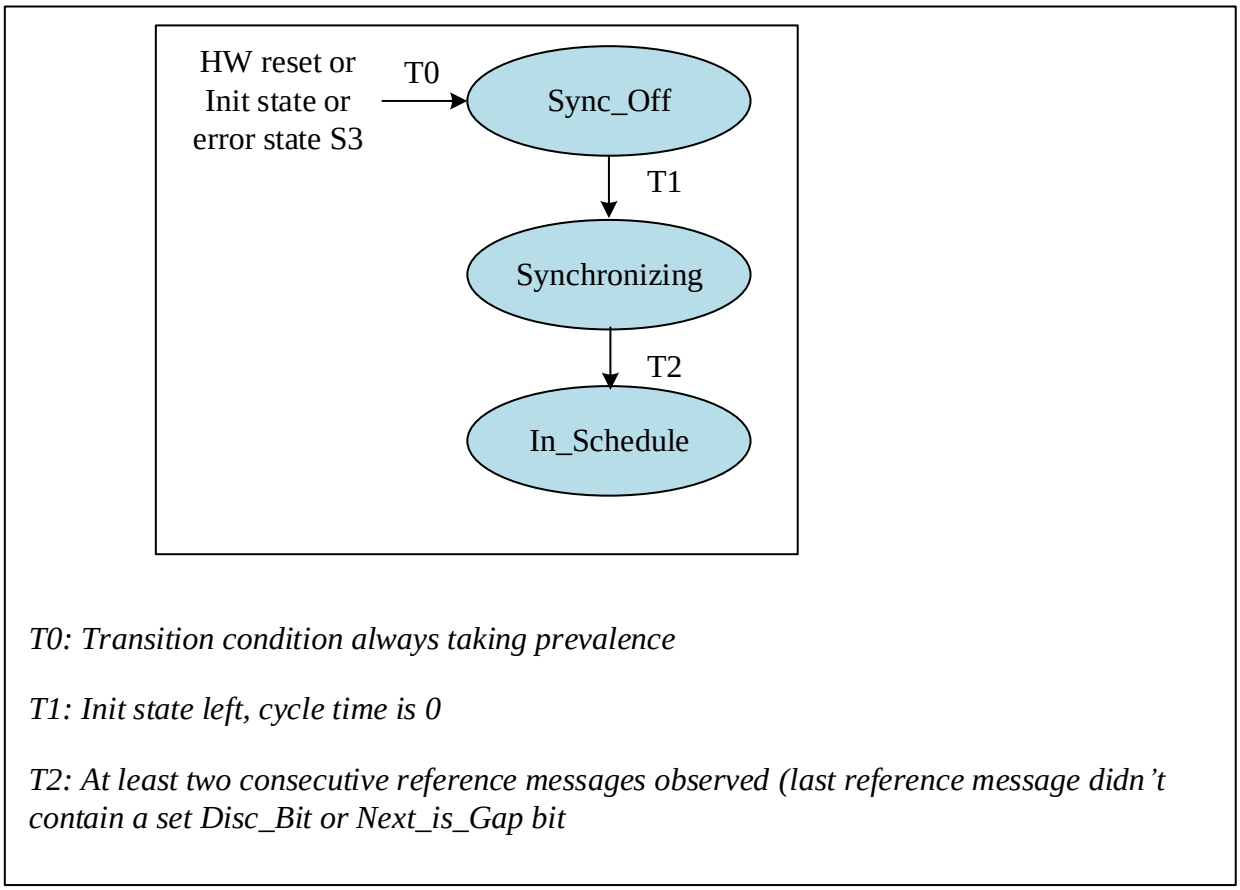
Figure 41-17 Level 0 schedule synchronization state machine



41.5.9.2 Handling of error levels

During level 0 operation only the following error conditions may occur:

- Watch_Trigger_Reached (S3), reached cycle time 0xFF00
- CAN_Bus_Off (S3)

Since no S1 and S2 errors are possible, the error level can only switch between S0 (No error) and S3 (Severe error). In TTCAN level 0 an S3 error is handled differently. When error level S3 is reached, both FDCAN_TTOST.SYS and FDCAN_TTOST.MS are reset, and interrupt flags FDCAN_TTIR.GTE and FDCAN_TTIR.GTD are set.

When error level S3 (FDCAN_TTOST.EL = 11) is entered, bus monitoring mode is (contrary to TTCAN level 1 and level 2) not entered. S3 error level is left automatically after transmission (time master) or reception (time slave) of the next reference message.

41.5.9.3 Master slave relation

Figure 41-18 describes the master slave relation in TTCAN level 0. In case of an S3 error the FDCAN returns to state Master_Off.

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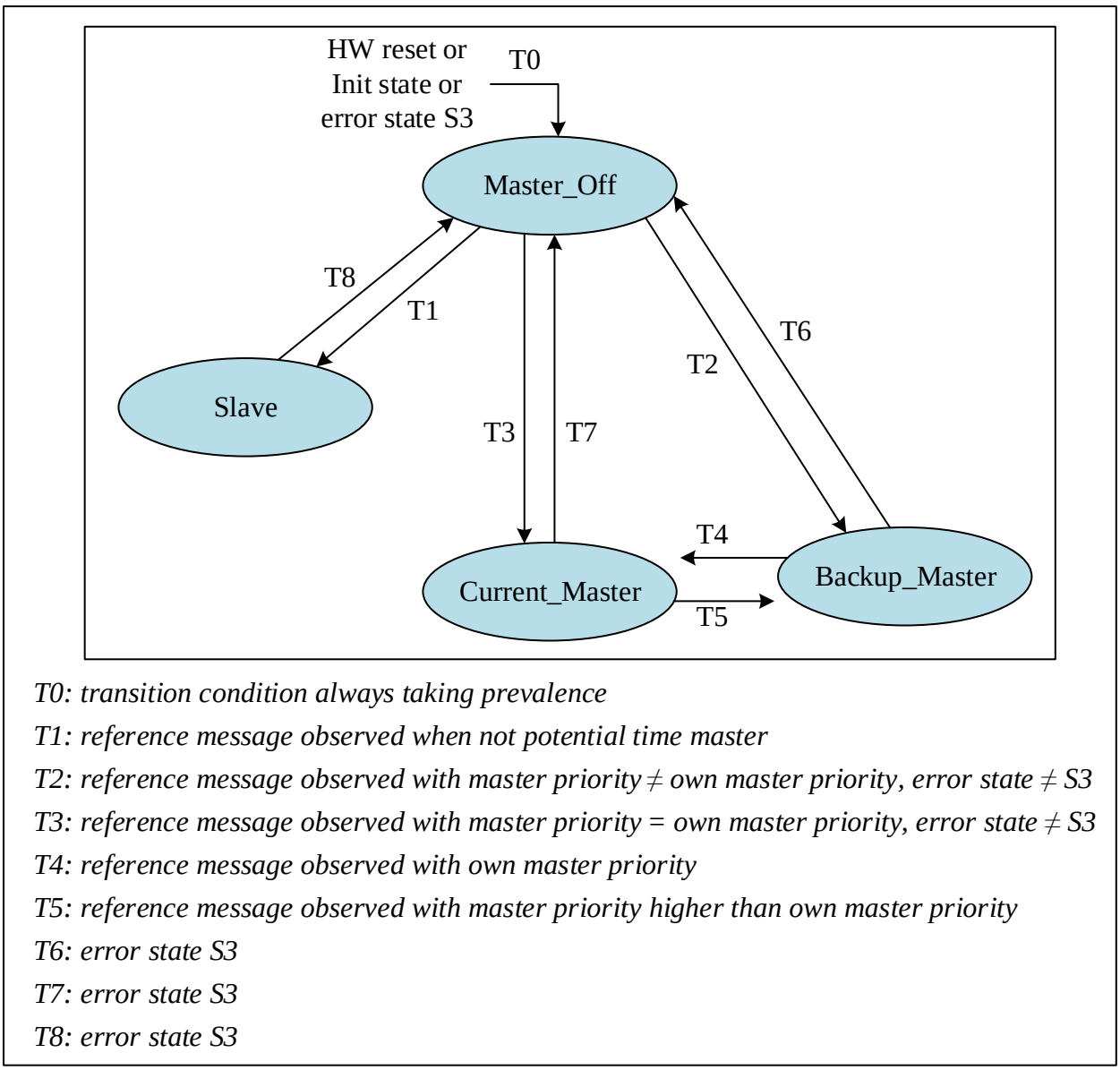
Figure 41-18 Level 0 master to slave relation



T0: transition condition always taking prevalence

T1: reference message observed when not potential time master

T2: reference message observed with master priority ≠ own master priority, error state ≠ S3

T3: reference message observed with master priority = own master priority, error state ≠ S3

T4: reference message observed with own master priority

T5: reference message observed with master priority higher than own master priority

T6: error state S3

T7: error state S3

T8: error state S3

41.5.10 Synchronization to external time schedule

This feature can be used to synchronize the phase of the FDCAN schedule to an external schedule (e.g. that of a second TTCAN network or FlexRay network). It is applicable only when the FDCAN is current time master (FDCAN_TTOST.MS = 11).

External synchronization is controlled by event trigger input pin fdcan_evt. If bit FDCAN_TTOCN.ESCN is set, a rising edge at event trigger pin fdcan_evt the FDCAN compares its actual cycle time with the target phase value configured by FDCAN_TTGTP.CTP.

Before setting FDCAN_TTOCN.ESCN the Host has to adapt the phases of the two time schedules e.g. by using the FDCAN gap control (see Section 41.5.3: TTCAN gap control). When the Host sets FDCAN_TTOCN.ESCN, FDCAN_TTOSTSPL is set.

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If the difference between the cycle time and the target phase value FDCAN_TTGTP.CTP at the rising edge at event trigger pin fdcan_evt is greater than 9 NTU, the phase lock bit FDCAN_TTOST.SPL is reset, and interrupt flag FDCAN_TTIR.CSM is set. FDCAN_TTOST.SPL is also reset (and FDCAN_TTIR.CSM is set), when another node becomes time master.

If both FDCAN_TTOST.SPL and FDCAN_TTOCN.ESCN are set, and if the difference between the cycle time and the target phase value FDCAN_TTGTP.CTP at the rising edge at event trigger pin fdcan_evt is lower or equal to nine NTU, the phase lock bit

FDCAN_TTOST.SPL remains set, and the measured difference is used as reference trigger offset value to adjust the phase at the next transmitted reference message.

Note: The rising edge detection at event trigger pin fdcan_evt is enabled with the start of each basic cycle. The first rising edge triggers the compare of the actual cycle time with FDCAN_TTGTP.CTP. All further edges until the beginning of the next basic cycle are ignored.

41.6 FDCAN Registers

FDCAN1 基地址：0x40000000

FDCAN2 基地址：0x40000400

FDCAN5 基地址：0x40000800

FDCAN6 基地址：0x40000C00

FDCAN3 基地址：0x400D0000

FDCAN4 基地址：0x400D0400

FDCAN7 基地址：0x400D0800

FDCAN8 基地址：0x400D0C00

41.6.1 FDCAN Core Release Register (FDCAN_CREL)

Address offset: 0x00

Reset value: 0x3313 0328

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL[3:0]				STEP[3:0]				SUBSTEP[3:0]				YEAR[3:0]			
r				r				r				r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON[7:0]								DAY[7:0]							
r								r							

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Bit Field	Name	Description
31:28	REL[3:0]	Core release, 1 bit BCD code.
27:24	STEP[3:0]	Step of Core release, 1 bit BCD code.
23:20	SUBSTEP[3:0]	Sub-step of Core release, 1 bit BCD code.
19:16	YEAR[3:0]	Timestamp Year, 1 bit BCD code.
15:8	MON[7:0]	Timestamp Month, 2 bit BCD code.
7:0	DAY[7:0]	Timestamp Day, 2 bit BCD code.

41.6.2 FDCAN Endianness Register (FDCAN_ENDN)

Address offset: 0x04

Reset value: 0x8765 4321

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV[15:0]															
r															

Bit Field	Name	Description
31:0	ETV[31:0]	Endianness Test Value Fixed is 0x8765 4321.

41.6.3 FDCAN Data Bit Timing and Prescaler Register (FDCAN_DBTP)

Address offset: 0x0C

Reset value: 0x0000 0A33

Data can only be written to this register when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT bits are set to 1. The CAN data time quantum tq is programmable, where tq = (DBRP+1) * fdcan_tq_ck clock cycles, ranging from 1 to 32 fdcan_tq_ck clock cycles.

DTSEG1 is the sum of Prop_Seg and Phase_Seg1. DTSEG2 is Phase_Seg2. Therefore, the length of the data bit time is (programmed value) (DTSEG1 + DTSEG2 + 3) * tq, ranging from 3 to 49 tq.

The information processing time (IPT) is zero, meaning that the data for the next bit is available at the first clock edge after the sampling point.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TDC	Reserved		DBRP[4:0]				
								rw			rw				

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			DTSEG1[4:0]					DTSEG2[3:0]				DSJW[3:0]			
			rw					rw				rw			

Bit Field	Name	Description
31:24	Reserved	Reserved, must be kept at reset value.
23	TDC	Transceiver Delay Compensation. 0: Disable Transceiver Delay Compensation 1: Enable Transceiver Delay Compensation
22:21	Reserved	Reserved, must be kept at reset value.
20:16	DBRP[4:0]	Data Bit Rate Prescaler. The value of the Data Bit Rate Prescaler, used to divide the fdcan_tq_ck clock to generate the bit time quantum (tq). The bit time is a multiple of this bit time quantum (tq). The valid range for the Data Bit Rate Prescaler is 0 to 31. When TDC = '1', the range is restricted to 0 and 1. The hardware interprets this value as the programmed value plus 1.
15:13	Reserved	Reserved, must be kept at reset value.
12:8	DTSEG1[4:0]	Data time segment before sample point. The valid values range from 0 to 31. The hardware interprets this value as the programmed value plus 1.
7::4	DTSEG2[3:0]	Data time segment after sample point. The valid values range from 0 to 31. The hardware interprets this value as the programmed value plus 1.
3:0	DSJW[3:0]	Synchronization Jump Width. The valid values range from 0 to 31. The hardware interprets this value as the programmed value plus 1.

Note:

1. *When using an 8MHz CAN clock (fdcan_tq_ck), the reset value 0x00000A33 configures the bit rate to 500 kBit/s.*
2. *The bit rate of the CAN FD data phase configured through DBTP must be higher than or equal to the bit rate of the arbitration phase configured through NBTP.*

41.6.4 FDCAN Test Register (FDCAN_TEST)

To enable write access to the test registers, the FDCAN_CCCR.TEST bit must be set to "1". When the FDCAN_CCCR.TEST bit is reset, all test register functions are set to their reset values.

The loopback mode and software control of the receive pin FDCANx_TX belong to the hardware test mode. Programming TX to a value other than "00" may interfere with message transmission on the CAN bus.

Address offset: 0x10

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RX	TX[1:0]		LBCK	Reserved			
								r	rw		rw				

Bit Field	Name	Description
31:8	Reserved	Reserved, must be kept at reset value.
7	RX	Receive Pin Monitoring the actual value of the receive pin FDCAN_RX 0: CAN bus is dominant (FDCAN_RX = '0') 1: CAN bus is recessive (FDCAN_RX = '1')
6:5	TX[1:0]	Control of Transmit Pin 00: Reset value, FDCAN_TX controlled by the CAN core, updated at the end of the CAN bit time 01: Monitoring the sampling point on the transmit pin FDCAN_TX 10: Dominant ('0') level on pin FDCAN_TX 11: Recessive ('1') level on pin FDCAN_TX
4	LBCK	Loop Back Mode 0: Reset value, disable loopback mode 1: Enable loopback mode
3:0	Reserved	Reserved, must be kept at reset value.

41.6.5 FDCAN RAM Watchdog Register (FDCAN_RWD)

The RAM watchdog monitors the READY signal output from the message RAM. Accessing the message RAM initiates the message RAM watchdog counter, with the initial value configured by FDCAN_RWD.WDC. When the access to the message RAM is successfully completed and the READY signal is issued, the counter is reset to the FDCAN_RWD.WDC value. If the counter decrements to 0 before the message RAM issues the READY signal, the counter stops counting, and the interrupt flag FDCAN_IR.WDI is set. The RAM watchdog counter is driven by the interface clock (fdcan_pclk).

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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WDV[7:0]	WDC[7:0]
r	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value.
15:8	WDV[7:0]	Watchdog value Value of the message RAM watchdog counter.)
7:0	WDC[7:0]	Watchdog configuration Starting value of the message RAM watchdog counter. If the reset value "00" is used, the counter is disabled. These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

41.6.6 FDCAN Control Register (FDCAN_CCCR)

Address offset: 0x18

Reset value: 0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NISO	TXP	EFBI	PXHD	Reserved		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
rw	rw	rw	rw			rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value.
15	NISO	Non ISO Operation If this bit is set to 1, FDCAN will use the CAN FD frame format specified in the Bosch CAN FD Specification V1.0. 0: Conforms to the CAN FD frame format specified in ISO 11898-1 1: Conforms to the CAN FD frame format specified in the Bosch CAN FD Specification V1.0
14	TXP	Transmit Pause If this bit is set to 1, after a successful frame transmission, FDCAN will pause for two CAN bit times before starting the next transmission. 0: Disable transmission pause 1: Enable transmission pause
13	EFBI	Edge Filtering during Bus Integration 0: Disable edge filtering

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Bit Field	Name	Description
		1: Require two consecutive dominant tq to detect a hard synchronization edge
12	PXHD	Protocol Exception Handling Disable 0: Enable protocol exception handling 1: Disable protocol exception handling *Note: When protocol exception handling is disabled, FDCAN will transmit error frames upon detecting protocol exception conditions.*
11:10	Reserved	Reserved, must be kept at reset value.
9	BRSE	Bit Rate Switch Enable 0: Disable bit rate switching during transmission 1: Enable bit rate switching during transmission *Note: BRSE is invalid when CAN FD operation is disabled (FDOE = '0').*
8	FDOE	FD Operation Enable 0: Disable FD operation 1: Enable FD operation
7	TEST	Test Mode Enable 0: Normal operation, register TEST retains reset value 1: Test mode, enables write access to register TEST
6	DAR	Disable Automatic Retransmission 0: Enable automatic retransmission of unsuccessfully transmitted messages 1: Disable automatic retransmission
5	MON	Bus Monitoring Mode The MON bit can only be set to 1 through software when both CCE and INIT are set to "1". This bit can be reset by the host at any time. 0: Disable bus monitoring mode 1: Enable bus monitoring mode
4	CSR	Clock Stop Request 0: Clock stop not requested 1: Clock stop requested. If clock stop is requested, INIT will be set to 1 first, followed by CSA after all pending transmission requests are completed and the CAN bus reaches the idle state.
3	CSA	Clock Stop Acknowledge 0: Clock stop not acknowledged 1: FDCAN can be powered down by stopping the fdcan_tq_ck clock and fdcan_pclk clock
2	ASM	Restricted Operation Mode ASM can only be set by the host when both CCE and INIT are set to '1'. This bit can be reset by the host at any time. 0: Normal CAN operation 1: Activate restricted operation mode
1	CCE	Configuration Change Enable 0: CPU does not have write access permission to protected configuration registers

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Bit Field	Name	Description
		1: CPU has write access permission to protected configuration registers (when CCCR.INIT = '1')
0	INIT	Initialization 0: Normal operation 1: Start initialization

Note: Due to the synchronization mechanism between the two clock domains, there is a delay after writing the INIT value before it can be read. Therefore, it is necessary to read INIT to ensure that the previously written INIT value has taken effect before setting it to a new value.

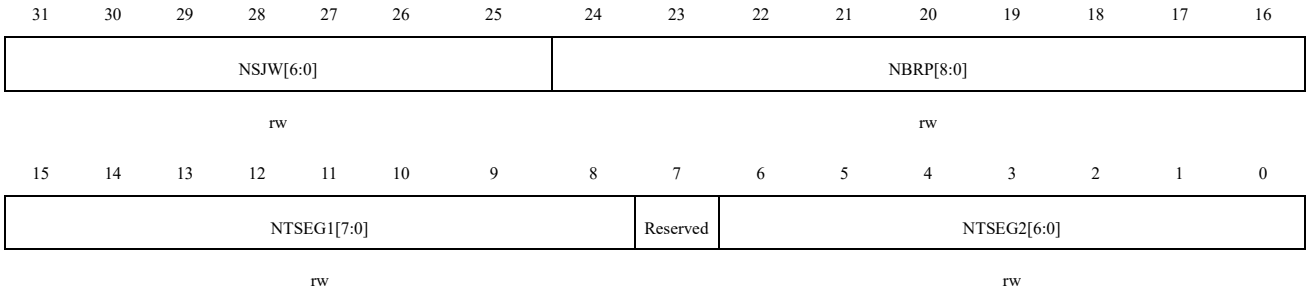
41.6.7 FDCAN Nominal Bit Timing and Prescaler Register (FDCAN_NBTP)

Data can only be written to this register when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT bits are set to 1. The CAN nominal time quantum tq is programmable, where tq = (NBRP+1) * fdcan_tq_ck clock cycles, ranging from 1 to 512 fdcan_tq_ck clock cycles.

NTSEG1 is the sum of Prop_Seg and Phase_Seg1. NTSEG2 is Phase_Seg2. Therefore, the length of the nominal bit time is (programmed value) (NTSEG1 + NDTSEG2 + 3) * tq, ranging from 4 to 385 tq.

Address offset: 0x1C

Reset value: 0x0600 0A03



Bit Field	Name	Description
31:25	NSJW[6:0]	Nominal (Re)Synchronization Jump Width The valid values range from 0 to 127. The hardware interprets this value as the programmed value plus 1. These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
24:16	NBRP[8:0]	Bit Rate Prescaler The bit time quantum tq is generated by dividing fdcan_tq_ck by this value, and the bit time is a multiple of this bit time quantum. The valid values for the bit rate prescaler range from 0 to 511. The hardware interprets this value as the programmed value plus 1. These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

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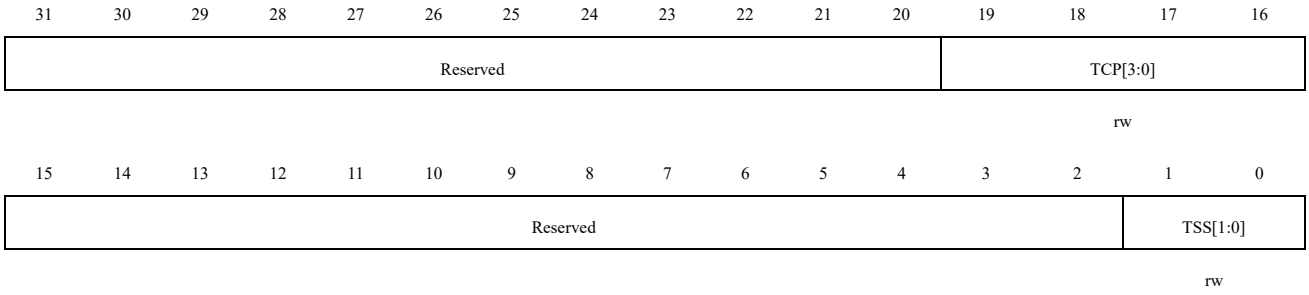
Bit Field	Name	Description
15:8	NTSEG1[7:0]	Nominal time segment before sample point The valid values range from 1 to 255. The hardware interprets this value as the programmed value plus 1. These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
7	Reserved	Reserved, must be kept at reset value.
6:0	NTSEG2[6:0]	Nominal time segment after sample point The valid values range from 1 to 127. The hardware interprets this value as the programmed value plus 1. These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

Note: If the CAN core clock is 8MHz, the reset value 0x00000A33 will configure the FDCAN bit rate to 500 kb/s.

41.6.8 FDCAN Timestamp Counter Configuration Register (FDCAN_TSCC)

Address offset: 0x20

Reset value: 0x0000 0000



Bit Field	Name	Description
31:20	Reserved	Reserved, must be kept at reset value.
19:16	TCP[3:0]	Timestamp Counter Prescaler Configures the timestamp and timeout counter time units as multiples of CAN bit time [1…16]. The hardware interprets this value as the programmed value plus 1. *Note: In CAN FD mode, an external counter is required for timestamp generation (TSS = "10"). These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.*
15:2	Reserved	Reserved, must be kept at reset value.
1:0	TSS[1:0]	Timestamp Select 00: Timestamp counter value always 0x0000 01: Timestamp counter value increments with TCP 10: Use external timestamp counter value 11: Same as "00"

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41.6.9 FDCAN Timestamp Counter Value Register (FDCAN_TSCV)

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value.
15:0	TSC[15:0]	Timestamp Counter The internal/external timestamp counter value is captured at the start of (receive and transmit) frames. When FDCAN_TSCC.TSS = "01", the timestamp counter increments by multiples of CAN bit time [1…16], depending on the configuration of FDCAN_TSCC.TCP. Counter wraparound sets the interrupt flag FDCAN_IR.TSW to 1. Write access resets the counter value to 0. When FDCAN_TSCC.TSS = "10", TSC reflects the external timestamp counter value, and write access has no effect.

Note:

1. "Wraparound" refers to the timestamp counter value changing from a non-zero value to 0, not due to write access to TSCV.

2. Byte access: Writing to register bytes 3/2/1/0 will reset the timestamp counter.

41.6.10 FDCAN Timeout Counter Configuration Register (FDCAN_TOCC)

Address offset: 0x28

Reset value: 0xFFFF 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													TOS[1:0]		ETOC
													rw		rw

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Bit Field	Name	Description
31:16	TOP[15:0]	Timeout Period Starting value of the timeout counter (decrementing counter).
15:3	Reserved	Reserved, must be kept at reset value.
2:1	TOS[1:0]	TOS: Timeout Select When operating in continuous mode, writing to FDCAN_TOCV will preset the counter to the value specified by FDCAN_TOCC.TOP and continue decrementing the count. When the timeout counter is controlled by one of the FIFOs and the FIFO is empty, the counter will be preset to the FDCAN_TOCC.TOP value. The countdown starts after writing the first FIFO element. 00: Continuous operation 01: Timeout controlled by Transmit Event FIFO 10: Timeout controlled by Receive FIFO 0 11: Timeout controlled by Receive FIFO 1 These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
0	ETOC	Enable Timeout Counter. 0: Disable timeout counter 1: Enable timeout counter These bits are write-protected and can only be accessed for writing when both FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

41.6.11 FDCAN Timeout Counter Value Register (FDCAN_TOCV)

Address offset: 0x2C

Reset value: 0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value.
15:0	TOC[15:0]	Timeout Counter The timeout counter decrements by multiples of CAN bit time [1…16], depending on the configuration of FDCAN_TSCC.TCP. When the counter decrements to 0, the interrupt flag FDCAN_IR.TOO is set to 1, and the timeout counter stops counting. The start and reset/restart conditions are configured through FDCAN_TOCC.TOS.

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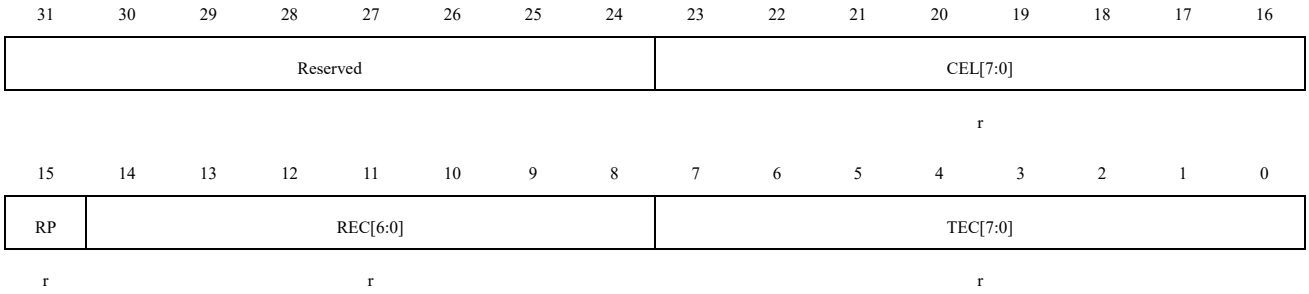
Bit Field	Name	Description
		Note: Byte Access: when TOCC.TOS = "00", write register byte 3/2/1/0 will preset the timeout counter.

41.6.12 FDCAN Error Counter Register (FDCAN_ECR)

Address offset: 0x40

Reset value: 0x0000 0000

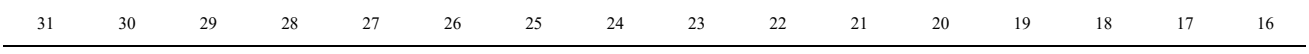


Bit Field	Name	Description
31:24	Reserved	Reserved, must be kept at reset value.
23:16	CEL[7:0]	CAN Error Logging Whenever a CAN protocol error causes the 8-bit Transmit Error Counter TEC or the 7-bit Receive Error Counter REC to increment, the Counter Error Limit CEL also increments. The increment of CEL occurs after REC or TEC increment. When reading CEL, the count value resets. The counter stops counting when the count value reaches 0xFF. The interrupt flag FDCAN_IR.ELO is set to 1 upon the next increment of TEC or REC.
15	RP	Receive Error Passive 0: Receive error counter below passive error level of 128 1: Receive error counter has reached passive error level of 128
14:8	REC[6:0]	Receive Error Counter Actual status of the receive error counter, with values ranging from 0 to 127
7:0	TEC[7:0]	Transmit Error Counter Actual status of the transmit error counter, with values ranging from 0 to 255. If FDCAN_CCCR.ASM is set to 1, in case of a CAN protocol error, TEC and REC will not increment, only CEL will increment.

41.6.13 FDCAN Protocol Status Register (FDCAN_PSR)

Address offset: 0x44

Reset value: 0x0000 0707



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Reserved	TDCV[6:0]
	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PXE	RFDF	RBRS	RESI	DLEC[2:0]			BO	EW	EP	ACT[1:0]		LEC[2:0]		
	r	r	r	r	r			r	r	r	r		r		

Bit Field	Name	Description
31:23	Reserved	Reserved, must be kept at reset value.
22:16	TDCV[6:0]	Transmitter Delay Compensation Value The position of the second sampling point (SSP) is defined as the sum of the delay time measured between pins FDCAN_TX and FDCAN_RX and FDCAN_TDCR.TDCO. During the data phase, the SSP position is the minimum number of time quanta (mtq) between the start of the transmitted bit and the second sampling point. The valid values range from 0 to 127 mtq.
15	Reserved	Reserved, must be kept at reset value.
14	PXE	Protocol Exception Event 0: No protocol exception event has occurred since the last read access 1: A protocol exception event has occurred
13	RFDF	Received a CAN FD Message This bit setting is independent of receive filtering. 0: No CAN FD message has been received since CPU reset 1: CAN FD format message received with FDF flag set to 1
12	RBRS	BRS flag of last received CAN FD Message This bit setting is independent of receive filtering. 0: No CAN FD message has been received since CPU reset 1: CAN FD format message received with FDF flag set to 1
11	RESI	ESI flag of last received CAN FD Message This bit is set together with RFDF and is independent of receive filtering. 0: ESI flag of the last received CAN FD message was not set to 1 1: ESI flag of the last received CAN FD message was set to 1
10:8	DLEC[2:0]	Data Phase Last Error Code The previous error type that occurred during the data phase of a CAN FD format frame with the BRS flag set to 1. The error type is defined according to LEC. This field is cleared when a CAN FD format frame with the BRS flag set to 1 has been successfully transmitted (received or sent) without errors.
7	BO	Bus_Off Status 0: FDCAN is not in Bus_Off state 1: FDCAN is in Bus_Off state
6	EW	Warning Status 0: Values of both error counters are less than the Error Warning limit of 96

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Bit Field	Name	Description
		1: At least one error counter has reached the Error Warning limit of 96)
5	EP	Error Passive 0: FDCAN is in Active Error state. It typically participates in bus communication and will send Active Error flags after detecting errors 1: FDCAN is in Passive Error state
4:3	ACT[1:0]	Activity Monitors the communication status of the CAN module. 00: Synchronized: Node is synchronized during CAN communication 01: Idle: Node is neither a receiver nor a transmitter 10: Receiver: Node operates as a receiver 11: Transmitter: Node operates as a transmitter *Note: ACT is set to "00" in case of a protocol exception event.*
2:0	LEC[2:0]	Last Error Code LEC indicates the type of the last error that occurred on the CAN bus. This field is cleared when a message is transmitted on the bus without errors (received or sent). 000: No Error: No errors occurred since the LEC was reset due to a successful message reception or transmission. 001: Form Error: More than 5 consecutive bits of the same level were detected in a received message, which is not allowed. 010: Stuff Error: The fixed format part of the received frame has an incorrect format. 011: Ack Error: A message sent by FDCAN was not acknowledged by other nodes. 100: Bit1 Error: During message transmission (except for the arbitration field), the device wanted to send a recessive level (bit logical value "1"), but the monitored bus value was dominant. 101: Bit0 Error: During message transmission (or ACK bit, active error flag, overload flag), the node wanted to send a dominant level (data or identifier bit logical value "0"), but the monitored bus value was recessive. During Bus_Off recovery, this status is set to 1 each time a sequence of 11 recessive bits is monitored. This allows the CPU to monitor the progression of the Bus_Off recovery sequence (indicating that the bus is not stuck in the dominant state or in continuous disturbance). 110: CRC Error: The CRC checksum of the received message is incorrect. The CRC value in the message does not match the CRC calculated from the received data. 111: No Change: Any read access to the protocol status register will reinitialize LEC to "7". If the value shown by LEC is "7", it indicates that no CAN bus event has been detected since the last read access to the protocol status register by the CPU.

Note 1: When a CAN FD frame data segment with the BRS flag set to 1 is reached, the next CAN event (error or valid frame) will be displayed in DLEC instead of LEC. Additionally, in a CAN FD CRC sequence, fixed stuffing bit errors will be treated as format errors rather than stuff errors.

Note 2: The Bus_Off recovery sequence (refer to CAN Specification 2.0 or ISO 11898-1:2015) cannot be shortened by setting FDCAN_CCCR.INIT to 1 or by reset. If the device enters Bus_Off state, FDCAN_CCCR.INIT is set to 1, and all bus activities are stopped. Once the CPU clears the FDCAN_CCCR.INIT bit, the device will return to normal

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operation only after waiting for 129 consecutive bus idle states (129×11 recessive bits). At the end of the Bus_Off recovery sequence, the error management counter values are reset. During the waiting period after the FDCAN_CCCR.INIT reset, each sequence of 11 recessive bits is monitored, and a Bit0 error code is written to FDCAN_PSR.LEC, allowing the CPU to detect whether the CAN bus remains dominant or is continuously disturbed, thus monitoring the Bus_Off recovery sequence. FDCAN_ECR.REC is used to count these sequences of recessive bits.

41.6.14 FDCAN Transmitter Delay Compensation Register (FDCAN_TDCR)

Address offset: 0x48

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TDCO[6:0]							Reserved	TDCF[6:0]						
	rw								rw						

Bit Field	Name	Description
31:15	Reserved	Reserved, must be kept at reset value.
14:8	TDCO[6:0]	Transmitter Delay Compensation SSP Offset Defines the difference between the delay measured from FDCAN_TX to FDCAN_RX and the second sampling point. The valid values range from 0 to 127 mtq.
7	Reserved	Reserved, must be kept at reset value.
6:0	TDCF[6:0]	Transmitter Delay Compensation Filter Window Length Defines the minimum value of the SSP position, disregarding dominant edges on FDCAN_RX that cause the SSP position to advance when measuring transmitter delay. The valid values range from 0 to 127 mtq.

41.6.15 FDCAN Interrupt Register (FDCAN_IR)

If the following conditions are detected (edge-sensitive), the corresponding flag is set to 1. The flag remains set to 1 until cleared by writing a "1" to the corresponding bit before host reset. Writing a "0" has no effect. Hardware reset clears the register. IE controls interrupt generation. ILS controls which interrupt line the interrupt is sent from.

Address offset: 0x50

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW

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		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30	Reserved	Reserved, must be kept at reset value.
29	ARA	Access to Reserved Register Address 0: No access to reserved register address 1: Access to reserved register address has occurred
28	PED	Protocol Error in Data Phase (Data Bit Time is used) 0: No protocol error during data phase 1: Protocol error detected during data phase (PSR.DLEC is not 0 or 7)
27	PEA	Protocol Error in Arbitration Phase(Nominal Bit Time is used) 0: No protocol error during data phase 1: Protocol error detected during data phase (PSR.DLEC is not 0 or 7)
26	WDI	Watchdog Interrupt 0: No message RAM watchdog event occurred 1: Message RAM watchdog event occurred due to missing READY
25	BO	Bus_Off Status 0：Bus_Off state unchanged 1：Bus_Off state changed
24	EW	Warning Status 0：Error_Warning state unchanged 1：Error_Warning state changed
23	EP	Error Passive 0：Error_Passive state unchanged 1：Error_Passive state changed
22	ELO	Error Logging Overflow 0: CAN error log counter not overflowed 1: CAN error log counter overflowed
21	BEU	Bit Error Uncorrected A Message RAM bit error of 2 bits or more was detected and not corrected. An uncorrected Message RAM bit error sets FDCAN_CCCR.INIT to "1". This is done to avoid transmitting corrupted data. 0= Uncorrected bit error not detected when reading from Message RAM 1= Uncorrected bit error detected.
20	BEC	Bit Error Corrected A 1bit Message RAM bit error is detected and corrected. 0= Bit error not detected when reading from Message RAM 1= Corrected bit error detected.

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Bit Field	Name	Description
19	DRX	Message stored to Dedicated Rx Buffer After the received message has been stored in the dedicated receive buffer, this flag is set to 1. 0: The receive buffer has not been updated 1: At least one received message has been stored in the dedicated receive buffer.
18	TOO	Timeout Occurred 0: No timeout 1: Timeout occurred
17	MRAF	When the receive processing meets the following conditions, the flag is set to 1: • Until the arbitration field of the next message is received, the reception filtering or storage of the current received message has not been completed. At this point, the filtering or storage of the current received message is aborted, and the next message is processed. • The current message cannot be written to the message RAM. At this point, the current message storage is aborted. In both cases, the FIFO put index will not be updated, and the new data flag of the dedicated receive buffer will not be set to 1. When the next message is stored in this position, the original message is overwritten. When the transmit processing unit cannot read data from the message RAM, this flag is also set to 1. At this point, message transmission is aborted. If the transmit processing unit access fails, the FDCAN will switch to restricted operation mode. To exit restricted operation mode, the host CPU must reset FDCAN_CCCR.ASM. 0: No message RAM access failure occurred 1: Message RAM access failure occurred
16	TSW	Timestamp Wraparound 0: Timestamp not rolled over 1: Timestamp rolled over
15	TEFL	Tx Event FIFO Element Lost 0: No loss of transmit event FIFO element 1: Loss of transmit event FIFO element, also set to 1 when attempting to write to a transmit event FIFO of size zero
14	TEFF	Tx Event FIFO Full 0: Transmit event FIFO not full 1: Transmit event FIFO full
13	TEFW	Tx Event FIFO Watermark Reached 0: Transmit event FIFO fill level below watermark flag 1: Transmit event FIFO fill level reaches watermark flag
12	TEFN	Tx Event FIFO New Entry 0: Transmit event FIFO unchanged 1: Transmit processing unit writes new transmit event FIFO element
11	TFE	Tx FIFO Empty 0: Transmit FIFO not empty

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Bit Field	Name	Description
		1: Transmit FIFO empty
10	TCF	Transmission Cancellation Finished 0: Transmit cancellation not completed 1: Transmit cancellation completed
9	TC	Transmission Completed 0: Transmit cancellation not completed 1: Transmit cancellation completed
8	HPM	High Priority Message 0: No high-priority message received 1: High-priority message received
7	RF1L	x FIFO 1 Message Lost 0: Receive FIFO 1 message not lost 1: Receive FIFO 1 message lost, also set to 1 when attempting to write to a receive FIFO 1 of size zero
6	RF1F	Rx FIFO 1 Full 0: Receive FIFO 1 not full 1: Receive FIFO 1 full
5	RF1W	Rx FIFO 1 Watermark Reached 0: Receive FIFO 1 fill level below watermark flag 1: Receive FIFO 1 fill level reaches watermark flag
4	RF1N	Rx FIFO 1 New Message 0: No new message written to receive FIFO 1 1: New message written to receive FIFO 1
3	RF0L	Rx FIFO 0 Message Lost 0: Receive FIFO 0 message not lost 1: Receive FIFO 0 message lost, also set to 1 when attempting to write to a receive FIFO 0 of size zero
2	RF0F	Rx FIFO 0 Full 0: Receive FIFO 0 not full 1: Receive FIFO 0 full
1	RF0W	Rx FIFO 0 Watermark Reached 0: Receive FIFO 0 fill level below watermark flag 1: Receive FIFO 0 fill level reaches watermark flag
0	RF0N	Rx FIFO 0 New Message 0: No new message written to receive FIFO 0 1: New message written to receive FIFO 0

41.6.16 FDCAN Interrupt Enable Register (FDCAN_IE)

The settings in the interrupt enable register determine which status changes in the interrupt register will be indicated on the interrupt line.

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Address offset: 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30	Reserved	Reserved, must be kept at reset value.
29	ARAE	Access to Reserved Address Enable 0: Disable interrupt 1: Enable interrupt
28	PEDE	Protocol Error in Data Phase Enable 0: Disable interrupt 1: Enable interrupt
27	PEAE	Protocol Error in Arbitration Phase Enable 0: Disable interrupt 1: Enable interrupt
26	WDIE	Watchdog Interrupt Enable 0: Disable interrupt 1: Enable interrupt
25	BOE	Bus_Off Status 0: Disable interrupt 1: Enable interrupt
24	EWE	Warning Status Interrupt Enable 0: Disable interrupt 1: Enable interrupt
23	EPE	Error Passive Interrupt Enable 0: Disable interrupt 1: Enable interrupt
22	ELOE	Error Logging Overflow Interrupt Enable 0: Disable interrupt 1: Enable interrupt
21	BEUE	Bit Error Uncorrected Interrupt Enable 0: Disable interrupt 1: Enable interrupt
20	BECE	Bit Error Corrected Interrupt Enable

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Bit Field	Name	Description
		0: Disable interrupt 1: Enable interrupt
19	DRXE	Message stored to Dedicated Rx Buffer Interrupt Enable 0: Disable interrupt 1: Enable interrupt
18	TOOE	Timeout Occurred Interrupt Enable 0: Disable interrupt 1: Enable interrupt
17	MRAFE	Message RAM Access Failure Interrupt Enable 0: Disable interrupt 1: Enable interrupt
16	TSWE	Timestamp Wraparound Interrupt Enable 0: Disable interrupt 1: Enable interrupt
15	TEFLE	Tx Event FIFO Element Lost Interrupt Enable 0: Disable interrupt 1: Enable interrupt
14	TEFFE	Tx Event FIFO Full Interrupt Enable 0: Disable interrupt 1: Enable interrupt
13	TEFWE	Tx Event FIFO Watermark Reached Interrupt Enable 0: Disable interrupt 1: Enable interrupt
12	TEFNE	Tx Event FIFO New Entry Interrupt Enable 0: Disable interrupt 1: Enable interrupt
11	TFEE	Tx FIFO Empty Interrupt Enable 0: Disable interrupt 1: Enable interrupt
10	TCFE	Transmission Cancellation Finished Interrupt Enable 0: Disable interrupt 1: Enable interrupt
9	TCE	Transmission Completed Interrupt Enable 0: Disable interrupt 1: Enable interrupt
8	HPME	High Priority Message Interrupt Enable 0: Disable interrupt 1: Enable interrupt
7	RF1LE	Rx FIFO 1 Message Lost Interrupt Enable 0: Disable interrupt 1: Enable interrupt

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Bit Field	Name	Description
6	RF1FE	Rx FIFO 1 Full Interrupt Enable 0: Disable interrupt 1: Enable interrupt
5	RF1WE	Rx FIFO 1 Watermark Reached Interrupt Enable 0: Disable interrupt 1: Enable interrupt
4	RF1NE	Rx FIFO 1 New Message Interrupt Enable 0: Disable interrupt 1: Enable interrupt
3	RF0LE	Rx FIFO 0 Message Lost Interrupt Enable 0: Disable interrupt 1: Enable interrupt
2	RF0FE	Rx FIFO 0 Full Interrupt Enable 0: Disable interrupt 1: Enable interrupt
1	RF0WE	Rx FIFO 0 Watermark Reached Interrupt Enable 0: Disable interrupt 1: Enable interrupt
0	RF0NE	Rx FIFO 0 New Message Interrupt Enable 0: Disable interrupt 1: Enable interrupt

41.6.17 FDCAN Interrupt Line Select Register (FDCAN_ILS)

The interrupt line select register assigns interrupts generated by specific interrupt flags in the interrupt register to one of the two module interrupt lines. To generate an interrupt, the respective interrupt line must be enabled through FDCAN_ILE.EINT0 and FDCAN_ILE.EINT1.

Address offset: 0x58

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30	Reserved	Reserved, must be kept at reset value.

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Bit Field	Name	Description
29	ARAL	Access to Reserved Address Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
28	PEDL	Protocol Error in Data Phase Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
27	PEAL	Protocol Error in Arbitration Phase Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
26	WDIL	Watchdog Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
25	BOL	Bus_Off Status 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
24	EWL	Warning Status Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
23	EPL	Error Passive Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
22	ELOL	Error Logging Overflow Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
21	BEUL	Bit Error Uncorrected Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
20	BECL	Bit Error Corrected Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
19	DRXL	Message stored to Dedicated Rx Buffer Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
18	TOOL	Timeout Occurred Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
17	MRAFL	Message RAM Access Failure Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
16	TSWL	Timestamp Wraparound Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0

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Bit Field	Name	Description
		1: Interrupt assigned to interrupt line fdcan_int1
15	TEFLL	Tx Event FIFO Element Lost Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
14	TEFFL	Tx Event FIFO Full Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
13	TEFWL	Tx Event FIFO Watermark Reached Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
12	TEFNL	Tx Event FIFO New Entry Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
11	TFEL	Tx FIFO Empty Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
10	TCFL	Transmission Cancellation Finished Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
9	TCL	Transmission Completed Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
8	HPML	High Priority Message Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
7	RF1LL	Rx FIFO 1 Message Lost Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
6	RF1FL	Rx FIFO 1 Full Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
5	RF1WL	Rx FIFO 1 Watermark Reached Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
4	RF1NL	Rx FIFO 1 New Message Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
3	RF0LL	Rx FIFO 0 Message Lost Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
2	RF0FL	Rx FIFO 0 Full Interrupt Line

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Bit Field	Name	Description
		0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
1	RF0WL	Rx FIFO 0 Watermark Reached Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1
0	RF0NL	Rx FIFO 0 New Message Interrupt Line 0: Interrupt assigned to interrupt line fdcan_int0 1: Interrupt assigned to interrupt line fdcan_int1

41.6.18 FDCAN Interrupt Line Enable Register (FDCAN_ILE)

You can enable/disable the two interrupt lines separately by configuring EINT0 and EINT1.

Address offset: 0x5C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														EINT1	EINT0
														rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved, must be kept at reset value.
1	EINT1	Enable Interrupt Line 1 0: Disable interrupt line fdcan_int1 1: Enable interrupt line fdcan_int1
0	EINT0	Enable Interrupt Line 0 0: Disable interrupt line fdcan_int0 1: Enable interrupt line fdcan_int0

41.6.19 FDCAN Global Filter Configuration Register (FDCAN_GFC)

Used for setting the global filter for message IDs, controls the filter path for standard and extended messages.

Address offset: 0x80

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										ANFS[1:0]		ANFE[1:0]		RRFS	RRFE
										rw		rw		rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved, must be kept at reset value.
5:4	ANFS[1:0]	Accept Non-matching Frames Standard Defines the handling of 11-bit ID messages received that do not match any element in the filter list. 00: Accept in receive FIFO 0 01: Accept in receive FIFO 1 10: Reject 11: Reject These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
3:2	ANFE[1:0]	Accept Non-matching Frames Extended Defines the handling of 29-bit ID messages received that do not match any element in the filter list. 00: Accept in receive FIFO 0 01: Accept in receive FIFO 1 10: Reject 11: Reject These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
1	RRFS	Reject Remote Frames Standard 0: Accept remote frames with 11-bit standard ID for filtering 1: Reject all remote frames with 11-bit standard ID These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
0	RRFE	Reject Remote Frames Extended 0: Accept remote frames with 29-bit extended ID for filtering 1: Reject all remote frames with 29-bit extended ID These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.

41.6.20 FDCAN Standard ID Filter Configuration Register (FDCAN_SIDFC)

Used for setting 11-bit standard message ID filtering. The standard ID filter configuration controls the filter path for standard messages, refer to the Figure 41-7.

Address offset: 0x84

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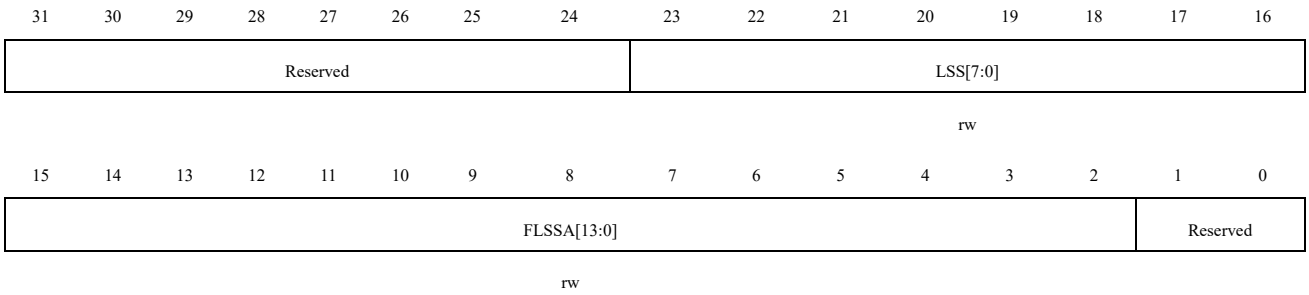
Reset value: 0x0000 0000



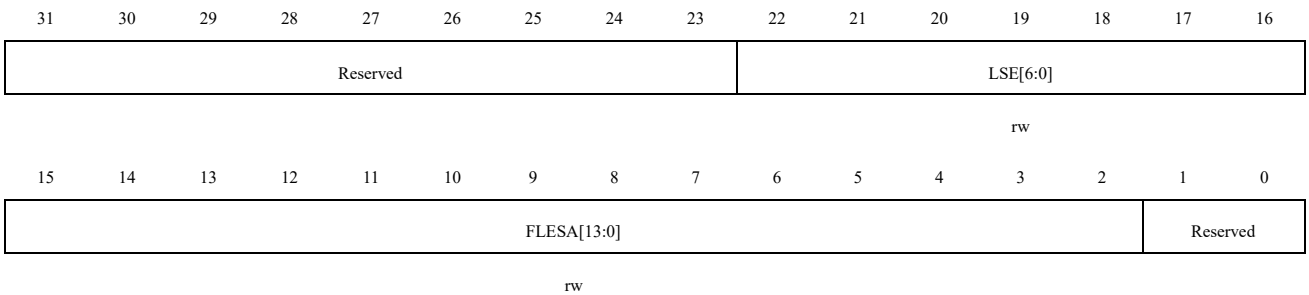
Bit Field	Name	Description
31:24	Reserved	Reserved, must be kept at reset value.
23:16	LSS[7:0]	List Size Standard 0: No standard message ID filters 1-128: Number of standard message ID filter elements >128: Values greater than 128 will be interpreted as 128. These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
15:2	FLSSA[13:0]	Filter List Standard Start Address The offset of the start address of the standard message ID filter list storage area relative to the start address of the message RAM, in words (32-bit units). These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
1:0	Reserved	Reserved, must be kept at reset value.

41.6.21 FDCAN Extended ID Filter Configuration Register (FDCAN_XIDFC)

Used for setting 29-bit extended message ID filtering. The extended ID filter configuration controls the filter path for extended messages, refer to Figure 41-8

Address offset: 0x88

Reset value: 0x0000 0000



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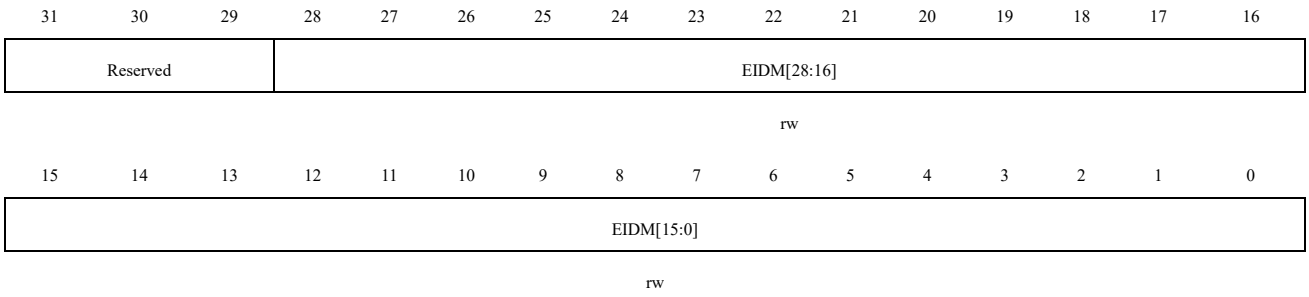
Bit Field	Name	Description
31:23	Reserved	Reserved, must be kept at reset value.
22:16	LSE[6:0]	List Size Extended 0: No extended message ID filters 1-64: Number of extended message ID filter elements >64: Values greater than 64 will be interpreted as 64. These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
15:2	FLESA[13:0]	Filter List Extended Start Address The offset of the start address of the extended message ID filter storage area relative to the start address of the message RAM, in words (32-bit units). These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
1:0	Reserved	Reserved, must be kept at reset value.

41.6.22 FDCAN Extended ID and Mask Register (FDCAN_XIDAM)

Address offset: 0x90

Reset value: 0x1FFF FFFF



Bit Field	Name	Description
31:29	Reserved	Reserved, must be kept at reset value.
28:0	EIDM[28:0]	Extended ID Mask Before receiving filtering for extended frames, the extended ID mask is first ANDed with the message ID of the received frame. Used to mask the 29-bit ID in SAE J1939. All bits are set to 1 after reset, making the mask invalid. These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.

41.6.23 FDCAN High Priority Message Status Register (FDCAN_HPMS)

When the message ID filter element is configured to generate a priority event, this register is updated with each match. This register can be used to monitor the status of incoming high-priority messages for quick access.

Address offset: 0x94

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX[6:0]							MSI[1:0]		BIDX[5:0]					
r	r							r		r					

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value.
15	FLST	Filter List Indicates the filter list where the matching filter element is located. 0: Standard filter list 1: Extended filter list
14:8	FIDX[6:0]	Filter Index Index of the filter element that matches the current message. Range is from 0 to FDCAN_SIDFC.LSS-1 or FDCAN_XIDFC.LSE-1.
7:6	MSI[1:0]	Message Storage Indicator 00: No FIFO selected 01: FIFO message lost 10: Message stored in FIFO 0 11: Message stored in FIFO 1
5:0	BIDX[5:0]	Buffer Index Index of the receive FIFO element where the message is stored. Only valid when MSI[1] = "1".

41.6.24 FDCAN New Data 1 Register (FDCAN_NDAT1)

Address offset: 0x98

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24	ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

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Bit Field	Name	Description
31:0	ND[31:0]	New Data[31:0] This register is the New Data flag for receive buffers 0 to 31. When a receive buffer is updated with a received frame, the corresponding flag is set to 1. The flag remains set to 1 until cleared by the host. Writing a 1 to the corresponding bit clears the flag. Writing "0" has no effect. The register is cleared on hardware reset. 0: Receive buffer not updated 1: New message received in receive buffer

41.6.25 FDCAN New Data 2 Register (FDCAN_NDAT2)

Address offset: 0x9C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56	ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40	ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31:0	ND[63:32]	New Data[63:32] This register is the New Data flag for receive buffers 32 to 63. When a receive buffer is updated with a received frame, the corresponding flag is set to 1. The flag remains set to 1 until cleared by the host. Writing a 1 to the corresponding bit clears the flag. Writing "0" has no effect. The register is cleared on hardware reset. 0: Receive buffer not updated 1: New message received in receive buffer

41.6.26 FDCAN Receive FIFO 0 Configuration Register (FDCAN_RXF0C)

Address offset: 0xA0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM[6:0]							Reserved	F0S[6:0]						
rw	rw								rw						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0SA[13:0]														Reserved	

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rw

Bit Field	Name	Description
31	F0OM	Rx FIFO 0 Operation mode 0: Receive FIFO 0 in blocking mode 1: Receive FIFO 0 in overwrite mode
30:24	F0WM[6:0]	0: Disable watermark interrupt 1-64: Level of receive FIFO 0 watermark interrupt (FDCAN_IR.RF0W) >64: Disable watermark interrupt These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
23	Reserved	Reserved, must be kept at reset value.
22:16	F0S[6:0]	Rx FIFO 0 Size 0: No receive FIFO 0 1-64: Number of elements in receive FIFO 0 >64: Values greater than 64 will be interpreted as 64 The index range of receive FIFO 0 elements is from 0 to F0S-1.
15:2	F0SA[13:0]	Rx FIFO 0 Start Address The offset of the start address of the receive FIFO 0 storage area in the message RAM relative to the start address of the message RAM, in words (32-bit units).)
1:0	Reserved	Reserved, must be kept at reset value.

41.6.27 FDCAN Receive FIFO 0 Status Register (FDCAN_RXF0S)

Address offset: 0xA4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						RF0L	F0F	Reserved		F0PI[5:0]					
						r	r			r					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		F0GI[5:0]						Reserved		F0FL[6:0]					
		r								r					

Bit Field	Name	Description
31:26	Reserved	Reserved, must be kept at reset value.
25	RF0L	Rx FIFO 0 Message Lost When FDCAN_IR.RF0L is reset, this bit is also reset. 0: No message lost in receive FIFO 0 1: Message lost in receive FIFO 0, also set to 1 when attempting to write to a receive

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Bit Field	Name	Description
		FIFO 0 of size zero
24	F0F	Rx FIFO 0 Full 0: Receive FIFO 0 not full 1: Receive FIFO 0 full
23:22	Reserved	Reserved, must be kept at reset value.
21:16	F0PI[5:0]	Rx FIFO 0 Put Index Receive FIFO 0 write index pointer, range from 0 to 63.
15:14	Reserved	Reserved, must be kept at reset value.
13:8	F0GI[5:0]	Rx FIFO 0 Get Index Receive FIFO 0 write index pointer, range from 0 to 63.
7	Reserved	Reserved, must be kept at reset value.
6:0	F0FL[6:0]	Rx FIFO 0 Fill Level Receive FIFO 0 write index pointer, range from 0 to 64.

41.6.28 FDCAN Receive FIFO 0 Acknowledge Register (FDCAN_RXF0A)

Address offset: 0xA8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										F0AI[5:0]					
										rw					

Bit Field	Name	Description
31:6	Reserved	Reserved, must be kept at reset value.
5:0	F0AI[5:0]	Rx FIFO 0 Acknowledge Index After the host reads a message or message sequence from receive FIFO 0, the host must write the buffer index of the last read element to F0AI. This operation sets the receive FIFO 0 get index FDCAN_RXF0S.F0GI to F0AI + 1 and updates the FIFO 0 fill level FDCAN_RXF0S.F0FL.

41.6.29 FDCAN Receive Buffer Configuration Register (FDCAN_RXBC)

Address offset: 0xAC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA[13:0]														Reserved	
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, must be kept at reset value.
15:2	RBSA[13:0]	Rx Buffer Start Address Configures the start address (32-bit word address) of the dedicated receive buffer section in the message RAM. Also used for referencing debug messages A, B, C. These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
1:0	Reserved	Reserved, must be kept at reset value.

41.6.30 FDCAN Receive FIFO 1 Configuration Register (FDCAN_RXF1C)

Address offset: 0xB0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM[6:0]							Reserved	F1S[6:0]						
rw	rw								rw						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F1SA[13:0]														Reserved	
rw															

Bit Field	Name	Description
31	F1OM	Rx FIFO 1 Operation mode 0: Receive FIFO 1 in blocking mode 1: Receive FIFO 1 in overwrite mode
30:24	F1WM[6:0]	0: Disable watermark interrupt 1-64: Level of receive FIFO 1 watermark interrupt (FDCAN_IR.RF1W) >64: Disable watermark interrupt These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
23	Reserved	Reserved, must be kept at reset value.
22:16	F1S[6:0]	Rx FIFO 1 Size 0: No receive FIFO 1

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Bit Field	Name	Description
		1-64: Number of elements in receive FIFO 1 >64: Values greater than 64 will be interpreted as 64 The index range of receive FIFO 1 elements is from 0 to F1S-1.
15:2	F1SA	Rx FIFO 1 Start Address The offset of the start address of the receive FIFO 1 storage area in the message RAM relative to the start address of the message RAM, in words (32-bit units).)
1:0	Reserved	Reserved, must be kept at reset value.

41.6.31 FDCAN Receive FIFO 1 Status Register (FDCAN_RXF1S)

Address offset: 0xB4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMS[1:0]		Reserved				RF1L	F1F	Reserved		F1PI[5:0]					
r						r	r			r					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		F1GI[5:0]						Reserved		F1FL[6:0]					
		r								r					

Bit Field	Name	Description
31:30	DMS[1:0]	Debug Message Status 00: Idle state, waiting to receive debug message 01: Debug message A received 10: Debug messages A and B received 11: Debug messages A, B, and C received
29:26	Reserved	Reserved, must be kept at reset value.
25	RF1L	Rx FIFO 1 Message Lost When FDCAN_IR.RF1L is reset, this bit is also reset. 0: No message lost in receive FIFO 1 1: Message lost in receive FIFO 1, also set to 1 when attempting to write to a receive FIFO 1 of size zero
24	F1F	Rx FIFO 1 Full 0: Receive FIFO 1 not full 1: Receive FIFO 1 full
23:22	Reserved	Reserved, must be kept at reset value.
21:16	F1PI[5:0]	Rx FIFO 1 Put Index Receive FIFO 1 write index pointer, range from 0 to 63.
15:14	Reserved	Reserved, must be kept at reset value.
13:8	F1GI[5:0]	Rx FIFO 1 Get Index

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Bit Field	Name	Description
		Receive FIFO 1 write index pointer, range from 0 to 63.
7	Reserved	Reserved, must be kept at reset value.
6:0	F1FL[6:0]	Rx FIFO 1 Fill Level Receive FIFO 1 write index pointer, range from 0 to 64.

41.6.32 FDCAN Receive FIFO 1 Acknowledge Register (FDCAN_RXF1A)

Address offset: 0xB8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										F1AI[5:0]					
										rw					

Bit Field	Name	Description
31:6	Reserved	Reserved, must be kept at reset value.
5:0	F1AI[5:0]	Rx FIFO 1 Acknowledge Index After the host reads a message or message sequence from receive FIFO 1, the host must write the buffer index of the last read element to F1AI. This operation sets the receive FIFO 1 get index FDCAN_RXF1S.F1GI to F1AI + 1 and updates the FIFO 1 fill level FDCAN_RXF1S.F1FL.

41.6.33 FDCAN Receive Buffer/FIFO Element Size Configuration Register (FDCAN_RXESC)

Configures the number of data field bytes for receive buffer and receive FIFO elements. Data field sizes greater than 8 bytes are only used for CAN FD.

Address offset: 0xBC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	RBDS[2:0]	Reserved	F1DS[2:0]	Reserved	F0DS[2:0]
	rw		rw		rw

Bit Field	Name	Description
31:11	Reserved	Reserved, must be kept at reset value.
10:8	RBDS[2:0]	Rx Buffer Data Field Size 000: 8-byte data field 001: 12-byte data field 010: 16-byte data field 011: 20-byte data field 100: 24-byte data field 101: 32-byte data field 110: 48-byte data field 111: 64-byte data field
7	Reserved	Reserved, must be kept at reset value.
6:4	F1DS[2:0]	Rx FIFO 0 Data Field Size 000: 8-byte data field 001: 12-byte data field 010: 16-byte data field 011: 20-byte data field 100: 24-byte data field 101: 32-byte data field 110: 48-byte data field 111: 64-byte data field
3	Reserved	Reserved, must be kept at reset value.
2:0	F0DS[2:0]	Rx FIFO 1 Data Field Size 000: 8-byte data field 001: 12-byte data field 010: 16-byte data field 011: 20-byte data field 100: 24-byte data field 101: 32-byte data field 110: 48-byte data field 111: 64-byte data field

Note: If the data field size of the received CAN frame exceeds the data field size configured for the Rx buffer or Rx FIFO, only the number of bytes configured by RXESC will be stored in the Rx buffer or Rx FIFO element, and the rest will be ignored.

41.6.34 FDCAN Transmit Buffer Configuration Register (FDCAN_TXBC)

Address offset: 0xC0

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Reset value: 0x0000 0000

Bit Field	Name	Description
31	Reserved	Reserved, must be kept at reset value.
30	TFQM	Tx FIFO/Queue Mode 0: Transmit FIFO mode 1: Transmit queue mode These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
29:24	TFQS[5:0]	Transmit FIFO/Queue Size 0: No transmit FIFO/queue 1-32: Number of transmit buffers used for transmit FIFO/queue >32: Values greater than 32 will be interpreted as 32 These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
23:22	Reserved	Reserved, must be kept at reset value.
21:16	NDTB[5:0]	Number of Dedicated Transmit Buffers 0: No dedicated transmit buffer 1-32: Number of dedicated transmit buffers >32: Values greater than 32 will be interpreted as 32 These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
15:2	TBSA[13:0]	Tx Buffer Start Address Start address (32-bit word address) of the transmit buffer section in the message RAM. These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
1:0	Reserved	Reserved, must be kept at reset value.

Note: The sum of TFQS and NDTB cannot exceed 32. FDCAN does not check for configuration errors. The transmit buffer section in the message RAM starts from the dedicated transmit buffer.

41.6.35 FDCAN Transmit FIFO/Queue Status Register (FDCAN_TXFQS)

The transmit FIFO/queue status is related to the transmit requests in FDCAN_TXBRP. Therefore, adding/canceling transmit requests may be delayed due to an ongoing transmit scan (FDCAN_TXBRP has not been updated yet).

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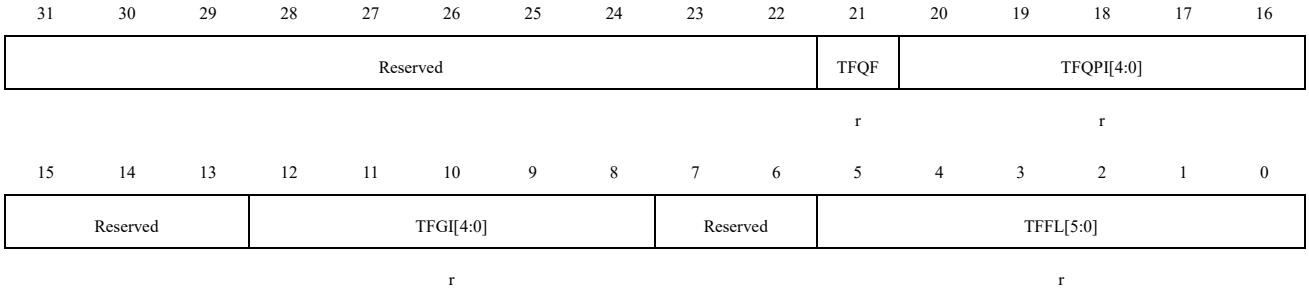
Address offset: 0xC4

Reset value: 0x0000 0000



Bit Field	Name	Description
31:22	Reserved	Reserved, must be kept at reset value.
21	TFQF	Tx FIFO/Queue Full 0: Transmit FIFO/queue not full 1: Transmit FIFO/queue full
20:16	TFQPI[4:0]	Tx FIFO/Queue Put Index Transmit FIFO/queue write index pointer, range from 0 to 31
15:13	Reserved	Reserved, must be kept at reset value.
12:8	TFGI[4:0]	Tx FIFO Get Index Transmit FIFO read index pointer, range from 0 to 31. If configured as a transmit queue (FDCAN_TXBC.TFQM = "1"), the readout value is always zero.
7:6	Reserved	Reserved, must be kept at reset value.
5:0	TFFL[5:0]	Tx FIFO Free Level Number of consecutive free transmit FIFO elements starting from TFGI, range from 0 to 32. If transmit queue operation is configured (FDCAN_TXBC.TFQM = "1"), the readout value is always zero.

Note: In a hybrid configuration combining dedicated transmit buffers with transmit FIFO or transmit queue, the write and get index pointers indicate the transmit buffer index starting from the first dedicated transmit buffer.

For example: In a hybrid configuration combining 12 dedicated transmit buffers with a transmit FIFO containing 20 buffers, a write index of 15 would point to the fourth transmit buffer in the transmit FIFO.

41.6.36 FDCAN Transmit Buffer Element Size Configuration Register (FDCAN_TXESC)

Configures the number of data segment bytes for transmit buffer elements. Data segment sizes greater than 8 bytes are only used for CAN FD.

Address offset: 0xC8

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													TBDS[2:0]		
													rw		

Bit Field	Name	Description
31:3	Reserved	Reserved, must be kept at reset value.
2:0	TBDS[2:0]	Tx Buffer Data Field Size 000: 8-byte data field 001: 12-byte data field 010: 16-byte data field 011: 20-byte data field 100: 24-byte data field 101: 32-byte data field 110: 48-byte data field 111: 64-byte data field

41.6.37 FDCAN Transmit Buffer Request Pending Register (FDCAN_TXBRP)

Address offset: 0xCC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24	TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP15	TRP14	TRRP13	TRP112	TRP11	TRP10	TRP9	TRP8	TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:0	TRP[31:0]	Transmission Request Pending Each transmit buffer has its own transmit request pending bit, set to 1 by the FDCAN_TXBAR register. The corresponding bit is reset once the requested transmission is completed or canceled via FDCAN_TXBCR. FDCAN_TXBRP will only set the position corresponding to the valid transmit buffer configured by FDCAN_TXBC to 1. Once a position in FDCAN_TXBRP is set to 1, a

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Bit Field	Name	Description
		transmit scan is initiated to check the transmit request with the highest priority (the transmit buffer with the smallest message ID). Canceling a request will reset the corresponding transmit request pending bit in the FDCAN_TXBRP register. If the transmission has already started when the request is canceled, the reset operation will be performed at the end of the transmission, regardless of its success. Once the corresponding FDCAN_TXBRP bit is reset, the cancel request bit will also be immediately reset. A request cancellation will be indicated as successful by setting the FDCAN_TXBCF bit to 1 under the following conditions: - Successful transmission, with the corresponding FDCAN_TXBTO bit set to 1 - Transmission was canceled before it started - Transmission was aborted due to arbitration loss - Error occurred during transmission In DAR mode, all transmissions are automatically canceled after a transmission failure. For all unsuccessful transmissions, the corresponding FDCAN_TXBCF bit is set to 1. 0: No transmit request pending 1: Transmit request pending

Note: If an FDCAN_TXBRP bit is set to 1 during an ongoing transmit scan, the current transmit scan will ignore this bit. If a request to cancel such a transmit buffer is made, the request will be immediately canceled, and the corresponding FDCAN_TXBRP bit will be reset.

41.6.38 FDCAN Transmit Buffer Add Request Register (TXBAR)

Address offset: 0xD0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	AR[31:0]	Add Request Each transmit buffer has its own add request bit. Writing a 1 will set the corresponding add request bit to 1, while writing a 0 has no effect. A single write operation by the host

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Bit Field	Name	Description
		to TXBAR can add transmit requests for multiple transmit buffers, but only the valid transmit buffer configured by FDCAN_TXBC will be set to 1. If no transmit scan is running, these bits will be immediately reset; otherwise, they will remain set to 1 until the transmit scan process is completed. 0: No transmit request added 1: Transmit request added

Note: If a transmit buffer for which the transmit request bit is already set to 1 receives an add request, the duplicate request will be ignored.

41.6.39 FDCAN Transmit Buffer Cancellation Request Register (FDCAN_TXBCR)

Address offset: 0xD4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	CR[31:0]	Cancellation Request Each transmit buffer has its own cancel request bit. Writing a 1 will set the corresponding cancel request bit to 1, while writing a 0 has no effect. A single write operation by the host to FDCAN_TXBCR can set cancel requests for multiple transmit buffers, but only the valid transmit buffer configured by FDCAN_TXBC will be set to 1. These bits will remain set to 1 until the corresponding FDCAN_TXBRP bit is reset. 0: No cancel request 1: Cancel requested

41.6.40 FDCAN Transmit Buffer Transmission Occurred Register (FDCAN_TXBTO)

Address offset: 0xD8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24	TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:0	TO[31:0]	Transmission Occurred Each transmit buffer has its own transmission occurred bit. When the corresponding FDCAN_TXBRP bit is cleared after a successful transmission, the respective bit in this register is set to 1. These bits are reset when a new transmission is requested by writing a 1 to the corresponding bit in FDCAN_TXBAR. 0: No transmission occurred 1: Transmission occurred

41.6.41 FDCAN Transmit Buffer Cancellation Finished Register (FDCAN_TXBCF)

Address offset: 0xDC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:0	CF[31:0]	Cancellation Finished Each transmit buffer has its own cancellation finished bit. When the corresponding FDCAN_TXBRP bit is cleared after a cancel request through the respective FDCAN_TXBCR bit, the corresponding bit in this register is set to 1. If the corresponding bit in this register is not set to 1 when a cancel request is made, the bit in this register is immediately set to 1. When a 1 is written to the corresponding bit in the FDCAN_TXBAR register to request a new transmission, the bit in this register is reset. 0: No transmit buffer cancellation 1: Transmit buffer cancellation finished

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41.6.42 FDCAN Transmit Buffer Transmission Interrupt Enable Register (FDCAN_TXBTIE)

Address offset: 0xE0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24	TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8	TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	TIE[31:0]	Transmission Interrupt Enable Each transmit buffer has its own transmission interrupt enable bit. 0: Disable transmission interrupt 1: Enable transmission interrupt

41.6.43 FDCAN Transmit Buffer Cancellation Finished Interrupt Enable Register (FDCAN_TXBCIE)

Address offset: 0xE4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	CFIE[31:0]	Cancellation Finished Interrupt Enable Each transmit buffer has its own cancel completion interrupt enable bit 0: Disable cancel completion interrupt

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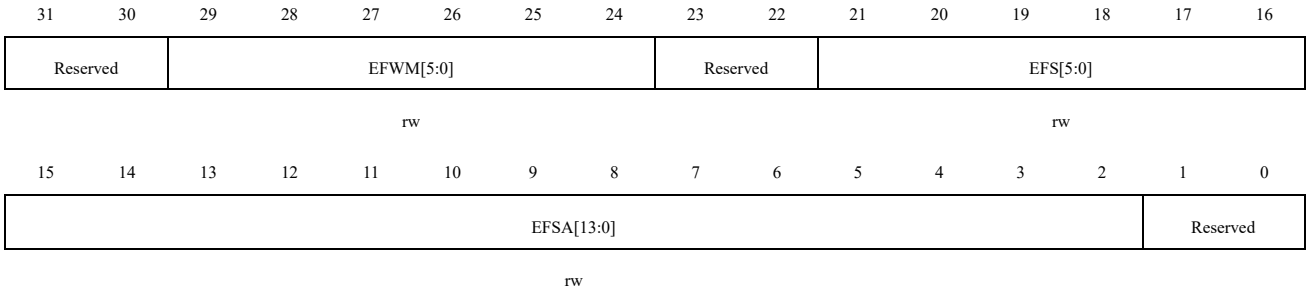
Bit Field	Name	Description
		1: Enable cancel completion interrupt

41.6.44 FDCAN Transmit Event FIFO Configuration Register (FDCAN_TXEFC)

Address offset: 0xF0

Reset value: 0x0000 0000



Bit Field	Name	Description
31:30	Reserved	Reserved, must be kept at reset value.
29:24	EFWM[5:0]	Event FIFO Watermark 0: Disable watermark interrupt 1-32: Level of transmit event FIFO watermark interrupt (FDCAN_IR.TEFW) >32: Disable watermark interrupt These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
23:22	Reserved	Reserved, must be kept at reset value.
21:16	EFS[5:0]	Event FIFO Size 0: Disable transmit event FIFO 1-32: Number of transmit event FIFO elements >32: Values greater than 32 will be interpreted as 32 The index of transmit event FIFO elements is from 0 to EFS – 1 These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
15:2	EFSA[13:0]	Event FIFO Start Address The offset of the start address of the transmit event FIFO storage area in the message RAM relative to the start address of the message RAM, in words (32-bit units). These bits are write-protected and can only be accessed for writing when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are both 1.
1:0	Reserved	Reserved, must be kept at reset value.

41.6.45 FDCAN Transmit Event FIFO Status Register (FDCAN_TXEFS)

Address offset: 0xF4

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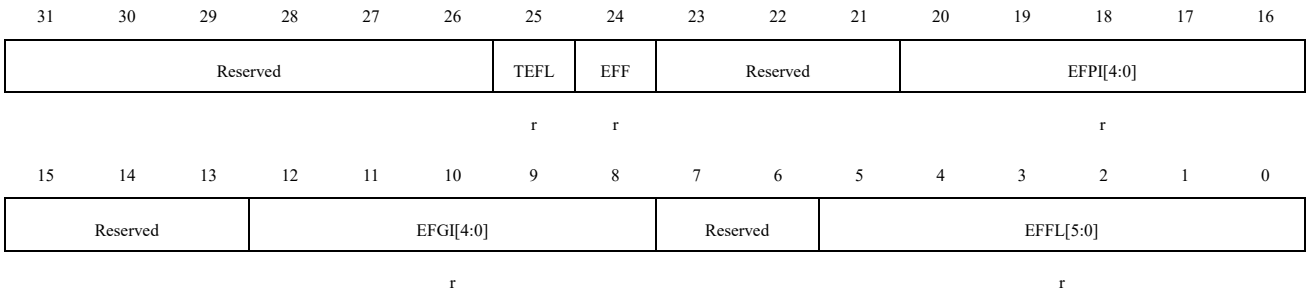
Reset value: 0x0000 0000

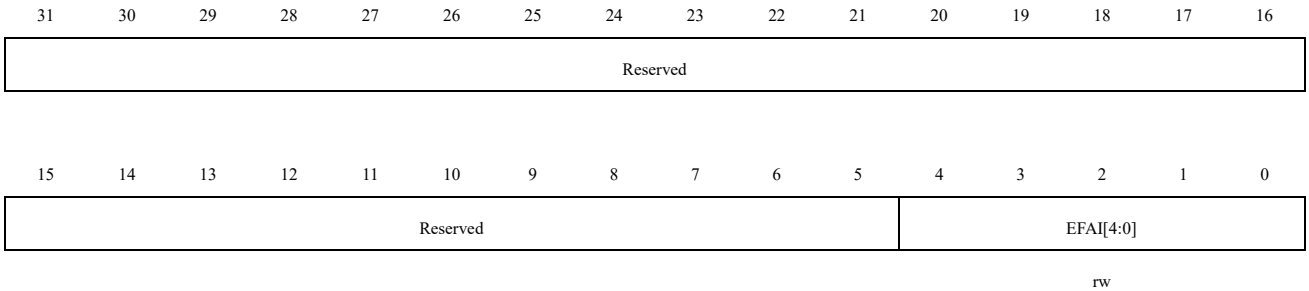


Bit Field	Name	Description
31:26	Reserved	Reserved, must be kept at reset value.
25	TEFL	Tx Event FIFO Element Lost When FDCAN_IR.TEFL is reset, this bit is also reset. 0: No transmit event FIFO element lost 1: Transmit event FIFO element lost, also set to 1 when attempting to write to a transmit event FIFO of size zero
24	EFF	Event FIFO Full 0: Transmit event FIFO not full 1: Transmit event FIFO full
23:21	Reserved	Reserved, must be kept at reset value.
20:16	EFPI[4:0]	Event FIFO Put Index Transmit event FIFO put index pointer, range from 0 to 31
15:13	Reserved	Reserved, must be kept at reset value.
12:8	EFGI[4:0]	Event FIFO Get Index Transmit event FIFO read index pointer, range from 0 to 31
7:6	Reserved	Reserved, must be kept at reset value.
5:0	EFFL[5:0]	Event FIFO Fill Level Number of elements stored in the transmit event FIFO, range from 0 to 31

41.6.46 FDCAN Transmit Event FIFO Acknowledge Register (FDCAN_TXEFA)

Address offset: 0xF8

Reset value: 0x0000 0000



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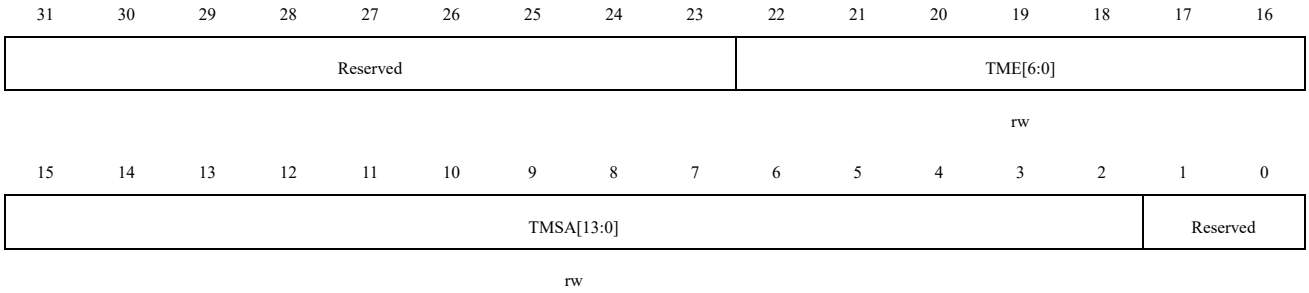
Bit Field	Name	Description
31:5	Reserved	Reserved, must be kept at reset value.
4:0	EFAI[4:0]	Event FIFO Acknowledge Index Once the host reads an element or a sequence of elements from the transmit event FIFO, it must write the index value of the last read element to EFAI. This action sets the transmit event FIFO get index FDCAN_TXEFS.EFGI to EFAI + 1 and updates the FIFO fill level FDCAN_TXEFS.EFFL.

41.6.47 FDCAN TT Trigger Memory Configuration Register (FDCAN_TTTMC)

Address offset: 0x0100

Reset value: 0x0000 0000



Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:16	TME[6:0]	Trigger memory elements 0: No trigger memory 1-64: Number of trigger memory elements >64: Values greater than 64 are interpreted as 64 These are protected write bits, write access is possible only when bit FDCAN_CCCR.CCE and bit FDCAN_CCCR.INIT are set to 1.
15:2	TMSA[13:0]	Trigger memory start address Start address of trigger memory in message RAM (32-bit word address, see Figure 41-1 Example diagram of FDCAN Message RAM allocation). These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1
1:0	Reserved	Reserved, the reset value must be maintained.

41.6.48 FDCAN TT Reference Message Configuration Register (FDCAN_TTRMC)

Address offset: 0x0104

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RMPS	XTD	Reserved	RID[28:16]												
rw	rw		rw												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RID[15:0]															
rw															

Bit field	Name	Description
31	RMPS	Reference message Payload select Ignored in case of time slaves. 0: Reference message has no additional payload 1: The following elements are taken from Tx buffer 0: Message marker MM, Event FIFO control EFC, Data length code DLC, Data Bytes DB (level 1: bytes 2-8, level 0, 2: bytes 5-8) These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
30	XTD	Extended identifier 0: 11-bit standard identifier 1: 29-bit extended identifier These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
29	Reserved	Reserved, the reset value must be maintained.
28:0	RID[28:0]	Reference identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

41.6.49 FDCAN TT Operation Configuration Register (FDCAN_TTOCF)

Address offset: 0x0108

Reset value: 0x0001 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					EVTP	ECC	EGTF	AWL[7:0]							
					rw	rw	rw	rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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EECS	IRTO[6:0]	LDSDL[2:0]	TM	GEN	Reserved	OM[1:0]
rw	rw	rw	rw	rw		rw

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	EVTP	Event trigger polarity. 0: Rising edge trigger 1: Falling edge trigger These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
25	ECC	Enable clock calibration. 0: Automatic clock calibration in FDCAN level 0, 2 is disabled 1: Automatic clock calibration in FDCAN level 0, 2 is enabled These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
24	EGTF	Enable global time Filtering. 0: Global time filtering in FDCAN level 0, 2 is disabled 1: Global time filtering in FDCAN level 0, 2 is enabled These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
23:16	AWL[7:0]	Application watchdog limit. The application watchdog can be disabled by programming AWL to 0x00. 0x00–FF: Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
15	EECS	Enable external clock synchronization If enabled, TUR configuration (FDCAN_TURCF.NCL only) may be updated during FDCAN operation. 0: External clock synchronization in FDCAN level 0, 2 disabled 1: External clock synchronization in FDCAN level 0, 2 enabled These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
14:8	IRTO[6:0]	Initial reference trigger offset. 0x00–7F Positive offset, range from 0 to 127 These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
7:5	LDSDL[2:0]	LD of synchronization deviation limit. The synchronization deviation limit SDL is configured by its dual logarithm LDSDL with SDL = 2 ^ (LDSDL + 5). SDL is comprised between 32 and 4096. It should not exceed the clock tolerance given by the CAN bit timing configuration.

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Bit field	Name	Description
		These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
4	TM	Time master. 0: Time master function disabled 1: Potential time master These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
3	GEN	Gap enable. 0: Strictly time-triggered operation 1: External event-synchronized time-triggered operation These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
2	Reserved	Reserved, the reset value must be maintained.
1:0	OM[1:0]	Operation mode. 00: Event-driven CAN communication, default 01: TTCAN level 1 10: TTCAN level 2 11: TTCAN level 0. These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

41.6.50 FDCAN TT Matrix Limits Register (FDCAN_TTMLM)

Address offset: 0x010C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				ENTT[11:0]											
				rw											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXEW[3:0]				CSS[1:0]		CCM[5:0]					
				rw				rw		rw					

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:16	ENTT[11:0]	Expected Number of Tx triggers 0x000–FFF Expected number of Tx triggers in one matrix cycle These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
15:12	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
11:8	TXEW[3:0]	Tx enable Window 0x0–F Length of Tx enable window, 1-16 NTU cycles These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
7:6	CSS[1:0]	Cycle start synchronization Enables sync pulse output . 00: No sync pulse 01: Sync pulse at start of basic cycle 10: Sync pulse at start of matrix cycle 11: Reserved These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
5:0	CCM[5:0]	Cycle count Max 0x00: 1 basic cycle per matrix cycle 0x01: 2 basic cycles per matrix cycle 0x03: 4 basic cycles per matrix cycle 0x07: 8 basic cycles per matrix cycle 0x0F: 16 basic cycles per matrix cycle 0x1F: 32 basic cycles per matrix cycle 0x3F: 64 basic cycles per matrix cycle Others: Reserved These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

41.6.51 FDCAN TUR Configuration Register (FDCAN_TURCF)

Address offset: 0x0110

Reset value: 0x1000 0000

The length of the NTU is given by: NTU = CAN clock period x NC/DC.

NC is an 18-bit value. Its high part, NCH[17:16] is hard wired to 0b01. Therefore the range of NC extends from 0x10000 to 0x1FFFF. The value configured by NCL is the initial value for FDCAN_TURNA.NAV[15:0]. DC is set to 0x1000 by hardware reset and it may not be written to 0x0000.

• Level 1: NC ≥ 4 × DC and NTU = CAN bit time

• Levels 0 and 2: NC ≥ 8 × DC

The actual value of FDCAN_TUR may be changed by the clock drift compensation function of TTCAN level 0 and level 2 in order to adjust the node local view of the NTU to the time master view of the NTU. DC will not be changed by the automatic drift compensation, FDCAN_TURNA.NAV may be adjusted around NC in the range of the synchronization deviation limit given by FDCAN_TTOCF.LDSDL. NC and DC should be programmed to the largest suitable values in achieve the best computational accuracy for the drift compensation process.

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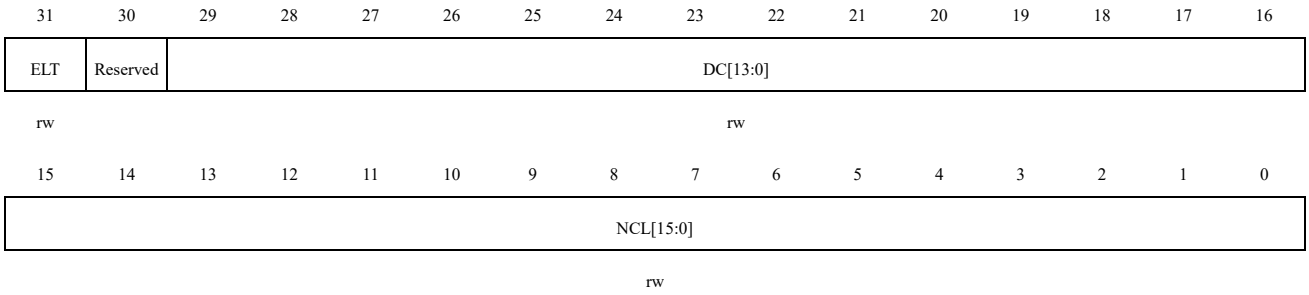
Note: If NC < 7 × DC in TTCAN level 1, it is required that subsequent time marks in the trigger memory must differ by at least two NTUs.



Bit field	Name	Description
31	ELT	Enable local time. 0: Local time is stopped, default 1: Local time is enabled These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1. *Note: The local time is started by setting ELT. It remains active until ELT is reset or until the next hardware reset. FDCAN_TURCF.DC is locked when FDCAN_TURCF.ELT = 1. If ELT is written to 0, the readable value will stay at 1 until the new value has been synchronized into the CAN clock domain. During this time write access to the other bits of the register remains locked.*
30	Reserved	Reserved, the reset value must be maintained.
29:16	DC[13:0]	Denominator configuration. 0x0000: Illegal value 0x0001 to 0x3FFF: Denominator configuration These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.
15:0	NCL[15:0]	Numerator configuration low. Write access to the TUR numerator configuration low is only possible during configuration with FDCAN_TURCF.ELT = 0 or if FDCAN_TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT configuration mode, the new value takes effect when FDCAN_TTOST.WECS is cleared to 0. NCL is locked FDCAN_TTOST.WECS is 1. 0x0000–FFFF Numerator configuration low These are protected write bits, write access is possible only when FDCAN_CCCR.CCE and FDCAN_CCCR.INIT are set to 1.

41.6.52 FDCAN TT Operation Control Register (FDCAN_TTOCN)

Address offset: 0x0114

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCKC	Reserved	ESCN	NIG	TMG	FGP	GCS	TTIE	TMC[1:0]		RTIE	SWS[1:0]		SWP	ECS	SGT
r		rw	rw	rw	rw	rw	rw	rw		rw	rw		rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	LCKC	TT operation control register Locked. Set by a write access to register FDCAN_TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0: Write access to FDCAN_TTOCN enabled 1: Write access to FDCAN_TTOCN locked
14	Reserved	Reserved, the reset value must be maintained.
13	ESCN	External synchronization control If enabled the FDCAN synchronizes its cycle time phase to an external event signaled by a rising edge at event trigger pin (see Section 41.5.10: Synchronization to external time schedule). 0: External synchronization disabled 1: External synchronization enabled
12	NIG	Next is Gap. This bit can only be set when the FDCAN is the actual time master and when it is configured for external event-synchronized time-triggered operation (FDCAN_TTOCF.GEN = 1) 0: No action, reset by reception of any reference message 1: Transmit next reference message with Next_is_Gap = 1
11	TMG	Time mark Gap. 0: Reset by each reference message 1: Next reference message started when register time mark interrupt FDCAN_TTIR.RTMI is activated
10	FGP	Finish Gap. Set by the CPU, reset by each reference message 0: No reference message requested 1: Application requested start of reference message
9	GCS	Gap control select 0: Gap control independent from event trigger 1: Gap control by input event trigger pin
8	TTIE	Trigger time mark interrupt pulse enable External time mark events are configured by trigger memory element TMEX. A trigger

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Bit field	Name	Description
		time mark interrupt pulse is generated when the trigger memory element becomes active, and the FDCAN is in synchronization state In_Schedule or In_Gap. 0: Trigger time mark interrupt output fdcan1_tmp for more than one instance and fdcan_tmp if only one instance disabled 1: Trigger time mark interrupt output fdcan1_tmp for more than one instance and fdcan_tmp if only one instance enabled
7:6	TMC[1:0]	Register time mark Compare. 00: No Register time mark interrupt generated 01: Register time mark interrupt if time mark = cycle time 10: Register time mark interrupt if time mark = local time 11: Register time mark interrupt if time mark = global time *Note: When changing the time mark reference (cycle, local, global time), it is recommended to first write TMC = 00, then reconfigure FDCAN_TTTMK, and finally set FDCAN_TMC to the intended time reference.*
5	RTIE	Register time mark interrupt pulse enable. Register time mark interrupts are configured by register FDCAN_TTTMK. A register time mark interrupt pulse with the length of one fdcan_tq_ck period is generated when time referenced by FDCAN_TTOCN.TMC (cycle, local, or global) equals FDCAN_TTTMK.TM, independent of the synchronization state. 0: Register time mark interrupt output disabled 1: Register time mark interrupt output enabled
4:3	SWS[1:0]	Stop watch source. 00: Stop watch disabled 01: Actual value of cycle time is copied to FDCAN_TTCPT.SWV 10: Actual value of local time is copied to FDCAN_TTCPT.SWV 11: Actual value of global time is copied to FDCAN_TTCPT.SWV
2	SWP	Stop watch polarity. 0: Rising edge trigger 1: Falling edge trigger
1	ECS	External clock synchronization. Writing a 1 to ECS sets FDCAN_TTOST.WECS if the node is the actual time master. ECS is reset after one APB clock period. The external clock synchronization takes effect at the start of the next basic cycle.
0	SGT	Set global time. Writing a 1 to SGT sets FDCAN_TTOST.WGDT if the node is the actual time master. SGT is reset after one APB clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to FDCAN_TTGTP.

41.6.53 FDCAN TT Global Time Preset Register (FDCAN_TTGTP)

Address offset: 0x0118

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Reset value: 0x0000 0000

If TTOST.WGDT is set, the next reference message will be transmitted with the Master_Ref_Mark modified by the preset value and with Disc_Bit = 1, presetting the global time in all nodes simultaneously.

TP is reset to 0x0000 each time a reference message with Disc_Bit = 1 becomes valid or if the node is not the current time master. TP is locked while FDCAN_TTOST.WGTD = 1 after setting FDCAN_TTOCN.SGT until the reference message with Disc_Bit = 1 becomes valid or until the node is no longer the current time master.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CTP[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP[15:0]															
rw															

Bit field	Name	Description
31:16	CTP[15:0]	Cycle time target phase CTP is write-protected while FDCAN_TTOCN.ESCN or FDCAN_TTOST.SPL are set (see Section 41.5.10: Synchronization to external time schedule). 0x0000–FFFF Defines the target value of cycle time when a rising edge of event trigger is expected
15:0	TP[15:0]	Time Preset. TP is write-protected while FDCAN_TTOST.WGTD is set. 0x0000–7FFF next master reference mark = master reference mark + TP 0x8000 reserved 0x8001–FFFF Next master reference mark = master reference mark - (0x10000 - TP).

41.6.54 FDCAN TT Time Mark Register (FDCAN_TTTMK)

Address offset: 0x011C

Reset value: 0x0000 0000

A time mark interrupt (FDCAN_TTIR.TMI = 1) is generated when the time base indicated by FDCAN_TTOCN.TMC (cycle time, local time, or global time) has the same value as TM.

Note: When using byte access to register FDCAN_TTTMK it is recommended to first disable the time mark compare function (FDCAN_TTOCN.TMC = 00) to avoid comparisons on inconsistent register values.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCKM	Reserved								TICC[6:0]						
r									rw						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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TM[15:0]

rw

Bit field	Name	Description
31	LCKM	TT time mark register Locked. Always set by a write access to registers FDCAN_TTOCN. Set by write access to register FDCAN_TTTMK when FDCAN_TTOCN.TMC 00. Reset when the registers have been synchronized into the CAN clock domain. 0: Write access to FDCAN_TTTMK enabled 1: Write access to FDCAN_TTTMK locked
30:23	Reserved	Reserved, the reset value must be maintained.
22:16	TICC[6:0]	Time mark cycle code. Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc
15:0	TM[15:0]	Time mark. 0x0000–FFFF time mark

41.6.55 FDCAN TT Interrupt Register (FDCAN_TTIR)

Address offset: 0x0120

Reset value: 0x0000 0000

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. A flag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CER	AW	WT
													rc_w1	rc_w1	rc_w1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IWTG	ELC	SE2	SE1	TXO	TXU	GTE	GTD	GTW	SWE	TTMI	RTMI	SOG	CSM	SMC	SBC
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

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Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	CER	Configuration error. Trigger out of order. 0: No error found in trigger list 1: Error found in trigger list
17	AW	Application watchdog. 0: Application watchdog served in time 1: Application watchdog not served in time
16	WT	Watch trigger. 0: No missing reference message 1: Missing reference message (level 0: cycle time 0xFF00)
15	IWTG	Initialization watch trigger. The initialization is restarted by resetting IWT. 0 No missing reference message during system startup 1 No system startup due to missing reference message
14	ELC	Error level Changed. Not set when error level changed during initialization. 0: No change in error level 1: Error level changed
13	SE2	Scheduling error 2. 0: No scheduling error 2 1: Scheduling error 2 occurred
12	SE1	Scheduling error 1. 0: No scheduling error 1 1: Scheduling error 1 occurred
11	TXO	Tx count overflow. 0: Number of Tx trigger as expected 1: More Tx trigger than expected in one cycle
10	TXU	Tx count underflow. 0: Number of Tx trigger as expected 1: Less Tx trigger than expected in one cycle
9	GTE	Global time error. Synchronization deviation SD exceeds limit specified by FDCAN_TTOCF.LDSDL, TTCAN level 0, 2 only. 0: Synchronization deviation within limit 1: Synchronization deviation exceeded limit
8	GTD	Global time discontinuity. 0: No discontinuity of global time 1: Discontinuity of global time
7	GTW	Global time wrap 0: No global time wrap occurred

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Bit field	Name	Description
		1: Global time wrap from 0xFFFF to 0x0000 occurred
6	SWE	Stop watch event 0: No rising/falling edge at stop watch trigger pin detected 1 :Rising/falling edge at stop watch trigger pin detected
5	TTMI	Trigger time mark event internal Internal time mark events are configured by trigger memory element TMIN (see Section 41.3.7: trigger memory). Set when the trigger memory element becomes active, and the FDCAN is in synchronization state In_Gap or In_Schedule. 0: Time mark not reached 1: Time mark reached (level 0: cycle time FDCAN_TTOCF.IRTO x 0x200)
4	RTMI	Register time mark interrupt. Set when time referenced by TTOCN.TMC (cycle, local, or global) equals FDCAN_TTTMK.TM, independently from the synchronization state. 0: Time mark not reached 1: Time mark reached
3	SOG	Start of Gap 0: No reference message seen with Next_is_Gap bit set 1: Reference message with Next_is_Gap bit set becomes valid
2	CSM	Change of synchronization mode. 0: No change in master to slave relation or schedule synchronization 1: Master to slave relation or schedule synchronization changed, also set when FDCAN_TTOST.SPL is reset
1	SMC	Start of matrix cycle. 0: No matrix cycle started since bit has been reset 1: Matrix cycle started
0	SBC	Start of basic cycle. 0: No basic cycle started since bit has been reset 1: Basic cycle started

41.6.56 FDCAN TT Interrupt Enable Register (FDCAN_TTIE)

Address offset: 0x0124

Reset value: 0x0000 0000

The settings in the TT interrupt enable register determine which status changes in the TT interrupt register will result in an interrupt.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CERE	AWE	WTE
													rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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IWTE	ELCE	SE2E	SE1E	TXOE	TXUE	GTEE	GTDE	GTWE	SWEE	TTMIE	RTMIE	SOGE	CSME	SMCE	SBCE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	CERE	Configuration error interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
17	AWE	Application watchdog interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
16	WTE	Watch trigger interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
15	IWTE	Initialization watch trigger interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
14	ELCE	Change error level interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
13	SE2E	Scheduling error 2 interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
12	SE1E	Scheduling error 1 interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
11	TXOE	Tx count overflow interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
10	TXUE	Tx count underflow interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
9	GTEE	Global time error interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
8	GTDE	Global time discontinuity interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
7	GTWE	Global time wrap interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled

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Bit field	Name	Description
6	SWEE	Stop watch event interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
5	TTMIE	Trigger time mark event internal interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
4	RTMIE	Register time mark interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
3	SOGE	Start of gap interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
2	CSME	Change of synchronization mode interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
1	SMCE	Start of matrix cycle interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled
0	SBCE	Start of basic cycle interrupt enable 0: TT interrupt disabled 1: TT interrupt enabled

41.6.57 FDCAN TT Interrupt Line Select Register (FDCAN_TTILS)

Address offset: 0x0128

Reset value: 0x0000 0000

The TT interrupt Line select register assigns an interrupt generated by a specific interrupt flag from the TT interrupt register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via FDCAN_ILE.EINT0 and FDCAN_ILE.EINT1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CERL	AWL	WTL
													rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IWTL	ELCL	SE2L	SE1L	TXOL	TXUL	GTEL	GTDL	GTWL	SWEL	TTMIL	RTMIL	SOGL	CSML	SMCL	SBCL
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
18	CERL	Configuration error interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
17	AWL	Application watchdog interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
16	WTL	Watch trigger interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
15	IWTL	Initialization watch trigger interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
14	ELCL	Change error level interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
13	SE2L	Scheduling error 2 interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
12	SE1L	Scheduling error 1 interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
11	TXOL	Tx count overflow interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
10	TXUL	Tx count underflow interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
9	GTEL	Global time error interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
8	GTDL	Global time discontinuity interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
7	GTWL	Global time wrap interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
6	SWEL	Stop watch event interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
5	TTMIL	Trigger time mark event internal interrupt Line 0: TT interrupt assigned to interrupt line 0

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Bit field	Name	Description
		1: TT interrupt assigned to interrupt line 1
4	RTMIL	Register time mark interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
3	SOGL	Start of gap interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
2	CSML	Change of synchronization mode interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
1	SMCL	Start of matrix cycle interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1
0	SBCL	Start of basic cycle interrupt Line 0: TT interrupt assigned to interrupt line 0 1: TT interrupt assigned to interrupt line 1

41.6.58 FDCAN TT Operation Status Register (FDCAN_TTOST)

Address offset: 0x012C

Reset value: 0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPL	WECS	AWE	WFE	GSI	TMP[2:0]			GFI	WGTD	Reserved					
r	r	r	r	r	r			r	r						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTO[7:0]								QCS	QGTP	SYS[1:0]		MSI[1:0]		EL[1:0]	
r								r	r	r		r		r	

Bit field	Name	Description
31	SPL	Schedule phase lock. The bit is valid only when external synchronization is enabled (FDCAN_TTOCN.ESCN = 1). In this case it signals that the difference between cycle time configured by FDCAN_TTGTP.CTP and the cycle time at the rising edge at event trigger pin is less or equal 9 NTU (see Section 41.5.10: Synchronization to external time schedule). 0: Phase outside range 1: Phase inside range
30	WECS	Wait for external clock synchronization. 0: No external clock synchronization pending

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Bit field	Name	Description
		1: Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle.
29	AWE	Application watchdog event. The application watchdog is served by reading FDCAN_TTOST. When the watchdog is not served in time, bit AWE is set, all FDCAN communication is stopped, and the FDCAN is set into bus monitoring mode. 0: Application watchdog served in time 1: Failed to serve application watchdog in time
28	WFE	Wait for event. 0: No Gap announced, reset by a reference message with Next_is_Gap = 0 1: Reference message with Next_is_Gap = 1 received
27	GSI	Gap started Indicator. 0: No Gap in schedule, reset by each reference message and for all time slaves 1: Gap time after basic cycle has started
26:24	TMP[2:0]	Time master priority. 0x0-7 Priority of actual time master
23	GFI	Gap finished Indicator. Set when the CPU writes FDCAN_TTOCN.FGP, or by a time mark interrupt if FDCAN_TTOCN.TMG = 1, or via input pin (event trigger) if FDCAN_TTOCN.GCS = 1. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0: Reset at the end of each reference message 1: Gap finished by FDCAN
22	WGTD	Wait for global time discontinuity. 0: No global time preset pending 1: Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = 1 or after it received a reference message.
21:16	Reserved	Reserved, the reset value must be maintained.
15:8	RTO[7:0]	Reference trigger offset. The reference trigger offset value is a signed integer with a range from -127 (0x81) to 127(0x7F). There is no notification when the lower limit of -127 is reached. In case the FDCAN becomes time master (MS[1:0] = 11), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by FDCAN_TTOCF.IRTO is read. 0x00-FF Actual reference trigger offset value
7	QCS	Quality of clock Speed. Only relevant in TTCAN level 0 and level 2, otherwise fixed to 1. 0: Local clock speed not synchronized to time master clock speed 1: Synchronization deviation ≤ SDL
6	QGTP	Quality of global time phase. Only relevant in TTCAN level 0 and level 2, otherwise fixed to 0.

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Bit field	Name	Description
		0: Global time not valid 1: Global time in phase with time master
5:4	SYS[1:0]	Synchronization state 00: Out of Synchronization 01: Synchronizing to FDCAN communication 10: Schedule suspended by Gap (In_Gap) 11: Synchronized to schedule (In_Schedule)
3:2	MS[1:0]	Master state. 00: Master_Off, no master properties relevant 01: Operating as time Slave 10: Operating as backup time master 11: Operating as current time master
1:0	EL[1:0]	Error level. 00: Severity 0 - No error 01: Severity 1 - Warning 10: Severity 2 - error 11: Severity 3 - Severe error

41.6.59 FDCAN TUR Numerator Actual Register (FDCAN_TURNA)

Address offset: 0x0130

Reset value: 0x0001 0000

There is no drift compensation in TTCAN level 1 (NAV = NC). In TTCAN level 0 and level 2, the drift between the node local clock and the time master local clock is calculated. The drift is compensated when the synchronization deviation (difference between NC and the calculated NAV) is lower than 2 ^(FDCAN_TTOCF.LDSDL + 5). With FDCAN_TTOCF.LDSDL < 7, this results in a maximum range for NAV of (NC - 0x1000) ≤ NAV ≤ (NC + 0x1000).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														NAV[17:16]	
														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAV[15:0]															
r															

Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17:0	NAV[17:0]	Numerator actual value. 0x0EFFF Illegal value 0x0F000–20FFF Actual numerator value

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Bit field	Name	Description
		0x21000 Illegal value

41.6.60 FDCAN TT Local and Global Time Register (FDCAN_TTLGT)

Address offset: 0x0134

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GT[15:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT[15:0]															
r															

Bit field	Name	Description
31:16	GT[15:0]	Global time. Non-fractional part of the sum of the node local time and its local offset (see Section 41.5.5: Local time, cycle time, global time, and external clock synchronization). 0x0000–FFFF Global time value of FDCAN network
15:0	LT[15:0]	Local time. Non-fractional part of local time, incremented once each local NTU (see Section 41.5.5: Local time, cycle time, global time, and external clock synchronization). 0x0000–FFFF Local time value of FDCAN node

41.6.61 FDCAN TT Cycle Time and Count Register (FDCAN_TTCTC)

Address offset: 0x0138

Reset value: 0x003F 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										CC[5:0]					
										r					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT[15:0]															
r															

Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
21:16	CC[5:0]	Cycle count. 0x00–3F Number of actual basic cycle in the system matrix
15:0	CT[15:0]	Cycle time Non-fractional part of the difference of the node local time and Ref_Mark (see Section 41.5.5: Local time, cycle time, global time, and external clock synchronization). 0x0000–FFFF Cycle time value of FDCAN basic cycle

41.6.62 FDCAN TT Capture Time Register (FDCAN_TTCPT)

Address offset: 0x013C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SWV[15:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										CCV[5:0]					
										r					

Bit field	Name	Description
31:16	SWV[15:0]	Stop watch value. On a rising / falling edge (as configured via FDCAN_TTOCN.SWP) at the stop watch trigger pin, when FDCAN_TTOCN.SWS is different from 00 and FDCAN_TTIR.SWE is 0, the actual time value as selected by FDCAN_TTOCN.SWS (cycle, local, global) is copied to SWV and TFDCAN_TIR.SWE will be set to 1.Capturing of the next stop watch value is enabled by resetting FDCAN_TTIR.SWE. 0x0000–FFFF Captured stop watch value
15:6	Reserved	Reserved, the reset value must be maintained.
5:0	CCV[5:0]	Cycle count value Cycle count value captured together with SWV. 0x00–3F Captured cycle count value

41.6.63 FDCAN TT Cycle Sync Mark Register (FDCAN_TTCSM)

Address offset: 0x0140

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSM[15:0]															
r															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CSM[15:0]	Cycle sync mark. The cycle sync mark is measured in cycle time. It is updated when the reference message becomes valid and retains its value until the next reference message becomes valid. 0x0000–FFFF Captured cycle time

41.6.64 FDCAN External Trigger Selection Register (FDCAN_TTSS)

Address offset: 0x144

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						RAMSEL	TS_EN	TS_SEL[2:0]			Reserved	SEVT[1:0]		SSWT[1:0]	
						rw	rw	rw				rw		rw	

Bit Field	Name	Description
31:9	Reserved	Reserved, must be kept at reset value.
9	RAMSEL	Message RAM select: 0: Select SRAM5 BANK1: 0x30050000 as FDCAN base address. 1: Select SRAM5 BANK2: 0x30054000 as FDCAN base address. *Note: When using multiple FDCANs at the same time, selecting SRAM BANK1/2 evenly can improve FDCAN execution efficiency.*
8	TS_EN	External timestamp vector enable 0: Disable external timestamp 1: Enable external timestamp
7:5	TS_SEL[2:0]	Select external timestamp's clock divided 000: Timestamp clock at 4x frequency 001: Timestamp clock at 8x frequency 010: Timestamp clock at 16x frequency 011: Timestamp clock at 32x frequency

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Bit Field	Name	Description
		100: Timestamp clock at 64x frequency 101: Timestamp clock at 128x frequency 110: Timestamp clock at 256x frequency 111: Timestamp clock at 512x frequency
4	Reserved	Reserved, must be kept at reset value.
3:2	SEVT[1:0]	Select EVT 0: select EVT[0] 1: select EVT[1] 2: select EVT[2] 3: select EVT[3]
1:0	SSWT[1:0]	Select SWT 0: select SWT[0] 1: select SWT[1] 2: select SWT[2] 3: select SWT[3]

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42 DSI Host(DSI)

42.1 DSI Introduction

The DSI-2 Controller Core provides a flexible, high-performance, easy-to-use Mobile Industry Processor Interface(MIPI) Display Serial Interface (DSI-2) controller.

42.2 DSI Main Features

The main features supported by DSI-2 are shown below:

- Implements all three DSI-2 Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Support 2048x1536 @30Hz
- Support input data format: RGB888/666/666(loosely)/565
- Support for Command and Video Modes.
- Scalable data lane support, 1 to 4 Data Lanes
  - Bidirectional support on lane 0
- Supports High Speed (2.5 Gbit/s) D-PHY operation
- Virtual Channel support
- Supports ULPS mode
- Supports continuous and non-continuous Clock Lane operation
- Supports multiple packets per transmission
- Support for all three Video mode packet sequences
  - Non-Burst Mode with Sync Pulses.
  - Non-Burst Mode with Sync Events.
  - Burst Mode

42.3 Block Diagram

Figure 42-1 shows MIPI DSI wrapper at top level.

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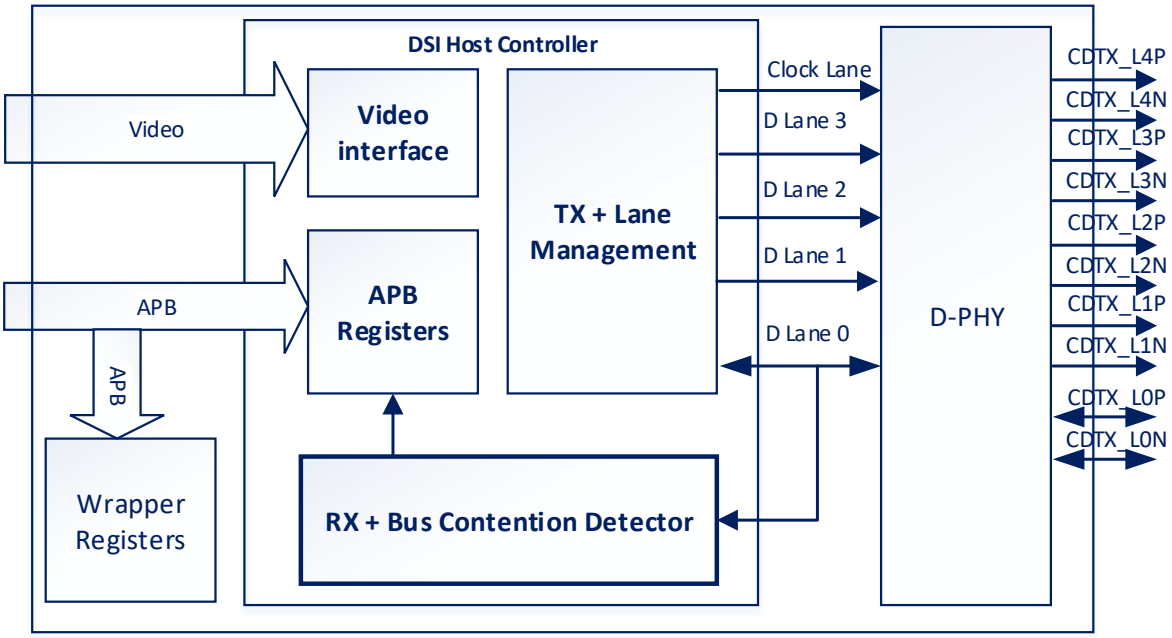
Figure 42-1 MIPI DSI wrapper architecture



DSI Host is deeply integrated with LCDC, DSI Host relies on obtaining pixel data and video synchronization signals from LCDC, and there are two interfaces in DSI Host:

- Video Interface: used for DSI Host to capture real-time pixel data streams and video synchronization signals from LCDC in video mode.
- APB Interface
  - Wrapper Register Interface：provide PHY control related to lane swapping, PLL configuration, reference clock configuration, PHY timing parameter, debug, test, etc. In addition, needed to perform skew calibration as well as interrupt control.
  - APB Register Interface：used to access the DSI Host registers for configuration and control, and to build DCS and generic instruction mode packets using the APB registers

42.4 Work Mode

The MIPI DSI Host controller supports both command mode and video mode (burst mode, non-burst mode with synchronous pulses, non-burst mode using synchronous events).

- Video mode: transmit RGB pixel data generated by LCD and related synchronization signals via high-speed link. The video interface captures the RGB pixel data and synchronization signals output from the LCDC and transmits them to the internal FIFO interface, which then transmits the packets over the DSI link. This continuous refresh is the best way to connect a display with no graphics RAM.
- APB Command Mode: used to send configuration command, using the DSI host APB interface to issue command.

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42.5 DSI-2 Host Video Interface

The LCDC is combined with the DSI to input the stream of pixels output from the LCDC directly to the DSI-2 host controller video interface, which then transmits it to the DSI-2 host controller's internal FIFO interface, which transmits it to the DSI link. The Table 42-1 table shows the mapping of the pixel data output from the LCD to the Video input interface.

Table 42-1 DSI-2 Host Video Interface Input Pixel Format

Data Type	Video input from LCDC																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18-bit RGB565 packet format (0x0E)	RED[4:0]								GREEN[5:0]								BLUE[4:0]							
18-bit RGB666 packet format (0x1E/0x2E)	RED[5:0]								GREEN[5:0]								BLUE[5:0]							
24-bit RGB888 Format (0x3E)	RED[7:0]								GREEN[7:0]								BLUE[7:0]							

Since the LCD output is directly connected to the MIPI DSI Video interface inside the chip, the direct input pixel data format from the LCD is RGB888, if you want to reduce the video bandwidth of the DSI link, you can configure a smaller pixel size as shown in the figure above, but the image quality will be affected.

42.5.1 DSI-2 Host Video Timing

The image data input to the DSI-2 video interface is synchronized using the Horizontal Sync Active (HSA), Horizontal Sync Back Porch (HBP), Horizontal Sync Front Porch (HFP), and Vertical Sync Active (VSA), Vertical Sync Back Porch (VBP), and Vertical Sync Front Porch (VFP). The video interface can be configured with HSA and VSA for positive or negative synchronization. Figure 42-2 shows the sync and spacing (blanking) between sync and active video.

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Figure 42-2 DSI-2 Host Video Interface Raster Timing

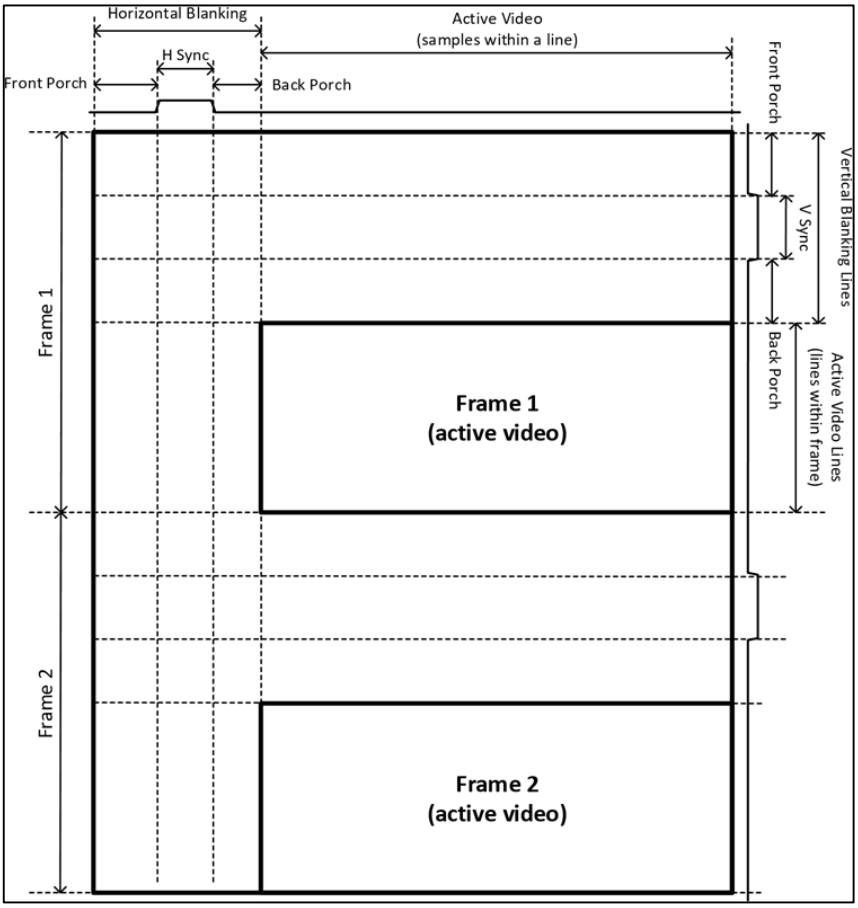

Table 42-2 describes each event that is measured and duplicated on the MIPI interface.

Table 42-2 DSI-2 Host Video Interface Video Events

Mnemonic	Event	Description
HFP	Horizontal Sync Front Porch Time	Time between last active video or vertical sync and the horizontal sync pulse
HSA	Horizontal Sync Active Time	The width of the horizontal sync pulse
HBP	Horizontal Sync Back Porch Time	Time between the falling edge of horizontal sync pulse and the start of active video
HACT	Horizontal Active Video Time	Time between start and end of the active video line
VFP	Vertical Sync Front Porch Time	Number of lines before the rise of the vertical sync pulse
VSA	Vertical Sync Active Time	The width in lines of the vertical sync pulse
VBP	Vertical Sync Back Porch Time	Number of lines between falling vertical sync pulse and the start of lines with active video
VACT	Vertical Active Video Time	Number of active video lines

The timing parameter values of these events in the preceding table can be set automatically or manually on the Video interface.

42.5.1.1 Automatic timing parameters

The DSI Host Controller's Video interface captures the timing parameter values in the first frame of the image output

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from the LCDC to automatically set the timing parameters, and then continuously captures and updates, so that the timing changes between any frames after the first frame are captured by the DSI Host Controller and the timing parameters are automatically updated. In this mode, the timing parameters of the first frame of image data are unknown, so the first frame of image data received by the Video interface is not transmitted to the DSI link. This function can be enabled by clearing the OVERIDE bit in the VID_OVERIDE register.

42.5.1.2 Manual timing parameters

Timing parameters are set by programming the VID_HFP, VID_HBP, VID_HSW, VID_VBP, VID_VFP, VID_VACT registers in the DSI Host controller registers, where the VID_HFP, VID_HBP, and VID_HSA ports define the payload bytes of the video blanking packet, which can be enabled by the OVERIDE bit in the VID_OVERIDE registers, Since the timing parameters have been manually set, the first image received by the video interface will be transmitted to the DSI link, and the timing parameters of each frame will be basically the same.

The horizontal timing parameters are set to reflect the number of DSI-2 packet bytes that HFP, HBP, and HSA need to send, so that the absolute time required for transmission is about the same as the absolute time it takes for a video event to be on the video interface. To correlate HFP, HBP, and HSA on a video interface with DSI-2 packet bytes, use the following relationship:

Time of video event = time to transmit <x number of bytes> on the DSI-2 interface

vid_event_size * vid_clk_period = (number_of_DSI-2_bytes / DSI_NUMLANES) / MIPI line rate in bytes per second

So, number_of_DSI-2_bytes = vid_event_size * vid_clk_period * DSI_NUMLANES * MIPI line rate in bytes per second

where the following definitions apply:

- number_of_DSI-2_bytes = value of [VID_HFP (HBP, or HSA) + any packet headers + packet CRC] bytes involved in video event
- vid_event_size = size of the video event (HFP, HBP, HSA) in video interface clock cycles
- vid_clk_period = period of vid_clk
- MIPI line rate = byte period of the MIPI data lanes in High Speed mode

For example, if approximating the Hsync video event while using the DSI-2 Controller mode Non-burst with Video Pulses, there will be 3 packet headers (Hsync Start, Hsync blanking, and Hsync End), each 4 bytes, and 1 Hsync blanking CRC, 2 bytes. The cfg_vid_hsa value is a count of only the Hsync blanking payload, the cfg_vid_hbp value is a count of only the HBP blanking payload, the cfg_vid_hfp value is a count of only the HFP blanking payload.

There are restrictions on the values used for cfg_vid_hsa, cfg_vid_hbp, and cfg_vid_hfp based on the video resolution of the controller and PHY combination.

- For Non-Burst with Sync Pulse mode, the packet transmission per line of video is {Hsync Start, Hsync blanking, Hsync End, HBP, Video Data, HFP}.
- For Non-Burst with Sync Event mode, the packet transmission per line of video is {Hsync Start, HBP, Video Data, HFP}.
- For Burst mode, the packet transmission per line of video is {Hsync Start, HBP, Video Data, Blanking/Low

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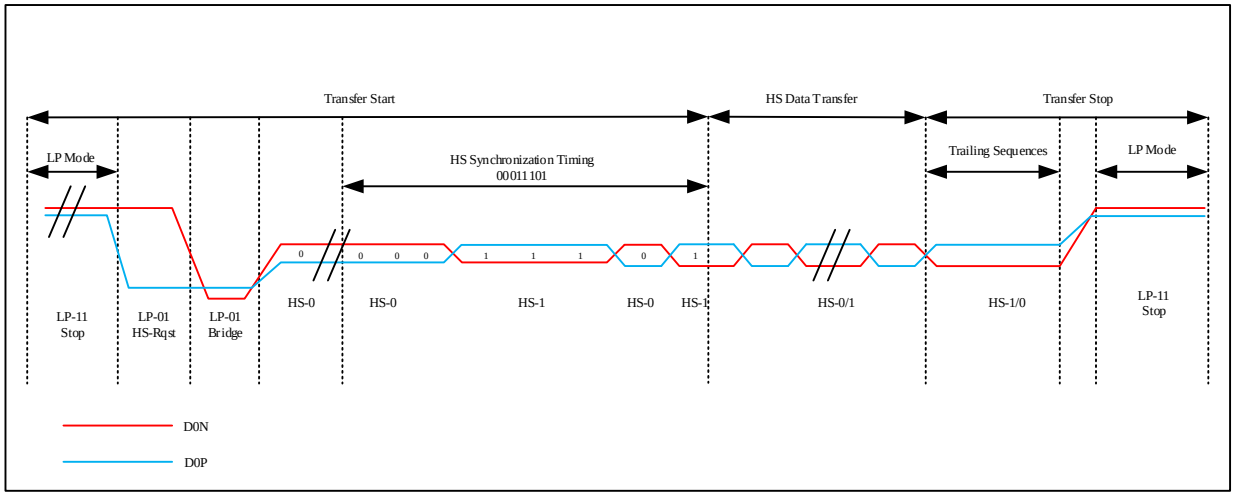
Power, HFP}.

The high-speed transmission begins and ends in a stopped state (LP-11). In order to synchronize between the host and the display, a header and tail label sequence needs to be added. On the receiver side, they are removed because they do not belong to the actual payload data. The specific process is as follows and see Figure 42-3:

1. SoT: when an HS request (LP-11, LP-01, LP-00) is received, the data channel enters HS mode. The host first drives the header sequence (HS-0) and then the HS synchronization sequence Sync Symbol Sequence (SSS:00011101) to allow the device to synchronize, and then the host continues to transmit HS data
2. EoT: after the HS data transfer is complete, the host sends a tailmark sequence (the tailmark sequence is the opposite of the last data bit transmitted: if the most payload bit is HS-0, then the transmitter sends HS-1 as the tailmark sequence, otherwise HS-0 is sent). The data channel returns to control mode via the stop state LP-11

Figure 42-3 DSI-2 Host Video Interface Raster Timing



The Sync Symbol Sequence (SSS) in the figure above is a key part of data channel synchronization and timing management, especially when switching from LP (Low-Power) mode to HS (High-Speed) mode. The Sync Symbol Sequence is sent before HS transmission, which is mainly used to help the receiver lock the HS clock to achieve clock synchronization and multi-data channel timing alignment. SSS is a synchronization symbol sequence of the MIPI DSI physical layer, which is used to maintain channel synchronization and anti-interference. They are not directly controlled by the application layer, but are automatically inserted by the physical layer after the packet is assembled:

- Short packet: insert SSS between Packet Header 1 and Header 2
- Long Packet: insert SSS between Packet Header 1 and Header 2, and insert SSS again after Header 2

Although SSS is not directly involved in packet length calculation, they will occupy the actual transmission time, so they need to be subtracted from the timing parameters (HSA/HBP/HFP), if the SSS time is not subtracted, the actual HSA/HBP/HFP duration will be longer than expected, which may cause the screen to display abnormally. Therefore number_of_DSI-2_bytes calculation formula is adjusted to:

number_of_DSI-2_bytes = (vid_event_size * vid_clk_period - <sets of SSS * 2 bytes/MIPI line rate in bytes per second>) * DSI_NUMLANES * MIPI line rate in bytes per second

The specific adjustments are as follows:

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1. Calculate the total number of SSS bytes (number of inserts based on packet type)
2. Calculate the time required to transmit SSS based on the MIPI rate (Lane Rate).

   SSS_time = (SSS_bytes x 8) / Lane_Rate
3. Subtract SSS_time from the HAS/HBP/HFP timing

Eg: transmits long packets, inserts 2-byte SSS between Header 1 and Header 2, inserts 2-byte SSS after Header 2, a total of 4-byte SSS, MIPI rate: 1 Gbps/lane (i.e., 1 bit per nanosecond), SSS time is 32ns, if HSA is designed to be 100ns, you need to adjust HAS to 100-32=68ns.

42.5.2 Video Mode

The following video modes are supported by the DSI Host controller:

- Burst mode
- Non-burst mode
  - Non-burst mode with sync pulse
  - Non-burst mode with sync event

In the time between each horizontal event (horizontal sync width and time between sync and active video), the DSI-2 protocol supports either sending a blanking packet or returning the MIPI interface to LP mode for power savings and allowing other non-video packets to be sent. For lines that do not contain active video, the HBP, HACT, and HFP are combined into what is called BLLP (Blanking or LP). The following combinations of blanking and LP are supported by which video mode (VID_VIDEOMOD) and the setting of the BLLP mode (VID_BLLPMOD), see Table 42-3.

Table 42-3 Blanking packet combination

<table>
<tr><th rowspan="2">VID_VIDEOMOD</th><th rowspan="2">VID_BLLPMOD</th><th rowspan="2">Active Video Line</th><th rowspan="2">HSA</th><th>HBP</th><th>HACT</th><th>HFP</th></tr>
<tr><th colspan="3">BLLP (HBP+HACT+HFP)</th></tr>
<tr><td rowspan="4">SYNC_PULSE</td><td rowspan="2">0</td><td>NO</td><td rowspan="4">BLANK</td><td colspan="3">Blank</td></tr>
<tr><td>YES</td><td>BLANK</td><td>VIDEO</td><td>BLANK</td></tr>
<tr><td rowspan="2">1</td><td>NO</td><td colspan="3">LP</td></tr>
<tr><td>YES</td><td>BLANK</td><td>VIDEO</td><td>BLANK</td></tr>
<tr><td rowspan="4">SYNC_EVENT</td><td rowspan="2">0</td><td>NO</td><td rowspan="4">No HSA in mode</td><td colspan="3">BLANK</td></tr>
<tr><td>YES</td><td>BLANK</td><td>VIDEO</td><td>BLANK</td></tr>
<tr><td rowspan="2">1</td><td>NO</td><td colspan="3">LP</td></tr>
<tr><td>YES</td><td>BLANK</td><td>VIDEO</td><td>BLANK</td></tr>
<tr><td rowspan="2">BURST_MODE</td><td rowspan="2">0</td><td>NO</td><td rowspan="2">No HSA in mode</td><td colspan="3">BLANK</td></tr>
<tr><td>YES</td><td>BLANK</td><td>VIDEO</td><td>BLANK</td></tr>
</table>

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	1	NO		LP		
		YES		BLANK	VIDEO	LP

For the last line of video in a frame, the BLLP will always be LP. The DSI-2 spec allows a blanking packet before an LP transition on the last line, but the DSI-2 Host Controller does not issue it to allow more time for other non-video packet transmission during the LP period.

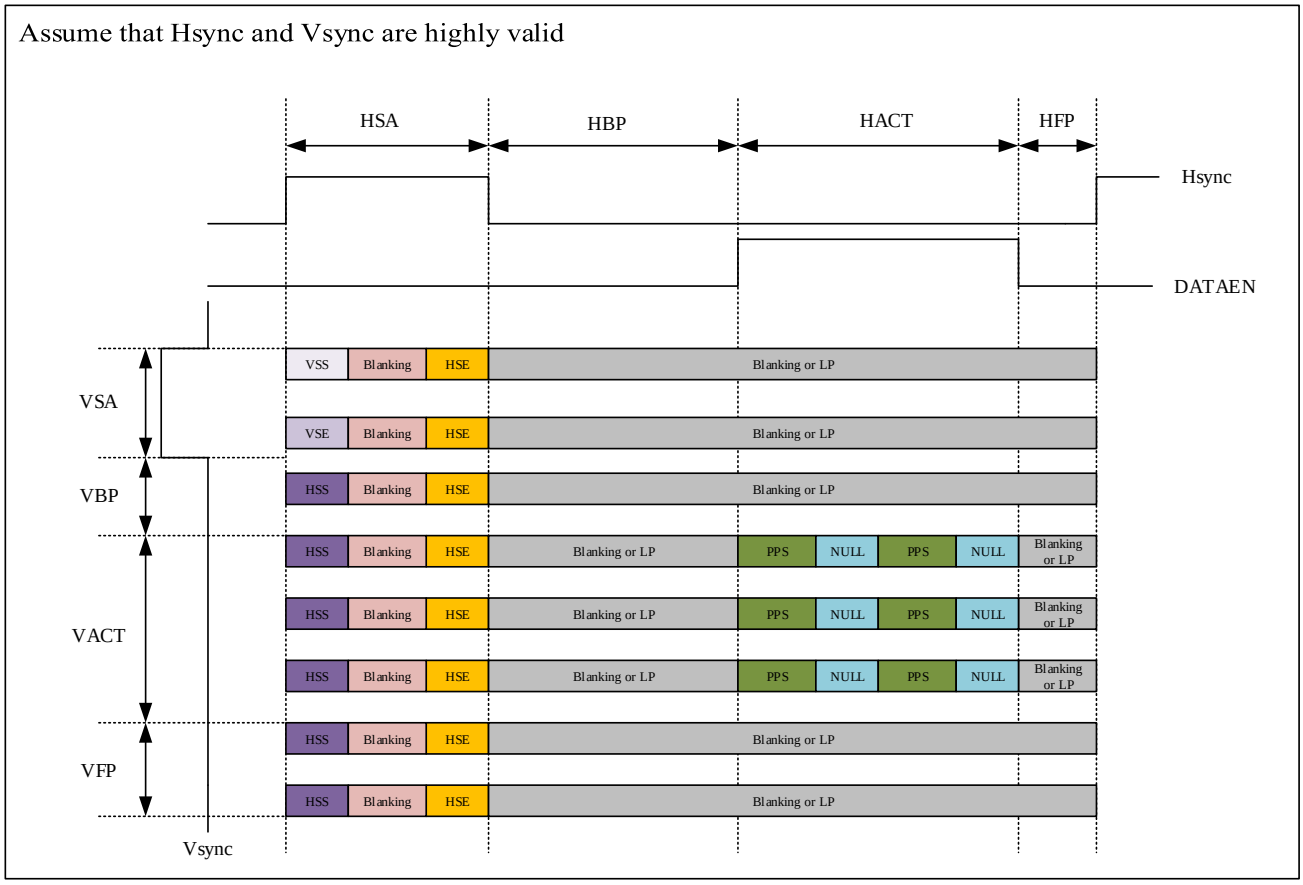
42.5.2.1 Non-burst mode

In this mode, the processor uses the partition properties of the DSI host to divide the video line transmission into multiple DSI packets, so the DSI Host controller does not need to store the entire pixel line data in the video interface FIFO, only one video packet of data. Since the DSI link is not allowed to enter the low-power mode throughout the active video line cycle, the LCDC output pixel bandwidth needs to be closely matched to the DSI link bandwidth.

Non-burst mode with sync pulse

Non-burst mode with sync pulse enables the peripherals to precisely reconstruct the original video timing, including the sync pulse width. The frame timing diagram for non-burst mode using synchronous pulses is shown Figure 42-4.

Figure 42-4 Non-burst mode with sync pulse frame



The HSA (Hsync Activation) cycle consists of HSS (Hsync Start), Blanking, and HSE (Hsync End) packets. Packets in this area are transmitted in high-speed mode, and the link does not enter the LP during the HSA cycle. The DSI host automatically calculates the size of the blanking packet required to match the timing HSA cycles between HSS

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and HSE packets.

When the DSI host detects a Vsync rising edge, the DSI host sends a VSS packet instead of the HSS packet to initiate the HSA cycle. When a Vsync falling edge is detected, the DSI host sends a VSE packet instead of an HSS packet marking the end of the VSA cycle. Other lines within the VSA region start with HSS packets. Outside of the VACT cycle, the link enters LP mode after the HSA cycle until the end of the horizontal line.

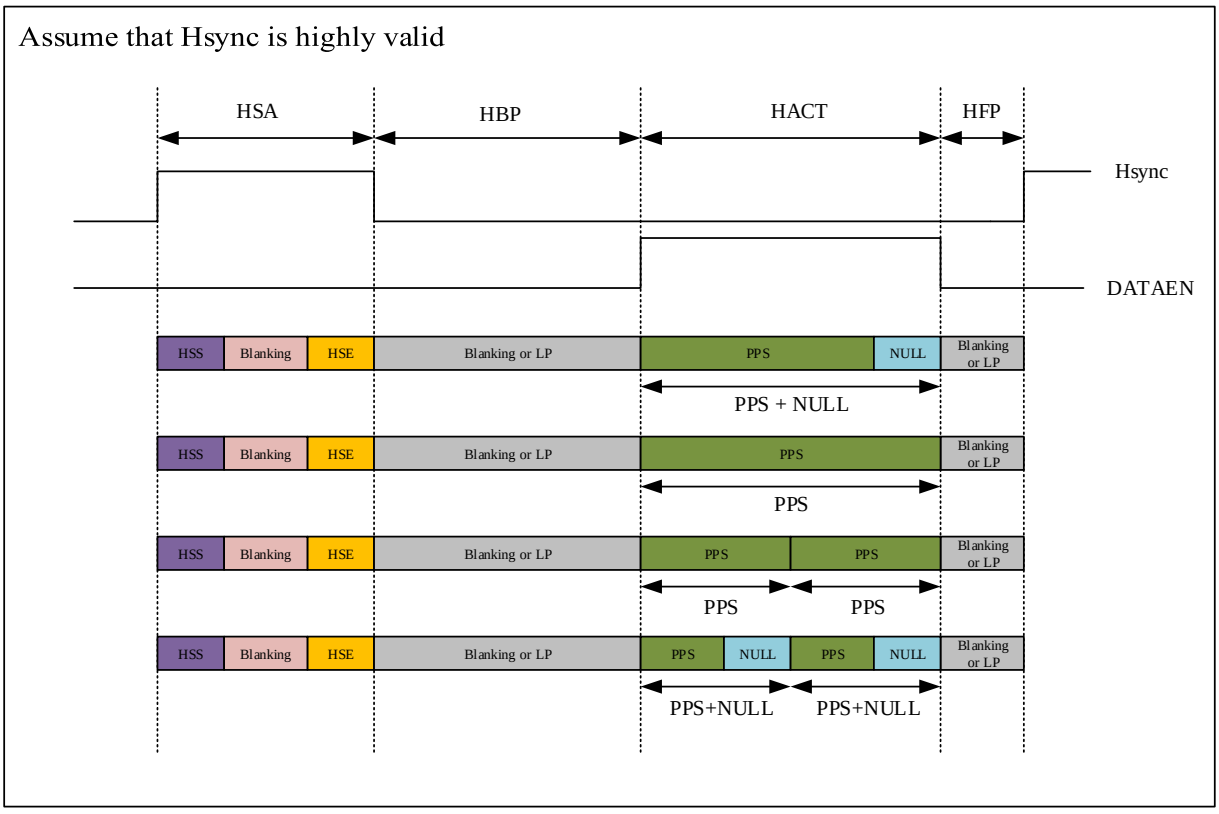
Within the VACT region, the DSI host transmits HSA cycles, and then the link enters the LP or sends blanking packets, with a continuous timing period equal to the HBP cycle. The DSI host then sends PPS packets in one or more blocks, and the last NULL packet is used to match the pixel transmission timing to the HACT cycle.

Once the HACT cycle ends, the DSI host enters the LP or sends a blanking packet for a duration equal to the HFP cycle.

The DSI host is able to calculate the number of bytes required to blank a packet in order to match the periodic timing. In the case of low-power mode, the DSI PHY will emit an end-of-transmission sequence before entering low-power mode. Then, before starting a new high-speed transmission, the DSI PHY emits a transmission start sequence. The DSI Host controller needs to be configured with registers such as DSI_TPRE, DSI_TPOST, and DSI_TXGAP for the DSI Host controller to understand the overhead of low-power conversion to determine whether it can switch to low-power mode within a specific cycle.

In non-burst mode with sync pulse, there are many different horizontal row configurations during the VACT cycle. As shown Figure 42-5:

Figure 42-5 VACT region of non-burst mode with sync pulse



The link can enter the LP during the HBP and HFP cycles, or send blanking packet when the DSI host does not have

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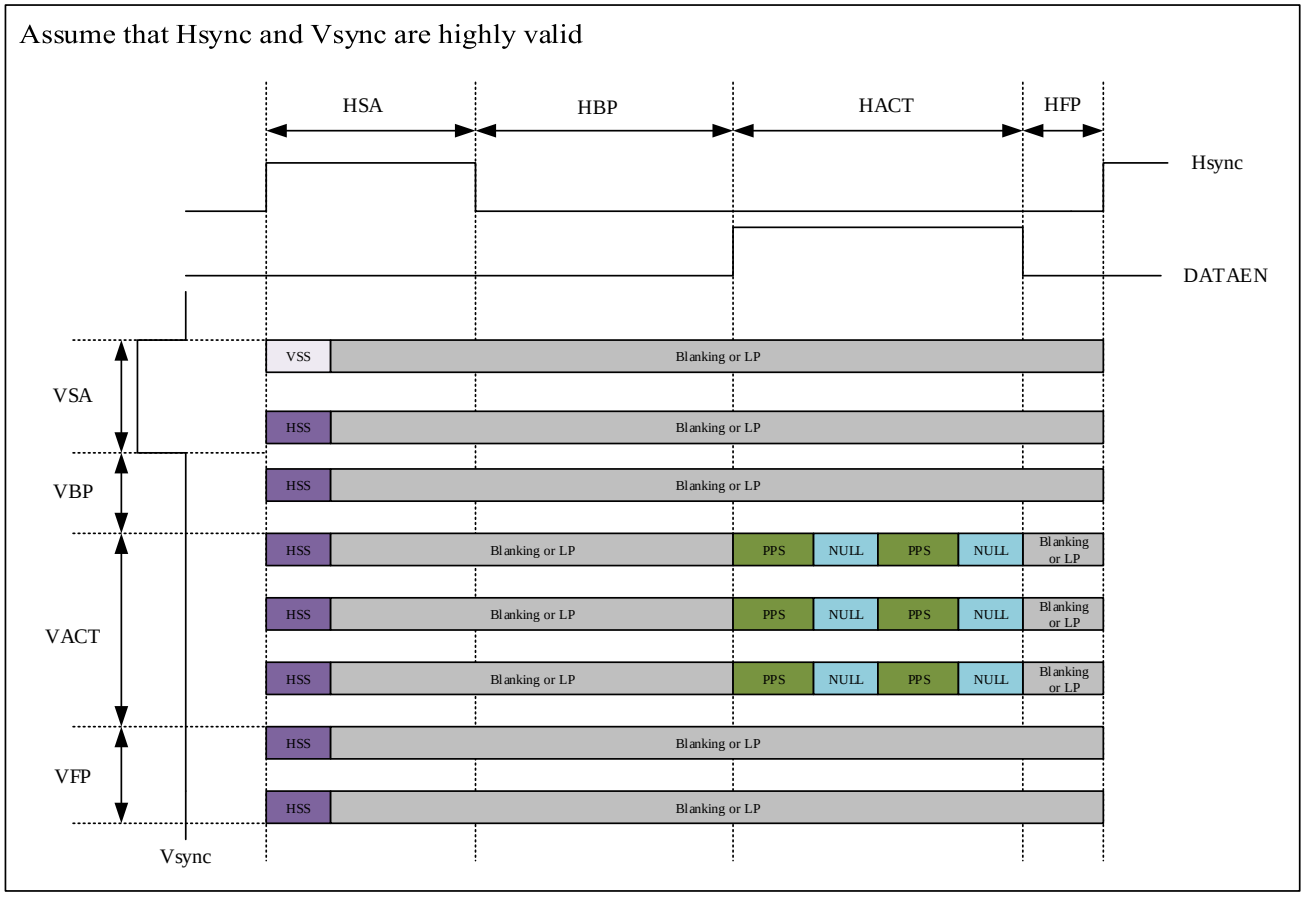
enough time to transition between HS and LP modes during that cycle. During the HACT cycle, the DSI host must send pixel data within a time series cycle that matches the LCDC HACT cycle. Depending on the DSI and pixel clock frequency, the DSI host can send pixel data using one or more blocks. Each block can contain only one Encapsulated Stream of Pixels (PPS) packet or PPS packet with NULL packets.

Non-burst mode with sync event

In this mode, there is no need for an exact reconstruction of the synchronization pulse width, thus replacing a single synchronization event. As shown Figure 42-6.

Figure 42-6 Non-burst mode with sync event frame



The line that begins with the VSS packet determines the beginning of the VSA zone. All other lines in the frame begin with an HSS packet.

In the inactive zone (VSA, VBP, VFP), the link goes into the LP or sends blanking packets after sending HSS packets up to the next line. In the VACT zone, the DSI host sends HSS packets and then enters the LP or sends blanking packets until the end of the HSA HBP cycle. The HACT region DSI host must send pixel data within a time series cycle that matches the LCDC HACT cycle. Depending on the DSI and pixel clock frequency, the DSI host can send pixel data using one or more blocks. Each block can contain only one Encapsulated Stream of Pixels (PPS) packet or PPS packet with NULL packets.

In Non-burst mode with sync event, there are many different horizontal line configurations during the VACT cycle. As shown Figure 42-7:

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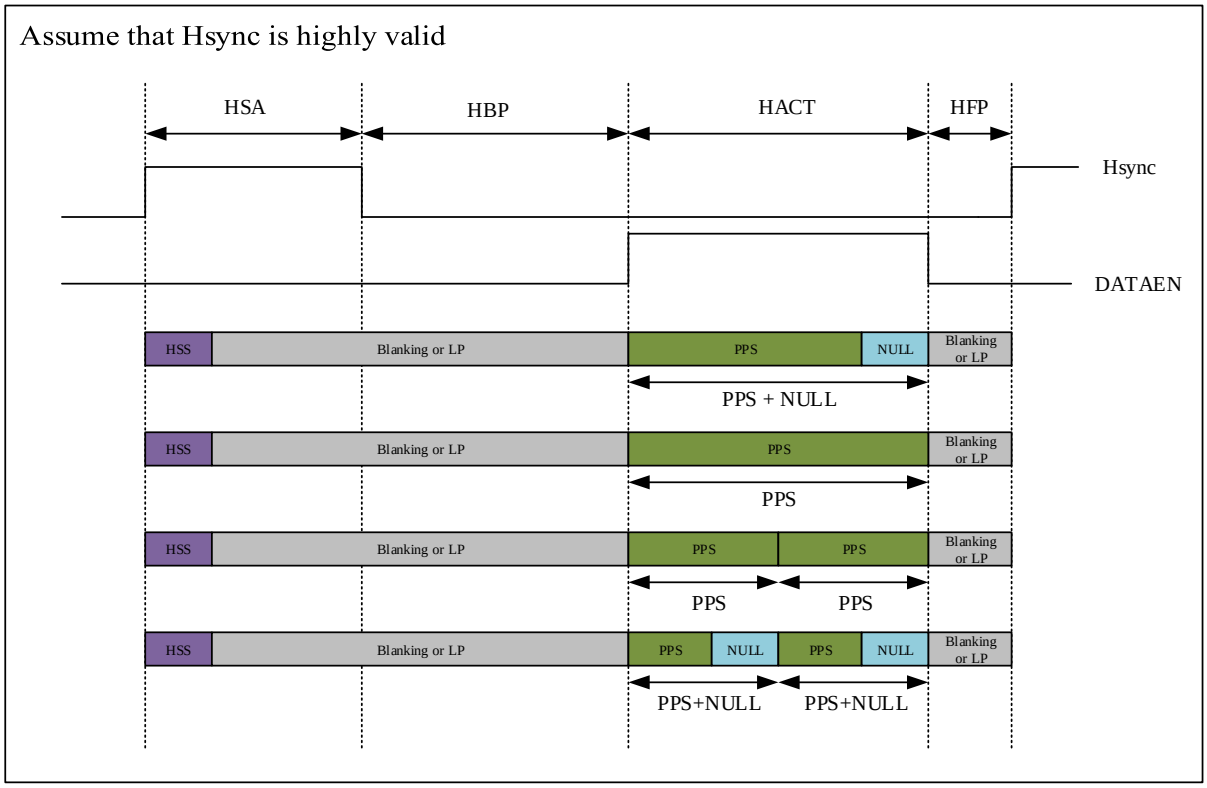
Figure 42-7 VACT region of non-burst mode with event pulse



42.5.2.2 Burst mode

In this mode, the entire line of effective pixels is buffered into the FIFO and transmitted non-interrupted as a single packet. This mode of transport requires the DPI pixel FIFO to be able to store an entire active pixel line data. This mode is best used when there is a large difference between the bandwidth required by the pixel and the bandwidth of the DSI link, which enables the DSI host to quickly send the entire active video line out in a single burst of data, and then return to low-power mode to bring the link to a halt. As shown Figure 42-8.

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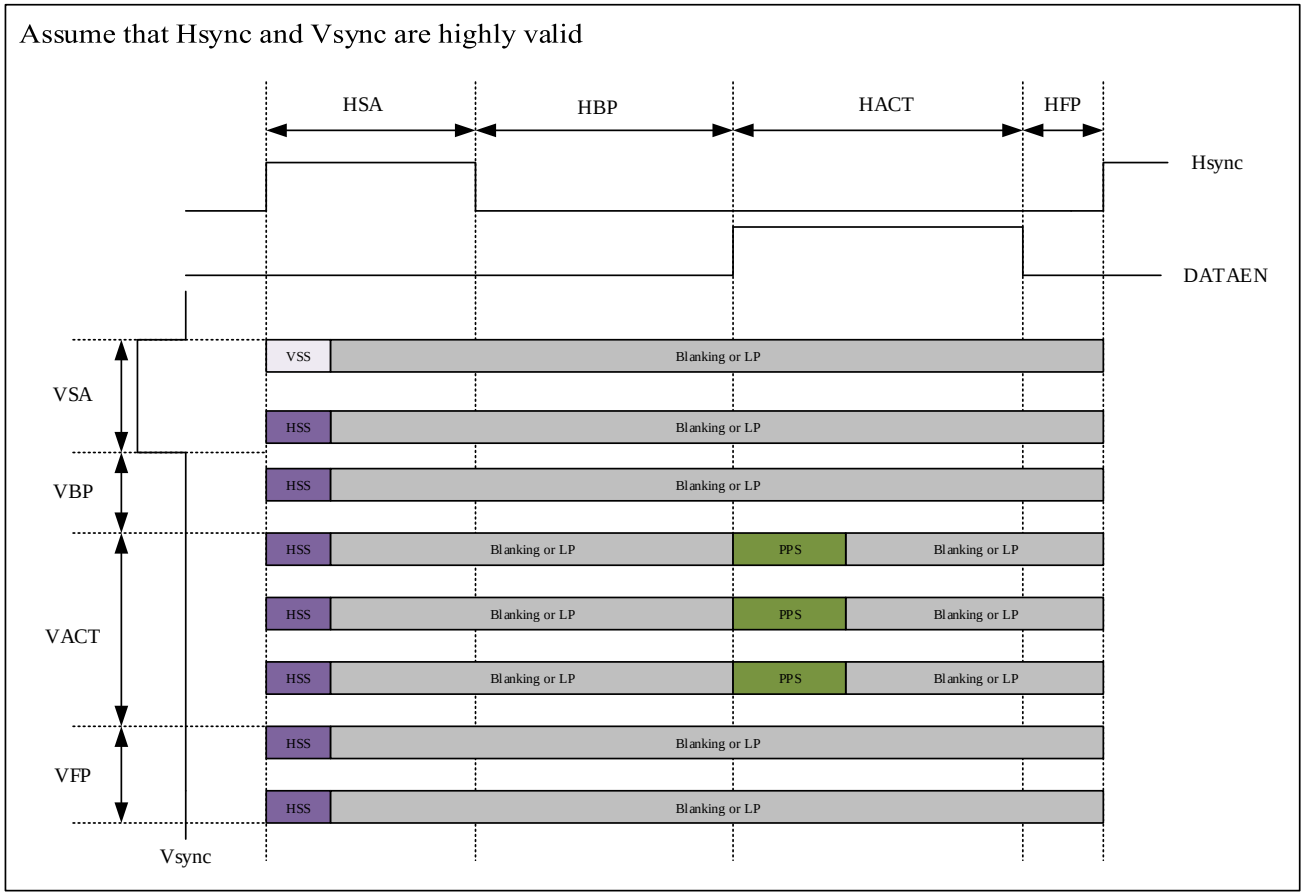
Figure 42-8 Burst mode frame



The guide to choosing a burst or non-burst mode

The choice of burst and non-burst mode depends primarily on system configuration and device requirements. The following conditions must be met to get the most advantage from burst mode:

- The DSI Host Core must have enough pixel memory to store the entire pixels line to avoid internal FIFO overflow
- The display device must support receiving the entire pixels line in a single packet burst to avoid overflow on the receive buffer
- The DSI output bandwidth must be higher than the video interface input bandwidth to achieve low power consumption once per line of the link

If the system does not meet these requirements, it is likely that pixel data will be lost when using burst mode, resulting in display device failure. If you can't meet all the criteria for using burst mode, use non-burst mode to avoid errors, non-burst mode can better match the pixel transfer rate, resulting in:

- Only a certain number of pixels are stored in memory, and a full pixels line is not required
- Runs with devices that only support a small amount of pixel buffer (smaller than a full pixel line).

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42.5.3 Timing Reconstruction Differences

The DSI-2 Host Video Interface preserves video timing by properly spacing the DSI-2 packets that carry the video information or by inserting blanking packets into the packet stream. Since the video interface is usually running at a different clock rate than the DSI-2 Host Controller MIPI clock rate, the video timing recreation will be an approximation of the video input converted to the MIPI rate and clock domain so it will not be a perfect recreation. Depending upon the clock ratio between video clock domain and MIPI clock domain, blanking widths can vary each line as horizontal sync events are sampled through a synchronizer and may be closer to one clock edge or another. The horizontal front porch width is also lengthened or shortened to compensate for cases were the video line takes less or more time to transmit the video data.

The larger the ratio between a faster video clock and a slower MIPI clock, the more inaccurate the horizontal sync and blank timing will be since the horizontal sync events and the blanking around them are measured in MIPI clock cycles. The sync and blank timings can easily be off a few cycles. The DSI-2 Host Video Interface will continuing adjust the sync and blank time to compensate for this and to prevent cases where the video timings drift over time and eventually overflow the FIFO. The larger the horizontal sync and blanking widths are in the incoming video, the more accurate the video interface. For example, a variance of a few cycles for a 5 cycle horizontal sync width is more significant than a few cycle variance of a 50 cycle horizontal sync width.

One additional source of video variance is the video clock to MIPI clock synchronizers. Since a synchronizer can become metastable depending on how close the change in data is to the clock edge, this can cause a cycle delay before a horizontal sync or video edge is detected. Also because of the synchronizers, the width of horizontal sync and width of the blanking must be wide enough so at the faster video clock domain they don’t change state multiple times in a single slower MIPI clock.

42.6 DSI-2 Host APB Interface

The DSI-2 Host Controller support DSI-2 packet transmission and reception through the APB interface. The APB packet interface is intended for low data rate applications, like setting configuration register values and checking status in a display device.

APB packet Interface key features include:

- Supports all data types, long and short
- Transmit, Bus Turn Around, and Receive
- High Speed or Low power packet transmission
- Interrupt driven (mask able) transactions or software polling

42.6.1 Transmit a packet using APB interface

DSI support to transmit a packet to DPHY via the APB interface by writing to the register set follow the flow as below.

- **To transmit a packet using the APB Packet Interface you must perform the following steps:**

1. Write the write command type value to the register DSI_PKTCTRL. HDTYP[5:0]

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2. If it is a short-write command, write the command parameters to DSI_PKTCTRL. CNT[15:0]； If it is a long-write command, write the length of the command parameter to DSI_PKTCTRL. CNT[15:0] and then write the command parameters to the DSI_TXPLD register to load the command parameters into the command FIFO
3. Set up DSI_SENDPKT. SENDPKT=1 enables data transmission
4. Wait for DSI_PKTSTS. TXD is set to confirm that the transmission is complete

■ **To perform a read operation from a DSI-2 peripheral, the following steps must be performed:**

1. Write the read command type value to the register DSI_PKTCTRL. HDTYP[5:0] and setting DSI_PKTCTRL. BTAIMM=1 instructs the APB packet interface to perform bus steering after sending the packet so that the peripheral gains control and sends the packet back to the host
2. If it is a short-read command, write the command parameters to the DSI_PKTCTRL. CNT[15:0]； If it is a long-read command, write the length of the command parameter to DSI_PKTCTRL. CNT[15:0] and then write the command parameters to the DSI_TXPLD register to load the command parameters into the command FIFO
3. Set up DSI_SENDPKT. SENDPKT=1 enables data transmission
4. Wait for DSI_PKTSTS. TXD is set to confirm that the transmission is complete
5. Wait for DSI_PKTSTS. RXPKTD and DSI_PKTSTS. The ALLRXPKTD is set, the DSI peripheral returns the data, and after the peripheral returns the data, it automatically performs the bus steering, returning control to the host

42.7 DSI Host Core Timing

The DSI-2 Host Controller supports both a Continuous Clock and a Non-Continuous Clock Mode. In Continuous Clock Mode, the D-PHY clock lane is always enabled and does not stop between packets. In Non-Continuous Clock Mode, the D-PHY clock lane is turned off when a packet is not being sent.

42.7.1 Continuous Clock Mode

For the operation mode of continuous clock, its clock channel maintains high-speed mode and generates a valid clock signal between HS packet transmissions. Continuous clock mode allows for higher data rates because the timing overhead of HS mode for exiting and re-entering clock channels is eliminated.

Figure 42-9 shows each timing parameter for continuous clock mode. This wave form is compressed for clarity and is not intended for cycle counting but only for order of parameters and their dependent signal transitions lists each timing parameter and value. The transition of each signal is given as ↑ for rising edge or ↓ for falling edge. Timing values are given in terms of main byte clock cycles (clk primary input). Some timing parameters are specific to a vendor’s PHY and what frequency the PHY is running at. For illustrative purposes, a typical number of cycles is given after each PHY specific timing value. These typical PHY specific counts should not be used for bandwidth analysis since PHYs may vary significantly from these values.

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Figure 42-9 DSI-2 Host Timing for Continuous Clock Mode

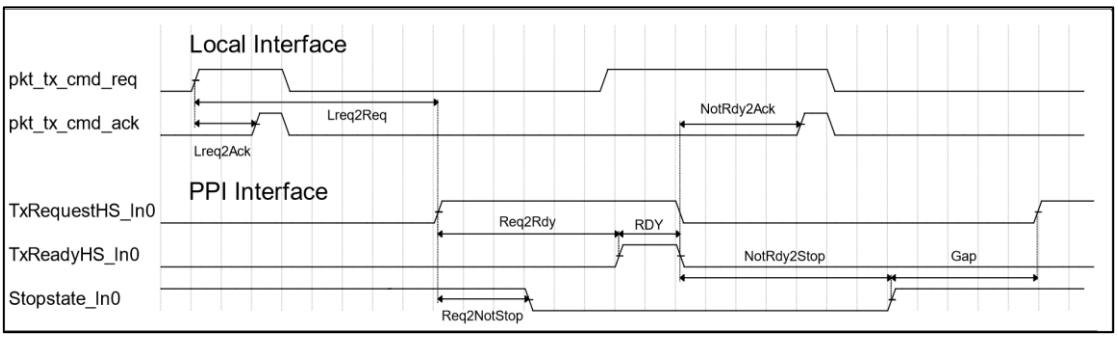

Table 42-4 DSI-2 Host Controller Core Timing for Continuous Clock Mode

Timing Parameter	Start	End	Value	Comment
Lreq2Req	↑ pkt_tx_cmd_req	↑ TxRequestHS_ln0	7 min (short pkt) 9 min(long pkt) +DSI_TPRE for first cycle	Some data types may take an extra cycle or two for processing.
Lreq2Ack	↑ pkt_tx_cmd_req	↑ pkt_tx_cmd_ack	2 cycle min	A cycle is taken to determine if valid data type
Req2Rdy	↑ TxRequestHS_ln0	↑ TxReadyHS_ln0	Phy Specific (40)	
Req2NotStop	↑ TxRequestHS_ln0	↓ Stopstate_ln0	Phy Specific (12)	Does not affect controller
RDY	↑ TxReadyHS_ln0	↓ TxReadyHS_ln0	1 cycle min	Width of RDY is: # packet bytes / # lanes
NotRdy2Stop	↓ TxReadyHS_ln0	↑ Stopstate_ln0	Phy Specific (18)	
NotRdy2Ack	↓ TxReadyHS_ln0	↑ pkt_tx_cmd_ack	3 cycles	If pkt_tx_cmd_req is asserted
Gap	↑ Stopstate_ln0	↑ TxRequestHS_ln0	DSI_TXGAP + 4	Gap until the next data request.

The first packet to be sent after a reset is a special case in Continuous Clock Mode. The DSI_TPRE value is used to add additional delay to give the PHY additional time between clock being enabled and the first packet.

42.7.2 Non-Continuous Clock Mode

For the operation mode of discontinuous clocks, the clock channel enters the LP-11 state between HS packet transmissions.

Figure 42-10 shows each timing parameter for non-continuous clock mode. This wave form is compressed for clarity and is not intended for cycle counting but only for order of parameters and their dependent signal transitions

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Figure 42-10 DSI-2 Host Timing for Non-Continuous Clock Mode

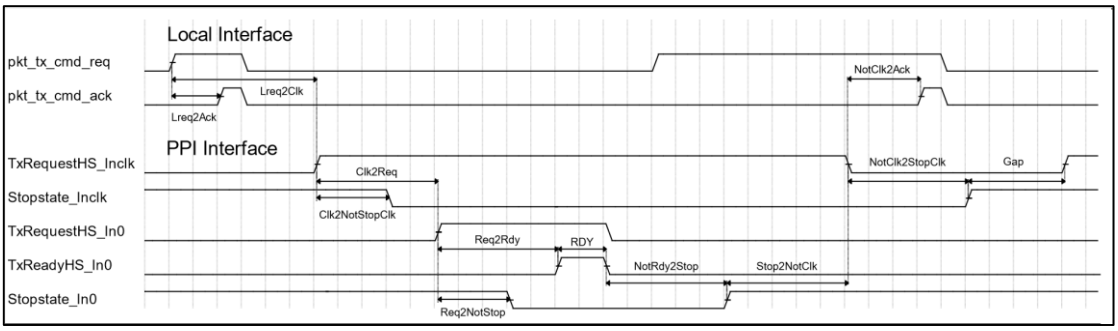

Table 42-5 lists each timing parameter and value. The transition of each signal is given as ↑ for rising edge or ↓ for falling edge. Timing values are given in terms of main byte clock cycles (clk primary input). Some timing parameters are specific to a vendor's PHY and what frequency the PHY is running at. For illustrative purposes, a typical number of cycles is given after each PHY specific timing value. These typical PHY specific counts should not be used for bandwidth analysis since PHYs may vary significantly from these values.

Table 42-5 DSI-2 Host Controller Core Timing for Non-Continuous Clock Mode

Timing Parameter	Start	End	Value	Comment
Lreq2Clk	↑ pkt_tx_cmd_req	↑ TxRequestHS_lnclk	7 min (short pkt) 9 min(long pkt)	Some packet types may take extra cycles for processing.
Lreq2Ack	↑ pkt_tx_cmd_req	↑ pkt_tx_cmd_ack	2 cycle min	A cycle is taken to determine if valid data type
Clk2Req	↑ TxRequestHS_lnclk	↑ TxRequestHS_ln0	DSI_TPRE	
Clk2NotStopClk	↑ TxRequestHS_lnclk	↓ Stopstate_lnclk	Phy Specific (12)	Does not affect controller
Req2Rdy	↑ TxRequestHS_ln0	↑ TxReadyHS_ln0	Phy Specific (40)	
Req2NotStop	↑ TxRequestHS_ln0	↓ Stopstate_ln0	Phy Specific (15)	Does not affect controller
RDY	↑ TxReadyHS_ln0	↓ TxReadyHS_ln0	1 cycle min	
NotRdy2Stop	↓ TxReadyHS_ln0	↑ Stopstate_ln0	Phy Specific (18)	
Stop2NotClk	↑ Stopstate_ln0	↓ TxRequestHS_lnclk	DSI_TPOST + 3	
NotClk2Ack	↓ TxRequestHS_lnclk	↑ pkt_tx_cmd_ack	3 cycles	If pkt_tx_cmd_req is asserted
NotClk2StopClk	↓ TxRequestHS_lnclk	↑ Stopstate_lnclk	Phy Specific (17)	
Gap	↑ Stopstate_lnclk	↑ TxRequestHS_lnclk	DSI_TXGAP + 4	Gap until the next clock request.

42.8 Skew Calibration

Skew Calibration, described in the MIPI DSI protocol, is a timing compensation mechanism for the D-PHY physical

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Email: sales@nsing.com.sg

layer at high speed (>1.5 Gbps), and its purpose is to solve the signal skew problem between multiple data lanes. Skew Calibration is usually done by a combination of DSI Host (TX) and Display Panel (RX), so it must be supported by the display to be used. In the MIPI DSI protocol, the timing of Skew Calibration's triggering is usually related to link initialization, state recovery, or specific signal conditions. Skew Calibration is typically performed in the following situations:

- Link Initialization Phase: When the DSI master or slave powers up or receives a hardware/software reset signal, Skew Calibration is performed to eliminate the timing skew between the CLK Lane and the Data Lane
- Low-Power Mode Wake-up: When switching from LP mode to HS mode, the timing shift may be caused by voltage/temperature changes, and recalibration is required

Skew Calibration Type:

- Initial Skew Calibration：before high-speed data transmission begins, it is initiated by the host by sending a special de-skew burst signal. It must be performed before each high-speed data transfer is started when the DSI link rate is >1.5 Gbps, and optional when the DSI link rate ≤ 1.5 Gbps
- Periodic Skew Calibration：it is dynamically initiated by the host during the high-speed data transmission gap, regardless of the link rate, and is used to dynamically adjust the timing drift caused by changes in temperature and voltage
- Alternate Calibration：an additional calibration mechanism for high-speed data transmission (>2.5 Gbps) to optimize signal integrity. When the data transfer rate is >2.5 Gbps, an Alternate Calibration must be performed after the Initial Skew Calibration; When the rate is ≤2.5 Gbps, Alternate Calibration is optional

As part of the MIPI specification for D-PHYs operating over 1.5 Gbps, the DSI-2 Host PHY is required to support skew calibration by the sending of special de-skew bursts to the receiver to initiate a de-skew operation in the receiver to calibrate the receiver. There is the initial skew calibration sequence which is transmitted before High Speed Data Transmission begins and a periodic skew calibration that can happen in-between high speed packets. For operations over 1.5 Gbps, the initial skew calibration is required. For 1.5 Gbps or below, the initial skew calibration is optional. Periodic skew calibration is always optional. When changing states (ULPS to HS, for example), skew calibration is optional as long as high speed operation resumes at a rate for which an initial skew calibration had previously been transmitted.

The skew calibration sequence is handled by DSI-2 Host D-PHY with the DSI-2 Host Core only enabling the clock lane (if not in continuous clock mode) and asserting the PPI TXSkewCalHS signal a specified number of clk cycles (set by a controller configuration signal). The DSI-2 Host D-PHY will start the skew calibration sequence when TXSkewCalHS is observed and will stop the skew calibration sequence when TXSkewCalHS is de-asserted.

For operations over 2.5 Gbps, an alternate calibration sequence is required following an initial skew calibration. For 2.5 Gbps or below, the alternate calibration is optional. With PHYs supporting the alternate calibration feature, the DSI-2 Host asserts TxAlternateCalHS_lnX following the initial skew calibration to start the alternate calibration sequence. The alternate calibration sequence stops when the DSI-2 Host de-asserts TxAlternateCalHS_lnX. The length of the alternate calibration sequence is determined by the DSI_ALTCALTIM input value.

Figure 42-11 shows an example of an initial skew calibration operation for lane 0. Skew calibration is always asserted for all lanes at the same time, but only lane 0 is shown in the diagram for clarity. User logic asserts the TX Core user interface skewcal_i signal which results in the controller asserting TxRequestHS_lnclk to enable the D-PHY clock

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lane. The PHY will respond with the de-assertion of Stopstate_lnclk. After an appropriate clk2req delay (see Table 42-5 for clk2req timing), TxSkewCalHS_ln0 will be asserted. This will start an internal counter in the DSI-2 Host Core which will start with the DSI_SKEWCALTIMI input value and count down to 0. In this figure, DSI_SKEWCALTIM is set for the minimum skewcal time of 4096 core clocks. When the timer reaches 0, TxSkewCalHS_ln0 is de-asserted. After an appropriate stop2notclk delay (see Table 42-5 for stop2notclk timing), TxRequestHS_lnclk is de-asserted followed by skewcal_done asserted after a gap delay (see Table 42-5 for gap timing) to indicate to user logic that the sequence has finished and to deassert skewcal_i.

Figure 42-11 TX Core Initial Skew Calibration operation

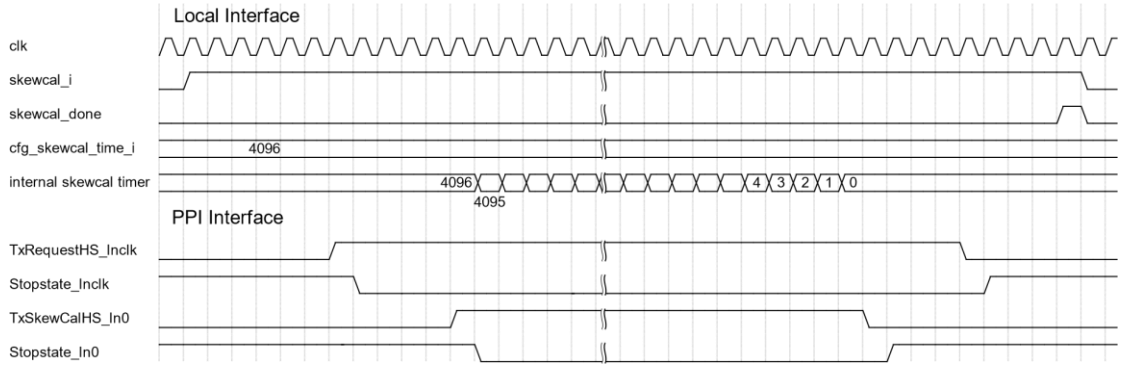
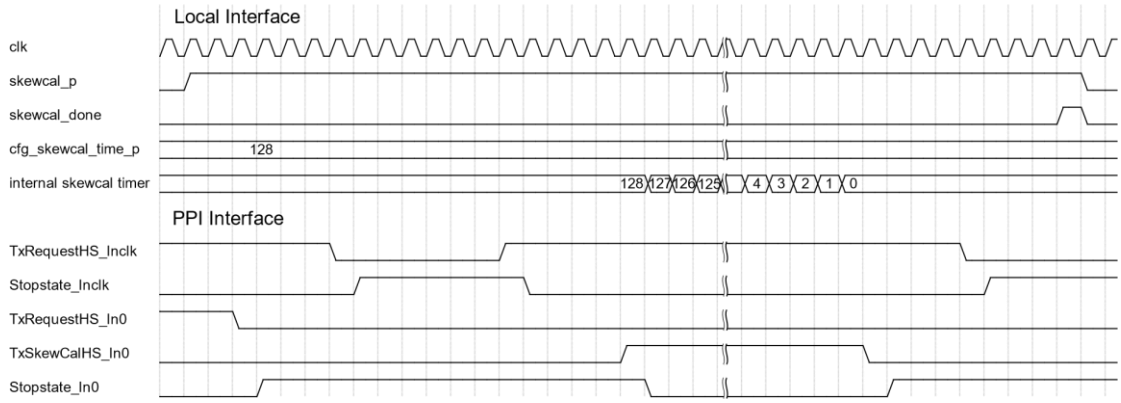


Figure 42-12 shows an example of a periodic skew calibration operation for lane 0. User logic asserts the DSI-2 Host Core user interface skewcal_p signal. However, an existing high-speed packet is currently being sent. The skew calibration DSI-2 Host Core logic will wait until the request finishes and then will assert TxRequestHS_lnclk to enable the Host D-PHY clock lane. The PHY will respond with the de-assertion of Stopstate_lnclk. After an appropriate clk2req delay (see Table 42-5 for clk2req timing), TxSkewCalHS_ln0 will be asserted. This will start an internal counter in the DSI-2 Host Core controller which will start with the DSI_SKEWCALTIMP input value and count down to 0. In this figure, DSI_SKEWCALTIM is set for the minimum skewcal time of 128 core clocks. When the timer reaches 0, TxSkewCalHS_ln0 is de-asserted. After an appropriate stop2notclk delay (see Table 42-5 for stop2notclk timing), TxRequestHS_lnclk is de-asserted followed by skewcal_done asserted after a gap delay (see Table 42-5 for gap timing) to indicate to user logic that the sequence has finished and to deassert skewcal_p.

Figure 42-12 TX Core Periodic Skew Calibration operation



Minimum and Maximum skew calibration lengths are specified by the MIPI spec in terms of minimum number of UI (time for one bit) cycles and a maximum of absolute time. The DSI-2 Host Core logic runs off the main clk input which is 1/8 the frequency of the bit rating resulting in the following minimum and maximums:

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Table 42-6 CSI-2 TX Controller SkewCal timer value ranges

SkewCal Mode	Minimum UI Units	Minimum Timer Value	Maximum Skew Time	Maximum Timer Value
Initial	32,768 (2^15)	4,096+OFFSET	100 us	(X Gbps * 12,500)-OFFSET
Periodic	1,024 (2^10)	128+OFFSET	10 us	(X Gbps * 1,250)-OFFSET

OFFSET is the number of clock cycles between the assertion of TxSkewCalHS and the lane actually starting the calibration sequence. It includes the transition into high speed settle time as well as the high speed zero and high speed sync time. This value can be PHY specific and ranges between 20 and 105 have been observed. A conservative value of 150 is recommended.

For example, if D-PHY is running at 1.5Gbps then the maximum initial skewcal timer value would be (1.5*12,500)-150 = 18,600. If D-PHY is running at 4.5Gbps then the initial skewcal maximum timer value would be (4.5*12,500)-150 = 56,100.

42.9 DSI-2 Host Controller Configuration

42.9.1 DSI-2 Host Controller clock input and selection

The DSI-2 Host Controller using below clock to operation.

42.9.1.1 hse_ref_clk

The DPHY use HSE as refer clock input and generate the **dsi_ref_txwordclkhs_clk**, which is using as one of inputs for the main clock for packet generation and transfer. HSE clock can be configured via RCC register.

DPHY uses HSE as input, and output HS-CLK after D-PHY PLL processing:

- HS-CLK/2 generates DDR clock for HS-CLANE
- HS-CLK/2 generates lane_byte_clk clock, i.e. dsi_ref_txwordclkhs_clk clock

42.9.1.2 dsi_bus_clk

DSI host controller connected to APB6 of the bus system, this clock is a MIPI DSI configuration clock.

42.9.1.3 dsi_ker_clk

The clk clock is used by the DSI-2 Host Controller to interface to the MIPI Tx DPHY High Speed PPI interface. The frequency is 1/8th the data rate of the DPHY Data Lane High Speed data rate. There are two clock that can be selected for dsi_ker_clk via RCC register RCC_AXISEL1.DSIKERSEL[1:0] DSI Kernel clock selection register.

- 00: DSI reference clock (dsi_ref_txwordclkhs_clk) is selected as DSI kernel clock
- 01: PLL3_C clock is selected as DSI kernel clock

42.9.1.4 dsi_ulps_clk

This clock input for DSI in ULPS transfer mode, and can be select by RCC register RCC_AXISEL1.DSIULPSSEL[1:0]: DSI ULPS clock selection register.

- 00: DSI reference clock (dsi_ref_txwordclkhs_clk) is selected as DSI ULPS clock

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- 01: PLL3_C clock is selected as DSI ULPS clock

42.9.1.5 dsi_tx_esc_clk

The clk_tx_esc clock is used by the MIPI Tx DPHY for state control and low power data transmission. The DSI-2 Host Controller also uses clk_tx_esc for the portion of controller logic that interfaces to the MIPI Tx DPHY that are synchronous to clk_tx_esc. This clock can be select by RCC register RCC_AXISEL1.DSIPPITXSEL[1:0]: "dsi_ppi_txclkesc_all_clk" clock selection register.

- 00: Divided DSI reference clock is selected as DSI PPI clock
- 01: PLL2_B clock is selected as DSI PPI clock
- 10: Peripheral clock is selected as DSI PPI clock
- 11: Divided AXI bus clock is selected as DSI PPI clock

42.9.1.6 dsi_vid_clk

The vid_clk(dsi_vid_clk) clock is used on the DSI-2 Host Video Interface. All of video interface signals are synchronous to this clock. The DSI-2 Host Video Interface module handles transferring video data received in the vid_clk clock domain over to the clk clock domain. The vid_clk and clk frequencies are related by the following formula:

clk_freq >= vid_clk_freq * video_pixel_size / (8 * (DSI_NUMLANES))

- DSI_NUMLANES = the configuration port setting that selects the number of active MIPI DPHY data lanes
- clk_freq = frequency of clk which is 1/8th the High Speed data lane rate
- vid_clk_freq = frequency of the vid_clk clock on the video interface
- video_pixel_size = size of pixels, in bits, on the video interface

This clock is input from LCDC output (pixel_clk_o), detail configuration of this clock please refer to LCDC part.

42.9.2 Host Controller Reset and Initialization

Reset and Initialization procedure for the DSI-2 Host Controller is as follows:

1. Assert all resets for DSI Host/Wrapper/PHY
2. Power on graphic domain
3. Enable clocks and wait until clocks to the Host Controller are stable
4. De-assert DSI wrapper register reset
5. Program DSI wrapper register to configure PHY parameters (clock, timing, lane, etc)
6. De-assert DSI core reset including PHY
7. Wait until PHY is ready in the DSIPHY_WRAP_DSR register
8. Configure DSI_CLKLANEN and DSI_DATLANEN. If Spread Spectrum Clock is needed, set DSIPHY_PLLCTRL3.SSC_EN = 1

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9. Wait for 100us of PHY initialization
10. Program DSI Host registers. Note that video alignment must be enabled for video mode
11. Set DSI_NUMLANES to enable the controller

42.9.3 DSI-2 Host Controller Interrupt

42.9.3.1 DSI-2 Host controller error handling

DSI-2 host controller has 4 video errors type as below, and each error above can be enabled to trigger an interrupt. As show Table 42-7.

Table 42-7 DSI-2 Host controller video error

Error name	Description
vid_error_fifo_overflow	Asserted if internal video FIFO overflows. The video rate might be higher than the MIPI rate or the delay for MIPI is long enough that the FIFO overflows. This may indicate that VID_CLK is too fast, or that the VID_x parameters are incorrectly set.
vid_error_fifo_underflow	Asserted if internal video FIFO underflows. The video rate might be lower than the MIPI rate. This may indicate that VID_CLK is too slow, or that the VID_x parameters are incorrectly set.
vid_error_sync_pulse	Only asserted if VID_VIDEOMOD is set to “Non-Burst mode with Sync Pulses”. New vid_hsync was detected while still sending blanking from last video line. This can occur if video rate is set to higher than MIPI rate and there are not enough cycles to transmit the video blanking after transmitting the video line. This may indicate that VID_CLK is too fast, or that the VID_x parameters are incorrectly set.
vid_error_blanking	Only asserted if VID_VIDEOMOD is set to “Burst Mode” and VID_BPLLMOD is set to 1’b1. Asserted if not enough blanking time between end of a video line and the next vid_hsync. If video line transmission to the controller is occurring when a new vid_hsync is detected, this error signal will be asserted. This may indicate that VID_CLK is too fast, or that the VID_x parameters are incorrectly set.

42.9.3.2 DSI-2 Host Controller Interrupt as Wakeup Events

DSI-2 Host controller interrupt can be used as events to wake up the CPU from low power state. Setting flow is as below:

1. Configure RCC to enable DSI clock in run mode and low power mode
2. Configure EXTI to enable DSI video error interrupt for the target CPU
3. Configure DPHY, DSI-2 host controller, setting enable DSI interrupt enable in DSI wrapper register
4. Configure LCDC to input to DSI, then DSI will operation and display to external display
5. Then can put CPU to low power state, each CPU or both CPU is all fine
6. Whenever the transmission has error, the interrupt will be trigger and it wake CPU to interrupt handler
7. In interrupt handler process, clear the interrupt source and resume

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42.10 D-PHY Physical Layer

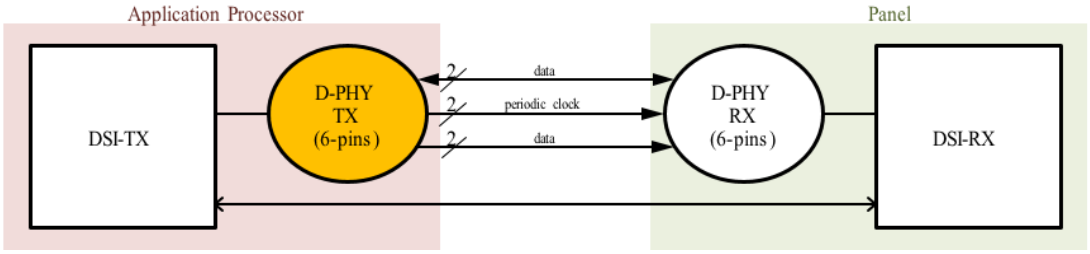
42.10.1 DPHY feature

- Complies MIPI D-PHY 8-bit PPI
- Supports up to four data lanes scalability in single channel mode
- Supports P/N pin swap function in each D-PHY lane
- Supports MIPI DSI interfaces
- Supports Triggers, ULPS and LPDT

42.10.2 DPHY System-Level Overview

Figure 42-13 shows a system-level block diagram of MIPI DSI with the MIPI D-PHY TX solution. It interfaces with MIPI DSI-TX controller by MIPI standard PPI for each state respectively. MIPI D-PHY interface on MIPI D-PHY TX block is defined by the differential lanes, which contains at least one clock lane and one data lane. These signals interface to the external world and connect to a MIPI D-PHY RX.

Figure 42-13 Typical Application and System-Level Diagram of MIPI D-PHY TX



42.10.3 Functional Overview

42.10.3.1 Clock Generator Operation

The clock generator is used to generate the clock signals required by this IP for high speed transmission. This clock generator is usually implemented by a phase-locked-loop (PLL) and several clock dividers.

42.10.3.2 LP-TX Operation

The Low-Power transmitter is a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a Low-Power transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low.

42.10.3.3 HS-TX Operation

A High Speed differential signal driven on the Dp and Dn pins is generated by a differential output driver. For reference, Dp is considered as the positive side and Dn as the negative side. The Lane state is called Differential-1 (HS-1) when the potential on Dp is higher than the potential of Dn. The Lane state is called Differential-0 (HS-0)

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when the potential on Dp is lower than the potential of Dn.

42.10.3.4 LP-RX Operation

The Low-Power receiver is an un-terminated, single-ended receiver circuit. The Low-Power receiver is used to detect the Low-Power state on each pin. For high robustness, the Low-Power receiver shall filter out noise pulses and RF interference. This low-power receiver design is featured with optimized power consumption.

42.10.3.5 LP-CD Operation

The Contention Detector in the MIPI DSI specification is a mechanism for detecting line contention and signal faults in low-power mode in bidirectional data channels. In low-power mode, the signal is transmitted over a low-power differential line at a single-ended level, so the host and display may try to drive a single data line at the same time, resulting in line contention.

The Contention Detector is a voltage monitoring circuit whose threshold voltage (VIHCD and VILCD) is stricter than that of ordinary LP receivers (VIH/VIL), satisfying the relationship: VILCD < VIL < VIH < VIHCD. LP-CD is used to detect two types of anomalies:

- Detect line contention: When the host and display drive the data line at the same time, the line voltage will be in the middle level, so LP-CD determines whether there is contention by comparing the line voltage with the threshold (VIHCD and VILCD).
  - The host driver is high (expected voltage ≥ VIH), but the actual voltage is pulled down to < VIHCD by the display device, and the LP-CD triggers race detection
  - The host driver is low (expected voltage ≤ VIL), but the actual voltage is pulled up to > VILCD by the display device, and the LP-CD triggers race detection
- Detect signal faults in low-power mode:
  - High-level fault: When the LP transmitter drives high, the expected line voltage should be ≥ VIH, but the actual voltage is lower than VIL, the normal LP receiver will detect the low level (< VIL), so the LP receiver will judge it as a high-level fault
  - Low Level Fault: When the LP transmitter drives low, the expected line voltage should be ≤ VIL, but the actual voltage is higher than the VIHCD, because the VIH of the normal LP receiver may not be sensitive enough, so the LP-CD will trigger the low level fault. The LP-CD reports a fault only when the line voltage is higher than the VIHCD

The general operation of a Contention Detector (LP-CD) is similar to that of a Low-Power receiver with lower threshold voltages. The Low-Power receiver and a separate Contention Detector shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-Power signal. The Contention Detector is required to detect line contention. The Low-Power receiver shall be used to detect a high fault in Low-Power mode when the Low-Power transmitter is driving high and the pin voltage is less than VIL. The LP-CD shall be used to detect a low fault in Low-Power mode when the LP transmitter is driving low and the pin voltage is greater than VIHCD. A low fault in Low-Power mode shall not be detected when the pin voltage is less than VILCD.

42.10.3.6 Logical PHY-Protocol Interface

The PHY Protocol Interface (PPI) is used to connect the PHY Lane Modules and the higher protocol layers of a communication stack. The interface described here is generic and application independent.

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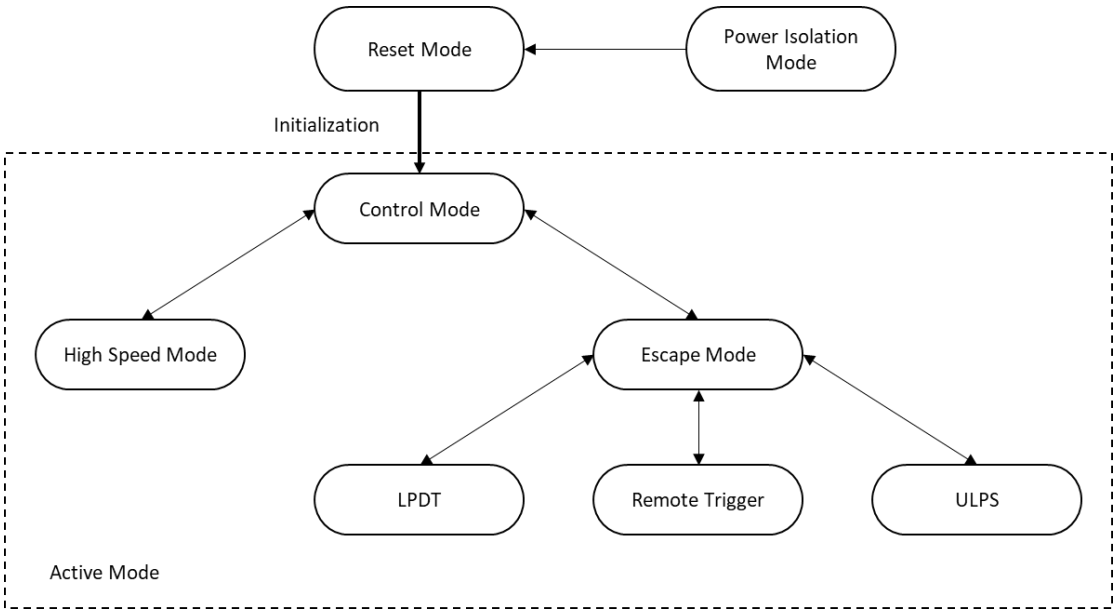
This PPI is optimized to control a D-PHY and transmit/receive the parallel data. This PPI is defined as an on-chip connection, and does not minimize signal count or define timing parameters/voltage levels for the PPI signals.

The PPI defines the signals connecting the PHY and the Controller. For a PHY with multiple Data Lanes, each lane uses a respective set of PPI signals.

42.10.4 Operation Overview

Figure 42-14 D-PHY Operation Modes Diagram



42.10.4.1 Power Isolation Mode

Power collapsing enables this IP to stay in power isolation mode (in any known combination of power supply availability, such as present, floating, or grounded) with low current consumption. This low current consumption remains similar to, or below, the current consumption in Suspend mode.

Power collapsing provides customers who require control over the power lines with the independent control of DPHY power supplies. Please check Chapter 42.11 for more details about power collapsing and power supply sequencing.

42.10.4.2 Reset Mode (Suspend)

This IP consumes less power in Reset mode when all analog blocks are disabled and the digital logic is reset. The current consumption comes from the analog stand-by current and the digital logic leakage current. Reset mode is entered asynchronously when “dsi_phy_rst_n” is in low-state. When “dsi_phy_rst_n” is set to logic high level, this IP leaves Reset mode and starts an initialization procedure.

This IP comprises four data lanes, but applications can operate with four or fewer data lanes. In such cases, users are granted access to individual enabling signals (ppi_enable_lanN) to control which lanes should be used and evolved through all the necessary initialization steps. Such configurations are assumed to be static or at least stable prior to de-asserting “dsi_phy_rst_n.”

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42.10.4.3 Initialization

In power supply sequence, “dsi_phy_rst_n” is held low until all power supplies are stable, this process is handled by hardware when MIPI DSI is powered up.

During initialization, this IP enables the clock generator, and wait until all clocks are stable.

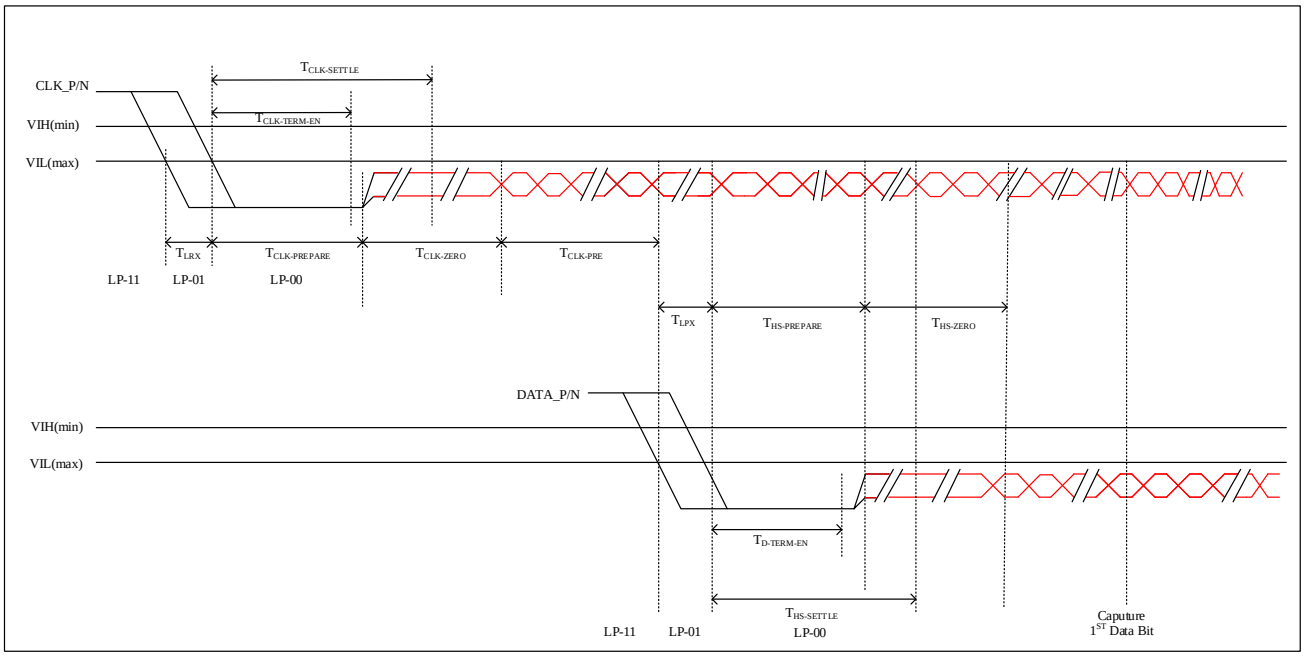
The master PHY shall drive a Stop state (LP-11 in D-PHY) for a period longer than TINIT to the slave PHY. The D-PHY specification v1.2 does place a minimum bound on the length of TINIT, which each shall be longer than 100 us. The first Stop state longer than the specified TINIT is called the initialization period. This IP does not set any limitation on the initialization period, meaning that it drives a Stop state immediately after an initialization and wait for the control signals from the controller.

In multi-lane configurations, all used lanes shall be initialized simultaneously.

42.10.5 DPHY Timing

To ensure proper entry into HS mode, it is critical to correctly configure the timing parameters of the transmitter and receiver. As show Figure 42-15.

Figure 42-15 The clock and data lane enter the HS transmission



The Table 42-8 describes the timing parameters in the preceding figure.

Table 42-8 D-PHY SoT timing parameter

Parameter	Description
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prio1to any associated Data Lane beginning the transition from LP to HS mode
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the Hs transmission
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting

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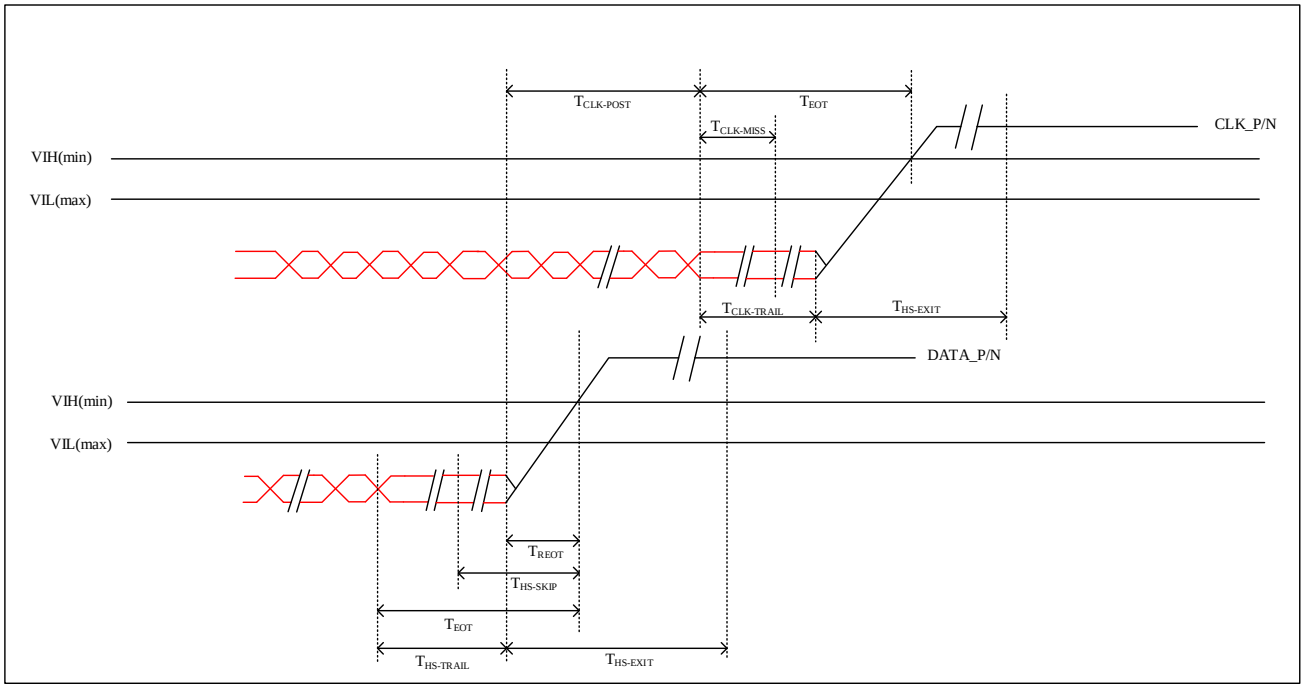
	from the beginning of TCLK-PREPARE
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock
TCLK-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL-MAX..
TCLK-ZERO	The time when the transmitter drives the HS-0 state before turning on the clock
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL-MAX.
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the Hs transmission
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.
THS-ZERO	The time for the transmitter to drive the HS-0 state before sending the synchronization sequence
TLPX	Transmitted length of any Low-Power state period

At the end of a high-speed data burst, the data channel exits high-speed transmission mode and enters a stop state through the "End of Transmission" (EoT) process. The following diagram shows the EoT timing relationship between the sender/receiver pairs of the clock and data channels. As show Figure 42-16.

Figure 42-16 The clock and data lane exit HS transmission



The following Table 42-9 describes the timing parameters in the preceding figure.

Table 42-9 D-PHY EoT timing parameter

Parameter	Description
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has

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	transitioned to LP Mode. Interval is defined as the period from the end of THS_TRAILto the beginning of TCLK-TRALL.
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL_MAX
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIl_MAX.
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The endpoint of the interval is defined as the beginning of the LP-1.state following the HS burst.
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst

42.10.6 DPHY Modes

42.10.6.1 Control Mode (Stop-State)

Control mode is the default operating mode. After the initialization is completed, this IP remains in this default mode until some requests are made. In Control mode, the transmitter side sets the LP-11 state in D-PHY, which is called the Stop state. Any request must start from and end in a Stop state. Following a request, a lane can leave Control mode for either High Speed Data Transfer mode, Escape mode, or even Ultra-Low Power state.

42.10.6.2 High Speed Mode

High speed data transmission occurs in bursts. It is only during these bursts that the lane is in high speed mode. A high speed burst must start from and return to a Stop state (LP-11). A high speed burst allows payload data transmission through data lanes. Such data transmission is inherent with the existence of a valid DDR clock in the clock lane.

High speed data bursts are independent for each lane, which means that each data lane can start from and end with a high speed transmission independently. A burst contains the low power request sequence, the high speed data payload, and the end of transmission sequence. Figure 42-17 shows the high speed data transfer sequence.

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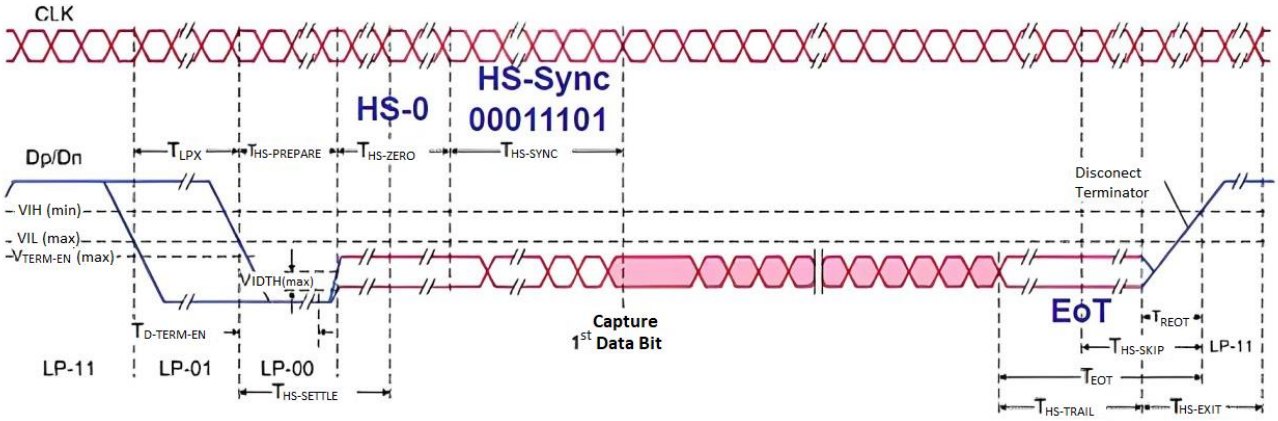
Figure 42-17 High Speed Data Transfer Sequence



The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER (Bit-Error-Rate) will not be zero.

When the high speed request input is disabled, each lane leaves the high speed data transmission mode. It is important that a clock lane must stay in high speed mode during the high speed data transmission. Therefore, ppi_enable_clk0 shall be set to high level to enable the clock lane module. The clock lane must enter the high speed mode before a high speed data transmission begins and must remain in this state until all data lanes have finished transmission bursts and returned to the Stop state.

Besides, it is important to consider different state diagrams for the clock lane and data lanes in high speed mode. According to Figure 42-18, the operation sequence for entering or leaving high speed mode is slightly different between clock and data lanes.

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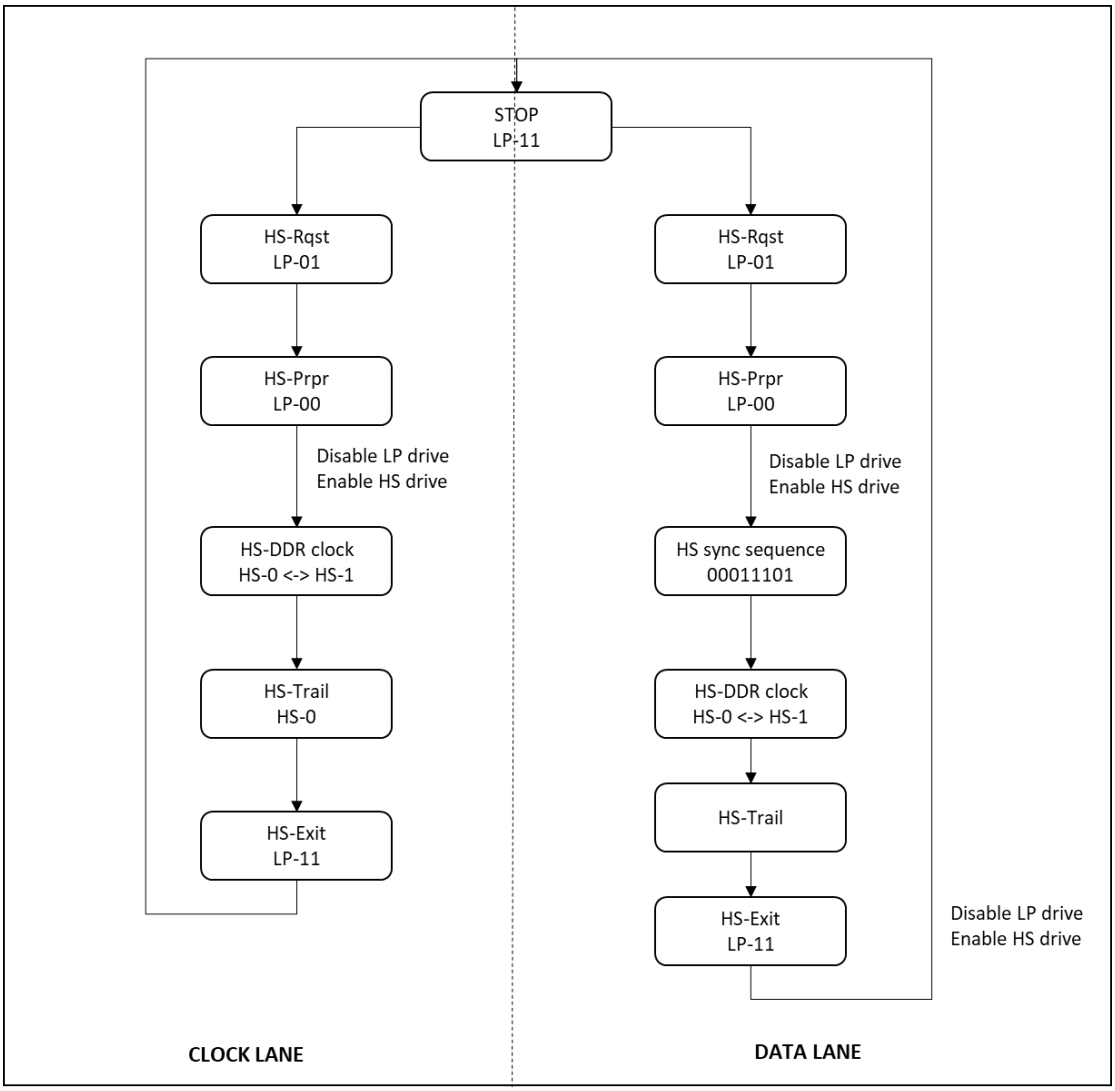
Figure 42-18 High Speed Transfer State Diagram



42.10.6.3 Escape Mode

Escape mode is a special mode of operation which can be used for low speed asynchronous data communication for data lanes using Low-Power states.

For data lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate a request. The following table lists all currently available Escape mode commands and actions. The MIPI D-PHY TX IP in Escape mode shall apply Space-One-Hot encoding (a Mark state is interleaved with a Space state) on commands and data.

Each symbol consists of the following two parts:

- One-Hot phase (Mark-0 or Mark-1)
- Space state

To transmit a “one bit,” a Mark-1 should be sent followed by a Space state. To transmit a “zero bit,” a Mark-0 should be sent followed by a Space state. A Mark that is not followed by a Space state does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not a part of the communicated bits, as it

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is not followed by a Space state. The length of each individual LP state period shall be at least TLPX, MIN.

Table 42-10 Escape mode entry command

Escape Mode Action	Command Type	Entry Command Pattern(first bit transmitted to last bit transmitted)
Low Power Data Transmission	Mode	11100001.
Ultra-Low Power State	Mode	00011110.
Undefined-1	Mode	10011111.
Undefined-2	Mode	11011110.
Reset-Trigger[remote application]	Trigger	01100010.
Unknown-3	Trigger	01011101.
Unknown-4	Trigger	00100001.
Unknown-5	Trigger	10100000.

42.10.6.4 Low-Power Data Transmission (LPDT)

In LPDT mode, data can be communicated by the protocol at low speed, while the lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code used for the entry commands. The last state before exiting Escape mode is Mark-1, which is not considered as one data bit, because it is followed by the Stop state.

42.10.6.5 Remote Trigger

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side.

Note that Trigger signaling including Reset-Trigger is a generic messaging system. The Trigger commands do not impact the behavior of the PHY itself. Therefore, Triggers can be used for any purpose by the Protocol layer.

42.10.6.6 Ultra Low Power State (ULPS)

ULPS is the lowest power consumption state in active mode.

During this state, the lines are in the Space state (LP-00). Although the clock lane does not support regular escape functions, the clock lane only supports the ULPS.

42.11 DPHY configuration

42.11.1 Reference Clock Period and Setting

Table 42-11 Phase Noise Mask Values of Reference Clock

refclk_in_sel [2:0]	refclk_in Frequency (MHz)
000	Reserved
001	12 MHz
010	19.2 MHz
011	25 MHz
100	26 MHz
101	27 MHz

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110	38.4 MHz
111	52 MHz

42.11.2 Escape Clock Period

The length of each individual LP state period shall be at least TLPX, MIN. The frequency of ppi_txclkesc_all should be less than or equal to 19.2 MHz.

Note: The ppi_txclkesc_all signal doesn't divide from any output of this IP.

42.11.3 Lane Swap function

DPHY support to swap the lane by change the physical port from one lane to the other lane.

Users can assign the relationship between PPI signals and each physical lane by setting CFG_L4_SWAP_SEL, CFG_L3_SWAP_SEL, CFG_L2_SWAP_SEL, CFG_L1_SWAP_SEL, and CFG_L0_SWAP_SEL input signals. MIPI D-PHY PPI uses number A=4 to represent CLK lane and number A(3-0) to present DATA lane 3-0, respectively.

For example, if DSIPHY_CTRL1.L4SEL[2:0] is set to 3'd3, DSIPHY_CTRL1.L3SEL[2:0] is set to 3'd2, DSIPHY_CTRL1.L2SEL[2:0] is set to 3'd4, DSIPHY_CTRL1.L1SEL[2:0] is set to 3'd1, and DSIPHY_CTRL1.L0SEL[2:0] is set to 3' d0, the corresponding CLK lane is set to the middle of physical layout. These are the suggested settings. Note that the assignment of DSIPHY_CTRL1.LxSEL[2:0] should be exclusive. The corresponding relationship is illustrated in Figure 42-19.

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Figure 42-19 Lane Swap Example

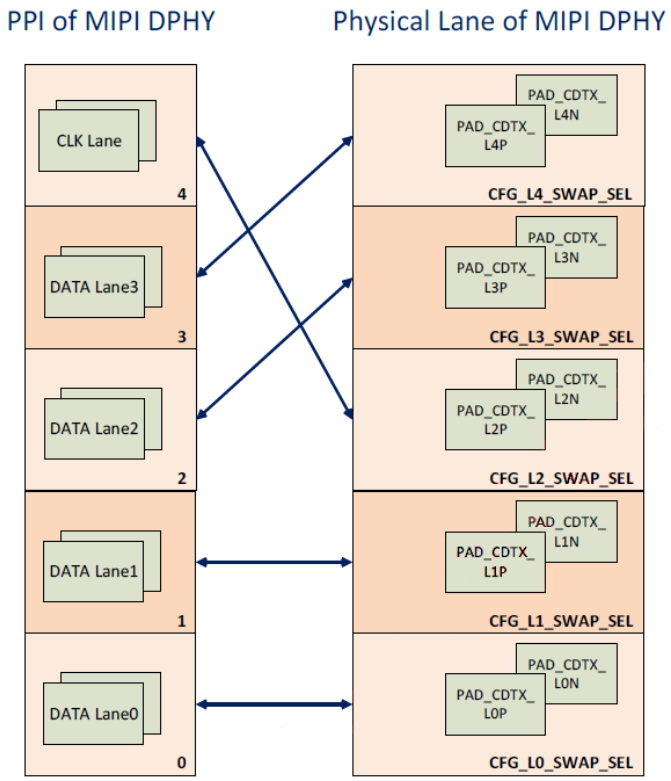

Table 42-12 shows the setting of DSIPHY_CTRL1.LxSEL[2:0]. We recommend users to set L0SEL[2:0] to 3'd0, L1SEL[2:0] to 3'd1, L2SEL[2:0] to 3'd4, L3SEL[2:0] to 3'd2, and L4SEL[2:0] to 3'd3.

Table 42-12 DSIPHY_CTRL1.LxSEL[2:0] Setting

Signal	Value	Mapping
DSIPHY_CTRL1.L0SEL[2:0]	3'd0	Data Lane0 <-> PAD_CDTX_L0x
DSIPHY_CTRL1.L1SEL[2:0]	3'd1	Data Lane1 <-> PAD_CDTX_L1x
DSIPHY_CTRL1.L2SEL[2:0]	3'd4	Clock Lane <-> PAD_CDTX_L2x
DSIPHY_CTRL1.L3SEL[2:0]	3'd2	Data Lane2 <-> PAD_CDTX_L3x
DSIPHY_CTRL1.L4SEL[2:0]	3'd3	Data Lane3 <-> PAD_CDTX_L4x

42.12 DSI registers

The DSI-2 Host controller registers contains the following two parts:

- DSI-2 Host controller registers, the starting address of this part of the register is 0x5000_0000.
- DSI Wrapper registers, the starting address of this part of the registers is 0x5004_AC00;

42.12.1 DSI host registers

42.12.1.1 DSI host lanes configuration register(DSI_NUMLANES)

Address offset: 0x00

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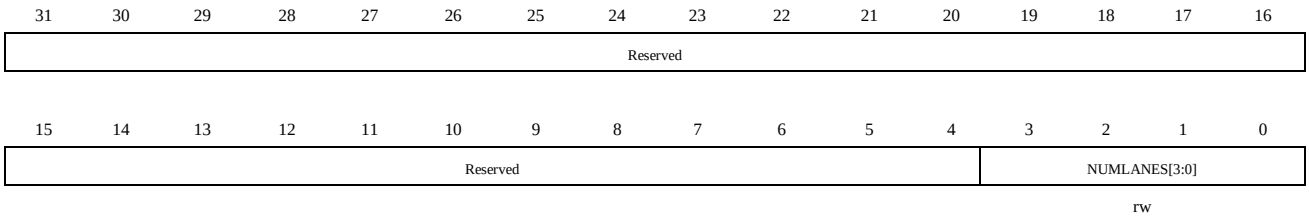
Reset value: 0x0000 0000

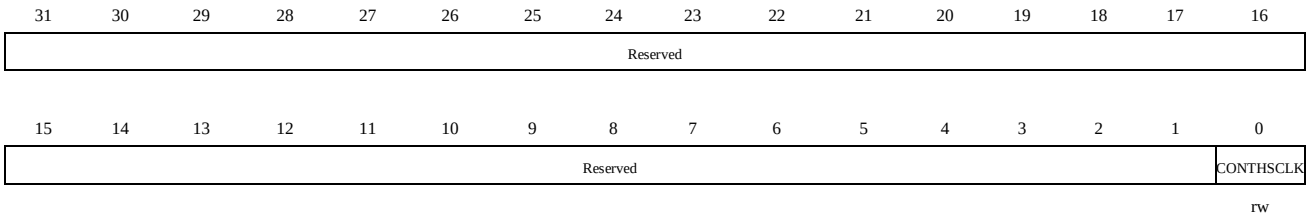


Bit field	Name	Description
31:4	Reserved	Reserved.
3:0	NUMLANES[3:0]	Sets the number of active lanes that are to be used for transmitting data. 0000: No active lanes (reset default) 0001: 1 Lanes 0010: 2 Lanes 0011: 3 Lanes 0100: 4 Lanes

42.12.1.2 DSI host continuous high-speed clock configuration register(DSI_CONTHSCLK)

Address offset: 0x04

Reset value: 0x0000 0000

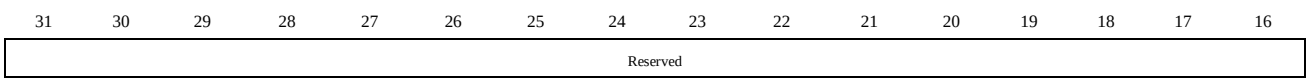


Bit field	Name	Description
31:1	Reserved	Reserved.
0	CONTHSCLK	Sets the Host Controller into continuous MIPI clock mode. When in non-continuous clock mode, the high speed clock will transition into low power mode between transmissions. 0: Non-Continuous high speed clock 1: Continuous high speed clock

42.12.1.3 DSI host DPHY configuration register1(DSI_TPRE)

Address offset: 0x08

Reset value: 0x0000 0000



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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TPRE[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved.
7:0	TPRE[7:0]	Sets the number of byte clock periods ('clk_byte' input) that the controller will wait after enabling the clock lane for HS operation before enabling the data lanes for HS operation. This setting represents the TCLK-PRE DPHY timing parameter. The minimum value for this port is 1.

42.12.1.4 DSI host DPHY configuration register2(DSI_TPOST)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TPOST[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved.
7:0	TPOST[7:0]	Sets the number of byte clock periods ('clk_byte' input) to wait before putting the clock lane into LP mode after the data lanes have been detected to be in Stop State. This setting represents the DPHY timing parameters TLPX + TCLK-PREPARE + TCLK-ZERO + TCLK-PRE requirement for the clock lane before the data lane is allowed to change from LP11 to start a high speed transmission. The minimum value for this port is 1.

42.12.1.5 DSI host DPHY configuration register3(DSI_TXGAP)

Address offset: 0x010

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TXGAP[7:0]							
								rw							

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Bit field	Name	Description
31:8	Reserved	Reserved.
7:0	TXGAP[7:0]	Sets the number of byte clock periods ('clk_byte' input) that the controller will wait after the clock lane has been put into LP mode before enabling the clock lane for HS mode again. This setting represents the THS-EXIT DPHY timing parameter. The minimum value for this port is 1.

42.12.1.6 DSI host auto insert EOTP register(DSI_AUTOINSERT_EOTP)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															AUTOINSEOTP
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	AUTOINSEOTP	Enables the Host Controller to automatically insert an EoTp short packet when switching from HS to LP mode. 0: EoTp is not automatically inserted 1: EoTp is automatically inserted

42.12.1.7 DSI host enable RX CRC check register(DSI_DISRXCRCCHK)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															DISRXCRCCHK
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	DISRXCRCCHK	Configures the DSI Host Controller to not check payload CRC from longs packets sent from the peripheral. 0: Check CRC 1: Not check CRC

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42.12.1.8 DSI host timeout counter configuration register1(DSI_HSTXTOCNT)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								HSTXTOCNT[23:16]							
								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSTXTOCNT[15:0]															
rw															

Bit field	Name	Description
31:24	Reserved	Reserved.
23:0	HSTXTOCNT[23:0]	Sets the value of the DSI Host High Speed TX timeout count in clk_byte clock periods that once reached will initiate a timeout error and follow the recovery procedure documented in the DSI specification.

42.12.1.9 DSI host timeout counter configuration register2(DSI_LRXTOCNT)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								LRXTOCNT [23:16]							
								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LRXTOCNT [15:0]															
rw															

Bit field	Name	Description
31:24	Reserved	Reserved.
23:0	LRXTOCNT[23:0]	Sets the value of the DSI Host low power RX timeout count in clk_byte clock periods that once reached will initiate a timeout error and follow the recovery procedure documented in the DSI specification.

42.12.1.10 DSI host timeout counter configuration register3(DSI_BTATOCNT)

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								BTATOCNT [23:16]							
								rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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BTATOCNT [15:0]

rw

Bit field	Name	Description
31:24	Reserved	Reserved.
23:0	BTATOCNT[23:0]	Sets the value of the DSI Host Bus Turn Around (BTA) timeout in clk_byte clock periods that once reached will initiate a timeout error.

42.12.1.11 DSI host timing wakeup register(DSI_TWAKEUP)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TWAKEUP[18:16]		
														rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TWAKEUP [15:0]															
rw															

Bit field	Name	Description
31:19	Reserved	Reserved.
18:0	TWAKEUP[18:0]	DPHY wakeup timing parameter. Sets the number of clk_esc clock periods to keep a clock or data lane in Mark-1 state after exiting ULPS. The MIPI DPHY spec requires a minimum of 1ms in Mark-1 state after leaving ULPS.

42.12.1.12 DSI host burst enable register(DSI_DISBST)

Address offset: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															DISBST
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	DISBST	Disables Host Controller bursting. 0: Packets are combined in a burst 1: Each packet is sent separately with a return to LP mode in between each packet

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42.12.1.13 DSI host periph status register(DSI_STS)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												BIT3	BIT2	BIT1	BIT0
												ro	ro	ro	ro

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROVILT	Reserved	INVLDTXL	VCIDINVLD	DATYPERR	CRCERR	ECCMERR	ECCSERR	COTDET	FCTRLERR	TOERR	LPTXSYNCERR	ESCMODERR	EOTSYNCERR	SOTSYNCERR	SOTERR
ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Bit field	Name	Description
31:20	Reserved	Reserved.
19	BIT3	Periph Status Register, bit 3 of last received Trigger This field is referenced to clock "core_clk".
18	BIT2	Periph Status Register, bit 2 of last received Trigger This field is referenced to clock "core_clk".
17	BIT1	Periph Status Register, bit 1 of last received Trigger This field is referenced to clock "core_clk".
16	BIT0	Periph Status Register, bit 0 of last received Trigger This field is referenced to clock "core_clk".
15	PROVILT	Periph Status Register, Protocol Violation This field is referenced to clock "core_clk".
14	Reserved	Periph Status Register, Reserved This field is referenced to clock "core_clk".
13	INVLDTXL	Periph Status Register, Invalid Transmission Length This field is referenced to clock "core_clk".
12	VCIDINVLD	Periph Status Register, VC ID Invalid This field is referenced to clock "core_clk".
11	DATYPERR	Periph Status Register, Data Type not Recognized This field is referenced to clock "core_clk".
10	CRCERR	Periph Status Register, CRC Err This field is referenced to clock "core_clk".
9	ECCMERR	Periph Status Register, Multi-bit ECC Err This field is referenced to clock "core_clk".
8	ECCSERR	Periph Status Register, Single-bit ECC Err This field is referenced to clock "core_clk".
7	COTDET	Periph Status Register, Contention Detected This field is referenced to clock "core_clk".
6	FCTRLERR	Periph Status Register, False Control Err This field is referenced to clock "core_clk".
5	TOERR	Periph Status Register, Periph Timeout Err This field is referenced to clock "core_clk".
4	LPTXSYNCERR	Periph Status Register, LP Transmit Sync Err This field is referenced to clock "core_clk".
3	ESCMODERR	Periph Status Register, Esc Mode Entry Err This field is referenced to clock "core_clk".
2	EOTSYNCERR	Periph Status Register, EoT Sync Err This field is referenced to clock "core_clk".
1	SOTSYNCERR	Periph Status Register, SotSync Err This field is referenced to clock "core_clk".
0	SOTERR	Periph Status Register, SoT Err This field is referenced to clock "core_clk".

42.12.1.14 DSI host RX error status register(DSI_ERRSTS)

Address offset: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					BATTOERR	LRXTOERR	HTXTOERR	CRCERR	ECCERRBIT[4:0]					ECCMERR	ECCSERR
					ro	ro	ro	ro	ro					ro	ro

Bit field	Name	Description
31:11	Reserved	Reserved.
10	BATTOERR	BTA timeout detected
9	LRXTOERR	Low power data receive timeout detected
8	HTXTOERR	High Speed forward TX timeout detected
7	CRCERR	CRC error detected
6:2	ECCERRBIT[4:0]	Error bit position for single bit ECC error
1	ECCMERR	ECC multi bit error detected
0	ECCSERR	ECC single bit error detected

42.12.1.15 DSI host CLK lane enable register(DSI_CLKLANEN)

Address offset: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															CLKLANEN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	CLKLANEN	Setting this bit enables the PHY clock lane, 0: Disable PHY clock lane 1: Enable PHY clock lane

42.12.1.16 DSI host DATA lane enable register(DSI_DATLANEN)

Address offset: 0x64

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DATLANEN[3:0]			
												rw			

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Bit field	Name	Description
31:4	Reserved	Reserved.
3:0	DATLANEN[3:0]	Setting bits to a '1' value causes PHY enable signals to be asserted [0] –Enable data lane 0 [1] –Enable data lane 1 [2] –Enable data lane 2 [3] –Enable data lane 3

42.12.1.17 DSI host initial skew calibration time register(DSI_SKEWCALTIMI)

Address offset: 0xC0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SKEWCALTIMI [15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	SKEWCALTIMI[15:0]	Host Initial Skew Calibration count. Sets the value of the initial skew calibration time in clk clock periods.

42.12.1.18 DSI host periodic skew calibration time register(DSI_SKEWCALTIMP)

Address offset: 0xC4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SKEWCALTIMP [15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	SKEWCALTIMP[15:0]	Host Periodic Skew Calibration count. Sets the value of the periodic skew calibration time in clk clock periods.

42.12.1.19 DSI host alternate calibration time register(DSI_ALTCALTIM)

Address offset: 0xC8

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALTCALTIM [15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	ALTCALTIM[15:0]	Host Alternate Calibration count. Sets the value of the alternate calibration time in clk clock periods.

42.12.1.20 DSI host periodic skew calibration line register(VID_SKEWCALINE)

Address offset: 0xCC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								SKEWCALINE[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved.
7:0	SKEWCALINE[7:0]	Sets the line to issue periodic skewcal. Set to zero for no skewcal.

42.12.1.21 DSI host VID enable register(VID_EN)

Address offset: 0x200

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	EN	Enables the video interface

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Bit field	Name	Description
		0: video interface off, no packets from the video interface are sent 1: video interface on, video on the video interface generate packets

42.12.1.22 DSI host VID pixels packet register(VID_PIXPERPKT)

Address offset: 0x204

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXPERPKT[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	PIXPERPKT[15:0]	Sets the number of pixels that are sent in a packet for each video line. If PIXPERPKT[15:0] == 1, would be set to the total pixels for each video line If PIXPERPKT[15:0] == 2, this should be set to half the number of pixels in a video line, and so on.

42.12.1.23 DSI host VID pixels size register(VID_PIXPLDSIZ)

Address offset: 0x208

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXPLDSIZ [15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	PIXPLDSIZ[15:0]	Maximum number of pixels that should be sent as one DSI packet. Recommended to be evenly divisible by the line size (in pixels).

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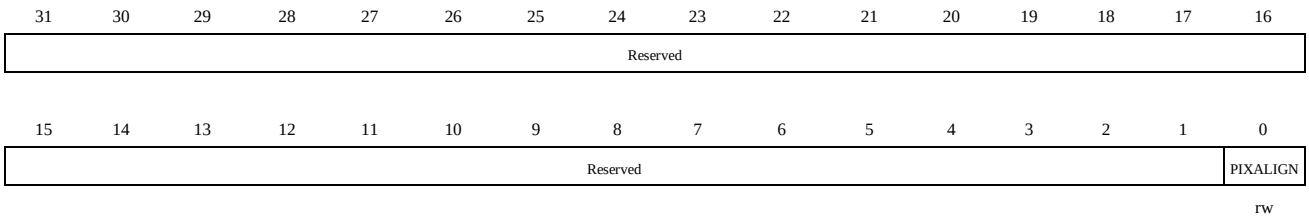
42.12.1.24 DSI host VID pixels alignment register(VID_PIXALIGN)

Address offset: 0x20c

Reset value: 0x0000 0000

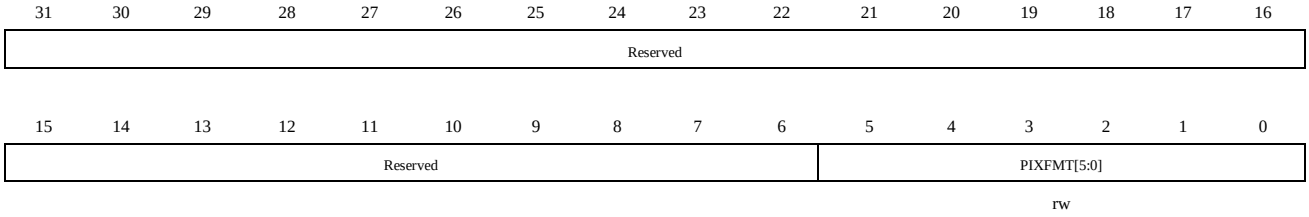


Bit field	Name	Description
31:1	Reserved	Reserved.
0	PIXALIGN	Sets the alignment for pixels smaller than the maximum pixel size. 0: LSB alignment 1: MSB alignment, Must be written 1 for video mode.

42.12.1.25 DSI host VID pixels format register(VID_PIXFMT)

Address offset: 0x210

Reset value: 0x0000 0000

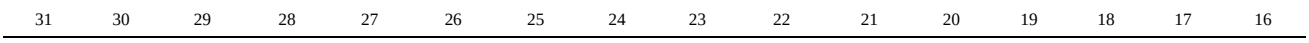


Bit field	Name	Description
31:6	Reserved	Reserved.
5:0	PIXFMT[5:0]	Sets the DSI-2 packet type of the pixels. Value is the actual data type sent across the MIPI interface. 0x0E: Packed Pixel Stream, 16-bit RGB, 5-6-5 format 0x1E: Packed Pixel Stream, 18-bit RGB, 6-6-6 format 0x2E: Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 0x3E: Packed Pixel Stream, 24-bit RGB, 8-8-8 Other value: Reserved

42.12.1.26 DSI host VID vsync polarity register(VID_VSYNCPOL)

Address offset: 0x214

Reset value: 0x0000 0000



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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															VSYNCPOL
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	VSYNCPOL	Sets polarity of VID vsync input 0: active low 1: active high

42.12.1.27 DSI host VID hsync polarity register(VID_HSYNCPOL)

Address offset: 0x218

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															HSYNCPOL
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	HSYNCPOL	Sets polarity of VID hsync input 0: active low 1: active high

42.12.1.28 DSI host VID video mode register(VID_VIDEOMOD)

Address offset: 0x21C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														VIDEOMOD[1:0]	
														rw	

Bit field	Name	Description
31:2	Reserved	Reserved.
1:0	VIDEOMOD[1:0]	Select DSI-2 video mode that the host VID module should generate packets for.

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Bit field	Name	Description
		00: Non-Burst mode with Sync Pulses 01: Non-Burst mode with Sync Events 10: Burst mode 11: Reserved

42.12.1.29 DSI host VID override mode register(VID_OVERIDE)

Address offset: 0x220

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OVERIDE
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	OVERIDE	Sets mode so VID parameters are used instead of measuring with first frame of video. 0: auto mode, first video frame is used to calibrate 1: override mode, VID values are used

42.12.1.30 DSI host VID line start delay register(VID_STD)

Address offset: 0x224

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	STD[15:0]	Sets the number of cycles to delay the start of line. Used to allow Pixel FIFO to fill.

42.12.1.31 DSI host VID HFP register(VID_HFP)

Address offset: 0x228

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HFP [15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	HFP[15:0]	Sets the DSI-2 packet payload size, in bytes, of the horizontal front porch blanking packet.

42.12.1.32 DSI host VID HBP register(VID_HBP)

Address offset: 0x22C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBP [15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	HBP[15:0]	Sets the DSI-2 packet payload size, in bytes, of the horizontal back porch blanking packet.

42.12.1.33 DSI host VID HSA register(VID_HSA)

Address offset: 0x230

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSA [15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.

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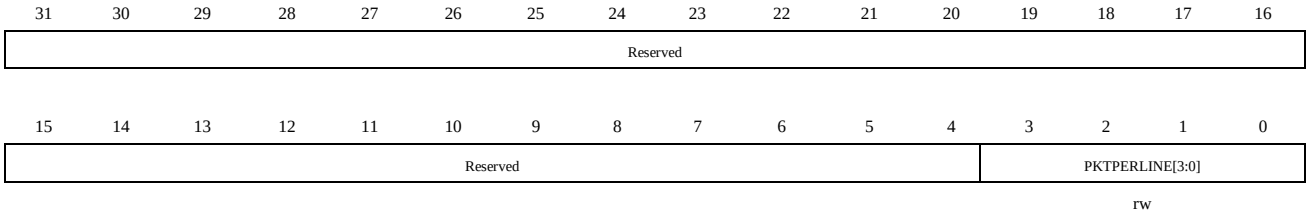
Bit field	Name	Description
15:0	HAS[15:0]	Sets the DSI-2 packet payload size, in bytes, of the horizontal sync width filler blanking packet.

42.12.1.34 DSI host VID packets number pre line register(VID_PKTPERLINE)

Address offset: 0x234

Reset value: 0x0000 0001

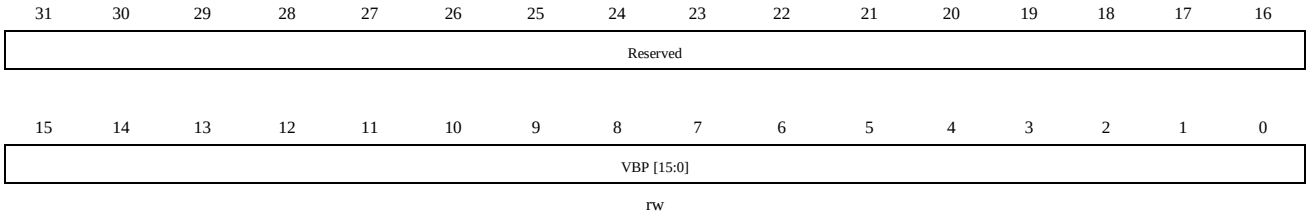


Bit field	Name	Description
31:4	Reserved	Reserved.
3:0	PKTPERLINE[3:0]	Set the number of packets per video line. Default is 1 0001: 1 packet sent per video line 0010: 2 packets sent 0100: 4 packets sent Others: Reserved

42.12.1.35 DSI host VID VBP register(VID_VBP)

Address offset: 0x238

Reset value: 0x0000 0000

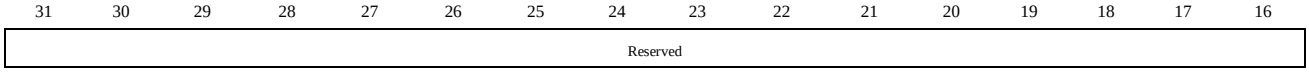


Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	VBP[15:0]	Sets the number of lines in the vertical back porch.

42.12.1.36 DSI host VID VFP register(VID_VFP)

Address offset: 0x23C

Reset value: 0x0000 0000



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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFP [15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	VFP[15:0]	Sets the number of lines in the vertical front porch.

42.12.1.37 DSI host VID BLLP mode register(VID_BLLPMOD)

Address offset: 0x240

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															BLLPMOD
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	BLLPMOD	Optimize BLLP periods to Low Power mode when possible 0: blanking packets are sent during BLLP periods 1: LP mode is used for BLLP periods

42.12.1.38 DSI host VID null packet BLLP register(VID_NULLPKTBLLP)

Address offset: 0x244

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															NULLPKTBLLP
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	NULLPKTBLLP	Selects type of blanking packet to be sent during BLLP region 0: Blanking packet used in BLLP region 1: Null packet used in BLLP region

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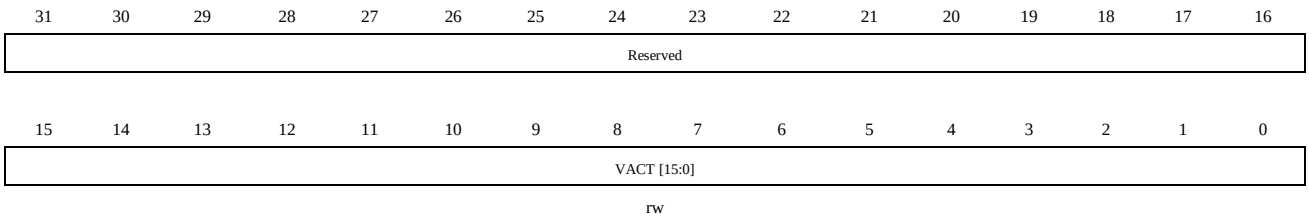
42.12.1.39 DSI host VID vertical active register(VID_VACT)

Address offset: 0x248

Reset value: 0x0000 0000

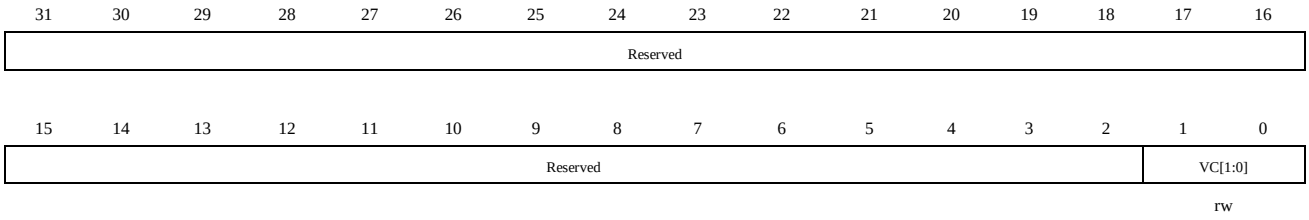


Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	VACT[15:0]	Sets the number of lines in the vertical active read.

42.12.1.40 DSI host VID virtual channel register(VID_VC)

Address offset: 0x24C

Reset value: 0x0000 0000

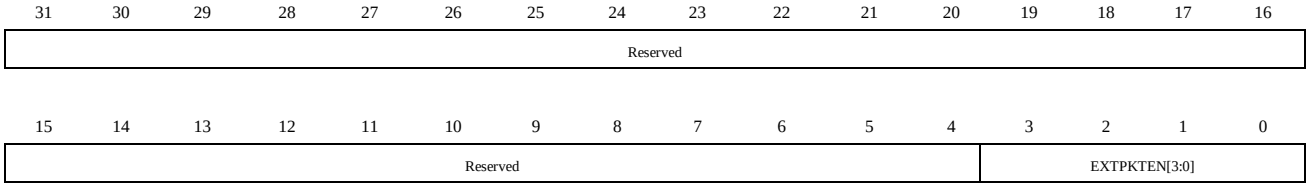


Bit field	Name	Description
31:2	Reserved	Reserved.
1:0	VC[1:0]	Sets the Virtual Channel (VC) of packets that will be sent to the receive packet interface. Packets with VC not equal to this value are discarded and the "DSI VC ID Invalid" bit (bit 12) in the DSI error report is set.

42.12.1.41 DSI host VID external packets register(VID_EXTPKTEN)

Address offset: 0x250

Reset value: 0x0000 0000



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rw

Bit field	Name	Description
31:4	Reserved	Reserved.
3:0	EXTPKTEN[3:0]	Selects when external to the video interface packet requests are allowed [0] - external packets are allowed during vertical sync [1] - external packets are allowed during vertical back porch [2] - external packets are allowed during active video lines [3] - external packets are allowed during vertical front porch

42.12.1.42 DSI host VID vertical sync start payload register(VID_VSSPLD)

Address offset: 0x254

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSSPLD [15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	VSSPLD[15:0]	Sets the payload value to be sent when a Vertical Sync Start Event.

42.12.1.43 DSI host VID payload per packet register(VID_PLDPERPKT))

Address offset: 0x258

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLDPERPKT [15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	PLDPERPKT[15:0]	Set the number of bytes that should be sent as one packet when VID_PKTPERLINE > 1. Each packet (compressed chunk) must contain the same number of bytes.

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42.12.1.44 DSI host TX payload register(DSI_TXPLD)

Address offset: 0x280

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXPLD [31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXPLD [15:0]															
rw															

Bit field	Name	Description
31:0	TXPLD[31:0]	Tx Payload data write register. Writes to this registers load the payload fifo with 32 bit values.

42.12.1.45 DSI host packet control register(DSI_PKTCTRL)

Address offset: 0x284

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					BTANOPKT	BTAIMM	MOD	HDTYP[5:0]						VC[1:0]	
					rw	rw	rw	rw						rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
rw															

Bit field	Name	Description
31:27	Reserved	Reserved.
26	BTANOPKT	Perform Bus Turn Around without sending a packet.
25	BTAIMM	Perform Bus Turn Around immediate after packet in transmitted
24	MOD	LP or HS select. 0: LP mode 1: HS mode
23:18	HDTYP[5:0]	Packet Data Type
17:16	VC[1:0]	Set Packet Virtual Channel
15:0	CNT[15:0]	Set Packet word count when send long packet Short packet data field when send short packet

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42.12.1.46 DSI host packet sent register(DSI_SENDPKT)

Address offset: 0x288

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															SENDPKT
															rw

Bit field	Name	Description
31:1	Reserved	Reserved.
0	SENDPKT	Writing a 1 to this bit will cause a packet to be transmitted with the packet header information loaded into DSI_PKTCTRL and if a long packet data type, using the payload data loaded into the tx payload FIFO via the DSI_TXPLD register.

42.12.1.47 DSI host packet status register(DSI_PKTSTS)

Address offset: 0x28C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							ALLRXPKTD	RXPKTD	RXFUNDER	RXFOVER	TXFUNDER	TXFOVER	DPHYDIR	TXD	NIDLE
							ro	ro	ro	ro	ro	ro	ro	ro	ro

Bit field	Name	Description
31:9	Reserved	Reserved.
8	ALLRXPKTD	All RX packet payload data has been received
7	RXPKTD	RX packet header has been received 0: RX packet headers has not been received 1: RX packet headers has been received
6	RXFUNDER	RX FIFO underflow 0: RX FIFO has not underflowed 1: RX FIFO has underflowed Clears to 1 upon read

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Bit field	Name	Description
5	RXFOVER	RX FIFO overflow 0: RX FIFO has not overflowed 1: RX FIFO has overflowed Clears to 1 upon read
4	TXFUNDER	TX FIFO underflow 0: TX FIFO has not underflowed 1: TX FIFO has underflowed Clears to 1 upon read
3	TXFOVER	TX FIFO overflow 0: TX FIFO has not overflowed 1: TX FIFO has overflowed Clears to 1 upon read
2	DPHYDIR	DPHY direction 0: TX had control 1: RX has control
1	TXD	TX packet done 0: TX packet has not been transmitted. 1: TX packet has been transmitted.
0	NIDLE	Machine state 0: State machine is idle 1: State machine is not idle

42.12.1.48 DSI host packet FIFO write register(DSI_PKTFWRLVL)

Address offset: 0x290

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PKTFWRLVL [15:0]															

ro

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	PKTFWRLVL[15:0]	Write level of TX payload FIFO.

42.12.1.49 DSI host packet FIFO read register(DSI_PKTFRDLVL)

Address offset: 0x294

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PKTFRDLVL[15:0]															
ro															

Bit field	Name	Description
31:16	Reserved	Reserved.
15:0	PKTFRDLVL[15:0]	Read level of TX payload FIFO.

42.12.1.50 DSI host packet RX payload register(DSI_PKTRXPLD)

Address offset: 0x298

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PKTRXPLD [31:16]															
ro															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PKTRXPLD [15:0]															
ro															

Bit field	Name	Description
31:0	PKTRXPLD[31:0]	Rx packet payload FIFO read access.

42.12.1.51 DSI host packet RX header register(DSI_PKTRXHDR)

Address offset: 0x29C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								VCN[1:0]		DATATYP[5:0]					
								ro		ro					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
ro															

Bit field	Name	Description
31:24	Reserved	Reserved.
23:22	VCN[1:0]	Rx packet Virtual Channel Number.
21:16	DATATYP[5:0]	Rx packet Data Type.
15:0	CNT[15:0]	Rx packet Word Count.

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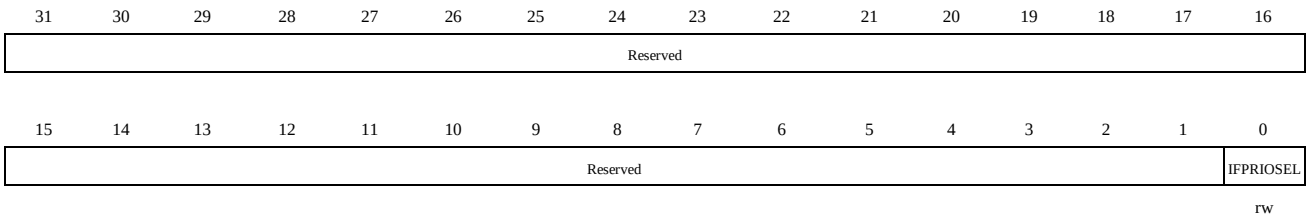
42.12.1.52 DSI host interface priority select register(DSI_IFPRIOSEL)

Address offset: 0x2B0

Reset value: 0x0000 0000



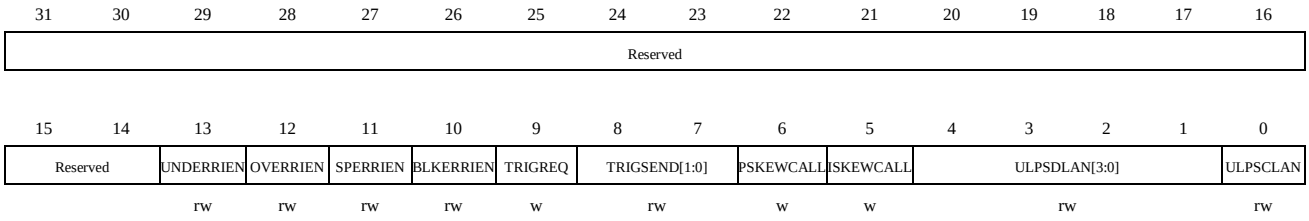
Bit field	Name	Description
31:1	Reserved	Reserved.
0	IFPRIOSEL	Host interface priority select: 0: Host Controller Core packet interface 1: APB packet interface

42.12.2 DSI wrapper registers

42.12.2.1 DSI wrapper control register(DSI_WRPCTRL)

Address offset: 0x00

Reset value: 0x0000 0000



Bit field	Name	Description
31:14	Reserved	Reserved
13	UNDERRIEN	Video underflow error interrupt enable.
12	OVERRIEN	Video overflow error interrupt enable.
11	SPERRIEN	Video sync pulse error interrupt enable.
10	BLKERRIEN	Video blanking error interrupt enable.
9	TRIGREQ	Transmit trigger request. This active high signal informs the controller that the trigger number on l_trigger_send is valid. The controller will assert l_trigger_ack when it accepts the command, after which, the user should either put update l_trigger_ack with the values for the next transmit packet or deassert l_trigger_req.
8:7	TRIGSEND[1:0]	Transmit trigger. The trigger number on trigger_send is sampled when trigger_ack is asserted high.

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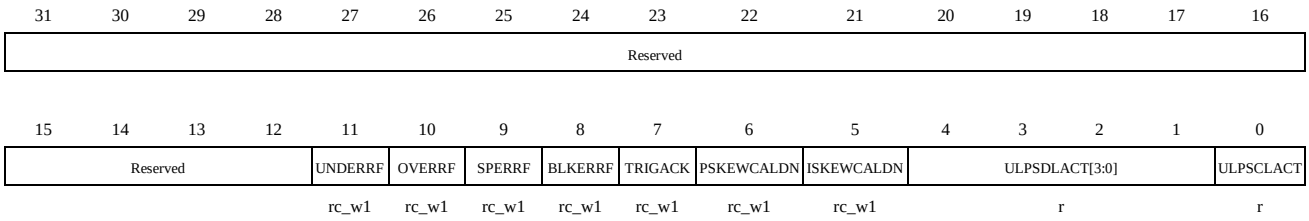
Bit field	Name	Description
		The format of trigger_send is as follows: 1'b00 = Trigger 0 (Reset-Trigger) 1'b01 = Trigger 1 ([Reserved]) 1'b10 = Trigger 2 ([Reserved]) 1'b11 = Trigger 3 ([Reserved])
6	PSKEWCAL	Periodic Skew Calibration Set by Software, Cleared by Hardware
5	ISKEWCAL	Initial Skew Calibration Set by Software, Cleared by Hardware
4:1	ULPSDLEN[3:0]	Ultra-Low Power State enable. When asserted (active high) the controller instructs the PHY to put the corresponding data lane into Ultra Low Power State. This signal is in the ulps_clk domain. Bit [0] – Data lane 0 Bit [1] – Data Lane 1 Bit [2] – Data Lane 2 Bit [3] - Data Lane 3
0	ULPSCLEN	Ultra-Low Power State enable for clock lane. When asserted (active high) the controller instructs the PHY to put the clock lane into Ultra Low Power State. This signal is in the ulps_clk domain.

42.12.2.2 DSI wrapper status register(DSI_WRPSTS)

Address offset: 0x04

Reset value: 0x0000 0000



Bit field	Name	Description
31:12	Reserved	Reserved
11	UNDERRF	Video underflow error interrupt flag.
10	OVERRF	Video overflow error interrupt flag.
9	SPERRF	Video sync pulse error interrupt flag.
8	BLKERRF	Video blanking error interrupt flag.
7	TRIGACK	Transmit trigger request acknowledge. This active high signal indicates that the controller has accepted the trigger request and the user logic should either submit a new request or deassert trigger_req on the next rising edge of pclk

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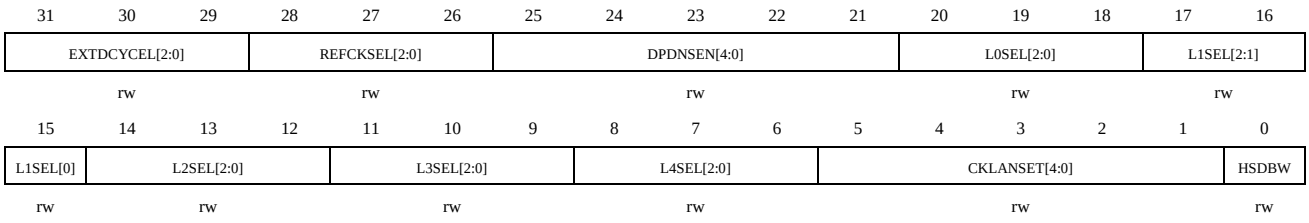
Bit field	Name	Description
		This bit is W1C by SW or cleared by HW when TRIGGER REQ is asserted
6	PSKEWCALDN	Periodic Skew Calibration DONE This bit is W1C by SW or cleared by HW when SKEWCAL_I asserted
5	ISKEWCALDN	Initial Skew Calibration DONE This bit is W1C by SW or cleared by HW when SKEWCAL_P asserted
4:1	ULPSDLACT[3:0]	Ultra Low Power State status. Bits assert high to indicate that the corresponding data lanes are in Ultra Low Power State. This signal is in the ulps_clk domain. Bit [0] – Data lane 0 Bit [1] – Data Lane 1 Bit [2] – Data Lane 2 Bit [3] – Data Lane 3
0	ULPSCLACT	Ultra Low Power State clock lane status. Asserted high to indicate that the clock lane is in Ultra Low Power State. This signal is in the ulps_clk domain.

42.12.2.3 DSI PHY wrapper control register1(DSIPHY_CTRL1)

Address offset: 0x08

Reset value: 0x0400 0020



Bit field	Name	Description
31:29	EXTDCYCEL[2:0]	High speed transmitter timing parameter.
28:26	REFCKSEL[2:0]	Reference Clock Selection. 000: Reserved. 001: 12 MHz (default) 010: 19.2 MHz. 011: 25 MHz. 100: 26 MHz. 101: 27 MHz. 110: 38.4 MHz. 111: 52 MHz. Synchronous to: refclk_in
25:21	DPDNSEN[4:0]	Enables DP/DN swap function.
20:18	L0SEL[2:0]	Configures Physical Lane 0 control source.
17:15	L1SEL[2:0]	Configures Physical Lane 1 control source.
14:12	L2SEL[2:0]	Configures Physical Lane 2 control source.
11:9	L3SEL[2:0]	Configures Physical Lane 3 control source.

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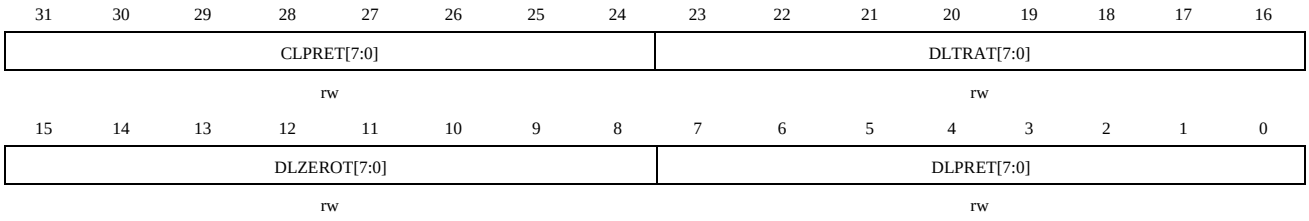
Bit field	Name	Description
8:6	L4SEL[2:0]	Configures Physical Lane 4 control source.
5:1	CKLANESET[4:0]	Sets the specified lane as the clock lane. Please tie this signal to 5'b10000 for the application of DPHY mode 1 x clock lane and 4 x data lanes.
0	HSDBW	Enable 16-bit data bus for HS mode. Low: normal 8-bit HS-PPI D-PHY mode. High: 16-bit HS-PPI D-PHY mode.

42.12.2.4 DSI PHY wrapper control register2(DSIPHY_CTRL2)

Address offset: 0x0C

Reset value: 0x0000 0000

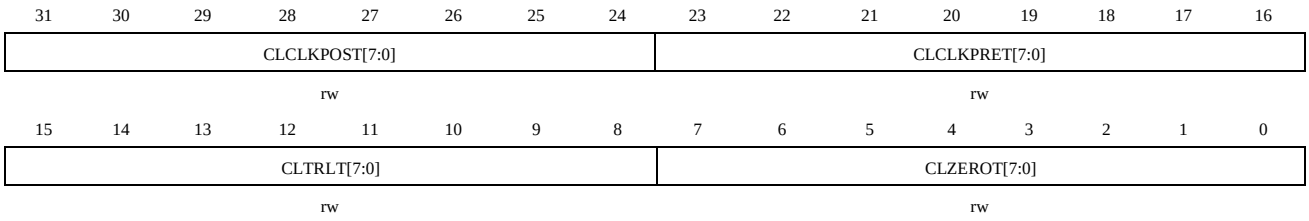


Bit field	Name	Description
31:24	CLPRET[7:0]	High speed transmitter timing parameter.
23:16	DLTRAT[7:0]	High speed transmitter timing parameter.
15:8	DLZEROT[7:0]	High speed transmitter timing parameter.
7:0	DLPRET[7:0]	High speed transmitter timing parameter.

42.12.2.5 DSI PHY wrapper control register3(DSIPHY_CTRL3)

Address offset: 0x10

Reset value: 0x0000 0000



Bit field	Name	Description
31:24	CLCLKPOST[7:0]	High speed transmitter timing parameter.
23:16	CLCLKPRET[7:0]	High speed transmitter timing parameter.
15:8	CLTRLT[7:0]	High speed transmitter timing parameter.
7:0	CLZEROT[7:0]	High speed transmitter timing parameter.

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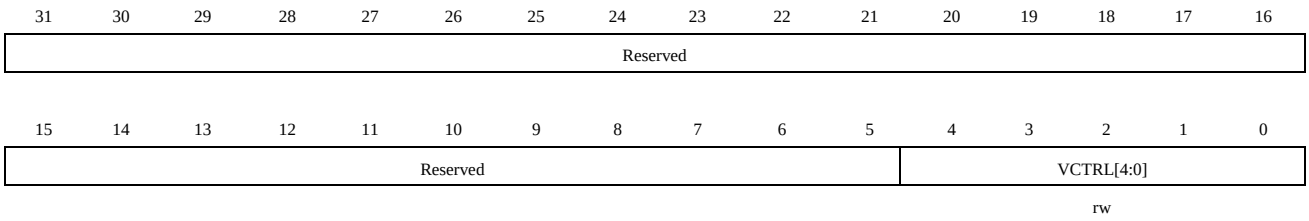
42.12.2.6 DSI PHY wrapper control register4(DSIPHY_CTRL4)

Address offset: 0x14

Reset value: 0x0000 0000

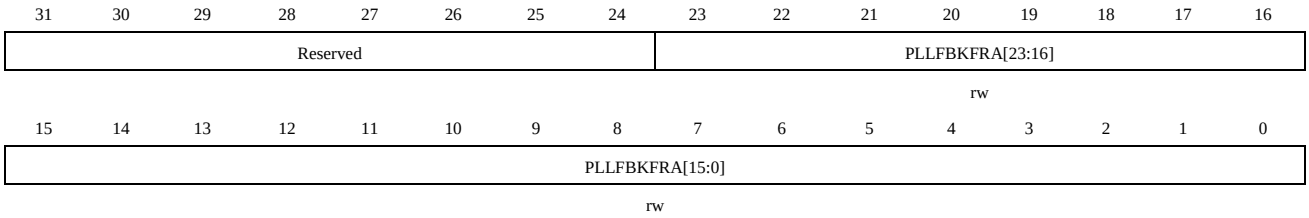


Bit field	Name	Description
31:5	Reserved	Must be kept at the reset value.
4:0	VCTRL[4:0]	Selection of PHY BIST mode. 5'd0: Normal mode 5'd1: LP RX DC test 5'd2: LP TX DC 1 5'd3: LP TX DC 0 5'd4: HS TX DC 1 5'd5: HS TX DC 0 5'd6 ~ 11: Reserved 5'd12: LP TX internal loopback 5'd13 ~ 28: Reserved 5'd29: HS TX internal loopback 5'd30: Reserved 5'd31: Suspend mode

42.12.2.7 DSI PHY PLL Control Register 1 (DSIPHY_PLLCTRL1)

Address offset: 0x64

Reset value: 0x0000 0000



Bit field	Name	Description
31:24	Reserved	Reserved
23:0	PLLFBKFRA[23:0]	Fractional part of the PLL feedback divider number

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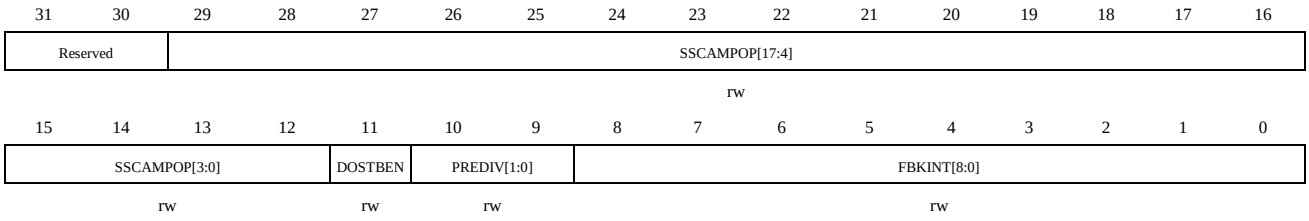
42.12.2.8 DSI PHY PLL Control Register 2 (DSIPHY_PLLCTRL2)

Address offset: 0x68

Reset value: 0x0000 0000

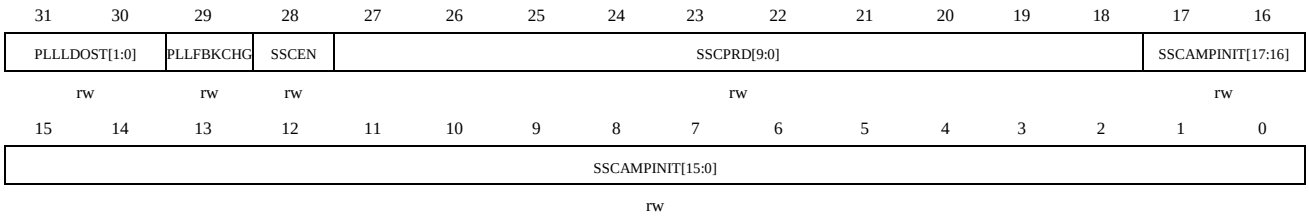


Bit field	Name	Description
31:30	Reserved	Reserved
29:12	SSCAMPOP[17:0]	SSC Amplitude Option
11	DOSTBEN	PLL internal LDO stable time adjustment
10:9	PREDIV[1:0]	PLL reference divider number that keeps pfd in a range of 10 MHz to 30 MHz
8:0	FBKINT[8:0]	Fractional part of the PLL feedback divider number

42.12.2.9 DSI PHY PLL Control Register 3 (DSIPHY_PLLCTRL3)

Address offset: 0x6C

Reset value: 0x0000 0000

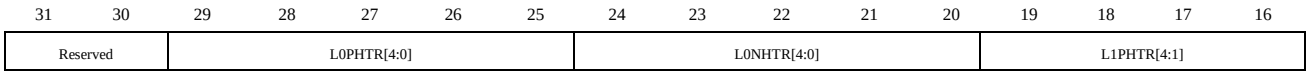


Bit field	Name	Description
31:30	PLLLDOST[1:0]	Internal LDO stable time option
29	PLLFBKCHG	Update signal of control setting of PLL feedback divider ratio, please update feedback divider ratio first, and then change RG_CDTX_PLL_FBK_CHG.
28	SSCEN	SSC Enable
27:18	SSCPRD[9:0]	SSC Period Option
17:0	SSCAMPINIT[17:0]	SSC Initial Amplitude Option

42.12.2.10 DSI PHY PLL Control Register 4 (DSIPHY_PLLCTRL4)

Address offset: 0x70

Reset value: 0x0000 0000



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				rw				rw				rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
L1PHTR[0]	L1NHTR[4:0]					L2PHTR[4:0]					L2NHTR[4:0]					
rw	rw					rw					rw					

Bit field	Name	Description
31:30	Reserved	Reserved.
29:25	L0PHTR[4:0]	HS-TX impedance option for lane 0 positive pin
24:20	L0NHTR[4:0]	HS-TX impedance option for lane 0 negative pin
19:15	L1PHTR[4:0]	HS-TX impedance option for lane 1 positive pin
14:10	L1NHTR[4:0]	HS-TX impedance option for lane 1 negative pin
9:5	L2PHTR[4:0]	HS-TX impedance option for lane 2 positive pin
4:0	L2NHTR[4:0]	HS-TX impedance option for lane 2 negative pin

42.12.2.11 DSI PHY PLL Control Register 5 (DSIPHY_PLLCTRL5)

Address offset: 0x74

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								PLLFMEN	PLLWTGEN	PLLFMTOR[1:0]		L3PHTR[4:1]			
								rw	rw	rw		rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3PHTR[0]	L3NHTR[4:0]					L4PHTR[4:0]					L4NHTR[4:0]				
rw	rw					rw					rw				

Bit field	Name	Description
31:24	Reserved	Reserved
23	PLLFMEN	PLL internal frequency meter enable
22	PLLWTGEN	Enable embedded watchdog to monitor the state of PLL reference clock and feedback clock
21:20	PLLFMTOR[1:0]	Control settings of frequency meter tolerance
19:15	L3PHTR[4:0]	HS-TX impedance option for lane 3 positive pin
14:10	L3NHTR[4:0]	HS-TX impedance option for lane 3 negative pin
9:5	L4PHTR[4:0]	HS-TX impedance option for lane 4 positive pin
4:0	L4NHTR[4:0]	HS-TX impedance option for lane 4 negative pin

42.12.2.12 DSI PHY PLL Status Register (DSIPHY_PLLSTS)

Address offset: 0x78

Reset value: 0x0000 0000

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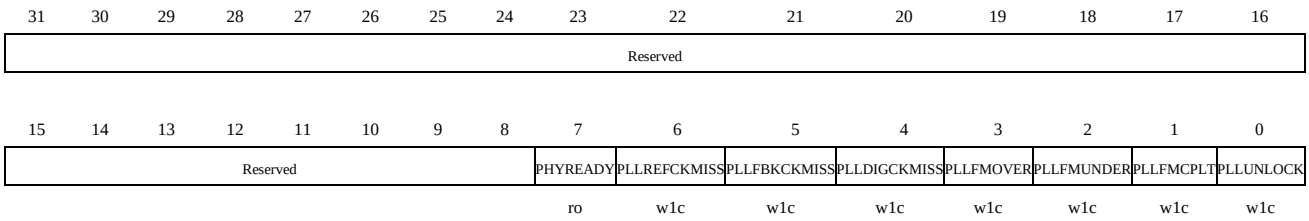

Bit field	Name	Description
31:8	Reserved	Reserved.
7	PHYREADY	PHY is ready
6	PLLREFCKMISS	Flags indicates that PLL reference clock is missing
5	PLLFBKCKMISS	Flags indicates that PLL feedback clock is missing
4	PLLDIGCKMISS	Flags indicates that embedded initial sequence is not complete
3	PLLFMOVER	Flag of PLL internal frequency meter calculation over spec
2	PLLFMUNDER	Flag of PLL internal frequency meter calculation under spec
1	PLLFMCPLT	Flag of PLL internal frequency meter calculation complete
0	PLLUNLOCK	Indicates that PLL is in unlock state

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43 JPEG Codec

43.1 Introduction

Supporting one JPEG codecs encode uncompressed image data streams or decode image data streams in JPEG compression mode. ISO/IEC 10918-1 standard are supported.

43.2 Main Features

The main features supported by ENCODER are shown below:

- Support for single frame images and Motion JPEG payloads
- Supports 8-bit color component sampling
- Supports up to 3 color components
- Support maximum image size of 64Kx64K
- Supports YCbCr and BW (grayscale) image color spaces
- YCbCr/YUV: 4:4:4, 4:2:2, 4:2:0
- Configurable JPEG header generator
- 4 8-bit programmable quantization tables
- 4 programmable Huffman tables (two AC meters and two DC meters)
- The minimum coding unit (MCU) is fixed at 8 x 8

The main features supported by DECODER are shown below:

- Support for single frame images and Motion JPEG payloads
- Supports 8-bit component sampling
- Supports up to 3 color components
- Support maximum image size of 64Kx64K
- Supports YCbCr and BW (grayscale) image color spaces
- YCbCr/YUV: 4:4:4, 4:2:2, 4:2:0
- 4 8-bit programmable quantization tables
- 4 programmable Huffman tables (two AC tables and two DC tables)

43.3 Abbreviations in the text

Table 43-1 Abbreviations in the text

Abbreviations	Hidden meaning
SOI	Start of Image

NSING Technologies Pte. Ltd.
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DRI	Define Restart interval
APP	Application Marker
COM	Comment marker
DQT	Define Quantization Table
DHT	Define Huffman Table
SOS	Start of Scan
ECS	Entropy Coded Segments
RST 0	Restart Marker 0
EOI	End of Image
DNL	Define number of line
EOB	End of Block
BRC	Block-to-Raster
RBC	Raster-to- Block
MCU	Minimum Coded Unit
SGDMA	Scatter-Gather Direct Memory Access
H2P	Host-to-Peripheral
P2H	Peripheral-to-Host
EOF	End of File
FSM	Finite State Machine)

43.4 Block Diagram

JPEG Codec block diagram is shown below:

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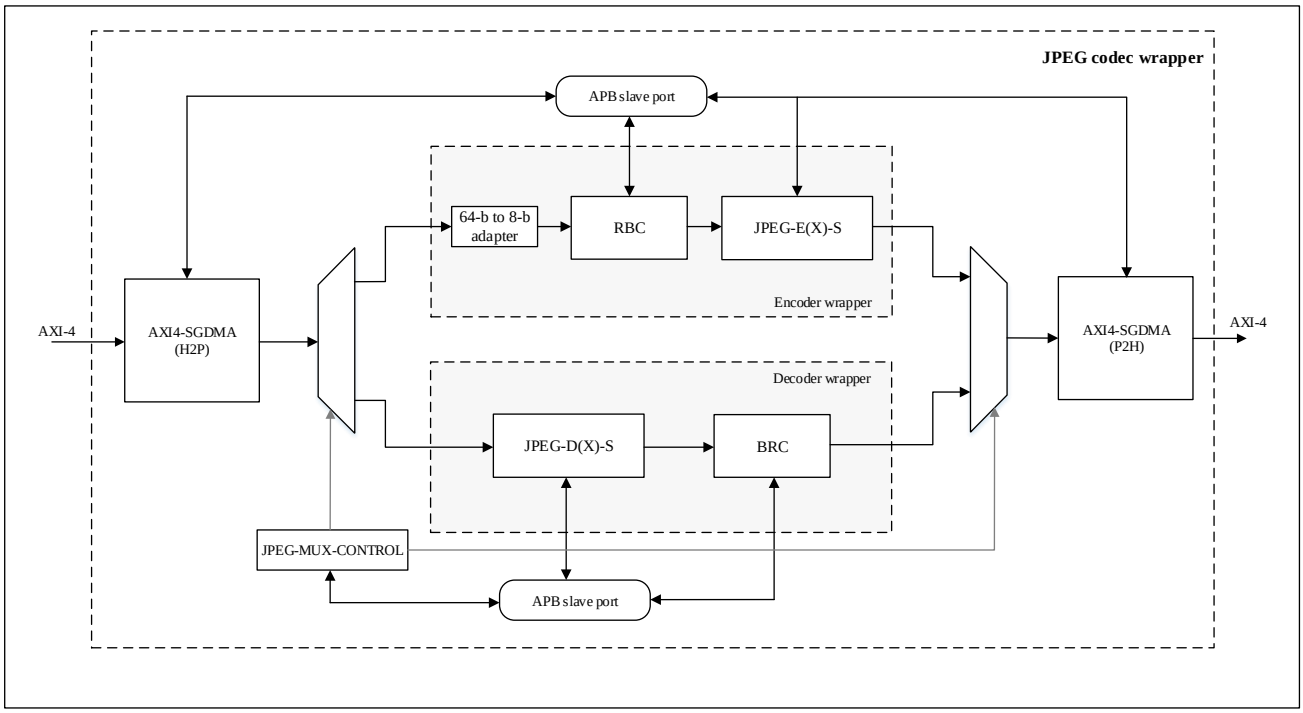
Figure 43-1 JPEG Codec wrapper architecture



- **H2P** (Host-to-Peripheral): H2P is used to connect AXI to RBC and DEC (decoder), RBC and DEC do not support memory mapping of AXI.
- **64-b to 8-b adapter**: Converts a 64-b image AXI stream from H2P to an 8-bit input format that RBC recognizes.
- **RBC** (Raster to Block conversion): Since ENC only supports block input format, RBC is used to convert raster-formatted images (line-by-line) to block sequences accepted by ENC.
- **BRC** (Block to Raster conversion): Since the LCD controller/GPU cannot directly process block-based images without software intervention, BRC is required to convert block-based images to raster images (line-by-line) for processing in the GPU or LCDC.
- **ENC** (Encoder): The JPEG Encoder Core is an encoder core that takes raw image samples on input, encodes them using the provided Hoffman and quantization tables, and outputs a fully compliant JPEG stream.
- **DEC** (Decoder): The JPEG Decoder Core is a decoder core that takes any standards-compliant JPEG stream as input and outputs raw image samples on its AXI interface.
- **P2H** (Peripheral to Host): P2H is used to connect AXI to BRC and ENC (Encoder), BRC and ENC do not support AXI memory mapping
- **JPEG_CTRL** (Type Control Register): Controls the execution of ENC or DEC operations.

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43.5 Function Description

43.5.1 JPEG Mux Control

This feature allow user can choose JPEG operation mode:

- Encoder (set JPEG_CTRL.TYPE register to 1'b1)
- Decoder (set JPEG_CTRL.TYPE register to 1'b0)

Also support Swap Data for YCbCr 4:2:2 Format in BRC when user set the JPEG_CTRL.SWAP register to 1'b1.

43.5.2 RBC

The role of the Raster-to-Block converter is to order incoming image samples (in a line-by-line format) into a sequence of blocks accepted by the encoder core.

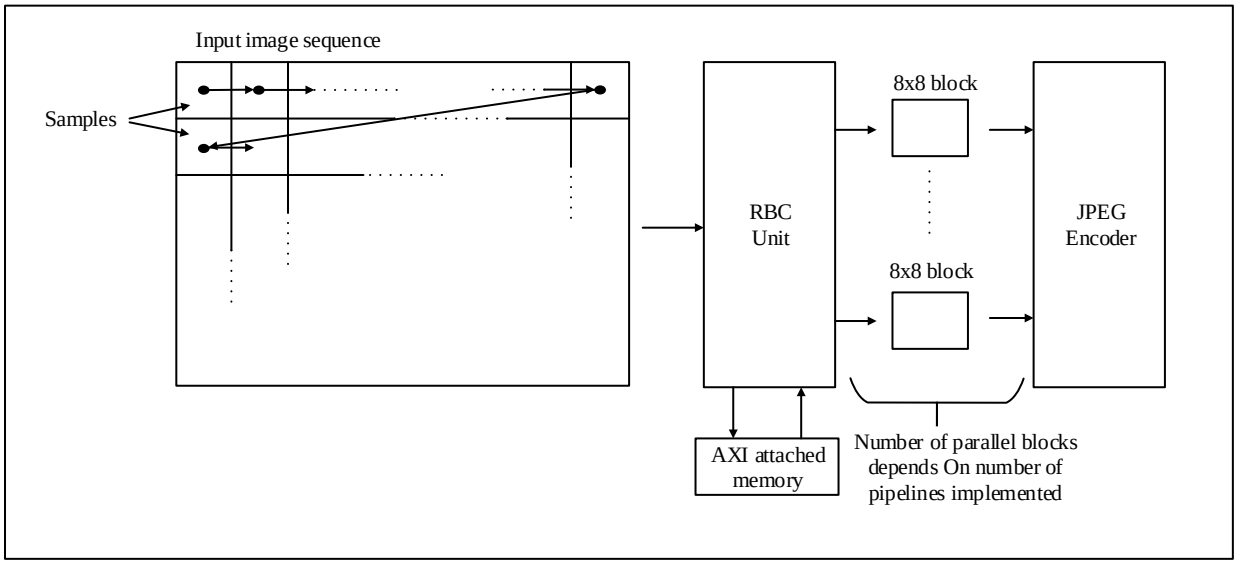
43.5.2.1 Features

- Interfaces identical to Beyond JPEG Encoder
- Block padding in accordance with JPEG (ISO/IEC 10918-1)
- Configurable image size from 16x1 to 64k x 64k (65535 x 65535)
- Supports 4:4:4, 4:2:2, 4:2:0 and monochrome input streams
- Supports both interleaved and non-interleaved input streams

43.5.2.2 Functional Overview

The Raster to Block converter (RBC) unit expects an input stream in the form of samples from left to right and line-by-line from top to bottom. The RBC unit then orders the samples into blocks and pads them as appropriate to feed directly into the JPEG encoder.

Figure 43-2 Figure showing the RBC's use in JPEG encoding



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The RBC unit requires an external AXI memory unit to operate. The external AXI memory buffer can be allocated at AXI_SRAM1-3 or AHB_SRAM1-5.

For a functional RBC unit, the user needs to complete the following steps:

1. Allocate the appropriate buffers on the AXI attached memory. For the required size of the memory for the number of block lines to be stored see at 43.5.2.4 chapter.
2. Set the start of the memory space and the number of block lines to be stored
3. Set the component names
4. Set the configuration regarding the input image sizes:
    a. Frame width, Frame height and Frame height half
    b. Blocks per Scan 0 and Blocks per Scan 1,2
    c. MCU rows Scan 0 and MCU rows Scan 1,2
    d. Block line stride Scan 0 and Block line stride Scan 1,2
    e. Blocks per MCU row Scan 0 and Blocks per MCU row Scan 1,2
5. Set the input format (4:4:4, 4:2:2, 4:2:0 interleaved/non-interleaved or Monochrome)
6. Set the init JPEGRBC_INIT.INIT bit to properly load all the logic
7. Check the JPEGRBC_INIT.INITF bit to confirm that the initialization procedure has finished
8. Set the JPEGRBC_INIT.INIT bit to 0.
9. Set the JPEGRBC_EN.EN bit to start processing input samples

43.5.2.3 Input formats

The following pixel formats are supported with selectable runtimes.

- Non-interlaced format
- 4:4:4 format
- 4:2:2 format
- 4:2:0 format
- Monochrome format

Each format supports both interleaved and non-interleaved versions, with the non-interleaved format being passed to the encoder in multiple scans.

Note that the input is only reordered and sent to the encoder, no format conversion occurs.

In the following, sample 0 is the first sample submitted to the RBC unit, sample 1 is the next sample, and so on.

Figure 43-3 input sample ordering

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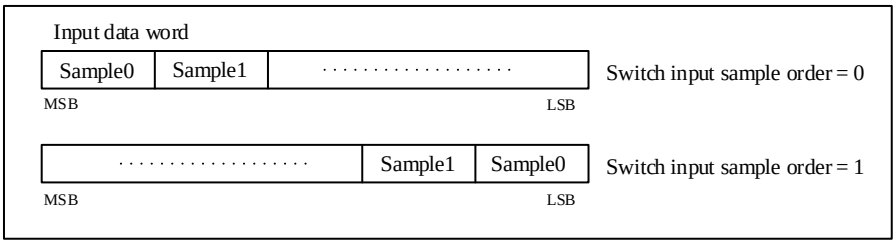

In the sample format descriptions below, the samples are denoted in the format $Y_{x,y}$, $Cb_{x,y}$ and $Cr_{x,y}$ for the Luminance, Blue and Red components respectively.

Figure 43-4 Guide to naming of samples in components used in this document

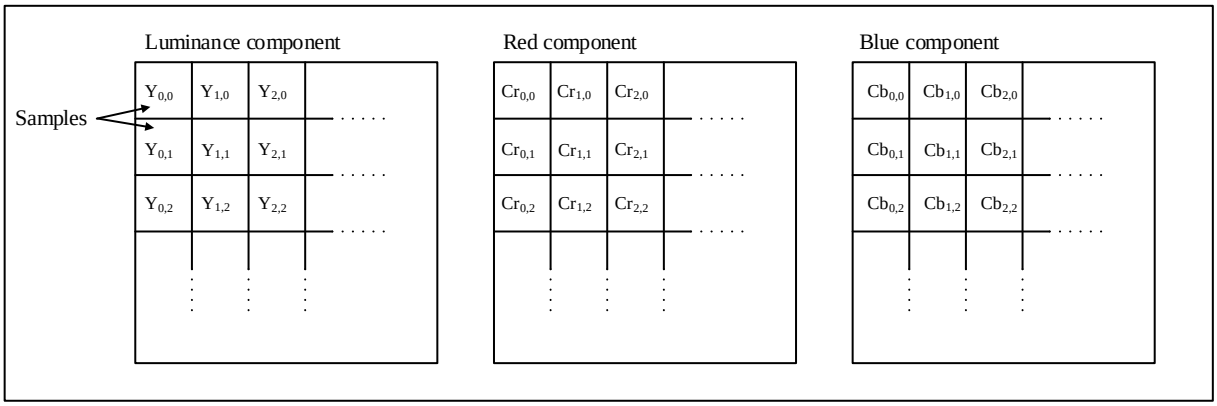

Table 43-2 Input component ordering for non-interleaved formats

Sample 0	Sample 1	…	Last Y Sample	First Cr Sample	…	…	Last Cr Sample	First Cb Sample	…	…	Last Cb Sample
$Y_{0,0}$	$Y_{1,0}$	…	$Y_{w-1,h-1}$	$Cb_{0,0}$	$Cb_{1,0}$	…	$Cb_{w-1,h-1}$	$Cr_{0,0}$	$Cr_{1,0}$	…	$Cr_{w-1,h-1}$

Table 43-3 Input component ordering for 4:4:4 interleaved format

Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	…
$Y_{0,0}$	$Cb_{0,0}$	$Cr_{0,0}$	$Y_{1,0}$	$Cb_{1,0}$	$Cr_{1,0}$	…

Table 43-4 Input component ordering for 4:2:2 interleaved format

Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	…
$Y_{0,0}$	$Y_{1,0}$	$Cb_{0,0}$	$Cr_{0,0}$	$Y_{2,0}$	$Y_{3,0}$	$Cb_{1,0}$	$Cr_{1,0}$	…

Table 43-5 Input component ordering for 4:2:0 interleaved format

Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	…
$Y_{0,0}$	$Y_{1,0}$	$Y_{0,1}$	$Y_{1,1}$	$Cb_{0,0}$	$Cr_{0,0}$	$Y_{2,0}$	$Y_{3,0}$	…

Table 43-6 Input component ordering for Monochrome interleaved format

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Sample 0	Sample 1	Sample 2	Sample 3	…
$Y_{0,0}$	$Y_{1,0}$	$Y_{2,0}$	$Y_{3,0}$	…

43.5.2.4 AXI attached memory

The raster to block conversion unit memory space is configured with the "JPEGRBC_C0SADD" and "JPEGRBC_C0EADD" registers (The address dependent on which SRAM being use… SRAM can be use like AXI_SRAM1-3, AHB_SRAM1-5). The value in the "JPEGRBC_C0EADD" register determines how many block rows of an image can be buffered inside the memory.

The start address of the buffer and of each subsequent block line in the buffer is required to start on a burst boundary. If the length of an image line is x, the number of bytes required for one buffered block line is as follows:

Table 43-7 Expressions for the "Block line Size" parameter for each supported mode

Format	Block line size
Non-interleave & mono	$\mathrm{BL}_{\mathrm{bytes}} = 64 \cdot \left\lceil \frac{x}{8} \right\rceil$
Interleave 4:4:4	$\mathrm{BL}_{\mathrm{bytes}} = 64 \cdot \left\lceil \frac{x}{8} \right\rceil \cdot 3$
Interleave 4:2:2	$\mathrm{BL}_{\mathrm{bytes}} = 64 \cdot \left\lceil \frac{x}{16} \right\rceil \cdot 4$
Interleave 4:2:0	$\mathrm{BL}_{\mathrm{bytes}} = 64 \cdot \left\lceil \frac{x}{16} \right\rceil \cdot 6$

For optimal performance, it is recommended to use 2 or more block lines.

43.5.3 Encoder

The JPEG Encoder core is an encoder core which takes raw image samples in its input, encodes it using the provided Huffman and Quantization tables and outputs a fully standards compliant JPEG stream.

43.5.3.1 Features

Baseline JPEG (ISO/IEC 10918-1) Encoder

- Single-frame jpeg images
- Programmable Huffman Tables and Quantization tables
- Up to four color components, and any image size up to 64k x 64k
- All scan configurations and all JPEG formats
- APP, COM, DNL and restart markers

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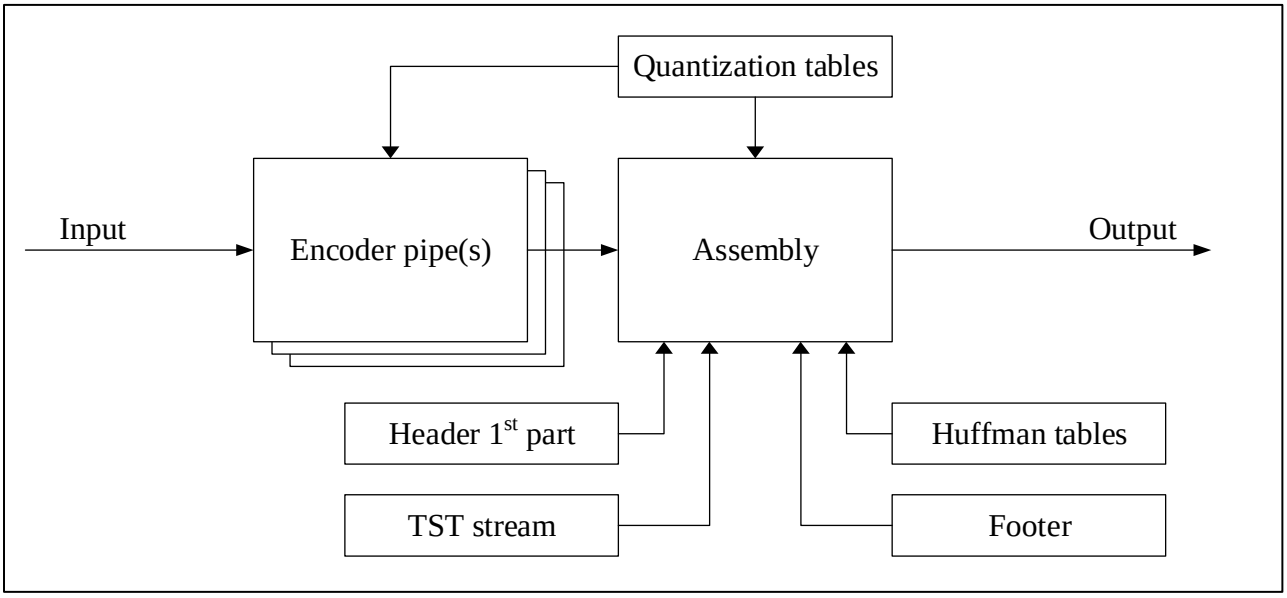
43.5.3.2 Functional Overview

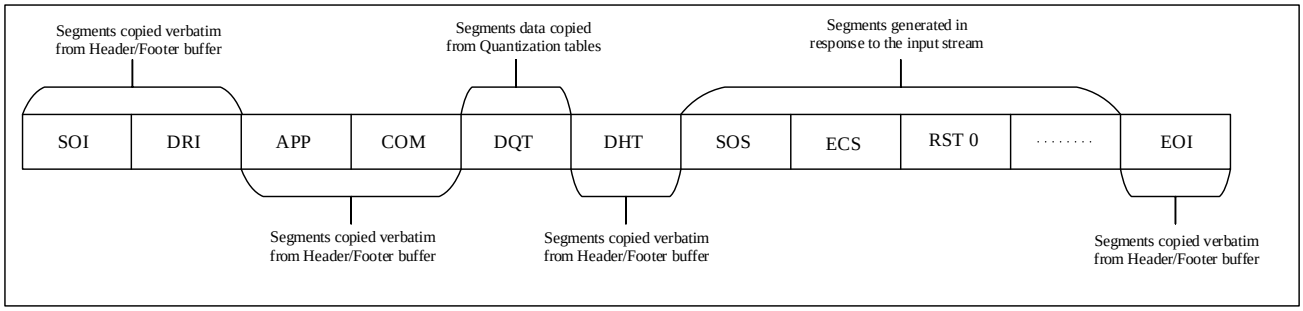
The JPEG core operates as a pipeline: raw image data is input and an encoded jpeg file is output. The block diagram is given below

Figure 43-5 JPEG encoder core block diagram



To construct the output JPEG stream the core copies marker segments from the header/footer (HDF) buffer, and completes the JPEG stream with entropy coded segments and automatically generated marker segments (see figure below).

Figure 43-6 Sequence of marker segment in output stream



For a functional encoder, the user needs to complete the following steps:

1. Upload the first portion of the header (including at least the SOI and SOF markers) to the header/footer buffer
2. Upload Quantization tables and headers
3. Upload Huffman tables and headers
4. Setup restart marker interval (if using restart markers)
5. Select Quantization tables and Huffman tables to use to encode each component and enable the core.

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43.5.3.3 Configuration

Upon reset the core first needs to be programmed with the encoding settings via the configuration interfaces. The user needs to also make sure that the Header/Footer buffer is initialized accordingly. The following table provides an outline of the contents of the Header/Footer buffer:

Table 43-8 Markers that generally appear in the Header/Footer buffer

Marker Segments	Marker	Payload	Comment
SOI	0xffd8	None	Indicates the start of an image. Must be the first marker in the header in all cases. Must be always present
SOF0	0xffc0	Variable Size	Specifies the width, height, number of components, and component subsampling. Must be always present
DHT	0xffc4	Variable Size	Specifies one or more Huffman tables. Its presence is not mandatory in a JPEG stream.
DQT	0xffdB	Variable Size	Specifies one or more quantization tables. Its presence is not mandatory in a JPEG stream.
DRI	0xffdd	4 Bytes	Specifies the Restart interval. Its presence is mandatory if the “JPEGENC_RICTRL” is set to a non-zero value.
APPn	0xffe0+n	Variable Size	Contains application-specific information. Its presence is not mandatory in a JPEG stream.
COM	0xfffe	Variable Size	Contains a text comment. Its presence is not mandatory in a JPEG stream.
EOI	0xffd9	None	Must be the last marker (footer) in all cases.

The user needs to make sure that the SOF0 marker segment (which defines the image resolution, number of components and components’ sampling format) stored in the Headers buffer is consistent with the image data format that will be input to the core.

The following table provides a quick reference to which registers need to be updated when updating various parts of the JPEG header.

Table 43-9 Connections between data in marker segments and the JPEG encoder's registers

JPEG header marker segment	Code assignment	Register
Define Huffman tables (DHT)	0xffc4	Huffman table 0-4. To calculate the register values from the header specification
Define quantization tables (DQT)	0xffdb	Quantization table 0-4.
Define restart interval (DRI)	0xffdd	JPEGENC_RICTRL register.
Start of frame (SOF_0/SOF_1)	0xffc0 or 0xffc1	The Quantization table selectors (Tqi) must match the Quantization

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		table selected in the QUAN_j field in the "JPEGENC_CTRL" register

43.5.3.4 Compressing Image

Once the core is configured, the user may start feeding samples to the core via the input stream interface. The core is able to compress an arbitrary number of images without any further actions from the user. Image samples in any color format are fed to the core in a MCU block by MCU block, raster scan order it. Correct ordering of samples at the input of the core can be facilitated by the optional Raster-To-Block-Converter (RBC) module.

43.5.3.5 Dynamic reconfiguration

The JPEG encoder provides two methods for dynamic reconfiguration of the core. If only the headers (the content of the Header/Footer buffer) are required to be changed with some application specific information (APP and/or COM markers), the 'Header reconfiguration' method may be used, otherwise the 'Full dynamic reconfiguration' method must be used (eg. To change Quantization and/or Huffman tables).

43.5.3.6 Header reconfiguration

Using this method, the Encoder core does not change its input processing characteristics (ie. it does not use any additional stall cycles), however only the Header/Footer memory may be changed.

If using a CPU to control the Encoder's reconfiguration, polled from JPEGENC_DYNRCFG.HSAFE register.

43.5.3.7 Full dynamic reconfiguration

Using this method, it is possible to reconfigure any Encoder state without any external hardware, including Quantization and Huffman tables. However, during the reconfiguration cycle, the Encoder does not accept any new input data. The procedure for full dynamic reconfiguration is as follows:

1. Set bit JPEGENC_DYNRCFG.DYNEN With this bit set, the encoder will accept all input data for the current frame and will then stall the input.
2. Wait for bit JPEGENC_DYNRCFG.DYNF to be set.
3. Update encoder configuration to the desired state
4. Clear bit JPEGENC_DYNRCFG.DYNEN
5. The encoder will now accept the next frame and continue processing.

43.5.3.8 Output Stream

The core's output is composed of various header part as specified in registers, the Entropy Coded Segments (ECS's) as output by the Encoder pipe and finally the "Footer". The complete output order is given below:

Figure 43-7 Description of the data sources for each marker segment

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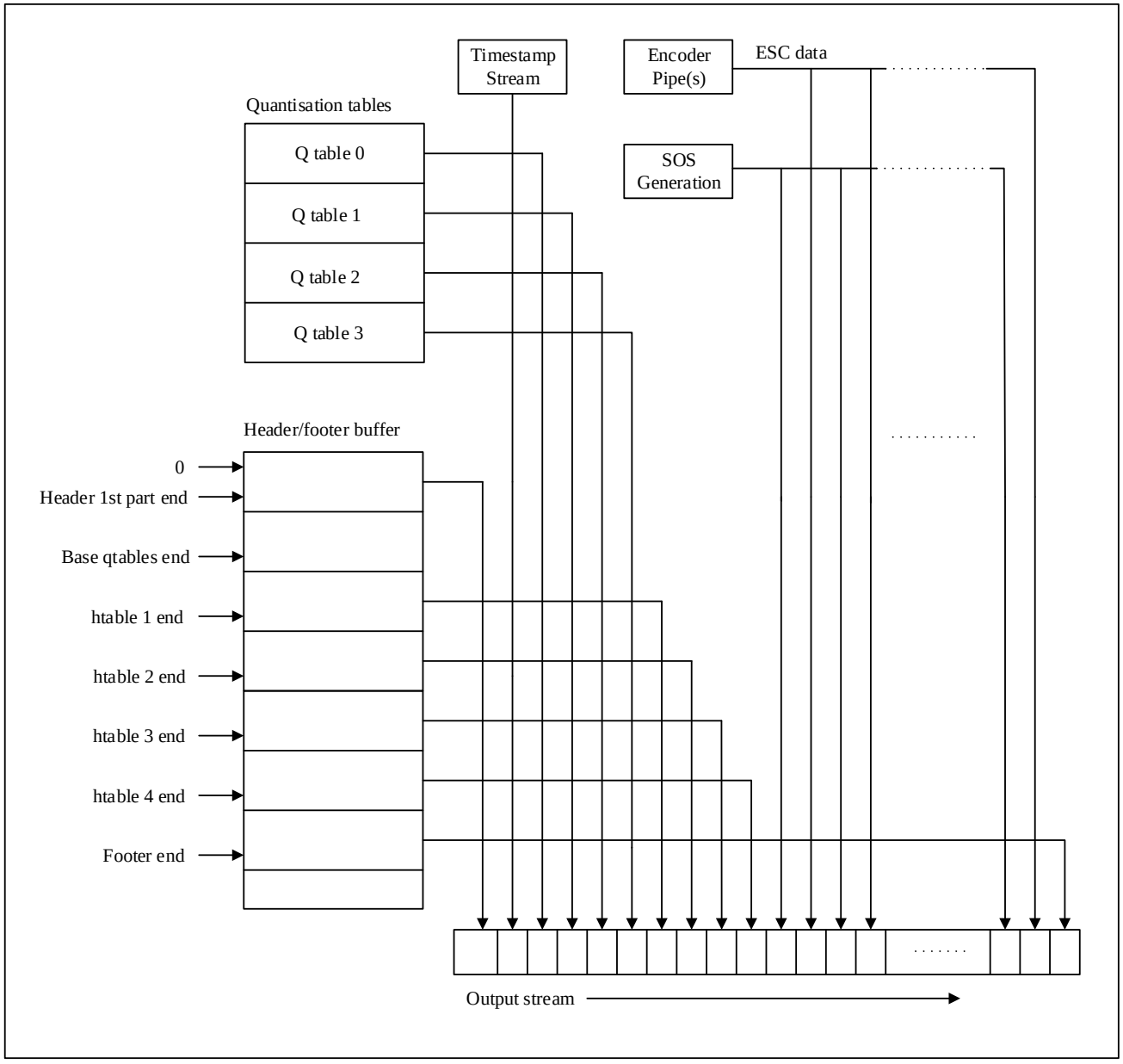

43.5.3.9 Headers

The core will assemble the output header from the "Header 1st part" and zero or more of the following portions:

1. Header 1st part
2. Quantization tables 1, 2, 3, and/or 4
3. Huffman tables 1, 2, 3, and/or 4

The Header 1st part is output first and is expected to include at least the SOI and SOF markers for a valid JPEG file on the output. The encoder provides the option to output the tables only on the next frame and not for any following frames.

43.5.3.10 Encoder pipe

After the header is output as above, the core will output the SOS marker for each scan input and then immediately

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follow the header with raw ECS data. The encoder pipe has the ability to insert restart markers at arbitrary intervals, as specified by the "JPEGENC_RICTRL" register.

Which Huffman table and Quantization table is used for each of the components defined in the "JPEGENC_CTRL".

43.5.3.11 Footer

Once the core receives the end-of-frame signal, the core will copy the footer verbatim to the output stream. It is expected that the footer ends with the End-of-Image marker

43.5.3.12 Abbreviated formats

The encoder supports output of both Abbreviated format for table-specification and compressed data. To produce "Abbreviated format for compressed data" output, the "JPEGENC_HSEL" register needs to set to all 0s. In this case, the encoder will not output any Quantization or Huffman tables in the output stream.

When using "Abbreviated format for compressed data" output:

the tables are either *(i)* pre-shared between encoder and decoder in which case no further output to the encoder is required,

(ii) sent to the decoder in non-abbreviated output including tables and ECS data,

or *(iii)* in separate "Abbreviated format for table-specification" output.

Whenever the tables are to be sent to the decoder, the user writes the "JPEGENC_HSEL" register selecting the tables they wish to send to the decoder with bit JPEGENC_HSEL.NFD set (NFD doesn't technically need to be set, however if it is not set, the encoder will produce non-abbreviated output until the user manually sets the register to 0).

If case *(iii)* above is required, bit JPEGENC_HSEL.ATF also needs to be set indicating that no ECS data is to be sent in the next frame, otherwise it must be cleared.

43.5.3.13 Throughput and Latency

Under ideal conditions while the core is processing ECS data a single input sample per implemented pipe is processed in each cycle. To reach the one sample per pipeline throughput the on the input when output is not stalled.

The latency of the encoder core is measured from the time the encoder accepts the last sample in the image to the last byte output for the frame under optimum throughput conditions. Depending on configuration, this time is between 176 and 200 cycles.

43.5.4 Decode

The JPEG Decoder core is a decoder core which takes as input any standards compliant JPEG stream and outputs raw image samples on its AXI-ST interface.

43.5.4.1 Features

Baseline JPEG (ISO/IEC 10918-1) Encoder

- Single-frame jpeg images
- Programmable Huffman Tables and Quantization tables
- Up to four color components, and any image size up to 64k x 64k

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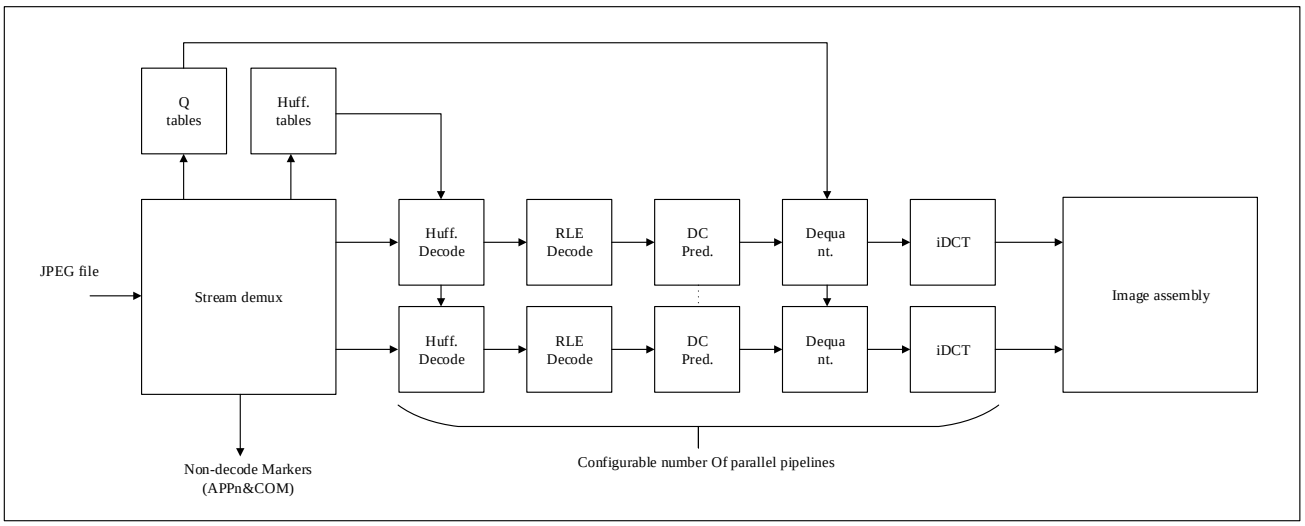
- All scan configurations and all JPEG formats
- APP, COM, DNL and restart markers

43.5.4.2 Functional Overview

The JPEG decoder core expects an input stream in the standard JPEG format and streams out the decoded image. A block diagram of the pipeline is given below.

Figure 43-8 JPEG decoder core block diagram



43.5.4.3 Markers

The JPEG decoder is able to decode the following markers present in the input stream. Any other marker is ignored and an error is signaled (for details refer to section 43.5.4.7 below).

Table 43-10 Markers interpreted by the decoder

Marker name	Value	Processing
SOF0	0xFFC0	Image parameters passed to decode pipelines
SOF1	0xFFC1	Image parameters passed to decode pipelines
DHT	0xFFC4	Huffman table data processed and stored in Huffman table buffer
RSTm	0xFFD0 through 0xFFD7	Next decode pipeline selected
SOI	0xFFD8	Preparations are made to process the following image
EOI	0xFFD9	End-of-image signal
SOS	0xFFDA	Image parameters passed to decode pipelines and encoded data decode begins.
DQT	0xFFDB	Quantization table data processed and stored in Quantization table buffer
DNL	0xFFDC	Number of lines field passed to output.
DRI	0xFFDD	Restart interval field passed to output.
APPn	0xFFE0 through 0xFFEF	Marker and marker data passed to application specific “Non-decode marker interface”

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COM	0xFFFE	Marker and marker data passed to application specific “Non-decode marker interface”

The input stream is expected to start with the SOI marker. This means that after reset and after the EOI marker, the first two bytes input to the decoder is expected to be the SOI marker. Any other bytes are ignored until the SOI marker is found. Following the SOI marker, any number of DQT, DHT, DRI, APPn, COM, SOF0 or SOF1 markers may be input, in any order. In the event that multiple SOF0/SOF1 or DHT, DQT markers writing the same table are present, the last such marker takes effect. After these markers, either the SOS marker is expected or, in the case of an abbreviated format, the EOI marker. If a SOS marker is present in the stream, failure to precede it with either a SOF0 or SOF1 header results in an error.

43.5.4.4 Abbreviated format for compressed data

If the input stream contains no table specifications or only partial table specifications (i.e. missing DHT or DQT markers), then the decoder will take the last table specification provided by any of the previous decoded images.

43.5.4.5 Abbreviated format for table-specification

If the input stream doesn’t contain the SOS marker, then all table specifications (DHT and DQT markers) will be processed and stored into the appropriate table buffers and used when followed by an abbreviated format for compressed data. In this case, no image data is output, but any COM or APPn markers present in the stream will still be output on the non-decode interface.

43.5.4.6 Limitations

The following limitations are placed on the input JPEG stream in addition to those specified in the JPEG standard.

1. The JPEG standard allows up to 255 components to be specified in the SOF marker. In this decoder, the maximum components that can be specified in the SOF marker is limited to 4. If more are specified, the first four are taken and the rest ignored. If the fifth or higher defined component is referenced by a SOS maker, bit “JPEGDEC_ERROR.CERR” is set. See section “Referencing undefined tables” below.
2. The Huffman tables as specified by the DHT markers must leave the code consisting of all ones undefined.

43.5.4.7 Error handling

The JPEG decoder strives to detect and record all errors in the input stream. Once an error has been detected, the decoder attempts to recover processing of the stream as early as possible. Each error is classified into one of the following three categories: Unknown marker, Unexpected marker or Huffman symbol error, which may be read from the “JPEGDEC_ERROR”. Once an error of a given type is detected, the error location is recorded. Until the error detected bit is set to 0 in the “JPEGDEC_ERROR”, the location registers are not updated, however recovery processing does occur. Common errors, with their recovery mechanism is given below.

43.5.4.7.1 Unknown marker error

If the decoder encounters any marker between SOI and EOI not given in Table 43-10 above, bit “JPEGDEC_ERROR.UNK” will be set and the location of the error will be recorded in the “JPEGDEC_UNLOC” register. The location of the error will be the number of bytes processed since the last SOI marker was received. Once the decoder has processed an EOI marker, the decoder will ignore all data until an SOI marker is found. Thus if there is any marker (valid or otherwise) between an EOI marker and the SOI marker, it will be ignored without any processing or error being signaled.

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The decoder does not attempt to interpret the invalid marker (ie. it will ignore the mandatory marker length field) and continue searching for the next valid marker sequence.

43.5.4.7.2 Unexpected marker error

If the decoder encounters an RSTm marker outside of scan data, it will set bit “JPEGDEC_ERROR.UNEXP” and the location of the error will be recorded in the “JPEGDEC_UELOC” register. The location of the error will be the number of bytes processed since the last SOI marker was received. If the decoder encounters a SOS marker without a preceding SOF marker since the last SOI, the unexpected marker error is also signaled.

Receiving a DNL marker when the height component in the SOF header was not zero (i.e. the number of lines was previously known) also signals an error as above and the DNL is ignored. Receiving an empty ECS (i.e. SOS or RSTm marker immediately followed by any marker) will similarly signal an unexpected marker error with its location recorded from the last SOI marker.

Incorrect ordering of RSTm markers is ignored. Any valid marker between EOI and SOI markers is ignored and is not signaled as an error. Once the unexpected marker is recorded, the decoder will continue searching for a valid marker.

43.5.4.7.3 Huffman decode error

If the decoder encounters an invalid Huffman symbol in the image, it will set bit “JPEGDEC_ERROR.HUF” and the location of the error will be recorded in the “JPEGDEC_HESYMECS” and “JPEGDEC_HUF_SELOC” registers. The “JPEGDEC_HESYMECS” is the ECS number of the error counted from the last SOI marker received while the “JPEGDEC_HUF_SELOC” holds the number of bits from the start of the ECS to the start of the invalid Huffman symbol. The Huffman symbol which is invalid is also stored in the “JPEGDEC_HESYM” register.

When an invalid Huffman symbol is found the decoder will ignore the rest of the frame (all scans) and continue processing the input when the next SOI marker is detected.

43.5.4.7.4 Too short marker segments

If a DQT, DHT or SOF marker is found that is too short, the missing bytes will be taken from the previous valid marker. For example, if a DQT marker is encountered (with 8-bit Q tables) of length 63, the last two Quantization table entries for the selected table will remain unchanged from the previous valid DQT marker. A similar situation occurs with the DHT marker. The marker segment processing ends at the defined length and searching for the next marker segment begins. In this case no error is signaled.

43.5.4.7.5 Referencing undefined components in SOS

If the SOS marker references a component name which was not defined in the preceding SOF marker, the decoder sets bit “JPEGDEC_ERROR.CERR” and proceeds to ignore the entire scan.

43.5.4.7.6 Referencing undefined tables

When invalid tables are referenced in DQT or DHT markers, the markers are silently ignored. If the table would be used (with a SOS marker), the decoder sets either bit “JPEGDEC_ERROR.QTERR” or “JPEGDEC_ERROR.HTERR” depending if an invalid Quantization table or Huffman table was referenced.

The decoder will ignore the entire scan and proceed to search for the next valid marker in the stream.

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43.5.4.7.7 Missing EOI marker

If the decoder encounters an SOI marker without a preceding EOI marker, the decoder will automatically insert the missing EOI and continue processing the SOI marker.

43.5.4.8 Pre-shared Huffman and Quantization tables

Usually the Huffman and Quantization tables are provided in the input stream and the decoder will generate its internal decode tables as appropriate. However, there may be cases when either the Huffman and/or Quantization tables are constant during the stream and are pre-shared between the encoder and decoder in the system. In this case it is not necessary to transfer the tables in the decoder's input stream, but may instead be uploaded by the user during system initialization.

Before uploading any table to the decoder, table access needs to be requested and granted by the Decoder as follows:

1. Write bit "JPEGDEC_TAB_ACCREQ.AQEQ".
2. Wait until bit JPEGDEC_TAB_ACCREQ.AOK is set to 1
3. Perform any table access required.
4. Write bit JPEGDEC_TAB_ACCREQ.AQEQ with 0

Note that during this procedure the Decoder will gracefully finish processing the current frame and will proceed to stall the input until bit JPEGDEC_TAB_ACCREQ.AQEQ is set to zero. For the Quantization tables, they are simply written to the "Quantization Table" registers (0x400-0x7ff) in zigzag order (i.e. in the same order as is specified in the DQT JPEG header).

Once the tables are calculated they are to be uploaded with the following procedure:

1. Gaining table access.
2. Set the "JPEGDEC_HUF_ADDR" register with the Huffman table number to upload
3. the AC/DC selector and the type of table to upload.
4. Write all the table entries sequentially to the "JPEGDEC_HUF_DATA" register.
5. Once the upload is complete the "JPEGDEC_HUF_REM"
6. register should be 0. If it is not, an error occurred during the upload.
7. Repeat 1-3 for all required table types
8. Write the "JPEGDEC_HUFTAB0_EOB~ JPEGDEC_HUFTAB3_EOB" register with the value of the EOB symbol.

43.5.4.9 Throughput and Latency

The throughput can generally be expected to be a single sample/cycle, however this depends on the configuration of the Huffman decoder, the input image, the quality factor used and the Huffman tables.

Assuming that restart markers are used the decoder will have the throughput of a single sample per pipe per cycle.

Processing latency is measured using an abbreviated format containing no tables (missing DQT and DHT markers), only encoded data. The number of cycles from the SOI marker entering the decoder to the first sample output is between 200 and 250 cycles.

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43.5.5 BRC

The role of the Block-to-Raster converter is to order incoming image samples from the decoder core into an easy to process line-by-line format.

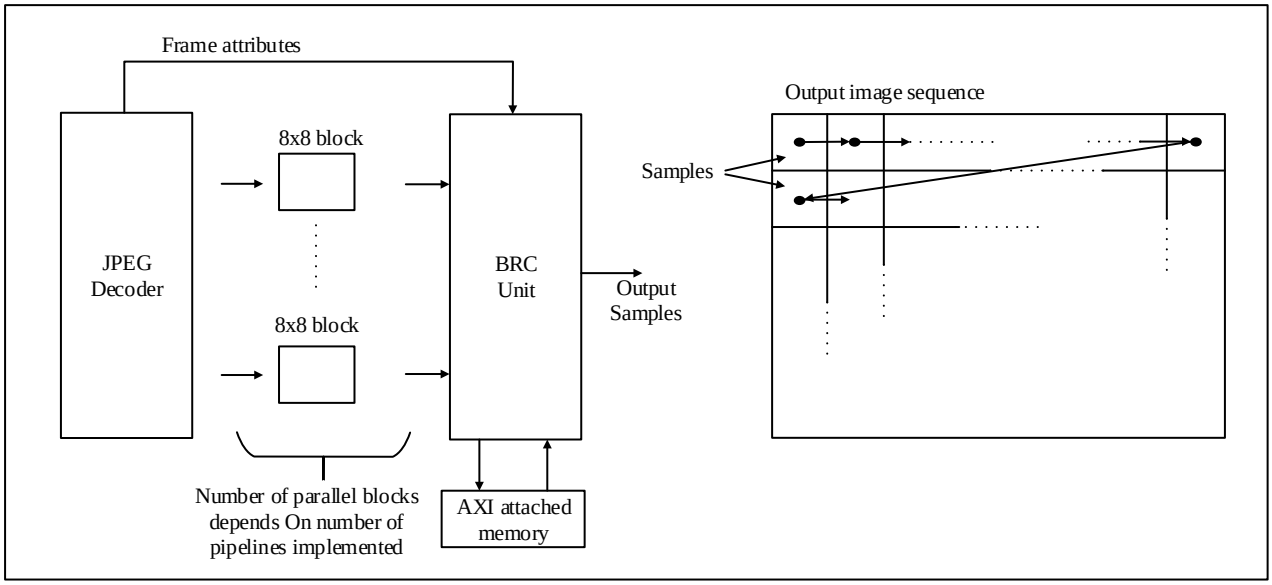
43.5.5.1 Features

- Interfaces identical to Beyond JPEG Decoder
- Block padding removal in accordance with JPEG (ISO/IEC 10918-1)
- Configurable image size from 1x1 to 64k x 64k (65535 x 65535)
- Supports 4:4:4, 4:2:2, 4:2:0 and monochrome input streams
- Supports both interleaved and non-interleaved input streams
- Dynamic, per-frame mode, width and height parameters

43.5.5.2 Functional Overview

The block to raster converter (BRC) unit expects the block output stream from the JPEG Decoder core on its input, removes any block padding and outputs the samples in raster scan order – line-by-line from top to bottom.

Figure 43-9 Figure showing the BRC's use in JPEG decoding



The BRC unit requires an external AXI memory unit to operate. The external AXI memory buffer can be allocated at AXI_SRAM1-3 or AHB_SRAM1-5.

For a functional BRC unit, the user needs to complete the following steps:

1. Allocate the appropriate buffers on the AXI attached memory. For the required size of the memory see section 43.5.5.4
2. Set the base address of the memory space and its size in a number of 8x8 blocks
3. Set the JPEGBRC_INIT.INIT bit to properly load all the logic

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4. Check the JPEGBRC_INITF bit to confirm that the initialization procedure has finished.
5. Set the JPEGBRC_INIT bit to 0.
6. Set the JPEGBRC_EN.EN bit to start processing input samples

The size and mode of the decoded image is not specified by the user, but is taken directly from the decoder, and may change from frame-to-frame.

43.5.5.3 Input formats

The core supports the following pixel formats.

- Non-interlaced format
- 4:4:4 format
- 4:2:2 format
- 4:2:0 format
- Monochrome format

The format is automatically detected based on information on the Frame Properties screen. Both interleaved and non-interleaved versions of each format are supported. In multiple scans, the decoder should provide the non-interleaved format.

Note that input from the decoder will only be reordered and no format conversion will occur.

The width of each sample is constant. In the below, Sample 0 is the first sample output from the BRC unit, Sample 1 the next, etc.

In the sample format descriptions below, the samples are denoted in the format $Y_{x,y}$, $Cb_{x,y}$ and $Cr_{x,y}$ for the Luminance, Blue and Red components respectively.

Figure 43-10 Guide to naming of samples in components

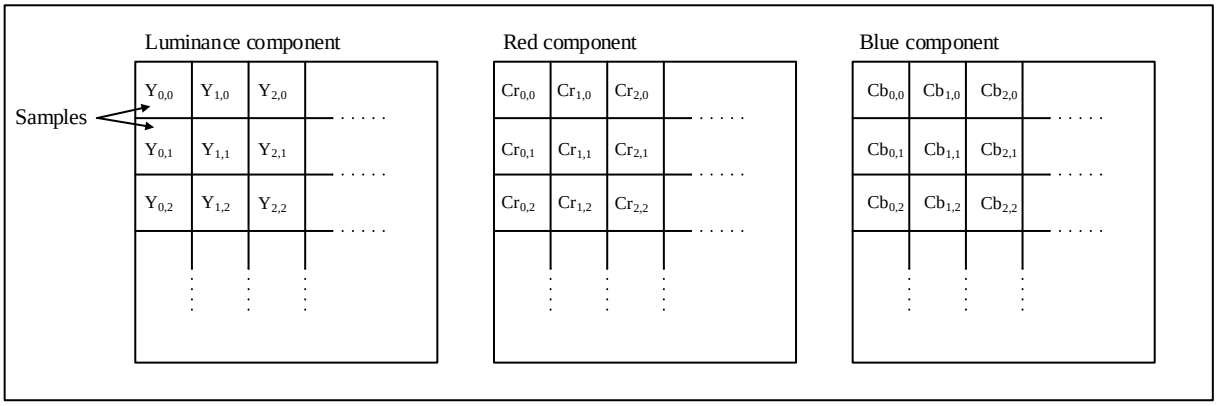

Table 43-11 Output component ordering for non-interleaved formats

Sample 0	Sample 1	…	Last Y Sample	First Cr Sample	…	…	Last Cr Sample	First Cb Sample	…	…	Last Cb Sample
$Y_{0,0}$	$Y_{1,0}$	…	$Y_{w-1,h-1}$	$Cb_{0,0}$	$Cb_{1,0}$	…	$Cb_{w-1,h-1}$	$Cr_{0,0}$	$Cr_{1,0}$	…	$Cr_{w-1,h-1}$

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Table 43-12 Output component ordering for 4:4:4 interleaved formats

Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	…
$Y_{0,0}$	$Cb_{0,0}$	$Cr_{0,0}$	$Y_{1,0}$	$Cb_{1,0}$	$Cr_{1,0}$	…

Table 43-13 Output component ordering for 4:2:2 interleaved formats

Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	…
$Y_{0,0}$	$Y_{1,0}$	$Cb_{0,0}$	$Cr_{0,0}$	$Y_{2,0}$	$Y_{3,0}$	$Cb_{1,0}$	$Cr_{1,0}$	…

Table 43-14 Output component ordering for 4:2:0 interleaved formats

Sample 0	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7	…
$Y_{0,0}$	$Y_{1,0}$	$Y_{0,1}$	$Y_{1,1}$	$Cb_{0,0}$	$Cr_{0,0}$	$Y_{2,0}$	$Y_{3,0}$	…

Table 43-15 Output component ordering for monochrome mode

Sample 0	Sample 1	Sample 2	Sample 3	…
$Y_{0,0}$	$Y_{1,0}$	$Y_{2,0}$	$Y_{3,0}$	…

43.5.5.4 AXI attached memory

The block to raster conversion unit memory buffer is configured with the "JPEGBRC_BUFBADD" and "JPEGBRC_BUFSIZE" registers. The value in the "JPEGBRC_BUFSIZE" register determines how many 8x8 blocks can be buffered inside the memory.

Each 8x8 block takes up 64 continuous samples in the AXI memory. For the core to function correctly, the buffer size needs to meet the minimum requirements listed in Table 43-16. However, note that these requirements are the absolute minimum required memory buffer for correct operation. For optimal performance it is recommended to have twice the minimum required buffer.

Table 43-16 Minimum number of bytes of memory required of correct operation

	Single pipe implemented or used
DNL support not used in input image	BMR · 64
DNL support used in input image	2 · BMR · 64

Where RI is the "Restart Interval", the value contained in the restart marker in the input image. While BMR is the number of 8x8 blocks per MCU row and BPM is the number of blocks in an MCU. The number of 8x8 blocks in an MCU for popular formats is given below together with the number of blocks in an MCU row, assuming that the width of the input image in pixels is x.

Table 43-17 Examples on how to calculate the number of blocks per MCU and the number of MCUs per row for the standard 4:4:4, 4:2:2 and 4:2:0 formats

Format	**8x8 Blocks per MCU**	**8x8 Block in an MCU Row**

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Non-interleave & mono	BPM = 1	$\mathrm{BMR} = \left\lceil \frac{x}{8} \right\rceil$
Interleave 4:4:4	BPM = 1	$\mathrm{BMR} = 3 \cdot \left\lceil \frac{x}{8} \right\rceil$
Interleave 4:2:2	BPM = 1	$\mathrm{BMR} = 4 \cdot \left\lceil \frac{x}{16} \right\rceil$
Interleave 4:2:0	BPM = 1	$\mathrm{BMR} = 6 \cdot \left\lceil \frac{x}{16} \right\rceil$

43.5.5.5 Up sampling modes

The BRC supports primitive up sampling modes where input subsampling modes are transformed to other modes. The up sampler simply repeats appropriate samples to achieve the target mode. The table below gives the transformation applied to the input stream for each of the up sampling modes. The up sampling mode is set in the register "JPEGBRC_USMODE".

Table 43-18 Up sampling modes supported by BRC core

Input mode	Output mode			
	Up sampling mode = 0	**Up sampling mode = 1**	**Up sampling mode = 2**	**Up sampling mode = 3**
4:4:4 Interleaved	4:4:4 Interleaved	4:4:4 Interleaved	4:4:4 Interleaved	4:4:4 Interleaved
4:2:2 Interleaved	4:2:2 Interleaved	4:2:2 Interleaved	4:4:4 Interleaved	4:4:4 Interleaved
4:2:0 Interleaved	4:2:0 Interleaved	4:2:2 Interleaved	4:2:0 Interleaved	4:4:4 Interleaved
All others	Same as the input	Same as the input	Same as the input	Same as the input

43.5.6 SGDMA

The AXI4-SGDMA Core is a Host-to-Peripheral (H2P), or Peripheral-to-Host (P2H) Direct Memory Access (DMA) engine, which interfaces the host system with an AXI4 Memory-Mapped master port and the peripheral with either a slave or a master AXI4-Stream port. The Core includes scatter-gather support, as well as a multi-channel implementation to support larger numbers of peripheral devices. Each channel is designed as a standalone component, complete with its own set of AXI4 interfaces for communication with the host and peripheral, as well as its Control-Status Registers. For a multi-channel implementation, an AXI4 crossbar and arbiter shall be added by the user to multiplex and prioritize host memory accesses. Finally, a wide array of user-configurable parameters allow for customization of various aspects of the Core, including bus and address widths, support for unaligned memory access, mode of operation and descriptor size.

43.5.6.1 Features

- Standalone Host-to-Peripheral and Peripheral-to-Host DMA channel modules
- Independent instantiation and functionality of the DMA channels
- Multi-channel implementation in the user design via an external multiplexer and arbiter
- Scatter-gather operation support.
- Descriptors are programmed from memory as well as through the CSR Registers.

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- End-of- File detection and reporting both for read and write operations. The descriptor updates in the write case.
- Unaligned host memory address access support.
- Control and status report through the CSR Register interface.
- Configurable interrupts.
- Support of a wide array of data bus widths:
  1. 32 - 1024 bits for data access to the host memory.
  2. 32 - 1024 bits stream interfaces to/from the peripheral devices.
  3. 32,64 bits for AXI4 Memory-Mapped address channels.
- AXI4 Memory-Mapped interfaces support both FIXED and INCREMENTING bursts.

43.5.6.2 Block Diagrams

Figure 43-11 H2P Channel Block Diagram

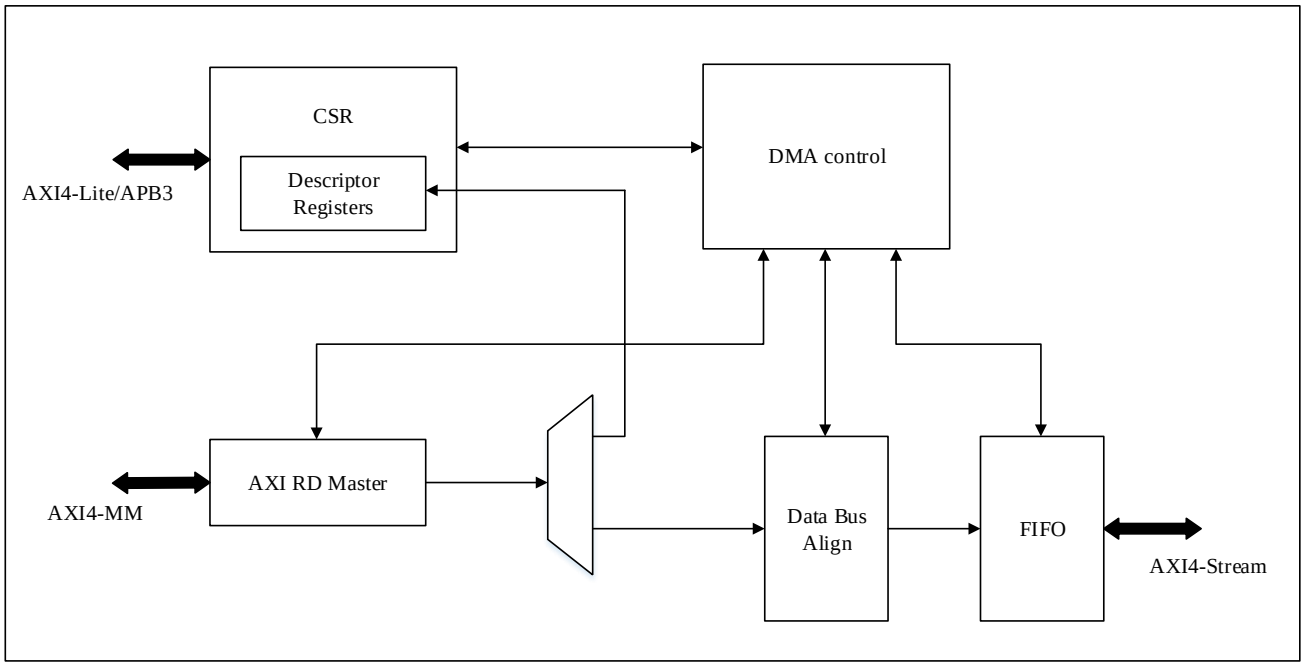

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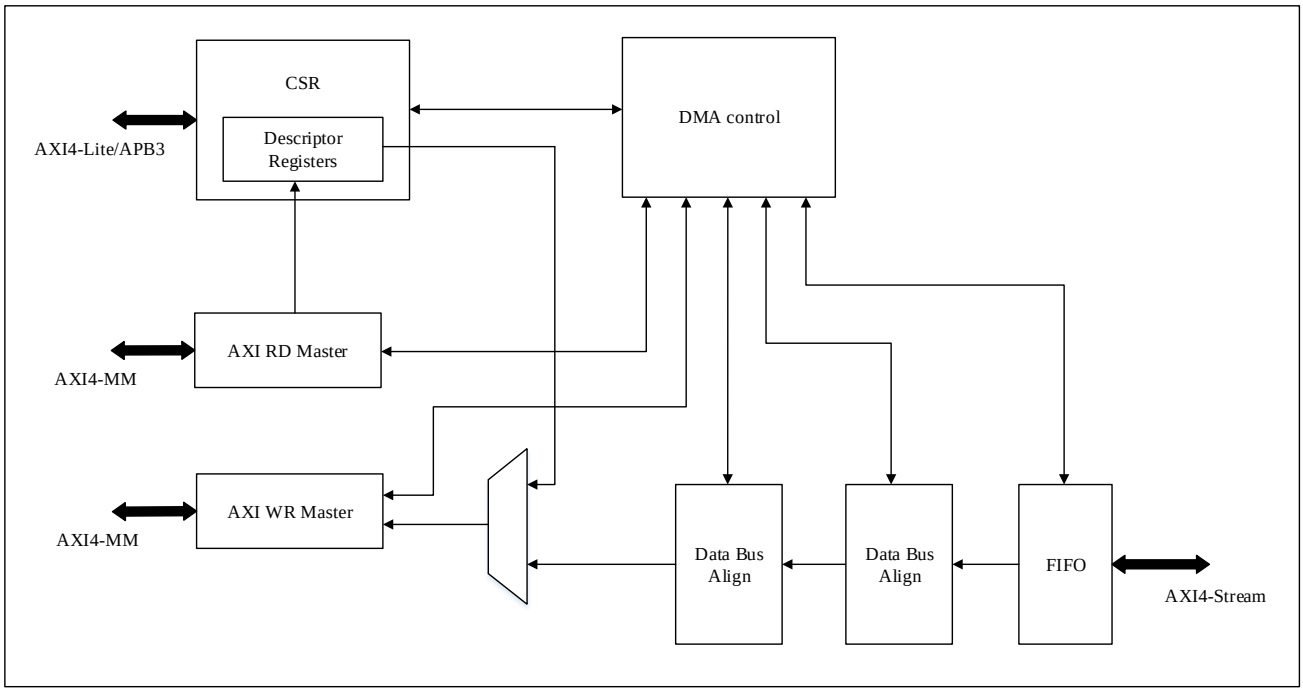
Figure 43-12 P2H Channel Block Diagram



43.5.6.3 Block Descriptions

The Scatter-Gather DMA core channels are structured as shown in Figure 43-11 and Figure 43-12 and are explained below.

43.5.6.3.1 AXI Scatter-Gather DMA Channel Top-Level Entities

Figure 43-11 and Figure 43-12 illustrate the top-level block diagrams of the AXI4-SGDMA Core's separate channels. The channels are separated into two different categories. The Host-to-Peripheral (H2P) Channel reads data from the host memory and transmits them to the peripheral, while the Peripheral-to-Host facilitates incoming transaction from the peripheral to the host memory.

Each channel is completely independent of all others, allowing for the instantiation of a greater number of highly configurable channels within the same DMA Core. All channels are comprised of their standardized AXI4 interfaces, Descriptor and Data buffers, CSR modules and control logic.

The channel also employs a simple AXI4 Stream interface to communicate with the peripheral. In the case of the H2P Channel, this interface is configured as a master interface, initiating transactions with the peripheral, while in the case of the P2H Channel the AXI4 Stream interface is configured as a slave, receiving incoming transactions from the peripheral. Finally, an AXI4 Memory-Mapped master is deployed to access the host memory directly for each channel. The AXI4 MM facilitates the transactions required to fetch both the Descriptors assigned to each channel, as well as the data they point to. In the case of the H2P Channel, the address and data write channels of the AXI4 MM interface are omitted since no write operations to the host memory are required. The Channel will simply increment the Descriptor address once the Descriptor is consumed to alert the host that the slot may be overwritten.

Both channel types utilize a set of Descriptor Registers used to store the current descriptor locally, a Data Bus Alignment module tasked with aligning the data to unaligned addresses at the host memory, as well as a data FIFO used for internal buffering if data with additional logic capable of converting the word size between the AXI4 MM

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and AXI4-Stream bus widths. The P2H Channel utilizes an additional smaller Data Buffer to collect full AXI4 MM bursts before issuing a write transaction.

Finally, each channel utilizes its own DMA Control module to synchronize and control the transactions made by the channel. The Control module communicates both with the CSR to ensure the correct operation of the Channel, as defined by the parameters set by the user, as well as with the Descriptor Registers to provide the correct Descriptor and Data addresses to the AXI4 MM interface. The DMA Control module is elaborated further in Section DMA Control

43.5.6.3.2 Control and Status Register (CSR)

The CSR module contains the control registers JPEGDMA_CTRL and status registers JPEGDMA_STS. These registers have a complex structure, which is described in Section SGDMA Registers. Host access to the CSR is facilitated through the AXI4-Lite configuration interface.

43.5.6.3.3 Data Bus Alignment Module

The AXI4-SGDMA Core implements a Data Bus Alignment module to account for unaligned access to the host memory through the AXI4 Memory-Mapped interface. The Alignment module utilizes two Barrel Shifter modules to facilitate the correct alignment of words depending on the initial address offset of the data block, as well as the size of the last word for each descriptor.

The Barrel Shifters are controlled by the FSM described in Figure 43-13, while its states are explained in Table 43-19. The Alignment module produces blocks of data that do not contain any gaps, except for the final word of the frame. In that case, a strobe signal is set to signify the valid bytes in the word. Remaining data from a Descriptor which do not occupy the full width of the word are stored internally and combined with the next data block that is input to the Core.

The data bus alignment module is an optional feature allowing to fully support unaligned accesses to the memory through the AXI4 Memory-Mapped interface. The module may be excluded from the design by setting the JPEGDMA_PARACFG.ALIGNEN synthesis parameter to zero. In case the data bus alignment module is not included, the user must ensure that all accesses to and from the AXI4 Memory-Mapped interface are aligned to the interface's data channel width. This applies to both the starting address of the data block of each Descriptor, as well as the overall size of the block. The only exception to this rule is the last word of a data block marked as the EOF, where data strobes are used to designate the valid data bytes. Failure to adhere to these requirements will produce incorrect results.

Table 43-19 Data Bus Alignment FSM States

State	Description
IDLE	No operation is performed. All control and data bits are deasserted.
NEW_FRAME	The next word that is received by the Alignment module belongs to a new frame. Only the address offset is taken into account.
NEW_DESCRIPTOR	The next input word belongs to a new descriptor. Address offset must be factored in the calculation of the number of bytes the word needs to be shifted by.
PROCESSING	Normal operation. Words are shifted by a static number of bytes in this state.

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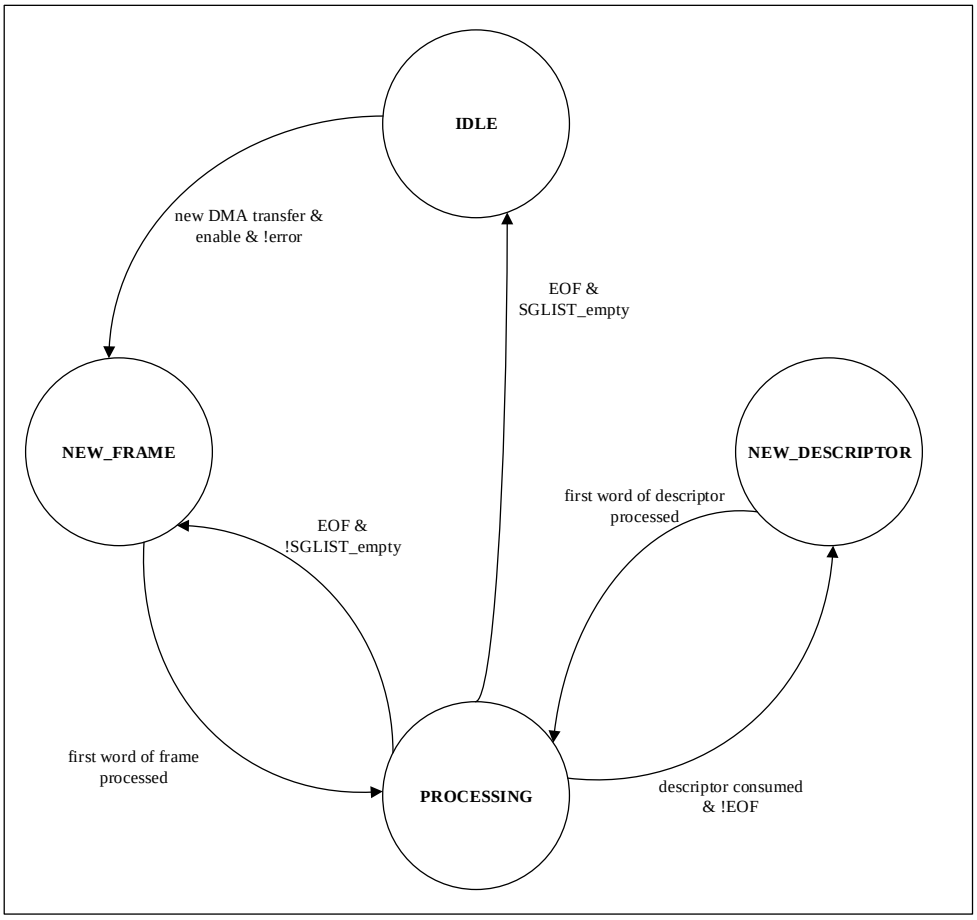
Figure 43-13 Data Bus Alignment FSM



43.5.6.3.4 Data FIFO and AXI4 Stream Peripheral Interfaces

The AXI4-SGDMA Core utilizes a data FIFO to buffer the data transmitted through each channel. The FIFO stores all transmitted data, along with the corresponding _keep and _strb utility signals and the _tlast flag, denoting an EOF to/from the peripheral. In addition, internal logic is implemented in the Data FIFO to account for different bus widths between the AXI4 Stream and AXI4 Memory-Mapped interfaces. In both channel types, this logic is implemented in the output of the FIFO to avoid stalls when receiving new data.

In the H2P Channel, the data FIFO is located before the AXI4 Stream master interface. Writes to the FIFO are performed when the Data Bus Alignment module has aligned words ready to be transferred through the AXI4 stream output interface. Reads from the FIFO are performed only by the AXI4 Stream interface tasked with providing data to the peripheral. Using this method, data are transmitted as soon as they are available and the peripheral's slave interface is ready to receive them.

In the P2H Channel, the data FIFO is located after the AXI4 Stream slave interface. Writes to the FIFO are performed exclusively by the AXI4 Stream slave. The slave interface asserts its ready signal as long as the FIFO can hold more data and no blocking interrupts are active. Reads from the FIFO are performed by the Data Bus Alignment module once the DMA Control module has provided a valid descriptor so that each word is aligned correctly to the correct memory address. Data received through the AXI4-Stream interface must always be aligned to the bus width of the interface.

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43.5.6.3.5 Data Buffer

The Data Buffer is a feature specific to the Peripheral-to-Host DMA Channel. It functions as a way to accumulate a complete aligned AXI4 burst before issuing a write transaction in the address write channel of the Memory-Mapped interface. The size of the buffer is equal to the maximum burst size of the AXI4 Memory-Mapped interface. Two burst size counters are implemented internally to account for transfers that are smaller than the maximum burst length, either due to an EOF or due to a transfer crossing the 4 KB page boundary. It is the job of the DMA Control module to alter the burst length of the next AXI4 transaction in each case.

Furthermore, a couple of word counters is implemented on the output of the buffer to track the remaining words of the current burst. Utilizing two such counters allow for two AXI4 transactions to be pending at any moment, thus alleviating the overhead of an address write access between two consequent data write accesses.

43.5.6.3.6 DMA Control

The DMA Control module provides the central control for each DMA Channel. There are two variations of the control module, specific to the H2P and P2H Channels respectively. This section details the behavior of the DMA Control units under specific events, as well as the FSMs driving the execution stages of the transfers.

43.5.6.3.6.1 Enable/CLR Behavior

To ensure uninterrupted and predictable behavior from the AXI4-SGDMA Core's FSMs the software enable signal (JPEGDMA_CTRL.EN) follows the following principles.

Software enable functionality is limited to the end of a full cycle from the FSM. A channel pause by the host is only possible after the current descriptor is consumed This ensures that no AXI4 violations occur during the pause of the channel. The DMA Control always checks whether the software enable is low before serving the new Descriptor. If this condition is met, the FSM defaults to its IDLE state. Asserting the enable signal and issuing a start pulse will force the Channel to resume operation.

Software clear (JPEGDMA_CTRL.CLR) may be asserted at any time during the core's operation. The CLR performs a synchronous soft reset of the core, flushing all storage elements and setting the FSMs to their IDLE states. It is the host's responsibility to decide the correct time to assert the CLR signal to avoid any AXI protocol violations.

43.5.6.3.6.2 Blocking/Non-blocking Interrupts

The AXI4-SGDMA Core utilizes a mixed set of blocking and non-blocking interrupts. Blocking interrupts halt the operation of the Core and require user action before resuming, while non-blocking interrupts serve a more informative functionality and the Core continues operating normally when they are set. Specific interrupts act as blocking or non-blocking depending on the Core configuration.

AOOD and EOD are always non-blocking interrupts, as they simply provide the host with information regarding the execution flow of the Core.

OOD is always a blocking interrupt since the Core is not able to resume operation without a new set of Descriptors. The same applies to non-recoverable errors. More information concerning error handling may be found in Section 43.5.6.3.6.3

EOFIN and EOFOUT may be configured as blocking or non-blocking interrupts. Not setting bit 0 of the JPEGDMA_CTRL.OPMODE[2:0] field forces the Core to consider them as blocking interrupts. When set EOFIN blocks the input of the Core from receiving new data until the interrupts are cleared without halting the entire

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Email: sales@nsing.com.sg

operation of the Core. When EOFOUT is set, the Core does not produce valid data at its output until the interrupt is cleared. If JPEGDMA_CTRL.OPMODE[2:0] bit 0 is high, both interrupts become non-blocking and the Core resumes execution immediately after they are set.

43.5.6.3.6.3 Error Handling

The following table lists all possible errors the DMA Control is configured to intercept and the actions needed for their resolution.

Fatal errors require a hard or soft reset as the normal operation of the core is not recoverable. A fatal error results in all state machines and interfaces being disabled. The state machines remain in their IDLE state awaiting a reset.

Both H2P and P2H channels complete all outstanding transfers issued through the AXI4 Memory-Mapped interface prior to deactivating the Core and writing the error to the CSR. After an error occurs, the AXI4 Stream interfaces will not accept or produce any data. If an AXI4 Stream transfer was already issued, the Peripheral AXI4 Stream interface should also be reset.

In the event of AXI4 bus errors data integrity cannot be guaranteed and the Core should be reset and reinitialized with the correct configuration to restart or resume data transfers.

Table 43-20 Error Types

Error Type	Severity	Resolution
AXI rd error for descriptor	Fatal	AXI read descriptor transaction failed. Hard/soft reset required.
AXI wr error for descriptor	Fatal	AXI write descriptor transaction failed. Hard/soft reset required.
AXI rd error for data	Fatal	AXI read data transaction failed. Hard/soft reset required.
AXI wr error for data	Fatal	AXI write data transaction failed. Hard/soft reset required.

43.5.6.3.6.4 AXI4 Address Alignment

The AXI4-SGDMA Core optionally supports unaligned incrementing data bursts through the JPEGDMA_PARACFG.ALIGNEN synthesis parameter.

The Core, however, does not support unaligned accesses for Descriptor read from the memory. Each Descriptor address should be aligned to the AXI4 Memory-Mapped data bus.

Similarly, all AXI4 fixed bursts should be aligned to the AXI4 Memory-Mapped data bus, since the address remains fixed for the entirety of the burst.

43.5.6.3.6.5 H2P Control FSM

The H2P Control FSM controls the read accesses performed by the Channel to the host memory. The states of the FSM can be seen in Table 43-21. The Control module starts a DMA operation by reading and decoding a descriptor. In the case the descriptors reside in host memory, DMA Control initiates an AXI4 read transaction to fetch the descriptors from the host memory. One descriptor is read at a time. In the cases of a preprogrammed descriptor or descriptors programmed through the CSR, DMA Control looks to the corresponding locations to receive the descriptor.

Once the descriptor is successfully read and decoded, the FSM starts facilitating the data transfers from the host memory to the local data FIFO. The size of the AXI4 burst is calculated based on the JPEGDMA_MBSIZE and the

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Email: sales@nsing.com.sg

JPEGDMA_DESC_MBSIZE descriptor field. After preparing the burst and If there is enough space in the data FIFO to accommodate the full burst, then the AXI4 burst is issued, else the Control waits for the FIFO to be decongested.

After each transaction is successfully issued, the Control either calculates the next one, or proceeds to consume the descriptor. The latter is the case when the total size of the transmitted data is equal to the JPEGDMA_DESC_MBSIZE descriptor parameter. In the H2P Channel, the consumption of a descriptor results simply in the increment of the SGList TAIL pointer by one, since the Descriptor does not hold any relevant information for the host at this point and therefore a memory access operation would be unnecessary. Note here that in case the JPEGDMA_CTRL.MMODE[1] = 0 implies the use of a simple List and the descriptor is consumed leaving the SGList empty, the TAIL pointer is reset to point to the first element of the list instead of being incremented during the INITIALIZATION state.

After the descriptor is consumed the FSM transitions to either the DESCRIPTOR_RD_RQ state when accessing descriptors through the host memory, READ_DESCRIPTOR state when accessing descriptors through the CSR, or the IDLE state. If the descriptor was consumed due to an EOF and the JPEGDMA_CTRL.OPMODE[2:0] of the channel is set so that the core should pause on an EOF, or if JPEGDMA_CTRL.EN is de-asserted, the FSM remains in the IDLE state. Once the interrupts are cleared, the JPEGDMA_CTRL.EN signal is active and a START pulse is received, the FSM continues its normal operation. Otherwise, if the SGList is empty after the descriptor is consumed, the FSM waits for the host to provide more descriptors and subsequently transitions to the INITIALIZATION state to process the new list. If there are still available descriptors when the previous one is consumed, then the FSM proceeds with processing them as normal.

Table 43-21 H2P Control FSM States

State	Description
IDLE	No operation is performed. All control and data bits are de-asserted.
INITIALIZATION	Initialize controls with the location of the first descriptor in the SG List.
DESCRIPTOR_RD_RQ	Issue an AXI read address channel transaction for the next descriptor. The location of the descriptor depends on the type of the previous descriptor (normal or link).
READ_DESCRIPTOR	Receive the descriptor from the AXI read data channel or CSR and store it in the descriptor registers.
DECODE_DESCRIPTOR	Verify descriptor integrity and set counters and addresses for data transfer to the appropriate values.
PREPARE_NEXT_BURST	Prepare the next AXI read burst depending on data FIFO occupancy, the JPEGDMA_MBSIZE and JPEGDMA_DESC_MBSIZE parameters.
DATA_RD_RQ	Issue a transaction for the AXI AR channel.
CONSUME_DESCRIPTOR	Increment TAIL pointer.

43.5.6.3.6.6 P2H Control FSM

The P2H Control FSM controls the write accesses performed by the Channel to the host memory. The states of the FSM can be seen in Table 43-22. The descriptor read and decode states operate identically to the H2P Channel FSM's corresponding states.

Once a valid descriptor is selected the FSM communicates the address offset and size of the data block inferred by it to the Data Bus Alignment module so that incoming data may be aligned to the data address correctly. It, subsequently, evaluates the availability of data in the Data Buffer and calculates the burst size based on the descriptor's

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JPEGDMA_MBSIZE, JPEGDMA_DESC_MBSIZE, and the EOF flag. When the appropriate size of data is available based on those criteria, an AXI4 write burst is issued to store the data in the host memory. This process is repeated until the allocated space tied to the descriptor is filled or an EOF is seen in the AXI4 Stream slave interface

When the data transactions are complete the Descriptor is consumed. This translates to updating the JPEGDMA_DESC_MUS field of the descriptor with the correct value, when an EOF occurs, and updating the JPEGDMA_DESCF. The Descriptor Consumed flag is set on all cases, while the EOF flag is set in case the descriptor is consumed due to receiving an EOF from the peripheral interface. The FSM then issues a write transaction to the AXI4 MM interface or overwrites the respective CSR fields to update the descriptor with the new values before incrementing the SGList TAIL pointer by one. Note here that in case the J JPEGDMA_CTRL.MMODE[1] = 0 implies the use of a simple List and after the consumption of a descriptor the SGList is empty, the TAIL pointer is reset to point to the first element of the list instead of being incremented.

After the descriptor is consumed, the DMA Control FSM transitions to either the DESCRIPTOR_RD_RQ, READ_DESCRIPTOR, or IDLE state. The state transition conditions for each case are identical to the H2P FSM.

Table 43-22 P2H Control FSM States

State	Description
IDLE	No operation is performed. All control and data bits are de-asserted.
INITIALIZATION	Initialize controls with the location of the first descriptor in the SG List.
DESCRIPTOR_RD_RQ	Issue an AXI read address channel transaction for the next descriptor. The location of the descriptor depends on the type of the previous descriptor (normal or link).
READ_DESCRIPTOR	Receive the descriptor from the AXI read data channel or CSR and store it in the descriptor registers.
DECODE_DESCRIPTOR	Verify descriptor integrity and set counters and addresses for data transfer to the appropriate values.
PREPARE_NEXT_BURST	Check for available data in the Data Buffer. If the amount of data present in the Buffer satisfy the JPEGDMA_MBSIZE and JPEGDMA_DESC_MBSIZE, or an EOF is seen, prepare the AXI burst according to those limitations.
DATA_WR_RQ	Request a memory write access from the AXI4 MM interface at the address the descriptor points to and with the appropriate burst size.
CONSUME_DESCRIPTOR	Update the JPEGDMA_DESCF Descriptor_Consumed field. If the descriptor is consumed due to an EOF, update the JPEGDMA_DESC_MUS value and the EOF flag. If the descriptor resides in the CSR, update the CSR Registers. Increment the TAIL pointer.
DESCRIPTOR_WR_RQ	Issue an AXI MM write transaction to write the updated descriptor to the host memory. If the transaction fails reissue the transaction.
WAIT_DESC_BURST_DONE	Wait for the data write transfer of the descriptor to complete.

43.5.6.4 AXI RD/WR Channel Control FSMs

The AXI data channels are controlled independently of the main DMA Control modules. The counts of the outstanding transactions are kept for each direction to synchronize the AXI RD and AXI WR FSMs with the H2P/P2H Control FSMs. When a transaction is performed in each of the address channels of the AXI interface, the corresponding outstanding transaction count is incremented. The count is decremented once the _last signal is

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asserted on the corresponding data channel.

The WR Channel Control FSM module is split into two smaller FSMs, controlling the write data and data response channel respectively. Using separate FSMs ensures that the latency of the write response does not affect the throughput of the write data channel. All FSMs utilize an IDLE state that is accessed when there are no more transactions issued for the interface. The core, if the JPEGDMA_CTRL.EN register is set and no error has occurred, transitions to a data transfer state in order to provide or receive data from the interface, depending on the channel's direction. Note that the FSM also takes into account the data FIFOs ready/valid signals to decide the value of the AXI's rready and wvalid signals.

Table 43-23 AXI RD Channel Control FSM States

State	Description
IDLE	No operation is performed. All control and data bits are de-asserted.
READ_DATA	A read transaction has been issued and the interface must be ready to receive the data transfers.

Table 43-24 AXI WR Data Channel Control FSM States

State	Description
IDLE	No operation is performed. All control and data bits are de-asserted.
WRITE_DATA	A write transaction has been issued and the interface must be ready to provide the data for the transfers.

Table 43-25 AXI WR Response Channel Control FSM States

State	Description
IDLE	No operation is performed. All control and data bits are de-asserted.
WR_RESP	Receive the writes response for the completed burst.

Figure 43-14 State transitions for AXI RD channel Control FSM

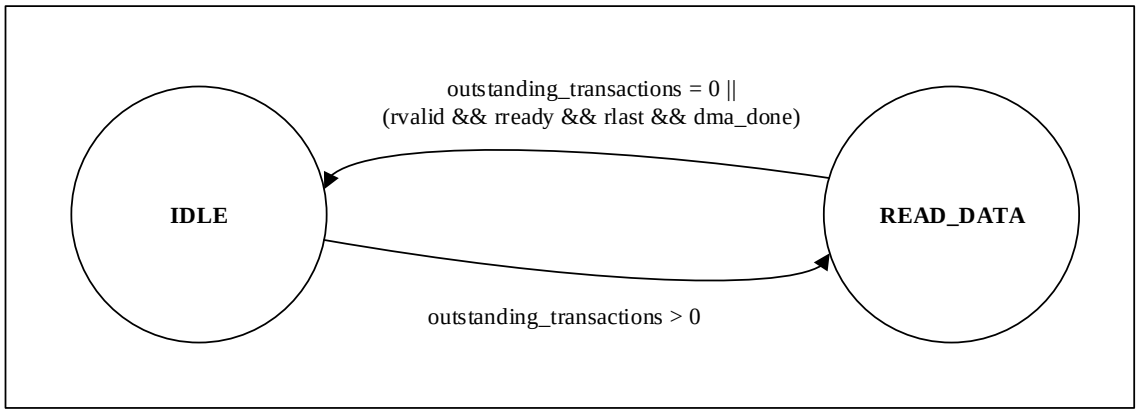

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Figure 43-15 State transitions for AXI WR Data channel Control FSM

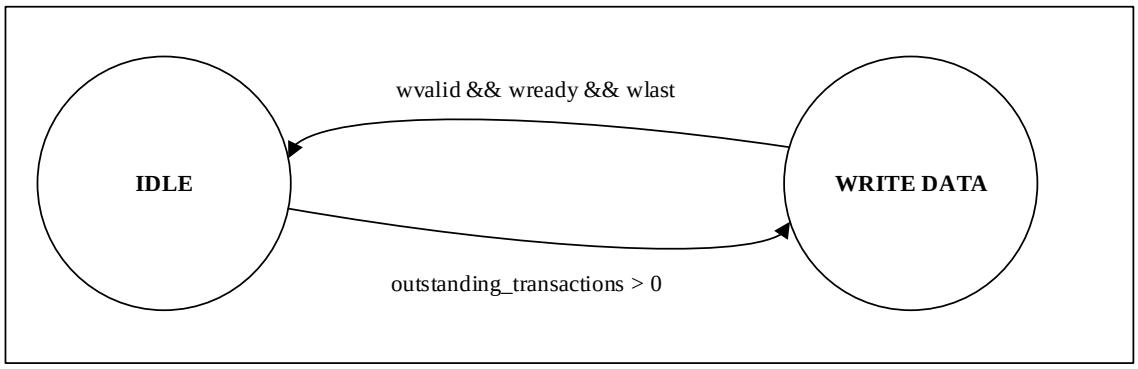
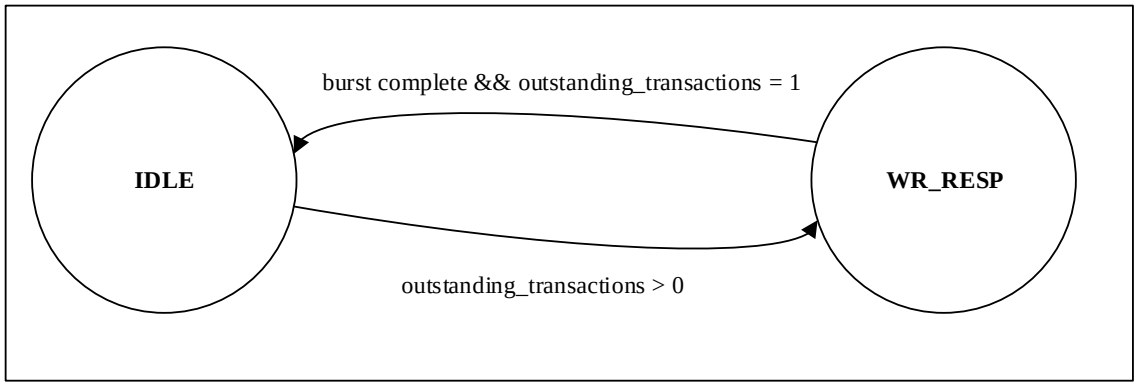


Figure 43-16 State transitions for AXI WR Response channel Control FSM



43.5.6.5 Descriptor and Descriptor List Structures

Descriptors are used by the DMA Core to acquire the memory locations and size of data blocks. The descriptor follows the structure illustrated in Table 43-26 and Table 43-27. The size of the descriptor is static and set to either 16 or 32 bytes, depending on the JPEGDMA_PARACFG.DESCSIZE parameter.

The first word contains the Desc_Flags, designating whether the data, associated with the descriptor, correspond to a start or end of a frame, as well as information on the presence of a linked descriptor and a flag that is asserted once the descriptor is consumed. The Descriptor Consumed flag does not have internal use for the Core, therefore any value set by the host does not affect. The flag's only purpose is to indicate to the host that the Descriptor has been processed.

The second and third words contain the allocated and effective size of the data block. In the Host-to Peripheral Channel, the effective size is the same as the allocated size and the BLOCK_USED field does not have any effect. In the Peripheral-to-Host Channel, the host should access the BLOCK_USED field to determine the correct size of the data written to the memory by the peripheral when the data block corresponds to an End of Frame. In the case of a 16-byte descriptor, those two fields are merged in a single word, each occupying one half of the second word.

In the 32-byte descriptor structure, words 3 and 4 contain the starting address of the data block referred to by the descriptor, covering both 32- and 64-bit addresses. The 16-byte descriptor structure only allows for 32-bit addresses, using the third word to communicate the data block's starting address.

Due to the descriptor structures not always residing in contiguous memory space, a descriptor may be one of two descriptor types, namely a simple or a link descriptor. A simple descriptor, denoted by the Link Enable flag set to 0,

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does not link to another descriptor and the next descriptor is located in the next valid descriptor address as expected. A link descriptor, denoted by the Link Enable flag set to 1, also contains a valid link to the address of the next descriptor. The linked address occupies word 6 of the descriptor, with word 7 used when a 64-bit address is required when the descriptor is set to 32 bytes, or word 4 when the descriptor is set to 16 bytes.

A Descriptor with a Block_Size equal to zero is still considered and valid Descriptor. However, if the Block_Size is zero and the Descriptor has its End of Frame flag set, data integrity cannot be guaranteed.

Table 43-26 8-word Descriptor Structure

Word	Bits	Field	Description
0	32	Desc_Flags	Descriptor flag bits: 0: Link Enable, 1: Start of Frame, 2: End of Frame, 3: Descriptor Consumed. 4-31: Reserved
1	32	Block_Size	Memory Block Size. Total allocated size of the memory space the descriptor points to.
2	32	Block_Used	Size of memory space utilized (field use when peripheral writes data to the host memory).
3	32	Block_Addr (LSB)	The starting address of the data block in host memory that this descriptor refers to.
4	32	Block_Addr (MSB)	The starting address of the data block in host memory that this descriptor refers to (upper 32 bits in case of 64-bit addresses).
5	32	Reserved	Reserved for future use. Reserved bits are read as 0.
6	32	Desc_Link_Addr (LSB)	Link to the next descriptor, used when Link Enable = 1.
7	32	Desc_Link_Addr (MSB)	Link to the next descriptor, used when Link Enable = 1 (upper 32 bits in case of 64-bit addresses).

Table 43-27 4-word Descriptor Structure

Word	Bits	Field	Description
0	32	Desc_Flags	Descriptor flag bits: 0: Link Enable, 1: Start of Frame, 2: End of Frame, 3: Descriptor Consumed. 4-31: Reserved
1	32	Block_Size [15:0] Block_Used [31:16]	[15:0] Block_Size: Total allocated size of memory space the descriptor points to. [31:16] Block_Used: Size of memory space utilized (field use when peripheral writes data to the host memory).

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2	32	Block_Addr	The starting address of the data block in host memory that this descriptor refers to.
3	32	Desc_Link_Addr	Link to the next descriptor. Used when Link Enable = 1.

43.5.6.5.1 Accessing Descriptors through Memory

The user can choose whether the descriptors reside in the host memory space, or will be programmed through the CSR interface of the Core. In the first case, the descriptors are accessed by the Core through the same AXI4 Memory-Mapped interface that is used for all data transfers. Each descriptor must be aligned to the data width of the interface. If the AXI4 MM data bus width is larger than the size of the Descriptor, additional padding must be introduced so that each Descriptor always occupies the least significant bytes of an AXI4 beat. The padding is discarded by the Core internally. Figure 43-17 and Figure 43-18 shows the two possible memory structures that hold the descriptors of each channel. The user can select between a simple List (Figure 43-17) and a Ring Buffer (Figure 43-18) through bit 1 of the JPEGDMA_CTRL.MMODE field.

When the simple List is selected as the Descriptor List structure, the host decides the Size of the List and populates it accordingly. The Tail pointer is updated after a Descriptor is consumed by the DMA Core to separate the consumed descriptor from the active descriptors.

When the Ring Buffer is selected as the Descriptor List structure, the Head pointer signifies the valid descriptors that have been initialized by the host, while the Tail pointer designates the descriptors that have been consumed by the DMA Core. The JPEGDMA_SGLSIZE parameter, in this case, denotes the total number of descriptors in the Ring Buffer, whether they are initialized, uninitialized, or consumed. As such, the Head and Tail pointers roll over to the first descriptor slot in the Ring when the JPEGDMA_SGLSIZE is reached. The Ring Buffer is empty when the Head and Tail pointers point to the same address, while it is considered full when the Tail equals to the Head+1.

Although the Size of the Descriptor List/Ring Buffer may be altered during runtime, it is highly recommended that it is considered a non-dynamic value while the Core is operational. No synchronization mechanism is provided between the host and the internal control of the Core in this case, which could result in unexpected behavior in certain corner cases. For this reason, it is advised that the user adheres to one of two possible SGList management schemes.

In the case of the Descriptor List, when more descriptors are required from the Core to resume execution due to all Descriptors from the List being consumed, the host should either allocate and provide a new Descriptor List or reuse the existing List by simply restarting the Core.

When using the Ring Buffer structure to store Descriptors, the Tail pointer will remain at the last Descriptor that was consumed. The host can then either refresh the previously consumed descriptors and increment the Head pointer or provide a new Ring Buffer. In the latter case, the Tail pointer needs to be reset by accessing the corresponding CSR field.

An important distinction between the two Channel types, requiring caution when handling the control signals and interrupts, is the moment when a Descriptor is consumed by the Channel. A Descriptor is considered consumed when the data block associated with it is accessed through the AXI4 MM interface. In the H2P Channel, this means when all the data from the data block have been read from the host memory. In this case, part of the data is still present in the pipeline of the Channel, but a transfer from a new Descriptor may be initiated. In the P2H Channel, the Descriptor is consumed when the data block inferred by it has no space to receive new data. As a result, no data related to that block remain in the Channel pipeline

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Note: Accessing descriptors through the AXI4 Memory-Mapped interface is viable only through incrementing bursts, regardless of the data burst type configuration.

43.5.6.5.2 Programming Descriptors through the CSR Interface

A Descriptor may optionally be programmed directly to the Core through the CSR interface, by populating the respective fields. This feature is enabled by setting bit 0 in the JPEGDMA_CTRL.MMODE field of the Control Register. In this case, the descriptor is read and updated directly from the CSR module and the host is responsible for providing the next descriptor once the previous one is consumed. A Descriptor can be programmed in the CSR fields at synthesis time by configuring the respective synthesis parameters. The host may then configure the rest of the CSR control fields and initiate a DMA transfer without the need to provide a Descriptor or SGList location.

This mode of descriptor access is incompatible with the descriptor memory structures. Therefore, using linked descriptors has no effect. When the Core is set to this mode, descriptors programmed through the CSR take precedence over any other descriptors.

The CSR Descriptor Registers and the Descriptor synthesis initialization parameters have fixed sizes and addresses, regardless of the DESCRIPTOR_SIZE parameter. Instead, the translation to the 4-word Descriptor Structure is performed internally. As such, writing to the CSR registers containing the MSBs of the Descriptor Block and Link Addresses has no effect and the returned value upon reading is zero. Similarly, the Block Size and Block Used Registers are truncated to 16 bits wide. Upper 16 bits for these Registers may not be written and are always zero upon reading.

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Figure 43-17 Representation of a simple List for Descriptor memory storage

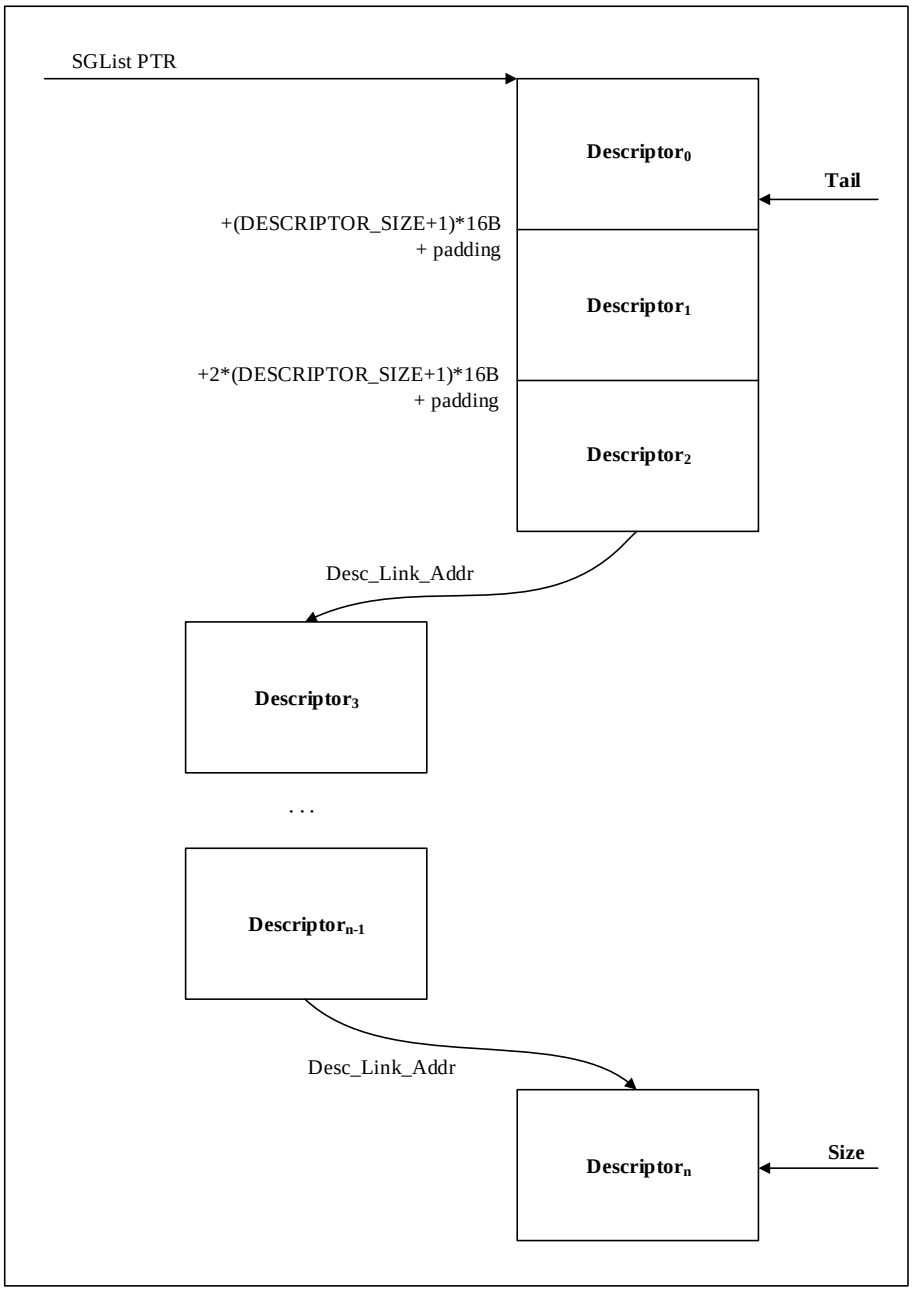

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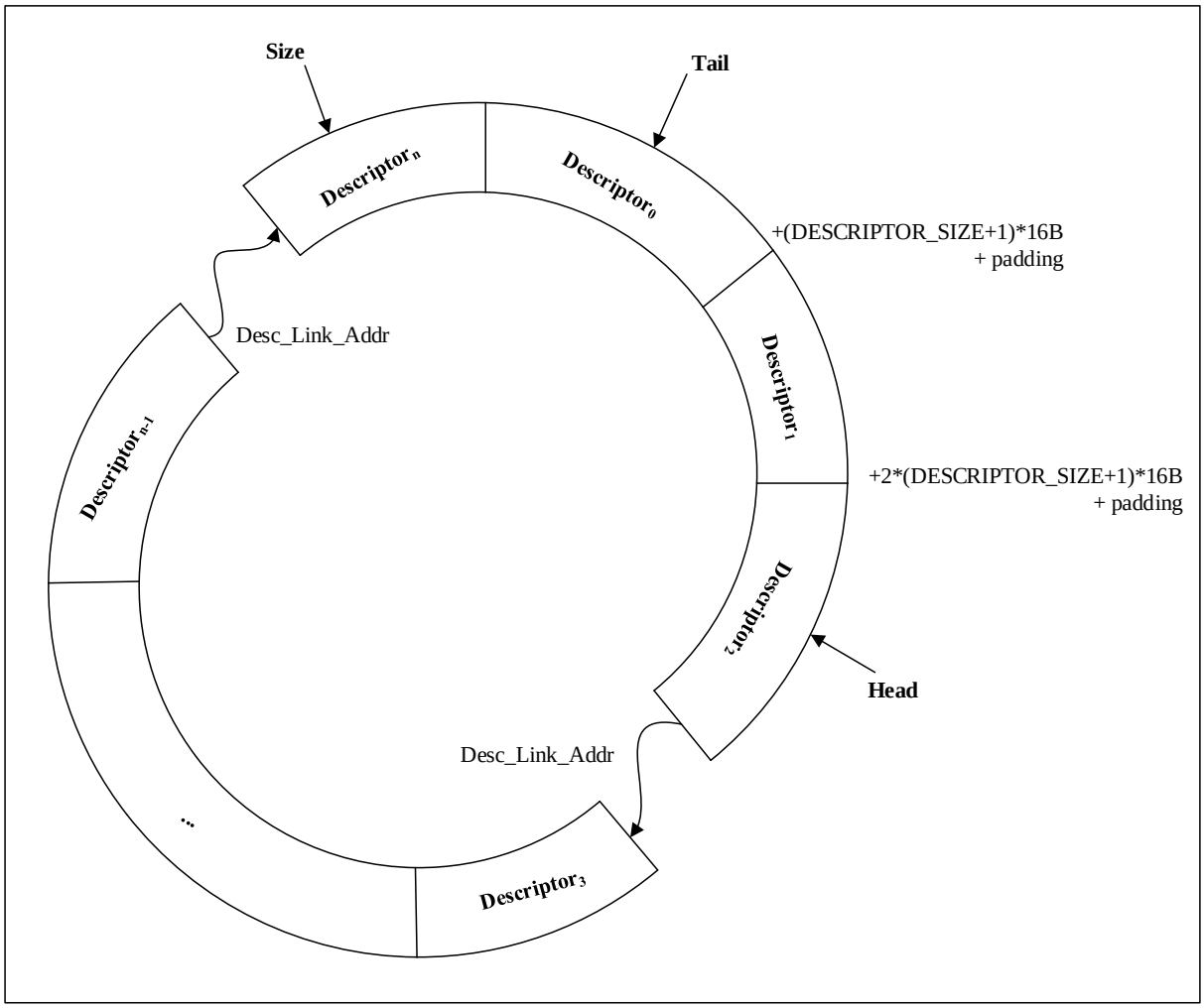
Figure 43-18 Representation of a Ring Buffer for Descriptor memory storage



43.5.7 Programming guide

The steps listed below are needed to program the JPEG

1. Power on for JPEG, please refer to PWR section
2. Enable the JPEG clock in the RCC register, please refer RCC section.
3. Choose JPEG operation: ENCODE/DECODE, refer to section 43.6.1
4. if JPEG work at ENCODE mode, configure RBC and Encoder refer section 43.5.2 and 43.5.3. Else configure BRC and Decoder refer section 43.5.4 and 43.5.5
5. Configure SGDMA, please refer section 43.5.6

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43.6 Registers

43.6.1 Type Control Register

Base Address：0x5009 0800

43.6.1.1 JPEG Control Register (JPEG_CTRL)

Offset Address：0x00

Reset Value：0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														SWAP	TYPE
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	SWAP	Swap Data for YCbCr 4:2:2 Format in BRC (Only be valid for decoding mode) 0: No swapping 1: WDATA[15:8] swapped with WDATA[23:16] and WDATA[47:40] swapped with WDATA[55:48] *Note: Only valid for decoding mode.* *Note: When using the MCU's built-in LCDC display, it is used to exchange YUV422 format data and convert it to a format that supports LCDC display.*
0	TYPE	Choose JPEG operation 0: JPEG decode 1: JPEG encode

43.6.2 SGDMA Register

The SGDMA registers can have two directions according to the JPEG_CTRL.TYPE selection, which are H2P and P2H, and there is a set of registers for each of the two directions with the following base addresses:

H2P base address: 0x5007 0400

P2H base address: 0x5009 0400

43.6.2.1 DMA Control Register (JPEGDMA_CTRL)

Offset Address：0x00

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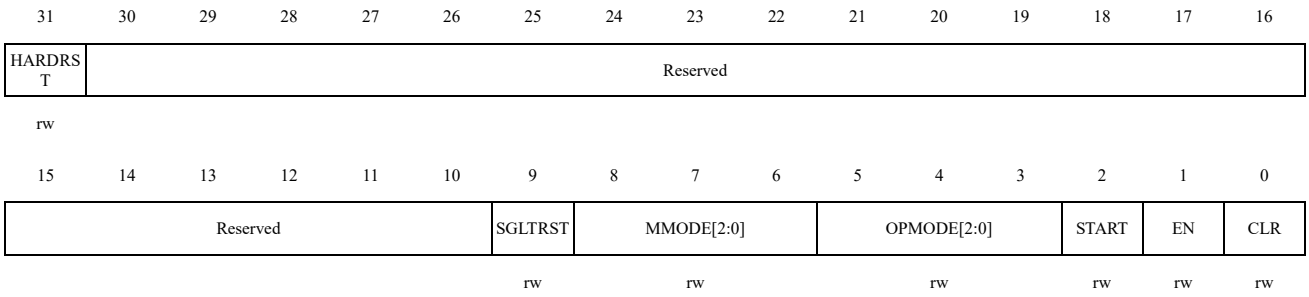
Reset Value：0x0000 0012



Bit field	Name	Description
31	HARDRST	Software hard reset. This bit forces a reset on the module regardless of its state. It is advised to not use this reset under normal circumstances, rather choose to reconfigure the module through CLR. This reset overrides any ongoing AXI4 transactions and may result in bus errors.
30:10	Reserved	Reserved,the reset value must be maintained
9	SGLTRST	Reset the TAIL of the SGList to zero when MMODE = 2
8:6	MMODE[2:0]	Descriptor Memory Mode settings: Bit 0： 0: Descriptors stored in memory. 1: Descriptors programmed through CSR. Bit 1： 0: The descriptor list structure is a simple List. 1: The descriptor list structure is a Ring Buffer. Bit 2: Reserved.
5:3	OPMODE[2:0]	Operation Mode Settings: Bit 0： 0: Pause DMA operation on EOF and wait for driver action. 1: Resume operation of the DMA normally after the EOF. Bit 1： 0: AXI4 MM FIXED burst (aligned addresses only). 1: AXI4 MM INCR burst. Bit 2: Reserved.
2	START	DMA Start. Assert this bit to initiate DMA transfers after a reset or pause. Auto clears after action is complete. Writing a value of 0 to this field no effect. 0: Disable 1: Enable
1	EN	Software enable
0	CLR	Software reset for the entire H2P/P2H. The bit must be set only when the H2P/P2H is not busy, to avoid AXI4 violations. The bit remains set and auto-clears when the reset is completed. Writing a value of 0 to this field has

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Bit field	Name	Description
		not affect.

43.6.2.2 DMA Status Register (JPEGDMA_STS)

Offset Address：0x04

Reset Value：0x0000 0080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RRERR	WRERR	WDATAERR	RDATAERR	WDESCERR	RDESCERR	Reserved	FIFOFULL	FIFOEMPTY	EOD	AOOD	OOD	EOFIN	EOFOUT	GINT	BUSY
r	r	r	r	r	r		r	r	rw	rw	rw	rw	rw	r	r

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15	RRERR	AXI Read response when error has occurred
14	WRERR	AXI Write response when error has occurred
13	WDATAERR	AXI MM Write Error when writing data
12	RDATAERR	AXI MM Read Error when reading data
11	WDESCERR	AXI MM Write Error when writing a descriptor
10	RDESCERR	AXI MM Read Error when reading a descriptor
9	Reserved	Reserved,the reset value must be maintained
8	FIFOFULL	Data FIFO is full
7	FIFOEMPTY	Data FIFO is empty
6	EOD	End-Of-Descriptor. The bit is set due to the consumed descriptor.
5	AOOD	Channel is Almost Out of Descriptors. The condition for this status is set through the JPEGDMA_AOODT register.
4	OOD	Out Of Descriptors. The bit is set when the channel runs out of descriptors.
3	EOFIN	End-Of-Frame sampled at the input of the channel.
2	EOFOUT	End-Of-Frame sampled at the output of the channel. DMA transfer is complete with an EOF sampled at the output of the Channel.
1	GINT	Global interrupt status bit for the Channel. This field is auto-cleared when all individual interrupts are cleared.
0	BUSY	H2P is processing a transfer.

43.6.2.3 DMA Interrupt Control Register (JPEGDMA_IE)

Offset Address：0x08

Reset Value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		WDATAERREN	RDATAERREN	WDESCERREN	RDESCERREN	Reserved			EODINTEN	AOODINTEN	OODINTEN	EOFININTEN	EOFOUTINTEN	GINTEN	Reserved
		rw	rw	rw	rw				rw	rw	rw	rw	rw	rw	

Bit field	Name	Description
31:14	Reserved	Reserved,the reset value must be maintained
13	WDATAERREN	Enable interrupt on AXI MM Write Error when writing data
12	RDATAERREN	Enable interrupt on AXI MM Read Error when reading data
11	WDESCERREN	Enable interrupt on AXI MM Write Error when writing a descriptor
10	RDESCERREN	Enable interrupt on AXI MM Read Error when reading a descriptor
9:7	Reserved	Reserved,the reset value must be maintained
6	EODINTEN	Enable for the End of Descriptor interrupt
5	AOODINTEN	Enable for the Almost Out of Descriptors interrupt
4	OODINTEN	Enable for the Out of Descriptors interrupt
3	EOFININTEN	Enable for the input EOF interrupt
2	EOFOUTINTEN	Enable for the output EOF interrupt
1	GINTEN	Global interrupt enable for the Channel
0	Reserved	Reserved,the reset value must be maintained

43.6.2.4 DMA Interrupt Status Register (JPEGDMA_INTSTS)

Offset Address：0x0C

Reset Value：0x0000 0000

The value of each bit of this register value is the “with” value of the corresponding bit segment of JPEGDMA_STS and JPEGDMA_IE.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		WDATAERR	RDATAERR	WDESCERR	RDESCERR	INTERERR	Reserved		EOD	AOO	OOD	EOFIN	EOFOUT	GINT	Reserved
		r	r	r	r	r			r	r	r	r	r	r	

Bit field	Name	Description
31:14	Reserved	Reserved,the reset value must be maintained
13	WDATAERR	Interrupt on AXI MM Write Error when writing data

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Bit field	Name	Description
12	RDATAERR	Interrupt on AXI MM Read Error when reading data
11	WDESCERR	Interrupt on AXI MM Write Error when writing a descriptor
10	RDESCERR	Interrupt on AXI MM Read Error when reading a descriptor
9	INTERERR	Interrupt on internal core error occurred
8:7	Reserved	Reserved,the reset value must be maintained
6	EOD	End of Descriptor interrupt This bit is set when a descriptor is used.
5	AOOD	Almost Out of Descriptors interrupt The condition for this state is set via the JPEGDMA_AOODT register.
4	OOD	Out of Descriptors interrupt This bit is set when the channel descriptors are exhausted.
3	EOFIN	Input EOF interrupt
2	EOFOUT	Output EOF interrupt The DMA transfer is completed after the EOF is sampled at the output of the channel.
1	GINT	Global interrupt for the Channel This field is automatically cleared when all individual interrupts are cleared.
0	Reserved	Reserved,the reset value must be maintained

43.6.2.5 DMA Almost Out Of Descriptors Threshold Register (JPEGDMA_AOODT)

Offset Address：0x10

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AOODTHR[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AOODTHR[15:0]															
rw															

Bit field	Name	Description
31:0	AOODTHR[31:0]	Almost Out Of Descriptors Threshold. If JPEGDMA_IE.AOODINTEN interrupt is enabled, an interrupt will be generated below this threshold. A value of 0 disables the threshold.

43.6.2.6 DMA Maximum Burst Size Register (JPEGDMA_MBSIZE)

Offset Address：0x14

Reset Value：0x0000 0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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MAXBSIZE[31:16]

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXBSIZE[15:0]															

rw

Bit field	Name	Description
31:0	MAXBSIZE[31:0]	Maximum allowed size for an AXI4 MM burst. The value must be smaller than the JPEGDMA_FIFODP.DEPTH[31:0].

43.6.2.7 DMA Scatter Gather List Pointer Register (JPEGDMA_SGLP)

Offset Address：0x18

Reset Value：0x0000 0000 0000 0000

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR[63:48]															

rw

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR[47:32]															

rw

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR [31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR [15:0]															

rw

Bit field	Name	Description
63:0	ADDR[63:0]	Scatter-Gather List Pointer. The register defines the 64-bit base address of the channel’s Scatter-Gather list in host memory. Field should be updated before JPEGDMA_SGLSIZE and JPEGDMA_SGLHEAD.

43.6.2.8 DMA Scatter Gather List Size Register (JPEGDMA_SGLSIZE)

Offset Address：0x20

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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SGLSIZE[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SGLSIZE[15:0]															
rw															

Bit field	Name	Description
31:0	SGLSIZE[31:0]	Scatter-Gather List Size. The register defines the number of descriptors in the decentralized aggregation list/ring (16 bits)

43.6.2.9 DMA Scatter Gather List Head Register (JPEGDMA_SGLHEAD)

Offset Address：0x24

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POS[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS[15:0]															
rw															

Bit field	Name	Description
31:0	POS[31:0]	Scatter-Gather List Head index pointer defines the position of the Head pointer in the list/ring. The values are integers interpreted as 1st, 2nd, etc. Descriptor and not as addresses.

43.6.2.10 DMA Scatter Gather List Tail Register (JPEGDMA_SGLTAIL)

Offset Address：0x28

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POS[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS[15:0]															
rw															

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Bit field	Name	Description
31:0	POS[31:0]	Scatter-Gather List Tail index pointer defines the position of the tail pointer in the list/ring. The values are integers interpreted as 1st, 2nd, etc. Descriptor and not as addresses.

43.6.2.11 DMA Memory Read Address Register (JPEGDMA_MRADD)

Offset Address：0x2C

Reset Value：0x0000 0000 0000 0000

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR [63:48]															
r															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR [47:32]															
r															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR [31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR [15:0]															
r															

Bit field	Name	Description
63:0	ADDR[63:0]	AXI memory read address reports the current address of the AXI MM interface’s read channel accesses. The value is used for debugging and error reporting.

43.6.2.12 DMA Memory Write Address Register (JPEGDMA_MWADD)

Offset Address：0x34

Reset Value：0x0000 0000 0000 0000

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR [63:48]															
r															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR [47:32]															
r															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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ADDR [31:16]

r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR [15:0]															

r

Bit field	Name	Description
63:0	ADDR[63:0]	AXI memory write address reports the current address of the AXI MM interface's read channel accesses. The value is used for debugging and error reporting.

43.6.2.13 DMA Descriptor Flag Register (JPEGDMA_DESCF)

Offset Address：0x3C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DESCCON	END	START	LINKE
												rw	rw	rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3	DESCCON	Descriptor Consumed 0: Disable 1: Enable
2	END	End of Frame 0: Disable 1: Enable
1	START	Start of Frame 0: Disable 1: Enable
0	LINKE	Link Enable 0: Disable 1: Enable

43.6.2.14 DMA Descriptor Memory Block Size Register (JPEGDMA_DESC_MBSIZE)

Offset Address：0x40

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Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIZE[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
rw															

Bit field	Name	Description
31:0	SIZE[31:0]	Descriptor Memory Block Size. Total allocated size of memory space the descriptor points to.

43.6.2.15 DMA Descriptor Memory Used Space Register (JPEGDMA_DESC_MUS)

Offset Address：0x44

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIZE[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
r															

Bit field	Name	Description
31:0	SIZE[31:0]	Descriptor Memory Used Space. Size of memory space utilized (field use when peripheral writes data to the host memory).

43.6.2.16 DMA Descriptor Memory Block Address Register (JPEGDMA_DESC_MBADD)

Offset Address：0x48

Reset Value：0x0000 0000

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR [63:48]															
rw															

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR [47:32]															
rw															

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR [31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR [15:0]															
rw															

Bit field	Name	Description
63:0	ADDR[63:0]	Descriptor Memory Block Address. The starting address of the data block in host memory that this descriptor refers to.

43.6.2.17 DMA Descriptor Link Address LSB Register (JPEGDMA_DESC_LINK)

Offset Address：0x54

Reset Value：0x0000 0000

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
ADDR [63:48]															
rw															

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDR [47:32]															
rw															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR [31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR [15:0]															
rw															

Bit field	Name	Description
63:0	ADDR[63:0]	Descriptor Link Address - link to the next descriptor. Used when JPEGDMA_DESCF.LINKE=1.

43.6.2.18 DMA Parameters Configuration Register (JPEGDMA_PARACFG)

Offset Address：0x5C

Reset Value：0x0000 0006

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													ALIGNEN	DESCSIZE	DTYPE
													r	r	r

Bit field	Name	Description
31:3	Reserved	Reserved,the reset value must be maintained
2	ALIGNEN	Alignment enabled or disabled for instance. 0: disabled 1: enabled
1	DESCSIZE	Size of descriptor (16 or 32 bytes) 0: 16 bytes 1: 32 bytes
0	DTYPE	Type of DMA Channel (H2P or P2H) 0: H2P 1: P2H

43.6.2.19 DMA Data FIFO Depth Register (JPEGDMA_FIFODP)

Offset Address：0x60

Reset Value：0x0000 0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DEPTH[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEPTH[15:0]															
r															

Bit field	Name	Description
31:0	DEPTH[31:0]	Field mirroring the DATA_FIFO_DEPTH parameter.

43.6.3 Decode Register

Base Address：0x5008 0000

43.6.3.1 Decode Mode Register (JPEGDEC_MODE)

Offset Address：0x00

Reset Value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable the decode mode 0: Disable 1: Enable

43.6.3.2 Decode Error Register (JPEGDEC_ERROR)

Offset Address：0x04

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										HTERR	QTERR	CERR	HUF	UNEXP	UNK
										rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained
5	HTERR	A Huffman table referenced in a scan (SOS header) is invalid.
4	QTERR	A Quantization Table referenced in a component referenced in a scan (SOS header) selected an invalid Quantization Table.
3	CERR	A component referenced in the scan header (SOS) was not defined in the previous frame header (SOF).
2	HUF	Huffman decode error detected
1	UNEXP	Unexpected marker detected
0	UNK	Unknown marker detected

43.6.3.3 Unknown Marker Error Location Register (JPEGDEC_UNLOC)

Offset Address：0x08

Reset Value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POS[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS[15:0]															
r															

Bit field	Name	Description
31:0	POS[31:0]	Unknown marker error location. In the event of an unknown marker error, the decoder stores the location of the unknown marker in this register. The location is the byte-offset from the last SOI marker processed.

43.6.3.4 Unexpected Marker Error Location Register (JPEGDEC_UELOC)

Offset Address：0x0C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POS[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS[15:0]															
r															

Bit field	Name	Description
31:0	POS[31:0]	Unexpected marker error location. In the event of an unexpected marker error, the decoder stores the location of the unexpected marker in this register. The location is the byte-offset from the last SOI marker processed.

43.6.3.5 Huffman Error Symbol Register (JPEGDEC_HESYM)

Offset Address：0x10

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HESYM[15:0]															

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r

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	HESYM[15:0]	The Huffman symbol that is in error. The first bit of the Huffman symbol is on bit [15], the second on bit [14], etc.

43.6.3.6 Huffman ECS Number Symbol Error Register (JPEGDEC_HESYMECS)

Offset Address：0x14

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NUM[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUM[15:0]															
r															

Bit field	Name	Description
31:0	NUM[31:0]	Huffman ECS Number Symbol . In the event of a Huffman decode error, the decoder stores the ECS number in which the error was found to this register. The ECS number is counted from the last SOI marker.

43.6.3.7 Huffman Symbol Error Location Register (JPEGDEC_HUF_SELOC)

Offset Address：0x18

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POS[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS[15:0]															
r															

Bit field	Name	Description
31:0	POS[31:0]	Huffman ECS Number Symbol Error location . In the event of a Huffman decode error, the decoder stores the location of the invalid Huffman symbol in this register. The location is the bit-offset from the start of ECS. The ECS number in

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Bit field	Name	Description
		which the error was found is stored to the “JPEGDEC_HESYMECS” register.

43.6.3.8 Table Access Request Register (JPEGDEC_TAB_ACCREQ)

Offset Address：0x1C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														AOK	AREQ
														r	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1	AOK	Table access flag . When this bit is set to 1, the tables (quantisation & Huffman) may be read or written. This bit is set to 1 if no frame is currently being processed – either the decoder has just been enabled and no frame was received or an EOI marker has been processed but the next SOI marker has not been received. While this bit is set to 1, no input data is processed.
0	AQEQ	Table access request. If any of the quantisation or Huffman tables are to be accessed, this bit is to be set to 1 and the SW is to wait for bit [1] to be set before accessing the tables. To resume processing input frames, this bit is to be set to 0.

43.6.3.9 Huffman Table0 EOB Symbol Register (JPEGDEC_HUFTAB0_EOB)

Offset Address：0x20

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOB0M[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOB0C[15:0]															
rw															

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Bit field	Name	Description
31:16	EOB0M[15:0]	Contains the EOB symbol mask for Huffman table 0.
15:0	EOB0C[15:0]	Contains the EOB symbol for Huffman table 0.

43.6.3.10 Huffman Table1 EOB Symbol Register (JPEGDEC_HUFTAB1_EOB)

Offset Address：0x24

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOB1M[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOB1C[15:0]															
rw															

Bit field	Name	Description
31:16	EOB1M[15:0]	Contains the EOB symbol mask for Huffman table 1.
15:0	EOB1C[15:0]	Contains the EOB symbol for Huffman table 1.

43.6.3.11 Huffman Table2 EOB Symbol Register (JPEGDEC_HUFTAB2_EOB)

Offset Address：0x28

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOB2M[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOB2C[15:0]															
rw															

Bit field	Name	Description
31:16	EOB2M[15:0]	Contains the EOB symbol mask for Huffman table 2.
15:0	EOB2C[15:0]	Contains the EOB symbol for Huffman table 2.

43.6.3.12 Huffman Table3 EOB Symbol Register (JPEGDEC_HUFTAB3_EOB)

Offset Address：0x2C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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EOB3M[15:0]

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOB3C[15:0]															

rw

Bit field	Name	Description
31:16	EOB3M[15:0]	Contains the EOB symbol mask for Huffman table 3.
15:0	EOB3C[15:0]	Contains the EOB symbol for Huffman table 3.

43.6.3.13 Huffman Table Access Address Register (JPEGDEC_HUF_ADDR)

Offset Address：0x80

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						TABLE[1:0]		Reserved			ACDC	Reserved		HNUM[1:0]	

rw rw rw

Bit field	Name	Description
31:10	Reserved	Reserved,the reset value must be maintained
9:8	TABLE[1:0]	Selects which table to access 0: Hoffman decoder table 1: D-vector 2: I-vector 3: Hoffman decoder gas pedal table
7:5	Reserved	Reserved,the reset value must be maintained
4	ACDC	AC/DC table selector encoded 0: Select DC table 1: Select AC table
3:2	Reserved	Reserved,the reset value must be maintained
1:0	HNUM[1:0]	Select the Hoffman table to be accessed 0: Table 0 1: Table 1 2: Table 2 3: Table 3

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43.6.3.14 Huffman Table Access Data Register (JPEGDEC_HUF_DATA)

Offset Address：0x84

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HDATA[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDATA[15:0]															
rw															

Bit field	Name	Description
31:0	HDATA[31:0]	Huffman Table Data . Accessing this register increments the Huffman table access address by one and decrements the "JPEGDEC_HUF_REM". Reading from this register reads the Huffman table selected by the JPEGDEC_HUF_ADDR and writing this register writes the selected Huffman table.

43.6.3.15 Huffman Table Access Remaining Words Register (JPEGDEC_HUF_REM)

Offset Address：0x88

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HREM[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HREM[15:0]															
rw															

Bit field	Name	Description
31:0	HREM[31:0]	Huffman table access number of words remaining from the currently selected Huffman table.

43.6.3.16 Quantization Table0 Register (JPEGDEC_QT0)

Offset Address：0x400 + (n*4) n = 0, 1, 2…63

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								QT0[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT0[7:0]	Quantization Table 0 factor n value (n = 0, 1, 2…63)

43.6.3.17 Quantization Table1 Register (JPEGDEC_QT1)

Offset Address：0x500 + (n*4)　n = 0, 1, 2…63

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								QT1[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT1[7:0]	Quantization Table 1 factor n value (n = 0, 1, 2…63)

43.6.3.18 Quantization Table2 Register (JPEGDEC_QT2)

Offset Address：0x600 + (n*4)　n = 0, 1, 2…63

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								QT2[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT2[7:0]	Quantization Table 2 factor n value (n = 0, 1, 2…63)

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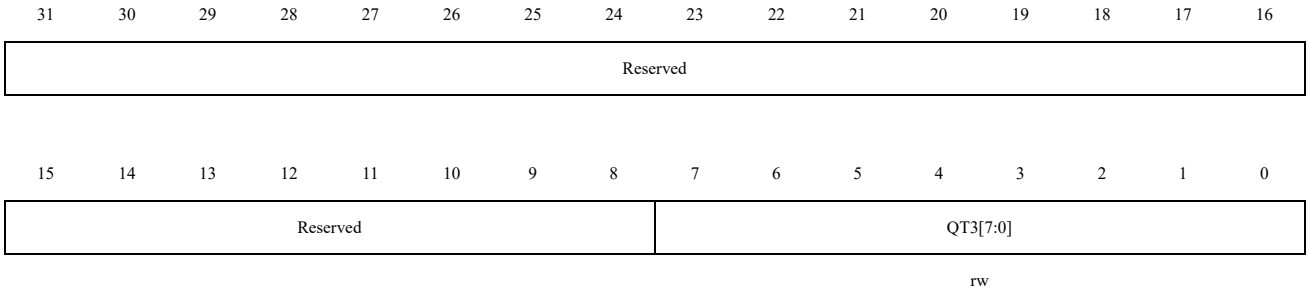
43.6.3.19 Quantization Table3 Register (JPEGDEC_QT3)

Offset Address：0x700 + (n*4) n = 0, 1, 2…63

Reset Value：0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT3[7:0]	Quantization Table 3 factor n value (n = 0, 1, 2…63)

43.6.4 Encode Register

Base Address：0x5006 0000

43.6.4.1 Huffman Table x Register (x = 0, 1, 2, 3)

Huffman Table 0 Register Offset Address: 0x0000

Huffman Table 1 Register Offset Address: 0x0800

Huffman Table 2 Register Offset Address: 0x1000

Huffman Table 3 Register Offset Address: 0x1800

43.6.4.1.1 Code offset and length Register(JPEGENC_HUFTAB_COL)

Offset Address inside table x (x = 0, 1, 2, 3)and corresponding content description:

Offset Address inside table	description
0x000	DC code offset and length for category 0
0x004	DC code offset and length for category 1
…	
0x03c	DC code offset and length for category 15
0x040	AC code offset and length for category 1, run 0
0x044	AC code offset and length for category 1, run 1
…	
0x07c	AC code offset and length for category 1, run 15
0x080	AC code offset and length for category 2, run 0
…	…

Reset Value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CL[3:0]				CO[7:0]							
				rw				rw							

Bit field	Name	Description
31:12	Reserved	Reserved,the reset value must be maintained
11:8	CL[3:0]	Length of this code 0: 1 … 15: 16
7:0	CO[7:0]	Gives the offset of this code word from the first code of this length

43.6.4.1.2 Code start Register(JPEGENC_HUFTAB_CST)

Offset Address inside table x (x = 0, 1, 2, 3)and corresponding content description:

Offset Address inside table	description
0x400	First DC code for 1 bit codes (constant 0) ($S_{1,DC}$)
0x404	First DC code for 2 bit codes ($S_{2,DC}$)
0x408	First DC code for 3 bit codes ($S_{3,DC}$)
…	…
0x43c	First DC code for 16 bit codes ($S_{16,DC}$)
0x440	First AC code for 1 bit codes (constant 0) ($S_{1,AC}$)
0x444	First AC code for 2 bit codes ($S_{2,AC}$)
0x448	First AC code for 3 bit codes ($S_{3,AC}$)
…	…
0x47c	First AC code for 16 bit codes ($S_{16,AC}$)

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS[15:0]															
rw															

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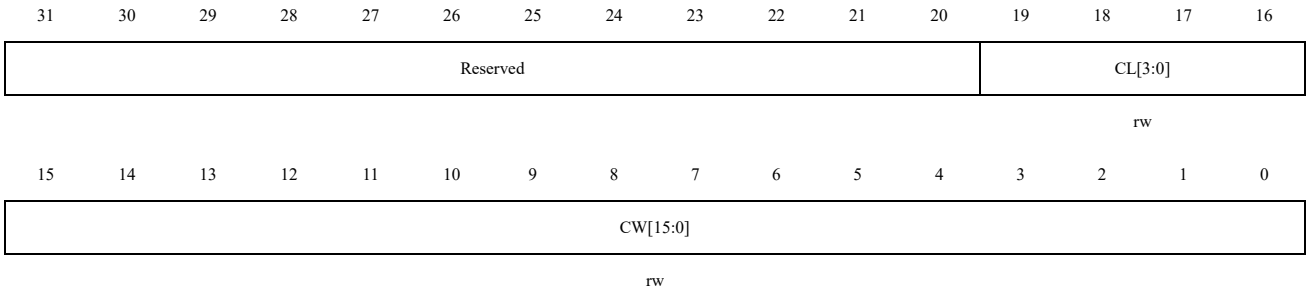
Bit field	Name	Description
31:0	CS[31:0]	Gives the first Huffman code word for the given length of code

43.6.4.1.3 ZRL and EOB symbols Register(JPEGENC_HUFTAB_SYM)

Offset Address inside table x (x = 0, 1, 2, 3)and corresponding content description:

Offset Address inside table	description
0x480	EOB symbol
0x484	ZRL symbol

Reset Value：0x0000 0000

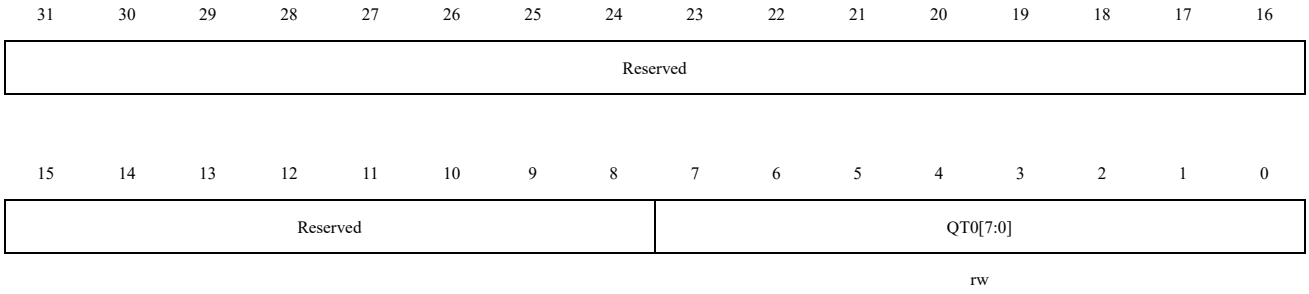


Bit field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained
19:16	CL[3:0]	Length of the code in bits 0: 1 … 15: 16
15:0	CW[15:0]	The code word. The most significant bit is the first bit of the code, however the code words are aligned on the least significant bit. Eg. if the code word is 01 (two bits long) the first bit is 0, followed by 1 and the code is to be written in this field as 0x0001.

43.6.4.2 Quantization Table0 Register (JPEGENC_QT0)

Offset Address：0x2000 + (n*4) n = 0, 1, 2…63

Reset Value：0x0000 0000



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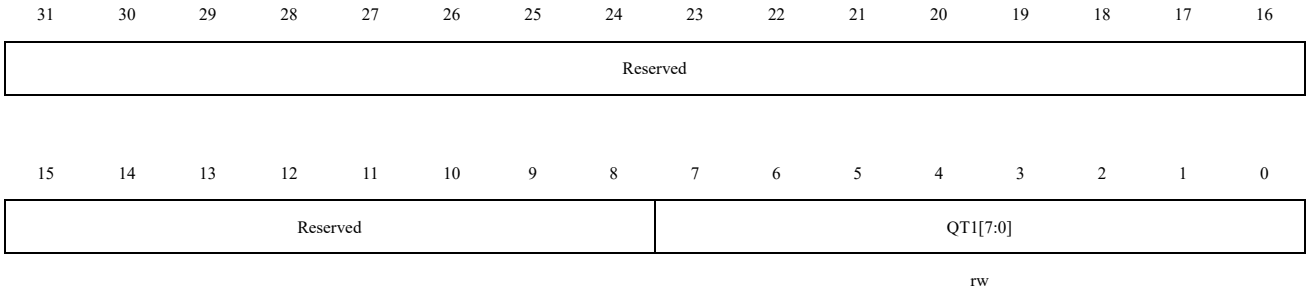
Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT0[7:0]	Quantization Table 0 factor n value (n = 0, 1, 2…63)

43.6.4.3 Quantization Table1 Register (JPEGENC_QT1)

Offset Address：0x2100 + (n*4) n = 0, 1, 2…63

Reset Value：0x0000 0000

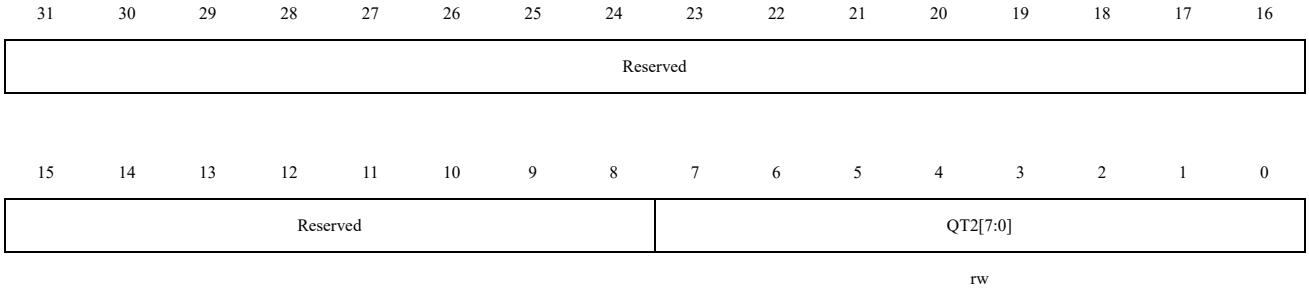


Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT1[7:0]	Quantization Table 1 factor n value (n = 0, 1, 2…63)

43.6.4.4 Quantization Table2 Register (JPEGENC_QT2)

Offset Address：0x2200 + (n*4) n = 0, 1, 2…63

Reset Value：0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT2[7:0]	Quantization Table 2 factor n value (n = 0, 1, 2…63)

43.6.4.5 Quantization Table3 Register (JPEGENC_QT3)

Offset Address：0x2300 + (n*4) n = 0, 1, 2…63

Reset Value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								QT3[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:0	QT3[7:0]	Quantization Table 3 factor n value (n = 0, 1, 2…63)

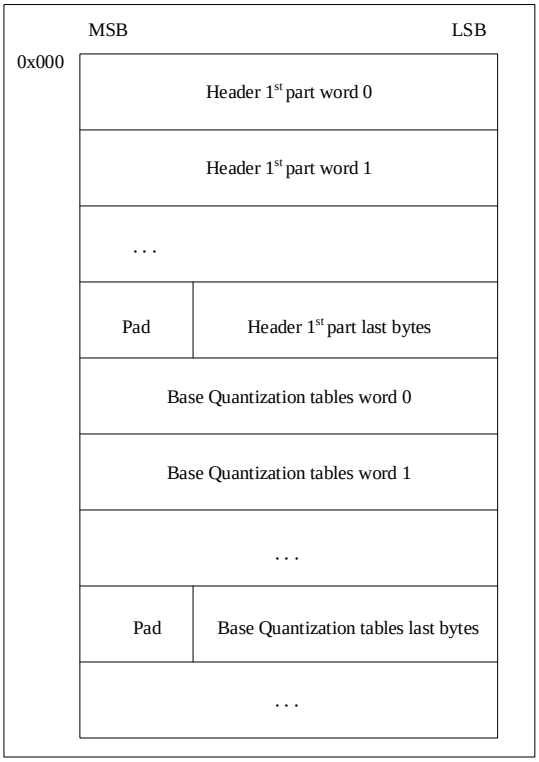
43.6.4.6 JPEG Header/Footer Buffer Register (JPEGENC_HFBUF)

Offset Address: 0x4000 + (n*4) n = 0, 1, 2…512

Reset Value: 0x0000 0000

The header/footer buffer is an area of memory which stores the header and footer of the output jpeg file. The buffer's size is given in the "JPEGENC_HFSIZE" register. Fill in word 0, word 1, word 2...word 512 in order from address 0x4000.

In the buffer at address 0 starts the 1st part of the header, immediately followed by Base Quantization tables aligned to a 4-byte boundary, followed directly by Huffman table 1 and again aligned on a 4-byte boundary, etc. The following figure illustrates this:



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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BYTE3[7:0]								BYTE2[7:0]							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE1[7:0]								BYTE0[7:0]							
rw								rw							

Bit field	Name	Description
31:24	BYTE3[7:0]	4th byte of header in word n (n=0,1,2…511)
23:16	BYTE2[7:0]	3rd byte of header in word n (n=0,1,2…511)
15:8	BYTE1[7:0]	2nd byte of header in word n (n=0,1,2…511)
7:0	BYTE0[7:0]	1st byte of header in word n (n=0,1,2…511)

43.6.4.7 JPEG Header End Address Register (JPEGENC_HEADD)

Offset Address：0x4800

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					ADDR[10:0]										
					rw										

Bit field	Name	Description
31:11	Reserved	Reserved,the reset value must be maintained
10:0	ADDR[10:0]	Address of the last byte of the 1st part of the JPEG header in the header/footer buffer.

43.6.4.8 Huffman Table0 End Address Register (JPEGENC_HUFTAB0E)

Offset Address：0x4814

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	ADDR[10:0]

rw

Bit field	Name	Description
31:11	Reserved	Reserved,the reset value must be maintained
10:0	ADDR[10:0]	Address of the last byte of Huffman table in the header/footer buffer. If this Huffman table is not used, this field is to be set to 0 and both the header output logic will skip this table.

43.6.4.9 Huffman Table1 End Address Register (JPEGENC_HUFTAB1E)

Offset Address：0x4818

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					ADDR[10:0]										

rw

Bit field	Name	Description
31:11	Reserved	Reserved,the reset value must be maintained
10:0	ADDR[10:0]	Address of the last byte of Huffman table in the header/footer buffer. If this Huffman table is not used, this field is to be set to 0 and both the header output logic will skip this table.

43.6.4.10 Huffman Table2 End Address Register (JPEGENC_HUFTAB2E)

Offset Address：0x481C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					ADDR[10:0]										

rw

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Bit field	Name	Description
31:11	Reserved	Reserved,the reset value must be maintained
10:0	ADDR[10:0]	Address of the last byte of Huffman table in the header/footer buffer. If this Huffman table is not used, this field is to be set to 0 and both the header output logic will skip this table.

43.6.4.11 Huffman Table3 End Address Register (JPEGENC_HUFTAB3E)

Offset Address：0x4820

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					ADDR[10:0]										
					rw										

Bit field	Name	Description
31:11	Reserved	Reserved,the reset value must be maintained
10:0	ADDR[10:0]	Address of the last byte of Huffman table in the header/footer buffer. If this Huffman table is not used, this field is to be set to 0 and both the header output logic will skip this table.

43.6.4.12 JPEG End of File Address Register (JPEGENC_FEADD)

Offset Address：0x4824

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						ADDR[9:0]									
						rw									

Bit field	Name	Description
31:10	Reserved	Reserved,the reset value must be maintained
9:0	ADDR[9:0]	The address of the last byte of the JPEG footer in the header/footer buffer.

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43.6.4.13 Encode Control Register (JPEGENC_CTRL)

Offset Address：0x5000

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												QT3[1:0]		QT2[1:0]	
												rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QT1[1:0]		QT0[1:0]		HUF3[1:0]		HUF2[1:0]		HUF1[1:0]		HUF0[1:0]		Reserved		ERST	EN
rw		rw		rw		rw		rw		rw				rw	rw

Bit field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained
19:18	QT3[1:0]	Quantization Table selector for component 3.
17:16	QT2[1:0]	Quantization Table selector for component 2.
15:14	QT1[1:0]	Quantization Table selector for component 1.
13:12	QT0[1:0]	Quantization Table selector for component 0.
11:10	HUF3[1:0]	Huffman table selector for component 3.
9:8	HUF2[1:0]	Huffman table selector for component 2.
7:6	HUF1[1:0]	Huffman table selector for component 1.
5:4	HUF0[1:0]	Huffman table selector for component 0.
3:2	Reserved	Reserved,the reset value must be maintained
1	ERST	If set to 1, reset the core if any error occurred (any bit in any pipe status register is set to non-zero) and wait for the next Start-of-Frame.
0	EN	If set to 1, the core is enabled and ready to process incoming frames. If set to 0, the core will not process any frames and produce no output. Should the core run into an error (any bit in any pipe status register is non-zero), the core should be reset by writing first a 0 to this register and then a 1.

43.6.4.14 Dynamic Reconfiguration Register (JPEGENC_DYNRCFG)

Offset Address：0x5004

Reset Value：0x0000 0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													HSAFE	DYNF	DYNEN
													rw	rw	rw

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Bit field	Name	Description
31:3	Reserved	Reserved,the reset value must be maintained
2	HSAFE	While this bit is set to 1, it is safe to change the contents of the Header/Footer buffer. As soon as it is set to 0, it is expected that a coherent set of headers and footers may be found in the Header/Footer buffer.
1	DYNF	Once bit [0] has been set, this bit indicates the state of the pipeline: 0: The pipeline is busy processing a frame: the encoder may not be reconfigured. 1: The pipeline is empty: the encoder may be reconfigured as desired.
0	DYNEN	If this bit is set, the core will finish processing the current frame and stall before accepting the next frame.

43.6.4.15 Header Parts Select Register (JPEGENC_HSEL)

Offset Address：0x503C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						ATF	NFD	HT3	HT2	HT1	HT0	QT3	QT2	QT1	QT0
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:10	Reserved	Reserved,the reset value must be maintained
9	ATF	If this bit is set to one, then the next output ""image"" will only contain the tables as mentioned on bits [7:0] of this register and without an ECS data. Once the output has been completed, this bit is reset to 0. When this bit is set, the encoder behaves as follows: 1, Processing of the current frame is completed 2, Output is generated containing only the specified tables and no ECS data. This happens irrespective of whether the first sample of the next frame is received or not. 3, Normal processing resumes with the next frame.
8	NFD	If this is set to one, then the next frame that is output will have all the tables marked by bits [7:0] output and once they are output, then bits [7:0] in this register will be set to 0. It means all following frames will have no tables output.
7	HT3	Ouptut Huffman table 3 in output stream 0: No output 1: Output
6	HT2	Ouptut Huffman table 2 in output stream 0: No output

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Bit field	Name	Description
		1: Output
5	HT1	Ouptut Huffman table 1 in output stream 0: No output 1: Output
4	HT0	Ouptut Huffman table 0 in output stream 0: No output 1: Output
3	QT3	Ouptut Quantization Table 3 in output stream 0: No output 1: Output
2	QT2	Ouptut Quantization Table 2 in output stream 0: No output 1: Output
1	QT1	Ouptut Quantization Table 1 in output stream 0: No output 1: Output
0	QT0	Ouptut Quantization Table 0 in output stream 0: No output 1: Output

43.6.4.16 Pipe Status Register (JPEGENC_PIPESTS)

Offset Address：0x5100

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															OOVF
															rw

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	OOVF	Assembly buffer overflow.

43.6.4.17 Restart Interval Control Register (JPEGENC_RICTRL)

Offset Address：0x6000

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	RIEN	BRI[27:16]
	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRI[15:0]															
rw															

Bit field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28	RIEN	Enable restart marker generation 0: disabled 1: enabled
27:0	BRI[27:0]	Number of blocks per restart interval minus one 0: 1 1: 2 ... 0xFFFFFFF: 0x10000000

43.6.4.18 Header/Footer Ram Size Register (JPEGENC_HFSIZE)

Offset Address：0xA004

Reset Value：0x0000 0400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIZE[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
r															

Bit field	Name	Description
31:0	SIZE[31:0]	Header/footer RAM size in bytes. Unit: byte

43.6.4.19 Output Buffer Size Register (JPEGENC_OBSIZE)

Offset Address：0xA024

Reset Value：0x0000 0200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OBSIZE[31:16]															

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r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OBSIZE[15:0]															

r

Bit field	Name	Description
31:0	OBSIZE[31:0]	Gives the number of bytes in the internal output buffer.

43.6.5 BRC Register

Base Address：0x5009 0000

43.6.5.1 BRC Initialization Register (JPEGBRC_INIT)

Offset Address：0x00

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											INITF	Reserved		BUSY	INIT
											rw			rw	rw

Bit field	Name	Description
31:5	Reserved	Reserved,the reset value must be maintained
4	INITF	Initialization completion flag This bit indicates that all transactions on the AXI interface have been completed after the following "INIT" bit is set to 1. If "INIT" is set to 0 before this bit is set to 1, a protocol violation may occur on the AXI bus, which may have a negative impact on the overall system. Once "INIT" is set to 0, this field is also set to 0.
3:2	Reserved	Reserved,the reset value must be maintained
1	BUSY	If it is set to 1 and bit[0] is set to high, bit[4] is immediately set to high.
0	INIT	If set to 1, the internal state of the core is reset. After writing a 1, the user needs to set it back to 0 if it needs to be reset again (rising edge control). *Note: This does not affect the state of any user-facing registries*

43.6.5.2 BRC Enable Register (JPEGBRC_EN)

Offset Address：0x04

Reset Value：0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable BRC 0: Disabled 1: Enabled *Note: If set to 0, input data is not accepted and output data is not generated.*

43.6.5.3 AXI Buffer Base Address Register (JPEGBRC_BUFBADD)

Offset Address：0x08

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit field	Name	Description
31:0	ADDR[31:0]	AXI buffer base address This must be aligned on 8 sample boundaries. I.e. the address must be the “Implemented AXI Maximum Burst Length” After setting this register, the kernel needs to be initialized by setting bit [0] of the “JPEGBRC_INIT” register to 1 before entering the input samples into the BRC.

43.6.5.4 AXI Buffer Size Register (JPEGBRC_BUFSIZE)

Offset Address：0x0C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	SIZE[15:0]	AXI buffer size The value written here is the number of 8x8 blocks in the buffer. To calculate the number of bytes that the core will use for a given value written here, use the following expression: $Buffer_{bytes} = SIZE*64$ For the calculation of the expression, please refer to Section 43.5.5.4. *Note: size of SIZE must be a power of 2.* After setting this register, the kernel needs to be initialized by setting bit [0] of the "JPEGBRC_INIT" register to 1 before inputting the input samples into the BRC.

43.6.5.5 Up Sampling Mode Register (JPEGBRC_USMODE)

Offset Address：0x44

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														MODE[1:0]	
														rw	

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1:0	MODE[1:0]	Up sampling mode Specifies the upsampling mode. If it is set to 0, no upsampling is performed. Refer to Section 43.5.5.5 above for other modes. *Note: When using the MCU's built-in LCDC display, this bit is required to upsample YUV420 format to YUV422 format.*

43.6.6 RBC Register

Base Address：0x5007 0000

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43.6.6.1 RBC Initialization Register (JPEGRBC_INIT)

Offset Address：0x00

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											INITF	Reserved			INIT
											r				rw

Bit field	Name	Description
31:5	Reserved	Reserved,the reset value must be maintained
4	INITF	Initialization completion flag This bit signals that all transactions have been completed on the AXI interface after the following “INIT” bit is set to 1. If “INIT” is set to 0 before this bit is set to 1, a protocol violation may occur on the AXI bus, which may have a negative impact on the overall system. Once “INIT” is set to 0, this field is also set to 0.
3:1	Reserved	Reserved,the reset value must be maintained
0	INIT	If set to 1, the core internal state is reset. After a 1 has been writen, the user needs to set it back to 0 if another reset is desired rising edge controled. *Note: This does not affect the state of any user-facing registry*

43.6.6.2 RBC Enable Register (JPEGRBC_EN)

Offset Address：0x04

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EN
															rw

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	EN	Enable RBC

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Bit field	Name	Description
		0: Disabled 1: Enabled *Note: If set to 0, input data is not accepted and output data is not generated.*

43.6.6.3 Switch Input Sample Order Register (JPEGRBC_SWITCH)

Offset Address：0x08

Reset Value：0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															SWITCH
															rw

Bit field	Name	Description
31:1	Reserved	Reserved,the reset value must be maintained
0	SWITCH	Enable switch input sample order If set to 0, the first sample extracted from the input data word is on the MSB If set to 1, the first sample is extracted from the LSB of this input data word.

43.6.6.4 Frame Width Register (JPEGRBC_FRMW)

Offset Address：0x0C

Reset Value：0x0003 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIDTH[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	WIDTH[15:0]	Input frame width in pixels. Actual size formula: Non-interlaced and monochrome: WIDTH Interlaced 4:4:4: WIDTH * 3

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Bit field	Name	Description
		Interlaced 4:2:2: WIDTH * 2 Interlaced 4:2:0: WIDTH * 3

43.6.6.5 Frame Height Register (JPEGRBC_FRMH)

Offset Address：0x10

Reset Value：0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEIGHT[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:0	HEIGHT[15:0]	Input frame height in pixels. 0: 1 1: 2 ... 0xFFFF: 0x10000

43.6.6.6 Pixel Format Register (JPEGRBC_PFORM)

Offset Address：0x18

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													FORMAT[2:0]		
													rw		

Bit field	Name	Description
31:3	Reserved	Reserved,the reset value must be maintained
2:0	FORMAT[2:0]	Pixel format. The following values may be written to this register: 0x0: 4:4:4 non-interleaved format

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Bit field	Name	Description
		0x1: 4:2:2 non-interleaved format 0x2: 4:20 non-interleaved format 0x3: monochrome 0x4: 4:4:4 interleaved 0x5: 4:2:2 interleaved 0x6: 4:2:0 interleaved 0x7: reserved

43.6.6.7 Component Names Register (JPEGRBC_CNAME)

Offset Address：0x1C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								C2[7:0]							
								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1[7:0]								C0[7:0]							
rw								rw							

Bit field	Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
23:16	C2[7:0]	Component names
15:8	C1[7:0]	Component names
7:0	C0[7:0]	Component names

43.6.6.8 Component 0 Start Address Register (JPEGRBC_C0SADD)

Offset Address：0x20

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit field	Name	Description
31:0	ADDR[31:0]	Start address of buffer in the AXI memory.

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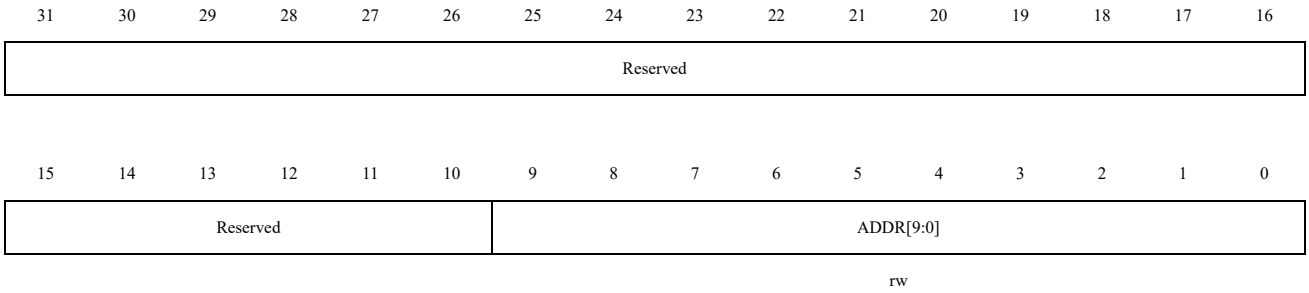
Bit field	Name	Description
		This must be aligned on an 8 sample boundary. It means the address must be a multiple of 8.

43.6.6.9 Component 0 End Address Register (JPEGRBC_C0EADD)

Offset Address：0x24

Reset Value：0x0000 0000

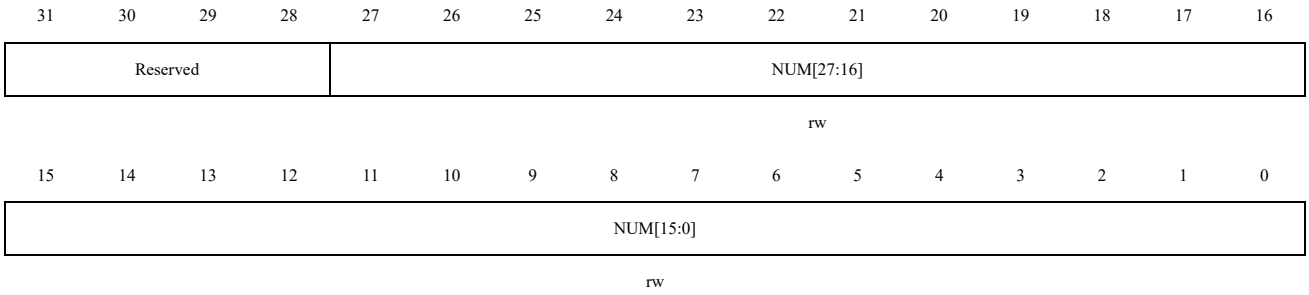


Bit field	Name	Description
31:10	Reserved	Reserved,the reset value must be maintained
9:0	ADDR[9:0]	Size of buffer in the AXI memory. 0: 1 1: 2 … 0x3FF: 0x400.

43.6.6.10 Blocks Of Per Scan 0 Register (JPEGRBC_BPS0)

Offset Address：0x60

Reset Value：0x0000 0000



Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:0	NUM[27:0]	Number of blocks in Scan 0. Formula: Non-interleaved,mono: (JPEGRBC_FRMW.WIDTH/8) * (JPEGRBC_FRMH.HEIGHT/8) - 1 Interleaved 4:4:4: (JPEGRBC_FRMW.WIDTH/8) * (JPEGRBC_FRMH.HEIGHT/8)*3 - 1

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Bit field	Name	Description
		Interleaved 4:2:2: (JPEGRBC_FRMW.WIDTH/16) * (JPEGRBC_FRMH.HEIGHT/8)*4 - 1 Interleaved 4:2:0: (JPEGRBC_FRMW.WIDTH/16) * (JPEGRBC_FRMH.HEIGHT/16)*6 – 1 0: 1 block 1: 2 blocks ... 0xFFFFFFF : 0x10000000 blocks

43.6.6.11 Blocks Of Per Scan 1 and 2 Register (JPEGRBC_BPS12)

Offset Address：0x64

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				NUM[27:16]											
				rw											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUM[15:0]															
rw															

Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:0	NUM[27:0]	Number of blocks in Scan 1, 2. Formula: Non-interlaced 4:4:4: (JPEGRBC_FRMW.WIDTH/8) * (JPEGRBC_FRMH.HEIGHT/8) - 1 Non-interlaced 4:2:2: (JPEGRBC_FRMW.WIDTH/16) * (JPEGRBC_FRMH.HEIGHT/8) - 1 Non-interlaced 4:2:0: (JPEGRBC_FRMW.WIDTH/16) * (JPEGRBC_FRMH.HEIGHT/16) - 1 Mono:(JPEGRBC_FRMW.WIDTH/8) * (JPEGRBC_FRMH.HEIGHT/8) - 1 Interlaced 4:4:4: (JPEGRBC_FRMW.WIDTH/8) * (JPEGRBC_FRMH.HEIGHT/8)*3 - 1 Interlaced 4:2:2: (JPEGRBC_FRMW.WIDTH/16) * (JPEGRBC_FRMH.HEIGHT/8)*4 - 1 Interlaced 4:2:0: (JPEGRBC_FRMW.WIDTH/16) * (JPEGRBC_FRMH.HEIGHT/16)*6 – 1 0: 1 block 1: 2 blocks ... 0xFFFFFFF : 0x10000000 blocks

43.6.6.12 Rows Scan 0 Register (JPEGRBC_ROWS0)

Offset Address：0x68

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			NUM[12:0]												
			rw												

Bit field	Name	Description
31:13	Reserved	Reserved,the reset value must be maintained
12:0	NUM[12:0]	Number of rows in Scan 0. Formula: Interleaved 4:2:0: (JPEGRBC_FRMH.HEIGHT/16) - 1 Other: (JPEGRBC_FRMH.HEIGHT/8) - 1 0:1 block 1:2 block ... 0x1FFF : 0x2000 block

43.6.6.13 Rows Scan 1 And 2 Register (JPEGRBC_ROWS12)

Offset Address：0x6C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ROWS12[12:0]												
			rw												

Bit field	Name	Description
31:13	Reserved	Reserved,the reset value must be maintained
12:0	ROWS12[12:0]	Number of rows in Scan 1, 2. Formula: Non-interlaced 4:4:4 : (JPEGRBC_FRMH.HEIGHT/8) - 1 Non-interlaced 4:2:2 : (JPEGRBC_FRMH.HEIGHT/8) - 1 Non-interlaced 4:2:0 : (JPEGRBC_FRMH.HEIGHT/16) - 1 Interlaced 4:2:0： (JPEGRBC_FRMH.HEIGHT/16) – 1 Others：(JPEGRBC_FRMH.HEIGHT/8) – 1 0: 1 block

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Bit field	Name	Description
		1: 2 blocks ... 0x1FFF: 0x2000 blocks

43.6.6.14 Frame Height Half Register (JPEGRBC_HHALF)

Offset Address：0x70

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	HHALF[14:0]														
	rw														

Bit field	Name	Description
31:15	Reserved	Reserved,the reset value must be maintained
14:0	HHALF[14:0]	Height of the input frame counted in pixels divided by 2. (JPEGRBC_FRMH.HEIGHT/2)-1 0: 1 block 1: 2 blocks ... 0x7FFF: 0x8000 blocks

43.6.6.15 Block Line Stride Scan 0 Register (JPEGRBC_BLSS0)

Offset Address：0x74

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														SIZE[17:16]	
														rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
rw															

Bit field	Name	Description
31:18	Reserved	Reserved,the reset value must be maintained
17:0	SIZE[17:0]	Size of one line inside a block line in buffer in bytes for Scan 0.

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Bit field	Name	Description
		Formula: Non-interlaced and mono: JPEGRBC_FRMW.WIDTH/8*8 Interlaced 4:4:4: JPEGRBC_FRMW.WIDTH/8*8 * 3 Interlaced 4:2:2: JPEGRBC_FRMW.WIDTH/16*8 * 4 Interlaced 4:2:0: JPEGRBC_FRMW.WIDTH/16*8 * 6

43.6.6.16 Block Line Stride Scan 1 And 2 Register (JPEGRBC_BLSS12)

Offset Address：0x78

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														SIZE[17:16]	
														rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
rw															

Bit field	Name	Description
31:18	Reserved	Reserved,the reset value must be maintained
17:0	SIZE[17:0]	Size of one line inside a block line in buffer in bytes for Scan 1, 2. Formula: Non-interleaved 4:4:4 & Mono: JPEGRBC_FRMW.WIDTH/8*8 Non-interleaved 4:2:2 & 4:2:0: JPEGRBC_FRMW.WIDTH/16*8 Interleaved 4:4:4: JPEGRBC_FRMW.WIDTH/8*8 * 3 Interleaved 4:2:2: JPEGRBC_FRMW.WIDTH/16*8 * 4 Interleaved 4 :2:0: JPEGRBC_FRMW.WIDTH/16*8 * 6

43.6.6.17 Blocks Of Per Row Scan 0 Register (JPEGRBC_BPRS0)

Offset Address：0x7C

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	NUM[14:0]														
	rw														

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Bit field	Name	Description
31:15	Reserved	Reserved,the reset value must be maintained
14:0	NUM[14:0]	Number of blocks in a block line for Scan 0. Formula: Non-interlaced and mono: JPEGRBC_FRMW.WIDTH/8 -1 Interlaced 4:4:4: JPEGRBC_FRMW.WIDTH/8 * 3 - 1 Interlaced 4:2:2: JPEGRBC_FRMW.WIDTH/16 * 4 - 1 Interlaced 4:2:0: JPEGRBC_FRMW.WIDTH/16 * 6 - 1 1

43.6.6.18 Blocks Of Per Row Scan 1 and 2 Register (JPEGRBC_BPRS12)

Offset Address：0x80

Reset Value：0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	NUM[14:0]														
rw															

Bit field	Name	Description
31:15	Reserved	Reserved,the reset value must be maintained
14:0	NUM[14:0]	Number of blocks in a block line for Scan 1, 2. Formula: Non-interlaced 4:4:4 & mono: JPEGRBC_FRMW.WIDTH/8 - 1 Non-interlaced 4:2:2 & 4:2:0: JPEGRBC_FRMW.WIDTH/16 - 1 Interlaced 4:4:4: JPEGRBC_FRMW.WIDTH/8 * 3 - 1 Interlaced 4:2:2: JPEGRBC_FRMW. WIDTH/16 * 4 - 1 Interleaved 4:2:0: JPEGRBC_FRMW.WIDTH/16 * 6 - 1

43.6.6.19 Maximum Supported Width Register (JPEGRBC_MAXW)

Offset Address：0x84

Reset Value：0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WIDTH[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIDTH[15:0]															
r															

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Bit field	Name	Description
31:0	WIDTH[31:0]	Maximum supported width

43.6.6.20 Maximum Supported Height Register (JPEGRBC_MAXH)

Offset Address：0x88

Reset Value：0x0001 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HEIGHT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEIGHT[15:0]															
r															

Bit field	Name	Description
31:0	HEIGHT[31:0]	Maximum supported height

43.6.6.21 Maximum Supported Buffer Size Register (JPEGRBC_MBSIZE)

Offset Address：0x8C

Reset Value：0x0000 FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SIZE[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE[15:0]															
r															

Bit field	Name	Description
31:0	SIZE[31:0]	Specifies the maximum number of block lines that can be set in JPEGRBC_C0EADD.ADDR.

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44 LCDC display controller(LCDC)

44.1 Introduction

The LCD display controller provides a parallel digital RGB(red, green, blue) and signals for horizontal, vertical synchronization, pixel clock and data enable as output to interface directly to a variety of LCD and TFT panels .

44.2 Main Features

The main features supported by LCDC are shown below:

- 24-bit RGB parallel pixel output; 8bits-per-pixel(RGB888)
- 4 display layers with dedicated FIFO(256x64-bit)
- Color look-up table(CLUT) up to 256 color(256x24-bit) per layer.
- 7 input color formats selectable per layer :
  - ARGB8888
  - ABGR8888
  - RGBA8888
  - BGRA8888
  - RGB888
  - RGB565
  - BGR565
- user-defined pixel formats(pixel formats size needs to be a multiple of byte) are also available, for example:
  - L8 (8-bit luminance or CLUT)
  - AL44 (4-bit alpha + 4-bit luminance)
  - AL88(8-bit alpha + 8-bit luminance)
  - ARGB1555
  - .....
- Pseudo-random dithering output for low bits per channel
  - Dither width 2 bits for red, green, blue
- Flexible blending between layers using alpha value(per pixel or constant)
- Color keying(transparency color)
- Programming window posizition and size
- Gamma correction

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- Scaling option
- Horizontal mirroring
- Vertical flip
- Dual view

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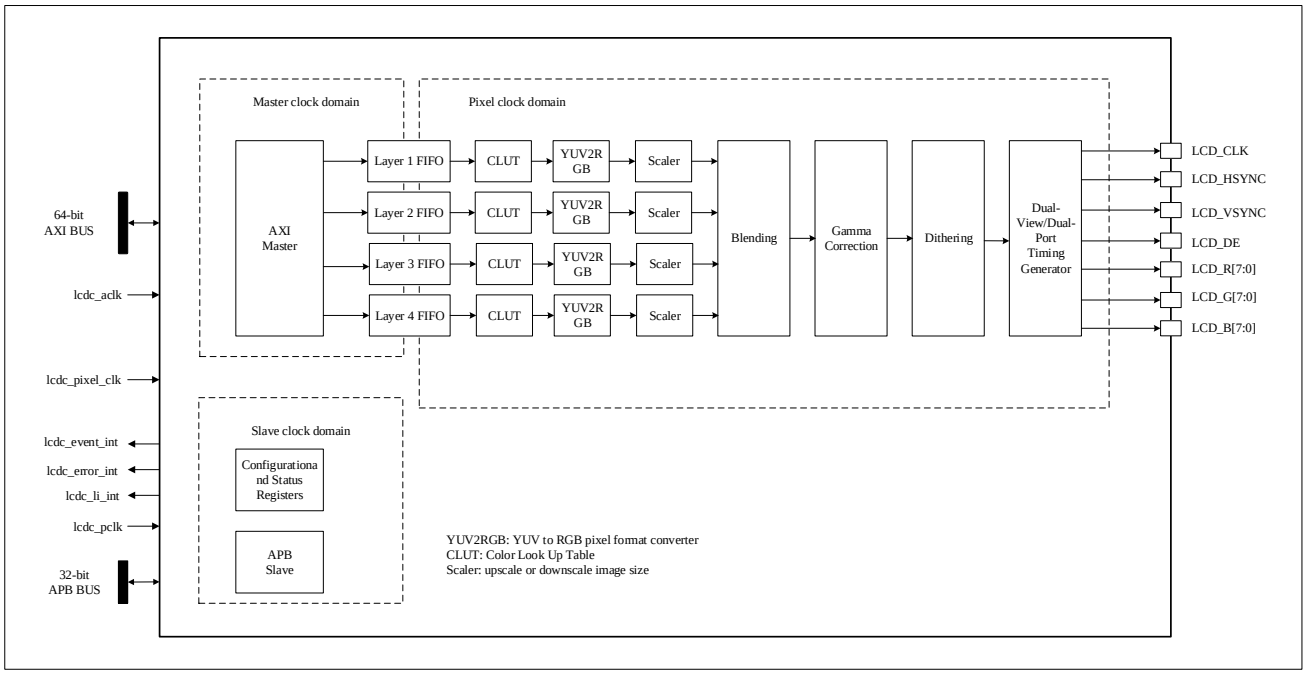
44.3 LCDC function descripition

44.3.1 Block diagram

Figure 44-1 Block diagram



44.3.2 LCDC pins and internal signals

Table 44-1 LCDC external pins

LCD-TFT signals	Signal type	Description
LCD_CLK	Output	Clock output
LCD_HSYNC	Output	Horizontal synchronization
LCD_VSYNC	Output	Vertical synchronization
LCD_DE	Output	Not data enable
LCD_R[7:0]	Output	8-bit red data
LCD_G[7:0]	Output	8-bit green data
LCD_B[7:0]	Output	8-bit blue data

The LCDC pins must be configured by the user application. The unused pins can be used for other puroses.

For LCDC outputs up to 24 bits (RGB888), if less than 8 bpp are used to output for example RGB565 to interface on 16-bit displays, the RGB display data lines must be connected to the MSB of the LCDC RGB data lines.

As an example, in the case of an LCDC interfacing with a RGB565 16-bit display, the LCDC display R[4:0], G[5:0] and B[4:0] data lines pins must be connected to the LCD_R[7:3], LCD_G[7:2] and LCD_B[7:3] pins.

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Table 44-2 LCDC internal signals

Names	Signal type	Description
lcdc_axi_clk	Input	LCDC AXI clock
lcdc_pixel_clk	Input	LCDC kernel clock used for LCD_CLK (pixel clock) generation
lcdc_event_int	Output	LCDC global interrupt
lcdc_error_int	Output	LCDC global error interrupt
lcdc_li_int	Output	LCDC line interrupt
lcdc_pclk	Input	LCDC APB clock for register access

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44.4 LCDC programmable paramters

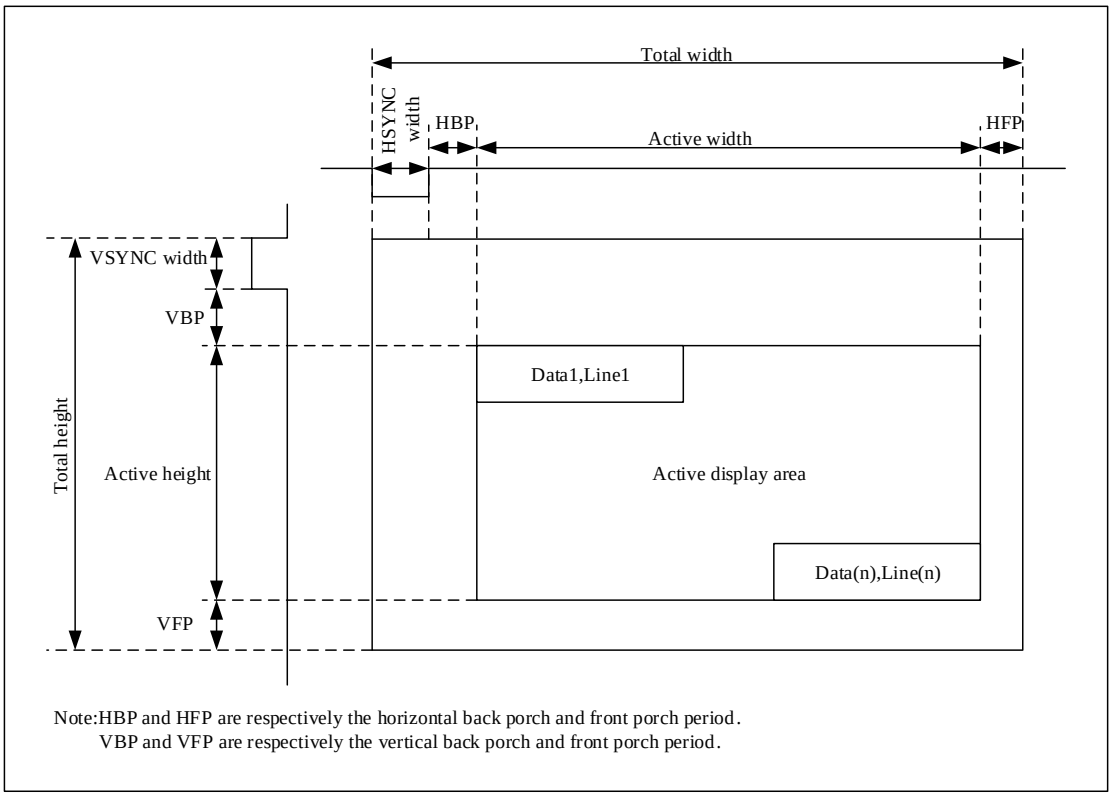
The LCDC controller provides flexible configurable paramters. It can be enabled or disabled through the LCDC_GCTRL register.

44.4.1 LCDC global configuration paramters

Synchronous timings

The figure below presents the configurable timing parameters generated by the synchronous timings generator block presented in the block diagram Figure 44-1. It generates the horizontal and vertical synchronization timings panel signals, the pixel clock and the data enable signals.

Figure 44-2 LCDC synchronous timings



The LCDC programmable synchronous timings are following:

- HSYNC and VSYNC width: horizontal and vertical synchronization width, configured by programming a value of HSYNC width - 1 and VSYNC width - 1 in the LCDC_SYNCCTRL register.
- HBP and VBP: horizontal and vertical synchronization back porch width, configured by programming the accumulated value HSYNC width + HBP – 1 and the accumulated value VSYNC width + VBP – 1 in the LCDC_BPCTRL register.
- Active width and active height: the active width and active height are configured by programming the accumulated value HSYNC width + HBP + active width – 1 and the VSYNC width + VBP + active height – 1

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in the LCDC_AWCTRL register.

- Total width : the total width is configured by programming the accumulated value HSYNC width + HBP + active width + HFP – 1 in the LCDC_TWCTRL register. The HFP is the horizontal front porch period.
- Total height : the total height is configured by programming the accumulated value VSYNC width + VBP + active height + VFP – 1 in the LCDC_TWCTRL register. The VFP is the vertical front porch period.

44.4.1.1 Example of synchronous timings configuration

LCDC timings(must be extracted from panel datasheet):

- Horizontal and vertical synchronization width: 0xA pixels and 0x2 lines.
- Horizontal and vertical back porch: 0x14 pixels and 0x2 lines.
- Active width and active height: 0x140 pixels, 0xF0 lines(320x240).
- Horizontal front porch: 0xA pixels.
- Vertical front porch: 0x4 lines.

The programmed values in the LCDC timings register are:

- LCDC_SYNCCTRL register to be programmed to 0x00090001

  (HSW[15:0] is 0x9 and VSH[15:0] is 0x1)
- LCDC_BPCTRL register to be programmed to 0x001D0003

  (AHBP[15:0] is 0x1D(0xA + 0x13) and AVBP[15:0] is 0x3(0x2 + 0x1))
- LCDC_AWCTRL register to be programmed to 0x015D00F3

  (AAW[15:0] is 0x15D(0xA + 0x14 + 0x13F) and AAH[15:0] is 0xF3(0x2 + 0x2 + 0xEF))
- LCDC_TWCTRL register to be programmed to 0x00000167

  (TOTALW[15:0] is 0x167(0xA + 0x14 + 0x140 + 0x9))
- LCDC_TWCTRL register to be programmed to 0x000000F7

  (TOTALH[15:0] is 0xF7(0x2 + 0x2 + 0xF0 + 0x3))

44.4.1.2 Programmable polarity

The horizontal and vertical synchronization, data enable and pixel clock output signals polarity can be programmed to active high or active low through the LCDC_GCTRL register.

44.4.1.3 Background color

A constant background coloe(RGB888) can programmed through the LCDC_BCCTRL register. It is used for blending with the bottom layer.

44.4.1.4 Dithering

The dithering pseudo-random technique using an LFSR is used to add a small random value(threshold) to each pixel color channel(R, G or B) value, thus rounding up the MSB in some cases when displaying a 24-bit data on 18-bit display. Thus the dithering technique is used to round data which is different from one frame to the other.

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The dithering pseudo-random technique is the same as comparing LSBs against a threshold value and adding a 1 to the MSB part only, if the LSB part is ≥ the threshold. The LSBs are typically dropped once dithering was applied.

The width of the added pseudo-random value is two bits for each color channel: two bits for red, two bits for green and two bits for blue.

Once the LCDC is enabled, the LFSR starts running with the first active pixel and it id kept running even during blanking periods and when dithering is switched off, If the LCDC is disabled, the LFSR is reset.

The dithering can be switched on and odd on the fly through the LCDC_GCTRL register.

44.4.1.5 Reload shadow registers

Some configuration registers are shadowed. The shadow registers values can be reloaded immediately to the active registers when writing to these registers or at the beginning of the vertical blanking period following the configuration in the LCDC_SRCTRL register. If the immediate reload configuration is selected, the reload must be activated only when all new registers have been written.

The shadow registers must not be modified again before the reload is done. Reading from the shadow registers returns the actual value. The new written value can only be read after the reload has taken place.

A register reload interrupt can be generated if enabled in the LCDC_INTEN register.

The shadowed registers are all Layerx registers except LCDC_CLUTWR.

44.4.1.6 Interrupt generation event

Refer to section 44.5 for the interrupt configuration.

44.4.2 Layer programmable parameters

Up to four layers can be enabled, disabled and configured separately.The layer display order is fixed and it is bottom up. If four layers are enabled, the layer 4 is the top displayed window.

44.4.2.1 Windowing

Every layer can be posizitioned and resized and it must be inside the active display area.

The window position and size are configured through the top-left and bottom-right X/Y positions and the internal timing generator that includes the synchronous, back porch size and the active data area. Refer to LCDC_WHPCTRL and LCDC_WVPCTRL registers.

The programmable layer position and size defines the first/last visible pixel of a line and the first/last visible line in the window. It allows to diplay either the full image frame or only a part of the image frame(see Figure 44-3):

- The first and the last visiable pixel in the layer are set by configuring the WHSTPOS[15:0] and WHSPPOS[15:0] in the LCDC_WHPCTRL register.
- The first and the last visiable line in the layer are set by configuring the WVSTPOS[15:0] and WVSPPOS[15:0] in the LCDC_WVPCTRL register.

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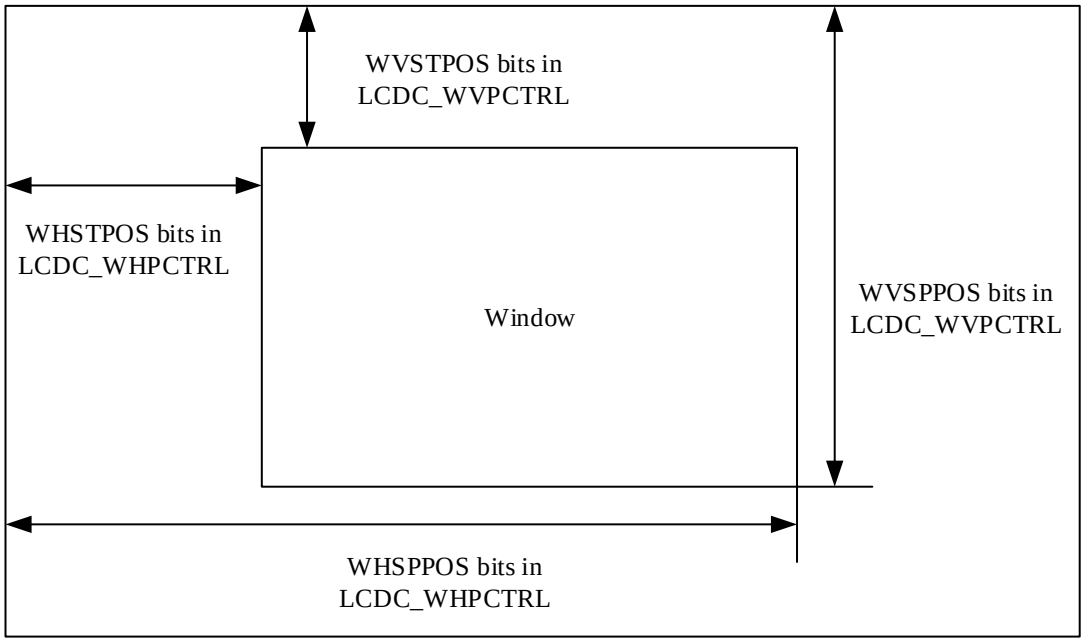
Figure 44-3 Layer window programmable parameters



44.4.2.2 Pixel input format

The programmable pixel format is used for the data stored in the frame buffer of a layer.

Up to seven pre-defined input pixel formats can be configured for every layer through the LCDC_PFCTRL register.

The pixel data is read from the frame buffer and then transformed to the internal 8888(ARGB) format as fllows:

components having a width of less than 8 bits get expanded to 8 bits by bit replication. The selected bit range is concatenated multiple times until it is longer than 8 bits. Of the resulting vector, the 8 MSB bits are chosen. Example: 5 bits of an RGB565 red channel become (bit positions) 4 3 2 1 0 4 3 2 (the three LSBs are filled with the three MSBs of the five bits)

The table below describes the pixel data mapping depending on the selected format.

Table 44-3 Pixel data mapping versus color format

ARGB8888			
@+3 A_x[7:0]	@+2 R_x[7:0]	@+1 G_x[7:0]	@ B_x[7:0]
@+7 A_{x+1}[7:0]	@+6 R_{x+1}[7:0]	@+5 G_{x+1}[7:0]	@+4 B_{x+1}[7:0]
ABGR8888			
@+3	@+2	@+1	@

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A_x[7:0]	B_x[7:0]	G_x[7:0]	R_x[7:0]
@+7 A_{x+1}[7:0]	@+6 B_{x+1}[7:0]	@+5 G_{x+1}[7:0]	@+4 R_{x+1}[7:0]
RGBA8888			
@+3 R_x[7:0]	@+2 G_x[7:0]	@+1 B_x[7:0]	@ A_x[7:0]
@+7 R_{x+1}[7:0]	@+6 G_{x+1}[7:0]	@+5 B_{x+1}[7:0]	@+4 A_{x+1}[7:0]
BGRA8888			
@+3 B_x[7:0]	@+2 G_x[7:0]	@+1 R_x[7:0]	@ A_x[7:0]
@+7 B_{x+1}[7:0]	@+6 G_{x+1}[7:0]	@+5 R_{x+1}[7:0]	@+4 A_{x+1}[7:0]
RGB565			
@+3 R_{x+1}[4:0]G_{x+1}[5:3]	@+2 G_{x+1}[2:0]B_{x+1}[4:0]	@+1 R_x[4:0]G_x[5:3]	@ G_x[2:0]B_x[4:0]
@+7 R_{x+3}[4:0]G_{x+3}[5:3]	@+6 G_{x+3}[2:0]B_{x+3}[4:0]	@+5 R_{x+2}[4:0]G_{x+2}[5:3]	@+4 G_{x+2}[2:0]B_{x+2}[4:0]
BGR565			
@+3 B_{x+1}[4:0]G_{x+1}[5:3]	@+2 G_{x+1}[2:0]R_{x+1}[4:0]	@+1 B_x[4:0]G_x[5:3]	@ G_x[2:0]R_x[4:0]
@+7 B_{x+3}[4:0]G_{x+3}[5:3]	@+6 G_{x+3}[2:0]R_{x+3}[4:0]	@+5 B_{x+2}[4:0]G_{x+2}[5:3]	@+4 G_{x+2}[2:0]R_{x+2}[4:0]
RGB888			
@+3 B_{x+1}[7:0]	@+2 R_x[7:0]	@+1 G_x[7:0]	@ B_x [7:0]

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@+7 G_{x+2}[7:0]	@+6 R_{x+2}[7:0]	@+5 R_{x+1}[7:0]	@+4 G_{x+1}[7:0]
L8			
@+3 L_{x+3}[7:0]	@+2 L_{x+2}[7:0]	@+1 L_{x+1}[7:0]	@ L_x [7:0]
@+7 L_{x+7}[7:0]	@+6 L_{x+6}[7:0]	@+5 L_{x+5}[7:0]	@+4 L_{x+4}[7:0]
AL44			
@+3 A_{x+3}[3:0]L_{x+3}[3:0]	@+2 A_{x+2}[3:0]L_{x+2}[3:0]	@+1 A_{x+1}[3:0]L_{x+1}[3:0]	@ A_x[3:0]L_x[3:0]
@+7 A_{x+7}[3:0]L_{x+7}[3:0]	@+6 A_{x+6}[3:0]L_{x+6}[3:0]	@+5 A_{x+5}[3:0]L_{x+5}[3:0]	@+4 A_{x+4}[3:0]L_{x+4}[3:0]
AL88			
@+3 A_{x+1}[7:0]	@+2 L_{x+1}[7:0]	@+1 A_x[7:0]	@ L_x[7:0]
@+7 A_{x+3}[7:0]	@+6 L_{x+3}[7:0]	@+5 A_{x+2}[7:0]	@+4 L_{x+2}[7:0]

44.4.2.3 Color look-up table(CLUT)

The CULT can be enabled at run-time for every layer through the LCDC_LCTRL register and it is only useful in case of indexd color when using the L8, AL44 and AL88 input pixel format.

First, the CLUT must be loaded with the R, G and B values that replace the original R, G, B values of that pixel (indexed color). Each color (RGB value) has its own address that is the position within the CLUT.

The R, G and B values and their own respective address are programmed through the LCDC_CLUTWR register:

- In case of L8 and AL88 input pixel format, the CLUT must be loaded by 256 colors. The address of each color is configured in the ADDR bits in the LCDC_CLUTWR register.
- In case of AL44 input pixel format, the CLUT must be loaded by only16 colors. The address of each color must be filled by replicating the 4-bit L channel to 8-bit as follows:
  - L0 (indexed color 0), at address 0x00

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- L1, at address 0x11
- L2, at address 0x22
- .....
- L15, at address 0xFF

44.4.2.4 Color frame buffer address

Every layer has a start address for the color frame buffer configured through the LCDC_CFBADDR register.

When a layer is enabled, the data is fetched from the color frame buffer.

44.4.2.5 Color frame buffer length

Every layer has a total line length setting for the color frame buffer in bytes and a number of lines in the frame buffer configurable in the LCDC_CFBLEN and LCDC_CFBLNUM register respectively.

The line length and the number of lines settings are used to stop the prefetching of data to the layer FIFO at the end of the frame buffer:

- If it is set to less bytes than required, a FIFO underrun interrupt is generated if it has been previously enabled.
- If it is set to more bytes than actually required, the useless data read from the FIFO is discarded. The useless data is not displayed.

44.4.2.6 Color frame buffer pitch

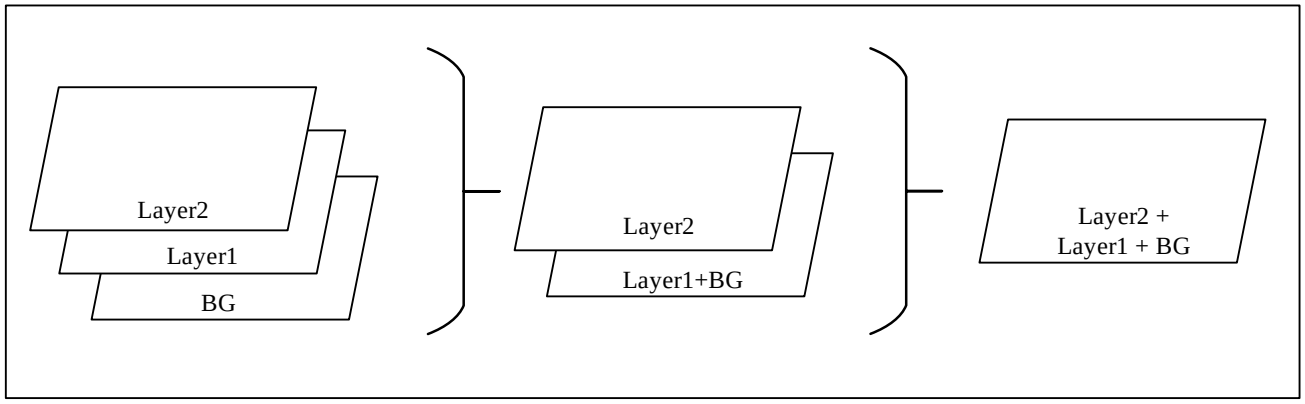
Every layer has a configurable pitch for the color frame buffer, that is the distance between the start of one line and the beginning of the next line in bytes. It is configured through the LCDC_CFBLEN register.

44.4.2.7 Layer blending

The blending is always active and the two layers can be blended following the blending factors configured through the LCDC_BFCTRL register.

The blending order is fixed and it is bottom up. If two layers are enabled, first the Layer1 is blended with the Background color, then the layer2 is blended with the result of blended color of layer1 and the background. Refer to the figure below.

Figure 44-4 Blending two layers with background



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44.4.2.8 Default color

Every layer can have a default color in the format ARGB which is used outside the defined layer window or when a layer is disabled.

The default color is configured through the LCDC_DCCTRL register.

The blending is always performed between the two layers even when a layer is disabled. To avoid displaying the default color when a layer is disabled, keep the blending factors of this layer in the LCDC_BFCTRL register to their reset value.

44.4.2.9 Color keying

A color key (RGB) can be configured to be representative for a transparent pixel.

If the color keying is enabled, the current pixels (after format conversion and before CLUT respectively blending) are compared to the color key. If they match for the programmed RGB value, all channels (ARGB) of that pixel are set to 0.

The color key value can be configured and used at run-time to replace the pixel RGB value.

The color keying is enabled through the LCDC_CKCTRL register.

The color keying is configured through the LCDC_CKCTRL register. The programmed value depends on the pixel format as it is compared to current pixel after pixel format conversion to ARGB8888.

Example: if the a mid-yellow color (50 % red + 50 % green) is used as the transparent color key:

- In RGB565, the mid-yellow color is 0x8400. Set the LCDC_CKCTRL to 0x848200.
- In ARGB8888, the mid-yellow color is 0x808000. Set LCDC_CKCTRL to 0x808000.
- In all CLUT-based color modes (L8, AL88, AL44), set one of the palette entry to the mid-yellow color 0x808000 and set the LCDC_CKCTRL to 0x808000.

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44.5 LCDC interrupts

The LCDC provides four maskable interrupts logically ORed to two interrupt vectors.

The interrupt sources can be enabled or disabled separately through the LCDC_INTEN register. Setting the appropriate mask bit to 1 enables the corresponding interrupt.

The two interrupts are generated on the following events:

- Line interrupt: generated when a programmed line is reached. The line interrupt position is programmed in the LCDC_LINTPCTRL register.
- Register reload interrupt: generated when the shadow registers reload is performed during the vertical blanking period.
- FIFO underrun interrupt: generated when a pixel is requested from an empty layer FIFO.
- Transfer error interrupt: generated when an bus error occurs during data transfer.

These interrupt events are connected to the NVIC controller as described in the figure below.

Figure 44-5 Interrupt events

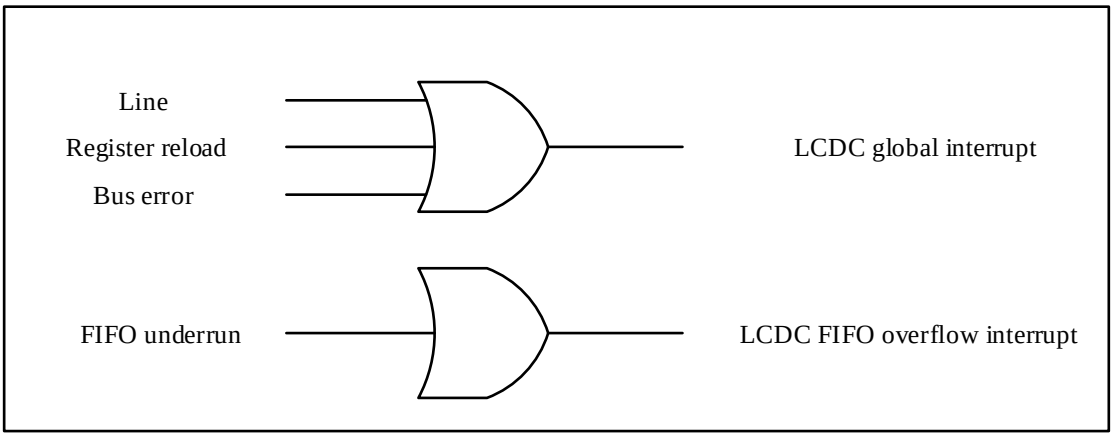

Table 44-4 LCDC interrupt requests

Interrupt event	event flag	Enable conctrol bit
Line	LIF	LIEN
FIFO underrun	FUIF	FUIEN
Bus error	BEIF	BEIEN
Register reload	RRIF	RRIEN

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44.6 LCDC programming procedure

The steps listed below are needed to program the LTDC:

1. Enable the LTDC clock in the RCC register.
2. Configure the required pixel clock following the panel datasheet.
3. Configure the synchronous timings: VSYNC, HSYNC, vertical and horizontal back porch, active data area and the front porch timings following the panel datasheet as described in the 44.4.1.
4. Configure the synchronous signals and clock polarity in the LCDC_GCTRL register.
5. If needed, configure the background color in the LCDC_BCCTRL register
6. Configure the needed interrupts in the LCDC_INTEN and LTDC_LINTPCTRL register.
7. Configure the layerx(x=1,2,3,4) parameters by:
   - Programming the layer window horizontal and vertical position in the LCDC_WHPCTRL and LCDC_WVPCTRL registers. The layer window must be in the active data area.
   - Programming the pixel input format in the LCDC_PFCTRL register.
   - Programming the color frame buffer start address in the LCDC_CFBADDR register.
   - Programming the line length and pitch of the color frame buffer in the LCDC_CFBLEN register.
   - Programming the number of lines of the color frame buffer in the LCDC_CFBLNUM register.
   - If needed, loading the CLUT with the RGB values and its address in the LCDC_CLUTWR register.
   - If needed, configuring the default color and the blending factors respectively in the LCDC_DCCTRL and LCDC_BFCTRL registers.
8. Enable layerx(x=1,2,3,4) and if needed the CLUT in the LCDC_LCTRL register.
9. If needed, enable dithering and color keying respectively in the LCDC_GCTRL and LCDC_CKCTRL registers. They can be also enabled on the fly.
10. Reload the shadow registers to active register through the LCDC_SRCTRL register.
11. Enable the LCDC controller in the LCDC_GCTRL register.
12. All layer parameters can be modified on the fly except the CLUT. The new configuration must be either reloaded immediately or during vertical blanking period by configuring the LCDC_SRCTRL register.

Note: All layer's registers are shadowed. Once a register is written, it must not be modified again before the reload has been done. Thus, a new write to the same register overrides the previous configuration if not yet reloaded.

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44.7 LCDC registers

44.7.1 LCDC synchronization size conctrl register (LCDC_SYNCCTRL)

Address offset: 0x08

Reset value: 0x0000 0000

This register defines the number of horizontal synchronization pixels minus 1 and the number of vertical synchronization lines minus 1. Refer to Figure 44-2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSW[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSH[15:0]															
rw															

Bit field	Name	Description
31:16	HSW[15:0]	Horizontal synchronization width (in uints of pixel clock period) These bits defines the number of horizontal synchronization pixels minus 1.
15:0	VSH[15:0]	Vertical synchronization hight (in uints of horizontal scan line) These bits defines the number of vertical synchronization lines minus 1.

44.7.2 LCDC back porch conctrl register (LCDC_BPCTRL)

Address offset: 0x0C

Reset value: 0x0000 0000

This register defines the accumulated number of horizontal synchronization and back porch pixels minus 1(HSYNC width + HBP - 1) and the accumulated number of vertical synchronization and back porch lines minus 1(VSYNC height + VBP - 1). Refer to Figure 44-2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AHBP[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AVBP[15:0]															
rw															

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Bit field	Name	Description
31:16	AHBP[15:0]	Accumulated horizontal back porch (in units of pixel clock period) These bits define the accumulated horizontal back porch width that includes the horizontal synchronization and horizontal back porch pixels minus 1. The horizontal back porch is the period between horizontal synchronization going inactive and the start of the active display part of the next scan line.
15:0	AVBP[15:0]	Accumulated vertical back porch (in uints of horizontal scan line) These bits define the accumulated vertical back porch width that includes the vertical synchronization and vertical back porch lines minus 1. The vertical back porch is the number of horizontal scan lines at a start of frame to the start of the first active scan line of the next frame.

44.7.3 LCDC active width configuration register (LCDC_AWCTRL)

Address offset: 0x10

Reset value: 0x0000 0000

This register defines the accumulated number of horizontal sync, back porch and active pixels(HSYNC width + HBP + active width - 1) and the accumulated number of vertical sync, back porch and active lines(VSYNC height + BVBP + active height - 1). Refer to Figure 44-2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AAW[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AAH[15:0]															
rw															

Bit field	Name	Description
31:16	AAW[15:0]	Accumulated active width (in units of pixel clock period) These bits define the accumulated active width which includes the horizontal synchronization, horizontal back porch and active pixels minus 1. The active width is the number of pixels in active display area of the panel scan line.
15:0	AAH[15:0]	Accumulated active height (in uints of horizontal scan line) These bits define the accumulated height which includes the vertical synchronization, vertical back porch and the active height lines minus 1. The active height is the number of active lines in the panel.

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44.7.4 LCDC total width configuration register (LCDC_TWCTRL)

Address offset: 0x14

Reset value: 0x0000 0000

This register defines the accumulated number of horizontal sync, back porch, active and front porch pixels (HSYNC width + HBP + active width + HFP - 1) and the accumulated number of vertical sync, back porch, active and front porch lines (VSYNC height + BVBP + active height + VFP - 1).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOTALW[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTALH[15:0]															
rw															

Bit field	Name	Description
31:16	TOTALW[15:0]	Total width (in units of pixel clock period) These bits defines the accumulated total width which includes the horizontal synchronization, orizontal back porch, active width and horizontal front porch pixels minus 1.
15:0	TOTALH[15:0]	Total height (in uints of horizontal scan line) These bits defines the accumulated height which includes the vertical synchronization, vertical back porch, the active height and vertical front porch height lines minus 1.

44.7.5 LCDC global control register (LCDC_GCTRL)

Address offset: 0x18

Reset value: 0x0000 2220

This register defines the global configuration of the LCDC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HSPOL	VSP0L	BPOL	PCLKPOL	Reserved											DEN
rw	rw	rw	rw												rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DRW[2:0]			Reserved	DGW[2:0]			Reserved	DBW[2:0]			Reserved		GCEN	LCDCEN
	r				r				r					rw	rw

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Bit field	Name	Description
31	HSPOL	Horizontal synchronization polarity. 0: Horizontal synchronization polarity is active low 1: Horizontal synchronization polarity is active high.
30	VSPOL	Vertical synchronization polarity. 0: Vertical synchronization polarity is active low 1: Vertical synchronization polarity is active high.
29	DEPOL	Not data enable polarity. 0: Not data enable polarity is active low. 1: Not data enable polarity is active high.
28	PCLKPOL	Pixel clock polarity. 0: Pixel clock polarity is active low. 1: Pixel clock polarity is active high.
27:17	Reserved	Reserved, the reset value must be maintained.
16	DEN	Dither enable. 0: Dither disabled. 1: Dither enable.
15	Reserved	Reserved, the reset value must be maintained.
14:12	DRW[2:0]	Dither red width. These bits return the dither red bits.
11	Reserved	Reserved, the reset value must be maintained.
10:8	DGW[2:0]	Dither green width. These bits return the dither green bits.
7	Reserved	Reserved, the reset value must be maintained.
6:4	DBW[2:0]	Dither blue width. These bits return the dither blue bits.
3:2	Reserved	Reserved, the reset value must be maintained.
1	GCEN	Gamma correction enable. 0: Gamma correction disabled. 1: Gamma correction enable. *Note: When it is disabled, the RGB data bypasses the gamma correction CLUT.*
0	EN	LCDC enable. 0: LCDC disabled. 1: LCDC enable.

44.7.6 LCDC shadow reload configuration register (LCDC_SRCTRL)

Address offset: 0x24

Reset value: 0x0000 0000

A write access to this register triggers an immediate or delayed update of the active registers from their associated shadow register values.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														VBR	IMR
														rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	VBR	Vertical blanking reload. This bit is set by software and cleared only by hardware after reload (it cannot be cleared through register write once it is set). 0: No effect. 1: The shadow registers are reloaded during the vertical blanking period (at the beginning of the first line after the active display area).
0	IMR	Immediate reload. This bit is set by software and cleared only by hardware after reload. 0: No effect. 1: The shadow registers are reloaded immediately.

44.7.7 LCDC background color conctrl register (LCDC_BCCTRL)

Address offset: 0x2C

Reset value: 0x0000 0000

This register defines the background color.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								BCR[7:0]							
								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCG[7:0]								BCB[7:0]							
rw								rw							

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:16	BCR[7:0]	These bits configure the background red value.
15:8	BCG[7:0]	These bits configure the background green value.
7:0	BCB[7:0]	These bits configure the background blue value.

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44.7.8 LCDC interrupt enable register (LCDC_INTEN)

Address offset: 0x34

Reset value: 0x0000 0000

The four available interrupts can be enabled/disabled (masked) independently in this register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RRIEN	BEIEN	FUIEN	LIEN
												rw	rw	rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	RRIEN	Register reload interrupt enable. 0: Register reload interrupt disable. 1: Register reload interrupt enable.
2	BEIEN	Bus error interrupt enable. 0: Bus error interrupt disable. 1: Bus error interrupt enable.
1	FUIEN	FIFO underrun warning interrupt enable. 0: FIFO underrun warning interrupt disable. 1: FIFO underrun warning interrupt enable.
0	LIEN	Line interrupt enable. 0: Line interrupt disable. 1: Line interrupt enable.

44.7.9 LCDC interrupt status register (LCDC_INTSTS)

Address offset: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RRIF	BEIF	FUIF	LIF
												r	r	r	r

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Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	RRIF	Register reload interrupt status. 0: No register reload interrupt generated. 1: Register reload interrupt generated when a vertical blanking reload occurs (and the first line after the active area is reached).
2	BEIF	Bus error interrupt status. 0: No Bus error interrupt generated. 1: Bus error interrupt generated, an error occurs on the AXI bus..
1	FUIF	FIFO underrun warning interrupt status. 0: No FIFO underrun warning interrupt generated. 1: FIFO underrun warning interrupt generated, if one of the layer FlFO is empty and pixel data is read from the FlFO.
0	LIF	Line interrupt status. 0: No line interrupt generated. 1: Line interrupt generated, a programmed line is reached.

44.7.10 LCDC interrupt clear register (LCDC_INTCLR)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												RRICLR	BEICLR	FUICLR	LICLR
												w	w	w	w

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	RRICLR	Clear register reload interrupt status. 0: No effect. 1: Clear register reload interrupt status.
2	BEICLR	Clear bus error interrupt status. 0: No effect. 1: Clear bus error interrupt status.
1	FUICLR	Clear FIFO underrun warning interrupt status. 0: No effect.

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Bit field	Name	Description
		1: Clear FIFO underrun warning interrupt status.
0	LICLR	Clear line interrupt status. 0: No effect. 1: Clear line interrupt status.

44.7.11 LCDC line interrupt position conctrl register (LCDC_LINTPCTRL)

Address offset: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINTP[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	LINTP[15:0]	Line interrupt position. These bits configure the line interrupt position.

44.7.12 LCDC current position status register (LCDC_CPSTS)

Address offset: 0x44

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CXPOS[15:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYPOS[15:0]															
r															

Bit field	Name	Description
31:16	CXPOS[15:0]	Current X position. These bits return the current X position.
15:0	CYPOS[15:0]	Current Y position.

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Bit field	Name	Description
		These bits return the current Y position.

44.7.13 LCDC current display status register (LCDC_CDSTS)

Address offset: 0x48

Reset value: 0x0000 0003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												HSYNCS	VSYNCS	HBS	VBS
												r	r	r	r

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	HSYNCS	Horizontal synchronization display status. 0: Active low. 1: Active high.
2	VSYNCS	Vertical synchronization display status. 0: Active low. 1: Active high.
1	HBS	Horizontal blanking display status. 0: Active low. 1: Active high.
0	VBS	Vertical blanking display status. 0: Active low. 1: Active high.

44.7.14 LCDC external display control register (LCDC_EXTDCTRL)

Address offset: 0x60

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							PCLKHES	PCLKHOEN	PCLKHEEN	SPMEN	DVEN	Reserved			
							r	r	r	r	r				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

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Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	PCLKHES	Pixel clock half odd/even active edge shift 0: No shift. 1: Shift to pixel clock falling edge. This bit shifts the rising edge of the two output clocks ‘pixel clock half odd’ and ‘pixel clock half even’ by half a pixel clock period when set to ‘1’. This feature is intended to ease external sampling in case of the simple dual-view mode, as it shifts the rising edge of these clocks to the center of the valid windows of the respective even and odd pixels.
23	PCLKHOEN	Pixel clock half odd enable. The clock output 'pixel_clk_half_odd_o' can be enabled. Output is set low if disabled.
22	PCLKHEEN	Pixel clock half even enable. The clock output 'pixel_clk_half_even_o' can be enabled. Output is set low if disabled.
21	SPMEN	Sub-pixel mixing enable. Sub-pixel mixing swaps the green channel values of two successive even and odd pixels when enabled. Only intended to be used with dual-view mode (Bit20).
20	DVEN	Dual-view enable. Enabling the dual-view mode using this bit effects the dithering: The same dither threshold is applied to two successive odd and even pixels, while in normal mode the dither threshold changes for every pixel. To assign the layers to the two logical displays, use layer registers 'dual-view insertion mode' control. The half-frequency pixel clocks even and odd (Bits 23 and 22) can be used in this mode to externally sample the even and odd pixel values, i.e. the two logical displays. Certain types of integrated dual-view displays (e.g. from Sharp) may require the sub-pixel mixing to be active (Bit 25).
19:0	Reserved	Reserved, the reset value must be maintained.

44.7.15 LCDC layer shadow reload control register (LCDC_LSRCTRL)

Address offset: 0x08 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													MGR	VBR	IMR

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rw rw w

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	MGR	Mask global reload. 0: No effect. 1: Shadow reload conctrl mask global reloading.
1	VBR	Vertical blanking reload. 0: No effect. 1: The shadow registers are reloaded during the vertical blanking period.
0	IMR	Immediate reload. 0: No effect. 1:The shadow registers are reloaded immediately.

44.7.16 LCDC layer control register (LCDC_LCTRL)

Address offset: 0x0C+ 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SEN	DCBEN	HMEN	DVMD[1:0]		CKREN	CLUTEN	HDEN	VDEN	CKEN	LEN
					rw	rw	rw	rw		rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	SEN	Scaler enable. 0: Scaler disable. 1: Scaler enable.
9	DCBEN	Default color blending enable . 0: Default color blending disable. 1: Default color blending enable. This bit enables blending with the default color for a layer which is disabled, or for pixels on a layer outside of the window. When default color blending is disabled, the color of the subjacent layer is simply passed through for such pixels.
8	HMEN	Horizontal mirroring enable . 0: Horizontal mirroring disable. 1: Horizontal mirroring enable .

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Bit field	Name	Description
		This bit enables horizontal mirroring for a layer when reading the frame buffer. Note that the color frame buffer start address has to be set to the last byte of the first line in this mode.
7:6	DVMD[1:0]	Dual-view insertion mode. These bits are intended for the dual-view mode.Using these bits, the layers are assigned to the two logical displays (odd/even) as follows: 00: Insert pixel values on both pixels (odd and even) 01: Insert pixel values on odd pixels only. 10: Insert pixel values on even pixels only. 11: Insert pixel values on both pixels, duplicating thesame pixel value. Pixel count starts with the active area, i.e. the first pixel after the end of the blanking is pixel 0, hence an even pixel.
5	CKREN	Color key replace enable. 0: Color key replace disable. 1: Color key replace enable. If set, the pixel color is set to the color key color, no matter what color the pixel had before.
4	CLUTEN	CLUT lookup enable. 0: CLUT lookup disable. 1: CLUT lookup enable. lf enabled, the blue component of the frame buffer pixel after conversion to the internal pixel format is used to look up a RGB value in the table.This RGB value replaces the original RGB value of that pixel.
3	HDEN	Horizontal duplication enable. 0: Horizontal duplication disable. 1: Horizontal duplication enable.
2	VDEN	Vertical duplication enable. 0: Vertical duplication disable. 1: Vertical duplication enable.
1	CKEN	Color key enable. 0: Color key disable. 1: Color key enable. If enabled, the pixels after format conversion and optional CLUT lookup are compared to the color key, if they match for the RGB values,all channels (ARGB) of that pixel are set to '0'.
0	LEN	Layer enable. 0: Layer disable. 1: Layer enable.

44.7.17 LCDC window horizontal position conctrl register (LCDC_WHPCTRL)

Address offset: 0x10+ 0x100*x, (x =1 to 4)

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WHSPPOS[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WHSTPOS[15:0]															
rw															

Bit field	Name	Description
31:16	WHSPPOS[15:0]	Window horizontal end position. These bits configure the last visible pixel of a line of the layer window.
15:0	WHSTPOS[15:0]	Window horizontal start position. These bits configure the first visible pixel of a line of the layer window.

44.7.18 LCDC window vertical position conctrl register (LCDC_WVPCTRL)

Address offset: 0x14 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WVSPPOS[15:0]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WVSTPOS[15:0]															
rw															

Bit field	Name	Description
31:16	WVSPPOS[15:0]	Window Vertical end position. These bits configure the last visible pixel of layer window.
15:0	WVSTPOS [15:0]	Window Vertical start position. These bits configure the first visible pixel of layer window.

44.7.19 LCDC color key conctrl register (LCDC_CKCTRL)

Address offset: 0x18 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	CKR[7:0]
	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKG[7:0]								CKB[7:0]							
rw								rw							

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:16	CKR[7:0]	Color key red value.
15:8	CKG[7:0]	Color key green value.
7:0	CKB[7:0]	Color key blue value.

44.7.20 LCDC pixel format conctrl register (LCDC_PFCTRL)

Address offset: 0x1C + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														PF[2:0]	
														rw	

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2:0	PF[2:0]	Pixel format. These bits configures the pixel format. 000: ARGB8888. 001: ABGR8888. 010: RGBA8888. 011: BGRA8888. 100: RGB565. 101: BGR565. 110: RGB888 111: Custom.

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44.7.21 LCDC constant alpha conctrl register (LCDC_CACTRL)

Address offset: 0x20 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CA[7:0]							
								rw							

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CA[7:0]	Constant alpha. These bits configure the Constant Alpha used for blending.

44.7.22 LCDC default color conctrl register (LCDC_DCCTRL)

Address offset: 0x24 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCA[7:0]								DCR[7:0]							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCG[7:0]								DCB[7:0]							
rw								rw							

Bit field	Name	Description
31:24	DCA[7:0]	Default color alpha.
23:16	DCR[7:0]	Default color red.
15:8	DCG[7:0]	Default color green.
7:0	DCB[7:0]	Default color blue.

44.7.23 LCDC blending conctrl register (LCDC_BFCTRL)

Address offset: 0x28 + 0x100*x, (x =1 to 4)

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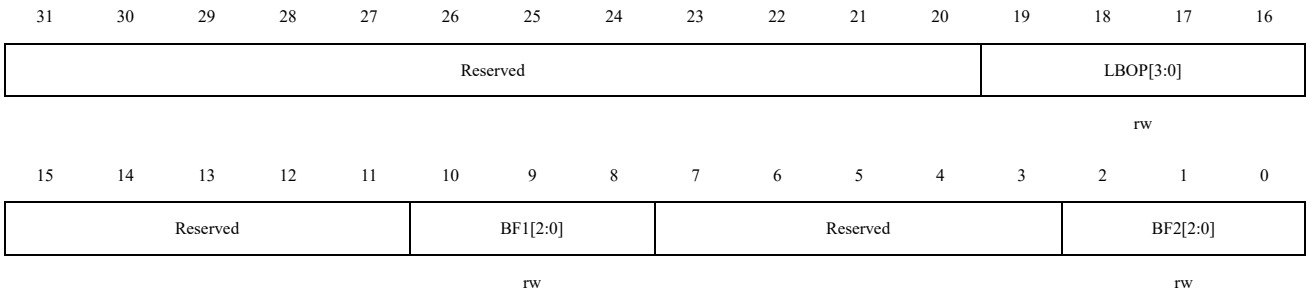
Reset value: 0x000y 0607(y = x-1)



Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:16	LBOP[3:0]	Layer blending order position (use low 3 bits) This register sets the position of the layer in the blending order and the blending factors f1 and f2: Layer Blending Order Position 1. The default position of a layer in the blending order is its physical position: (background layer →) layer 1 → layer 2 → layer 3 → ... 2. You can change this order by assigning different position numbers to the layers. 3.Duplicate/missing/out-of-range position entries will result in the positions of all layers being set to their default values. Blending Factors The general blending formula is: c' = f1 · c + f2 · cs c': blend color f1: blending factor 1 c: current layer color f2: blending factor 2 cs: lower layer color of the blend
15:11	Reserved	Reserved, the reset value must be maintained.
10:8	BF1[2:0]	Blending factor 1 These bits select the blending factor 1 000: Reserved 001: Reserved 010: Reserved 011: Reserved 100: Constant Alpha 101: Reserved 110: Pixel Alpha x Constant Alpha 111:Reserved
7:3	Reserved	Reserved, the reset value must be maintained.
2:0	BF2[2:0]	Blending Factor 2

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Bit field	Name	Description
		These bits select the blending factor F2 000: Reserved 001: Reserved 010: Reserved 011: Reserved 100: Reserved 101: 1 - Constant Alpha 110: Reserved 111: 1 - (Pixel Alpha x Constant Alpha)

44.7.24 LCDC auxiliary frame buffer contorl register LCDC_AFBCTRL)

Address offset: 0x30 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						YHEN	YUVIMDO[2:0]			YUVMD[1:0]		YUVEN	HDEN	VDEN	APEN
						rw	rw			rw		rw	rw	rw	rw

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	YHEN	Y headroom enable. When enabled, incoming Y values in range 16..235 arere-scaled to range 0..255, as required for ITU-R BT.601 conversion.
8:6	YUVIMDO[2:0]	YCbCr 4:2:2 intereaved mode component input order. These control bits set the order of YoY,/Cb/Cr components in the frame buffer when using YCbCr 4:2:2 interleaved input mode. See table below for a list of available settings.
5:4	YUVMD[1:0]	YCbCr input conversion mode 0:YCbCr 4:2:2 interleaved 1:YCbCr 4:2:0 semi-planar 2:YCbCr 4:2:0 planar 3:YCbCr 4:4:4
3	YUVEN	YCbCr input conversion enable. If enabled, the color and auxiliary FB pixel data is converted from YCbCr to RGB according to the mode setting in bits 5..4.If disabled, no conversion is performed, and the mode setting has no effect on FB data.

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Bit field	Name	Description
2	HDEN	Horizontal duplication enable.
1	VDEN	Vertical duplication enable.
0	APEN	Alpha plane enable.

44.7.25 LCDC color frame buffer address register (LCDC_CFBADDR)

Address offset: 0x34 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFBADDR[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFBADDR [31:0]															
rw															

Bit field	Name	Description
31:0	CFBADDR[31:0]	Color frame buffer start address.

44.7.26 LCDC color frame buffer length register (LCDC_CFBLEN)

Address offset: 0x38 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

Example: A frame buffer having the format RGB565 (2 bytes per pixel) and a width of 256 pixels(total number of bytes per line is 256 * 2 = 512), where pitch = line length requires a value of 0x02000207 to be written into this register.

Example: A frame buffer having the format RGB888 (3 bytes per pixel) and a width of 320 pixels(total number of bytes per line is 320 * 3 = 960), where pitch = line length requires a value of 0x02000207 to be written into this register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFBP[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFBLLEN[15:0]															
rw															

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Bit field	Name	Description
31:16	CFBP[15:0]	Color frame buffer pitch in bytes. These bits define the pitch which is the increment from the start of one line of pixels to the start of the next line in bytes. It is a signed value: negative values result in a vertical flip of the frame buffer. When reading this register, the sign bit [30] is expanded to bit [31].
15:0	CFBLLEN[15:0]	Color frame buffer line length. These bits define the length of one line of pixels in bytes + 7. The line length is computed as follows: active high width * number of bytes per pixel + 7.

44.7.27 LCDC color frame buffer line number register (LCDC_CFBLNUM)

Address offset: 0x3C + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFBLNUM[15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CFBLNUM[15:0]	These bits define the number of lines in the frame buffer that corresponds to the active high width.

44.7.28 LCDC auxiliary frame buffer 0 address register (LCDC_AFBADDR0)

Address offset: 0x40 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFBADDR0[31:0]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFBADDR0[31:0]															

rw

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Bit field	Name	Description
31:0	AFBADDR0[31:0]	Auxiliary 0 FB start address.

44.7.29 LCDC auxiliary frame buffer 1 address register (LCDC_AFBADDR1)

Address offset: 0x44 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFBADDR1[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFBADDR1[31:0]															
rw															

Bit field	Name	Description
31:0	AFBADDR1[31:0]	Auxiliary 1 FB start address.

44.7.30 LCDC auxiliary frame buffer length register (LCDC_AFBLEN)

Address offset: 0x48 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFBP[15:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFBLLEN[15:0]															
rw															

Bit field	Name	Description
31:16	AFBP[15:0]	Pitch of auxiliary 0/1 FB in bytes.
15:0	AFBLLEN[15:0]	Line length of auxiliary FB in bytes-1 + (width of bus in bytes).

44.7.31 LCDC auxiliary frame buffer line number register (LCDC_AFBLNUM)

Address offset: 0x4C + 0x100*x, (x =1 to 4)

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LNUM[15:0]															
rw															

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	AFBLNUM[15:0]	Number of lines in the auxiliary 0/1 frame buffer.

44.7.32 LCDC CLUT write access register (LCDC_CLUTWR)

Address offset: 0x50 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLUTADDR[7:0]								CLUTR[7:0]							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLUTG[7:0]								CLUTB[7:0]							
rw								rw							

Bit field	Name	Description
31:24	CLUTADDR[7:0]	CLUT address.
23:15	CLUTR[7:0]	Red value.
15:8	CLUTG[7:0]	Green value.
7:0	CLUTB[7:0]	Blue value.

44.7.33 LCDC scaler input size register (LCDC_SINS)

Address offset: 0x54 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				SINH[11:0]											
				rw											

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SINW[11:0]											
				rw											

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:16	SINH[11:0]	Scaler input height.
15:12	Reserved	Reserved, the reset value must be maintained.
15:0	SINW[11:0]	Scaler input height.

44.7.34 LCDC scaler output size register (LCDC_SOUTS)

Address offset: 0x58 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				SOUTH[11:0]											
				rw											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SOUTW[11:0]											
				rw											

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:16	SOUTH[11:0]	Scaler output height.
15:12	Reserved	Reserved, the reset value must be maintained.
15:0	SOUTW[11:0]	Scaler output width.

44.7.35 LCDC vertical scaler factor register (LCDC_VSF)

Address offset: 0x5C + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSF[15:0]															

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rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	VSF[15:0]	Vertical scaling factor.

44.7.36 LCDC vertical scaler phase register (LCDC_VSP)

Address offset: 0x60 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSP[15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	VSP[15:0]	Vertical scaling phase.

44.7.37 LCDC horizontal scaler factor register (LCDC_HSF)

Address offset: 0x64 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSF[15:0]															

rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	HSF[15:0]	Horizontal scaling factor.

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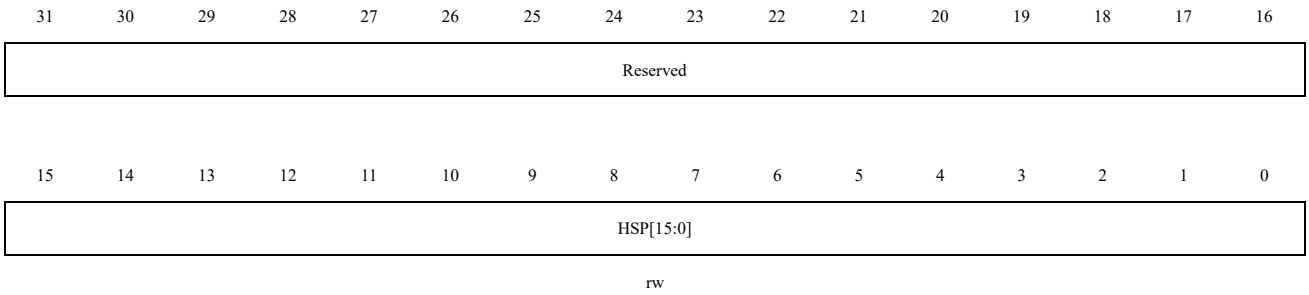
44.7.38 LCDC horizontal scaler phase register (LCDC_HSP)

Address offset: 0x68 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	HSP[15:0]	Horizontal scaling phase.

44.7.39 LCDC YCbCr scaler register 1 (LCDC_YUVS1)

Address offset: 0x6C + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	BUCS[9:0]	Blue Cb scale.
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	RVCS[9:0]	Red Cr scale.

44.7.40 LCDC YCbCr scaler register 2 (LCDC_YUVS2)

Address offset: 0x70 + 0x100*x, (x =1 to 4)

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						GUCS[9:0]									
						rw									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						GVCS[9:0]									
						rw									

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	GUCS[9:0]	Green Cb scale.
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	GVCS[9:0]	Green Cr scale.

44.7.41 LCDC flexible color format register 1 (LCDC_FCF1)

Address offset: 0x74 + 0x100*x, (x =1 to 4)

Reset value: 0x0002 2100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														RLENB[3:0]	
														rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RLENB[3:0]		RSB[4:0]					ALENB[3:0]				ASB[4:0]				
rw		rw					rw				rw				

Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17:14	RLENB[3:0]	Red length bits.
13:9	RSB[4:0]	Red start bit.
8:5	ALENB[3:0]	Alpha length bits.
4:0	ASB[4:0]	Alpha start bit.

44.7.42 LCDC flexible color format register 2 (LCDC_FCF2)

Address offset: 0x78 + 0x100*x, (x =1 to 4)

Reset value: 0x0012 3110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	BPP[2:0]	BLENB[3:0]
	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLENB[3:0]		BSB[4:0]					GLENB[3:0]				GSB[4:0]				
rw		rw					rw				rw				

Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:18	BPP[2:0]	Bytes per pixel.
17:14	BLENB[3:0]	Blue length bits.
13:9	BSB[4:0]	Blue start bit.
8:5	GLENB[3:0]	Green length bits.
4:0	GSB[4:0]	Green start bit.

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45 2.5D GPU

45.1 Introduction

N32H7xxx supports one 2.5D GPU targeting high resolution displays in embedded systems.The module is optimized for high frame rates even when processing multiple MPixels per frame.

45.2 Main Features

The main features supported by 2.5D GPU are shown below:

- High Rendering Quality
  - Sub-pixel accurate rendering
  - Direct-edge anti-aliasing
  - Blurring of primitive edges
  - Static dithering at framebuffer write back to enhance RGB565 output
- High Performance
  - 300 M pixels/second fill rate (300MHz clock, single pipeline)
  - Prefetching caches
- Hardware accelerated primitives
  - Fast clear/rectangle fill
  - Lines
  - Triangles
  - Quadrangles
  - Beziers
  - Advanced Blit operations supporting sacling,stretching,rotating,coloring and alpha blending
  - Convolution filtering
- Blending
  - Normal alpha blending
  - Independent alpha/color blending
  - Source/Destination factors: 0,1,source alpha, 1-source alpha
- Textures
  - 4096 x 4096 Texture size
  - Flexible texture color format handling

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- ARGB8888, RGBA8888, RGB888, BGR888, ARGB8565, RGBA5658, ARGB4444, RGBA4444, ARGB1555, RGBA5551, RGB565, AL88, AL44, AL17,AL8, AL4, AL2, AL1, ARGB2222, RGBA2222

◆ Indexed formats for CLUT(Color Look Up Table)

- For all ALx formats

◆ RLE texture decompression

◆ Texture address modes

- Standard linear
- Swizzling
- Inverse swizzling
- Virtual tiling

■ Frame buffer

◆ 4096 x 4096 Supported

◆ ARGB8888, RGBA8888, RGB888, BGR888, ARGB8565, RGBA5658, ARGB4444, RGBA4444, ARGB1555, RGBA5551, RGB565, A8, L8, AL17, ARGB2222, RGBA2222

◆ Blend Modes: Blend, Multiply, Multiply-add, Darken, Lighten

■ Performance Verification

◆ Performance Counters

◆ Visualize enumeration efficiency

◆ Visualize cache burst access lengths

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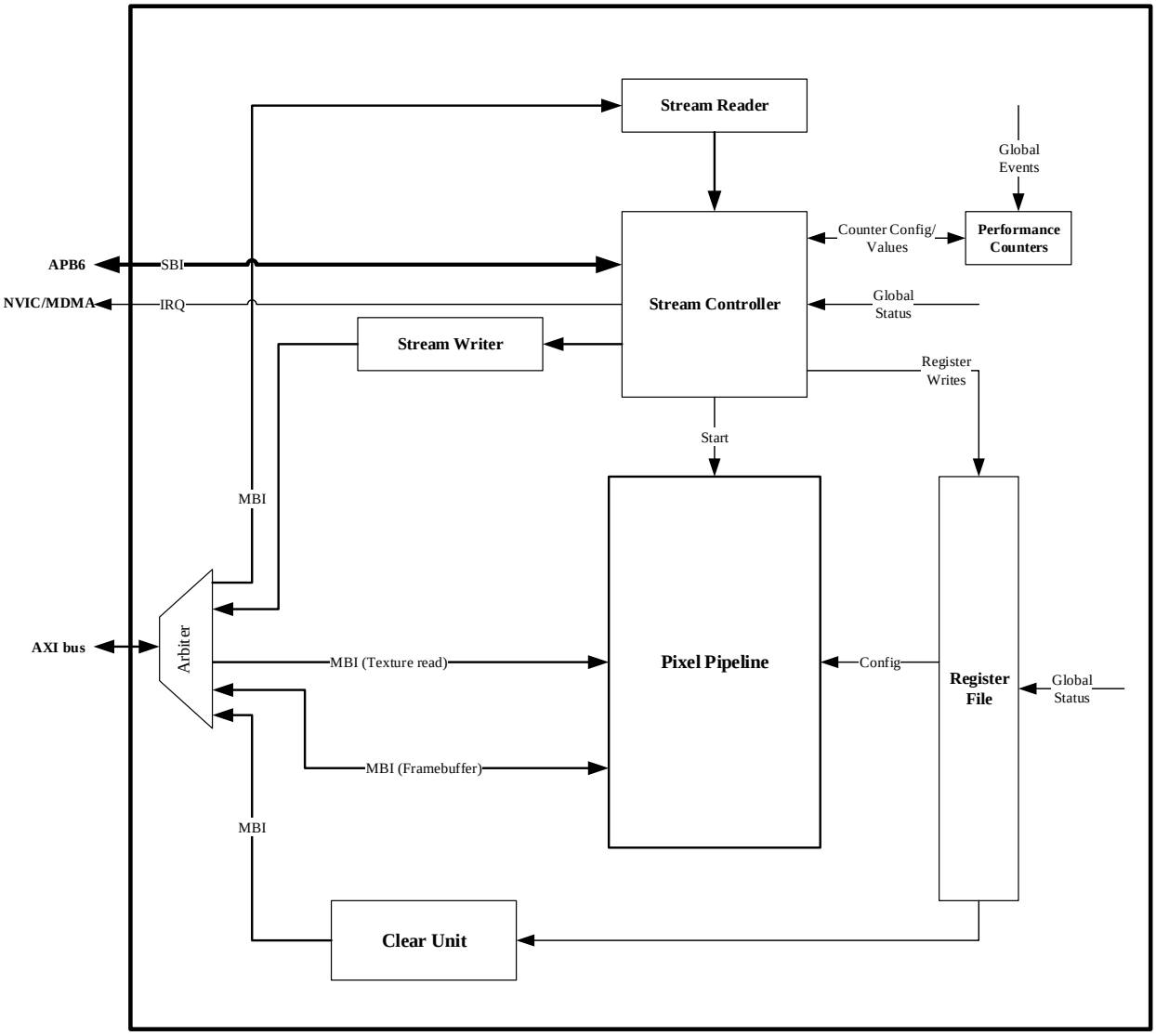
45.3 Block Diagram

Figure 45-1 GPU Block Diagram



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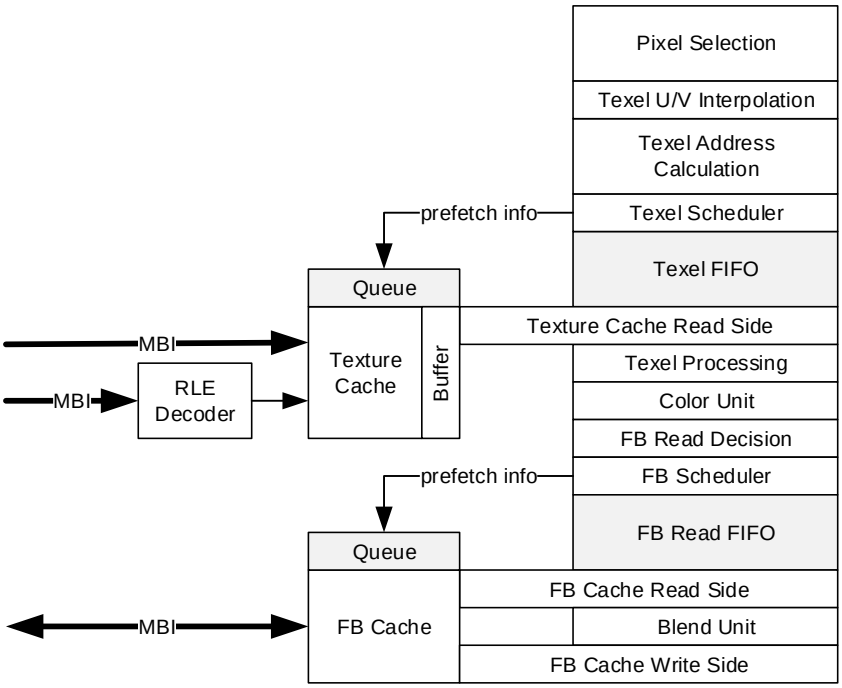

⑴Stream Controller (STC)

①Through MBI (Master Bus Interface) to read and write pixel data from frame buffer, read textures, etc.

②Through SBI (Slave Bus Interface) to provide external register access, etc.

⑵Pixel Selection Unit (PSU)

Scans through the bounding box of an object and determines for every pixel whether it is inside or outside of the object to be rendered. Pixels which are inside are output to the next block along with their x/y coordinates and an 8-bit coverage value for anti-aliasing.

⑶Texel U/V Interpolation (TXI)

This module calculates the normalized texture u/v coordinates based on a (homogenous) 2D matrix multiplication with the pixel x/y coordinates. It supports multiple texture units (maximum number of texture units is configuration dependent) which are serialized into the pixel pipeline here: The normalized u/v coordinates are output along with a texture unit ID.

⑷Texel Address Calculation (TXA)

Calculates four absolute texel offsets based on the normalized texture coordinates by applying texture width and height. Four absolute texel offsets are required for parallel processing in case of bilinear filtering. In addition, this module also supports a multi-cycle output of multiples of these four texel offsets per pixel (and per texture unit) to support convolution filtering.It supports linear, swizzled and virtual-tiled addressing modes.

⑸RLE Decoder (RLD)

The texture cache can optionally fetch the data through the run-length decoding unit into the cache instead of directly via MBI to support run-length.

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⑹Texel Processing (TXP)

Combines the four texture samples received from the texture cache to a single output color per texture. Contains a flexible Look-up-table (LUT) to support indexed texture formats as well as special modes like ARGB color mapping (LUT stores mapped color channel values) and convolution filtering (LUT stores convolution filter weights).Also implements color keying.

⑺Color Unit (COL)

Combines multiple constant color values and texture color values to a single output color value in multiple passes per pixel (maximum number of colorization passes is configuration dependent).

⑻Blend Unit (BLU)

Combines the source color (from color unit) and destination color (from framebuffer cache read side) to a single output color dependent on the select.

⑼Performance Counters (PFC)

It is available to enable corresponding events performance counters to read the current value.

⑽Clear Unit (CLR)

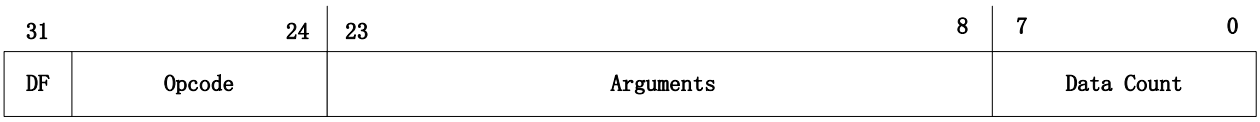
Fills a given memory area with a constant value. The memory area can be specified via width, height and pitch and a byte mask can be provided to leave out bytes in the target area.

45.4 Function Description

45.4.1 Stream Controller (STC)

45.4.1.1 Stream Format

The stream is a sequence of 32-bit words, which are either commands or data associated with commands. The command layout is as follows:



- Bit 31：Data Following（1bit）
- Bit 30…Bit 24：Command Opcode (7bits)
- Bit 23…Bit 8：Command Arguments (16bits)
- Bit 7…Bit 0：Data Count (8bits)

After every command with DF=1, as many data words as encoded in data count follow. A data count of 0 to 255 encodes 1 to 256 data words contained. After the data, the next word is a command again.

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45.4.1.2 Stream Commands

Command	Opcode	Arguments	Data
NOP	0x00	0	Optional (be used to pad stream), will be discarded
Wait	0x01	bit wait mask	none
Register Write	0x04	12-bit register start address	1 to 256 register words
Register Dump	0x05	12-bit register start address	2 words, 1st word: target address, 2nd word: number of registers to be dumped -1
Jump/Call	0x08	0=Jump, 1=Call	1 or 2 words, end address (in case of a call only) + target address
Return	0x09	0	none
Checksum	0x7e	Bit 0： 0=disable checksum protection mode 1= enable checksum protection mode Bit11～1:0x5d4	1 word, start checksum
Stream End	0x7f	bit wait mask	none

45.4.1.3 Starting command stream execution

Doing a write to register STREAM_ADDRESS triggers a fetch request and starts the command stream execution for the call stack level from register CALL_STACK_POINTER. The call stack pointer should normally be set to 0 before this and the end address of call stack level 0 should be set to 0xffffffff. This may be different in case of a resume after Halting command stream execution or in case the Ring-Buffer mode is being used.

45.4.1.4 Interrupts/Errors

There are five different IRQs:

- Stop IRQ: On stop of stream execution due to stream end, halt or stream error
- Pause IRQ: Used in Ring-Buffer mode
- Stall IRQ: Stalling has finished after stall request
- MBI error IRQ: An external MBI error has been received
- Sync IRQ: When register Synchronization ID 0 was changed

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All IRQs have a status bit in register Interrupt_Status which is set when they are triggered and which can be written as '1' to clear the IRQ. The enable bits for these IRQs in the Control register control, whether the respective external IRQ output line is asserted when the respective interrupt status is set. Masking an IRQ line using the enable control does not affect the status register itself.

While the above five IRQ signals are separate output lines of the STC, they are combined to three separate IRQ lines in total on the toplevel of the core:

- Pause IRQ has a separate IRQ line
- Sync IRQ has a separate IRQ line
- Stop IRQ, Stall IRQ and MBI error IRQ are or-combined to a 'Special IRQ' line

A pause IRQ is indicated as long as the stream reader pauses prefetching at the pause address. A sync IRQ is indicated whenever a write to register Synchronization ID 0 occurs. On stop of stream execution due to stream end, stall or stream error will generate stream abnormal interrupt.

45.4.2 Pixel Selection (PSU)

The purpose of the Pixel Selection Unit (PSU) is to send out the x/y coordinates of all pixels of an object together with their coverage values. Pixels with a coverage of 0 are not output.In order to draw the pixels of an object into the framebuffer, it is necessary to enumerate all pixels that belong to the object. An object can be a triangle, a quadrangle or even a Bézier curve. Every object lies inside a rectangular axis-aligned Bounding Box (Bbox) defined by LIM_BBOX_XMIN, LIM_BBOX_XMAX, LIM_BBOX_YMIN and LIM_BBOX_YMAX registers and is delimited by a set of linear edges (Limiters) which are defined by LIM_VSTART, LIM_DX and LIM_DY registers.In addition to the Bbox, the enumeration is clipped by two max values for x and y coordinates (M_LIM_XMAX and M_LIM_YMAX of the LIM_BBOX_MAX register) as a security feature to avoid that pixels outside of the framebuffer are generated.

The PSU enumerates the inside of the Bbox pixel by pixel while trying to enumerate only pixels which belong to an object to minimize the number of cycles wasted on invisible pixels.The enumeration starts at the left border of the Bbox at the vertical position that is set in the register LIM_START_Y. The limiter start values (LIM_VSTART) related to that start position must be set accordingly.

The whole enumeration process is started on a write to the control register (LIM_CTRL). The control register also controls how the limiters output their individual coverage values. An optional Bezier post-process calculates a coverage value by combining the first two limiter values to a Bezier coverage value.

45.4.2.1 Limiters

A limiter implements a linear edge function: value = vstart + x*dx + y*dy, which is calculated incrementally in the hardware.

The output values of all limiters are combined as follows for the coverage output of the PSU: The two smallest of the seven internal coverage values (six linear limiters + optional Bezier post-process) are multiplied. When the Bezier unit is disabled, it is fully bypassed, i.e. the latency of the PSU is reduced compared to the case when it is

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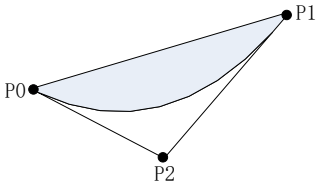
enabled.

45.4.2.2 Enumeration stepping

The PSU enumerates as few pixels as possible which do not belong to the object. In general, it starts at the position x/y = LIM_BBOX_XMIN.M_LIM_BBOX_XMIN/ LIM_START.M_LIM_START_Y and steps into the inside of the object with the smallest possible number of steps (right, up and down). Inside of the object, it steps left to right and top down first and left to right bottom up afterwards if necessary. A state machine controls the Bbox enumeration unit and the Limiter units. It checks the limits of the bounding box and the output of all limiters and determines the next step.

A special functionality is the 'striped enumeration' mode, which is enabled when LIM_STRIPE.M_LIM_STRIPE_WIDTH is set to a value different from 0. In this mode, the enumeration does not step to the right border of the bounding box in one go, but stops at vertical borders at a distance of LIM_STRIPE.M_LIM_STRIPE_WIDTH and processes a full stripe first, before going to the next stripe to the right. This mode is sensible when doing texture mapping in a tiled or swizzled texturing mode to reduce the number of texture cache misses. LIM_STRIPE.M_LIM_STRIPE_OFFSET can be used to achieve that the first stripe inside the bounding box has a width different from LIM_STRIPE.M_LIM_STRIPE_WIDTH by providing a start value different from 0. This feature may be used e.g. to align the stripe borders with the framebuffer cache tag borders (provided the framebuffer cache line length is a multiple of the stripe width).

45.4.2.3 Bézier post-process



The Bézier function unit is an optional post processing block to the coverage value. It sets the coverage of all pixels to zero that do not belong to a quadratic Bézier curve. The quadratic Bézier curve is defined by a control triangle which is at the same time the triangle that gets enumerated.

The Bézier mode is enabled by LIM_CTRL.M_BEZ_CTRL[0]. LIM_CTRL.M_BEZ_CTRL[1] controls the convex (0) and concave (1) shape of the Bézier curve if BEZ_AA_CTRL.M_BEZ_WIDTH is 0.

If BEZ_AA_CTRL.M_BEZ_AA is not 0 then Anti-aliasing is applied to the curve. The width of the Anti-aliasing must be set to the register as the reciprocal value.

The position of the Anti-aliasing can be shifted towards the inside or outside of the curve by the signed value of BEZ_AA_CTRL.M_BEZ_AA_OFFSET.

If BEZ_AA_CTRL.M_BEZ_WIDTH is greater than 0 then the Bézier curve is drawn as a line with the specified width.

If the Anti-aliasing extends the Limiters of the control triangle, this region gets cut off. To avoid this the corresponding Limiter can be calculate using an offset so that the region gets included into the enumeration. If that Limiter is also used for the Bézier calculation the offset must be compensated and set into BEZ_VOFF Registers.

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For large Bézier curves the values of the Limiters can become very small. This can lead to quantization artifacts. To increase the precision of the calculations the range of the Limiters can be scaled up. This scaling value must be set to BEZ_CTRL.M_BEZ_LIM_SCALE.

45.4.3 Clear Unit (CLR)

Clear Unit can fills a given memory area with a constant value. The memory area can be specified via width, height and pitch and a byte mask can be provided to leave out bytes in the target area.

On a write of CLR_START_ADDRESS, the Clear Unit writes the value of CLR_VALUE.CLR_VALUE using the mask CLR_CTRL.CLR_MASK to all bytes in the memory area starting at CLR_START_ADDRESS, defined by CLR_CTRL.M_CLR_NUM_LINES, CLR_LINE_CONFIG.M_CLR_LINE_LENGTH and CLR_LINE_CONFIG.M_CLR_PITCH.

45.4.4 Texel U/V Interpolation (TXI)

The TXI module calculates a normalized U/V pair for all active texture units.

The results for the two texture units are serialized into two cycles when two units are enabled (TEX_GLOBAL.M_TEX_NUM_UNITS), which is why the texture ID is required in the pipeline. When depth interpolation is enabled as well (TEX_GLOBAL.M_TEX_DEPTH_ENABLE), an additional cycle is required per pixel.

The texel coordinate flags are used to allow correct wrapping in the Texel Address Calculation (TXA) unit: TXI effectively discards the integer part of the normalized texture coordinate, but part of that lost information is relevant for the TXA in certain wrapping modes, so it gets encoded in the texel coordinate flags.

45.4.5 Texel Address Calculation (TXA)

45.4.5.1 Basic functionality

The primary purpose of the TXA module is to generate the absolute offsets (in bits) of four texels per cycle based on a single normalized texture U/V input coordinate. For bilinear filtering, the fractional parts of the U/V position (8 bits each) are output towards the TXP unit, which finally performs the filtering. Furthermore, the TXA module supports multi-cycle address calculation for convolution filtering.

There are three basic modes of usage of the TXA unit regarding filtering of textures:

• Nearest Neighbor filtering: Filtering is off, filter kernel is 1x1, single output per texture unit (Last_Sample always '1')

• Bilinear filtering: Filtering is on, filter kernel is 2x2, single output per texture unit (Last_Sample always '1')

• Convolution filtering: Filtering is on, filter kernel is NxM, potentially multiple outputs per texture unit (i.e. multiple cycles)

To support kernel sizes above 2x2 for convolution filtering, multiple steps and multiple output cycles are required. For different kernels, this looks as follows:

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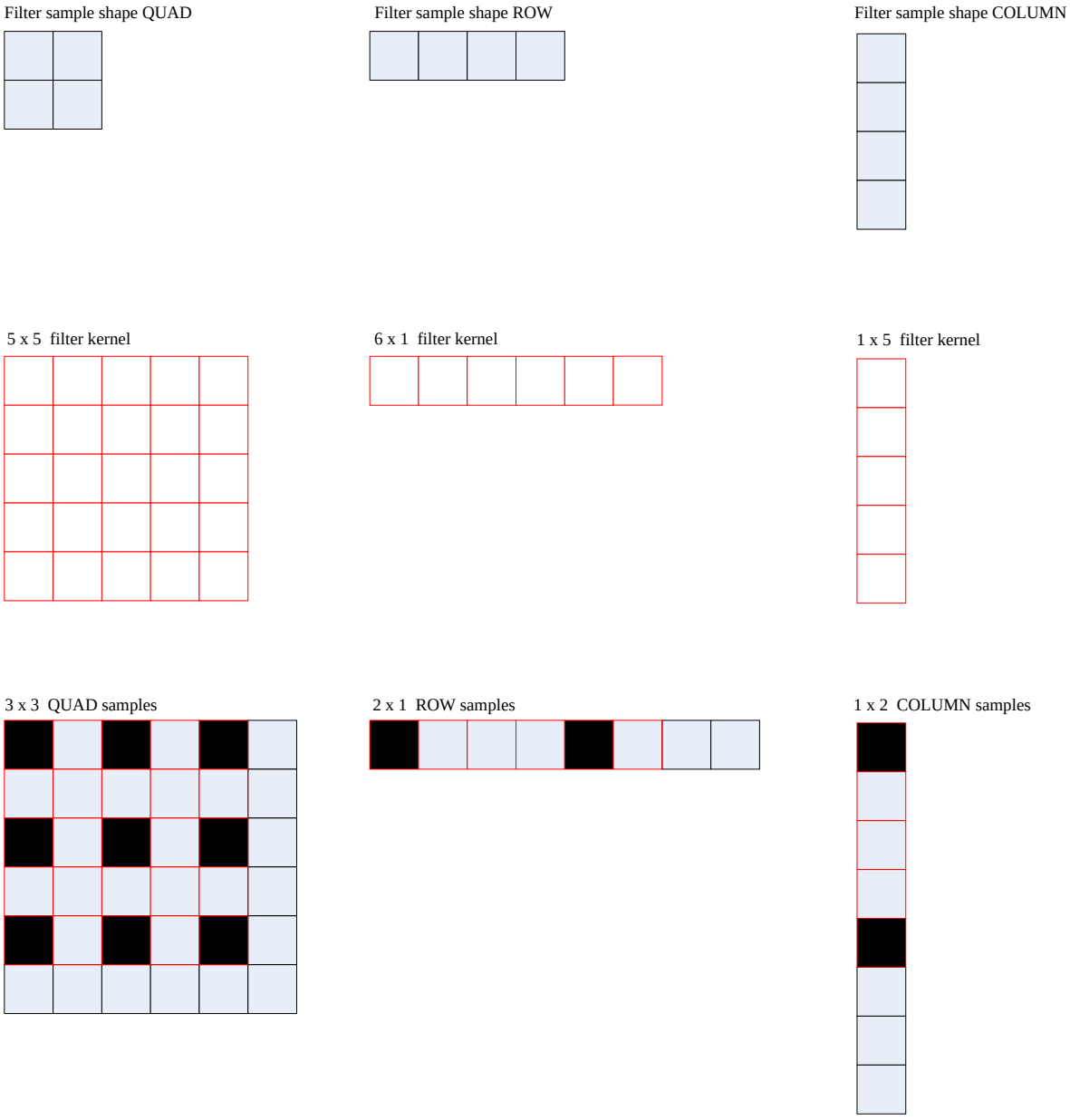
Figure 45-2 Examples for different filter kernels



Consider the left-most example: The basic filter sample shape is still 2x2 texels ('QUAD') as in case of the bilinear filtering (top). The full kernel (center) requires 5x5 texels. Multiple of the 2x2 samples are thus used to cover the complete 5x5 kernel (bottom). On the right side and at the bottom, the 'QUAD' samples overlap the 5x5 kernel: The respective sub-samples need to be ignored.

The scheme works for one-dimensional kernels as can be seen in the center and on the right side: In these cases, the filter shapes 'ROW' and 'COLUMN' are used instead of 'QUAD'.

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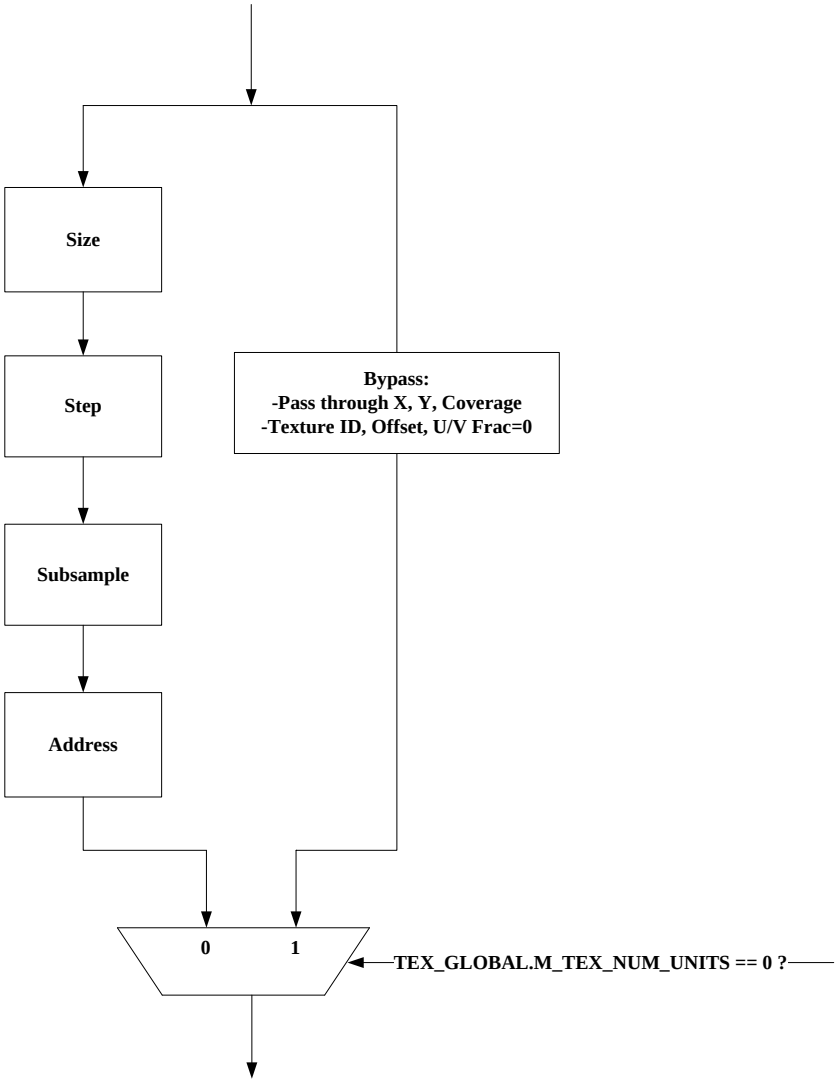
45.4.5.2 Sub-module structure

Figure 45-3 Block structure of Texel Address Calculation



The TXA module consists of four sub modules which are simply cascaded. In case texturing is fully disabled (TEX_GLOBAL.M_TEX_NUM_UNITS == 0), the bypass shown above is used (i.e. no pipeline delay occurs for this module).

The purpose of the sub modules can best be understood considering the above example Image:

• 'Size' multiplies the normalized u/v coordinates by width/height and thus converts to absolute coordinates. This is still for a single coordinate per cycle.

• 'Step' is important for bigger kernels which require multiple samples. The coordinates calculated by 'Size' are for the top-left sample. This module calculates the top-left coordinates of the other samples and thus potentially generates multiple pipeline entries at the output per input entry. The last sample of a kernel is flagged 'Last_Sample' from here on. This module still outputs a single coordinate per cycle.

• 'Subsample' generates the missing 3 coordinates per sample. The output of this block is 4 coordinates per cycle.

• 'Address' converts from u/v to real bit offsets considering the tiling mode and pitch as well as the bits per

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pixel.

45.4.6 Texture Cache/Scheduler (TXC/TXS)

45.4.6.1 Fetching cache lines

The texture cache provides 2 sets of 4 cache lines, each (4-way set associative) per texture unit. So the overall number of cache lines is 2x2x4 = 16 lines, but only 8 lines may be used per texture unit. The advantage of independent cache lines per unit is that no cache thrashing may occur between the units. The length of a cache line is 16.

The allocation of texels to cache lines is already done in the scheduler part. This allows prefetching to hide the MBI read latency.

The actual fetch of cache lines is done by the cache part based on the 'prefetch jobs' from the scheduler. A cache line is normally fetched via MBI relative to the address TXC_START_ADDRESS, but may be fetched through the RLE Decoder (RLD) instead if TXC_USE_RLD is set.

In case a virtual tiling mode (TEX_MODE.M_TEX_VIRTUAL_TILING_MODE) other than NONE is selected, the cache will fill a cache line using multiple bursts which are offset by TXP_CTRL.M_TXC_BURST_PITCH. (This mode only works for MBI fetches, not for fetches from the RLD.)

The cache is fully invalidated on a write to TXC_START_ADDRESS for any unit, i.e. a following read access to previously cached content will trigger a new fetch.

45.4.6.2 Debug mode

The texture cache can change the color of a pixel to visualize certain performance events per pixel when a debug mode is selected via register TEX_GLOBAL.M_TXC_DEBUG_MODE. It encodes this color on the Coverage signal, meaning that the debug colorization of the blend unit (see register BLU_WRITE.M_BLU_COVERAGE_DEBUG_ENABLE) must be enabled to use this feature.

There are four events inside the texture cache, which influence the debug colorization:

- FIRST_PIXEL: First pixel accessing a line
- REFRESH: Pixel triggering one or multiple access count overflows
- FETCH_WAIT: Pixel needed to wait for fetch at input of the cache, i.e. the prefetch latency could not be fully hidden.
- RAM_WAIT: Pixel needed to wait at the cache RAM because not all texels could be accessed through the texel buffer or through the single cache RAM access cycle, which is possible per pixel without penalty.

45.4.7 RLE Decoder (RLD)

45.4.7.1 Functionality

The RLD unit allows to use run-length encoded textures with 1 to 4 bytes per pixel. The RLE texture is transparently fetched by the texture cache from the RLD unit when TXP_CTRL.M_TXC_USE_RLD is enabled for a single texture unit.

The RLD unit has been designed to provide transparent access to run-length encoded textures.

For this purpose, the texture cache requests absolute byte offsets from the RLD unit and the

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RLD unit internally tracks the decoding progress relative to that offset. Two special performance features are implemented to speed up decoding in case the requests from the texture cache are not to successive offsets and to provide virtual random access:

▪ **Fast-forward**: When the offset of the request from the texture cache effectively skips a part of the texture (e.g. pitch > width), run-length encoded packets from the RLE texture are skipped in a single cycle instead of being 'counted down'.

▪ **Rewind**: In case the requested offset is lower than the previously requested offset, the RLE decoding will start again from the beginning, using the fast-forward feature to skip to the requested offset as fast as possible.

Three byte RLE textures are virtually accessed as four byte textures from texture cache point of view, i.e. the RLD unit will prepend 0xff to every chuck of 24 bits (i.e. ARGB8888 format is assumed).

45.4.7.2 RLE format

Run-length encoded (RLE) images comprise two types of data elements: Run-length Packets and Raw Packets. The first field (1 byte) of each packet is called the Pixel Count field. The second field is called the Pixel Value field (1, 2, 3 or 4 bytes).

For Run-length Packets, the Pixel Value field contains a single pixel value.

For Raw Packets, this field has a variable number of pixel values.

The highest order bit of the Pixel Count indicates whether the packet is a Raw Packet or a Runlength Packet. If bit 7 of the Pixel Count is set to 1, the packet is a Run-length Packet, otherwise it is a Raw Packet.

The lower 7 bits of the Pixel Count specify how many pixel values are represented by the packet. In the case of a Run-length packet, this count indicates how many successive pixels have the pixel value specified by the Pixel Value field. For Raw Packets, the Pixel Count specifies how many pixel values are actually following until the start of the next packet. This 7-bit value is encoded as 1 less than the number of pixels in the packet (a value of 0 indicates 1 pixel while a value of 0x7f indicates 128 pixels).

Table 45-1 RLE format Run-length Packet

Field Name	Packet Type	Pixel Count	Pixel Data
Field Size	1 bit	7 bits	Pixel Width (register setting of RLE Decoder)
Content	Must be '1' for run-length	Number of pixels encoded by this packet-1 (Repetition Count)	The common pixel value to be used

Run-length Packets are composed of two parts. The first is a repetition count and the second is the pixel value to be repeated

Table 45-2 RLE format Raw Packet

Field Name	Packet Type	Pixel Count	Pixel Data

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Field Size	1 bit	7 bits	Pixel Width * Pixel Count +1
Content	Must be '0' for raw packet	Number of pixels encoded by this packet-1	Sequence of raw pixels contained in this packet

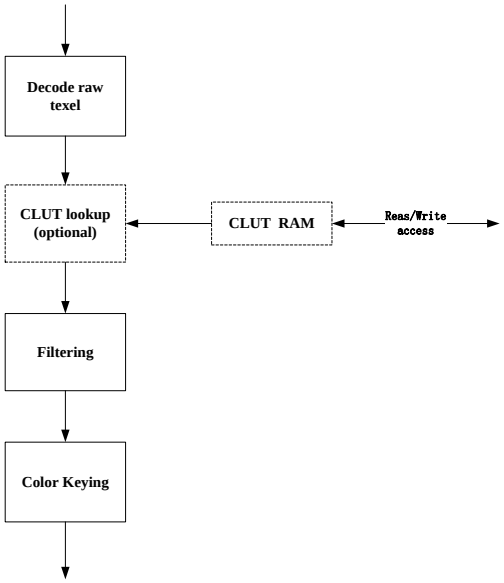
The Raw Packet is always composed of two fields. The first field is the Pixel Count and the second field is the Pixel Data field. The length of the second field depends on the value of the Pixel Count field.

45.4.8 Texel Processing (TXP)

45.4.8.1 Sub-module structure

The TXP module generates a single output color value per pixel and texture unit. It consists of four sub-modules:

Figure 45-4 Texel Processing Block Diagram



45.4.8.2 CLUT lookup

The CLUT is a single-port RAM inside the TXP block, which can be read/written via SBI or from the command stream.

It is accessed as part of the TXP operation when TXP_CTRL.M_TXP_CLUT_MODE is other than OFF. While the CLUT is actively used by the TXP, any other accesses to the CLUT RAM (reads or writes), whether from external via SBI or from the command stream, are not allowed. They lead to incorrect lookup results being obtained by the TXP operation.

The CLUT logically contains different kinds of values, depending on TXP_CTRL.M_TXP_CLUT_MODE:

- INDEXED_COLOR: CLUT contains color values
- MAP_(A)RGB: CLUT contains mapped channels values
- CONVOLUTION(_SIGNED): CLUT contains filter weights for convolution filtering

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45.4.8.3 Filtering / ARGB map combine

This stage determines the final output color depending on the CLUT mode:

• MAP_(A)RGB: No filtering is performed, the CLUT lookup result is directly used as output color.

• CONVOLUTION(_SIGNED): The CLUT lookup results are used as filter weights, overriding the default bilinear weights based on Texel_U_Frac and Texel_V_Frac.

• OFF: Bilinear filtering, weights based on Texel_U_Frac and Texel_V_Frac.

Filtering weights the four texels per clock cycle using bilinear filter weights or convolution filter weights from the CLUT. In case of convolution filtering, the weighted color values may be accumulated over multiple clock cycles. At the end of an accumulation cycle, a scale and bias is applied on the accumulated values.

45.4.9 Color Unit (COL)

Inside the Color Unit, there are four parallel instances of the below Alpha/Color path module for Alpha, R, G and B. The Alpha path has separate registers, while the color paths for R, G and B are controlled by the same set of registers except for the 'input_select' control, for which there are individual registers for R, G and B.

The Alpha/Color path of the color unit is shown in the following figure：

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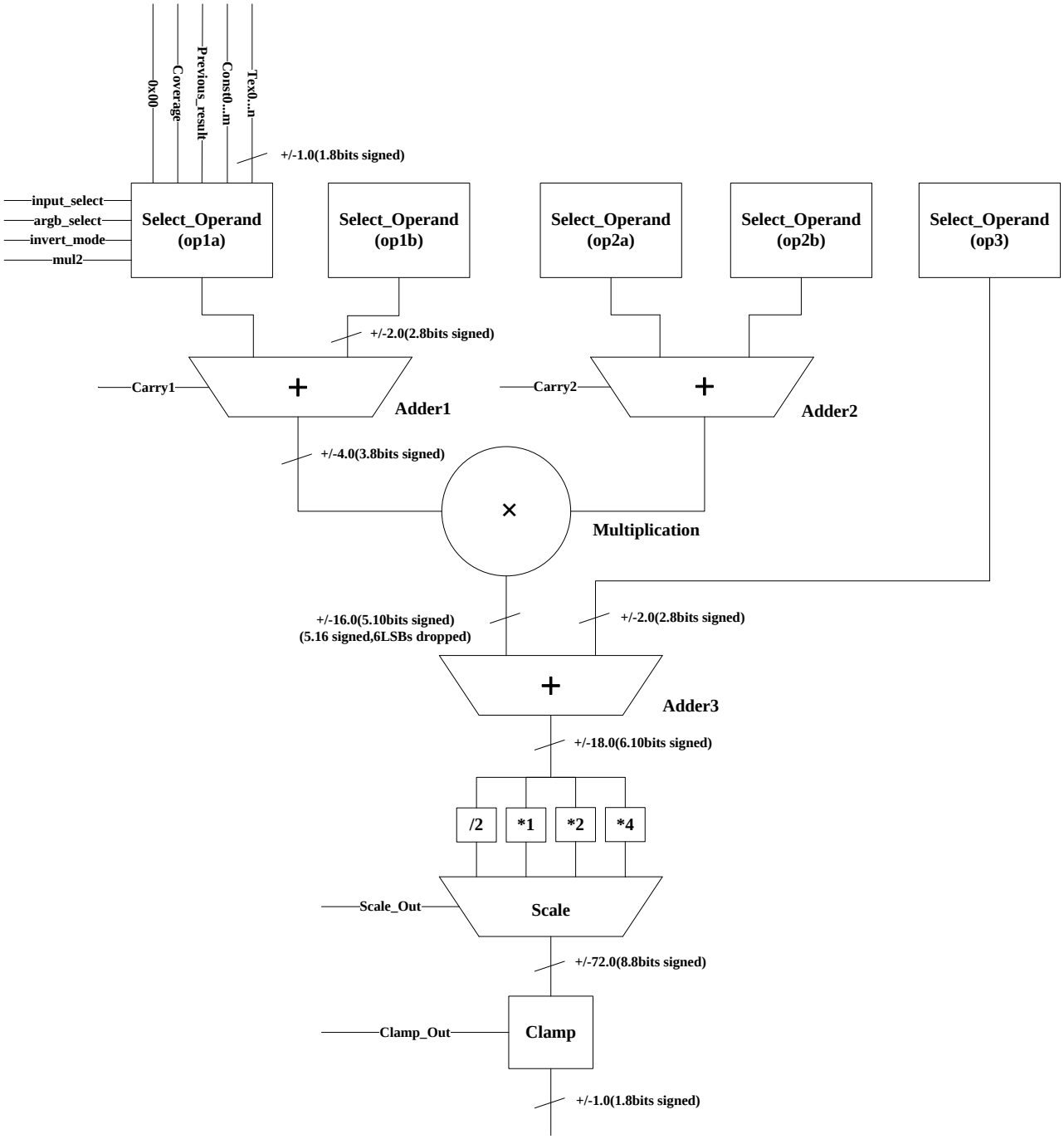

45.4.10 Framebuffer Read Decision (FBD)

The FBD module implements the alpha test functionality which can be used to discard colorized texels based on their alpha values e.g. to avoid unnecessary read-modify-write accesses. In normal blending cases, the alpha test would be configured to 'pass if greater 0' to effectively discard transparent source pixels already at this stage.

Furthermore, the read decision flags are used to generate a per-pixel read indication for the framebuffer scheduler. These flags need to be set in accordance with the blend mode configured in the blend unit.

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45.4.11 Framebuffer Cache + Scheduler (FBC/FBS)

45.4.11.1 Functionality

The scheduler part basically calculates the offset into the framebuffer (in bytes) based on the input x/y coordinates and FBS_PITCH as well as the bytes per pixel defined by FB_PIXEL_ORG. It then scans for consecutive spans of offsets (gap-less sequences of pixels) and schedules those for prefetching by the framebuffer cache. The cache in turn gets these jobs from a queue and allocates every span to a cache line.

A cache line is always written as a single burst on the MBI interface. The longer the spans, the more efficient are the burst accesses.

Since there are not necessarily closed 'read spans' in the framebuffer, there may be effectively multiple closed read spans inside a span with gaps (i.e. pixels which do not require a read) in between. The register FBS_SPAN_CONFIG.M_FBS_READ_GAP_LENGTH_LIMIT may be used to control generation of multiple read spans for a span when the read gaps get too long. It is assumed that there is a system dependent optimum for this value. Note that when using anti-aliasing without transparency, there are potentially a lot of spans, which have 'read enabled' (i.e. not fully covered pixels) at the start and end of a scan line while the inner pixels are opaque. Tuning the value of FBS_SPAN_CONFIG.M_FBS_READ_GAP_LENGTH_LIMIT for these cases may improve performance and/or save bus cycles.

The maximum number of bytes in a span is limited by the framebuffer cache line length (16x8 = 128 bytes). Depending on FB_PIXEL_ORG this is equivalent to 32, 64 or 128 pixels. As a result, there are 'cache line borders' every 32, 64 or 128 pixels counting from the start of the framebuffer at FBC_START_ADDRESS, which a span of pixels may not cross and where a span is always split into two spans.

For certain performance tweaking tricks, the maximum length of a span may further be reduced using FBS_SPAN_CONFIG.M_FBS_SPAN_LENGTH_LIMIT. This could be used e.g. to force maximum 64 pixel spans in case of an 8-bit framebuffer format.

45.4.11.2 Debug Mode

When FBS_PITCH.M_FBS_DEBUG_ENABLE is set to '1', the color at the pixel output is overwritten as follows:

- Write-only: 0xFFFFFF (white)
- Read+Write: 0x00CC00 (green)
- Span end on write-only: 0xFF0000 (red)
- Span end on read+write: 0xFF9400 (orange)
- Last pixel of a job which was split in two because the read gap length limit was reached: 0xA101A6 (violet)

45.4.12 Blend Unit (BLU)

45.4.12.1 Functionality

The Blend Unit performs the following operations as illustrated in the image below:

• Convert raw destination input pixel data (pixel FB_Read_Data read from framebuffer) to internal ARGB8888 format according to the current framebuffer format

• Premultiply destination input when enabled

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• Blend source input pixel color (Color) and converted destination input color independently for A and R, G, B in the following steps

◦ Select source and destination factors

◦ Blend according to blend mode, factors and write mask

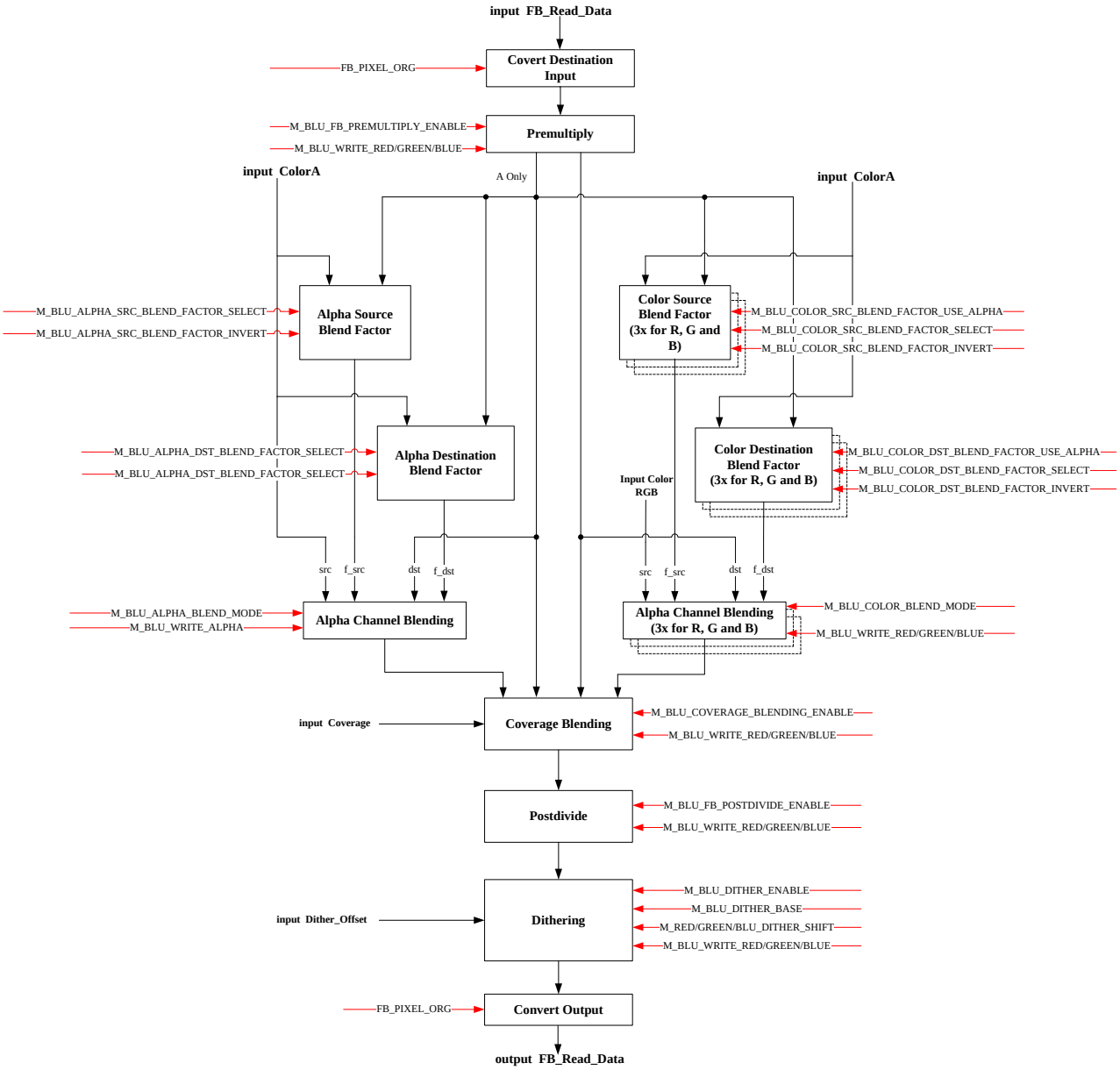
▪ The write mask can be used to pass through the destination color for all 4 channels individually, i.e. to disable blending on individual channels

• Do coverage blending when enabled

• Postdivide coverage blended result when enabled

• Apply dithering to R, G and B channels when enabled

• Convert output ARGB8888 format back to current framebuffer format



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45.4.12.2 Premultiply

When pre-multiplication is enabled, the color channels of the destination color are multiplied by their alpha value. Otherwise they are left unchanged. The write mask suppresses the premultiplication per channel.

45.4.12.3 Alpha/Color write mask

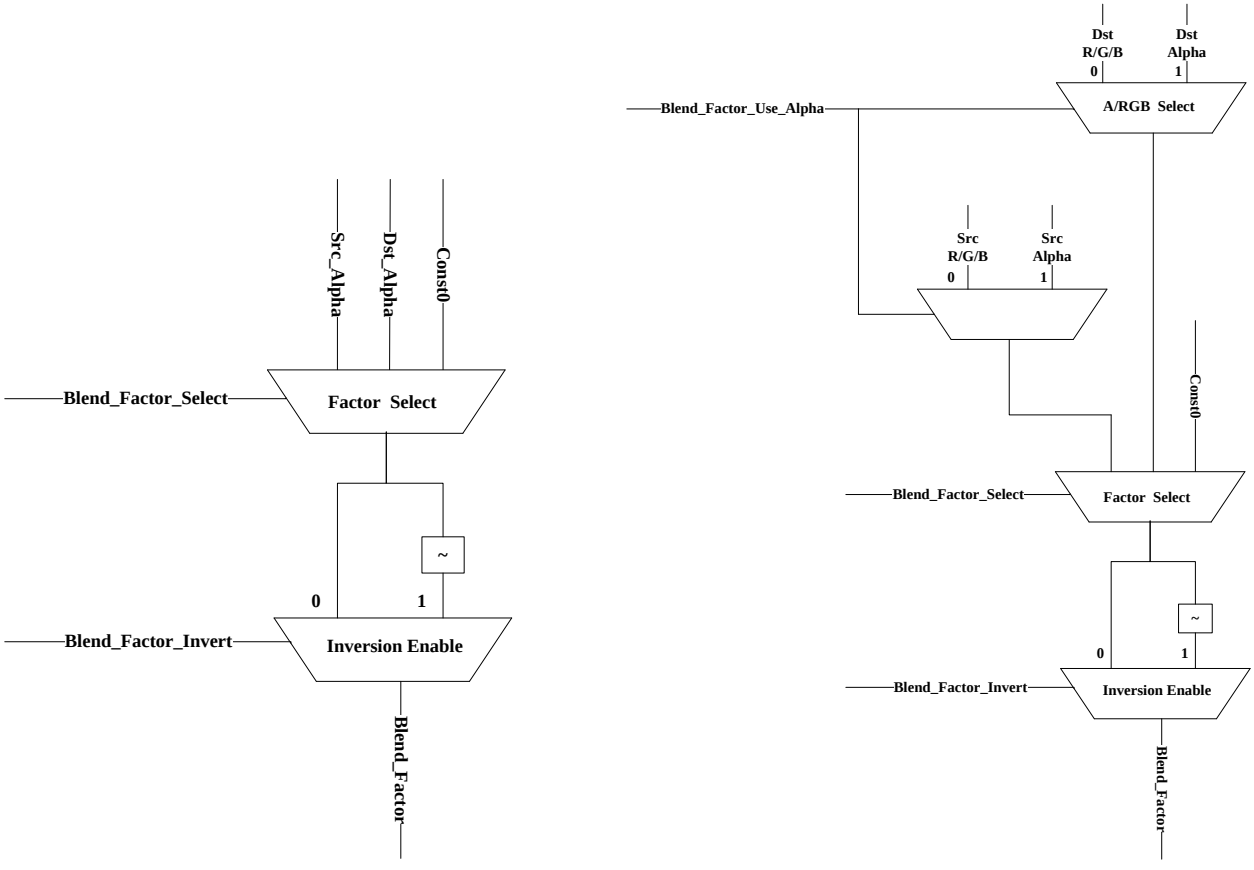
The color write mask enables blending for the selected alpha/color channel. If disabled, the original framebuffer value of the corresponding channel is sent to the output format converter stage.

45.4.12.4 Alpha/Color Blend Factors

The alpha blend factor generation is used two times for source and destination blend factor generation.
The color blend factor generation is used six times in total: Three times each for R, G and B for both source and destination blend factor generation.

The difference between alpha and color blend factor generation is that in color blend factor generation, the control 'USE_ALPHA' is used to select between Alpha and the respective color channel (R/G/B) at the input.

Figure 45-5 Alpha Blend Factor generation



45.4.12.5 Color Channel Blending

This module is used 3 times for R, G and B. R, G and B share a single set of blend factors and blend mode as can be seen in the image above. The 'BLU_WRITE_X' control exists one time for each of the 3 instances.

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45.4.12.6 Coverage Blending

The coverage blending applies the coverage value by blending the result of the alpha/color channel blending stage with the framebuffer content.

45.4.12.7 Postdivide

When post-division is enabled, the color channels after coverage blending are divided by their alpha channel. Otherwise they are left unchanged. The write mask suppresses the post-division per channel.

45.4.12.8 Dithering

Dithering is only done on the R, G and B channels. When enabled, it adds a 1- to 4-bit value (selectable through the channels 'dither_shift' register controls) to the respective color channels. The purpose is to add some 'noise' in case the output format has less than 8 bits per channel to reduce e.g. banding artefacts.

45.4.12.9 Convert Output

Assembles a raw_pixel of 8-, 16- or 32-bit width by concatenating the respective number of MSBs from the alpha and color channels. In case of less than 4 bytes in the format, the pixel is repeated 2 or 4 times.

45.5 Registers

45.5.1 Stream Controller (STC) Register

Base Address 0x5004 0000

45.5.1.1 Hardware Version Register (VERSION)

The register is read-only include hardware version.

Offset Address 0x00

Reset Value 0xD404 0701

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CONSTANT[7:0]								HW_CONFIG_ID[7:0]							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_VERSION[7:0]								HW_REVISION[7:0]							
r								r							

Bit field	Name	Description
31:24	CONSTANT[7:0]	Constant 0xD4
23:16	HW_CONFIG_ID[7:0]	Hardware configuration ID
15:8	HW_VERSION[7:0]	Hardware version
7:0	HW_REVISION[7:0]	Hardware revision (for bug fixes etc)

45.5.1.2 Configure 1 Register (CONFIG_1)

The register is read-only.

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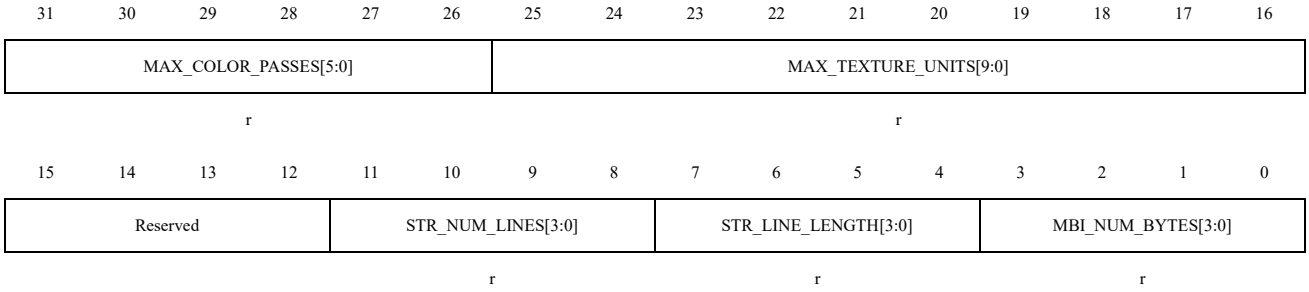
Offset Address 0x04

Reset Value 0x0302 0243



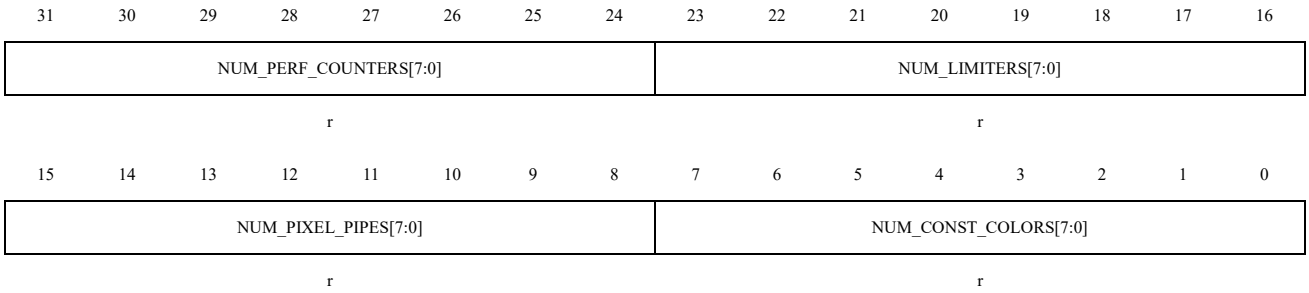
Bit field	Name	Description
31:26	MAX_COLOR_PASSES[5:0]	Maximum numbers of color passes.
25:16	MAX_TEXTURE_UNITS[9:0]	Maximum numbers of texture units.
15:12	Reserved	Reserved,the reset value must be maintained
11:8	STR_NUM_LINES[3:0]	Numbers of stream reader lines.
7:4	STR_LINE_LENGTH[3:0]	Length of stream reader lines.
3:0	MBI_NUM_BYTES[3:0]	Numbers of MBI in bytes.

45.5.1.3 Configure 2 Register (CONFIG_2)

The register is read-only.

Offset Address 0x08

Reset Value 0x0406 0104



Bit field	Name	Description
31:24	NUM_PERF_COUNTERS[7:0]	Numbers of performance counters.
23:16	NUM_LIMITERS[7:0]	Numbers of limiters.
15:8	NUM_PIXEL_PIPES[7:0]	Numbers of pixel pipes.
7:0	NUM_CONST_COLORS[7:0]	Numbers of const colors.

45.5.1.4 Configure 3 Register (CONFIG_3)

The register is read-only.

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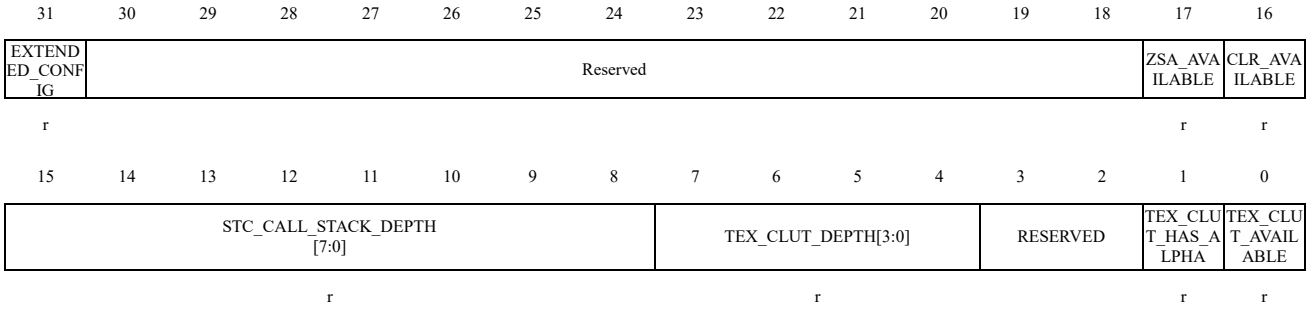
Offset Address 0x0C

Reset Value 0x8001 0493



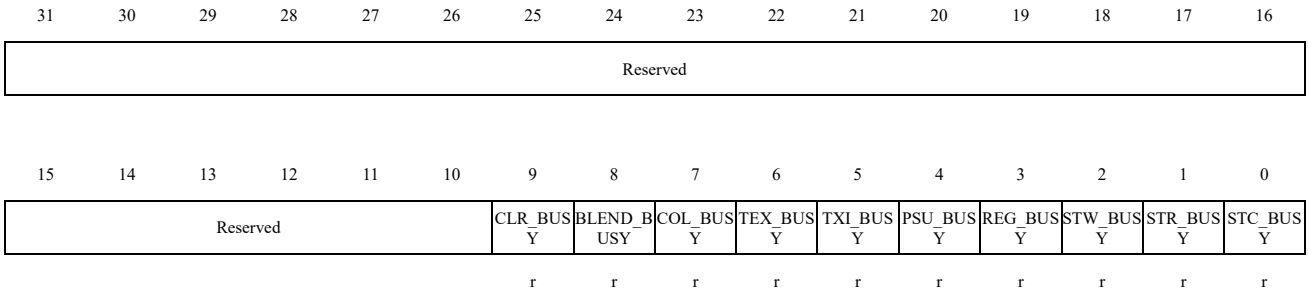
Bit field	Name	Description
31	EXTENDED_CONFIG	Extended config
30:18	Reserved	Reserved,the reset value must be maintained
17	ZSA_AVAILABLE	ZSA available
16	CLR_AVAILABLE	CLR available
15:8	STC_CALL_STACK_DEPTH[7:0]	STC call stack depth
7:4	TEX_CLUT_DEPTH[3:0]	TEX CLUT depth
3:2	Reserved	Reserved,the reset value must be maintained
1	TEX_CLUT_HAS_ALPHA	TEX CLUT has alpha
0	TEX_CLUT_AVAILABLE	TEX CLUT available

45.5.1.5 Busy Status Flag Register (BUSY_STATUS)

The register is read-only.

Offset Address 0x10

Reset Value 0x0000 0000



Bit field	Name	Description
31:10	Reserved	Reserved,the reset value must be maintained
9	CLR_BUSY	Clear unit busy bits, 1 indicates busy, 0 indicates idle.
8	BLEND_BUSY	BLEND Modules after FBS, up to FBC busy bits, 1 indicates busy, 0 indicates idle.

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Bit field	Name	Description
7	COL_BUSY	COL Modules after TXS, up to FBS busy bits, 1 indicates busy, 0 indicates idle.
6	TEX_BUSY	TEX Modules after ZSS, up to TXS busy bits, 1 indicates busy, 0 indicates idle.
5	TXI_BUSY	TXI Modules after PSU, up to ZSS busy bits, 1 indicates busy, 0 indicates idle.
4	PSU_BUSY	Pixel selection busy bits, 1 indicates busy, 0 indicates idle.
3	REG_BUSY	Register file busy bits, 1 indicates busy, 0 indicates idle.
2	STW_BUSY	Stream writer busy bits, 1 indicates busy, 0 indicates idle.
1	STR_BUSY	Stream reader busy bits, 1 indicates busy, 0 indicates idle.
0	STC_BUSY	Stream controller busy bits, 1 indicates busy, 0 indicates idle.

45.5.1.6 STC Control Register (CONTROL)

The register is read-write.

Offset Address 0x14

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LIMIT_RING_PREFETCH	STREAM_HALT_REQUEST	STALL_REQUEST	Reserved	CHECKSUM_PROTECTION_MODE	Reserved	PERMANENT_ENABLE_CLOCK	Reserved			SYNC_IRQ_ENABLE	MBI_ERROR_IRQ_ENABLE	STALL_IRQ_ENABLE	PAUSE_IRQ_ENABLE	STOP_IRQ_ENABLE
	rw	rw	rw		rw		rw				rw	rw	rw	rw	rw

Bit field	Name	Description
31:15	Reserved	Reserved,the reset value must be maintained
14	LIMIT_RING_PREFETCH	Limit prefetch in ring (stack level 0)
13	STREAM_HALT_REQUEST	Stream halt request (automatically reset on successful stream halt)
12	STALL_REQUEST	Stall request
11	Reserved	Reserved,the reset value must be maintained
10	CHECKSUM_PROTECTION_MODE	Checksum protection mode
9	Reserved	Reserved,the reset value must be maintained
8	PERMANENT_ENABLE_CLOCK	Permanent clock enable
7:5	Reserved	Reserved,the reset value must be maintained
4	SYNC_IRQ_ENABLE	Sync IRQ enable
3	MBI_ERROR_IRQ_ENABLE	MBI error IRQ enable
2	STALL_IRQ_ENABLE	Stall IRQ enable
1	PAUSE_IRQ_ENABLE	Pause IRQ enable
0	STOP_IRQ_ENABLE	Stop IRQ enable

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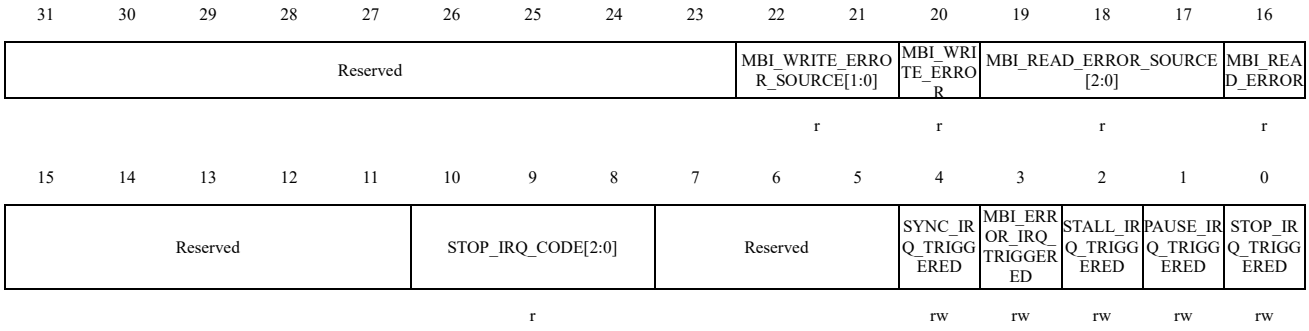
45.5.1.7 Interrupt Status Register (INTERRUPT_STATUS)

The register is read-write.

Offset Address 0x18

Reset Value 0x0000 0000



Bit field	Name	Description
31:23	Reserved	Reserved,the reset value must be maintained
22:21	MBI_WRITE_ERROR_SOURCE[1:0]	MBI write error source 0 = STW : Stream writer 1 = CLR : Clear unit 2 = FBC : Framebuffer cache write side 3 = ZSC : ZSA cache write side
20	MBI_WRITE_ERROR	See Bus error handling on the meaning of this error status bits.
19:17	MBI_READ_ERROR_SOURCE[2:0]	MBI read error source 0 = FBC : Framebuffer cache read side 1 = TXC : Texture cache 2 = RLD : Run-Length decoder 3 = ZSC : ZSA cache read side 4 = STR : Stream reader
16	MBI_READ_ERROR	See Bus error handling on the meaning of this error status bits.
15:11	Reserved	Reserved,the reset value must be maintained
10:8	STOP_IRQ_CODE[2:0]	Stop IRQ code 0 = STREAM_END : Normal end of stream 1 = STREAM_HALT : Halt reached, after halt request 2 = START_WHEN_BUSY : Start signal received while still busy 3 = INVALID_COMMAND : Invalid command (decode error) 4 = STACK_OVERFLOW : Call stack overflow (nesting limit reached) 5 = INVALID_REGISTER : Attempt to write invalid register 6 = CHECKSUM_ERROR : Checksum error detected 7 = STREAM_DATACOUNT : Wrong data count for given opcode
7:5	Reserved	Reserved,the reset value must be maintained
4	SYNC_IRQ_TRIGGERED	Sync IRQ triggered

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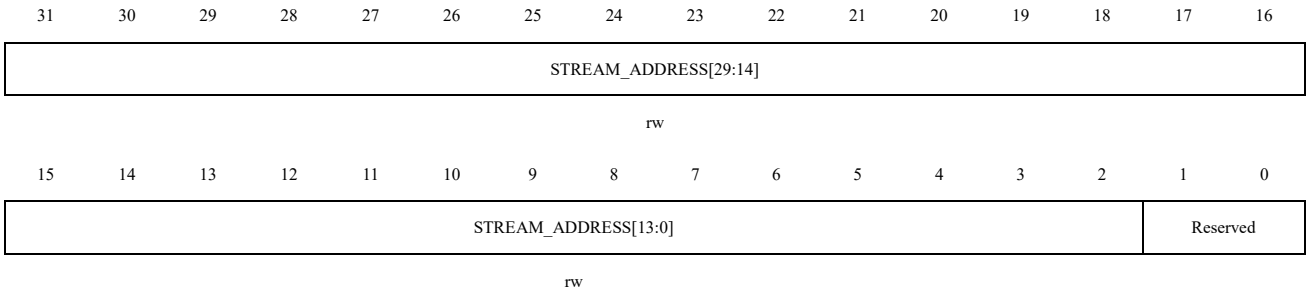
Bit field	Name	Description
3	MBI_ERROR_IRQ_TRIGGERED	MBI error IRQ triggered
2	STALL_IRQ_TRIGGERED	Stall IRQ triggered (see Core Stalling)
1	PAUSE_IRQ_TRIGGERED	Pause IRQ triggered (see Ring-Buffer mode)
0	STOP_IRQ_TRIGGERED	Stop IRQ triggered

45.5.1.8 Stream Address Register (STREAM_ADDRESS)

The register is read-write.

Offset Address 0x1C

Reset Value 0x0000 0000



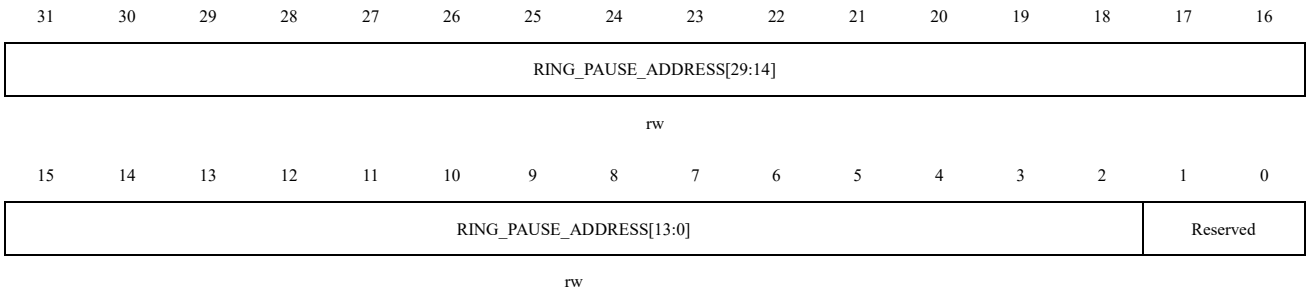
Bit field	Name	Description
31:2	STREAM_ADDRESS[29:0]	Stream start address. A write to this register triggers a start of the stream controller at the given address.
1:0	Reserved	Reserved,the reset value must be maintained

45.5.1.9 Ring Pause Address Register (RING_PAUSE_ADDRESS)

The register is read-write.

Offset Address 0x20

Reset Value 0x0000 0000



Bit field	Name	Description
31:2	RING_PAUSE_ADDRESS[29:0]	Ring-buffer pause address. Address of last word which may be processed before a pause is required.

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Bit field	Name	Description
1:0	Reserved	Reserved,the reset value must be maintained

45.5.1.10 Current Ring Address Register (CURRENT_RING_ADDRESS)

The register is read-write.

Offset Address 0x24

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURRENT_RING_ADDRESS[29:14]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_RING_ADDRESS[13:0]														Reserved	
rw															

Bit field	Name	Description
31:2	CURRENT_RING_ADDRESS[29:0]	Current stream address inside ring-buffer, i.e. on call stack level 0.
1:0	Reserved	Reserved,the reset value must be maintained

45.5.1.11 Current Stream Address Register (CURRENT_STREAM_ADDRESS)

The register is read-write.

Offset Address 0x28

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURRENT_STREAM_ADDRESS[29:14]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_STREAM_ADDRESS[13:0]														Reserved	
rw															

Bit field	Name	Description
31:2	CURRENT_STREAM_ADDRESS[29:0]	Current stream address (possibly inside sub-stream).
1:0	Reserved	Reserved,the reset value must be maintained

45.5.1.12 Current Checksum Register (CURRENT_CHECKSUM)

The register is read-write.

Offset Address 0x2C

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Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURRENT_REFERENCE_CHECKSUM[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_REFERENCE_CHECKSUM[15:0]															
rw															

Bit field	Name	Description
31:0	CURRENT_REFERENCE_CHECKSUM[31:0]	Checksum. A read returns the current stream checksum. A write sets the checksum for the next checksum test, see Checksum Protection.

45.5.1.13 Synchronization ID Register (SYNC_ID_n, n=0～2)

The register is read-write.

Offset Address 0x30+n*4

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNCHRONIZATION_ID_n[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCHRONIZATION_ID_n[15:0]															
rw															

Bit field	Name	Description
31:0	SYNCHRONIZATION_ID_n[31:0]	Synchronization ID for driver usage.

45.5.1.14 Call Stack Pointer Register (CALL_STACK_POINTER)

The register is read-write.

Offset Address 0x3C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	CALL_STACK_POINTER[1:0]
	rw

Bit field	Name	Description
31:2	Reserved	Reserved,the reset value must be maintained
1:0	CALL_STACK_POINTER[1:0]	Call stack pointer.

45.5.1.15 Call Stack Entry Register (CALL_STACK_ENTRY_n, n=0～7)

The register is read-write.

Offset Address 0x40+n*4

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALL_STACK_ENTRY_n[29:14]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALL_STACK_ENTRY_n[13:0]														Reserved	
rw															

Bit field	Name	Description
31:2	CALL_STACK_ENTRY_n[29:0]	Addresses on call stack, 16 successive registers maximum, depending on C_STC_CALL_STACK_DEPTH. Note that one call stack entry is a pair of end address and return address. These two addresses are mapped alternately here in the register map, so the maximum depth of the call stack is 8 entries.
1:0	Reserved	Reserved,the reset value must be maintained

45.5.1.16 Performance Counter Register (PERFORMANCE_COUNTER_VALUES_n, n=0～3)

The register is read-write.

Offset Address 0x80+n*4

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PERFORMANCE_COUNTER_VALUES_n[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PERFORMANCE_COUNTER_VALUES_n[15:0]															
r															

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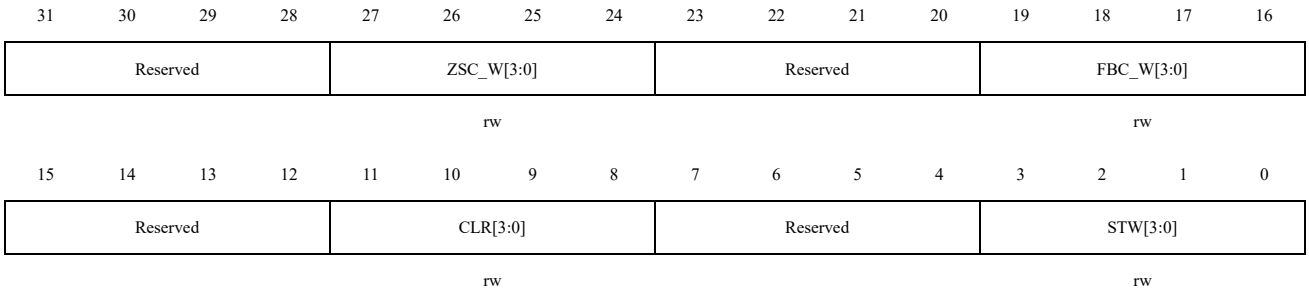
Bit field	Name	Description
31:0	PERFORMANCE_COUNTER_VALUES_n[31:0]	Performance Counter Value

45.5.1.17 Burst Length Limit Write Register (BURST_LENGTH_LIMIT_WRITE)

The register is read-write.

Offset Address 0xC0

Reset Value 0x0F0F 0F0F



Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:24	ZSC_W[3:0]	ZSC write burst length limit (reserved)
23:20	Reserved	Reserved,the reset value must be maintained
19:16	FBC_W[3:0]	FBC write burst length limit (reserved)
15:12	Reserved	Reserved,the reset value must be maintained
11:8	CLR[3:0]	CLR burst length limit (reserved)
7:4	Reserved	Reserved,the reset value must be maintained
3:0	STW[3:0]	STW burst length limit (reserved)

45.5.1.18 Burst Length Limit Read 0 Register (BURST_LENGTH_LIMIT_READ_0)

The register is read-write.

Offset Address 0xC4

Reset Value 0x0F0F 0F0F

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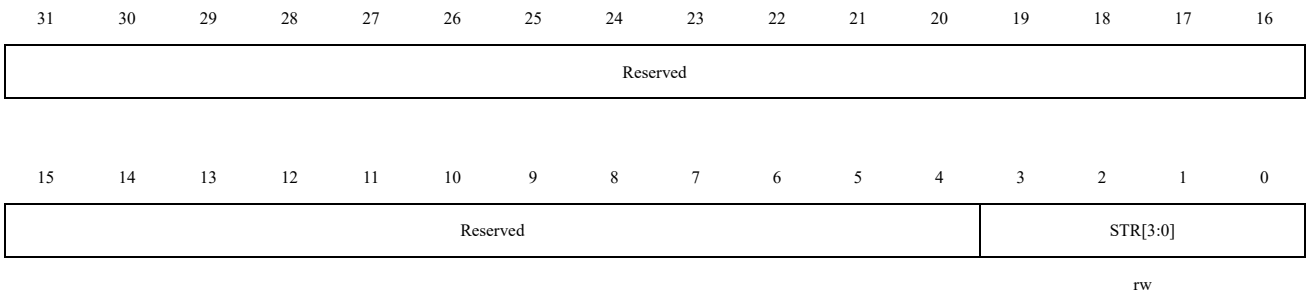
Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:24	ZSC_R[3:0]	ZSC read burst length limit (reserved)
23:20	Reserved	Reserved,the reset value must be maintained
19:16	RLD[3:0]	RLD burst length limit
15:12	Reserved	Reserved,the reset value must be maintained
11:8	TXC[3:0]	TXC burst length limit
7:4	Reserved	Reserved,the reset value must be maintained
3:0	FBC[3:0]	FBC read burst length limit (reserved)

45.5.1.19 Burst Length Limit Read 1 Register (BURST_LENGTH_LIMIT_READ_1)

The register is read-write.

Offset Address 0xC8

Reset Value 0x0000 000F



Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3:0	STR[3:0]	STR burst length limit (reserved)

45.5.2 Pixel Selection Unit (PSU) Register

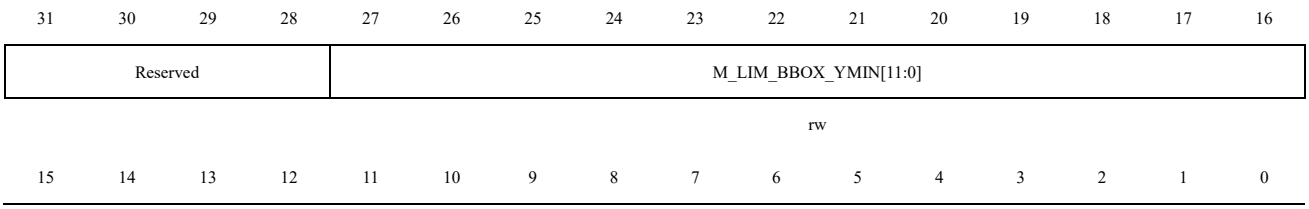
Base Address 0x5004 0200

45.5.2.1 Limiter BoundingBox Minimum Value Register (LIM_BBOX_MIN)

The register is read-write.

Offset Address 0x00

Reset Value 0x0000 0000



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Reserved	M_LIM_BBOX_XMIN[11:0]

rw

Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:16	M_LIM_BBOX_YMIN[11:0]	The minimum y-coordinate of the limiter bounding box
15:12	Reserved	Reserved,the reset value must be maintained
11:0	M_LIM_BBOX_XMIN[11:0]	The minimum x-coordinate of the limiter bounding box

45.5.2.2 Limiter BoundingBox Maximum Value Register (LIM_BBOX_MAX)

The register is read-write.

Offset Address 0x04

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				M_LIM_BBOX_YMAX[11:0]											

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				M_LIM_BBOX_XMAX[11:0]											

rw

Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:16	M_LIM_BBOX_YMAX[11:0]	The maximum y-coordinate of the limiter bounding box
15:12	Reserved	Reserved,the reset value must be maintained
11:0	M_LIM_BBOX_XMAX[11:0]	The maximum x-coordinate of the limiter bounding box

45.5.2.3 Limiter Start Position Register (LIM_START)

The register is read-write.

Offset Address 0x08

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				M_LIM_START_Y[11:0]											

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

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Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:16	M_LIM_START_Y[11:0]	The y-coordinate of the starting position of the Limiter (the starting position of x is the left boundary of the bounding box).
15:0	Reserved	Reserved,the reset value must be maintained

45.5.2.4 Limiter Control Register (LIM_CTRL)

The register is read-write.

Offset Address 0x0C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		M_BEZ_CTRL[1:0]		Reserved				M_LIM_CTRL_5[3:0]				M_LIM_CTRL_4[3:0]			
		rw						rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_LIM_CTRL_3[3:0]				M_LIM_CTRL_2[3:0]				M_LIM_CTRL_1[3:0]				M_LIM_CTRL_0[3:0]			
rw				rw				rw				rw			

Bit field	Name	Description
31:30	Reserved	Reserved,the reset value must be maintained
29:28	M_BEZ_CTRL[1:0]	Bézier control register Bit 0 :Set 1 to enable Bezier function Bit 1 :Select concave(1) or convex(0) Bezier element
27:24	Reserved	Reserved,the reset value must be maintained
23:20	M_LIM_CTRL5[3:0]	LIMITER_n control register M_LIM_CTRL_n[3:0]
19:16	M_LIM_CTRL4[3:0]	Bit 0 :Enable limiter
15:12	M_LIM_CTRL3[3:0]	Bit 1 :Shared edges (no Anti-aliasing)
11:8	M_LIM_CTRL2[3:0]	Bit 2 :Use for enumeration (a Limiter can be used for Bezier function only)
7:4	M_LIM_CTRL1[3:0]	Bit 3 :Invert Limiter,reuse dx and dy inverted
3:0	M_LIM_CTRL0[3:0]	

45.5.2.5 Limiter Stripe Register (LIM_STRIPE)

The register is read-write.

Offset Address 0x10

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Reserved	M_LIM_STRIPE_OFFSET[7:0]

rw

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved	M_LIM_STRIPE_OFFSET[7:0]

rw

Bit field	Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
23:16	M_LIM_STRIPE_OFFSET[7:0]	Limiter stripe offset
15:8	Reserved	Reserved,the reset value must be maintained
7:0	M_LIM_STRIPE_WIDTH[7:0]	Limiter stripe width (0 = full span, no stripe-wise enumeration)

45.5.2.6 Bézier Control Register (BEZ_CTRL)

The register is read-write.

Offset Address 0x14

Reset Value 0x0000 0000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

Reserved

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved	M_BEZ_LIM_SCALE[5:0]

rw

Bit field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained
5:0	M_BEZ_LIM_SCALE[5:0]	Bézier limiter scale

45.5.2.7 Bézier Limiter Offset 0 Register (BEZ_VOFF_0)

The register is read-write.

Offset Address 0x18

Reset Value 0x0000 0000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

M_BEZ_VOFF_0[31:16]

rw

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

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M_BEZ_VOFF_0[15:0]

rw

Bit field	Name	Description
31:0	M_BEZ_VOFF_0[31:0]	Bézier limiter offset 0 (14.18 signed fixed point)

45.5.2.8 Bézier Limiter Offset 1 Register (BEZ_VOFF_1)

The register is read-write.

Offset Address 0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_BEZ_VOFF_1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_BEZ_VOFF_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_BEZ_VOFF_1[31:0]	Bézier limiter offset 1 (14.18 signed fixed point)

45.5.2.9 Bézier Limiter Anti-Aliasing Control Register (BEZ_AA_CTRL)

The register is read-write.

Offset Address 0x20

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						M_BEZ_AA[9:0]									
						rw									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_BEZ_AA_OFFSET[7:0]								M_BEZ_WIDTH[7:0]							
rw								rw							

Bit field	Name	Description
31:26	Reserved	Reserved,the reset value must be maintained
25:16	M_BEZ_AA[9:0]	1/width of anti-aliasing for Bezier element (4.6 unsigned fixed point)
15:8	M_BEZ_AA_OFFSET[7:0]	Anti-aliasing offset to shift anti-aliasing region from inside to outside of

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Bit field	Name	Description
		curve (4.4 signed fixed point)
7:0	M_BEZ_WIDTH[7:0]	Bezier width control (4.4 unsigned fixed point): 0 : full convex or concave Bezier segment >0 : Bezier line

45.5.2.10 Bézier Limiter Start Value Register (LIM_VSTART_n, n=0～5)

The register is read-write.

Offset Address 0x24+n*0x0C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_LIM_VSTART_n[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_LIM_VSTART_n[15:0]															
rw															

Bit field	Name	Description
31:0	M_LIM_VSTART_n[31:0]	Initial Limiter value of enumeration start position (14.18 signed fixed point)，n=0～5

45.5.2.11 Bézier Limiter x increment Register (LIM_DX_n, n=0～5)

The register is read-write.

Offset Address 0x28+n*0x0C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												M_LIM_DX_n[19:16]			
												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_LIM_DX_n[15:0]															
rw															

Bit field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained
19:0	M_LIM_DX_n[19:0]	Fractional part of Limiter x step (2.18 signed fixed point)，n=0～5

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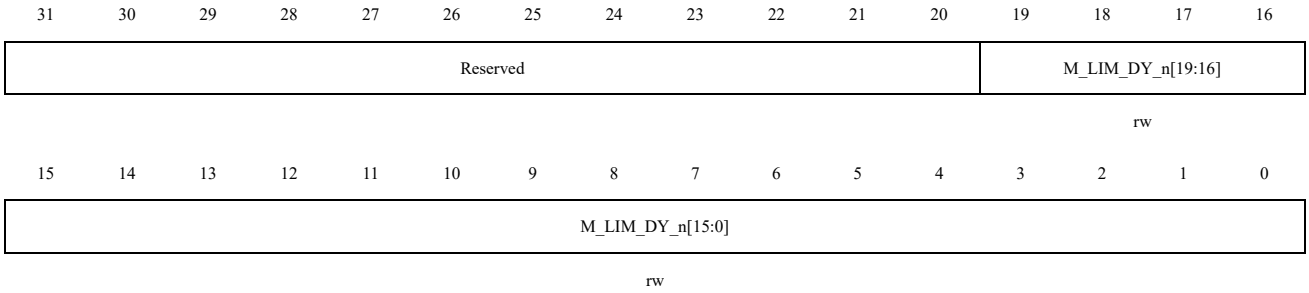
45.5.2.12 Bézier Limiter y increment Register (LIM_DY_n, n=0～5)

The register is read-write.

Offset Address 0x2C+n*0x0C

Reset Value 0x0000 0000



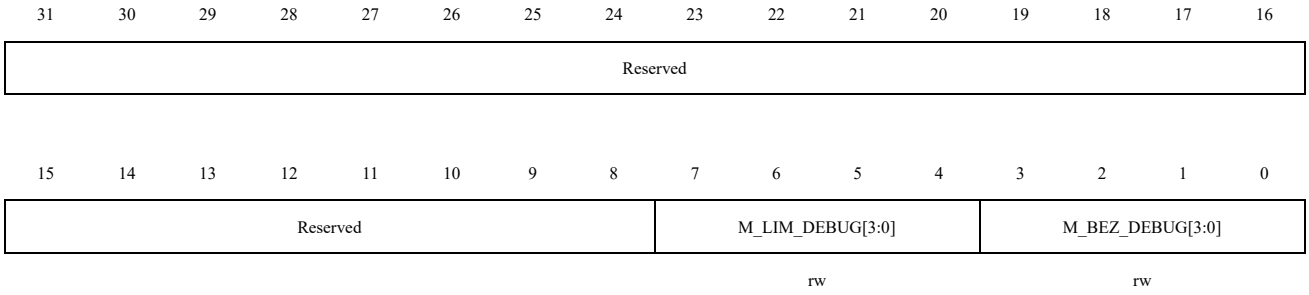
Bit field	Name	Description
31:20	Reserved	Reserved,the reset value must be maintained
19:0	M_LIM_DY_n[19:0]	Fractional part of Limiter y step (2.18 signed fixed point)，n=0～5

45.5.2.13 Debug Control Register (DEBUG_CTRL)

The register is read-write.

Offset Address 0x6C

Reset Value 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved,the reset value must be maintained
7:4	M_LIM_DEBUG[3:0]	Limiter debug control bit (reserved)
3:0	M_BEZ_DEBUG[3:0]	Bézier limiter debug control bit (reserved)

45.5.2.14 Limiter Bounding Box Register (LIM_BBOX_MAX)

The register is read-write.

Offset Address 0x70

Reset Value 0x0FFF 0FFF

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				M_LIM_YMAX[11:0]											
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				M_LIM_XMAX[11:0]											
rw															

Bit field	Name	Description
31:28	Reserved	Reserved,the reset value must be maintained
27:16	M_LIM_YMAX[11:0]	Boundary box clipping limit y maximum coordinate
15:12	Reserved	Reserved,the reset value must be maintained
11:0	M_LIM_XMAX[11:0]	Boundary box clipping limit x maximum coordinate

45.5.3 Texel U/V Interpolation Register

Base Address 0x5004 0300

45.5.3.1 U Offset 0 Register (TXA_U_OFFSET_0)

The register is read-write.

Offset Address 0x00

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_U_OFFSET_0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_U_OFFSET_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_U_OFFSET_0[31:0]	Start value (offset) for texture unit 0 U coordinate. Refers to the object start position respectively to the screen origin (depends on the implementation of the texel coordinate calculation).

45.5.3.2 V Offset 0 Register (TXA_V_OFFSET_0)

The register is read-write.

Offset Address 0x04

Reset Value 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_V_OFFSET_0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_V_OFFSET_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_V_OFFSET_0[31:0]	Start value (offset) for texture unit 0 V coordinate. Refers to the object start position respectively to the screen origin (depends on the implementation of the texel coordinate calculation).

45.5.3.3 X Increment of U Register (TXA_DUX_0)

The register is read-write.

Offset Address 0x08

Reset Value 0x3F80 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DUX_0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DUX_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DUX_0[31:0]	Increment of texture U coordinate for a pixel step in X direction.

45.5.3.4 Y Increment of U Register (TXA_DUY_0)

The register is read-write.

Offset Address 0x0C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DUY_0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DUY_0[15:0]															

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rw

Bit field	Name	Description
31:0	M_TXA_DUY_0[31:0]	Increment of texture U coordinate for a pixel step in Y direction

45.5.3.5 X Increment of V Register (TXA_DVX_0)

The register is read-write.

Offset Address 0x10

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DVX_0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DVX_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DVX_0[31:0]	X0 increment of V

45.5.3.6 Y Increment of V Register (TXA_DVY_0)

The register is read-write.

Offset Address 0x14

Reset Value 0x3F80 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DVY_0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DVY_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DVY_0[31:0]	Y0 increment of V

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45.5.3.7 U Offset 1 Register (TXA_U_OFFSET_1)

The register is read-write.

Offset Address 0x18

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_U_OFFSET_1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_U_OFFSET_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_U_OFFSET_1 [31:0]	Start value (offset) for texture unit 1 U coordinate. Refers to the object start position respectively to the screen origin (depends on the implementation of the texel coordinate calculation).

45.5.3.8 V Offset 1 Register (TXA_V_OFFSET_1)

The register is read-write.

Offset Address 0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_V_OFFSET_1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_V_OFFSET_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_V_OFFSET_1[31:0]	Start value (offset) for texture unit 1 V coordinate. Refers to the object start position respectively to the screen origin (depends on the implementation of the texel coordinate calculation).

45.5.3.9 X Increment of U Register (TXA_DUX_1)

The register is read-write.

Offset Address 0x20

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Reset Value 0x3F80 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DUX_1[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DUX_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DUX_1[31:0]	Increment of texture U coordinate for a pixel step in X direction.

45.5.3.10 Y Increment of U Register (TXA_DUY_1)

The register is read-write.

Offset Address 0x24

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DUY_1[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DUY_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DUY_1[31:0]	Increment of texture U coordinate for a pixel step in Y direction.

45.5.3.11 X Increment of V Register (TXA_DVX_1)

The register is read-write.

Offset Address 0x28

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DVX_1[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DVX_1[15:0]															

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rw

Bit field	Name	Description
31:0	M_TXA_DVX_1[31:0]	Increment of texture V coordinate for a pixel step in X direction.

45.5.3.12 Y Increment of V Register (TXA_DVY_1)

The register is read-write.

Offset Address 0x2C

Reset Value 0x3F80 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DVY_1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DVY_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DVY_1[31:0]	Increment of texture V coordinate for a pixel step in Y direction.

45.5.4 Texel RHW and Z Interpolation Register

Base Address 0x5004 0400

45.5.4.1 TXA Z Offset Register (TXA_Z_OFFSET)

The register is read-write.

Offset Address 0x08

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_Z_OFFSET[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_Z_OFFSET[15:0]															
rw															

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Bit field	Name	Description
31:0	M_TXA_Z_OFFSET[31:0]	Start value (offset) for Z coordinate

45.5.4.2 TXA ZX Increment Register (TXA_DZX)

The register is read-write.

Offset Address 0x0C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DZX[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DZX[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DZX[31:0]	Increment of Z coordinate for a pixel step in X direction.

45.5.4.3 TXA ZY Increment Register (TXA_DZY)

The register is read-write.

Offset Address 0x10

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DZY[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DZY[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DZY[31:0]	Increment of Z coordinate for a pixel step in Y direction.

45.5.4.4 TXA Z_RHW Offset Register (TXA_Z_RHW_OFFSET)

The register is read-write.

Offset Address 0x14

Reset Value 0x3F80 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_Z_RHW_OFFSET[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_Z_RHW_OFFSET[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_Z_RHW_OFFSET[31:0]	Start value (offset)for RHW attribute (1/w) of Z.

45.5.4.5 TXA Z_RHWX Increment Register (TXA_Z_DRHWX)

The register is read-write.

Offset Address 0x18

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_Z_DRHWX[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_Z_DRHWX[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_Z_DRHWX[31:0]	Increment of RHW attribute of Z for a pixel step in X direction.

45.5.4.6 TXA Z_RHWY Increment Register (TXA_Z_DRHWY)

The register is read-write.

Offset Address 0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_Z_DRHWY[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_Z_DRHWY[15:0]															
rw															

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Bit field	Name	Description
31:0	M_TXA_Z_DRHWY[31:0]	Increment of RHW attribute of Z for a pixel step in X direction.

45.5.4.7 TXA RHW Offset Register (TXA_RHW_OFFSET_0)

The register is read-write.

Offset Address 0x20

Reset Value 0x3F80 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_RHW_OFFSET_0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_RHW_OFFSET_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_RHW_OFFSET_0[31:0]	Start value for RHW attribute (1/w) of texture unit 0.

45.5.4.8 TXA RHWX Increment Register (TXA_DRHWX_0)

The register is read-write.

Offset Address 0x24

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DRHWX_0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DRHWX_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DRHWX_0[31:0]	Increment of RHW attribute for a pixel step in X direction

45.5.4.9 TXA RHWY Increment Register (TXA_DRHWY_0)

The register is read-write.

Offset Address 0x28

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Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DRHWY_0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DRHWY_0[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DRHWY_0[31:0]	Increment of RHW attribute for a pixel step in Y direction

45.5.4.10 TXA RHW Offset Register (TXA_RHW_OFFSET_1)

The register is read-write.

Offset Address 0x2C

Reset Value 0x3F80 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_RHW_OFFSET_1[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_RHW_OFFSET_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_RHW_OFFSET_1[31:0]	Start value for RHW attribute (1/w) of texture unit 1.

45.5.4.11 TXA RHWX Increment Register (TXA_DRHWX_1)

The register is read-write.

Offset Address 0x30

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DRHWX_1[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DRHWX_1[15:0]															

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rw

Bit field	Name	Description
31:0	M_TXA_DRHWX_1[31:0]	Increment of RHW attribute for a pixel step in X direction

45.5.4.12 TXA RHW Y Increment Register (TXA_DRHWY_1)

The register is read-write.

Offset Address 0x34

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_DRHWY_1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXA_DRHWY_1[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXA_DRHWY_1[31:0]	Increment of RHW attribute for a pixel step in Y direction

45.5.5 Texel Address Calculation (TXA) Register

Base Address 0x5004 0600

45.5.5.1 Texture Unit Size Register 0 (TXA_SIZE_0)

The register is read-write.

Offset Address 0x10

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			M_TXA_HEIGHT_0[12:0]												
			rw												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M_TXA_WIDTH_0[12:0]												
			rw												

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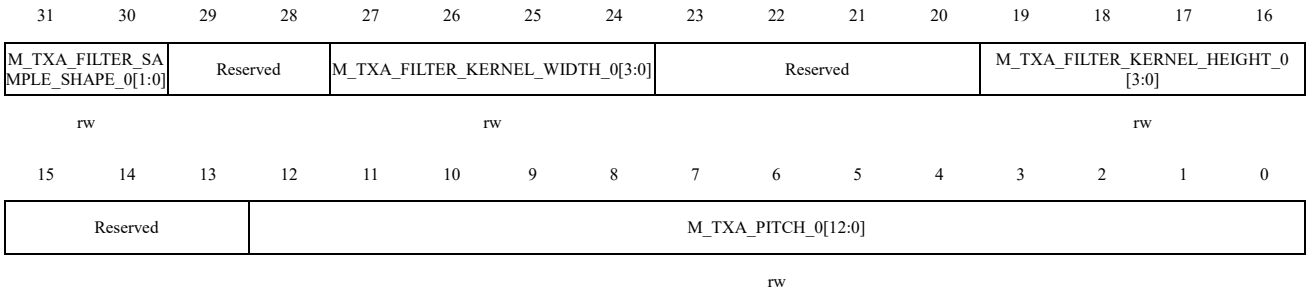
Bit field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28:16	M_TXA_HEIGHT_0[12:0]	Height of the texture in texels.
15:13	Reserved	Reserved,the reset value must be maintained
12:0	M_TXA_WIDTH_0[12:0]	Width of the texture in texels.

45.5.5.2 Texture Unit Access Register 0 (TXA_ACCESS_0)

The register is read-write.

Offset Address 0x14

Reset Value 0x0101 0000



Bit field	Name	Description
31:30	M_TXA_FILTER_SAMPLE_SHAPE_0[1:0]	Shape of a texture filter sample. 0 = QUAD : 2x2 samples (for bilinear filtering or general convolution filtering using a n x m kernel) 1 = ROW : 1x4 samples (for horizontal convolution filtering using a n x 1 kernel) 2 = COLUMN : 4x1 samples (for vertical convolution filtering using a 1 x m kernel)
29:28	Reserved	Reserved,the reset value must be maintained
27:24	M_TXA_FILTER_KERNEL_WIDTH_0[3:0]	Size of filter kernel in U direction-1.
23:20	Reserved	Reserved,the reset value must be maintained
19:16	M_TXA_FILTER_KERNEL_HEIGHT_0[3:0]	Size of filter kernel in V direction-1.
15:13	Reserved	Reserved,the reset value must be maintained
12:0	M_TXA_PITCH_0[12:0]	Unsigned pitch of the texture in texels. Needs to be 0 in case of full swizzling!

45.5.5.3 Texture Unit Size Register 1 (TXA_SIZE_1)

The register is read-write.

Offset Address 0x18

Reset Value 0x0000 0000

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Reserved	M_TXA_HEIGHT_1[12:0]

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M_TXA_WIDTH_1[12:0]												

rw

Bit field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28:16	M_TXA_HEIGHT_1[12:0]	Height of the texture in texels.
15:13	Reserved	Reserved,the reset value must be maintained
12:0	M_TXA_WIDTH_1[12:0]	Width of the texture in texels.

45.5.5.4 Texture Unit Access Register 1 (TXA_ACCESS_1)

The register is read-write.

Offset Address 0x1C

Reset Value 0x0101 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXA_FILTER_SAMPLE_SHAPE_1[1:0]		Reserved		M_TXA_FILTER_KERNEL_WIDTH_1[3:0]				Reserved				M_TXA_FILTER_KERNEL_HEIGHT_1[3:0]			

rw rw rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M_TXA_PITCH_1[12:0]												

rw

Bit field	Name	Description
31:30	M_TXA_FILTER_SAMPLE_SHAPE_1[1:0]	Shape of a texture filter sample. 0 = QUAD : 2x2 samples (for bilinear filtering or general convolution filtering using a n x m kernel) 1 = ROW : 1x4 samples (for horizontal convolution filtering using a n x 1 kernel) 2 = COLUMN : 4x1 samples (for vertical convolution filtering using a 1 x m kernel)
29:28	Reserved	Reserved,the reset value must be maintained
27:24	M_TXA_FILTER_KERNEL_WIDTH_1[3:0]	Size of filter kernel in U direction-1.
23:20	Reserved	Reserved,the reset value must be maintained
19:16	M_TXA_FILTER_KERNEL_HEIGHT_1[3:0]	Size of filter kernel in V direction-1.
15:13	Reserved	Reserved,the reset value must be maintained
12:0	M_TXA_PITCH_1[12:0]	Unsigned pitch of the texture in texels. Needs to be 0 in case of full

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Bit field	Name	Description
		swizzling!

45.5.6 Global and Framebuffer Register

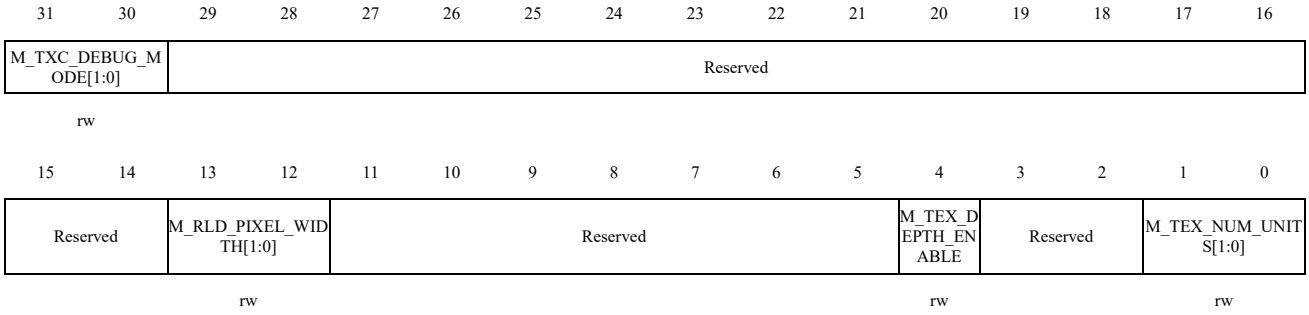
Base Address 0x5004 0800

45.5.6.1 Global Texture Unit Register (TEX_GLOBAL)

The register is read-write.

Offset Address 0x00

Reset Value 0x0000 0000



Bit field	Name	Description
31:30	M_TXC_DEBUG_MODE[1:0]	Texture cache debug mode 0 = NONE : No debugging 1 = SCHEDULING : Highlight pixels, for which a fetch or refresh job was scheduled 2 = WAIT_CYCLES : Highlight pixels, for which a wait at TXC input and/or cache RAM was necessary
29:14	Reserved	Reserved,the reset value must be maintained
13:12	M_RLD_PIXEL_WIDTH[1:0]	Number of bytes per pixel (0=1byte; 1=2bytes; 2=3bytes; 3=4bytes).
11:5	Reserved	Reserved,the reset value must be maintained
4	M_TEX_DEPTH_ENABLE	Activate interpolation of depth as additional pair of U/V coordinates.
3:2	Reserved	Reserved,the reset value must be maintained
1:0	M_TEX_NUM_UNITS[1:0]	Number of active texture units.

45.5.6.2 Global Color Unit Register (COL_GLOBAL)

The register is read-write.

Offset Address 0x04

Reset Value 0x0000 0001

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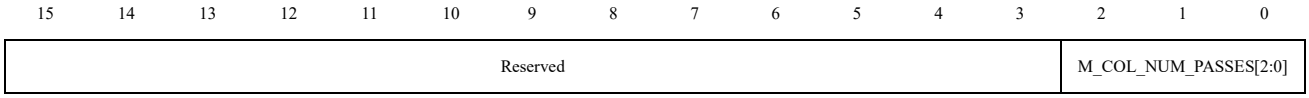


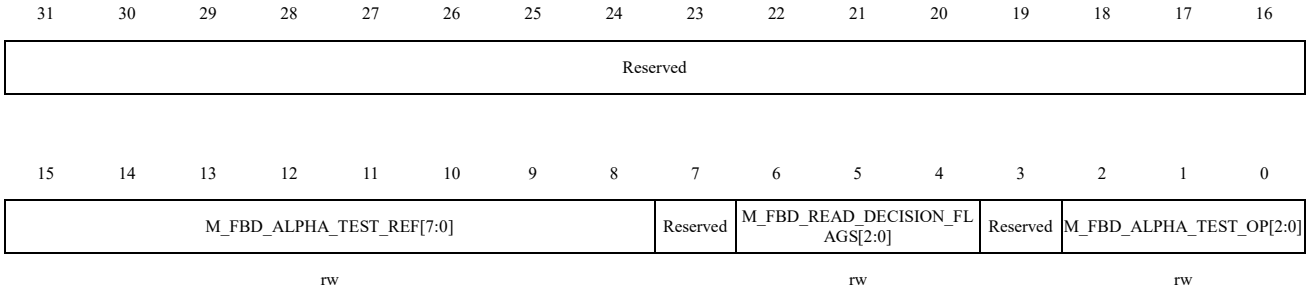
Bit field	Name	Description
31:3	Reserved	Reserved,the reset value must be maintained
2:0	M_COL_NUM_PASSES[2:0]	Number of active color unit passes.

45.5.6.3 Framebuffer Read Decision Register (FBD_CONFIG)

The register is read-write.

Offset Address 0x08

Reset Value 0x0000 0007



Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained
15:8	M_FBD_ALPHA_TEST_REF[7:0]	Alpha test comparison reference value.
7	Reserved	Reserved,the reset value must be maintained
6:4	M_FBD_READ_DECISION_FLAGS[2:0]	Framebuffer read decision flags Bit 0: If enabled,read when pixel alpha != 1.0 Bit 1 : If enabled,read when pixel alpha != 0.0 Bit 2: If enabled,read when coverage != 1.0
3	Reserved	Reserved,the reset value must be maintained
2:0	M_FBD_ALPHA_TEST_OP[2:0]	Alpha test operation: Decides whether the source pixel is passed on or dropped 0 = NEVER : never pass, always drop 1 = LESS : pass if alpha < alpha_ref 2 = EQUAL : pass if alpha == alpha_ref 3 = LESS_OR_EQUAL : pass if alpha less or equal 4 = GREATER : pass if alpha > alpha_ref

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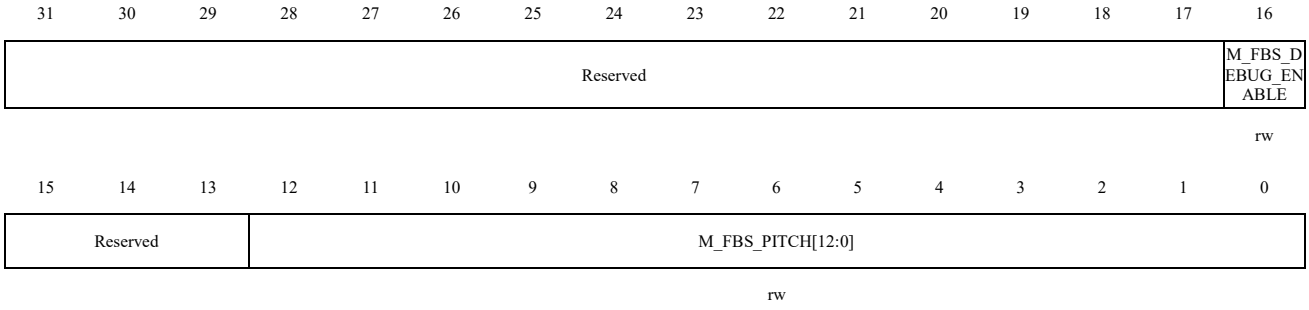
Bit field	Name	Description
		5 = NOT_EQUAL : pass if alpha != alpha_ref 6 = GREATER_OR_EQUAL : pass if alpha >= alpha_ref 7 = ALWAYS : always pass

45.5.6.4 Framebuffer Cache Scheduler Pitch Register (FBS_PITCH)

The register is read-write.

Offset Address 0x0C

Reset Value 0x0000 0000



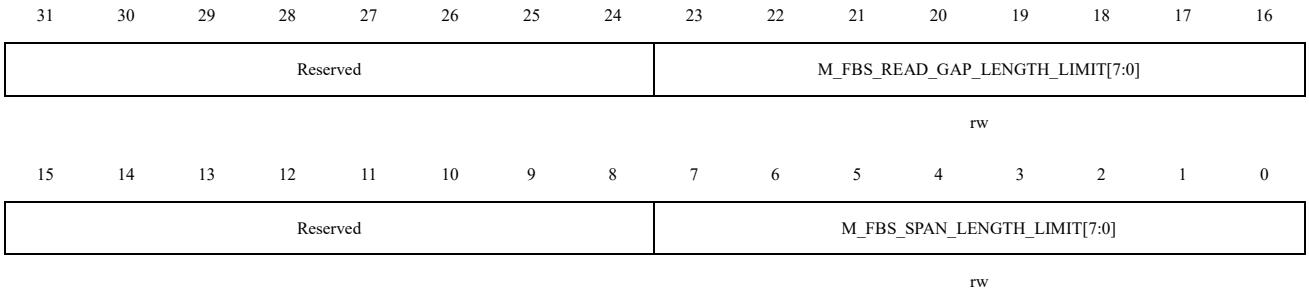
Bit field	Name	Description
31:17	Reserved	Reserved,the reset value must be maintained
16	M_FBS_DEBUG_ENABLE	Enable framebuffer cache scheduler debug mode.
15:13	Reserved	Reserved,the reset value must be maintained
12:0	M_FBS_PITCH[12:0]	Framebuffer pitch.

45.5.6.5 Framebuffer Cache Scheduler Span Config Register (FBS_SPAN_CONFIG)

The register is read-write.

Offset Address 0x10

Reset Value 0x0010 00FF



Bit field	Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
23:16	M_FBS_READ_GAP_LENGTH_LIMIT[7:0]	Maximum length of a read gap inside a span for the framebuffer cache

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Bit field	Name	Description
		in pixels.
15:8	Reserved	Reserved,the reset value must be maintained
7:0	M_FBS_SPAN_LENGTH_LIMIT[7:0]	Maximum length of a span for the framebuffer cache in pixels-1.

45.5.6.6 RLE Start Address Register (RLD_START_ADDRESS)

The register is read-write.

Offset Address 0x14

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_RLD_START_ADDRESS[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_RLD_START_ADDRESS[15:0]															
rw															

Bit field	Name	Description
31:0	M_RLD_START_ADDRESS[31:0]	Start address of RLE code of the texture in memory. Must be aligned to MBI bus width.

45.5.6.7 Constant Color Register (COL_CONST_COLOR_n, n=0～3)

The register is read-write.

Offset Address 0x18+n*4

Reset Value 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_COL_CONST_COLOR_n[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_COL_CONST_COLOR_n[15:0]															
rw															

Bit field	Name	Description
31:0	M_COL_CONST_COLOR_n[31:0]	constant color register [31..24] : 8-Bit alpha channel [23..16] : 8-Bit red channel [15..8] : 8-Bit green channel

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Bit field	Name	Description
		[7..0] : 8-Bit blue channel

45.5.7 Texture and Texel Processing (TXP) Register

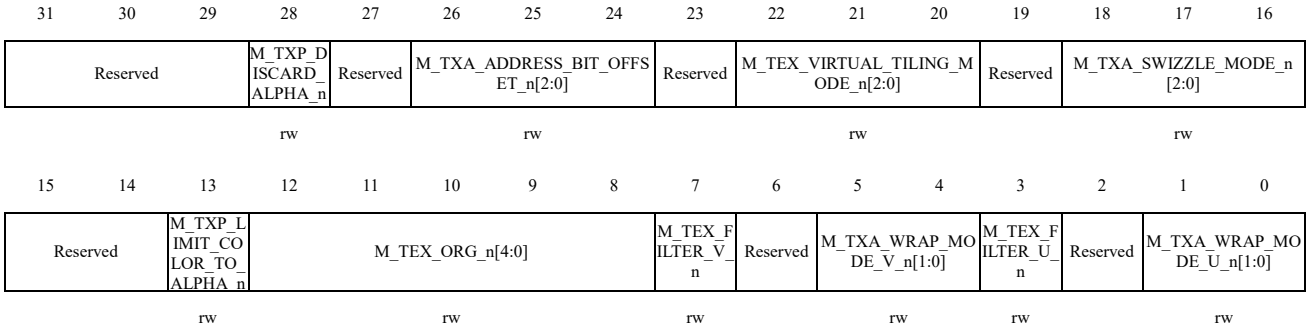
Base Address 0x5004 0A00

45.5.7.1 TXP Texture Mode Register (TEX_MODE_n, n=0～1)

The register is read-write.

Offset Address 0x00+n*0x1C

Reset Value 0x0000 0000



Bit field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28	M_TXP_DISCARD_ALPHA_n	Set alpha to 1.0 instead of using value read from texture. Can be used to set alpha to 1.0 in RGB565 and luminance formats. When CLUT is enabled and contains an alpha value, the alpha value from the CLUT is used instead of a constant 1.0.
27	Reserved	Reserved,the reset value must be maintained
26:24	M_TXA_ADDRESS_BIT_OFFSET_n[2:0]	Bit offset of start of texture relative to byte pointed to by TXC_START_ADDRESS.
23	Reserved	Reserved,the reset value must be maintained
22:20	M_TEX_VIRTUAL_TILING_MODE_n[2:0]	Virtual tiling mode of texture 0 : no virtual tiling (1 burst per cache line) 1 : 2 x virtual tiling (2 bursts per cache line) 2 : 4 x virtual tiling (4 bursts per cache line) 3 : 8 x virtual tiling (8 bursts per cache line) 4 : 16 x virtual tiling (16 bursts per cache line)
19	Reserved	Reserved,the reset value must be maintained
18:16	M_TXA_SWIZZLE_MODE_n[2:0]	Swizzle mode of texture 0= Linear: Normal linear storage 1=Interleaved 4: Limitations regarding pitch/height and start address alignment apply

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Bit field	Name	Description
		2=Interleaved 16: Limitations regarding pitch/height and start address alignment apply 3=Interleaved Full: Limitations regarding pitch/height and start address alignment apply 4=Inverse Interleaved 4: Check TRM regarding usage of this mode 5=Inverse Interleaved 16: Check TRM regarding usage of this mode 6=Virtual Tiled: Limitations regarding pitch/height and start address alignment apply
15:14	Reserved	Reserved,the reset value must be maintained
13	M_TXP_LIMIT_COLOR_TO_ALPHA_n	Boolean value: Limit color values of R, G and B channels to the alpha channel value when enabled (for pre-multiplied formats).
12:8	M_TEX_ORG_n[4:0]	Texel organization/format of texture 0 = ARGB_8888 : 4 channel 8888, 32 bit 1 = RGBA_8888 : 4 channel 8888, 32 bit 2 = ARGB_4444 : 4 channel 4444, 16 bit 3 = RGBA_4444 : 4 channel 4444, 16 bit 4 = ARGB_1555 : 4 channel 1555, 16 bit 5 = RGBA_5551 : 4 channel 5551, 16 bit 6 = RGB_565 : 3 channel 565, 16 bit (alpha=blue channel) 7 = AL_88 : 2 channel 88, 16 bit (alpha=channel1, R/G/B=channel0) 8 = AL_44 : 2 channel 44, 8 bit (alpha=channel1, R/G/B=channel0) 9 = AL_17 : 2 channel 17, 8 bit (alpha=channel1, R/G/B=channel0) 10 = AL_8 : 1 channel, 8 bit (A/R/G/B=same value) 11 = AL_4 : 1 channel, 4 bit (A/R/G/B=same value) 12 = AL_2 : 1 channel, 2 bit (A/R/G/B=same value) 13 = AL_1 : 1 channel, 1 bit (A/R/G/B=same value) 14 = ARGB_2222 : 4 channel 2222, 8 bit 15 = RGBA_2222 : 4 channel 2222, 8 bit 16 = RGB_888 : 3 channel 888, 24 bit (alpha=blue channel) 17 = BGR_888 : 3 channel 888, 24 bit (alpha=blue channel) 18 = ARGB_8565 : 4 channel 8565, 24 bit 19 = RGBA_5658 : 4 channel 5658, 24 bit
7	M_TEX_FILTER_V_n	Filter enable in V direction.
6	Reserved	Reserved,the reset value must be maintained
5:4	M_TXA_WRAP_MODE_V_n[1:0]	Wrap mode in V direction 0 = CLAMP : Clamp texture 1 = REPEAT : Repeat texture 2 = MIRROR : Mirror texture 3 = FILL : Fill texture
3	M_TEX_FILTER_U_n	Filter enable in U direction.
2	Reserved	Reserved,the reset value must be maintained
1:0	M_TXA_WRAP_MODE_U_n[1:0]	Wrap mode in U direction

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Bit field	Name	Description
		0 = CLAMP : Clamp texture 1 = REPEAT : Repeat texture 2 = MIRROR : Mirror texture 3 = FILL : Fill texture

45.5.7.2 TXP Texture Start Address Register (TXC_START_ADDRESS_n, n=0～1)

The register is read-write.

Offset Address 0x04+n*0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXC_START_ADDRESS_n[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXC_START_ADDRESS_n[15:0]															
rw															

Bit field	Name	Description
31:0	M_TXC_START_ADDRESS_n[31:0]	Start address of top-left texel of the texture in memory. May be unaligned to MBI bus width in case of linear stored textures with linear addressing: LSB part is applied inside TXA module.

45.5.7.3 TXP Control Register (TXP_CTRL_n, n=0～1)

The register is read-write.

Offset Address 0x08+n*0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	M_TXC_BURST_PITCH_n[14:0]														
	rw														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							M_TXC_USE_RLD_n	Reserved		M_TXP_COLOR_KEY_ENABLE_n		Reserved	M_TXP_CLUT_MODE_n[2:0]		
							rw			rw			rw		

Bit field	Name	Description
31	Reserved	Reserved,the reset value must be maintained
30:16	M_TXC_BURST_PITCH_n[14:0]	Pitch in bytes between two bursts if texture cache operates in virtual tiling

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Bit field	Name	Description
		mode.
15:9	Reserved	Reserved,the reset value must be maintained
8	M_TXC_USE_RLD_n	Texture is run length encoded (RLE), use RLD for decoding (since there is only one RLD unit max one of the texture units can set this bit).
7:5	Reserved	Reserved,the reset value must be maintained
4	M_TXP_COLOR_KEY_ENABLE_n	Replace alpha and RGB of pixel by all 0 when color key matches.
3	Reserved	Reserved,the reset value must be maintained
2:0	M_TXP_CLUT_MODE_n[2:0]	Configure usage of LUT in texel processing 0 = OFF : don't use the LUT 1 = INDEXED_COLOR : LUT contains colors to be indexed 2 = MAP_RGB : LUT contains RGB color map values 3 = MAP_ARGB : LUT contains ARGB color map values 4 = CONVOLUTION : LUT contains weights for convolution (unsigned) 5 = CONVOLUTION_SIGNED : LUT contains weights for convolution (signed)

45.5.7.4 TXP CLUT Offset Register (TXP_CLUT_OFFSET_n, n=0～1)

The register is read-write.

Offset Address 0x0C+n*0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							M_TXP_CLUT_OFFSET_n[8:0]								
							rw								

Bit field	Name	Description
31:9	Reserved	Reserved,the reset value must be maintained
8:0	M_TXP_CLUT_OFFSET_n[8:0]	Offset for all CLUT lookups of the texture unit.

45.5.7.5 TXP Color Key Register (TXP_COLOR_KEY_n, n=0～1)

The register is read-write.

Offset Address 0x10+n*0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								M_TXP_COLOR_KEY_n[23:16]							

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rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXP_COLOR_KEY_n[15:0]															

rw

Bit field	Name	Description
31:24	Reserved	Reserved,the reset value must be maintained
23:0	M_TXP_COLOR_KEY_n[23:0]	Color key comparison value [7..0] = B : COLOR8 : 8-Bit blue channel [15..8] = G : COLOR8 : 8-Bit green channel [23..16] = R : COLOR8 : 8-Bit red channel

45.5.7.6 TXP Fill Color Register (TXP_FILL_COLOR_n, n=0～1)

The register is read-write.

Offset Address 0x14+n*0x1C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_TXP_FILL_COLOR_n[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXP_FILL_COLOR_n[15:0]															

rw

Bit field	Name	Description
31:0	M_TXP_FILL_COLOR_n[31:0]	Texel fill color for wrap mode FILL [7..0] = B : COLOR8 : 8-Bit blue channel [15..8] = G : COLOR8 : 8-Bit green channel [23..16] = R : COLOR8 : 8-Bit red channel [31..24] = A : ALPHA8 : 8-Bit alpha channel

45.5.7.7 TXP Filter Scale Bias Register (TXP_FILTER_SCALE_BIAS_n, n=0～1)

The register is read-write.

Offset Address 0x18+n*0x1C

Reset Value 0x0000 0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			M_TXP_FILTER_BIAS_n[8:0]									Reserved		M_TXP_FILTER_SHIFT_n[5:4]	

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						rw									rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_TXP_FILTER_SHIFT_n[3:0]				Reserved		M_TXP_FILTER_SCALE_n[9:0]									
rw						rw									

Bit field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28:20	M_TXP_FILTER_BIAS_n[8:0]	Bias for filtering in TXP unit.
19:18	Reserved	Reserved,the reset value must be maintained
17:12	M_TXP_FILTER_SHIFT_n[5:0]	Shift of scale for filtering in TXP unit.
11:10	Reserved	Reserved,the reset value must be maintained
9:0	M_TXP_FILTER_SCALE_n[9:0]	Scale for filtering in TXP unit.

45.5.8 Color Unit (COL) Register

Base Address 0x5004 0B00

45.5.8.1 COL ARGB Op1a Register (COL_ARGB_OP1A_n, n=0～2)

The register is read-write.

Offset Address 0x00+n*0x18

Reset Value 0x0000 06C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	M_COL_ALPHA_OP1A_MUL2_n	M_COL_ALPHA_OP1A_INVERT_MODE_n[1:0]		Reserved		M_COL_ALPHA_OP1A_ARGB_SELECT_n[1:0]		Reserved			M_COL_ALPHA_OP1A_INPUT_SELECT_n[4:0]				
	rw	rw				rw					rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	M_COL_RGB_OP1A_MUL2_n	M_COL_RGB_OP1A_INVERT_MODE_n[1:0]		M_COL_RED_OP1A_ARGB_SELECT_n[1:0]		M_COL_GREEN_OP1A_ARGB_SELECT_n[1:0]		M_COL_BLUE_OP1A_ARGB_SELECT_n[1:0]		Reserved	M_COL_RGB_OP1A_INPUT_SELECT_n[4:0]				
	rw	rw		rw		rw		rw			rw				

Bit field	Name	Description
31	Reserved	Reserved,the reset value must be maintained
30	M_COL_ALPHA_OP1A_MUL2_n	Enable shift left by 1 for alpha op1a.
29:28	M_COL_ALPHA_OP1A_INVERT_MODE_n[1:0]	Select inversion mode for alpha op1a. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
27:26	Reserved	Reserved,the reset value must be maintained

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Bit field	Name	Description
25:24	M_COL_ALPHA_OP1A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1a (alpha path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
23:21	Reserved	Reserved,the reset value must be maintained
20:16	M_COL_ALPHA_OP1A_INPUT_SELECT_n[4:0]	Select alpha input for op1a. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.
15	Reserved	Reserved,the reset value must be maintained
14	M_COL_RGB_OP1A_MUL2_n	Enable shift left by 1 for RGB op1a.
13:12	M_COL_RGB_OP1A_INVERT_MODE_n[1:0]	Select inversion mode for RGB op1a. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
11:10	M_COL_RED_OP1A_ARGB_SELECT	Select A, R, G or B for op1a (red path).

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Bit field	Name	Description
	_n[1:0]	0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
9:8	M_COL_GREEN_OP1A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1a (green path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
7:6	M_COL_BLUE_OP1A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1a (blue path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
5	Reserved	Reserved,the reset value must be maintained
4:0	M_COL_RGB_OP1A_INPUT_SELECT_n[4:0]	Select RGB input for op1a. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6.

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Bit field	Name	Description
		26: Select texel color value from texture unit 7.

45.5.8.2 COL ARGB Op1b Register (COL_ARGB_OP1B_n, n=0～2)

The register is read-write.

Offset Address 0x04+n*0x18

Reset Value 0x0000 06C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_COL_ALPHA_CARRY1_n	M_COL_ALPHA_OP1B_MUL2_n	M_COL_ALPHA_OP1B_INVERT_MODE_n[1:0]		Reserved		M_COL_ALPHA_OP1B_ARGB_SELECT_n[1:0]		Reserved			M_COL_ALPHA_OP1B_INPUT_SELECT_n[4:0]				
rw	rw	rw				rw					rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_COL_RGB_CARRY1_n	M_COL_RGB_OP1B_MUL2_n	M_COL_RGB_OP1B_INVERT_MODE_n		M_COL_RED_OP1B_ARGB_SELECT_n[1:0]		M_COL_GREEN_OP1B_ARGB_SELECT_n[1:0]		M_COL_BLUE_OP1B_ARGB_SELECT_n[1:0]		Reserved	M_COL_RGB_OP1B_INPUT_SELECT_n[4:0]				
rw	rw	rw		rw		rw		rw			rw				

Bit field	Name	Description
31	M_COL_ALPHA_CARRY1_n	Enable carry in for first adder in color unit for alpha.
30	M_COL_ALPHA_OP1B_MUL2_n	Enable shift left by 1 for alpha op1b.
29:28	M_COL_ALPHA_OP1B_INVERT_MODE_n[1:0]	Select inversion mode for alpha op1b. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
27:26	Reserved	Reserved,the reset value must be maintained
25:24	M_COL_ALPHA_OP1B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1b (alpha path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
23:21	Reserved	Reserved,the reset value must be maintained
20:16	M_COL_ALPHA_OP1B_INPUT_SELECT_n[4:0]	Select alpha input for op1b. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4.

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Bit field	Name	Description
		8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.
15	M_COL_RGB_CARRY1_n	Enable carry in for first adder in color unit for RGB.
14	M_COL_RGB_OP1B_MUL2_n	Enable shift left by 1 for RGB op1b.
13:12	M_COL_RGB_OP1B_INVERT_MODE_n[1:0]	Select inversion mode for RGB op1b. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
11:10	M_COL_RED_OP1B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1b (red path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
9:8	M_COL_GREEN_OP1B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1b (green path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
7:6	M_COL_BLUE_OP1B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op1b (blue path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
5	Reserved	Reserved,the reset value must be maintained

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4:0	M_COL_RGB_OP1B_INPUT_SELECT_n[4:0]	Select RGB input for op1b. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.

45.5.8.3 COL ARGB Op2a Register (COL_ARGB_OP2A_n, n=0～2)

The register is read-write.

Offset Address 0x08+n*0x18

Reset Value 0x0000 06C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	M_COL_ALPHA_OP2A_MUL2_n	M_COL_ALPHA_OP2A_INVERT_MODE_n[1:0]		Reserved		M_COL_ALPHA_OP2A_ARGB_SELECT_n[1:0]		Reserved			M_COL_ALPHA_OP2A_INPUT_SELECT_n[4:0]				
	rw	rw				rw					rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	M_COL_RGB_OP2A_MUL2_n	M_COL_RGB_OP2A_INVERT_MODE_n[1:0]		M_COL_RED_OP2A_ARGB_SELECT_n[1:0]		M_COL_GREEN_OP2A_ARGB_SELECT_n[1:0]		M_COL_BLUE_OP2A_ARGB_SELECT_n[1:0]		Reserved	M_COL_RGB_OP2A_INPUT_SELECT_n[4:0]				

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rw rw rw rw rw rw

Bit field	Name	Description
31	Reserved	Reserved,the reset value must be maintained
30	M_COL_ALPHA_OP2A_MUL2_n	Enable shift left by 1 for alpha op2a.
29:28	M_COL_ALPHA_OP2A_INVERT_MODE_n[1:0]	Select inversion mode for alpha op2a. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
27:26	Reserved	Reserved,the reset value must be maintained
25:24	M_COL_ALPHA_OP2A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2a (alpha path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
23:21	Reserved	Reserved,the reset value must be maintained
20:16	M_COL_ALPHA_OP2A_INPUT_SELECT_n[4:0]	Select alpha input for op2a. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4.

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Bit field	Name	Description
		24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.
15	Reserved	Reserved,the reset value must be maintained
14	M_COL_RGB_OP2A_MUL2_n	Enable shift left by 1 for RGB op2a.
13:12	M_COL_RGB_OP2A_INVERT_MODE_n[1:0]	Select inversion mode for RGB op2a. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
11:10	M_COL_RED_OP2A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2a (red path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
9:8	M_COL_GREEN_OP2A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2a (green path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
7:6	M_COL_BLUE_OP2A_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2a (blue path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
5	Reserved	Reserved,the reset value must be maintained
4:0	M_COL_RGB_OP2A_INPUT_SELECT_n[4:0]	Select RGB input for op2a. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11.

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Bit field	Name	Description
		15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.

45.5.8.4 COL ARGB Op2b Register (COL_ARGB_OP2B_n, n=0～2)

The register is read-write.

Offset Address 0x0C+n*0x18

Reset Value 0x0000 06C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_COL_ALPHA_CARRY2_n	M_COL_ALPHA_OP2B_MUL2_n	M_COL_ALPHA_OP2B_INVERT_MODE_n[1:0]		Reserved		M_COL_ALPHA_OP2B_ARGB_SELECT_n[1:0]		Reserved			M_COL_ALPHA_OP2B_INPUT_SELECT_n[4:0]				
rw	rw	rw				rw					rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_COL_RGB_CARRY2_n	M_COL_RGB_OP2B_MUL2_n	M_COL_RGB_OP2B_INVERT_MODE_n[1:0]		M_COL_RED_OP2B_ARGB_SELECT_n[1:0]		M_COL_GREEN_OP2B_ARGB_SELECT_n[1:0]		M_COL_BLUE_OP2B_ARGB_SELECT_n[1:0]		Reserved	M_COL_RGB_OP2B_INPUT_SELECT_n[4:0]				
rw	rw	rw		rw		rw		rw			rw				

Bit field	Name	Description
31	M_COL_ALPHA_CARRY2_n	Enable carry in for second adder in color unit for alpha.
30	M_COL_ALPHA_OP2B_MUL2_n	Enable shift left by 1 for alpha op2b.
29:28	M_COL_ALPHA_OP2B_INVERT_MODE_n[1:0]	Select inversion mode for alpha op2b. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
27:26	Reserved	Reserved,the reset value must be maintained
25:24	M_COL_ALPHA_OP2B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2b (alpha path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input.

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Bit field	Name	Description
		3: Use B from the selected input.
23:21	Reserved	Reserved,the reset value must be maintained
20:16	M_COL_ALPHA_OP2B_INPUT_SELECT_n[4:0]	Select alpha input for op2b. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.
15	M_COL_RGB_CARRY2_n	Enable carry in for second adder in color unit for RGB.
14	M_COL_RGB_OP2B_MUL2_n	Enable shift left by 1 for RGB op2b.
13:12	M_COL_RGB_OP2B_INVERT_MODE_n[1:0]	Select inversion mode for RGB op2b. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
11:10	M_COL_RED_OP2B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2b (red path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.

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Bit field	Name	Description
9:8	M_COL_GREEN_OP2B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2b (green path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
7:6	M_COL_BLUE_OP2B_ARGB_SELECT_n[1:0]	Select A, R, G or B for op2b (blue path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
5	Reserved	Reserved,the reset value must be maintained
4:0	M_COL_RGB_OP2B_INPUT_SELECT_n[4:0]	Select RGB input for op2b. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.

45.5.8.5 COL ARGB Op3 Register (COL_ARGB_OP3_n, n=0～2)

The register is read-write.

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Offset Address 0x10+n*0x18

Reset Value 0x0003 06C3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	M_COL_ALPHA_OP3_MUL2_n	M_COL_ALPHA_OP3_INVERT_MODE_n[1:0]		Reserved		M_COL_ALPHA_OP3_ARGB_SELECT_n[1:0]		Reserved			M_COL_ALPHA_OP3_INPUT_SELECT_n[4:0]				
	rw	rw				rw					rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	M_COL_RGB_OP3_MUL2_n	M_COL_RGB_OP3_INVERT_MODE_n[1:0]		M_COL_RED_OP3_ARGB_SELECT_n[1:0]		M_COL_GREEN_OP3_ARGB_SELECT_n[1:0]		M_COL_BLUE_OP3_ARGB_SELECT_n[1:0]		Reserved	M_COL_RGB_OP3_INPUT_SELECT_n[4:0]				
	rw	rw		rw		rw		rw			rw				

Bit field	Name	Description
31	Reserved	Reserved,the reset value must be maintained
30	M_COL_ALPHA_OP3_MUL2_n	Enable shift left by 1 for alpha op3.
29:28	M_COL_ALPHA_OP3_INVERT_MODE_n[1:0]	Select inversion mode for alpha op3. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
27:26	Reserved	Reserved,the reset value must be maintained
25:24	M_COL_ALPHA_OP3_ARGB_SELECT_n[1:0]	Select A, R, G or B for op3 (alpha path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
23:21	Reserved	Reserved,the reset value must be maintained
20:16	M_COL_ALPHA_OP3_INPUT_SELECT_n[4:0]	Select alpha input for op3. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1. 5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10.

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Bit field	Name	Description
		14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.
15	Reserved	Reserved,the reset value must be maintained
14	M_COL_RGB_OP3_MUL2_n	Enable shift left by 1 for RGB op3.
13:12	M_COL_RGB_OP3_INVERT_MODE_n[1:0]	Select inversion mode for RGB op3. 0: No inversion. 1: Invert all 9 bits. 2: Invert the 8 LSBs (all but the MSB bit 8). 3: Invert bit 7 and sign extend to bit 8 (unsigned 8 bit value-128).
11:10	M_COL_RED_OP3_ARGB_SELECT_n[1:0]	Select A, R, G or B for op3 (red path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
9:8	M_COL_GREEN_OP3_ARGB_SELECT_n[1:0]	Select A, R, G or B for op3 (green path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
7:6	M_COL_BLUE_OP3_ARGB_SELECT_n[1:0]	Select A, R, G or B for op3 (blue path). 0: Use A from the selected input. 1: Use R from the selected input. 2: Use G from the selected input. 3: Use B from the selected input.
5	Reserved	Reserved,the reset value must be maintained
4:0	M_COL_RGB_OP3_INPUT_SELECT_n[4:0]	Select RGB input for op3. 0: Select constant value 0x00. 1: Select coverage_alpha. 2: Select previous result. 3: Select constant color 0. 4: Select constant color 1.

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Bit field	Name	Description
		5: Select constant color 2. 6: Select constant color 3. 7: Select constant color 4. 8: Select constant color 5. 9: Select constant color 6. 10: Select constant color 7. 11: Select constant color 8. 12: Select constant color 9. 13: Select constant color 10. 14: Select constant color 11. 15: Select constant color 12. 16: Select constant color 13. 17: Select constant color 14. 18: Select constant color 15. 19: Select texel color value from texture unit 0. 20: Select texel color value from texture unit 1. 21: Select texel color value from texture unit 2. 22: Select texel color value from texture unit 3. 23: Select texel color value from texture unit 4. 24: Select texel color value from texture unit 5. 25: Select texel color value from texture unit 6. 26: Select texel color value from texture unit 7.

45.5.8.6 COL ARGB Out Register (COL_ARGB_OUT_n, n=0～2)

The register is read-write.

Offset Address 0x14+n*0x18

Reset Value 0x1001 1001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			M_COL_ALPHA_CLAMP_OUT_n	Reserved										M_COL_ALPHA_SCALE_OUT_n[1:0]	
			rw											rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M_COL_RGB_CLAMP_OUT_n	Reserved										M_COL_RGB_SCALE_OUT_n[1:0]	
			rw											rw	

Bit field	Name	Description
31:29	Reserved	Reserved,the reset value must be maintained
28	M_COL_ALPHA_CLAMP_OUT_n	Enable clamping of alpha output value to range. 0~255(-256~255 otherwise)

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Bit field	Name	Description
27:18	Reserved	Reserved,the reset value must be maintained
17:16	M_COL_ALPHA_SCALE_OUT_n[1:0]	Select scale mode for alpha output value. 0: Shift right 1 (/2) 1: No shift (*1) 2: Shift left 1 (*2) 3: Shift left 2 (*4)
15:13	Reserved	Reserved,the reset value must be maintained
12	M_COL_RGB_CLAMP_OUT_n	Enable clamping of RGB output value to range. 0~255(-256~255 otherwise)
11:2	Reserved	Reserved,the reset value must be maintained
1:0	M_COL_RGB_SCALE_OUT_n[1:0]	Select scale mode for RGB output value. 0: Shift right 1 (/2) 1: No shift (*1) 2: Shift left 1 (*2) 3: Shift left 2 (*4)

45.5.9 Blend Unit (BLU) Register

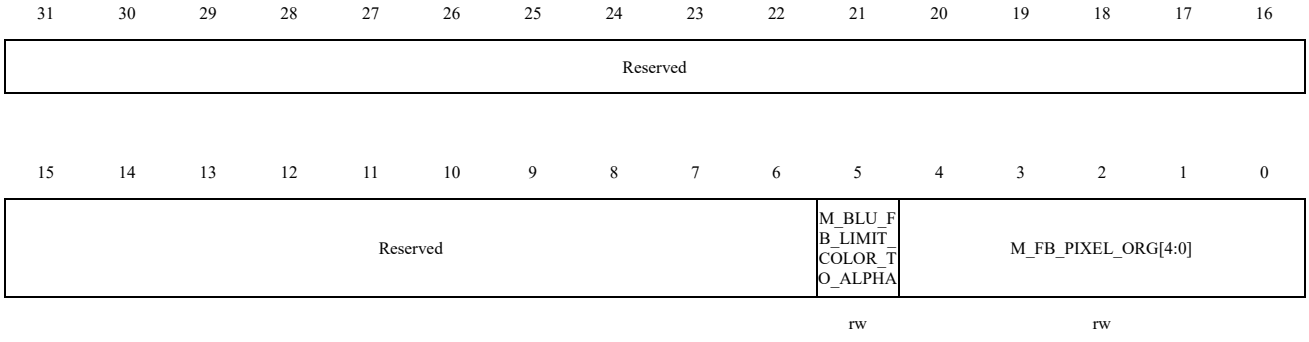
Base Address 0x5004 0C00

45.5.9.1 Frame Buffer Pixel Organization Register (FB_PIXEL_ORG)

The register is read-write.

Offset Address 0x00

Reset Value 0x0000 0000



Bit field	Name	Description
31:6	Reserved	Reserved,the reset value must be maintained
5	M_BLU_FB_LIMIT_COLOR_TO_ALPHA	Limit color values of R G and B channels to the alpha channel value after frame buffer read when enabled (for pre-multiplied formats).
4:0	M_FB_PIXEL_ORG[4:0]	Framebuffer pixel organization/format. 0 ARGB_8888,4 channels 32bits 1: RGBA_8888,4 channels 32bits 2: ARGB_4444,4 channels 16bits

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Bit field	Name	Description
		3: RGBA_4444,4 channels 16bits 4: ARGB_1555,4 channels 16bits 5: RGBA_5551,4 channels 16bits 6: RGB_565,3 channels 16bits 7: AL_88,2 channels 16bits 8: AL_44,2 channels 8bits 9: A_8,1 channel 8bits 10: L_8,1 channel 8bits 11: AL_17,2 channels 8bits 12: ARGB_2222,4 channels 8bits 13: RGBA_2222,4 channels 8bits 14: RGB_888,3 channels 24bits 15: BGR_888,3 channels 24bits 16: ARGB_8565,4 channels 24bits 17: RGBA_8565,4 channels 24bits

45.5.9.2 FBC Start Address Register (FBC_START_ADDRESS)

The register is read-write.

Offset Address 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_FBC_START_ADDRESS[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_FBC_START_ADDRESS[15:0]															
rw															

Bit field	Name	Description
31:0	M_FBC_START_ADDRESS[31:0]	Framebuffer start address. Must be aligned to MBI bus width.

45.5.9.3 BLU Blend Register (BLU_BLEND)

The register is read-write.

Offset Address 0x08

Reset Value 0x0122 0D22

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_BLU_FB_POSTDIVIDE_ENABLE	M_BLU_FB_PREMULTIPLY_ENABLE	Reserved	M_BLU_ALPHA_BLEND_MODE	Reserved		M_BLU_ALPHA_DST_BLEND_FACTOR_INVERT	M_BLU_ALPHA_SRC_BLEND_FACTOR_INVERT	Reserved		M_BLU_ALPHA_DST_BLEND_FACTOR_SELECT[1:0]		Reserved		M_BLU_ALPHA_SRC_BLEND_FACTOR_SELECT[1:0]	

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rw	rw		rw			rw	rw			rw					rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	M_BLU_COLOR_BLEND_MODE[2:0]			M_BLU_COLOR_DST_BLEND_FACTOR_USE_ALPHA	M_BLU_COLOR_SRC_BLEND_FACTOR_USE_ALPHA	M_BLU_COLOR_DST_BLEND_FACTOR_INVERT	M_BLU_COLOR_SRC_BLEND_FACTOR_INVERT	Reserved		M_BLU_COLOR_DST_BLEND_FACTOR_SELECT[1:0]		Reserved		M_BLU_COLOR_SRC_BLEND_FACTOR_SELECT[1:0]	
		rw		rw	rw	rw	rw			rw				rw	

Bit field	Name	Description
31	M_BLU_FB_POSTDIVIDE_ENABLE	Divide color channels by alpha channel after blending (before coverage blending) when enabled.
30	M_BLU_FB_PREMULTIPLY_ENABLE	Multiply destination colors by destination alpha before blending when enabled.
29	Reserved	Reserved,the reset value must be maintained
28	M_BLU_ALPHA_BLEND_MODE	Alpha channel blending blend mode. 0: normal blending，out=src*f_src+dst*f_dst 1: Multiply add，add 2nd factor only，out=src*f_src+ f_dst
27:26	Reserved	Reserved,the reset value must be maintained
25	M_BLU_ALPHA_DST_BLEND_FACTOR_INVERT	Destination blend factor inversion for alpha channel blending.
24	M_BLU_ALPHA_SRC_BLEND_FACTOR_INVERT	Source blend factor inversion for alpha channel blending.
23:22	Reserved	Reserved,the reset value must be maintained
21:20	M_BLU_ALPHA_DST_BLEND_FACTOR_SELECT[1:0]	Destination blend factor for alpha channel blending. 0: Use source alpha and color respectively. 1: Use destination alpha and color respectively. 2: Use 0.0
19:18	Reserved	Reserved,the reset value must be maintained
17:16	M_BLU_ALPHA_SRC_BLEND_FACTOR_SELECT[1:0]	Source blend factor for alpha channel blending. 0: Use source alpha and color respectively. 1: Use destination alpha and color respectively. 2: Use 0.0
15	Reserved	Reserved,the reset value must be maintained
14:12	M_BLU_COLOR_BLEND_MODE[2:0]	Color channel blending blend mode. 0: normal blending，out=src*f_src+dst*f_dst 1: Multiply add，add 2nd factor only， out=src*(f_src+dst)+ dst*f_dst 2: OVG darken，out=min(src+dst*f_dst+ src*f_src) 3: OVG lighten，out=max(src+dst*f_dst+ src*f_src)
11	M_BLU_COLOR_DST_BLEND_FACTOR_USE_ALPHA	Destination blend factor A / RGB selection for color channel blending.
10	M_BLU_COLOR_SRC_BLEND_FACT	Source blend factor A / RGB selection for color channel blending.

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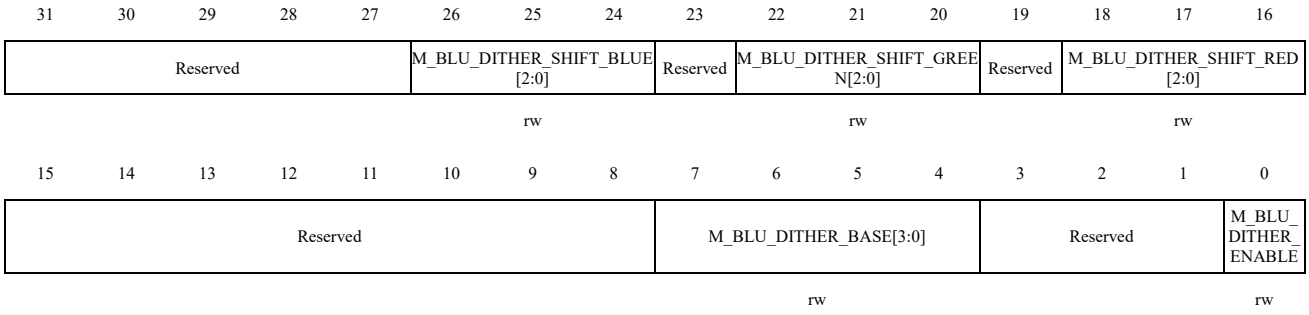
Bit field	Name	Description
	OR_USE_ALPHA	
9	M_BLU_COLOR_DST_BLEND_FACTOR_INVERT	Destination blend factor inversion for color channel blending.
8	M_BLU_COLOR_SRC_BLEND_FACTOR_INVERT	Source blend factor inversion for color channel blending.
7:6	Reserved	Reserved,the reset value must be maintained
5:4	M_BLU_COLOR_DST_BLEND_FACTOR_SELECT[1:0]	Destination blend factor for color channel blending. 0: Use source alpha and color respectively. 1: Use destination alpha and color respectively. 2: Use 0.0
3:2	Reserved	Reserved,the reset value must be maintained
1:0	M_BLU_COLOR_SRC_BLEND_FACTOR_SELECT[1:0]	Source blend factor for color channel blending. 0: Use source alpha and color respectively. 1: Use destination alpha and color respectively. 2: Use 0.0

45.5.9.4 BLU Dither Register (BLU_DITHER)

The register is read-write.

Offset Address 0x0C

Reset Value 0x0000 0000



Bit field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained
26:24	M_BLU_DITHER_SHIFT_BLUE[2:0]	Number of remaining framebuffer bits for the blue channel.
23	Reserved	Reserved,the reset value must be maintained
22:20	M_BLU_DITHER_SHIFT_GREEN [2:0]	Number of remaining framebuffer bits for the green channel.
19	Reserved	Reserved,the reset value must be maintained
18:16	M_BLU_DITHER_SHIFT_RED[2:0]	Number of remaining framebuffer bits for the red channel.
15:8	Reserved	Reserved,the reset value must be maintained
7:4	M_BLU_DITHER_BASE[3:0]	X/Y shift of the dither matrix relative to the dither offset of the pixel.
3:1	Reserved	Reserved,the reset value must be maintained

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Bit field	Name	Description
0	M_BLU_DITHER_ENABLE	Enable dithering after blending.

45.5.9.5 BLU Write Control Register (BLU_WRITE)

The register is read-write.

Offset Address 0x10

Reset Value 0x0001 000F

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														M_BLU_COVERAGE_DEBUG_ENABLE	M_BLU_COVERAGE_BLENDING_ENABLE
														rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												M_BLU_WRITE_ALPHA	M_BLU_WRITE_RED	M_BLU_WRITE_GREEN	M_BLU_WRITE_BLUE
												rw	rw	rw	rw

Bit field	Name	Description
31:18	Reserved	Reserved,the reset value must be maintained
17	M_BLU_COVERAGE_DEBUG_ENABLE	Enable coverage debug mode.
16	M_BLU_COVERAGE_BLENDING_ENABLE	Enable coverage blending.
15:4	Reserved	Reserved,the reset value must be maintained
3	M_BLU_WRITE_ALPHA	Enable writing of the alpha channel.
2	M_BLU_WRITE_RED	Enable writing of the red channel.
1	M_BLU_WRITE_GREEN	Enable writing of the green channel.
0	M_BLU_WRITE_BLUE	Enable writing of the blue channel.

45.5.10 Performance Counters (PFC) Register

Base Address 0x5004 0E00

45.5.10.1 PFC Enable Register (PFC_ENABLE)

The register is read-write.

Offset Address 0x00

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	M_PFC_ENABLE_3	M_PFC_ENABLE_2	M_PFC_ENABLE_1	M_PFC_ENABLE_0
	rw	rw	rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3	M_PFC_ENABLE_3	Enable performance counter 3
2	M_PFC_ENABLE_2	Enable performance counter 2
1	M_PFC_ENABLE_1	Enable performance counter 1
0	M_PFC_ENABLE_0	Enable performance counter 0

45.5.10.2 PFC Clear Register (PFC_CLEAR)

The register is read-write.

Offset Address 0x04

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												M_PFC_CLEAR_3	M_PFC_CLEAR_2	M_PFC_CLEAR_1	M_PFC_CLEAR_0
												rw	rw	rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained
3	M_PFC_CLEAR_3	Clear performance counter 3
2	M_PFC_CLEAR_2	Clear performance counter 2
1	M_PFC_CLEAR_1	Clear performance counter 1
0	M_PFC_CLEAR_0	Clear performance counter 0

45.5.10.3 PFC Event Select Register (PFC_EVENT_SELECT_n, n=0～3)

The register is read-write.

Offset Address 0x08+n*4

Reset Value 0x0000 003B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	M_PFC_EVENT_SELECT_n[6:0]
	rw

Bit field	Name	Description
31:7	Reserved	Reserved,the reset value must be maintained
6:0	M_PFC_EVENT_SELECT_n[6:0]	Performance counters event select. 0: Stream reader start of fetch event. 1: Stream reader did a burst read on MBI. 2: Stream reader received a word from MBI (1 event for every word in a burst). 3: Stream writer did a burst write on MBI. 4: Stream writer did a word write on MBI (1 event for every word in a burst). 5: Clear unit did a burst write on MBI. 6: Clear unit did a word write on MBI (1 event for every word in a burst). 7: New primitive enumerated. 8: New stripe enumerated. 9: Visible pixel enumerated: A visible pixel may nevertheless have an 8-bit coverage value of 0 due to rounding. Potential Bezier post-process is not considered. 10: Invisible pixel enumerated: Potential Bezier post-process is not considered. 11: ZSA buffer span split due to span length limit reached. 12: ZSA buffer cache did a burst read on MBI. 13: ZSA buffer cache did a burst write on MBI. 14: ZSA buffer cache received a word from MBI (1 event for every word in a burst). 15: ZSA buffer cache did a word write on MBI (1 event for every word in a burst). 16: ZSA buffer cache processed a pixel read. 17: ZSA buffer cache processed a read without any wait cycle. 18: ZSA buffer cache wait cycles on read side (>= 1 event per miss). 19: ZSA buffer cache processed a pixel write. 20: ZSA buffer span conflict occured between new job requiring a read and a line already in the ZSA cache: Read range of new job overlaps write range of open line. 21: Wait cycles at ZSA buffer prefetch queue interface due to span conflict. 22: Wait cycles at ZSA buffer prefetch queue interface because line could not be allocated as there is no unused line available. 23: Pixel failed depth test. 24: Pixel failed stencil test. 25: Pixel dropped through alpha test. 26: Span split due to span length limit reached. 27: Span split due to read gap limit reached.

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Bit field	Name	Description
		28: Framebuffer cache did a burst read on MBI. 29: Framebuffer cache did a burst write on MBI. 30: Framebuffer cache received a word from MBI (1 event for every word in a burst). 31: Framebuffer cache did a word write on MBI (1 event for every word in a burst). 32: Framebuffer cache processed a pixel read. 33: Framebuffer cache processed a read without any wait cycle. 34: Framebuffer cache wait cycles on read side (>= 1 event per miss). 35: Framebuffer cache processed a pixel write. 36: Span conflict occured between new job requiring a read and a line already in the framebuffer cache: Read range of new job overlaps write range of open line. 37: Wait cycles at prefetch queue interface due to span conflict. 38: Wait cycles at prefetch queue interface because line could not be allocated as there is no unused line available. 39: Cache miss in the prefetching texture cache scheduler. 40: Line refresh job sent from texel schedule to texture cache. 41: Texture cache did a burst read on MBI. 42: Texture cache received a word from MBI (1 event for every word in a burst). 43: Texture cache processed a pixel read (i.e. potentially multiple texel reads. 44: Texture cache processed a pixel read without the need to wait for a fetch. 45: Wait cycles at pipeline read interface because of wait for line to be fetched. 46: Wait cycles inserted in pipeline read path because read RAM needed to be accessed more than once and prefetch was not successful. 47: A job was taken from the prefetch queue without the need to wait for the access count to reach the replace count. 48: Wait cycles at prefetch queue interface because job could not be fetched as the access count had not yet reached the replace count. 49: RLD did a burst read on MBI. 50: RLD did a word read on MBI (1 event for every word in a burst). 51: RLD rewinds to start of texture code. 52: Wait cycles when accessing CLUT: Count every additional cycle of CLUT access which exceeds the optimal throughput of 1 cycle/pixel. 53: Finished execution of a stream command. 54: Wait cycles when STC waits for data from STR. 55: Wait cycles when STC waits for register write acknowledge from register file. 56: Wait cycles when STC waits because of wait command. 57: Active cycles of the STC while not in pause-reached mode. 58: Active cycles of the STC-Core only when the ACG would be enabled. 59: Busy cycles of STC.

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Bit field	Name	Description
		60: Busy cycles of STR. 61: Busy cycles of STW. 62: Busy cycles of REG. 63: Busy cycles of PSU. 64: Busy cycles of modules after PSU. 65: Busy cycles of modules after ZSS. 66: Busy cycles of modules after TXS. 67: Busy cycles of modules after FBS. 68: Busy cycles of clear unit. 69: Every clock cycle.

45.5.11 Clear Unit (CLR) Register

Base Address 0x5004 0F00

45.5.11.1 CLR Clear Unit Color Value Register (CLR_VALUE)

The register is read-write.

Offset Address 0x00

Reset Value 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_CLR_VALUE[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_CLR_VALUE[15:0]															
rw															

Bit field	Name	Description
31:0	M_CLR_VALUE[31:0]	Clear unit color value.

45.5.11.2 CLR Line Config Register (CLR_LINE_CONFIG)

The register is read-write.

Offset Address 0x04

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	M_CLR_PITCH[14:0]														
	rw														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	M_CLR_LINE_LENGTH[13:0]

rw

Bit field	Name	Description
31	Reserved	Reserved,the reset value must be maintained
30:16	M_CLR_PITCH[14:0]	Clear unit pitch in bytes.
15:14	Reserved	Reserved,the reset value must be maintained
13:0	M_CLR_LINE_LENGTH[13:0]	Clear unit line length in bytes-1

45.5.11.3 CLR Control Register (CLR_CTRL)

The register is read-write.

Offset Address 0x08

Reset Value 0x003F 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										M_CLR_BPP[1:0]		M_CLR_MASK[3:0]			
rw	rw	rw								rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				M_CLR_NUM_LINES[11:0]											

rw

Bit field	Name	Description
31:22	Reserved	Reserved,the reset value must be maintained
21:20	M_CLR_BPP[1:0]	Clear unit bytes-1 per pixel.
19:16	M_CLR_MASK[3:0]	Clear unit write byte mask.
15:12	Reserved	Reserved,the reset value must be maintained
11:0	M_CLR_NUM_LINES[11:0]	Clear unit number of lines-1.

45.5.11.4 CLR Start Address Register (CLR_START_ADDRESS)

The register is read-write.

Offset Address 0x0C

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M_CLR_START_ADDRESS[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_CLR_START_ADDRESS[15:0]															

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rw

Bit field	Name	Description
31:0	M_CLR_START_ADDRESS[31:0]	Start address for clear unit.

45.5.12 Lookup Table (LUT) Entry Register

The register is read-write.

Address 0x5004 2000

Reset Value 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUT_ENTRY[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LUT_ENTRY[15:0]															
rw															

Bit field	Name	Description
31:0	LUT_ENTRY[31:0]	Lookup table entry. The CLUT logically contains different kinds of values, depending on TXP_CTRL.M_TXP_CLUT_MODE: • INDEXED_COLOR: CLUT contains color values • MAP_(A)RGB: CLUT contains mapped channels values • CONVOLUTION(_SIGNED): CLUT contains filter weights for convolution filtering Do not access while TXP unit is actively using the CLUT! Always wait for TXP unit first!

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46 Digital Video Peripheral (DVP)

46.1 Introduction

Support two DVP interfaces. DVP is a flexible and powerful CMOS optical sensor interface that can easily meet customers' image acquisition requirements, and the entire acquisition process does not require CPU intervention.

DVP is capable of receiving high-speed data from traditional or ITU-R BT.656 format CMOS image sensors, and supports their data formats: YCbCr422 and RGB565 progressive, as well as compressed data (JPEG).

46.2 Main Features

- Support 8, 10, 12, 14 and 16-bit traditional synchronous parallel interface
- Support 8-bit and 10-bit ITU-R BT.656 video format
- Support 8-bit and 16-bit data port for YCbCr, YUV and RGB data format
- Support 8, 10, 12, 14 and 16-bit data port for Bayer data format
- Support clock output (through MCO output, typical value 48MHz) to provide clock to external CMOS optical sensor
- The polarities of the input pixel clock (DVP_PCLK), field synchronization signal (DVP_VSYNC) and line synchronization signal (DVP_HSYNC) can be configured independently.
- 320x64 bytes FIFO for receiving pixel data
- Support Receive FIFO overflow protection
- Support DMA function, the entire image acquisition process does not require CPU intervention.
- Support hardware cropping
- Support multiple data formats:
  - YCbCr422 progressive video
  - RGB565 progressive video
  - Compressed data (JPEG)

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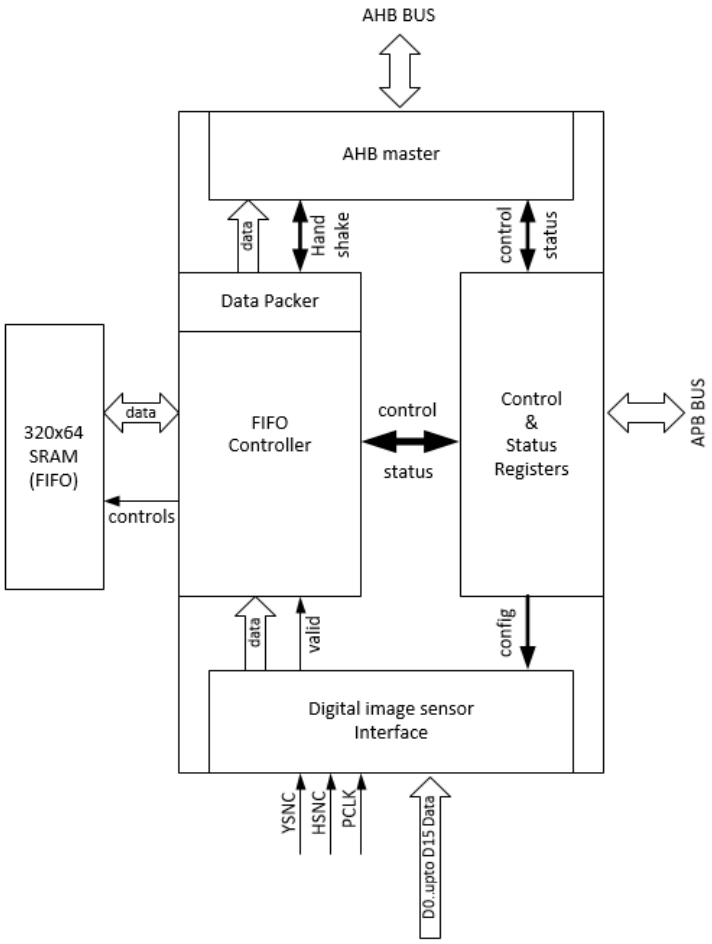
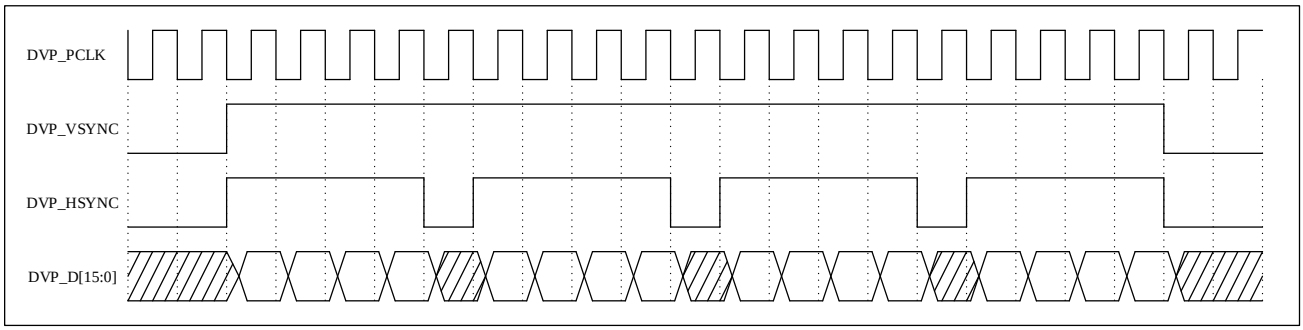
46.3 DVP Block Diagram

Figure 46-1 DVP Block Diagram



46.4 DVP timing

Figure 46-2 Example of DVP interface timing



As shown in the above figure:

- DVP_PCLK is the pixel clock, capturing 2 bytes (16 bits) of valid data per clock cycle.

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- DVP_VSYNC is the vertical synchronization (frame synchronization) signal, active high.
- DVP_HSYNC is the horizontal synchronization signal, active high.
- When both DVP_VSYNC and DVP_HSYNC are high, the captured data is valid.
- There is at least one pixel clock cycle interval between every two lines.
- According to the timing diagram above, users need to configure DVP_VSYNC and DVP_HSYNC as active high in the DVP module, and capture on the falling edge of DVP_PCLK to correctly receive data.
- DVP data is only valid when the DVP port enable bit (DVP_CTRL.DVPEN) is set to 1, and the enable bit must be set to 1 at least 4 pixel clock cycles before the DVP_VSYNC active signal (high level) to prevent the current frame from being discarded.

46.5 DVP Clock

The maximum frequence of the clock is 110Mhz.

The AHB interface clock (hclk) must be equal to or faster than the pixel clock.

46.6 DVP Function Description

46.6.1 Configuration Process

- Switch on the CMOS optical sensor clock, enable the relevant control ports (typically I2C interface), and configure the sensor parameters.
- Configure the DVP port and parameters (e.g., capture mode, DMA, etc.).
- Configure the DVP port enable bit (DVP_CTRL.DVPEN), and prepare to receive data.
- Enable the CMOS sensor to start sending data.

46.6.2 Data Transmission And Synchronization

The DVP module can receive 8-bit, 10-bit, 12-bit, 14-bit, or 16-bit parallel pixel data. The effective data position in the interface can be configured based on the DBIT[2:0] setting in the DVP_PORTCFG register, as shown in the table below.

Table 46-1 DVP interface signals

Port	DVP_DBIT[2:0]	Description
DVP_D[7:0]	000 (8 bits)	pixel data bus, all bits are used to capture data
DVP_D[9:0]	001 (10 bits)	

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DVP_D[11:0]	010 (12 bits)	
DVP_D[13:0]	011 (14 bits)	
DVP_D[15:0]	100 (16 bits)	
DVP_D[9:0]	101	pixel data bus, only [9:2] (8-bit) are used to capture data
DVP_D[11:0]	110	pixel data bus, only [11:2] (10-bit) are used to capture data
DVP_D[11:0]	111	pixel data bus, only [11:4] (8-bit) are used to capture data
DVP_VSYNC	N/A	vertical synchronization signal
DVP_HSYNC	N/A	horizontal synchronization signal
DVP_PCLK	N/A	pixel clock

The polarity of DVP_VSYNC, DVP_HSYNC, and DVP_PCLK can be configured through the DVP_PORTCFG register.

To integrate the transmitted data into an image, horizontal synchronization and vertical synchronization are required. The digital camera interface supports embedded synchronization or hardware (HSYNC and VSYNC) synchronization. When using embedded synchronization, the digital camera module ensures that the values 0x00 and 0xFF are used solely for synchronization (not in the data).

46.6.2.1 Hardware Synchronization

In hardware synchronization mode, the CMOS image camera can provide horizontal sync signals and vertical sync signals for synchronization at the receiving end. Setting DVP_PORTCFG.EMBSEN to 0 allows the DVP to receive in this synchronous mode. Each effective interval of the DVP_VSYNC signal represents a frame of data, and each effective interval of the DVP_HSYNC signal represents a line of data. The DVP_VSYNC signal is low active by default, and the DVP_HSYNC signal is high active by default. When both DVP_VSYNC and DVP_HSYNC are active, valid pixel data is captured at the rising edge of the pixel clock.

46.6.2.2 Embedded Synchronization

In embedded synchronization mode, pixel data synchronization does not depend on DVP_VSYNC and DVP_HSYNC, but rather inserts synchronization codes in the data stream. The DVP can receive in this synchronous mode. The synchronization code (0xFF0000XX) consists of 4 bytes of data, with the first 3 bytes fixed, where the first byte is all 1s, followed by all 0s for the second and third bytes. The content of the fourth byte data varies based on the synchronization information. Configuration of the HS_PTTN, HE_PTTN, VS_PTTN, and VE_PTTN registers in the DVP_EMSC register is required according to the synchronization code format and content used by the camera manufacturer. Embedded code synchronization has two modes, namely normal mode and Sony mode, with specific processes as shown in the diagram below.

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Figure 46-3 Frame format in normal mode

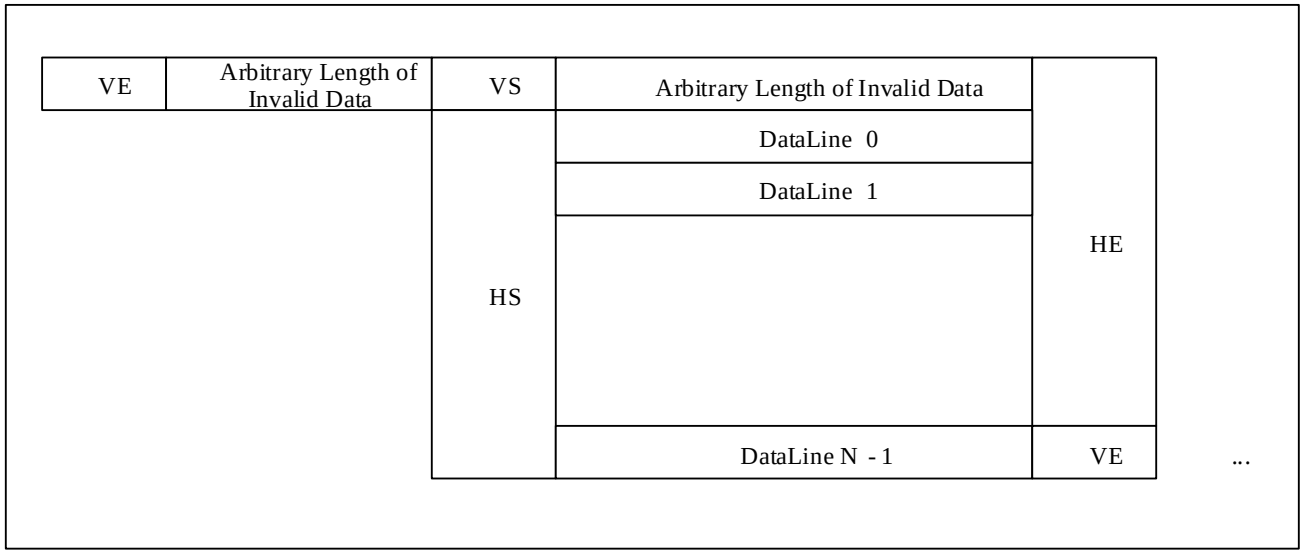
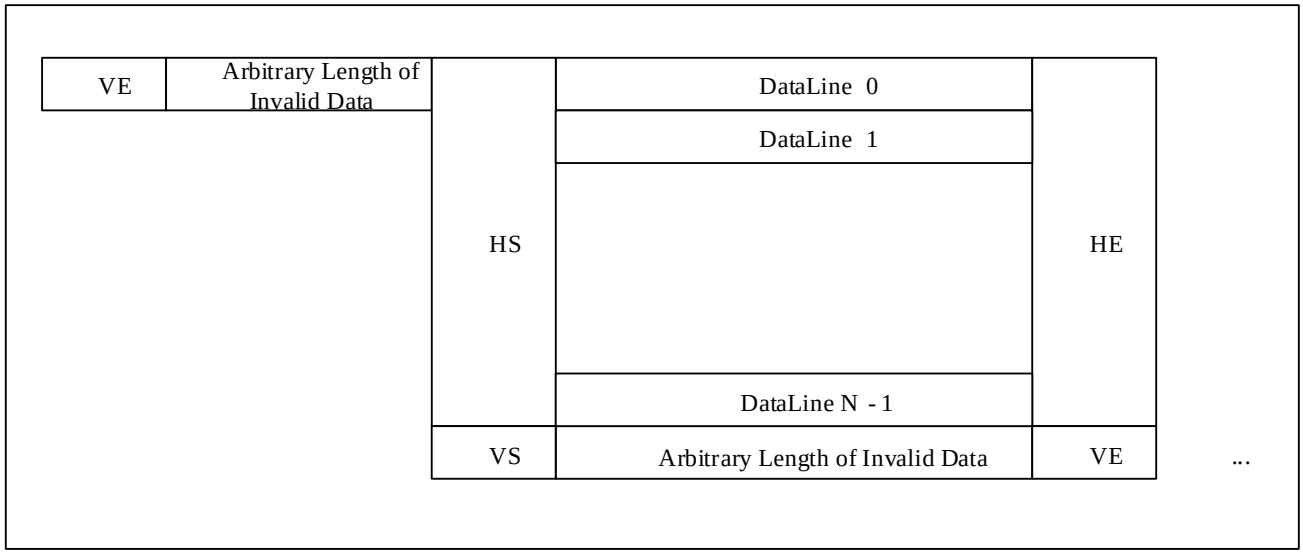


Figure 46-4 Frame format in sony mode



46.6.3 DVP capture mode

There are two capture modes:one is continuous capturing mode, and the other one is snap-shot mode.While receiving an image frame, if FIFO overflow occurs, the overflow flag of the corresponding receiving frame buffer is set, and if a frame is skipped, the frame-skipping flag will get set too.

46.6.3.1 Snap-shot mode (single frame capture)

Enable this mode by setting DVP_CTRL.CM register bit to “1”. In snap-shot mode, it depends on the number of the frame buffer getting configured. If only one frame buffer is in place, DVP will stop capturing a new frame after a frame is received. And at the same time, the hardware sets the DVP_INTSTS.M1TCF bit to "1" to indicate that the hardware has completed the current frame reception. For the DVP to start capturing a new frame again, the software

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has to clear DVP_INTSTS.M1TCF. Similarly, if two frame buffers are in place, the DVP will stop capturing frame after two frames are received, and the DVP_INTSTS.M1TCF and the DVP_INTSTS.M2TCF bits are pending for the software to clear them. The software must clear the flags in the order as they are received. Once the software clears one of the flags, the DVP starts capturing frame again.

46.6.3.2 Continuous capturing mode

In this mode, DVP will continue to capture image data and put it into frame memory regardless of whether the previous frame data is being read. It does not wait for the software to clear the completion Flag (DVP_INTSTS. MxRCF). If two frame buffers are set up, frames are received into these frame buffers in ping-pong fashion.

To enable this mode, make sure DVP_CTRL.CMregister bit to “0”.

46.6.4 DVP crop function

Set DVP_CTRL.CROPEN bit to "1" to enter the crop function. For this function, a user only needs to provide two coordinates to DVP, the start and end coordinates. The user must enter the coordinates first before setting the CROPEN bit. Each image pixel can be represented by 1 or 2 data bytes. If the image pixel needs two data bytes, then DVP_PORTCFG. PIXELDB bit has to be "1". DVP crop function is illustrated in Figure 30-5 below.

The user must enter the coordinates first before setting the CROPEN bit. Users needs to set the following registers:

Start coordinate register: DVP_CSXY.CSTAX = 'd1

Start coordinate register: DVP_CSXY.CSTAY = 'd3

End coordinate register: DVP_CEXY.CENDX = 'd10

End coordinate register: DVP_CEXY.CENDY = 'd8

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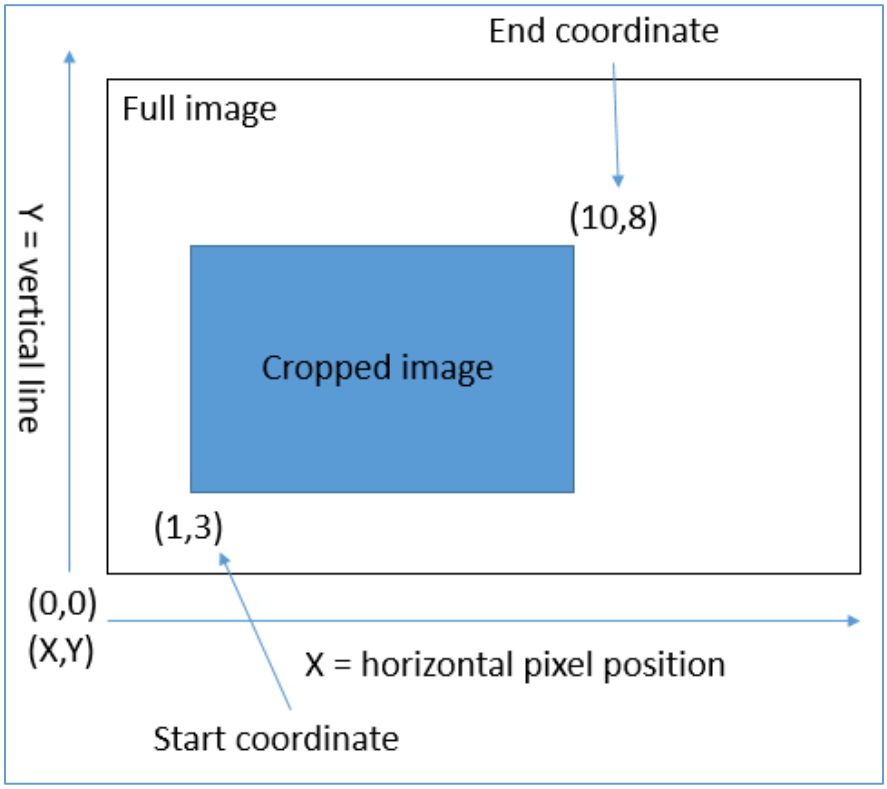
Figure 46-5 DVP crop function



46.6.5 DVP frame line skipping function

The frame line skipping function is controlled by two registers:the DVP_PORTCFG.HISKIP register controls the number of initial frame line skip. The DVP_PORTCFG.HRSKIP register controls line skip pattern.

There are two types of line skipping pattern controlled by the DVP_PORTCFG.HRSKIP register:

- capture all even or odd lines
- capture a line followed by the number of skip lines.

When these two registers are used in combination, there are two possible scenarios. For example, when configuring DVP_PORTCFG.HISKIP as 3 and DVP_PORTCFG.HRSKIP as 3, the actual situation is as shown in the diagram below.

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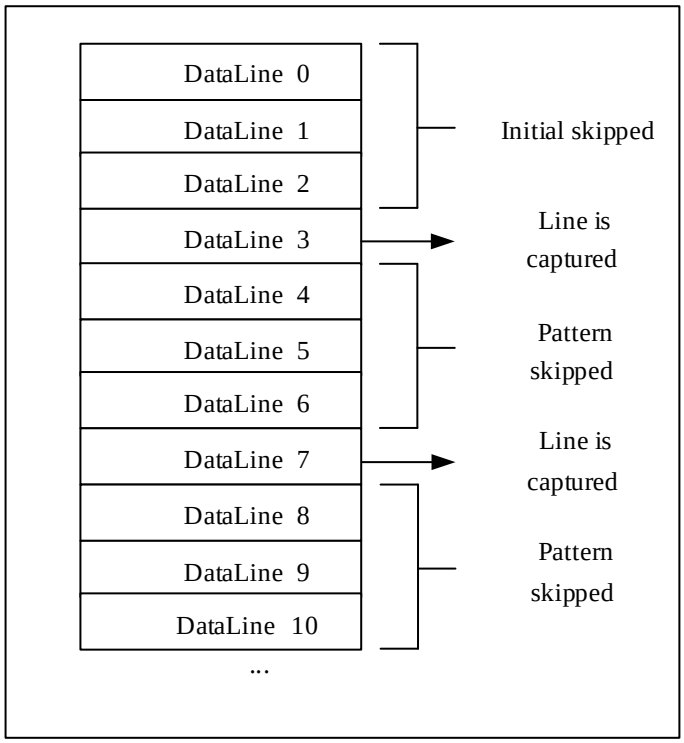
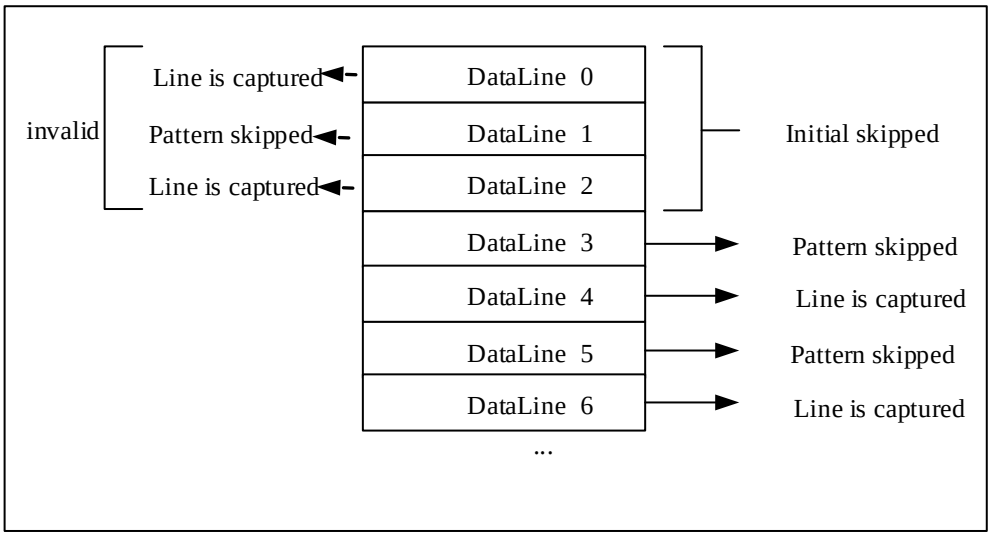
Figure 46-6 Line skip function (HISKIP=3，HRSKIP=3)



When configuring DVP_PORTCFG.HISKIP as 3 and DVP_PORTCFG.HRSKIP as 14, the actual situation is as shown in the diagram below.

Figure 46-7 Line skip function (HISKIP=3，HRSKIP=14)



46.6.6 FIFO and DMA

The DVP module has a embedded DMA, which functions to transfer data from the FIFO to the corresponding frame buffer 1/2 when the data in the FIFO reaches a threshold. The TXBURSZ in the DVP_FIFOCFG register controls the amount of data transferred in a single DMA transfer, and burst transfer is used when the configured value is greater than 0. It is important to note that the configured amount of data for a single transfer must be greater than or

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equal to the FIFO transfer threshold. The M1ADDREN/M2ADDREN in the DVP_FIFOCFG register enable the frame buffer, and in conjunction with the information in the DVP_SMADDR1, DVP_SMADDR2, and DVP_FBS registers, the DMA can determine the address for transferring each data entry.

46.6.7 Interrupt

There are two registers related to interrupts: DVP_INTSTS and DVP_INTEN:

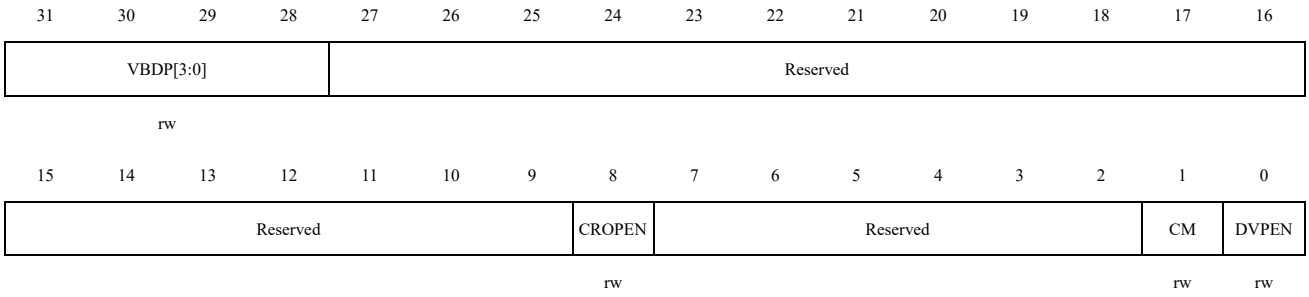
- DVP_INTEN is the interrupt enable register.
- DVP_INTSTS is the interrupt status register. Even if the interrupt is not enabled, the interrupt status will change, but the interrupt will not be reported to the system. The corresponding interrupt will only be reported when the corresponding interrupt enable bit in DVP_INTEN is enabled.
- Before the user wants to use a specific interrupt, they must first clear the corresponding flag in the DVP_INTSTS register (write 0 to clear) to avoid generating incorrect interrupts.

46.7 DVP Register

46.7.1 DVP control register (DVP_CTRL)

Address offset: 0x00

Reset value: 0x8000 0000



Bit field	Name	Description
31:28	VBFLT[3:0]	VSYNC blanking glitch filtering control. By default, it is set to 8. It means 8 consecutive sampling on VSYNC signal and all the samples are "1" which confirms the vertical blanking is detected. You can change the number of detection sampling of VSYNC to confirm the vertical blanking by programming this regiser, and it ranges from 0 to 15. Note: The software can only modify this bit when DVP_CTRL.DVPEN.
27:9	Reserved	Reserved, the reset value must be maintained
8	CROPEN	Cropping Feature Enable bit. 0: no cropping, normal mode. 1: cropping mode.

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Bit field	Name	Description
		Before enabling this function, the start and end of cropping coordinates need to be specified respectively in the register DVP_CSXY and DVP_CEXY.
7:2	Reserved	Reserved, the reset value must be maintained
1	CM	Capture Mode Control. 0: continuous capture mode. 1: single capture mode. In the continuous capture mode, and if it is configured to have two frame buffers the frames are continuously received into the two buffers in alternative manner. In this mode, the buffer does not wait for DVP_INTSTS.MxRCF(x=1,2) to be clear before it can be used to receive a new frame again. If there is a bus error occurred on one of the buffers the other buffer will continue to receive all the new frames until the error is removed then they resume to receive the frames alternatively. In the single capture mode, it is recommended to use single frame buffer. Single frame buffer enabled (M1): when the frame buffer is completed with a frame, i.e. DVP_INTSTS.M1TCF is set, it waits for DVP_INTSTS.M1TCF to be clear before it starts to capture a new frame again. Two frame buffers are enabled (M1 and M2): When the current frame buffer finishes transferring a frame and the DVP_INTSTS.MxRCF (x=1,2) of the other buffer is not set, the next frame will be transferred to the other buffer and the DVP_INTSTS.MxRCF (x=1,2) of that buffer will be set. If both DVP_INTSTS.MxRCF (x=1,2) flags are set to 1, the system will wait until one of the flags is cleared.
0	DVPEN	DVP_ENB DVP port enable bit. Write "1" to this bit which enables DVP function. Note: This is a Write-1-Only bit; writing "0" to this bit has no effect. Refer to the register, DVP_INTSTS.DVPDIS bit for disabling this function.

46.7.2 DVP interrupt enable register (DVP_INTEN)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												FMSIE	SERRIE	CERRIE	SKIPIE
												rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							FBOIE	AHBERRIE	Reserved	FOIE	Reserved	M2TCIE	M1TCIE	M2SIE	M1SIE
							rw	rw		rw		rw	rw	rw	rw

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Bit field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained
19	FMSIE	Start of Frame detection interrupt Enable bit. 1: send an interrupt when start of frame (Vsync or equivalent vsync in embedded mode) is detected at the DVP port. 0: don't send an interrupt when start of frame is detected at the DVP port.
18	SERRIE	SYNC Code error sequence detected interrupt enable bit. 1: send an interrupt when a SYNC Code error sequence is detected. 0: don't send an interrupt when a SYNC Code error sequence is detected. Note: this is only applied to embedded synchronization mode.
17	CERRIE	SYNC Code mismatch detected interrupt enable bit. 1: send an interrupt when a SYNC Code mismatch is detected. 0: don't send an interrupt when a SYNC Code mismatch is detected. Note: This is only applied to embedded synchronization mode.
16	SKIPIE	Frame skipping interrupt enable bit. 1: send an interrupt when a frame skipping is detected. 0: don't send an interrupt when a frame skipping is detected. This occurs when the data FIFO is over flow or no more available frame buffer to receive a new frame. At this time, a new frame will be dropped and a frame skip flag will be set.
15:9	Reserved	Reserved, the reset value must be maintained
8	MOIE	Frame Buffer Over Flow interrupt enable bit. 1: send an interrupt when frame buffer overflow event occurred. 0: don't send an interrupt when frame buffer overflow event occurred.
7	AHBERRIE	AHB bus error response interrupt enable bit. 1: send an interrupt when the AHB master receives an error response while sending data to frame memory. 0: don't send an interrupt when the above situation is occurred.
6	Reserved	Reserved, the reset value must be maintained
5	FOIE	Data FIFO Over Flow interrupt enable it. 1: send an interrupt when data FIFO overflow occurs. 0: don't send an interrupt when data FIFO overflow occurs.
4	Reserved	Reserved, the reset value must be maintained
3	M2TCIE	Image data to frame buffer 2 transfer complete interrupt enable bit. 1: send an interrupt when data to frame buffer 2 is completed. 0: no interrupt is sent when data to frame buffer 2 is completed.
2	M1TCIE	Image data to Frame Buffer 1 transfer complete interrupt enable bit. 1: send an interrupt when data to frame buffer 1 is completed. 0: no interrupt is sent when data to frame buffer 1 is completed.
1	M2SIE	Frame Buffer 2 is started to receive image data interrupt enable bit. 1: send an interrupt when frame buffer 2 is starting to receive data

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Bit field	Name	Description
		0: don't send an interrupt when frame buffer 2 is starting to receive data
0	M1SIE	Frame Buffer 1 is started to receive image data interrupt enable bit. 1: send an interrupt when frame buffer 1 is starting to receive data 0: don't send an interrupt when frame buffer 1 is starting to receive data

46.7.3 DVP interrupt flag and status register (DVP_INTSTS)

Address offset: 0x08

Reset value: 0x0100 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CROPENS	CMS						DVPDIS	Reserved				FMSF	SERRF	CERRF	SKIPF
r	r						rs					rc_w1	rc_w1	rc_w1	rc_w1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						M2OF	M1OF	AHB ERR2F	AHB ERR1F	M2FOF	M1FOF	M2TCF	M1TCF	M2SF	M1SF
						rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit field	Name	Description
31	CROPENS	This is the DVP_CTRL.CROPEN shadow bit. It is read only. This bit is conveniently placed here for the software to access while it is accessing to other status bits. It will save the software to read the configuration register separately again.
30	CMS	This is the DVP_CTRL.CM shadow bit. It is read only. This bit is conveniently placed here for the software to access while it is accessing to other status bits. It will save the software to read the configuration register separately again.
29:25	Reserved	Reserved, the reset value must be maintained.
24	DVPDIS	This is DVP port disable bit. Write "1" to this bit it disables DVP port. Write "0" to this bit no effect. *Note: After writing "1" to disable DVP port it may not immediately stops; it depends on the state of the hardware at that time. Logic "1" will be returned to this bit when the hardware is completely stopped. To ensure the hardware is stopped the software should check this bit whether logic "1" is returned. When this bit returns to 0, it means that the DVP is in an active state.*
23:20	Reserved	Reserved, the reset value must be maintained.
19	FMSF	Start of frame detected flag. This bit is set to "1" when start of frame (Vsync or equivalent vsync in embedded mode) is detected. Write "0" to this bit no effect. Write "1" to this bit it clears this flag. Note: It starts to detect start of frame only after DVP_CTRL.DVPEN is set to '1'.
18	SERRF	SYNC code sequence error detected flag. This bit is only used in embedded

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Bit field	Name	Description
		synchronization mode. This bit is set to "1" when a SYNC code sequence error is detected while it is in image active region, and it will not detect this error while it is in vertical blanking region. If it is set and its corresponding DVP_INTEN.SERRIE =1， then an interrupt will be sent. Write "1" to this bit to clear. Write "0" no effect.
17	CERRF	sync code mismatch error detected flag. This bit is only used in embedded synchronization mode. This bit is set to "1" when a SYNC code mismatch is detected while it is in image active region, and it will not detect this error while it is in vertical blanking region. If it is set and its corresponding DVP_INTEN.CERRIE=1， then an interrupt will be sent. Write "1" to this bit to clear. Write "0" no effect.
16	SKIPF	Frame skipping detected flag. This bit is set to "1" when there is no more FIFO space or frame buffer memory to receive a new frame. This bit is only valid when the DVP port is enabled(DVP_CTRL.DVPEN=1). Write "1" to this bit to clear. Write "0" no effect.
15:10	Reserved	Reserved, the reset value must be maintained.
9	MO2F	Frame Buffer 2 Over Flow 0: no over flow event 1: over flow event detected When a frame data is exceeded the allocated frame buffer size this flag will be set to "1" and the data will be only written up to the frame buffer size. The remaining data will be dropped. Write "1" to this bit to clear. Write "0" no effect.
8	MO1F	Frame Buffer 1 Over Flow 0: no over flow event 1: over flow event detected When a frame data is exceeded the allocated frame buffer size this flag will be set to "1" and the data will be only written up to the frame buffer size. The remaining data will be dropped. Write "1" to this bit to clear. Write "0" no effect.
7	AHBERR2F	Receiving AHB bus error response on accessing to Frame Buffer 2 flag. This bit is set to "1" when the AHB master receives an error response from the bus while accessing Frame Buffer 2. If this occurs the Frame Buffer 2 will become unavailable until AHBERR2F is clear. Write "1" to this bit to clear. Write "0" no effect.
6	AHBERR1F	Receiving AHB bus error response on accessing to Frame Buffer 1 flag. This bit is set to "1" when the AHB master receives an error response from the bus while accessing Frame Buffer 1. If this occurs the Frame Buffer 1 will become unavailable until AHBERR1F is clear. Write "1" to this bit to clear. Write "0" no effect.
5	M2FOF	Frame Buffer 2 FIFO over flow flag.

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Bit field	Name	Description
		This bit is set to "1" when the FIFO overflow occurs while receiving frame data for Frame Buffer 2. Write "1" to this bit to clear. Write "0" no effect.
4	M1FOF	Frame Buffer 1 FIFO over flow flag. This bit is set to "1" when the FIFO overflow occurs while receiving frame data for Frame Buffer 1. Write "1" to this bit to clear. Write "0" no effect.
3	M2TCF	Data to Frame Buffer 2 completion flag. This bit is set to "1" when the Frame Buffer 2 is completed on receiving frame data. In single capture mode, this buffer only becomes available again when M2TCF is clear. Write "1" to this bit to clear. Write "0" no effect.
2	M1TCF	Data to Frame Buffer 1 completion flag. This bit is set to "1" when the Frame Buffer 1 is completed on receiving frame data. In single capture mode, this buffer only becomes available again when M1TCF M1_CMPL_FG is clear. Write "1" to this bit to clear. Write "0" no effect.
1	M2SF	Data to Frame Buffer 2 start flag. This bit is set to "1" when the Frame Buffer 2 starts receiving frame data. Write "1" to this bit to clear. Write "0" no effect.
0	M1SF	Data to Frame Buffer 1 start flag. This bit is set to "1" when the Frame Buffer 1 starts receiving frame data. Write "1" to this bit to clear. Write "0" no effect.

46.7.4 DVP port configuration register (DVP_PORTCFG)

Address offset: 0x0C

Reset value: 0x00E4 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HRSKIP[3:0]				HISKIP[3:0]				BMAP[7:0]							
rw				rw				rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PIXELDB	Reserved	DBIT[2:0]			EMBSEN	SLC	Reserved	DATRVS	DATINV	VSPOL	HSPOL	PCLKPOL
			rw		rw				rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:28	HRSKIP[3:0]	Repeat Line Skip Pattern Control (include even/odd line capturing) There are two configurations for this register: 0000~1101: After capturing a line of data, skip a certain number of lines, then continue capturing the next line, and repeat this process.

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Bit field	Name	Description
		1110、1111: Capture only odd or even lines. The specific situation is as follows: 0000: no skipping line。 0001: each captured line followed by one skip line. 0010: each captured line followed by two skip line. 0011: each captured line followed by three skip line. ….. 1101: each captured line followed by thirteen skip lines. 1110: only capture even lines and all odd lines are skipped (first line(row0) is captured, second line(row1) is dropped, etc). 1111: only capture odd lines and all even lines are skipped (first line(row0) is dropped, second line(row1) is captured, etc). The software can only modify this register when DVP_CTRL.DVPEN=0.
27:24	HISKIP[3:0]	Initial frame line skip control This register controls the number of the horizontal lines skipped at the beginning of each frame. The number of skip lines is ranged from 1 to 15. For example, if you set this register to 3 then the first 3 lines of each frames will not be captured. The software can only modify this register when DVP_CTRL.DVPEN=0.
23:16	BMAP[7:0]	Received pixel data to Frame Buffer mapping. Every 4 bytes of data received from DVP port can be treated as a data group. Within a data group (4 bytes) their byte positions can be repositioned before writing to Frame Buffer. BMAP [1:0]: where the first received data byte will be repositioned. BMAP [3:2]: where the second received data byte will be repositioned BMAP [5:4]: where the third received data byte will be repositioned. BMAP [7:6]: where the fourth received data byte will be repositioned. For example, if you want to swap the first and the second data bytes then you need to program BMAP [1:0]=01 and BMAP [3:2]=00。In normal operation, you can reposition all four bytes in any order, and the all 2-bit fields should not have the same value. If you try to remap 2 bytes to the same byte position then the lower order 2-bit field will take precedence. If a byte position is not remapped then the byte data at that position is remainded unchanged. In normal case, byte re-mapping should only be used for 8-bit mode.
15:13	Reserved	Reserved, the reset value must be maintained.
12	PIXELDB	2 bytes per pixel The software should set this bit to "1" when it is operated in 8-bit mode and it requires 2 bytes to describe a pixel, otherwise set this bit to "0". The software can only modify this bit when DVP_CTRL.DVPEN=0. *Note: This bit is only used for CROP mode. Only one byte per pixel and two bytes per pixel are supported for CROP mode.*
11	Reserved	Reserved, the reset value must be maintained.
10:8	DBIT[2:0]	DVP data port mode.

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Bit field	Name	Description
		000:8-bit physical data port, and data is captured on all data lines. 001:10-bit physical data port, and data is captured on all data lines. 010:12-bit physical data port, and data is captured on all data lines. 011:14-bit physical data port, and data is captured on all data lines. 100:16-bit physical data port, and data is captured on all data lines. 101: 10-bit physical data port, and data is captured on 8 data lines [9:2] only. 110: 12-bit physical data port, and data is captured on 10 data lines [11:2] only. 111: 12-bit physical data port, and data is captured on 8 data lines [11:4] only. The software can only modify this bit when DVP_CTRL.DVPEN=0.
7	EMBSEN	Embedded Synchronization Mode enable bit. 1: enable embedded synchronization mode. 0: use VSYNC and HSYNC to do synchronization The software can only modify this bit when DVP_CTRL.DVPEN=0.
6	SLC	Embedded Synchronization Code Position. 1: the sync code is aligned to the least significant bit of the data lines. e.g.when DBIT=1, the sync code is at [7:0]. DBIT=2, the sync code is at [7:0]. DBIT=6, the sync code is at [9:2]. 0: the sync code is aligned to the most significant bit of the data lines. e.g. when DBIT=1, the sync code is at [9:2]. DBIT=2, the sync code is at [11:4]. DBIT=6, the sync code is at [11:4]. This register can only be modified when DVP_PORTCFG.EMBSEN=0
5	Reserved	Reserved, the reset value must be maintained.
4	DATRVS	To reverse data bit order. 1: enable to reverse data bit order on the DVP port data. 0: remain original data bit order.
3	DATINV	Data bit inversion. 1: enable data bit inversion on the DVP port data. 0: data bit inversion is not enabled.
2	VSPOL	VSYNC polarity control. 1: when VSYNC=0 is vertical blanking at the DVP port. 0: when VSYNC=1 is vertical blanking at the DVP port. The software can only modify this bit when DVP_CTRL.DVPEN=0.
1	HSPOL	1: when HSYNC=1 is horizontal blanking at the DVP port. 0: when HSYNC=0 is horizontal blanking at the DVP port. The software can only modify this bit when DVP_CTRL.DVPEN=0.
0	PCLKPOL	DVP port pixel clock polarity control. DVP port pixel clock polarity control.。 1: the data from the sensor is expected to be latched at the falling edge of the pixel clock. 0: the data from the sensor is expected to be latched at the rising edge of the pixel clock. The software can only modify this bit when DVP_CTRL.DVPEN=0.

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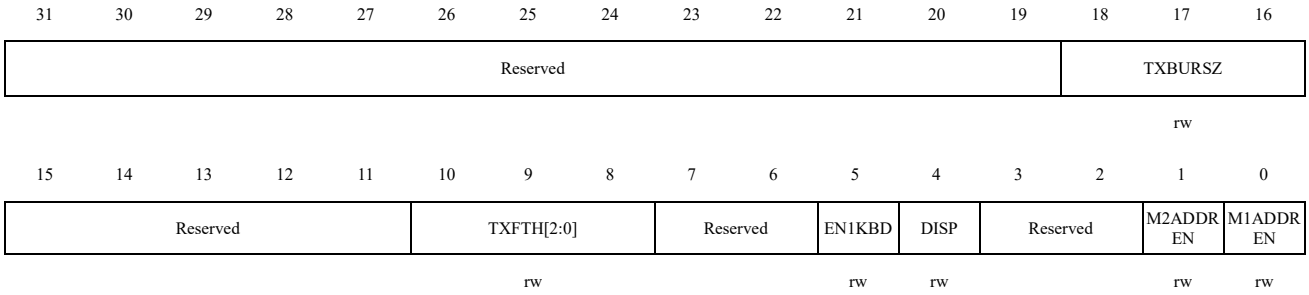
46.7.5 DVP FIFO configuration register (DVP_FIFOCFG)

Address offset: 0x10

Reset value: 0x0000 0000



Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18:16	TXBURSZ[2:0]	AHB master data burst setting. When FIFO data reaches transmit threshold the master initiates memory write burst cycle according to burst setting: 000: burst size is 8 bytes 001: burst size is 16 bytes 010: burst size is 24 bytes 011: burst size is 32 bytes 100: burst size is 40 bytes 101: burst size is 48 bytes 110: burst size is 56 bytes 111: burst size is 64 bytes *Note: Make sure DVP_FIFOCFG.TXBURSZ setting is same or smaller than DVP_FIFOCFG .TXFTH setting, otherwise it may encounter FIFO under run issue.*
15:11	Reserved	Reserved, the reset value must be maintained
10:8	TXFTH[2:0]	FIFO transmit threshold setting. When FIFO data reaches transmit threshold the master initiates memory write burst cycle according to burst setting: 000: transmit threshold is 8 bytes. 001: transmit threshold is 16 bytes. 010: transmit threshold is 32 bytes. 011: transmit threshold is 64 bytes. 100: transmit threshold is 128 bytes. 101: transmit threshold is 256 bytes. 110: transmit threshold is 512 bytes. 111: transmit threshold is 1024 bytes. *Note: Make sure DVP_FIFOCFG.TXBURSZ setting is same or smaller than*

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Bit field	Name	Description
		DVP_FIFOCFG .TXFTH setting, otherwise it may encounter FIFO under run issue.
7:6	Reserved	Reserved, the reset value must be maintained
5	EN1KBD	Bursting across 1K boundary Control 0: increamental bursting across 1K boundary is disabled 1: increamental bursting across 1K boundary is allowed/enabled *Note: If this is disabled every increamental bursting across 1K boundary will be break up and send non-sequential transaction, once it acrosses 1K boundary, it will resume increamental sequential transaction again. This control bit is for debug purpose, in normal case should leave it as default setting, '0'.*
4	DISPMODE	To show current frame buffer status in term of image data byte count or buffer address control. 1: buffer address is output on DVP_FPBC1 and DVP_FPBC2 registers 0: number of data bytes which have been sent to Frame buffer is output on DVP_FPBC1 and DVP_FPBC2 registers
3:2	Reserved	Reserved, the reset value must be maintained
1	M2ADDREN	Frame Buffer 2 enable control 1: Frame Buffer 2 is enabled. 0: Frame Buffer 2 is not enabled. *Note: There is a restriction to enable Frame Buffer 2: it can only be enabled at the same time as Frame Buffer 1 is enabled. Frame Buffer 2 is not allowed to be used alone. If you just need one frame buffer then you have to use Frame Buffer 1.* *The software can only modify this bit when DVP_CTRL.DVPEN=0*
0	M1ADDREN	Frame Buffer 1 enable control 1: Frame Buffer 1 is enabled. 0: Frame Buffer 1 is not enabled. The software can only modify this bit when DVP_CTRL.DVPEN=0 and DVP_FBS.FMSIZE has to be non-zero.

46.7.6 DVP frame 1 start memory address register (DVP_SMADDR1)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MADDR[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MADDR[31:0]															
rw															

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Bit field	Name	Description
31:0	MADDR[31:0]	Frame Buffer 1 Start Address. This address is only valid when DVP_FIFOCFG.M1ADDREN=1. This address has to be 32-bit align, which means MADDR[1:0] = 0. This register can only be modified when DVP_FIFOCFG.M1ADDREN=0.

46.7.7 DVP frame 2 start memory address register (DVP_SMADDR2)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MADDR[31:0]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MADDR[31:0]															
rw															

Bit field	Name	Description
31:0	MADDR[31:0]	Frame Buffer 2 Start Address. This address is only valid when DVP_FIFOCFG.M2ADDREN=1. This address has to be 32-bit align, which means MADDR[1:0] = 0. This register can only be modified when DVP_FIFOCFG.M2ADDREN=0.

46.7.8 DVP frame buffer size register (DVP_FBS)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										FMSIZE[21:0]					
										rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMSIZE[21:0]															
rw															

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21:0	FMSIZE[21:0]	Set the frame buffer size. This register is used to protect the hardware from writing

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Bit field	Name	Description
		frame data beyond this range.

46.7.9 DVP frame 1 pixel byte count register (DVP_FPBC1)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIXLC[31:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXLC[31:0]															
r															

Bit field	Name	Description
31:0	PIXLC[31:0]	This register is read only. When DVP_FIFOCFG.DISPMODE = 0, it stores the data byte count of frame buffer 1. When DVP_FIFOCFG.DISPMODE = 1, it stores the address of frame buffer 1.

46.7.10 DVP frame 2 pixel byte count register (DVP_FPBC2)

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIXLC[31:0]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXLC[31:0]															
r															

Bit field	Name	Description
31:0	PIXLC[31:0]	This register is read only. When DVP_FIFOCFG.DISPMODE = 0, it stores the data byte count of frame buffer 2. When DVP_FIFOCFG.DISPMODE = 1, it stores the address of frame buffer 2.

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46.7.11 DVP crop start XY register (DVP_CSXY)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					CSTAY[10:0]										
					rw										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CSTAX[11:0]											
				rw											

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained
26:16	CSTAY[10:0]	Y-coordinate of crop image start point. It is in term of vertical lines. This register will only be used when DVP_CTRL.CROPEN=1. *Note: The first pixel coordinate is (0,0).*
15:12	Reserved	Reserved, the reset value must be maintained
11:0	CSTAX[11:0]	X-coordinate of crop image start point. It is in term of image pixels. This register will only be used when DVP_CTRL.CROPEN=1. *Note: The first pixel coordinate is (0,0).*

46.7.12 DVP crop end XY register (DVP_CEXY)

Address offset: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					CENDY[10:0]										
					rw										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CENDX[11:0]											
				rw											

Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained
26:16	CENDY[10:0]	Y-coordinate of crop image end point. It is in term of vertical lines. This register will only be used when DVP_CTRL.CROPEN=1

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Bit field	Name	Description
		Note: The first pixel coordinate is (0,0).
15:12	Reserved	Reserved, the reset value must be maintained
11:0	CENDX[11:0]	X-coordinate of crop image end point. It is in term of image pixels. This register will only be used when DVP_CTRL.CROPEN=1. *Note: The first pixel coordinate is (0,0).*

46.7.13 DVP embedded synchronization code marker register (DVP_EMSC)

Address offset: 0x30

Reset value: 0x9D80 B6AB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HE_PTTN [7:0]								HS_PTTN [7:0]							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VE_PTTN [7:0]								VS_PTTN [7:0]							
rw								rw							

Bit field	Name	Description
31:24	HE_PTTN [7:0]	Line valid ending synchronization code. This bit can configure the fourth byte data of the synchronization code in the embedded synchronization mode, serving as a feature value to send the line valid ending synchronization code to the DVP system. This register can only be modified when DVP_PORTCFG.EMBSEN =0.
23:16	HS_PTTN [7:0]	Line valid starting synchronization code This bit can configure the fourth byte data of the synchronization code in the embedded synchronization mode, serving as a feature value to send the line valid starting synchronization code to the DVP system. This register can only be modified when DVP_PORTCFG.EMBSEN=0.
15:8	VE_PTTN [7:0]	Frame ending synchronization code This bit can configure the fourth byte data of the synchronization code in the embedded synchronization mode, serving as a feature value to send the frame ending synchronization code to the DVP system. This register can only be modified when DVP_PORTCFG.EMBSEN=0.
7:0	VS_PTTN [7:0]	Frame starting synchronization code This bit can configure the fourth byte data of the synchronization code in the embedded synchronization mode, serving as a feature value to send the frame starting synchronization code to the DVP system. This register can only be modified when DVP_PORTCFG.EMBSEN=0.

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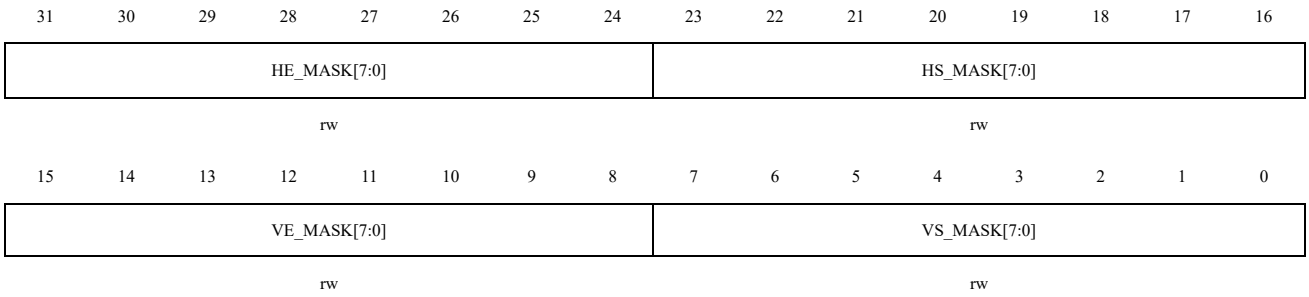
46.7.14 DVP embedded synchronization code mask register (DVP_EMSCM)

Address offset: 0x34

Reset value: 0x0000 0000



Bit field	Name	Description
31:24	HE_MASK[7:0]	This is mask register for HE_PTTN register. If the corresponding HE_PTTN mask bits are set to "1" then these bits in HE_PTTN will be excluded from this pattern detection. This register can only be modified when DVP_PORTCFG.EMBSEN=0.
23:16	HS_MASK[7:0]	This is mask register for HS_PTTN register. If the corresponding HS_PTTN mask bits are set to "1" then these bits in HS_PTTN will be excluded from this pattern detection. This register can only be modified when DVP_PORTCFG.EMBSEN=0.
15:8	VE_MASK[7:0]	This is mask register for VE_PTTN register. If the corresponding VE_PTTN mask bits are set to "1" then these bits in VE_PTTN will be excluded from this pattern detection. This register can only be modified when DVP_PORTCFG.EMBSEN=0.
7:0	VS_MASK[7:0]	This is mask register for VS_PTTN register. If the corresponding VS_PTTN mask bits are set to "1" then these bits in VS_PTTN will be excluded from this pattern detection. This register can only be modified when DVP_PORTCFG.EMBSEN=0.

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Email: sales@nsing.com.sg

47 Ethernet (ETH)

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47.1 Introduction

The N32H7xx supports two Ethernet peripheral modules, ETH1 contains 10/100/1000Mbps Ethernet MAC and ETH2 contains 10/100Mbps Ethernet MAC. The Ethernet module uses dedicated DMA to optimize the performance of transmitting and receiving packets. The ETH module supports standard interfaces to communicate with the physical layer (PHY): MII, RMII, GMII (*Note: ETH2 does not support GMII interface*) to realize the transmission and reception of Ethernet packets. The Ethernet module adheres to the following standards:

- IEEE 802.3-2015 for Ethernet MAC, GMII, MII
- IEEE 1588-2008 for precision networked clock synchronization
- IEEE 802.3az-2010 for EEE
- AMBA 2.0 for AHB master, AHB slave
- RMII specification version 1.2 from RMII consortium

47.2 Main Features

47.2.1 MAC Features

MAC Tx and Rx Common Features

- Separate transmission, reception, and control interfaces to the application
- 10, 100, and 1000 Mbps data transfer rates with the following PHY interfaces:
  - MII interface to communicate with external Fast Ethernet PHY
  - RMII interface to communicate with an external Fast Ethernet PHY
  - GMII interface to communicate with external Gigabit Ethernet PHY
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support
- 32-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- Support network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction

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- Flexibility to control the Pulse-Per-Second (PPS) output signal
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

MAC Tx Features

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets with up to 16 KB of size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in full-duplex mode)
- Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
- Insertion, replacement, or deletion of up to two VLAN tags
- Transmit packets with reduced preamble size in full-duplex mode
- Insert, replace, or delete queue/channel-based VLAN tags

MAC Rx Features

- Automatic Pad and CRC Stripping
- Preamble and SFD deletion
- Programmable watchdog timeout limit
- Flexible address filtering modes:
  - four 48-bit perfect (DA) address filters with masks for each byte
  - four 48-bit SA address comparison check with masks for each byte
  - 64 bit Hash filter for multicast and unicast (DA) addresses
  - Support to pass all multi-cast addressed packets
  - Promiscuous mode to pass all packets without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Additional packet filtering:
  - VLAN tag-based: Perfect match and Hash-based (optional) filtering. Filtering based on either outer or inner VLAN tag is possible
  - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
- IEEE 802.1Q VLAN tag detection and delete the VLAN tags in received packets
- Detect remote wake-up packets and AMD magic packets

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- Forwarding of received Pause packets to the application (in full-duplex mode)
- Receive module for Layer 3/Layer 4 checksum offload for received packets

47.2.2 MAC Transaction Layer (MTL) Features

MTL Tx and Rx Common Features

- 32-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Optimization for packet-oriented transfers with packets delimiters
- Dual-port RAM based asynchronous FIFO controllers
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)

MTL Tx Features

- 2KB transmit FIFO with programmable threshold capability
- One queues on the Transmit path
- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Automatic retransmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO
- Packet-level control for:
  - VLAN tag insertion or replacement
  - Ethernet source address insertion
  - Layer3/Layer4 Checksum insertion control
  - One-step timestamp
  - Timestamp control
  - CRC and pad control

MTL Rx Features

- 2KB receive FIFO with programmable threshold capability
- One queues on the Receive path
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in

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Store-and-Forward mode)

- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level

47.2.3 DMA Features

- 32-bit data transfers
- Separate DMA for transmit and receive paths
- Optimization for packet-oriented DMA transfers with packet delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host CSR access and host data interface
- TCP Segmentation Offload (TSO)

47.2.4 Bus Features

AHB Master Interface Features

- 32-bit, Interfaces with the application through AHB
- Little-endian modes
- Software-selected type of AHB burst (fixed burst, indefinite burst, or mix of both)

AHB Slave Interface Features

- 32-bit, AHB slave interface for CSR access

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- Little-endian modes
- All AHB burst types

47.2.5 Monitoring, Testing, and Debugging Features

- Internal loopback from Tx to Rx on the GMII or MII for debugging
- DMA states (Tx and Rx) as status bits
- Debug status register that gives status of FSMs in Transmit and Receive data paths and FIFO fill-levels
- Application Abort status bits
- MMC (RMON) module
- Current Tx or Rx Buffer pointer as status registers
- Current Tx or Rx Descriptor pointer as status registers
- Tx or Rx Queues memory accessible through Slave port for debug

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47.3 Block Diagram

The Ethernet peripheral primarily consists of the following four functional modules:

- Control and Status Register module (CSR)

  The CSR space comprises all internal control registers and status registers of the Ethernet peripheral and is accessed via an AHB 32-bit slave interface.

- Direct Memory Access control module (DMA)

  Includes one physical channel for receiving and one physical channel for transmitting. It controls data transmission between the MAC and system memory via the AHB 32-bit master interface.

- MAC Transaction Layer module (MTL)

  It controls data flow between the application and MAC.

- Media Access Control module (MAC)

  It implements the Ethernet protocol.

Additionally, it includes a protocol adaptation module to support the RMII PHY medium-independent interface. The functional block diagram of the Ethernet peripheral is shown in Figure 47-1.

47.3.1 DMA

The DMA has independent Transmit (Tx) and Receive (Rx) engines, and a CSR space. The Tx engine transfers data from the system memory to the device port (MTL), whereas the Rx engine transfers data from the device port to the system memory.

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed to interrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

47.3.2 MTL

The MAC Transaction Layer (MTL) provides the FIFO memory Interface to buffer and regulate the packets between the application system memory and the MAC. It also enables the data to be transferred between the application clock and MAC clock domains. The MTL layer has two data paths: Transmit path and Receive Path. The data path for both directions can be 32-bit wide.

The MTL communicates with the application through Application Transmit Interface (ATI) on the Transmit path and Application Receive Interface (ARI) on the Receive path. The MTL also provides the MAC Control Interface (MCI) as a control path.

47.3.3 MAC

The MAC is responsible for processing Ethernet protocol packets. In transmit mode, the MAC receives data from the

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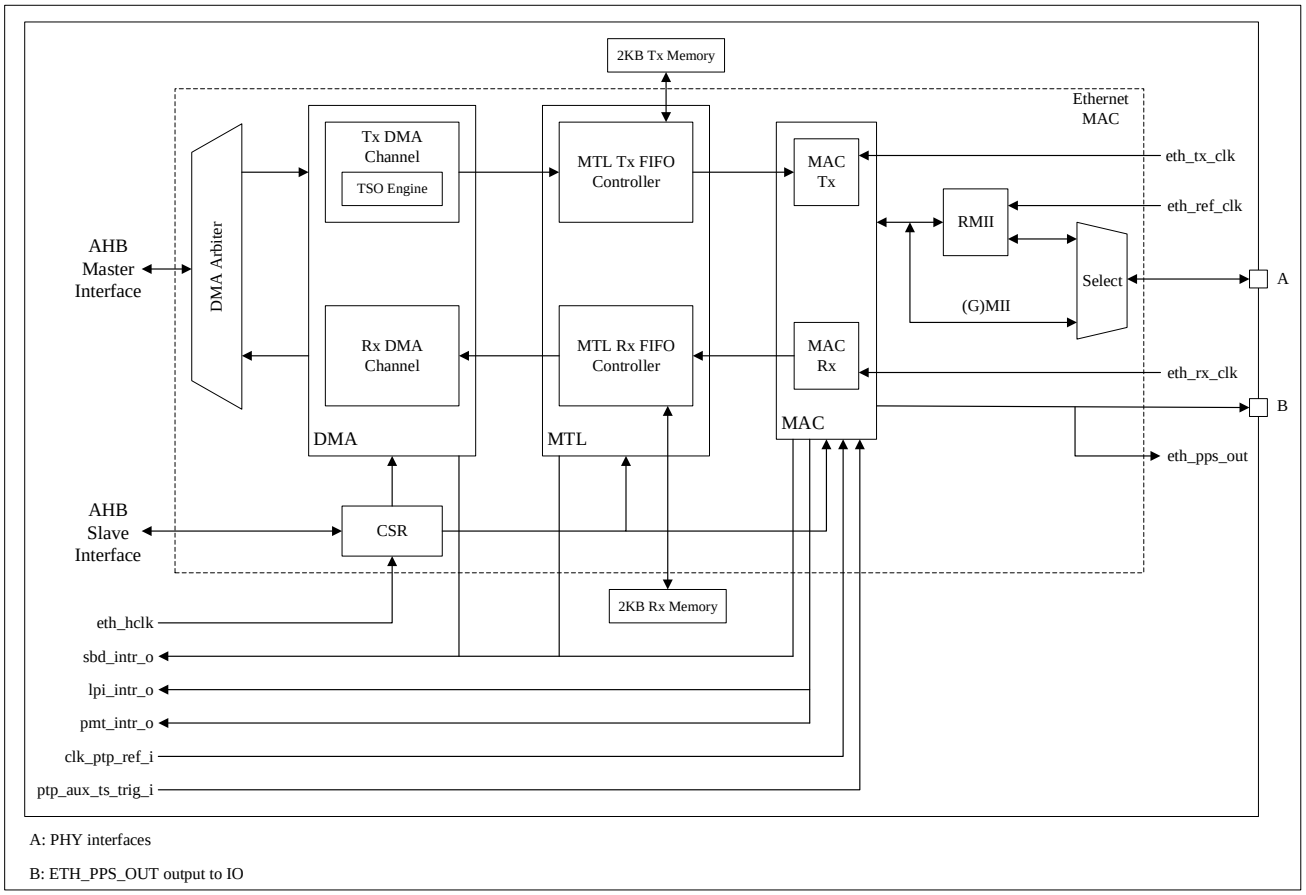
Tx FIFO of the MTL module and then transmits it to the PHY interface. In receive mode, the MAC receives data from the PHY interface and then transmits it to the Rx FIFO of the MTL module.

The MAC supports many interfaces towards the PHY chip. The PHY interface can be selected only once after reset. The MAC communicates with the application side with the MAC Transmit Interface (MTI), MAC Receive Interface (MRI), and MAC Control Interface (MCI).

Figure 47-1 ETH Block Diagram



A: PHY interfaces

B: ETH_PPS_OUT output to IO

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47.4 Pin Definitions

This section lists the Ethernet input/output signals connected to the GPIO, and also lists and explains the internal Ethernet signals involved in Figure 47-1 and the following text. Specific descriptions are shown in Table 47-1 , Table 47-3 and Table 47-3:

Table 47-1 ETH1 peripheral pins

Alternate Function	Pin Name(1)	Description
ETH1_CLK125	PD10	125M clock signal, GMII only
ETH1_MII_RXD0 ETH1_RMII_RXD0 ETH1_GMII_RXD0	PC4	Receive data line 0
ETH1_MII_RXD1 ETH1_RMII_RXD1 ETH1_GMII_RXD1	PC5	Receive data line 1
ETH1_MII_RXD2 ETH1_GMII_RXD2	PB0, PH6	Receive data line 2, MII/GMII only
ETH1_MII_RXD3 ETH1_GMII_RXD3	PB1, PH7	Receive data line 3, MII/GMII only
ETH1_GMII_RXD4	PE12, PH8	Receive data line 4, GMII only
ETH1_GMII_RXD5	PE13, PH9	Receive data line 5, GMII only
ETH1_GMII_RXD6	PE14, PH10	Receive data line 6, GMII only
ETH1_GMII_RXD7	PE15, PH11	Receive data line 7, GMII only
ETH1_MII_TXD0 ETH1_RMII_TXD0 ETH1_GMII_TXD0	PB12, PG13	Transmit data line 0
ETH1_MII_TXD1 ETH1_RMII_TXD1 ETH1_GMII_TXD1	PB13, PG12, PG14	Transmit data line 1
ETH1_MII_TXD2 ETH1_GMII_TXD2	PB7, PC2, PE3	Transmit data line 2, MII/GMII only
ETH1_MII_TXD3 ETH1_GMII_TXD3	PB8, PE2	Transmit data line 3, MII/GMII only
ETH1_GMII_TXD4	PF0, PI4	Transmit data line 4, GMII only
ETH1_GMII_TXD5	PF1, PI5	Transmit data line 5, GMII only
ETH1_GMII_TXD6	PF2, PI6	Transmit data line 6, GMII only
ETH1_GMII_TXD7	PF3, PI7	Transmit data line 7, GMII only
ETH1_MDC	PC1	Station management interface clock signal
ETH1_MDIO	PA2	Station management interface data signal
ETH1_MII_COL ETH1_GMII_COL	PA3, PH3	Collision detection signal, MII/GMII only
ETH1_MII_CRS	PA0, PH2	Carrier sense signal, MII/GMII only

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Alternate Function	Pin Name(1)	Description
ETH1_GMII_CRS		
ETH1_MII_RX_CLK ETH1_RMII_REF_CLK ETH1_GMII_RX_CLK	PA1	Reference clock signal, 50 MHz, RMII only; Receive clock signal, 2.5 MHz at 10 Mbps, 25 MHz at 100 Mbps, MII only; Receive clock signal, 2.5 MHz at 10 Mbps, 25 MHz at 100 Mbps, 125 MHz at 1000 Mbps , GMII only
ETH1_MII_RX_DV ETH1_RMII_CRS_DV ETH1_GMII_RX_DV	PA7	Receive data valid signal for MII/GMII, multiplexed with carrier sense and receive data valid signal for RMII
ETH1_MII_RX_ER ETH1_GMII_RX_ER	PB10, PI10	Receive error signal, MII/GMII only
ETH1_MII_TX_CLK ETH1_GMII_TX_CLK	PC3	Transmit clock signal, 2.5 MHz at 10 Mbps, 25 MHz at 100 Mbps, MII only; Transmit clock signal, 2.5 MHz at 10 Mbps, 25 MHz at 100 Mbps, 125 MHz at 1000 Mbps , GMII only
ETH1_MII_TX_EN ETH1_RMII_TX_EN ETH1_GMII_TX_EN	PB11, PG11	Transmit data enable signal, shared by MII/ RMII/GMII
ETH1_MII_TX_ER ETH1_GMII_TX_ER	PA9, PB2	Transmit error signal, MII/GMII only
ETH1_PHY_INTN	PB4, PD15, PG7, PG15	External PHY interrupt signal
ETH1_PPS_OUT	PB5, PD14, PG8	Second pulse output signal

1. For the pin alternate function mapping of ETH1, please refer to the GPIO section.

Table 47-2 ETH2 peripheral pins

Alternate Function	Pin Name(1)	Description
ETH2_MII_RXD0 ETH2_RMII_RXD0	PG2, PG9, PI1	Receive data line 0
ETH2_MII_RXD1 ETH2_RMII_RXD1	PG3, PG10, PI2	Receive data line 1
ETH2_MII_RXD2	PG4, PJ8	Receive data line 2, MII only
ETH2_MII_RXD3	PG5, PJ9	Receive data line 3, MII only
ETH2_MII_TXD0 ETH2_RMII_TXD0	PF12, PH4, PH14	Transmit data line 0
ETH2_MII_TXD1 ETH2_RMII_TXD1	PF13, PH5, PH15	Transmit data line 1
ETH2_MII_TXD2	PF14, PJ0	Transmit data line 2, MII only
ETH2_MII_TXD3	PF15, PJ1	Transmit data line 3, MII only
ETH2_MDC	PF7	Station management interface clock signal
ETH2_MDIO	PF6	Station management interface data signal
ETH2_MII_COL	PF8, PK0	Collision detection signal, MII only
ETH2_MII_CRS	PF9, PK1	Carrier sense signal, MII only
ETH2_MII_RX_CLK ETH2_RMII_REF_CLK	PA8, PF4, PJ4	Reference clock signal, 50 MHz, RMII only; Receive clock signal, 2.5 MHz at 10 Mbps, 25 MHz at 100 Mbps, MII only

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Alternate Function	Pin Name(1)	Description
ETH2_MII_RX_DV ETH2_RMII_CRS_DV	PC0, PH12, PJ3	Receive data valid signal for MII, multiplexed with carrier sense and receive data valid signal for RMII
ETH2_MII_RX_ER	PG6, PI3	Receive error signal, MII only
ETH2_MII_TX_CLK	PG0, PI8	Transmit clock signal, 2.5 MHz at 10 Mbps, 25 MHz at 100 Mbps, MII only
ETH2_MII_TX_EN ETH2_RMII_TX_EN	PF11, PH13	Transmit data enable signal, shared by MII/ RMII
ETH2_MII_TX_ER	PG1, PJ5	Transmit error signal, MII only
ETH2_PHY_INTN	PD15, PE4, PE7	External PHY interrupt signal
ETH2_PPS_OUT	PD10, PF10, PI15	Second pulse output signal

1. For the pin alternate function mapping of ETH2, please refer to the GPIO section.

Table 47-3 ETH internal signals

Signal Name	I/O Type	Description
eth_hclk	Digital input	AHB Clock
sbd_intr_o	Digital output	Ethernet module global interrupt signal, which is the output signal after logical AND operation of DMA, MTL, and MAC-related interrupt signals
sbd_perch_tx_intr_o[0]	Digital output	DMA transmit channel 0 interrupt signal
sbd_perch_rx_intr_o[0]	Digital output	DMA receive channel 0 interrupt signal
lpi_intr_o	Digital output	Interrupt signal when the transmitter or receiver enters or exits LPI state. This signal for ETH1 is connected to EXTI Line 83, and this signal for ETH2 is connected to EXTI Line 84
pmt_intr_o	Digital output	Interrupt signal when receiving a magic packet or remote wake-up packet. This signal for ETH1 is connected to EXTI Line 83, and this signal for ETH2 is connected to EXTI Line 84
clk_ptp_ref_i	Digital input	PTP reference clock input signal
ptp_aux_ts_trig_i	Digital input	Timestamp auxillary snapshot trigger input signal, connected to CAN and TIM
eth_tx_clk	Digital input	MII/GMII transmit clock
eth_ref_clk	Digital input	RMII reference clock
eth_rx_clk	Digital input	MII/GMII receive clock
eth_pps_out	Digital output	Second pulse output signal, specifically the signal output to other peripheral modules such as CAN and TIM. The second pulse signal output to GPIO is denoted in uppercase: ETH_PPS_OUT
phy_intr_i	Digital input	External PHY interrupt input signal. The MAC detects the rising edge of this signal and triggers the PHY interrupt.

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47.5 Function Description

47.5.1 DMA Function Description

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The DMA supports 1 Tx and 1 Rx Descriptor list (or DMA channel). The base address of each list is written to the respective DMA CH0 Tx Descriptor List Address register and DMA CH0 Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA CH0 Control register. The number of descriptors in the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. After processing the last descriptor in the list, DMA automatically jumps back to the descriptor in the List Address register to create a descriptor ring.

The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.

The Ethernet peripheral supports the ring structure for the DMA descriptor. For more information on the descriptor, see 47.5.15 that describes the descriptor structure and how the DMA accesses the descriptors.

47.5.1.1 Bus Burst Access

The DMA engines attempts to transfer data in a burst of maximum size as programmed in the PBL fields of Transmit Control and Receive Control registers of the respective DMA. The Rx and Tx descriptors are always accessed in the maximum possible (limited by PBL or 16 * 8/bus width) burst length for 16 bytes to be read. The burst transfers initiated by the DMA can be split into multiple burst transfers as per the Application Interface protocol (AHB) requirements and the settings of DMA SysBus Mode register.

The Tx DMA initiates a data transfer only when sufficient space is available in the MTL Tx Queue to accommodate either of the following:

- Bytes corresponding to the configured burst (PBL * bus_width/8)
- Remaining bytes in Tx Buffer without EOP
- Number of bytes till EOP

The Rx DMA initiates a data transfer in the following conditions:

- Sufficient data is available in MTL Rx Queue to accommodate the configured burst
- EOP (when it is less than the configured burst length) is detected in the Rx Queue

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Email: sales@nsing.com.sg

The DMA indicates the start address and the number of transfers required to the AHB master interface. When the AHB Interface is configured for fixed-length burst, it transfers the data by using the best combination of INCR4, INCR8, or INCR16 and SINGLE transactions. If EOP is reached before the fixed-burst ends on the AHB interface, dummy transfers are performed in-order to complete the fixed-burst. Otherwise [Bit 0 of DMA SysBus Mode register is reset], the DMA transfers the data using INCR (undefined length) and SINGLE transactions.

When the AHB interface is configured for address-aligned beats, both DMA engines ensure that the first burst transfer initiated by the AHB is less than or equal to the size of the configured PBL. Therefore, all subsequent beats start at an address that is aligned to the configured PBL. The DMA can only align the address for beats up to size 16 (for PBL > 16) for AHB interface because it does not support more than INCR16.

47.5.1.2 Data Buffer Alignment

The Tx and Rx data buffers do not have any restrictions on start address alignment. For example, in systems with 32-bit memory, the start address for buffers can be aligned to any of the four bytes. However, the DMA always initiates write transfers with address aligned to the bus width and dummy data (old data) in the invalid byte lanes. This typically happens during the transfer of the beginning or end of an Ethernet packet. The software driver should discard the dummy bytes based on the start address of the buffer and size of the packet.

Table 47-4 Application Data Buffer Alignment Examples

Access operation	Description
Buffer Read	If the Tx buffer address is 32'h00000FF2 (for 32-bit data bus), and 15 bytes is to be transferred, the DMA reads five full words from address 32'h00000FF0. But when transferring data to the MTL Tx queue, the extra bytes (the first two bytes) are dropped or ignored. Similarly, the last 3 bytes of the last transfer are also ignored. The DMA always ensures that it transfers a full 32-bit data to the MTL Tx queue, unless it is the end of packet.
Buffer Write	If the Rx buffer address is 32'h0000FF2 (for 64-bit data bus) and 16 bytes of a received packet is to be transferred, the DMA writes 3 full words from address 32'h00000FF0. However, the first 2 bytes of the first transfer and the last 6 bytes of the third transfer have dummy data. The DMA considers the offset address only if it is the first Rx buffer of the packet. The DMA ignores the offset address and performs full word writes for the middle and the last Rx buffer of the packet.

47.5.1.3 Buffer Size Calculations

The DMA does not update the size fields in the Tx and Rx descriptors. The DMA updates only the status fields (RDES and TDES) of the descriptors. The driver has to perform the size calculations.

The Tx DMA transfers the exact number of bytes (indicated by buffer size field of TDES2) towards the MAC. If a descriptor is marked as first (FD bit of TDES3 is set), the DMA marks the first transfer from the buffer as SOP. If a descriptor is marked as last (LD bit of TDES3), the DMA marks the last transfer from that data buffer as EOP to the MTL.

The Rx DMA transfers data to a buffer until the buffer is full or the end of packet is received from the MTL. When the FD bit of a descriptor is set, the amount of valid data in a buffer is accurately indicated by the buffer size field (programmed in DMA Channel Receive Control register) minus the data buffer pointer offset. The offset is zero when the data buffer pointer is aligned to the data bus width. If a descriptor is marked as last, the buffer may not be full (as indicated by the buffer size in Bits [14:1] of Receive Control register). To compute the amount of valid data in this

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final buffer, the driver must read the packet length (PL bits of RDES3[14:0]) and subtract the sum of the buffer sizes of the preceding buffers in this packet. The Rx DMA always transfers the start of next packet with a new descriptor.

Note: Even when the start address of a Rx buffer is not aligned to the data width of system bus, the system should allocate a Rx buffer of a size aligned to the system bus width. For example, if the system allocates a Rx buffer of 1,024 bytes (1 KB) starting from address 0x1000, the software can program the buffer start address in the Rx descriptor to have a 0x1002 offset. The Rx DMA writes the packet to this buffer with dummy data in the first two locations (0x1000 and 0x1001). The actual packet is written from location 0x1002. Therefore, the actual useful space in this buffer is 1,022 bytes, even though the buffer size is programmed as 1,024 bytes, because of the start address offset.

47.5.1.4 DMA Arbiter

The arbiter inside the DMA module performs the arbitration between the Tx and Rx channel accesses to the AHB master interface. The following two types of arbitrations are supported:

- Round-Robin Arbitration

  When Bit 1 of the DMA Mode register is reset and both Tx and Rx DMAs are simultaneously requesting for access, the arbiter allocates the data bus in ratio set by Bits [14:12] of DMA Mode register.

- Fixed-Priority Arbitration

  When Bit 1 of the DMA Mode register is set, the Rx DMA always gets priority over the Tx DMA for data access by default. When Bit 11 of DMA Mode register is also set, the Tx DMA gets priority over the Rx DMA.

47.5.1.5 Transmit Operation: Default (Non-OSP) Mode

The Tx DMA engine in default mode proceeds as follows:

1. The application sets up the Transmit descriptor (TDES0–TDES3) and sets the Own bit (TDES3[31]) after setting up the corresponding data buffer(s) with Ethernet Packet data.
2. The application advances the Descriptor Tail pointer offset value of the Transmit Channel.
3. The DMA fetches the descriptor from the application memory.
4. If the DMA detects one of the following conditions, the transmission from that channel is suspended and Bit 2 and Bit 16 of DMA CH0 Status register are set and the Tx Engine proceeds to step 10:
   - The descriptor is flagged as owned by the application (TDES3 [31] = 1'b0)
   - The Descriptor Tail pointer is equal to the Current Descriptor pointer in Ring Descriptor list Mode
   - An error condition occurs
5. If the acquired descriptor is flagged as owned by the DMA (TDES3[31] = 1’b1), the DMA decodes the Transmit Data Buffer address from the acquired descriptor.
6. The DMA fetches the Transmit data from the system memory and transfers the data to the MTL for transmission.
7. If an Ethernet packet is stored over data buffers in multiple descriptors, the DMA closes the intermediate descriptor and fetches the next descriptor. Steps 3 through 6 are repeated until the end of-Ethernet-packet data is transferred to the MTL.

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8. When packet transmission is complete, if IEEE 1588 Timestamp feature was enabled for the packet (as indicated in the Tx status), the timestamp value obtained from MTL is written to the Tx descriptor (TDES0 and TDES1) that contains the EOP buffer. The status information is written to this Tx descriptor (TDES3). The application now owns this descriptor because the Own bit is cleared during this step.

   If timestamp feature is not enabled for this packet, the DMA does not alter the contents of TDES0 and TDES1.

9. Bit 0 of DMA CH0 Status register is set after completing transmission of a packet that has Interrupt on Completion (TDES2[31]) set in its Last Descriptor. The DMA engine returns to step 3.

10. In the Suspend state, the DMA tries to acquire the descriptor again (and thereby return to step 3). A poll demand command is triggered by writing any value to the DMA CH0 TxDesc Tail Pointer register when it receives a Transmit Poll demand and the Underflow Interrupt Status bit is cleared. If the application stopped the DMA by clearing Bit 0 of DMA CH0 Transmit Control register, the DMA enters the Stop state.

Note: In non-OSP mode, it is not required for the driver/application to extract the packet status and release the descriptor for the packet, even though FD is set to 1. The driver must track the descriptor that has OWN=0 and LD=1, as 1; such a descriptor contains the transmission status for the packet. This indicates that descriptors up to this descriptor can be released for reuse by the driver/application for subsequent packets.

The Tx DMA transmission flow in default mode is shown in Figure 47-2.

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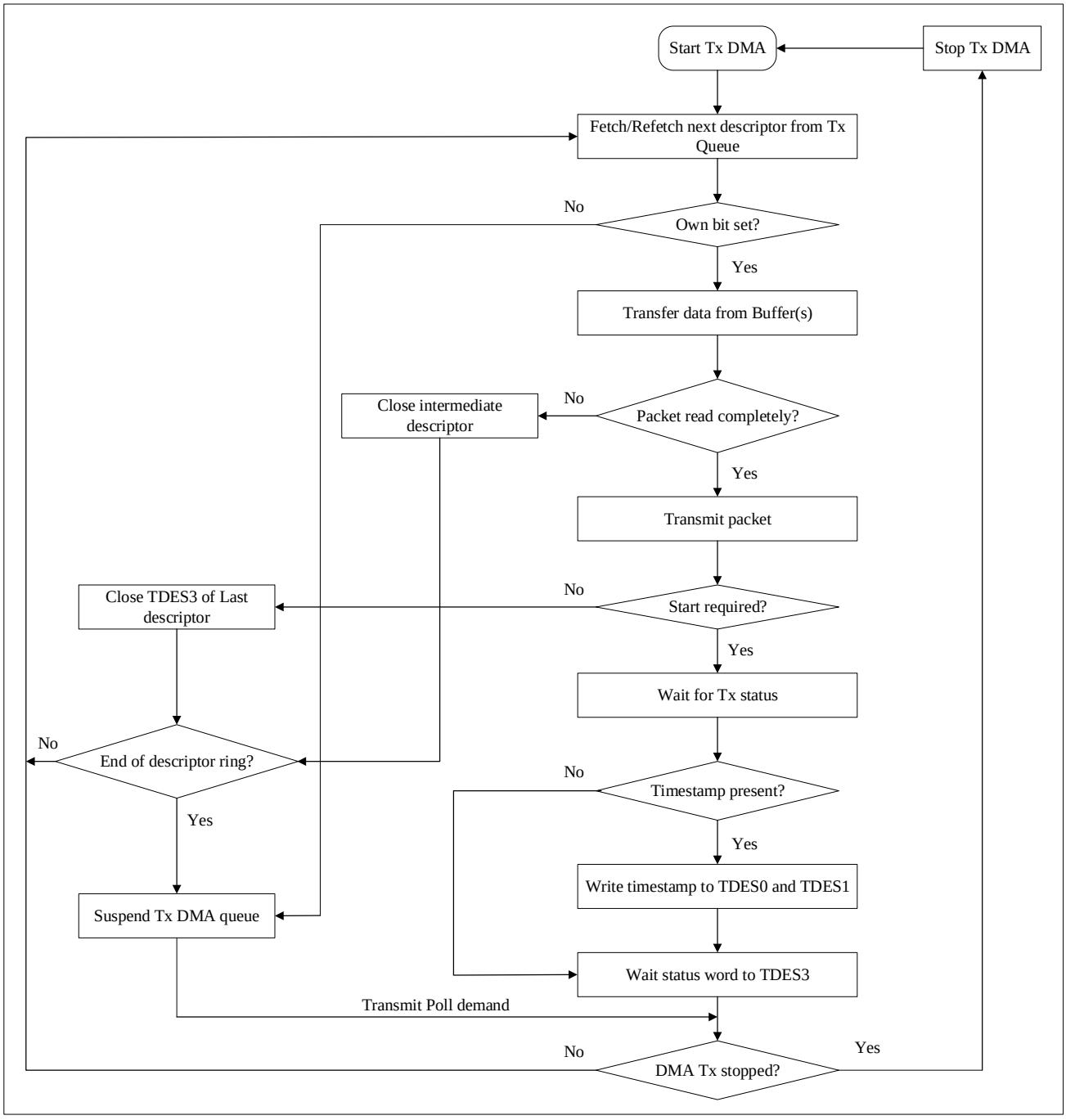
Figure 47-2 Tx DMA Operation in Default Mode



47.5.1.6 Transmit Operation: OSP Mode

In the Run state, if Bit 4 is set in the DMA CH0 Tx Control register, the Transmit process can simultaneously acquire two packets without closing the Status descriptor of the first packet. As the Transmit process finishes transferring the first packet, it immediately polls the Transmit Descriptor list for the second packet. If the second packet is valid, the Transmit process transfers this packet before writing the status information of the first packet.

In OSP mode, the Run state Tx DMA operates in the following sequence:

1. The DMA operates as described in step 1 to step 7 of the Tx DMA (default mode).

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2. The DMA fetches the next descriptor without closing the last descriptor of previous packet.
3. If the DMA owns the acquired descriptor, the DMA decodes the transmit buffer address in this descriptor. If the DMA does not own the descriptor, the DMA goes into Suspend mode and skips to step 7.
4. The DMA fetches the Transmit packet from the system memory and transfers the packet to the MTL until the EOP data is transferred, closing the intermediate descriptors if this packet is split across multiple descriptors.
5. The DMA waits for the packet transmission status and timestamp of previous packet. When the status is available, the DMA writes the timestamp to TDES0 and TDES1 if such timestamp was captured (as indicated by a status bit). The DMA writes the status, with a cleared Own bit, to the corresponding TDES3, thus closing the descriptor.

   If Timestamp feature is not enabled for the previous packet, the DMA does not alter the contents of TDES2 and TDES3.
6. The Transmit interrupt is set (if enabled). The DMA fetches the next descriptor and proceeds to step 3 (when Status is normal). If the previous transmission status shows an underflow error, the DMA goes into Suspend mode (step 7).
7. In Suspend mode, if a pending status and timestamp are received from the MTL, the DMA does the following:
   - Writes the timestamp (if enabled for the current packet) to TDES0 and TDES1
   - Writes the status to the corresponding TDES3
   - Sets relevant interrupts and returns to Suspend mode

   If no status is pending and the application stopped the DMA by clearing Bit 0 of DMA CH0 Transmit Control register, the DMA enters the Stop state.
8. The DMA can exit Suspend mode and enter the Run state (goes to step 1 or step 2 depending on pending status) only after receiving a Transmit Poll demand in DMA CH0 Transmit Descriptor Tail Pointer register.

Note: The DMA fetches the next descriptor before closing the current descriptor. Therefore, the descriptor ring length must be more than two. We recommends having a minimum descriptor length of four. In the OSP mode, all except the last descriptor is closed immediately. The last descriptor is closed after the packet is transmitted on the line. Therefore, to minimize the complexity, the transmission status and only the required control bits are updated in the pending last descriptor of the previous packet.

The Tx DMA transmission flow in OSP mode is shown in Figure 47-3.

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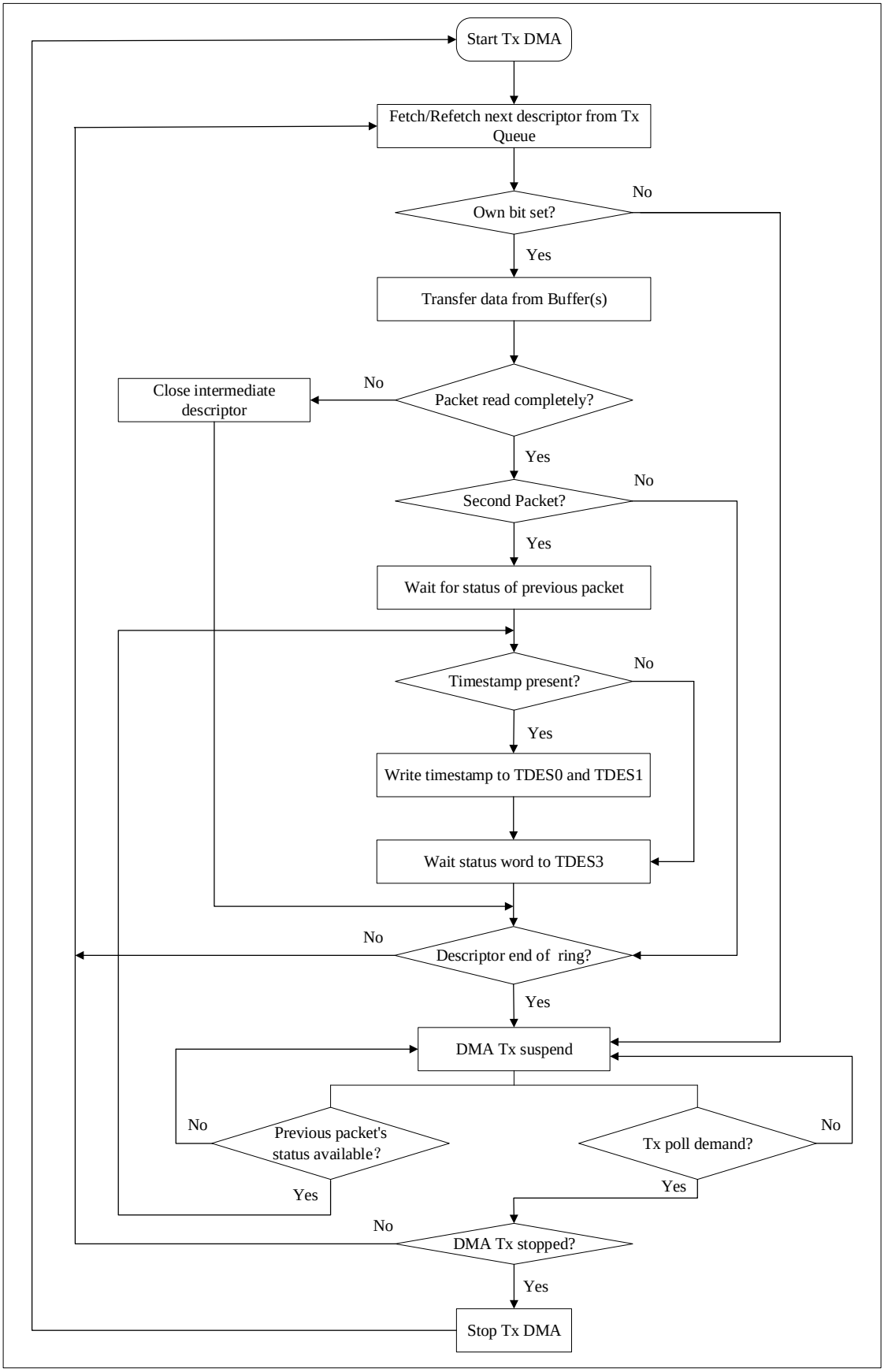
Figure 47-3 Tx DMA Operation in OSP Mode



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47.5.1.7 Transmit Packet Processing

The Tx DMA expects that the data buffers contain complete Ethernet packets, excluding preamble, pad bytes, and FCS fields. The DA, SA, and Type/Length fields contain valid data. If the Tx Descriptor indicates that the MAC must disable CRC or PAD insertion, the buffer must have complete Ethernet packets (excluding preamble), including the CRC bytes.

Packets can be data-chained and can span several buffers. Packets must be delimited by the FD (TDES3[29]) and the LD (TDES3 [28]). As transmission starts, the FD must have set. When this occurs, the packet data is transferred from the application buffer to the MTL Tx Queue. Concurrently, if the current packet has the LD clear, the Tx Process attempts to acquire the Next Descriptor. The Tx Process expects this descriptor to have FD clear. If LD is clear, it indicates an intermediary buffer. If LD is set, it indicates the last buffer of the packet.

After the last buffer of the packet has been transmitted, the DMA writes back the final status information to the Transmit Descriptor 3 (TDES3) word of the descriptor that has the LD Bit set in Transmit Descriptor 3 (TDES3[28]). At this time, if Interrupt on Completion (TDES2[31]) is set, bit 0 of DMA CH0 Status register is set, the Next Descriptor is fetched, and the process repeats. The actual packet transmission begins after either of the following:

- The MTL Tx Queue has reached a programmable Transmit threshold (Bits [6:4] of MTL Transmit Queue Operation Mode register)
- A full packet is contained in the FIFO

You can also use the store-and-forward mode (Bit 1 of MTL Transmit Operation Mode Register of a queue). In this mode, descriptors are released (Own bit TDES0[31] clears) when the DMA finishes transferring the packet.

Note: To ensure proper transmission of a packet and the next packet, you must specify a non-zero buffer size for the Transmit descriptor that has the Last Descriptor (TDES3[28]) set.

47.5.1.8 Transmit Polling Suspended

Transmit polling can be suspended by any of the following conditions:

- The DMA detects a descriptor owned by the application (TDES3[31]=0).

  To resume, the driver must give descriptor ownership to the DMA and then issue a Poll Demand command by writing the Tail Pointer register. If the DMA goes into SUSPEND state because of this condition, bit 15 and bit 2 of DMA CH0 Status register are set.

- A packet transmission is aborted when a Transmit error is detected because of underflow.

  The appropriate Transmit Descriptor 3 (TDES3) bit is set. When this condition occurs, the following bits are set and the information is written to TDES3, causing the suspension:

  – Bit 14 (Abnormal Interrupt Summary bit) of DMA CH0 Status register

  – Bit 0 (Transmit Queue Underflow bit) of MTL Queue Interrupt Control Status register

- The DMA detects that the Tail Pointer is equal to the Current descriptor closed by the it.

  To resume, the software driver must modify the Tail Pointer register.

In all conditions, the position in the Transmit List is retained. The retained position is that of the descriptor following the Last Descriptor closed by the DMA. The driver must explicitly issue a Transmit Poll Demand command after

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rectifying the suspension cause.

47.5.1.9 Receive Operation

In the Receive path, the DMA reads a packet from the MTL receive queue and writes it to the packet data buffers of the DMA channel. The Rx DMA engine operates as follows:

1. The application sets up the Rx descriptors (RDES0-RDES3) and the Own bit (RDES3[31]). The application must set the correct value in the DMA CH0 Receive Descriptor Tail Pointer register.
2. When Bit 0 of DMA CH0 Receive Control register is set, the DMA enters the Run state. The DMA looks for free descriptors based on the Rx Current Descriptor and Descriptor Tail Pointer register values. If there are no free descriptors, the DMA Channel enters the suspend state and goes to step 11.
3. The DMA fetches the next available descriptor in the ring and decodes the receive data buffer address from acquired descriptors.
4. If IEEE 1588 timestamping is enabled and the timestamp is available for the previous packet, the DMA writes the timestamp (if available) to the RDES0 and RDES1 of current descriptor and sets the CTXT field (RDES3[30]).
5. The DMA processes the incoming packets and places these in the data buffers of acquired descriptor.
6. If the current packet transfer is not complete, the DMA closes the current descriptor as intermediate and goes to step 10.
7. The DMA takes the status of the Receive frame from the MTL and writes the status word to current descriptor with the Own bit cleared and the Last Descriptor bit set.
8. The DMA writes the Frame Length to RDES3 and VLAN Tag to RDES0. The DMA also writes the MAC control frame opcode, OAM control frame code, and extended status information (if available) to RDES1 of the last descriptor.
9. If IEEE 1588 Timestamp feature is enabled, the DMA stores the timestamp (if available). The DMA writes the context descriptor after the last descriptor for the current packet (in the next available descriptor).
10. If more descriptors are available in the Rx DMA Descriptor Ring, go to step 3; otherwise, go to the Suspend state (step 11).
11. The Receive DMA exits the Suspend state when a Receive Poll demand is given and the application advances the Receive Tail Pointer register of a channel. The engine proceeds to step 2 and re-fetches the next descriptor.

Figure 47-4 shows the reception sequence for Rx DMA engine.

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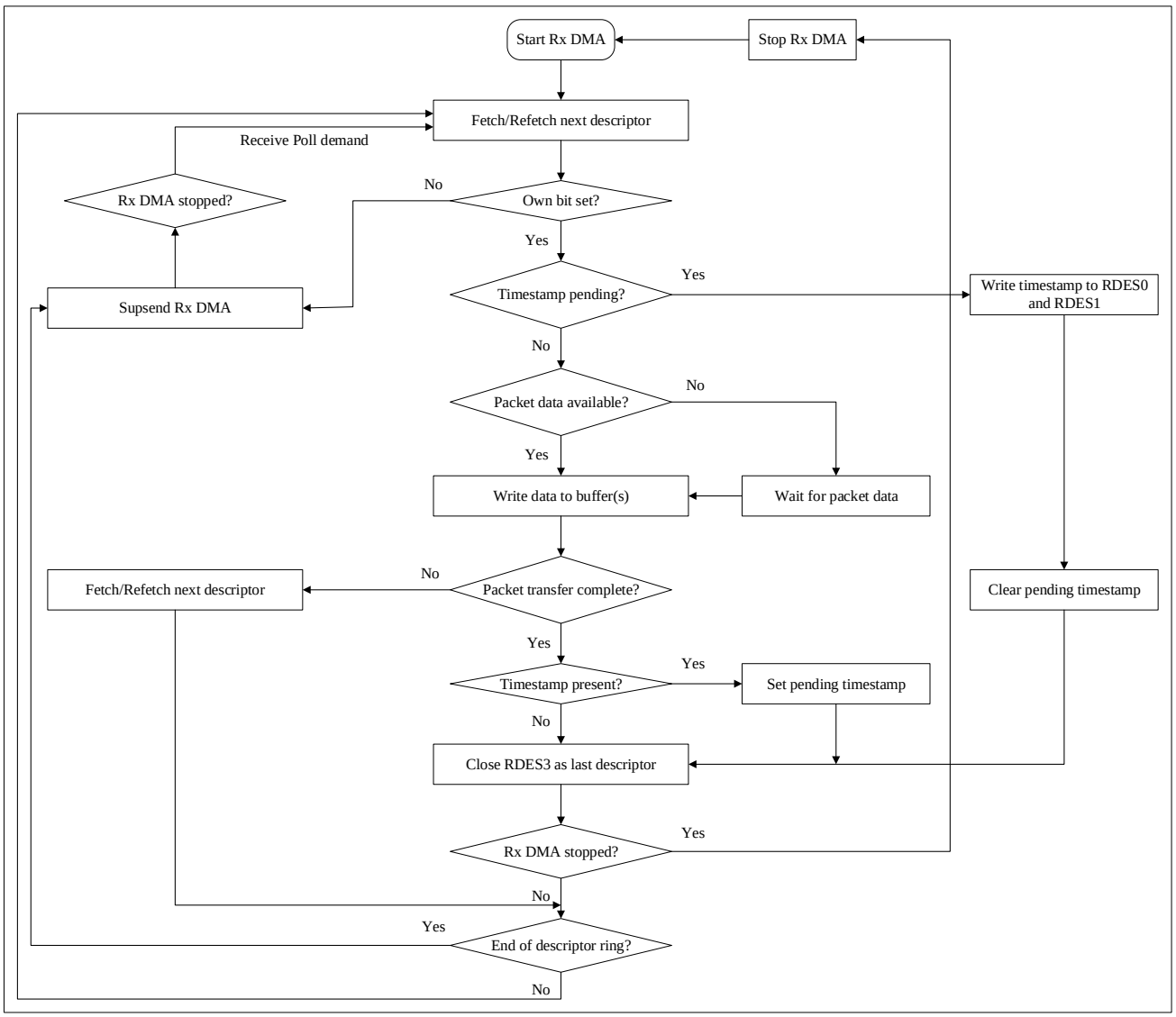
Figure 47-4 Rx DMA Operation



47.5.1.10 Receive Descriptor Acquisition

The Receive Engine always attempts to acquire an extra descriptor in anticipation of an incoming packet. Descriptor acquisition is attempted if any of the following conditions is satisfied:

- Bit 0 of DMA CH0 Receive Control register is set immediately after being placed in the Run state.
- The Descriptor Tail pointer register value is ahead of the Current Descriptor acquired by the Rx DMA.
- The controller has completed packet reception, but the current Receive Descriptor is not yet closed.
- A Receive poll demand is issued (update of the Tail Pointer register).

47.5.1.11 Receive Packet Processing

The sequence for processing a Receive packet is as follows:

1. The MAC transfers the received packets to the MTL memory only if the packet passes the address filter. If the packet fails the address filtering, it is dropped in the MAC block (unless Bit 31 of MAC Packet Filter register is

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set).

2. If packet size is greater than or equal to configurable threshold bytes set for Rx Queue of MTL, or when the complete packet is written to the queue in the store-and-forward mode, the MTL block requests the DMA block to begin transferring the packet data to the Receive Buffer pointed by the current descriptor.

   Packets smaller than 64 bytes, because of collision or premature termination, are removed from the MTL Receive Queue.

3. When the DMA application Interface (AHB or MDC) becomes ready, it transfers the data and sets the following:

   - If the packet fits in a single descriptor, the DMA sets both Last Descriptor (RDES3[28]) and First Descriptor (RDES3[29]).
   - If the packets fits into more than one descriptor, the DMA sets the First Descriptor (RDES3[29]) to delimit the packet.

4. The DMA releases the descriptors by resetting the Own (RDES3[31]) bit to 1'b0, either because the Receive buffer filled up or the last segment of the packet is transferred to the Receive buffer. The received packets status is updated in the last descriptor.

5. If Interrupt Enabled on Completion (RDES3[30]) bit is set in any of the Descriptors between the First and Last Descriptor of the Packet and Bit 6 of DMA CH0 Interrupt Enable register is set, the DMA sets Bit 6 of DMA CH0 Status register.

   The same process repeats unless the DMA encounters a descriptor flagged as being owned by the application or when there are no more descriptors in the ring. When the DMA finds a descriptor owned by the application and if Bit 7 of DMA CH0 Interrupt Enable register is set, the Receive Process sets Bit 7 of DMA CH0 Status register and then enters the Suspend state. The position in the receive list is retained.

47.5.1.12 Error Response to DMA

For any data transfer initiated by a DMA channel, if the slave replies with an error response, the DMA stops all operations and updates the error bits and the Fatal Bus Error bit in the DMA CH0 Status register. The application can either perform a reset to Ethernet peripheral or re-initialize the DMA descriptor list and start again.

47.5.2 MTL Function Description

Transmit Path: The application module drives all transactions related to the Transmit path through ATI. The internal DMA handles all transactions for the Transmit path through ATI. The application or internal DMA pushes the Ethernet packets read from the application or system memory into the queue. The packet is then popped out and transferred to the MAC when the queue threshold is reached (threshold mode) or complete packet is in the queue (store-and-forward mode). When EOP is transferred, the status of the transmission is taken from the MAC and transferred back to the application or internal DMA. The Tx queue has a default size of 2K bytes. The fill level of the queue is indicated to the application or internal DMA (using PBL and watermark) so that it can initiate a data fetch in required bursts from the application or system memory. The application or internal DMA indicates the SOP and EOP as packet delimiters through ATI interface.

Receive Path: The MTL Rx module receives the packets from the MAC and pushes them into the Rx Queue. The status (fill level) of the queue is indicated to the application or DMA when it crosses the configured Receive threshold

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(RTC bits [1:0] of MTL Rx Queue Operation Mode register), or the complete packet is received. The MTL also indicates the fill level of the queue so that the DMA can initiate preconfigured burst transfers towards the AHB interface.

47.5.2.1 Transmit Operation

The following two modes of operation trigger reading of the data towards the MAC:

- Threshold mode:

  In Threshold (or cut-through) mode, as soon as the number of bytes in the Queue cross the configured threshold level (or when the end of packet is written before the threshold is crossed), the data is ready to be popped out and forwarded to the MAC. The threshold level is configured by using the TTC bits of MTL Tx Queue Operation Mode register.

- Store-and-forward mode:

  In store-and-forward mode, the MTL pops out the packet towards the MAC only when one or more of the following conditions are true:

  – A complete packet is stored in the Queue

  – The Tx FIFO becomes almost full

  – The ATI watermark becomes low

  The watermark becomes low when the requested Queue does not have space to accommodate the requested burst length on the ATI. Therefore, the MTL when operating in the store-and-forward mode allows packet transmission even if the packet length is bigger than the Tx Queue size.

The application can flush complete content of the Tx Queue by setting Bit 0 (FTQ) of MTL Tx Queue Operation Mode register. This bit is self-clearing and initializes the Queue pointers to the default state. If the FTQ bit is set during a packet transfer from the MTL to the MAC, the MTL stops further transfer because the queue is considered to be empty. Therefore, an underflow event occurs at the MAC transmitter.

47.5.2.2 Single-Packet Transmit Operation

The following flow is valid when the core is operating in non-OSP mode, that is, when bit 4 (OSP) of the DMA CH0 Tx Control register is set to 0.

During a Transmit operation, the MTL block is a slave for the DMA controller. The general sequence of events for a Transmit operation is as follows:

1. If the system has data to be transferred, the DMA controller (if enabled) fetches the data from the application through the AHB and starts forwarding it to the MTL. The DMA descriptor memory contains the information related to packet control which is used to drive the ATI Control Word. The DMA data buffer memory contains the packet data.
2. The MTL pushes the data received from the DMA into the queue. This process continues until the EOP is transferred.
3. When the threshold level is crossed or a full packet of data is received into the queue, the MTL reads the packet data and drives it to the MAC.

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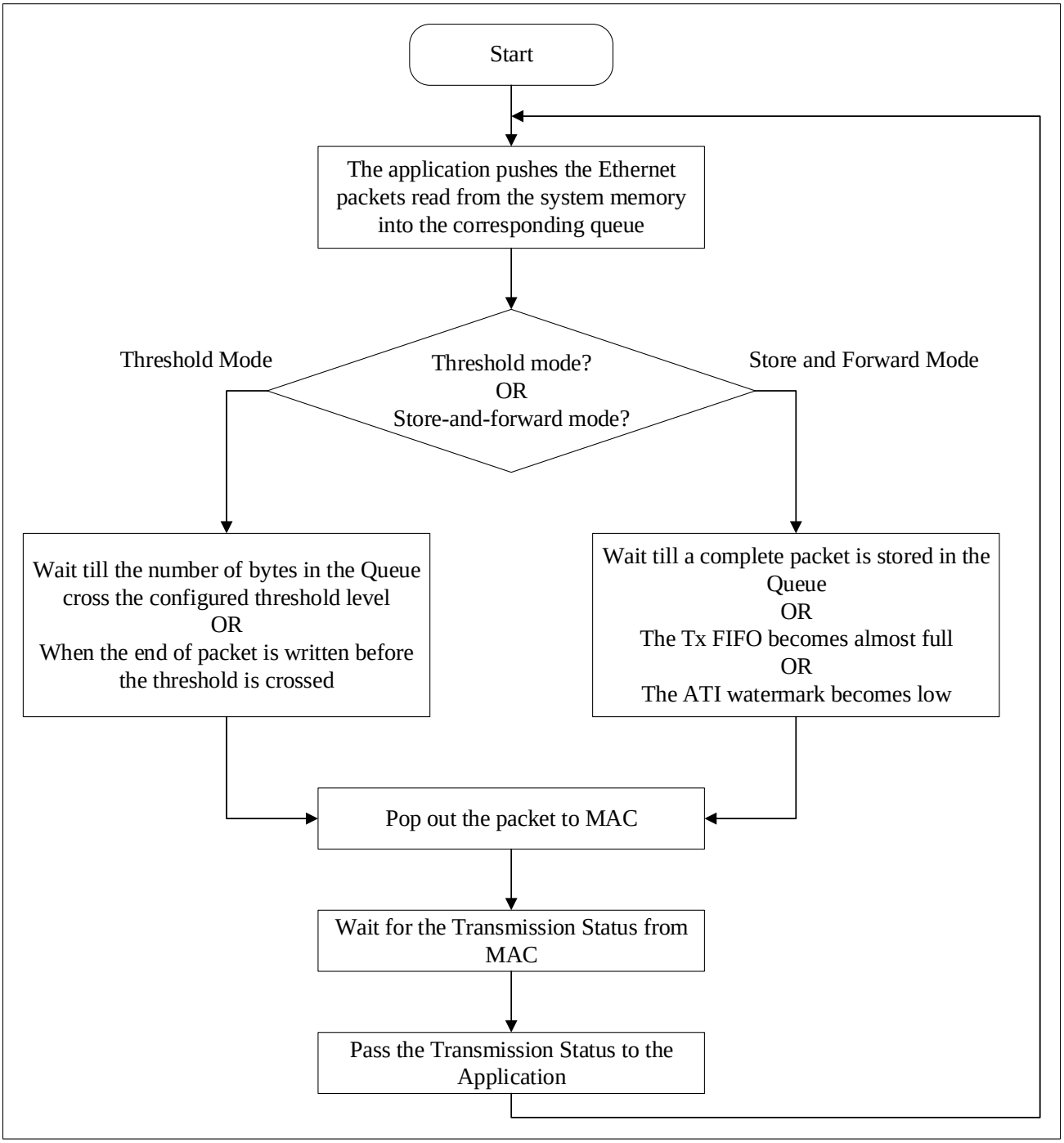
4. The queue controller continues to transfer data from the queue until a complete packet is transferred to the MAC.
5. When the packet transfer is complete, the MTL receives the status from the MAC and notifies the DMA controller.

Figure 47-5 shows the MTL single-packet transmit operation.

Figure 47-5 MTL Single Packet Transmit Flow



Note: When the Bit 1 (DTXSTS) of MTL Operation Mode register is set, the MTL does not provide any status to the DMA.

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Email: sales@nsing.com.sg

47.5.2.3 Two-Packets Transmit Operation

The following flow is valid when the core is operating in OSP mode, that is, when bit 4 (OSP) of the DMA CH0 Tx Control register is set to 1.

The flow is similar to the flow described in 47.5.2.2. However after fetching a packet DMA instead of waiting for the status, it continues to fetch another packet if available in the system memory. So, MTL can receive the second packet while it is processing the first packet. This flow improves the performance because the DMA can process two packets back to back before waiting for the status of the first packet.

47.5.2.4 Retransmission During Collision

While a packet is being transferred from the MTL to the MAC, a collision event can occur on the MAC line interface in half-duplex mode. The MAC indicates a Retry attempt to the MTL by giving the status even before the EOP is transferred from the MTL. The MTL then enables the retransmission by popping out the packet again from the queue.

After more than 96 bytes (or 548 bytes in 1000-Mbps mode) are read out towards the MAC, the Queue Controller frees up that space and makes it available to the application or the DMA to push in more data. This means that the retransmission is not possible after this threshold is crossed or when the MAC indicates a late-collision event.

When a packet transmission is aborted because of underflow and a collision event immediately follows (initiating a retry), retry has higher priority than abort.

47.5.2.5 Transmit Status Word

At the end of transfer of the Ethernet packet to the MAC and after the MAC completes the transmission of the packet, the MTL will provide the valid Transmit status. The detailed description of the Transmit Status is the same as for Bits [17:0] of TDES3 normal descriptor in write-back format, given in 47.5.15. If IEEE 1588 Timestamp feature is enabled, the MTL returns 64-bit timestamp of the packet, along with the Transmit status of ATI.

You can program Bit 1 (DTXSTS) of MTL Operation Mode register to disable the dependency of the application or DMA to read the status words from the status FIFO.

47.5.2.6 Receive Operation

During a Receive operation, the MTL is a slave for the MAC. The general sequence of events is as follows:

1. When the MAC receives a packet, it indicates the availability of receive data.
2. The MAC indicates the SOP and EOP delimiters.
3. The MTL accepts the data and pushes it into Rx queue.
4. After the EOP is transferred, the MAC drives the status word which is also pushed into the Rx queue by the MTL.

   Note: In Threshold (cut-through) mode, the status words are stored after the packet EOP. In store-and-forward mode, the location for the maximum status words are reserved before writing the SOP and the status is written to reserved locations after writing the EOP.
5. If IEEE 1588 timestamp feature is enabled and the 64-bit timestamp is available along with the packet status, it is pushed into the Rx queue as a part of the status word. Therefore, in 32-bit data bus mode, two additional locations are taken per packet to store the timestamp in the Rx queue.

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6. The MTL takes the data out of the queue and sends it to the DMA depending on the mode:

   - Threshold Mode

     In the (default) Threshold mode, the MTL reads the data and indicates its availability to the application or DMA when one of the following occurs:

     – Data bytes equal to the threshold amount are written to the Rx queue (RTC bits [1:0] of MTL Rx Queue Operation Mode register)

     – A full packet of data is received into the queue

   - Store-and-Forward Mode

     In the store-and-forward mode (when Bit 5 of MTL Rx Queue Operation Mode register is set to 1), the initial Rx queue locations are reserved for the status words before writing the SOP. A packet is read out only after it is completely written into the Rx queue. In this mode, all error packets are dropped (if configured through Bit 4 of MTL Rx Queue Operation Mode register) such that only valid packets are read and forwarded to the application.

47.5.2.7 Multi-Packet Receive Operation

In Threshold mode, the packet status is available immediately after the packet data. In store-and-forward mode, the packet data is available after the packet status. The MTL is capable of storing any number of packets into the queue as long as it is not full.

If the MAC receives a packet when the Rx queue is full, the MTL ignores that packet. In addition, the MTL increments the overflow counter in the MTL Rx Queue Missed Packet Overflow Cnt register.

47.5.2.8 Error Handling in Receive Operation

If the MTL Rx queue is full before it receives the EOP data from the MAC, the following happens:

1. An overflow is declared
2. The whole packet (including the status word) is dropped
3. The overflow counter in the DMA (Overflow Counter register of MTL queue) is incremented.

This is true even if Bit 4 (FEP) of MTL Rx Queue Operation Mode register is set.

If the start address of such a packet has already been transferred to the Read Controller, the rest of the packet is dropped and a dummy EOP is written to the queue along with the status word with overflow status. The status indicates a partial packet because of overflow. In such packets, the Packet Length field is invalid. If the MTL Receive Queue is configured to operate in the store-and-forward mode and the length of the received packet is more than the queue size, overflow occurs and all such packets are dropped.

The MTL Rx Control logic can filter error and undersized packets, if enabled by using the FEP and FUP bits of MTL Rx Queue Operation Mode register. If the start address of such a packet has already been transferred to the Rx Queue Read Controller, that packet is not filtered. The start address of the packet is transferred to the Read Controller after the packet crosses the receive threshold set by Bits [1:0] of MTL Rx Queue Operation Mode register.

If the MTL Receive Queue is configured to operate in the store-and-forward mode, all error packets can be filtered and dropped. The MTL then stops transferring data to the application (DMA). It internally reads the rest of the packet

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

and drops it. The MTL then starts the transfer of next packet (if available).

47.5.2.9 Receive Status Word Format

The Rx packet status words are sent to the application after the packet data in Threshold mode and before the packet data in the Store and Forward Mode as explained in 47.5.2.7. The detailed description of the Receive Status is the same as the normal descriptor write-back format of RDES3. For specific information, please refer to 47.5.15 section.

47.5.3 MAC Function Description

47.5.3.1 MAC Transmission

The MAC transmission process is as follows:

1. Transmission is initiated when the MTL application pushes in data with the SOP signal asserted.
2. When the SOP signal is detected, the MAC accepts the data and begins transmitting to the GMII or MII. The time required to transmit the packet data to the GMII or MII after the application initiates the transmission depends on delay factors such as IPG delay, time to transmit preamble or SFD, and any back-off delays for half-duplex mode. While the packets data is being transmitted, the MAC can stop accepting the data received from the MTL.
3. After the EOP is transferred to the MAC, the MAC does one of the following:
   - The MAC completes the normal transmission and gives the transmission status to the MTL.
   - If a normal collision (in half-duplex mode) occurs during transmission, the MAC gives the Transmit Status with retry bit set to the MTL. The MAC gives the Retry request till one of the following is true:
     - Packet is successfully transmitted
     - Maximum retry requests expire

     When maximum retry requests expire, the MAC aborts the packet transmission with Excessive Collision Transmit Status. The MAC accepts and drops all further data until the next SOP is received. The MTL block should retransmit the same packet from SOP on observing a Retry request (in the Status) from the MAC.
   - If any one of the following occurs, the MAC aborts the packet transmission:
     - No carrier (half-duplex mode)
     - Loss of carrier (half-duplex mode)
     - Excessive deferral (half-duplex mode)
     - Late collisions (half-duplex mode)
     - Jabber

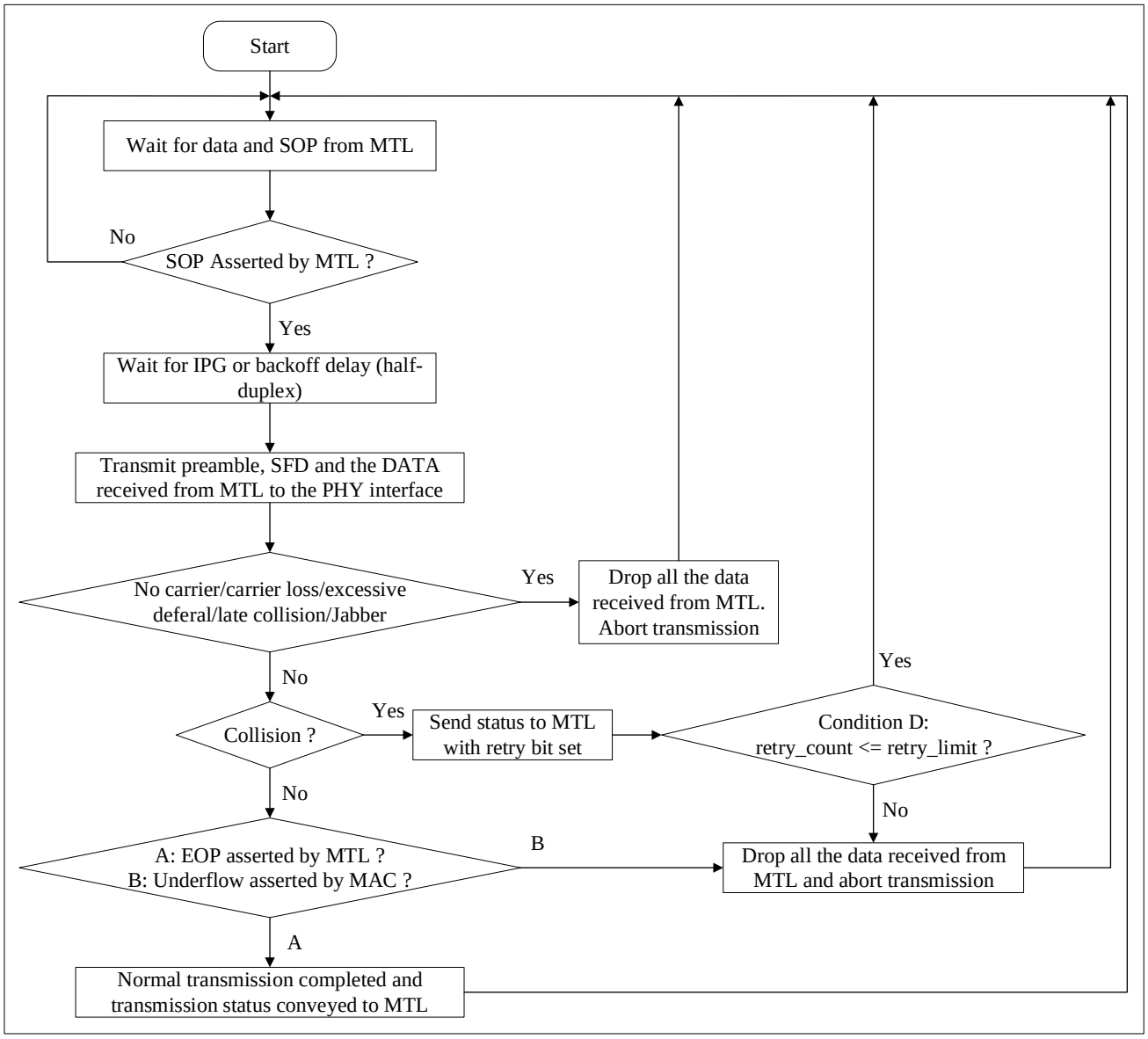
     The MAC accepts and drops all further data until the next SOP is received.
4. The MAC issues an underflow status if the MTL is not able to provide the data continuously during the transmission. The MAC accepts and drops all further data until the next SOP is received.
5. During the normal transfer of a packet from MTL, if the MAC receives a SOP without getting an EOP for the

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

previous packet, it ignores the SOP and considers the new packet as continuation of the previous packet.

Figure 47-6 illustrates the MAC transmission process flow.

Figure 47-6 MAC Transmission Process Flow



47.5.3.2 Transmit Bus Interface Unit Module

The MAC Transmit Bus Interface Unit (TBU) accepts data in 32-bit wide bus and runs on the Tx clock of GMII interface.

The TBU module connects the Transmit path of the MAC with an external packet through a FIFO interface.

The TBU module performs the following functions:

- Outputs the (32-bit) Transmit status to the application at the end of normal transmission or collision
- Outputs the Transmit snapshot register value to the MTI timestamp output signal and asserts the MTI status valid signal

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- Performs the Endian conversion of data bus by swapping the byte lanes and corresponding byte enables
- Converts the input data into an 8-bit bus towards the Transmit Packet Controller

47.5.3.3 Transmit Packet Controller Module

The Transmit Packet Controller (TPC) module consists of eight registers to hold the data and the last data control received from the TBU.

The register provides a buffer between the application and the Transmit Protocol Engine (TPE) to regulate data flow.

When the number of bytes received from the application are less than 60 (DA+SA+LT+DATA), the state machine that interfaces with TBU automatically appends zeros to the packet being transmitted. This is done to make the data length exactly 46 bytes to meet the minimum data field requirement of IEEE 802.3.

The cyclic redundancy check (CRC) for the Frame Check Sequence (FCS) field is calculated before transmission to the TPE module. This value is computed by the CTX module. The TPC module receives the computed CRC and appends it to the data being transmitted to the TPE module. When the MAC is programmed (through sideband signal (mti_crc_pad_ctrl_i) from the application interface) to not append the CRC value to the end of Ethernet packets, the TPC module ignores the computed CRC and transmits only the data received from the TBU module to the TPE module. An exception to this rule is that when the MAC is programmed to append pads for packets (DA+SA+LT+DATA) less than 60 bytes sent by the TBU module, the TPC module appends the CRC at the end of padded packet irrespective of the value on the mti_crc_pad_ctrl_i signal.

47.5.3.4 Transmit Protocol Engine Module

The Transmit Protocol Engine (TPE) module consists of a Transmit State Machine that controls the operation of Ethernet packet transmission.

The Transmit State Machine of this module contains the following features to meet the IEEE 802.3/802.3z specification:

- Generates preamble and SFD
- Generates JAM pattern in the half-duplex mode after normal collision
- Generates carrier extension in the half-duplex (only in the GMII) mode when packet is smaller than 512 bytes
- Supports packet bursting in the half-duplex (only in the GMII) mode
- Supports jabber timeout
- Supports flow control for the half-duplex mode (backpressure)
- Generates Transmit packet status
- Contains timestamp snapshot logic for IEEE 1588 support

When the TPC module requests the TPE module for a new packet transmission, the Transmit State Machine sends out the preamble and SFD, followed by the data received. The preamble is defined as 7 bytes of 8'b10101010 pattern and the SFD is defined as 1 byte of 8b'10101011 pattern.

The collision window is defined as 1 slot time (512-bit times for 10/100 Mbps Ethernet and 4,096 bit times for 1,000 Mbps Ethernet). The JAM pattern generation is applicable only to half-duplex mode, not to full duplex mode. In full-duplex mode, the Transmit State Machine ignores the collision input signal from the PHY.

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Email: sales@nsing.com.sg

In MII mode, if a collision occurs any time from the beginning of the packet to the end of the CRC field, the Transmit State Machine sends a 32-bit JAM pattern of 32'h55555555 on MII to inform all other stations that a collision has occurred. If the collision is seen during the preamble transmission phase, the Transmit state machine completes the transmission of preamble and SFD, and then sends the JAM pattern.

In GMII mode, if a collision occurs any time between the beginning of the packet and the end of the extension field, the Transmit State Machine sends a 32-bit JAM pattern of 32'h55555555 on GMII to inform all other stations of the collision. If the collision is seen during the preamble transmission phase, the Transmit State Machine completes the transmission of preamble and SFD, and then sends the JAM pattern. If a collision occurs during the extension field, the Transmit State Machine sends a 32-bit JAM pattern of 32'h1F1F1F1F.

If the collision occurs after the collision window and before the end of the FCS field (or the end of Burst if the Packet Burst mode is enabled), the Transmit State Machine sends a 32-bit JAM pattern and sets the late collision bit in the Transmit packet status.

Note: At the GMII or MII interface, the collision signal (phy_col_i) being asynchronous is checked by the transmitter after it is double-synchronized to clk_tx domain. This additional latency delays the recognition of collision or late-collision event. When the output of phy_col_i synchronizer is asserted after the complete packet is transmitted, it is not recognized as collision even if the COL signal is high at the GMII interface before the end of transmission. Similarly, an assertion of COL signal at the GMII input at the last byte of normal collision window might be identified as late collision because of the synchronizer delay.

In GMII half-duplex mode (1000 Mbps), the Transmit State Machine ensures that all valid carrier events exceed a slot time of 4,096 bit times. To accomplish this, any Transmit packet shorter than 512 bytes from the TFC module is extended using a carrier extension. On GMII, this is signaled to the PHY by asserting TX_ER, de-asserting TX_EN, and setting TXD[7:0] to 8h'0F.

When the Packet Burst mode is enabled, only the first packet of the burst is carrier extended if it is shorter than 512 bytes. The carrier extension is not applicable for MII half-duplex and GMII or MII full-duplex modes. When the Packet Burst mode is enabled, the Transmit State Machine transmits a burst of packets (as long as packets are available from the TFC module) without releasing the carrier of the PHY. To accomplish this, the state machine inserts the carrier extension for a minimum IPG period (96 bit times) between the packets. The Transmit State Machine continues to burst packets as long as additional packets are available from the TPC module and a burst limit of 8,192 byte times has not been exceeded. If an additional packet is not available at the end of the IPG period in the middle of the burst, the Transmit State Machine releases the carrier by de-asserting the TX_ER and TX_EN signals on GMII.

Packet bursting is applicable only for the GMII half-duplex mode. It is not applicable in the MII and GMII full-duplex modes. In the GMII half-duplex mode, the size of the first packet in a packet burst should at least be equal to the slot time. If the first packet (including carrier extension) is less than the slot time, the MAC considers all data bytes, received for the first packet and subsequent packets, which end immediately after the slot time is reached as first packet in the burst. This may result in CRC error. However, if the packet burst ends (both RX_DV and RX_ER go low) before the slot time, the subsequent packet is considered as a new packet. This behavior is according the IEEE 802.3.

The TPE module maintains a jabber timer to stop the transmission of Ethernet packets if the TFC module transfers more than 2,048 (default) bytes. The timeout is changed to 10,240 bytes when the Jumbo packet is enabled.

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Email: sales@nsing.com.sg

The Transmit State Machine uses the deferral mechanism for flow control (backpressure) in the half-duplex mode. When the application requests to stop receiving packets, the Transmit State Machine sends a JAM pattern of (8'h55) 32 bytes whenever it senses a reception of a packet, provided the Transmit flow control is enabled. This results in a collision and the remote station backs off. The application requests the flow control by setting BPA bit of the Tx Flow Control register. If the application requests a packet to be transmitted, it is scheduled and transmitted even when the backpressure is activated. If the backpressure is kept activated for a long time (and more than 16 consecutive collision events occur), the remote stations abort their transmissions because of excessive collisions.

If IEEE 1588 timestamp is enabled for the Transmit packet, this block takes a snapshot of the system time when the SFD is put onto the Transmit GMII or MII bus. The system time source is either an external input or it is internally generated according to the configuration selected.

Note: The Collision input is an asynchronous signal and should be asserted for at least 32-bit times (4 clocks for 1Gbps, and 8 clocks for slower speeds).

47.5.3.5 Transmit Scheduling Module

The Scheduling of Transmit (STX) module is responsible for scheduling the packet transmission on GMII or MII. It provides an enable signal to the TPE module after satisfying the IPG and back-off delays. The STX module performs the following functions:

- Maintains the inter-packet gap between two transmitted packets

  The STX module maintains an idle period of the configured inter-packet gap (IPG bits of MAC Configuration register) between any two transmitted packets. If packets from the TPC arrive at the TPE module sooner than the configured IPG time, the TPE module waits for the enable signal from the STX module before starting the transmission on GMII or MII. The STX module starts its IPG counter as soon as the carrier signal of GMII or MII goes inactive. At the end of programmed IPG value, the module issues an enable signal to the TPE module in the full-duplex mode.

  In the half-duplex mode and when IPG is configured for 96-bit times, the STX module follows the rule of deference specified in the IEEE 802.3, Section 4.2.3.2.1. The module resets its IPG counter if a carrier is detected during the first two-thirds (64-bit times for all IPG values) of the IPG interval. If the carrier is detected during the final one-third of the IPG interval, the STX module continues the IPG count and enables the transmitter after the IPG interval.

- Implements the Truncated Binary Exponential Back-off algorithm

  The STX module implements the Truncated Binary Exponential Back-off algorithm when it operates in the half-duplex mode.

47.5.3.6 Transmit CRC Module

The MAC Transmit CRC Generator (CTX) module interfaces with the TFC module to generate CRC for the FCS field of the Ethernet packet.

The CTX module interfaces with the TFC module to generate CRC for the FCS field of the Ethernet packet.

The TPC module sends the packet data and any necessary padding to the CTX module through an 8-bit interface.

The CTX module calculates the 32-bit CRC for the FCS field of the Ethernet packet. The encoding is defined by the following generating polynomial:

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$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

The CTX module gets the byte data of Ethernet packet from the TPC module (DA + SA + LT + DATA + PAD) qualified with a Data Valid signal. The TPC also indicates to the CTX when to reset the previously calculated CRC and to start the new CRC calculation for the coming packet. The TPC module issues the start command before sending the new packet data for calculation. The calculated CRC is valid on the next clock after the data is received.

In GMII mode, the Data Valid signal is valid for every clock, from the first data byte through the last data byte. In MII mode, this signal is valid every alternate clock.

47.5.3.7 Transmit Flow Control Module

The Transmit Flow Control (FTX) module generates and transmits the Pause packets to the TFC module based on the flow control triggers in full-duplex mode (backpressure in half-duplex mode). The TFC module receives the Pause packet from the FTX module, appends the calculated CRC, and sends the packet to the TPE module.

Flow Control in Full-Duplex Mode

In full-duplex mode, the Ethernet peripheral uses IEEE 802.3x Pause packets for flow control. Table 47-5 describes the fields of a Pause packet.

Table 47-5 Pause Packet Fields

Field	Description
DA	Contains the special multicast address
SA	Contains the MAC address 0
Type	0x8808
MAC Control opcode	Contains 0001 for IEEE 802.3x Pause Control packets
PT	Contains Pause time specified in the PT field of the MAC Tx Flow Control register

When the FCB bit is set, the MAC generates and transmits a single Pause packet. If the FCB bit is set again after the Pause packet transmission is complete, the MAC sends another Pause packet irrespective of whether the pause time is complete or not. To extend the pause or terminate the pause prior to the time specified in the previously-transmitted Pause packet, the application should program the Pause Time register with appropriate value and then again set the FCB bit.

If the DZPQ bit in MAC Tx Flow Control register is set to 0, the MAC transmits a Pause packet with zero Pause time to indicate to the remote end that the Receive buffer is ready to receive new data packets.

Flow Control in Half-Duplex Mode

In half-duplex mode, the MAC uses the deferral mechanism for the flow control (backpressure). When the application requests to stop receiving packets, the MAC sends a JAM pattern of 32 bytes when it senses a packet reception, provided the transmit flow control is enabled. This results in a collision and the remote station backs off. If the application requests a packet to be transmitted, it is scheduled and transmitted even when the backpressure is activated. If the backpressure is kept activated for a long time (and more than 16 consecutive collision events occur), the remote stations abort the transmission because of excessive collisions.

Table 47-6 describes the flow control in the Tx path for Queue 0 based on the setting of the following bits:

- TFE bit of MAC Tx Flow Control register

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Email: sales@nsing.com.sg

- DM bit of MAC Configuration register

Table 47-6 Tx MAC Flow Control

TFE	DM	Description
0	x	The MAC transmitter does not perform the flow control or backpressure operation.
1	0	The MAC transmitter performs back-pressure when Bit 0 of MAC Tx Flow Control register is set.
1	1	The MAC transmitter sends the Pause packet when Bit 0 of MAC Tx Flow Control register is set.

47.5.3.8 MAC Reception

A receive operation is initiated when the MAC detects an SFD on GMII or MII. The MAC strips the preamble and SFD before proceeding to process the packet. The header fields are checked for filtering and the FCS field used to verify the CRC for the packet. The received packet is stored in a shallow buffer until the address filtering is performed. The packet is dropped in the MAC if it fails the address filter.

47.5.3.9 Receive Protocol Engine Module

The Receive Protocol Engine (RPE) consists of the Receive State Machine which strips the preamble, SFD, and carrier extension of the received Ethernet packet (in half-duplex 1000-Mbps mode).

The sequence is as follows:

1. When the RX_DV signal of GMII or MII becomes active, the Receive State Machine of RPE starts looking for the SFD field (byte 0x5D in GMII mode; 0xD nibble in MII mode).

   The state machine drops received packets until it detects SFD.

2. When SFD is detected, the state machine begins sending the data of Ethernet packet to the RPC module, beginning with the first byte following the SFD (destination address).

3. If IEEE 1588 Timestamp feature is enabled, the RPE takes a snapshot of the system time at which SFD of any packet is detected on GMII or MII. If this packet is not dropped during MAC filtering, the timestamp is passed to the application. In MII mode, the RPE converts the received nibble data into bytes and forwards the valid packet data to the RFC module.

4. The Receive State Machine of the RPE module decodes the Length/Type field of the receiving Ethernet packet.

   If the Length/Type field is less than 1,536 and if the MAC is programmed for the Auto CRC/Pad Stripping (Bit 20 of the MAC Configuration register), the state machine sends the data of the packet up to the count specified in the Length/Type field and starts dropping bytes (including the FCS field). The state machine of the RPE module decodes the Length/Type field and checks for the Length interpretation.

   If the Length/Type field is greater than or equal to 1,536, the RPE module sends all received Ethernet packet data to the RFC module if you have not enabled the CRC stripping for Type packet in Bit 21 of the MAC Configuration register. However, if you have enabled the CRC stripping for Type packets and not enabled the Receive Checksum Offload Engine, the MAC strips and drops the last 4 bytes of all packets of Ether type before forwarding the packets to the application.

5. By default, the MAC is programmed for watchdog timer to be enabled, that is, packets larger than 2,048 (10,240 if Jumbo Packet is enabled) bytes, (DA + SA + LT + DATA + PAD + FCS) are cut off at the RPE module. In addition, you can use a programmable watchdog timer (Bit 16 of MAC Watchdog Timeout register) to override

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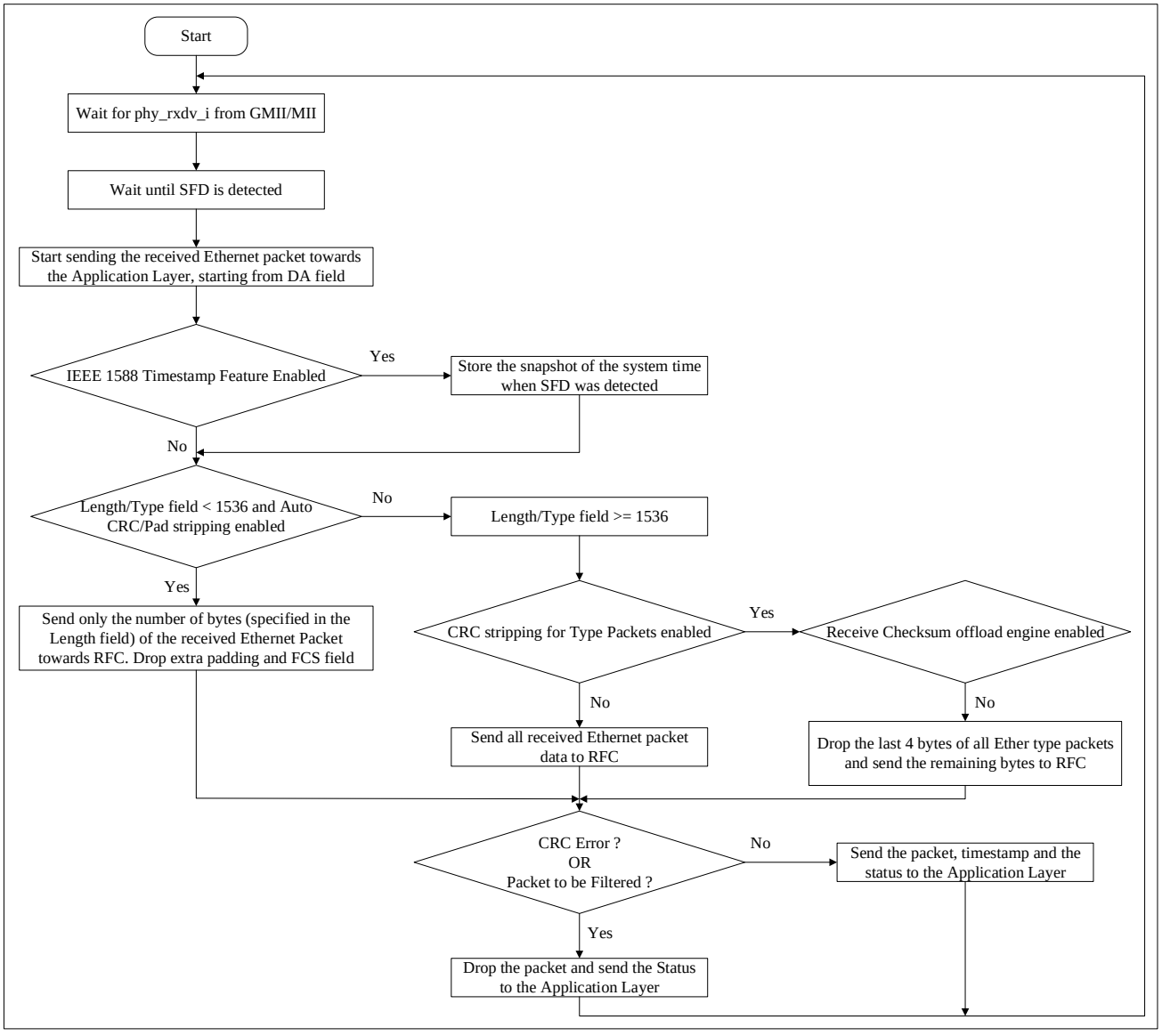
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

the fixed timeout of 2,048 or 10,240 bytes. You can disable the watchdog timer by programming Bit 19 of MAC Configuration register. However, even if the watchdog timer is disabled, a packet greater than 32 KB size is cut off and a watchdog timeout status is given.

At the end of every received packet, the RPE module generates received packet status and sends it to the RPC module. Control, missed packet, and filter fail status are added to the receive status in the RPC module.

Figure 47-7 shows the Receive transmission flow in the RPE.

Figure 47-7 MAC Receive flow



47.5.3.10 Receive CRC Module

The MAC Receive CRC (CRX) interfaces with the RPE module to check any CRC error in the packet being received.

This module calculates the 32-bit CRC for received packet that includes the Destination address field through the FCS field.

The encoding is defined by the following generating polynomial:

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Email: sales@nsing.com.sg

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

The module gets the data from the RPE module (DA+SA+LT+DATA+PAD+FCS). The RPE module also sends a control signal that indicates the validity of the data. Irrespective of the Auto Pad or CRC strip, the CRX module receives the entire packet to compute the CRC check for received packet.

47.5.3.11 Receive Packet Controller Module

The MAC Receive Packet Controller (RPC) receives the Ethernet packet data and status from the RPE module.

The RPC module consists of a FIFO of parameterized depth (default set to 4 deep and 33-bits wide) and two state machines for writing and reading the FIFO. The FIFO holds the received Ethernet packet data and byte enables, along with a control bit to indicate the last data. The state machines manage the FIFO and provide a packet buffering for the Ethernet packet being received from the RPE module. The following are main functions of the RPC module:

- Converting Data path: converts 8-bit data to 32-bit data to the RBU module
- Packet filtering
- Attaching the calculated IP Checksum input from IPC
- Updating the Receive Status and forwarding it to RBU

If RA bit of the MAC Packet Filter register is set, the RPC module initiates the data transfer to the RBU module when 4 bytes of Ethernet data are received from the RPE module. At the end of the data transfer, the RPC module sends out the received packet status that includes the packet filter bits (SA Filterfail and DA Filterfail) and status from the RPC module. These bits are generated based on the filter-fail signals from the AFM module. This status bit indicates to the application whether the received packet has passed the filter controls (both address filter and Packet Filter controls from CSR). The RPC module does not drop any packet on its own in this mode.

If the RA bit is reset, the RPC module performs packet filtering based on the destination or source address. If the application does not want to receive any bad packets such as runt, CRC error packets, the application still needs to perform another level of filtering. The RPC module waits to receive the first 14 bytes of received data (type field) from the RPE module. Until then, the module does not initiate any transfers to the RBU module. After receiving the destination or source address bytes, the RPC checks the filter-fail signal from the AFM module for an address match. On detecting filter-fail from AFB, the packet is dropped at the RPC module and not transferred to the application.

On a delayed filter response from the AFM (this can only occur if you change the AFM logic), the RPC module waits until the FIFO is full, and then proceeds with the packet transfer to the RBU module. However, the RPC module still takes the delayed response from the AFM module and if it is a (DA or SA) filter failure, it drops the rest of the packet and sends the Rx Status Word (with zero packet-length, CRC Error and Runt Error bits set) immediately indicating the filter fail. If there is no response from the AFM until EOP is transmitted, the filter fail status in the Rx Status Word is updated accordingly.

When the optional PMT module is present and configured for power-down mode, this block drops all received packets and does not forward the packets to the application.

47.5.3.12 Receive Flow Control Module

The Receive Flow Controller (FRX) detects the Pause packet being received and pauses the packet transmission for the delay specified within the received Pause packet. The FRX module is enabled only in the full-duplex mode. If any Pause packet is received in the half-duplex mode, the packet is considered as a normal control packet.

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Note: Receive pause packets should have a frame size of 64 bytes.

Table 47-7 describes the flow control in the Rx path based on the setting of the following bits:

- RFE bit of MAC Rx Flow Control register
- DM bit of MAC Configuration register

Table 47-7 Rx MAC Flow Control

RFE	DM	Description
0	x	The MAC receiver does not detect the received Pause packets.
1	0	The MAC receiver does not detect the received Pause packets but recognizes such packets as Control packets.
1	1	The MAC receiver detects or processes the Pause packets and responds to such packets by stopping the MAC transmitter.

The following list describes the Rx flow control:

1. The MAC checks the destination address of the received Pause packet for either of the following:
   - Multicast destination address: The DA matches the unique multicast address specified for the control packet (48'h0180C2000001).
   - Unicast destination address: The DA matches the content of the MAC Address Register 0 and the UP bit of MAC Rx Flow Control register is set.

     If the UP bit is set and the MAC processes Pause packets with unicast destination address in addition to the unique multicast address.
2. The MAC decodes the following fields of the received packet:
   - Type field: This field is checked for 16'h8808.
   - Opcode field: This field is checked for 16'h0001 (Pause packet).
   - Pause Time field: The Pause time (for Pause packet) is captured to determine the time for which transmitter needs to be blocked.
3. If the byte count of the status indicates 64 bytes and there is no CRC error, the MAC transmitter does one of the following:
   - For 802.3x Pause packets, the MAC pauses the transmission of any data packet for the duration of the decoded Pause Time value multiplied by the slot time (64 byte times).
4. The MAC transfers the received control packet to the application based on the setting of the PCF field in MAC Packet Filter register.

47.5.3.13 Receive Bus Interface Unit Module

The Receive Bus Interface Unit (RBU) converts the 32-bit data received from the RPC module into a 32-bit FIFO protocol on the Application side. The RBU module interfaces with the application through the MAC receive interface (MRI).

If IEEE 1588 Timestamp feature is enabled, the RBU module also outputs the timestamp captured from the received

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packet, along with the status.

47.5.3.14 Address Filtering Module

The Address Filtering (AFM) module performs the destination and source address checking function on all received packets and reports the address filtering status to the RPC module.

The address checking is done based on different parameters (Packet Filter register) chosen by the application. These parameters are inputs to the AFM module as control signals, and the AFM module reports the status of the address filtering based on the combination of these inputs. The AFM module does not filter the receive packets but reports the status of the address filtering (whether to drop the packet or not) to the RFC module. The AFM module also reports address filter status and whether the received packet is a multicast packet or a broadcast packet.

The AFM module probes the 8-bit receive data path between the RPE module and the RFC module and checks the destination and source address field of each incoming packet. In GMII mode, the module takes 8/14 clocks (from the start of packet) to compare the destination/source address of the packet being received. Similarly, in MII mode, the module takes 14/26 clocks (from the start of packet) to compare the destination or source address of the receiving packet. The AFM module gets the physical (MAC) address of the station and the Multicast Hash table from CSR module for address checking. The CSR module provides the Packet Filter register parameters to AFM.

For other filter-related features, please refer to 47.5.5 section.

47.5.3.15 Double VLAN Processing

Ethernet peripheral supports two VLAN tags, namely inner and outer, for processing double VLANs. With this feature, the Ethernet peripheral supports the following:

- Insertion, replacement, or deletion of up to two VLAN tags in the Transmit path.
- Packet filtering and stripping based on any one of the two VLAN Tags in the Receive path. Stripping and providing up to two VLAN Tags in the Receive path as a part of the Receive status.

Transmit Path:

Table 47-8 describes the features supported by the MAC on the Transmit side.

Table 47-8 Double VLAN Processing Features in Transmit Path

Feature	Description
Support for C-VLAN and S-VLAN Tag types	The inner or outer VLAN tag can be of C-VLAN and S-VLAN type. The VLAN type is specified through the CSVL bit of MAC VLAN Incl and MAC Inner VLAN Incl registers. The Ethernet peripheral supports processing of any sequence of outer and inner VLAN tags. *Note: The Ethernet peripheral does not support the C-VLAN S-VLAN sequence.* The MAC does not check whether the packet provided by the application has a valid sequence of the VLAN Tag types or the insertion or replacement operation results in invalid sequence of VLAN Tag type. Therefore, the application must provide correct sequence of VLAN Tag types and program the MAC in such a way that it results in correct sequence of VLAN Tag types in the transmitted packet. The application must ensure the following: ■ The inner tag should not be S-VLAN when outer C-VLAN Tag insertion is enabled. ■ The outer tag should not be C-VLAN when inner S-VLAN Tag insertion is enabled. ■ The inner tag should not be S-VLAN when outer tag should be replaced with C-VLAN.

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Feature	Description
	■ The outer tag should not be C-VLAN when inner tag should be replaced with S-VLAN.
VLAN Tag deletion	You can enable the VLAN tag deletion for outer or inner tag through VLC field in the MAC VLAN Incl or MAC Inner VLAN Incl register, respectively. When VLAN deletion is enabled, the MAC deletes the tag present at the corresponding position. When a packet has only one tag, it is considered as the outer tag. If inner tag deletion is enabled and the packet has only one tag, the MAC does not delete the tag.
VLAN Tag Insertion or Replacement	You can enable the VLAN tag insertion or replacement for outer or inner tag through VLC field in the MAC VLAN Incl or MAC Inner VLAN_Incl register, respectively. When VLAN tag insertion or replacement is enabled, the VLTI bit in the MAC VLAN Incl or MAC Inner VLAN Incl register is used to determine whether the VLAN tag should be taken from the register or the Control Word.

Receive Path:

Table 47-9 describes the features supported by the MAC on the Receive side and the corresponding bits in the MAC VLAN Tag register.

Table 47-9 Double VLAN Processing in Receive Path

Feature	Description
Outer or inner VLAN tag-based filtering	The MAC can filter packets based on the outer or inner VLAN tag through the ERIVLT bit.
C-VLAN or S-VLAN tag-based filtering	The MAC can filter packets based on the C-VLAN or S-VLAN type based on the ERSVLM bit.
Outer and Inner VLAN Tag stripping	The MAC can strip the outer and inner VLAN Tags from received frame based on the EVLS and EIVLS bits.
16-bit outer and inner VLAN Tag and Type in Rx status	The MAC can provide the 16-bit outer and inner VLAN Tag and Type in the Rx status based on the EVLRXS and EIVLRXS bits, respectively.
Disabling or skipping checking of outer VLAN Tag type	The MAC can disable or skip checking of outer VLAN Tag type to match C-VLAN or S-VLAN based on the DOVLTC bit.

47.5.3.16 SA and VLAN Insertion, Replacement, or Deletion

The source address (SA) and VLAN fields are Tx packet-related control information that are provided as part of the control word through ATI interfaces. Ethernet peripheral supports the feature to insert or replace the source address based on the information in the MAC Address Registers, and also the feature to insert, replace or delete the VLAN fields (VLAN Type and VLAN Tag) based on the setting of the VLTI bit in the MAC VLAN Incl register. You can enable the SA insertion or replacement feature for all Transmit packets or selective packets. Similarly, you can enable the VLAN insertion, replacement, or deletion feature for all Tx packets or selective packets.

SA Insertion or Replacement:

The software can use the SA insertion or replacement feature to instruct the MAC to do the following for Tx packets:

- Insert the content of the MAC Address Registers in the SA field
- Replace the content of the SA field with the content of the MAC Address Registers

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When SA insertion is enabled, the application must ensure that the packets sent to the MAC do not have the SA field. The MAC does not check whether the SA field is present in the Transmit packet and it inserts the content of MAC Address Registers in the SA field. Similarly, when SA replacement is enabled, the application must ensure that the SA field is present in the packets sent to the MAC. The MAC replaces the six bytes following the Destination Address field in the Transmit packet with the content of the MAC Address Registers.

You can enable the SA insertion or replacement feature for all Transmit packets or selective packets:

- Enabling SA insertion or replacement for all packets

  To enable this feature for all packets, program the SARC field of the MAC Configuration register.

- Enabling SA insertion or replacement for selective packets

  To enable this feature for selective packets, program the SA Insertion Control field (Bits[25:23] of TDES3) in the first Transmit descriptor of the packet. When Bit 25 of TDES3 is set, the SA Insertion Control field indicates insertion or replacement by MAC Address1 registers. When Bit 25 of TDES3 is reset, it indicates insertion or replacement by MAC Address0 registers.

If MAC Address1 Registers are not enabled, the MAC Address0 registers are used for insertion or replacement irrespective of the value of the most-significant bit of the SA Insertion Control field.

VLAN Insertion, Replacement, or Deletion:

The software can use the VLAN insertion, replacement, or deletion feature to instruct the MAC to do the following for Tx packets:

- Delete the VLAN Type and VLAN Tag fields
- Insert or replace the VLAN Type and VLAN Tag fields

Insertion or replacement is done based on the setting of VLTI bit in the MAC VLAN Incl register.

VLTI bit is set, The MAC inserts or replaces the following:

- VLAN Type field (C-VLAN or S-VLAN as indicated by the CSVL bit of MAC VLAN Incl register)
- VLAN Tag field with the content of the VT field of Transmit context descriptor of the packet

VLTI bit is reset, The MAC inserts or replaces the following:

- VLAN Type field (C-VLAN or S-VLAN as indicated by the CSVL bit of MAC VLAN Incl register)
- VLAN Tag field with the VLT field of MAC VLAN Incl register

When VLAN replacement or deletion is enabled, the MAC checks if the VLAN Type field (0x8100 or 0x88a8) is present after the DA and SA fields in the Transmit packet. The replace or delete operation does not occur if the VLAN Type field is not detected in two bytes following the DA and SA fields. However, when VLAN insertion is enabled, the MAC does not check the presence of VLAN Type field in the Transmit packet and just inserts the VLAN Type and VLAN Tag fields.

You can enable the VLAN insertion, replacement, or deletion feature for all Tx packets or selective packets:

- Enabling VLAN insertion, replacement, or deletion for all packets

  To enable this feature for all packets, program the VLC and VLP fields of MAC VLAN Incl register.

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- Enabling VLAN insertion, replacement, or deletion for selective packets

  To enable this feature for selective packets, program the VTIR field of TDES2 Normal Descriptor

In addition, the VLP (VLAN Priority control) bit must be reset in MAC VLAN Incl register (for outer VLAN) and MAC Inner VLAN Incl register (in inner VLAN) for the MAC to take the control inputs from the host, depending on the configuration.

47.5.4 PHY Interfaces Description

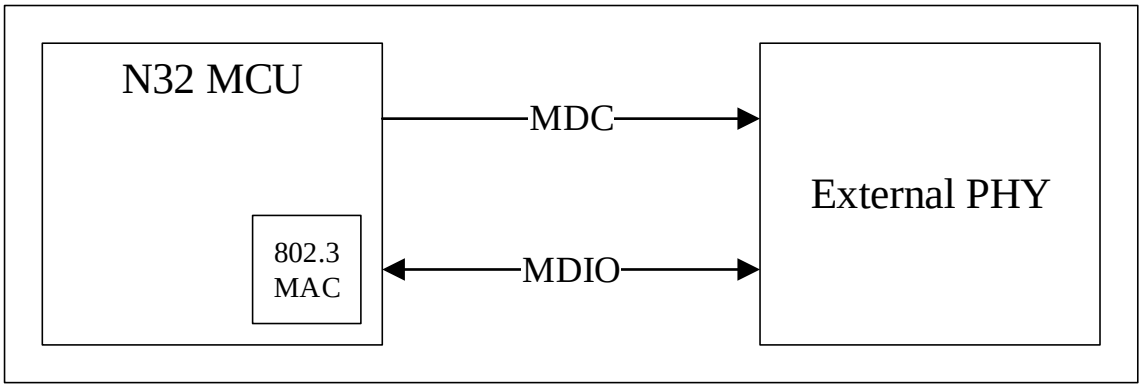
The Ethernet peripheral supports multiple PHY interfaces, with ETH1 supporting GMII, MII, and RMII, and ETH2 supporting MII and RMII. This section describes the SMA (Station Management Agent) interface used for PHY control (management) and the different PHY interfaces.

47.5.4.1 SMA

The application can access the PHY registers through the Station Management Agent (SMA). SMA is a two-wire Station Management interface.

The SMA module supports access to up to 32 PHYs. The application can address any one of the 32 registers in any one of the 32 PHYs. However, only one register in one PHY can be addressed at a time. The application sends control data to the PHY and receives status information from the PHY via the SMA module.

Figure 47-8 SMA signals



For MIM accesses, the maximum operating frequency of the MDC is 2.5 MHz, as specified in the IEEE 802.3. In the peripheral, the MDC clock is derived from the application or CSR clock, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC MDIO Address register

The MDIO frame structure is as follows:

Table 47-10 MDIO Clause 45 Frame Structure

Field	Description
IDLE	The MDIO line is in tri-state; there is no clock on MDC signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2’b00
OPCODE	■ 2'b00: Address ■ 2'b01: Write

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Field	Description
	■ 2'b10: Read + Address ■ 2'b11: Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address select for one of 32 devices
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY. ■ In address and data write cycles, the Ethernet peripheral drives the MDIO line during the transfer of these 16 bits. ■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16 bits.

The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC MDIO Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table 47-11 shows the Clause 22 frame format.

Table 47-11 MDIO Clause 22 Frame Structure

Field	Description
IDLE	The MDIO line is in tri-state; there is no clock on MDC signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b01
OPCODE	■ 2'b01: Write ■ 2'b10: Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address to select the register within each MMD
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	Any 16-bit value: ■ In a write operation, the Ethernet peripheral drives MDIO. ■ In read operation, the PHY drives MDIO.

GMII/MII Management Write Operation

After the Station Management Agent receives the PHY address and the write data from the MAC CSR module, the SMA starts a Write operation to the PHY registers.

The flow of a Management write operation is as follows:

1. Set bits [3:2] in the MAC MDIO address register to 2'b01 and device bit 0.

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2. The MAC CSR module transfers the PHY address, the register address in the PHY, and the data to be written (MAC MDIO data register) to the SMA to initiate the write operation to the PHY register.
3. The SMA module initiates the write operation on the GMII management interface using the management packet format specified in the GMII specification (according to Section 22.2.4.5 of IEEE 802.3-2002).
4. When the SMA module begins the write operation on MDIO, the write packet is transmitted over the MDIO lines. The MAC drives the MDIO lines throughout the entire duration of the packet. The "busy" bit is set to 1 until the write operation is complete. During this period (when the "busy" bit is high), the CSR ignores write operations to the MAC MDIO address register or MAC MDIO data register.
5. When the Write operation is complete, the SMA indicates this to the CSR.
6. The CSR resets the "busy" bit.

GMII/MII Management Read Operation

After the Station Management Agent receives the PHY address and the register address in the PHY from the MAC CSR module, the SMA initiates a Read operation to the PHY registers.

The flow of a Management read operation is as follows:

1. Set Bit [3:2] to 2'b11 and Bit 0 in the MAC MDIO Address register
2. The MAC CSR module transfers the PHY address and the register address in PHY to the SMA to initiate a Read operation in the PHY registers
3. The SMA module starts a Read operation on the GMII Management Interface using the Management Packet Format specified in the GMII specifications (as per IEEE 802.3-2002, Section 22.2.4.5).
4. When the SMA module starts a Read operation on the MDIO, the CSR ignores the Write operations to the MAC MDIO Address or MAC MDIO Data register during this period (the Busy bit is high) and the transaction is completed without any error on the MCI interface.
5. When the Read operation is complete, the SMA indicates this to the CSR.
6. The CSR resets the Busy bit and updates the MAC MDIO Data register with the data read from the PHY.

For more information about the communication from the application to the PHYs, see the Reconciliation Sublayer and Media Independent Interface Specifications sections of the IEEE 802.3z, 1000BASE Ethernet.

47.5.4.2 MII

The media-independent interface (MII) defines the interconnection between the MAC sublayer and the PHY for data transfer at 10 Mbit/s and 100 Mbit/s.

MII signals are given in Figure 47-9.

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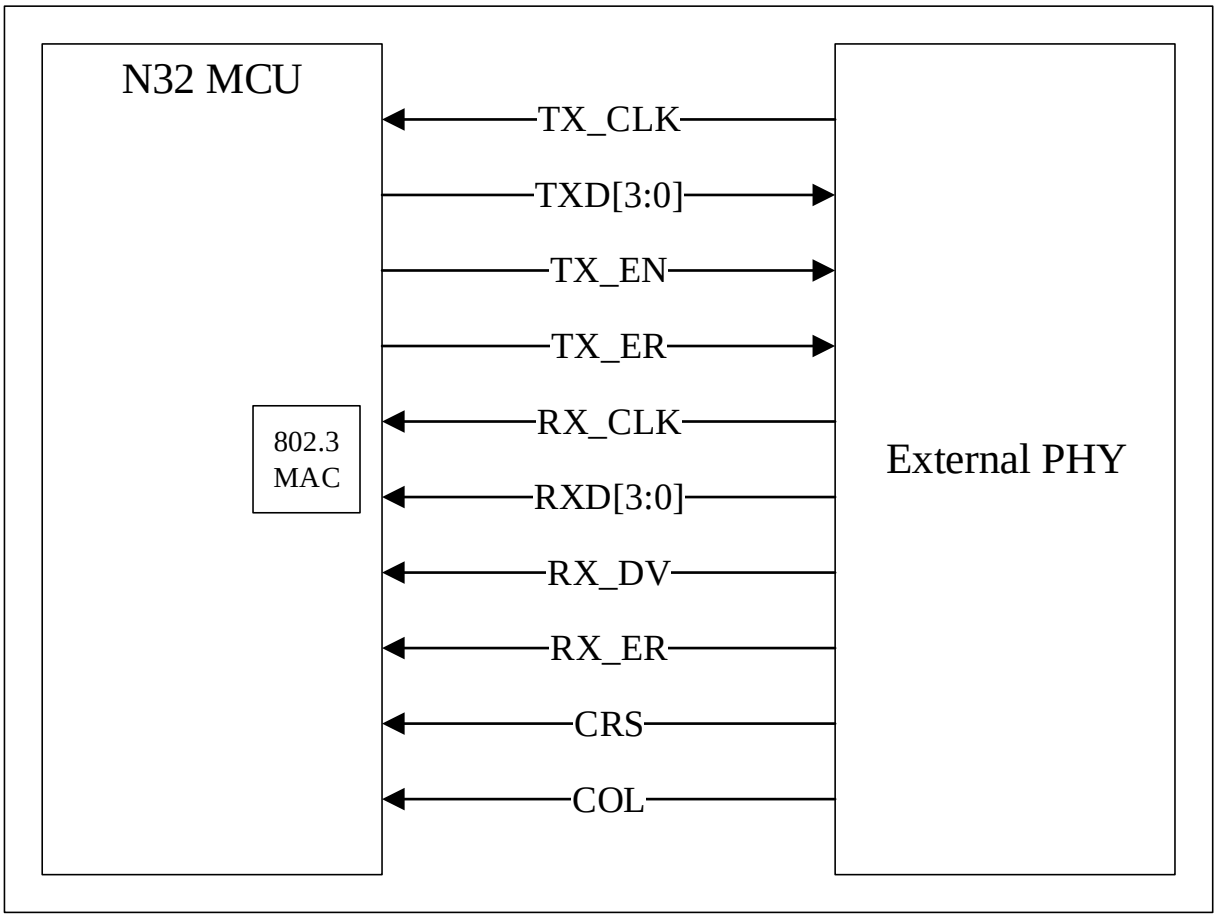
Figure 47-9 MII signals



- TX_CLK: Continuous clock that provides the timing reference for Tx data transfers. The nominal frequency is 2.5 MHz at 10 Mbit/s and 25 MHz at 100 Mbit/s.
- TXD[3:0]: Transmit data. TXD is a bundle of 4 data signals driven synchronously by the MAC sublayer and qualified (valid data) on the assertion of the TX_EN signal. TXD[0] is the least significant bit, TXD[3] is the most significant bit. While TX_EN is deasserted, the transmit data must have no effect upon the PHY.
- TX_EN: Transmission enable signal indicating that the MAC is presenting nibbles on the MII for transmission. It must be asserted synchronously (TX_CLK) with the first nibble of the preamble and must remain asserted while all nibbles to be transmitted are presented to the MII.
- TX_ER (optional): Required only for Energy Efficient Ethernet (EEE). The transmit error is indicated by inverting the CRC. The remote station can detect the Transmit error through incorrect CRC.
- RX_CLK: Continuous clock that provides the timing reference for Rx data transfers. The nominal frequency is 2.5 MHz at 10 Mbit/s, 25 MHz at 100 Mbit/s.
- RXD[3:0]: Receive data. RXD is a bundle of 4 data signals driven synchronously by the PHY and qualified (valid data) on the assertion of the RX_DV signal. RXD[0] is the least significant bit, RXD[3] is the most significant bit. While RX_EN is deasserted and RX_ER is asserted, a specific RXD[3:0] value is used to transfer specific information from the PHY.
- RX_DV: Receive data valid. This signal indicates that the PHY is presenting recovered and decoded nibbles on

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the MII for reception. It must be asserted synchronously (RX_CLK) with the first recovered nibble of the frame and must remain asserted through the final recovered nibble. It must be deasserted prior to the first clock cycle that follows the final nibble. In order to receive the frame correctly, the RX_DV signal must encompass the frame, starting no later than the SFD field.

- RX_ER: Receive error. This signal must be asserted for one or more clock periods (RX_CLK) to indicate to the MAC sublayer that an error was detected somewhere in the frame. This error condition must be qualified by RX_DV assertion.
- CRS: Carrier sense. This signal is asserted by the PHY when either the transmit or receive medium is non idle. It must be deasserted by the PHY when both transmit and receive media are idle.

  The PHY must ensure that the CS signal remains asserted throughout the duration of a collision condition. This signal is not required to transition synchronously with respect to the Tx and Rx clocks. In Full-duplex mode the state of this signal is don't care for the MAC sublayer.
- COL: Collision detection signal. This signal must be asserted by the PHY upon detection of a collision on the medium and must remain asserted while the collision condition persists. This signal is not required to transition synchronously with respect to the Tx and Rx clocks. In Full-duplex mode, the state of this signal is don't care for the MAC sublayer

Note: MII complies with the IEEE 802.3-2015 standard. For more information about MII, please refer to the relevant IEEE 802.3-2015 documentation.

47.5.4.3 RMII

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port — a 62.5% decrease in pin count The RMII module is instantiated between the MAC and the PHY. This helps in translating the MII of the MAC into the RMII. The RMII block has the following characteristics:

- Supports 10 Mbps and 100 Mbps operating rates. It does not support the 1000 Mbps operation
- Provides independent 2-bits wide Transmit and Receive paths by sourcing two clock references externally.

Figure 47-10 shows the position of the RMII block relative to the Ethernet peripheral and RMII PHY. The RMII block is placed in front of the Ethernet peripheral to translate the MII signals to RMII signals.

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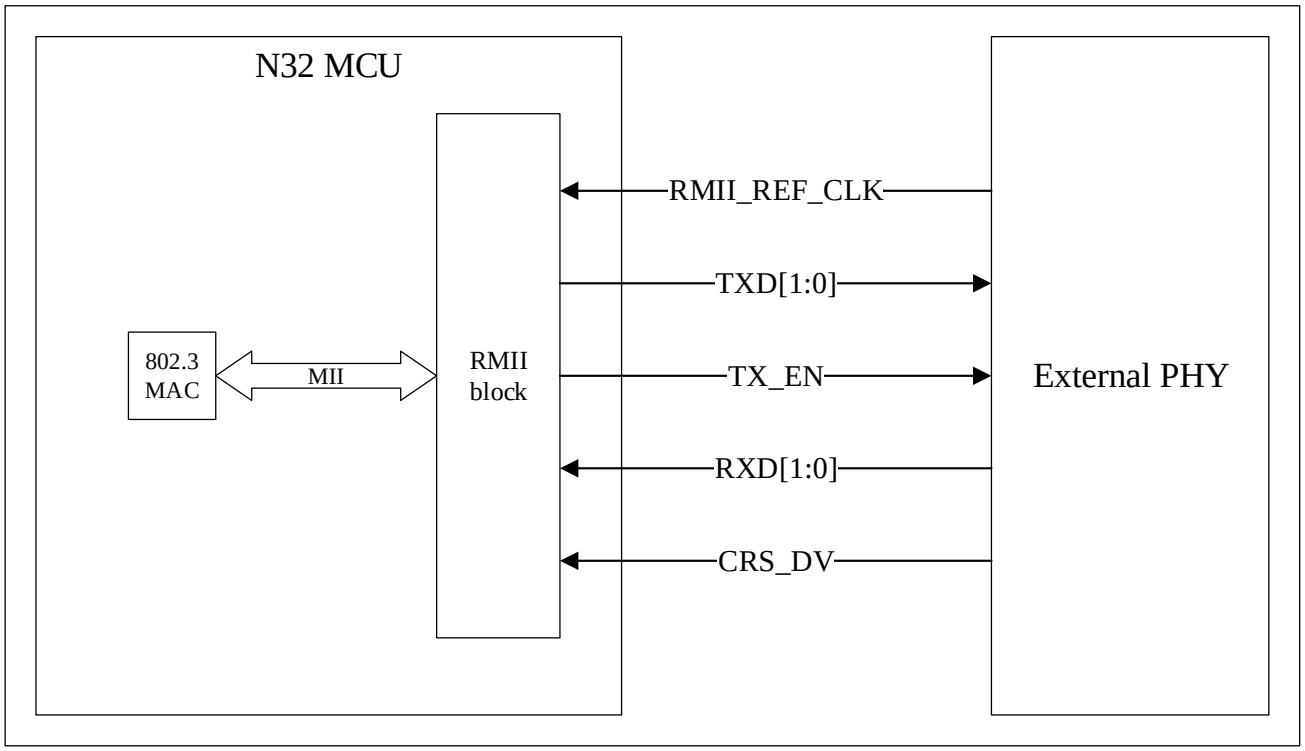
Figure 47-10 RMII signals



- RMII_REF_CLK: Continuous 50 MHz reference clock input.
- TXD[1:0]: Transmit data.
- TX_EN: Transmit data enable. When high, this bit indicates that valid data are being transmitted on TXD[1:0].
- RXD[1:0]: Receive data.
- CRS_DV: Carrier Sense (CRS) and Rx Data Valid (RX_DV) multiplexed on alternate clock cycles. In 10 Mbit/s mode, it alternates every 10 clock cycles.

Note: RMII complies with RMII Alliance Specification Version 1.2. For more information about RMII, please refer to the relevant documentation for RMII Alliance Specification Version 1.2.

Transmit Bit Ordering

Each nibble from the MII interface must be transmitted on the RMII interface di-bit at a time with the order of di-bit transmission shown in Figure 47-11. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

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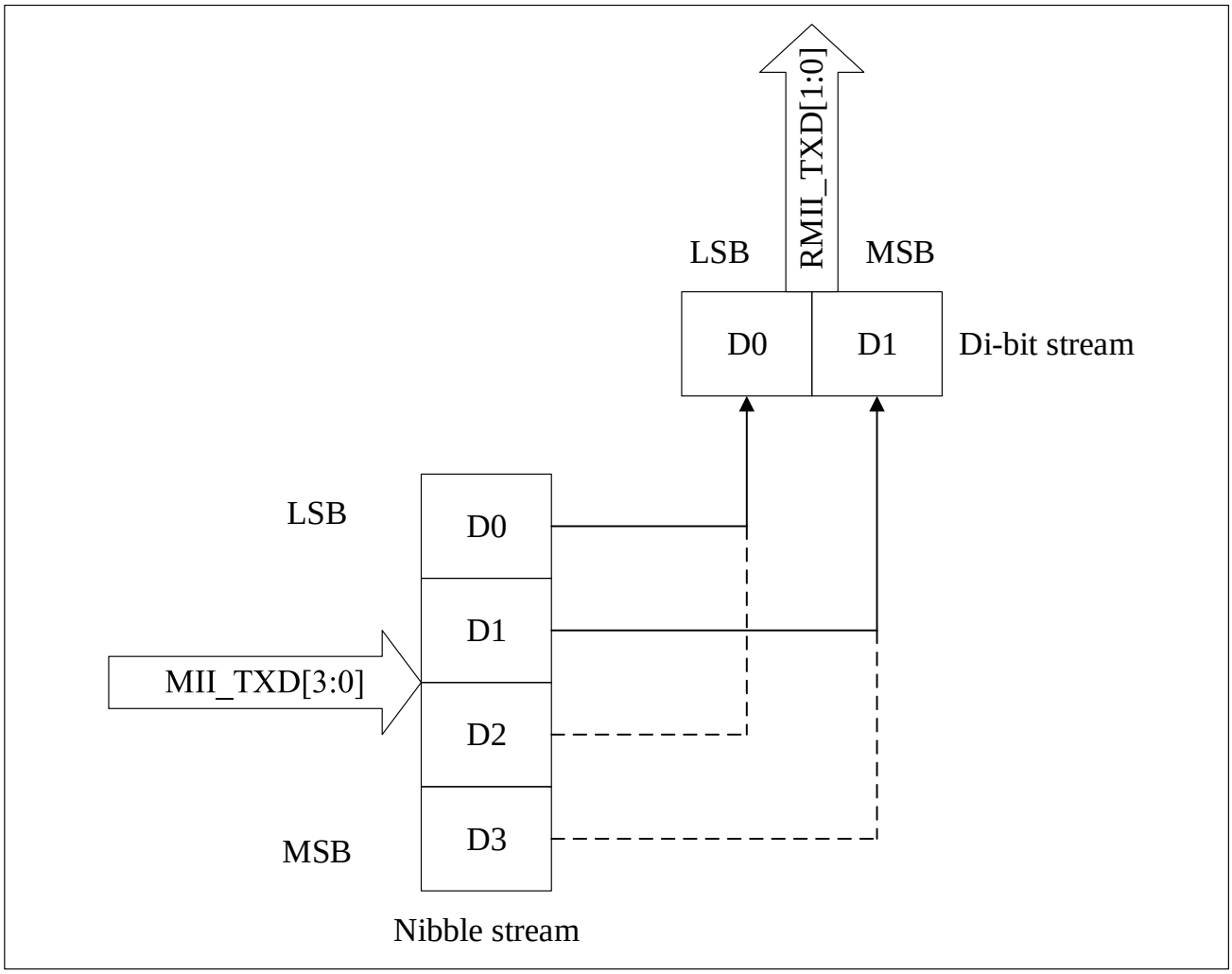
Figure 47-11 Transmit Bit Ordering



Receive Bit Ordering

Each nibble is transmitted to the MII interface from the di-bit received from the RMII interface in the nibble transmission order shown in Figure 47-12. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

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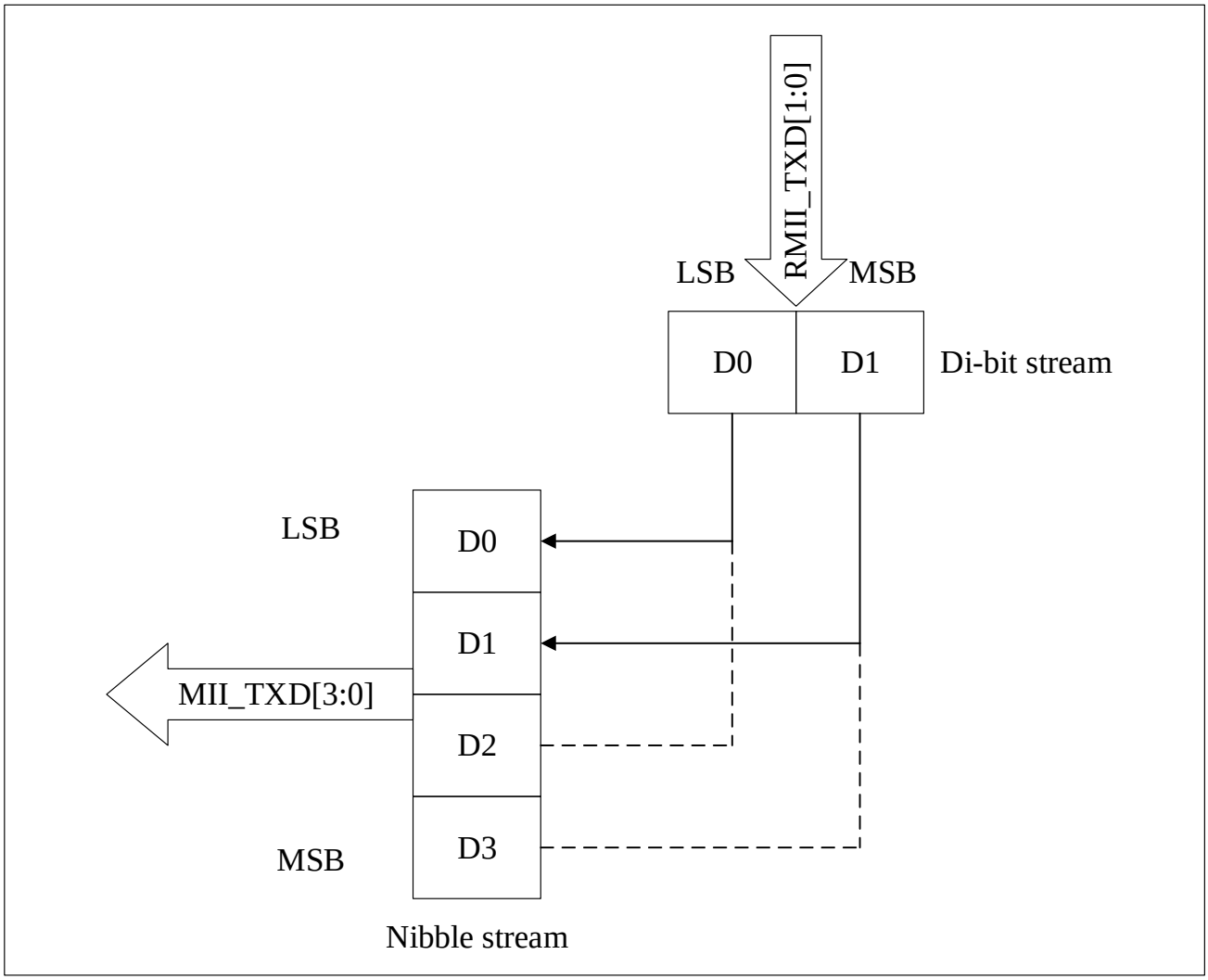
Figure 47-12 Receive Bit Ordering



47.5.4.4 GMII

GMII defines the interconnection between the MAC sublayer and the PHY for 10 Mb/s, 100 Mb/s, and 1000 Mbit/s data transmission.

The GMII signals are shown in the figure below:

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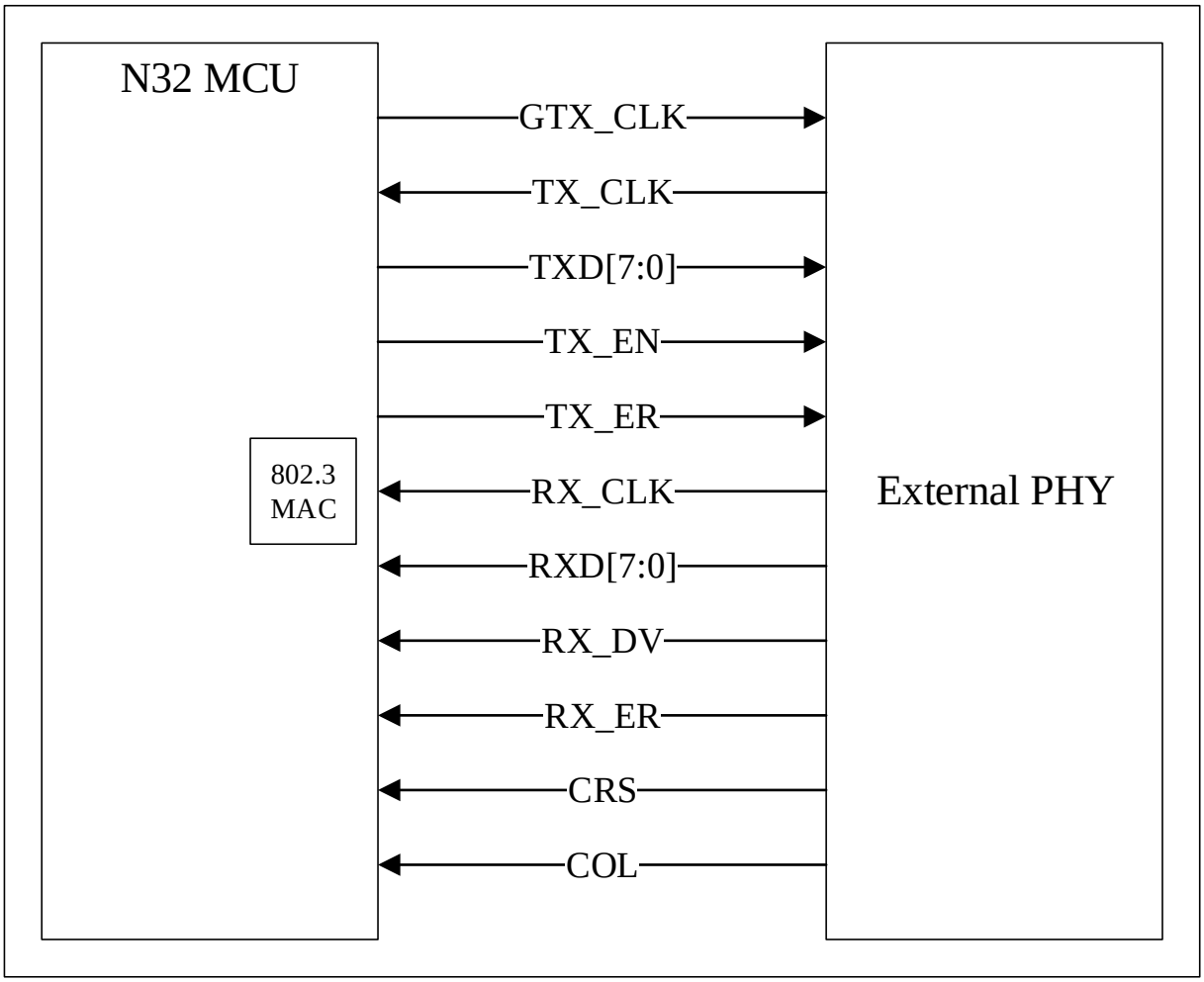
Figure 47-13 GMII signals



- GTX_CLK: Continuous clock signal for 1000 Mbit/s operation. This clock signal is generated internally by the chip and transmitted to the PHY interface. The nominal frequency is 125 MHz.
- TX_CLK: Continuous clock signal. Provides timing reference for Tx data transmission at 10 Mbit/s and 100 Mbit/s. The nominal frequency is 2.5 MHz at 10 Mbit/s and 25 MHz at 100 Mbit/s.
- TXD[7:0]: Transmit data. TXD is a bundle of eight data signals synchronously driven by the MAC sublayer, which are active only when the TX_EN signal is active (valid data). TXD[0] is the least significant bit, and TXD[7] is the most significant bit. When TX_EN is inactive, the transmit data has no effect on the PHY.
- TX_EN: Transmit enable signal. This signal indicates that the MAC is currently transmitting byte data to GMII. It must be synchronized with the first byte of the preamble (GTX_CLK/TX_CLK) and remain active until all bytes to be transmitted have been sent to GMII.
- TX_ER: Indicates a transmit error or carrier extension on TXD[7:0].
- RX_CLK: Continuous clock signal. Provides timing reference for Rx data transmission. Nominal frequency is 2.5MHz at 10Mbit/s, 25MHz at 100Mbit/s, and 125MHz at 1000Mbit/s.
- RXD[7:0]: Received data. RXD is a bundle of eight data signals synchronously driven by the PHY and is only valid when the RX_DV signal is active (valid data). RXD[0] is the least significant bit, and RXD[7] is the most

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Email: sales@nsing.com.sg

significant bit. When RX_EN is inactive and RX_ER is active, specific RXD[7:0] values are used to transmit specific information from the PHY.

- RX_DV: Receive Data Valid. This signal indicates that the PHY is currently receiving restored and decoded byte data for GMII. This signal must be synchronized with the first restored byte of the frame (RX_CLK) and remain active until the last restored byte. This signal must be deactivated before the first clock cycle following the last byte. To correctly receive a frame, the RX_DV signal must span the entire frame, with its start time no later than the SFD field.
- RX_ER: Receive Error. This signal must remain active for one or more clock cycles (RX_CLK) to indicate to the MAC sublayer that an error was detected somewhere in the frame. This error condition must be bounded by the active state of RX_DV.
- CRS: Carrier Sense. The PHY sets this signal active when the transmit or receive medium is not idle. When both the transmit and receive media are idle, the PHY must set this signal inactive. The PHY must ensure that the CS signal remains active during the duration of a collision condition. This signal does not need to be synchronized with the transmit and receive clocks. In full-duplex mode, the state of this signal is meaningless to the MAC sublayer.
- COL: Collision detection. When a collision is detected on the medium, the PHY must set this signal to active and keep it active during the collision condition. This signal does not need to be synchronized with the transmit and receive clocks. In full-duplex mode, the state of this signal is meaningless to the MAC sublayer.

Note: GMII complies with the IEEE 802.3-2015 standard. For more information on GMII, please refer to the relevant IEEE 802.3-2015 documentation.

47.5.5 Packet Filtering

MAC supports the following types of Rx packet filtering:

- MAC source address or destination address filtering:

  The Address Filtering Module (AFM) checks the source address and destination address fields of each incoming packet.

- VLAN filtering:

  MAC supports filtering based on VLAN tags and VLAN hashes.

- Layer 3 and Layer 4 filtering:

  Layer 3 filtering refers to IP source address and destination address filtering. Layer 4 filtering refers to source port and destination port filtering.

These three filtering types can be cascaded. The following diagram shows the filtering sequence for Rx packets:

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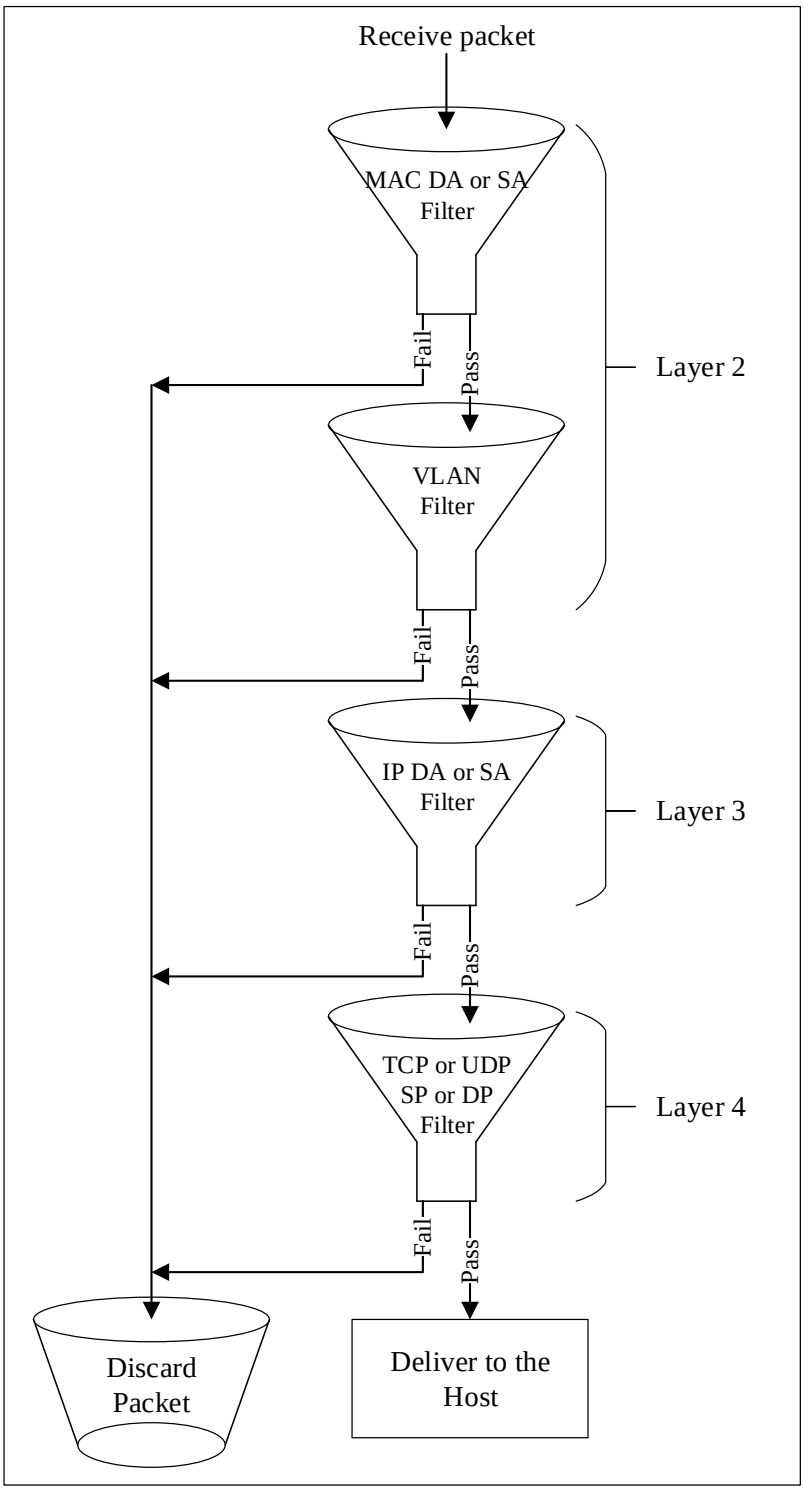
Figure 47-14 Packet Filtering Sequence



The sequence shown in Figure 47-14 is valid when all the filters (L2, VLAN, L3, L4) are active. If any of the Layer filters are not enabled, that filter is bypassed and the subsequent filter is applied. A packet that fails any of the filters is discarded. However, the discarded packet can be forwarded to the host based on the register control. For example, when Bit RA of MAC Packet Filter register is set to 1, all discarded packets are forwarded to the host but with its packet status indicating the specific filter-failure. If RA=0, Bits VTFE and IPFE of MAC Packet Filter register

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controls if the packets that fail the VLAN filter and Layer 3-4 filter should be discarded or forwarded to the host.

47.5.5.1 Source Address or Destination Address Filtering

The Address Filtering Module of the MAC checks the source address (SA) and destination address (DA) fields of each incoming packet.

Unicast Destination Address Filtering

The MAC supports up to 4 MAC addresses for unicast perfect filtering. If perfect filtering is selected (HUC bit of MAC Packet Filter register is reset), the MAC compares all 48 bits of received unicast address with the programmed MAC address for any match. The default MacAddr0 is always enabled.

The MacAddr1 to MacAddr3 addresses are selected with an individual enable bit. For MacAddr1 to MacAddr3 addresses, you can mask each byte during comparison with corresponding received DA byte by setting the corresponding Mask Byte Control bit in the register. This enables group address filtering for the DA.

In hash filtering mode (when HUC bit is set), the MAC performs imperfect filtering for unicast addresses using a 64-bit Hash table. For hash filtering, the MAC uses the upper 6 bits CRC of the received destination address to index the content of the Hash table. A value of 00000 selects Bit 0 of selected register, and a value of 11111 selects Bit 63 of Hash Table register. If the corresponding bit (indicated by the 6-bit CRC) is set to 1, the unicast packet is considered to have passed the Hash filter; otherwise, the packet is considered to have failed the Hash filter.

Multicast Destination Address Filtering

To program the MAC to pass all multicast packets, set the PM bit in MAC Packet Filter register. If the PM bit is reset, the MAC performs the filtering for multicast addresses based on the HMC bit of the MAC Packet Filter register.

The multicast address is compared with the programmed MAC Destination Address registers (1–3). Group address filtering is also supported.

In Hash filtering mode, the MAC performs imperfect filtering using a 64-bit Hash table. The MAC uses the upper 6-bits CRC of received multicast address to index the content of the Hash table. A value of 000000 selects Bit 0 of selected register and a value of 111111 selects Bit 63 of the Hash Table register. If the corresponding bit is set to 1, the multicast packet is considered to have passed the Hash filter. Otherwise, the packet is considered to have failed the Hash filter.

Hash or Perfect Address Filtering

To configure the DA filter to pass a packet when its DA matches either the Hash filter or the Perfect filter, set the HPF bit and the corresponding HUC or HMC bits in MAC Packet Filter register. This is applicable to both unicast and multicast packets. If the HPF bit is reset, only one of the filters (Hash or Perfect) is applied to received packet.

Broadcast Address Filtering

The MAC does not filter any broadcast packets by default. To program the MAC to reject all broadcast packets, set the DBF bit in MAC Packet Filter register

Unicast Source Address Filtering

The MAC can perform perfect filtering based on the source address field of received packets. By default, the MAC compares the SA field with the values programmed in the SA registers. You can configure the MAC Address registers [1–3] to use SA instead of DA for comparison by setting Bit 30 of corresponding register.

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The MAC also supports group filtering with SA. You can filter a group of addresses by masking one or more bytes of the address. The MAC drops the packets that fail the SA filter if the SAF bit is set in MAC Packet Filter register. Otherwise, the result of the SA filter is given as a status bit in the Receive Status word. When the SAF bit is set, the SA filter and DA filter result is AND'ed to decide whether the packet needs to be forwarded. This means that the packet is dropped if either filter fails. The packet is forwarded to the application only if the packet passes both filters in-order.

Inverse Filtering

For DA and SA filtering, you can invert the filter-match result at the final output by setting the DAIF and SAIF bits of MAC Packet Filter register. The DAIF bit is applicable for both Unicast and Multicast DA packets. The result of the unicast or multicast destination address filter is inverted in this mode. Similarly, when the SAIF bit is set, the result of unicast SA filter is reversed.

Note: When the RA bit of MAC Packet Filter register is set, all packets are forwarded to the system along with the correct result of the address filtering in the Rx Status.

Table 47-12 and Table 47-13 summarize the DA and SA filtering based on the type of packets received.

Table 47-12 Destination Address Filtering

Packet Type	PM	HPF	HUC	DAIF	HMC	PAM	DBP	DA Filter Operation
Broadcast	1	x	x	x	x	x	x	Pass
	0	x	x	x	x	x	0	Pass
	0	x	x	x	x	x	1	Fail
Unicast	1	x	x	x	x	x	x	Pass all packets
	0	x	0	0	x	x	x	Pass on Perfect/Group filter match
	0	x	0	1	x	x	x	Fail on Perfect/Group filter match
	0	0	1	0	x	x	x	Pass on Hash filter match
	0	0	1	1	x	x	x	Fail on Hash filter match
	0	1	1	0	x	x	x	Pass on Hash or Perfect/Group filter match
	0	1	1	1	x	x	x	Fail on Hash or Perfect/Group filter match
Multicast	1	x	x	x	x	x	x	Pass all packets
	x	x	x	x	x	1	x	Pass all packets
	0	x	x	0	0	0	x	Pass on Perfect/Group filter match and drop Pause packets if PCF = 0x
	0	0	x	0	1	0	x	Pass on Hash filter match and drop Pause packets if PCF = 0x
	0	1	x	0	1	0	x	Pass on Hash or Perfect/Group filter match and drop Pause packets if PCF = 0x
	0	x	x	1	0	0	x	Fail on Perfect/Group filter match and drop Pause packets if PCF = 0x
	0	0	x	1	1	0	x	Fail on Hash filter match and drop Pause packets if PCF = 0x
	0	1	x	1	1	0	x	Fail on Hash or Perfect/Group filter match and drop Pause packets if PCF = 0x

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Table 47-13 Source Address Filtering

Packet Type	PM	SAIF	SAF	SA Filter Operation
	1	x	x	Pass all packets
	0	0	0	Pass status on Perfect or Group filter match but do not drop packets that fail
Unicast	0	1	0	Fail status on Perfect or Group filter match but do not drop packet
	0	0	1	Pass on Perfect or Group filter match and drop packets that fail
	0	1	1	Fail on Perfect or Group filter match and drop packets that fail

Note: x represents any value (0 or 1).

47.5.5.2 VLAN Filtering

VLAN Tag Perfect Filtering

In VLAN tag perfect filtering, the MAC compares the VLAN tag of received packet and provides the VLAN packet status to the application. Based on the programmed mode, the MAC compares the lower 12 bits or all 16 bits of received VLAN tag to determine the perfect match.

If VLAN tag perfect filtering is enabled, the MAC forwards the VLAN-tagged packets along with VLAN tag match status and drops the VLAN packets that do not match. You can also enable the inverse matching for VLAN packets by setting the VTIM bit of MAC VLAN Tag register. In addition, you can enable processing of S-VLAN tagged packets along with the default C-VLAN tagged packets by setting the ESVL bit of MAC VLAN Tag register. The VLAN packet status bit (Bit 10 of RDES0) indicates the VLAN tag match status for the matched packets.

Note: The source or destination address (if enabled) has precedence over the VLAN tag filters. This means that a packet that fails the source or destination address filter is dropped irrespective of the VLAN tag filter results. By default, the VLAN tag-based perfect filter is available in all configurations.

VLAN Tag Hash Filtering

The 16-bit VLAN Hash Table is used for group address filtering based on the VLAN tag. The VLAN Tag Hash Filtering feature can be enabled using the VTHM (VLAN Tag Hash Table Match Enable) bit of the MAC VLAN Tag register.

The MAC provides VLAN tag hash filtering with a 16-bit Hash table.

The MAC performs the VLAN hash matching based on the VTHM of the MAC VLAN Tag register. If the VTHM bit is set, the most significant four bits of CRC-32 of VLAN tag are used to index the content of the MAC VLAN Hash Table register. A value of 1 in the MAC VLAN Hash Table register, corresponding to the index, indicates that the VLAN tag of the packet matched and the packet should be forwarded. A value of 0 indicates that VLAN-tagged packet should be dropped.

Note: The 16 or 12 bits of VLAN Tag are considered for CRC-32 computation based on ETV bit in MAC VLAN TAG register. When ETV bit is reset, most significant four bits of CRC-32 of VLAN Tag are inverted and used to index the content of MAC VLAN Hash Table register. When ETV bit is set, most significant four bits of CRC-32 of VLAN Tag are directly used to index the content of MAC VLAN Hash Table register.

The MAC also supports the inverse matching for VLAN packets. In the inverse matching mode, when the VLAN tag of a packet matches the perfect or hash filter, the packet should be dropped. If the VLAN perfect and VLAN hash match are enabled, a packet is considered as matched if either the VLAN hash or the VLAN perfect filter matches.

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When inverse match is set, a packet is forwarded only when both perfect and hash filters indicate mismatch.

Table 47-14 shows the different possibilities for VLAN matching and the final VLAN match status. When the RA bit of MAC Packet Filter register is set, all packets are received and the VLAN match status is indicated in the VF bit of RDES2 Normal Descriptor (Write-Back Format). When the RA bit is not set and the VTFE bit is set in MAC Packet Filter register, the packet is dropped if the final VLAN match status is Fail.

When VLAN VID is programmed to 0 in the VL field of MAC VLAN Tag register, all VLAN-tagged packets are considered as perfect matched but the status of the VLAN hash match depends on the VTHM and VTIM bits in MAC VLAN Tag register.

Table 47-14 VLAN Match Status

VID	VLAN Perfect Filter Match Result	VTHM	VLAN Hash Filter Match Result	VTIM	Final VLAN Match Status
VID = 0	Pass	0	x	x	Pass
	Pass	1	x	0	Pass
	Pass	1	Fail	1	Pass
	Pass	1	Pass	1	Fail
VID != 0	Pass	x	x	0	Pass
	Fail	0	x	0	Fail
	Fail	1	Fail	0	Fail
	Fail	1	Pass	0	Pass
	Fail	0	x	1	Pass
	Pass	x	x	1	Fail
	Fail	1	Pass	1	Fail
	Fail	1	Fail	1	Pass

Note: x represents any value (0 or 1).

47.5.5.3 Layer 3 and Layer 4 Filtering

The Ethernet peripheral supports Layer 3 and Layer 4 based packet filtering. The Layer 3 filtering refers to the IP Source or Destination Address filtering in the IPv4 or IPv6 packets whereas Layer 4 filtering refers to the Source or Destination Port number filtering in TCP or UDP.

When Layer 3 and Layer 4 filtering is enabled, the packets are filtered in the following way:

- Matched Packets: The MAC forwards the packets that match all enabled fields to the application along with the status. The MAC gives the matched field status only if the IPC bit of MAC Configuration register is set and one of the following conditions is true:
  - All enabled Layer 3 and Layer 4 fields match
  - At least one of the enabled field matches and other fields are bypassed or disabled

  When multiple Layer 3 and Layer 4 filters are enabled, any filter match is considered as a match. If more than one filter matches, the MAC provides the status of the lowest filter where Filter 0 is the lowest filter and Filter 3 is the highest filter. For example, if Filter 0 and Filter 1 match, the MAC gives the status corresponding to filter 0.

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Note: The source or destination address and VLAN tag filters (if enabled) have precedence over Layer 3 and Layer 4 filter. This means that a packet which fails the source or destination address or VLAN tag filter is dropped irrespective of the Layer 3 and Layer 4 filter results.

- Unmatched Packets: The MAC drops the packets that do not match any of the enabled fields. You can use the inverse match feature to block or drop a packet with specific TCP or UDP over IP fields and forward all other packets.

  The aborted or partial packets can be dropped in the MTL Rx FIFO. If the Rx FIFO operates in the Threshold (cut-through) mode and the threshold is programmed to a small value, such that packet transfer to application starts before the failed Layer 3 and Layer 4 filter results are available, the application may receive a partial packet with appropriate abort status.

- Non-TCP or UDP IP Packets: By default, all non-TCP or UDP IP packets are bypassed from the Layer 3 and Layer 4 filters. You can optionally program the MAC to drop all non-TCP or UDP over IP packets.

Layer 3 Filtering

The Ethernet peripheral supports perfect matching or inverse matching for IP Source Address and Destination Address. In addition, you can match the complete IP address or mask the lower bits matching, that is, compare all bits of the address except the specified lower mask bits.

For IPv6 packets filtering, you can enable the last four data registers of a register set to contain the 128-bit IP Source Address or IP Destination Address. The IP Source Address or Destination Address should be programmed in the order defined in the IPv6 specification, that is, the first byte of the IP Source Address or Destination Address in the received packet is in the higher byte of the register and the subsequent registers follow the same order.

For IPv4 packet filtering, you can enable the second and third data registers of a register set to contain the 32-bit IP Source Address and IP Destination Address. The remaining two data registers are reserved. The IP Source Address or Destination Address should be programmed in the order defined in the IPv4 specification, that is, the first byte of IP Source Address and Destination Address in the received packet in the higher byte of the respective register.

Layer 4 Filtering

The Ethernet peripheral supports perfect matching or inverse matching for TCP or UDP Source and Destination Port numbers. However, you can program only one type (TCP or UDP) at a time. The first data register contains the 16-bit Source and Destination Port numbers of TCP or UDP, that is, the lower 16 bits for Source Port number and higher 16 bits for Destination Port number.

The TCP or UDP Source and Destination Port numbers should be programmed in the order defined in the TCP or UDP specification, that is, the first byte of TCP or UDP Source and Destination Port number in the received packet is in the higher byte of the register.

Layer 3 and Layer 4 Filters Registers

The MAC implements a set of registers for Layer 3 and Layer 4 based packet filtering. In a register set, there is a control register, such as MAC L3 L4 Filter 0 Control register, to control the packet filtering. In addition, there are five address registers to program the Layer 3 and Layer 4 fields to be matched, such as:

- ETH MAC L3 L4 Filter n Control register (ETH_MACL3L4FnCTRL)
- ETH MAC L4 Filter n Port register (ETH_MACL4FnPORT)

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- ETH MAC L3 Filter n Address 0 register (ETH_MACL3FnADDR0)
- ETH MAC L3 Filter n Address 1 register (ETH_MACL3FnADDR1)
- ETH MAC L3 Filter n Address 2 register (ETH_MACL3FnADDR2)
- ETH MAC L3 Filter n Address 3 register (ETH_MACL3FnADDR3)

47.5.6 IEEE 1588 Timestamp

The IEEE 1588 defines a Precision Time Protocol (PTP) which enables precise synchronization of time in measurement and control systems. This protocol enables heterogeneous systems that include clocks of varying inherent precision, resolution, and stability to synchronize. The protocol supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources.

The Ethernet peripheral supports the IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2). The IEEE 1588-2002 supports PTP transported over UDP/IP and IEEE 1588-2008 supports PTP transported over Ethernet. The Ethernet peripheral provides programmable support for both standards.

The controller supports the following features:

- Provides an option to take snapshot of all packets or only PTP type packets
- Provides an option to take snapshot of only event messages
- Provides an option to take the snapshot based on the clock type: ordinary, boundary, end-to-end transparent, and peer-to-peer transparent
- Provides an option to select the node to be a master or slave for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format

47.5.6.1 Clock Types

Ordinary Clock

The ordinary clock in a domain supports a single copy of the protocol. The ordinary clock has a single PTP state and a single physical port. In typical industrial automation applications, an ordinary clock is associated with an application device such as a sensor or an actuator. In telecom applications, the ordinary clock can be associated with a timing demarcation device.

The ordinary clock can be a grandmaster or a slave clock. It supports the following features:

- Sends and receives PTP messages. The timestamp snapshot can be controlled as described in MAC Timestamp Control register.
- Maintains the data sets such as timestamp values.

Table 47-15 shows the messages for which you can take the timestamp snapshot on the receive side for master and slave nodes.

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Table 47-15 Ordinary Clock: PTP Messages for Snapshot

Master	Slave
Delay_Req	SYNC

For an ordinary clock, you can take the snapshot of either of the following PTP message types: version 1 or version 2. You cannot take the snapshots for both PTP message types. You can take the snapshot by setting the TSVER2ENA bit and selecting the snapshot mode in MAC Timestamp Control register.

Boundary Clock

The boundary clock typically has several physical ports communicating with the network. The messages related to synchronization, master-slave hierarchy, and signaling terminate in the protocol engine of the boundary clock and such messages are not forwarded. The PTP message type status given by the MAC helps you to identify the type of message and take appropriate action.

The boundary clock is similar to the ordinary clock except for the following features:

- The clock data sets are common to all ports of the boundary clock.
- The local clock is common to all ports of the boundary clock.

End-to-End Transparent Clock

The end-to-end transparent clock supports the end-to-end delay measurement mechanism between the slave clocks and the master clock. The end-to-end transparent clock forwards all messages like normal bridge, router, or repeater. The residence time of a PTP packet is the time taken by the PTP packet from the Ingress port to the Egress port.

The residence time of a SYNC packet inside the end-to-end transparent clock is updated in the correction field of the associated Follow_Up PTP packet before it is transmitted. Similarly, the residence time of a Delay_Req packet, inside the end-to-end transparent clock, is updated in the correction field of the associated Delay_Resp PTP packet before it is transmitted. Therefore, the snapshot must be taken at both Ingress and Egress ports only for the messages mentioned inTable 47-16. You can take the snapshot by setting the SNAPTYPSEL bits to 10 in the MAC Timestamp Control register.

Table 47-16 End to End Transparent Clock: PTP Messages for Snapshot

PTP Messages
SYNC
Delay_Req

Peer-to-Peer Transparent Clock

In the peer-to-peer transparent clock, the computation of the link delay is based on an exchange of Pdelay_Req, Pdelay_Resp, and Pdelay_Resp_Follow_Up messages with the link peer.

The peer-to-peer transparent clock differs from the end-to-end transparent clock in the way it corrects and handles the PTP timing messages. In all other aspects, it is identical to the end-to-end transparent clock.

In the peer-to-peer transparent clock, the computation of the link delay is based on an exchange of Pdelay_Req, Pdelay_Resp, and Pdelay_Resp_Follow_Up messages with the link peer. The residence time of the Pdelay_Req and the associated Pdelay_Resp packets is added and inserted into the correction field of the associated Pdely_Resp_Followup packet. Therefore, support for taking snapshot for the event messages related to Pdelay is

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added as shown in Table 47-17.

Table 47-17 Peer-to-Peer Transparent Clock: PTP Messages for Snapshot

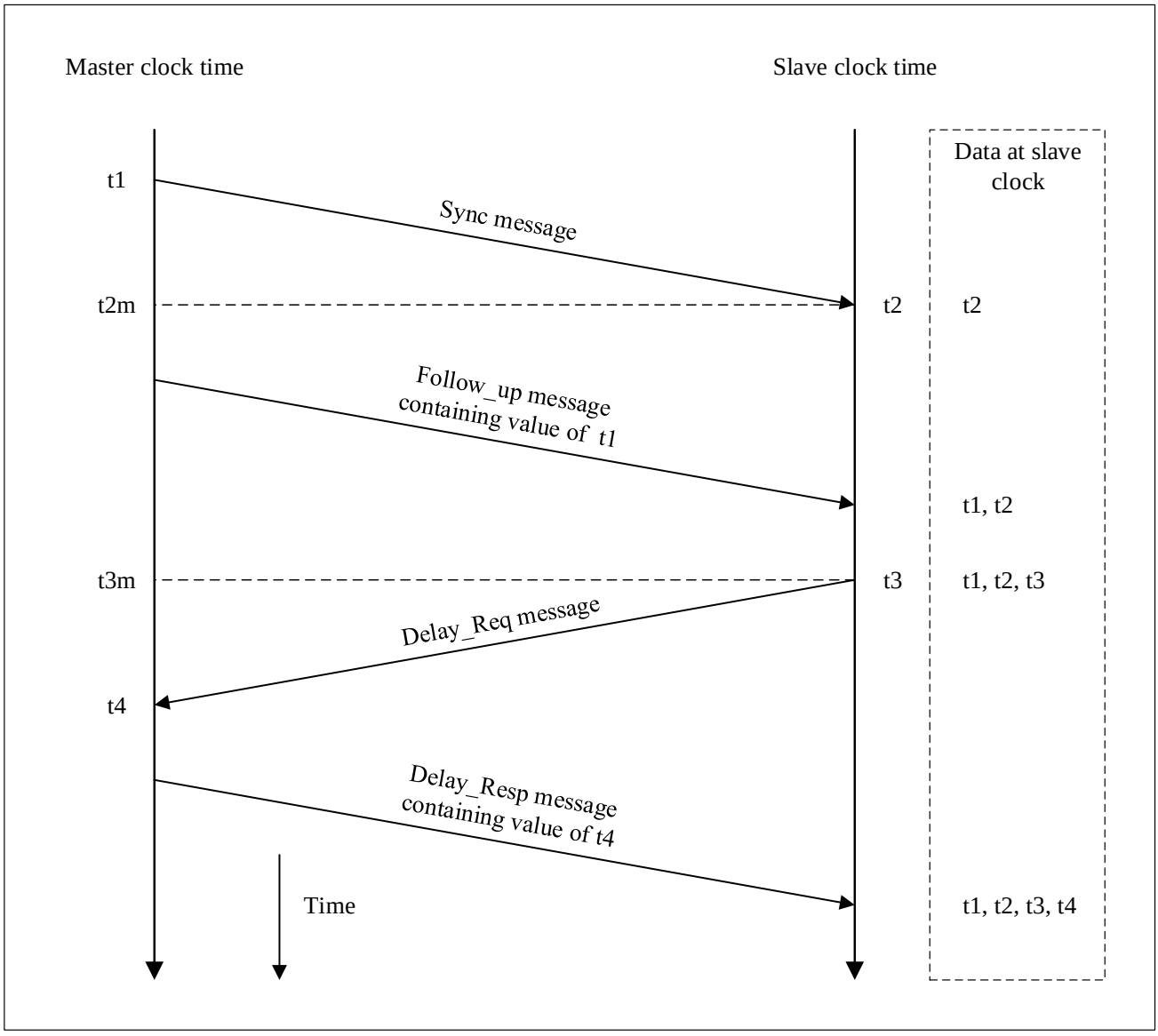
PTP Messages
SYNC
Pdelay_Req
Pdelay_Resp

You can take the snapshot by setting the SNAPTYPESEL bit to 11 in MAC Timestamp Control register.

47.5.6.2 Delay Request-Response Mechanism

The system or network is classified into the master and slave nodes for distributing the timing and clock information. Figure 47-15 shows the process that PTP uses for synchronizing a slave node to a master node by exchanging PTP messages.

Figure 47-15 Networked Time Synchronization



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As shown in Figure 47-15, PTP uses the following process:

1. The master broadcasts the PTP Sync messages to all its nodes. The Sync message contains the reference time information of the master. This message leaves the system of the master at t1. This time must be captured for Ethernet ports at GMII or MII.
2. The slave receives the Sync message and also captures the exact time, t2, using its timing reference.
3. The master sends a Follow_up message to the slave, which contains t1 information for later use.
4. The slave sends a Delay_Req message to the master and notes the exact time, t3, at which this packet leaves the GMII or MII interface.
5. The master receives the message, capturing the exact time t4, at which the message enters its system.
6. The master sends the t4 information to the slave in the Delay_Resp message.
7. The slave uses the four values of t1, t2, t3, and t4 to synchronize its local timing reference to the timing reference of the master.

Most of the PTP implementation is done in the software above the Ethernet/UDP layer. However, the hardware support is required to capture the exact time when specific PTP packets enter or leave the Ethernet port at the GMII or MII interface. This timing information must be captured and returned to the software for proper implementation of PTP with high accuracy.

47.5.6.3 Peer-to-Peer PTP Transparent Clock (P2P TC) Message

The IEEE 1588-2008 supports peer-to-peer PTP (Pdelay) message in addition to the SYNC, Delay Request, Follow-up, and Delay Response messages. Figure 47-16 shows the method to calculate the propagation delay in clocks supporting peer-to-peer path correction.

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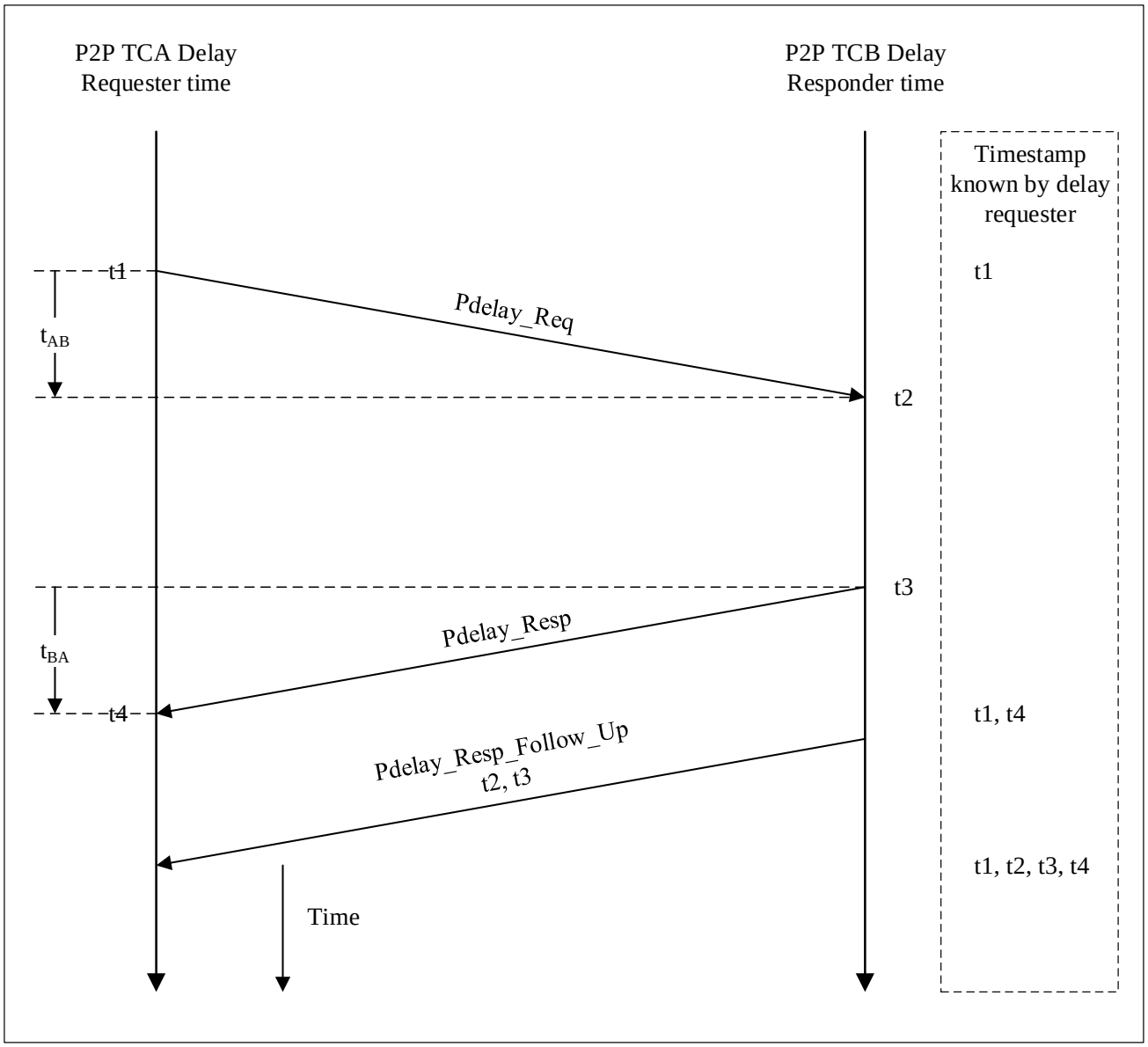
Figure 47-16 Propagation Delay Calculation in Clocks Supporting Peer-to-Peer Path Correction



As shown in Figure 47-16, the propagation delay is calculated in the following way:

1. Port 1 issues a Pdelay_Req message and generates a timestamp (t1) for the Pdelay_Req message.
2. Port 2 receives the Pdelay_Req message and generates a timestamp (t2) for this message.
3. Port 2 returns a Pdelay_Resp message and generates a timestamp (t3) for this message.

   To minimize errors because of any frequency offset between the two ports, Port 2 returns the Pdelay_Resp message as quickly as possible after the receipt of the Pdelay_Req message. Port 2 returns any one of the following:

   - Difference between the timestamps t2 and t3 in the Pdelay_Resp message
   - Difference between the timestamps t2 and t3 in the Pdelay_Resp_Follow_Up message
   - Timestamps t2 and t3 in the Pdelay_Resp and Pdelay_Resp_Follow_Up messages, respectively

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4. Port 1 generates a timestamp (t4) on receiving the Pdelay_Resp message.

5. Port 1 uses all four timestamps to compute the mean link delay.

47.5.6.4 Timestamp Correction

According to the IEEE 1588 specification, a timestamp must be captured when the PTP message timestamp point (leading edge of the first bit of the octet immediately following the Start Frame Delimiter octet) crosses the boundary between the node and the network. As the MAC takes the timestamp at an internal point far from the actual boundary of the node and network, this captured timestamp is corrected/updated for the ingress/egress path latency (including the delay in the PHY layers). Further correction is done for the inaccuracies/errors introduced due to the clock (GMII Tx, Rx clock) being different at the capture point as compared to the PTP clock (clk_ptp_ref_i) that is used to generate the time. The resultant CDC (Clock Domain Crossing) circuits add error depending on the clock period of the GMII and PTP clocks.

Ingress Correction

In the Receive side the timestamp captured at the internal snapshot point is delayed (later in time) as compared to the time at which that packet's SFD bit is received at the port's boundary. Therefore, the captured timestamp must be reduced by the ingress latency and the errors in CDC sampling. This correction value must be determined/calculated by the software and written into the MAC Timestamp Ingress Corr registers.

The correction value consists of the following 3 components:

1. External latency in the PHY layer between boundary point and the input of the core.

   If the PHY is compliant to the IEEE 802.3 Clause 45 MMD registers, it has a register indicating the maximum and minimum ingress latency. The software can read these registers and determine the average ingress latency in the PHY. Alternatively (if the PHY does not support these registers), the ingress latency must be determined from its datasheet or timing characteristics.

2. Internal latency from the input of the core to the internal capture point.

   The internal ingress latency can be read from the MAC Ingress Timestamp Latency register. This is a read-only register and gives the latency in scaledNanoseconds format defined in IEEE 1588 Clause 5.3.2. The latency differs based on the active PHY interface (RGMII, RMII, so on) and the operating speed. Therefore, the software must read this register after any speed change in the MAC to determine the current internal latency.

3. CDC Synchronization.

   The CDC synchronization error is almost equal to 2 times the clock-period of the PTP clock (clk_ptp_ref_i).

The values determined from these 3 components should be added by the software and must be written into the TSIC & TSICSNS fields of the MAC Timestamp Ingress Corr registers.

Note: The value written to the register must be negative (two's complement), because it has to be subtracted from the captured timestamp. The MAC Receiver adds the value in this register to the captured timestamp and then gives the resultant value as the timestamp of the received packet.

When TSCTRLSSR bit in MAC Timestamp Control register is set, the nanoseconds field of the captured timestamp is in decimal format with a granularity of 1ns. So the Bit31 of TSIC must be set to 1 (for negative value) and bits[30:0] must be written with "10^9 - total ingress correction value[nanosecond part]" represented in binary. For example, if

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Email: sales@nsing.com.sg

the required correction value is -5 ns, then the value is 0xBB9A_C9FB.

When TSCTRLSSR bit in MAC Timestamp Control register is reset, the nanoseconds field of the captured timestamp is in binary format with a granularity of ~0.466ns. Therefore, bits[30:0] must be written with "2^{31} - total ingress correction value" represented in binary with bit[31] = 1.

Egress Correction

In the Transmit side the timestamp captured at the internal snapshot point is earlier (advanced in time) as compared to the time at which that packet's SFD bit is output at the port's boundary. Therefore, the captured timestamp must be compensated by the egress latency and the errors in CDC sampling. This correction value must be determined/calculated by the software and written into the MAC Timestamp Egress Corr registers.

The correction value consists of the following 3 components:

1. External latency in the PHY layer between the output of the core and the boundary of the port and the network.

   If the PHY is compliant to the IEEE 802.3 Clause 45 MMD registers, it has a register indicating the maximum and minimum egress latency. The software can read these registers and determine the average egress latency in the PHY. Alternatively (if the PHY does not support these registers), the egress latency must be determined from its datasheet or timing characteristics.

2. Internal latency from the internal capture point and the output of the core.

   This internal egress latency can be read from the MAC Egress Timestamp Latency register. This is a read-only register and gives the latency in scaledNanoseconds format defined in IEEE 1588 Clause 5.3.2. The latency differs based on the active PHY interface (RGMII, RMII, so on) and the operating speed. Therefore, the software must read this register after any speed change in the MAC, to determine the current internal latency.

3. CDC synchronization error.

   The CDC synchronization error value differs depending on the One-step timestamping mode. When One-step timestamping is enabled, the value = (1 * period of clk_ptp_ref_i + 4 * period of clk_tx_i). Otherwise (Two-step timestamping mode), the value = -(2 * period of clk_ptp_ref_i).

47.5.6.5 PTP Processing and Control

Table 7-6 shows the common message header for the PTP messages. This format is taken from the IEEE 1588-2008.

Table 47-18 PTP Message Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Octet	Offset
transportSpecific				messageType				1	0
Reserved				versionPTP				1	1
messageLength								2	2
domainNumber								1	4
Reserved								1	5
flagField								2	6
correctionField								8	8
Reserved								4	16
sourcePortIdentity								10	20

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Email: sales@nsing.com.sg

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Octet	Offset
sequenceId								2	30
controlField(1)								1	32
logMessageInterval								1	33

1. control Field is used in version 1. In version 2, message Type field is used for detecting different message types.

There are some fields in the Ethernet payload that you can use to detect the PTP packet type and control the snapshot to be taken. These fields are different for the following PTP packets:

PTP Packets Over IPv4 Table 47-19 provides information about the fields that are matched to control snapshot for the PTP packets sent over UDP over IPv4 for IEEE 1588 version 1 and 2. The octet positions for the tagged packets are offset by 4. This is based on the IEEE 1588-2008 and the message format defined in Table 47-18.

Table 47-19 IPv4-UDP PTP Packet Fields Required for Control and Status

Field Matched	Octet Position	Matched Value	Description
MAC Packet Type	12,13	0x0800	IPv4 datagram
IP version and Header Length	14	0x45	IP version is IPv4
Layer 4 Protocol	23	0x11	UDP
IP Multicast Address (IEEE 1588 version 1)	30,31,32,33	0xE0, 0x00, 0x01, 0x81 (/0x82/0x83/0x84)	Multicast IPv4 addresses allowed: ■ 224.0.1.129 ■ 224.0.1.130 ■ 224.0.1.131 ■ 224.0.1.132
IP Multicast Address (IEEE 1588 version 2)	30,31,32,33	0xE0, 0x00, 0x01, 0x81 0xE0, 0x00, 0x00, 0x6B	■ PTP Primary multicast address: 224.0.1.129 ■ PTP Pdelay multicast address: 224.0.0.107
UDP Destination Port	36,37	0x013F, 0x0140	■ 0x013F: PTP event messages (1) ■ 0x0140: PTP general messages
PTP Control Field (IEEE 1588 version 1)	74	0x00, 0x01, 0x02, 0x03, 0x04	■ 0x00: SYNC ■ 0x01: Delay_Req ■ 0x02: Follow_Up ■ 0x03: Delay_Resp ■ 0x04: Management
PTP Message Type Field (IEEE 1588 version 2)	42 (nibble)	0x0, 0x1, 0x2, 0x3, 0x8, 0x9, 0xB, 0xC, 0xD	■ 0x0: SYNC ■ 0x1: Delay_Req ■ 0x2: Pdelay_Req ■ 0x3: Pdelay_Resp ■ 0x8: Follow_Up ■ 0x9: Delay_Resp ■ 0xA:

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Field Matched	Octet Position	Matched Value	Description
			Pdelay_Resp_Follow_Up ■ 0xB: Announce ■ 0xC: Signaling ■ 0xD: Management
PTP Version	43 (nibble)	0x1/0x2	■ 0x1: PTP version 1 ■ 0x2: PTP version 2

1. PTP event messages are SYNC, Delay_Req (IEEE 1588 version 1 and 2) or Pdelay_Req, Pdelay_Resp (IEEE 1588 version 2 only).

PTP Frames Over IPv6

Table 47-20 provides information about the fields that are matched to control the snapshots for the PTP packets sent over UDP over IPv6 for IEEE 1588 version 1 and 2. The octet positions for the tagged packets are offset by 4. This is based on the IEEE 1588-2008 and the message format defined in Table 47-18.

Table 47-20 IPv6-UDP PTP Packet Fields Required for Control and Status

Field Matched	Octet Position	Matched Value	Description
MAC Packet Type	12,13	0x86DD	IPv4 datagram
IP version	14	0x6	IP version is IPv6
Layer 4 Protocol	20(1)	0x11	UDP
IP Multicast Address (IEEE 1588 version 1)	38~53	FF0x:0:0:0:0:0:0:181 (Hex) FF02:0:0:0:0:0:0:6B (Hex)	■ PTP Primary multicast address: FF0x:0:0:0:0:0:0:0:181 (Hex) ■ PTP Pdelay multicast address: FF02:0:0:0:0:0:0:0:6B (Hex)
UDP Destination Port	56,57a	0x013F, 0x0140	■ 0x013F: PTP event message ■ 0x0140: PTP general messages
PTP Control Field (IEEE 1588 version 1)	94a	0x00, 0x01, 0x02, 0x03, 0x04	■ 0x00: SYNC ■ 0x01: Delay_Req ■ 0x02: Follow_Up ■ 0x03: Delay_Resp ■ 0x04: Management (version 1)
PTP Message Type Field (IEEE 1588 version 2)	62a (nibble)	0x0, 0x1, 0x2, 0x3, 0x8, 0x9, 0xB, 0xC, 0xD	■ 0x0: SYNC ■ 0x1: Delay_Req ■ 0x2: Pdelay_Req ■ 0x3: Pdelay_Resp ■ 0x8: Follow_Up ■ 0x9: Delay_Resp

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Field Matched	Octet Position	Matched Value	Description
			■ 0xA: Pdelay_Resp_Follow_Up ■ 0xB: Announce ■ 0xC: Signaling ■ 0xD: Management
PTP Version	63 (nibble)	0x1/0x2	■ 0x1: PTP version 1 ■ 0x2: PTP version 2

1. The Extension Header is not defined for PTP packets.

PTP Packets Over Ethernet

Table 47-21 provides information about the fields that are matched to control the snapshots for the PTP packets sent over Ethernet for IEEE 1588 version 1 and 2. The octet positions for the tagged packets are offset by 4. This is based on the IEEE 1588-2008 and the message format defined in Table 47-18.

Table 47-21 Ethernet PTP Packet Fields Required for Control And Status

Field Matched	Octet Position	Matched Value	Description
MAC Destination Multicast Address (1)	0~5	01-1B-19-00-00-00 01-80-C2-00-00-0E	All PTP messages can use any of the following multicast addresses: ■ 01-1B-19-00-00-00 ■ 01-80-C2-00-00-0E(2)
MAC Packet Type	12,13	0x88F7	PTP Ethernet packet
PTP Control Field (IEEE 1588 version 1)	46	0x00, 0x01, 0x02, 0x03, 0x04	■ 0x00: SYNC ■ 0x01: Delay_Req ■ 0x02: Follow_Up ■ 0x03: Delay_Resp ■ 0x04: Management
PTP Message Type Field (IEEE 1588 version 2)	14 (nibble)	0x0, 0x1, 0x2, 0x3, 0x8, 0x9, 0xB, 0xC, 0xD	■ 0x0: SYNC ■ 0x1: Delay_Req ■ 0x2: Pdelay_Req ■ 0x3: Pdelay_Resp ■ 0x8: Follow_Up ■ 0x9: Delay_Resp ■ 0xA: Pdelay_Resp_Follow_Up ■ 0xB: Announce ■ 0xC: Signaling ■ 0xD: Management
PTP Version	15 (nibble)	0x1/0x2	■ 0x1: PTP version 1 ■ 0x2: PTP version 2

1. The unicast address match of destination addresses (DA), programmed in MAC address 0 to 31, is used if the TSENMACADDR

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bit of MAC Timestamp Control register is set.

2. The MAC does not consider the PTP version 1 messages with Peer delay multicast address (01-80-C2-00-00-0E) as valid PTP messages.

47.5.6.6 Transmit Path Functions

The MAC captures a timestamp when the Start Packet Delimiter (SFD) of a packet is sent on the GMII or MII interface. The packets, for which the timestamps has to be captured can be controlled on per-packet basis. Each Transmit packet can be marked to indicate whether a timestamp should be captured for it.

The MAC does not process the transmitted packets to identify the PTP packets. You need to specify the packets for which you want to capture timestamps. You can specify the packets by using the control bits in the Transmit descriptor. The MAC returns the timestamp to the software inside the corresponding Transmit descriptor, thus connecting the timestamp automatically to the specific PTP packet.

The 64-bit timestamp information is written to the TDES0 and TDES1 fields. The TDES0 field holds the 32 least significant bits of the timestamp.

47.5.6.7 Receive Path Functions

The MAC can be programmed to capture the timestamp of all packets received on the GMII or MII interface or to process packets to identify the valid PTP messages. Use the following options of the MAC Timestamp Control register to control the snapshot of the time to be sent to the application:

- Enable snapshot for all packets
- Enable snapshot for IEEE 1588 version 1 or version 2 timestamp
- Enable snapshot for PTP packets transmitted directly over Ethernet or UDP-IP-Ethernet
- Enable timestamp snapshot for the received packet for IPv4 or IPv6
- Enable timestamp snapshot only for EVENT messages (SYNC, DELAY_REQ, PDELAY_REQ, or PDELAY_RESP)
- Enable the node to be a master or slave and select the snapshot type

  This feature controls the type of messages for which snapshots are taken.

Note: The Ethernet peripheral also supports the PTP messages over VLAN packets.

Table 47-22 Timestamp Snapshot Dependency on Register Bits

SNAPTYPSEL	TSMSTRENA	TSEVNTENA	PTP Messages
00	x	0	SYNC, Follow_Up, Delay_Req, Delay_Resp
00	0	1	SYNC
00	1	1	Delay_Req
01	x	0	SYNC, Follow_Up, Delay_Req, Delay_Resp, Pdelay_Req, Pdelay_Resp, Pdelay_Resp_Follow_Up
01	0	1	SYNC, Pdelay_Req, Pdelay_Resp
01	1	1	Delay_Req, Pdelay_Req, Pdelay_Resp
10	x	x	SYNC, Delay_Req

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SNAPTYPSEL	TSMSTRENA	TSEVNTENA	PTP Messages
00	x	0	SYNC, Follow_Up, Delay_Req, Delay_Resp
11	x	x	Pdelay_Req, Pdelay_Resp

The DMA returns the timestamp to the software inside the corresponding Receive Descriptor. The extended status, containing the timestamp message status and the IPC status, is written in normal descriptor RDES1 and the snapshot of the timestamp is written in RDES0 and RDES1 fields of context descriptor. The RDES0 field holds the 32 least significant bits of the timestamp.

47.5.6.8 IEEE 1588 System Time Source

To get a snapshot of the time, the MAC requires a reference time in 64-bit format as defined in the IEEE 1588-2002 (80-bit format as defined in the IEEE 1588-2008). The Ethernet peripheral takes only the reference clock input and uses it to internally generate the Reference time (also called the system time) and capture timestamps.

When the internal reference time is used as the system time source, the timestamp has the following fields:

- UInteger48 seconds Field

  The seconds field is the integer portion of the timestamp in units of seconds. It is 48-bits wide. For example, 2.000000001 seconds are represented as seconds Field = 0x0000_0000_0002.

- UInteger32 nano secondsField

  The nanoseconds field is the fractional portion of the timestamp in units of nanoseconds. For example, 2.000000001 seconds are represented as nanoSeconds = 0x0000_0001. The nanoseconds field supports the following two modes:

  – Digital rollover mode: In this mode, the maximum value in the nanoseconds field is 0x3B9A_C9FF, that is, (10e9-1) nanoseconds.

  – Binary rollover mode: In this mode, the nanoseconds field rolls over and increments the seconds field after value 0x7FFF_FFFF. Accuracy is ~0.466 ns per bit.

47.5.6.9 System Time Register Module

The system time generator module is an optional module. It is not available if external time updating is enabled. The 80-bit time is maintained in this module and updated using the input reference clock (clk_ptp_ref_i). This time is the source for taking snapshots (timestamps) of Ethernet packets being transmitted or received at the GMII interface.

The system time counter can be initialized or corrected using the coarse correction method. In this method, the initial value or the offset value is written to the Timestamp Update register. For initialization, the system time counter is written with the value in the Timestamp Update register. For system time correction, the offset value is added to or subtracted from the system time.

In the fine correction method, the frequency offset and/or frequency drift of a slave clock (clk_ptp_ref_i) with respect to the master clock (as defined in IEEE 1588-2002) is corrected over a period of time instead of in one clock, as in coarse correction. This helps maintain linear time and does not introduce drastic changes (or a large jitter) in the reference time between PTP Sync message intervals. In this method, an accumulator sums up the contents of the Addend register, as shown in Figure 47-17. The arithmetic carry that the accumulator generates is used as a pulse to increment the system time counter. The accumulator and the addend are 32-bit registers. The accumulator acts as a high-precision frequency multiplier or divider.

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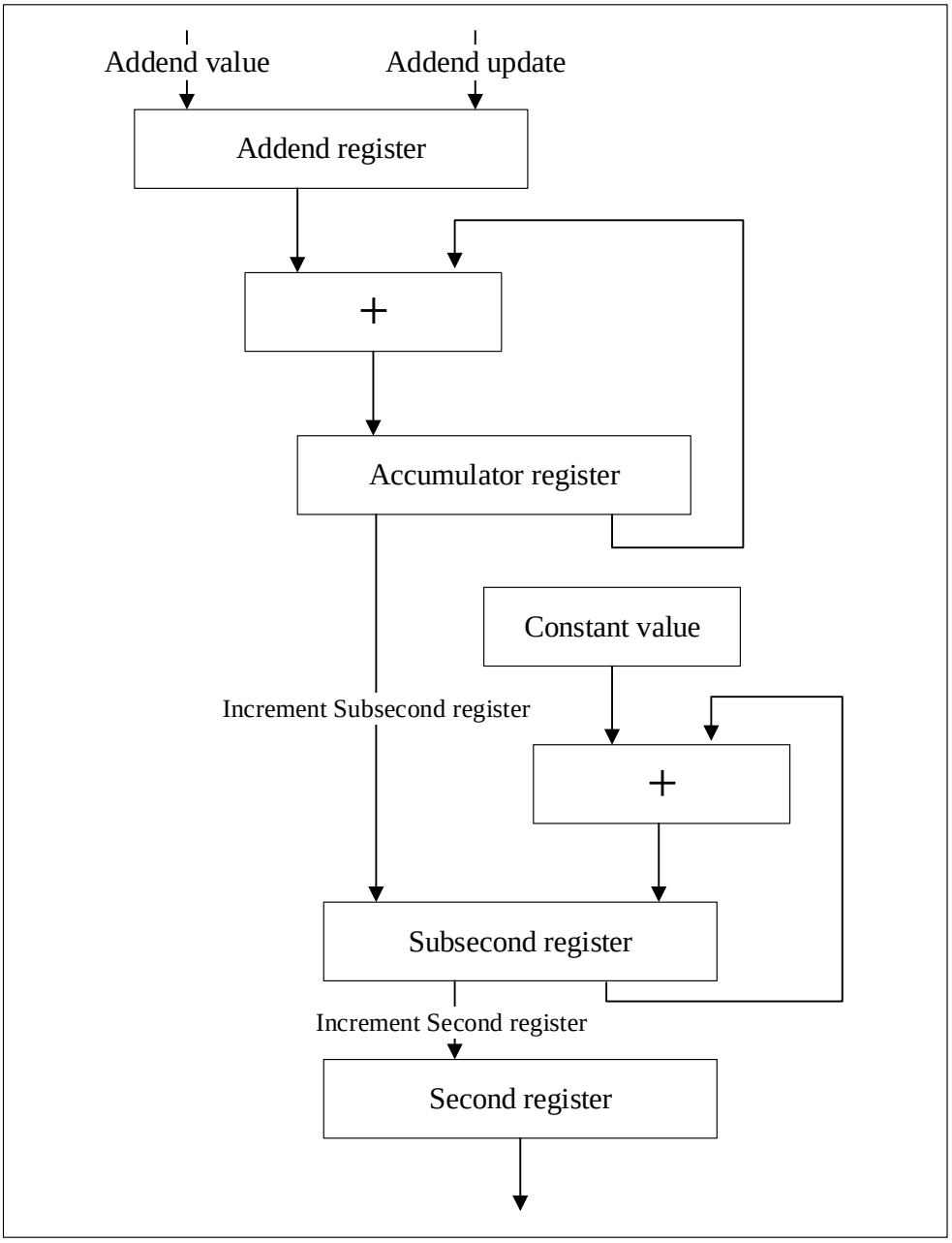
Note: You must connect a PTP clock with a frequency higher than the frequency required for the specified accuracy.

Figure 47-17 System Time Update Using Fine Method



The System Time Update logic requires a 50-MHz clock frequency to achieve 20-ns accuracy. The frequency division is the ratio of the reference clock frequency to the required clock frequency. For example, if the reference clock (clk_ptp_ref_i) is 66 MHz, this ratio is calculated as 66 MHz / 50 MHz = 1.32. Therefore, the default addend value to be set in the register is 2^{32}/ 1.32, 0xC1F07C1F.

If the reference clock drifts lower, for example, to 65 MHz, the ratio is 65 / 50, or 1.3 and the value to set in the addend register is 2^{32} / 1.30, or 0xC4EC4EC4. If the clock drifts higher, for example, to 67 MHz, the addend register must be set to 0xBF0B7672. When the clock drift is nil, the default addend value of 0xC1F07C1F (2^{32} / 1.32) must be programmed.

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In Figure 47-17, the constant value used to accumulate the sub-second register is decimal 43, which achieves an accuracy of 20 ns in the system time (in other words, it is incremented in 20 ns steps). When External Time Update is enabled, the optional System Time module is not available.

The software must calculate the drift in frequency based on the Sync messages and accordingly update the Addend register.

Initially, the slave clock is set with FreqCompensationValue0 in the Addend register. This value is as follows:

$$FreqCompensationValue0 = 2^{32} / FreqDivisionRatio$$

If MasterToSlaveDelay is initially assumed to be the same for consecutive Sync messages, the algorithm given in this section must be applied. After a few Sync cycles, frequency lock occurs. The slave clock can then determine a precise MasterToSlaveDelay value and re-synchronize with the master using the new value.

The algorithm is as follows:

- At time $MasterSyncTime_n$ the master sends the slave clock a Sync message. The slave receives this message when its local clock is $SlaveClockTime_n$ and computes $MasterClockTime_n$ as $MasterClockTime_n = MasterSyncTime_n + MasterToSlaveDelay_n$
- The master clock count for current Sync cycle, $MasterClockCount_n$ is $MasterClockCount_n = MasterClockTime_n – MasterClockTime_n – 1$ (assuming that MasterToSlaveDelay is the same for Sync cycles n and n – 1)
- The slave clock count for current Sync cycle, $SlaveClockCount_n$ is $SlaveClockCount_n = SlaveClockTime_n – SlaveClockTime_n – 1$
- The difference between master and slave clock counts for current Sync cycle, $ClockDiffCount_n$ is $ClockDiffCount_n = MasterClockTime_n – SlaveClockTime_n$
- The frequency-scaling factor for slave clock, $FreqScaleFactor_n$ is $FreqScaleFactor_n = (MasterClockCount_n + ClockDiffCount_n) / SlaveClockCount_n$
- The frequency compensation value for Addend register, $FreqCompensationValue_n$ is $FreqCompensationValue_n = FreqScaleFactor_n * FreqCompensationValue_n – 1$

In theory, this algorithm achieves lock in one Sync cycle. However, it may take several cycles, because of changing network propagation delays and operating conditions. This algorithm is self-correcting. If the slave clock is initially set to an incorrect value from the master, the algorithm corrects it at the cost of more Sync cycles.

47.5.6.10 IEEE 1588 Higher Word Register

The timestamp maintained in the MAC is 64-bit wide. The overflow to upper 16-bits of seconds register happens once in 130 years. The values of the upper 16-bits of the seconds field can be read from the CSR register.

47.5.6.11 IEEE 1588 Auxillary Snapshot

The auxiliary snapshot feature allows you to store a snapshot of the system time based on an external event. The event is considered to be the rising edge of the ptp_aux_ts_trig_i sideband signal. Up to 4 auxiliary snapshot inputs can be configured.

The snapshots taken for any input are stored in a common FIFO. The application can read the MAC Timestamp Status register to know the timestamp of which input is available for reading at the top of this FIFO.

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Email: sales@nsing.com.sg

The MAC stores these snapshots in a FIFO. Only 64-bits of the timestamp are stored in the FIFO. You can read the upper 16-bits of seconds from the MAC System Time Higher Word Seconds register when it is present. When a snapshot is stored, the MAC indicates this to the application with an interrupt. The value of the snapshot is read through a FIFO register access. If the FIFO becomes full and an external trigger to take the snapshot is asserted, a snapshot trigger-missed status (ATSSTM) is set in the MAC Timestamp Status register. This indicates that the latest auxiliary snapshot of the timestamp is not stored in the FIFO. The latest snapshot is not written to the FIFO when it is full.

When an application reads the 64-bit timestamp from the FIFO, the space becomes available to store the next snapshot. You can clear a FIFO by setting the ATSFC bit in MAC Auxiliary Control register. When multiple snapshots are present in the FIFO, the count is indicated in Bits[27:25] of MAC Timestamp Status register.

47.5.6.12 Flexible Pulse-Per-Second Output

The Ethernet peripheral provides the flexibility to program the start or stop time, width, and interval of the pulse generated on the ptp_pps_o output.

Note: By default, Ethernet peripheral is in the "Fixed Pulse-Per-Second Output" mode (fixed mode for short) and indicates 1 second interval. When fixed mode is selected by setting PPSEN0 = 0 in the MAC PPS Control register, the output on all PPS outputs is controlled by the value programmed in the PPSCTRL_PPSCMD field. Independent control of individual PPS output is not supported in the fixed mode. MAC PPS Target Time Seconds/Nanoseconds registers are used only for generating target time reached interrupt; they are not used for PPS output generation. TRGTMODSEL0 must be programmed to 0. The frequency of the PPS output can be changed by setting the PPSCTRL0 field in the MAC PPS Control register.

The Ethernet peripheral supports the following features with the flexible PPS output:

- Programming the start or stop time in terms of system time.
- Programming the start point of the single pulse and start and stop points of the pulse train in terms of 64-bit system time. The Target Time registers are used to program the start and stop time.
- Programming the stop time in advance, that is, you can program the stop time before the actual start time has elapsed.
- Programming the width between the rising edge and corresponding falling edge of PPS signal output in terms of number of units of sub-second increment value programmed in the MAC Sub Second Increment register. You can program the width of pulse from 1 to 2^{32}-1 units of sub-second increment value.
- Programming the interval, between the rising edges of PPS signal, in terms of number of units of sub-second increment value. You can program the interval between pulses from 1 to 2^{32}-1 units of sub-second increment value.
- Option to cancel the programmed PPS start or stop request.
- Error if the start or stop time being programmed has already elapsed.

Note: The PTP Reference clock mentioned in the following sections is the clock at which the system time gets updated. When the TSCFUPDT bit of MAC Timestamp Control register is set to 0, this clock is similar to the clk_ptp_ref_i clock. In the Fine Correction mode, this is the clock tick at which the system time gets updated (using MAC Sub Second Increment register (as shown in Figure 47-17).

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PPS Start or Stop Time

You can initially program the start time in the Target Time registers.

If required, you can again program the start or stop time but you can do it only after the earlier programmed value is synchronized to the PTP clock domain. Bit 31 of MAC PPS Target Time Nanoseconds register indicates that the synchronization is complete. This enables you to program the start or stop time in advance even before the earlier stop or start time has elapsed.

To ensure proper PPS signal output, you should program advanced system time for the start or stop time. If the application programs a start or stop time that has already elapsed, the MAC sets an error status bit indicating the programming error. If enabled, the MAC also sets the Target Time Reached interrupt event. The application can cancel the start or stop request only if the corresponding start or stop time has not elapsed. If the time has elapsed, the cancel command has no effect.

PPS Width and Interval

The PPS width and interval are programmed in terms of granularity of system time, that is, number of the units of sub-second increment value. For example, to have a PPS pulse width of 40 ns and interval of 100 ns with PTP reference clock of 50 MHz, you should program the width and interval to values 2 and 5, respectively. You can achieve smaller granularity by using a faster PTP reference clock.

Before giving the command to trigger a pulse or pulse train on the PPS output, you should program or update the interval and width of the PPS signal output.

47.5.6.13 PTP Timestamp Offload

PTP Timestamp Offload Function is an optional feature that enables the automatic generation of specific PTP packets when the MAC is working as a specific node in the PTP network.

These packets may be generated periodically or triggered by the host software. In other modes, this feature can parse the incoming PTP packets on the receiver, and automatically generate and respond to the required PTP packets. This helps in offloading certain functions of a PTP node with better accuracy and lower latency of responses.

Based on the programmed mode, the MAC generates PTP Ethernet messages periodically or from the application, or based on reception of a particular PTP message.

Table 47-23 indicates the PTP message generation criteria.

Table 47-23 PTP Message Generation Criteria

SNAPTYPSEL	TSMSTRENA	TSEVNTENA	Mode	Criteria for Generation of PTP Messages	PTP Message Type Generated
2'b00	0	1	Ordinary or Boundary Slave	SYNC message reception	Delay_Req
2'b00	1	1	Ordinary or Boundary Master	Periodic or on trigger from application	SYNC
				Delay_Req message reception	Delay_Resp
2'b01	0	1	Transparent Slave	Periodic or on trigger from application	Pdelay_Req

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SNAPTYPSEL	TSMSTRENA	TSEVNTENA	Mode	Criteria for Generation of PTP Messages	PTP Message Type Generated
				Pdelay_Req message reception	Pdelay_Resp
				SYNC message reception	Delay_Req
2'b01	1	1	Transparent Master	Periodic or on trigger from application	Pdelay_Req
				Pdelay_Req message reception	Pdelay_Resp
				Periodic or on trigger from application	SYNC
				Delay_Req message reception	Delay_Resp
2'b11	x	x	Peer-to-Peer Transparent	Periodic or on trigger from application	Pdelay_Req
				Pdelay_Req message reception	Pdelay_Resp
All other programming combinations are invalid for PTP Offload feature.					

Note: Clocks supporting peer delay mechanism must not generate delay request/delay response messages, according to IEEE 1588-2008 specification. However, the Ethernet peripheral controller supports this for flexibility, with a programmable control bit (DRRDIS). You can use the DRRDIS bit to control the response generation for delay request/delay response message. For example, in transparent slave mode, delay request is generated in response to received sync only when the bit is reset.

For example, when the MAC is set as an Ordinary or Boundary Slave clock in the PTP network, it can respond to the reception of SYNC messages with an automatic generation and transmission of the corresponding Delay_Req message. Similarly, various other modes of operation are explained inTable 47-23.

The MAC supports the multicast communication model for the generation of SYNC and Pdelay_Req PTP messages. For instance, the Destination Address field of the generated PTP over Ethernet packet is the defined special multicast addresses (0x011B19000000 for all except peer delay mechanism messages and 0x0180C200000E for peer delay mechanism messages).

When the MAC responds to received SYNC, Delay_Req and Pdelay_Req PTP messages with special multicast destination address, it also uses the corresponding special multicast address in the DA field of the automatically generated Delay_Req, Delay_Resp, and Pdelay_Resp PTP messages, respectively.

When the MAC responds to received SYNC, Delay_Req and Pdelay_Req PTP messages with unicast destination address, it takes the SA field of the received packets and makes them as the DA field of the automatically generated Delay_Req, Delay_Resp, and Pdelay_Resp PTP messages, respectively.

At the same time, all the received PTP messages are forwarded to the application along with Rx status, indicating whether the response was generated by the MAC, if it satisfies the packet filtering logic of the MAC receiver.

When the MAC automatically generates a PdelayReq or responds with a Delay_Req, the egress timestamp of these two PTP messages are provided in the Tx TS status (Tx Timestamp Status register and interrupt generated).

In addition to messageType and versionPTP fields match for basic PTP over Ethernet message detection, the following additional fields are matched to qualify the received PTP message type:

1. The domainNumber field is checked for a match against the value programmed in the CSR.

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2. The twoStepFlag in flagField field is checked for one-step indication (1'b0).
3. The transportSpecific field is checked for Default PTP over Ethernet (4'h0) or 802.1AS mode (4'h1) when enabled.

PTP Packet Generation

This section explains the format and content of the automatically generated PTP packets by the MAC when this mode is enabled. The template of the Common PTP Message Header is provided, as well as the detailed description of the fields of specific PTP packets generated. See Table 47-18 for fields in the PTP message header.

- messageType

  The following encoded values are used for PTP message types:

  – SYNC - 4'h0
  – Delay_Req - 4'h1
  – Pdelay_Req - 4'h2
  – Pdelay_Resp - 4'h3
  – Delay_Resp - 4'h9

- transportSpecific

  The following transport protocol encoding is used:

  – Default PTP over Ethernet - 4'h0
  – 802.1AS mode - 4'h1

- versionPTP

  It is always set to 2 because PTP version 2 is supported.

- domainNumber

  This contains the value from the MAC PTO Control register.

- flagField

  The following values are used:

  – alternateMasterFlag (Octet 0 bit 0) - 1b0 for SYNC and Delay_Resp
  – twoStepFlag (Octet 0 bit 1) - 1'b0 for SYNC and Pdelay_Resp
  – unicastFlag (Octet 0 bit 2) - 1'b0 for Multicast Address, 1'b1 for Unicast Address

- correctionField

  For more information, see Table 47-24.

- sourcePortIdentity

  This field takes the value programmed in the MAC Source Port Identityx registers.

- sequenceId

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Pdelay_Resp and Delay_Resp use the same sequenceId field from received Pdelay_Req and Delay_Req PTP messages. For SYNC/Delay_Req, Pdelay_Req, a separate sequenceId counter is maintained. These sequenceId counters get incremented by 1 every time the corresponding message is generated and transmitted.

- controlField

  The following encoded values are used for controlField:

  – SYNC - 8'h00

  – Delay_Req - 8'h01

  – Pdelay_Req - 8'h02

  – Pdelay_Resp - 8'h05

  – Delay_Resp - 8'h03

- logMessageInterval

  – SYNC - This contains logSyncInterval from the corresponding MAC Log Message Interval register.

  – Delay_Resp - This contains the sum of DRSYNCR and logSyncInterval value taken from the MAC Log Message Interval register for a multicast PTP message and 8'h7F for unicast PTP message.

  – Delay_Req, Pdelay_Req and Pdelay_Resp - 8'h7F where logSyncInterval = log2 (Mean Value of Interval in seconds)

  The MAC supports values of -15 to 15 for logSyncInterval fields, which translates to a range from 32.768 micro second (2^{-15}) to 215 second. For a given value of log sync interval (N), the time interval between two SYNC packets is given by the following:

  – $2^{(30+N)}$ ns, when N is negative (-1 to -15)

  – 2^{N} seconds, when N is positive (0 to 15)

  For example:

  – When logSyncInterval is programmed to 1, the interval is 2^{1}; therefore, the SYNC message is sent once every 2 seconds.

  – When logSyncInterval is programmed to -1, the interval is 2^{-1} = 0.536 seconds; therefore, the SYNC message is sent once every 536 milliseconds. The value is 0.536 seconds, because 2^{-30} = 1 ns.

  – When logSyncInterval is programmed to -5, the interval is 2^{-5} = 33.55ms; therefore, the SYNC message is sent once every 33.55 milliseconds.

Note: The MAC uses the PTP system time to generate the intervals for periodic packet transmission. For negative values of log message interval programmed, the generated period may deviate from the value given by the equation $2^{(30+N)}$, because of the non-binary nature of the nanoseconds field of the system time.

- messageLength

  There is no suffix supported, so this field contains the length of the PTP message that includes 34 byte PTP common header and the body specific to the message type.

  For SYNC and Delay_Req packets, this field contains 44, whereas for Delay_Resp, Pdelay_Req and

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Pdelay_Resp, it contains 54.

- originTimestamp

  This field is the captured egress timestamp for SYNC, Delay_Req, and Pdelay_Req PTP messages.

- receiveTimestamp

  For Delay_Resp PTP message, this is the ingress timestamp of the corresponding received Delay_Req PTP message.

- requestingPortIdentity

  For Delay_Resp and Pdelay_Resp PTP messages, this is the sourcePortIdentity field taken from the corresponding received Delay_Req and Pdelay_Req PTP messages.

- requestReceiptTimestamp

  For the Pdelay_Resp PTP message, this field is set to 0.

47.5.6.14 One-Step Timestamp

The Ethernet peripheral supports the one-step timestamp feature. When the One step timestamp feature is enabled, the MAC identifies the offset in the packet and inserts the timestamp received from the application at that offset.

MAC Transmit PTP Mode

Depending upon the type of message and its mode, the MAC updates the following fields of Transmit PTP packets:

- correctionField in the PTP header of messages
- originTimestamp in SYNC, Delay_Req, and Pdelay_Req messages

Table 47-24 shows how the PTP mode is selected based on the settings of SNAPTYPSEL, TSMSTRENA, and TSEVNTENA bits of the MAC Timestamp Control register and the fields that are updated for the incoming PTP packets based on the message type in that mode, during the one-step timestamping operation.

Table 47-24 MAC Transmit PTP Mode and One-Step Timestamping Operation(1)

SNAPTYPSEL	TSMSTRENA	TSEVNTENA	Mode	TTSE(2)	OSTC(3)	TTS(4)	Messages Processed on Tx
x	x	x	N/A	1	x	x	Timestamp is captured and returned to application
x	x	x	N/A	x	0	x	OST operation is not performed (PTP packet is not modified)
2'b00	x	0	End-to-end transparent	0	1	Ingress TS	Sync (correction field for residence time and Ingress Asym cor)
							Delay_Req

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SNAPTYPSEL	TSMSTRENA	TSEVNTENA	Mode	TTSE(2)	OSTC(3)	TTS(4)	Messages Processed on Tx
							(correction field for residence time and Egress Asym Cor)
2'b00	0	1	Ordinary or Boundary Slave	1	1	x	Delay_Req (originTimestamp field) Delay_Req (correction field for Egress Asym cor)
2'b00	1	1	Ordinary or Boundary Master	0	1	x	Sync (originTimestamp field) Sync (correction field for sub-nanosecond cor)
2'b01	x	0	End-to-End Transparent with support for peer delay mechanism	0	1	Ingress TS	Sync (correction field for residence time and Ingress Asym cor)
						Ingress TS	Pdelay_Req (correction field for residence time and Egress Asym Cor)
						Ingress TS	Pdelay_Resp (correction field for residence time and Ingress Asym Cor)
2'b01	0	1	Ordinary or Boundary Slave with support for peer delay mechanism or Peer to Peer Transparent	0	1	Ingress TS	Sync (correction field for residence time and Ingress Asym cor) (applicable only for Peer to Peer transparent clock operation)
				1	1	x	Delay_Req (originTimestamp field) Delay_Req (correction field for Egress Asym cor)
				1	1	x	Pdelay_Req (originTimestamp field) Pdelay_Req (correction field for

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SNAPTYPSEL	TSMSTRENA	TSEVNTENA	Mode	TTSE(2)	OSTC(3)	TTS(4)	Messages Processed on Tx
							Egress Asym Cor)
				0	1	Ingress TS for Pdelay_Req	Pdelay_Resp (correction field for turnaround time and Ingress Asym Cor)
2'b01	1	1	Ordinary or Boundary Master with support for peer delay mechanism	0	1	x	Sync (originTimestamp field) Sync (correction field for sub-nanosecond cor)
				1	1	x	Pdelay_Req (originTimestamp field) Pdelay_Req (correction field for Egress Asym Cor)
				0	1	Ingress TS for Pdelay_Req	Pdelay_Resp (correction field for turnaround time and Ingress Asym Cor)
2'b10	x	x	End-to-End Transparen	0	1	Ingress TS	Sync (correction field for residence time and Ingress Asym cor)
						Ingress TS	Delay_Req (correction field for residence time and Egress Asym Cor)
2'b11	x	x	Peer-to-Peer Transparent	0	1	Ingress TS	Sync (correction field for residence time and Ingress Asym cor)
				1	1	x	Pdelay_Req (originTimestamp field) Pdelay_Req (correction field for Egress Asym Cor)
				0	1	Ingress TS for Pdelay_Req	Pdelay_Resp (correction field for turnaround time and Ingress Asym Cor)

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1. The per packet control values (TTSE, OSTC and TTS) provided here are the recommended settings used by devices in typical PTP operation.
2. TTSE represents TTSE bit of transmit descriptor. The TTSE function is independent of the OST function and the programmed operation mode for OST. The MAC captures and returns the timestamp when the TTSE bit is set.
3. OSTC represents OSTC bit of transmit descriptor.
4. TTS represents the timestamp value provided in the TTSH, TTSL fields of transmit descriptor.

Note: Residence time/ turnaround time is calculated as the difference between the captured timestamp (egress timestamp) and the ingress timestamp. When sub-nanosecond feature is enabled, residence time calculation includes sub-nanosecond accuracy. Clocks supporting peer delay mechanism do not use delay request or response, but it is included in OST for flexibility.

47.5.7 Transmit Checksum Offload

The MAC has a Checksum Offload Engine (COE) to support checksum calculation and insertion in the Transmit path, using which, the software can offload the task of checksum insertion to the hardware. In the transmit path MAC calculates the checksum and inserts it in the Tx packet. This feature helps in reducing the load on the software and can improve the overall throughput of the system.

The checksum offload engine module supports two types of checksum calculation and insertion. The checksum engine can be controlled for each packet by setting the CIC bits (TDES3 Bits[17:16]).

Note: The checksum for TCP, UDP, or ICMP is calculated over a complete packet, and then inserted into its corresponding header field. Because of this requirement, when this function is enabled, the Tx FIFO automatically operates in the store-and-forward mode even if the Ethernet peripheral is configured for Threshold (cut-through) mode.

Hint: See IETF specifications RFC 791, RFC 793, RFC 768, RFC 792, RFC 2460, and RFC 4443 for IPv4, TCP, UDP, ICMP, IPv6, and ICMPv6 packet header specifications, respectively.

47.5.7.1 IP Header Checksum Engine

In IPv4 datagrams, the integrity of the header fields is indicated by the 16-bit Header Checksum field (the eleventh and twelfth bytes of the IPv4 datagram). The COE detects an IPv4 datagram when the Type field of Ethernet packet has the value 0x0800 and the Version field of IP datagram has the value 0x4. The checksum field of the input packet is ignored during calculation and replaced with the calculated value.

Note: IPv6 headers do not have a checksum field. Therefore, the COE does not modify the IPv6 header fields.

The result of this IP header checksum calculation is indicated by the IP Header Error status bit in the Transmit status (bit 0 of Normal descriptor write-back format TDES3). This status bit is set whenever the values of the Ethernet Type field and the Version field of IP header are not consistent, or when the Ethernet packet does not have enough data, as indicated by the IP header Length field. In other words, this bit is set when an IP header error is asserted under the following circumstances:

- For IPv4 datagrams:
  - The received Ethernet type is 0x0800, but the Version field of IP header is not equal to 0x4.

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- The IPv4 Header Length field indicates a value less than 0x5 (20 bytes).
- The total packet length is less than the value given in the IPv4 Header Length field.

- For IPv6 datagrams:
  - The Ethernet type is 0x86dd but the IP header Version field is not equal to 0x6.
  - The packet ends before the IPv6 header (40 bytes) or extension header (as given in the corresponding Header Length field in an extension header) is completely received.

47.5.7.2 TCP/UDP/ICMP Checksum Engine

The TCP/UDP/ICMP Checksum Engine processes the IPv4 or IPv6 header (including extension headers) and determines whether the encapsulated payload is TCP, UDP, or ICMP. The checksum is calculated for the TCP, UDP, or ICMP payload and inserted into its corresponding field in the header. The Tx COE can work in the following two modes:

- The TCP, UDP, or ICMPv6 pseudo-header is not included in the checksum calculation and is assumed to be present in the Checksum field of the input packet. This engine includes the Checksum field in the checksum calculation, and then replaces the Checksum field with the final calculated checksum.
- The engine ignores the Checksum field, includes the TCP, UDP, or ICMPv6 pseudo-header data into the checksum calculation, and overwrites the checksum field with the final calculated value.

Note: For ICMP-over-IPv4 packets, the Checksum field in the ICMP packet must always be 16'h0000 in both modes, because pseudo-headers are not defined for such packets. If it does not equal 16'h0000, an incorrect checksum may be inserted into the packet.

The result of this operation is indicated by the Payload Checksum Error status bit in the Transmit Status vector (Bit 12 of Normal descriptor read format TDES1). This engine sets the Payload Checksum Error status bit when it detects that the packet has been forwarded to the MAC Transmitter engine in the store-and-forward mode without the end of packet (EOP) being written to the FIFO, or when the packet ends before the number of bytes indicated by the Payload Length field in the IP Header is received. When the packet is longer than the indicated payload length, the COE ignores them as stuff bytes, and no error is reported. When this engine detects the first type of error, it does not modify the TCP, UDP, or ICMP header. For the second error type, it still inserts the calculated checksum into the corresponding header field.

Table 47-25 describes the functions supported by Transmit Checksum Offload engine based on the packet type. When the MAC does not insert the checksum, it is indicated as “No” in the table.

Table 47-25 Transmit Checksum Offload Engine Functions for Different Packet Types

Packet Type	Hardware IP Header Checksum Insertion	Hardware TCP/UDP Checksum Insertion
Non-IPv4 or IPv6 packet	No	No
IPv4 with TCP, UDP, or ICMP	Yes	Yes
IPv4 packet has IP options (IP header is longer than 20 bytes)	Yes	Yes
Packet is an IPv4 fragment	Yes	No
IPv6 packet with the following next header fields in main or extension headers:		

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Packet Type	Hardware IP Header Checksum Insertion	Hardware TCP/UDP Checksum Insertion
■ Hop-by-hop options (in IPv6 main header)	■ Not Applicable	■ Yes
■ Hop-by-hop options (in IPv6 extension header)	■ Not Applicable	■ No
■ Destinations options	■ Not Applicable	■ Yes
■ Routing (with segment left 0)	■ Not Applicable	■ No
■ Routing (with segment left > 0)	■ Not Applicable	■ No
■ TCP, UDP, or ICMP	■ Not Applicable	■ Yes
■ Authentication	■ Not Applicable	■ No
■ Any other next header field in main or extension headers	■ Not Applicable	■ No
IPv4 packet has TCP header with Options fields	Yes	Yes
IPv4 Tunnels: ■ IPv4 packet in an IPv4 tunnel ■ IPv6 packet in an IPv4 tunnel	 ■ Yes (IPv4 tunnel header) ■ Yes (IPv4 tunnel header)	 ■ No ■ No
IPv6 Tunnels: ■ IPv4 packet in an IPv6 tunnel ■ IPv6 packet in an IPv6 tunnel	 ■ Not applicable ■ Not applicable	 ■ No ■ No
IPv4 packet has 802.3ac tag (with C-VLAN Tag or S-VLAN Tag when enabled)	Yes	Yes
IPv6 packet has 802.3ac tag (with C-VLAN Tag or S-VLAN Tag when enabled)	Not applicable	Yes
IPv4 frames with security features (such as encapsulated security payload)	Yes	No
IPv6 frames with security features (such as encapsulated security payload)	Not applicable	No

47.5.8 Receive Checksum Offload

The Ethernet peripheral provides the Checksum Offload Engine that is used to detect any error in an IPv4 or IPv6 packet in the receive path. The MAC verifies the checksum field of the received packet with the internally calculated checksum and provides the status.

The Receive Checksum Offload engine is used to detect errors in IP packets by calculating the header checksum and further matching it with the received header checksum. This engine also identifies a TCP, UDP, or ICMP payload in received IP packets and calculates the checksum of such payloads appropriately.

Here, both IPv4 and IPv6 packet in the received Ethernet packets are detected and processed for data integrity. The MAC receiver identifies IPv4 or IPv6 packets by checking for value 0x0800 or 0x86DD, respectively, in the Type field of the received Ethernet packet. This identification is applicable to single VLAN-tagged packets. It is also applicable to double VLAN-tagged packets when the Enable Double VLAN Processing option is selected and the EDVLP bit of the MAC VLAN Tag register is set.

The Rx COE calculates the IPv4 header checksums and checks that they match the received IPv4 header checksums. The result of this operation (pass or fail) is given to the RFC module for insertion into the receive status word. The IP Header Error bit is set for any mismatch between the indicated payload type (Ethernet Type field) and the IP header

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Email: sales@nsing.com.sg

version, or when the received packet does not have enough bytes, as indicated by the Length field of the IPv4 header (or when fewer than 20 bytes are available in an IPv4 or IPv6 header).

Packets with TCP/IP errors (header or payload) are dropped in MTL when DISTCPEF bit of the MTL RxQ Operation Mode register is reset and FEP bit is set.

This engine also identifies a TCP, UDP, or ICMP payload in the received IP datagrams (IPv4 or IPv6) and calculates the checksum of such payloads properly, as defined in the TCP, UDP, or ICMP specifications. This engine includes the TCP, UDP, or ICMPv6 pseudo-header bytes for checksum calculation and checks whether the received checksum field matches the calculated value. The result of this operation is given as a Payload Checksum Error bit in the receive status word. This status bit is also set if the length of the TCP, UDP, or ICMP payload does not match the expected payload length given in the IP header.

Table 47-26 describes the functions supported by the Rx COE based on the packet type. When the payload of an IP packet is not processed (indicated as "No" in the table), the information (whether the checksum engine is bypassed or not) is given in the receive status.

Note: The MAC does not append any payload checksum bytes to the received Ethernet packets.

Table 47-26 Receive Checksum Offload Engine Functions for Different Packet Types

Packet Type	Hardware IP Header Checksum Insertion	Hardware TCP/UDP Checksum Insertion
Non-IPv4 or IPv6 packet	No	No
IPv4 with TCP, UDP, or ICMP	Yes	Yes
IPv4 header's protocol field contains a protocol other than TCP, UDP, or ICMP	Yes	No
IPv4 packet has IP options (IP header is longer than 20 bytes)	Yes	Yes
Packet is an IPv4 fragment	Yes	No
IPv6 packet with the following next header fields in main or extension headers:		
■ Hop-by-hop options (in IPv6 main header)	■ Not Applicable	■ Yes
■ Hop-by-hop options (in IPv6 extension header)	■ Not Applicable	■ No
■ Destinations options	■ Not Applicable	■ Yes
■ Routing (with segment left 0)	■ Not Applicable	■ Ye
■ Routing (with segment left > 0)	■ Not Applicable	■ No
■ TCP, UDP, or ICMP	■ Not Applicable	■ Yes
■ Any other next header field in main or extension headers	■ Not Applicable	■ No
IPv4 packet has TCP header with Options fields	Yes	Yes
IPv4 Tunnels:		
■ IPv4 packet in an IPv4 tunnel	■ Yes (IPv4 tunnel header)	■ No
■ IPv6 packet in an IPv4 tunnel	■ Yes (IPv4 tunnel header)	■ No
IPv6 Tunnels:		
■ IPv4 packet in an IPv6 tunnel	■ Not applicable	■ No
■ IPv6 packet in an IPv6 tunnel	■ Not applicable	■ No
IPv4 packet has 802.3ac tag (with C-VLAN Tag or S-VLAN Tag	Yes	Yes

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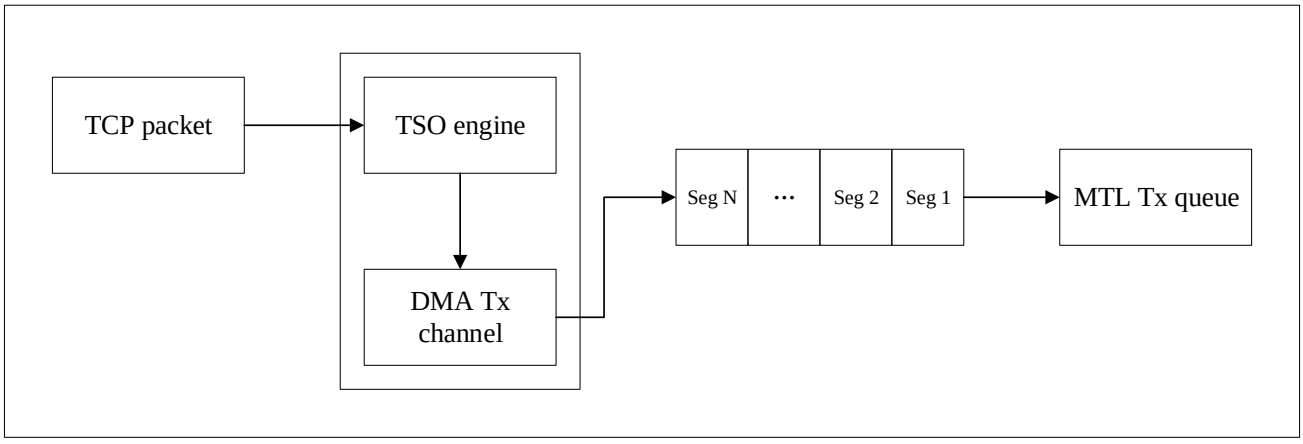
Packet Type	Hardware IP Header Checksum Insertion	Hardware TCP/UDP Checksum Insertion
when enabled)		
IPv6 packet has 802.3ac tag (with C-VLAN Tag or S-VLAN Tag when enabled)	Not applicable	Yes
IPv4 frames with security features (such as encapsulated security payload)	Yes	No
IPv6 frames with security features (such as encapsulated security payload)	Not applicable	No

47.5.9 TCP/IP Segmentation Offload

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware. It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.

In the TSO feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL as shown in Figure 47-18.

Figure 47-18 TCP Segmentation Offload Overview



47.5.9.1 DMA Operation with TSO Feature

For the TSO feature, the Tx DMA operation is as follows, the Figure 47-19 shows the TSO flow:

1. The application sets up the Transmit descriptor (TDES0-TDES3) and sets the Own bit (TDES3[31]) after setting up the corresponding data buffer(s) with Ethernet Packet data.
2. The application increases the offset value of the Descriptor Tail pointer of the DMA Tx channel.
3. While in the Run state, the DMA fetches the next available descriptor and does one of the following:
   - If the descriptor is a context descriptor and the context is not between the first and last descriptors of a packet, the DMA stores the context values.

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- If the descriptor is a context descriptor and the context is between the first and last descriptors of a packet, the DMA closes the context descriptor indicating a Context Descriptor Error (TDES3[23]) and fetches the next descriptor.
- If the descriptor is a normal descriptor, the DMA checks for the TSE bit. If TSE bit is not set, the DMA continues with the default mode of operation or OSF operation (if enabled).

4. The DMA calculates the number of segments from the TCP payload length(TDES3[17:0]) and the MSS value.
5. The DMA goes through channel arbitration to fetch the data buffers. The DMA fetches the header and payload separately.
6. For the first segment, the DMA fetches the header from the system memory and stores it in the TSO memory (if present and when the length of header is not greater than the TSO memory size).

   If the current segmented packet is not the first segment, the DMA fetches the header from the local TSO memory if available. Otherwise, it fetches the header buffer in system memory again, as done for the first segment. In such cases (header not available is TSO memory), the DMA does not close the first descriptor containing the header buffer, until the header for last segment is fetched.
7. The required fields in the header bytes are modified/updated as per the segmentation requirements and written into the corresponding MTL TxQ.
8. The DMA then takes the payload buffer pointer, fetches the MSS number of payload bytes from the system memory and directly pushes it into the MTL TxQ. In case the buffer(s) in the descriptor do not have enough data for the MSS payload (except for the last segment), the DMA closes this descriptor.
9. The DMA jumps to Step 3 and repeats the process until the last segment is written into the TxQ.
10. The DMA closes the last descriptor and also the first descriptor (containing the header buffer when it is not stored in TSO memory) and then moves on to the next packet transfer.

The DMA repeats all these steps if more descriptors are available. When no descriptor is available, the DMA enters the suspend state.

Note: The TSO engine determines whether to perform TSO or USO operation based on the THL field (TCP Header Length) in TDES3 of first Normal Tx descriptor for the packet. The value of 2 indicates USO and any value greater than or equal to 5 indicates TSO.

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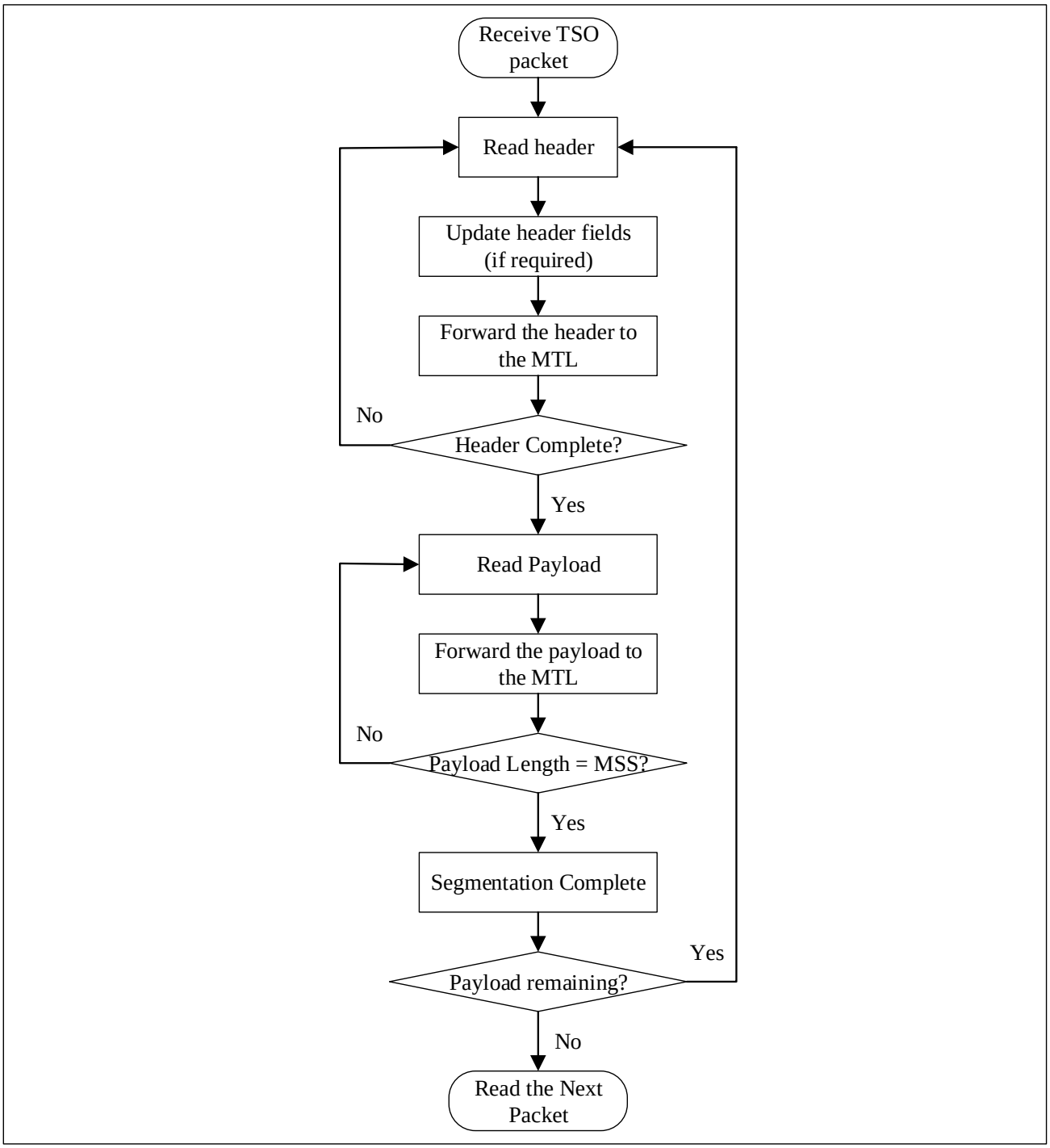
Figure 47-19 TCP Segmentation Offload Flow



47.5.9.2 TCP/IP Header Fields

While segmenting a TCP packet, the DMA automatically updates the TCP/IP header fields. Table 47-27 describes how the TCP and IP headers are updated.

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Table 47-27 TSO: TCP and IP Header Fields

Packet Sequence	TCP Header	IP Header
First packet	1. The sequence number is not updated. The value provided in the header is used. 2. The TCP checksum is calculated again. 3. If set, the FIN and PSH flags are cleared.	■ IPv4 Header – Total Length = MSS + TCP Header Length + IP Header Length – Identification field is not modified. It is sent as per the header provided by the software. – IPv4 Header Checksum is recalculated. ■ IPv6 Header – Payload Length = MSS + TCP Header Length + IPExtension Header Length
Subsequent packets	1. The sequence number is updated. The MSS value is added to the sequence number value of previous segment. 2. If set, the FIN and PSH flags are cleared. 3. The TCP checksum is calculated again.	■ IPv4 Header – Total Length = MSS + TCP Header Length + IP Header Length – Identification field = Previous Identification Field + 1 – IPv4 Header Checksum is recalculated ■ IPv6 Header – Payload Length = MSS + TCP Header Length + IPExtension Header Length
Last packet	1. The sequence number is updated. The MSS value is added to the sequence number value of previous segment. 2. If FIN and PSH flags were set in original header, these flags are set. 3. The TCP checksum is calculated again.	■ IPv4 Header – Total Length = Remaining Payload + TCP Header Length + IP Header Length – Identification Field = Previous Identification Field + 1 – IPv4 header Checksum is recalculated ■ IPv6 Header – Payload Length = Remaining Payload Length + TCP Header Length + IP Extension Header Length

Note: In case of USO, the engine updates only the following fields in the IP-UDP headers:

- *Total Length, Identification Field, and Header Checksum field in IPv4 header*
- *Payload Length field in IPv6 header*
- *Length and Checksum field in UDP header*

47.5.9.3 Header and Payload Fields of Segmented Packets

After segmentation, the split packets use the same header as the parent TCP packet for header fields other than the ones described in Table 47-27. Figure 47-20 shows how the same header is used for the header fields of segmented packets.

The application must create the header in Buffer 1 of the first descriptor of the packet to be segmented and provide

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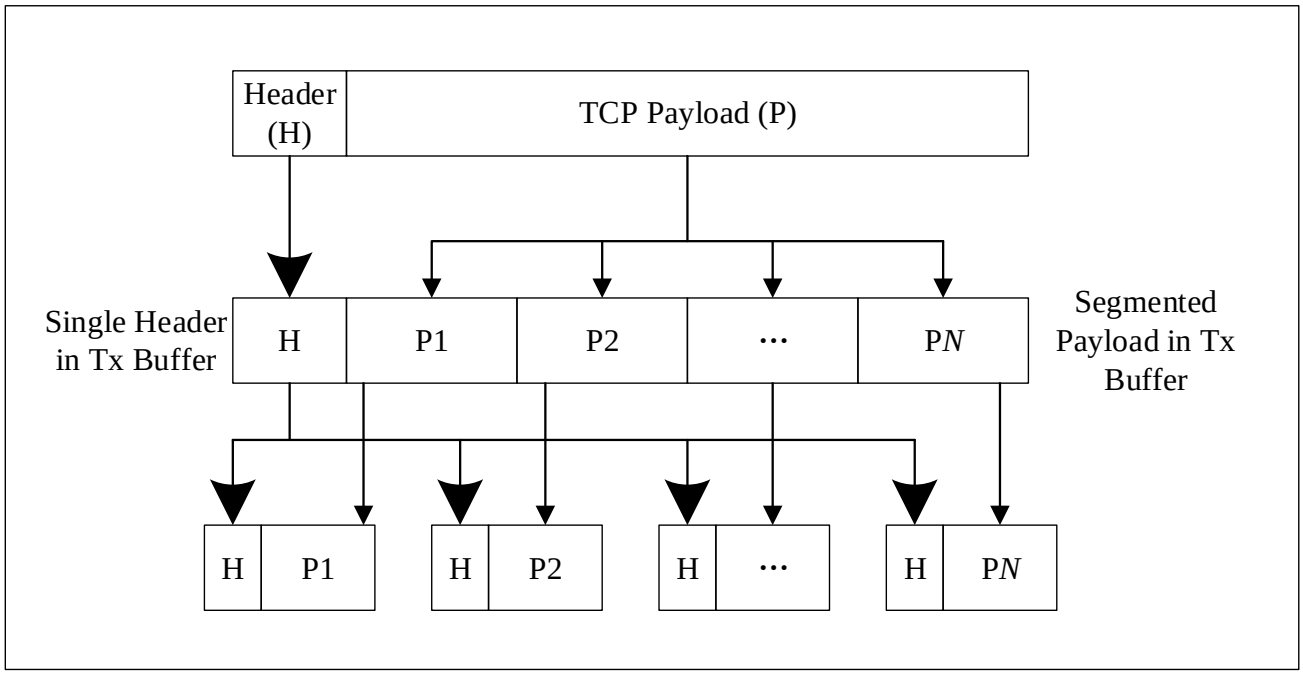
Email: sales@nsing.com.sg

the header length in TDES2 of the first descriptor (FD = 1). When the FD bit is set, the DMA reads the header from the header buffer to which the TDES0 is pointing. Buffer 2 of the first descriptor can be used for payload and TDES0 and TDES1 of subsequent descriptors. For subsequent descriptors (FD = 0), the address to which the TDES0 and TDES1 are pointing is treated as payload buffer address of the same packet.

Figure 47-20 Header and Payload Fields of Segmented Packets



47.5.9.4 Context Descriptor Sequence

You can use the context descriptor to provide the MSS value for segmentation. The application must provide the context descriptor before the normal descriptor to be used for the corresponding TCP packet. If the application wants to provide a new MSS, it must create the context descriptor in the descriptor list before the first normal descriptor of the packet to be segmented with the new MSS value. The MSS value in the context descriptor is valid only if the TCMSSV bit of TDES3 in context descriptor is set and the OSTC bit is reset.

When the application provides a context descriptor with a valid MSS value, the DMA internally stores the MSS value and uses this MSS value for all subsequent packets that have the TSO Enabled through the TSE bit of TDES3 normal descriptor.

If the application places a context descriptor in the middle of a packet (between the first and last descriptors of a packet), the DMA does the following:

1. The DMA ignores the context and closes the descriptor.
2. The DMA indicates the error in descriptor status.
3. The DMA generates an interrupt if the CDEE bit is set in the DMA CH0 Interrupt Enable register.

The application can read the interrupt status through CDE bit of DMA CH0 Status register.

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47.5.9.5 Building the Descriptor and the Packet for the TSO Feature

Set the TSE bit of TDES3 of first normal descriptor. If the TSE bit is set in TDES3 for a non TCP/IP packet, the DMA behavior is unpredictable.

The application must program the length of the TCP packet payload in TDES3[17:0] and the TCP header in TDES3[22:19]. The maximum length of TCP packet payload that can be segmented is 256 KB.

The header of the packet including Ethernet header, L3 header and L4 header should be provided in Buffer1 of the first normal descriptor of the TSO packet. Only buffer 1 of the first normal descriptor of a packet enabled for TSO is taken as the buffer containing the header.

The TCP payload can begin from buffer 2 of the first normal descriptor and continue to buffer1 and buffer 2 of second normal descriptor and subsequent descriptors.

The TCP payload may span across multiple buffers and multiple descriptors. The size of buffers containing the TCP payload should add up to be equal to the TCP payload length provided in TDES3[17:0] of the first normal descriptor.

The MAC always calculates and appends CRC and inserts Padding (if required) for all packets segmented by the DMA. If the TSE bit of TDES3 is enabled, the CRC PAD Control (CPC) field of TDES3 is reserved. To determine the size of a TCP packet after segmentation, the DMA uses the Maximum Segment Size (MSS) provided by the application through context descriptor. The DMA segments only those packets which have payload size greater than MSS. The application must provide the MSS by either programming the MSS value in the DMA CH0 Control register or by providing a context descriptor. The DMA uses the last programmed value of MSS or the last MSS value provided through context (whichever is provided later).

The header length plus the MSS size (which is equal to the size of each TCP segment) should not exceed 16383 bytes otherwise the MAC transmitter truncates the packet after 16383 bytes causing a CRC error.

The header length plus MSS size plus programmed PBL value in DMA CH0 Tx Control register should be lesser than the Tx Queue size programmed in TQS field of MTL Tx Queue Operation mode register. It is recommends that MSS + header is equal to half the programmed Tx Queue size.

The DMA also supports segmentation of VLAN Tagged TCP/IP frames, so if the TCP packet has a VLAN Tag, then the same tag is used for all the segments irrespective of the VLAN tag type provided (C-VLAN or S-VLAN). The VLAN Tag insert/replace control bits are used for all segments.

If the Double VLAN Feature is selected, then the DMA passes both the tags for all segments irrespective of the VLAN tag types provided (C-VLAN or S-VLAN). The VLAN Tag Insert/Replace control bits for both tags is applicable for all segments.

If Double VLAN feature is not selected, then the application must not set the TSE bit in TDES3 for a TCP/IP packet with two tags. The DMA behavior in this scenario is unpredictable. If the TSE bit is set in TDES3 for the packet and TCP header length provided is less than 5 (meaning an invalid TCP header because it is less than 20 bytes), the DMA does not perform segmentation, instead it transmits the entire packet as a single packet. In this scenario, the CRC pad control bits are forced by DMA to 2'b00 (MAC does CRC and padding) and checksum insertion control bits are forced to 2'b11 (Hardware does the checksum calculation for both header and payload).

Note: The TSO feature is supported only when the MAC operates in Full Duplex mode. The TCP Segmentation Offload (TSO) feature is not supported for TxPBL values programmed to less than 8 in the DMA CH0 Tx Control

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Email: sales@nsing.com.sg

register.

47.5.10 IPv4 ARP Offload

The Ethernet peripheral supports the Address Recognition Protocol (ARP) Offload for IPv4 packets. This feature allows the processing of the IPv4 ARP request packet in the receive path and generating corresponding ARP response packet in the transmit path. The Ethernet peripheral generates the ARP reply packets for appropriate ARP request packets. The ARP packet for IPv4 is L2 layer packet with Length/Type of 0x0806.

The ARP offloading process is as follows:

1. The MAC receiver gets an ARP request if the Target Protocol Address of request matches the IPv4 address programmed in the L3 register of the MAC.
2. The MAC generates an ARP reply packet.
3. The MAC copies the Sender Hardware Address field in the ARP request to the following fields:
   - DA field of the Ethernet packet header
   - Target Hardware Address field of the ARP reply packet
4. The MAC copies the Sender Protocol Address field in the ARP request to the Target Protocol Address field in the ARP reply packet.
5. The MAC places its MAC address in the following fields:
   - SA field of the Ethernet packet header
   - Sender Hardware Address field of the ARP reply packet
6. The MAC copies the Target Protocol Address field in the ARP request to the Sender Protocol Address field in the ARP reply packet.
7. The MAC sets the opcode field in ARP reply packet to 2 indicating ARP reply.
8. The MAC recalculates the CRC and performs padding for generated ARP reply packet.
9. The MAC transmitter sends the ARP reply.

The MAC processes only one ARP request at a time. It does not store the fields of multiple ARP requests. If the MAC receives an ARP request when it is already processing an earlier ARP request, the MAC does not generate the ARP reply for new ARP request. The MAC forwards the new ARP request packet to application with ARP Reply Not Generated (Bit 34) status bit set. However, in power-down mode, if the MAC receives an ARP request when it is already processing an earlier ARP request, the MAC drops the new ARP request.

If the Disable CRC check bit of the MAC Extension Configuration bit is set, then the MAC does not check for valid CRC of a ARP request Packet. It can generate an ARP response packet if the other conditions are valid. If PMT function is enabled, the ARP request Packet must always have a valid CRC.

Note: When the received ARP request is less than 64 bytes packet length, The Ethernet peripheral does not send a ARP response. It is treated as normal packet and forwarded to the application based on the The Ethernet peripheral filter settings.

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47.5.11 Low-Power Management (PMT)

The Ethernet peripheral supports the following techniques to save power:

- Magic Packet
- Remote Wakeup

The Magic Packet and Remove Wakeup techniques are used to save power in the host system when it is idle (Sleep mode) and has to be woken up only at the reception of specific packets from the Ethernet network. In the Sleep mode, the power to the host logic along with majority of the Ethernet peripheral (except the MAC receiver logic), can be shut down. On receiving the specific packets from the network, the MAC provides the trigger to restore the power to the host system and come back to normal state.

When you enable the low-power mode in the PMT block, the MAC drops all received packets and does not forward any packet to the MTL Rx Queue or the application.

47.5.11.1 Magic Packet Mode

In the Magic Packet based power saving is a mode, the reception of valid magic packet by MAC receiver triggers an exit from low-power mode. The MAC enters power saving mode when PWRDWN bit of MAC PMT Control Status register is programmed to 1. Exit from the magic packet based low-power mode is enabled by setting the MGKPKTEN bit of MAC PMT Control Status register to 1.

The magic packet contains a unique pattern at any offset after the Destination address, Source address, and Length/Type fields. In addition to the unique pattern matching, the MAC receiver also checks for the following, to detect the received packet as a valid magic packet:

- The packet must be addressed to it (Destination Address of the received packet should perfect match the MAC Address0 High and MAC Address0 Low registers) or with multicast/broadcast address
- The packet must not have length error, FCS error, dribble bit error, GMII error, and collision
- The packet must not be runt (length including Ethernet header and FCS is at least 64 bytes)

Note: The magic packet feature is based on the Magic Packet technology white paper from Advanced Micro Device (AMD). The watchdog timeout limit for a magic packet is 2,048 bytes irrespective of the value programmed in WD bit of MAC Configuration register and PWE bit in MAC Watchdog Timeout register.

Magic Packet Data Format

The content of the unique pattern in magic packet is described as:

- 6 bytes of all-ones (48'hFF_FF_FF_FF_FF_FF) called the synchronization stream. There can be more than six bytes of 8'hFF, but last 6 are considered
- The synchronization stream is immediately followed by 16 repetitions of Destination address field of the packet (MAC Address (MAC Address0 High and MAC Address0 Low registers) or multicast/broadcast address)
- No break or interruption between synchronization stream and first repetition of Destination address field or within its 16 repetitions

If the MAC address of a node is 48'h00_11_22_33_44_55, the MAC scans for the following data sequence:

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Destination Address Source Address Length/Type……FF FF FF FF FF FF

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 …CRC

47.5.11.2 Remote Wakeup Packet Mode

In the Remote Wakeup Magic Packet based power saving mode, the reception of expected remote wakeup packet by MAC receiver triggers the exit from low-power mode. The MAC enters power saving mode when PWRDWN bit of MAC PMT Control Status register is programmed to 1. Exit from the remote wakeup based low-power mode is enabled by programming RWKPKTEN bit of MAC PMT Control Status register to 1.

The MAC implements a filter lookup table (programmed through MAC RWK Packet Filter register) in which CRC, offset, and byte mask of the pattern embedded in remote wakeup packet and the filter operation commands are programmed.

The pattern embedded in the remote wakeup packet is located at any offset after the Destination address and Source address fields. In addition to the CRC match for the pattern, the MAC receiver also checks the following, to detect the received packet as a valid remote wakeup packet:

- The packet must be addressed to it (Destination Address of the received packet should perfect match the MAC Address0 High and MAC Address0 Low registers) or with multicast/broadcast address
- The packet must not have length error, FCS error, dribble bit error, GMII error, and collision
- The packet must not be runt (length including Ethernet header and FCS is at least 64 bytes)

When a valid remote wakeup packet is received, the MAC receiver sets the RWKPRCVD bit in MAC PMT Control Status register and triggers the interrupt on *pmt_intr_o* output port. The PMTIS bit in MAC Interrupt Status register is set when power-gating is not enabled in low-power mode. An interrupt is triggered to the application when interrupt is enabled (PMTIE bit in MAC Interrupt Enable register is set) and CSR clock is not gated off in low-power mode.

Remote Wake-Up Packet Filters

When Remote Wakeup based power saving mode is selected, it allows selection of 4 Remote Wakeup Filters. The Remote Wakeup Filters structure is shown in Table 47-28.

Table 47-28 Remote Wake-Up Packet Filter Register

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
wkuppktfilter_reg0	Filter 0 Byte Mask																															
wkuppktfilter_reg1	Filter 1 Byte Mask																															
wkuppktfilter_reg2	Filter 2 Byte Mask																															
wkuppktfilter_reg3	Filter 3 Byte Mask																															
wkuppktfilter_reg4	Reserved				Filter 3 Command				Reserved				Filter 2 Command				Reserved				Filter 1 Command				Reserved				Filter 0 Command			
wkuppktfilter_reg5	Filter 3 Offset								Filter 2 Offset								Filter 1 Offset								Filter 0 Offset							

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Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
wkuppktfilter_reg6	Filter 1 CRC-16																Filter 0 CRC-16															
wkuppktfilter_reg7	Filter 3 CRC-16																Filter 2 CRC-16															

The fields of Remote Wakeup Filter are as follows:

Filter i Byte Mask

The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3) to determine whether or not a packet is a wake-up packet.

- The MSB (31st bit) must be zero.
- Bit j[30:0] is the byte mask.
- If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored

Filter i Command

The 4-bit filter i command controls the filter i operation.

- Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet
- Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC-16 value. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".
- Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. The details are as follows:
  - The And_Previous bit setting is applicable within a set of 4 filters.
  - Setting of And_Previous bit of filter that is not enabled has no effect, that is setting And_Previous bit of lowest number filter in the set of 4 filters has no effect. For example, setting of And_Previous bit of Filter 0 has no effect.
  - If And_Previous bit is set for filter to form AND chained filter, the AND chain breaks at the point any filter is not enabled. For example: If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set) but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result ANDed with Filter 3 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 2 is not enabled (bit 0 in Filter 2 command is reset), then since setting of Filter 2 And_Previous bit has no effect only Filter 1 result ORed with Filter 3 result is considered.
  - If filters chained by And_Previous bit setting have complementary programming, then a frame may never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is

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Email: sales@nsing.com.sg

set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type.

- Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled.

Filter i Offset

The filter i offset register defines the offset (within the packet) from which the filter i examines the packets.

- This 8-bit pattern-offset is the offset for the filter i first byte to be examined.
- The minimum allowed offset is 12, which refers to the 13th byte of the packet.
- The offset value 0 refers to the first byte of the packet.

Filter i CRC-16

The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register.

- The 16-bit CRC calculation uses the following polynomial:

$$G(x) = x^{16} + x^{15} + x^2 + 1$$

- Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following:
  - 32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC-16 calculation.
  - 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations.

The Remote Wakeup Filter registers are implemented as 8 indirect access registers (wkuppktfilter_reg#i) based on whether 4 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC RWK Packet Filter register. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight register values in MAC RWK Packet Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg7 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC PMT Control Status register.

Note: When MAC RWK Packet Filter register is written, the content is transferred from CSR clock domain to PHY receive clock domain after the write operation, there should not be any further write to the MAC RWK Packet Filter register until the first write is updated in PHY receive clock domain. Otherwise, the second write operation does not get updated to the PHY receive clock domain. Therefore, the delay between two writes to the MAC RWK Packet Filter register should be at least 4 cycles of the PHY receive clock.

47.5.12 Energy Efficient Ethernet (EEE)

EEE is an operational mode that enables the IEEE 802.3 Media Access Control (MAC) sub layer along with a family of physical layers to operate in the Low-Power Idle (LPI) mode. The EEE operational mode supports the IEEE 802.3

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

MAC operation at 100 Mbps and 1000 Mbps. The Ethernet peripheral supports the IEEE 802.3az-2010 for EEE.

The LPI mode allows power saving by switching off the parts of the communication device functionality when there is no data to be transmitted and received. The systems on both sides of the link can disable some functionalities to save power during the periods of low-link utilization. The MAC controls whether the system should enter or exit the LPI mode and communicates this to the PHY.

The EEE specifies the capabilities negotiation methods that the link partners can use to determine whether EEE is supported, and then select the set of parameters that are common to both devices.

47.5.12.1 Transmit Path Functions

The transmit path functions include tasks that the MAC must perform to make the PHY to enter the LPI state. In the transmit path, the software must set the LPIEN bit of the MAC LPI Control Status register to indicate to the MAC to stop transmission and initiate the LPI protocol. The MAC completes the transmission in progress, generates its transmission status, and starts transmitting the LPI pattern instead of the IDLE pattern if the link status has been up continuously for a period specified in the LST field of MAC LPI Timers Control register. The PHY Link Status bit of the MAC LPI Control Status register indicates the link status of the PHY.

Note: The EEE feature is not supported when the MAC is configured to use the RMII. According to the standard (IEEE 802.3az-2010), the PHY must not stop the Tx_CLK clock during the LPI state in the MII (10 or 100) mode. However, the MAC can stop the GTX_CLK clock during the LPI state in the GMII (1000) code.

To make the PHY enter the LPI state, the MAC performs the following tasks:

1. De-asserts TX_EN
2. Asserts TX_ER
3. Sets TXD[3:0] to 0x1 (for 100 Mbps) or TXD[7:0] to 0x01 (for 1,000 Mbps)

   Note: The MAC maintains the same state of the TX_EN, TX_ER, and TXD signals for the entire duration during which the PHY remains in the LPI state.
4. Updates the status (TLPIEN bit of MAC LPI Control Status register) and generates an interrupt

To bring the PHY out of the LPI state, that is, when the software resets the LPIEN bit, the MAC performs the following tasks:

1. Stops transmitting the LPI pattern and starts transmitting the IDLE pattern
2. Starts the LPI TW TIMER

   The MAC cannot start the transmission until the wake-up time specified for the PHY expires. The auto-negotiated wake-up interval is programmed in the TWT field of the MAC LPI Timers Control register.
3. Updates the LPI exit status (TLPIEX bit of the MAC LPI Control Status register) and generates an interrupt.

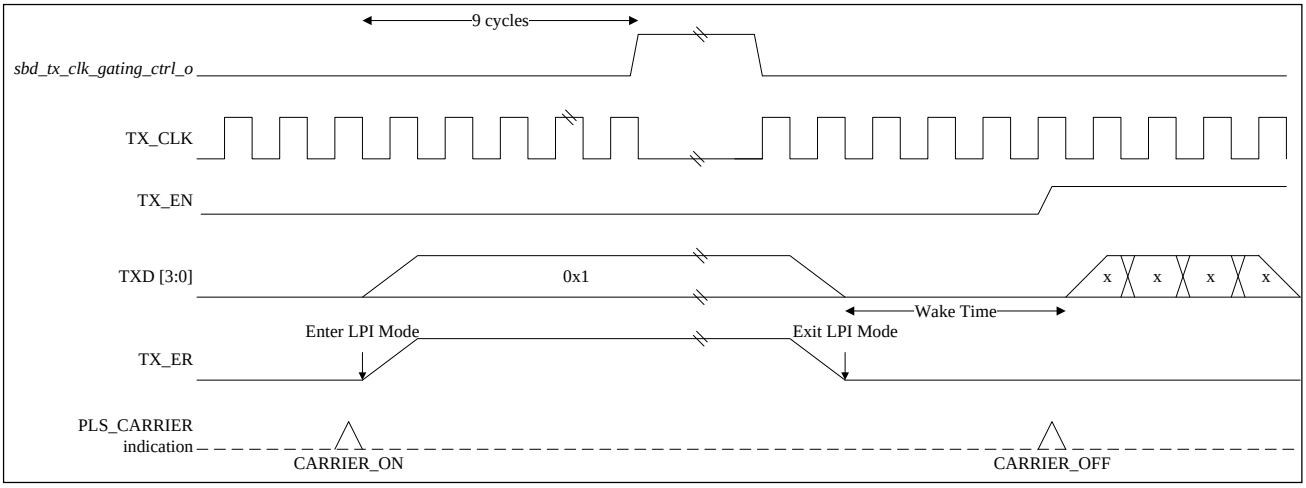
Figure 47-21 shows the behavior of TX_EN, TX_ER, and TXD[3:0] signals during the LPI mode transitions.

Note: The MAC does not stop the TX_CLK clock. You can stop this clock (as shown in Figure 47-21*) if your PHY supports it and when the MAC sets the sbd_tx_clk_gating_ctrl_o signal to 1. The sbd_tx_clk_gating_ctrl_o signal is asserted after nine Tx Clock Cycles, one Pulse Synchronizer delay, and one CSR clock cycle. The assertion of the sbd_tx_clk_gating_ctrl_o signal is dependent on the LPITCSE bit of the MAC LPI Control Status register. If the MAC*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

is in the Tx LPI mode and the Tx clock is stopped, the application should not write to CSR registers that are synchronized to Tx clock domain. If the MAC is in the LPI mode and the application issues a soft reset or hard reset, the MAC transmitter comes out of the LPI mode.

Figure 47-21 LPI Transitions (Transmit)



47.5.12.2 Automated Entry/Exit of LPI mode in Transmit Path

The MAC transmitter can be programmed to enter and exit LPI IDLE mode automatically based on whether it is IDLE for a specific period of time or has a packet to transfer. These modes are enabled and controlled by MAC LPI Control Status register.

When LPITXA (Bit[19]) and LPITXEN (Bit[16]) of MAC LPI Control_Status register are set, the MAC transmitter enters LPI IDLE state when the MAC transmit path (including the MTL layers and DMA layers) are idle. The MAC transmitter exits the LPI IDLE state and clear the LPITXEN bit as soon as any of functions in the TX path (DMA, MTL or MAC) becomes non-idle due to initiation of a packet transfer.

In addition, when Bit[20] (LPIATE) is also set, the MAC transmitter enters LPI IDLE state only if the Transmit path remains in idle state (no activity) for the time period indicated by the value in MAC LPI Entry Timer register. In this mode also, the MAC transmitter exits the LPI IDLE state as soon as any of the functions becomes non-idle. However, the LPITXEN bit is not cleared but remains active so that reentry to LPI IDLE state is possible without any software intervention when the MAC becomes idle again.

When both LPIATE and LPITXA bits are cleared, you can directly control the entry and exit of LPI IDLE state by programming the LPITXEN bit.

47.5.12.3 Receive Path Functions

The receive path functions include the tasks that the PHY and MAC must perform when the PHY receives signals from the link partner to exit the LPI state.

In the receive path, when the PHY receives the signals from the link partner to enter into the LPI state, the PHY and MAC perform the following tasks:

1. The PHY asserts RX_ER
2. The PHY sets RXD[7:0] to 0x01

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Email: sales@nsing.com.sg

3. The PHY de-asserts RX_DV

   Note: The PHY maintains the same state of the RX_ER, RXD, and RX_DV signals for the entire duration during which it remains in the LPI state.

4. The MAC updates the RLPIEN bit of the MAC LPI Control Status register and immediately generates an interrupt

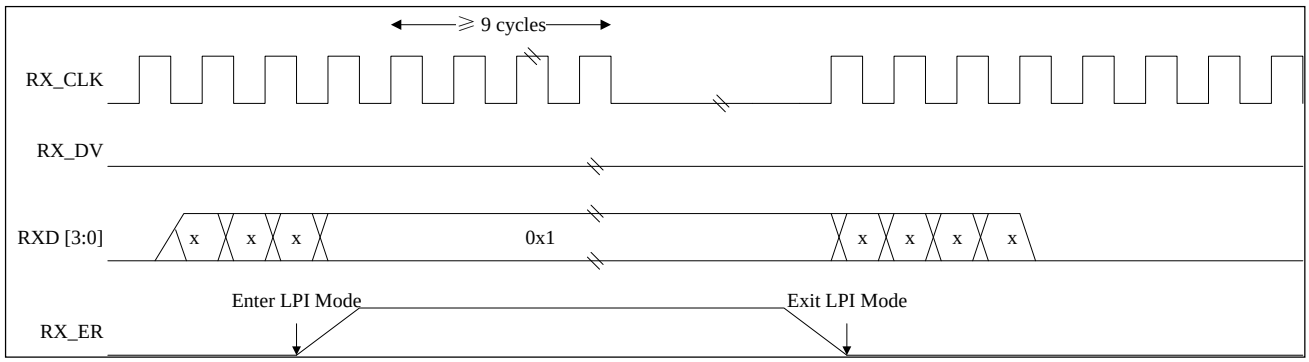
Note: If the LPI pattern is detected for a very short duration (that is, less than two cycles of Rx clock), the MAC does not enter the Rx LPI mode. If the duration between end of the current Rx LPI pattern and start of the next Rx LPI pattern, is very short (that is, less than two cycles of Rx clock), then the MAC exits and again enters the Rx LPI mode. The MAC does not give the Rx LPI Exit and Entry interrupts.

When the PHY receives signals from the link partner to exit the LPI state, the PHY and MAC perform the following tasks:

1. The PHY de-asserts RX_ER and returns to a normal inter-packet state.
2. The MAC updates the RLPIEX bit of the MAC LPI Control Status register and generates an interrupt immediately. The sideband signal *lpi_intr_o* (synchronous to Rx clock) is also asserted.

Figure 47-22 shows the behavior of RX_ER, RX_DV, and RXD[3:0] signals during the LPI mode transitions.

Figure 47-22 LPI Transitions (Receive)



Note: If the RX_CLK_stoppable bit (in the PHY register written through MDIO) is asserted when the PHY is indicating LPI to the MAC, the PHY may halt the RX_CLK at any time more than nine clock cycles after the start of the LPI state as shown in Figure 47-22. If the MAC is in the LPI mode and the application issues a soft reset or hard reset, the MAC receiver comes out of the LPI mode during reset. If the LPI pattern is still received after the reset is de-asserted, the MAC receiver again enters the LPI state. If the RX clock is stopped in the RX LPI mode, the application should not write to the CSR registers that are being synchronized to the RX clock domain. When the PHY sends the LPI pattern, if EEE feature is enabled, the MAC automatically enters the LPI state. There is no software control to prevent the MAC from entering the LPI state.

47.5.12.4 LPI Timers

The transmitter maintains the LPI LS TIMER, LPI TW TIMER, and LPI AUTO ENTRY TIMER timers.

Following are the LPI timers that are loaded with the respective values from the MAC LPI Timers Control and MAC LPI Entry Timer registers:

- LPI LS TIMER

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The LPI LS TIMER counts, in milliseconds, the time expired since the link status is up.

The link status is indicated to the MAC by value programmed by the software in the PLS bit of the MAC LPI Control Status register. The software should get the PHY link status by reading the PHY register and accordingly update the PLS bit.

This timer is cleared every time the link goes down. It starts to increment when the link is up again and continues to increment until the value of the timer becomes equal to the terminal count. Once the terminal count is reached, the timer remains at the same value as long as the link is up. The terminal count is the value programmed in Bits[25:16] of the MAC LPI Timers Control register. The GMII interface does not assert the LPI pattern unless the terminal count is reached. This ensures a minimum time for which no LPI pattern is asserted after a link is established with the remote station. This period is defined as 1 second in the IEEE 802.3-az-2010. The LPI LS TIMER is 10-bit wide. Therefore, the software can program up to 1023 milliseconds.

- LPI TW TIMER

  The LPI TW TIMER counts, in microseconds, the time expired since the de-assertion of LPI. The terminal count should be programmed in Bit[15:0] of LPI Timers Control register. The terminal count of the timer is the value of resolved Transmit TW that is the auto-negotiated time after which the MAC can resume the normal transmit operation. After exiting the LPI mode, the MAC resumes its normal operation after the TW timer reaches the terminal count.

  The MAC supports the LPI TW TIMER in units of microsecond. The LPI TW TIMER is 16-bit wide. Therefore, the software can program up to 65535 micro seconds.

- LPI AUTO ENTRY TIMER

  This timer counts in steps of eight microseconds, the time for which the MAC transmit path has to remain in idle state (no activity), before the MAC Transmitter enters the LPI IDLE state and starts transmitting the LPI pattern. This timer is enabled when LPITE bit in MAC LPI Control Status register is set.

Note: Program the PLS bit of MAC LPI Control Status to 1'b0 before switching between the GMII and MII modes. This resets the internal timers. If the mode is changed after the LPI LS TIMER or LPI TW TIMER starts, the change in the Tx clock frequency can result in incorrect timeout.

47.5.13 MAC Management Counters

The Ethernet peripheral supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.

The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Each register is 32-bits wide. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.

The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter

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is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the MAC Packet Filter register.

The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

The following definitions define the terminology used in MMC register descriptions:

- Transmitted packets are considered “good” if transmitted successfully. In other words, a transmitted packet is good if the packets transmission is not aborted because of any of the following errors:
  - Jabber Timeout
  - No Carrier or Loss of Carrier
  - Late Collision
  - Packet Underflow
  - Excessive Deferral
  - Excessive Collision
- Received packets are considered “good” if none of the following errors exists:
  - CRC error
  - Runt packet (shorter than 64 bytes)
  - Alignment error (in 10/100 Mbps only)
  - Length error (non-Type packet only)
  - Out of Range (non-Type packet only, longer than 1518 bytes)
  - GMII_RXER Input error
- The maximum transmit frame size depends on the frame type, as follows:
  - Untagged frame maxsize = 1,518
  - VLAN Frame maxsize = 1,522
  - Jumbo Frame maxsize = 9,018
  - JumboVLAN Frame maxsize = 9,022
- The maximum receive packet size depends on the packet type and control bits (JE, S2KP, GPSLCE and EDVLP), as shown in the Table 47-29 table.

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Table 47-29 Size of the Maximum Receive Packet

JE	S2KP	GPSLCE	EDVLP	Untagged Frame maxsize in bytes	Single VLAN Frame maxsize in bytes	Double VLAN Frame maxsize in bytes
1	x	x	1	9018	9022	9026
0	1	x	x	2000	2000	2000
0	0	1	1	GPSL	GPSL + 4	GPSL + 8
0	0	0	1	1518	1522	1526
1	x	x	0	9018	9022	9022
0	0	1	0	GPSL	GPSL + 4	GPSL + 4
0	0	0	0	1518	1522	1522

47.5.14 Loopback Mode

The MAC supports Loopback of transmitted packets to its receiver. The following are some guidelines for using the loopback mode:

- Enable loopback only with the full-duplex mode. In half-duplex mode, the carrier sense signal (crs) or collision (col) signal inputs get sampled which may result into issues such as packet dropping.
- If the loopback mode is enabled without connecting a PHY chip, you should externally generate the Tx and Rx clocks and provide these clocks to the MAC.
- Do not loop back big packets. Big packets may get corrupted in the loopback FIFO.

The MAC does not process ARP or PMT packets that are looped back. To enable this feature, program the LM bit of the MAC Configuration register.

47.5.15 Descriptors

The DMA in the Ethernet subsystem transfers data based on a linked list of descriptors. The application creates the descriptors in the system memory. The Ethernet peripheral supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted.
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted.

Each normal descriptor contains two buffers and two address pointers. These buffers enable the adapter port to be compatible with various types of memory management schemes.

Note: There is no limit for the number of descriptors that can be used for a single packet.

47.5.15.1 Descriptor Structure

The Ethernet peripheral supports the ring structure for DMA descriptor as shown in Figure 47-23.

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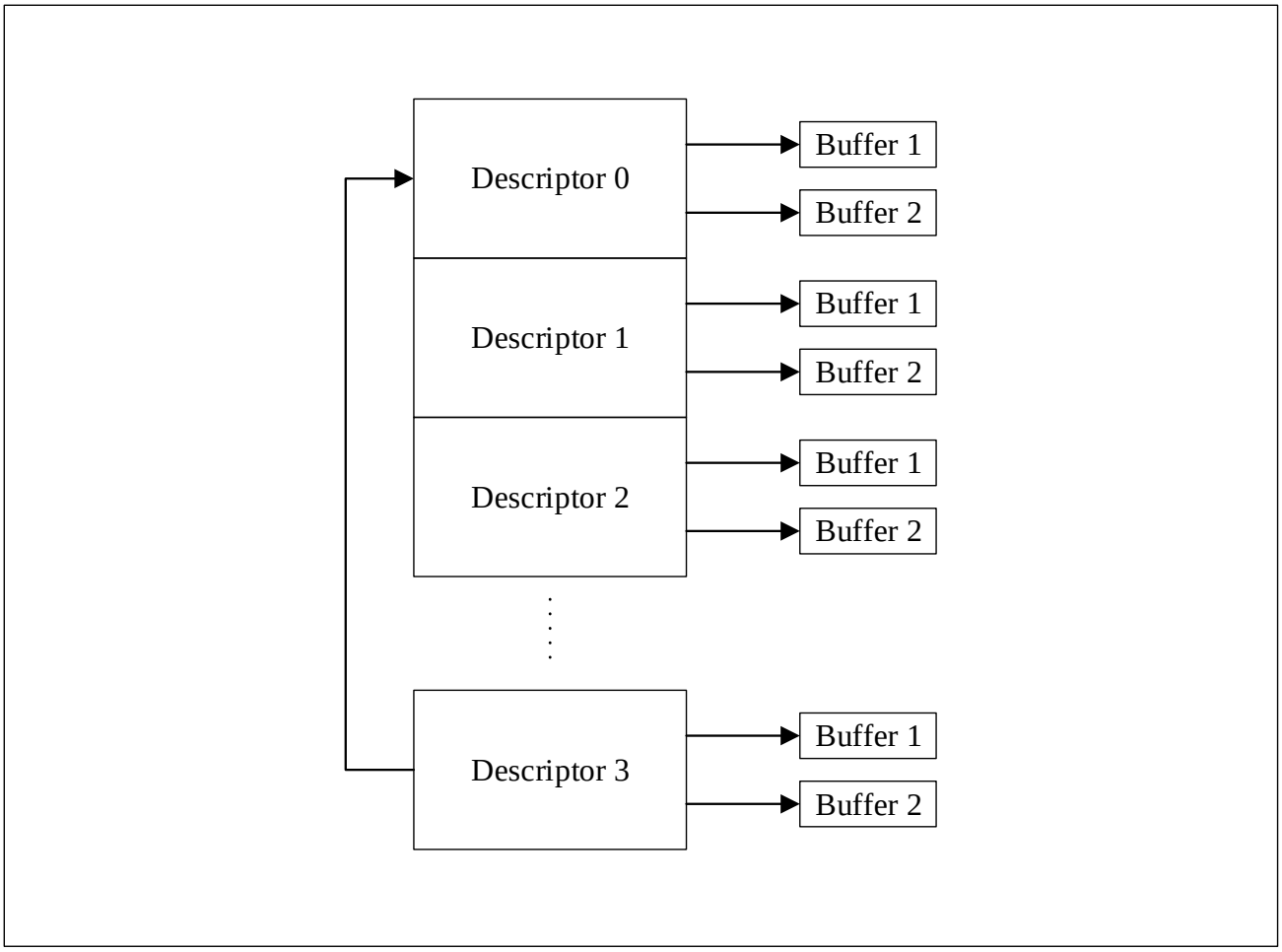
Figure 47-23 Descriptor Ring Structure



In Ring structure, descriptors are separated by the Word (32-bits) number programmed in the DSL field of the DMA CH0 Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- ETH DMA CH0 TxDesc Ring Length register (ETH_DMACH0TXDRLEN)
- ETH DMA CH0 Rx Control register 2 (ETH_DMACH0RXCTRL2)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process. The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer;

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer;

The DMA automatically wraps around the base address when the end of ring is reached, as shown in Figure 47-24.

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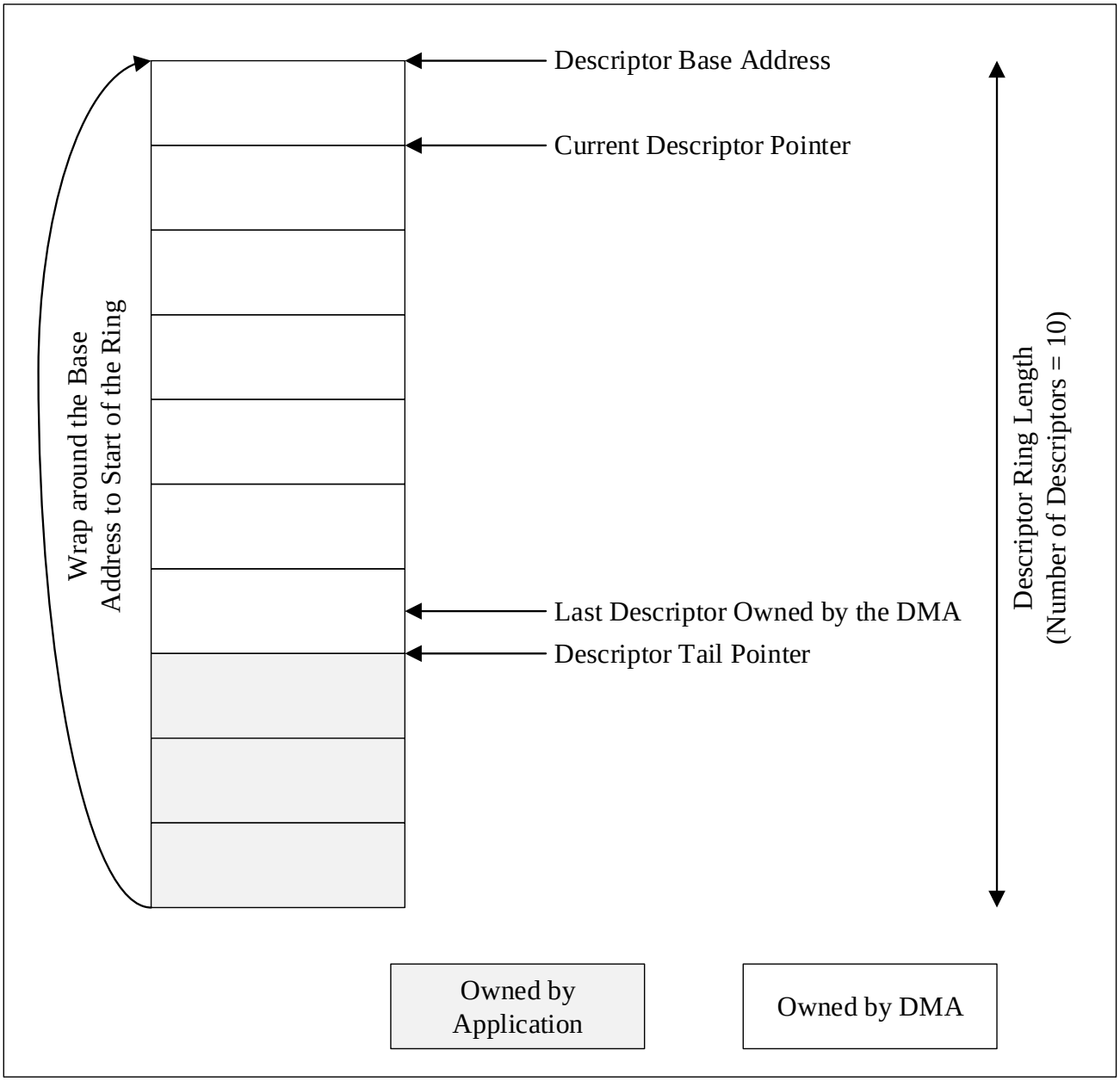
Figure 47-24 DMA Descriptor Ring



For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

47.5.15.2 Transmit Descriptor

The DMA in Ethernet peripheral requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis. The Transmit Normal descriptor has two formats: Read format and Write-Back format.

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Transmit Normal Descriptor (Read Format)

Table 47-30 shows the Read Format for a Transmit normal descriptor. Table 47-31 through Table 47-34 describe the read format for the Transmit Normal Descriptors: TDES0, TDES1, TDES2, and TDES3.

Table 47-30 Transmit Normal Descriptor (Read Format)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDES0	Header or Buffer 1 Address[31:0]																															
TDES1	Buffer 2 Address[31:0]																															
TDES2	IOC	TTSE	Buffer 2 Length[29:16]														VTIR	Header or Buffer 1 Length[13:0]														
TDES3	OWN	Control[30:16] or Control[30:18]															Frame Length[14:0] or Payload Length[17:0]															

Table 47-31 TDES0 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TSO Header Address pointer when the following bits are set: ■ TSE bit of TDES3 ■ FD bit of TDES3

Table 47-32 TDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment.

Table 47-33 TDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31	IOC	Interrupt on completion This bit controls the setting of TI and ETI status bits in the DMA CH0 Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE	Transmit Timestamp Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set.

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Bit	Name	Description
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length.
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: ■ 2'b00: Do not add a VLAN tag. ■ 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the VLAN packets. ■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC VLAN Incl register or context descriptor. ■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC VLAN Incl register or context descriptor. This option should be used only with the VLAN packets.
13:0	HL/B1L	Header Length or Buffer 1 Length For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.

Table 47-34 TDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:26	CPC	CRC Pad Control

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Bit	Name	Description
		This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits[27:26]: ■ 2'b00: CRC and Pad Insertion The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. ■ 2'b01: CRC Insertion (Disable Pad Insertion) The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. ■ 2'b10: Disable CRC Insertion The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. ■ 2'b11: CRC Replacement The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. This field is valid only for the first descriptor. *Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.*
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[24:23]: ■ 2'b00: Do not include the source address ■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. ■ 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. ■ 2'b11: Reserved This field is valid only for the first descriptor.
22:19	THL	TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor
18	TSE	TCP Segmentation Enable

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Bit	Name	Description
		When this bit is set, the DMA performs the TCP/UDP segmentation for a packet. This bit is valid only if the FD bit is set.
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length These bits control the checksum calculation and insertion. The following list describes the bit encoding: ■ 2'b00: Checksum Insertion Disabled. ■ 2'b01: Only IP header checksum calculation and insertion are enabled. ■ 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. ■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0].
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: *Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length* When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not include Ethernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOT enabled, value written into this field is not used when TSE = 0.

Transmit Normal Descriptor (Write-Back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits.

The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet.

Table 47-35 illustrates the write-back format of the Transmit Descriptor.

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Table 47-35 Transmit Normal Descriptor (Write-Back Format)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDES0	Timestamp Low																															
TDES1	Timestamp High																															
TDES2	Reserved																															
TDES3	OWN	Status																														

Table 47-36 TDES0 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set.

Table 47-37 TDES1 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 47-38 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	Reserved	Reserved.

Table 47-39 TDES3 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DWC_ether_qos DMA owns the descriptor. The DMA clears this bit when it completes the packet transmission. After the write-

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Bit	Name	Description
		back is complete, this bit is set to 'b0.
30	CTXT	Context Type This bit should be set to 'b0 for Normal descriptor.
29	FD	First Descriptor This bit indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor This bit is set 'b1 for last descriptor of a packet. The DMA writes the status fields only in the last descriptor of the packet.
27:24	Reserved	Reserved.
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet. ■ All 1s ■ CTXT is set to 1 along with LD or FD bits set to 1. *Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA sets the TI bit in the DMA CH0 Status register.* *Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.*
22:18	Reserved	Reserved
17	TTSS	Tx Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. *Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) PF = 1. This is because, all such packets are flushed by The Ethernet peripheral.*
15	ES	Error Summary This bit indicates the logical OR of the following bits: ■ TDES3[0]: IP Header Error ■ TDES3[14]: Jabber Timeout ■ TDES3[13]: Packet Flush ■ TDES3[12]: Payload Checksum Error ■ TDES3[11]: Loss of Carrier

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Bit	Name	Description
		■ TDES3[10]: No Carrier ■ TDES3[9]: Late Collision ■ TDES3[8]: Excessive Collision ■ TDES3[3]: Excessive Deferral ■ TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set.
14	JT	Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC Configuration register is not set.
13	PF	Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer.
11	LOC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the CRS signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC Configuration register, this bit is set after first collision and the transmission of the packet is aborted.
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.

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Bit	Name	Description
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ■ The DMA encountered an empty Transmit Buffer while transmitting the packet ■ The application filled the MTL Tx FIFO slower than the MAC transmit rate The transmission process enters the suspended state and sets the underflow bit corresponding to a queue in the MTL Interrupt Status register.
1	DB	Deferred Bit This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload.

Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature.

The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

Table 47-40 shows the format of the Transmit Context descriptor.

Table 47-40 Transmit Context Descriptor Format

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDES0	Timestamp Low																															
TDES1	Timestamp High																															
TDES2	Inner VLAN Tag																Rsvd			Maximum Segment Size											

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	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDES3	OWN	Control															VLAN Tag																

Table 47-41 TDES0 Context Descriptor

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 47-42 TDES1 Context Descriptor

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 47-43 TDES2 Context Descriptor

Bit	Name	Description
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	Reserved	Reserved.
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.

Table 47-44 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is

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Bit	Name	Description
		reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.
30	CTXT	Context Type This bit should be set to 1'b1 for Context descriptor.
29:28	Reserved	Reserved.
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMSSV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.
25:24	Reserved	Reserved.
23	CDE	Context Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the context descriptor. Context Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet. ■ All 1s. ■ CD, LD, and FD bits set to 1. *Note 1: When the Context Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA sets the TI bit in the DMA CH0 Status register* *Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.* *Note3: This error is categorized as an abnormal event; recovery is only by issuing a software reset (DMA stopping-reconfiguring-restarting recovery mechanism is not supported)*
22:20	Reserved	Reserved.
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: 2'b00: Do not add the inner VLAN tag. 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC Inner

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Bit	Name	Description
		VLAN Incl register or context descriptor. 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC Inner VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames.
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC VLAN Incl register is reset.

47.5.15.3 Receive Descriptor

The DMA in the Ethernet peripheral attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.

All RX descriptors are prepared by the software and given to the DMA as “Normal” Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA closes the descriptor with the corresponding packet status. The format of this status is given in the “Receive Normal Descriptor (Write-Back Format)”.

For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded in that descriptor). The format and content of the descriptor write back is described in “Receive Context Descriptor”.

Receive Normal Descriptor (Read Format)

The read format for a Receive Normal descriptor is made up of a header or Buffer 1 address, reserved field, payload or Buffer 2 or Next Descriptor address, a 30-bit reserved filed, OWN bit, and an interrupt bit.

Table 47-45 shows the Read Format for a Receive Normal Descriptor.

Table 47-45 Receive Normal Descriptor (Read Format)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDES0	Buffer 1 Address																															
RDES1	Reserved																															
RDES2	Buffer 2 Address																															
RDES3	OWN	IOC	Reserved																													

Note: In the Receive Descriptor (Read Format), if the Buffer Address field is all 0s, the Ethernet peripheral does not

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transfer data to that buffer and skips to the next buffer or next descriptor.

Table 47-46 RDES0 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1.

Table 47-47 RDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	Reserved	Reserved.

Table 47-48 RDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 Address Pointer These bits indicate the physical address of Buffer 2.

Table 47-49 RDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the Ethernet peripheral DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Reserved	Reserved.
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:0	Reserved	Reserved.

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Receive Normal Descriptor (Write-Back Format)

Table 47-50 illustrates the write-back format for a Receive Normal descriptor

Table 47-50 Receive Normal Descriptor (Write-Back Format)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDES0	Inner VLAN Tag																Outer VLAN Tag															
RDES1	OAM code, or MAC Control Opcode																Extended Status															
RDES2	MAC Filter																Reserved					ARPNR	Reserved									
RDES3	OWN	CTXC	FD	LD	Status												Packet Length															

Table 47-51 RDES0 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:16	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.

Table 47-52 RDES1 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code: If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode: The bits[15:8] of RDES3 contains the subtype and bits [7:0] contains the code.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow.
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal

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Bit	Name	Description
		descriptor for a packet.
13	PV	PTP Version This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet.
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: ■ 0000: No PTP message received ■ 0001: SYNC (all clock types) ■ 0010: Follow_Up (all clock types) ■ 0011: Delay_Req (all clock types) ■ 0100: Delay_Resp (all clock types) ■ 0101: Pdelay_Req (in peer-to-peer transparent clock) ■ 0110: Pdelay_Resp (in peer-to-peer transparent clock) ■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) ■ 1000: Announce ■ 1001: Management ■ 1010: Signaling ■ 1011–1110: Reserved ■ 1111: PTP packet with Reserved message type
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP. Bit 15 (ES) of RDES3 is not set when this bit is set.
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error

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Bit	Name	Description
		When this bit is set, it indicates either of the following: ■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes. ■ The IP datagram version is not consistent with the Ethernet Type value. ■ Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set.
2:0	PT	Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): ■ 3'b000: Unknown type or IP payload not processed ■ 3'b001: UDP ■ 3'b010: TCP ■ 3'b011: ICMP ■ Other values: Reserved If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

Table 47-53 RDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: 000: Filter 0 001: Filter 1 010: Filter 2 011: Filter 3 100: Filter 4 101: Filter 5 110: Filter 6 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter.
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ■ Layer 3 fields are not enabled and all enabled Layer 4 fields match ■ All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29].

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Bit	Name	Description
27	L3FM	Layer 3 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed ■ All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29].
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register.
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hash value.
17	DAF	Destination Address Filter Fail When this bit is set, it indicates that the packet failed the DA Filter in the MAC.
16	SAF	SA Address Filter Fail When this bit is set, it indicates that the packet failed the SA Filter in the MAC.
15	VFS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter.
14:11	Reserved	Reserved.
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time).
9:0	Reserved	Reserved.

Table 47-54 RDES3 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full

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Bit	Name	Description
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} 2'b00: Intermediate Descriptor 2'b01: First Descriptor 2'b10: Reserved 2'b11: Descriptor Error (due to all 1s) *Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data. Receive DMA sets the CDE field of the DMA CH0 Status register but does not the RI field even when IOC field is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.*
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last descriptor When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). *Note: Giant packet indicates only the packet length. It does not cause any packet truncation.*
22	RWT	Receive Watchdog Timeout

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Email: sales@nsing.com.sg

Bit	Name	Description
		When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. *Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial packets are dropped completely in Rx FIFO.*
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: 3'b000: The packet is a length packet 3'b001: The packet is a type packet 3'b011: The packet is a ARP Request packet type 3'b100: The packet is a type packet with VLAN Tag 3'b101: The packet is a type packet with Double VLAN Tag 3'b110: The packet is a MAC Control packet type 3'b111: The packet is a OAM packet type 3'b010: Reserved
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: ■ RDES3[24]: CRC Error ■ RDES3[19]: Dribble Error ■ RDES3[20]: Receive Error ■ RDES3[22]: Watchdog Timeout ■ RDES3[21]: Overflow Error ■ RDES3[23]: Giant Packet ■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled ■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled This field is valid only when the LD bit of RDES3 is set
14:0	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset.

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Bit	Name	Description
		The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 47-55 Receive Context Descriptor Format

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDES0	Timestamp Low																															
RDES1	Timestamp High																															
RDES2	Reserved																															
RDES3	OWN	CTXT	Reserved																													

Table 47-56 RDES0 Context Descriptor

Bit	Name	Description
31:0	RTSL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.

Table 47-57 RDES1 Context Descriptor

Bit	Name	Description
31:0	RTSL	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt.

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Table 47-58 RDES2 Context Descriptor

Bit	Name	Description
31:0	Reserved	Reserved.

Table 47-59 RDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2'b11 to indicate a descriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} ■ 2'b00: Reserved ■ 2'b01: Reserved ■ 2'b10: Context Descriptor ■ 2'b11: Descriptor Error *Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA sets the CDE bit in DMA CH0 Status register but does not set the RI field even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.*
29	DE	Descriptor Error See the CTXT bit description for details of using the DE bit along with CTXT bit.
28:0	Reserved	Reserved.

47.5.16 Interrupts

Interrupts can be generated as a result of various events in the Ethernet peripheral controller. These events are captured in status registers, and interrupt enables are provided for each source of an interrupt such that the interrupt signal (*sbd_intr_o*) is asserted for an event only when the corresponding interrupt enable is set.

The interrupt status and corresponding enable registers are organized in an hierarchical manner so that it is easier for software to traverse and identify the source of an interrupt event quickly. When *sbd_intr_o* is asserted, the DMA Interrupt Status register is the first level that indicates the major blocks for the interrupt event source. This register is read-only, and it contains bits corresponding to each DMA channel (TX and RX), the MTL, and the MAC. The software application must then read one (or more) of the following registers corresponding to the bits that are set:

■ ETH MAC Interrupt Status register (ETH_MACINTSTS)

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Email: sales@nsing.com.sg

- ETH MTL Interrupt Status register (ETH_MTLINTSTS)
- ETH DMA CH0 Status register (ETH_DMACH0STS)

47.5.16.1 Interrupts from DMA

The DMA CH0 Status register captures all the interrupt events of that Tx DMA and Rx DMA channel. The DMA CH0 Interrupt Enable register contains the corresponding enable bits for each of the interrupt event. There are two groups of interrupts in the DMA channel namely Normal and Abnormal interrupts. They are indicated by Bits[15:14] of DMA CH0 Status register respectively. The normal group is for events that happen during the normal transfer of packets (TI, RI, TBU) while the abnormal interrupt events are for error events. Interrupt events are cleared by writing 1'b1 to the corresponding bit position. When all the enabled interrupt events are cleared (including the NIS and AIS), the interrupt source from the DMA Channel is cleared and the corresponding bit in DMA Interrupt Status register is also cleared.

Interrupts are not queued. If the same interrupt event occurs again before the driver responds to the previous one, no additional interrupts are generated. For example, Receive Interrupt Bit[6] of DMA CH0 Status register indicates that one or more packets were transferred to the application buffer. The driver must scan all descriptors, from the last recorded position to the first one, owned by the DMA to determine how many packets are received. An interrupt is generated only once for multiple events. The driver must scan the DMA Interrupt Status register for the cause of the interrupt and clear the source in the respective Status register. The *sbd_intr_o* is cleared only when all the bits of DMA Interrupt Status register are cleared.

Periodic Scheduling of Transmit and Receive Interrupt

To improve the throughput and performance, the Ethernet peripheral supports interrupt timer and transmit descriptor to generate interrupts periodically, instead of every DMA transfer. It is not preferable to generate interrupts for every packet transferred by DMA (RI and TI) for system throughput performance reasons. The Ethernet peripheral gives the flexibility to schedule the interrupt at regular intervals using two methods:

- Set Interrupt on Completion bit in Transmit descriptor (TDES2[31]) once for every "required" number of packets to be transmitted.
- Similarly, set the IOC (RDES3[30]) bit only at some specific intervals of Receive descriptors. This way, whenever a received packet transfer to system memory is complete and any of the descriptors used for that packet transfer has the IOC bit set, only then the RI event is generated.

In addition, an interrupt timer (DMA CH0 Rx Interrupt Watchdog Timer register) is given for flexible control and periodic scheduling of Receive Interrupt. When this interrupt timer is programmed with a nonzero value, it gets activated as soon as the Rx DMA completes a transfer of a received packet to system memory without asserting the Receive Interrupt because the corresponding interrupt of completion IOC bit (RDES3[30]) is not set. When this timer runs out as per the programmed value, RI bit is set and the interrupt is asserted if the corresponding RIE is enabled in DMA CH0 Interrupt Enable register. The timer is stopped and cleared before it expires, if the RI is set for a packet transfer whose descriptor's IOC was set. The timer is reactivated automatically after the next packet transfer is complete without the RI event being generated.

Channel Transfer Complete Interrupt

The Transmit Transfer complete interrupt (TI) and Receive Transfer complete interrupt (RI) is reflected in DMA CH0 Status register. The TI bit is set whenever the Tx DMA channel closes the transmit descriptor in which the IOC

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Email: sales@nsing.com.sg

(Interrupt On Completion - TDES2[31]) bit is set. Similarly, the RI bit is set whenever the Rx DMA channel closes the receive descriptor with LD bit set and in any of the descriptors used for transferring that packet, IOC (Interrupt Enable on completion - RDES3[30]) bit is set.

The common *sbd_intr_o* output signal is asserted for the Transfer complete interrupts only when the corresponding interrupts are enabled in DMA CH0 Interrupt Enable register.

Also supports the following per Channel Transfer Complete interrupt signals.

- sbd_perch_tx_intr_o[0] (Transmit Channel 0 Interrupts)
- sbd_perch_rx_intr_o[0] (Receive Channel 0 Interrupts)

The behavior of the RI/TI/sbd_perch_tx_intr_o[0]/sbd_perch_rx_intr_o[0] changes depending on the settings of INTM field bit[17:16] in DMA Mode register. Table 47-60 explains the Transfer Complete Interrupt behavior.

Table 47-60 Transfer Complete Interrupt Behavior

Interrupt Mode	Behavior of the sbd_perch_tx_intr_o[0] and sbd_perch_rx_intr_o[0]	Behavior of TI/RI and sbd_intr_o
INTM = 0	A pulse is asserted on these output signals when corresponding TX/RX transfer complete event (for which IOC descriptor bits are enabled) is detected, irrespective of the corresponding interrupt status.	The TI/RI status signals are set whenever the “Transfer complete” event is detected. The bits get cleared whenever the software driver writes ‘1’ to these bits. The *sbd_intr_o* is asserted when ever the corresponding interrupts are also enabled in the DMA CH0 Interrupt Enable register. The NIS status bit is asserted for RI/TI events.
INTM = 1	These signals reflect the value of corresponding TI/RI bits in the DMA CH0 Status register when the corresponding interrupt enable is set. Therefore, they are level signals and are cleared by the application by writing 1’b1 to the RI/TI status bits. This signal is not asserted when the corresponding interrupt enable bit is not set.	The *sbd_intr_o* signal and NIS status bit are not asserted for RI/TI events.
INTM = 2	In this mode, RI/TI interrupts are queued. These signals reflect the value of corresponding TI/RI bits in the DMA CH0 Status register when the corresponding interrupt enable is set. They are level signals and cleared by software by writing 1’b1 to the RI/TI status bits. However, it is set again if another TI/RI event(s) is detected before the TI/RI bits are cleared for the previous event.	The RI/TI status bits are set whenever the Transfer Complete event is detected and gets reset whenever software driver clears those bits by writing 1. However, if another Transfer Complete event is detected before it is cleared (serviced) by the software, then Ethernet peripheral automatically set these status bits again. However, the *sbd_intr_o* signal is not generated based on TI/RI. The NIS status bit is not asserted for RI/TI events.

47.5.16.2 Interrupts from MTL

MTL interrupt events are combined with events in DMA to generate interrupt signals. The MTL interrupt status register reports the queue number responsible for the event. The MTL queue interrupt control status register should be read to obtain event descriptions.

MTL interrupts are disabled by default. When the corresponding bit in the MTL queue interrupt control status register

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

is set to 1, each event can trigger an interrupt.

MTL interrupt signals are driven by one of the following events:

- Receive queue overflow
- Transmit queue underflow

47.5.16.3 Interrupts from MAC

Interrupts can be generated from the MAC as a result of various events in the MAC Receiver, Transmitter, or the optional modules/functions such as RMON counters, EEE and so on.

These interrupt events are combined with the events in the DMA on the *sbd_intr_o* signal. The MAC interrupts are of level type, that is, the interrupt remains asserted (high) until it is cleared by the application or software.

The MAC Interrupt Status register describes the events that can cause an interrupt from the MAC. The MAC interrupts are disabled by default. Each event can assert the interrupt on the *sbd_intr_o* signals when the corresponding bit is set in the MAC Interrupt Enable register.

The interrupt register bits only indicate the block from which the event is reported. You must read the corresponding status registers and other registers to clear the interrupt.

MAC interrupt signals are triggered by one of the following events:

- Receive status interrupt
- Transmit status interrupt
- Timestamp interrupt status
- MMC interrupt status
- MMC receive checksum offload interrupt status
- MMC transmit interrupt status
- MMC receive interrupt status
- LPI interrupt status
- PMT interrupt status
- PHY interrupt

Note: The following two sideband signals are generated together with the LPI and PMT interrupts: lpi_intr_o and pmt_intr_o. These signals are used for wake-up event detection at the EXTI level.

Note: By default, the MAC interrupt status bits are cleared when the register that contains the source of the interrupt is read. If RCWE bit in the MAC CSR SW Ctrl register is programmed to 1, the MAC interrupt status bits are cleared when the bit that contains the source of the interrupt is explicitly written to 1.

LPI interrupt

The MAC generates the LPI interrupt when the Tx or Rx side enters or exits the LPI state. The interrupt *sbd_intr_o* is asserted when the LPI interrupt status is set. The LPI interrupt can be cleared by reading the MAC LPI Control Status register.

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Email: sales@nsing.com.sg

When the MAC exits the Rx LPI state, then in addition to the *sbd_intr_o*, the sideband signal *lpi_intr_o* (synchronous to Rx clock) is asserted. The *lpi_intr_o* signal can be used to trigger the external clock-gating circuitry to restore the application clock to the MAC. The *lpi_intr_o* signal, synchronous to the Rx clock domain, is provided so that you can stop the application clock when the MAC is in the LPI state.

The *lpi_intr_o* signal is generated in the Rx clock domain. It may not be cleared immediately after the MAC LPI Control Status register is read. This is because the clear signal, generated in CSR clock domain, has to cross the Rx clock domain, and then clear the interrupt source. This delay is at least four clock cycles of Rx clock and can be significant when the Ethernet peripheral is operating in the 10Mbps mode.

47.5.17 Programming Guide

This chapter provides instructions on how to initialize DMA or MAC registers in the correct order, as well as a programming guide for some functions.

Note: When any register content is being transferred to a different clock domain after a write operation, there should not be any further writes to the same location until the first write is updated. Otherwise, the second write operation does not get updated to the destination clock domain. Therefore, the delay between two writes to the same register location should be at least 4 cycles of the destination clock (PHY Receive clock, PHY Transmit clock, or PTP clock).

47.5.17.1 Initializing DMA

Complete the following steps to initialize the DMA:

1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA Mode register).
2. Wait for the completion of the reset process (poll bit 0 of the DMA Mode register, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA SysBus Mode register:
   a) AAL
   b) Fixed burst or undefined burst
   c) Burst mode values in case of AHB bus interface
4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see 47.5.15.
5. Program the Transmit and Receive Ring length registers (DMA CH0 TxDesc Ring Length register and DMA CH0 RxDesc Ring Length register). The ring length programmed must be at least 4.

   Note: The descriptor address from the start to the end of the ring must not cross the 4GB boundary.
6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA CH0 TxDesc List Address register, DMA CH0 RxDesc List Address register). Also, program transmit and receive tail pointer registers indicating to the DMA about the available descriptors (DMA CH0 TxDesc Tail Pointer register and DMA CH0 RxDesc Tail Pointer register).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:

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Email: sales@nsing.com.sg

- ETH DMA CH0 Control register (ETH_DMACH0CTRL)
- ETH DMA CH0 Tx Control register (ETH_DMACH0TXCTRL)
- ETH DMA CH0 Rx Control register (ETH_DMACH0RXCTRL)

8. Enable the interrupts by programming the DMA CH0 Interrupt Enable register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of the DMA CH0 RX Control register and ST (bit 0) of the DMA CH0 TX Control register.

47.5.17.2 Initializing MTL

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands. Complete the following steps to initialize the MTL registers:

1. Program the following fields to initialize the mode of operation in the MTL Tx Queue Operation Mode register.
   a) Transmit Store and Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
2. Program the following fields to initialize the mode of operation in the MTL Rx Queue Operation Mode register:
   a) Receive Store and Forward (RSF) or RTC in case of Threshold mode
   b) Error Packet and undersized good Packet forwarding enable (FEP and FUP)

47.5.17.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA. The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.

1. Provide the MAC address registers: MAC Address0 High register and MAC Address0 Low register. And appropriately program the other 3 additional MAC addresses.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC Packet Filter register:
   a) Receive All
   b) Promiscuous mode
   c) Hash or Perfect Filter
   d) Unicast, multicast, broadcast, and control frames filter settings
3. Program the following fields for proper flow control in the MAC Tx Flow Ctrl register:
   a) Pause time and other Pause frame control bits
   b) Transmit Flow control bits
   c) Flow Control Busy
4. Program the MAC Interrupt Enable register, as required, and if applicable, for your configuration.
5. Program the appropriate fields in the MAC Configuration register. For example: Inter-packet gap while

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

transmission and jabber disable.

6. Set bit 0 and 1 in the MAC Configuration register to start the MAC transmitter and receiver.

To support Jumbo Transmit/Receive packets, follow these steps:

In the MAC Configuration register

a) Set JE field to 1

b) Set JD and WD fields to 0

To avoid giant packet error reporting

c) Set GPSLCE field to 1

d) Set GPSL field of the MAC Ext Configuration register to a value > 9026

To support Transmit/Receive packets, up to 16K, follow these steps:

In the MAC Configuration register

a) Set JD and WD fields to 1

To avoid giant packet error reporting

b) Set GPSLCE field to 1

c) Set GPSL field of the MAC Ext Configuration register to 16383

47.5.17.4 Performing Normal Receive and Transmit Operation

During normal operation of the Ethernet peripheral, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging. For normal operation, complete the following steps:

1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA CH0 TxDesc Tail Pointer register and DMA CH0 RxDesc Tail Pointer register).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA CH Current App TxDesc register and DMA CH0 Current App RxDesc register).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (DMA CH0 Current App TxBuffer register and DMA CH0 Current App RxBuffer register).

47.5.17.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.

1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA CH0 TX Control register.

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2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL TxQ Debug register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC Configuration register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL TxQ Debug register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 in MTL TxQ Debug register and RXQSTS is 0 in MTL RxQ Debug register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

Note: Do not change the configuration (such as duplex mode, speed, port, or loop back) when the MAC is actively transmitting or receiving. These parameters are changed by software only when the MAC transmitter and receiver are not active. Similarly, do not change the DMA-related configuration when Transmit and Receive DMA are active.

47.5.17.6 Switching to New Descriptor List in RxDMA

Switching to a new descriptor list is different in the Rx DMA compared to the Tx DMA. Switching to a new descriptor list is permitted when the RxDMA is in SUSPEND state, as clarified by the following points:

- Generally, RxDMA prepares the descriptors in advance.
- If the RxDMA goes to SUSPEND due to descriptors not being available, a major failure occurs (software is not able to free the filled-up descriptors/buffers). If this issue is not rectified immediately, frames are lost because of an RxFIFO Overflow. Therefore, the software is allowed to create a new descriptor list and program the RxDMA to start using it immediately, without going into STOP state.

47.5.17.7 Switching the AHB Clock Frequency

To dynamically change the AHB clock frequency (without applying soft reset or hard reset), follow these steps:

1. Disable the Transmit DMA (if applicable) and wait for any previous frame transmissions to complete. When the frame transmissions is complete, the Tx FIFO becomes empty and the Tx DMA enters the STOP state. The Tx FIFO status is given in the MTL TxQ Debug register and the status of DMA is given in the DMA Debug Status register.
2. Disable the MAC transmitter and the MAC receiver by clearing the appropriate bits in MAC Configuration register.
3. Disable the Receive DMA (if applicable) after making sure that the data in the Rx FIFO is transferred to the system memory. The Rx FIFO empty status is given in MTL RxQ Debug register.
4. Ensure that the application does not perform any register read or write operation.
5. Change the frequency of the AHB clock.
6. Enable the MAC Transmitter or the MAC Receiver and the Transmit or Receive DMA.

These steps ensure that no valid data is present in the Tx FIFO or Rx FIFO at the time of clock frequency switching and prevent any data corruption

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Email: sales@nsing.com.sg

47.5.17.8 GMII Link State Transitions -- Transmit and Receive Clocks Running when Link Down

Complete the following steps when the link is down but the Transmit and Receive clocks are running:

1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA CH0 TX Control register.
2. Disable the MAC receiver by clearing Bit 2 (RE) of MAC Configuration register.
3. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL TxQ Debug register (TRCSTS is not 01). Or, Flush the Tx FIFO for faster empty operation.
4. Disable the MAC transmitter by clearing Bit 1(TE) of the MAC Configuration register.
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 in MTL TxQ Debug register and RXQSTS is 0 in MTL RxQ Debug register).
6. After the link is up, read the PHY registers to know the latest configuration and accordingly program the MAC registers.
7. Restart the operation by starting the Tx DMA, and then enabling the MAC Transmitter and Receiver.You do not need to disable the Rx DMA. As the Receiver is disabled, the FIFO does not get any data in the Rx FIFO.

47.5.17.9 GMII Link State Transitions -- Transmit and Receive Clocks Stopped when Link Down

Complete the following steps when the link is down and the Transmit and Receive clocks are stopped:

1. Disable the MAC Transmitter and Receiver by clearing bits RE and TE of MAC Configuration register. This does not take effect immediately as the clocks are absent.
2. Wait until the link is up and the clocks are restored.
3. Wait for the completion of the transfer of any partial frame, if any, at time of stopping of Transmit/Receive clock. This can be checked by reading the MAC Debug register (should be all-zero). Some old packets may still remain in the TXFIFO as the MAC Transmitter is stopped.
4. Read the PHY registers to know the latest operating mode and accordingly program the MAC registers.
5. Restart the MAC Transmitter and Receiver by setting RE and TE bits.

47.5.17.10 IEEE 1588 Timestamping -- System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC Timestamp Control register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during Ethernet peripheral initialization:

1. Mask the Timestamp Trigger interrupt by clearing the bit 12 of MAC Interrupt Enable register.
2. Set Bit 0 of MAC Timestamp Control register to enable timestamping.
3. Program MAC SubSecond Increment register based on the PTP clock frequency.
4. If you are using the Fine Correction approach, program MAC Timestamp Addend and set Bit 5 of MAC Timestamp Control register.
5. Poll the MAC Timestamp Control register until Bit 5 is cleared.

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6. Program Bit 1 of MAC Timestamp Control register to select the Fine Update method (if required).
7. Program MAC System Time Seconds Update register and MAC System Time Nanoseconds Update register with the appropriate time value.
8. Set Bit 2 in MAC Timestamp Control register. The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers.

   If one-step timestamping is enabled

   a) To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.

   b) Program registers MAC Timestamp Ingress Asym Corr and MAC Timestamp Egress Asym Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

Note: If timestamp operation is disabled by clearing Bit 0 of MAC Timestamp Control register, repeat all these steps to restart the timestamp operation.

47.5.17.11 IEEE 1588 Timestamping -- System Time Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:

1. Set the offset (positive or negative) in the Timestamp Update registers (MAC System Time Seconds Update register and MAC System Time Nanoseconds Update register).
2. Set Bit 3 (TSUPDT) of MAC Timestamp Control register.

The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

47.5.17.12 IEEE 1588 Timestamping -- System Time Fine Correction Method

To synchronize or update the system time to reduce system-time jitter (fine correction method), complete the following steps:

1. With the help of the algorithm explained in 47.5.6.9 calculate the rate by which you want to make the system time increments slower or faster.
2. Update the MAC Timestamp Addend register with the new value and set Bit 5 of the MAC Timestamp Control register.
3. Wait for the time for which you want the new value of the Addend register to be active. You can do this by enabling the Timestamp Trigger interrupt after the system time reaches the target value.
4. Program the required target time in MAC PPS Target Time Seconds register and MAC PPS Target Time Nanoseconds register.
5. Enable the Timestamp interrupt in bit 12 of MAC Interrupt Enable register.
6. When this trigger causes an interrupt, read MAC Interrupt Status register.
7. Reprogram MAC Timestamp Addend register with the old value and set bit 5 again

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Email: sales@nsing.com.sg

47.5.17.13 PTP Offload -- Automatic Periodic Generation of PTP Sync Messages

Follow these steps to enable automatic periodic generation of PTP sync messages:

1. Program SNAPTYPSEL, TSMSTRENA, and TSEVNTENA fields of MAC Timestamp Control register to 0, 1, and 1 respectively, to configure the node as Ordinary or Boundary Master (1, 1, and 1 for Transparent Master).
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to send in egress PTP Sync message.
3. Program the ASYNCEN bit of MAC PTO Control register to enable periodic generation of PTP Sync messages.
4. Program the 80-bit Source Port Identity in MAC Source Port Identity0, MAC Source Port Identity1 and MAC Source Port Identity2 registers to send in egress PTP Sync message.
5. Program the LSI field of MAC Log Message Interval register to program the periodicity of the PTP Sync messages. For example, value of 1 corresponds to 2^1 which translates to PTP Sync message every 2 seconds and value of 0xFF (twos complement of -1) corresponds to 2^{-1} which translates to PTP Sync message every 0.536 seconds.
6. Program the TSIE bit of MAC Interrupt Enable register to enable generation of Timestamp Interrupt.
7. Wait for *sbd_intr_o* interrupt generated on setting of TXTSSIS bit in MAC Timestamp Status register, which indicates that the timestamp for PTP Sync message is captured in MAC Tx Timestamp Status Seconds and MAC Tx Timestamp Status Nanoseconds registers.

47.5.17.14 PTP Offload -- Periodic Generation of PTP Pdelay_Req Messages

Follow these steps to enable automatic periodic generation of PTP Pdelay_Req messages:

1. Program SNAPTYPSEL, TSMSTRENA and TSEVNTENA fields of MAC Timestamp Control register to 1, 0, and 1 respectively to configure the node as Transparent Slave (1, 1, and 1 for Transparent Master OR 3, X, and X for Peer-to-Peer Transparent).
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to send in egress PTP Pdelay_Req message.
3. Program the APDREQEN bit of MAC PTO Control register to enable periodic generation of PTP Pdelay_Req messages.
4. Program the 80-bit Source Port Identity in MAC Source Port Identity0, MAC Source Port Identity1 and MAC Source Port Identity2 registers to send in egress PTP Pdelay_Req message.
5. Program the LMPDRI field of MAC Log Message Interval register to program the periodicity of the PTP Pdelay_Req messages. For example, value of 1 corresponds to 2^1 which translates to PTP Pdelay_Req message every 2 seconds and value of 0xFF (twos complement of -1) corresponds to 2^{-1} which translates to PTP Pdelay_Req message every 0.536 seconds.
6. Program the TSIE bit of MAC Interrupt Enable register to enable generation of Timestamp Interrupt.
7. Wait for sbd_intr_o interrupt generated on setting of TXTSSIS bit in MAC Timestamp Status register, which indicates that the timestamp for PTP Sync message is captured in MAC Tx Timestamp Status Seconds and MAC Tx Timestamp Status Nanoseconds registers.

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Email: sales@nsing.com.sg

47.5.17.15 PTP Offload -- Generation of PTP Response Messages for Ordinary or Boundary Master mode

Follow these steps to enable generation of PTP response messages for Ordinary or Boundary Master mode (Periodic PTP Sync messages generated and PTP Delay_Resp message generated in response to PTP Delay_Req message):

1. Program SNAPTYPSEL, TSMSTRENA and TSEVNTENA fields of MAC Timestamp Control register to 0, 1, and 1 respectively.
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to match with ingress PTP Delay_Req message and send in egress PTP Delay_Resp message.
3. Program the 80-bit Source Port Identity in MAC Source Port Identity0, MAC Source Port Identity1 and MAC Source Port Identity2 registers to match with ingress PTP Delay_Req message and send in egress PTP Delay_Resp message.
4. Program the DRSYNCR and LSI fields in MAC Log Message Interval register, the sum of both these fields is updated in logMinDelayReqInterval field of PTP Delay_Resp message.

47.5.17.16 PTP Offload -- Generation of PTP response messages for Ordinary or Boundary Slave mode

Follow these steps to enable generation of PTP response messages for Ordinary or Boundary Slave mode (PTP Delay_Req message generated in response to PTP Sync message):

1. Program SNAPTYPSEL, TSMSTRENA and TSEVNTENA fields of MAC Timestamp Control register to 0, 0, and 1 respectively.
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to match with ingress PTP Sync message and send in egress PTP Delay_Req message.
3. Program the 80-bit Source Port Identity in MAC Source Port Identity0, MAC Source Port Identity1 and MAC Source Port Identity2 registers to match with ingress PTP Sync message and send in egress PTP Delay_Req message.
4. Program the DRSYNCR field in MAC Log Message Interval register to indicate one PTP Delay_Req message is generated in response to how many received PTP Sync messages.

47.5.17.17 PTP Offload -- Generation of PTP response messages for Transparent Slave mode

Follow these steps to enable generation of PTP response messages for Transparent Slave mode (PTP Delay_Req message generated in response to PTP Sync message, PTP Pdelay_Resp message generated in response to PTP Pdelay_Req message and Periodic PTP Pdelay_Req messages generated):

1. Program SNAPTYPSEL, TSMSTRENA and TSEVNTENA fields of MAC Timestamp Control register to 1, 0, and 1 respectively.
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to match with ingress PTP Sync or Pdelay_Req message and send in egress PTP Delay_Req or Pdelay_Resp or Pdelay_Req message.
3. Program the 80-bit Source Port Identity in MAC Source Port Identity0, MAC Source Port Identity1 and MAC Source Port Identity2 registers to match with ingress PTP Sync or Pdelay_Req message and send in egress PTP

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Email: sales@nsing.com.sg

Delay_Req or Pdelay_Resp or Pdelay_Req message.

4. Program the DRSYNCR and LMPDRI fields in MAC Log Message Interval register to indicate one PTP Delay_Req message is generated in response to how many received PTP Sync messages and periodicity of the PTP Pdelay_Req messages.
5. Program the TSIE bit of MAC Interrupt Enable register to enable generation of Timestamp Interrupt.
6. Wait for *sbd_intr_o* interrupt generated on setting of TXTSSIS bit in MAC Timestamp Status register, which indicates that the timestamp for PTP Sync message is captured in MAC Tx Timestamp Status Seconds and MAC Tx Timestamp Status Nanoseconds registers for egress PTP Pdelay_Req and Pdelay_Resp messages.

47.5.17.18 PTP Offload -- Generation of PTP response messages for Transparent Master mode

Follow these steps to enable generation of PTP response messages for Transparent Master mode (PTP Delay_Resp message generated in response to PTP Delay_Req message, PTP Pdelay_Resp message generated in response to PTP Pdelay_Req message and Periodic PTP Pdelay_Req or Sync messages generated):

1. Program SNAPTYPSEL, TSMSTRENA and TSEVNTENA fields of MAC Timestamp Control register to 1, 1, and 1 respectively.
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to match with ingress PTP Delay_Req or Pdelay_Req message and send in egress PTP Delay_Resp or Pdelay_Resp or Pdelay_Req or Sync message.
3. Program the 80-bit Source Port Identity in MAC Source Port_Identity0, MAC Source Port Identity1 and MAC Source Port Identity2 registers to match with ingress PTP Delay_Req or Pdelay_Req message and send in egress PTP Delay_Resp or Pdelay_Resp or Pdelay_Req or Sync message.
4. Program the DRSYNCR, LSI and LMPDRI fields in MAC Log Message Interval register, the sum of DRSYNCR and LSI is updated in logMinDelayReqInterval field of PTP Delay_Resp message and periodicity of the PTP Sync or Pdelay_Req messages.
5. Program the TSIE bit of MAC Interrupt Enable register to enable generation of Timestamp Interrupt.
6. Wait for *sbd_intr_o* interrupt generated on setting of TXTSSIS bit in MAC Timestamp Status register, which indicates that the timestamp for PTP Sync message is captured in MAC Tx Timestamp Status Seconds and MAC Tx Timestamp Status Nanoseconds registers for egress PTP Sync, Pdelay_Req and Pdelay_Resp messages.

47.5.17.19 PTP Offload -- Generation of PTP response messages for Peer-to-Peer Transparent mode

Follow these steps to enable generation of PTP response messages for Peer-to-Peer Transparent mode (PTP Pdelay_Resp message generated in response to PTP Pdelay_Req message and Periodic PTP Pdelay_Req messages generated):

1. Program the SNAPTYPSEL, TSMSTRENA and TSEVNTENA fields of MAC Timestamp Control register to 3, X, and X respectively.
2. Program the PTOEN bit and DN field of MAC PTO Control register to enable PTP Offload feature and domain Number to match with ingress PTP Pdelay_Req message and send in egress PTP Pdelay_Resp message.
3. Program the 80-bit Source Port Identity in MAC Source Port Identity0, MAC Source Port Identity1 and MAC

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Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Source Port Identity2 registers to match with ingress PTP Pdelay_Req message and send in egress PTP Pdelay_Resp message.

4. Program the LMPDRI field in MAC Log Message Interval register to indicate periodicity of the PTP Pdelay_Req messages.
5. Program the TSIE bit of MAC Interrupt Enable register to enable generation of Timestamp Interrupt
6. Wait for *sbd_intr_o* interrupt generated on setting of TXTSSIS bit in MAC Timestamp Status register, which indicates that the timestamp for PTP Sync message is captured in MAC Tx Timestamp Status Seconds and MAC Tx Timestamp Status Nanoseconds registers for egress PTP Pdelay_Req and Pdelay_Resp messages.

47.5.17.20 Energy Efficient Ethernet (EEE) -- Entering and Exiting the Tx LPI Mode

During the ETH initialization, after you enable the EEE you can program how to enter and exit Tx LPI mode: EEE enables the IEEE 802.3 Media Access Control (MAC) sub layer along with a family of Physical layers to operate in the Low-Power Idle (LPI) mode. In the Transmit path, the software must set the LPIEN bit of the MAC LPI Control Status register to indicate to the MAC to stop transmission and initiate the LPI protocol. Follow these steps while initializing ETH:

1. Read the PHY register through the MDIO interface, check if the remote end has the EEE capability, and then negotiate the timer values.
2. Program the PHY registers through the MDIO interface (including the RX_CLK_stoppable bit that indicates to the PHY whether to stop Rx clock in LPI mode.)
3. Program Bits[25:16] and Bits[15:0] in MAC LPI Timers Control register.
4. Read the link status of the PHY chip by using the MDIO interface and update Bit 17 of MAC LPI Control Status accordingly. This update should be done whenever the link status in the PHY chip changes.
5. Program the MAC 1US Tick Counter as per the frequency of the clock used for accessing the CSR slave port.
6. Program the MAC LPI Entry Timer register (LPIET) with the IDLE time for which the MAC should wait before entering the LPI state on its own.
7. Set LPITE and LPITXA (bit[20:19]) of MAC LPI Control Status register to enable the auto-entry into LPI and auto-exit of MAC from LPI state.
8. Program the MAC 1US Tick Counter as per the frequency of the clock used for accessing the CSR slave port.
9. Program the MAC LPI Entry Timer register (LPIET) with the IDLE time for which the MAC should wait before entering the LPI state on its own.
10. Set LPITE and LPITXA (bit[20:19]) of MAC LPI Control Status register to enable the auto-entry into LPI and auto-exit of MAC from LPI state.
11. Set Bit 16 of MAC LPI Control Status register to make the MAC Transmitter enter the LPI state. The MAC enters the LPI mode after completing all scheduled packets and remains IDLE for the time indicated by LPIET. It sets the TLPIEN (bit[0]) after entry to LPI state.
12. When a packet is scheduled for transmission (when the TxDMA comes out of IDLE state or when a packet is presented at ATI or MTI interface), the MAC Transmitter exits LPI state automatically. It waits for TWT time before setting the TLPIEX interrupt status bit and then resume the packet transmission.

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13. MAC Transmitter re-enters LPI state if it remains IDLE for LPIET time and sets the TLPIEN bit and the entry-exit cycle continues.
14. Reset LPITXEN in case the application wants to over-ride the auto-entry/exit modes and make the MAC Transmitter exit the LPI state directly.

Note: To ensure MAC enter the LPI state only after completion of transmission of all the queued frames in the Tx FIFO, you should set Bit 19 in MAC LPI Control Status register.

47.5.17.21 Flexible Pulse-Per-Second Output -- Generating Single Pulse on PPS

To generate single pulse on PPS:

1. Program 11 or 10 (for interrupt) in Bits [6:5], TRGTMODSEL, of MAC PPS Control register. This instructs the MAC to use the Target Time registers (MAC PPS Target Time Seconds register and MAC PPS Target Time Nanoseconds register) for start time of PPS signal output.
2. Program the start time value in the Target Time registers (MAC PPS Target Time Seconds register and MAC PPS Target Time Nanoseconds register).
3. Program the width of the PPS signal output in MAC PPS Width register.
4. Program Bits [3:0], PPSCMD, of MAC PPS Control register to 0001. This instructs the MAC to generate single pulse on the PPS signal output at the time programmed in the Target Time registers.

47.5.17.22 Flexible Pulse-Per-Second Output -- Generating Next Pulse on PPS

When the PPSCMD is executed (PPSCMD bits = 0), you can cancel the pulse generation by giving the Cancel Start Command (PPSCMD=0011) before the programmed start time elapses. You can also program the behavior of the next pulse in advance. To program the next pulse, follow this procedure:

1. Program the start time for the next pulse in the Target Time registers. This time should be more than the time at which the falling edge occurs for the previous pulse.
2. Program the width of the next PPS signal output in MAC PPS Width register.
3. Program Bits [3:0], PPSCMD, of MAC PPS Control to generate a single pulse after the time at which the previous pulse is de-asserted. This instructs the MAC to generate single pulse on the PPS signal output, at the time programmed in Target Time registers.

   If you give this command before the previous pulse becomes low, then the new command overwrites the previous command and the QOS may generate only 1 extended pulse.

47.5.17.23 Flexible Pulse-Per-Second Output -- Generating a Pulse Train on PPS

Complete the following steps to generate a pulse train on PPS:

1. Program 11 or 10 (for interrupt) in Bits [6:5], TRGTMODSEL, of MAC PPS Control register. This instructs the MAC to use the Target Time registers for start time of the PPS signal output.
2. Program the start time value in the Target Time registers.
3. Program the interval value between the train of pulses on the PPS signal output in the MAC PPS Interval register.
4. Program the width of the PPS signal output in MAC PPS Width register.

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5. Program Bits[3:0], PPSCMD, of MAC PPS Control register to 0010. This instructs the MAC to generate train of pulses on the PPS signal output with start time programmed in Target Time registers. By default, the PPS pulse train is free-running unless stopped by 'STOP Pulse train at time' or 'STOP Pulse Train immediately' commands.
6. Program the stop value in the Target Time registers. Ensure that Bit 31 (TSTRBUSY) of MAC PPS Target Time Nanoseconds register is reset before programming the Target Time registers again.
7. Program the PPSCMD field (bit 3:0) of MAC PPS Control to 0100. This stops the train of pulses on PPS signal output after the programmed stop time specified in Step 6 elapses.

   You can stop the pulse train at any time by programming 0101 in the PPSCMD field. Similarly, you can cancel the Stop Pulse train command (given in Step 7) by programming 0110 in the PPSCMD field before the time (programmed in Step 6) elapses. You can cancel the pulse train generation by programming 0011 in the PPSCMD field before the programmed start time (in Step 2) elapses

47.5.17.24 Flexible Pulse-Per-Second Output -- Generating an Interrupt without Affecting the PPS

The Bits [6:5], TRGTMODSEL, of the MAC PPS Control register enable you to program the Target Time registers to do any one of the following:

- Generate only interrupts.
- Generate interrupts and the PPS start and stop time.
- Generate only PPS start and stop time.

Complete the following steps to program the Target Time registers to generate only interrupt event:

1. Program 00 (for interrupt) in Bits [6:5], TRGTMODSEL, of MAC PPS Control register. This instructs the MAC to use the Target Time registers for target time interrupt.
2. Program a target time value in the Target Time registers. This instructs the MAC to generate an interrupt when the target time elapses.

   If Bits [6:5], TRGTMODSEL, are changed (for example, to control the PPS), then the interrupt generation is over-written with the new mode and new programmed Target Time register value.

Note: The interrupt is generated when the programmed target time is smaller (that is, time in the past) compared to system time in the MAC System Time Seconds and MAC System Time Nanoseconds registers. Therefore, to avoid unwanted interrupt, the correct writing order is as follows:

1. *ETH MAC PPS Target Time Nanoseconds register (ETH_MACPPSTTNS)*
2. *ETH MAC PPS Target Time Seconds register (ETH_MACPPSTTS)*
3. *ETH MAC PPS Interval register (ETH_MACPPSINTE)*
4. *ETH MAC PPS Width register (ETH_MACPPSWID)*
5. *PPSCTRL_PPSCMD and PPSEN0 fields of MAC PPS Control register*

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Email: sales@nsing.com.sg

47.5.17.25 TCP Segmentation Offload (TSO)

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet. Complete the following steps to program TSO:

1. Program the TSE bit of corresponding DMA CH0 Tx Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
   a) Enable TSE in Bit 18 of TDES3
   b) Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3
   c) Program the maximum size of the segment in MSS of DMA CH0 Control register or MSS in the context descriptor.

      If MSS field is programmed in both DMA CH0 Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

Note: If TSE is enabled in TDES3 for a non-TCP-IP packet, the result is unpredictable.

47.5.17.26 VLAN Filtering on Receive

Complete the following steps to program VLAN filtering on receive:

1. Program MAC VLAN Tag register for the following bit to select the filtering method:
   a) ETV: Enable 12-Bit VLAN Tag Comparison or 16-bit VLAN Tag comparison
   b) VTHM: VLAN Tag Hash Table Match Enable
   c) ERIVLT: Enable inner VLAN Tag or outer VLAN Tag (to enable the inner or outer VLAN Tag filtering, Double VLAN Processing should enabled by setting EDVLP)
   d) ERSVLM: Enable Receive S-VLAN Match or C-VLAN match (for S-VLAN processing to be enabled, set ESVL)
   e) DOVLTC: Ignores VLAN Type for Tag Match
   f) VTIM: to enable VLAN Tag Inverse Match instead of the normal VLAN Tag matching
2. Program VL field of MAC VLAN Tag register for the 12-bit or 16-bit VLAN tag.
3. If Hash filtering of VLAN tag is enabled, program MAC VLAN Hash Table register. When ETV bit is reset, upper 4 bits of the calculated CRC-32 of VLAN Tag are inverted and used to index the content of MAC VLAN Hash Table register. When ETV bit is set, upper 4 bits of calculated CRC-32 of VLAN Tag are used to index the content of MAC VLAN Hash Table register. For example, when ETV bit is set, a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table. When ETV bit is reset a hash value of 4'b1000 selects Bit 7 of the VLAN Hash

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Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

table.

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Email: sales@nsing.com.sg

47.6 Registers

ETH consists of the following registers:

- MAC registers, which include MMC-related registers (refer to section 47.6.1)
- MTL registers (refer to section 47.6.2)
- DMA registers (refer to section 47.6.3)

47.6.1 ETH MAC Registers

47.6.1.1 ETH MAC Configuration register (ETH_MACCFG)

Address offset: 0x0000

Reset value: 0x0000 0000

The MAC Configuration Register establishes the operating mode of the MAC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ARPEN	SARC[2:0]			CSO	IPG[2:0]			GPSLCE	S2KP	CST	ACS	WD	BE	JD	JE
rw	rw			rw	rw			rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS	FES	DM	LM	ECRSFD	DO	DCRS	DR	Reserved	BL[1:0]		DC	PRELEN[1:0]		TE	RE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw		rw	rw

Bit Field	Name	Description
31	ARPEN	ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. 0: ARP Offload is disabled 1: ARP Offload is enabled
30:28	SARC	Source Address Insertion or Replacement Control This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28]: **2'b0x**: ■ The mti_sa_ctrl_i and ati_sa_ctrl_i (internal signal) input signals control the SA field generation. **2'b10:** ■ If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers

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Bit Field	Name	Description
		in the SA field of all transmitted packets. ■ If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the IP, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. **2'b11**: ■ If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. ■ If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. *Note: Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.*
27	CSO	Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. 0: IP header/payload checksum checking is disabled 1: IP header/payload checksum checking is enabled
26:24	IPG	Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. This function (IPG less than 96 bit times) is valid only when EIPGEN bit in ETH_MACEXTCFG register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in ETH_MACEXTCFG register. 000: 96 bit times 001: 88 bit times 010: 80 bit times ... 111: 40 bit times
23	GPSLCE	Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in ETH_MACEXTCFG register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518

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Bit Field	Name	Description
		bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. 0x0: Giant Packet Size Limit Control is disabled 0x1: Giant Packet Size Limit Control is enabled
22	S2KP	IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. For more information about how the setting of this bit and the JE bit impact the Giant packet status, see the Table, Giant Packet Status based on S2KP and JE Bits. 0x0: Support upto 2K packet is disabled 0x1: Support upto 2K packet is enabled *Note: When the JE bit is set, setting this bit has no effect on the giant packet status.*
21	CST	CRC Stripping for Type Packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. 0: CRC stripping for Type packets is disabled 1: CRC stripping for Type packets is enabled
20	ACS	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. 0: Automatic Pad or CRC Stripping is disabled 1: Automatic Pad or CRC Stripping is enabled
19	WD	Disable Watchdog When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is

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Bit Field	Name	Description
		set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. 0: Watchdog is enabled 1: Watchdog is disabled
18	BE	Packet Burst Enable When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0: Packet Burst is disabled 1: Packet Burst is enabled *Note: ETH2 does not support this bit.*
17	JD	Disable Jabber When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. 0: Jabber is enabled 1: Jabber is disabled
16	JE	Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0: Jumbo Packet is disabled 1: Jumbo Packet is enabled
15	PS	Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. 0: For 1000Mbps operations 1: For 10Mbps or 100Mbps operations *Note: This bit is a read/write bit in ETH1 and a read-only bit in ETH2 and always reads 1.*
14	FES	Speed This bit selects the speed mode. 0: 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0 1: 100 Mbps when PS bit is 1 *Note: This bit is shared with the PS bit only in ETH1.*
13	DM	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. 0: Half-duplex mode 1: Full-duplex mode

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Bit Field	Name	Description
12	LM	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. 0: Loopback is disabled 1: Loopback is enabled
11	ECRSFD	Enable Carrier Sense Before Transmission in Full-Duplex Mode When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal. 0: ECRSFD is disabled 1: ECRSFD is enabled
10	DO	Disable Receive Own When this bit is set, the MAC disables the reception of packets when the gmii_txen_o is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode. 0: Enable Receive Own 1: Disable Receive Own
9	DCRS	Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. 0: Enable carrier sense during transmission 1: Disable carrier sense during transmission
8	DR	Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. 0: Enable retry 1: Disable retry
7	Reserved	Reserved, the reset value must be maintained.
6:5	BL[1:0]	Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt.

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Bit Field	Name	Description
		The random integer r ranges from 0 ≤ r < 2^k. This bit applicable only to half-duplex mode. 00: k = min(n, 10) 01: k = min(n, 8) 10: k = min(n, 4) 11: k = min(n, 1)
4	DC	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. 0: Deferral check function is disabled 1: Deferral check function is enabled
3:2	PRELEN[1:0]	Preamble Length for Transmit Packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 00: 7-bytes of preamble 01: 5-bytes of preamble 10: 3-bytes of preamble 11: Reserved
1	TE	Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. 0: Transmitter is disabled 1: Transmitter is enabled
0	RE	Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is

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Email: sales@nsing.com.sg

Bit Field	Name	Description
		disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. 0: Receiver is disabled 1: Receiver is enabled

Table 47-1 Gigantic Packet Status based on S2KP and JE Bits

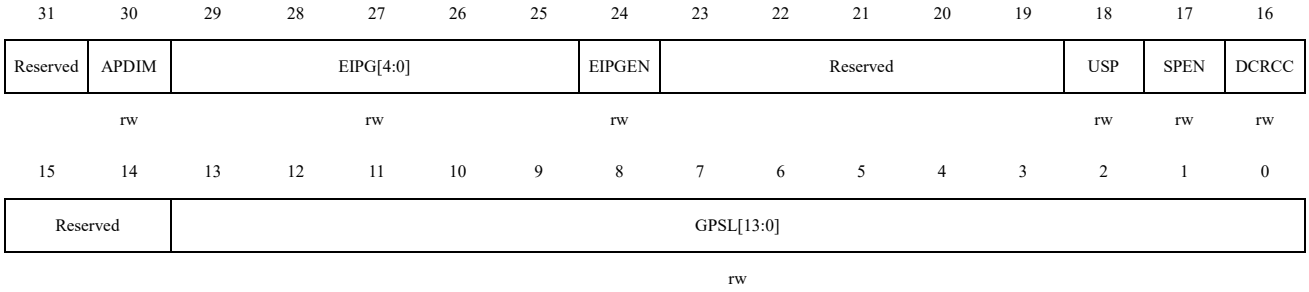
Length/Type Field	Received Packet Length	S2KP	JE	Giant Packet Status
Untagged data packet	＞1518	0	0	1
	＞2000	1	0	1
	＞9018	x	1	1
VLAN tagged data packet	＞1522	0	0	1
	＞2000	1	0	1
	＞9022	x	1	1

47.6.1.2 ETH MAC Extended Configuration register (ETH_MACEXTCFG)

Address offset: 0x0004

Reset value: 0x0000 0000

The MAC Extended Configuration Register establishes the operating mode of the MAC.



Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	APDIM	ARP Packet Drop if IP Address Mismatch When this bit is set, Packet for which Target Protocol Address does not match IPv4 address is dropped in the MTL layer. When this bit is reset, when target Protocol Address does not match, packet is forwarded to MTL maintaining backward compatibility. 0: Mux select to drop the arp packet if target protocol address mismatches IPv4 address disabled 1: Mux select to drop the arp packet if target protocol address mismatches IPv4 address enabled
29:25	EIPG	Extended Inter-Packet Gap (EIPG)

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Bit Field	Name	Description
		The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 0x00: 104 bit times 0x01: 112 bit times 0x02: 120 bit times ... 0xFF: 2144 bit times
24	EIPGEN	Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in ETH_MACCFG register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in ETH_MACCFG register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times 0: Extended Inter-Packet Gap is disabled 1: Extended Inter-Packet Gap is enabled *Note: Enable the extended Inter-Packet Gap feature only when operating in Full-Duplex mode. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode.*
23:19	Reserved	Reserved, the reset value must be maintained.
18	USP	Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC Address 0 High Register and MAC Address 0 Low Register. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. 0: Unicast Slow Protocol Packet Detection is disabled 1: Unicast Slow Protocol Packet Detection is enabled
17	SPEN	Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. 0: Slow Protocol Detection is disabled 1: Slow Protocol Detection is enabled
16	DCRCC	Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. 0: CRC Checking is enabled 1: CRC Checking is disabled

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Email: sales@nsing.com.sg

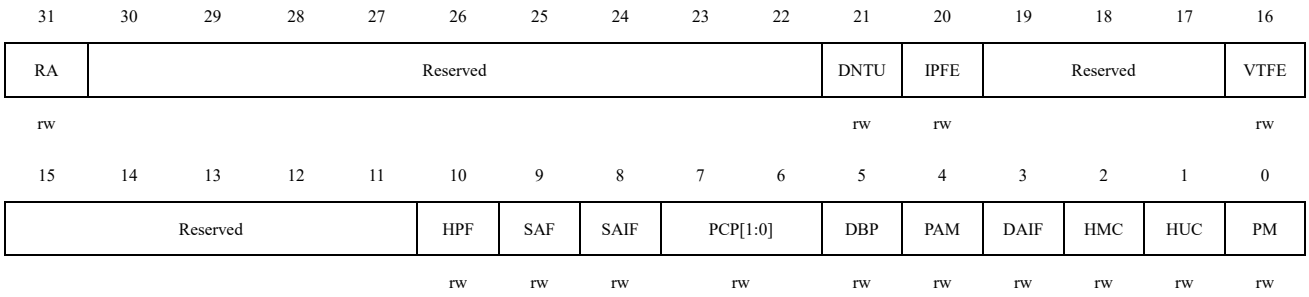
Bit Field	Name	Description
15:14	Reserved	Reserved, the reset value must be maintained.
13:0	GPSL	Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in ETH_MACCFG register.

47.6.1.3 ETH MAC Packet Filter register (ETH_MACPFLT)

Address offset: 0x0008

Reset value: 0x0000 0000

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.



Bit Field	Name	Description
31	RA	Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0: Receive All is disabled 0x1: Receive All is enabled
30:22	Reserved	Reserved, the reset value must be maintained.
21	DNTU	Drop Non-TCP/UDP over IP Packets When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC

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Bit Field	Name	Description
		forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets. 0x0: Forward Non-TCP/UDP over IP Packets 0x1: Drop Non-TCP/UDP over IP Packets
20	IPFE	Layer 3 and Layer 4 Filter Enable When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields. 0x0: Layer 3 and Layer 4 Filters are disabled 0x1: Layer 3 and Layer 4 Filters are enabled
19:17	Reserved	Reserved, the reset value must be maintained.
16	VTFE	VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. 0x0: VLAN Tag Filter is disabled 0x1: VLAN Tag Filter is enabled
15:11	Reserved	Reserved, the reset value must be maintained.
10	HPF	Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. 0x0: Hash or Perfect Filter is disabled 0x1: Hash or Perfect Filter is enabled
9	SAF	Source Address Filter Enable When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. 0x0: SA Filtering is disabled 0x1: SA Filtering is enabled *Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in this IP, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.*
8	SAIF	SA Inverse Filtering When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter.

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Bit Field	Name	Description
		When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter. 0x0: SA Inverse Filtering is disabled 0x1: SA Inverse Filtering is enabled
7:6	PCP	Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0x0: MAC filters all control packets from reaching the application 0x1: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 0x2: MAC forwards all control packets to the application even if they fail the Address filter 0x3: MAC forwards the control packets that pass the Address filter
5	DBP	Disable Broadcast Packets When this bit is set, the AFM module blocks all the incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. 0x0: Enable Broadcast Packets 0x1: Disable Broadcast Packets
4	PAM	Pass All Multicast When this bit is set, it indicates that all the received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. 0x0: Pass All Multicast is disabled 0x1: Pass All Multicast is enabled
3	DAIF	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. 0x0: DA Inverse Filtering is disabled 0x1: DA Inverse Filtering is enabled
2	HMC	Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0: Hash Multicast is disabled 0x1: Hash Multicast is enabled
1	HUC	Hash Unicast When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table.

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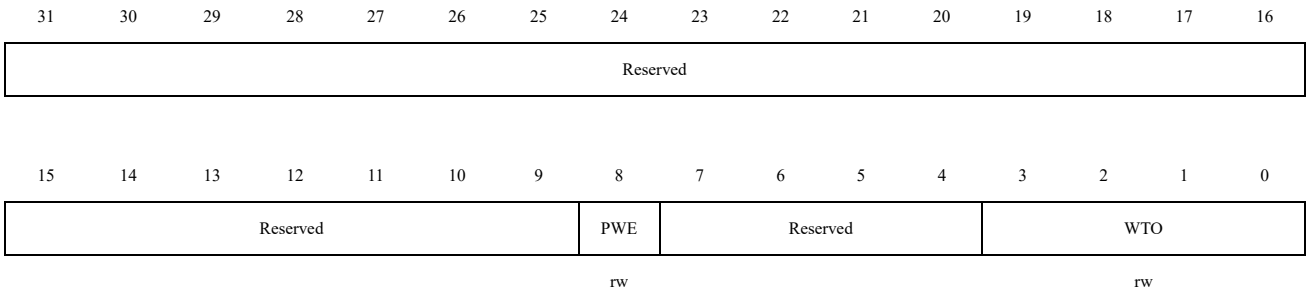
Bit Field	Name	Description
		When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. 0x0: Hash Unicast is disabled 0x1: Hash Unicast is enabled
0	PM	Promiscuous Mode When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. 0x0: Promiscuous Mode is disabled 0x1: Promiscuous Mode is enabled

47.6.1.4 ETH MAC Watchdog Timeout register (ETH_MACWDGTO)

Address offset: 0x000C

Reset value: 0x0000 0000

The Watchdog Timeout register controls the watchdog timeout for received packets.



Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	PWE	Programmable Watchdog Enable When this bit is set and the WD bit of the ETH_MACCFG register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in ETH_MACCFG register. 0x0: Programmable Watchdog is disabled 0x1: Programmable Watchdog is enabled
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	WTO[3:0]	Watchdog Timeout When the PWE bit is set and the WD bit of the ETH_MACCFG register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet.

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Bit Field	Name	Description
		0x0: 2Kbytes 0x1: 3Kbytes 0x2: 4Kbytes 0x3: 5Kbytes 0x4: 6Kbytes 0x5: 7Kbytes ... 0xD: 15Kbytes 0xE: 16383 bytes 0xF: Reserved *Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped.*

47.6.1.5 ETH MAC Hash Table register 0 (ETH_MACHASHTR0)

Address offset: 0x0010

Reset value: 0x0000 0000

The Hash Table Register 0 contains the first 32 bits of the hash table (64-bits).

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper 6-bits of the CRC register are used to index the content of the Hash table.

The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC Packet Filter register, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HT31T0[31:16]															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT31T0[15:0]															

rw

Bit Field	Name	Description
31:0	HT31T0[31:0]	MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table.

47.6.1.6 ETH MAC Hash Table register 1 (ETH_MACHASHTR1)

Address offset: 0x0014

Reset value: 0x0000 0000

The Hash Table Register 1 contains the second 32 bits of the hash table.

The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six bits of the CRC register are used to index the content of the Hash table.

The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1.

The hash value of the destination address is calculated in the following way:

- Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
- Perform bitwise reversal for the value obtained in Step 1.
- Take the upper 6 bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC Packet Filter register, all multicast packets are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HT63T32[31:16]															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT63T32[15:0]															

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Bit Field	Name	Description
31:0	HT63T32[31:0]	MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

47.6.1.7 ETH VLAN Tag register (ETH_MACVLANTAG)

Address offset: 0x0050

Reset value: 0x0000 0000

The VLAN Tag register identifies the IEEE 802.1Q VLAN type packets.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EIVLRXS	Reserved	EIVLS[1:0]		ERIVLT	EDVLP	VTHM	EVLRXS	Reserved	EVLS[1:0]		DOVLTC	ERSVLM	ESVL	VTIM	ETV
rw		rw		rw	rw	rw	rw		rw		rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VL[15:0]															

rw

Bit Field	Name	Description
31	EIVLRXS	Enable Inner VLAN Tag in Rx Status When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status. 0x0: Inner VLAN Tag in Rx status is disabled 0x1: Inner VLAN Tag in Rx status is enabled
30	Reserved	Reserved, the reset value must be maintained.
29:28	EIVLS	Enable Inner VLAN Tag Stripping on Receive This field indicates the stripping operation on inner VLAN Tag in received packet. 0x0: Do not strip 0x1: Strip if VLAN filter passes 0x2: Strip if VLAN filter fails 0x3: Always strip
27	ERIVLT	Enable Inner VLAN Tag When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present). The ERSVLM bit determines which VLAN type is enabled for filtering or matching. 0x0: Inner VLAN tag is disabled 0x1: Inner VLAN tag is enabled
26	EDVLP	Enable Double VLAN Processing

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Bit Field	Name	Description
		When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present). 0x0: Double VLAN Processing is disabled 0x1: Double VLAN Processing is enabled
25	VTHM	VLAN Tag Hash Table Match Enable When this bit is set, the most significant four bits of CRC of VLAN Tag are used to index the content of the ETH_MACVHASHT register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed. 0x0: VLAN Tag Hash Table Match is disabled 0x1: VLAN Tag Hash Table Match is enabled
24	EVLRXS	Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. 0x0: VLAN Tag in Rx status is disabled 0x1: VLAN Tag in Rx status is enabled
23	Reserved	Reserved, the reset value must be maintained.
22:21	EVLS	Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet. 0x0: Do not strip 0x1: Strip if VLAN filter passes 0x2: Strip if VLAN filter fails 0x3: Always strip
20	DOVLTC	Disable VLAN Type Check When this bit is set, the MAC does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. The VLAN filter is bypassed when VLAN Type of received packet do not match the programmed VLAN Type in the VLAN filter. 0x0: VLAN Type Check is enabled 0x1: VLAN Type Check is disabled
19	ERSVLM	Enable Receive S-VLAN Match When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for filtering or

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Bit Field	Name	Description
		matching. 0x0: Receive S-VLAN Match is disabled 0x1: Receive S-VLAN Match is enabled
18	ESVL	Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. 0x0: S-VLAN is disabled 0x1: S-VLAN is enabled
17	VTIM	VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. 0x0: VLAN Tag Inverse Match is disabled 0x1: VLAN Tag Inverse Match is enabled
16	ETV	Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. Similarly, when enabled, only 12 bits of the VLAN tag in the received packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for comparison and VLAN hash filtering. 0x0: 12-Bit VLAN Tag Comparison is disabled 0x1: 12-Bit VLAN Tag Comparison is enabled
15:0	VL[15:0]	VLAN Tag Identifier for Receive Packets This field contains the 802.1Q VLAN tag to identify the VLAN packets. This VLAN tag identifier is compared to the 15th and 16th bytes of the packets being received for VLAN packets. The following list describes the bits of this field: Bits [15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits [11:0]: VLAN Identifier (VID) field of VLAN tag When the ETV bit is set, only the VID is used for comparison. If this field ([11:0] if ETV is set) is all zeros, the MAC does not check the 15th and 16th bytes for VLAN tag comparison and declares all packets with Type field value of 0x8100 or 0x88a8 as VLAN packets.

47.6.1.8 ETH VLAN Hash Table register (ETH_MACVHASHT)

Address offset: 0x0058

Reset value: 0x0000 0000

When VTHM bit of the ETH_MACVLANTAG register is set, the 16-bit VLAN Hash Table register is used for group

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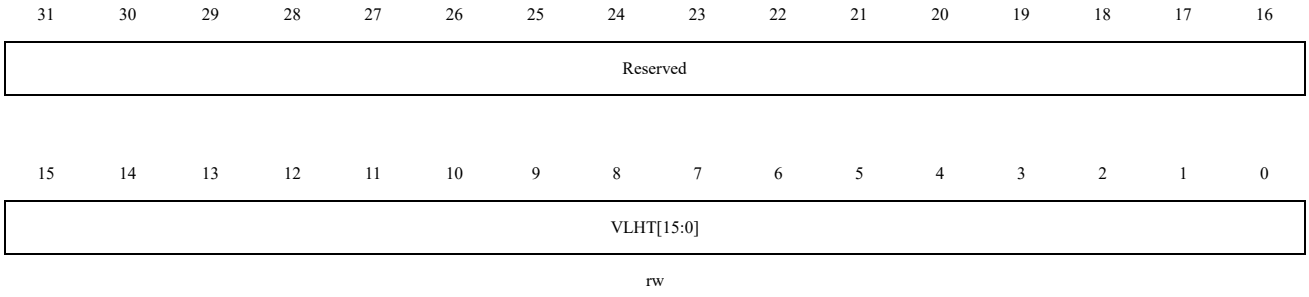
Email: sales@nsing.com.sg

address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of ETH_MACVLANTAG Register) in the incoming packet is passed through the CRC logic. The upper four bits of the calculated hash value are used to index the contents of the VLAN Hash table. For example, hash value of 4b'1000 selects Bit 8 of the VLAN Hash table.

The hash value for the destination address is calculated as follows:

1. Calculate a 32-bit CRC for the VLAN tag or ID (refer to section 3.2.8 of IEEE 802.3 for CRC32 calculation steps).
2. Perform a bit-wise reversal on the value obtained in step 1.
3. Take the high 4 bits from the value obtained in step 2.

If the VLAN hash table register is configured to be double synchronized with the (G)MII clock domain, synchronization is triggered only when writing to bit [15:8] (little-endian mode) or bit [7:0] (big-endian mode) of the register. If double synchronization is enabled, consecutive writes to this register should occur at least four clock cycles after the target clock domain.



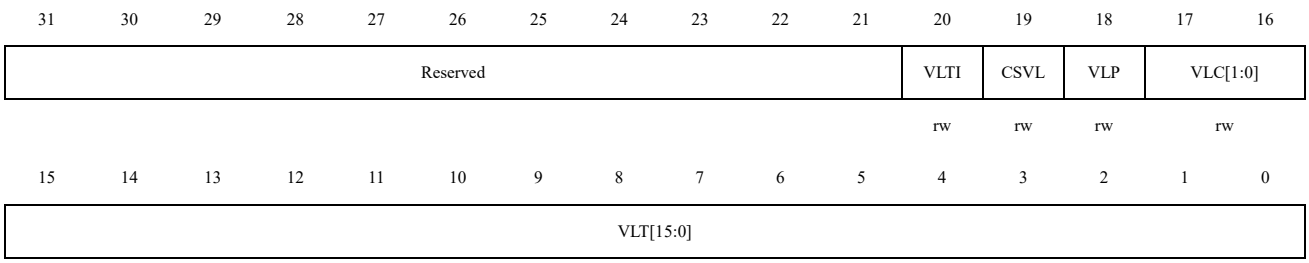
Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	VLHT[15:0]	VLAN Hash Table This field contains the 16-bit VLAN Hash Table.

47.6.1.9 ETH VLAN Inclusion register (ETH_MACVLANINC)

Address offset: 0x0060

Reset value: 0x0000 0000

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.



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Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20	VLTI	VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: The Tx descriptor. 0x0: VLAN Tag Input is disabled 0x1: VLAN Tag Input is enabled
19	CSVL	C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets. 0x0: C-VLAN type (0x8100) is inserted or replaced 0x1: S-VLAN type (0x88A8) is inserted or replaced
18	VLP	VLAN Priority Control When this bit is set, the control bits [17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits [17:16] are ignored. 0x0: VLAN Priority Control is disabled 0x1: VLAN Priority Control is enabled
17:16	VLC	VLAN Tag Control in Transmit Packets 2'b00: No VLAN tag deletion, insertion, or replacement 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). 0x0: No VLAN tag deletion, insertion, or replacement 0x1: VLAN tag deletion 0x2: VLAN tag insertion 0x3: VLAN tag replacement *Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.*
15:0	VLT	VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value

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Email: sales@nsing.com.sg

Bit Field	Name	Description
		must only be changed when the transmit lines are inactive or during the initialization phase. Bits [15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits [11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: Bits [15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits [11:0]: VLAN Identifier (VID) field of VLAN tag

47.6.1.10 ETH Inner VLAN Inclusion register (ETH_MACIVLANINC)

Address offset: 0x0064

Reset value: 0x0000 0000

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											VLTI	CSVL	VLP	VLC[1:0]	
											rw	rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLT[15:0]															
rw															

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20	VLTI	VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: The Tx descriptor. 0x0: VLAN Tag Input is disabled 0x1: VLAN Tag Input is enabled
19	CSVL	C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 17th and 18th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 17th and 18th bytes of transmitted packets. 0x0: C-VLAN type (0x8100) is inserted or replaced 0x1: S-VLAN type (0x88A8) is inserted or replaced
18	VLP	VLAN Priority Control When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored.

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Bit Field	Name	Description
		0x0: VLAN Priority Control is disabled 0x1: VLAN Priority Control is enabled
17:16	VLC	VLAN Tag Control in Transmit Packets 2'b00: No VLAN tag deletion, insertion, or replacement 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). 0x0: No VLAN tag deletion, insertion, or replacement 0x1: VLAN tag deletion 0x2: VLAN tag insertion 0x3: VLAN tag replacement *Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.*
15:0	VLT	VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits [15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits [11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: Bits [15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits [11:0]: VLAN Identifier (VID) field of VLAN tag

47.6.1.11 ETH MAC Tx Flow Control register (ETH_MACTXFLWCTRL)

Address offset: 0x0070

Reset value: 0x0000 0000

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the "Busy" bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The "Busy" bit remains set until the control packet is transferred onto the cable. The application must make sure that the "Busy" bit is cleared before writing to the register.

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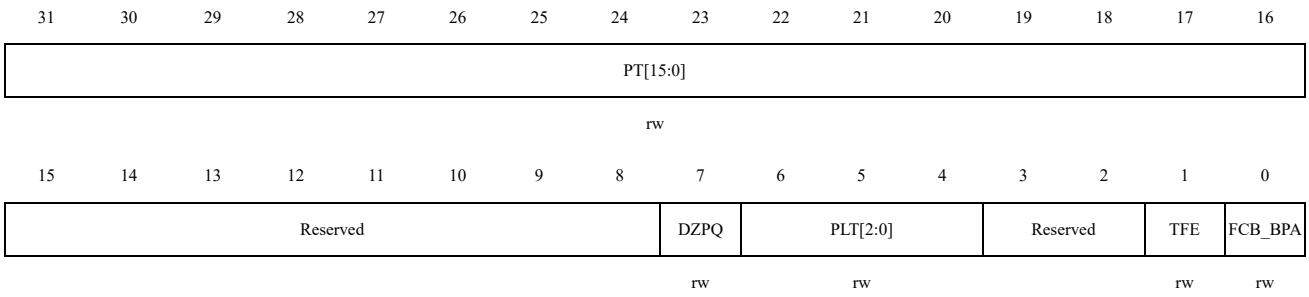

Bit Field	Name	Description
31:16	PT	Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	Reserved	Reserved, the reset value must be maintained.
7	DZPQ	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. 0x0: Zero-Quanta Pause packet generation is enabled 0x1: Zero-Quanta Pause packet generation is disabled
6:4	PLT	Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits [31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0x0: Pause Time minus 4 Slot Times (PT -4 slot times) 0x1: Pause Time minus 28 Slot Times (PT -28 slot times) 0x2: Pause Time minus 36 Slot Times (PT -36 slot times) 0x3: Pause Time minus 144 Slot Times (PT -144 slot times) 0x4: Pause Time minus 256 Slot Times (PT -256 slot times) 0x5: Pause Time minus 512 Slot Times (PT -512 slot times)

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Bit Field	Name	Description
		0x6: Reserved
3:2	Reserved	Reserved, the reset value must be maintained.
1	TFE	Transmit Flow Control Enable **Full-Duplex Mode:** In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. **Half-Duplex Mode:** In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. 0x0: Transmit Flow Control is disabled 0x1: Transmit Flow Control is enabled
0	FCB_BPA	Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. **Full-Duplex Mode:** In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. **Half-Duplex Mode:** When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. 0x0: Flow Control Busy or Backpressure Activate is disabled 0x1: Flow Control Busy or Backpressure Activate is enabled *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*

47.6.1.12 ETH MAC Rx Flow Control register (ETH_MACRXFLWCTRL)

Address offset: 0x0090

Reset value: 0x0000 0000

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	UP	RFE
	rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	UP	Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC Address0 High register and MAC Address0 Low register. When this bit is reset, the MAC only detects Pause packets with unique multicast address. 0: Unicast Pause Packet Detect disabled 1: Unicast Pause Packet Detect enabled *Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011.*
0	RFE	Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. 0x0: Receive Flow Control is disabled 0x1: Receive Flow Control is enabled

47.6.1.13 ETH MAC Interrupt Status register (ETH_MACINTSTS)

Address offset: 0x00B0

Reset value: 0x0000 0000

The Interrupt Status register contains the status of interrupts.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MDIOIS	Reserved	
													r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	RXSTSIS	TXSTSIS	TSIS	MMCRXIPIS	MMCTXIS	MMCRXIS	MMCIS	Reserved		LPIIS	PMTIS	PHYIS	Reserved		
	r	r	r	r	r	r	r			r	r	r			

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.

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Bit Field	Name	Description
18	MDIOIS	MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC CSR software control register is set. 0x0: MDIO Interrupt status not active 0x1: MDIO Interrupt status active *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
17:15	Reserved	Reserved, the reset value must be maintained.
14	RXSTSIS	Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC Rx Tx Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC CSR software control register is set) in the MAC Rx Tx Status register. 0x0: Receive Interrupt status not active 0x1: Receive Interrupt status active
13	TXSTSIS	Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC Rx Tx Status register: ■ Excessive Collision (EXCOL) ■ Late Collision (LCOL) ■ Excessive Deferral (EXDEF) ■ Loss of Carrier (LCARR) ■ No Carrier (NCARR) ■ Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC CSR software control register is set) in the MAC Rx Tx Status register. 0x0: Transmit Interrupt status not active 0x1: Transmit Interrupt status active
12	TSIS	Timestamp Interrupt Status If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: ■ The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. ■ There is an overflow in the Seconds register. ■ The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. When drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC Tx Timestamp Status Nanoseconds and MAC Tx

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Bit Field	Name	Description
		Timestamp Status Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC Tx Timestamp Status Nanoseconds and MAC Tx Timestamp Status Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC CSR software control register is set) in the MAC Timestamp Status register. 0x0: Timestamp Interrupt status not active 0x1: Timestamp Interrupt status active *Note: To generate a timestamp interrupt (if enabled) when the first condition is true, ensure that the third condition is false and set bit 4 (TSTRIG) in the MAC timestamp control register to 1.*
11	MMCRXIPIS	MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. 0: MMC Receive Checksum Offload Interrupt status not active 1: MMC Receive Checksum Offload Interrupt status active
10	MMCTXIS	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. 0: MMC Transmit Interrupt status not active 1: MMC Transmit Interrupt status active
9	MMCRXIS	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. 0: MMC Receive Interrupt status not active 1: MMC Receive Interrupt status active
8	MMCIS	MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. 0: MMC interrupt status not active 1: MMC interrupt status active
7:6	Reserved	Reserved, the reset value must be maintained.
5	LPIIS	LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC LPI Control Status register is read (or corresponding interrupt source bit of MAC LPI Control Status register is written to 1 when RCWE bit of MAC CSR software control register is set). 0x0: LPI Interrupt status not active 0x1: LPI Interrupt status active

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Bit Field	Name	Description
4	PMTIS	PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC PMT Control Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC PMT Control Status register (or corresponding interrupt source bit of MAC PMT Control Status register is written to 1 when RCWE bit of MAC CSR software control register is set). 0: PMT interrupt status not active 1: PMT interrupt status active
3	PHYIS	PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC CSR software control register is set). 0: PHY interrupt not detected 1: PHY interrupt detected
2:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.14 ETH MAC Interrupt Enable register (ETH_MACINTEN)

Address offset: 0x00B4

Reset value: 0x0000 0000

The Interrupt Enable register contains the masks for generating the interrupts.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													MDIOIE	Reserved	
													rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	RXSTSIE	TXSTSIE	TSIE	Reserved						LPIIE	PMTIE	PHYIE	Reserved		
	rw	rw	rw							rw	rw	rw			

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	MDIOIE	MDIO Interrupt Enable When this bit is set to 1, the interrupt signal is enabled in the MDIOIS bit of the MAC interrupt status register. 0: MDIO interrupt is disabled 1: MDIO interrupt is enabled
17:15	Reserved	Reserved, the reset value must be maintained.
14	RXSTSIE	Receive Status Interrupt Enable When this bit is set to 1, the interrupt signal is enabled due to the RXSTSIS bit in the

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Bit Field	Name	Description
		MAC interrupt status register. 0: Receive Status interrupt is disabled 1: Receive Status interrupt is enabled
13	TXSTSIE	Transmit Status Interrupt Enable When this bit is set to 1, the interrupt signal is enabled due to the TXSTSIS bit in the MAC interrupt status register. 0: Transmit Status interrupt is disabled 1: Transmit Status interrupt is enabled
12	TSIE	Timestamp Interrupt Enable When this bit is set to 1, the interrupt signal is enabled due to the TSIS bit in the MAC interrupt status register. 0: Timestamp interrupt is disabled 1: Timestamp interrupt is enabled
11:6	Reserved	Reserved, the reset value must be maintained.
5	LPIIE	LPI Interrupt Enable When this bit is set to 1, the interrupt signal is enabled due to the LPIIS bit in the MAC interrupt status register. 0: LPI interrupt is disabled 1: LPI interrupt is enabled
4	PMTIE	PMT Interrupt Enable When this bit is set to 1, the interrupt signal is enabled due to the PMTIS bit in the MAC interrupt status register. 0: PMT interrupt is disabled 1: PMT interrupt is enabled
3	PHYIE	PHY Interrupt Enabl When this bit is set to 1, the interrupt signal is enabled due to the PHYIS bit in the MAC interrupt status register. 0: PHY interrupt is disabled 1: PHY interrupt is enabled
2:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.15 ETH MAC Rx Tx Status register (ETH_MACRXTXSTS)

Address offset: 0x00B8

Reset value: 0x0000 0000

The Receive Transmit Status register contains the Receive and Transmit Error status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	RWT	Reserved	EXCOL	LCOL	EXDEF	LCARR	NCARR	TJT
	r		r	r	r	r	r	r

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	RWT	Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC Configuration register. 0: No Receive Watchdog Timeout 1: Receive Watchdog Time out *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
7:6	Reserved	Reserved, the reset value must be maintained.
5	EXCOL	Excessive Collisions When the DTXSTS bit is set in the MTL Operation Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC Configuration register, this bit is set after the first collision and the packet transmission is aborted. 0: No collisions 1: Excessive Collisions is sensed *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
4	LCOL	Late Collision When the DTXSTS bit is set in the MTL Operation Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. 0: No collisions 1: Late Collision is sensed *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
3	EXDEF	Excessive Deferral When the DTXSTS bit is set in the MTL Operation Mode register and the DC bit is set in the MAC Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000 Mbps mode or

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Bit Field	Name	Description
		when Jumbo packet is enabled). 0: No Excessive Deferral 1: Excessive Deferral *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
2	LCARR	Loss of Carrier When the DTXSTS bit is set in the MTL Operation Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. 0: Carrier present 1: Loss of Carrier *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
1	NCARR	No Carrier When the DTXSTS bit is set in the MTL Operation Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. 0: Carrier present 1: No Carrier *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
0	TJT	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC Configuration register. 0: No Transmit Jabber Timeout 1: Transmit Jabber Timeout occurred *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*

47.6.1.16 ETH PMT Control Status register (ETH_MACPMTCTRLSTS)

Address offset: 0x00C0

Reset value: 0x0000 0000

This register contains control and status bits related to remote wake-up packets and magic packets.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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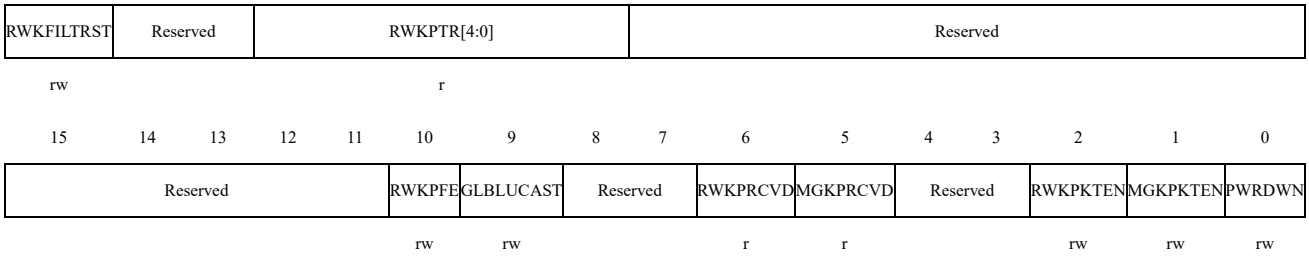

Bit Field	Name	Description
31	RWKFILTRST	Remote Wakeup Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. 0: Remote wakeup packet filter register pointer is not reset 1: Remote wakeup packet filter register pointer is reset
30:29	Reserved	Reserved, the reset value must be maintained.
28:24	RWKPTR[4:0]	Remote Wakeup FIFO Pointer This field gives the current value (0 to 7) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	Reserved	Reserved, the reset value must be maintained.
10	RWKPFE	Remote Wakeup Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. 0: Remote Wake-up Packet Forwarding is disabled 1: Remote Wake-up Packet Forwarding is enabled *Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application.* *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*
9	GLBLUCAST	Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. 0: Global Unicast is disabled 1: Global Unicast is enabled

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Bit Field	Name	Description
8:7	Reserved	Reserved, the reset value must be maintained.
6	RWKPRCVD	Remote wakeup Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. 0: No remote wakeup packet received 1: Remote wakeup packet received *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
5	MGKPRCVD	Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. 0: No magic packet received 1: Magic packet received *Note: This bit has access restrictions. Reading (or writing 1 when the RCWE bit in the MAC CSR software control register is set) clears it. It is automatically set to 1 during internal events.*
4:3	Reserved	Reserved, the reset value must be maintained.
2	RWKPKTEN	Remote Wakeup Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. 0: Remote Wake-up Packet is disabled 1: Remote Wake-up Packet is enabled
1	MGKPKTEN	Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet. 0: Magic Packet is disabled 1: Magic Packet is enabled
0	PWRDWN	Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. 0: Power Down is disabled 1: Power Down is enabled *Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the software cannot clear this bit.*

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47.6.1.17 ETH MAC Remote Wakeup Filter register (ETH_MACRWUPFLT)

Address offset: 0x00C4

Reset value: 0x0000 0000

The Remote Wakeup Filter registers are implemented as 8 indirect access registers (wkuppktfilter_reg#i) and accessed by application through MAC Remote Wakeup Filter register. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight register values in MAC Remote Wakeup Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg7 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC PMT Control Status register.

For a description of the fields in the Remote Wakeup Filter Register, refer to section 47.5.11.2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WKUPFRMFTR[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUPFRMFTR[15:0]															
rw															

Bit Field	Name	Description
31:0	WKUPFRMFTR	Remote Wakeup Filter (RWK Packet Filter) This field contains various controls of RWK packet filter.

47.6.1.18 ETH LPI Control and Status register (ETH_MACLPICTRLSTS)

Address offset: 0x00D0

Reset value: 0x0000 0000

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										LPITCSE	LPIATE	LPITXA	Reserved	PLS	LPIEN
										rw	rw	rw		rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						RLPIST	TLPIST	Reserved				RLPIEX	RLPIEN	TLPIEX	TLPIEN
						r	r					r	r	r	r

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Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	LPITCSE	LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. 0x0: LPI Tx Clock Stop is disabled 0x1: LPI Tx Clock Stop is enabled
20	LPIATE	LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC LPI Entry Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. 0x0: LPI Timer is disabled 0x1: LPI Timer is enabled
19	LPITXA	LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the IP) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL TxQ0 Operation Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. 0x0: LPI Tx Automate is disabled 0x1: LPI Tx Automate is enabled
18	Reserved	Reserved, the reset value must be maintained.
17	PLS	PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down.

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Bit Field	Name	Description
		0x0: link is down 0x1: link is okay (UP)
16	LPIEN	LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. 0x0: LPI state is disabled 0x1: LPI state is enabled
15:10	Reserved	Reserved, the reset value must be maintained.
9	RLPIST	Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. 0x0: Receive LPI state not detected 0x1: Receive LPI state detected
8	TLPIST	Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. 0x0: Transmit LPI state not detected 0x1: Transmit LPI state detected
7:4	Reserved	Reserved, the reset value must be maintained.
3	RLPIEX	Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC CSR software control register is set). 0x0: Receive LPI exit not detected 0x1: Receive LPI exit detected *Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.*
2	RLPIEN	Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC CSR software control register is set). 0x0: Receive LPI entry not detected 0x1: Receive LPI entry detected *Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.*
1	TLPIEX	Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC CSR

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Bit Field	Name	Description
		software control register is set). 0x0: Transmit LPI exit not detected 0x1: Transmit LPI exit detected
0	TLPIEN	Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC CSR software control register is set). 0x0: Transmit LPI entry not detected 0x1: Transmit LPI entry detected

47.6.1.19 ETH LPI Timers Control register (ETH_MACLPITIMCTRL)

Address offset: 0x00D4

Reset value: 0x03E8 0000

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						LST[9:0]									
						rw									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TWT[15:0]															
rw															

Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:16	LST	LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	TWT	LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

47.6.1.20 ETH LPI Entry Timer register (ETH_MACLPIETYTIM)

Address offset: 0x00D8

Reset value: 0x0000 0000

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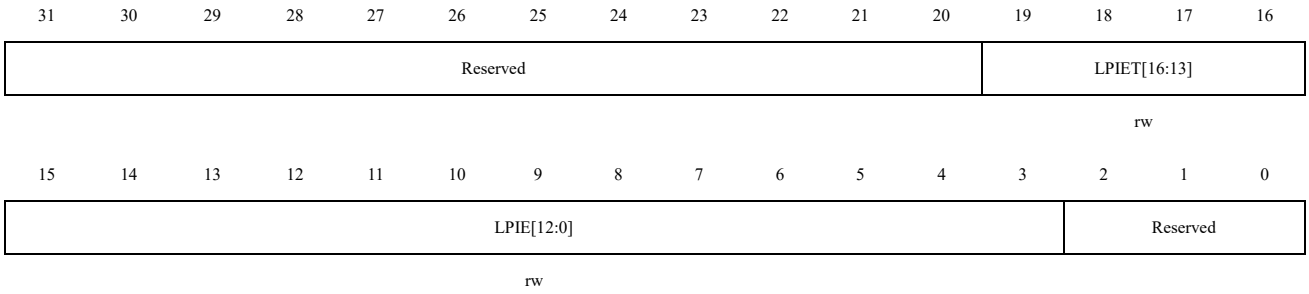
This register controls the Tx LPI entry timer. This counter is enabled only when bit 20 (LPITE) bit of MAC LPI Control Status is set to 1.



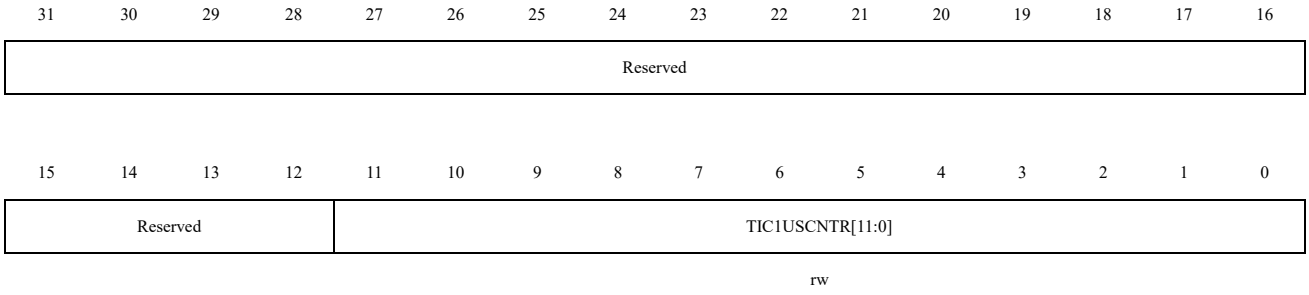
Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19:3	LPIET	LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.21 ETH MAC 1us Tick Counter register (ETH_MAC1USTICCNT)

Address offset: 0x00DC

Reset value: 0x0000 0063

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.



Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	TIC1USCNTR	1US Tick Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is

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Bit Field	Name	Description
		0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

47.6.1.22 ETH MAC Version register (ETH_MACVER)

Address offset: 0x0110

Reset value: 0x0000 1052

The version register identifies the version of the ETH. This register contains two bytes: one that Synopsys uses to identify the IP release number, and the other that you set while configuring the IP.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USERVER[7:0]								SNPSVER[7:0]							
r								r							

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:8	USERVER[7:0]	User-defined Version (configured with coreConsultant)
7:0	SNPSVER[7:0]	Synopsys-defined Version

47.6.1.23 ETH MAC Debug register (ETH_MACDBG)

Address offset: 0x0114

Reset value: 0x0000 0000

The Debug register provides the debug status of various MAC blocks.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TFCSTS[1:0]		TPESTS
													r		r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													RFCFCSTS[1:0]		RPESTS
													r		r

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18:17	TFCSTS	MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module.

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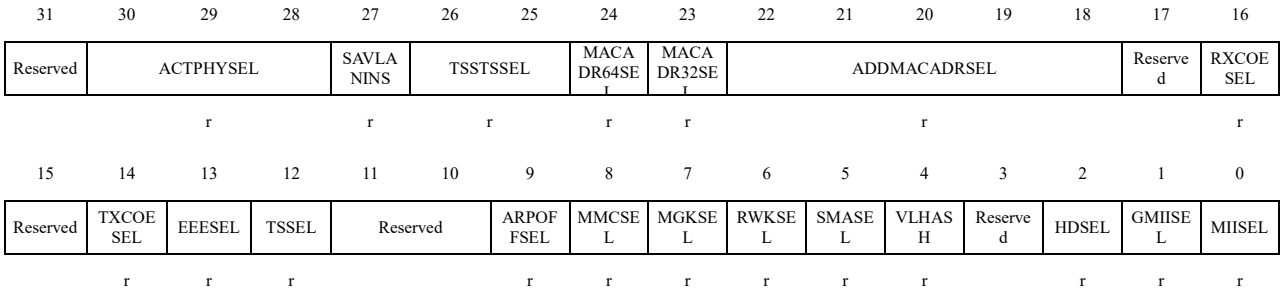
Bit Field	Name	Description
		0x0: Idle state 0x1: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 0x2: Generating and transmitting a Pause control packet (in full-duplex mode) 0x3: Transferring input packet for transmission
16	TPESTS	MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. 0x0: MAC GMII or MII Transmit Protocol Engine Status not detected 0x1: MAC GMII or MII Transmit Protocol Engine Status detected
15:3	Reserved	Reserved, the reset value must be maintained.
2:1	RFCFCSTS	MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	RPESTS	MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. 0x0: MAC GMII or MII Receive Protocol Engine Status not detected 0x1: MAC GMII or MII Receive Protocol Engine Status detected

47.6.1.24 ETH MAC HW Feature register 0 (ETH_MACHWF0)

Address offset: 0x011C

Reset value: 0x0A0D 73F7

This register indicates the presence of first set of the optional features or functions of the Ethernet peripheral. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.



Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	ACTPHYSEL	Active PHY Selected When there are multiple PHY interfaces in the configuration, this field indicates the sampled value of phy_intf_sel_i during reset support. 0x0: GMII or MII

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Bit Field	Name	Description
		0x4: RMII Other values: Reserved
27	SAVLANINS	Source Address or VLAN Insertion Enabled When the "Enable SA and VLAN Insertion on Tx" option is selected, this bit is set to 1. 0: The "Enable SA and VLAN Insertion" option is not selected 1: The "Enable SA and VLAN Insertion" option is selected
26:25	TSSTSSEL	Timestamp System Time Source This field indicates the source of the timestamp system time: 0x0: Internal 0x1: External 0x2: Internal and External
24	MACADR64SEL	MAC Addresses 64-127 Selected When the "Enable Additional MAC Addresses Register 64-127" option is selected, this bit is set to 1. 0: The "Additional MAC Addresses Register 64-127" option is not selected 1: The "Additional MAC Addresses Register 64-127" option is selected
23	MACADR32SEL	MAC Addresses 32-63 Selected When the "Enable Additional MAC Addresses Register 32-63" option is selected, this bit is set to 1. 0: The "Additional MAC Addresses Register 32-63" option is not selected 1: The "Additional MAC Addresses Register 32-63" option is selected
22:18	ADDMACADRSEL	MAC Addresses 1-31 Selected This field indicates the additional MAC addresses. 0x1: Enable Additional MAC Address 1 0x2: Enable Additional MAC Address 2 0x3: Enable Additional MAC Address 3 ... 0x1F: Enable Additional MAC Address 31
17	Reserved	Reserved, the reset value must be maintained.
16	RXCOESEL	Receive Checksum Offload Enabled When the "Enable Receive TCP/IP Checksum Offload" option is selected, this bit is set to 1. 0: The "Receive Checksum Offload" option is not selected 1: The "Receive Checksum Offload" option is selected
15	Reserved	Reserved, the reset value must be maintained.
14	TXCOESEL	Transmit Checksum Offload Enabled When the "Enable Transmit TCP/IP Checksum Offload" option is selected, this bit is set to 1. 0: The "Transmit Checksum Offload" option is not selected 1: The "Transmit Checksum Offload" option is selected
13	EEESEL	Energy Efficient Ethernet Enabled When the "Enable Energy Efficient Ethernet" option is selected, this bit is set to 1.

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Bit Field	Name	Description
		0: The "Enable Energy Efficient Ethernet" option is not selected 1: The "Enable Energy Efficient Ethernet" option is selected
12	TSSEL	IEEE 1588-2008 Timestamp Enabled When the "Enable IEEE 1588 Timestamp" option is selected, this bit is set to 1. 0: The "Enable IEEE 1588 Timestamp" option is not selected 1: The "Enable IEEE 1588 Timestamp" option is selected
11:10	Reserved	Reserved, the reset value must be maintained.
9	ARPOFFSEL	ARP Offload Enabled: When the "Enable IPv4 ARP Offload" option is selected, this bit is set to 1. 0: The "Enable IPv4 ARP Offload" option is not selected 1: The "Enable IPv4 ARP Offload" option is selected
8	MMCSEL	RMON Module Enabled When the "Enable MAC Management Counters (MMC)" option is selected, this bit is set to 1. 0: The "Enable MAC Management Counters (MMC)" option is not selected 1: The "Enable MAC Management Counters (MMC)" option is selected
7	MGKSEL	PMT Magic Packet Enabled When the "Enable Magic Packet Detection" option is selected, this bit is set to 1. 0: The "Enable Magic Packet Detection" option is not selected 1: The "Enable Magic Packet Detection" option is selected
6	RWKSEL	PMT Remote Wake-up Packet Enabled When the "Enable Remote Wake-up Packet Detection" option is selected, this bit is set to 1. 0: The "Enable Remote Wake-up Packet Detection" option is not selected 1: The "Enable Remote Wake-up Packet Detection" option is selected
5	SMASEL	SMA (MDIO) Interface When the "Enable Station Management (MDIO Interface)" option is selected, this bit is set to 1. 0: SMA (MDIO) Interface not selected 1: SMA (MDIO) Interface selected
4	VLHASH	VLAN Hash Filter Selected When the "Enable VLAN Hash Filter" option is selected, this bit is set to 1. 0: VLAN Hash Filter not selected 1: VLAN Hash Filter selected
3	Reserved	Reserved, the reset value must be maintained.
2	HDSEL	Half-duplex Support When the "Half-duplex Mode" option is selected, this bit is set to 1. 0: Half-duplex not supported 1: Half-duplex supported
1	GMIISEL	1000 Mbps Support When the "1000 Mbps Mode" option is selected, this bit is set to 1.

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Bit Field	Name	Description
		0: 1000 Mbps not supported 1: 1000 Mbps supported
0	MIISEL	10/100 Mbps Support When the "10/100 Mbps Mode" option is selected, this bit is set to 1. 0: 10/100 Mbps not supported 1: 10/100 Mbps supported

47.6.1.25 ETH MAC_HW Feature register 1 (ETH_MACHWF1)

Address offset: 0x0120

Reset value: 0x1104 3904

This register indicates the presence of second set of the optional features or functions of the Ethernet peripheral. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	L3L4FNUM				Reserved	HASHTBLSZ		POUOST	Reserved	RAVSEL	AVSEL	DBGMEMA	TSOEN	SPHEN	DCBEN
r					r			r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR64		ADVTHWORD	PTOEN	OSTEN	TXFIFOSIZE					SPRAM	RXFIFOSIZE				
r		r	r	r	r					r	r				

Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:27	L3L4FNUM	Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters: 0000: No L3 or L4 filters 0001: 1 L3 or L4 filter 0010: 2 L3 or L4 filters ... 1000: 8 L3 or L4 filters
26	Reserved	Reserved, the reset value must be maintained.
25:24	HASHTBLSZ	Hash Table Size This field indicates the size of the hash table: 00: No hash table 01: 64 10: 128 11: 256
23	POUOST	One Step for PTP over UDP/IP Feature Enable When the "One Step for PTP over UDP/IP" feature is selected, this bit is set to 1. 0: "One Step for PTP over UDP/IP" feature not selected

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Bit Field	Name	Description
		1: "One Step for PTP over UDP/IP" feature selected
22	Reserved	Reserved, the reset value must be maintained.
21	RAVSEL	Rx Side Only AV Feature Enabled When the "Enable Rx Side Audio/Video Bridging" option is selected, this bit is set to 1. 0: "Rx Side Audio/Video Bridging (AV)" feature not selected 1: "Rx Side Audio/Video Bridging (AV)" feature selected
20	AVSEL	AV Feature Enabled When the "Enable Audio/Video Bridging" option is selected, this bit is set to 1. 0: "Audio/Video Bridging (AV)" feature not selected 1: "Audio/Video Bridging (AV)" feature selected
19	DBGMEMA	DMA Debug Registers Enabled When the "Enable Debug Mode" option is selected, this bit is set to 1. 0: "DMA Debug Registers" option not selected 1: "DMA Debug Registers" option selected
18	TSOEN	TCP Segmentation Offload Enabled When the "Enable TCP Segmentation Offload for TCP/IP packets" option is selected, this bit is set to 1. 0: "TCP Segmentation Offload" feature not selected 1: "TCP Segmentation Offload" feature selected
17	SPHEN	Split Header Feature Enabled When the "Enable Split Header" option is selected, this bit is set to 1. 0: "Split Header" feature not selected 1: "Split Header" feature selected
16	DCBEN	DCB Feature Enabled When the "Enable Data Center Bridging (DCB)" option is selected, this bit is set to 1. 0: "Data Center Bridging" feature not selected 1: "Data Center Bridging" feature selected
15:14	ADDR64	Address Width This field indicates the configured address width: 0x0: 32 0x1: 40 0x2: 48 0x3: Reserved
13	ADVTHWORD	IEEE 1588 High Word Register Enabled When the "Add IEEE 1588 High Word Register" option is selected, this bit is set to 1. 0: "IEEE 1588 High Word Register" option not selected 1: "IEEE 1588 High Word Register" option selected
12	PTOEN	PTP Offload Enabled When the "Enable PTP Timestamp Offload" feature is selected, this bit is set to 1. 0: "PTP Offload" feature not selected 1: "PTP Offload" feature selected

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Bit Field	Name	Description
11	OSTEN	One-Step Timestamping Enabled When the "Enable One-Step Timestamping" feature is selected, this bit is set to 1. 0: "One-Step Timestamping" feature not selected 1: "One-Step Timestamping" feature selected
10:6	TXFIFOSIZE	MTL Transmit FIFO Size This field contains the configuration value of the MTL Tx FIFO (in bytes), represented as the logarithm to the base 2 minus 7, i.e., Log2(TXFIFO_SIZE) - 7: 0x0: 128 bytes 0x1: 256 bytes 0x2: 512 bytes 0x3: 1024 bytes 0x4: 2048 bytes 0x5: 4096 bytes 0x6: 8192 bytes 0x7: 16384 bytes 0x8: 32KB 0x9: 64KB 0xA: 128KB 0xB: Reserved
5	SPRAM	Single Port RAM Enabled When the "Use Single Port RAM" feature is selected, this bit is set to 1. 0: "Single Port RAM" feature not selected 1: "Single Port RAM" feature selected
4:0	RXFIFOSIZE	MTL Receive FIFO Size This field contains the configuration value of the MTL Rx FIFO (in bytes), represented as the logarithm to the base 2 minus 7, i.e., Log2(RXFIFO_SIZE) - 7: 0x0: 128 bytes 0x1: 256 bytes 0x2: 512 bytes 0x3: 1024 bytes 0x4: 2048 bytes 0x5: 4096 bytes 0x6: 8192 bytes 0x7: 16384 bytes 0x8: 32KB 0x9: 64KB 0xA: 128KB 0xB: 256KB 0xC: Reserved

47.6.1.26 ETH MAC HW Feature register 2 (ETH_MACHWF2)

Address offset: 0x0124

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Reset value: 0x4141 0000

This register indicates the presence of third set of the optional features or functions of the Ethernet peripheral. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	AUXSNAPNUM			Reserved	PPSOUTNUM			TDCSZ		TXCHCNT				RDCSZ	
	r				r			r		r				r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXCHCNT				Reserved		TXQCNT				Reserved		RXQCNT			
r						r						r			

Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:28	AUXSNAPNUM	Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs: 0x0: No auxiliary inputs 0x1: 1 auxiliary input 0x2: 2 auxiliary inputs 0x3: 3 auxiliary inputs 0x4: 4 auxiliary inputs 0x5: Reserved
27	Reserved	Reserved, the reset value must be maintained.
26:24	PPSOUTNUM	Number of PPS Outputs This field indicates the number of PPS outputs: 0x0: No PPS outputs 0x1: 1 PPS output 0x2: 2 PPS outputs 0x3: 3 PPS outputs 0x4: 4 PPS outputs 0x5: Reserved
23:22	TDCSZ	Tx DMA Descriptor Cache Size in terms of 16 bytes descriptors 0x0: Cache not configured 0x1: 4 0x2: 8 0x3: 16
21:18	TXCHCNT	Number of DMA Transmit Channels This field indicates the number of DMA transmit channels: 0x0: 1 DMA transmit channel 0x1: 2 DMA transmit channels ... 0x7: 8 DMA transmit channels

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Bit Field	Name	Description
17:16	RDCSZ	Rx DMA Descriptor Cache Size in terms of 16 bytes descriptors 0x0: Cache not configured 0x1: 4 0x2: 8 0x3: 16
15:12	RXCHCNT	Number of DMA Receive Channels This field indicates the number of DMA receive channels: 0x0: 1 DMA receive channel 0x1: 2 DMA receive channels ... 0x7: 8 DMA receive channels
11:10	Reserved	Reserved, the reset value must be maintained.
9:6	TXQCNT	Number of MTL Transmit Queues This field indicates the number of MTL transmit queues: 0x0: 1 MTL transmit queue 0x1: 2 MTL transmit queues ... 0x7: 8 MTL transmit queues
5:4	Reserved	Reserved, the reset value must be maintained.
3:0	RXQCNT	Number of MTL Receive Queues This field indicates the number of MTL receive queues: 0x0: 1 MTL receive queue 0x1: 2 MTL receive queues ... 0x7: 8 MTL receive queues

47.6.1.27 ETH MAC HW Feature register 3 (ETH_MACHWF3)

Address offset: 0x0128

Reset value: 0x0000 0020

This register indicates the presence of fourth set of the optional features or functions of the Ethernet peripheral. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		ASP		TBSSEL	FPESEL	Reserved				ESTWID		ESTDEP			ESTSEL
		r		r	r					r		r			r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	FRPES		FRPBS		FRPSEL	PDUPSEL	Reserved			DVLAN	CBTISEL	Reserved	NRVF		
	r		r		r	r				r	r		r		

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Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:28	ASP	Automotive Safety Package The following are the codes for different safety features: 0x0: No safety features selected 0x1: Only "ECC protection for external memory" feature selected 0x2: All automotive safety features selected, but "Enable external interface parity check port" feature not selected 0x3: All automotive safety features selected, including "Enable external interface parity check port" feature
27	TBSSEL	Time Based Scheduling Enable When the "Enable Time Based Scheduling" feature is selected, this bit is set to 1. 0: "Time Based Scheduling" feature not selected 1: "Time Based Scheduling" feature selected
26	FPESEL	Frame Preemption Enable When the "Enable Frame Preemption" feature is selected, this bit is set to 1. 0: "Frame Preemption" feature not selected 1: "Frame Preemption" feature selected
25:22	Reserved	Reserved, the reset value must be maintained.
21:20	ESTWID	Width of the Time Interval field in the Gate Control List This field indicates the width of the configured time interval field. 0x0: Width not configured 0x1: 4 0x2: 8 0x3: 16
19:17	ESTDEP	Depth of the Gate Control List This field indicates the depth of the gate control list, represented as Log2(DWC_EQOS_EST_DEP) - 5. 0x0: Depth not configured 0x1: 64 0x2: 128 0x3: 256 0x4: 512 0x5: 1024 0x6: Reserved
16	ESTSEL	Enhancements to Scheduled Traffic Enable When the "Enable Enhancements to Scheduled Traffic" feature is selected, this bit is set to 1. 0: "Enhancements to Scheduled Traffic" feature not selected 1: "Enhancements to Scheduled Traffic" feature selected
15	Reserved	Reserved, the reset value must be maintained.
14:13	FRPES	Flexible Receive Parser Table Entries size This field indicates the maximum number of parser entries supported by the flexible

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Bit Field	Name	Description
		receive parser. 0x0: 64 0x1: 128 0x2: 256 0x3: Reserved
12:11	FRPBS	Flexible Receive Parser Buffer size This field indicates the maximum number of bytes of packet data that can be parsed by the flexible receive parser. 0x0: 64 bytes 0x1: 128 bytes 0x2: 256 bytes 0x3: Reserved
10	FRPSEL	Flexible Receive Parser Selected When the "Enable Flexible Programmable Receive Parser" option is selected, this bit is set to 1. 0: "Flexible Receive Parser" feature not selected 1: "Flexible Receive Parser" feature selected
9	PDUPSEL	Broadcast/Multicast Packet Duplication When the "Broadcast/Multicast Packet Duplication" feature is selected, this bit is set to 1. 0: "Broadcast/Multicast Packet Duplication" feature not selected 1: "Broadcast/Multicast Packet Duplication" feature selected
8:6	Reserved	Reserved, the reset value must be maintained.
5	DVLAN	Double VLAN Tag Processing Selected When the "Enable Double VLAN Tag Processing" feature is selected, this bit is set to 1. 0: "Double VLAN Tag Processing" option not selected 1: "Double VLAN Tag Processing" option selected
4	CBTISEL	Queue/Channel based VLAN tag insertion on Tx Enabled When the "Enable Queue/Channel based VLAN tag insertion on Tx" feature is selected, this bit is set to 1. 0: "Queue/Channel based VLAN tag insertion on Tx" feature not selected 1: "Queue/Channel based VLAN tag insertion on Tx" feature selected
3	Reserved	Reserved, the reset value must be maintained.
2:0	NRVF	Queue/Channel based VLAN tag insertion on Tx Enabled When the "Enable Queue/Channel based VLAN tag insertion on Tx" feature is selected, this bit is set to 1. 0: "Queue/Channel based VLAN tag insertion on Tx" feature not selected 1: "Queue/Channel based VLAN tag insertion on Tx" feature selected

47.6.1.28 ETH MAC MDIO Address register (ETH_MACMDIOADDR)

Address offset: 0x0200

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Reset value: 0x0000 0000

The MDIO Address register controls the management cycles to external PHY through a management interface.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				PSE	BTB	PA					RDA				
				rw	rw			rw					rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	NTC			CR				Reserved			SKAP	GOC1	GOC0	C45E	GB
	rw			rw							rw	rw	rw	rw	rw

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	PSE	Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. 0x0: Preamble Suppression disabled 0x1: Preamble Suppression enabled
26	BTB	Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. 0x0: Back to Back transactions disabled 0x1: Back to Back transactions enabled
25:21	PA	Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	RDA	Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	Reserved	Reserved, the reset value must be maintained.
14:12	NTC	Number of Training Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles

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Bit Field	Name	Description
		on the MDC line after the end of MDIO frame transfer.
11:8	CR	CSR Clock Range The CSR Clock Range determines the frequency of the MDC clock based on the CSR clock frequency used in the design: 0000: CSR clock = 60~100MHz; MDC clock = CSR clock/42 0001: CSR clock = 100~150MHz; MDC clock = CSR clock/62 0010: CSR clock = 20~35MHz; MDC clock = CSR clock/16 0011: CSR clock = 35~60MHz; MDC clock = CSR clock/26 0100: CSR clock = 150~250MHz; MDC clock = CSR clock/102 0101: CSR clock = 250~300MHz; MDC clock = CSR clock/124 0110: CSR clock = 300~500MHz; MDC clock = CSR clock/204 0111: CSR clock = 500~800MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is beyond the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 1000: CSR clock/4 1001: CSR clock/6 1010: CSR clock/8 1011: CSR clock/10 1100: CSR clock/12 1101: CSR clock/14 1110: CSR clock/16 1111: CSR clock/18
7:5	Reserved	Reserved, the reset value must be maintained.
4	SKAP	Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0x0: Skip Address Packet is disabled 0x1: Skip Address Packet is enabled
3	GOC1	GMII Operation Command 1 This bit is higher bit of the operation command to the PHY, GOC1 and GOCO is encoded as follows: 00: Reserved 01: Write operation 10: Post-read operation on an incremental address for a PHY compliant with Clause 45 11: Read operation When enabling a PHY compliant with Clause 22, only read and

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Bit Field	Name	Description
		write commands are valid.
2	GOC0	GMII Operation Command 0 This is the lower bit of the operation command to the PHY. When in SMA mode (MDIO master) this bit along with GOC1 determines the operation to be performed to the PHY. 0x0: GMII Operation Command 0 is disabled 0x1: GMII Operation Command 0 is enabled
1	C45E	Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0x0: Clause 45 PHY is disabled 0x1: Clause 45 PHY is enabled
0	GB	GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC MDIO Address and MAC MDIO Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC MDIO Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC MDIO Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC MDIO Data register. *Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. There are access restrictions on this bit: writing 1 is effective and it is automatically cleared, writing 0 has no effect.*

47.6.1.29 ETH MAC MDIO Data register (ETH_MACMDIODATA)

Address offset: 0x0204

Reset value: 0x0000 0000

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC MDIO Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RA															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GD															
rw															

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Bit Field	Name	Description
31:16	RA	Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	GD	GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

47.6.1.30 ETH MAC ARP Address register (ETH_MACARPADDR)

Address offset: 0x0210

Reset value: 0x0000 0000

The ARP Address register contains the IPv4 Destination Address of the MAC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ARPPA[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARPPA[15:0]															
rw															

Bit Field	Name	Description
31:0	ARPPA	ARP Protocol Address This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

47.6.1.31 ETH CSR Software Control register (ETH_MACCSRSWCTRL)

Address offset: 0x0230

Reset value: 0x0000 0000

This register contains software programmable controls for changing the CSR access response and status bits clearing.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SEEN	Reserved							RCWE
							rw								rw

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Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	SEEN	Slave Error Response Enable When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space. 0x0: Slave Error Response is disabled 0x1: Slave Error Response is enabled
7:1	Reserved	Reserved, the reset value must be maintained.
0	RCWE	Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. 0x0: Register Clear on Write 1 is disabled 0x1: Register Clear on Write 1 is enabled

47.6.1.32 ETH MAC Presentation Time Nanoseconds register (ETH_MACPTNS)

Address offset: 0x0240

Reset value: 0x0000 0000

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MPTN[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPTN[15:0]															
rw															

Bit Field	Name	Description
31:0	MPTN	MAC 1722 Presentation Time in ns These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns.

47.6.1.33 ETH MAC Presentation Time Update register (ETH_MACPTUPDT)

Address offset: 0x0244

Reset value: 0x0000 0000

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC Timestamp Control register).

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MPTU[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPTU[15:0]															
rw															

Bit Field	Name	Description
31:0	MPTU	MAC 1722 Presentation Time Update This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC Timestamp Control register). When ADDSUB field of MAC System Time Nanoseconds Update is set, this value is directly used for subtraction.

47.6.1.34 ETH MAC Address0 High register (ETH_MACADDR0H)

Address offset: 0x0300

Reset value: 0x8000 FFFF

The MAC Address 0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MAC Address 0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address 0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AE	Reserved														
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRHI															
rw															

Bit Field	Name	Description
31	AE	Address Enable This bit is always set to 1.

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Bit Field	Name	Description
30:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI	MAC Address 0 [47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

47.6.1.35 ETH MAC Address0 Low register (ETH_MACADDR0L)

Address offset: 0x0304

Reset value: 0xFFFF FFFF

The MAC Address 0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Bit Field	Name	Description
31:0	ADDRLO	MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

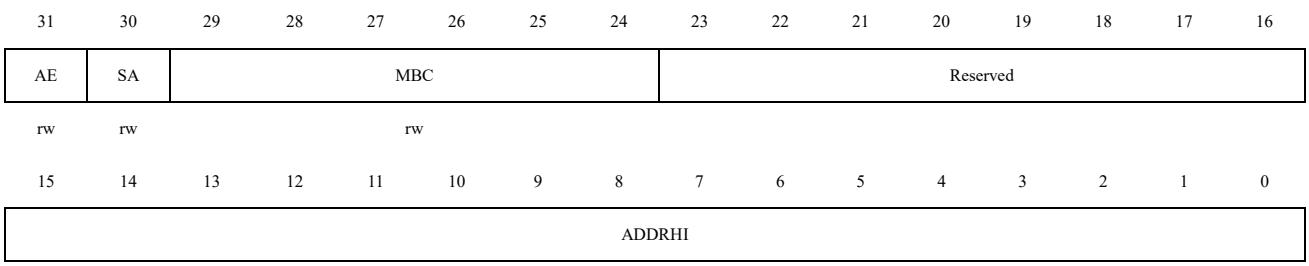
47.6.1.36 ETH MAC Address1 High register (ETH_MACADDR1H)

Address offset: 0x0308

Reset value: 0x0000 FFFF

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits [31:24] (in little-endian mode) or Bits [7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.



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rw

Bit Field	Name	Description
31	AE	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0: Address is ignored 1: Address is enabled
30	SA	Source Address When this bit is set, the MAC Address 1 [47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address 1 [47:0] is used to compare with the DA fields of the received packet. 0: Compare with destination address 1: Compare with source address
29:24	MBC	Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: bit29: bits [15:8] of MAC Address 1 High Register bit28: bits [7:0] of MAC Address 1 High Register bit27: bits [31:24] of MAC Address 1 Low Register ... bit24: bits [7:0] of MAC Address 1 Low Register You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI	MAC Address 1 [47:32] This field contains the upper 16 bits [47:32] of the second 6-byte MAC address.

47.6.1.37 ETH MAC Address1 Low register (ETH_MACADDR1L)

Address offset: 0x030C

Reset value: 0xFFFF FFFF

The MAC Address 1 Low register holds the lower 32 bits of the 6-byte second MAC address of the station.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDRLO[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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ADDRLO[15:0]

rw

Bit Field	Name	Description
31:0	ADDRLO	MAC Address 1 [31:0] This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

47.6.1.38 ETH MAC Address2 High register (ETH_MACADDR2H)

Address offset: 0x0310

Reset value: 0x0000 FFFF

The MAC Address 2 High register holds the upper 16 bits of the third 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits [31:24] (in little-endian mode) or Bits [7:0] (in big-endian mode) of the MAC Address 2 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AE	SA	MBC						Reserved							
rw	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRHI															

rw

Bit Field	Name	Description
31	AE	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0: Address is ignored 1: Address is enabled
30	SA	Source Address When this bit is set, the MAC Address 2 [47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address 2 [47:0] is used to compare with the DA fields of the received packet. 0: Compare with destination address 1: Compare with source address
29:24	MBC	Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When

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Bit Field	Name	Description
		set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address 2 registers. Each bit controls the masking of the bytes as follows: bit29: bits [15:8] of MAC Address 2 High Register bit28: bits [7:0] of MAC Address 2 High Register bit27: bits [31:24] of MAC Address 2 Low Register ... bit24: bits [7:0] of MAC Address 2 Low Register You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI	MAC Address 2 [47:32] This field contains the upper 16 bits [47:32] of the third 6-byte MAC address.

47.6.1.39 ETH MAC Address2 Low register (ETH_MACADDR2L)

Address offset: 0x0314

Reset value: 0xFFFF FFFF

The MAC Address 2 Low register holds the lower 32 bits of the 6-byte third MAC address of the station.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDRLO[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRLO[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDRLO	MAC Address 2 [31:0] This field contains the lower 32 bits of third 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

47.6.1.40 ETH MAC Address3 High register (ETH_MACADDR3H)

Address offset: 0x0318

Reset value: 0x0000 FFFF

The MAC Address 3 High register holds the upper 16 bits of the fourth 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits [31:24] (in little-endian mode) or Bits [7:0] (in big-endian mode) of the MAC Address 3 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AE	SA	MBC						Reserved							
rw	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRHI															
rw															

Bit Field	Name	Description
31	AE	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. 0: Address is ignored 1: Address is enabled
30	SA	Source Address When this bit is set, the MAC Address 3 [47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address 3 [47:0] is used to compare with the DA fields of the received packet. 0: Compare with destination address 1: Compare with source address
29:24	MBC	Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address 3 registers. Each bit controls the masking of the bytes as follows: bit29: bits [15:8] of MAC Address 3 High Register bit28: bits [7:0] of MAC Address 3 High Register bit27: bits [31:24] of MAC Address 3 Low Register ... bit24: bits [7:0] of MAC Address 3 Low Register You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI	MAC Address 3 [47:32] This field contains the upper 16 bits [47:32] of the fourth 6-byte MAC address.

47.6.1.41 ETH MAC Address3 Low register (ETH_MACADDR3L)

Address offset: 0x031C

Reset value: 0xFFFF FFFF

The MAC Address 3 Low register holds the lower 32 bits of the 6-byte fourth MAC address of the station.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDRLO[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRLO[15:0]															
rw															

Bit Field	Name	Description
31:0	ADDRLO	MAC Address 3 [31:0] This field contains the lower 32 bits of fourth 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

47.6.1.42 ETH MMC Control register (ETH_MMCCTRL)

Address offset: 0x0700

Reset value: 0x0000 0000

This register establishes the operating mode of MMC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							UCDBC	Reserved		CNTPRSTLVL	CNTPRST	CNTFREEZ	RSTONRD	CNTSTOPRO	CNTRST
							rw			rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	UCDBC	Update MMC Counters for Dropped Broadcast Packets When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC Packet Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. 0: Update MMC Counters for Dropped Broadcast Packets is disabled 1: Update MMC Counters for Dropped Broadcast Packets is enabled *Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set.*
7:6	Reserved	Reserved, the reset value must be maintained.
5	CNTPRSTLVL	Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to

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Bit Field	Name	Description
		almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. 0x0: Full-Half Preset is disabled 0x1: Full-Half Preset is enabled
4	CNTPRST	Counter Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. 0x0: Counters Preset is disabled 0x1: Counters Preset is enabled
3	CNTFREEZ	MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. 0x0: MMC Counter Freeze is disabled 0x1: MMC Counter Freeze is enabled
2	RSTONRD	Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits [7:0]) is read. 0x0: Reset on Read is disabled 0x1: Reset on Read is enabled
1	CNTSTOPRO	Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0x0: Counter Stop Rollover is disabled 0x1: Counter Stop Rollover is enabled
0	CNTRST	Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. 0x0: Counters are not reset 0x1: All counters are reset

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47.6.1.43 ETH MMC Rx Interrupt register (ETH_MMCRXINT)

Address offset: 0x0704

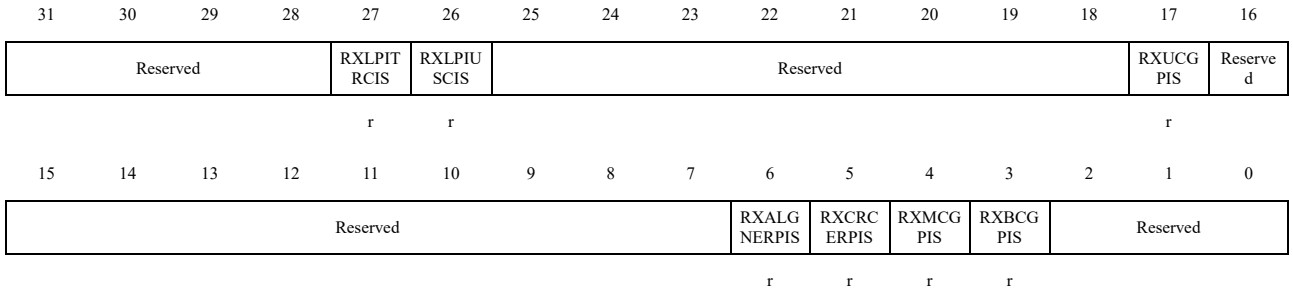
Reset value: 0x0000 0000

This register maintains the interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur:

- Receive statistic counters reach half of their maximum values (0x8000_0000).
- Receive statistic counters cross their maximum values (0xFFFF_FFFF).

When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits [7:0]) of the respective counter must be read to clear the interrupt bit.



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	RXLPITRCIS	MMC Receive LPI transition counter interrupt status This bit is set when the Rx LPI Transition Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive LPI transition Counter Interrupt Status not detected 0x1: MMC Receive LPI transition Counter Interrupt Status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
26	RXLPIUSCIS	MMC Receive LPI microsecond counter interrupt status This bit is set when the Rx LPI Microsecond Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive LPI microsecond Counter Interrupt Status not detected 0x1: MMC Receive LPI microsecond Counter Interrupt Status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
25:18	Reserved	Reserved, the reset value must be maintained.
17	RXUCGPIS	Receive Unicast Good Packet Counter Interrupt Status This bit is set when the Rx Unicast Good Packet Counter reaches half of the maximum

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Bit Field	Name	Description
		value or the maximum value. 0: MMC receive unicast good packet counter interrupt status not detected 1: MMC receive unicast good packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
16:7	Reserved	Reserved, the reset value must be maintained.
6	RXALGNERPIS	MMC Receive Alignment Error Packet Counter Interrupt Status This bit is set when the Rx Receive Alignment Error Counter reaches half of the maximum value or the maximum value. 0: MMC receive alignment error packet counter interrupt status not detected 1: MMC receive alignment error packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
5	RXCRCERPIS	MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the Rx CRC Error Counter reaches half of the maximum value or the maximum value. 0: MMC receive CRC error packet counter interrupt status not detected 1: MMC receive CRC error packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
4	RXMCGPIS	Receive Multicast Good Packet Counter Interrupt Status This bit is set when the Rx Multicast Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive multicast good packet counter interrupt status not detected 1: MMC receive multicast good packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
3	RXBCGPIS	Receive Broadcast Good Packet Counter Interrupt Status This bit is set when the Rx Broadcast Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive broadcast good packet counter interrupt status not detected 1: MMC receive broadcast good packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
2:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.44 ETH MMC Tx Interrupt register (ETH_MMCTXINT)

Address offset: 0x0708

Reset value: 0x0000 0000

This register maintains the interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half

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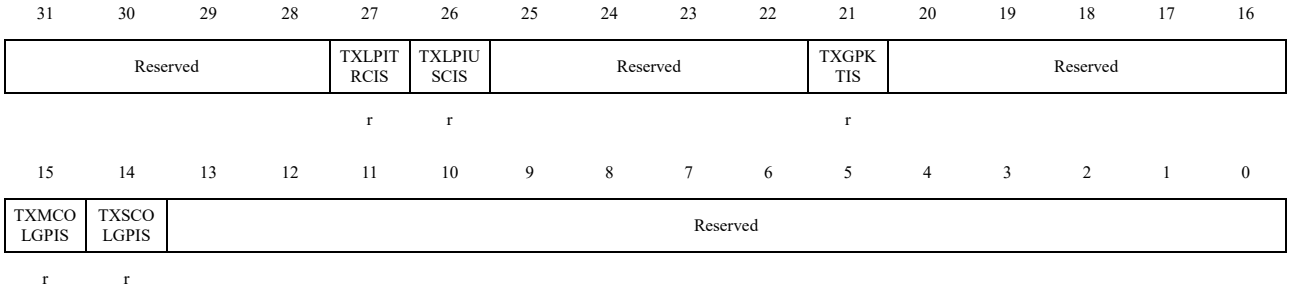
their maximum values (0x8000_0000), and when they cross their maximum values (0xFFFF_FFFF).

When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read.

The least significant byte lane (Bits [7:0]) of the respective counter must be read to clear the interrupt bit.



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	TXLPITRCIS	MMC Transmit LPI transition counter interrupt status This bit is set when the Tx LPI Transition Counter reaches half of the maximum value or the maximum value. 0x0: MMC Transmit LPI transition Counter Interrupt Status not detected 0x1: MMC Transmit LPI transition Counter Interrupt Status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
26	TXLPIUSCIS	MMC Transmit LPI microsecond counter interrupt status This bit is set when the Tx LPI Microsecond Counter reaches half of the maximum value or the maximum value. 0x0: MMC Transmit LPI microsecond Counter Interrupt Status not detected 0x1: MMC Transmit LPI microsecond Counter Interrupt Status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
25:22	Reserved	Reserved, the reset value must be maintained.
21	TXGPKTIS	MMC Transmit Good Packet Counter Interrupt Status This bit is set when the Tx Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC transmit good packet counter interrupt status not detected 1: MMC transmit good packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
20:16	Reserved	Reserved, the reset value must be maintained.
15	TXMCOLGPIS	MMC Transmit Multiple Collision Good Packet Counter Interrupt Status This bit is set when the Tx Multiple Collision Good Packet Counter reaches half of the

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Bit Field	Name	Description
		maximum value or the maximum value. 0: MMC transmit multiple collision good packet counter interrupt status not detected 1: MMC transmit multiple collision good packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
14	TXSCOLGPIS	MMC Transmit Single Collision Good Packet Counter Interrupt Status This bit is set when the Tx Single Collision Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC transmit single collision good packet counter interrupt status not detected 1: MMC transmit single collision good packet counter interrupt status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
13:0	Reserved	Reserved, the reset value must be maintained.

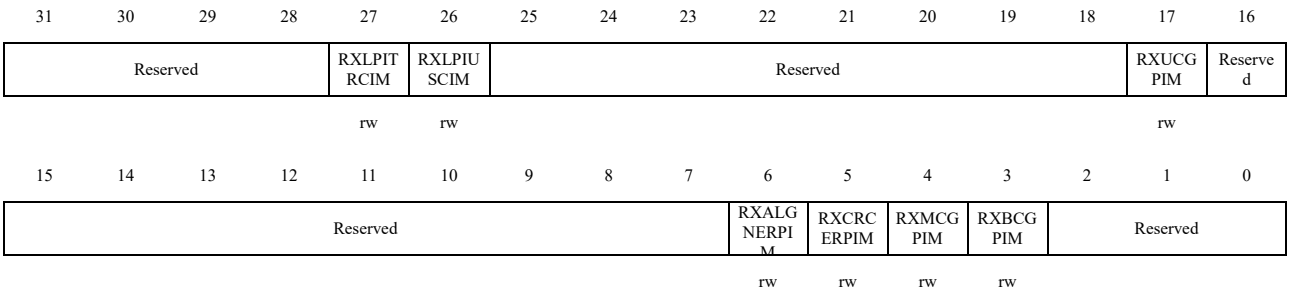
47.6.1.45 ETH MMC Rx Interrupt Mask register (ETH_MMCRXINTMSK)

Address offset: 0x070C

Reset value: 0x0000 0000

This register maintains the masks for interrupts generated from all Receive statistics counters.

The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values.



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	RXLPITRCIM	MMC Receive LPI transition counter interrupt Mask Setting this bit masks the interrupt when the Rx LPI Transition Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive LPI transition counter interrupt Mask is disabled 0x1: MMC Receive LPI transition counter interrupt Mask is enabled
26	RXLPIUSCIM	MMC Receive LPI microsecond counter interrupt Mask Setting this bit masks the interrupt when the Rx LPI Microsecond Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive LPI microsecond counter interrupt Mask is disabled

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Bit Field	Name	Description
		0x1: MMC Receive LPI microsecond counter interrupt Mask is enabled
25:18	Reserved	Reserved, the reset value must be maintained.
17	RXUCGPIM	Receive Unicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx Unicast Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive unicast good packet counter interrupt Mask is disabled 1: MMC receive unicast good packet counter interrupt Mask is enabled
16:7	Reserved	Reserved, the reset value must be maintained.
6	RXALGNERPIM	MMC Receive Alignment Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx Alignment Error Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive alignment error packet counter interrupt Mask is disabled 1: MMC receive alignment error packet counter interrupt Mask is enabled
5	RXCRCERPIM	MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx CRC Error Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive CRC error packet counter interrupt Mask is disabled 1: MMC receive CRC error packet counter interrupt Mask is enabled
4	RXMCGPIM	Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx Multicast Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive multicast good packet counter interrupt Mask is disabled 1: MMC receive multicast good packet counter interrupt Mask is enabled
3	RXBCGPIM	Receive Broadcast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx Broadcast Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC receive broadcast good packet counter interrupt Mask is disabled 1: MMC receive broadcast good packet counter interrupt Mask is enabled
2:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.46 ETH MMC Tx Interrupt Mask register (ETH_MMCTXINTMSK)

Address offset: 0x0710

Reset value: 0x0000 0000

This register maintains the masks for interrupts generated from all Transmit statistics counters.

The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				TXLPITRCIM	TXLPIUSCIM	Reserved				TXGPKTIM	Reserved				
				rw	rw					rw					

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXMCOLGPIM	TXSCOLGPIM	Reserved													
rw	rw														

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	TXLPITRCIM	MMC Transmit LPI transition counter interrupt Mask Setting this bit masks the interrupt when the Tx LPI Transition Counter reaches half of the maximum value or the maximum value. 0x0: MMC Transmit LPI transition counter interrupt Mask is disabled 0x1: MMC Transmit LPI transition counter interrupt Mask is enabled
26	TXLPIUSCIM	MMC Transmit LPI microsecond counter interrupt Mask Setting this bit masks the interrupt when the Tx LPI Microsecond Counter reaches half of the maximum value or the maximum value. 0x0: MMC Transmit LPI microsecond counter interrupt Mask is disabled 0x1: MMC Transmit LPI microsecond counter interrupt Mask is enabled
25:22	Reserved	Reserved, the reset value must be maintained.
21	TXGPKTIM	MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Tx Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC transmit good packet counter interrupt Mask is disabled 1: MMC transmit good packet counter interrupt Mask is enabled
20:16	Reserved	Reserved, the reset value must be maintained.
15	TXMCOLGPIM	MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Tx Multiple Collision Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC transmit multiple collision good packet counter interrupt Mask is disabled 1: MMC transmit multiple collision good packet counter interrupt Mask is enabled
14	TXSCOLGPIM	MMC Transmit Single Collision Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Tx Single Collision Good Packet Counter reaches half of the maximum value or the maximum value. 0: MMC transmit single collision good packet counter interrupt Mask is disabled 1: MMC transmit single collision good packet counter interrupt Mask is enabled
13:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.47 ETH Tx Single Collision Good Packets register (ETH_MMCTXSCGP)

Address offset: 0x074C

Reset value: 0x0000 0000

This register provides the number of successfully transmitted packets by the Ethernet peripheral after a single collision occurs in half-duplex mode.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXSNGLCOLG[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXSNGLCOLG[15:0]															
r															

Bit Field	Name	Description
31:0	TXSNGLCOLG	Tx Single Collision Good Packets This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

47.6.1.48 ETH Tx Multiple Collision Good Packets register (ETH_MMCTXMCGP)

Address offset: 0x0750

Reset value: 0x0000 0000

This register provides the number of successfully transmitted packets by the Ethernet peripheral after multiple collisions occur in half-duplex mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXMULTCOLG[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXMULTCOLG[15:0]															
r															

Bit Field	Name	Description
31:0	TXMULTCOLG	Tx Multiple Collision Good Packets This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

47.6.1.49 ETH Tx Packet Count Good register (ETH_MMCTXPCG)

Address offset: 0x0768

Reset value: 0x0000 0000

This register provides the number of good packets transmitted by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXPKTG[31:16]															

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r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXPKTG[15:0]															

r

Bit Field	Name	Description
31:0	TXPKTG	Tx Packet Count Good This field indicates the number of good packets transmitted.

47.6.1.50 ETH Rx Broadcast Packets Good register (ETH_MMCRXBPG)

Address offset: 0x078C

Reset value: 0x0000 0000

This register provides the number of good broadcast packets received by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXBCASTG[31:16]															

r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBCASTG[15:0]															

r

Bit Field	Name	Description
31:0	RXBCASTG	Rx Broadcast Packets Good This field indicates the number of good broadcast packets received.

47.6.1.51 ETH Rx Multicast Packets Good register (ETH_MMCRXMPG)

Address offset: 0x0790

Reset value: 0x0000 0000

This register provides the number of good multicast packets received by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXMCASTG[31:16]															

r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXMCASTG[15:0]															

r

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Bit Field	Name	Description
31:0	RXMCASTG	Rx Multicast Packets Good This field indicates the number of good multicast packets received.

47.6.1.52 ETH Rx CRC Error Packets register (ETH_MMCRXCRCEP)

Address offset: 0x0794

Reset value: 0x0000 0000

This register provides the number of packets with CRC errors received by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXCRCERR[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXCRCERR[15:0]															
r															

Bit Field	Name	Description
31:0	RXCRCERR	Rx CRC Error Packets This field indicates the number of packets received with CRC errors.

47.6.1.53 ETH Rx Alignment Error Packets register (ETH_MMCRXAEP)

Address offset: 0x0798

Reset value: 0x0000 0000

This register provides the number of packets with alignment (dribble) errors received by the Ethernet peripheral. This counter register is only valid in 10/100M mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXALGNERR[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXALGNERR[15:0]															
r															

Bit Field	Name	Description
31:0	RXALGNERR	Rx Alignment Error Packets This field indicates the number of packets received with alignment (dribble) errors.

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47.6.1.54 ETH Rx Unicast Packets Good register (ETH_MMCRXUPG)

Address offset: 0x07C4

Reset value: 0x0000 0000

This register provides the number of good unicast packets received by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXUCASTG[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXUCASTG[15:0]															
r															

Bit Field	Name	Description
31:0	RXUCASTG	Rx Unicast Packets Good This field indicates the number of good unicast packets received.

47.6.1.55 ETH Tx LPI Microseconds Counter register (ETH_MMCTXLPIUS)

Address offset: 0x07EC

Reset value: 0x0000 0000

This register provides the number of microseconds Tx LPI is asserted by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXLPIUSC[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXLPIUSC[15:0]															
r															

Bit Field	Name	Description
31:0	TXLPIUSC	Tx LPI Microseconds Counter This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

47.6.1.56 ETH Tx LPI Transition Counter register (ETH_MMCTXLPITRAN)

Address offset: 0x07F0

Reset value: 0x0000 0000

This register provides the number of times Ethernet has entered Tx LPI.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXLPITRC[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXLPITRC[15:0]															
r															

Bit Field	Name	Description
31:0	TXLPITRC	Tx LPI Transition counter This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments.

47.6.1.57 ETH Rx LPI Microseconds Counter register (ETH_MMCRXLPIUS)

Address offset: 0x07F4

Reset value: 0x0000 0000

This register provides the number of microseconds Rx LPI is sampled by the Ethernet peripheral.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXLPIUSC[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXLPIUSC[15:0]															
r															

Bit Field	Name	Description
31:0	RXLPIUSC	Rx LPI Microseconds Counter This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

47.6.1.58 ETH Rx LPI Transition Counter register (ETH_MMCRXLPITRAN)

Address offset: 0x07F8

Reset value: 0x0000 0000

This register provides the number of times Ethernet has entered Rx LPI.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXLPITRC[31:16]															

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r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXLPITRC[15:0]															
r															

Bit Field	Name	Description
31:0	RXLPITRC	Rx LPI Transition counter This field indicates the number of times Rx LPI Entry has occurred.

47.6.1.59 ETH MMC IPC Rx Interrupt Mask register (ETH_MMCIPCRXINTMSK)

Address offset: 0x0800

Reset value: 0x0000 0000

This register maintains the mask for the interrupt generated from the receive IPC statistic counters.

The MMC Receive Checksum Offload Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Offload) statistic counters reach half their maximum value, and when they reach their maximum values.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		RXICMPERPIM	RXICMPGPIM	RXTCPERPIM	RXTCPGPIM	RXUDPERPIM	RXUDPGPIM	Reserved		RXIPV6GPIM	Reserved				RXIPV4GPIM
		rw	rw	rw	rw	rw	rw			rw					rw

Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	RXICMPERPIM	MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx ICMP Error Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled 0x1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled
12	RXICMPGPIM	MMC Receive ICMP Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx ICMP Good Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive ICMP Good Packet Counter Interrupt Mask is disabled 0x1: MMC Receive ICMP Good Packet Counter Interrupt Mask is enabled
11	RXTCPERPIM	MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx TCP Error Packet Counter reaches half

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Bit Field	Name	Description
		of the maximum value or the maximum value. 0x0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled 0x1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled
10	RXTCPGPIM	MMC Receive TCP Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx TCP Good Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive TCP Good Packet Counter Interrupt Mask is disabled 0x1: MMC Receive TCP Good Packet Counter Interrupt Mask is enabled
9	RXUDPERPIM	MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx UDP Error Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled 0x1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled
8	RXUDPGPIM	MMC Receive UDP Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx UDP Good Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive UDP Good Packet Counter Interrupt Mask is disabled 0x1: MMC Receive UDP Good Packet Counter Interrupt Mask is enabled
7:6	Reserved	Reserved, the reset value must be maintained.
5	RXIPV6GPIM	MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx IPV6 Good Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled 0x1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled
4:1	Reserved	Reserved, the reset value must be maintained.
0	RXIPV4GPIM	MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the Rx IPV4 Good Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disabled 0x1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled

47.6.1.60 ETH MMC IPC Rx Interrupt register (ETH_MMCIPCRXINT)

Address offset: 0x0808

Reset value: 0x0000 0000

This register maintains the interrupt that the receive IPC statistic counters generate.

The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000), and when they cross their maximum values (0xFFFF_FFFF). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones.

The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits [7:0]) must

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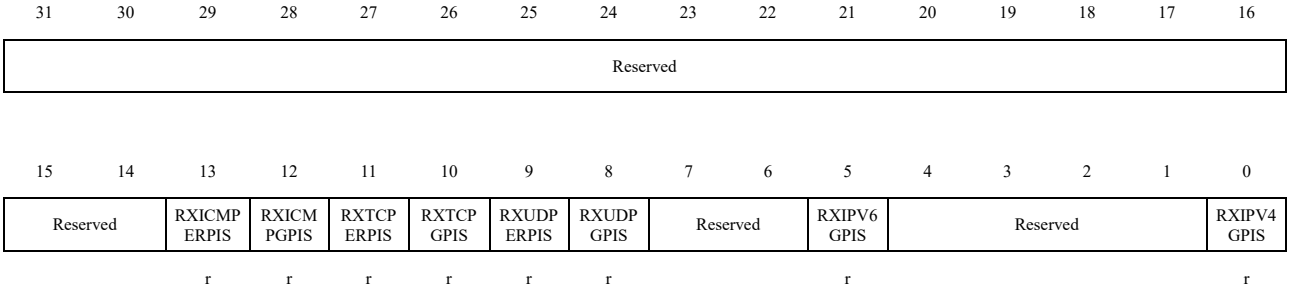
be read to clear the interrupt bit.



Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	RXICMPERPIS	MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the Rx ICMP Error Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected 0x1: MMC Receive ICMP Error Packet Counter Interrupt Status detected
12	RXICMPGPIS	MMC Receive ICMP Good Packet Counter Interrupt Status This bit is set when the Rx ICMP Good Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive ICMP Good Packet Counter Interrupt Status not detected 0x1: MMC Receive ICMP Good Packet Counter Interrupt Status detected
11	RXTCPERPIS	MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the Rx TCP Error Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive TCP Error Packet Counter Interrupt Status not detected 0x1: MMC Receive TCP Error Packet Counter Interrupt Status detected
10	RXTCPGPIS	MMC Receive TCP Good Packet Counter Interrupt Status This bit is set when the Rx TCP Good Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive TCP Good Packet Counter Interrupt Status not detected 0x1: MMC Receive TCP Good Packet Counter Interrupt Status detected
9	RXUDPERPIS	MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the Rx UDP Error Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive UDP Error Packet Counter Interrupt Status not detected 0x1: MMC Receive UDP Error Packet Counter Interrupt Status detected

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Bit Field	Name	Description
8	RXUDPGPIS	MMC Receive UDP Good Packet Counter Interrupt Status This bit is set when the Rx UDP Good Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive UDP Good Packet Counter Interrupt Status not detected 0x1: MMC Receive UDP Good Packet Counter Interrupt Status detected
7:6	Reserved	Reserved, the reset value must be maintained.
5	RXIPV6GPIS	MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the Rx IPV6 Good Packet Counter reaches half of the maximum value or the maximum value. 0x0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected 0x1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected
4:1	Reserved	Reserved, the reset value must be maintained.
0	RXIPV4GPIS	MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the Rx IPV4 Good Packet Counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected 0x1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected

47.6.1.61 ETH Rx IPv4 Good Packets register (ETH_MMCRXIPV4GP)

Address offset: 0x0810

Reset value: 0x0000 0000

This register provides the number of good IPv4 datagrams received by the Ethernet peripheral with the TCP, UDP, or ICMP payload.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXIPV4GDPKT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXIPV4GDPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXIPV4GDPKT	RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

47.6.1.62 ETH Rx IPv6 Good Packets register (ETH_MMCRXIPV6GP)

Address offset: 0x0824

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Reset value: 0x0000 0000

This register provides the number of good IPv6 datagrams received by the Ethernet peripheral with the TCP, UDP, or ICMP payload.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXIPV6GDPKT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXIPV6GDPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXIPV6GDPKT	RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

47.6.1.63 ETH Rx UDP Good Packets register (ETH_MMCRXUDPGP)

Address offset: 0x0830

Reset value: 0x0000 0000

This register provides the number of good IP datagrams received by the Ethernet peripheral with a good UDP payload.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXUDPGDPKT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXUDPGDPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXUDPGDPKT	RxUDP Good Packets This field indicates the number of good IP datagrams received with a good UDP payload.

47.6.1.64 ETH Rx UDP Error Packets register (ETH_MMCRXUDPEP)

Address offset: 0x0834

Reset value: 0x0000 0000

This register provides the number of good IP datagrams received by the Ethernet peripheral whose UDP payload has a checksum error.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXUDPERRPKT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXUDPERRPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXUDPERRPKT	RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

47.6.1.65 ETH Rx TCP Good Packets register (ETH_MMCRXTCPGP)

Address offset: 0x0838

Reset value: 0x0000 0000

This register provides the number of good IP datagrams received by the Ethernet peripheral with a good TCP payload.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXTCPGDPKT[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXTCPGDPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXTCPGDPKT	RxTCP Good Packets This field indicates the number of good IP datagrams received with a good TCP payload.

47.6.1.66 ETH Rx TCP Error Packets register (ETH_MMCRXTCPEP)

Address offset: 0x083C

Reset value: 0x0000 0000

This register provides the number of good IP datagrams received by the Ethernet peripheral whose TCP payload has a checksum error.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXTCPERRPKT[31:16]															

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r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXTCPERRPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXTCPERRPKT	RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

47.6.1.67 ETH Rx ICMP Good Packets register (ETH_MMCRXICMPGP)

Address offset: 0x0840

Reset value: 0x0000 0000

This register provides the number of good IP datagrams received by the Ethernet peripheral with a good ICMP payload.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXICMPGDPKT[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXICMPGDPKT[15:0]															
r															

Bit Field	Name	Description
31:0	RXICMPGDPKT	RxICMP Good Packets This field indicates the number of good IP datagrams received with a good ICMP payload.

47.6.1.68 ETH Rx ICMP Error Packets register (ETH_MMCRXICMPEP)

Address offset: 0x0844

Reset value: 0x0000 0000

This register provides the number of good IP datagrams received by the Ethernet peripheral whose ICMP payload has a checksum error.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXICMPERRPKT[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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RXICMPERRPKT[15:0]
r

Bit Field	Name	Description
31:0	RXICMPERRPKT	RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

47.6.1.69 ETH MAC L3 L4 Filter n Control register (ETH_MACL3L4FnCTRL)

Address offset: 0x0900 + 0x30 × n (n = 0 to 1)

Reset value: 0x0000 0000

This register controls the operations of filter n of Layer 3 and Layer 4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										L4DPIM	L4DPM	L4SPIM	L4SPM	Reserved	L4PEN
										rw	rw	rw	rw		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3HDBM					L3HSBM					L3DAIM	L3DAM	L3SAIM	L3SAM	Reserved	L3PEN
rw					rw					rw	rw	rw	rw		rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	L4DPIM	Layer 4 Destination Port Inverse Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM bit is set high. 0x0: Layer 4 Destination Port Inverse Match is disabled 0x1: Layer 4 Destination Port Inverse Match is enabled
20	L4DPM	Layer 4 Destination Port Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching. 0x0: Layer 4 Destination Port Match is disabled 0x1: Layer 4 Destination Port Match is enabled
19	L4SPIM	Layer 4 Source Port Inverse Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching.

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Bit Field	Name	Description
		This bit is valid and applicable only when the L4SPM bit is set high. 0x0: Layer 4 Source Port Inverse Match is disabled 0x1: Layer 4 Source Port Inverse Match is enabled
18	L4SPM	Layer 4 Source Port Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching. 0x0: Layer 4 Source Port Match is disabled 0x1: Layer 4 Source Port Match is enabled
17	Reserved	Reserved, the reset value must be maintained.
16	L4PEN	Layer 4 Protocol Enable When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM or L4DPM bit is set. 0x0: Layer 4 Protocol is disabled 0x1: Layer 4 Protocol is enabled
15:11	L3HDBM	Layer 3 IP DA Higher Bits Match **IPv4 Packets:** This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSB [0] is masked 2: Two LSBs [1:0] are masked .. 31: All bits except MSB are masked. **IPv6 Packets:** Bits [12:11] of this field correspond to Bits [6:5] of L3HSBM which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM [1:0] and L3HSBM bits: 0: No bits are masked. 1: LSB [0] is masked. 2: Two LSBs [1:0] are masked .. 127: All bits except MSB are masked. This field is valid and applicable only when the L3DAM or L3SAM bit is set.
10:6	L3HSBM	Layer 3 IP SA Higher Bits Match **IPv4 Packets:** This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked.

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Bit Field	Name	Description
		1: LSB [0] is masked 2: Two LSBs [1:0] are masked .. 31: All bits except MSB are masked. **IPv6 Packets:** This field contains Bits [4:0] of L3HSBM. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM or L3SAM bit is set high.
5	L3DAIM	Layer 3 IP DA Inverse Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM bit is set high. 0x0: Layer 3 IP DA Inverse Match is disabled 0x1: Layer 3 IP DA Inverse Match is enabled
4	L3DAM	Layer 3 IP DA Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. 0x0: Layer 3 IP DA Match is disabled 0x1: Layer 3 IP DA Match is enabled *Note: When the L3PEN bit is set, you should set either this bit or the L3SAM bit because either IPv6 DA or SA can be checked for filtering.*
3	L3SAIM	Layer 3 IP SA Inverse Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM bit is set. 0x0: Layer 3 IP SA Inverse Match is disabled 0x1: Layer 3 IP SA Inverse Match is enabled
2	L3SAM	Layer 3 IP SA Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. 0x0: Layer 3 IP SA Match is disabled 0x1: Layer 3 IP SA Match is enabled *Note: When the L3PEN bit is set, you should set either this bit or the L3DAM bit because either IPv6 SA or DA can be checked for filtering.*
1	Reserved	Reserved, the reset value must be maintained.
0	L3PEN	Layer 3 Protocol Enable When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets.

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Bit Field	Name	Description
		The Layer 3 matching is done only when the L3SAM or L3DAM bit is set. 0x0: Layer 3 Protocol is disabled 0x1: Layer 3 Protocol is enabled

47.6.1.70 ETH MAC L4 Filter n Port register (ETH_MACL4FnPORT)

Address offset: 0x0904 + 0x30 × n (n = 0 to 1)

Reset value: 0x0000 0000

This register holds the destination/source port number used for Layer 4 filter n.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L4DP															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L4SP															
rw															

Bit Field	Name	Description
31:16	L4DP	Layer 4 Destination Port Number Field When the L4PEN bit is reset and the L4DPM bit is set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN and L4DPM bits are set in MAC L3 L4 Filter n Control register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	L4SP	Layer 4 Source Port Number Field When the L4PEN bit is reset and the L4SPM bit is set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN and L4SPM bits are set in MAC L3 L4 Filter n Control register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

47.6.1.71 ETH MAC L3 Filter n Address 0 register (ETH_MACL3FnADDR0)

Address offset: 0x0910 + 0x30 × n (n = 0 to 1)

Reset value: 0x0000 0000

For IPv4 packets, this register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits [31:0] of the 128-bit IP Source Address or Destination Address field.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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L3A0[31:16]

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3A0[15:0]															

rw

Bit Field	Name	Description
31:0	L3A0	Layer 3 Address 0 Field When the L3PEN and L3SAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN and L3DAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN bit is reset and the L3SAM bit is set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

47.6.1.72 ETH MAC L3 Filter n Address 1 register (ETH_MACL3FnADDR1)

Address offset: 0x0914 + 0x30 × n (n = 0 to 1)

Reset value: 0x0000 0000

For IPv4 packets, this register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits [63:32] of the 128-bit IP Source Address or Destination Address field.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L3A1[31:16]															

rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3A1[15:0]															

rw

Bit Field	Name	Description
31:0	L3A1	Layer 3 Address 1 Field When the L3PEN and L3SAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN and L3DAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [63:32] of the IP Destination

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Bit Field	Name	Description
		Address field in the IPv6 packets. When the L3PEN bit is reset and the L3SAM bit is set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

47.6.1.73 ETH MAC L3 Filter n Address 2 register (ETH_MACL3FnADDR2)

Address offset: 0x0918 + 0x30 × n (n = 0 to 1)

Reset value: 0x0000 0000

For IPv4 packets, this register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits [95:64] of the 128-bit IP Source Address or Destination Address field.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L3A2[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3A2[15:0]															
rw															

Bit Field	Name	Description
31:0	L3A2	Layer 3 Address 2 Field When the L3PEN and L3SAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN and L3DAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN bit is reset and the L3SAM bit is set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

47.6.1.74 ETH MAC L3 Filter n Address 3 register (ETH_MACL3FnADDR3)

Address offset: 0x091C + 0x30 × n (n = 0 to 1)

Reset value: 0x0000 0000

For IPv4 packets, this register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits [127:96] of the 128-bit IP Source Address or Destination Address field.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
L3A3[31:16]															
rw															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3A3[15:0]															
rw															

Bit Field	Name	Description
31:0	L3A3	Layer 3 Address 3 Field When the L3PEN and L3SAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN and L3DAM bits are set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with Bits [127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN bit is reset and the L3SAM bit is set in the MAC L3 L4 Filter n Control register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

47.6.1.75 ETH MAC Timestamp Control register (ETH_MACTSCTRL)

Address offset: 0x0B00

Reset value: 0x0000 2000

This register controls the operation of the system time generator and the processing of PTP packets for the receiver timestamps.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			AV8021 ASMEN	Reserved			TXTSST SM	Reserved					TSENM ACADD R	SNAPTYPSEL	
			rw				rw						rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSMST RENA	TSEVN TENA	TSIPV4E NA	TSIPV6 ENA	TSIPEN A	TSVER2 ENA	TSCTR LSSR	TSENA LL	Reserve d	PTGE	TSADD REG	Reserve d	TSUPD T	TSINIT	TSCFUP DT	TSENA
rw	rw	rw	rw	rw	rw	rw	rw		rw	rw		rw	rw	rw	rw

Bit Field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	AV8021ASMEN	AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. 0x0: AV 802.1AS Mode is disabled 0x1: AV 802.1AS Mode is enabled
27:25	Reserved	Reserved, the reset value must be maintained.
24	TXTSSTSM	Transmit Timestamp Status Mode

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Bit Field	Name	Description
		When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC Tx Timestamp Status Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC Tx Timestamp Status Nanoseconds register. 0x0: Transmit Timestamp Status Mode is disabled 0x1: Transmit Timestamp Status Mode is enabled
23:19	Reserved	Reserved, the reset value must be maintained.
18	TSENMACADDR	Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 3 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. 0x0: MAC Address for PTP Packet Filtering is disabled 0x1: MAC Address for PTP Packet Filtering is enabled
17:16	SNAPTYPSEL	Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Table 47-22.
15	TSMSTRENA	Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. 0x0: Snapshot for Messages Relevant to Master is disabled 0x1: Snapshot for Messages Relevant to Master is enabled
14	TSEVNTENA	Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Table 47-22. 0x0: Timestamp Snapshot for Event Messages is disabled 0x1: Timestamp Snapshot for Event Messages is enabled
13	TSIPV4ENA	Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default.

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Bit Field	Name	Description
		0x0: Processing of PTP Packets Sent over IPv4-UDP is disabled 0x1: Processing of PTP Packets Sent over IPv4-UDP is enabled
12	TSIPV6ENA	Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. 0x0: Processing of PTP Packets Sent over IPv6-UDP is disabled 0x1: Processing of PTP Packets Sent over IPv6-UDP is enabled
11	TSIPENA	Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. 0x0: Processing of PTP over Ethernet Packets is disabled 0x1: Processing of PTP over Ethernet Packets is enabled
10	TSVER2ENA	Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 47.5.6.5. 0x0: PTP Packet Processing for Version 2 Format is disabled 0x1: PTP Packet Processing for Version 2 Format is enabled
9	TSCTRLSSR	Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. 0x0: Timestamp Digital or Binary Rollover Control is disabled 0x1: Timestamp Digital or Binary Rollover Control is enabled
8	TSENALL	Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. 0x0: Timestamp for All Packets disabled 0x1: Timestamp for All Packets enabled
7	Reserved	Reserved, the reset value must be maintained.
6	PTGE	Presentation Time Generation Enable When this bit is set the Presentation Time generation is enabled. 0x0: Presentation Time Generation is disabled 0x1: Presentation Time Generation is enabled
5	TSADDREG	Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set.

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Bit Field	Name	Description
		0x0: Addend Register is not updated 0x1: Addend Register is updated *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*
4	Reserved	Reserved, the reset value must be maintained.
3	TSUPDT	Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC System Time Seconds Update and MAC System Time Nanoseconds Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register is not updated. When Media Clock Generation and Recovery is configured and enabled MAC Presentation Time update should also be updated before setting this field. 0x0: Timestamp is not updated 0x1: Timestamp is updated *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*
2	TSINIT	Initialize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC System Time Second Update and MAC System Time Nanosecond Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register can only be initialized. When Media Clock Generation and Recovery is configured and enabled MAC Presentation Time update should also be updated before setting this field. 0x0: Timestamp is not initialized 0x1: Timestamp is initialized *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*
1	TSCFUPDT	Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. 0x0: Coarse method is used to update system timestamp 0x1: Fine method is used to update system timestamp
0	TSENA	Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set. 0x0: Timestamp is disabled 0x1: Timestamp is enabled

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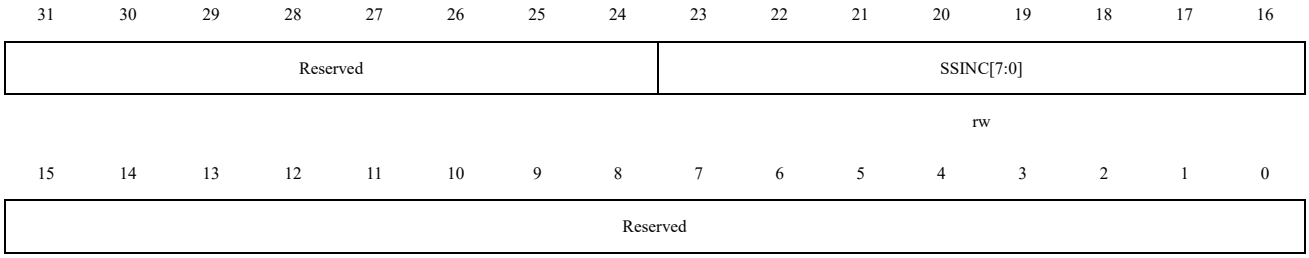
47.6.1.76 ETH MAC Sub Second Increment register (ETH_MACSUBSINC)

Address offset: 0x0B04

Reset value: 0x0000 0000

This register specifies the value added to the internal system time register for each clk_ptp_ref_i clock cycle.



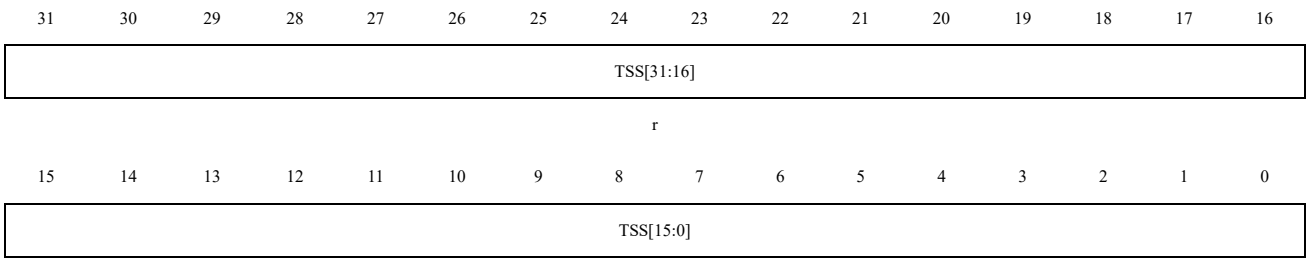
Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:16	SSINC	Sub-second Increment Value The value programmed in this field will be accumulated with the content of the sub-second register for each clock cycle of PTP. For example, when the PTP clock is 50MHz (period is 20ns), and the precision of the system time nanoseconds register is 1ns (TSCTRLSSR set to 1 in the MAC Timestamp Control register), it should be programmed as 20 (0x14). When TSCTRLSSR is cleared, the resolution of the nanoseconds register is ~0.465ns. In this case, the programmed value should be 43 (0x2B), derived from 20ns/0.465.
15:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.77 ETH MAC System Time Seconds register (ETH_MACSYSTS)

Address offset: 0x0B08

Reset value: 0x0000 0000

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).



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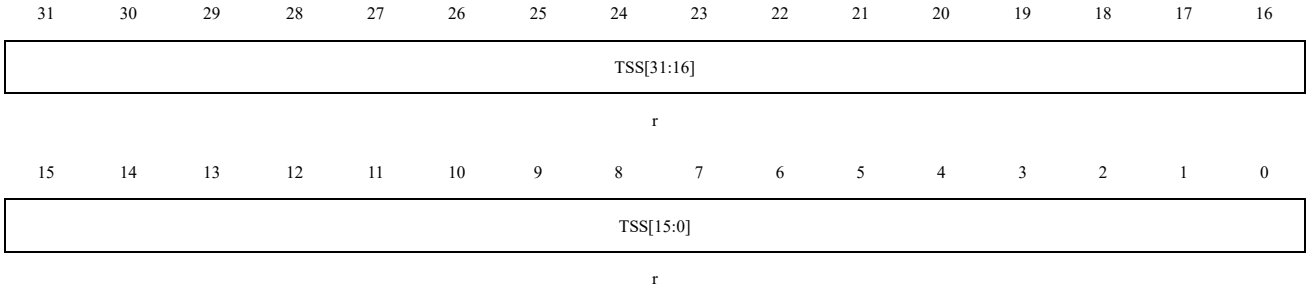
Bit Field	Name	Description
31:0	TSS	Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

47.6.1.78 ETH MAC System Time Nanoseconds register (ETH_MACSYSTNS)

Address offset: 0x0B0C

Reset value: 0x0000 0000

The system time nanoseconds register and system time seconds register indicate the current value of the system time maintained by the MAC.



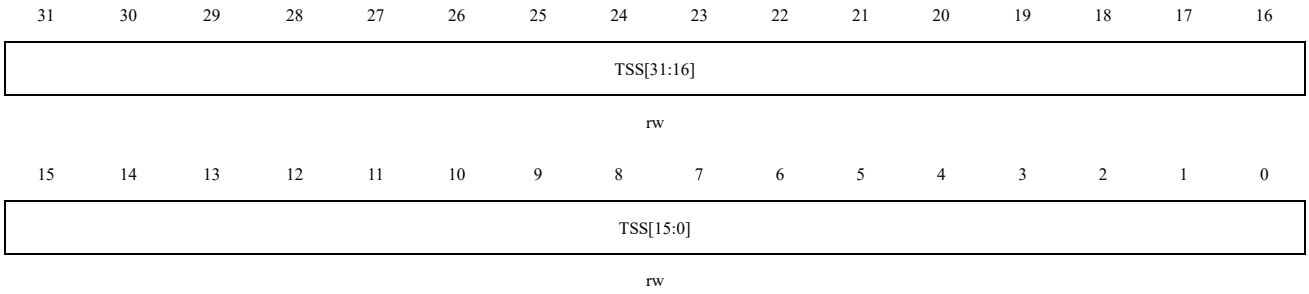
Bit Field	Name	Description
31:0	TSS	Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC Timestamp Control register, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

47.6.1.79 ETH MAC System Time Seconds Update register (ETH_MACSYSTSUP)

Address offset: 0x0B10

Reset value: 0x0000 0000

The system time seconds update register, along with the system time nanoseconds update register, is used for initializing or updating the system time maintained by the MAC. Before setting the second bit (TSINIT) or third bit (TSUPDT) in the MAC Timestamp Control register, both of these registers (system time seconds update register and system time nanoseconds update register) must be written to.



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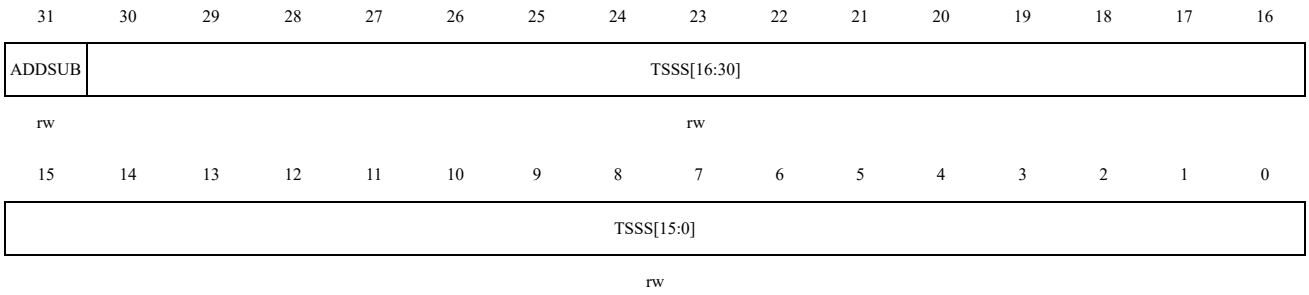
Bit Field	Name	Description
31:0	TSS	Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, to subtract 2.000000001 seconds from the system time, the TSS field in the MAC Timestamp Seconds Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

47.6.1.80 ETH MAC System Time Nanoseconds Update register (ETH_MACSYSTNSUP)

Address offset: 0x0B14

Reset value: 0x0000 0000



Bit Field	Name	Description
31	ADDSUB	Add or Subtract Time When this bit is set to 1, the time value will be subtracted from the content of the update register. When this bit is reset, the time value will be added to the content of the update register. 0: Add Time 1: Subtract Time
30:0	TSSS	Timestamp Sub-seconds The value in this field represents the sub-second part of the update value. ADDSUB is 1: The field must be programmed with the two's complement of the sub-second part of the update value as described. ADDSUB is 0: The field must be programmed with the sub-second part of the update value, with the precision based on the TSCTRLSSR bit in the MAC Timestamp Control register. For TSCTRLSSR bit field as 1: The programmed value must be 10^9 - <sub-second value>; each bit represents 1ns, and the programmed value should not exceed 0x3B9A_C9FF. For TSCTRLSSR bit field as 0: The programmed value must be 2^31 - <sub-second value>: each bit represents a precision of 0.46ns. For example, to subtract 2.000000001 seconds from the system time, the TSSS field in

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Bit Field	Name	Description
		the MAC System Time Nanoseconds Update Register must be 0x7FFF_FFFF (i.e., 2^31 - 1) when the TSCTRLSSR bit is 0 in the MAC Timestamp Control Register, and must be 0x3B9A_C9FF (i.e., 10^9 - 1) when the TSCTRLSSR bit is 1 in the MAC Timestamp Control Register.

47.6.1.81 ETH MAC Timestamp Addend register (ETH_MACTSADD)

Address offset: 0x0B18

Reset value: 0x0000 0000

Only when the system time is configured in fine update mode (by setting the TSCFUPDT bit in the MAC Timestamp Control register), will the value of this register be used. The content of this register is added to a 32-bit accumulator every clock cycle (clk_ptp_ref_i), and when the accumulator overflows, the system time will be updated.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSAR[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSAR[15:0]															
rw															

Bit Field	Name	Description
31:0	TSAR	Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

47.6.1.82 ETH MAC System Time Higher Word Seconds register (ETH_MACSYSTHWS)

Address offset: 0x0B1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSHWR[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.

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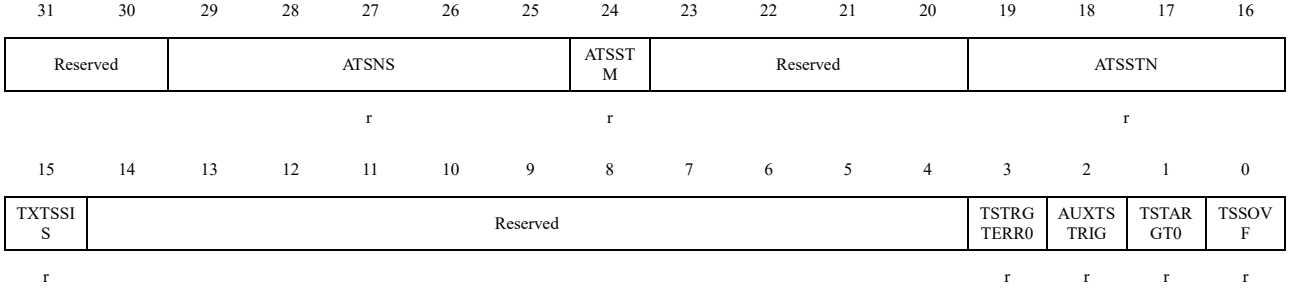
Bit Field	Name	Description
15:0	TSHWR	Timestamp Higher Word Register This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register.

47.6.1.83 ETH MAC Timestamp Status register (ETH_MACTSSTS)

Address offset: 0x0B20

Reset value: 0x0000 0000

All bits except Bits [27:25] gets cleared when the application reads this register.



Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:25	ATSNS	Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set.
24	ATSSTM	Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. 0x0: Auxiliary Timestamp Snapshot Trigger Missed status not detected 0x1: Auxiliary Timestamp Snapshot Trigger Missed status detected
23:20	Reserved	Reserved, the reset value must be maintained.
19:16	ATSSTN	Auxiliary Timestamp Snapshot Trigger Identifier These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: Bit 16: Auxiliary trigger 0 Bit 17: Auxiliary trigger 1

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Bit Field	Name	Description
		Bit 18: Auxiliary trigger 2 Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken.
15	TXTSSIS	Tx Timestamp Status Interrupt Status If the discard transmit status is enabled in the MTL, this bit will be set to 1 when the captured transmit timestamp is updated in the MAC Transmit Timestamp Status Nanoseconds register and MAC Transmit Timestamp Status Seconds register. Clear this bit when reading the MAC Transmit Timestamp Status Seconds register (or when writing to the MAC Transmit Timestamp Status Seconds register by setting the RCWE bit in the MAC CSR Software Control Register). 0: Tx Timestamp Status Interrupt status not detected 1: Tx Timestamp Status Interrupt status detected
14:4	Reserved	Reserved, the reset value must be maintained.
3	TSTRGTERR0	Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC PPS0 Target Time Seconds register and MAC PPS0 Target Time Nanoseconds register elapses. This bit is cleared when the application reads this bit. 0: Timestamp Target Time Error status not detected 1: Timestamp Target Time Error status detected *Note: This bit has access restrictions. Read (or write 1 when the RCWE bit in the MAC CSR Software Control Register is set) to clear. Automatically set to 1 on internal events.*
2	AUXTSTRIG	Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. 0x0: Auxiliary Timestamp Trigger Snapshot status not detected 0x1: Auxiliary Timestamp Trigger Snapshot status detected *Note: This bit has access restrictions. Read (or write 1 when the RCWE bit in the MAC CSR Software Control Register is set) to clear. Automatically set to 1 on internal events.*
1	TSTARGT0	Timestamp Target Time Reached When this bit is set and MCGREN0 of MAC PPS Control register is reset, it indicates that the value of system time is greater than or equal to the value specified in the MAC PPS0 Target Time Seconds register and MAC PPS0 Target Time Nanoseconds register. When this bit is set and MCGREN0 of MAC PPS Control register is set, it indicates that mcgr_dma_req_o [0] is asserted. 0: Timestamp Target Time Reached status not detected 1: Timestamp Target Time Reached status detected *Note: This bit has access restrictions. Read (or write 1 when the RCWE bit in the MAC CSR Software Control Register is set) to clear. Automatically set to 1 on internal events.*
0	TSSOVF	Timestamp Seconds Overflow

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Bit Field	Name	Description
		When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. 0: Timestamp Seconds Overflow status not detected 1: Timestamp Seconds Overflow status detected *Note: This bit has access restrictions. Read (or write 1 when the RCWE bit in the MAC CSR Software Control Register is set) to clear. Automatically set to 1 on internal events.*

47.6.1.84 ETH MAC Tx Timestamp Status Nanoseconds register (ETH_MACTXTSSTSNS)

Address offset: 0x0B30

Reset value: 0x0000 0000

This register contains the nanosecond part of the timestamp of the transmitted packet captured when the transmit status is disabled.

The MAC Transmit Timestamp Status Nanoseconds Register, together with the MAC Transmit Timestamp Status Seconds Register, provides a 64-bit timestamp captured when the MAC successfully transmits a PTP packet. When reading the last byte of the MAC Transmit Timestamp Status Nanoseconds Register, it is assumed that the application has read this value. In little-endian mode, this means reading bits [31:24]; in big-endian mode, it means reading bits [7:0].

If the application does not read these registers and captures a timestamp of another packet, the current timestamp will be lost (overwritten) or the new timestamp will be lost (discarded), depending on the setting of the TXTSSTSM bit in the MAC Timestamp Control Register. When the MAC transmitter captures a timestamp, the status bit TXTSSIS (bit [15]) in the MAC Timestamp Status Register will be set.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXTSSMIS	TXTSSLO[16:30]														
rw	r														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXTSSLO[15:0]															
r															

Bit Field	Name	Description
31	TXTSSMIS	Transmit Timestamp Status Missed When this bit is set to 1, it indicates one of the following: ■ If the TXTSSTSM bit in the MAC Timestamp Control Register is 0, the timestamp of the current packet is ignored. ■ If the TXTSSTSM bit in the MAC Timestamp Control Register is 1, the timestamp of the previous packet is overwritten by the timestamp of the current packet. 0: Transmit Timestamp Status Missed status not detected

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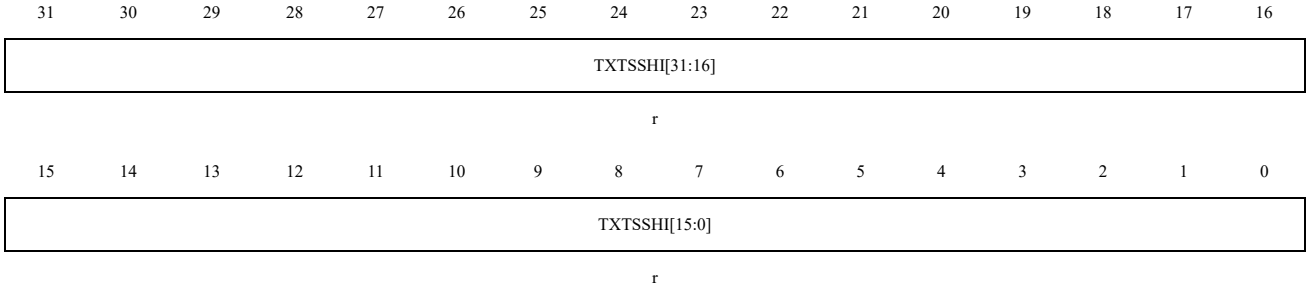
Bit Field	Name	Description
		1: Transmit Timestamp Status Missed status detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 on internal events.*
30:0	TXTSSLO	Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp

47.6.1.85 ETH MAC Tx Timestamp Status Seconds register (ETH_MACTXTSSTSS)

Address offset: 0x0B34

Reset value: 0x0000 0000

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.



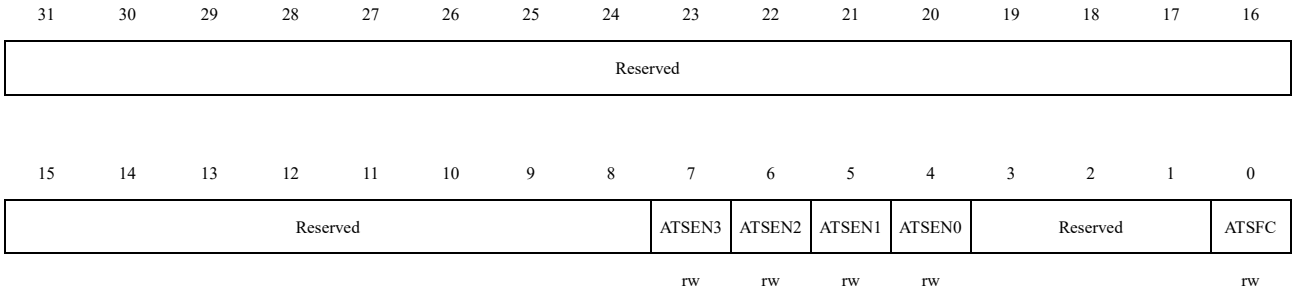
Bit Field	Name	Description
31:0	TXTSSHI	Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

47.6.1.86 ETH MAC Auxiliary Control register (ETH_MACAUXCTRL)

Address offset: 0x0B40

Reset value: 0x0000 0000

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.



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Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	ATSEN3	Auxiliary Snapshot 3 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 3. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i [3] input is enabled. When this bit is reset, the events on this input are ignored. 0x0: Auxiliary Snapshot 3 is disabled 0x1: Auxiliary Snapshot 3 is enabled
6	ATSEN2	Auxiliary Snapshot 2 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 2. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i [2] input is enabled. When this bit is reset, the events on this input are ignored. 0x0: Auxiliary Snapshot 2 is disabled 0x1: Auxiliary Snapshot 2 is enabled
5	ATSEN1	Auxiliary Snapshot 1 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i [1] input is enabled. When this bit is reset, the events on this input are ignored. 0x0: Auxiliary Snapshot 1 is disabled 0x1: Auxiliary Snapshot 1 is enabled
4	ATSEN0	Auxiliary Snapshot 0 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i [0] input is enabled. When this bit is reset, the events on this input are ignored. 0x0: Auxiliary Snapshot 0 is disabled 0x1: Auxiliary Snapshot 0 is enabled
3:1	Reserved	Reserved, the reset value must be maintained.
0	ATSFC	Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0: Auxiliary Snapshot FIFO Clear is disabled 0x1: Auxiliary Snapshot FIFO Clear is enabled

47.6.1.87 ETH MAC Auxiliary Timestamp Nanoseconds register (ETH_MACAUXTSNS)

Address offset: 0x0B48

Reset value: 0x0000 0000

The Auxiliary Timestamp Nanoseconds register, along with MAC Auxiliary Timestamp Seconds register, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4.

You can store multiple snapshots in this FIFO. Bits [29:25] in MAC Timestamp Status register indicate the fill-level

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of the FIFO. The top of the FIFO is removed only when the last byte of MAC Auxiliary Timestamp Seconds register is read. In the little-endian mode, this means when Bits [31:24] are read and in big-endian mode, Bits [7:0] are read.

Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30:0	AUXTSLO	Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

47.6.1.88 ETH MAC Auxiliary Timestamp Seconds register (ETH_MACAUXTSS)

Address offset: 0x0B4C

Reset value: 0x0000 0000

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Bit Field	Name	Description
31:0	AUXTSHI	Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

47.6.1.89 ETH MAC Timestamp Ingress Asymmetry Correction register (ETH_MACTSIGASYC)

Address offset: 0x0B50

Reset value: 0x0000 0000

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSTIAC[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSTIAC[15:0]															
rw															

Bit Field	Name	Description
31:0	OSTIAC	One-Step Timestamp Ingress Asymmetry Correction This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

47.6.1.90 ETH MAC Timestamp Egress Asymmetry Correction register (ETH_MACTSEGASYC)

Address offset: 0x0B54

Reset value: 0x0000 0000

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSTEAC[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSTEAC[15:0]															
rw															

Bit Field	Name	Description
31:0	OSTEAC	One-Step Timestamp Egress Asymmetry Correction This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000 (2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216).

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47.6.1.91 ETH MAC Timestamp Ingress Correction Nanosecond register (ETH_MACTSIGCNS)

Address offset: 0x0B58

Reset value: 0x0000 0000

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSIC[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSIC[15:0]															
rw															

Bit Field	Name	Description
31:0	TSIC	Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression.

47.6.1.92 ETH MAC Timestamp Egress Correction Nanosecond register (ETH_MACTSEGCNS)

Address offset: 0x0B5C

Reset value: 0x0000 0000

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSEC[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSEC[15:0]															
rw															

Bit Field	Name	Description
31:0	TSEC	Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

47.6.1.93 ETH MAC Timestamp Ingress Latency register (ETH_MACTSIGLAT)

Address offset: 0x0B68

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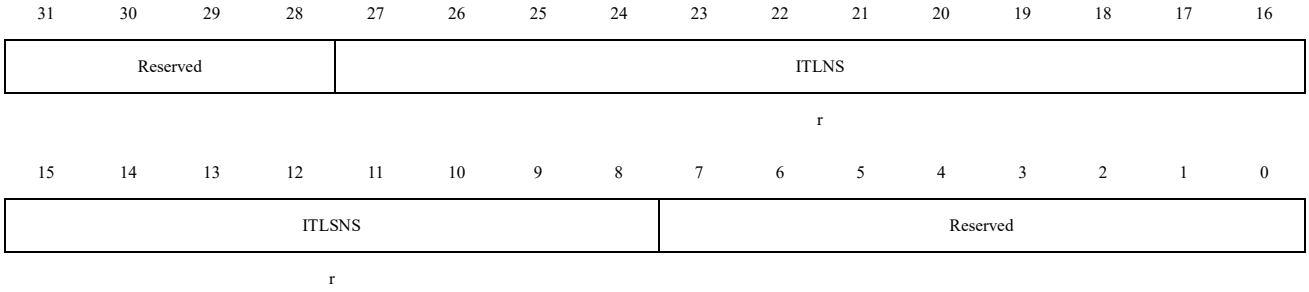
Reset value: 0x0000 0000

This register holds the Ingress MAC latency.



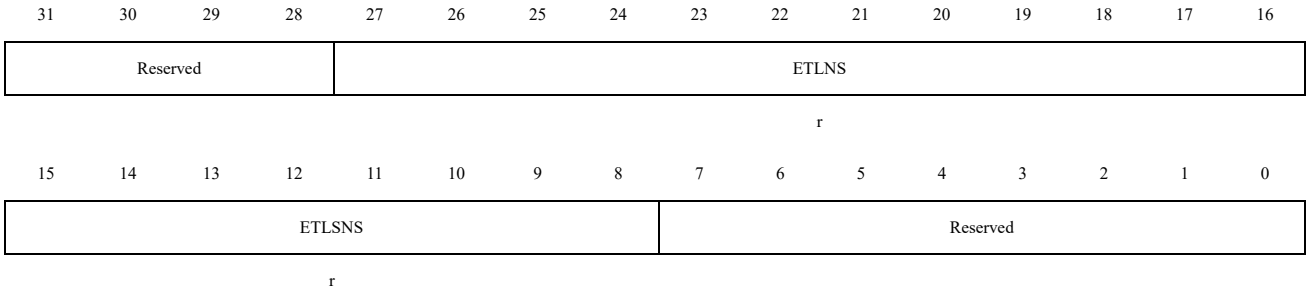
Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:16	ITLNS	Ingress Timestamp Latency, in nanoseconds This register stores the average delay (in nanoseconds) between the MAC input port (TXD) and the actual point of ingress timestamp capture (MII). The calculation method for the ingress correction value is as described in section 47.5.6.4.
15:8	ITLSNS	Ingress Timestamp Latency, in sub-nanoseconds This register stores the average delay (in sub-nanoseconds) between the MAC input port (TXD) and the actual point of ingress timestamp capture (MII). The calculation method for the ingress correction value is as described in section 47.5.6.4.
7:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.94 ETH MAC Timestamp Egress Latency register (ETH_MACTSEGLAT)

Address offset: 0x0B6C

Reset value: 0x0000 0000

This register holds the Egress MAC latency.



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27:16	ETLNS	Egress Timestamp Latency, in nanoseconds This register stores the average delay (in nanoseconds) between the MAC output port

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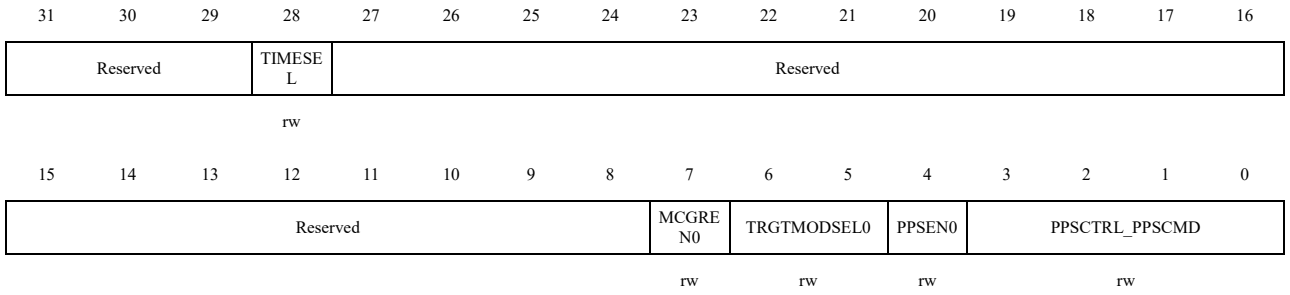
Bit Field	Name	Description
		(RXD) and the actual point of egress timestamp capture (MII). The calculation method for the egress correction value is as described in section 47.5.6.4.
15:8	ETLSNS	Egress Timestamp Latency, in sub-nanoseconds This register stores the average delay (in sub-nanoseconds) between the MAC output port (RXD) and the actual point of egress timestamp capture (MII). The calculation method for the egress correction value is as described in section 47.5.6.4.
7:0	Reserved	Reserved, the reset value must be maintained.

47.6.1.95 ETH MAC PPS Control register (ETH_MACPPSCTRL)

Address offset: 0x0B70

Reset value: 0x0000 0000

PPS Control register (PPS).



Bit Field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	TIMESEL	Time Select When this bit is set, 64 bit PTP time is used to capture time at MCGR trigger[0] input When this bit is reset, presentation time is used to capture time at trigger input, maintaining backward compatibility
27:8	Reserved	Reserved, the reset value must be maintained.
7	MCGREN0	MCGR Mode Enable for PPS0 Output This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. 0x0: 0th PPS instance is enabled to operate in PPS mode 0x1: 0th PPS instance is enabled to operate in MCGR mode
6:5	TRGTMODSEL0	Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC PPS Target Time Seconds and MAC PPS Target Time Nanoseconds) mode for PPS output signal: 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding ptp_pps_o output port. 0x1 (MCGR): Enables MCGR Interrupt whose status bit is indicated by TSTARGT0.

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Bit Field	Name	Description
		0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS output signal generation. 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS output signal generation. No interrupt is asserted.
4	PPSEN0	Flexible PPS Output Mode Enable When this bit is: ■ 1: Bits [3:0] function as PPSCMD. ■ 0: Bits [3:0] function as PPSCTRL (Fixed PPS mode). 0x0: Flexible PPS Output Mode is disabled 0x1: Flexible PPS Output Mode is enabled
3:0	PPSCTRL_PPSCMD	**PPS Output Frequency Control:** This field controls the frequency of the PPS0 output (ptp_pps_o [0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. .. 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. *Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies.* *In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example:* ■ *When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms* ■ *When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period, Second clock of 463 ms period (268 ms low and 195 ms high)* ■ *When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period, Fourth clock of 195 ms period (134 ms low and 61 ms high)* *This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC System Time Nanoseconds register.* **Flexible PPS Output (ptp_pps_o [0]) Control:** Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: 0000: No Command.

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Bit Field	Name	Description
		0001: START Single Pulse. This command generates single pulse rising at the start point defined in MAC PPS Target Time Seconds and MAC PPS Target Time Nanoseconds register and of a duration defined in the PPS Width Register. 0010: START Pulse Train. This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. 0011: Cancel START. This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. 0100: STOP Pulse train at time.This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. 0101: STOP Pulse Train immediately. This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). 0110: Cancel STOP Pulse train. This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. 0111-1111: Reserved. **Presentation Time Control:** When MCGREN0 is 1, these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed. 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i [0] into the MAC PPS Target Time Seconds register. 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i [0] into the MAC PPS Target Time Seconds register. 0011: Capture the Presentation time at both edges of mcg_pst_trig_i [0] into the MAC PPS Target Time Seconds register. 0100-1000: Reserved. 1001: Toggle output on compare. 1010: Pulse output low on compare for one PTP-clock cycle. 1011: Pulse output high on compare for one PTP-clock cycle. 1100-1111: Reserved.

47.6.1.96 ETH MAC PPS Target Time Seconds register (ETH_MACPPSTTS)

Address offset: 0x0B80

Reset value: 0x0000 0000

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event (Bit 1 of the MAC Timestamp Status register) when the system time exceeds the value

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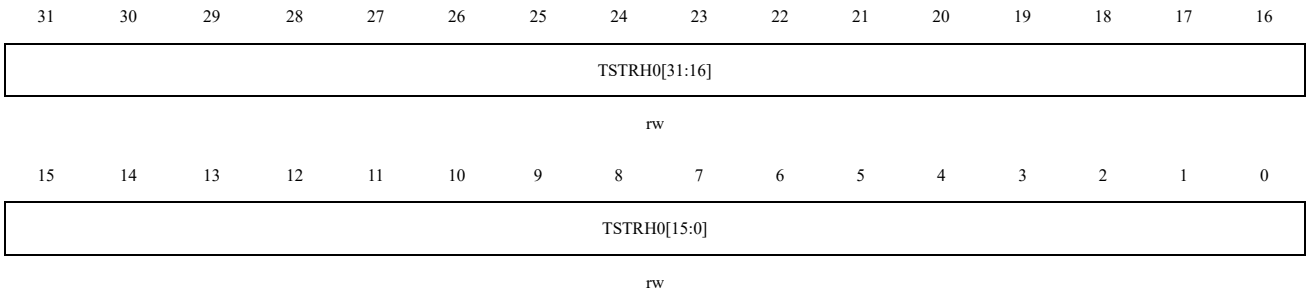
programmed in these registers.



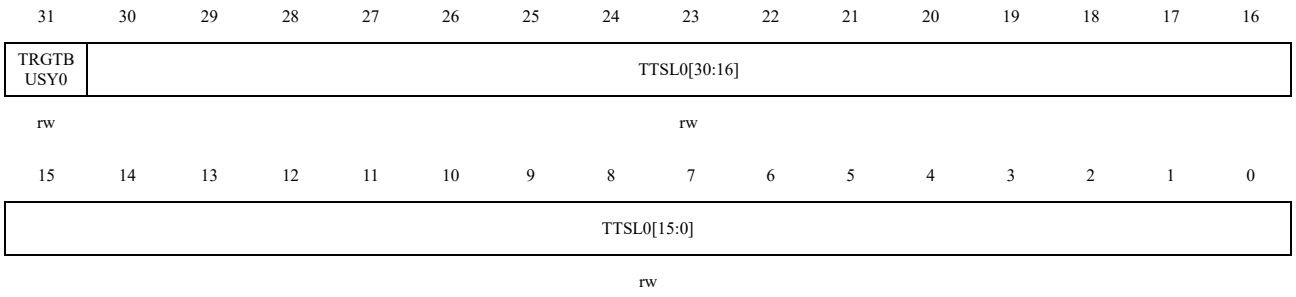
Bit Field	Name	Description
31:0	TSTRH0	PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC PPS Control register.

47.6.1.97 ETH MAC PPS Target Time Nanoseconds register (ETH_MACPPSTTNS)

Address offset: 0x0B84

Reset value: 0x0000 0000

PPS Target Time Nanoseconds register.



Bit Field	Name	Description
31	TRGTBUSY0	PPS Target Time Register Busy The MAC sets this bit when the PPSCMD field in the MAC PPS Control register is programmed to 010 or 011. Programming the PPSCMD field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. 0x0: PPS Target Time Register Busy status is not detected 0x1: PPS Target Time Register Busy is detected
30:0	TTSL0	Target Time Low for PPS Register

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Bit Field	Name	Description
		This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC PPS Control register. When the TSCTRLSSR bit is reset in the MAC Timestamp Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC Timestamp Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value.

47.6.1.98 ETH MAC PPS Interval register (ETH_MACPPSINTE)

Address offset: 0x0B88

Reset value: 0x0000 0000

The PPS Interval register contains the number of units of sub-second increment value between the rising edges of PPS signal output (ptp_pps_o [0]).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PPSINT0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPSINT0[15:0]															
rw															

Bit Field	Name	Description
31:0	PPSINT0	PPS Output Signal Interval These bits store the interval between the rising edges of PPS signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

47.6.1.99 ETH MAC PPS Width register (ETH_MACPPSWID)

Address offset: 0x0B8C

Reset value: 0x0000 0000

The PPS Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS signal output (ptp_pps_o [0]).

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PPSWIDTH0[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPSWIDTH0[15:0]															
rw															

Bit Field	Name	Description
31:0	PPSWIDTH0	PPS Output Signal Width These bits store the width between the rising edge and corresponding falling edge of PPS signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. *Note: The value programmed in this register must be lesser than the value programmed in MAC PPS Interval register.*

47.6.1.100 ETH MAC PTO Control register (ETH_MACPTOCTRL)

Address offset: 0x0BC0

Reset value: 0x0000 0000

This register controls the PTP Offload Engine operation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DN								PDRDIS	DRRDIS	APDREQTRIG	ASYNCTRIG	Reserved	APDREQEN	ASYNCEN	PTOEN
rw								rw	rw	rw	rw		rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:8	DN	Domain Number This field indicates the domain Number in which the PTP node is operating.
7	PDRDIS	Disable Peer Delay Response response generation When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not be generated for received Peer Delay Request (Pdelay_Req) request packet, as required by

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Bit Field	Name	Description
		the programmed mode. 0x0: Peer Delay Response response generation is enabled 0x1: Peer Delay Response response generation is disabled *Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in hardware and/or Pdelay_Resp generation is handled by software.*
6	DRRDIS	Disable PTO Delay Request/Response response generation When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode. 0x0: PTO Delay Request/Response response generation is enabled 0x1: PTO Delay Request/Response response generation is disabled
5	APDREQTRIG	Automatic PTP Pdelay_Req message Trigger When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0: Automatic PTP Pdelay_Req message Trigger is disabled 0x1: Automatic PTP Pdelay_Req message Trigger is enabled
4	ASYNCTRIG	Automatic PTP SYNC message Trigger When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0: Automatic PTP SYNC message Trigger is disabled 0x1: Automatic PTP SYNC message Trigger is enabled
3	Reserved	Reserved, the reset value must be maintained.
2	APDREQEN	Automatic PTP Pdelay_Req message Enable When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode. 0x0: Automatic PTP Pdelay_Req message is disabled 0x1: Automatic PTP Pdelay_Req message is enabled
1	ASYNCEN	Automatic PTP SYNC message Enable When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Master mode. 0x0: Automatic PTP SYNC message is disabled 0x1: Automatic PTP SYNC message is enabled
0	PTOEN	PTP Offload Enable When this bit is set, the PTP Offload feature is enabled. 0x0: PTP Offload feature is disabled 0x1: PTP Offload feature is enabled

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47.6.1.101 ETH MAC Source Port Identity 0 register (ETH_MACSRCPID0)

Address offset: 0x0BC4

Reset value: 0x0000 0000

This register contains Bits [31:0] of the 80-bit Source Port Identity of the PTP node.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPI0[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI0[15:0]															
rw															

Bit Field	Name	Description
31:0	SPI0	Source Port Identity 0 This field indicates bits [31:0] of sourcePortIdentity of PTP node.

47.6.1.102 ETH MAC Source Port Identity 1 register (ETH_MACSRCPID1)

Address offset: 0x0BC8

Reset value: 0x0000 0000

This register contains Bits [63:32] of the 80-bit Source Port Identity of the PTP node.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPI1[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI1[15:0]															
rw															

Bit Field	Name	Description
31:0	SPI1	Source Port Identity 1 This field indicates bits [63:32] of sourcePortIdentity of PTP node.

47.6.1.103 ETH MAC Source Port Identity 2 register (ETH_MACSRCPID2)

Address offset: 0x0BCC

Reset value: 0x0000 0000

This register contains Bits [79:64] of the 80-bit Source Port Identity of the PTP node.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI2[15:0]															
rw															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	SPI2	Source Port Identity 2 This field indicates bits [79:64] of sourcePortIdentity of PTP node.

47.6.1.104 ETH MAC Log Message Interval register (ETH_MACLOGMINTE)

Address offset: 0x0BD0

Reset value: 0x0000 0000

This register contains the periodic intervals for automatic PTP packet generation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LMPDRI								Reserved							
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DRSYNCR			LSI							
					rw			rw							

Bit Field	Name	Description
31:24	LMPDRI	Log Min Pdelay_Req Interval This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15. Negative value must be represented in 2's complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	Reserved	Reserved, the reset value must be maintained.
10:8	DRSYNCR	Delay_Req to SYNC Ratio In Slave mode, it is used for controlling frequency of Delay_Req messages transmitted. The master sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the slave. The ETH Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Slave mode, the host must not write/update this register unless it has to override the received value. In Master mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message.

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Bit Field	Name	Description
		Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. 0x0 (SYNC1): DelayReq generated for every received SYNC 0x1 (SYNC2): DelayReq generated every alternate reception of SYNC 0x2 (SYNC4): for every 4 SYNC messages 0x3 (SYNC8): for every 8 SYNC messages 0x4 (SYNC16): for every 16 SYNC messages 0x5 (SYNC32): for every 32 SYNC messages 0x6 (RSVD): Reserved
7:0	LSI	Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Master. Allowed values are -15 to 15. Negative value must be represented in 2's complement form. For example, if the required value is -1, the value programmed must be 0xFF.

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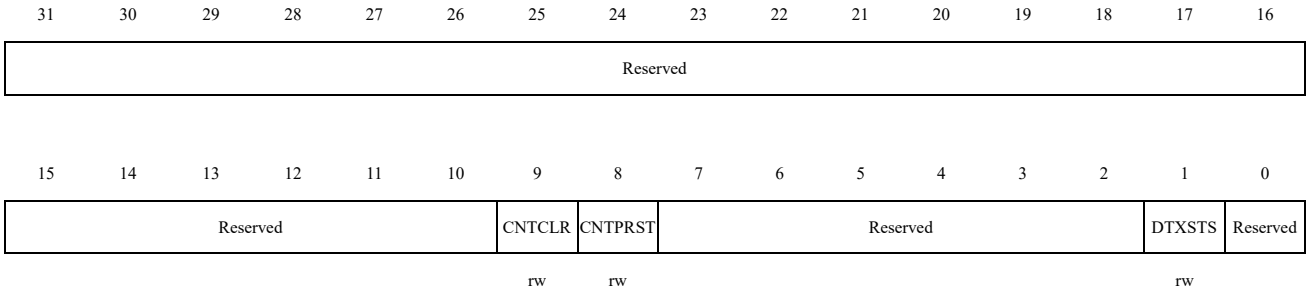
47.6.2 ETH MTL Registers

47.6.2.1 ETH MTL Operation Mode register (ETH_MTLOPMOD)

Address offset: 0x0C00

Reset value: 0x0000 0000

The Operation Mode register establishes the Transmit and Receive operating modes and commands.



Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	CNTCLR	Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNTPRST bit, CNTPRST has precedence. 0x0: Counters are not reset 0x1: All counters are reset *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*
8	CNTPRST	Counter Preset When this bit is set, ■ MTL TxQ Underflow register is initialized/preset to 12'h7F0. ■ Missed Packet and Overflow Packet counters in MTL RxQ Missed Packet Overflow Cnt register is initialized/preset to 12'h7F0. 0x0: Counters Preset is disabled 0x1: Counters Preset is enabled *Note: This bit has access restrictions, writing 1 is effective, automatically cleared, writing 0 has no effect.*
7:2	Reserved	Reserved, the reset value must be maintained.
1	DTXSTS	Drop Transmit Status ■ 1: Tx packet status received from the MAC is dropped in the MTL ■ 0: Tx packet status received from the MAC is forwarded to the application 0x0: Drop Transmit Status is disabled 0x1: Drop Transmit Status is enabled

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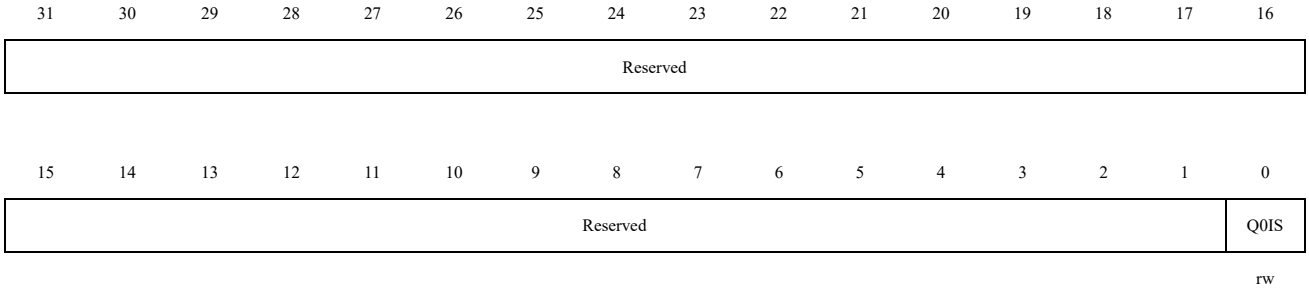
Bit Field	Name	Description
0	Reserved	Reserved, the reset value must be maintained.

47.6.2.2 ETH MTL Interrupt Status register (ETH_MTLINTSTS)

Address offset: 0x0C20

Reset value: 0x0000 0000

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.



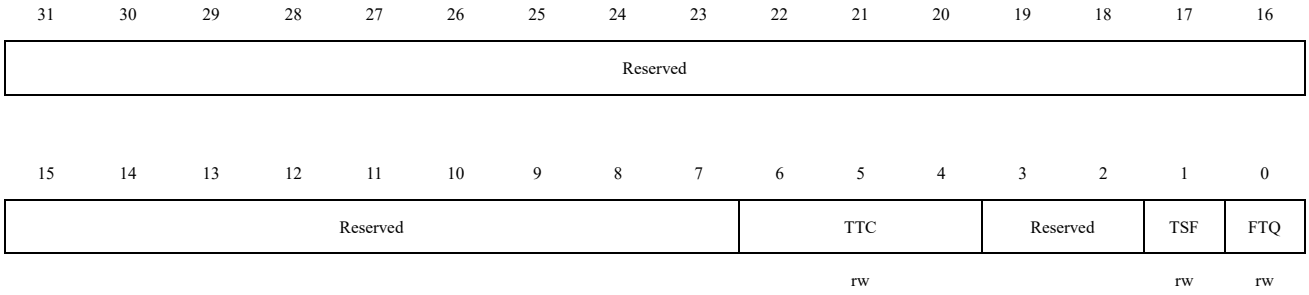
Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	Q0IS	Queue 0 Interrupt Status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. 0x0: Queue 0 Interrupt status not detected 0x1: Queue 0 Interrupt status detected

47.6.2.3 ETH MTL Tx Queue Operation Mode register (ETH_MTLTXQOPMOD)

Address offset: 0x0D00

Reset value: 0x0000 0000

This register establishes the Transmit queue operating modes and commands.



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Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6:4	TTC	Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. 0x0 (M_32BYTES): 32 0x1 (M_64BYTES): 64 0x2 (M_96BYTES): 96 0x3 (M_128BYTES): 128 0x4 (M_192BYTES): 192 0x5 (M_256BYTES): 256 0x6 (M_384BYTES): 384 0x7 (M_512BYTES): 512
3:2	Reserved	Reserved, the reset value must be maintained.
1	TSF	Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits [6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0x0: Transmit Store and Forward is disabled 0x1: Transmit Store and Forward is enabled
0	FTQ	Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL TxQ Operation Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0: Flush Transmit Queue is disabled 0x1: Flush Transmit Queue is enabled *Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active.*

47.6.2.4 ETH MTL Tx Queue Underflow register (ETH_MTLTXQUDF)

Address offset: 0x0D04

Reset value: 0x0000 0000

This register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				UFCNTOVF	UFFRMCNT										
				r	r										

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	UFCNTOVF	Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0: Overflow not detected for Underflow Packet Counter 0x1: Overflow detected for Underflow Packet Counter
10:0	UFFRMCNT	Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i [0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

47.6.2.5 ETH MTL Tx Queue Debug register (ETH_MTLTXQDBG)

Address offset: 0x0D08

Reset value: 0x0000 0000

This register gives the debug status of various blocks related to the Transmit queue.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									STXSTSF			Reserved	PTXQ		
										r				r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TXSTSFSTS	TXQSTS	TWCSTS	TRCSTS		TXQPAUSED
										r	r	r	r		r

Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22:20	STXSTSF	Number of Status Words in Tx Status FIFO of Queue

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Bit Field	Name	Description
		This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL Operation Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	Reserved	Reserved, the reset value must be maintained.
18:16	PTXQ	Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL Operation Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	Reserved	Reserved, the reset value must be maintained.
5	TXSTSFSTS	MTL Tx Status FIFO Full Status When this bit is set to 1, it indicates that the MTL Tx status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. 0: MTL Tx status FIFO full status is not detected 1: MTL Tx status FIFO full status is detected
4	TXQSTS	MTL Tx Queue Not Empty Status When this bit is set to 1, it indicates that the MTL Tx queue is not empty and some data is left for transmission. 0: MTL Tx queue not empty status is not detected 1: MTL Tx queue not empty status is detected
3	TWCSTS	MTL Tx Queue Write Controller Status When this bit is set to 1, it indicates that the MTL Tx queue write controller is active, and it is transferring the data to the Tx Queue 0: MTL Tx Queue Write Controller status is not detected 1: MTL Tx Queue Write Controller status is detected
2:1	TRCSTS	MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: 0x0 (IDLE): Idle state 0x1 (READ): Read state (transferring data to the MAC transmitter) 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC
0	TXQPAUSED	Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: ■ Reception of 802.3x Pause packet 0x0: Transmit Queue in Pause status is not detected 0x1: Transmit Queue in Pause status is detected

47.6.2.6 ETH MTL Queue Interrupt Control Status register (ETH_MTLQINTCTRLSTS)

Address offset: 0x0D2C

Reset value: 0x0000 0000

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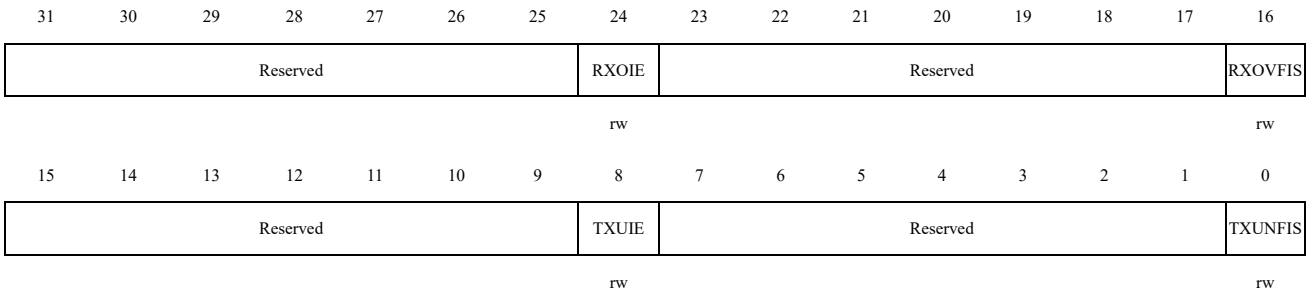
This register contains the interrupt enable and status bits for the queue interrupts.



Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	RXOIE	Receive Queue Overflow Interrupt Enable 0x0: Receive Queue Overflow Interrupt is disabled 0x1: Receive Queue Overflow Interrupt is enabled
23:17	Reserved	Reserved, the reset value must be maintained.
16	RXOVFIS	Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3 [21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected
15:9	Reserved	Reserved, the reset value must be maintained.
8	TXUIE	Transmit Queue Underflow Interrupt Enable 0x0: Transmit Queue Underflow Interrupt Status is disabled 0x1: Transmit Queue Underflow Interrupt Status is enabled
7:1	Reserved	Reserved, the reset value must be maintained.
0	TXUNFIS	Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3 [2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Transmit Queue Underflow Interrupt Status not detected 0x1: Transmit Queue Underflow Interrupt Status detected

47.6.2.7 ETH MTL Rx Queue Operation Mode register (ETH_MTLRXQOPMOD)

Address offset: 0x0D30

Reset value: 0x0000 0000

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This register establishes the Receive queue operating modes and command.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									DISTCPEF	RSF	FEP	FUP	Reserved	RTC	
									rw	rw	rw	rw		rw	

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	DISTCPEF	Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. 0x0: Dropping of TCP/IP Checksum Error Packets is enabled 0x1: Dropping of TCP/IP Checksum Error Packets is disabled
5	RSF	Receive Queue Store and Forward When this bit is set, the Ethernet peripheral reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. 0x0: Receive Queue Store and Forward is disabled 0x1: Receive Queue Store and Forward is enabled
4	FEP	Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA. 0x0: Forward Error Packets is disabled 0x1: Forward Error Packets is enabled
3	FUP	Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is

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Bit Field	Name	Description
		reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. 0x0: Forward Undersized Good Packets is disabled 0x1: Forward Undersized Good Packets is enabled
2	Reserved	Reserved, the reset value must be maintained.
1:0	RTC	Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. 0x0 (M_64BYTE): 64 0x1 (M_32BYTE): 32 0x2 (M_96BYTE): 96 0x3 (M_128BYTE): 128

47.6.2.8 ETH MTL Rx Queue Missed Packet Overflow Cnt register (ETH_MTLRXQMPOFCNT)

Address offset: 0x0D34

Reset value: 0x0000 0000

This register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				MISCNTOVF	MISPKTCNT										
				r	r										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OVFCNTOVF	OVFPKTCNT										
				r	r										

Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	MISCNTOVF	Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. 0x0: Missed Packet Counter overflow not detected 0x1: Missed Packet Counter overflow detected *Note: This Bit Field has access restrictions. Read-clear. Automatically set to 1 during*

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Bit Field	Name	Description
		internal events.
26:16	MISPKTCNT	Missed Packet Counter This field indicates the number of packets that the Ethernet peripheral has missed due to a packet flush request by the application for that queue. This counter is reset when a read operation is performed on this register. The counter is incremented when the DMA discards packets due to unavailable buffers. *Note: This Bit Field has access restrictions. Read-clear. Automatically set to 1 during internal events.*
15:12	Reserved	Reserved, the reset value must be maintained.
11	OVFCNTOVF	Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. 0: Overflow counter overflow not detected 1: Overflow counter overflow detected *Note: This bit has access restrictions. Read-clear. Automatically set to 1 during internal events.*
10:0	OVFPKTCNT	Overflow Packet Counter This field indicates the number of packets that the Ethernet peripheral has discarded due to an overflow in the receive queue. Each time the Ethernet peripheral discards an incoming packet due to overflow, the value of this counter is incremented. This counter is reset when a read operation is performed on this register. *Note: This Bit Field has access restrictions. Read-clear. Automatically set to 1 during internal events.*

47.6.2.9 ETH MTL Rx Queue Debug register (ETH_MTLRXQDBG)

Address offset: 0x0D38

Reset value: 0x0000 0000

This register gives the debug status of various blocks related to the Receive queue.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		PRXQ													
		r													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										RXQSTS		Reserved	RRCSTS		RWCSTS
										r			r		r

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29:16	PRXQ	Number of Packets in Receive Queue

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Bit Field	Name	Description
		This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	Reserved	Reserved, the reset value must be maintained.
5:4	RXQSTS	MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: 0x0 (EMPTY): Rx Queue empty 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold 0x3 (FULL): Rx Queue full
3	Reserved	Reserved, the reset value must be maintained.
2:1	RRCSTS	MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: 0x0 (IDLE): Idle state 0x1 (READ_DATA): Reading packet data 0x2 (READ_STS): Reading packet status (or timestamp) 0x3 (FLUSH): Flushing the packet data and status
0	RWCSTS	MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. 0x0: MTL Rx Queue Write Controller Active Status not detected 0x1: MTL Rx Queue Write Controller Active Status detected

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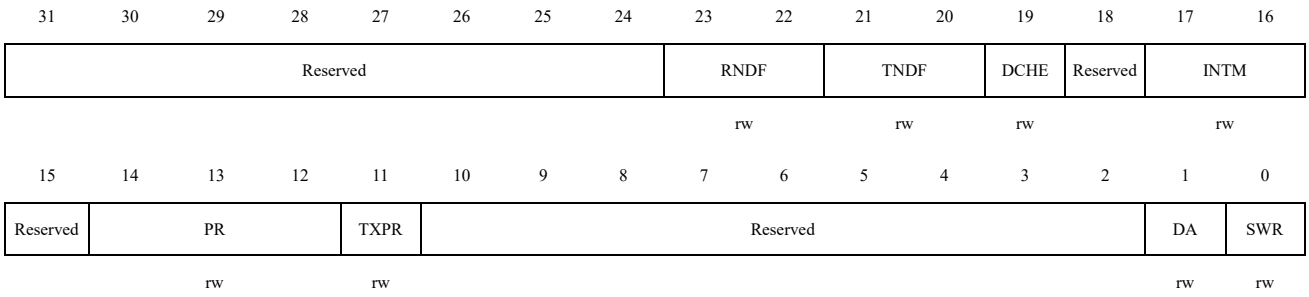
47.6.3 ETH DMA Registers

47.6.3.1 ETH DMA Mode register (ETH_DMAMODE)

Address offset: 0x1000

Reset value: 0x0000 0000

The Bus Mode register establishes the bus operating modes for the DMA.



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:22	RNDF	Rx DMA's Maximum Number of Descriptors to be fetched in a burst 00: 4 01: 2 10: 1 11: Reserved
21:20	TNDF	Tx DMA’s Maximum Number of Descriptors to be fetched in a burst 00: 4 01: 2 10: 1 11: Reserved
19	DCHE	Descriptor Cache Enable When set enables prefetching of descriptors to the Descriptor Cache. When reset descriptor cache feature is disabled. 0x0: Descriptor Cache Support is disabled 0x1: Descriptor Cache Support is enabled
18	Reserved	Reserved, the reset value must be maintained.
17:16	INTM	Interrupt Mode This field defines the interrupt mode of Ethernet peripheral. The behavior of the following outputs change depending on the following settings: ■ sbd_perch_tx_intr_o (Transmit Per Channel Interrupt) ■ sbd_perch_rx_intr_o (Receive Per Channel Interrupt) ■ sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA CH0 Status register.

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Bit Field	Name	Description
		00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 11: Reserved For more details, see Table 47-60.
15	Reserved	Reserved, the reset value must be maintained.
14:12	PR	Priority Ratio These bits control the priority ratio in weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when the DA bit is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether the TXPR bit is reset or set. 0x0 (R_1_1): The priority ratio is 1:1 0x1 (R_2_1): The priority ratio is 2:1 0x2 (R_3_1): The priority ratio is 3:1 0x3 (R_4_1): The priority ratio is 4:1 0x4 (R_5_1): The priority ratio is 5:1 0x5 (R_6_1): The priority ratio is 6:1 0x6 (R_7_1): The priority ratio is 7:1 0x7 (R_8_1): The priority ratio is 8:1
11	TXPR	Transmit Priority When set, this bit indicates that the Tx DMA has higher priority than the Rx DMA during arbitration for the system-side bus or Descriptor reads from DCACHE memory. 0x0: Transmit Priority is disabled 0x1: Transmit Priority is enabled
10:2	Reserved	Reserved, the reset value must be maintained.
1	DA	DMA Tx or Rx Arbitration Scheme This bit specifies the arbitration scheme between the Transmit and Receive paths of all channels: 0: Weighted Round-Robin with Rx:Tx or Tx:Rx. The priority between the paths is according to the priority specified in Bits [14:12] and the priority weight is specified in the TXPR bit. 1: Fixed Priority. The Tx path has priority over the Rx path when the TXPR bit is set. Otherwise, the Rx path has priority over the Tx path.

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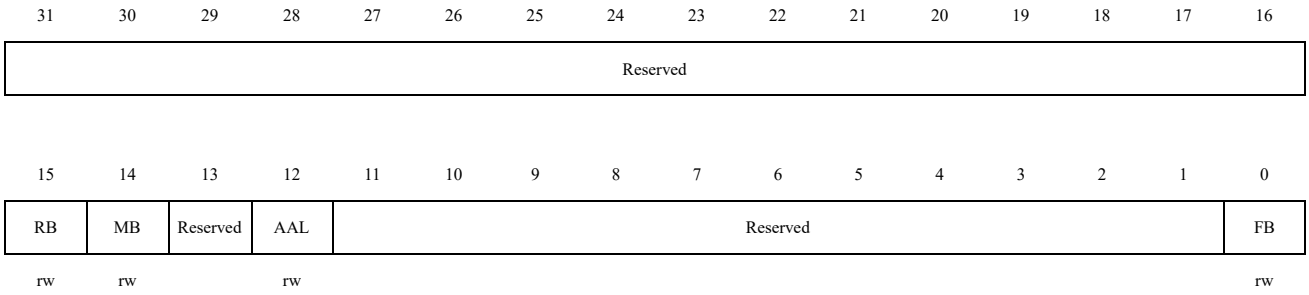
Bit Field	Name	Description
0	SWR	Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all Ethernet peripheral clock domains. Before reprogramming any Ethernet peripheral register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0x0: Software Reset is disabled 0x1: Software Reset is enabled *Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.*

47.6.3.2 ETH DMA System Bus Mode register (ETH_DMASBMODE)

Address offset: 0x1004

Reset value: 0x0000 0000

The System Bus mode register controls the behavior of the AHB master. It mainly controls burst splitting and number of outstanding requests.



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	RB	Rebuild INCRx Burst When this bit is set high and the AHB master gets SPLIT, RETRY, or Early Burst Termination (EBT) response, the AHB master interface rebuilds the pending beats of any initiated burst transfer with INCRx and SINGLE transfers. By default, the AHB master interface rebuilds the pending beats of an EBT with an unspecified (INCR) burst. 0x0: Rebuild INCRx Burst is disabled 0x1: Rebuild INCRx Burst is enabled
14	MB	Mixed Burst

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Bit Field	Name	Description
		When this bit is high and the FB bit is low, the AHB master performs undefined bursts transfers (INCR) for burst length of 16 or more. For burst length of 16 or less, the AHB master performs fixed burst transfers (INCRx and SINGLE). 0x0: Mixed Burst is disabled 0x1: Mixed Burst is enabled
13	Reserved	Reserved, the reset value must be maintained.
12	AAL	Address-Aligned Beats When this bit is set to 1, the AHB master performs address-aligned burst transfers on Read and Write channels. When this bit is set to 0, the AHB master performs burst transfers on Read and Write channels without aligning to address boundaries. 0x0: Address-Aligned Beats is disabled 0x1: Address-Aligned Beats is enabled
11:1	Reserved	Reserved, the reset value must be maintained.
0	FB	Fixed Burst Length 0: AHB master initiates transfers of unspecified length (INCR) or SINGLE transfers. 1: AHB master initiates burst transfers of specified length (INCRx or SINGLE).

47.6.3.3 ETH DMA Interrupt Status register (ETH_DMAINTSTS)

Address offset: 0x1008

Reset value: 0x0000 0000

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														MACIS	MTLIS
														r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															DC0IS
															r

Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	MACIS	MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. 0x0: MAC Interrupt Status not detected 0x1: MAC Interrupt Status detected

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Bit Field	Name	Description
16	MTLIS	MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. 0x0: MTL Interrupt Status not detected 0x1: MTL Interrupt Status detected
15:1	Reserved	Reserved, the reset value must be maintained.
0	DC0IS	DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. 0x0: DMA Channel 0 Interrupt Status not detected 0x1: DMA Channel 0 Interrupt Status detected

47.6.3.4 ETH DMA Debug Status register (ETH_DMADBGSTS)

Address offset: 0x100C

Reset value: 0x0000 0000

The Debug Status register gives the Receive and Transmit process status for DMA Channel 0 for debugging purpose.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0				RPS0				Reserved							AHBMS
r				r											r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:12	TPS0	DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued) 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor) 0x2 (RUN_WS): Running (Waiting for status) 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 0x4 (TSTMP_WS): Timestamp write state 0x5 (RSVD): Reserved for future use 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow)

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Bit Field	Name	Description
		0x7 (RUN_CTD): Running (Closing Tx Descriptor)
11:8	RPS0	DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. 0x0 (STOP): Stopped (Reset or Stop Receive Command issued) 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor) 0x2 (RSVD): Reserved for future use 0x3 (RUN_WRP): Running (Waiting for Rx packet) 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable) 0x5 (RUN_CRD): Running (Closing the Rx Descriptor) 0x6 (TSTMP): Timestamp write state 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory)
7:1	Reserved	Reserved, the reset value must be maintained.
0	AHBMS	AHB Master Status When high, this bit indicates that the AHB master FSMs are in the non-idle state. 0x0: AHB Master Status not detected 0x1: AHB Master Status detected

47.6.3.5 ETH DMA CH0 Control register (ETH_DMACH0CTRL)

Address offset: 0x1100

Reset value: 0x0000 0000

This register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											DSL			Reserved	PBLx8
												rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		MSS													
		rw													

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:18	DSL	Descriptor Skip Length This bit specifies the Word (32-bits) number to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as

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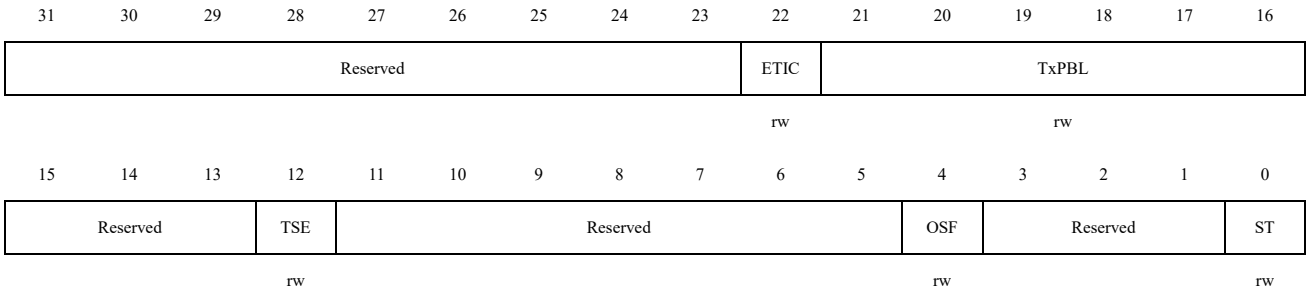
Bit Field	Name	Description
		contiguous.
17	Reserved	Reserved, the reset value must be maintained.
16	PBLx8	8xPBL mode When this bit is set, the PBL value programmed in Bits [21:16] in DMA CH0 Tx Control register and Bits [21:16] in DMA CH0 Rx Control register is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.
15:14	Reserved	Reserved, the reset value must be maintained.
13:0	MSS	Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA CH0 Tx Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

47.6.3.6 ETH DMA CH0 Tx Control register (ETH_DMACH0TXCTRL)

Address offset: 0x1104

Reset value: 0x0000 0000

This register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.



Bit Field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained.
22	ETIC	Early Transmit Interrupt Control When this bit is set, Early Transmit Interrupt (ETI) status is set after completion of transfer of data from buffers of a transmit descriptor in which IOC bit (TDES2 [31]) is set. When this bit is reset, ETI is set only after a complete packet is transferred to the MTL TX FIFO memory. 0x0: Early Transmit Interrupt is disabled 0x1: Early Transmit Interrupt is enabled
21:16	TxPBL	Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block

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Bit Field	Name	Description
		data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1 Set the 8xPBL mode in DMA CH0 Control register. 2 Set the TxPBL.
15:13	Reserved	Reserved, the reset value must be maintained.
12	TSE	TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0 [19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0: TCP Segmentation is disabled 0x1: TCP Segmentation is enabled
11:5	Reserved	Reserved, the reset value must be maintained.
4	OSF	Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0: Operate on Second Packet disabled 0x1: Operate on Second Packet enabled
3:1	Reserved	Reserved, the reset value must be maintained.
0	ST	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: ■ The current position in the list. This is the base address of the Transmit list set by the DMA CH0 TxDesc List Address register. ■ The position at which the transmission was previously stopped. If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA CH0 Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA CH0 TxDesc List Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA CH0 TxDesc List Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state.

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Bit Field	Name	Description
		0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command

47.6.3.7 ETH DMA CH0 Rx Control register (ETH_DMACH0RXCTRL)

Address offset: 0x1108

Reset value: 0x0000 0000

This register controls the Rx features such as PBL, buffer size, and extended status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RPF	Reserved								ERIC	RxPBL					
rw									rw	rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	RBSZH												RBSZL		SR
	rw												r		rw

Bit Field	Name	Description
31	RPF	Rx Packet Flush 1: Ethernet automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, are flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing is done on the Read side of the Rx Queue. 0: Ethernet does not flush the packet in the Rx Queue destined to this RxDMA Channel when it is in STOP state. This might cause head-of-line blocking in the corresponding RxQueue. 0x0: Rx Packet Flush is disabled 0x1: Rx Packet Flush is enabled
30:23	Reserved	Reserved, the reset value must be maintained.
22	ERIC	Early Receive Interrupt Control When this bit is set, Early Receive Interrupt (ERI) status is set after the completion of every burst transfer of data from the Rx DMA to the buffer. When this bit is reset, ERI is set only after a complete buffer is filled up by the RxDMA. 0x0: Early Receive Interrupt is disabled 0x1: Early Receive Interrupt is enabled
21:16	RxPBL	Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it

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Bit Field	Name	Description
		starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1 Set the 8xPBL mode in the DMA CH0 Control register. 2 Set the RxPBL.
15	Reserved	Reserved, the reset value must be maintained.
14:3	RBSZH	Receive Buffer Size High RBSZ [13:0] is split into two fields higher RBSZH and lower RBSZL. The RBSZ [13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. *Note: The buffer size must be a multiple of 4 depending on the data bus widths (32-bit). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZL bits are read-only and the value is considered as all-zero. Thus the RBSZH indicates the buffer size in terms of locations (with the width same as bus-width).*
2:1	RBSZL	Receive Buffer Size Low RBSZ [13:0] is split into two fields RBSZH and RBSZL. The RBSZL is the lower field whose width is based on data bus width of the configuration. This field is read-only (RO).
0	SR	Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: ■ The current position in the list. This is the address set by the DMA CH0 RxDesc List Address register. ■ The position at which the Rx process was previously stopped. If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA CH0 Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA CH0 RxDesc List Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive 0x1 (START): Start Receive

47.6.3.8 ETH DMA CH0 TxDesc List Address register (ETH_DMACH0TXDLA)

Address offset: 0x1114

Reset value: 0x0000 0000

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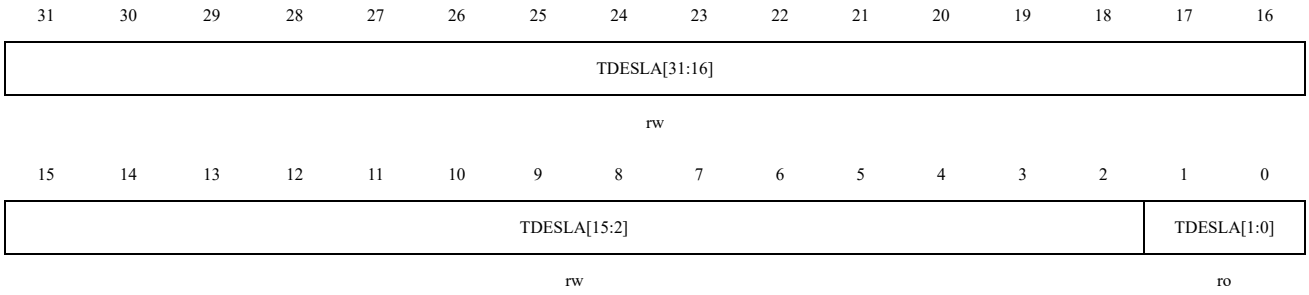
This register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word-aligned (for 32-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low.

You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA CH0 Tx Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.



Bit Field	Name	Description
31:0	TDESLA	Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0) for 32-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO).

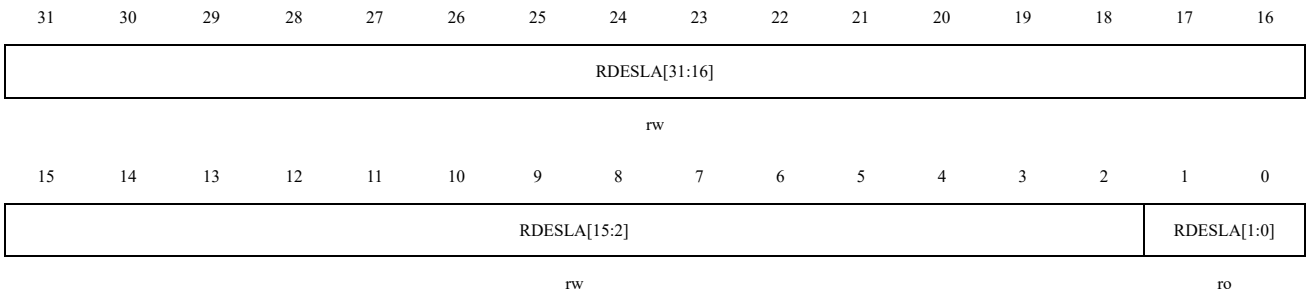
47.6.3.9 ETH DMA CH0 RxDesc List Address register (ETH_DMACH0RXDLA)

Address offset: 0x111C

Reset value: 0x0000 0000

This register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word-aligned (for 32-bit data bus). The DMA internally converts it to bus width aligned address by making the corre-sponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given.

You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA CH0 Rx Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.



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Bit Field	Name	Description
31:0	RDESLA	Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0) for 32-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO).

47.6.3.10 ETH DMA CH0 TxDesc Tail Pointer register (ETH_DMACH0TXDTP)

Address offset: 0x1120

Reset value: 0x0000 0000

This register points to an offset from the base and indicates the location of the last valid descriptor.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDTP[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDTP[15:2]														TDTP[1:0]	
rw														ro	

Bit Field	Name	Description
31:0	TDTP	Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. *Note: The LSB bits (1:0) are read-only (RO).*

47.6.3.11 ETH DMA CH0 RxDesc Tail Pointer register (ETH_DMACH0RXDTP)

Address offset: 0x1128

Reset value: 0x0000 0000

This register points to an offset from the base and indicates the location of the last valid descriptor

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDTP[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDTP[15:2]														RDTP[1:0]	
rw														ro	

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Bit Field	Name	Description
31:0	RDTP	Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. *Note: The LSB bits (1:0) are read-only (RO).*

47.6.3.12 ETH DMA CH0 TxDesc Ring Length register (ETH_DMACH0TXDRLEN)

Address offset: 0x112C

Reset value: 0x0000 0000

This register contains the length of the Transmit descriptor ring.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						TDRL									
						rw									

Bit Field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9:0	TDRL	Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Synopsys recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

47.6.3.13 ETH DMA CH0 Rx Control register 2 (ETH_DMACH0RXCTRL2)

Address offset: 0x1130

Reset value: 0x0000 0000

This register controls the Rx features such as Rx Descriptor Ring Length and Alternate Rx Buffer Size.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								ARBS							
								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Reserved	RDRL
	rw

Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:16	ARBS	Alternate Receive Buffer Size Indicates size in bytes for Buffer 1 when ARBS is programmed to a non-zero value (when split header feature is not enabled). When split header feature is enabled, ARBS indicates the buffer size for header data. The maximum alternate buffer is limited to 1020-bytes depending on the data bus widths (32-bit). When ARBS=0, Rx Buffer1 and Rx Buffer2 sizes are based on RBSZ field of DMA CH0 Rx Control register.
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	RDRL	Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

47.6.3.14 ETH DMA CH0 Interrupt Enable register (ETH_DMACH0INTEN)

Address offset: 0x1134

Reset value: 0x0000 0000

This register enables the interrupts reported by the Status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NIE	AIE	CDEE	FBEE	ERIE	ETIE	RWTE	RSE	RBUE	RIE	Reserved			TBUE	TXSE	TIE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	NIE	Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA CH0 Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt

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Bit Field	Name	Description
		Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0: Normal Interrupt Summary is disabled 0x1: Normal Interrupt Summary is enabled
14	AIE	Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA CH0 Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0: Abnormal Interrupt Summary is disabled 0x1: Abnormal Interrupt Summary is enabled
13	CDEE	Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0: Context Descriptor Error is disabled 0x1: Context Descriptor Error is enabled
12	FBEE	Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0: Fatal Bus Error is disabled 0x1: Fatal Bus Error is enabled
11	ERIE	Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0: Early Receive Interrupt is disabled 0x1: Early Receive Interrupt is enabled
10	ETIE	Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0: Early Transmit Interrupt is disabled 0x1: Early Transmit Interrupt is enabled
9	RWTE	Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0: Receive Watchdog Timeout is disabled 0x1: Receive Watchdog Timeout is enabled

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Bit Field	Name	Description
8	RSE	Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. 0x0: Receive Stopped is disabled 0x1: Receive Stopped is enabled
7	RBUE	Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0: Receive Buffer Unavailable is disabled 0x1: Receive Buffer Unavailable is enabled
6	RIE	Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0: Receive Interrupt is disabled 0x1: Receive Interrupt is enabled
5:3	Reserved	Reserved, the reset value must be maintained.
2	TBUE	Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0: Transmit Buffer Unavailable is disabled 0x1: Transmit Buffer Unavailable is enabled
1	TXSE	Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0: Transmit Stopped is disabled 0x1: Transmit Stopped is enabled
0	TIE	Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0: Transmit Interrupt is disabled 0x1: Transmit Interrupt is enabled

47.6.3.15 ETH DMA CH0 Rx Interrupt Watchdog Timer register (ETH_DMACH0RXINTWT)

Address offset: 0x1138

Reset value: 0x0000 0000

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA CH0 Status register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														RWTU	

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Teleteck Park, East Wing, Singapore 117674
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rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RWT							
								rw							

Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17:16	RWTU	Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	RWT	Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA CH 0 Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3 [30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3 [30] of any received packet.

47.6.3.16 ETH DMA CH0 Current App TxDesc register (ETH_DMACH0CATXD)

Address offset: 0x1144

Reset value: 0x0000 0000

This register points to the current Transmit descriptor read by the DMA.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURTDESAPTR[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURTDESAPTR[15:0]															
r															

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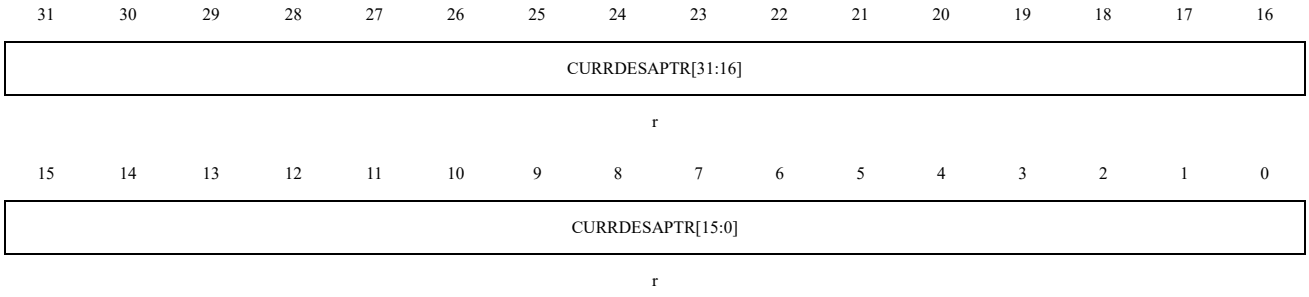
Bit Field	Name	Description
31:0	CURTDESAPTR	Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

47.6.3.17 ETH DMA CH0 Current App RxDesc register (ETH_DMACH0CARXD)

Address offset: 0x114C

Reset value: 0x0000 0000

This register points to the current Receive descriptor read by the DMA.



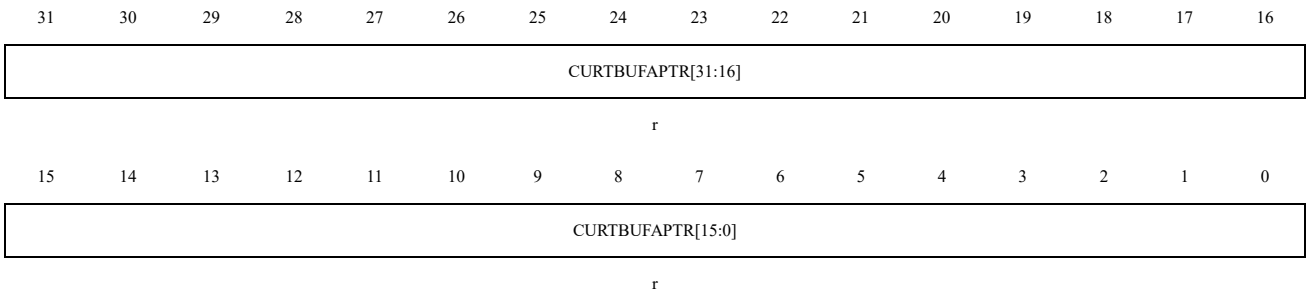
Bit Field	Name	Description
31:0	CURRDESAPTR	Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

47.6.3.18 ETH DMA CH0 Current App TxBuffer register (ETH_DMACH0CATXB)

Address offset: 0x1154

Reset value: 0x0000 0000

This register points to the current Tx buffer address read by the DMA.



Bit Field	Name	Description
31:0	CURTBUFAPTR	Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

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47.6.3.19 ETH DMA CH0 Current App RxBuffer register (ETH_DMACH0CARXB)

Address offset: 0x115C

Reset value: 0x0000 0000

This register points to the current Rx buffer address read by the DMA.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURRBUFAPTR[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRBUFAPTR[15:0]															
r															

Bit Field	Name	Description
31:0	CURRBUFAPTR	Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

47.6.3.20 ETH DMA CH0 Status register (ETH_DMACH0STS)

Address offset: 0x1160

Reset value: 0x0000 0000

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										REB			TEB		
										r			r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NIS	AIS	CDE	FBE	ERI	ETI	RWT	RPS	RBU	RI	Reserved			TBU	TPS	TI
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw				rw	rw	rw

Bit Field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21:19	REB	Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB interface. ■ Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA

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Bit Field	Name	Description
		■ Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access ■ Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	TEB	Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB interface. ■ Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA ■ Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access ■ Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	NIS	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA CH0 Interrupt Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA CH0 Interrupt Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Normal Interrupt Summary status not detected 0x1: Normal Interrupt Summary status detected
14	AIS	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA CH0 Interrupt Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable

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Bit Field	Name	Description
		Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Abnormal Interrupt Summary status not detected 0x1: Abnormal Interrupt Summary status detected
13	CDE	Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Context Descriptor Error status not detected 0x1: Context Descriptor Error status detected
12	FBE	Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Fatal Bus Error status not detected 0x1: Fatal Bus Error status detected
11	ERI	Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configurations supporting ERIC: ■ ERIC = 0: This bit is set only after the Rx DMA has completely filled up a receive buffer with packet data. ■ ERIC = 1: This bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Early Receive Interrupt status not detected 0x1: Early Receive Interrupt status detected
10	ETI	Early Transmit Interrupt

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Bit Field	Name	Description
		This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configurations supporting ERIC: ■ ETIC = 0: This bit is set only after the Tx DMA has transferred a complete packet to MTL. ■ ETIC = 1: This bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC = 1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Early Transmit Interrupt status not detected 0x1: Early Transmit Interrupt status detected
9	RWT	Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Receive Watchdog Timeout status not detected 0x1: Receive Watchdog Timeout status detected
8	RPS	Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Receive Process Stopped status not detected 0x1: Receive Process Stopped status detected
7	RBU	Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Receive Buffer Unavailable status not detected 0x1: Receive Buffer Unavailable status detected
6	RI	Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state.

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Bit Field	Name	Description
		Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Receive Interrupt status not detected 0x1: Receive Interrupt status detected
5:3	Reserved	Reserved, the reset value must be maintained.
2	TBU	Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA Debug Status register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: ■ Change the ownership of the descriptor by setting Bit 31 of TDES3. ■ Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Transmit Buffer Unavailable status not detected 0x1: Transmit Buffer Unavailable status detected
1	TPS	Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Transmit Process Stopped status not detected 0x1: Transmit Process Stopped status detected
0	TI	Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0: Transmit Interrupt status not detected 0x1: Transmit Interrupt status detected

47.6.3.21 ETH DMA CH0 Miss Frame Counter register (ETH_DMACH0DPCNT)

Address offset: 0x1164

Reset value: 0x0000 0000

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA CH0 Rx Control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPCO	Reserved				DPC										
r					r										

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	DPCO	Overflow status of the DPC Counter When this bit is set then the DPC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.
14:11	Reserved	Reserved, the reset value must be maintained.
10:0	DPC	Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA CH0 Rx Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

47.6.3.22 ETH DMA CH0 RX ERI Counter register (ETH_DMACH0RXERICNT)

Address offset: 0x116C

Reset value: 0x0000 0000

This register provides the count of the number of times ERI was asserted.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				ECNT											
				r											

Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	ECNT	ERI Counter When ERIC bit of DMA CH0 RX Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet.

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48 EtherCAT Slave Controller (ESC)

The EtherCAT Slave Controller (ESC) IP core is licensed from Beckhoff Automation GmbH, Germany. The company owns EtherCAT technology. More information about EtherCAT can be found on the EtherCAT Technology Group website (ETG, http://www.ethercat.org).

Note: Only N32H7x5EC series chips support the ESC module.

48.1 Introduction

The N32H7x5EC supports one EtherCAT Slave Controller (ESC). The ESC takes care of the EtherCAT communication as an interface between the EtherCAT fieldbus and the slave application. When using standard Ethernet packets or frames (according to IEEE 802.3) the ESC does not receive, interpret, and copy the process data at every node. Instead the ESC reads the data specifically addressed to it as the telegram passes through the device.

48.2 Main Features

The main features supported by ESC are shown below:

- 2 MII Ports to connect Ethernet PHYs
- 8 Fieldbus Memory Management Units (FMMU)
- 8 SyncManagers (SM)
- 8 Kbyte of Process Data Memory
- 64-bit Distributed Clocks (DC)
- On-chip bus as Process Data Interface (PDI)

48.3 Block Diagram

The N32H7x5EC slave controller contains a top-level wrapper. The block diagram of this wrapper is shown below:

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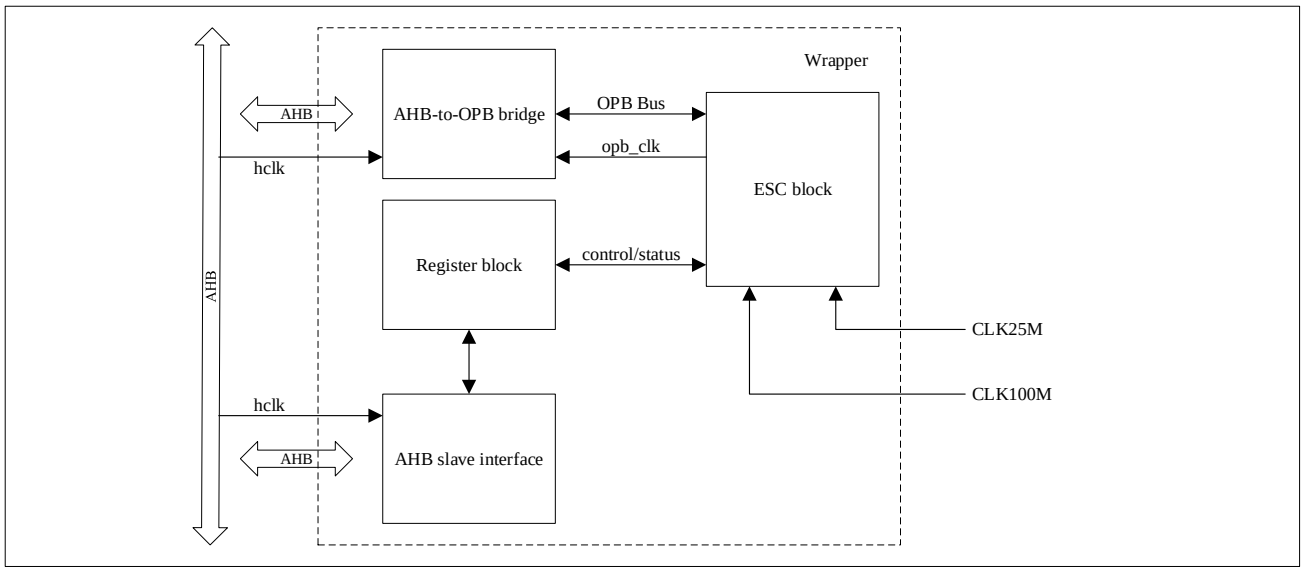
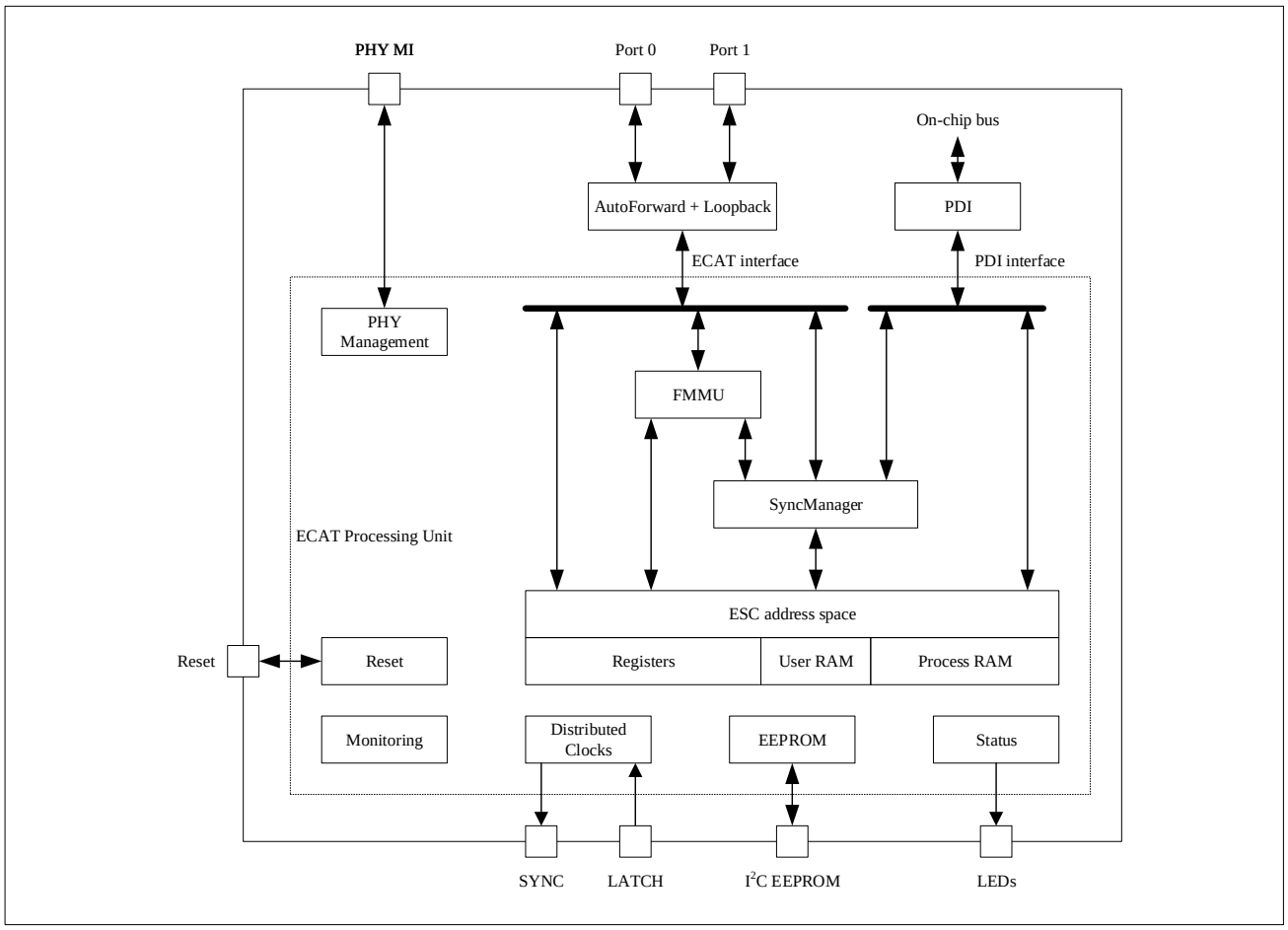
Figure 48-1 Top-level Wrapper Block Diagram



The general functionality of an ESC is shown in Figure 48-2.

Figure 48-2 ESC Block Diagram



EtherCAT Interfaces (Ethernet)

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The EtherCAT interfaces or ports connect the ESC to other EtherCAT slaves and an EtherCAT master. The MAC layer is integral part of the ESC. The physical layer is the same as Ethernet, external Ethernet PHYs connect to the MII ports of the ESC. Transmission speed for EtherCAT is fixed to 100 Mbit/s with Full Duplex communication. Link state and communication status are reported to the Monitoring device. EtherCAT slaves support 2 ports, the logical ports are numbered 0-1.

EtherCAT Processing Unit

The EtherCAT Processing Unit (EPU) receives, analyses and processes the EtherCAT data stream. It is logically located between port 0 and port 1. The main purpose of the EtherCAT Processing unit is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT master and from the local application via the PDI. Data exchange between master and slave application is comparable to a dual-ported memory (process memory), enhanced by special functions e.g. for consistency checking (Sync-Manager) and data mapping (FMMU). The EtherCAT Processing Units contains the main function blocks of EtherCAT slaves besides Auto-Forwarding, Loop-back function, and PDI.

Auto-Forwarder

The Auto-Forwarder receives the Ethernet frames, performs frame checking and forwards it to the Loop-back function. Time stamps of received frames are generated by the Auto-Forwarder.

Loop-back function

The Loop-back function forwards Ethernet frames to the next logical port if there is either no link at a port, or if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT Processing Unit. The loop settings can be controlled by the EtherCAT master.

FMMU

Fieldbus Memory Management Units are used for bitwise mapping of logical addresses to physical addresses of the ESC. Refer to section 48.5.5 for details.

SyncManager

SyncManagers are responsible for consistent data exchange and mailbox communication between EtherCAT master and slaves. The communication direction can be configured for each SyncManager. Read or write transactions may generate events for the EtherCAT master and an attached µController respectively. The SyncManagers are responsible for the main difference between and ESC and a dual-ported memory, because they map addresses to different buffers and block accesses depending on the SyncManager state. This is also a fundamental reason for bandwidth restrictions of the PDI. Refer to section 48.5.6 for details.

Monitoring

The Monitoring unit contains error counters and watchdogs. The watchdogs are used for observing communication and returning to a safe state in case of an error. Error counters are used for error detection and analysis. Refer to section 48.5.12 and section 48.5.13 for details.

PHY Management

The PHY Management unit communicates with Ethernet PHYs via the MII management interface. This is either used by the master or by the slave. The MII management interface is used by the ESC itself for optionally restarting auto negotiation after receive errors with the enhanced link detection mechanism, and for the MI link detection and

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configuration feature. Refer to section 48.5.4 for details.

Distributed Clock

Distributed Clocks (DC) allow for precisely synchronized generation of output signals and input sampling, as well as time stamp generation of events. The synchronization may span the entire EtherCAT network. Refer to section 48.5.9 for details.

Memory

The EtherCAT slave's addressable memory space consists of three parts. The first block of 4 Kbyte (0x0000-0x0FFF) is used for registers and user memory. The memory space from address 0x1000 onwards is used as the process memory (up to 8 Kbyte). Refer to section 48.5.9 for details.

SII EEPROM

One non-volatile memory is needed for EtherCAT Slave Information (ESI) storage, typically an I²C EEPROM. Refer to section 48.5.10 for details.

Status/LEDs

The Status block provides ESC and application status information. It controls external LEDs like the application RUN LED/ERR LED and port Link/Activity LEDs. Refer to section 48.5.14 for details.

48.4 Pin Definitions

Table 48-1 shows the pins used by ESC and their corresponding alternate functions.

Table 48-1 ESC Pin Definitions

Alternate Function	Pin Name	Description
ESC_P0_LINK	PE0, PE11, PK2	Port 0 EtherCAT PHY link status input pin, i.e. LINK_MII signal, see 48.5.4.2.1.1.
ESC_P0_MII_RX_CLK	PA1, PA1_C, PF5	Port 0 MII receive clock input pin.
ESC_P0_MII_RX_DV	PA0, PA0_C, PA7	Port 0 MII receive data valid input pin.
ESC_P0_MII_RX_ERR	PB10, PH3, PI10	Port 0 MII receive data error input pin.
ESC_P0_MII_RXD0	PC4, PF8	Port 0 MII receive data 0 to 3 input pins.
ESC_P0_MII_RXD1	PC5, PF9	
ESC_P0_MII_RXD2	PB0, PH6, PH10	
ESC_P0_MII_RXD3	PB1, PH7, PH11	
ESC_P0_MII_TX_CLK	PC3, PC3_C	Port 0 MII transmit clock input pin.
ESC_P0_MII_TX_EN	PB11, PG11	Port 0 MII transmit data enable output pin.
ESC_P0_MII_TXD0	PB12, PG13	Port 0 MII transmit data 0 to 3 output pins.
ESC_P0_MII_TXD1	PB13, PG12, PG14	
ESC_P0_MII_TXD2	PB7, PC2, PC2_C, PC10, PE3, PJ12	
ESC_P0_MII_TXD3	PC11, PE2, PJ13	
ESC_P1_LINK	PA2, PA6, PA10, PG8	Port 1 EtherCAT PHY link status input pin, i.e. LINK_MII signal, see 48.5.4.2.1.1.
ESC_P1_MII_RX_CLK	PA8, PF4, PJ4	Port 1 MII receive clock input pin.

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Alternate Function	Pin Name	Description
ESC_P1_MII_RX_DV	PC0, PH12, PJ3	Port 1 MII receive data valid input pin.
ESC_P1_MII_RX_ERR	PG6, PI3	Port 1 MII receive data error input pin.
ESC_P1_MII_RXD0	PG2, PG9, PI1	Port 1 MII receive data 0 to 3 input pins.
ESC_P1_MII_RXD1	PG3, PG10, PI2	
ESC_P1_MII_RXD2	PG4, PJ8	
ESC_P1_MII_RXD3	PG5, PJ9	
ESC_P1_MII_TX_CLK	PG0, PI8	Port 1 MII transmit clock input pin.
ESC_P1_MII_TX_EN	PF10, PF11, PH2, PH13	Port 1 MII transmit data enable output pin.
ESC_P1_MII_TXD0	PF12, PH4, PH14	Port 0 MII transmit data 0 to 3 output pins.
ESC_P1_MII_TXD1	PF13, PH5, PH15	
ESC_P1_MII_TXD2	PF14, PJ0	
ESC_P1_MII_TXD3	PF15, PJ1	
ESC_MDC	PC1, PC7, PE12, PF7	Management data clock output pin.
ESC_MDIO	PA2, PC6, PE13, PF6	Management data input/output pin.
ESC_RESET_IN	PE1, PI0, PI11	ESC reset signal input pin.
ESC_RESET_OUT	PC6, PD1, PD13	ESC reset signal output pin.
ESC_SYNC0	PA9, PD9, PI4	SYNC0 signal output pin.
ESC_SYNC1	PA12, PD5, PJ2	SYNC1 signal output pin.
ESC_LATCH0	PC0, PD11, PI9, PK7	LATCH0 signal input pin.
ESC_LATCH1	PD6, PI5, PK4	LATCH1 signal input pin.
ESC_EEPROM_CLK	PE5, PE8, PJ10	EEPROM I^2C clock signal output pin.
ESC_EEPROM_DATA	PE6, PE9, PJ11	EEPROM I^2C data signal input/output pin.
ESC_LED_RUN	PA4, PE15, PK1	ESC run LED signal output pin. See 48.5.14.1.
ESC_LED_ERR	PB2, PD0, PD8, PG15, PK0	ESC error LED signal output pin. See 48.5.14.2.
ESC_LED_STATE_RUN	PA5, PE4, PE10, PJ15	ESC Dual-color state LED signal output pin. See 48.5.14.3.
ESC_LINK_ACT0	PC12, PD12, PG15, PH2	ESC link/activity LED signal output pin. See 48.5.14.4.
ESC_LINK_ACT1	PA11, PD7, PI7	
ESC_IRQ	PC8, PD3, PI6, PJ5	ESC IRQ signal output pin.

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48.5 Function Description

48.5.1 EtherCAT Protocol

EtherCAT uses standard IEEE 802.3 Ethernet frames, thus a standard network controller can be used and no special hardware is required on master side.

EtherCAT has a reserved EtherType of 0x88A4 that distinguishes it from other Ethernet frames. Thus, EtherCAT can run in parallel to other Ethernet protocols. In this case, ESCs have to be configured to forward non-EtherCAT frames via DL Control register bit 0.

EtherCAT does not require the IP protocol, however it can be encapsulated in IP/UDP. The EtherCAT Slave Controller processes the frame in hardware. Thus, communication performance is independent from processor power.

An EtherCAT frame is subdivided into the EtherCAT frame header followed by one or more EtherCAT datagrams. At least one EtherCAT datagram has to be in the frame. Only EtherCAT frames with Type 1 in the EtherCAT Header are currently processed by the ESCs. The ESCs also support IEEE802.1Q VLAN Tags, although the VLAN Tag contents are not evaluated by the ESC.

If the minimum Ethernet frame size requirement isnot fulfilled, padding bytes have to be added. Otherwise the EtherCAT frame is exactly as large as the sum of all EtherCAT datagrams plus EtherCAT frame header.

48.5.1.1 EtherCAT Header

Figure 48-3 shows how an Ethernet frame containing EtherCAT data is assembled.

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Figure 48-3 Ethernet Frame with EtherCAT Data

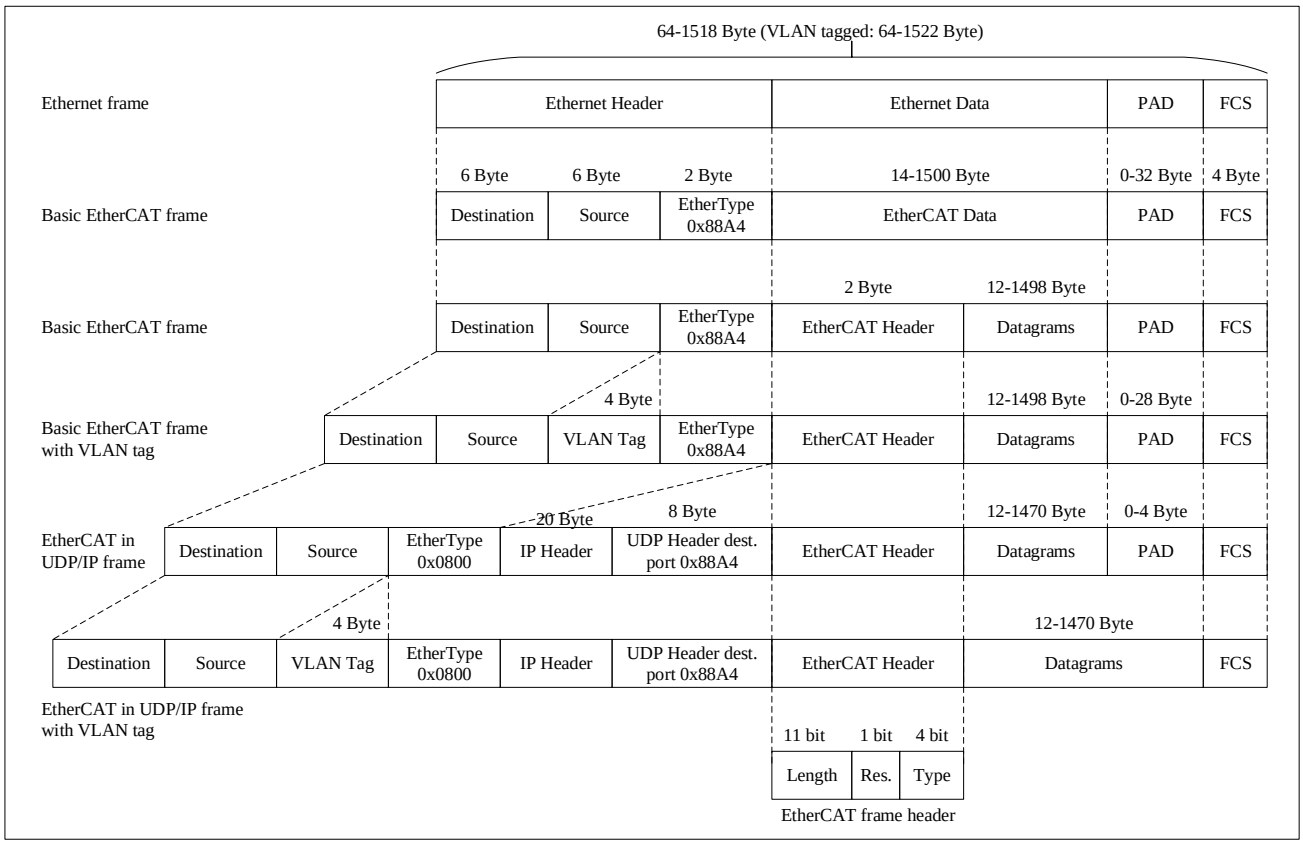

Table 48-2 shows the definition of each field of the EtherCAT frame header.

Table 48-2 EtherCAT Frame Header

Field	Length	Value/Description
Length	11 bit	Length of the EtherCAT datagrams (excl. FCS)
Res.	1 bit	Reserved, 0
Type	4 bit	Protocol type. Only EtherCAT commands (Type = 0x1) are supported by ESCs

NOTE: The EtherCAT header length field is ignored by ESCs, they rely on the datagram length fields.

48.5.1.2 EtherCAT Datagram

Table 48-3 shows the structure of an EtherCAT datagram.

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Figure 48-4 EtherCAT Datagram

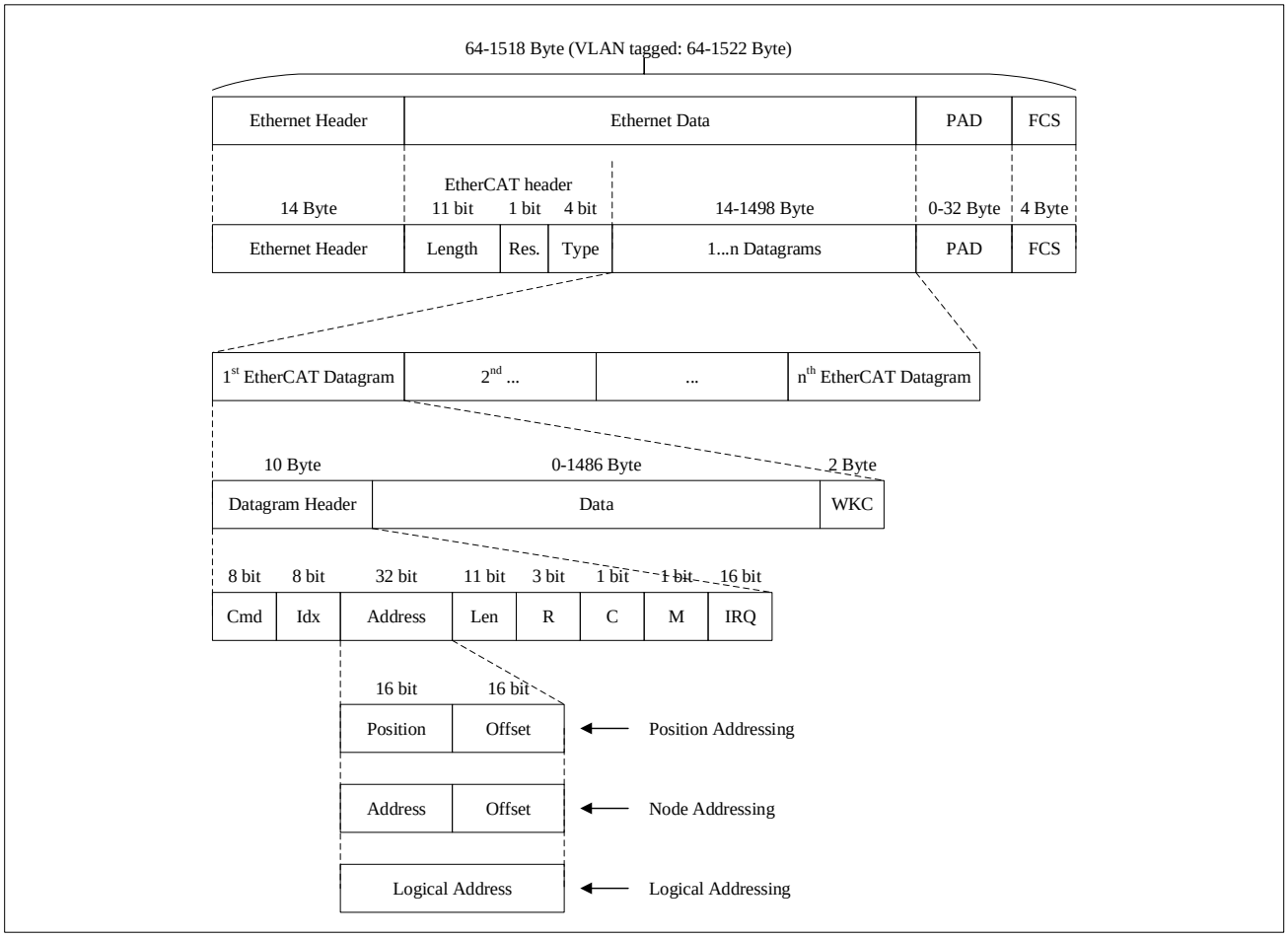

Table 48-4 shows the definition of each field of the EtherCAT datagram.

Table 48-3 EtherCAT Datagram

Field	Length	Value/Description
Cmd	8 bit	EtherCAT Command Type (see 48.5.1.5)
Idx	8 bit	The index is a numeric identifier used by the master for identification of duplicates/lost datagrams. It shall not be changed by EtherCAT slaves
Address	32 bit	Address (Auto Increment, Configured Station Address, or Logical Address, see 48.5.1.3)
Len	11 bit	Length of the following data within this datagram
R	3 bit	Reserved, 0
C	1 bit	Circulating frame (see 48.5.2.4): 0: Frame is not circulating 1: Frame has circulated once
M	1 bit	More EtherCAT datagrams 0: Last EtherCAT datagram 1: More EtherCAT datagrams will follow
IRQ	16 bit	EtherCAT Event Request registers of all slaves combined with a logical OR (see 48.5.11.2)
Data	n Byte	Read/Write Data

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Field	Length	Value/Description
WKC	2 Byte	Working Counter (see 48.5.1.4)

48.5.1.3 EtherCAT Addressing Modes

Two addressing modes of EtherCAT devices are supported within one segment: device addressing and logical addressing. Three device addressing modes are available: auto increment addressing, configured station address, and broadcast. EtherCAT devices can have up to two configured station addresses, one is assigned by the master (Configured Station Address), the other one is stored in the SII EEPROM and can be changed by the slave application (Configured Station Alias address). The EEPROM setting for the Configured Station Alias address is only taken over at the first EEPROM loading after power-on or reset.

48.5.1.3.1 Device Addressing

The device can be addressed via Device Position Address (Auto Increment address), by Node Address (Configured Station Address / Configured Station Alias), or by a Broadcast.

- Position Address / Auto Increment Address:

  The datagram holds the position address of the addressed slave as a negative value. Each slave increments the address. The slave which reads the address equal zero is addressed and will execute the appropriate command at receive.

  Position Addressing should only be used during start-up of the EtherCAT system to scan the fieldbus and later only occasionally to detect newly attached slaves. Using Position addressing is problematic if loops are closed temporarily due to hot connecting or link problems. Position addresses are shifted in this case, and e.g., a mapping of error register values to devices becomes impossible, thus the faulty link cannot be localized.

- Node Address /Configured Station Address and Configured Station Alias:

  The configured Station Address is assigned by the master during start up and cannot be changed by the EtherCAT slave. The Configured Station Alias address is stored in the SIl EEPROM and can be changed by the EtherCAT slave. The Configured Station Alias has to be enabled by the master. The appropriate command action will be executed if Node Address matches with either Configured Station Address or Configured Station Alias.

  Node addressing is typically used for register access to individual and already identified devices.

- Broadcast:

  Each EtherCAT slave is addressed.

  Broadcast addressing is used e.g. for initialization of all slaves and for checking the status of all slaves if they are expected to be identical.

Each slave device has a 16 bit local address space (offset address range 0x0000:0x0FFF is dedicated for EtherCAT registers, offset address range 0x1000:0xFFFF is used as process memory) which is addressed via the Offset field of the EtherCAT datagram. The process memory address space is used for application communication (e.g. mailbox access).

48.5.1.3.2 Logical Addressing

All devices read from and write to the same logical 4 Gbyte address space (32 bit address field within the EtherCAT datagram). A slave uses a mapping unit (FMMU, Fieldbus Memory Management Unit) to map data from the logical

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process data image to its local address space. During start up the master configures the FMMUs of each slave. The slave knows which parts of the logical process data image have to be mapped to which local address space using the configuration information of the FMMUs.

Logical Addressing supports bit wise mapping. Logical Addressing is a powerful mechanism to reduce the overhead of process data communication, thus it is typically used for accessing process data.

48.5.1.4 Working Counter

Every EtherCAT datagram ends with a 16 Bit Working Counter (WKC). The Working Counter counts the number of devices that were successfully addressed by this EtherCAT datagram. Successfully means that the ESC is addressed and the addressed memory is accessible (e.g., protected SyncManager buffer). EtherCAT Slave Controllers increment the Working Counter in hardware. Each datagram should have an expected Working Counter value calculated by the master. The master can check the valid processing of EtherCAT datagrams by comparing the Working Counter with the expected value.

The Working Counter is increased if at least one byte/one bit of the whole multi-byte datagram was successfully read and/or written. For a multi-byte datagram, you cannot tell from the Working Counter value if all or only one byte was successfully read and/or written. This allows reading separated register areas using a single datagram by ignoring unused bytes.

The Read-Multiple-Write commands ARMW and FRMW are either treated like a read command or like a write command, depending on the address match.

The following table shows the WKC increment under different commands.

Table 48-4 Working Counter Increment

Command	Condition	Increment
Read	No success	no change
	Successful read	+1
Write	No success	no change
	Successful write	+1
ReadWrite	No success	no change
	Successful read	+1
	Successful write	+2
	Successful read and write	+3

48.5.1.5 EtherCAT Command Types

All supported EtherCAT Command types are listed in Table 48-5. For ReadWrite operations, the Read operation is performed before the Write operation.

Table 48-5 EtherCAT Command Types

CMD	Abbr.	Name	Description
0	NOP	No Operation	Slave ignores command.
1	APRD	Auto Increment Read	Slave increments address. Slave puts read data into the EtherCAT datagram if received address is zero.
2	APWR	Auto Increment Write	Slave increments address. Slave writes data into memory location if

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CMD	Abbr.	Name	Description
			received address is zero.
3	APRW	Auto Increment Read Write	Slave increments address. Slave puts read data into the EtherCAT datagram and writes the data into the same memory location if received address is zero.
4	FPRD	Configured Address Read	Slave puts read data into the EtherCAT datagram if address matches with one of its configured addresses.
5	FPWR	Configured Address Write	Slave writes data into memory location if address matches with one of its configured addresses.
6	FPRW	Configured Address Read Write	Slave puts read data into the EtherCAT datagram and writes data into the same memory location if address matches with one of its configured addresses.
7	BRD	Broadcast Read	All slaves put logical OR of data of the memory area and data of the EtherCAT datagram into the EtherCAT datagram. All slaves increment position field.
8	BWR	Broadcast Write	All slaves write data into memory location. All slaves increment position field.
9	BRW	Broadcast Read Write	All slaves put logical OR of data of the memory area and data of the EtherCAT datagram into the EtherCAT datagram, and write data into memory location. BRW is typically not used. All slaves increment position field.
10	LRD	Logical Memory Read	Slave puts read data into the EtherCAT datagram if received address matches with one of the configured FMMU areas for reading.
11	LWR	Logical Memory Write	Slaves writes data to into memory location if received address matches with one of the configured FMMU areas for writing.
12	LRW	Logical Memory Read Write	Slave puts read data into the EtherCAT datagram if received address matches with one of the configured FMMU areas for reading. Slaves writes data to into memory location if received address matches with one of the configured FMMU areas for writing.
13	ARMW	Auto Increment Read Multiple Write	Slave increments address. Slave puts read data into the EtherCAT datagram if received address is zero, otherwise slave writes the data into memory location.
14	FRMW	Configured Read Multiple Write	Slave puts read data into the EtherCAT datagram if address matches with one of its configured addresses, otherwise slave writes the data into memory location.
15-255	Reserved		

48.5.2 Frame Processing

The N32H7x5EC slave controller only support Direct Mode addressing: neither a MAC address nor an IP address is assigned to the ESC, they process EtherCAT frames with any MAC or IP address.

It is not possible to use unmanaged switches between ESCs or between master and the first slave, because source and

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destination MAC addresses are not evaluated or exchanged by the ESCs. Only the source MAC address is modified when using the default settings, so outgoing and incoming frames can be distinguished by the master.

NOTE: Attaching an ESC directly to an office network will result in network flooding, since the ESC will reflect any frame – especially broadcast frames – back into the network (broadcast storm).

The frames are processed by the ESC on the fly, i.e., they are not stored inside the ESC. Data is read and written as the bits are passing the ESC. The forwarding delay is minimized to achieve fast cycle times. The forwarding delay is defined by the receive FIFO size and the EtherCAT Processing Unit delay. A transmit FIFO is omitted to reduce delay times.

The ESCs support EtherCAT, UDP/IP, and VLAN tags. EtherCAT frames and UDP/IP frames containing EtherCAT datagrams are processed. Frames with VLAN tags are processed by the ESCs, the VLAN settings are ignored and the VLAN tag is not modified.

The source MAC address is changed for every frame passing the EtherCAT Processing Unit (SOURCE_MAC[1] is set to 1 – locally administered address). This helps to distinguish between frames transmitted by the master and frames received by the master.

48.5.2.1 Loop Control and Loop State

Each port of an ESC can be in one of two states: open or closed. If a port is open, frames are transmitted to other ESCs at this port, and frames from other ESCs are received. A port which is closed will not exchange frames with other ESCs, instead, the frames are forwarded internally to the next logical port, until an open port is reached.

The loop state of each port can be controlled by the master (ESC DL Control register). The ESCs supports four loop control settings, two manual configurations, and two automatic modes:

Manual open

The port is open regardless of the link state. If there is no link, outgoing frames will be lost.

Manual close

The port is closed regardless of the link state. No frames will be sent out or received at this port, even if there is a link with incoming frames.

Auto

The loop state of each port is determined by the link state of the port. The loop is open if there is a link, and it is closed without a link.

Auto close (manual open)

The port is closed depending on the link state, i.e., if the link is lost, the loop will be closed (auto close). If the link is established, the loop will not be automatically opened, instead, it will remain closed (closed wait state). Typically, the port has to be opened by the master explicitly by writing the loop configuration again to the ESC DL Control register. This write access has to enter the ESC via a different open port. There is an additional fallback option for opening the port: if a valid Ethernet frame is received from the external link at the closed port in Auto close mode, it will also be opened after the CRC is received correctly. The content of the frame is not evaluated.

A port is considered open if the port is available, i.e., it is enabled in the configuration, and one of the following conditions is met:

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- The loop setting in the DL Control register is Auto and there is an active link at the port.
- The loop setting in the DL Control register is Auto close and there is an active link at the port and the DL Control register was written again after the link was established.
- The loop setting in the DL Control register is Auto close and there is an active link at the port and a valid frame was received at this port after the link was established.
- The loop setting in the DL control register is always open.

A port is considered closed if one of the following conditions is met:

- The port is not available or not enabled in the configuration.
- The loop setting in the DL Control register is Auto and there is no active link at the port.
- The loop setting in the DL Control register is Auto close and there is no active link at the port or the DL Control register was not written again after the link was established.
- The loop setting in the DL Control register is always closed.

NOTE: If all ports are closed (either manually or automatically), port 0 will be opened as the recovery port. Reading and writing via this port is possible, although the DL status register reflects the correct status. This can be used to correct DL control register settings.

48.5.2.2 Frame Processing Order

The N32H7x5EC supports two ports and frames are processed in the following order: port 0 → EPU → port 1.

The direction through an ESC including the EtherCAT Processing Unit is called “processing” direction, other directions without passing the EtherCAT Processing Unit are called “forwarding” direction.

Ports which are not implemented behave similar to closed ports, the frame is forwarded to the next port.

Figure 48-5 shows the frame processing in general:

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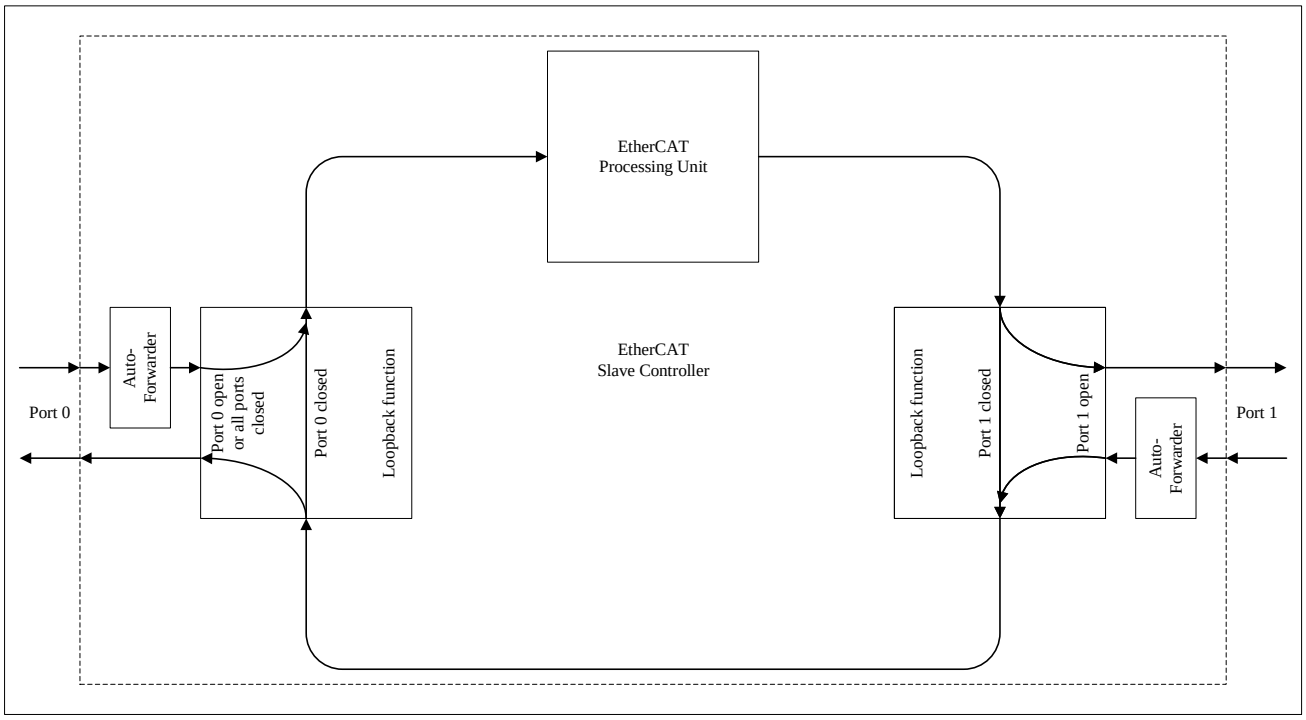
Figure 48-5 Frame Processing



48.5.2.3 Shadow Buffer

The ESC have shadow buffers for write operations to registers (offset address: 0x0000 to 0x0F7F). During a frame, write data is stored in the shadow buffers. If the frame is received correctly, the values of the shadow buffers are transferred into the effective registers. Otherwise, the values of the shadow buffers are not taken over. As a consequence of this behavior, registers take their new value shortly after the FCS of an EtherCAT frame is received. SyncManagers also change the buffers after the frame was received correctly.

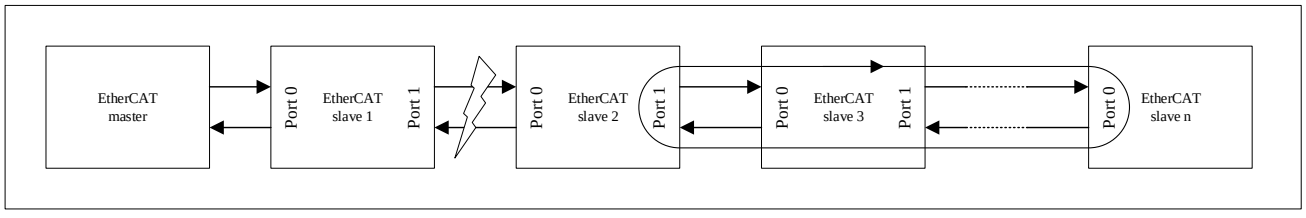
User and Process Memory do not have shadow buffers. Accesses to these areas are taking effect directly. If a SyncManager is configured to User Memory or Process Memory, write data will be placed in the memory, but the buffer will not change in case of an error.

48.5.2.4 Circulating Frames

The ESC incorporate a mechanism for prevention of circulating frames. This mechanism is very important for proper watchdog functionality.

The following figure shows an example of a failed link between slave 1 and slave 2:

Figure 48-6 Circulating Frames



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Both slave 1 and slave 2 detect the link failure and close their ports (port 1 at slave 1 and port 0 at slave 2). A frame currently traveling through the ring at the right side of slave 2 might start circulating. If such a frame contains output data, it might trigger the built-in watchdog of the ESCs, so the watchdog never expires, although the EtherCAT master cannot update the outputs anymore.

To prevent this, a slave with loop closed at port 0 and loop control for port 0 set to Auto or Auto close (ESC DL Control register) will do the following inside the EtherCAT Processing Unit:

- If the Circulating bit of the EtherCAT datagram is 0, set the Circulating bit to 1.
- If the Circulating bit is 1, do not process the frame and destroy it.

The result is that circulating frames are detected and destroyed. Since the ESCs do not store the frames for processing, a fragment of the frame will still circulate triggering the Link/Activity LEDs. Nevertheless, the fragment is not processed.

48.5.2.5 Non-EtherCAT Protocols

If non-EtherCAT protocols are used, the forwarding rule in the ESC DL Control register (bit 0) has to be set to forward non-EtherCAT protocols. Otherwise they are destroyed by the ESC.

48.5.2.6 Special Functions of Port 0

Port 0 of each EtherCAT is characterized by some special functions in contrast to ports 1:

- Port 0 leads to the master, i.e., port 0 is the upstream port, port 1 is the downstream port (unless an error has occurred and the network is in redundancy mode).
- The link state of Port 0 influences the Circulating Frame bit, and frames are dropped at port 0 if the bit is set and the link is automatically closed.
- Port 0 loop state is open if all ports are closed (either automatically or manually).

48.5.3 Physical Layer Common Features

The N32H7x5EC slave controller supports Ethernet physical layer. It requires 100 Mbit/s links with full duplex communication. The Ethernet-based physical layer uses standard Ethernet physical layer devices (PHY) according to IEEE 802.3. The N32H7x5EC slave controller use MII for connecting to external Ethernet PHYs.

48.5.3.1 Link Status

The link status of each port is available in the ESC DL Status register, most important are the “Communication established” bits (bit 9 and 11). Additional link information is available in the PHY Port Status register if MI link detection and configuration is used. All other status bits are mainly for debugging purposes.

If all ports are closed (either manually or automatically, e.g., because no port has a communication link), port 0 is automatically opened as the recovery port. Reading and writing via this port is possible, although the DL Status register reflects the correct status. This can be used to correct erroneous DL Control register settings or to fix LINK_MII polarity configuration.

48.5.3.2 FIFO Size Reduction

The ESCs incorporate a receive FIFO (RX FIFO) for decoupling receive clock and processing clock. The FIFO size

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is programmable by the EtherCAT master (ESC DL Control register).

The FIFO size values determine a reduction of the FIFO size, the FIFO cannot be disabled completely. The FIFO size can be reduced considering these three factors:

- Accuracy of the receiver's clock source
- Accuracy of the sender's clock source
- Maximum frame size

The default FIFO size is sufficient for maximum Ethernet Frames and default Ethernet clock source accuracy (100 ppm). If the clock accuracy is 25 ppm or better, the FIFO size can be reduced to the minimum. If the FIFO size was accidentally reduced too much, a short 64 Byte frame should be sent for resetting the FIFO size to the default value, since a smaller frame is not utilizing the FIFO as much as a larger frame.

The FIFO size can be reduced to minimum if both sender and receiver have 25 ppm accuracy of their clock sources, even with maximum frame size.

Since 25 ppm clock accuracy can typically not be guaranteed for the entire life-time of a clock source, the actual clock deviation has to be measured on a regular basis for FIFO size reduction. If the actual deviation is larger than 25 ppm, the FIFO size of all neighbors and the slave itself cannot be reduced. The actual deviation can be measured using Distributed Clocks:

- Compare DC Receive Times over a period of time for slaves which only support DC Receive Times. Do not use this method if both slaves which are compared support DC Time Loop, since the measured deviation will approximate zero if the DC control loop has settled, but the actual deviation determining the FIFO size might be larger than 25 ppm.
- Compare calculated deviation from register Speed Counter Diff for adjacent slaves with DC Time Loop support after the DC control loop has settled (i.e., System Time Difference register is at its minimum).

NOTE: Be careful with FIFO size reduction at the first slave if off-the-shelf network interface cards without 25 ppm accuracy are used by master.

48.5.4 Ethernet Physical Layer

EtherCAT slave devices with Ethernet Physical Layer usually support use the MII interface, some do also support the RMII interface. Since RMII PHYs include FIFOs, they increase the forwarding delay of an EtherCAT slave device as well as the jitter. RMII as an Ethernet Physical Layer is not supported by the N32H7x5EC slave controller due to these reasons.

48.5.4.1 MII Interface

There are differences in the use of the MII interface for EtherCAT slave devices compared to normal Ethernet devices. The following table shows MII signals that have special uses and are not used:

Table 48-6 Special/Unused MII Interface signals

Signal	Description
TX_CLK	Transmit clock. TX_CLK is optionally used for automatic TX Shift compensation.
COL	Collision detected. Unused, leave unconnected.

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Signal	Description
CRS	Carrier sense. Unused, leave unconnected.
TX_ER	Transmit error. Connect to GND.

For more details about the MII interface, refer to IEEE Standard 802.3 (Clause 22), available from the IEEE.

48.5.4.2 Link Detection

The major goal of the link detection is to detect a link loss very fast. This is required to maintain communication in the rest of the network by appropriately closing communication loops.

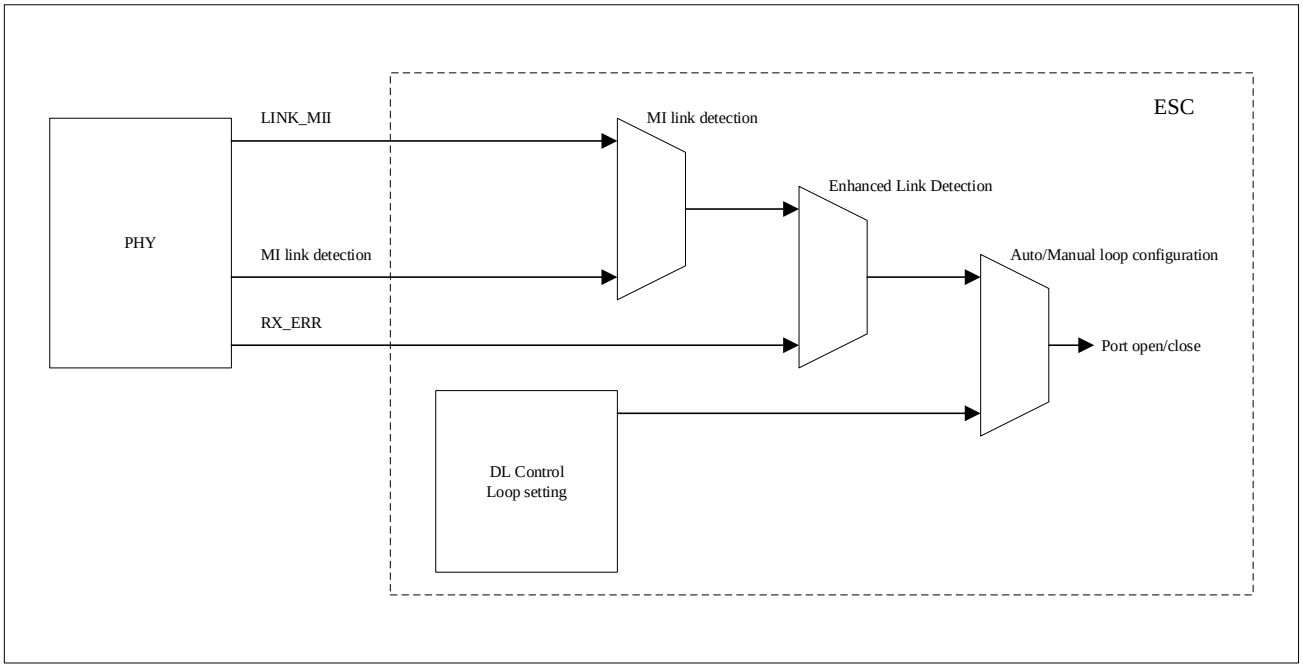
The following link status sources are available for Ethernet PHYs:

- LINK_MII signal from an Ethernet PHY
- MI link detection and configuration (MII management interface)
- RX_ERR signal used by Enhanced Link Detection

The MI link detection is generally not fast enough for EtherCAT when a link loss happens. For many PHYs, the LINK_MII signal is fast enough, but others need Enhanced Link Detection (RX_ERR).

The results of the different link status sources are evaluated inside the ESC according to the DL Control loop setting (ESC DL Control register):

Figure 48-7 Link Detection



At first, the LINK_MII signal and the result of the MI link detection is combined. The result of the LINK_MII signal is available in the ESC DL Status register (bit 4 and 5). The result of the MI link detection is available in the PHY Port Status register (offset address range 0x0518:0x0519).

Enhanced link detection overrides the previous result, if it is enabled and too many RX_ERR have been detected. The result is reflected in the ESC DL Status register (bit 9 and 11 – Communication established), and it is also used for LINKACT LED.

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Finally, the DL Control settings select if the link result is evaluated (and how). The loop state of each port is reflected in the ESC DL Status register (bit 8 and 10 – Loop open/closed).

48.5.4.2.1 Standard Link Detection

The results of the different sources for Standard MII link detection are combined by a specific logic. The main combinations are shown in the following table.

Table 48-7 Ethernet Link Detection combination

LINK_MII	MI link	MI no link	Link result	Description
No	No	No	No link	-
Yes	No	No	Link	-
Yes	No	No	Link	-
Yes	Yes	No	Link	MI link detection found valid link, status of LINK_MII is accepted.
Don't care	No	Yes	No link	MI link detection found invalid link status, either local or at link partner, overrides other status.
Link down event	Yes	Yes	No link	A link down event (edge) overrides MI link detection.
No	Yes	Yes	Link	Test only, because link-loss reaction time is too slow: MI link is used without LINK_MII.

NOTE: "MI link" means that MI link detection successfully read the PHY, and the result is OK. "MI no link" means that MI link detection successfully read the PHY, but the result is not OK. If MI link detection could not properly read from the PHY, the result is undefined.

48.5.4.2.1.1 LINK_MII Signal

The LINK_MII signal used for link detection is typically an LED output signal of the Ethernet PHY. If available, LINK_MII should be connected to a combined signal indicating a 100 Mbit/s Full Duplex link. If such a signal is not available, a signal indicating a 100 Mbit/s link (speed LED) might be used. If only a Link signal is available (link LED), this might be used. Never use (combined) activity signals, e.g., Link/Act LED outputs, because the link state will toggle upon activity.

The main advantage of using a dedicated link signal instead of reading out MII management interface registers is the fast reaction time in case of a link loss. This is crucial for redundancy operation, since only one lost frame is tolerated. The EtherCAT port of an ESC which loses a link has to be closed as fast as possible to maintain EtherCAT communication at the other ports and to reduce the number of lost frames.

48.5.4.2.1.2 MI Link Detection and Configuration

The N32H7x5EC slave controller supports link detection and PHY configuration by using the MII management interface. Initially, the PHY configuration is checked and updated if necessary. Afterwards, the link status of each Ethernet port is cyclically polled. PHY accesses of the EtherCAT master are inferred upon request.

The MI Link Configuration mechanism configures the Ethernet PHYs to use Auto negotiation and advertise only 100BASE-TX Full-Duplex connections. ESCs which support FX operation natively are configuring the FX ports to use fixed 100BASE-TX Full-Duplex connections without Auto negotiation.

Depending on the physical layer configuration and the supported ESC features (e.g., TX vs. FX), the MI Link

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Detection will check if the link characteristics fulfill EtherCAT requirements (Auto negotiation, Speed, Duplex, etc.). If all conditions are met, an MI Link is detected.

Since the MI Link Detection does not solely rely on the PHY link status bit (PHY status register), the local PHY and the remote PHY may indicate a link, but the ESC refuses it because it does not fulfill EtherCAT requirements. The current MI Link Detection state is reflected in the MI Interface registers (PHY Port 0/1 Status registers).

MI Link Detection and Configuration must not be used without link detection via LINK_MII signal, because link loss reaction time would otherwise be to slow for redundancy operation. Enhanced Link Detection might not be a suitable solution in this case if too few RX_ERR are issued to the ESC before the PHY takes down the link.

NOTE: For testing it is possible to use MI Link Detection without LINK_MII signals: If the LINK_MII signals are statically set to "no link", only MI Link Detection is used.

The MI Link Detection and Configuration checks the management communication with Ethernet PHYs. If communication is not possible – e.g. because no PHY is configured for the expected PHY address – the results are ignored. Take care of proper PHY address configuration to prevent erroneous behavior.

NOTE: Proper PHY address settings and PHY address offset configuration is crucial for MI Link Detection and Configuration.

48.5.4.2.2 Enhanced Link Detection

For Ethernet, the enhanced MII link detection feature is a feature of link error detection and reaction. This has to be distinguished from the actual link detection, which tells the ESC if a physical link is available (i.e., the LINK_MII signal or the MI link detection and configuration mechanism).

Enhanced MII link detection will additionally disconnect a link if at least 32 RX errors (RX_ERR) occur in a fixed interval of time (~10 µs). The local loop is closed and the link partner is informed by restarting the Auto-Negotiation mechanism via the MII Management Interface. This informs the link partner of the error condition, and the link partner will close the loop.

The ESC keeps the port closed until the link goes down during Auto-Negotiation and comes up again (the port remains closed if the link does not go down).

The availability of Enhanced MII Link Detection depends on a supported PHY address configuration, otherwise it has to be disabled.

48.5.4.3 MII Management Interface (MI)

Most EtherCAT slave controllers with MII/RMII/RGMII ports use the MII management interface for communication with the Ethernet PHYs. The MII management interface can be used by the EtherCAT master or the local µController if supported by the ESC. Enhanced MII link detection uses the management interface for configuration and restarting auto negotiation after communication errors occurred (TX PHYs only). For fast link detection, the ESCs require to use a separate signal (LINK_MII).

Refer to chapter 48.5.4.2 for details about link detection with Ethernet PHYs. For more details about the MII management interface, refer to IEEE Standard 802.3 (Clause 22), available from the IEEE.

The ESCs support a shared MII Management Interface for all PHYs, i.e., MCLK and MDIO are connected to the ESC and to all PHYs.

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48.5.4.3.1 PHY Addressing/PHY Address Offset

Proper PHY address configuration is crucial for Enhanced Link Detection and MI Link Detection and configuration, because the ESC itself needs to relate logical ports to the corresponding PHY addresses. The EtherCAT master can access the Ethernet PHYs using any address by means of the PHY address register.

Typically, the logical port numbers match with the PHY addresses, i.e. the EtherCAT master and the ESC itself use PHY address 0 for accessing the PHY at port 0 (PHY address 1 for the PHY at port 1).

N32H7x5EC slave controller config PHY address by PHY address offset:

The ESC accesses a PHY at logical port x with the address “x + PHY address offset”. The EtherCAT master uses the PHY addresses 0/1 to access the logical ports 0/1. These addresses are incremented by the PHY address offset inside the ESC. If the master uses PHY addresses 2-31, these addresses are also incremented by the PHY address offset inside the ESC.

The PHY address configuration of N32H7x5EC slave controller is a strapped at power-up, configured in advance.

Typically, the PHY address offset should be 0, and the logical port numbers match with the PHY addresses. Some Ethernet PHYs associate a special function with PHY address 0, e.g., address 0 is a broadcast PHY address. In these cases, PHY address 0 cannot be used. Instead, a PHY address offset different from 0 should be selected, preferably an offset which is supported by the ESC (The maximum offset supported is 31). If PHY addresses are chosen which are not supported by the ESC, Enhanced Link Detection and MI Link Detection and Configuration cannot be used and have to be disabled (the PHY address offset should be 0 in these cases). Nevertheless, the EtherCAT master can communicate with the PHYs using the actual PHY addresses, and EtherCAT communication is possible anyway – using the LINK_MII signal. It is recommended that the PHY addresses are selected to be equal to the logical port number plus 1 in this case.

If the PHY address offset configuration of an ESC reflects the actual PHY address settings, the EtherCAT master can use addresses 0/1 in PHY address register for accessing the PHYs of logical ports 0/1, regardless of the PHY address offset.

48.5.4.3.2 MI read/write example

The MI supports two commands: write to one PHY register or read one PHY register. The following steps have to be performed for a PHY register access:

1 Check if the "Busy" bit of the MI Status register is cleared and the MI is not busy.

2 Write PHY address to PHY Address register.

3 Write PHY register number to be accessed into PHY Register Address register (0-31).

4 Write command only: put write data into PHY Data register (16 bits).

5 Issue command by writing to Control register.

For read commands, write 1 into MII Management Control/Status register's (offset address 0x0510) bit 8.

For write commands, write 1 into MII Management Control/Status register's bit 0 (Write Enable bit) and also 1 into MII Management Control/Status register's bit 9. Both bits have to be written in one frame. The Write enable bit realizes a write protection mechanism. It is valid for subsequent MI commands issued in the same frame and self-clearing afterwards.

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6 The command is executed after the EOF, if the EtherCAT frame had no errors.

7 Wait until the "Busy" bit of the MI Status register is cleared.

8 Check the Error bits of the MI Status register. The command error bit is cleared with a valid command or by clearing the command register. The read error bit indicates a read error, e.g., a wrong PHY address. It is cleared by writing to the register.

9 Read command only: Read data is available in PHY Data register.

NOTE: The Command register bits are self-clearing. Manually clearing the command register will also clear the status information.

48.5.4.3.3 MI Interface Assignment to ECAT/PDI

The EtherCAT master controls the MI Interface (default) if the MII Management PDI Access State register's bit 0 is not set. The EtherCAT master can prevent PDI control over the MI Interface, and it can force the PDI to release the MI Interface control. After power-on, the PDI can take over MI Interface control without any master transactions.

48.5.4.3.4 MI Protocol

Each MI access begins with a Preamble of "Ones" (32 without preamble suppression, less if both ESC and PHY support preamble suppression), followed by a Start-of-Frame (01) and the Operation Code ('01' for write and '10' for read operations). Then the PHY address (5 bits) and the PHY register address (5 bits) are transmitted to the PHY. After a Turnaround ('10' for write and 'Z0' for read operations – Z means MDIO is high impedance), two bytes of data follow. The transfer finishes after the second data byte and at least one IDLE cycle.

48.5.4.4 MII management example schematic

The MII management interface is a shared bus for all PHYs. The example schematic shows the connection between ESC and PHYs. Take care of proper PHY address configuration.

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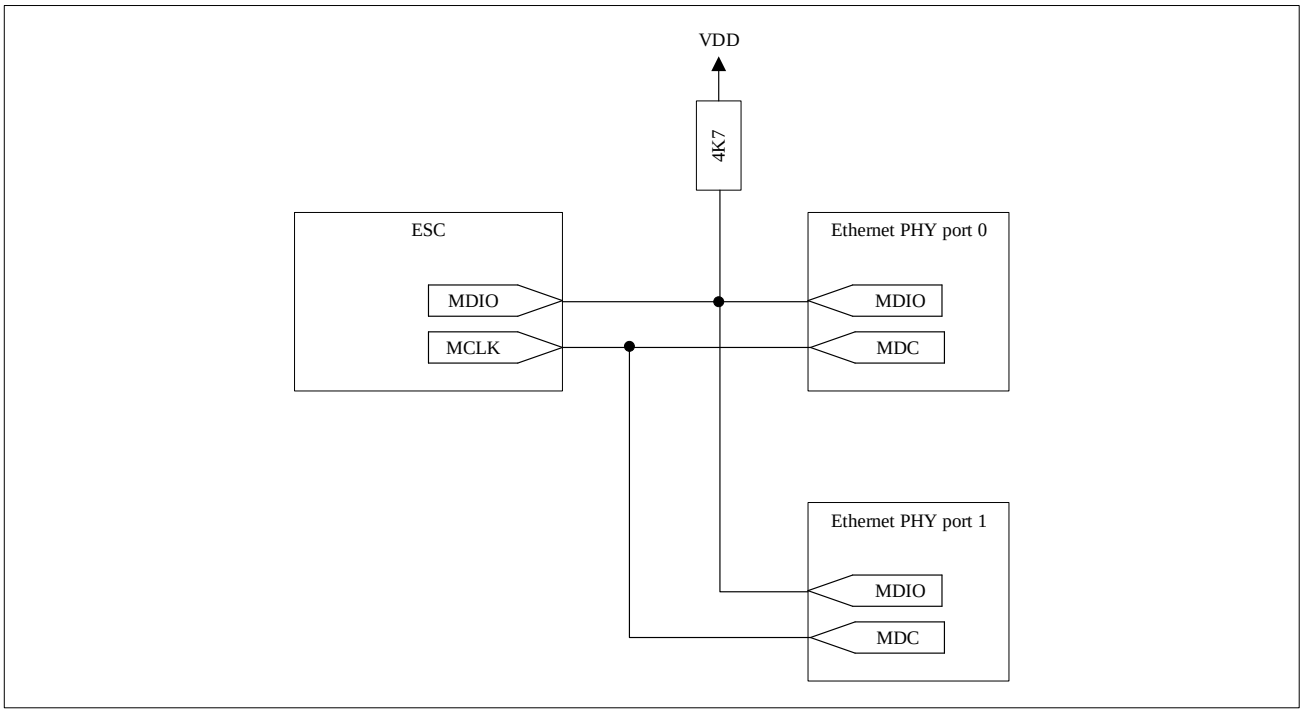
Figure 48-8 MII management example schematic



48.5.5 FMMU

Fieldbus Memory Management Units (FMMU) convert logical addresses into physical addresses by the means of internal address mapping. Thus, FMMUs allow to use logical addressing for data segments that span several slave devices: one datagram addresses data within several arbitrarily distributed ESCs. Each FMMU channel maps one continuous logical address space to one continuous physical address space of the slave. The FMMUs of N32H7x5EC slave controller support bit wise mapping, and support 8 FFMUs. The access type supported by an FMMU is configurable to be either read, write, or read/write.

NOTE: Logical process image: up to 4 GByte.

48.5.5.1 FMMU Mapping Example

The following example illustrates the functions of an FMMU configured to map 14 bits from logical address 0x00010011.3 to 0x00010013.0 to the physical register bits 0x1000.1 to 0x1001.6. The FMMU length is 3 Byte, since the mapped bits span 3 Bytes of the logical address space. Length calculation begins with the first logical byte which contains mapped bits, and ends with the last logical byte which contains mapped bits.

In this case, the relevant registers of the FMMU are configured as shown in the table below:

Table 48-8 Example FMMU Configuration

FMMU configuration register	Value
Logical Start Address	0x00010011
Length	3
Logical Start bit	3

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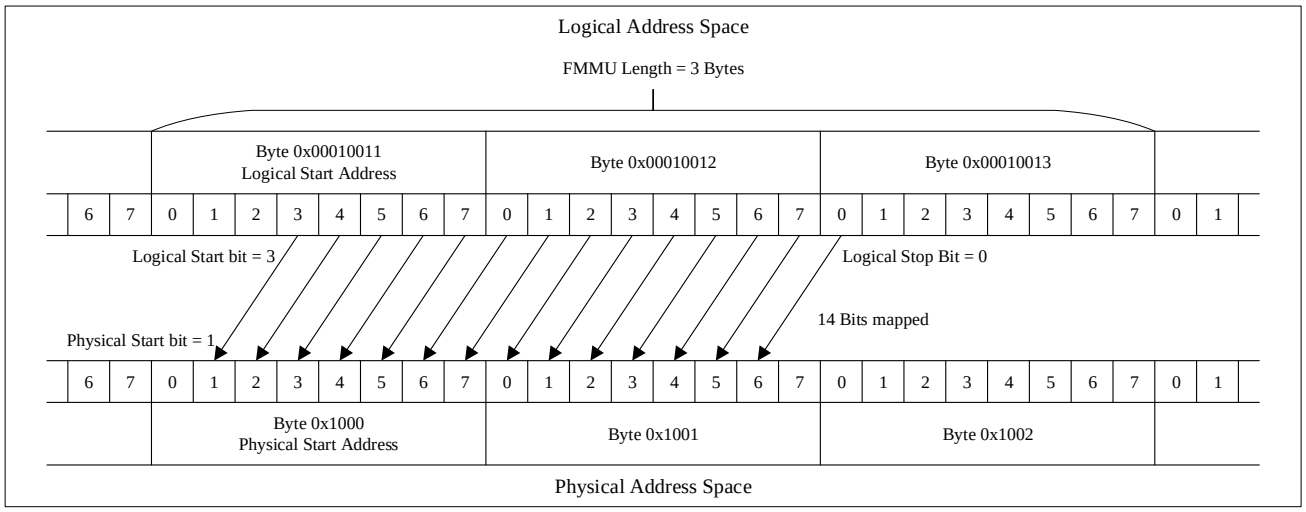
FMMU configuration register	Value
Logical Stop bit	0
Physical Start Address	0x1000
Physical Start bit	1
Type	read and/or write
Activate	1 (enabled)

In this case, the mapping relationship of FMMU is shown below:

Figure 48-9 FMMU Mapping Example



48.5.5.2 FMMU Restriction

The FMMUs are subject to restrictions. The logical address ranges of two FMMUs of the same direction (read or write) in one ESC must be separated by at least 3 logical bytes not configured by any FMMU of the same type, if one of the FMMUs or both use bit-wise mapping (logical start bit $\neq$ 0, logical stop bit $\neq$ 7, or physical start bit $\neq$ 0). In the above example, the first logical address area after the one shown must have a logical start address of 0x00010017 or higher (the last byte of the example FMMU is 0x00010013, three bytes free 0x00010014 - 0x00010016).

If only byte-wise mapping is used (logical start bit = 0, logical stop bit = 7, or physical start bit = 0), the logical address ranges can be adjacent.

If bit-wise mapping is used, bits without mapping to logical addresses are written with undefined values (e.g., if only physical address bit 0x1000.0 is mapped by a write FMMU, the bits 1-7 are written with undefined values).

48.5.5.3 Additional FMMU Characteristics

- Each logical address byte can at most be mapped either by one FMMU (read) plus one FMMU (write), or by one FMMU (read/write). If two or more FMMUs (with the same direction – read or write) are configured for the same logical byte, the FMMU with the lower number (lower configuration address space) is used, the other ones are ignored.
- One or more FMMUs may point to the same physical memory, all of them are used. Collisions cannot occur.
- It is the same to use one read/write FMMU or two FMMUs – one read, the other one write – for the same logical

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address.

- A read/write FMMU cannot be used together with SyncManagers, since independent read and write SyncManagers cannot be configured to use the same (or overlapping) physical address range.
- Bit-wise reading is supported at any address. Bits which are not mapped to logical addresses are not changed in the EtherCAT datagram. E.g., this allows for mapping bits from several ESCs into the same logical byte.
- A frame/datagram addressing a logical address space which is not configured in the ESC will not change data in the ESC, and no data from the ESC is placed in the frame/datagram.

48.5.6 SyncManager

The memory of an ESC can be used for exchanging data between the EtherCAT master and a local application (on a µController attached to the PDI) without any restrictions. Using the memory for communication like this has some drawbacks which are addressed by the SyncManagers inside the ESCs:

- Data consistency is not guaranteed. Semaphores have to be implemented in software for exchanging data in a coordinated way.
- Data security is not guaranteed. Security mechanisms have to be implemented in software.
- Both EtherCAT master and application have to poll the memory in order to find out when the access of the other side has finished.

SyncManagers enable consistent and secure data exchange between the EtherCAT master and the local application, and they generate interrupts to inform both sides of changes.

SyncManagers are configured by the EtherCAT master. The communication direction is configurable, as well as the communication mode (Buffered Mode and Mailbox Mode). SyncManagers use a buffer located in the memory area for exchanging data. Access to this buffer is controlled by the hardware of the SyncManagers.

A buffer has to be accessed beginning with the start address, otherwise the access is denied. After accessing the start address, the whole buffer can be accessed, even the start address again, either as a whole or in several strokes. A buffer access finishes by accessing the end address, the buffer state changes afterwards and an interrupt or a watchdog trigger pulse is generated (if configured). The end address cannot be accessed twice inside a frame.

Two communication modes are supported by SyncManagers:

- Buffered Mode

  The buffered mode allows both sides, EtherCAT master and local application, to access the communication buffer at any time. The consumer gets always the latest consistent buffer which was written by the producer, and the producer can always update the content of the buffer. If the buffer is written faster than it is read out, old data will be dropped.

  The buffered mode is typically used for cyclic process data.

- Mailbox Mode

  The mailbox mode implements a handshake mechanism for data exchange, so that no data will be lost. Each side, EtherCAT master or local application, will get access to the buffer only after the other side has finished its access. At first, the producer writes to the buffer. Then, the buffer is locked for writing until the consumer has

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read it out. Afterwards, the producer has write access again, while the buffer is locked for the consumer.

The mailbox mode is typically used for application layer protocols, e.g. Ethernet over EtherCAT (EoE), CAN application layer over EtherCAT (CoE), File Access over EtherCAT (FoE), Automation device specification over EtherCAT (AoE), etc.

The SyncManagers accept buffer changes caused by the master only if the FCS of the frame is correct, thus, buffer changes take effect shortly after the end of the frame.

48.5.6.1 Buffered Mode

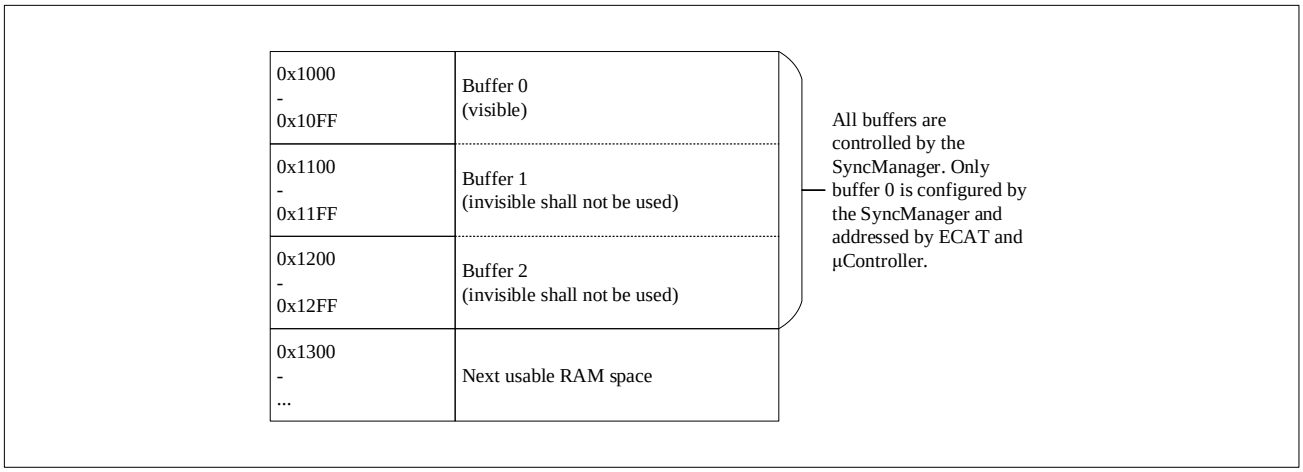
The buffered mode is also known as 3-buffer-mode.

Physically, 3 buffers of identical size are used for buffered mode. The start address and size of the first buffer is configured in the SyncManager configuration. The addresses of this buffer have to be used by the master and the local application for reading/writing the data. Depending on the SyncManager state, accesses to the first buffer's (0) address range are redirected to one of the 3 buffers. The memory used for buffers 1 and 2 cannot be used and should be taken into account for configuring other SyncManagers.

One buffer of the three buffers is allocated to the producer (for writing), one buffer to the consumer (for reading), and the third buffer keeps the last consistently written data of the producer.

As an example, Figure 48-10 demonstrates a configuration with start address 0x1000 and Length 0x100. The other buffers shall not be read or written. Access to the buffer is always directed to addresses in the range of buffer 0.

Figure 48-10 SyncManager Buffer allocation



The buffer interaction is shown in Figure 48-11:

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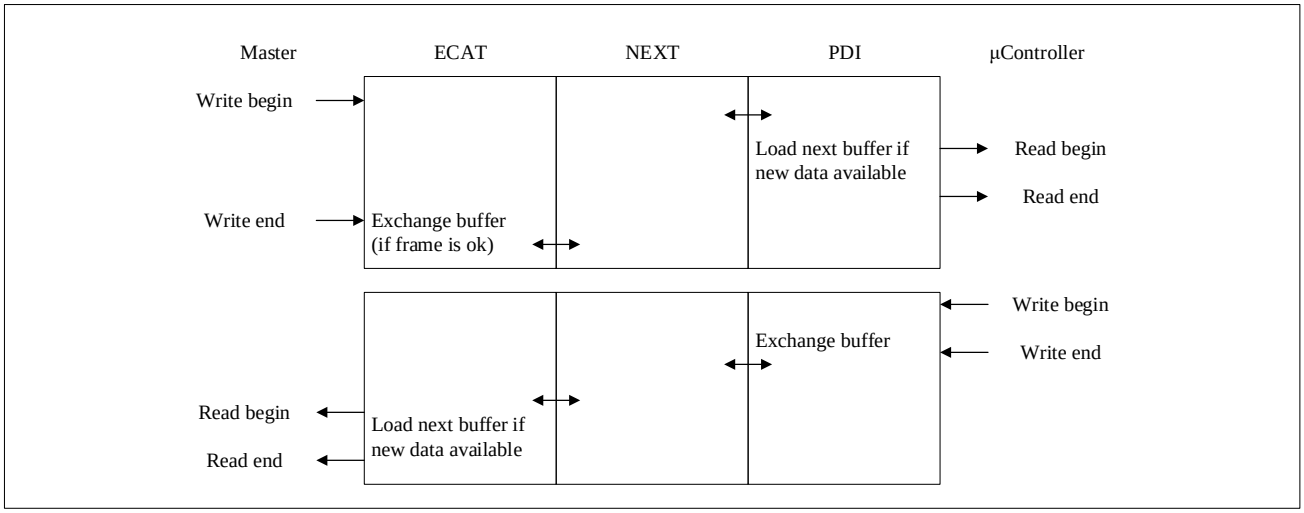
Figure 48-11 SyncManager Buffered Mode Interaction



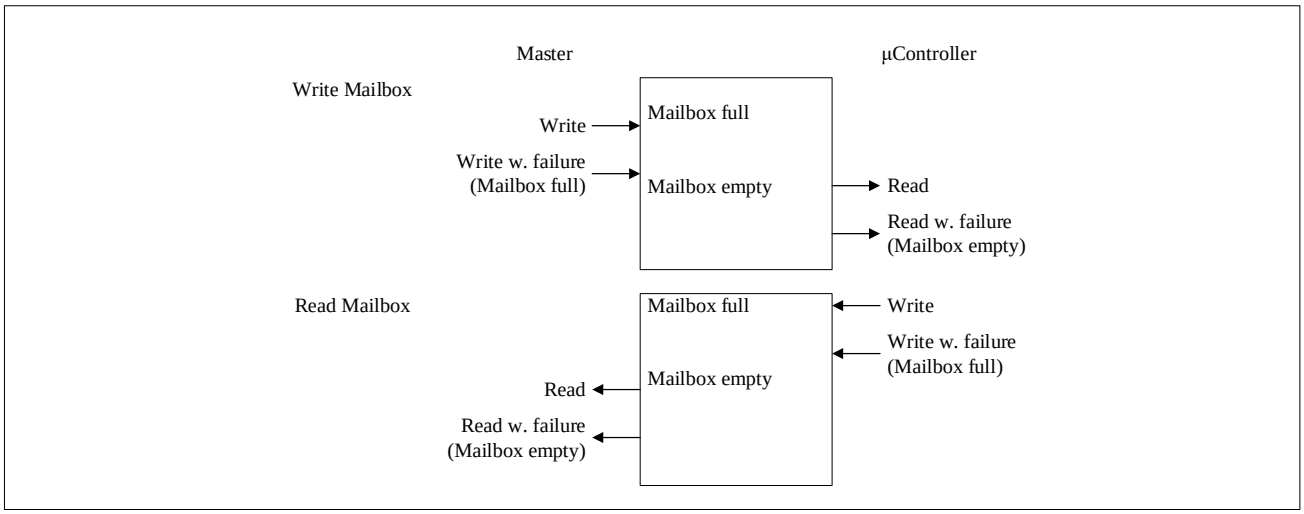
The Status register of the SyncManager reflects the current state. The last written buffer is indicated (informative only, access redirection is performed by the ESC), as well as the interrupt states. If the SyncManager buffer was not written before, the last written buffer is indicated to be 3 (start/empty).

48.5.6.2 Mailbox Mode

The mailbox mode only allows alternating reading and writing. This assures all data from the producer reaches the consumer. The mailbox mode uses just one buffer of the configured size.

At first, after initialization/activation, the buffer (mailbox, MBX) is writeable. Once it is written completely, write access is blocked, and the buffer can be read out by the other side. After it was completely read out, it can be written again.

Figure 48-12 SyncManager Mailbox Interaction



48.5.6.3 PDI register function acknowledge by Write

Refer to chapter 48.5.15.2 for the background of this function, which only affects the SyncManager operation when the PDI reads a buffer. The EtherCAT operation is not influenced by this feature.

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Reading a SyncManager buffer consists of the following steps, if PDI register function acknowledge by Write is enabled:

- Read the first byte.

  This will open the buffer. Accidentally reading subsequent bytes has no influence.

- Read any byte of the buffer.

  This includes the first byte, the last byte, and any inner byte. The buffer remains open, and the buffer can even be read multiple times. Accidentally reading the last byte has no influence.

- Write to the last byte of the buffer.

  Byte enable signals are used, write data is ignored (write 0). This write operation closes the buffer.

Accidentally reading the first byte of a second SyncManager buffer behind the one to be read is still possible, this will open the second SyncManager buffer. This can easily be prevented by aligning SyncManager buffer start addresses to the data width of the µController. It is recommended to align SyncManager buffer start addresses to 64 bit (8 byte) boundaries anyway.

48.5.6.4 Interrupt and Watchdog Trigger Generation, Latch Event Generation

Interrupts can be generated when a buffer was completely and successfully written or read. A watchdog trigger signal can be generated to rewind (trigger) the Process Data watchdog after a buffer was completely and successfully written. Interrupt and watchdog trigger generation are configurable. The SyncManager Status register reflects the current buffer state.

For debugging purposes it is also possible to trigger Distributed Clock Latch events upon successful buffer accesses.

48.5.6.5 Repeating Mailbox Communication

A lost datagram with mailbox data is handled by the application layer. The Repeat Request/Repeat Acknowledge bits in the SyncManager Activation register and the PDI Control register are used in mailbox mode for retransmissions of buffers from a slave to the master. If a mailbox read frame gets lost/broken on the way back to the master, the master can toggle the Repeat Request bit. The slave polls this bit or receives an interrupt (SyncManager activation register changed, AL Event Request register's bit 4) and writes the last buffer again to the SyncManager. Then the PDI toggles the Repeat Acknowledge bit in the PDI Control register. The master will read out this bit and read the buffer content. Communication resumes afterwards.

This mechanism is shown in Figure 48-13 for a mailbox write service. The Mailbox confirmation is lost on its way from the slave to the master and has to be repeated again.

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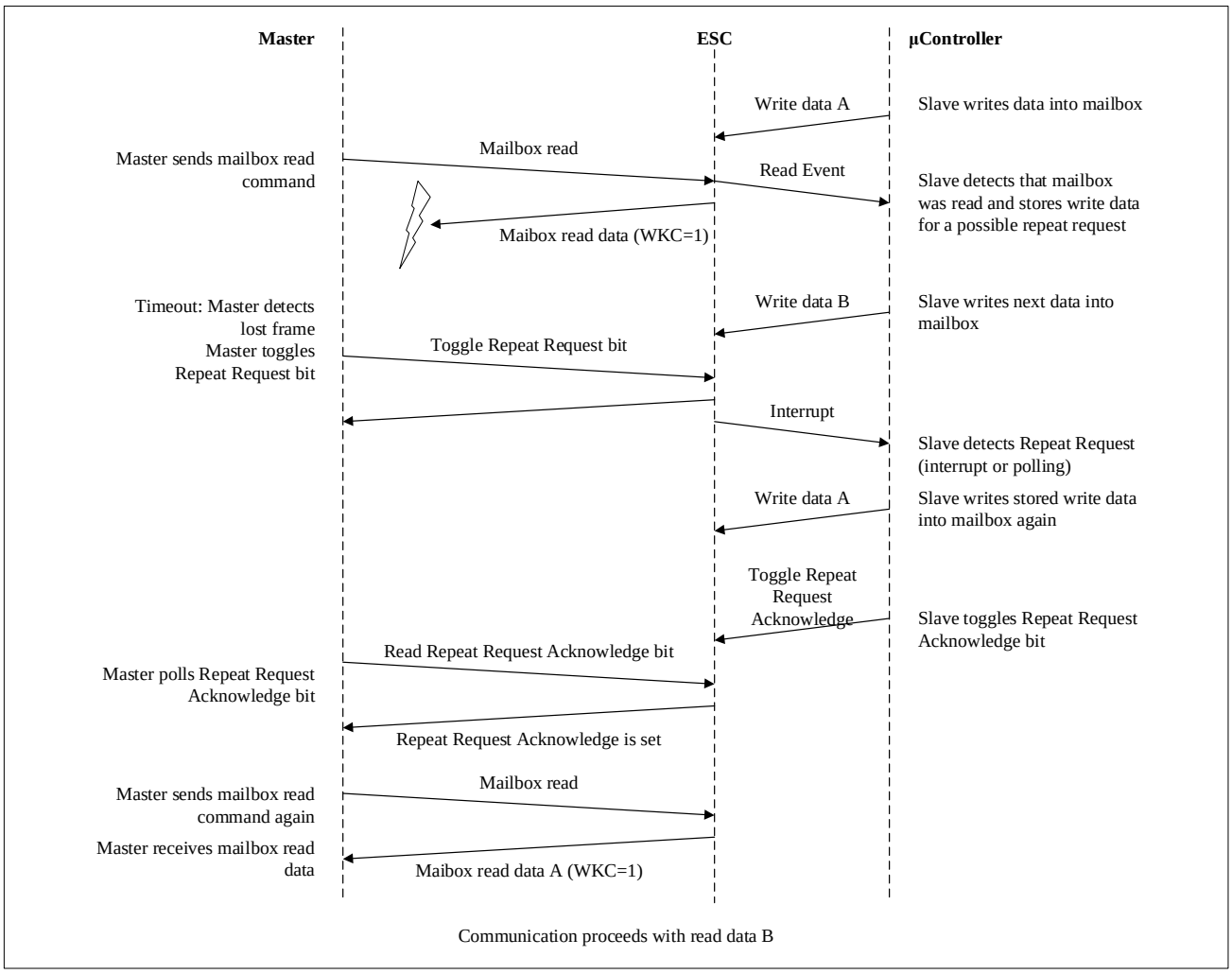
Figure 48-13 Handling of a Repeat Request with Read Mailbox



48.5.6.6 SyncManager Deactivation by the PDI

A SyncManager can be deactivated by the PDI to inform the master of local problems (typically used in buffered mode only). The master can detect SyncManager deactivation by checking the Working Counter, which is not incremented if a deactivated SyncManager buffer is accessed. If a SyncManager is deactivated by the PDI (PDI Control SyncManager register's bit 0 to 1), the state of the SyncManager is reset, interrupts are cleared and the SyncManager has to be written first after re-activation. The entire SyncManager buffer area is read/write protected while the SyncManager is deactivated by the PDI.

48.5.7 Distributed Clocks

The Distributed Clocks (DC) unit of EtherCAT slave controllers supports the following features:

- Clock synchronization between the slaves (and the master)
- Generation of synchronous output signals (SyncSignals)
- Precise time stamping of input events (LatchSignals)
- Generation of synchronous interrupts

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48.5.7.1 Clock Synchronization

DC clock synchronization enables all EtherCAT devices (master and slaves) to share the same EtherCAT System Time. The EtherCAT devices can be synchronized to each other, and consequently, the local applications are synchronized as well.

For system synchronization all slaves are synchronized to one Reference Clock. Typically, the first ESC with Distributed Clocks capability after the master within one segment holds the reference time (System Time). This System Time is used as the reference clock to synchronize the DC slave clocks of other devices and of the master. The propagation delays, local clock sources drift, and local clock offsets are taken into account for the clock synchronization.

The ESCs can generate SyncSignals for local applications to be synchronized to the EtherCAT System Time. SyncSignals can be used directly (e.g., as interrupts). Additionally, LatchSignals can be time stamped with respect to the EtherCAT System Time.

48.5.7.1.1 System Time

- Beginning on January, 1st 2000 at 0:00h
- Base unit is 1 ns
- 64 bit value (enough for more than 500 years)
- Lower 32 bits span over 4.2 seconds (typically enough for communication and time stamping)

48.5.7.1.2 Reference Clock

One EtherCAT device will be used as a Reference Clock. Typically, the Reference Clock is the first ESC with DC capability between master and all the slaves to be synchronized (DC slaves). The Reference Clock might be adjusted to a “global” reference clock, e.g. to an IEEE 1588 grandmaster clock. The reference clock provides the System Time.

48.5.7.1.3 Local Clock

Each DC slave has a local clock, initially running independent of the Reference Clock. The difference between local clock and Reference Clock (offset) can be compensated, as well as clock drifts. The offset is compensated by adding it to the local clock value. The drift is compensated by measuring and adjusting the local clock speed.

Each DC slave holds a copy of the Reference Clock, which is calculated from the local clock and the local offset. The Reference Clock has a local clock, too.

48.5.7.1.4 Master Clock

The Reference Clock is typically initialized by the EtherCAT master using the master clock to deliver the System Time according to the System Time definition. The EtherCAT master clock is typically bound to a global clock reference (RTC or the master PC, IEEE1588, GPS, etc.), which is either directly available to the master or indirectly by an EtherCAT slave providing access to the reference.

48.5.7.1.5 Offset

The offset between local clock and Reference Clock has two reasons: the propagation delay from the ESC holding the Reference Clock to the device with the slave clock, and initial differences of the local times resulting from different times at which the ESCs have been powered up. This offset is compensated locally in each slave.

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The ESC holding the Reference Clock derives the System Time from its local time by adding a local offset. This offset represents the difference between local time (started at power-up) and master time (starting on January, 1st 2000 at 0:00h).

48.5.7.1.6 Drift

Since Reference Clock and DC slaves are typically not sourced by the same clock source (e.g., a quartz), their clock sources are subject to small deviations of the clock periods. The result is that one clock is running slightly faster than the other one, their local clocks are drifting apart.

48.5.7.2 Clock Synchronization Process

The clock synchronization process consists of four steps:

1 Propagation Delay Measurement:

The master initiates propagation delay measurement between all slaves in all directions. Each EtherCAT slave controller measures the receive time of the measurement frame. The master collects the time stamps afterwards and calculates the propagation delays between all slaves.

2 Offset compensation to Reference Clock (System Time):

The local time of each slave clock is compared to the System Time. The difference is compensated individually by writing it to each slave. All devices get the same absolute System Time.

3 Resetting the Time Control Loop:

The current filter status needs to be reset to eliminate influences of previous measurements and improve repeatability.

4 Drift compensation to Reference Clock:

The drift between Reference Clock and local clock has to be compensated by regularly measuring the differences and readjusting the local clocks.

The following figure illustrates the compensation calculations for two cases, in the first case the System Time is less than the slave's local time, in the second case, it is the other way around.

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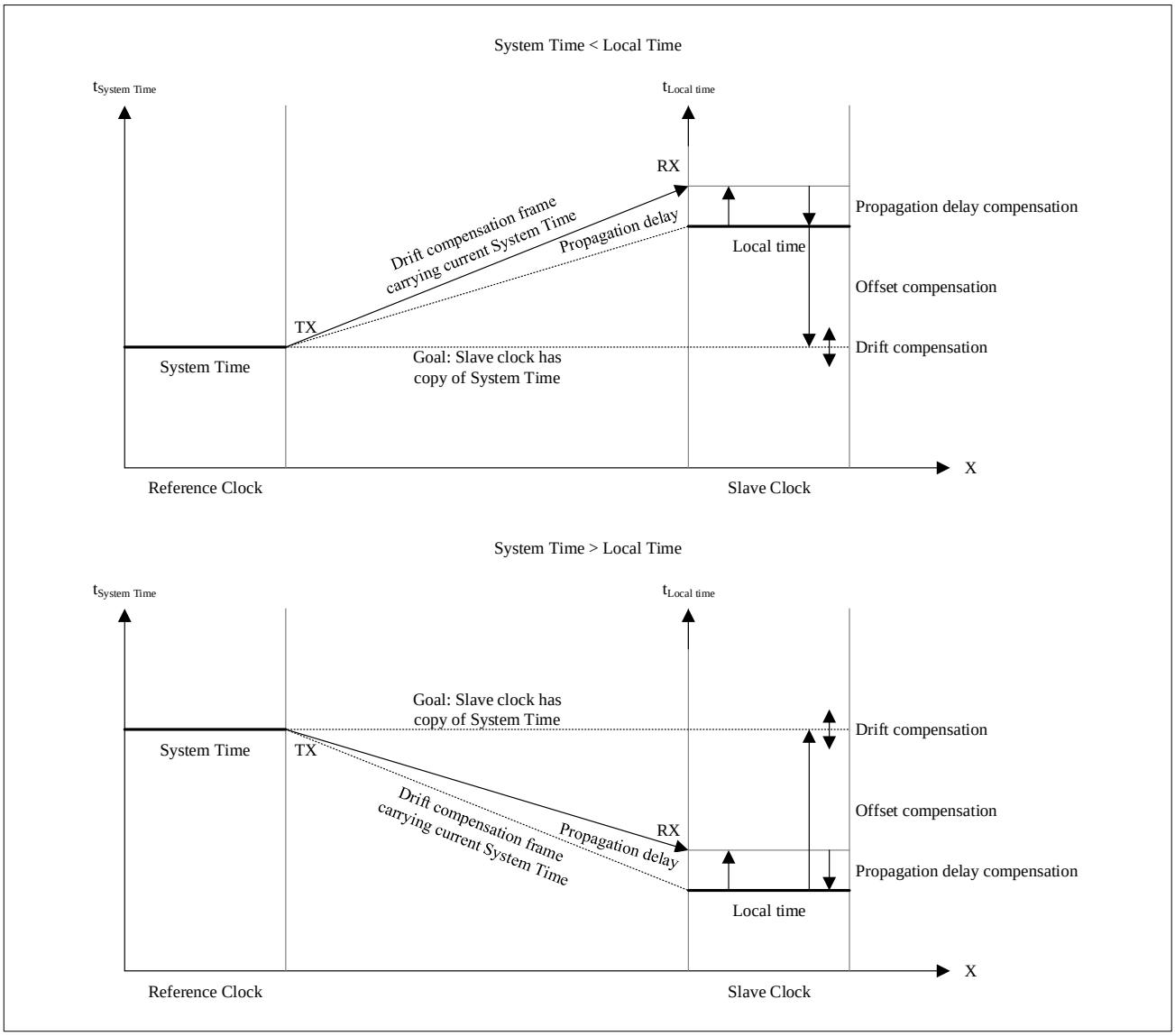
Figure 48-14 Propagation Delay, Offset, and Drift Compensation



48.5.7.2.1 Propagation Delay Measurement

Since each slave introduces a small processing/forwarding delay in each direction (within the device and also in the PHY), as well as the cable between the ESCs has a delay, the propagation delay between Reference Clock and the respective slave clock has to be considered for the synchronization of the slave clocks.

1 For measuring the propagation delay, the master sends a broadcast write to register Receive Time Port 0 (at least the first byte).

2 Each slave device stores the time of its local clock when the first bit of the Ethernet preamble of the frame was received, separately for each port (Receive Time Port 0-1 registers).

3 The master reads all time stamps and calculates the delay times with respect to the topology. The delay time between Reference Clock and an individual slave is written to the slave's System Time Delay register.

The Receive Time registers are used to sample the receive time of a specific frame (a broadcast write to Receive

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Time Port 0 register).

The clocks must not be synchronized for the delay measurement, only local clock values are used. Since the local clocks of the slaves are not synchronized, there is no relation between the Receive Times of different slaves. So the propagation delay calculation has to be based on receive time differences between the ports of a slave.

48.5.7.2.2 Offset Compensation

The local time of each device is a free-running clock which typically will not have the same time as the Reference Clock. To achieve the same absolute System Time in all devices, the offset between the Reference Clock and every slave device's clock is calculated by the master. The offset time is written to System Time Offset register to adjust the local time for every individual device. Small offset errors are eliminated by the drift compensation after some time, but this time might become extremely high for large offset errors – especially for 64 bit DCs.

Each DC slave calculates its local copy of the System time using its local time and the local offset value:

$$t_{\text{Local copy of System Time}} = t_{\text{Local time}} + t_{\text{Offset}}$$

This time is used for SyncSignal generation and time stamping of LatchSignals. It is also provided to the PDI for use by µControllers.

$t_{\text{Local copy of System Time}}$: Indicates the value of the register with offset addresses 0x0910:0x0917.

$t_{\text{Local time}}$: Indicates the value of the register with offset addresses 0x0918:0x091F.

t_{Offset}: Indicates the value of the register with offset addresses 0x0920:0x0927.

The System Time of the Reference Clock is bound to the master clock by calculating the difference and compensating it using the System Time Offset of the Reference Clock.

48.5.7.2.3 Resetting the Time Control Loop

Before starting drift compensation, the internal filters of the Time Control Loop must be reset. Their current status is typically unknown, and they can have negative impact on the settling time. The filters are reset by writing the Speed Counter Start value to the Speed Counter Start register. Writing the current value of the register again is sufficient to reset the filters.

48.5.7.2.4 Drift Compensation

After the delay time between the Reference Clock and the slave clocks has been measured, and the offset between both clocks has been compensated, the natural drift of every local clock (emerging from quartz variations between the Reference Clock's quartz and the local quartz) is compensated by the time control loop which is integrated into each ESC.

For drift compensation, the master distributes the System Time from the Reference Clock to all slave clocks periodically. The ARMW or FRMW commands can be used for this purpose. The time control loop of each slave takes the lower 32 bit of the System Time received from the Reference Clock and compares it to its local copy of the System Time. For this difference, the propagation delay has to be taken into account:

$$\Delta t = \left(t_{\text{Local time}} + t_{\text{Offset}} - t_{\text{Propagation delay}}\right) - t_{\textit{Received System Time}}$$

If Δt is positive, the local time is running faster than the System time, and has to be slowed down. If Δt is negative, the local time is running slower than the System time, and has to speed up. The time control loop adjusts the speed of the local clock.

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For a fast compensation of the static deviations of the clock speeds, the master should initially send many ARMW / FRMW commands (e.g. 15,000) for drift compensation in separate frames after initialization of the propagation delays and offsets. The control loops compensate the static deviations and the distributed clocks are synchronized. Afterwards, the drift compensation frames are sent periodically for compensation of dynamic clock drifts.

NOTE: The System Time Offset allows fast compensation of differences between local copy of the system time and the System Time, the drift compensation is very slow. Thus, shortly before drift compensation is started, the offset should be roughly compensated using the System Time Offset register. Otherwise settling time might become very high.

NOTE: Δt must not exceed 2^{30} ns (~ 1 second), otherwise stability is not guaranteed. For fast settling times, Δt should be as low as possible.

48.5.7.3 Clock Synchronization Initialization Example

The initialization procedure of clock synchronization including propagation delay measurement, offset compensation, filter reset, and drift compensation is shown in the following. After initialization, all DC slaves are synchronized with the Reference Clock.

1 Master reads the DL Status register of all slaves and calculates the network topology.

2 Master sends a broadcast write to Receive Time Port 0 register (at least first byte). All slaves latch the local time of the first preamble bit of this frame at all ports and at the ECAT Processing Unit.

3 Master waits until the broadcast write frame has returned.

4 Master reads all Receive Time Port 0-1 registers (depending on the topology) and the Receive Time ECAT Processing Unit register which contains the upper 32 bits of the receive times.

5 Master calculates individual propagation delays and writes them to System Time Delay registers of the slaves. Possible overruns of the 32 bit Receive Times have to be checked and taken into account.

6 Master sets System Time Offset register of the Reference Clock so that the Reference Clock is bound to the master time. The offset for the Reference Clock is master time minus Receive Time ECAT Processing Unit (local time) of the Reference Clock.

7 Master calculates System Time offsets for all DC slaves and writes them to the System Time Offset registers. The offset of each slave is Receive Time ECAT Processing Unit from Reference Clock minus Receive Time ECAT Processing Unit from each DC slave.

8 Master resets all slaves's Time Control Loop filters by writing to the Speed Counter Start register.

9 For static drift compensation, the master sends many separate ARMW or FRMW drift compensation frames (e.g., 15,000 frames) to distribute the System Time of the Reference Clock to all DC slaves.

10 For dynamic drift compensation, the master sends ARMW or FRMW commands periodically to distribute the System Time of the Reverence Clock to all DC slaves. The rate of the drift compensation commands depends on the acceptable maximum deviation.

48.5.7.4 SyncSignals and LatchSignals

ESCs with Distributed Clocks support generation of SyncSignals and time stamping of LatchSignals.

The SyncSignals can be used internally for interrupt generation (mapping to AL Event Request register and PDI IRQ)

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The SyncSignals can also be directly mapped to output signals (SYNC0/1) for use by external devices, e.g., as interrupt signals (less jitter than PDI IRQ, no interrupt source decoding).

The Latch Event unit supports time stamping of up to two LatchSignals (LATCH0/1, rising and falling edge separately), and time stamping of SyncManager events for debugging purposes.

The mapping of Distributed Clocks SyncSignals and LatchSignals to the external SYNC/LATCH signals is controlled by the setting of the Sync/Latch PDI Configuration register. The SYNC0/1 driver characteristics are also selected in this register. The SyncSignals are internally available for interrupt generation regardless of the Sync/Latch PDI Configuration. The mapping of SyncSignals to the AL Event Request register is also controlled by the Sync/Latch PDI Configuration register.

The length of a SyncSignal pulse is defined in the DC Pulse Length of SYNC Signals register. A value of 0 selects acknowledged modes.

The N32H7x5EC slave controller support power saving options (partly disabling DC units) controlled by two bits of the ESC Configuration register (bit 2, 3).

The Sync/Latch signals are not driven (high-impedance) by the N32H7x5EC slave controller until the SII EEPROM is successfully loaded. Take care of proper SyncSignal usage while the EEPROM is not loaded (e.g. pull-down/pull-up resistors).

48.5.7.4.1 SyncSignal Generation

The DC Cyclic Unit / Sync Unit supports the generation of a base SyncSignal SYNC0 and a dependent SyncSignal SYNC1. The SyncSignals can both be used internally and externally of the ESC. SyncSignals can be generated at a specific System Time. Four operation modes are supported: cyclic generation, single shot, cyclic acknowledge, and single shot acknowledge mode. The acknowledged modes are typically used for interrupt generation.

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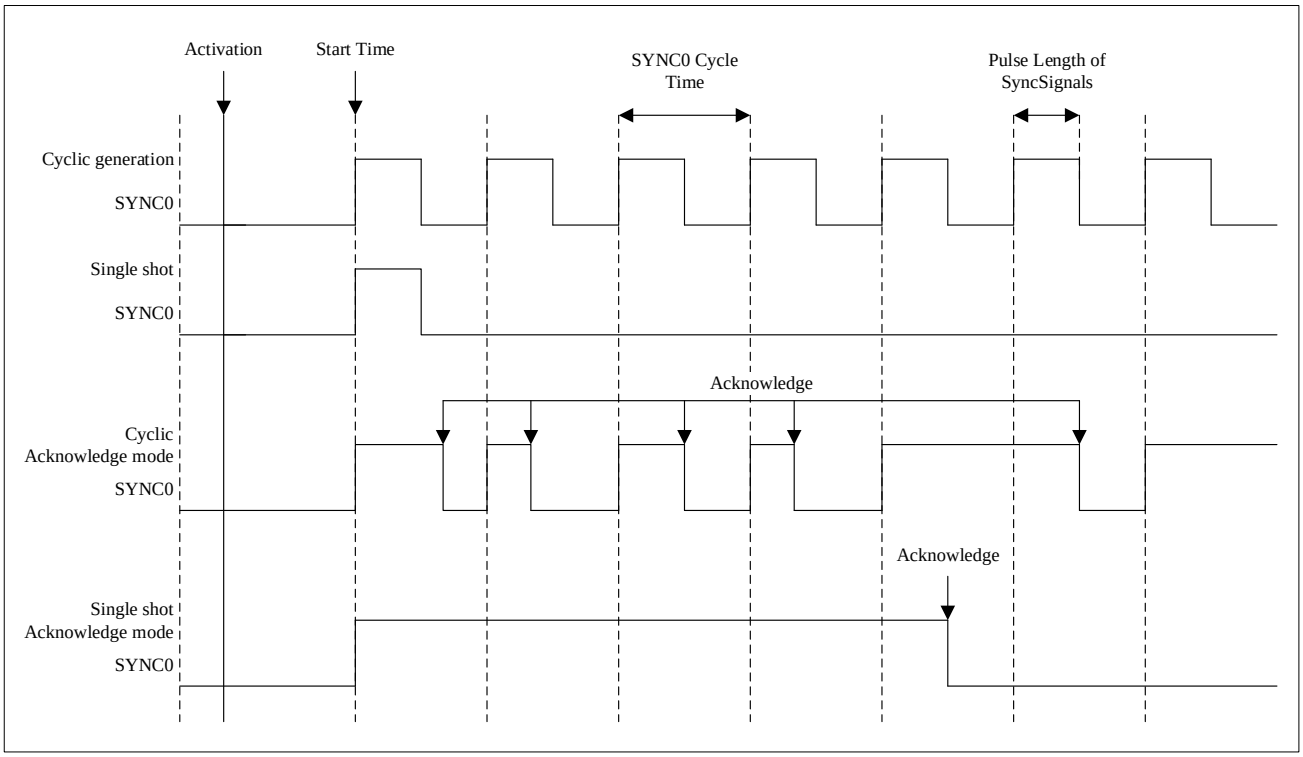
Figure 48-15 SyncSignal Generation Modes



The SyncSignal operation mode is selected by the configuration of the Pulse Length of SyncSignals register and the SYNC0 Cycle Time register.

The cycle time of the SYNC0 signal is configured in the SYNC0 Cycle Time register, the start time is set in the Start Time Cyclic Operation register. After the Sync Unit is activated and the output of the SYNC0/1 signals is enabled (DC Activation register), the Sync Unit waits until the start time is reached and generates the first SYNC0 pulse.

The N32H7x5EC slave controller support additional activation options like auto-activation when the Start Time is written, or 64 bit extension if only 32 bit of the Start Time is written. Other options are to detect invalid Start Times and provide debug output of SyncSignals.

Internally, the SyncSignals are generated with an update rate of 100 MHz (10 ns update cycle). The jitter of the internal SyncSignal generation in comparison to the local copy of the System Time is 12 ns.

Cyclic Generation

In Cyclic Generation mode, the Sync unit generates isochronous SyncSignals after the Start Time. The generation ends if the Cyclic Unit is deactivated or SYNC0/1 generation is deactivated. The Cycle times are determined by the SYNC0/1 Cycle Time registers. The Pulse Length of the SYNC signals has to be greater than 0. If the Pulse Length is greater than the Cycle Time, the SyncSignal will always be activated after the Start Time.

Single Shot Mode

In Single Shot mode (SYNC0 Cycle Time set to 0), only one SyncSignal pulse is generated after the Start Time is reached. Another pulse can only be generated by deactivating the Cyclic Unit (Set bit 0 of DC Activation register register to 0), reprogramming the Start Time, and reactivation of the Cyclic Unit.

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Cyclic Acknowledge Mode

The Cyclic Acknowledge mode is typically used for generation of isochronous interrupts. The acknowledged modes are selected by setting the Pulse Length of SYNC Signals to 0. Each SyncSignal pulse remains active until it is acknowledged – typically by a µController – by reading the appropriate SYNC0 or SYNC1 Status register. The first pulse is generated after the Start Time is reached, following pulses are generated when the next regular SYNC0/1 event would occur.

Single Shot Acknowledge Mode

In Single Shot Acknowledge mode (both Pulse Length of SYNC Signals and SYNC0 Cycle Time are 0), only one pulse is generated when the Start Time is reached. The pulse remains active until it is acknowledged by reading the appropriate SYNC0/1 Status registers. Another pulse can only be generated by deactivating the Cyclic Unit, re-programming the Start Time, and reactivation of the Cyclic Unit.

48.5.7.4.2 SYNC1 Generation

The second SyncSignal (SYNC1) depends on SYNC0, it can be generated with a predefined delay after SYNC0 pulses. The delay is configured in the SYNC1 Cycle Time register.

If the SYNC1 Cycle Time is larger than the SYNC0 Cycle Time, it will be generated as follows: when the Start Time Cyclic Operation is reached, a SYNC0 pulse is generated. The SYNC1 pulse is generated after the SYNC0 pulse with a delay of SYNC1 Cycle Time. The next SYNC1 pulse is generated when the next SYNC0 pulse was generated, plus the SYNC1 Cycle Time.

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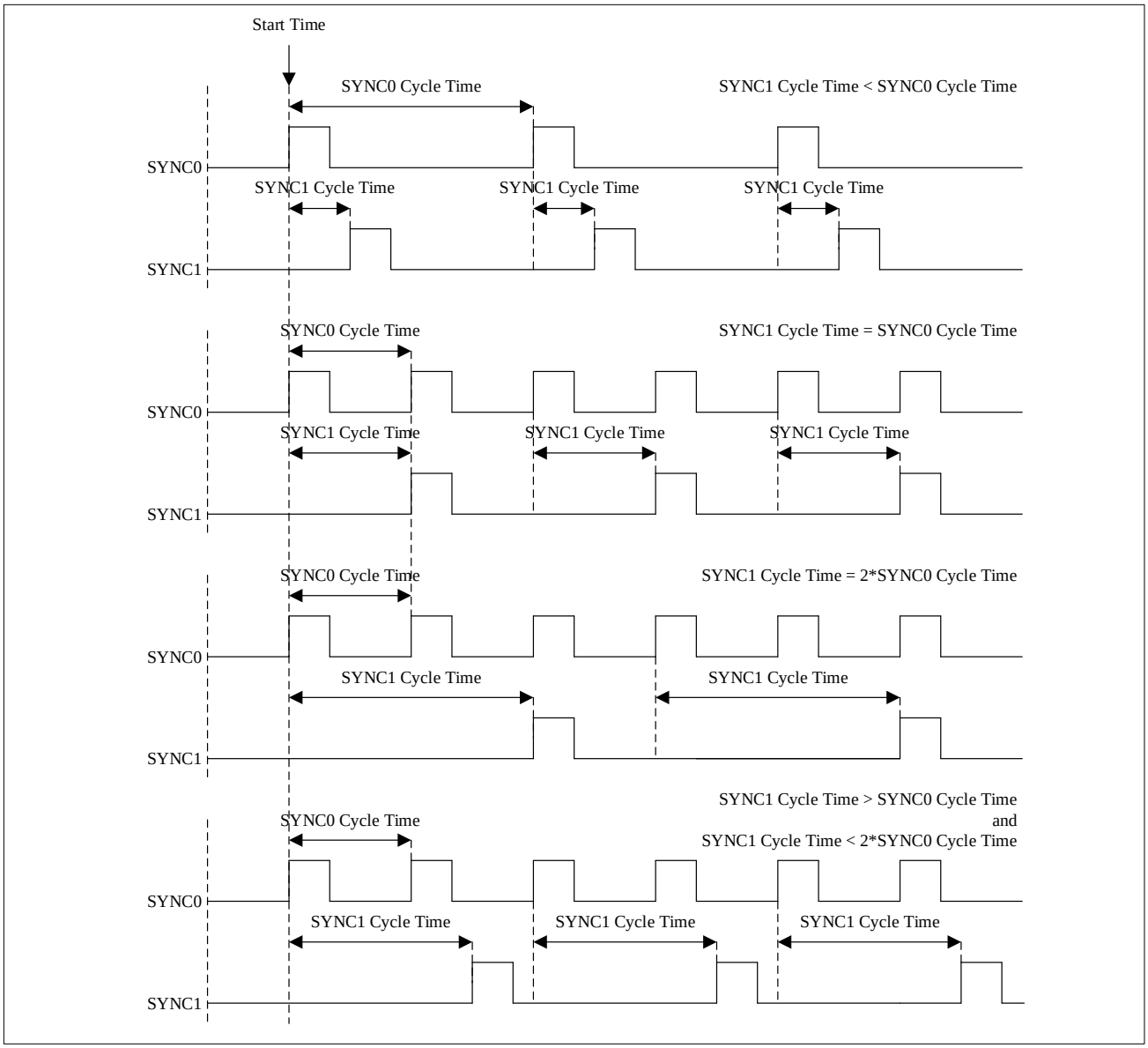
Figure 48-16 SYNC0/1 Cycle Time Examples



NOTE: If The SYNC1 Cycle Time is 0, SYNC1 reflects SYNC0.

48.5.7.4.3 SyncSignal Initialization Example

Refer to section 48.5.18.2 for the initialization process.

48.5.7.4.4 LatchSignals

The DC Latch Unit enables time stamping of LatchSignal events for two external signals, LATCH0 and LATCH1. Both rising edge and falling edge time stamps are recorded. Additionally, time stamping of SyncManager events is possible with the N32H7x5EC slave controller.

LatchSignals are sampled with a sample rate of 100 MHz, the corresponding time stamp has an internal jitter of 11 ns.

The state of the LatchSignals can be read from the Latch Status registers.

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The DC Latch Unit supports two modes: single event or continuous mode, configured in the Latch0/1 Control register.

Single Event Mode

In single event mode, only the timestamps of the first rising and the first falling edge of the LatchSignals are recorded. The Latch0/1 Status registers contain information about the events which already have occurred. The Latch0/1 Time Positive/Negative Edge registers contain the time stamps.

Each event is acknowledged by reading the corresponding Latch Time register. After reading the Latch Time register, the Latch unit is waiting for the next event. Latch events are mapped to the AL Event Request register in single event mode.

Continuous Mode

In continuous mode, each event is stored in the Latch Time registers. At reading, the time stamp of the last event is read. The Latch0/1 Status registers do not reflect the latch event states in continuous mode.

SyncManager Event

The N32H7x5EC slave controller support debugging of SyncManager interactions with time stamps for buffer events. The last event can be read out at the SyncManager Event Time registers (EtherCAT Buffer Change/PDI Buffer Start/PDI Buffer Change Event Time register), if the SyncManager is configured appropriately.

48.5.7.4.5 ECAT or PDI Control

The SyncSignal unit and the two LatchSignal units of the Distributed Clocks entity can be assigned independently by the master to be controlled either by ECAT or a local µController (PDI) using the Cyclic Unit Control register. With PDI control, a µController can e.g. set up cyclic interrupts for itself.

48.5.7.5 Communication Mode

Three communication modes are possible:

- Free Run

  EtherCAT Communication and application are running independently from each other.

- Synchronized to Output Event

  The slave application is synchronized to an Output event. If no Outputs are used the Input event is used for synchronization.

- Synchronized to SyncSignal

  Application is synchronized to the SyncSignal.

48.5.8 EtherCAT State Machine

The EtherCAT State machine (ESM) is responsible for the coordination of master and slave applications at start up and during operation. State changes are typically initiated by requests of the master. They are acknowledged by the local application after the associated operations have been executed. Unsolicited state changes of the local application are also possible.

There are four states an EtherCAT slave shall support, plus one optional state:

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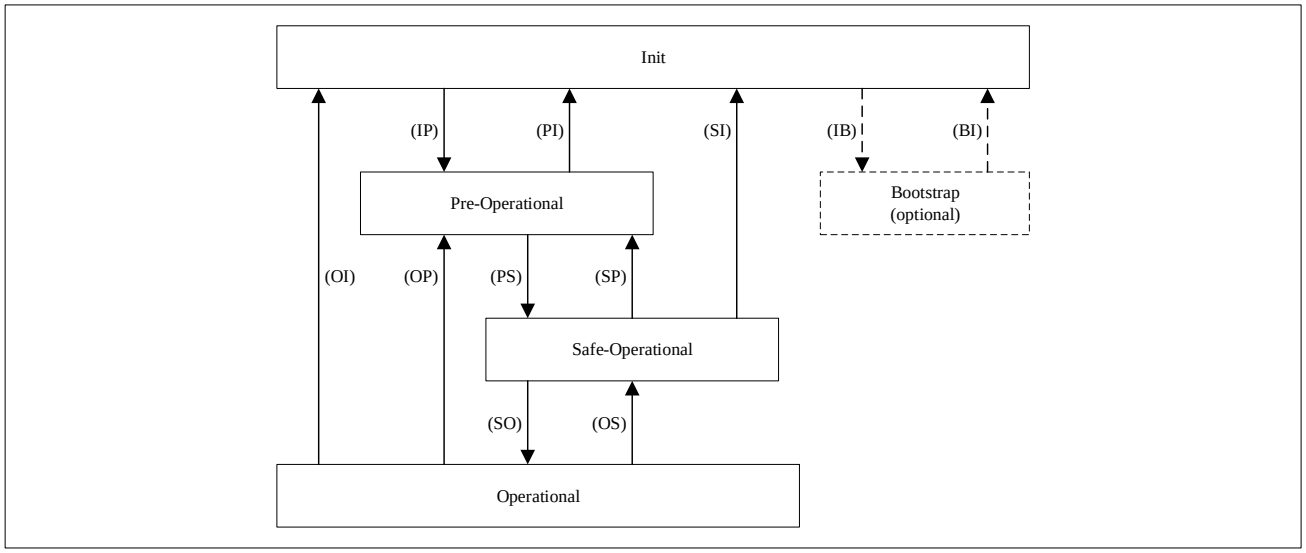
- Init (state after Reset)
- Pre-Operational
- Safe-Operational
- Operational
- Bootstrap (optional)

The states and the allowed state changes are shown in Figure 48-17:

Figure 48-17 EtherCAT State Machine



NOTE: Not all state changes are possible, e.g., the transition from 'Init' to 'Operational' requires the following sequence: Init → Pre-Operational → Save-Operational → Operational.

Each state defines required services. Before a state change is confirmed by the slave all services required for the requested state have to be provided or stopped respectively.

For more details please refer to the EtherCAT Technology Group website (http://www.ethercat.org).

The state machine is controlled and monitored via registers within the ESC. The master requests state changes by writing to the AL Control register. The slave indicates its state in the AL Status register and puts error codes into the AL Status Code register.

48.5.9 Memory Space

The memory space of the N32H7x5EC Slave Controller consists of two blocks: the first for registers and user RAM, and the second for process data RAM. The distribution of each portion of the address space is shown in Figure 48-18.

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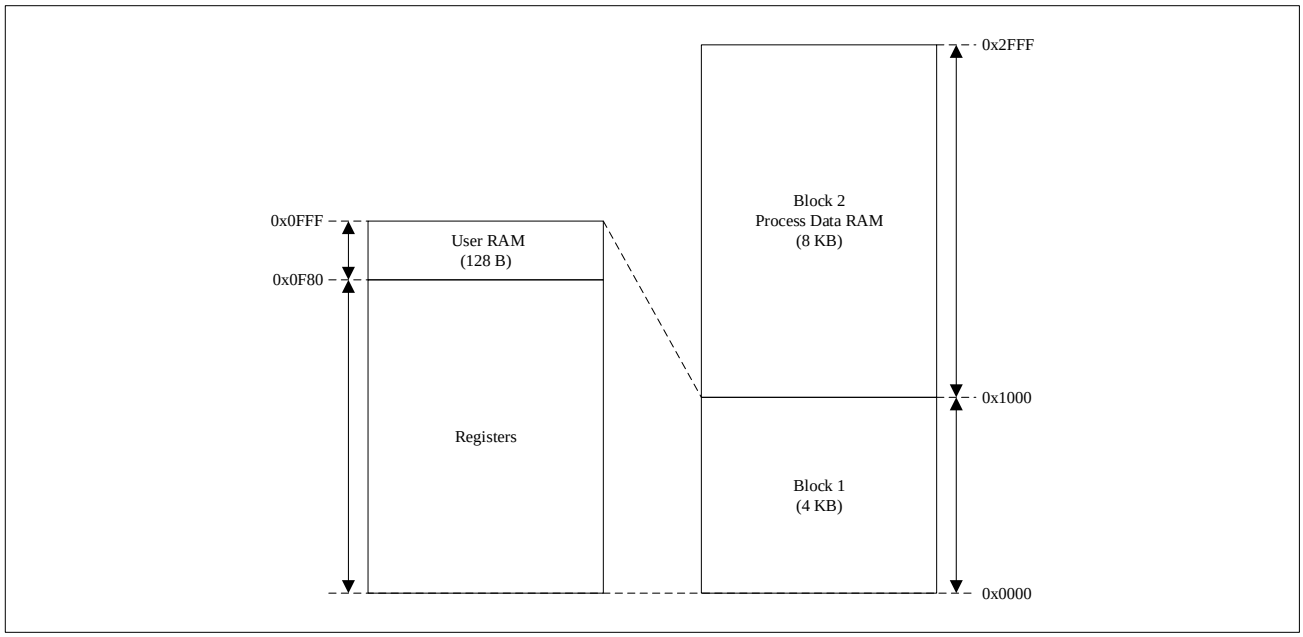
Figure 48-18 Memory Address Space Overview



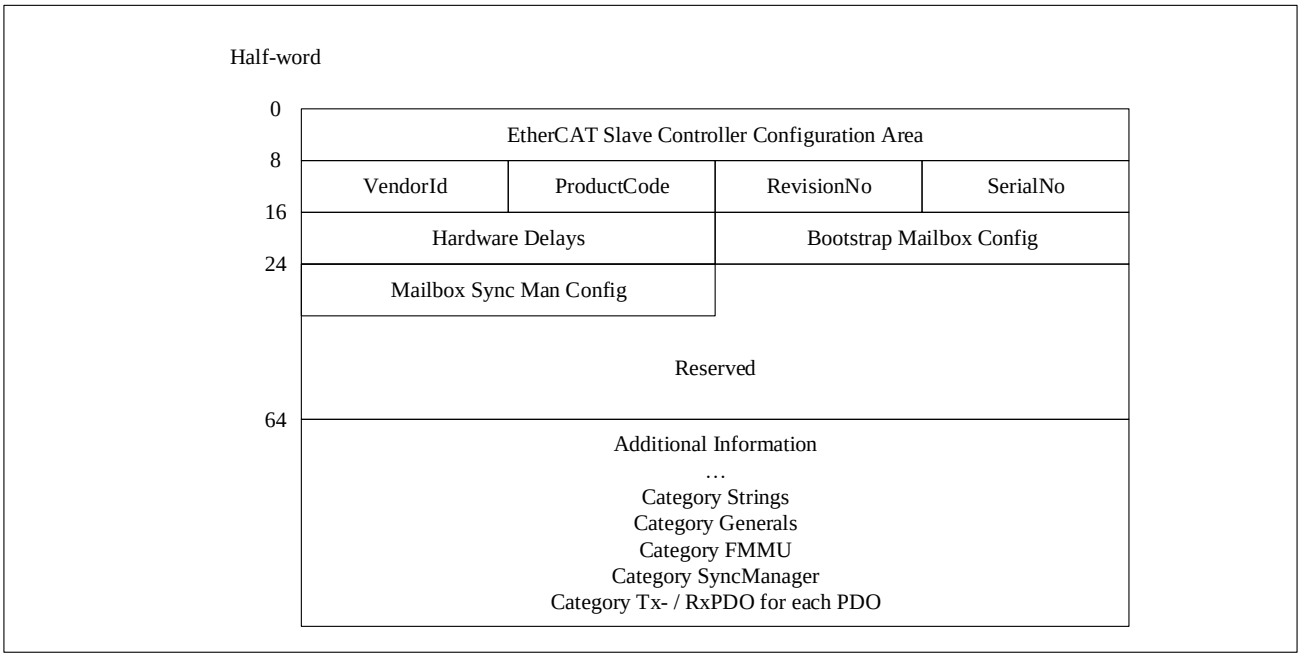
NOTE: The addresses in the figure are offset addresses and the ESC start address is: 0x400B 0000.

48.5.10 SII EEPROM

EtherCAT slave controllers use a mandatory NVRAM (typically a serial EEPROM with I²C interface) to store EtherCAT Slave Information (ESI). The N32H7x5EC slave controller supports EEPROM sizes up to 1Mbit.

The EEPROM structure is shown in Figure 48-19. The ESI uses half-word (16 bits) addressing.

Figure 48-19 SII EEPROM Layout



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At least the information stored in the address range from half-word 0 to 63 (0x00 to 0x3F) is mandatory.

48.5.10.1 SII EEPROM Content

The ESC Configuration Area (EEPROM half-word addresses 0 to 7) is automatically read by the ESC after power-on or reset. It contains the PDI configuration, DC settings, and the Configured Station Alias. The consistency of the ESC Configuration data is secured with a checksum.

The EtherCAT master can invoke reloading the EEPROM content. In this case the Configured Station Alias register and ESC Configuration register bit1,4,5,6,7 (enhanced link detection) are not transferred into the registers, they are only transferred at the initial EEPROM loading after power-on or reset.

The ESC Configuration Area is shown in Table 48-9.

Table 48-9 ESC Configuration Area

Half-Word Address	Parameter	Description	Register Offset Address
0x0	PDI Control/ESC Configuration	Initialization value for PDI Control register (EEPROM ADR bit9 is also mapped to ESC DL Status register bit2)	0x0140:0x0141
0x1	PDI Configuration	Initialization value for PDI Configuration register	0x0150:0x0151
0x2	Pulse Length of SYNC Signals	Initialization value for Pulse Length of SYNC Signals register	0x0982:0x0983
0x3	Extended PDI Configuration	Initialization value for extended PDI Configuration register	0x0152:0x0153
0x4	Configured Station Alias	Initialization value for Configured Station Alias Address register	0x0012:0x0013
0x5	Reserved	Reserved, shall be zero	-
0x6	Reserved	Reserved, shall be zero	-
0x7	Checksum	Low byte contains remainder of division of 0x0 to 0x6 as unsigned number divided by the polynomial x^8+x^2+x+1 (initial value 0xFF)	-

NOTE: Reserved words or reserved bits of the ESC Configuration Area should be filled with 0.

An excerpt of the SII EEPROM content following the ESC Configuration area is shown in Table 48-10.

Table 48-10 SII EEPROM Content Excerpt

Half-Word Address	Parameter	Half-Word Address	Parameter
0x8:0x9	Vendor ID	0x1C	Mailbox Protocol
0xA:0xB	Product Code	0x1D:0x1F	Reserved
0xC:0xD	Revision Number	0x20:0x22	Vendor specific
0xE:0xF	Serial Number	0x23:0x27	Reserved
0x10:0x13	Reserved	0x28:0x2F	Additional ESC configuration
0x14	Bootstrap Receive Mailbox Offset	0x30:0x3D	Reserved
0x15	Bootstrap Receive Mailbox Size	0x3E	Size
0x16	Bootstrap Send Mailbox Offset	0x3F	Version
0x17	Bootstrap Send Mailbox Size	0x40	Category header
0x18	Standard Receive Mailbox Offset	0x41	Category Word Size
0x19	Standard Receive Mailbox Size	0x42	Category Data

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Half-Word Address	Parameter	Half-Word Address	Parameter
0x1A	Standard Send Mailbox Offset	…	Second Category header …
0x1B	Standard Send Mailbox Size		

48.5.10.2 SII EEPROM Logical Interface

The SII EEPROM interface of the ESC is either controlled by EtherCAT or by the PDI. Initially, EtherCAT has EEPROM interface access, but it can transfer access to the PDI.

The EEPROM interface supports three commands: write to one EEPROM address (16 bits), read from EEPROM (32 bits), or reload ESC configuration from EEPROM.

48.5.10.2.1 SII EEPROM Errors

The ESC retries reading the EEPROM after power-on or reset once if an error has occurred (missing acknowledge, wrong checksum). If reading the ESC Configuration Area fails twice, the Error Device Information bit is set, and the PDI Operational bit in the ESC DL Status register remains clear and the EEPROM_Loaded signal (if available) remains inactive. The process memory is not accessible until the ESC Configuration Area is loaded successfully.

All registers initialized by the ESC Configuration Area keep their values in case of an error. This is also true for the Error Device Information bit as well as the PDI Operational bit. Only if the EEPROM was loaded/reloaded successfully, the registers take over the new values (except for Configured Station Alias register and ESC Configuration register's bit 1, 4, 5 – enhanced link detection).

48.5.10.2.2 SII EEPROM Interface Assignment to ECAT/PDI

The EtherCAT master controls the EEPROM interface (default) if EEPROM configuration register's bit 0 is 0 and EEPROM PDI Access State register's bit 0 is 0, otherwise PDI controls the EEPROM interface. These access rights should be checked by both sides before using the EEPROM Interface.

A typical EEPROM interface control hand-over is as follows:

1 ECAT assigns EEPROM interface to PDI by writing EEPROM configuration register's bit 0 to 1.

2 If PDI wishes to access EEPROM, it takes over EEPROM control by writing EEPROM PDI Access State register's bit 0 to 1.

3 PDI issues EEPROM commands.

4 After PDI has finished EEPROM commands, PDI releases EEPROM control by writing EEPROM PDI Access State register's bit 0 to 0.

5 ECAT may take back the EEPROM interface by writing EEPROM configuration register's bit 0 to 0.

6 ECAT checks EEPROM control by reading EEPROM PDI Access State register.

7 ECAT issues EEPROM commands.

If the PDI does not release EEPROM control (e.g. because of a software failure), ECAT can force releasing the access:

1 ECAT writes 0x02 to EEPROM configuration register (as the result, EEPROM PDI Access State register's bit 0 is cleared).

2 ECAT writes 0x00 to EEPROM configuration register.

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3 ECAT has control over EEPROM interface.

48.5.10.2.3 Read/Write/Reload Example

The following steps have to be performed for an SII EEPROM read or write access:

1 Check if the "Busy" bit of the EEPROM Status register is cleared (EEPROM Control/Status register's bit 15 is 0) and the EEPROM interface is not busy, otherwise wait until the EEPROM interface is not busy anymore.

2 Check if the Error bits of the EEPROM Status register are cleared. If not, write "000" to the command register (EEPROM Control/Status register's bits [10:8]).

3 Write EEPROM word address to EEPROM Address register.

4 Write command only: put write data into EEPROM Data register (2 Bytes only).

5 Issue command by writing to Control register.

- For a read command, write "001" into EEPROM Control/Status register's bits [10:8].
- For a write command, write 1 into EEPROM Control/Status register's bit 0 (Write Enable) and "010" into EEPROM Control/Status register's bits [10:8]. Both bits have to be written in one frame. The Write enable bit realizes a write protection mechanism. It is valid for subsequent EEPROM commands issued in the same frame and self-clearing afterwards. The Write enable bit needs not to be written from PDI if it controls the EEPROM interface.
- For a reload command, write "100" into EEPROM Control/Status register's bits [10:8].

6 The command is executed after the EOF if the EtherCAT frame had no errors. With PDI control, the command is executed immediately.

7 Wait until the "Busy" bit of the EEPROM Status register is cleared.

8 Check the Error bits of the EEPROM Status register. The Error bits are cleared by clearing the command register. Retry command (back to step 5) if EEPROM acknowledge was missing. If necessary, wait some time before retrying to allow slow EEPROMs to store the data internally.

9 For a Read command: Read data is available in EEPROM Data registers (4 Bytes only).

For a Reload command: ESC configuration is reloaded into appropriate registers.

NOTE: The Command register bits are self-clearing. Manually clearing the command register will also clear the status information.

48.5.10.3 SII EEPROM Electrical Interface

The SII EEPROM Interface is intended to be a point-to-point interface between the ESC and the I²C EEPROM. If other I²C masters are required to access the I²C bus, the ESC must be held in reset state (e.g. for in-circuit-programming of the EEPROM), otherwise access collisions are possible.

Both EEPROM_CLK and EEPROM_DATA must have a pull-up resistor (4.7 kΩ recommended).

48.5.10.3.1 Addressing

EtherCAT and ESCs use half-word (16 bits) addressing when accessing the EEPROM, although the I²C interface actually uses byte addressing. The lowest address bit A[0] is added internally by the EEPROM interface controller

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of the ESCs. I.e., the EEPROM Address register reflects the physical EEPROM Address bits A[18:1] (higher address bits are reserved/are zero).

SII EEPROM half-word 0 is typically located at I²C address 0, i.e., the I²C device address has to be set to 0.

48.5.10.3.2 Write Access

An EEPROM write access always writes one half-word (2 bytes) to the EEPROM. In this case, page boundaries are not relevant, because they will not be violated.

48.5.10.3.3 Read Access

An EEPROM read access reads two half-words (4 bytes) from the EEPROM, the load or reload EEPROM access typically reads 8 half-words (16 bytes). The address wraparound at the end of the EEPROM address space has to be taken into account by the application; the ESC has no knowledge about it.

48.5.11 Interrupts

ESCs support two types of interrupts: AL Event Requests targeted at a µController, and ECAT event requests targeted at the EtherCAT master. Additionally, the Distributed Clocks SyncSignals can be used as interrupts for a µController as well.

48.5.11.1 AL Event Request (PDI Interrupt)

AL Event Requests can be signaled to a µController using the PDI Interrupt Request signal (IRQ, etc.). For IRQ generation, the AL Event Request register is combined with the AL Event Mask register using a logical AND operation, then all resulting bits are combined (logical OR) into one interrupt signal. The output driver characteristics of the IRQ signal are configurable using the SYNC/LATCH PDI Configuration register. The AL Event Mask register allows for selecting the interrupts which are relevant for the µController and handled by the application.

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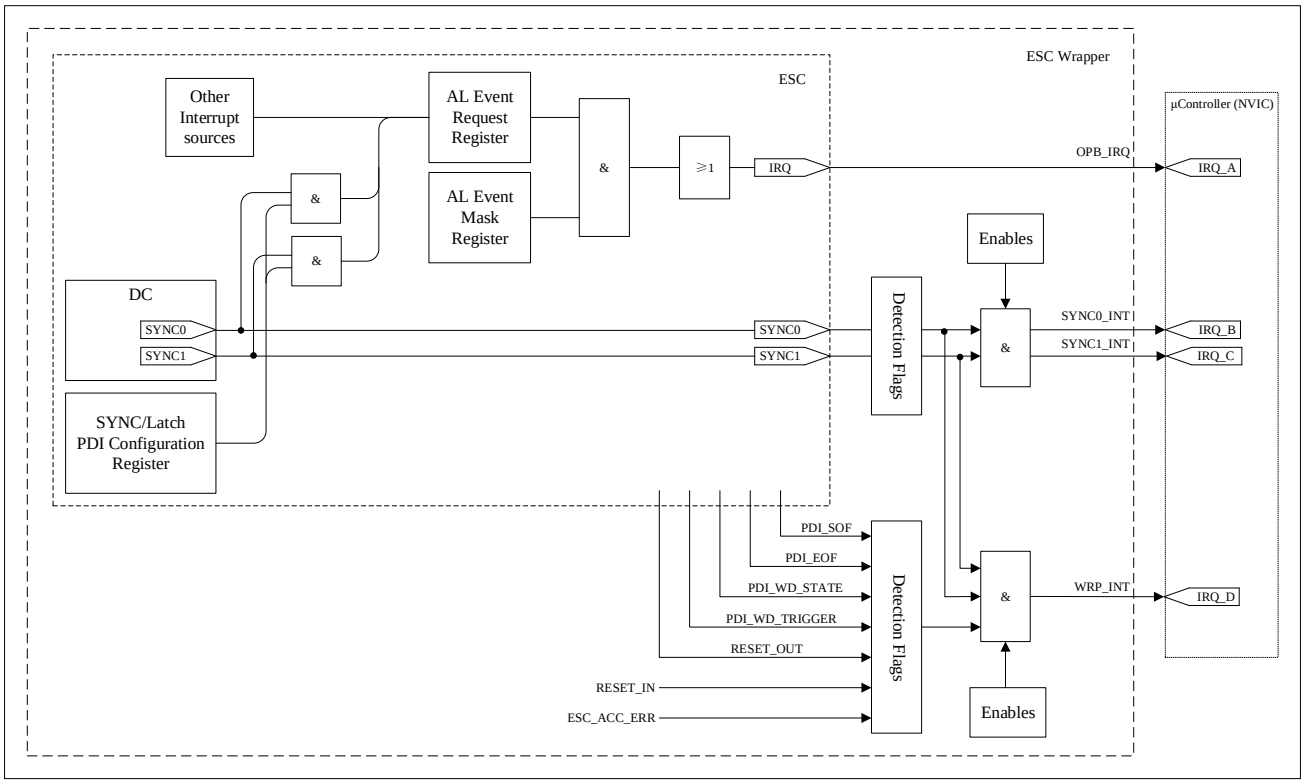
Figure 48-20 PDI Interrupt Masking and interrupt signals



NOTE: IRQ_A, IRQ_B, IRQ_C and IRQ_D indicate interrupts ECAT_OPB_IRQ, ECAT_SYNC0_INT, ECAT_SYNC1_INT and ECAT_WRP_INT connected to the NVIC, respectively.

The DC SyncSignals can be used for interrupt generation in two ways:

- The DC SYNC signals are mapped into the AL Event Request Register (configured with SYNC/LATCH PDI Configuration register's bit 3, 7). In this case, all interrupts from the ESC to the µController are combined into one IRQ signal, and the Distributed Clocks LATCH0/1 inputs can still be used. The IRQ signal has a jitter of ~40 ns.
- The DC SyncSignals are directly connected to µController interrupt inputs. The µController can react on DC SyncSignal interrupts faster (without reading AL Request register), but it needs more interrupt inputs. The jitter of the SyncSignals is ~12 ns. The DC Latch functions are only available for one Latch input or not at all (if both DC SYNC outputs are used).

48.5.11.2 ECAT Event Request (ECAT Interrupt)

ECAT event requests are used to inform the EtherCAT master of slave events. ECAT events make use of the IRQ field inside EtherCAT datagrams (see 48.5.1.2). The ECAT Event Request register is combined with the ECAT Event Mask register using a logical AND operation. The resulting interrupt bits are combined with the incoming ECAT IRQ field using a logical OR operation, and written into the outgoing ECAT IRQ field. The ECAT Event Mask register allows for selecting the interrupts which are relevant for the EtherCAT master and handled by the master application.

NOTE: The master cannot distinguish which slave (or even more than one) was the origin of an interrupt.

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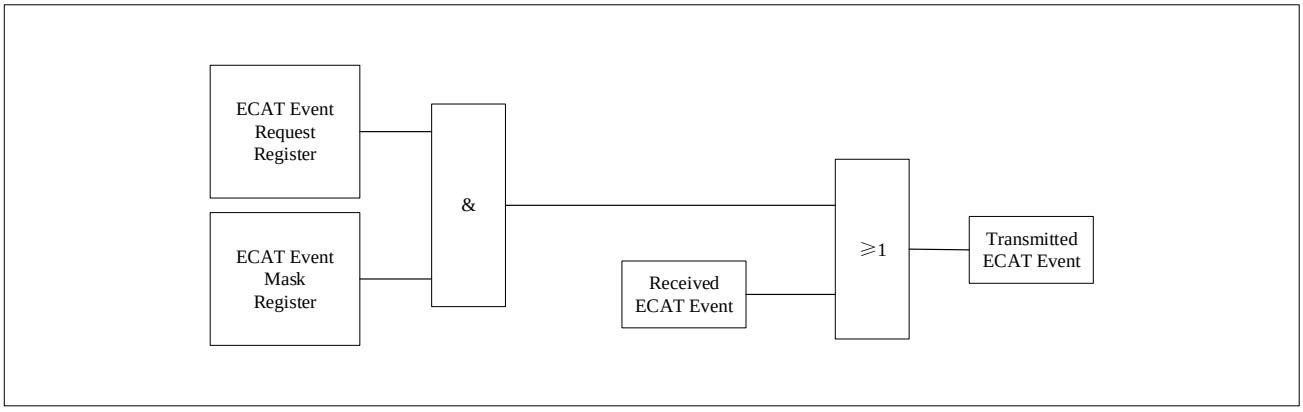
Figure 48-21 ECAT Interrupt Masking



48.5.12 Watchdogs

The ESCs support up to two internal watchdogs (WD), a Process Data watchdog used for monitoring process data accesses, and a PDI watchdog monitoring PDI activity.

The timeout for both watchdogs can be configured individually, but they share a single Watchdog Divider (WD_DIV, Watchdog Divider register). The watchdog timeout is calculated from the Watchdog Divider settings multiplied with the Watchdog Time settings for PDI (WD_PDI, Watchdog Time PDI register) or Process Data (WD_PD, Watchdog Time Process Data register). Base time unit is 40 ns. The Watchdog timeout jitters, the jitter depends on the Watchdog Divider settings. I.e., selecting smaller Watchdog Divider settings results in smaller jitter.

The following equations are used for a quick estimation of the watchdog timeout (they are not exact in terms of nanoseconds):

$$t_{\mathrm{WD_Div}} = (\mathrm{WD_DIV} + 2) * 40ns$$

$$t_{\mathrm{WD_PDI}} = \left[t_{\mathrm{WD_Div}} * \mathrm{WD_PDI};\ \ t_{\mathrm{WD_Div}} * \mathrm{WD_PDI} + t_{\mathrm{WD_Div}}\right]$$

$$t_{\mathrm{WD_PD}} = \left[t_{\mathrm{WD_Div}} * \mathrm{WD_PD};\ \ t_{\mathrm{WD_Div}} * \mathrm{WD_PD} + t_{\mathrm{WD_Div}}\right]$$

48.5.12.1 Process Data Watchdog

The Process Data watchdog is rewound (triggered) by a write access to a SyncManager buffer area if the SyncManager is configured to generate a watchdog trigger signal (Set SyncManager Control register's bit 6 for SyncManager 0, etc.). The watchdog trigger signal is generated after the buffer was completely and successfully written (similar to the Interrupt Write of a SyncManager).

The Process Data watchdog can be disabled by setting the Process Data Watchdog Time to 0.

A timeout of the Process Data watchdog has these consequences:

- Watchdog Status Process Data register's bit 0 reflects the watchdog status.
- The Watchdog Counter Process Data register is incremented.

48.5.12.2 PDI Watchdog

The PDI watchdog is rewound (triggered) by any correct read or write access by the PDI. The PDI watchdog can be disabled by setting the PDI Watchdog Time to 0.

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A timeout of the PDI watchdog has these consequences:

- ESC DL Status register's bit 1 reflects the watchdog status. This can be mapped to the ECAT Interrupt to inform the master.
- The Watchdog Counter PDI register is incremented.

48.5.13 Error Counters

The ESCs have numerous error counters which help in detecting and locating errors. All error counters are saturated at 0xFF (no wrap-around) and they are cleared individually or group-wise by writing any value to them.

Table 48-11 Error Counter Overview

Error Counter		Register	Description
Port 0/1 Error Counters	Invalid Frame Counter	ESC_RXERRCNTn (Low 8 bits)	Invalid frame initially detected (includes RX Errors)
	RX Error Counter	ESC_RXERRCNTn (High 8 bits)	Physical layer RX Errors (inside/outside frame): MII: RX_ER
Forwarded RX Error Counter		ESC_FWDRXERRCNTn	Invalid frame with marking from previous ESC detected (per port)
ECAT Processing Unit Error Counter		ESC_EPUERRCNT	Invalid frame passing the EtherCAT Processing Unit (additional checks by processing unit)
PDI Error Counter		ESC_PDIERRCNT	Physical Errors detected by the PDI
Lost Link Counter		ESC_LOSTLINKCNTn	Link lost events (per port), counts only if port is in Auto or Auto close mode
Watchdog Counter Process Data		ESC_WDCNTPD	Watchdog timeout events
Watchdog Counter PDI		ESC_WDCNTPDI	Watchdog timeout events

NOTE: Some errors will be counted in multiple registers. E.g., a physical layer RX Error received at port 0 is counted in RX Error Counter register and ECAT Processing Unit Error Counter register. A forwarded error received at port 0 is counted in Forwarded RX Error Counter register and ECAT Processing Unit Error Counter register.

48.5.13.1 Frame error detection

EtherCAT frame error detection takes place at three functional blocks, at the physical layer (device), inside the Auto-Forwarder and inside the EtherCAT Processing Unit. The following errors are detected and counted in these registers:

Table 48-12 Errors and corresponding error counters

Error type	RX Error counter Register	Invalid frame counter Register	Forwarded error counter Register	ECAT Processing Unit error counter Register
Physical layer error MII/RMII: RX_ER event	yes	if inside frame only	no	EPU inbound port only
FIFO overrun/underrun	no	yes	no	EPU inbound port only
Frames without Ethernet SOF	no	yes	no	EPU inbound port only
Too long frames (> ~	no	yes	no	EPU inbound port only

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Error type	RX Error counter Register	Invalid frame counter Register	Forwarded error counter Register	ECAT Processing Unit error counter Register
2000 Byte)				
CRC error without odd nibble	no	yes	no	EPU inbound port only
CRC error with odd nibble	no	no	yes	EPU inbound port only
Too short frames (< 64 Byte)	no	no	no	EPU inbound port only
EtherCAT frame length errors (e.g., frame ends although more header/data bytes are expected, padding > 64 Byte)	no	no	no	EPU inbound port only
Non-EtherCAT frames if ESC DL Control register's bit 0 is 1	no	no	no	EPU inbound port only
Circulating bit=1 and port 0 automatically closed	no	no	no	EPU inbound port only

Any of the above errors will have these consequences:

- The frame transmission is aborted (a frame with an RX Error at the beginning is truncated). The CRC of the transmitted data is modified (or appended) so that it becomes bad. A special marking for Forwarded Errors is added.
- The EtherCAT Processing Unit discards register operations, e.g., write operations to registers, SyncManager buffer changes, etc. RAM areas will be written, because they do not have a shadow buffer for write data like registers.
- Error counters are increased.

48.5.13.2 Errors and Forwarded Errors

The ESCs distinguish errors initially detected by an ESC and forwarded errors detected by a previous ESC. This is useful for error location when interpreting the RX Error/Forwarded RX Error counters.

The first device detecting an error (e.g., a CRC error or an RX Error of the physical layer), will discard register operations and count a port error. The outgoing frame gets a special marking, consisting of one extra nibble added after the (invalid) CRC.

A device receiving a frame with a CRC error and an additional nibble will also discard register operations, but it will count one Forwarded RX Error instead of a normal port error.

NOTE: A forwarded error is sometimes called "green error", the initial error is sometimes called "red error". A physical layer RX Error is always a "red error", because it could not have been forwarded.

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48.5.14 LED Signals (Indicators)

EtherCAT slave controllers support different LEDs regarding link state and AL status. For details about EtherCAT indicators refer to the ETG.1300 EtherCAT Indicator and Labeling Specification, available from the download section of the EtherCAT Technology Group website (http://www.ethercat.org).

48.5.14.1 RUN LED

The AL status is displayed with the RUN LED (green). The RUN output of an ESC is controlled by the AL Status register and supports the following states, which are automatically translated into blink codes:

Table 48-13 RUN LED state indication

RUN LED	Description
Off	The device is in state INIT
Blinking (slow)	The device is in state PRE-OPERATIONAL
Single Flash	The device is in state SAFE-OPERATIONAL
On	The device is in state OPERATIONAL
Flickering (fast)	The device is in state BOOTSTRAP or loading the SII EEPROM

The N32H7x5EC slave controller support optional RUN LED outputs by overriding the state indication of the RUN LED. The output can be set by master or local application. This can be used e.g. for locating a specific slave by forcing the RUN LED to indicate a triple flash (Device Identification).

The RUN LED override is disabled automatically by a following ESM state change.

48.5.14.2 ERR LED

The ERR LED indicates local errors and application errors. It is either connected to the application controller or to the ESC (optional ESC feature). If it is connected to the ESC, some errors are automatically indicated by the ESC, other error states are detected by the application controller and indicated by writing to the ERR LED Override register.

The following ERR LED states can be automatically generated by an ESC, without interaction of an application controller. The support of individual error states is ESC specific.

Table 48-14 Automatic ESC ERR LED state indication

ERR LED	Description
Off	No error
Flickering (fast)	SII EEPROM loading error
Blinking (slow)	Invalid hardware configuration
Single Flash	AL Status register Error Indication bit is set while device emulation is disabled. E.g., if the µController makes a state change with Error Indication bit set after a Process Data Watchdog Timeout, it has to manually set the ERR LED to Double Flash again (otherwise the ESC would generate a Single Flash due to the Error Indication bit automatically)
Double Flash	Process Data Watchdog timeout (edge detected) while device is OPERATIONAL
On	PDI Watchdog timeout (edge detected) or Build-In self-test error

The ERR LED override is disabled automatically if an error is detected by the ESC which is associated with an ERR LED blink code.

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48.5.14.3 STATE LED and STATE_RUN LED Signal

The STATE LED is a bicolor-LED combining RUN and ERR LED. Since the RUN LED part of the STATE LED must be turned off while the ERR LED part is active, the RUN and ERR LED signals cannot be simply combined to drive the bicolor LED. The N32H7x5EC slave controller support a STATE_RUN signal, which is turned off while ERR LED is on, so STATE_RUN and ERR signals can be used to drive the bicolor STATE LED. Otherwise the logical combination “RUN and not (ERR)” has to be used to control the RUN LED part of the STATE LED.

48.5.14.4 LINKACT LED

The Link/Activity state of each port is displayed with the LINKACT LED (green).

Table 48-15 LINKACT LED States

LINKACT LED	Description
Off	No link
Blinking	Link and activity
On	Link without activity

It is highly recommended to use the LINKACT LED signals of the ESCs for driving visible LEDs, instead of the Link/Activity LED signals of the PHY, because the ESC signals reflect the actual link/activity state of the device – not only the state of the PHYs.

The LINKACT LED indicates the link status after evaluation of the Enhanced link detection plus MI link detection and configuration, it corresponds with the ESC DL Status register (bit 11, 9 – Communication established).

48.5.15 Process Data Interface (PDI)

The Process Data Interface (PDI) realizes the connection between slave application and ESC. The N32H7x5EC slave controller supports the following PDI types: on-chip bus. It is connected to the AHB through an AHB-to-OPB bridge. See Figure 48-1.

48.5.15.1 PDI Selection and Configuration

Typically, the PDI selection and configuration is part of the ESC Configuration Area of the SII EEPROM.

The N32H7x5EC slave controller have the PDI selected and configured at power-on time. In this case, the ESC Configuration Area should reflect the actual settings, although they are not evaluated by the ESC itself.

The PDI of the N32H7x5EC slave controller is active after reset is released, which enables e.g. EEPROM emulation by a µController.

Take care of Digital Output signals and DC SyncSignals while the EEPROM is not loaded to achieve proper output behavior.

48.5.15.2 PDI register function acknowledge by write

Some ESC functions are triggered by writing or reading individual byte addresses, e.g., SyncManager buffer change or AL event request acknowledge. With an increasing data bus width of the µControllers, this can lead to restrictions or even problems.

Consider a SyncManager buffer area from 0x1000-0x1005. A 32 bit µController application might read the buffer

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Email: sales@nsing.com.sg

byte-wise. The first access to 0x1000 would open the buffer, and it would also read 0x1001-0x1003. The second access would read 0x1001, and also 0x1000/0x1002-0x1003. The problem occurs when address 0x1004 is to be read, because this would also read 0x1005. The data of 0x1005 is discarded, but the buffer is closed. When the µC reads 0x1005, it will always get 0 – the data seems to be corrupted. A similar issue occurs for DC SyncSignal acknowledging (registers 0x098E and 0x098F). A 32 bit µController would always acknowledge SYNC0 and SYNC1 at the same time, it is not possible to acknowledge them separately.

This problem can be overcome by enabling PDI register function acknowledge by write. In this mode, all functions which are originally triggered by read access are now triggered by corresponding write accesses – which use byte enables and thus can be restricted to certain bytes.

The current status has to be checked by the µController application in PDI information register 0x014E [0], before using this function.

This feature affects reading of SyncManager buffers and reading of certain registers from PDI side. There is no change to the EtherCAT master side at all. Refer to chapter 48.5.6 for SyncManager behavior. The following registers are affected by the PDI register function acknowledge by write feature:

Table 48-16 Functions/registers affected by PDI register function acknowledge by write

Address	Name	Trigger function
Any	SyncManager buffer end address	Read SyncManager buffer, then write to buffer end address to acknowledge buffer reading.
0x0120:0x0121	AL Control	Read 0x0120:0x0121 after AL Control changes, then write to 0x0120 to acknowledge reading.
0x0440	Watchdog Status Process Data	Read 0x0440, then write to 0x0440 to clear AL event request 0x0220 [6].
0x0806+y*16	SyncManager Activate	Read 0x0806+y*16, then write to 0x0806 (SyncManager 0) only to clear AL event request 0x0220 [4] for all SyncManagers.
0x098E	SYNC0 Status	Read 0x098E, then write to 0x098E to acknowledge DC Sync0 Status 0x098E [0].
0x098F	SYNC1 Status	Read 0x098E, then write to 0x098E to acknowledge DC Sync1 Status 0x098F [0].
0x09B0:0x09B7	Latch0 Time Positive Edge	Read 0x09B0:0x09B7, then write to 0x09B0 to clear DC Latch0 Status 0x09AE [0].
0x09B8:0x09BF	Latch0 Time Negative Edge	Read 0x09B8:0x09BF, then write to 0x09B8 to clear DC Latch0 Status 0x09AE [1]
0x09C0:0x09C7	Latch1 Time Positive Edge	Read 0x09C0:0x09C7, then write to 0x09C0 to clear DC Latch1 Status 0x09AF [0]
0x09C8:0x09CF	Latch1 Time Negative Edge	Read 0x09C8:0x09CF, then write to 0x09C8 to clear DC Latch1 Status 0x09AF [1]

48.5.16 Write Protection

48.5.16.1 Register Write Protection

With register write protection, only the register areas with offset addresses from 0x0000 to 0x0F7F are write protected

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(except for the two registers with offset addresses 0x0020 and 0x0030). User RAM (0x0F80:0x0FFF) and Process Data RAM (0x1000:0x2FFF) are not protected.

If register write protection is enabled (set Register Write Protection register's bit 0 to 1), the Register Write Enable register's bit 0 has to be set in the same frame before any register write operations. This is also true for disabling the register write protection. Otherwise, write operations to registers are discarded.

48.5.16.2 ESC Write Protection

ESC write protection disables write operations to any memory location (except for the two registers with offset addresses 0x0020 and 0x0030).

If ESC write protection is enabled (set ESC Write Protection register's bit 0 to 1), the ESC Write Enable register's bit 0 has to be set in the same frame before any write operations. This is also true for disabling the ESC write protection as well as the register write protection. Otherwise, write operations are discarded.

NOTE: If both register write protection and ESC write protection are enabled (not recommended), both enable bits have to be set before the write operations are allowed.

48.5.17 ESC Reset

The N32H7x5EC slave controller can issue a hardware reset via the EtherCAT master or even the PDI. A special sequence of three independent and consecutive frames/commands has to be sent to the slave (Register with offset address 0x0040 or 0x0041). Afterwards, the slave is reset. Reset signals are also supported to be output via GPIOs, e.g. output to PHY reset signal.

NOTE: It is likely that the last frame of the sequence will not return to the master (depending on the topology), because the links to and from the slave which is reset will go down.

48.5.18 Programming Guide

48.5.18.1 ESC configuration and initialization

The ESC configuration and initialization process is shown in the following steps:

1 Upon powering up, the EtherCAT slave is disabled (as it is under reset).

2 The user should refer to the RCC block for enabling all ECS-related clocks and to the GPIO block for configuring all pads required for the EtherCAT slave.

3 To configure the following wrapper registers if needed:

- By default, the TXCLK pin is configured as an input pin, which means external PHY will supply the TX clock to the EtherCAT slave for transmitting TX data. There is an option for the EtherCAT slave to supply the TX clock (25 MHz) to PHY as a reference clock. In this mode, the timing for data transmission is required to be manually tuned by utilizing the TXSHIFT0/1 (bits [1:0] and bits [5:4]) of ESC_WRACFG0 register. This needs to be done for both ports.
- By default, select 1 to 16 Kbits EEPROM. If using 32 Kbits to 4 Mbits EEPROM, set EEPROMSIZE of ESC_WRACFG1 register to "1".

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- By default, the EtherCAT slave expects Link Up from PHY to be active LOW for both ports. If whichever Link Up polarity does not match, set the corresponding polarity control bits (LINKPOL0/1 (bit 16 or bit 17) of ESC_WRACFG0 register) so that they match.
- Similarly, check the active polarity for RESET_IN and RESET_OUT (for PHY reset). By default, both are active HIGH. Adjust their polarity control bits accordingly if they are not active HIGH.
- The EtherCAT has two MII ports: port 0 and port 1. The corresponding PHY device addresses should be set as the Port number + ADDROFFSET (bits [28:24] of ESC_WRACFG0 register). For example, if ADDROFFSET = 2, the PHY device address of the MII port 0 should be 2 (0 + 2), and the PHY device address of the MII port 1 should be 3 (1 + 2).
- Clean up the interrupt status flags (ESC_WRAINTSTS register) by reading to each byte that holds the flags in this register.
- A wrapper interrupt can be generated by enabling the corresponding interrupt enable bits if needed in the ESC_WRACFG1 register.
- To enable the EtherCAT slave by programming the ESCRST (bit 0 of ESC_WRACTRLSTS register) bit to “0”. By default, the external RESET_IN does not reset the EtherCAT unless the RSTESC (bit 16 of ESC_WRACFG1 register) bit is set to “0”.

4 The EtherCAT slave starts to load EEPROM configuration data right after the reset is de-asserted. It is ready when the EEPROM loading is completed.

48.5.18.2 SyncSignal Initialization

The SyncSignal generation is initialized with the following procedure:

1 Enable DC SYNC Out Unit in ESC Configuration register (set bit2 to 1).

2 Set SYNC/Latch PDI Configuration register (initialized by SII EEPROM) to SYNC0/1 output with appropriate driver settings.

3 Set Pulse Length register (initialized by EEPROM) to pulse length of SYNC signals. Select a value > 0 ns for cyclic repetition of the SyncSignals.

4 Assign Sync Unit to ECAT or PDI (part of ESI).

5 Set cycle time of SYNC0 signal (SYNC0 Cycle Time register) and for SYNC1 signal (SYNC1 Cycle Time register).

6 Set Start Time Cyclic Operation register to a time later than the time the cyclic generation will be activated (end of activation frame; e.g., read the System Time and add the time for writing Start Time and Activation).

7 Activate Cyclic Operation (set Activation register's bit 0) to start cyclic generation of SyncSignals and activate SYNC0/1 generation (set Activation register's bit 1, 2). The Sync Unit waits until the Start Time of Cyclic Operation is reached for the generation of the first SYNC0 pulse.

Register Start Time of Cyclic Operation and register Next SYNC1 pulse can be read to get the time of the next output event. In the acknowledged modes, the Sync0/1 Status registers give the status of the SyncSignals. The SyncSignals are acknowledged by reading the SYNC0/1 Status registers.

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48.6 Registers

The ESC registers contains the following two parts:

- Top-level wrapper-related registers, the starting address of this part of the registers is 0x400C 0000;
- ESC module registers, the starting address of this part of the register is 0x400B 0000.

NOTE: ESC module registers can be accessed by both ECAT and PDI interfaces, but the access rights to some register bits may be different (e.g., ECAT is writable, but PDI is not). In the following descriptions, the two interfaces have the same access rights to all bits by default, unless otherwise stated, and users should pay attention to the relevant descriptions. In addition, the corresponding rights descriptions in the register bitmap are for PDI only.

48.6.1 ESC Wrapper Registers

48.6.1.1 ESC Wrapper Control Status register (ESC_WRACTRLSTS)

Address offset: 0x0000

Reset value: 0x0000 0003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														RSTINSTS	PDIWDSTS
														r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						LATCH1EN	LATCH0EN	Reserved						RSTOUTEN	ESCRST
						rw	rw							rw	rw

Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	RSTINSTS	RESET_IN signal status indication: This bit is to provide the current status of RESET_IN signal with some synchronization delay. RESET_IN is used to reset the ESC if ESC_WRACFG1.RSTESC = 0. 0: Signal deactivated 1: Signal activated *NOTE: Refer to RSTINPOL bit for its polarity control.*
16	PDIWDSTS	PDI_WD_STATE signal status indication: This bit shows the current status of the ESC PDI_WD_STATE signal. The PDI_WD_STATE is an output signal from the ESC and is associated with the PDI watchdog function, triggers when there is no PDI communication with the EtherCAT Slave for longer than the PDI watchdog time being set and activated. 0: Signal deactivated 1: Signal activated
15:10	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
9	LATCH1EN	LATCH1 signal enable: This control bit provides CPU an option to create LATCH1 pulse whenever it is necessary. The pulse width is controlled by LATCHPW. Write '1' to this bit to launch the pulse. While this bit = '1' writing '1' or '0' will have no effect. This bit will automatically return to '0' when the pulse generation is completed.
8	LATCH0EN	LATCH0 signal enable: This control bit provides CPU an option to create LATCH0 pulse whenever it is necessary. The pulse width is controlled by LATCHPW. Write '1' to this bit to launch the pulse. While this bit = '1' writing '1' or '0' will have no effect. This bit will automatically return to '0' when the pulse generation is completed.
7:2	Reserved	Reserved, the reset value must be maintained.
1	RSTOUTEN	RESET_OUT signal enable: 0: RESET_OUT is not active. 1: RESET_OUT is active. (default) *NOTE: Refer to RSTOUTPOL bit for its polarity control.*
0	ESCRST	This is ESC reset control bit. 0: ESC is out of reset. 1: ESC is in reset. (default) *NOTE: This reset bit is not the only reset source for ESC. It also has an external reset source if implemented. If it has both reset sources, ESC can only be out of reset when both reset sources are de-asserted.*

48.6.1.2 ESC Wrapper Configuration register 0 (ESC_WRACFG0)

Address offset: 0x0004

Reset value: 0x000C 0800

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			ADDROFFSET[4:0]					Reserved				RSTOUTPOL	RSTINPOL	LINKPOL1	LINKPOL0
			rw									rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			LATCHPW[5:0]					Reserved		TXSHIFT1		Reserved		TXSHIFT0	
			rw							rw				rw	

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28:24	ADDROFFSET	PHY Address Offset setting. Program this register to match MII PHY0/1 address offset, range from 0 to 31. *NOTE: This phy offset is common to both MII PHYs.*
23:20	Reserved	Reserved, the reset value must be maintained.
19	RSTOUTPOL	RESET_OUT signal polarity setting:

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Bit field	Name	Description
		0: Low active 1: High active
18	RSTINPOL	RESET_IN signal polarity setting: 0: Low active 1: High active
17	LINKPOL1	Port1 PHY link signal polarity setting: 0: Low active 1: High active
16	LINKPOL0	Port0 PHY link signal polarity setting: 0: Low active 1: High active
15:14	Reserved	Reserved, the reset value must be maintained.
13:8	LATCHPW	LATCH0/1 signal Pulse Width setting: 'h00: no pulse will be generated 'h01: pulse width = 1 ahb clock cycle 'h02: pulse width = 2 ahb clock cycles 'h03: pulse width = 3 ahb clock cycles … 'h08: pulse width = 8 ahb clock cycles (default setting) … 'h3F: pulse width = 63 ahb clock cycles
7:6	Reserved	Reserved, the reset value must be maintained.
5:4	TXSHIFT1	Port1 TX shift compensation setting: 00: Port1 TX_CLK signal shifted by 0°, in term of delay 0ns 01: Port1 TX_CLK signal shifted by 90°, in term of delay 10ns 10: Port1 TX_CLK signal shifted by 180°, in term of delay 20ns 11: Port1 TX_CLK signal shifted by 270°, in term of delay 30ns
3:2	Reserved	Reserved, the reset value must be maintained.
1:0	TXSHIFT0	Port0 TX shift compensation setting: 00: Port0 TX_CLK signal shifted by 0°, in term of delay 0ns 01: Port0 TX_CLK signal shifted by 90°, in term of delay 10ns 10: Port0 TX_CLK signal shifted by 180°, in term of delay 20ns 11: Port0 TX_CLK signal shifted by 270°, in term of delay 30ns

48.6.1.3 ESC Wrapper Configuration register 1 (ESC_WRACFG1)

Address offset: 0x0008

Reset value: 0x1801 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			TXCLKCTRL1	TXCLKCTRL0	Reserved		EEPROMSIZE	Reserved	RSTOUTSRC	SOIRQEN1	SOIRQEN0	Reserved	LATCHEN	PDIEMUEN	RSTESC
			rw	rw			rw		rw	rw	rw		rw	rw	rw

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						SOINTEN1	SOINTEN0	ESCAEINTEN	PDIWDSCFINTEN	PDIWDSCRINTEN	RSTOUTINTEN	PDISOFINTEN	PDIEOFINTEN	PDIWDTRGINTEN	RSTININTEN
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	TXCLKCTRL1	MII TXCLK1 input control: 0: CLK25 (25Mhz) is output to TXCLK1 pin 1: TXCLK0 is an input pin
27	TXCLKCTRL0	MII TXCLK0 input control: 0: CLK25 (25Mhz) is output to TXCLK0 pin 1: TXCLK0 is an input pin
26:25	Reserved	Reserved, the reset value must be maintained.
24	EEPROMSIZE	EEPROM size setting: 0: 16 Kbits or less 1: 32 Kbits to 4 Mbits
23	Reserved	Reserved, the reset value must be maintained.
22	RSTOUTSRC	RESET_OUT output source setting: 0: The reset signal is generated by setting bit1 of the ESC_WRACTRLSTS register 1: The reset signal is directly generated by the ESC internal signal source
21	SOIRQEN1	SYNC_OUT1 as IRQ enable: Use the SYNC_OUT1 event as an interrupt, and it has its own interrupt vector. In other words, the SYNC_OUT1 event can directly interrupt the CPU. 0: SYNC_OUT1 as IRQ is disabled 1: SYNC_OUT1 as IRQ is enabled *NOTE: SOINTEN1 and SOIRQEN1, only one of them can be set to "1" at any one time. Setting SOIRQEN1 to "1" has higher priority than setting SOINTEN1 to "1". If software is trying to set both SOINTEN1 and SOIRQEN1 to "1" at the same time SOIRQEN1 will be set to "1". This bit will be reset to "1" if SOINTEN1 is set to "1".*
20	SOIRQEN0	SYNC_OUT0 as IRQ enable: Use the SYNC_OUT0 event as an interrupt, and it has its own interrupt vector. In other words, the SYNC_OUT0 event can directly interrupt the CPU. 0: SYNC_OUT0 as IRQ is disabled 1: SYNC_OUT0 as IRQ is enabled *NOTE: SOINTEN0 and SOIRQEN0, only one of them can be set to "1" at any one time. Setting SOIRQEN0 to "1" has higher priority than setting SOINTEN0 to "1". If software is trying to set both SOINTEN0 and SOIRQEN0 to "1" at the same time SOIRQEN0 will be set to "1". This bit will be reset to "1" if SOINTEN0 is set to "1".*
19	Reserved	Reserved, the reset value must be maintained.
18	LATCHEN	LATCH generation enable: When this is set to '1' set bit9/8 of the ESC_WRACTRLSTS register to launch LATCH

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Bit field	Name	Description
		pulse. 0: LATCH generation is disabled 1: LATCH generation is enabled
17	PDIEMUEN	PDI device emulation enable: 0: PDI device emulation is disabled 1: PDI device emulation is enabled
16	RSTESC	RESET_IN resets the ESC setting: 0: The ESC will be reset if RESET_IN is active 1: RESET_IN will not reset the ESC directly *NOTE: The active polarity of RESET_IN is controlled by RSTINPOL.*
15:10	Reserved	Reserved, the reset value must be maintained.
9	SOINTEN1	SYNC_OUT1 interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set *NOTE: SOINTEN1 and SOIRQEN1, only one of them can be set to "1" at any one time. Setting SOIRQEN1 to "1" has higher priority than setting SOINTEN1 to "1". If software is trying to set both SOINTEN1 and SOIRQEN1 to "1" at the same time SOIRQEN1 will be set to "1". This bit will be reset to "1" if SOIRQEN1 is set to "1".*
8	SOINTEN0	SYNC_OUT0 interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set *NOTE: SOINTEN0 and SOIRQEN0, only one of them can be set to "1" at any one time. Setting SOIRQEN0 to "1" has higher priority than setting SOINTEN0 to "1". If software is trying to set both SOINTEN0 and SOIRQEN0 to "1" at the same time SOIRQEN0 will be set to "1". This bit will be reset to "1" if SOIRQEN0 is set to "1".*
7	ESCAEINTEN	ESC access error interrupt enable: 0: No interupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set
6	PDIWDSCFINTEN	PDI_WD_STATE state changes from "HIGH" to "LOW" interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set
5	PDIWDSCRINTEN	PDI_WD_STATE state changes from "LOW" to "HIGH" interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set
4	RSTOUTINTEN	RESET_OUT interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set
3	PDISOFINTEN	PDI_SOF interrupt enable: The PDI_SOF is Ethernet Start-Of-Frame signal. Here is to generate an interrupt if the PDI_SOF is detected. 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set

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Bit field	Name	Description
2	PDIEOFINTEN	PDI_EOF interrupt enable: The PDI_EOF is Ethernet End-Of-Frame signal. Here is to generate an interrupt if the PDI_EOF is detected. 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set
1	PDIWDTRGINTEN	PDI_WD_TRIGGER interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set
0	RSTININTEN	RESET_IN interrupt enable: 0: No interrupt will be generated 1: An interrupt will be generated if its corresponding interrupt flag is set

48.6.1.4 ESC Wrapper Interrupt Status register (ESC_WRAINTSTS)

Address offset: 0x000C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						SOINTF1	SOINTF0	ESCAEINTF	PDIWDSCFINTF	PDIWDSCRINTF	RSTOUTINTF	PDISOFINTF	PDIEOFINTF	PDIWDTRGINTF	RSTININTF
						r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	SOINTF1	SYNC_OUT1 interrupt flag: It is detected at rising edge. 0: No SYNC_OUT1 active is detected 1: SYNC_OUT1 active is detected This bit will be automatically cleared if the register is read.
8	SOINTF0	SYNC_OUT0 interrupt flag: It is detected at rising edge. 0: No SYNC_OUT0 active is detected 1: SYNC_OUT0 active is detected This bit will be automatically cleared if the register is read.
7	ESCAEINTF	ESC access error interrupt flag: When AHB is accessing ESC registers while the ESC is in or under reset. The reset can come from external or from wrapper reset register. 0: No error is detected 1: An error is detected

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Bit field	Name	Description
		This bit will be automatically cleared if the register is read.
6	PDIWDSCFINTF	PDI_WD_STATE state change interrupt flag: It is detected at failing edge of PDI_WD_STATE signal. 0: No failing edge is detected 1: Failing edge is detected This bit will be automatically cleared if the register is read.
5	PDIWDSCRINTF	PDI_WD_STATE state change interrupt flag: It is detected at rising edge of PDI_WD_STATE signal. 0: No rising edge is detected 1: Rising edge is detected This bit will be automatically cleared if the register is read.
4	RSTOUTINTF	RESET_OUT interrupt flag: It is to detect RESET_OUT goes active. 0: No RESET_OUT event detected 1: RESET_OUT event is detected This bit will be automatically cleared if the register is read.
3	PDISOFINTF	PDI_SOF interrupt flag: It is detected at rising edge. 0: No PDI_SOF active is detected 1: PDI_SOF active is detected This bit will be automatically cleared if the register is read.
2	PDIEOFINTF	PDI_EOF interrupt flag: It is detected at rising edge. 0: No PDI_EOF active is detected 1: PDI_EOF active is detected This bit will be automatically cleared if the register is read.
1	PDIWDTRGINTF	PDI_WD_TRIGGER interrupt flag: It is detected at rising edge. 0: No PDI_WD_TRIGGER active is detected 1: PDI_WD_TRIGGER active is detected This bit will be automatically cleared if the register is read.
0	RSTININTF	RESET_IN interrupt flag: 0: No RESET_IN active (high active) is detected 1: RESET_IN active is detected This bit will be automatically cleared if the register is read. *NOTE: If ESC_WRACFG1.RSTESC = '1' this flag will not be set even when RESET_IN is active.*

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48.6.2 ESC Module Registers

48.6.2.1 ESC Type register (ESC_TYPE)

Address offset: 0x0000

Reset value: 0xAC

Note: This register reset value is 0xAC for Nations products and 0xAD for NSING products.

7	6	5	4	3	2	1	0
TYPE[7:0]							
r							

Bit field	Name	Description
7:0	TYPE	Type of EtherCAT controller.

48.6.2.2 ESC Revision register (ESC_REVISION)

Address offset: 0x0001

Reset value: 0x00

7	6	5	4	3	2	1	0
REVISION[7:0]							
r							

Bit field	Name	Description
7:0	REVISION	Revision of EtherCAT controller (version X.Y.Z). [7:0]: Major version X

48.6.2.3 ESC Build register (ESC_BUILD)

Address offset: 0x0002

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUILD[15:0]															
r															

Bit field	Name	Description
15:0	BUILD	Build of EtherCAT controller (version X.Y.Z). [3:0]: Maintenance version Z [7:4]: Minor version Y

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Bit field	Name	Description
		[15:8]: Patch level / Development build: 0x00: original release; 0x01-0x0F: patch level of original release; 0x10-0xFF: development build

48.6.2.4 ESC FMMU Number register (ESC_FMMUNUM)

Address offset: 0x0004

Reset value: 0x08

7	6	5	4	3	2	1	0
CHNUM[7:0]							
r							

Bit field	Name	Description
7:0	CHNUM	Number of supported FMMU channels (or entities).

48.6.2.5 ESC SyncManagers Number register (ESC_SMNUM)

Address offset: 0x0005

Reset value: 0x08

7	6	5	4	3	2	1	0
CHNUM[7:0]							
r							

Bit field	Name	Description
7:0	CHNUM	Number of supported SyncManager channels (or entities).

48.6.2.6 ESC RAM Size register (ESC_RAMSIZE)

Address offset: 0x0006

Reset value: 0x08

7	6	5	4	3	2	1	0
PDRS[7:0]							
r							

Bit field	Name	Description
7:0	PDRS	Process Data RAM Size supported in KByte.

48.6.2.7 ESC Port Descriptor register (ESC_PORTDES)

Address offset: 0x0007

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Reset value: 0x0F

7	6	5	4	3	2	1	0
PC3[1:0]		PC2[1:0]		PC1[1:0]		PC0[1:0]	
r		r		r		r	

Bit field	Name	Description
7:6	PC3	Port 3 Configuration: 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII / RGMII
5:4	PC2	Port 2 Configuration: 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII / RGMII
3:2	PC1	Port 1 Configuration: 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII / RGMII
1:0	PC0	Port 0 Configuration: 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII / RGMII

48.6.2.8 ESC Features register (ESC_FEATURE)

Address offset: 0x0008

Reset value: 0x01CC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				FFSMC	RWCS	LRWCS	ESYNC	SHFCSER R	MIIELD	EBUSELD	EBUSLJ	DCW	DC	URA	FMMUO
				r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	FFSMC	Fixed FMMU/SyncManager Configuration: 0: Variable configuration 1: Fixed configuration

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Bit field	Name	Description
10	RWCS	EtherCAT read/write command support (BRW, APRW, FPRW): 0: Supported 1: Not supported
9	LRWCS	EtherCAT LRW command support: 0: Supported 1: Not supported
8	ESYNC	Enhanced DC SYNC Activation: 0: Not available 1: Available *NOTE: This feature refers to registers 0x0981[7:3] and 0x0984*
7	SHFCSERR	Separate Handling of FCS Errors: 0: Not supported 1: Supported, frames with wrong FCS and additional nibble will be counted separately in Forwarded RX Error Counter
6	MIIELD	Enhanced Link Detection MII: 0: Not available 1: Available
5	EBUSELD	Enhanced Link Detection EBUS: 0: Not available 1: Available
4	EBUSLJ	Low Jitter EBUS: 0: Not available, standard jitter 1: Available, jitter minimized
3	DCW	Distributed Clocks (width): 0: 32 bit 1: 64 bit
2	DC	Distributed Clocks: 0: Not available 1: Available
1	URA	Unused register access: 0: Allowed 1: Not supported
0	FMMUO	FMMU Operation: 0: Bit oriented 1: Byte oriented

48.6.2.9 ESC Configured Station Address register (ESC_CFGSA)

Address offset: 0x0010

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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ADDR[15:0]

r

Bit field	Name	Description
15:0	ADDR	Address used for node addressing (FPRD/FPWR/FPRW/FRMW commands). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.10 ESC Configured Station Alias register (ESC_CFGSALIAS)

Address offset: 0x0012

Reset value: 0 until first EEPROM load, then EEPROM 4th half-word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
rw															

Bit field	Name	Description
15:0	ADDR	Alias Address used for node addressing (FPRD/FPWR/FPRW/FRMW commands). The use of this alias is activated by Register DL Control Bit 0x0100[24]. *NOTE: EEPROM value is only transferred into this register at first EEPROM load after power-on or reset.* *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

48.6.2.11 ESC Register Write Enable register (ESC_REGWEN)

Address offset: 0x0020

Reset value: 0x0000

7	6	5	4	3	2	1	0
Reserved							VALUE
r							r

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	VALUE	If register write protection is enabled, this register has to be written in the same Ethernet frame (value does not matter) before other writes to this station are allowed. This bit is self-clearing at the beginning of the next frame (SOF), or if Register Write Protection is disabled. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

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48.6.2.12 ESC Register Write Protection register (ESC_REGWP)

Address offset: 0x0021

Reset value: 0x0000

7	6	5	4	3	2	1	0
Reserved							RWPEN
r							

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	RWPEN	Register write protection: 0: Protection disabled 1: Protection enabled Registers 0x0000:0x0F7F are write-protected, except for 0x0020 and 0x0030. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.13 ESC Write Enable register (ESC_ESCWEN)

Address offset: 0x0030

Reset value: 0x0000

7	6	5	4	3	2	1	0
Reserved							VALUE
r							

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	VALUE	If ESC write protection is enabled, this register has to be written in the same Ethernet frame (value does not matter) before other writes to this station are allowed. This bit is self-clearing at the beginning of the next frame (SOF), or if ESC Write Protection is disabled. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.14 ESC Write Protection register (ESC_ESCWP)

Address offset: 0x0031

Reset value: 0x0000

7	6	5	4	3	2	1	0
Reserved							WPEN
r							

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Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	WPEN	Write protection: 0: Protection disabled 1: Protection enabled All areas are write-protected, except for 0x0030. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.15 ESC Reset by ECAT register (ESC_RSTECAT)

Address offset: 0x0040

Reset value: 0x00

7	6	5	4	3	2	1	0
VALUE[7:0]							
r							

Bit field	Name	Description
7:0	VALUE	**Write:** A reset is asserted after writing 0x52 (‘R’), 0x45 (‘E’) and 0x53 (‘S’) in this register with 3 consecutive frames. **Read:** Progress of the reset procedure: 0x1: After writing 0x52 0x2: After writing 0x45 (if 0x52 was written before) 0x0: Others *NOTE: Only the lower two bits are valid for read operations in this bit field.* *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.16 ESC Reset by PDI register (ESC_RSTPDI)

Address offset: 0x0041

Reset value: 0x00

7	6	5	4	3	2	1	0
VALUE[7:0]							
rw							

Bit field	Name	Description
7:0	VALUE	**Write:** A reset is asserted after writing 0x52 (‘R’), 0x45 (‘E’) and 0x53 (‘S’) in this register

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Bit field	Name	Description
		with 3 consecutive frames. **Read:** Progress of the reset procedure: 0x1: After writing 0x52 0x2: After writing 0x45 (if 0x52 was written before) 0x0: Others *NOTE: Only the lower two bits are valid for read operations in this bit field.* *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

48.6.2.17 ESC DL Control register (ESC_DLCTRL)

Address offset: 0x0100

Reset value: 0x0007 C001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							SA	Reserved	RLDST	Reserved		LJ	RXFS[2:0]		
							r		r			r	r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				LP1		LP0		Reserved						TU	FR
				r		r								r	r

Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	SA	Station alias: 0: Ignore Station Alias 1: Alias can be used for all configured address command types (FPRD, FPWR, …) *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
23	Reserved	Reserved, the reset value must be maintained.
22	RLDST	EBUS remote link down signaling time: 0: Default (~660 ms) 1: Reduced (~80 µs) *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
21:20	Reserved	Reserved, the reset value must be maintained.
19	LJ	EBUS Low Jitter: 0: Normal jitter 1: Reduced jitter *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
18:16	RXFS	RX FIFO Size (ESC delays start of forwarding until FIFO is at least half full). RX FIFO Size/RX delay reduction value: 0: -40 ns 1: -40 ns

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Bit field	Name	Description
		2: -40 ns 3: -40 ns 4: no change 5: no change 6: no change 7: default *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
15:12	Reserved	Reserved, the reset value must be maintained.
11:10	LP1	Loop Port 1: 00: Auto 01: Auto Close 10: Open 11: Closed *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
9:8	LP0	Loop Port 0: 00: Auto 01: Auto Close 10: Open 11: Closed *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
7:2	Reserved	Reserved, the reset value must be maintained.
1	TU	Temporary use of settings in LP0-LP1: 0: Permanent use 1: Use for about 1 second, then revert to previous settings *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
0	FR	Forwarding rule: 0: EtherCAT frames are processed, non-EtherCAT frames are forwarded without processing or modification. The source MAC address is not changed for any frame. 1: EtherCAT frames are processed, non-EtherCAT frames are destroyed. The source MAC address is changed by the Processing Unit for every frame (SOURCE_MAC [1] is set to 1 – locally administered address). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Changes to loop configurations are delayed until any current reception or transmission of a frame through the port is completed.

NOTE: The possibility of RX FIFO Size reduction depends on the clock source accuracy of the ESC and of every connected EtherCAT/Ethernet devices (master, slave, etc.). RX FIFO Size of 7 is sufficient for 100ppm accuracy, FIFO Size 0 is possible with 25ppm accuracy (frame size of 1518/1522 Byte).

48.6.2.18 ESC Physical Read/Write Offset register (ESC_RWOFFSET)

Address offset: 0x0108

Reset value: 0x0000

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This register is used for Read/Write commands in Device Addressing mode (FPRW, APRW, BRW).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE[15:0]															
r															

Bit field	Name	Description
15:0	VALUE	Offset value between Read and Write Addresses. The internal read address is directly taken from the offset address field of the EtherCAT datagram header, while the internal write address is calculated by adding the Physical Read/Write Offset value to the offset address field. Internal read address = ADR, internal write address = ADR + R/W Offset *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.19 ESC DL Status register (ESC_DLSTS)

Address offset: 0x0110

Reset value: 0x0004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CSTSP1	LSTSP1	CSTSP0	LSTSP0	Reserved		PLSTSP1	PLSTSP0	Reserved	ELD	PDIWDSTS	POELSTS
				r	r	r	r			r	r		r	r	r

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	CSTSP1	Port 1 Communication Status: 0: No stable communication 1: Communication established
10	LSTSP1	Port 1 Loop Status: 0: Open 1: Closed
9	CSTSP0	Port 0 Communication Status: 0: No stable communication 1: Communication established
8	LSTSP0	Port 0 Loop Status: 0: Open 1: Closed
7:6	Reserved	Reserved, the reset value must be maintained.
5	PLSTSP1	Port 1 Physical Link Status: 0: No link

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Bit field	Name	Description
		1: Link detected
4	PLSTSP0	Port 0 Physical Link Status: 0: No link 1: Link detected
3	Reserved	Reserved, the reset value must be maintained.
2	ELD	Enhanced Link Detection: 0: Deactivated for all ports 1: Activated for at least one port *NOTE: EEPROM value is only transferred into this register at first EEPROM load after power-on or reset.*
1	PDIWDSTS	PDI Watchdog Status: 0: Watchdog expired 1: Watchdog reloaded
0	POELSTS	PDI Operation/EEPROM Load Status: 0: EEPROM not loaded, PDI not operational (no access to Process Data RAM) 1: EEPROM loaded correctly, PDI operational (access to Process Data RAM)

NOTE: Reading DL Status register from ECAT clears bit 2 of the ECAT Event Request register. Avoid reading DL Status register from PDI.

48.6.2.20 ESC AL Control register (ESC_ALCTRL)

Address offset: 0x0120

Reset value: 0x0001

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										DIR	EIA	DSMR[3:0]			
										r	r	r			

Bit field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5	DIR	Device Identification Request: 0: No request 1: Device Identification request *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
4	EIA	Error Indication Acknowledge: 0: No Ack of Error Ind in AL status register 1: Ack of Error Ind in AL status register *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
3:0	DSMR	Device State Machine Request: Initiate State Transition of the Device State Machine: 0x1: Initial state request

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Bit field	Name	Description
		0x2: Pre-operational state request 0x3: Bootstrap state request 0x4: Safe-operational state request 0x8: Operational state request Others: Reserved *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.21 ESC AL Status register (ESC_ALSTS)

Address offset: 0x0130

Reset value: 0x0004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										DILSTS	EISTS	DSMSTS[3:0]			
										rw	rw	rw			

Bit field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5	DILSTS	Device Identification Load Status: 0: Device Identification not valid 1: Device Identification loaded *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*
4	EISTS	Error Indication Status: 0: Device is in State as requested or Flag cleared by command 1: Device has not entered requested State or changed State as result of a local action *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*
3:0	DSMSTS	Device State Machine Status: Actual State of the Device State Machine: 0x1: Initial state 0x2: Pre-operational state 0x3: Request bootstrap state 0x4: Safe-operational state 0x8: Operational state *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

NOTE: Reading AL Status register from ECAT clears bit 3 of the ECAT Event Request register. Avoid reading DL Status register from PDI.

48.6.2.22 ESC AL Status Code register (ESC_ALSTSC)

Address offset: 0x0134

Reset value: 0x0000

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE[15:0]															
rw															

Bit field	Name	Description
15:0	CODE	AL Status Code. *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

48.6.2.23 ESC RUN LED Override register (ESC_RUNLEDOVE)

Address offset: 0x0138

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved			OVEEN	LEDCODE[3:0]			
			rw	rw			

Bit field	Name	Description
7:5	Reserved	Reserved, the reset value must be maintained.
4	OVEEN	Enable Override: 0: Override disabled 1: Override enabled
3:0	LEDCODE	LED Code (FSM state: Bits [3:0] of the AL Status register): 0x0: Off (FSM: 1-Init) 0x1: Flash 1x (FSM: 4-SafeOp) 0xD: Blinking (FSM: 2-PreOp) 0xE: Flickering (FSM: 3-Bootstrap) 0xF: On (FSM: 8-Op) Others: Flash 2x - 12x (FSM: -)

NOTE: Changes to AL Status register with valid values will disable RUN LED Override (clear bit 4). The value read in this register always reflects current LED output.

48.6.2.24 ESC ERR LED Override register (ESC_ERRLEDOVE)

Address offset: 0x0139

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved			OVEEN	LEDCODE[3:0]			
			rw	rw			

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Bit field	Name	Description
7:5	Reserved	Reserved, the reset value must be maintained.
4	OVEEN	Enable Override: 0: Override disabled 1: Override enabled
3:0	LEDCODE	LED Code: 0x0: Off 0x1-0xC: Flash 1x – 12x 0xD: Blinking 0xE: Flickering 0xF: On

NOTE: New error conditions will disable ERR LED Override (clear bit 4). The value read in this register always reflects current LED output.

48.6.2.25 ESC PDI Control register (ESC_PDISTRL)

Address offset: 0x0140

Reset value: 0x80

7	6	5	4	3	2	1	0
PDI[7:0]							
r							

Bit field	Name	Description
7:0	PDI	Process Data Interface: 0x80: On-chip bus

48.6.2.26 ESC Configuration register (ESC_CFG)

Address offset: 0x0141

Reset value: 0x3E

7	6	5	4	3	2	1	0
ELDP3	ELDP2	ELDP1	ELDP0	DCLATCH	DCSYNC	ELDAP	DE
r	r	r	r	r	r	r	r

Bit field	Name	Description
7	ELDP3	Port 3 Enhanced Link Detection: 0: Disabled 1: Enabled
6	ELDP2	Port 2 Enhanced Link Detection: 0: Disabled

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Bit field	Name	Description
		1: Enabled
5	ELDP1	Port 1 Enhanced Link Detection: 0: Disabled 1: Enabled
4	ELDP0	Port 0 Enhanced Link Detection: 0: Disabled 1: Enabled
3	DCLATCH	Distributed Clocks Latch In Unit: 0: Disabled (power saving) 1: Enabled
2	DCSYNC	Distributed Clocks SYNC Out Unit: 0: Disabled (power saving) 1: Enabled
1	ELDAP	Enhanced Link detection all ports: 0: Disabled (if bits [7:4]=0) 1: Enabled at all ports (overrides bits [7:4])
0	DE	Device emulation (control of AL status): 0: AL status register has to be set by PDI 1: AL status register will be set to value written to AL control register

NOTE: EEPROM values of bits 1, 4, 5, 6, and 7 are only transferred into this register at first EEPROM load after power-on or reset.

48.6.2.27 ESC PDI Information register (ESC_PDIINFO)

Address offset: 0x014E

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PDICFG	PDIACT	ESCLOAD	PDIACK
												r	r	r	r

Bit field	Name	Description
15:4	Reserved	Reserved, the reset value must be maintained.
3	PDICFG	PDI configuration invalid: 0: PDI configuration ok 1: PDI configuration invalid
2	PDIACT	PDI active: 0: PDI not active 1: PDI active
1	ESCLOAD	ESC configuration area loaded from EEPROM: 0: Not loaded

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Bit field	Name	Description
		1: Loaded
0	PDIACK	PDI function acknowledge by write: 0: Disabled 1: Enabled

48.6.2.28 ESC PDI Configuration register (ESC_PDICFG)

Address offset: 0x0150

Reset value: 0x81

7	6	5	4	3	2	1	0
OCBTYPE[2:0]			OCBCLK[4:0]				
r			r				

Bit field	Name	Description
7:5	OCBTYPE	On-Chip Bus Type. Indicate the type of on-chip bus. 100: OPB Others: reserved
4:0	OCBCLK	On-Chip Bus Clock. Indicate the frequency of the on-chip bus clock. The value is always 1 (corresponding to 1 * 25 MHz).

48.6.2.29 ESC Sync/Latch PDI Configuration register (ESC_PDISLCFG)

Address offset: 0x0151

Reset value: 0xEE

7	6	5	4	3	2	1	0
S1MAP	S1L1CFG	S1OUT[1:0]		S0MAP	S0L0CFG	S0OUT[1:0]	
r	r	r		r	r	r	

Bit field	Name	Description
7	S1MAP	SYNC1 State Mapping: Indicates enabling or disabling of mapping of the SYNC1 state to bit 3 of the AL Event Request register. 0: Disabled 1: Enabled
6	S1L1CFG	SYNC1/LATCH1 configuration: 0: LATCH1 input 1: SYNC1 output

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Bit field	Name	Description
5:4	S1OUT	SYNC1 output driver/polarity: 00: Push-Pull (active low) 01: Open Drain (active low) 10: Push-Pull (active high) 11: Open Source (active high)
3	S0MAP	SYNC0 State Mapping: Indicates enabling or disabling of mapping of the SYNC0 state to bit 2 of the AL Event Request register. 0: Disabled 1: Enabled
2	S0L0CFG	SYNC0/LATCH0 configuration: 0: LATCH0 input 1: SYNC0 output
1:0	S0OUT	SYNC0 output driver/polarity: 00: Push-Pull (active low) 01: Open Drain (active low) 10: Push-Pull (active high) 11: Open Source (active high)

NOTE: The IP Core has concurrent SYNC1/0 outputs and LATCH1/0 inputs, independent of this configuration (Configuration of bit 2 and bit 6).

48.6.2.30 ESC PDI Extended Configuration register (ESC_PDIEXTCFG)

Address offset: 0x0152

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														DBWID[1:0]	
r															

Bit field	Name	Description
15:2	Reserved	Reserved, the reset value must be maintained.
1:0	DBWID	PDI Data Bus Width: Indicate the data bus width of the PDI. 00: 4 bytes 01: 1 byte 10: 2 bytes 11: Reserved

48.6.2.31 ESC ECAT Event Mask register (ESC_ECATEMSK)

Address offset: 0x0200

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Reset value: 0x0000

The ECAT Event Request (ECAT interrupt) is used to transmit the slave event to the EtherCAT master. This register is used to set mask to each event of the ECAT Event Request register. The logical AND of each effective bit in the ECAT Event Request register and the corresponding bit of this register is taken and the result produces the interrupt signal.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK[15:0]															
r															

Bit field	Name	Description
15:0	MASK	ECAT Event masking of the ECAT Event Request Events for mapping into ECAT event field of EtherCAT frames: 0: Corresponding ECAT Event Request register bit is not mapped 1: Corresponding ECAT Event Request register bit is mapped *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.32 ESC AL Event Mask register (ESC_ALEMSK)

Address offset: 0x0204

Reset value: 0x00FF FF0F

The AL event request (PDI interrupt) is used to transmit the ESC interrupt to the slave application. This register is used to set mask to each event of the AL Event Request register. The logical AND of each effective bit in the AL Event Request register and the corresponding bit of this register is taken and the result produces the interrupt signal.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MASK[31:15]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK[15:0]															
rw															

Bit field	Name	Description
31:0	MASK	AL Event masking of the AL Event Request register Events for mapping to PDI IRQ signal: 0: Corresponding AL Event Request register bit is not mapped 1: Corresponding AL Event Request register bit is mapped *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

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48.6.2.33 ESC ECAT Event Request register (ESC_ECATEREQ)

Address offset: 0x0210

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SM7STS	SM6STS	SM5STS	SM4STS	SM3STS	SM2STS	SM1STS	SM0STS	ALSTS	DLSTS	Reserved	DCLATCH
				r	r	r	r	r	r	r	r	r	r		r

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	SM7STS	Mirror value of SyncManager 7 Status: 0: No Sync Channel 7 event 1: Sync Channel 7 event pending
10	SM6STS	Mirror value of SyncManager 6 Status: 0: No Sync Channel 6 event 1: Sync Channel 6 event pending
9	SM5STS	Mirror value of SyncManager 5 Status: 0: No Sync Channel 5 event 1: Sync Channel 5 event pending
8	SM4STS	Mirror value of SyncManager 4 Status: 0: No Sync Channel 4 event 1: Sync Channel 4 event pending
7	SM3STS	Mirror value of SyncManager 3 Status: 0: No Sync Channel 3 event 1: Sync Channel 3 event pending
6	SM2STS	Mirror value of SyncManager 2 Status: 0: No Sync Channel 2 event 1: Sync Channel 2 event pending
5	SM1STS	Mirror value of SyncManager 1 Status: 0: No Sync Channel 1 event 1: Sync Channel 1 event pending
4	SM0STS	Mirror value of SyncManager 0 Status: 0: No Sync Channel 0 event 1: Sync Channel 0 event pending
3	ALSTS	AL Status event: This bit is cleared by reading out the AL Status register from the ECAT. 0: No change in AL Status 1: AL Status change
2	DLSTS	DL Status event: This bit is cleared by reading out the DL Status register from the ECAT. 0: No change in DL Status

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Bit field	Name	Description
		1: DL Status change
1	Reserved	Reserved, the reset value must be maintained.
0	DCLATCH	DC Latch event: This bit is cleared by reading DC Latch event times from the ECAT for ECAT controlled latch units, so the Latch 0/1 Status registers indicate no event. 0: No change on DC Latch Inputs 1: At least one change on DC Latch Inputs

48.6.2.34 ESC AL Event Request register (ESC_ALEREQ)

Address offset: 0x0220

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SM7INT	SM6INT	SM5INT	SM4INT	SM3INT	SM2INT	SM1INT	SM0INT	Reserved	WDPD	Reserved	SMACT	SYNC1STS	SYNC0STS	DCLATCH	ALCTRL
r	r	r	r	r	r	r	r		r		r	r	r	r	r

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	SM7INT	SyncManager 7 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 7 interrupt 1: SyncManager 7 interrupt pending
14	SM6INT	SyncManager 6 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 6 interrupt 1: SyncManager 6 interrupt pending
13	SM5INT	SyncManager 5 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 5 interrupt 1: SyncManager 5 interrupt pending
12	SM4INT	SyncManager 4 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 4 interrupt 1: SyncManager 4 interrupt pending
11	SM3INT	SyncManager 3 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 3 interrupt 1: SyncManager 3 interrupt pending
10	SM2INT	SyncManager 2 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 2 interrupt 1: SyncManager 2 interrupt pending
9	SM1INT	SyncManager 1 interrupt (bit 0 or 1 of the SyncManager Status register)

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Bit field	Name	Description
		0: No SyncManager 1 interrupt 1: SyncManager 1 interrupt pending
8	SM0INT	SyncManager 0 interrupt (bit 0 or 1 of the SyncManager Status register) 0: No SyncManager 0 interrupt 1: SyncManager 0 interrupt pending
7	Reserved	Reserved, the reset value must be maintained.
6	WDPD	Watchdog Process Data: This bit is cleared by reading the Watchdog Status Process Data register from the PDI. 0: Has not expired 1: Has expired
5	Reserved	Reserved, the reset value must be maintained.
4	SMACT	SyncManager activation: Change of the SyncManager Activation register. This bit is cleared by reading SyncManager Activation registers from the PDI. 0: No change in any SyncManager 1: At least one SyncManager changed
3	SYNC1STS	DC SYNC1 State Indication. This bit is cleared by reading the SYNC1 Status register from the PDI, use only in Acknowledge mode.
2	SYNC0STS	DC SYNC0 State Indication. This bit is cleared by reading the SYNC0 Status register from the PDI, use only in Acknowledge mode.
1	DCLATCH	DC Latch event: This bit is cleared by reading DC Latch event times from the PDI for PDI controlled latch units, so the Latch 0/1 Status registers indicate no event. 0: No change on DC Latch Inputs 1: At least one change on DC Latch Inputs
0	ALCTRL	AL Control event: This bit is cleared by reading the AL Control register from the PDI. 0: No AL Control Register change 1: AL Control Register has been written

48.6.2.35 ESC RX Error Counter n register (ESC_RXERRCNTn)

Address offset: 0x0300 + 2 ∗ n (n = 0, 1), n Indicates logical port numbers 0 and 1.

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFECV[7:0]								IFCV[7:0]							
r								r							

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Bit field	Name	Description
15:8	RXFECV	RX Frame Error Counter Value. Counter value of RX errors for port n counting is stopped when 0xFF is reached. The number of RX errors of MII interface is counted. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
7:0	IFCV	Invalid Frame Counter Value. Counter value of invalid frames for port n counting is stopped when 0xFF is reached. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Error Counters (Includes RX Error Counter and Forwarded RX Error Counter) are cleared if one of the implemented RX Error counters (Includes RX Error Counter and Forwarded RX Error Counter) is written (preferably RX Error Counter 0). Write value is ignored (write 0). Errors are only counted if the loop of the port is open.

48.6.2.36 ESC Forwarded RX Error Counter n register (ESC_FWDRXERRCNTn)

Address offset: 0x0308 + n (n = 0, 1), n Indicates logical port numbers 0 and 1.

Reset value: 0x00

7	6	5	4	3	2	1	0
FECV[7:0]							
r							

Bit field	Name	Description
7:0	FECV	Forwarded Error Counter Value. Counter value of forwarded RX error frames for port n counting is stopped when 0xFF is reached. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Error Counters (Includes RX Error Counter and Forwarded RX Error Counter) are cleared if one of the implemented RX Error counters (Includes RX Error Counter and Forwarded RX Error Counter) is written (preferably RX Error Counter 0). Write value is ignored (write 0). Errors are only counted if the loop of the port is open.

48.6.2.37 ESC ECAT Processing Unit Error Counter register (ESC_EPUERRCNT)

Address offset: 0x030C

Reset value: 0x00

7	6	5	4	3	2	1	0
EPUECV[7:0]							
r							

Bit field	Name	Description
7:0	EPUECV	ECAT Processing Unit Error Counter Value. ECAT processing unit error counter value counting is stopped when 0xFF is reached.

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Bit field	Name	Description
		NOTE: This bit field ECAT is readable and writable, PDI is read-only.

NOTE: This register counts errors of frames passing the processing unit. Writing to this register clears it. Write value is ignored (write 0).

48.6.2.38 ESC PDI Error Counter register (ESC_PDIERRCNT)

Address offset: 0x030D

Reset value: 0x00

7	6	5	4	3	2	1	0
EPUECV[7:0]							
r							

Bit field	Name	Description
7:0	EPUECV	PDI Error Counter Value. Counting is stopped when 0xFF is reached. Counting starts when an interface error occurs due to access to the PDI. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: PDI Error Counter and PDI Error Code are cleared if PDI Error Counter is written. Write value is ignored (write 0).

48.6.2.39 ESC PDI Error Code register (ESC_PDIERRCODE)

Address offset: 0x030E

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved				WADDR	RADDR	WBUSY	RBUSY
				r	r	r	r

Bit field	Name	Description
7:4	Reserved	Reserved, the reset value must be maintained.
3	WADDR	Addressing error for a write access (odd address without BHE) 0: No error 1: Error detected
2	RADDR	Addressing error for a read access (odd address without BHE) 0: No error 1: Error detected
1	WBUSY	Busy violation during write access 0: No error 1: Error detected

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Bit field	Name	Description
0	RBUSY	Busy violation during read access 0: No error 1: Error detected

NOTE: PDI Error Counter and PDI Error Code are cleared if PDI Error Counter is written. Write value is ignored (write 0).

48.6.2.40 ESC Lost Link Counter n register (ESC_LOSTLINKCNTn)

Address offset: 0x0310 + n (n = 0, 1), n Indicates logical port numbers 0 and 1.

Reset value: 0x00

7	6	5	4	3	2	1	0
LLCV[7:0]							
r							

Bit field	Name	Description
7:0	LLCV	Lost Link Counter Value. Lost link counter value for port n counting is stopped when 0xFF is reached. Counting starts only when port loop is Auto or Auto-Close. Only lost links at open ports are counted. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Lost Link Counters are cleared if one of the implemented Lost Link Counters is written (preferably Lost Link Counter 0). Write value is ignored (write 0).

48.6.2.41 ESC Watchdog Divider register (ESC_WDDIV)

Address offset: 0x0400

Reset value: 0x09C2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDD[15:0]															
r															

Bit field	Name	Description
15:0	WDD	Watchdog divider: Number of 25 MHz tics (minus 2) that represent the basic watchdog increment. (Default value is 100µs = 2498). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.42 ESC Watchdog Time PDI register (ESC_WDTPDI)

Address offset: 0x0410

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Reset value: 0x03E8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDT[15:0]															
r															

Bit field	Name	Description
15:0	WDT	Watchdog Time PDI: Set the time until the PDI watchdog timer overflows as a number of times the watchdog is incremented. With the default values for these bits and the setting of the watchdog divider, the time for a single incrementation is 100 µs, so the watchdog timer overflows when 100 µs ×1000 = 100 ms elapsed. Setting these bits to 0 disables the watchdog timer. Access to the PDI restarts the watchdog timer. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.43 ESC Watchdog Time Process Data register (ESC_WDTPD)

Address offset: 0x0420

Reset value: 0x03E8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDT[15:0]															
r															

Bit field	Name	Description
15:0	WDT	Watchdog Time Process Data: Set the time until the process data watchdog timer overflows as a number of times the watchdog is incremented. With the default values for these bits and the setting of the watchdog divider, the time for a single incrementation is 100 µs, so the watchdog timer overflows when 100 µs × 1000 = 100 ms elapsed. There is one watchdog for all SyncManagers. Setting these bits to 0 disables the watchdog timer. Access to the Watchdog Trigger Enable bit of SyncManager restarts the watchdog timer. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.44 ESC Watchdog Status Process Data register (ESC_WDSTSPD)

Address offset: 0x0440

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															WDS
r															

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Bit field	Name	Description
15:1	Reserved	Reserved, the reset value must be maintained.
0	WDS	Watchdog State: Indicates the state of the process data watchdog timer triggered by SyncManagers. Reading this register clears bit 6 of the AL Event Request register 0: Watchdog Process Data expired 1: Watchdog Process Data is active or disabled

48.6.2.45 ESC Watchdog Counter Process Data register (ESC_WDCNTPD)

Address offset: 0x0442

Reset value: 0x00

7	6	5	4	3	2	1	0
WDCV[7:0]							
r							

Bit field	Name	Description
7:0	WDCV	Watchdog Counter Value. Indication Counter value of the process data watchdog timer counting stops when 0xFF is reached. Counting starts on a timeout of the process data watchdog timer. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Watchdog Counters (Includes Watchdog Counter Process Data and Watchdog Counter PDI) are cleared if one of the Watchdog Counters (Includes Watchdog Counter Process Data and Watchdog Counter PDI) is written. Write value is ignored (write 0).

48.6.2.46 ESC Watchdog Counter PDI register (ESC_WDCNTPDI)

Address offset: 0x0443

Reset value: 0x00

7	6	5	4	3	2	1	0
WDCV[7:0]							
r							

Bit field	Name	Description
7:0	WDCV	Watchdog Counter Value. Counter value of the PDI watchdog timer counting stops when 0xFF is reached. Counting starts on a timeout of the PDI watchdog timer. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

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NOTE: Watchdog Counters (Includes Watchdog Counter Process Data and Watchdog Counter PDI) are cleared if one of the Watchdog Counters (Includes Watchdog Counter Process Data and Watchdog Counter PDI) is written. Write value is ignored (write 0).

48.6.2.47 ESC EEPROM Configuration register (ESC_EEPROMCFG)

Address offset: 0x0500

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						FECATA	PDICTRL
						r	r

Bit field	Name	Description
7:2	Reserved	Reserved, the reset value must be maintained.
1	FECATA	Force ECAT Access: 0: Do not change EEPROM PDI Access State register's bit 0 1: Reset EEPROM PDI Access State register's bit 0 to 0 *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
0	PDICTRL	PDI EEPROM Control: Specifies whether EEPROM control is offered to the PDI. 0: The PDI has no EEPROM control 1: The PDI has EEPROM control *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.48 ESC EEPROM PDI Access State register (ESC_EEPROMPDIAS)

Address offset: 0x0501

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved							AE
							rw

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	AE	Access to EEPROM: 0: PDI releases EEPROM access 1: PDI takes EEPROM access (PDI has EEPROM control) Write access from the PDI is only possible when bit 0 is 1 and bit 1 is 0 in the EEPROM Configuration register. *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

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48.6.2.49 ESC EEPROM Control/Status register (ESC_EEPROMCTRLSTS)

Address offset: 0x0502

Reset value: 0x0040

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUSY	WENERR	ACKCMDERR	LOADSTS	CSERR	CMD[2:0]			SEA	RBYTE	EMU	Reserved				ECATWEN
r	r	r	r	r	rw			r	r	r					r

Bit field	Name	Description
15	BUSY	Busy: 0: EEPROM Interface is idle 1: EEPROM Interface is busy
14	WENERR	Error Write Enable: 0: No error 1: Write Command without Write enable
13	ACKCMDERR	Error Acknowledge/Command: 0: No error 1: Missing EEPROM acknowledge or invalid command
12	LOADSTS	EEPROM loading status: 0: EEPROM loaded, device information ok 1: EEPROM not loaded, device information not available (EEPROM loading in progress or finished with a failure)
11	CSERR	Checksum Error in ESC Configuration Area: 0: Checksum ok 1: Checksum error
10:8	CMD	Command: **Write:** Initiate command. **Read:** Currently executed command Commands: 000: No command/EEPROM idle (clear error bits) 001: Read 010: Write 100: Reload Others: Reserved/invalid commands (do not issue)
7	SEA	Selected EEPROM Algorithm: 0: 1 address byte (1Kbit – 16Kbit EEPROMs) 1: 2 address bytes (32Kbit – 4 Mbit EEPROMs)
6	RBYTE	Supported number of EEPROM read bytes: 0: 4 Bytes 1: 8 Bytes

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Bit field	Name	Description
5	EMU	EEPROM emulation: 0: Normal operation (I²C interface used) 1: PDI emulates EEPROM (I²C not used)
4:1	Reserved	Reserved, the reset value must be maintained.
0	ECATWEN	ECAT write enable: 0: Write requests are disabled 1: Write requests are enabled This bit is always 1 if PDI has EEPROM control. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is blocked if EEPROM interface is busy (bit15 equals 1).

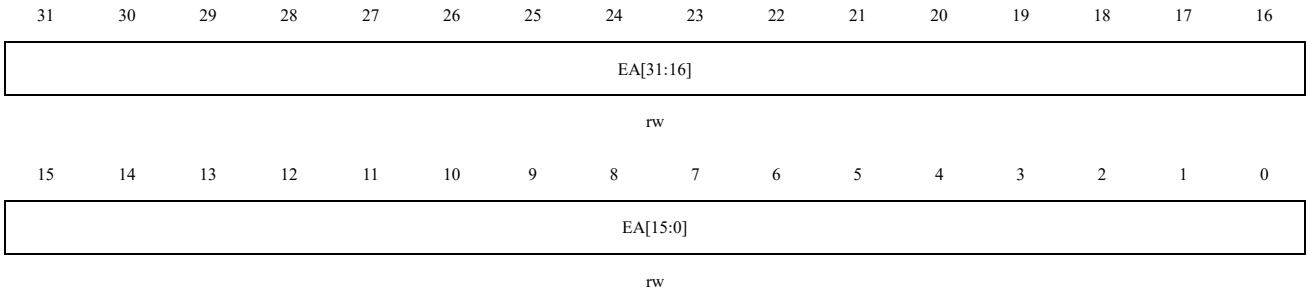
NOTE: WENERR and ACKCMDERR bits are cleared by writing 000b (or any valid command) to CMD bit field.

NOTE: Bit 0 (ECAT write enable bit) is self-cleared at the SOF of the next frame. CMD bit field are also self-cleared after the command is executed (EEPROM busy ends). Writing 000b to CMD bit field also clears the error bits 14 and 13. CMD bit field are ignored if bit 13 (Acknowledge/Command error bit) is 1.

48.6.2.50 ESC EEPROM Address register (ESC_EEPROMADDR)

Address offset: 0x0504

Reset value: 0x0000 0000



Bit field	Name	Description
31:0	EA	EEPROM Address: 0: First half-word (= 16 bit) 1: Second half-word … Actually used EEPROM Address bits: [9:0]: EEPROM size up to 16 Kbit [17:0]: EEPROM size 32 Kbit – 4 Mbit

NOTE: write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is blocked if EEPROM interface is busy (bit15 equals 1).

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48.6.2.51 ESC EEPROM Data register (ESC_EEPROMDAT)

Address offset: 0x0508

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HIGH[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOW[15:0]															
rw															

Bit field	Name	Description
31:16	HIGH	EEPROM Read data (data read from EEPROM, higher bytes)
15:0	LOW	EEPROM Write data (data to be written to EEPROM) or EEPROM Read data (data read from EEPROM, lower bytes)

NOTE: write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is blocked if EEPROM interface is busy (bit15 equals 1).

48.6.2.52 ESC MII Management Control/Status register (ESC_MICTRLSTS)

Address offset: 0x0510

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUSY	CMDERR	RERR	Reserved			CMD[1:0]		PHYADDR0[4:0]					MICFG	PDICTRL	WEN
r	r	rw				rw		r					r	r	r

Bit field	Name	Description
15	BUSY	Busy: 0: MII Management Interface is idle 1: MII Management Interface is busy
14	CMDERR	Command error: 0: Last Command was successful 1: Invalid command or write command without Write Enable This bit is cleared by executing a valid command or writing 00b to CMD [1:0].
13	RERR	Read error: 0: No read error 1: Read error occurred (PHY or register not available) This bit is cleared by writing to the high 8 bits of this register.
12:10	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
9:8	CMD	Command: **Write:** Initiate command. **Read:** Currently executed command Commands: 00: No command/MI idle (clear error bits) 01: Read 10: Write 11: Reserved/invalid command (do not issue)
7:3	PHYADDR0	PHY address of port 0.
2	MICFG	MI link detection and configuration: 0: Disabled for all ports 1: Enabled for at least one MII port, refer to PHY Port Status register for details
1	PDICTRL	PDI Control: Management Interface can be controlled by PDI (MII Management ECAT Access State register and MII Management PDI Access State register): 0: Only ECAT control 1: PDI control possible
0	WEN	Write enable: 0: Write disabled 1: Write enabled This bit is always 1 if PDI has MI control. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: write access depends upon the assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (bit15 equals 1).

NOTE: Bit 0 (Write enable bit) is self-cleared at the SOF of the next frame. CMD bit field are also self-cleared after the command is executed (Busy ends). Writing 00b to CMD bit field also clears the error bits 14 and 13.

48.6.2.53 ESC PHY Address register (ESC_PHYADDR)

Address offset: 0x0512

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved			ADDR[4:0]				
			rw				

Bit field	Name	Description
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	ADDR	PHY Address.

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NOTE: write access depends upon the assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (MII Management Control/Status register's bit 15 equals 1).

48.6.2.54 ESC PHY Register Address register (ESC_PHYREGADDR)

Address offset: 0x0513

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved			ADDR[4:0]				
			rw				

Bit field	Name	Description
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	ADDR	Address of PHY Register that shall be read/written.

NOTE: write access depends upon the assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (MII Management Control/Status register's bit 15 equals 1).

48.6.2.55 ESC PHY Data register (ESC_PHYDAT)

Address offset: 0x0514

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT[15:0]															
rw															

Bit field	Name	Description
15:0	DAT	PHY Read/Write Data.

NOTE: write access depends upon the assignment of MI (ECAT/PDI). Write access is blocked if Management interface is busy (MII Management Control/Status register's bit 15 equals 1).

48.6.2.56 ESC MII Management ECAT Access State register (ESC_MIECATAS)

Address offset: 0x0516

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved							ACSMII
							r

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Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	ACSMII	Access to MII management: 0: ECAT enables PDI takeover of MII management interface 1: ECAT claims exclusive access to MII management interface *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: write access is only possible if MII Management PDI Access State register's bit 0 equals 0.

48.6.2.57 ESC MII Management PDI Access State register (ESC_MIPDIAS)

Address offset: 0x0517

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						FPDIA	ACSMII
						r	rw

Bit field	Name	Description
7:2	Reserved	Reserved, the reset value must be maintained.
1	FPDIA	Force PDI Access State: 0: Do not change bit 0 1: Reset bit 0 to 0 *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
0	ACSMII	Access to MII management: 0: ECAT has access to MII management 1: PDI has access to MII management *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

NOTE: assigning access to PDI (bit 0 equals 1) is only possible if MII Management ECAT Access State register's bit 0 equals 0 and MII Management PDI Access State register's bit 1 equals 0.

48.6.2.58 ESC PHY Port n Status register (ESC_PHYPnSTS)

Address offset: 0x0518 + n (n = 0, 1), n Indicates logical port numbers 0 and 1.

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved		PHYCFGUD	LPERR	RERR	LSERR	LS	PLS
		rw	r	rw	r	r	r

Bit field	Name	Description
7:6	Reserved	Reserved, the reset value must be maintained.
5	PHYCFGUD	PHY Configuration Updated:

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Bit field	Name	Description
		0: No update 1: PHY configuration was updated This bit cleared by writing any value to at least one of the PHY Port n Status registers.
4	LPERR	Link Partner error: 0: No error detected 1: Link partner error
3	RERR	Read error: 0: No read error occurred 1: A read error has occurred This bit cleared by writing any value to at least one of the PHY Port n Status registers.
2	LSERR	Link Status error: 0: No error 1: Link error, link inhibited
1	LS	Link Status (100 Mbit/s, Full Duplex, Auto negotiation): 0: No link 1: Link detected
0	PLS	Physical Link Status (PHY status register 1.2): 0: No physical link 1: Physical link detected

NOTE: write access depends on assignment of MI (ECAT/PDI).

48.6.2.59 ESC FMMU n Logical Start Address register (ESC_FMMUnLSA)

Address offset: 0x0600 + 0x10 × n (n = 0 to 7)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
r															

Bit field	Name	Description
31:0	ADDR	Logical Start Address: Set the start of the logical address within the EtherCAT address space. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.60 ESC FMMU n Length register (ESC_FMMUnLEN)

Address offset: 0x0604 + 0x10 × n (n = 0 to 7)

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Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET[15:0]															
r															

Bit field	Name	Description
15:0	OFFSET	Offset from the first logical FMMU byte to the last FMMU byte + 1 (e.g., if two bytes are used, then this parameter shall contain 2). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.61 ESC FMMU n Logical Start Bit register (ESC_FMMUnLSATB)

Address offset: 0x0606 + 0x10 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved					BIT[2:0]		
					r		

Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained.
2:0	BIT	Logical starting bit that shall be mapped (bits are counted from least significant bit 0 to most significant bit 7). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.62 ESC FMMU n Logical Stop Bit register (ESC_FMMUnLSTPB)

Address offset: 0x0607 + 0x10 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved					BIT[2:0]		
					r		

Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained.
2:0	BIT	Last logical bit that shall be mapped (bits are counted from least significant bit 0 to most significant bit 7). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

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48.6.2.63 ESC FMMU n Physical Start Address register (ESC_FMMUnPSA)

Address offset: 0x0608 + 0x10 × n (n = 0 to 7)

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
r															

Bit field	Name	Description
15:0	ADDR	Physical Start Address: Set the physical start address to which the logical start address will be mapped. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.64 ESC FMMU n Physical Start Bit register (ESC_FMMUnPSATB)

Address offset: 0x060A + 0x10 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						BIT[2:0]	
						r	

Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained.
2:0	BIT	Physical starting bit as target of logical start bit mapping (bits are counted from least significant bit 0 to most significant bit 7). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.65 ESC FMMU n Type register (ESC_FMMUnTYPE)

Address offset: 0x060B + 0x10 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						WAM	RAM
						r	r

Bit field	Name	Description
7:2	Reserved	Reserved, the reset value must be maintained.
1	WAM	Write Access Mapping 0: Ignore mapping for write accesses

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Bit field	Name	Description
		1: Use mapping for write accesses *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
0	RAM	Read Access Mapping 0: Ignore mapping for read accesses 1: Use mapping for read accesses *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.66 ESC FMMU n Activate register (ESC_FMMUnACT)

Address offset: 0x060C + 0x10 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved							FA
							r

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	FA	FMMU Activate/Deactivate: 0: FMMU deactivated 1: FMMU activated. FMMU checks logically addressed blocks to be mapped according to configured mapping *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.67 ESC SyncManager n Physical Start Address register (ESC_SMnPSA)

Address offset: 0x0800 + 0x8 × n (n = 0 to 7)

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[15:0]															
r															

Bit field	Name	Description
15:0	ADDR	Physical Start Address: Set the physical start address for the area assigned to SyncManager. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Register can only be written if SyncManager is disabled (bit 0 is 0 in the SyncManager n Activate register).

48.6.2.68 ESC SyncManager n Length register (ESC_SMnLEN)

Address offset: 0x0802 + 0x8 × n (n = 0 to 7)

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Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUM[15:0]															
r															

Bit field	Name	Description
15:0	NUM	Number of bytes assigned to SyncManager (shall be greater than 1, otherwise Sync-Manager is not activated. If set to 1, only Watchdog Trigger is generated if configured). *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Register can only be written if SyncManager is disabled (bit 0 is 0 in the SyncManager n Activate register).

48.6.2.69 ESC SyncManager n Control register (ESC_SMnCTRL)

Address offset: 0x0804 + 0x8 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved	WDTEN	PDIINT	ECATINT	DIR[1:0]		OM[1:0]	
	r	r		r		r	

Bit field	Name	Description
7	Reserved	Reserved, the reset value must be maintained.
6	WDTEN	Watchdog Trigger Enable: 0: Disabled 1: Enabled *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
5	PDIINT	Interrupt in AL Event Request Register: 0: Disabled 1: Enabled *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
4	ECATINT	Interrupt in ECAT Event Request Register: 0: Disabled 1: Enabled *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
3:2	DIR	Direction: 00: Read: ECAT read access, PDI write access 01: Write: ECAT write access, PDI read access Others: Reserved *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
1:0	OM	Operation Mode:

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Bit field	Name	Description
		00: Buffered (3 buffer mode) 10: Mailbox (Single buffer mode) Others: Reserved *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Register can only be written if SyncManager is disabled (bit 0 is 0 in the SyncManager n Activate register).

48.6.2.70 ESC SyncManager n Status register (ESC_SMnSTS)

Address offset: 0x0805 + 0x8 × n (n = 0 to 7)

Reset value: 0x30

7	6	5	4	3	2	1	0
WBUFSTS	RBUFSTS	BUFSTS[1:0]		MBSTS	Reserved	RINT	WINT
r	r	r		r		r	r

Bit field	Name	Description
7	WBUFSTS	Write Status Indication: Indicates that the buffer is being written.
6	RBUFSTS	Read Status Indication: Indicates that the buffer is being written.
5:4	BUFSTS	Buffer Status Indication: Indicates the buffer status in buffer mode (last written buffer). This bit is not used in mailbox mode. 00: 1st buffer 01: 2nd buffer 10: 3rd buffer 11: No buffer written
3	MBSTS	Mailbox Status Indication: This bit is not used in buffer mode. 0: Mailbox empty 1: Mailbox full
2	Reserved	Reserved, the reset value must be maintained.
1	RINT	Interrupt Read: 0: Interrupt cleared after first byte of buffer was written 1: Interrupt after buffer was completely and successfully read *NOTE: This interrupt is signalled to the writing side if enabled in the SM Control register.*
0	WINT	Interrupt Write: 0: Interrupt cleared after first byte of buffer was read 1: Interrupt after buffer was completely and successfully written *NOTE: This interrupt is signalled to the reading side if enabled in the SM Control*

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Bit field	Name	Description
		register.

48.6.2.71 ESC SyncManager n Activate register (ESC_SMnACT)

Address offset: 0x0806 + 0x8 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
PDILE	ECATLE	Reserved				REPREQ	SMEN
r	r					r	r

Bit field	Name	Description
7	PDILE	Latch Event PDI: 0: No latch events 1: Generate Latch events when PDI issues a buffer exchange or when PDI accesses buffer start address *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
6	ECATLE	Latch Event ECAT: 0: No latch events 1: Generate Latch event when EtherCAT master issues a buffer exchange *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
5:2	Reserved	Reserved, the reset value must be maintained.
1	REPREQ	Repeat Request: A toggle of Repeat Request means that a mailbox retry is needed (primarily used in conjunction with ECAT Read Mailbox) *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
0	SMEN	SyncManager Enable/Disable: 0: Disable: Access to Memory without SyncManager control 1: Enable: SyncManager is active and controls Memory area set in configuration *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Reading this register from the PDI in all SyncManagers which have changed activation clears bit 4 of the AL Event Request register.

48.6.2.72 ESC SyncManager n PDI Control register (ESC_SMnPDICTRL)

Address offset: 0x0807 + 0x8 × n (n = 0 to 7)

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						REPACK	DACTSM
						rw	rw

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Bit field	Name	Description
7:2	Reserved	Reserved, the reset value must be maintained.
1	REPACK	Repeat Acknowledge: If this bit is set to the same value as set by bit 1 (Repeat Request) of the SyncManager Activate register, the PDI acknowledges the execution of a previous set repeat request. *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*
0	DACTSM	Deactivate SyncManager: **Read:** 0: Normal operation, SyncManager activated 1: SyncManager deactivated and reset. SyncManager locks access to Memory area **Write:** 0: Activate SyncManager 1: Request SyncManager deactivation Writing 1 is delayed until the end of the frame, which is currently processed. *NOTE: This bit field ECAT is read-only, PDI is readable and writable.*

48.6.2.73 ESC DC Receive Time Port 0 register (ESC_DCRXTIMP0)

Address offset: 0x0900

Reset value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIMEH[23:8]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEH[7:0]								TIMEL[7:0]							
r								r							

Bit field	Name	Description
31:8	TIMEH	Local time at the beginning of the last receive frame containing a write access to this register.
7:0	TIMEL	**Write:** A write access to this register with BWR or FPWR latches the local time at the beginning of the receive frame (start first bit of preamble) at each port **Read:** Local time at the beginning of the last receive frame containing a write access to this register FPWR requires an address match for accessing this register like any FPWR command. All write commands with address match will increment the working counter (e.g., APWR), but they will not trigger receive time latching.

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Bit field	Name	Description
		NOTE: This bit field ECAT is readable and writable, PDI is read-only.

NOTE: The time stamps cannot be read in the same frame in which this register was written.

48.6.2.74 ESC DC Receive Time Port 1 register (ESC_DCRXTIMP1)

Address offset: 0x0904

Reset value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[31:16]															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME[15:0]															
r															

Bit field	Name	Description
31:0	TIME	Local time at the beginning of a frame (start first bit of preamble) received at port 1 containing a BWR or FPWR to the DC Receive Time Port 0 register.

48.6.2.75 ESC DC System Time register (ESC_DCSYSTIM)

Address offset: 0x0910

Reset value: 0x0000 0000

63	32
TIMEH[63:32]	
r	

31	0
TIMEL[31:0]	
r	

Bit field	Name	Description
63:32	TIMEH	**ECAT read access:** Local copy of the System Time when the frame passed the reference clock (i.e., including System Time Delay). Time latched at beginning of the frame (Ethernet SOF delimiter). **PDI read access:** Local copy of the System Time. Time latched when reading first byte.
31:0	TIMEL	**ECAT/PDI read access:**

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Bit field	Name	Description
		Same behavior as bits [63:32]. **ECAT write access:** Written value will be compared with the local copy of the System time. The result is an input to the time control loop. Written value will be compared at the end of the frame with the latched (SOF) local copy of the System time if at least the first byte was written. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.76 ESC DC Receive Time ECAT Processing Unit register (ESC_DCRXTIMEPU)

Address offset: 0x0918

Reset value: Undefined

63	32
TIME[63:32]	
r	

31	0
TIME[31:0]	
r	

Bit field	Name	Description
63:0	TIME	Local time at the beginning of a frame (start first bit of preamble) received at the ECAT Processing Unit containing a write access to the DC Receive Time Port 0 register.

NOTE: E.g., if port 0 is open, this register reflects the Receive Time Port 0 as a 64 Bit value. Any valid EtherCAT write access to the DC Receive Time Port 0 register triggers latching, not only BWR/FPWR commands as with the DC Receive Time Port 0 register.

48.6.2.77 ESC DC System Time Offset register (ESC_DCSYSTIMOST)

Address offset: 0x0920

Reset value: 0x0000 0000

63	32
TIME[63:32]	
r	

31	0
TIME[31:0]	
r	

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Bit field	Name	Description
63:0	TIME	Difference between local time and System Time. Offset is added to the local time. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.78 ESC DC System Time Delay register (ESC_DCSYSTIMDLY)

Address offset: 0x0928

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DELAY[31:16]															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAY[15:0]															
r															

Bit field	Name	Description
31:0	DELAY	Delay between Reference Clock and the ESC. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.79 ESC DC System Time Difference register (ESC_DCSYSTIMDIFF)

Address offset: 0x092C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCP	VALUE[30:16]														
r	r														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE[15:0]															
r															

Bit field	Name	Description
31	LCP	System Time Greater/Less Indication: 0: Local copy of System Time less than received System Time 1: Local copy of System Time greater than or equal to received System Time
30:0	VALUE	Mean difference between local copy of System Time and received System Time values: Difference = Received System Time – local copy of System Time

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

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48.6.2.80 ESC DC Speed Counter Start register (ESC_DCSCSAT)

Address offset: 0x0930

Reset value: 0x1000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	VALUE[14:0]														
r															

Bit field	Name	Description
15	Reserved	Reserved, the reset value must be maintained.
14:0	VALUE	Bandwidth for adjustment of local copy of System Time (larger values → smaller bandwidth and smoother adjustment). A write access resets DC System Time Difference register and DC Speed Counter Difference register. Valid values: 0x0080 to 0x3FFF *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.81 ESC DC Speed Counter Difference register (ESC_DCSCDIFF)

Address offset: 0x0932

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE[15:0]															
r															

Bit field	Name	Description
15:0	VALUE	Representation of the deviation between local clock period and Reference Clock's clock period (representation: two's complement). Range: ± (ESC_DCSCSAT – 0x7F).

NOTE: Calculate the clock deviation after System Time Difference has settled at a low value as follows:

$$Deviation = \frac{ESC_DCSCNTDIFF}{5(ESC_DCSCSAT + ESC_DCSCDIFF + 2)(ESC_DCSCSAT - ESC_DCSCDIFF + 2)}$$

48.6.2.82 ESC DC System Time Difference Filter Depth register (ESC_DCSTDFD)

Address offset: 0x0934

Reset value: 0x04

7	6	5	4	3	2	1	0
Reserved				DEPTH[3:0]			

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r

Bit field	Name	Description
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DEPTH	Filter depth for averaging the received System Time deviation. A write access resets the DC System Time Difference register. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.83 ESC DC Speed Counter Filter Depth register (ESC_DCSCFD)

Address offset: 0x0935

Reset value: 0x0C

7	6	5	4	3	2	1	0
Reserved				DEPTH[3:0]			
				r			

Bit field	Name	Description
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DEPTH	Filter depth for averaging the clock period deviation. A write access resets the internal speed counter filter. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

NOTE: Reset internal speed counter filter by writing the DC Speed Counter Start register after changing this value.

48.6.2.84 ESC DC Cyclic Unit Control register (ESC_DCCUCTRL)

Address offset: 0x0980

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved		LATCH1	LATCH0	Reserved			SYNC
		r	r				r

Bit field	Name	Description
7:6	Reserved	Reserved, the reset value must be maintained.
5	LATCH1	Latch In unit 1: 0: ECAT-controlled 1: PDI-controlled Latch interrupt is routed to ECAT/PDI depending on this setting.

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Bit field	Name	Description
		NOTE: This bit field ECAT is readable and writable, PDI is read-only.
4	LATCH0	Latch In unit 0: 0: ECAT-controlled 1: PDI-controlled Latch interrupt is routed to ECAT/PDI depending on this setting. *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*
3:1	Reserved	Reserved, the reset value must be maintained.
0	SYNC	SYNC out unit control: 0: ECAT-controlled 1: PDI-controlled *NOTE: This bit field ECAT is readable and writable, PDI is read-only.*

48.6.2.85 ESC DC Activation register (ESC_DCACT)

Address offset: 0x0981

Reset value: 0x00

7	6	5	4	3	2	1	0
SSDP	NFCFG	STPC	STCOEXT	AUTOACT	SYNC1	SYNC0	SYNCACT
rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
7	SSDP	SyncSignal Debug Pulse: 0: Deactivated 1: Immediately generates a single debug ping on the SYNC0/1 pins in accord with the setting of bits 1 and 2 of this register This bit is self-clearing, always read 0. All pulses are generated at the same time, the cycle time is ignored. The configured pulse length is used.
6	NFCFG	Near Future Configuration: 0: ½ DC width future (2^{31} ns or 2^{63} ns) 1: ~2.1 sec. future (2^{31} ns)
5	STPC	Start Time Plausibility Check: 0: Disabled. SyncSignal generation if Start Time is reached 1: Immediate SyncSignal generation if Start Time is outside near future (see bit 6)
4	STCOEXT	Extension of Start Time Cyclic Operation: 0: No extension 1: Extend 32 bit written Start Time to 64 bit
3	AUTOACT	Auto-activation by writing Start Time Cyclic Operation: 0: Disabled 1: Auto-activation enabled. Bit 0 is set automatically after Start Time is written.

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Bit field	Name	Description
2	SYNC1	SYNC1 generation: 0: Deactivated 1: SYNC1 pulse is generated
1	SYNC0	SYNC0 generation: 0: Deactivated 1: SYNC0 pulse is generated
0	SYNCACT	Sync Out Unit activation: 0: Deactivated 1: Activated

NOTE: Writing to this register depends on the setting of bit 0 of the DC Cyclic Unit Control register.

48.6.2.86 ESC DC Pulse Length of SyncSignals register (ESC_DCSSPLEN)

Address offset: 0x0982

Reset value: 0x0064

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PULSELEN[15:0]															
r															

Bit field	Name	Description
15:0	PULSELEN	Pulse length of SyncSignals (in Units of 10ns). 0: Acknowledge mode: SyncSignal will be cleared by reading SYNC0/1 Status register.

48.6.2.87 ESC DC Activation Status register (ESC_DCACTSTS)

Address offset: 0x0984

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved					PLARES	SYNC1STS	SYNC0STS
					r	r	r

Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained.
2	PLARES	Plausibility Result indication: Indicates the plausibility check result of the DC Start Time Cyclic Operation register while the Sync output unit is activated. 0: Start Time was within near future 1: Start Time was out of near future (DC Activation register bit 6)
1	SYNC1STS	SYNC1 Status indication:

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Bit field	Name	Description
		0: First SYNC1 pulse is not pending 1: First SYNC1 pulse is pending
0	SYNC0STS	SYNC0 Status indication: 0: First SYNC0 pulse is not pending 1: First SYNC0 pulse is pending

48.6.2.88 ESC DC SYNC0 Status register (ESC_DCSYNC0STS)

Address offset: 0x098E

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved							STATE
							r

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	STATE	SYNC0 State for Acknowledge mode: SYNC0 in Acknowledge mode is cleared by reading this register from PDI, use only in Acknowledge mode.

NOTE: Reading this register from PDI clears AL Event Request register bit 2.

48.6.2.89 ESC DC SYNC1 Status register (ESC_DCSYNC1STS)

Address offset: 0x098F

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved							STATE
							r

Bit field	Name	Description
7:1	Reserved	Reserved, the reset value must be maintained.
0	STATE	SYNC1 State for Acknowledge mode: SYNC1 in Acknowledge mode is cleared by reading this register from PDI, use only in Acknowledge mode.

NOTE: Reading this register from PDI clears AL Event Request register bit 3.

48.6.2.90 ESC DC Start Time Cyclic Operation register (ESC_DCSTCOPE)

Address offset: 0x0990

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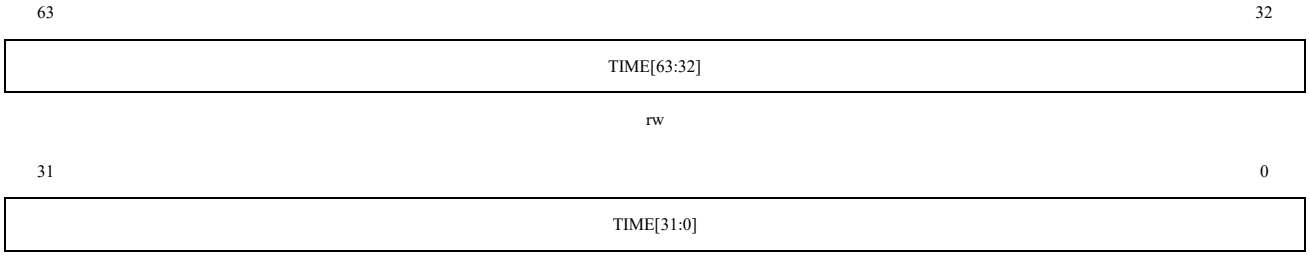
Reset value: 0x0000 0000 0000 0000



Bit field	Name	Description
63:0	TIME	**Write:** Start time (System time) of cyclic operation in ns. **Read:** System time of next SYNC0 pulse in ns.

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

Write to this register depends upon setting of bit 0 of the DC Cyclic Unit Control register. Write value is taken over when bit 0 of the DC Activation register has a transition to 1.

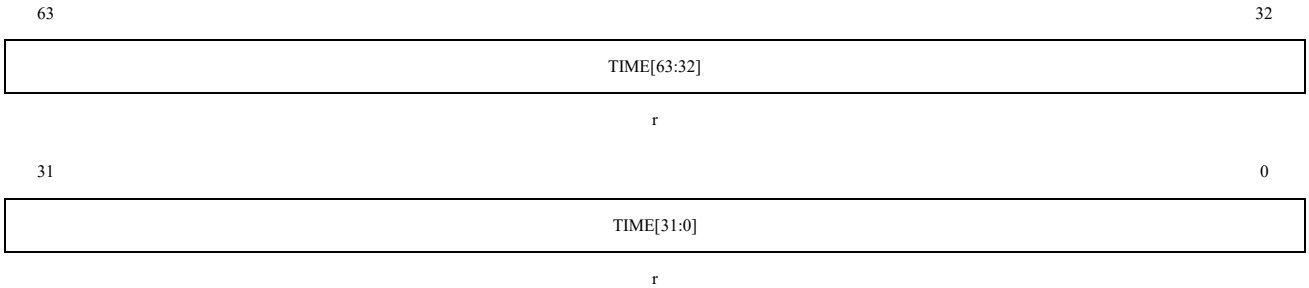
Auto-activation (bit 3 of the DC Activation register is 1): bit 0 of the DC Activation register is set automatically after this register is written.

Extension of Start Time (bit 4 of the DC Activation register is 1): upper 32 bits are automatically extended after writing this register if only lower 32 bits are written within one frame.

48.6.2.91 ESC DC Next SYNC1 Pulse register (ESC_DCNSYNC1P)

Address offset: 0x0998

Reset value: 0x0000 0000 0000 0000



Bit field	Name	Description
63:0	TIME	System time of next SYNC1 pulse in ns.

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which

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guarantees reading a consistent value.

48.6.2.92 ESC DC SYNC0 Cycle Time register (ESC_DCSYNC0CT)

Address offset: 0x09A0

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME[15:0]															
rw															

Bit field	Name	Description
31:0	TIME	Time between two consecutive SYNC0 pulses in ns. 0: Single shot mode, generate only one SYNC0 pulse.

NOTE: Writing to this register depends on the setting of bit 0 of the DC Cyclic Unit Control register.

48.6.2.93 ESC DC SYNC1 Cycle Time register (ESC_DCSYNC1CT)

Address offset: 0x09A4

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[31:16]															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME[15:0]															
rw															

Bit field	Name	Description
31:0	TIME	Time between SYNC0 pulse and SYNC1 pulse in ns.

NOTE: Writing to this register depends on the setting of bit 0 of the DC Cyclic Unit Control register.

48.6.2.94 ESC DC Latch0 Control register (ESC_DCLATCH0CTRL)

Address offset: 0x09A8

Reset value: 0x00

7	6	5	4	3	2	1	0

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Reserved	NEGEDGE	POSEDGE
	rw	rw

Bit field	Name	Description
7:2	Reserved	Reserved, the reset value must be maintained.
1	NEGEDGE	Latch0 negative edge: 0: Continuous Latch active 1: Single event (only first event active)
0	POSEDGE	Latch0 positive edge: 0: Continuous Latch active 1: Single event (only first event active)

NOTE: Write access depends upon setting of bit 4 of the DC Cyclic Unit Control register.

48.6.2.95 ESC DC Latch1 Control register (ESC_DCLATCH1CTRL)

Address offset: 0x09A9

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						NEGEDGE	POSEDGE
						rw	rw

Bit field	Name	Description
7:2	Reserved	Reserved, the reset value must be maintained.
1	NEGEDGE	Latch1 negative edge: 0: Continuous Latch active 1: Single event (only first event active)
0	POSEDGE	Latch1 positive edge: 0: Continuous Latch active 1: Single event (only first event active)

NOTE: Write access depends upon setting of bit 5 of the DC Cyclic Unit Control register.

48.6.2.96 ESC DC Latch0 Status register (ESC_DCLATCH0STS)

Address offset: 0x09AE

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved					PINSTS	EVENTNEG	EVENTPOS
					r	r	r

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Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained.
2	PINSTS	Latch0 pin state: Indicates the state of the Latch 0 input pin.
1	EVENTNEG	Event Latch0 negative edge: 0: Negative edge not detected or continuous mode 1: Negative edge detected in single event mode only Flag cleared by reading out the DC Latch0 Time Negative Edge register.
0	EVENTPOS	Event Latch0 positive edge: 0: Positive edge not detected or continuous mode 1: Positive edge detected in single event mode only Flag cleared by reading out the DC Latch0 Time Positive Edge register.

48.6.2.97 ESC DC Latch1 Status register (ESC_DCLATCH1STS)

Address offset: 0x09AF

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved					PINSTS	EVENTNEG	EVENTPOS
					r	r	r

Bit field	Name	Description
7:3	Reserved	Reserved, the reset value must be maintained.
2	PINSTS	Latch1 pin state: Indicates the state of the Latch 1 input pin.
1	EVENTNEG	Event Latch1 negative edge: 0: Negative edge not detected or continuous mode 1: Negative edge detected in single event mode only Flag cleared by reading out the DC Latch1 Time Negative Edge register.
0	EVENTPOS	Event Latch1 positive edge: 0: Positive edge not detected or continuous mode 1: Positive edge detected in single event mode only Flag cleared by reading out the DC Latch1 Time Positive Edge register.

48.6.2.98 ESC DC Latch0 Time Positive Edge register (ESC_DCNLATCH0TPE)

Address offset: 0x09B0

Reset value: 0x0000 0000 0000 0000

63	32
TIME[63:32]	
r	

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31	0
TIME[31:0]	
r	

Bit field	Name	Description
63:0	TIME	System time at the positive edge of the Latch0 signal.

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears DC Latch0 Status register's bit 0 if bit 4 of the Cyclic Unit Control register is 0.

48.6.2.99 ESC DC Latch0 Time Negative Edge register (ESC_DCNLATCH0TNE)

Address offset: 0x09B8

Reset value: 0x0000 0000 0000 0000

63	32
TIME[63:32]	
r	

31	0
TIME[31:0]	
r	

Bit field	Name	Description
63:0	TIME	System time at the negative edge of the Latch0 signal.

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears DC Latch0 Status register's bit 1 if bit 4 of the Cyclic Unit Control register is 0.

48.6.2.100 ESC DC Latch1 Time Positive Edge register (ESC_DCNLATCH1TPE)

Address offset: 0x09C0

Reset value: 0x0000 0000 0000 0000

63	32
TIME[63:32]	
r	

31	0
TIME[31:0]	
r	

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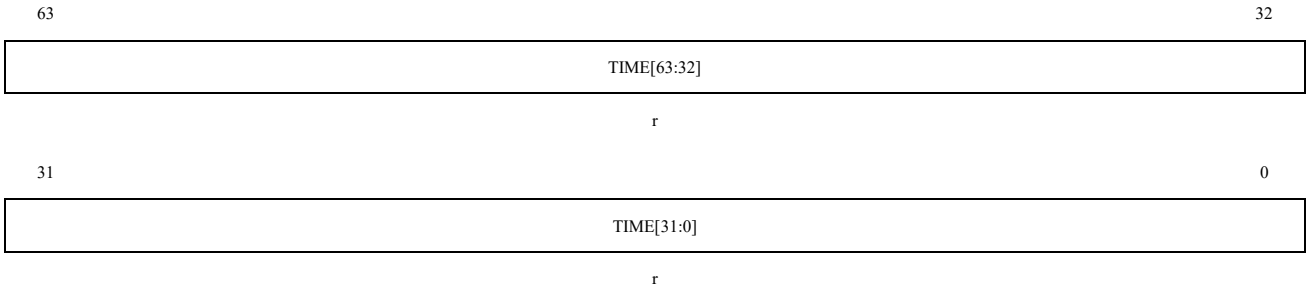
Bit field	Name	Description
63:0	TIME	System time at the positive edge of the Latch1 signal.

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears DC Latch1 Status register's bit 0 if bit 5 of the Cyclic Unit Control register is 0.

48.6.2.101 ESC DC Latch1 Time Negative Edge register (ESC_DCNLATCH1TNE)

Address offset: 0x09C8

Reset value: 0x0000 0000 0000 0000



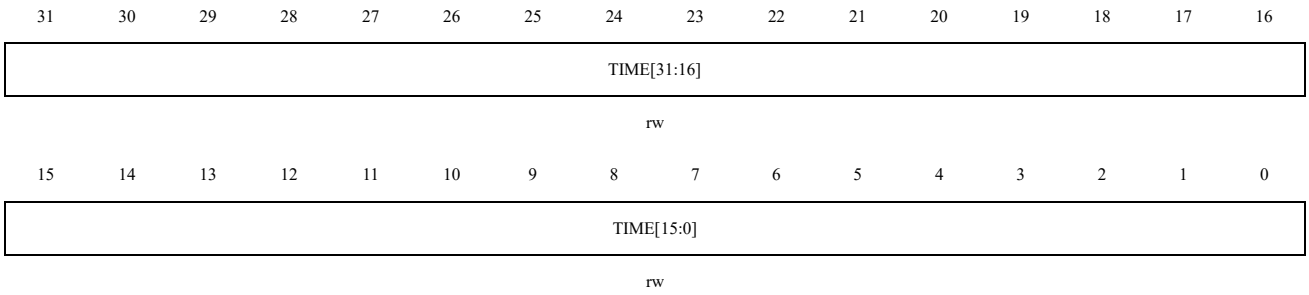
Bit field	Name	Description
63:0	TIME	System time at the negative edge of the Latch1 signal.

NOTE: Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value. Reading this register from ECAT clears DC Latch1 Status register's bit 1 if bit 5 of the Cyclic Unit Control register is 0.

48.6.2.102 ESC DC ECAT Buffer Change Event Time register (ESC_DCECATBCET)

Address offset: 0x09F0

Reset value: 0x0000 0000



Bit field	Name	Description
31:0	TIME	Local time at the beginning of the frame which causes at least one SyncManager to assert an ECAT event (switching the buffers).

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NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

48.6.2.103 ESC DC PDI Buffer Start Event Time register (ESC_DCPDIBSET)

Address offset: 0x09F8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME[15:0]															
rw															

Bit field	Name	Description
31:0	TIME	Local time when at least one SyncManager asserts a PDI buffer start event (access to the address where a buffer starts).

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

48.6.2.104 ESC DC PDI Buffer Change Event Time register (ESC_DCPDIBCET)

Address offset: 0x09FC

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME[15:0]															
rw															

Bit field	Name	Description
31:0	TIME	Local time when at least one SyncManager asserts a PDI buffer change event (switching the buffers).

NOTE: Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

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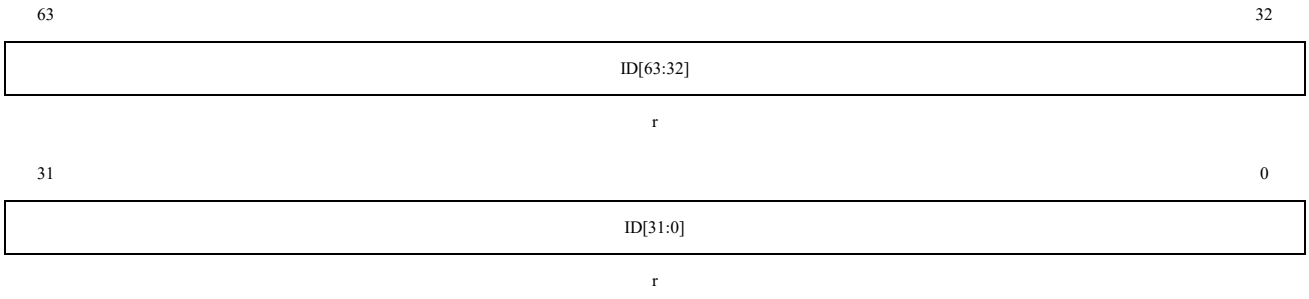
48.6.2.105 ESC Product ID register (ESC_PRODUCTID)

Address offset: 0x0E00

Reset value: 0x0030 0020 0010 0000

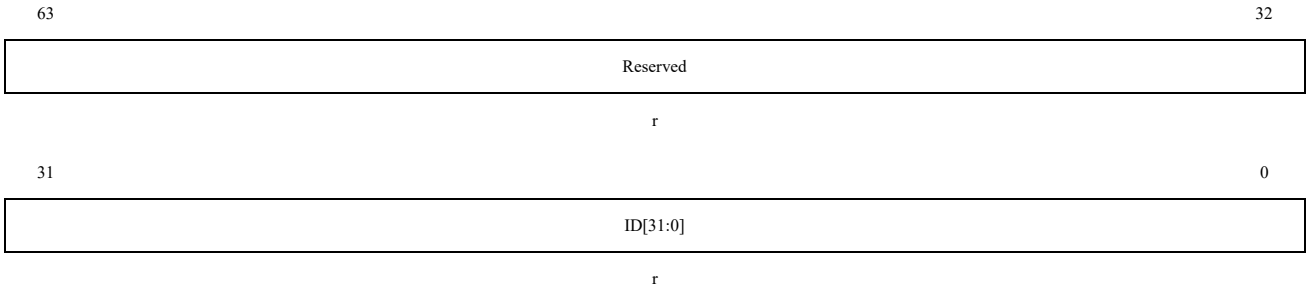


Bit field	Name	Description
63:0	ID	Product ID.

48.6.2.106 ESC Vendor ID register (ESC_VENDORID)

Address offset: 0x0E08

Reset value: 0xEEEE EEEE 0030 0077



Bit field	Name	Description
63:32	Reserved	Reserved, the reset value must be maintained.
31:0	ID	Vendor ID.

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49 Secure Data Process Unit (SDPU)

49.1 Introduction

SDPU combine SAC and SDMA modules together, SAC includes AES, DES, SM4, SHA and RNGC(Entropy Post Process) algorithms. SDMA transfer calculation data from SRAM to SAC and calculation result from SAC to SRAM.

49.2 Main Features

- Supports DES symmetric algorithm
  - DES and 3DES encryption and decryption operations are supported
  - TDES supports 2KEY and 3KEY modes.
  - Support CBC and ECB modes
- Supports the SYMMETRIC AES algorithm
  - 128bit/192bit/ 256bit key length is supported
  - Supports CBC, ECB and CTR modes
- Supports SM4 symmetric algorithm
  - Supports CBC, ECB modes
- Supports SHA hash algorithm
  - Support SHA1,SHA224,SHA256,SHA384,SHA512
- Supports RNG.
  - Support TRNG & PRNG mode
  - Support LSFR129 for post process
  - Support XOR combine all the source
  - Support FIPS-140 CAVP
- Support RNG and other algorithms running at the meantime
- Support FIFO configure
  - Support algorithm data configured through FIFO
- Support SDMA Data Transport
  - Support auto transport data as a master from/to SRAM through AHB interface
  - Support base address of SRAM transport through parameter
  - Support data transport max size = 4KB (1024words)
  - Support data transport data size check

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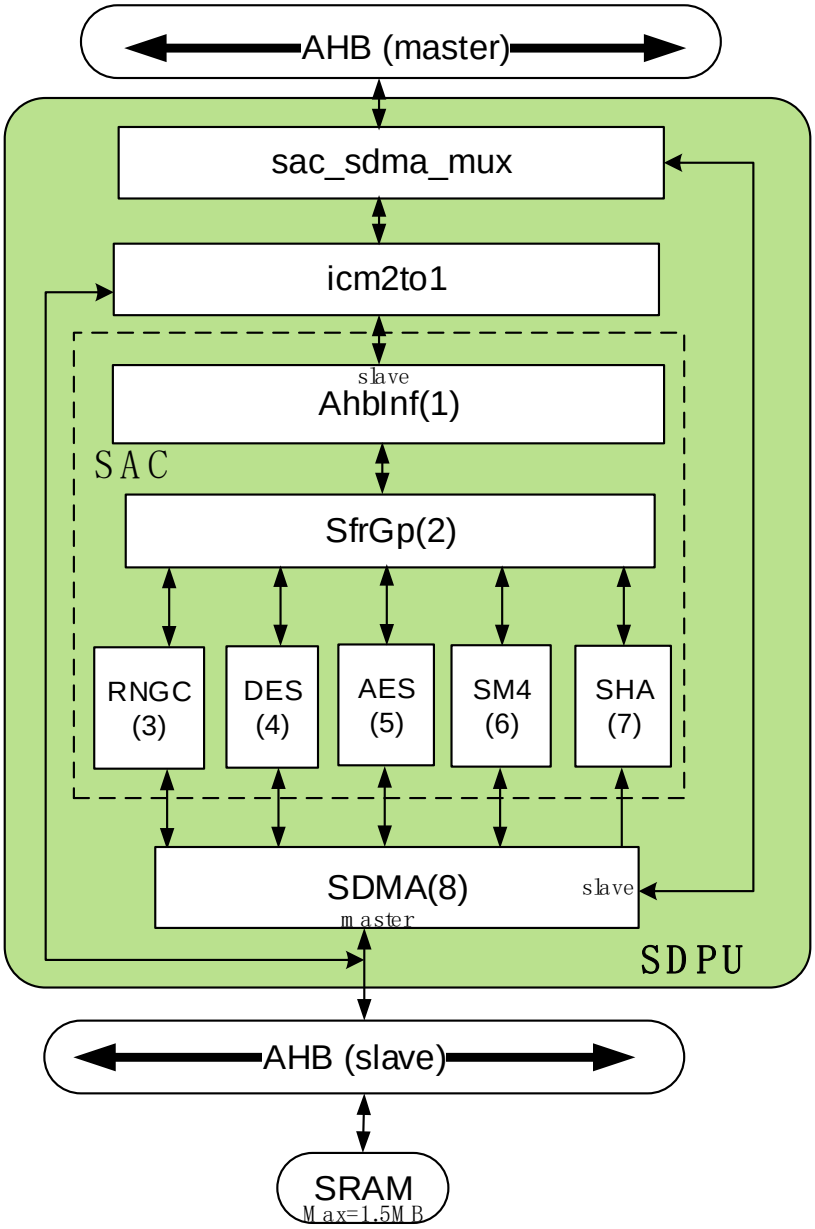
– Support data transport CRC16 calculation

– Support SRAM max size = 2MB (512Kwords)

– Support Data rejoin in the case of source/destination address offset = 1/2/3

49.3 Block diagram

Figure 49-1 I2S Block Diagram



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50 CRC Calculation Unit (CRC)

50.1 Introduction

The CRC (cyclic redundancy check) calculation unit generates a CRC code from 8-, 16- or 32-bit data word using a configurable generator polynomial. CRC-based methods are widely employed to ensure the integrity of data during transmission or storage. Specially, for the functional safety standards, this method provides a way to verify the storage integrity. The CRC calculation unit plays a critical role in this process by computing a software signature during runtime. This runtime signature is then compared with a reference signature generated at link time and stored in a given memory location.

50.2 Main Features

- Uses CRC-32 (Ethernet) polynomial as default: 0x4C11DB7
  - X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 +X8 + X7 + X5 + X4 + X2+ X +1
- Alternatively, uses fully programmable polynomial with programmable size (7, 8, 16, 32bits)
- Handles 8-,16-, 32-bit data size
- Programmable CRC initial value
- Single input/output 32-bit data register
- Input buffer to avoid bus stall during calculation
- CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size
- General-purpose 32-bit register (can be used for temporary storage)
- Reversibility option on I/O data
- Support CRC Data input and output XOR operation with configurable data

50.3 Block Diagram

The block diagram of CRC module is described as below:

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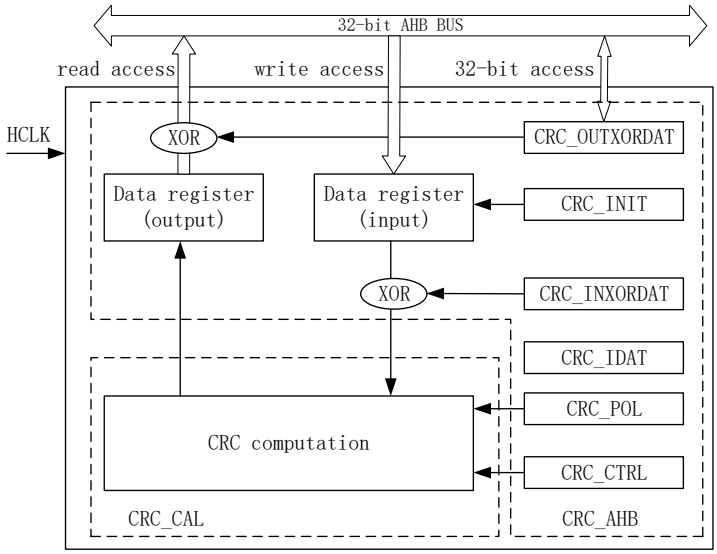
Figure 50-1 CRC Block Diagram



CRC_AHB

This module is the interface component that connects the CRC calculation unit module to a 32-bit AHB master. It handles both read and write accesses from the bus. The module consists of several registers to control and receive status from the CRC calculation core.

CRC_CAL

This module is the core component responsible for CRC calculations. It receives data from the CRC_AHB for CRC processing, calculate CRC and output data after CRC processing.

50.4 Function Description

50.4.1 CRC Programming Sequence

1. Configure CRC_CTRL[7:5] select bit order of input and output data.

   Configure CRC_CTRL[2:1] select byte order of input data.

   Configure CRC_CTRL[4:3] select the size of polynomial.
2. Configure CRC_POL select polynomial of CRC.
3. Configure CRC_CTRL [0]=1 or CRC_INIT if need, reset initial CRC calculation result.
4. Configure CRC_INXORDAT and CRC_OUTXORDAT set input and output XOR data.
5. Write CRC_DAT, configure data to be verified.
6. Read CRC_DAT, get CRC calculation result.
7. If following data still be verified, go to step 5.

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50.4.2 Detail operation

50.4.2.1 Data Reversal

The data written to CRC_DAT register can have its bit order reversed in 8-bit, 16-bit or 32-bit chunks based on the REVIN[1:0] in the CRC_CTRL register. Below table show an example of write data reverse function, with write data is 0x1A2B3C4D

Table 50-1 REV_IN Function Example

REVIN[1:0]	Write data after reversal	Description
00	0x1A2B3C4D	Not reverse. Original write data is kept.
01	0x58D43CB2	The bit order in each byte is reversed.
10	0xD458B23C	The bit order in each half-word is reversed.
11	0xB23CD458	The bit order of the whole word is reversed.

The data written to CRC_DAT register can also be reversed based on the BYTEENDIAN [1:0] bits in the CRC_CTRL register. Below table shows an example of byte reversal function, with original write data is 0x1A2B3C4D.

Table 50-2 BYTEENDIAN Function Example

BYTEENDIAN [1:0]	Write data after reversal	Description
00/01	0x1A2B3C4D	Not reverse. Original write data is kept.
10	0x2B1A4D3C	2 bytes in each half-word are reversed in order.
11	0x4D3C2B1A	4 bytes in the word are reversed in order.

CRC_DAT write operation performs BYTEENDIAN reversal firstly and REVIN reversal secondly.

The CRC_DAT output data can also be reversed by setting the REVOUT bit in the CRC_CTRL register. Below table shows an example of CRC_DAT output reversal function, with original output data is 0x11223344.

Table 50-3 REV_OUT Function Example

REVOUT	CRC_DAT output after reversal	Description
0	0x11223344	Not reverse. Data output is kept.
1	0x22CC4488	Each bit of data output is reversed in order.

50.4.2.2 Initialization Operation

The CRC calculator can be initialized to a programmable value using the RESET control bit in the CRC_CTRL register (the default value is 0xFFFFFFFF).

The initial CRC value can be programmed with the CRC_INIT register. The CRC_DAT register is automatically initialized upon CRC_INIT register write access.

50.4.2.3 Independent Data Register

The CRC_IDAT register can be used to hold a temporary value related to CRC calculation. It is not affected by the RESET bit in the CRC_CTRL register

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50.4.2.4 Polynomial Programmability

The polynomial coefficients are fully programmable through the CRC_POL register, and the polynomial size can be configured to be 7, 8, 16 or 32 bits by programming the POLYSIZE[1:0] bits in the CRC_CTRL register. If the CRC data is less than 32-bit, its value can be read from the least significant bits of the CRC_DAT register. To obtain a reliable CRC calculation, the change on-fly of the polynomial value or size cannot be performed during a CRC calculation. As a result, if a CRC calculation is ongoing, the application must either reset it or perform a CRC_DAT read before changing the polynomial.

The default polynomial value is the CRC-32 (Ethernet) polynomial: 0x4C11DB7.

Table 50-4 CRC Polynomial Example

polynomial size	polynomial (P=CRC_POL)
CRC7	$x^7+P[6]x^6+P[5]x^5+P[4]x^4+P[3]x^3+P[2]x^2+P[1]x+P[0]$
CRC8	$x^8+P[7]x^7+P[6]x^6+P[5]x^5+P[4]x^4+P[3]x^3+P[2]x^2+P[1]x+P[0]$
CRC16	$x^{16}+P[15]x^{15}+P[14]x^{14}+P[13]x^{13}+P[12]x^{12}+P[11]x^{11}+P[10]x^{10}+P[9]x^9+P[8]x^8+P[7]x^7+P[6]x^6+P[5]x^5+P[4]x^4$ $+P[3]x^3+P[2]x^2+P[1]x+P[0]$
CRC32	$X^{32}+P[31]x^{31}+P[30]x^{30}+P[29]x^{29}+P[28]x^{28}+P[27]x^{27}+P[26]x^{26}+P[25]x^{25}+P[24]x^{24}+P[23]x^{23}+P[22]x^{22}+$ $P[21]x^{21}+P[20]x^{20}+P[19]x^{19}+P[18]x^{18}+P[17]x^{17}+P[16]x^{16}+P[15]x^{15}+P[14]x^{14}+P[13]x^{13}+P[12]x^{12}+P[11]x^{11}+$ $P[10]x^{10}+P[9]x^9+P[8]x^8+P[7]x^7+P[6]x^6+P[5]x^5+P[4]x^4+P[3]x^3+P[2]x^2+P[1]x+P[0]$

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50.5 CRC Registers

50.5.1 CRC Register Overview

Table 50-5 CRC Register Overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	CRC_DAT	DAT[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x04	CRC_IDAT	IDAT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	CRC_CTRL	Reserved																								REVOUT	REVIN[1:0]		POLYSIZE[1:0]		BYTEENDIAN [1:0]		RESET
	Reset Value																									0	0	0	0	0	0	0	0
0x0C	CRC_LRC	LRC[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	CRC_INIT	INIT[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x14	CRC_POL	POL[31:0]																															
	Reset Value	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	0	1	1	0	1	1	1
0x18	CRC_INXORDAT	INXOR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	CRC_OUTXORDAT	OUTXOR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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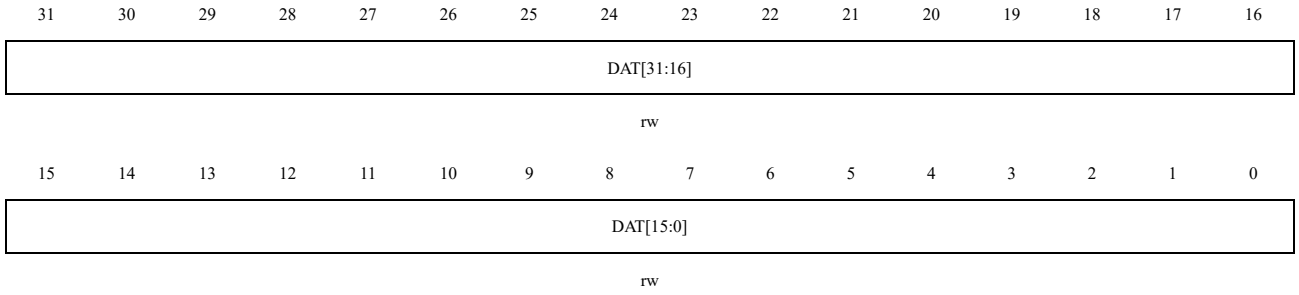
50.5.2 CRC Data Register (CRC_DAT)

Address offset: 0x00

Reset value: 0xFFFF FFFF

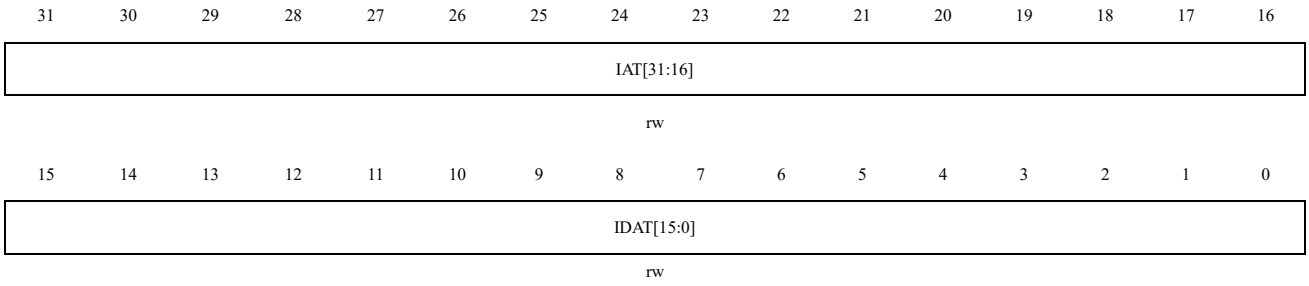


Bit Field	Name	Description
31:0	DAT[31:0]	This register is used to write new data to the CRC calculator. It holds the previous CRC calculation result when it is read. If the data size is less than 32 bits, the least significant bits are used to write/read the correct value.

50.5.3 CRC Independent Data Register (CRC_IDAT)

Address offset: 0x04

Reset value: 0x0000 0000



Bit Field	Name	Description
31:0	IDAT[31:0]	General-purpose 32-bit data register. These bits can be used as a temporary storage location for four bytes. This register is not affected by CRC resets generated by the RESET bit in the CRC_CTRL register.

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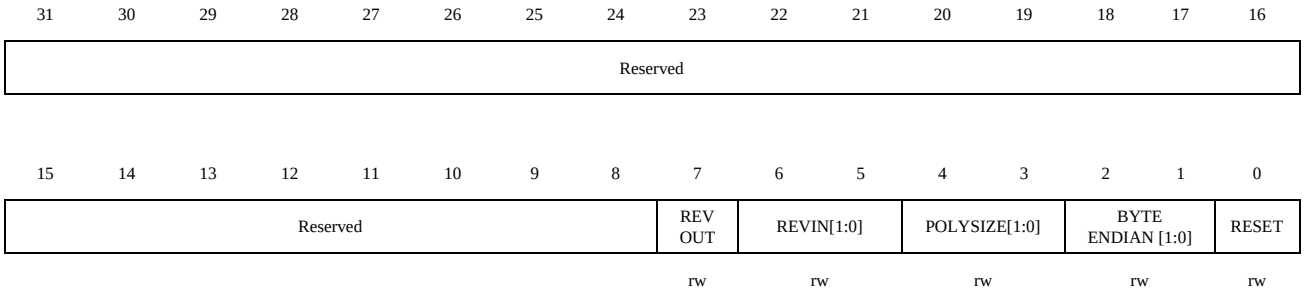
50.5.4 CRC Control Register (CRC_CTRL)

Address offset: 0x08

Reset value: 0x0000 0000



Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	REVOUT	Reverse output data. This bit controls the reversal of the bit order of the output data. 0: Bit order not affected 1: Bit-reversed output format
6:5	REVIN[1:0]	Reverse input data. These bits control the reversal of the bit order of the input data. 00: Bit order not affected 01: Bit reversal done by byte 10: Bit reversal done by half-word 11: Bit reversal done by word
4:3	POLYSIZE[1:0]	Polynomial size. These bits control the size of the polynomial. 00: 32 bit polynomial 01: 16 bit polynomial 10: 8 bit polynomial 11: 7 bit polynomial
2:1	BYTEENDIAN [1:0]	CRC byte Endian These bits control the reversal of the byte order of the input data. 00,01: Byte sequence not affected 10: Byte reversal done by half-word 11: Byte reversal done by word
0	RESET	RESET bit This bit is set by software to reset the CRC calculation unit and set the data register to the value stored in the CRC_INIT register. This bit can only be set, it is automatically cleared by hardware.

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50.5.5 LRC Value Register(CRC_LRC)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LRC[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LRC[15:0]															
rw															

Bit Field	Name	Description
31:0	LRC[31:0]	LRC value register CRC_DAT calculation value, no related to ReverseIn, ReverseOut, ByteEndian, CRC_INXORDAT and CRC_OUTXORDAT.

50.5.6 CRC Initial Value Register(CRC_INIT)

Address offset: 0x10

Reset value: 0xFFFF FFFF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INIT[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INIT[15:0]															
rw															

Bit Field	Name	Description
31:0	INIT[31:0]	Programmable initial CRC value This register is used to write the CRC initial value

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50.5.7 CRC Polynomial Register (CRC_POL)

Address offset: 0x14

Reset value: 0x04C1 1DB7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POL[31:16]															
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POL[15:0]															
rw															

Bit Field	Name	Description
31:0	POL[31:0]	Programmable polynomial This register is used to write the coefficients of the polynomial to be used for CRC calculation. If the polynomial size is less than 32 bits, the least significant bits have to be used to program the correct value.

50.5.8 CRC Input XOR data Register (CRC_INXORDAT)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INXOR [31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INXOR [15:0]															
rw															

Bit Field	Name	Description
31:0	INXOR[31:0]	This register is used to set CRC_DAT XOR calculation value before CRC calculation.

50.5.9 CRC Output XOR data Register (CRC_OUTXORDAT)

Address offset: 0x1C

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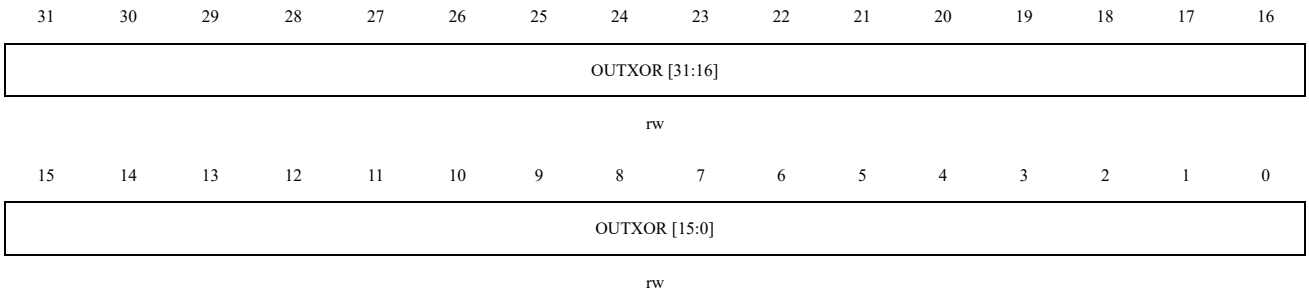
Reset value: 0x0000 0000



Bit Field	Name	Description
31:0	OUTXOR[31:0]	This register is used to set CRC_DAT XOR calculation value after CRC calculation.

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51 Debug Support (DBG)

51.1 Introduction

N32H78x dual core debug sub-system enables software developers to debug and trace their embedded firmware through the use of JTAG or Serial-wire debug access port using industry standard debugging tools. Trace data can be captured via a trace port for logging and analysis

51.2 Main Features

- Independent breakpoint debugging for each CPU core
- Core execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output for Cortex-M7 only
- Serial wire Trace port
- Synchronous Trace port
- Debug and trace during low power modes

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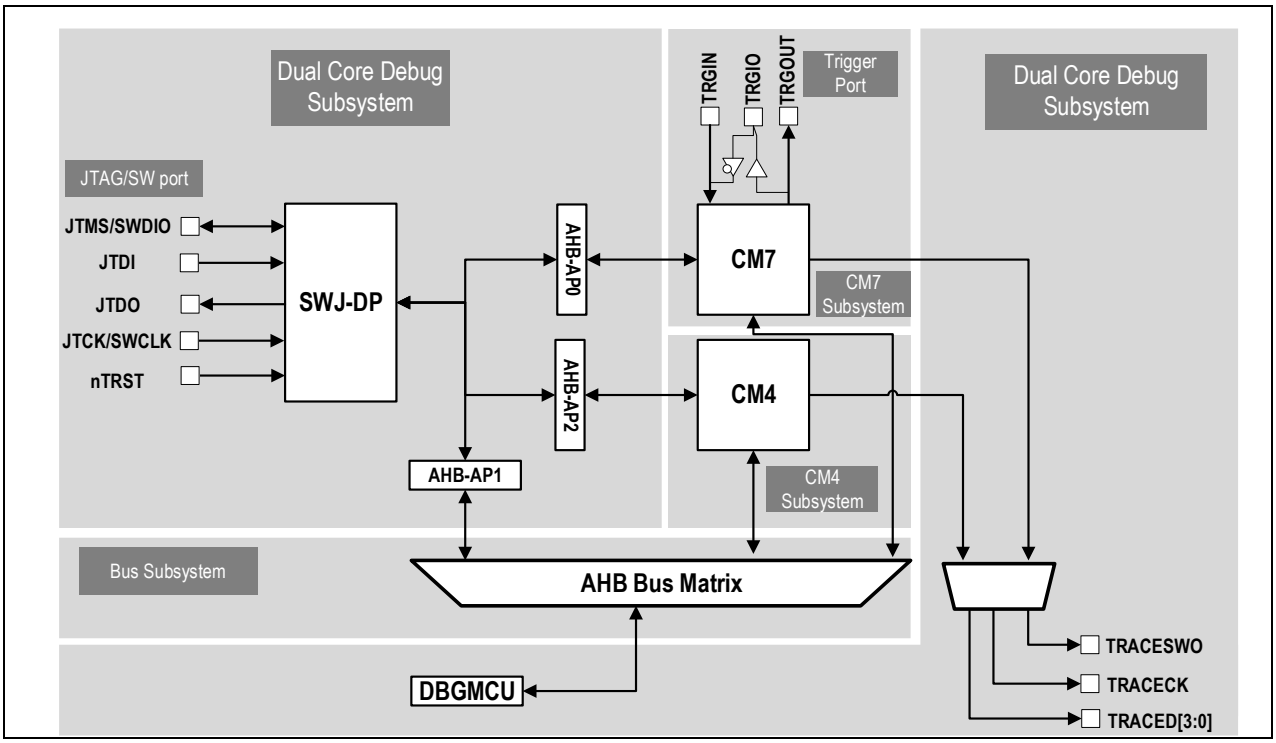
51.3 Debug infrastructure functional description

51.3.1 Debug infrastructure block diagram

The N32H78x debug subsystem is shown in Figure 51-1. Single debug port is shared between ARM Cortex-M7 and ARM Corext-M4. It allows debuggers to connect to the CPUs via JTAG or serial-wire interface as described in chapter 51.3.3.1. Each CPU is assigned to an access port. Additional access port is designed for debug configuration via DBGMCU as shown in chapter. Debug feature of each CPU is described in chapter 51.3.4 and 51.3.5.

Figure 51-1 Debug Block Diagram



51.3.2 Debug ports

Table 51-1 JTAG/Serial-wire debug port pins

Pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Description	
JTMS/SWDIO	I	JTAG test mode select	IO	Serial wire data in/out	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial Wire Clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO	O	JTAG test data output	-	-	PB3
nJTRST	I	JTAG test reset	-	-	PB4

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Table 51-2 Trace port pins

Pin name	Type	Description	Pin assignment
TRACED0	O	Trace synchronous data out 0	PE3
TRACED1	O	Trace synchronous data out 0	PE4
TRACED2	O	Trace synchronous data out 0	PE5
TRACED3	O	Trace synchronous data out 0	PE6
TRACECK	O	Trace clock	PE2

Table 51-3 Serial-wire trace port pins

Pin name	Type	Description	Pin assignment
TRACESWO	O	Single wire trace asynchronous data out	PC12

Note: TRACESWO is multiplexed with JTDO. This means that single wire trace is only available when using the serial wire debug interface, not when using JTAG.

Table 51-4 Trigger pins (Only channel 0 of CTI/CTO of CM7 is used)

Pin name	Type	Description	Pin assignment
TRGIN	I	External trigger input	PJ7
TRGOUT	O	External trigger output	PJ12
TRGIO	IO	External trigger in/out	PC7

Note: TRGIO can be configured as an input or an output by the TRGOEN bit in the DBGMCU. If configured as an input, it is connected to TRGIN. If an output, it is connected to TRGOUT. This is because TRGIN and TRGOUT are not available on certain packages.

Table 51-5 Trace mode configuration

Control Bits		Description	TRACE IO pins					
TRACE_ IOEN	TRACE_ MODE		TRACE SWO	TRACE CK	TRACE D0	TRACE D1	TRACE D2	TRACE D3
0	xx	No Trace (default state)	Released	-				
1	00	Asynchronous Trace	TRACESWO	-	-	Released (usable as GPIO)		
1	01	1-bit Synchronous Trace	Released	TRACECK	TRACED[0]	-	-	-
1	10	2-bit Synchronous Trace		TRACECK	TRACED[0]	TRACED[1]	-	-
1	11	4-bit Synchronous Trace		TRACECK	TRACED[0]	TRACED[1]	TRACED[2]	TRACED[3]

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51.3.3 Debug Access Port Functional Description

The debug access port (DAP) is a debug subsystem including serial-wire and JTAG debug port (SWJ-DP) and three access ports as shown in Figure 51-1.

51.3.3.1 Serial-wire and JTAG debug port (SWJ-DP)

The SWJ-DP is an ARM Coresight component, which is a combined JTAG-DP and SW-DP that enables the chip to connect to a debug tool via either a 2-pin SWD or 5-pin JTAG port

Five debug IOs are configured as debug alternate function mode by default out of reset with internal pull up resistors on JTDI, JTMS/SWDIO, and nJTRST lines as well as pull-down resistors on JTCK/SWCLK line.

A special sequence on the JTMS/SWDIO pin switches between JTAG-DP and SW-DP. When the switching sequence is transmitted to the SWJ-DP, it behaves as a dedicated JTAG-DP or SW-DP depending on which sequence is performed.

In SW-DP mode, the unused JTAG pins (such as JTDI, JTDO and nJTRST) can be utilized for other purposes.

Similarly, software can use these IO pins for other purposes when debug is not needed.

For programming capabilities and features of the SWJ-DP, refer Arm® CoreSight™ SoC-400 Technical Reference Manual..

Serial wire debug port

The Serial wire debug protocol uses two pins:

- SWCLK: clock from host to target
- SWDIO: bi-directional serial data (pull-up required)

Serial data is transferred LSB first, synchronously with the clock. A transfer comprises three phases:

- 8-bit packet request transmitted by the host as described in Table 51-6
- 3-bit acknowledge response transmitted by the target as described in Table 51-7
- 33-bit data transfer phase transmitted by the host (in the case of a write) or target (in the case of a read) as shown in Table 51-8

The data transfer only occurs if the acknowledge response is OK.

If the direction of the data is reversed between each phase, a single clock cycle turn-around time is inserted.

Table 51-6 Packet request phase

Field bits	Name	Description
0	Start	Must be “1”
1	APnDP	0: DP register access 1: AP register access
2	RnW	0: Write request 1: Read request
4:3	A(3:2)	Address field of the DP or AP register

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5	Parity	Single bit parity of preceding bits
6	Stop	0
7	Park	Not driven by host. Must be read as “1” by target.

Table 51-7 Acknowledge response

Field bits	Name	Description
2:0	ACK	000b: FAULT 010b: WAIT 100b: OK

Table 51-8 Data transfer phase

Bit field	Name	Description
31:0	WDATA or RDATA	Write or Read data
32	Parity	Single bit parity of 32 data bits

Figure 51-2 shows a successful SWD write transfer.

Figure 51-2 SWD successful write transfer

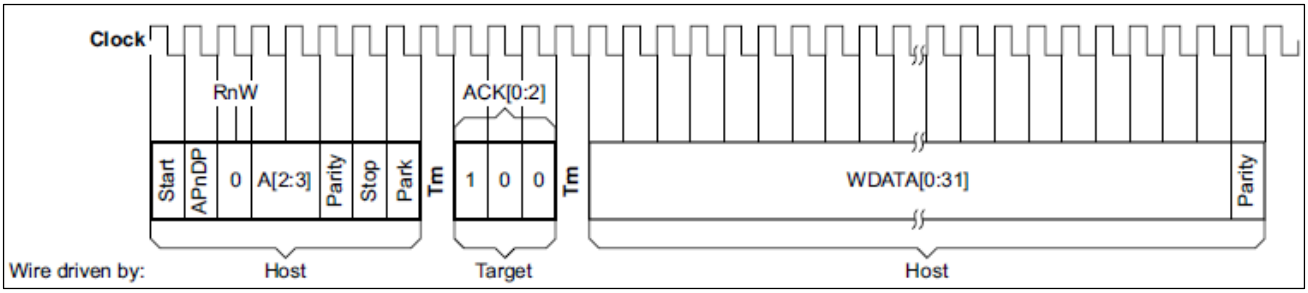
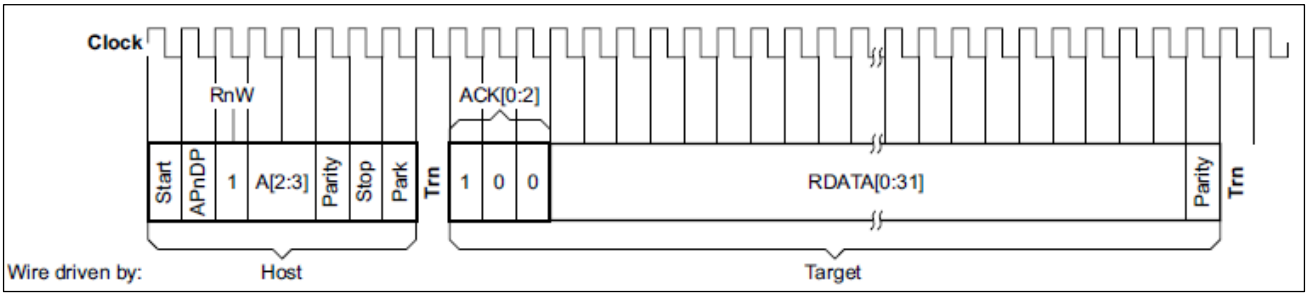


Figure 51-3 shows a successful SWD read transfer.

Figure 51-3 SWD successful read transfer



The data transfer phase is discarded if FAULT or WAIT ACK response is sent out from the target, except when overrun detection is enabled, the data will be ignored by the target (in the case of a write), or not driven (in the case of a read).

If the direction of the data is reversed between each phase, a single clock cycle turn-around time is inserted.

A line reset comprises of over 50 SWDIO high cycles, followed by two low cycles. The line reset must be transferred

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by the host when it is first connected, or a protocol error is detected.

For more details on the Serial Wire debug protocol, refer to the Arm® Debug Interface Architecture Specification.

JTAG debug port

The JTAG-DP contains a debug port state machine that controls the JTAG-DP mode operation, including controlling the scan chain interface that provides the external physical interface to the JTAG-DP. It is based closely on the JTAG.

When operating as a JTAG-DP, the Debug Port operates as defined in the Arm® Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2. The specification also contains an explanation of its programmers model, capabilities, and features.

The JTAG-DP IEEE 1149.1 compliant scan chains are used to read or write register information. A pair of scan chain registers accesses the main control and access registers within the Debug Port.

The scan chain registers are:

- DPACC, for DP accesses.
- APACC, for AP accesses.

An APACC access might access a register of a debug component of the system to which the interface is connected.

The scan chain model implemented by a JTAG-DP has the concepts of capturing the current value of APACC or DPACC, and of updating APACC or DPACC with a new value. An update might cause a read or write access to a DAP register that might then cause a read or write access to a debug register of a connected debug component. For information on the operations available on JTAGDP, see the Arm® Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2.

Debug port registers

The SW-DP and JTAG-DP both can access the debug port (DP) registers.

DP registers are described in more detail in the Arm® Debug Interface Architecture Specification.

51.3.3.2 Access port functional description

The access ports (AP) attached to the DP as the following:

- AP0: Cortex-M7 access port (AHB-AP).

  Allows access to the debug and trace features integrated in the Cortex-M7 processor core via an AHB-Lite bus connected to the AHBD port of the processor.

- AP1: System Debug Access port (AHB-AP).

  Allow access to the DBGMCU unit to control dual core debug modes.

- AP2: Cortex-M4 access port (AHB-AP).

  Allows access to the debug and trace features integrated in the Cortex-M4 processor core via its internal AHB bus.

All access ports are of MEM-AP types. The AP is seen by debuggers as a set of 32-bit registers. Some are used for configuration or monitoring whereas others are to perform the transaction itself.

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AP register access:

- Select the AP to be accessed by writing the APSEL field in the SELECT register

  APSEL is decoded as follows:

  - 0: to access AP0 (ARM Cortex-M7)
  - 1: to access AP1 (DBGMCU)
  - 2: to access AP2 (ARM Cortex-M4)
  - others: reserved
- Write the A[3:2] field in the APACC register to choose which registers to be accessed
- Write RnW field to choose write or read operation
- Write data into the DATA field in case of a write for JTAG. SWD data is transferred in the data phase.

Accessing memory-mapped debug component registers

- Write the address in the TAR register
- Write the CSW register, if needed, with the transfer parameters such as auto address increment
- Write to or read from DRW register to initiate a debug access at the address written in the TAR register. In addition, a read or write to banked data register BDn can also create an access to address TAR[31:4] + n.

For more detailed information on the MEM-AP, refer to the Arm® Debug Interface Architecture Specification.

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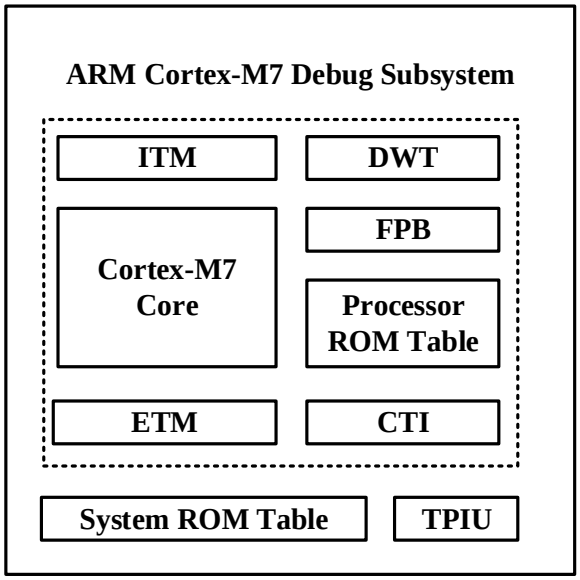
51.3.4 Cortex-M7 debug functional description

The Cortex-M7 subsystem features the following CoreSight™ components as shown in Figure 51-4:

- ROM tables: System ROM table, Processor ROM table and internal PPB ROM Table
- System control space (SCS)
- Breakpoint unit (FPB)
- Data watchpoint and trace unit (DWT)
- Instrumentation trace macrocell (ITM)
- Embedded trace macrocell (ETM)
- Cross trigger interface (CTI)

These components are accessible by the debugger via the Cortex-M7 AHB-AP0 and its associated AHBD bus.

Figure 51-4 ARM Cortex-M7 Debug Subsystem



Refer to ARM Cortex M7 Processor Technical Reference Manual for more details on ROM Table structure and address mapping of all the debug components in the Cortex-M7 debug subsystem.

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51.3.5 Cortex-M4 debug functional description

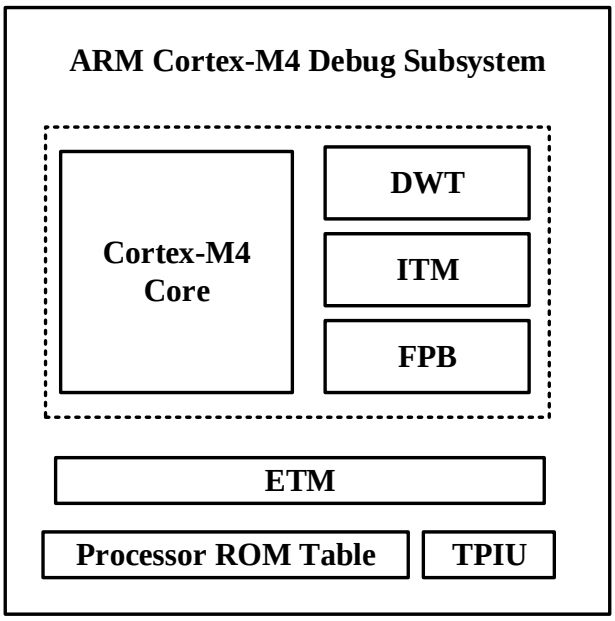
The Cortex-M4 subsystem features the following CoreSight™ components:

- Cortex-M4 ROM table
- Cortex-M4 system control space (SCS)
- Breakpoint unit (FPB)
- Data watchpoint and trace unit (DWT)
- Instrumentation trace macrocell (ITM)
- Embedded trace macrocell (ETM)

These components are accessible by the debugger via the Cortex-M4 AHB-AP2.

Refer to ARM Cortex M4 Processor Technical Reference Manual for more details on ROM Table structure and address mapping of all the debug components in the Cortex-M4 debug subsystem.

Figure 51-5 ARM Cortex-M4 Debug Subsystem



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51.3.6 DBG Functional Description

51.3.6.1 Debug support in different modes

The DBGMCU component contains a number of registers that control the power and clock behavior in Debug mode. Specifically it allows the debugger, or debug software, to:

- Maintain the clock and power to the processor cores when in low-power modes (sleep, stop0/stop2 or standby)
- Maintain the clock and power to the system debug and trace components when in low power modes
- Stop the clock to certain peripherals (I2C SMBUS timeout, WWDG, IWDG, Timers, RTC) when either the processor core is stopped in Debug mode. For timers having complementary outputs, these outputs are disabled (as if the MOE bit was reset) for safety purposes when the counter is stopped

processor core is stopped in Debug mode. For timers having complementary outputs, these outputs are disabled (as if the MOE bit was reset) for safety purposes when the counter is stopped

The DBGMCU registers are not reset by a system reset, only by a power on reset. They are accessible to the debugger via the AHB-AP1 at base address 0xE0043000. They are also accessible by both processor cores at base address 0x58035400.

Note: the DBGMCU is not a standard CoreSight component. Therefore, it does not appear in the system ROM table.

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51.4 Registers

51.4.1 ID Register (DBG_ID)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REV_NUM_H[3:0]				REV_NUM_L[3:0]				DEV_NUM_H[3:0]				DEV_NUM_M[3:0]			
r				r				r				r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_NUM_L[3:0]				PINS[3:0]				FLASH[1:0]		ENC[2:0]		Reserved			
r				r				r		r					

Bit field	Name	Description
31:28	REV_NUM_H[3:0]	High 4 bits of MCU version number
27:24	REV_NUM_L[3:0]	Low 4 bits of MCU version number
23:20	DEV_NUM_H[3:0]	Lower 4 digits of device model. Device model consists of 12 bits, including high, medium and low, representing the model of MCU. The values are as follows: 0x760: N32H760 Series 0x762: N32H762 Series 0x765:N32H765 Series 0x785:N32H785 Series 0x787:N32H787 Series 0x788:N32H788 Series Others: invalid
19:16	DEV_NUM_M[3:0]	See the description of DEV_NUM_H[3:0].
15:12	DEV_NUM_L[3:0]	See the description of DEV_NUM_H[3:0].
11:8	PINS[3:0]	The number of pins consists of 4 bits. 0x2: 100 pins 0x4: 144 pins 0x6: 169 pins 0x8: 176 pins 0xA: 208 pins 0xC: 240 pins
7:6	FLASH[1:0]	FLASH capacity. 01: SIP 2MB 10: SIP 4MB Other; Reserved

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Bit field	Name	Description
5:4	ENC[1:0]	Chip encapsulation format; 01: BGA encapsulation 10: LQFP encapsulation Other; Reserved
3:0	Reserved	Reserved, the reset value must be maintained.

51.4.2 Debug Control Register (DBG_CTRL)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TRACE_CFG	TRACE_MODE[1:0]		TRACE_IOEN	TRGOEN	M7 STBY	M7STOP	M7SLEEP	M4 STBY	M4STOP	M4SLEEP
					rw	rw		rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	TRACE_CFG	Trace Select 0: Trace from CM7 1: Trace from CM4
9:7	TRACE_MODE[1:0] and TRACE_IOEN	Trace pin assignment control – With TRACE_IOEN=0: TRACE_MODE=xx: TRACE pins not assigned (default state) – With TRACE_IOEN=1: TRACE_MODE = 00: TRACE pin assignment for Asynchronous Mode TRACE_MODE = 01: TRACE pin assignment for Synchronous Mode with a TRACEDATA size of 1 TRACE_MODE = 10: TRACE pin assignment for Synchronous Mode with a TRACEDATA size of 2 TRACE_MODE=11: TRACE pin assignment for Synchronous Mode with a TRACEDATA size of 4
6	TRGOEN	External trigger output enable 0: Input TRGIO is connected to TRGIN 1: Output TRGIO is connected to TRGOUT
5	M7STBY	CM7 in debug standby mode 0: Normal operation - CM7 powered down in standby mode 1: CM7 debug standby mode - Power and clocks are maintained for debug activities.

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Bit field	Name	Description
4	M7STOP	CM7 in debug stop mode 0: Normal operation - CM7 powered down in stop2 mode and clock is disabled in stop0 mode 1: CM7 debug stop mode - Power and clocks are maintained for debug activities.
3	M7SLEEP	CM7 in debug sleep mode 0: Normal operation - processor clock is stopped automatically in Sleep mode 1: Automatic clock stop disabled - processor clock continues to run, allowing full debug capability
2	M4STBY	CM4 in debug standby mode 0: Normal operation - CM4 powered down in standby mode 1: CM4 debug standby mode - Power and clocks are maintained for debug activities.
1	M4STOP	CM4 in debug stop mode 0: Normal operation - CM4 powered down in stop2 mode and clock is disabled in stop0 mode 1: CM4 debug stop mode - Power and clocks are maintained for debug activities.
0	M4SLEEP	CM4 in debug sleep mode 0: Normal operation - processor clock is stopped automatically in Sleep mode 1: Automatic clock stop disabled - processor clock continues to run, allowing full debug capability

51.4.3 Debug M7 APB1 Freeze Register (DBG_M7APB1FZ)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CANFD6_STOP	CANFD5_STOP	CANFD2_STOP
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CANFD1_STOP	WWDG2_STOP	I2C3_STOP	I2C2_STOP	I2C1_STOP	GTIMB3_STOP	GTIMB2_STOP	GTIMB1_STOP	GTIMA7_STOP	GTIMA6_STOP	GTIMA5_STOP	GTIMA4_STOP	BTIM4_STOP	BTIM3_STOP	BTIM2_STOP	BTIM1_STOP
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18:15	CANFDx_STOP	When the CM7 enters debug state, the debug CANFD stops (x= 6, 5, 2, 1) operating. It can be set to 1 or cleared by software. 0: The counter of the selected CANFD continues to operate normally. 1: The counter of the selected CANFD continues timer stops operating.
14	WWDG2_STOP	When the CM7 enters debug state, the debug window watchdog 2 stops operating. It can be set to 1 or cleared by software.

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Bit field	Name	Description
		0: The window watchdog 2 counter continues to operate normally. 1: The window watchdog 2 counter stops operating.
13:11	I2Cx_STOP	When the CM7 stops, the SMBus timeout mode stops (x= 3, 2, 1). It can be set to 1 or cleared by software. 0: Operates the same as normal mode. 1: Freezes the SMBus timeout control.
10:4	GTIMx_STOP	When the CM7 enters the debug state, the counter of the general purpose timer stops operating (x=10, 9, 8, 7, 6, 5, 4). It can be set to 1 or cleared by software. 0: The counter of the selected general purpose timer continues to operate normally. 1: The counter of the selected general purpose timer stops operating.
3:0	BTIMx_STOP	When the CM7 enters the debug state, the counter of the basic timer stops operating (x=4,3,2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected basic timer continues to operate normally. 1: The counter of the selected basic timer stops operating.

51.4.4 Debug M4 APB1 Freeze Register (DBG_M4APB1FZ)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													CANFD6_STOP	CANFD5_STOP	CANFD2_STOP
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CANFD1_STOP	WWDG2_STOP	I2C3_STOP	I2C2_STOP	I2C1_STOP	GTIMB3_STOP	GTIMB2_STOP	GTIMB1_STOP	GTIMA7_STOP	GTIMA6_STOP	GTIMA5_STOP	GTIMA4_STOP	BTIM4_STOP	BTIM3_STOP	BTIM2_STOP	BTIM1_STOP
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18:15	CANFDx_STOP	When the CM4 enters debug state, the debug CANFD stops (x= 6, 5, 2, 1) operating. It can be set to 1 or cleared by software. 0: The counter of the selected CANFD continues to operate normally. 1: The counter of the selected CANFD continues timer stops operating.
14	WWDG2_STOP	When the CM4 enters debug state, the debug window watchdog 2 stops operating. It can be set to 1 or cleared by software. 0: The window watchdog 2 counter continues to operate normally. 1: The window watchdog 2 counter stops operating.
13:11	I2Cx_STOP	When the CM4 stops, the SMBus timeout mode stops (x= 3, 2, 1). It can be set to 1 or cleared by software. 0: Operates the same as normal mode.

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Bit field	Name	Description
		1: Freezes the SMBus timeout control.
10:4	GTIMx_STOP	When the CM4 enters the debug state, the counter of the general purpose timer stops operating (x=B3, B2, B1, A7, A6, A5, A4). It can be set to 1 or cleared by software. 0: The counter of the selected general purpose timer continues to operate normally. 1: The counter of the selected general purpose timer stops operating.
3:0	BTIMx_STOP	When the CM4 enters the debug state, the counter of the basic timer stops operating (x=4,3,2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected basic timer continues to operate normally. 1: The counter of the selected basic timer stops operating.

51.4.5 Debug M7 APB2 Freeze Register (DBG_M7APB2FZ)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CANFD8_STOP	CANFD7_STOP	CANFD4_STOP	CANFD3_STOP	I2C6_STOP	I2C5_STOP	I2C4_STOP	ATIM2_STOP	ATIM1_STOP	GTIMA3_STOP	GTIMA2_STOP	GTIMA1_STOP	SHRTIM2_STOP	SHRTIM1_STOP
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:10	CANFDx_STOP	When the CM7 enters debug state, the debug CANFD stops (x= 8, 7, 4, 3) operating. It can be set to 1 or cleared by software. 0: The counter of the selected CANFD continues to operate normally. 1: The counter of the selected CANFD continues timer stops operating.
9:7	I2Cx_STOP	When the CM7 stops, the SMBus timeout mode stops (x= 6, 5, 4). It can be set to 1 or cleared by software. 0: Operates the same as normal mode. 1: Freezes the SMBus timeout control.
6:5	ATIMx_STOP	When the CM7 enters the debug state, the counter of the advanced timer stops operating (x= 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected advanced timer continues to operate normally. 1: The counter of the selected advanced timer stops operating.
4:2	GTIMAx_STOP	When the CM4 enters the debug state, the counter of the general purpose timer A stops operating (x=3, 2, 1). It can be set to 1 or cleared by software.

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Bit field	Name	Description
		0: The counter of the selected general purpose timer A continues to operate normally. 1: The counter of the selected general purpose timer A stops operating.
1:0	SHRTIMx_STOP	When the CM7 enters the debug state, the counter of high precision timer stops operating (x= 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected high precision timer continues to operate normally. 1: The counter of the selected high precision timer stops operating.

51.4.6 Debug M4 APB2 Freeze Register (DBG_M4APB2FZ)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CANFD8_STOP	CANFD7_STOP	CANFD4_STOP	CANFD3_STOP	I2C6_STOP	I2C5_STOP	I2C4_STOP	ATIM2_STOP	ATIM1_STOP	GTIMA3_STOP	GTIMA2_STOP	GTIMA1_STOP	SHRTIM2_STOP	SHRTIM1_STOP
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:10	CANFDx_STOP	When the CM4 enters debug state, the debug CANFD stops (x= 8, 7, 4, 3) operating. It can be set to 1 or cleared by software. 0: The counter of the selected CANFD continues to operate normally. 1: The counter of the selected CANFD continues timer stops operating.
9:7	I2Cx_STOP	When the CM4 stops, the SMBus timeout mode stops (x= 6, 5, 4). It can be set to 1 or cleared by software. 0: Operates the same as normal mode. 1: Freezes the SMBus timeout control.
6:5	ATIMx_STOP	When the CM4 enters the debug state, the counter of the advanced timer stops operating (x= 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected advanced timer continues to operate normally. 1: The counter of the selected advanced timer stops operating.
4:2	GTIMAx_STOP	When the CM4 enters the debug state, the counter of the general purpose timer A stops operating (x=3, 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected general purpose timer A continues to operate normally. 1: The counter of the selected general purpose timer A stops operating.
1:0	SHRTIMx_STOP	When the CM4 enters the debug state, the counter of high precision timer stops

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Bit field	Name	Description
		operating (x= 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected high precision timer continues to operate normally. 1: The counter of the selected high precision timer stops operating.

51.4.7 Debug M7 APB5 Freeze Register (DBG_M7APB5FZ)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		RTC_STOP	LPTIM5_STOP	LPTIM4_STOP	LPTIM3_STOP	LPTIM2_STOP	LPTIM1_STOP	IWDG2_STOP	IWDG1_STOP	I2C10_STOP	I2C9_STOP	I2C8_STOP	I2C7_STOP	ATIM4_STOP	ATIM3_STOP
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	RTC_STOP	When the CM7 enters debug state, the debug RTC stops operating. It can be set to 1 or cleared by software. 0: The RTC counter continues to operate normally. 1: The RTC counter continues timer stops operating.
12:8	LPTIMx_STOP	When the CM7 enters the debug state, the counter of the low power timer stops operating (x= 5, 4, 3, 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected low power timer continues to operate normally. 1: The counter of the selected low power timer stops operating.
7:6	IWDGx_STOP	When the CM7 enters debug state, the watchdog stops (x=2, 1) operating. It can be set to 1 or cleared by software. 0: The watchdog counter continues to operate normally. 1: The watchdog counter stops operating.
5:2	I2Cx_STOP	When the CM7 stops, the SMBus timeout mode stops (x= 10, 9, 8, 7). It can be set to 1 or cleared by software. 0: Operates the same as normal mode. 1: Freezes the SMBus timeout control.
1:0	ATIMx_STOP	When the CM7 enters the debug state, the counter of the advanced timer stops operating (x= 4, 3). It can be set to 1 or cleared by software. 0: The counter of the selected advanced timer continues to operate normally. 1: The counter of the selected advanced timer stops operating.

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51.4.8 Debug M4 APB5 Freeze Register (DBG_M4APB5FZ)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		RTC_STOP	LPTIM5_STOP	LPTIM4_STOP	LPTIM3_STOP	LPTIM2_STOP	LPTIM1_STOP	IWDG2_STOP	IWDG1_STOP	I2C10_STOP	I2C9_STOP	I2C8_STOP	I2C7_STOP	ATIM4_STOP	ATIM3_STOP
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	RTC_STOP	When the CM4 enters debug state, the debug RTC stops operating. It can be set to 1 or cleared by software. 0: The RTC counter continues to operate normally. 1: The RTC counter continues timer stops operating.
12:8	LPTIMx_STOP	When the CM4 enters the debug state, the counter of the low power timer stops operating (x= 5, 4, 3, 2, 1). It can be set to 1 or cleared by software. 0: The counter of the selected low power timer continues to operate normally. 1: The counter of the selected low power timer stops operating.
7:6	IWDGx_STOP	When the CM4 enters debug state, the watchdog stops (x=2, 1) operating. It can be set to 1 or cleared by software. 0: The watchdog counter continues to operate normally. 1: The watchdog counter stops operating.
5:2	I2Cx_STOP	When the CM4 stops, the SMBus timeout mode stops (x= 10, 9, 8, 7). It can be set to 1 or cleared by software. 0: Operates the same as normal mode. 1: Freezes the SMBus timeout control.
1:0	ATIMx_STOP	When the CM4 enters the debug state, the counter of the advanced timer stops operating (x= 4, 3). It can be set to 1 or cleared by software. 0: The counter of the selected advanced timer continues to operate normally. 1: The counter of the selected advanced timer stops operating.

51.4.9 Debug M7 APB6 Freeze Register (DBG_M7APB6FZ)

Address offset: 0x20

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Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															WWDG1_STOP
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	WWDG1_STOP	When the CM7 enters debug state, the debug window watchdog 1 stops operating. It can be set to 1 or cleared by software. 0: The window watchdog 1 counter continues to operate normally. 1: The window watchdog 1 counter stops operating.

51.4.10 Debug M4 APB6 Freeze Register (DBG_M4APB6FZ)

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw	rw	rw													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															WWDG1_STOP
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	WWDG1_STOP	When the CM4 enters debug state, the debug window watchdog 1 stops operating. It can be set to 1 or cleared by software. 0: The window watchdog 1 counter continues to operate normally. 1: The window watchdog 1 counter stops operating.

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52 Version history

Date	Version	Modify
2025.4.30	V1.0.0	1. Initial version
2025.6.27	V1.1.0	1. Add content to sections 47.3, 47.4, and 47.5 of the ETH module. 2. Modify N32H785xxxxEC in chapter ESC to N32H7x5EC. 3. Delete shadow register mode related function description in MDMA module. 4. Update PLL frequency range 5. Optimize LSE crystal mode configuration steps 6. Optimize SDRAM device's suspend and wakeup sequences 7. Modify "ETH2_MII_REF_CLK" to "ETH2_RMII_REF_CLK" in Table 12-79. 8. Modify Figure 2-2 9. Add chapter descriptions for the LCDC, DVP, XSPI, JPEG, and DSI modules. 10. Add notes on RTC frequency division in Section 25.2.4 11. Modify Table 18-16, Table 20-14 12. Modify the functional description of the CORDIC function in 31.4.1 13. Add Figure 36-2 and Figure 36-3 to Chapter 36 14. Delete the note of TIMx_CTRL1. ASYMMETRIC

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Email: sales@nsing.com.sg

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NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg