N32H785 Product Brief

The N32H785 series uses an ARM Cortex-M7 core, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. It features (2/4MB) on-chip FLASH, integrates up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM. It includes 3 12-bit 5Msps ADCs, 4 high-speed comparators, 6 12-bit DACs, and integrates multiple high-speed communication interfaces: U(S)ART, I2C, xSPI, SPI, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet.

The series supports digital camera interface (DVP), TFT-LCD graphical interface, JPEG hardware codec and GPU. It features a built-in high-performance encryption algorithm hardware acceleration engine, supporting AES/TDES, SHA、SM4 algorithms, TRNG true random number generator, and CRC8/16/32. It supports up to 126 GPIOs, and is available in LQFP176、BGA176+25 and BGA240+25 packages.

Key Features

- **Dual-core Architecture CPU (Cortex-M7 and Cortex-M4F)**
  - ARM Cortex-M7
    - 32-bit ARM Cortex-M7 core with a double-precision floating-point unit, supporting DSP instructions and MPU
    - Built-in 32 KB instruction Cache and 32 KB data Cache with ECC
    - Maximum operating frequency of 600 MHz, delivering 1284 DMIPS
  - ARM Cortex-M4F
    - 32-bit ARM Cortex-M4F core with FPU, featuring single-cycle hardware multiplication and division instructions, and supporting DSP instructions and MPU
    - Built-in 16 KB instruction Cache and 16 KB data Cache with parity check, supporting zero-wait execution of programs via the Flash accelerator unit
    - Maximum operating frequency of 300 MHz, delivering 375 DMIPS
- **Encrypted Memory**
  - On-chip Flash (2/4MB), supports encrypted storage and automatic program decryption during execution
  - 1504KB built-in SRAM, supports ECC verification
    - 1024KB TCM SRAM, configurable as D-TCM, I-TCM or SRAM
    - 480KB on-chip SRAM
  - 4KB Backup SRAM, supports ECC
- **Operating Modes**
  - Run mode
  - SLEEP mode: AXI enabled, AHB enabled
  - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled

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- Stop2 mode: Flash standby mode, SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled, I/O maintained
- Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled, SRAM, TCM disabled
- VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled

- **Clock**
  - 4MHz~48MHz external high-speed crystal
  - 4MHz~50MHz external clock input
  - 32.768KHz external low-speed crystal
  - Built-in 3 high-speed PLLs
  - Built-in MSI clock, supporting configuration of 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz clocks
  - Internal high-speed RC 64MHz
  - Internal low-speed RC 32KHz
- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset and software system reset
  - Supports programmable voltage detection
- **High-Speed Communication Interfaces**
  - 8 USART interfaces/7 UART interfaces, supporting ISO7816, IrDA, LIN
  - 2 LPUART interfaces
  - 7 SPI interfaces, supporting master/slave modes, rates up to 50 MHz
  - 10 I2C interfaces, rates up to 3.4 MHz, configurable master/slave modes, dual address response in slave mode
  - 2 USBHS Dual Role interfaces
  - 8 CAN-FD bus interfaces
  - 2 Ethernet MAC interface, ETH1 supports 10M/100M/1000M communication rates, ETH2 supports 10M/100M communication rates . Supports IEEE 1588 time synchronization protocol
- High-Performance Analog Interfaces
  - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling up to 16-bit, supporting single-ended and differential modes
  - 4 high-speed analog comparators
  - 6 12-bit DACs, of which 2 1Msps DACs support output with or without Buffer separately, internal output only supports mode without Buffer; simultaneous internal and external output must enable Buffer; the other 2 DACs only support 1 output channel to the internal chip, with 15Msps sampling rate, supporting internal output without Buffer
  - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64 or PLL clock division
  - Supports 1 reference voltage VREFBUF (configurable as 1.5V/1.8V/2.048V/2.5V)
  - 1 temperature sensor

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- **Audio Interfaces**
  - 4 I2S, supporting master/slave modes, audio sampling frequencies from 8KHz to 192KHz
  - 8 PDM digital microphone interfaces built into DSMU
- **Memory Extension Interfaces**
  - 1 FEMC (Flexible External Memory Controller) interface, bus rate 100 MHz, SRAM/PSRAM/Nor Flash supporting configurable 16/32-bit data width, NAND Flash supporting configurable 8/16-bit data width
  - 1 xSPI interface, supporting 1/2/4/8-bit data width, configurable master/slave, rates up to 133 MHz, can be used for external SRAM, PSRAM and Flash, supports XIP
  - 1 SDRAM interface, rates up to 133 MHz
  - 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, rates up to 104MHz
- **Image Processing Interfaces**
  - 2 digital camera interface (DVP), supporting 8/10/12/16bit, rates up to 110MHz
  - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD, providing all signal interfaces, can directly connect to various LCD and TFT panels, resolution up to 1920x1080
  - Built-in 2.5D graphics processor, supporting image scaling, rotation, blending, anti-aliasing, texture mapping, etc.
  - Hardware JPEG codec
- **Maximum support for 168 GPIOs, low-speed GPIOs support 5V tolerance (under VDD = 3.3V ±10% conditions)**
- **Motor control Cordic accelerator, supporting trigonometric and hyperbolic function acceleration, supporting floating-point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filtering algorithm accelerator FMAC, supporting FIR, IIR filtering**
- **3 high-speed DMA controllers, each controller supporting 8 channels, 1 MDMA supporting 16 channels, freely configurable channel source and destination addresses**
- **RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, supporting internal and external clock calibration**
- **Timer Counters**
  - 2 16bit super high-resolution timer (SHRTIM1/ SHRTIM2). Supports maximum control precision of 100ps, Each super high-resolution timer counter consists of 1 master timer unit and 6 16-bit slave timer units. each timer unit has 2 independent channels. Supports 12 independent PWM outputs or 6 pairs of complementary PWM outputs.
  - 4 16-bit advanced timer counters(ATIM1~4), supporting input capture, complementary output, quadrature encoding input and other functions, highest control precision 3.3ns; each timer has 6 independent channels, of which 4 channels support 4 pairs of complementary PWM outputs

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- 10 16-bit general-purpose timers (GTIMA1~GTIMA7, GTIMB1~ GTIMB3), each timer with 4 independent channels, supporting input capture, output compare, PWM generation
- 4 32-bit basic timer counters (BTIM1~4)
- 5 16-bit low-power timers (LPTIM1~5), can work in Stop2 mode
- 2x 24-bit SysTick, 2x 14-bit window watchdog (WWDG), 2x 12-bit independent watchdog (IWDG)

- Programming Methods
  - Supports SWD/JTAG online debugging interface
  - Supports USB, USART Bootloader
- Security Features
  - FLASH has up to 4 encryption partitions, supporting storage encryption
  - Supports write protection (WRP), multiple levels of read protection (RDP) (L0/L1/L2)
  - Built-in password algorithm hardware acceleration engine, supporting AES/TDES, SHA, algorithms
  - TRNG true random number generator, CRC8/16/32 operations
  - Supports secure boot, encrypted program download, secure update, supports external high-speed and low-speed clock failure detection
  - Supports tamper detection
- **OTP supports 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range:
    - 2.3V~3.6V
    - Chip junction temperature range: -40°C~125°C
- **Security Features**
  - USB IF
  - IEC61508 SIL2
- **Security Features**
  - LQFP176(24mm x 24mm)
  - BGA176+25(10mm x 10mm)
  - BGA240+25(14mm x 14mm)
- **Ordering Models**

Series	Models
N32H785xxx7	N32H785IKL7, N32H785IIL7, N32H785IKB7, N32H785IIB7, N32H785XKB7, N32H785XIB7

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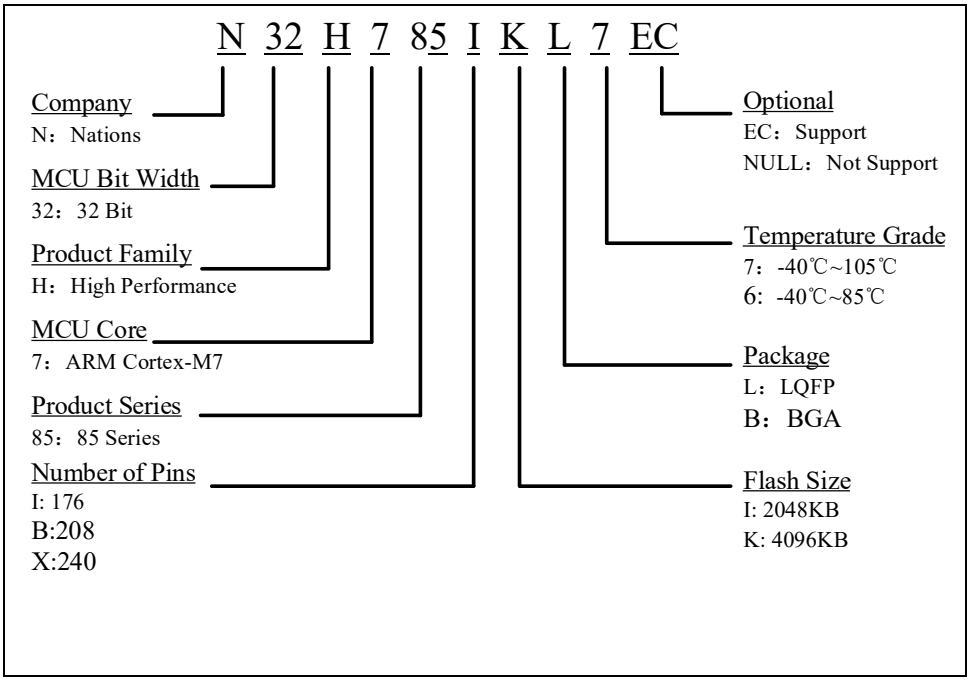
1 Naming Convention



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2 Device Overview

Table 2-1 N32H785 Series Resource Configuration

Device Model		N32H785IKL7	N32H785IIL7	N32H785IKB7	N32H785IIB7	N32H785XKB7	N32H785XIB7
Flash（KB）		4096	2048	4096	2048	4096	2048
SRAM（KB）	TCM	1024(1)					
	System RAM	480					
	Backup RAM	4					
Core	M7	600MHz					
	M4	300MHz					
Operating Voltage		2.3V~3.6V					
DCDC（step-down）		Yes					
Co-processor	Cordic	Yes					
	DSMU	Yes					
	FMAC	Yes					
Timers	SHRTIM	2					
	ADTIM	3(2)				4	
	GPTIM	10					
	BSTIM	4					
	LPTIM	5					
	SysTick timer	2					
	WWDG	2*14bit					
	IWDG	2*12bit					
	RTC	Yes					
Communication Interfaces	SPI/I2S	6/4(3)				7/4	
	I2C	8(4)				10	
	USART	7(5)				8	
	UART	6(6)				7	
	LPUART	2					
	USBHS Dual Role	2					
	CAN FD	8(7)					
	10/100M ETH	2(8)					
	10/100/1000M ETH	1(8)					
Extended memory	SDRAM	Yes					
	xSPI	1(9)					
	FEMC	Yes					
	SDMMC	2					
Analog	12bit ADC Number of channels	3 28		3 36		3 43	
	12bit DAC Number of channels	2+4(10) 2 External channels					
	Comparators	4					

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	VREFBUF	Yes		
Imaging	LCDC	Yes		
	GPU	Yes		
	JPEG	Yes		
	DVP	2		
GPIO		121	126	168
DMA Number of channels		3 24Channel		
MDMA Number of channels		1 16Channel		
Algorithm support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32		
Security Protection		Read/write protection (RDP/WRP), storage encryption, secure boot		
Packages		LQFP176 (24mm x 24mm)	BGA176+25 (10mm x 10mm)	BGA240+25 (14mm x 14mm)

Note：

1. SRAM is the default memory upon power-on, and users can independently configure the size allocation of ITCM, DTCM and SRAM.
2. ATIM interfaces: ATIM1~3
3. SPI interfaces: SPI1~6; I2S interfaces: I2S1~4
4. I2C interfaces: I2C1~8
5. USART interfaces: USART1~7
6. UART interfaces: UART9~14
7. FDCAN interfaces: FDCAN1~8
8. ETH1 supports 10M/100M/1000M; ETH2 supports 10M/100M
9. xSPI interface: xSPI2
10. The 4 DACs only support internal connection and cannot output to GPIOs.

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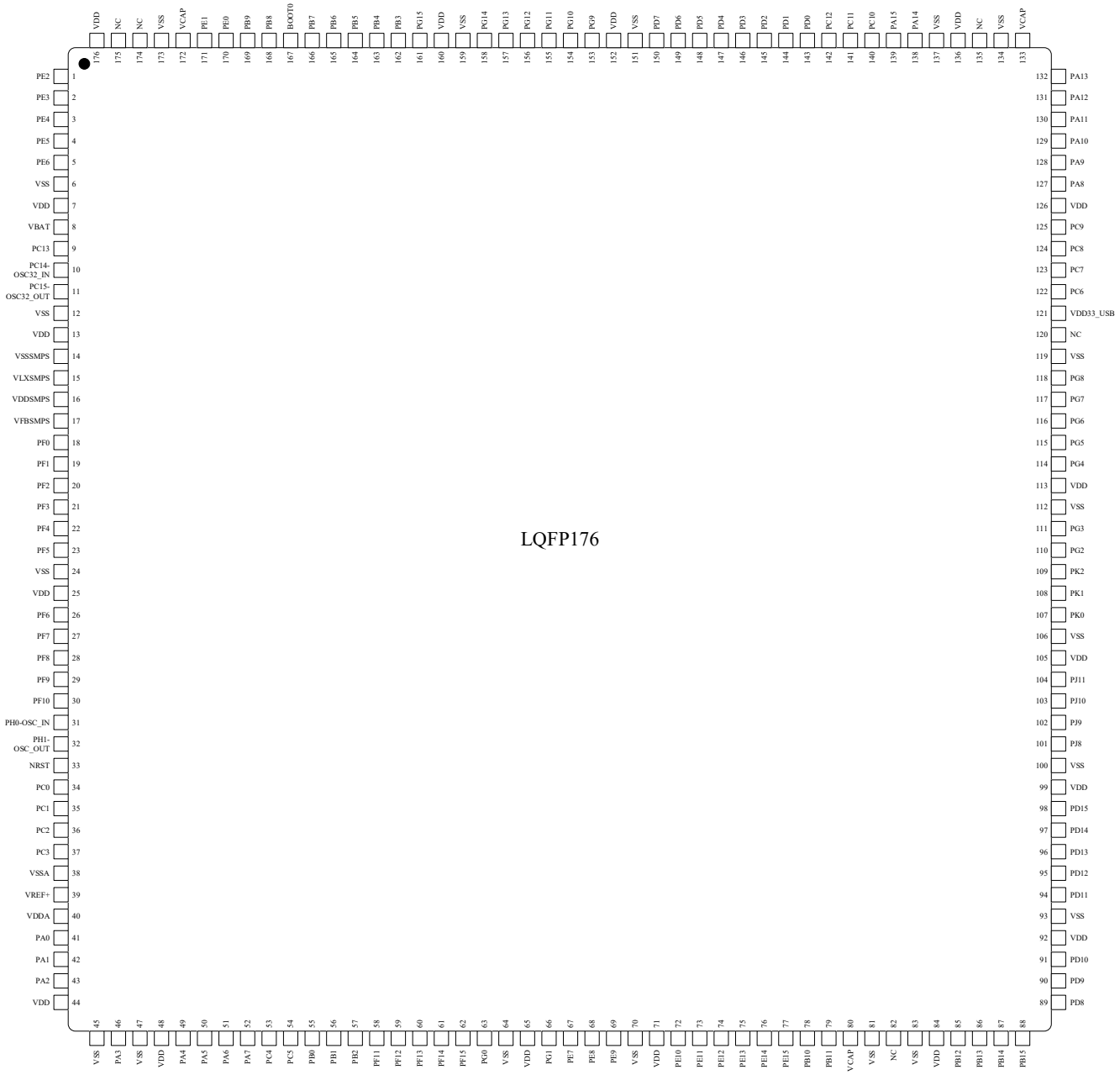
3 Package Information

3.1 LQFP176 Package

3.1.1 LQFP176 Pin Distribution



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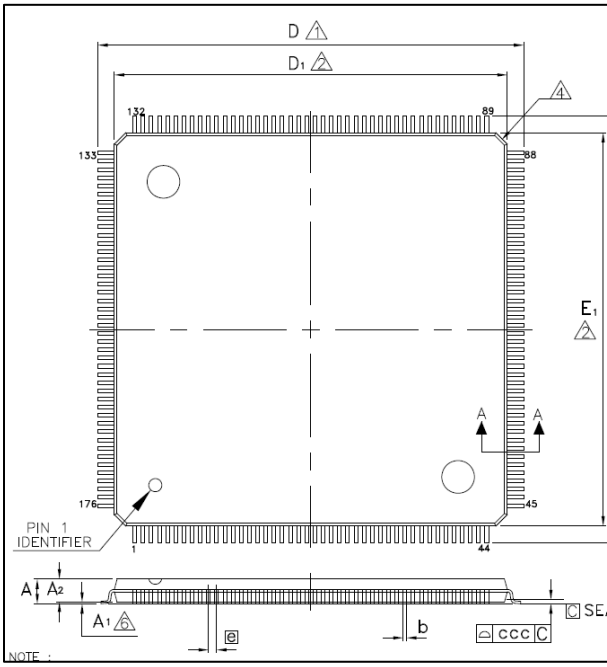
3.1.2 LQFP176 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.025	—	0.127	0.001	—	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

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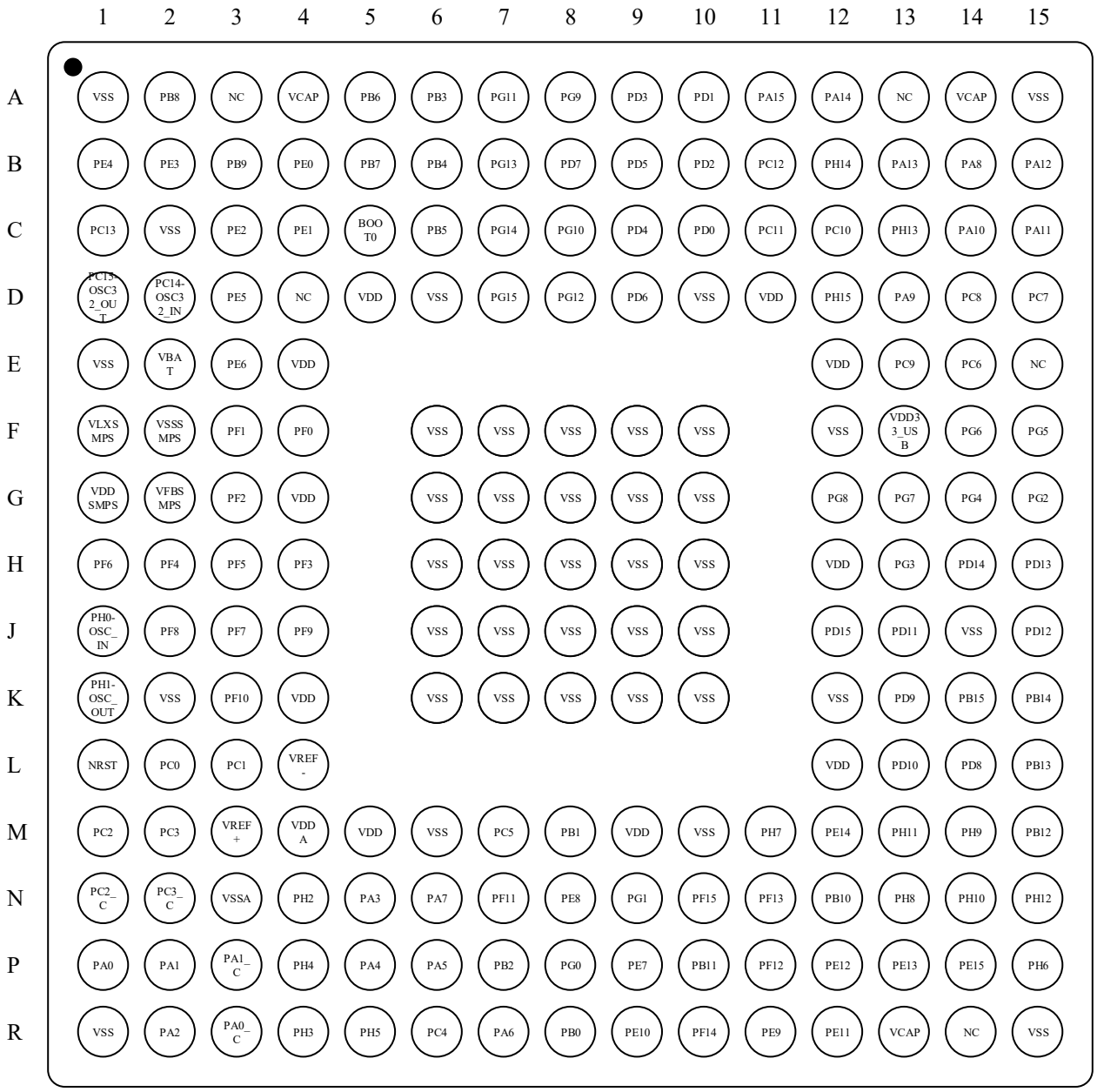
3.2 BGA176+25 Package

3.2.1 BGA176+25 Pin Distribution



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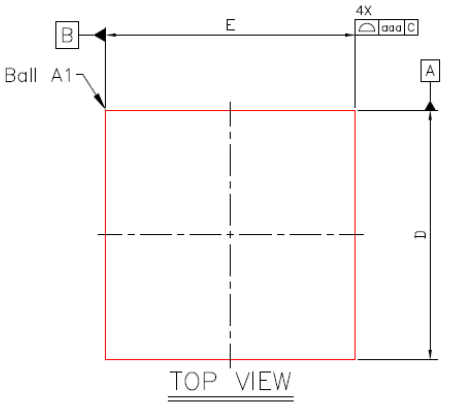
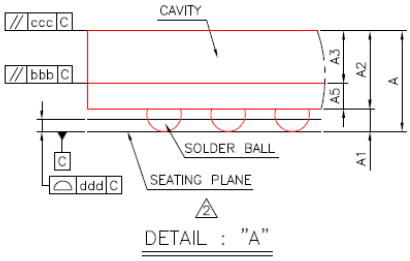
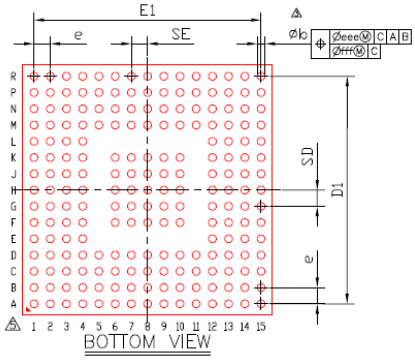
3.2.2 BGA176+25 Package Size





Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0,919	1.000	1.081	0,036	0,039	0,043
A1	0,160	0,210	0,260	0,006	0,008	0,010
A2	0.726	0,790	0,854	0,029	0,031	0,034
A3	0,480	0,530	0,580	0,019	0,021	0,023
A5	0,220	0,260	0,300	0,009	0,010	0,012
E	9,900	10,000	10,100	0,390	0,394	0,398
D	9,900	10,000	10,100	0,390	0,394	0,398
E1	—	9,100	—	—	0,358	—
D1	—	9,100	—	—	0,358	—
e	—	0,650	—	—	0,026	—
b	0,260	0,310	0,360	0,010	0,012	0,014
aaa		0,150			0,006	
bbb		0.100			0,004	
ccc		0,100			0,004	
ddd		0,100			0,004	
eee		0.150			0,006	
fff		0,080			0,003	
MD/ME		15/15				
SE		0.650			0,026	
SD		0.650			0,026	



NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc & ddd (SPIL STANDARD).
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.300 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

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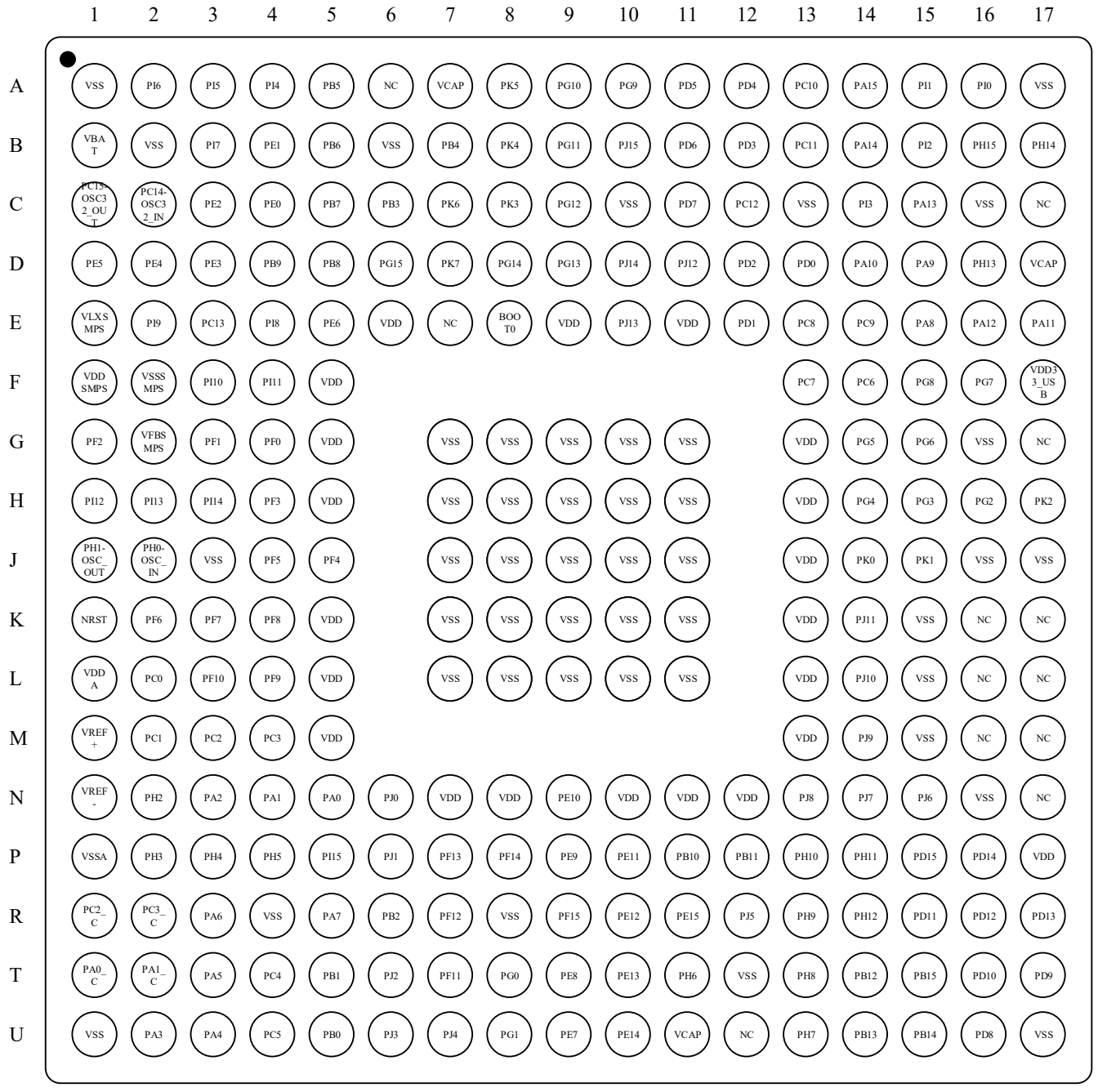
3.3 BGA240+25 Package

3.3.1 BGA240+25 Pin Distribution



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PI6	PI5	PI4	PB5	NC	VCAP	PK5	PG10	PG9	PD5	PD4	PC10	PA15	PI1	PI0	VSS
B	VBAT	VSS	PI7	PE1	PB6	VSS	PB4	PK4	PG11	PJ15	PD6	PD3	PC11	PA14	PI2	PH15	PH14
C	PC13-OSC32_OUT	PC14-OSC32_IN	PE2	PE0	PB7	PB3	PK6	PK3	PG12	VSS	PD7	PC12	VSS	PI3	PA13	VSS	NC
D	PE5	PE4	PE3	PB9	PB8	PG15	PK7	PG14	PG13	PJ14	PJ12	PD2	PD0	PA10	PA9	PH13	VCAP
E	VLXSMPS	PI9	PC13	PI8	PE6	VDD	NC	BOOT0	VDD	PJ13	VDD	PD1	PC8	PC9	PA8	PA12	PA11
F	VDDSMPS	VSSSMPS	PI10	PI11	VDD								PC7	PC6	PG8	PG7	VDD33_USB
G	PF2	VFBSMPS	PF1	PF0	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG5	PG6	VSS	NC
H	PI12	PI13	PI14	PF3	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG4	PG3	PG2	PK2
J	PH1-OSC_OUT	PH0-OSC_IN	VSS	PF5	PF4		VSS	VSS	VSS	VSS	VSS		VDD	PK0	PK1	VSS	VSS
K	NRST	PF6	PF7	PF8	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ11	VSS	NC	NC
L	VDDA	PC0	PF10	PF9	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ10	VSS	NC	NC
M	VREF+	PC1	PC2	PC3	VDD								VDD	PJ9	VSS	NC	NC
N	VREF-	PH2	PA2	PA1	PA0	PJ0	VDD	VDD	PE10	VDD	VDD	VDD	PJ8	PJ7	PJ6	VSS	NC
P	VSSA	PH3	PH4	PH5	PI15	PJ1	PF13	PF14	PE9	PE11	PB10	PB11	PH10	PH11	PD15	PD14	VDD
R	PC2_C	PC3_C	PA6	VSS	PA7	PB2	PF12	VSS	PF15	PE12	PE15	PJ5	PH9	PH12	PD11	PD12	PD13
T	PA0_C	PA1_C	PA5	PC4	PB1	PJ2	PF11	PG0	PE8	PE13	PH6	VSS	PH8	PB12	PB15	PD10	PD9
U	VSS	PA3	PA4	PC5	PB0	PJ3	PJ4	PG1	PE7	PE14	VCAP	NC	PH7	PB13	PB14	PD8	VSS

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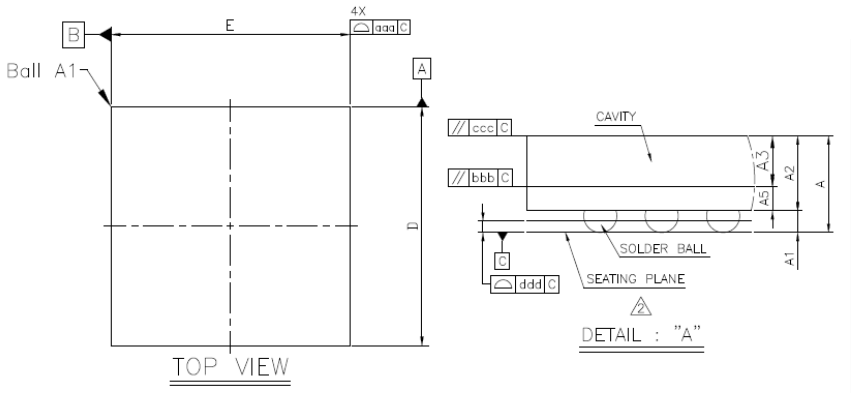
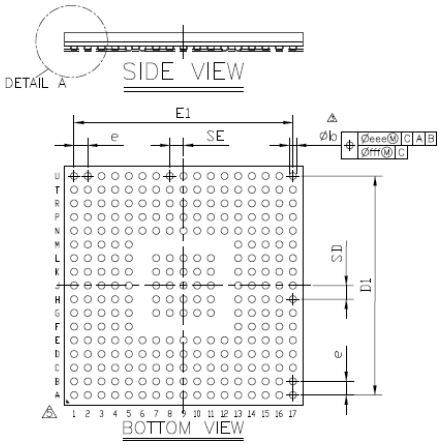
3.3.2 BGA240+25 Package Size



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.009	1.090	1.171	0.040	0.043	0.046
A1	0.250	0.300	0.350	0.010	0.012	0.014
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0.480	0.530	0.580	0.019	0.021	0.023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	13.900	14.000	14.100	0.547	0.551	0.555
D	13.900	14.000	14.100	0.547	0.551	0.555
E1	---	12.800	---	---	0.504	---
D1	---	12.800	---	---	0.504	---
e	---	0.800	---	---	0.031	---
b	0.360	0.410	0.460	0.014	0.016	0.018
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.130			0.005	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME	17/17					
SE		0.800			0.031	
SD		0.800			0.031	



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4 Version History

Version	Date	Changes
V1.1.0	2025.10.17	First release

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Email: sales@nsing.com.sg

5 Notice

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NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg