N32H7xx Series Errata Sheet

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Errata List

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Errata List

Errata link		Chip Version
		Version A
GPIO and AFIO	No digital filter function when reading GPIO I/J/K registers	●
Cache	The Issue with CM4 cache	●
PWR	The issue with System STOP2 mode	●
BKP SRAM	The issue with BKP SRAM erasure	●
U(S)ART	The issue of inability to send data properly in 485+DMA mode	●
I2C	The issue of the I2C_STSINT.TFC flag not being cleared timely	●
TIM	The issue of switching from others mode to 0% duty cycle PWM mode	●
	Abnormal counting issue of GTIMA in pulse-level encoding mode 1	●
DEUG	The I2C issue in DEBUG mode	●
	The LPTIM issue in DEBUG mode	●
	The issue of Switching from DEBUG SLEEP Mode to Normal SLEEP/STOP/STANDBY Mode	●
SEMA4	The issue of Dual-core concurrent access to SEMA4	●
TCM	The issue of TCM size configuration not being retained after power-off	●

●: The issue exists

-: The issue does not exist

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1 GPIO and AFIO

1.1 No digital filter function when reading GPIO I/J/K registers

Description

GPIO I/J/K ports do not support the digital filtering function when reading registers. The digital filtering function works normally when these ports are configured for other alternate functions.

Solution

None

2 Cache

2.1 The issue with CM4 cache

Description

Enabling the Cache during CM4 code execution will cause an exception.

Solution

None

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3 PWR

3.1 The issue with System STOP2 mode

Description

The Retention registers may behave abnormally after the chip wakes up from system STOP2 mode

Workaround

It is not recommended to use the system STOP2 mode.

4 BKP SRAM

4.1 The issue with BKP SRAM erasure

Description

When ECC check is enabled for BKP SRAM, an RTC tamper event may result in a failure to clear the word that is currently being written.

Workaround

None.

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5 U(S)ART

5.1 The issue of inability to send data properly in 485+DMA mode

Description

Data loss occurs when using USART in 485+DMA mode for transmission.

Workaround

Configure USART_CTRL1.DEDT as 0, and read the USART_STS register before setting USART_CTRL1.UEN to 1. If DMA is enabled again, the USART_STS register needs to be read before enabling DMA.

Note: If you want to use the 485+non-DMA function, when DEDT is not 0, the TXDE interrupt is not available. You need to determine data transmission completion by checking the TXC transmission complete flag, write data after checking TXC=1. When DEDT is 0, the TXDE interrupt can be used.

6 I2C

6.1 The issue of the I2C_STSINT.TFC flag not being cleared timely

Description

Setting I2C_CTRL2.START to 1 cannot clear the TFC flag immediately. The flag will only be cleared once a START condition is issued on the bus. During this period, the interrupt will be triggered repeatedly.

Workaround

Clear the TFC flag by setting I2C_CTRL2.STOP to 1. If communication needs to be continued, reconfigure I2C_CTRL2.START to 1.

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7 TIM

7.1 The issue of switching from others mode to 0% duty cycle PWM mode

Description

When switching from any mode to PWM1/2 mode on all ATIM/GTIMA/GTIMB, if the PWM duty cycle is set to 0%, the mode transition to PWM mode fails.

Workaround

When switching from forced active/forced inactive/ set channel x to the active level on match./ set channel x as inactive level on match modes to PWM1/2 mode with a 0% duty cycle, modify CCxP to achieve the desired 0% duty cycle.

For frozen/toggle/combined PWM Mode 1/combined PWM Mode 2/retriggerable single pulse mode 1/retriggerable single pulse mode 2 switching to PWM1/2 mode with a 0% duty cycle results in abnormal behavior, and no solution is currently available.

7.2 Abnormal counting issue of GTIMA in pulse-level encoding mode 1

Description

When GTIMA operates in Pulse-level Encoding Mode 1, the generation of a valid TRGO signal (the default signal is ITR0) on this timer will reset the timer's CNT count value.

Workaround

When GTIMA is used in Pulse-level Encoding Mode 1, configure the TRGO trigger source of this timer to an unused and invalid signal.

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8 DEBUG

8.1 The I2C issue in DEBUG mode

Description

In Debug mode, if the I2C timeout function is enabled and DBG_MxAPBxFZ.I2Cx_STOP is activated, the timeout counter will be cleared to 0 when the code stops running (the core is halted).

Workaround

None

8.2 The LPTIM issue in DEBUG mode

Description

In Debug mode, when the LPTIM operates in external clock mode and DBG_MxAPB5FZ.LPTIMx_STOP is enabled, the LPTIM counter will not stop even if the code ceases to run (the core is halted).

Workaround

None

8.3 The issue of switching from DEBUG SLEEP mode to normal SLEEP/STOP/STANDBY mode

Description

When the chip enters DEBUG SLEEP mode and then switches to normal SLEEP/STOP/STANDBY mode, the system will erroneously enter DEBUG SLEEP/STOP/STANDBY mode.

Workaround

Perform a power cycle before switching the system from DEBUG SLEEP mode to normal SLEEP/STOP/STANDBY mode.

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9 SEMA4

9.1 The issue of Dual-core concurrent access to SEMA4

Description

Concurrent access to SEMA4 by both cores may cause errors in the ProcessID and CoreID of SEMA4

Workaround

Replace it with DCMU.

10 TCM

10.1 The issue of TCM size configuration not being retained after power-off

Description

After the TCM size configuration is completed. The previous configuration will be lost when the chip is powered off.

Workaround

When the chip is powered on for the first time, perform a system reset actively after configuring the TCM size.

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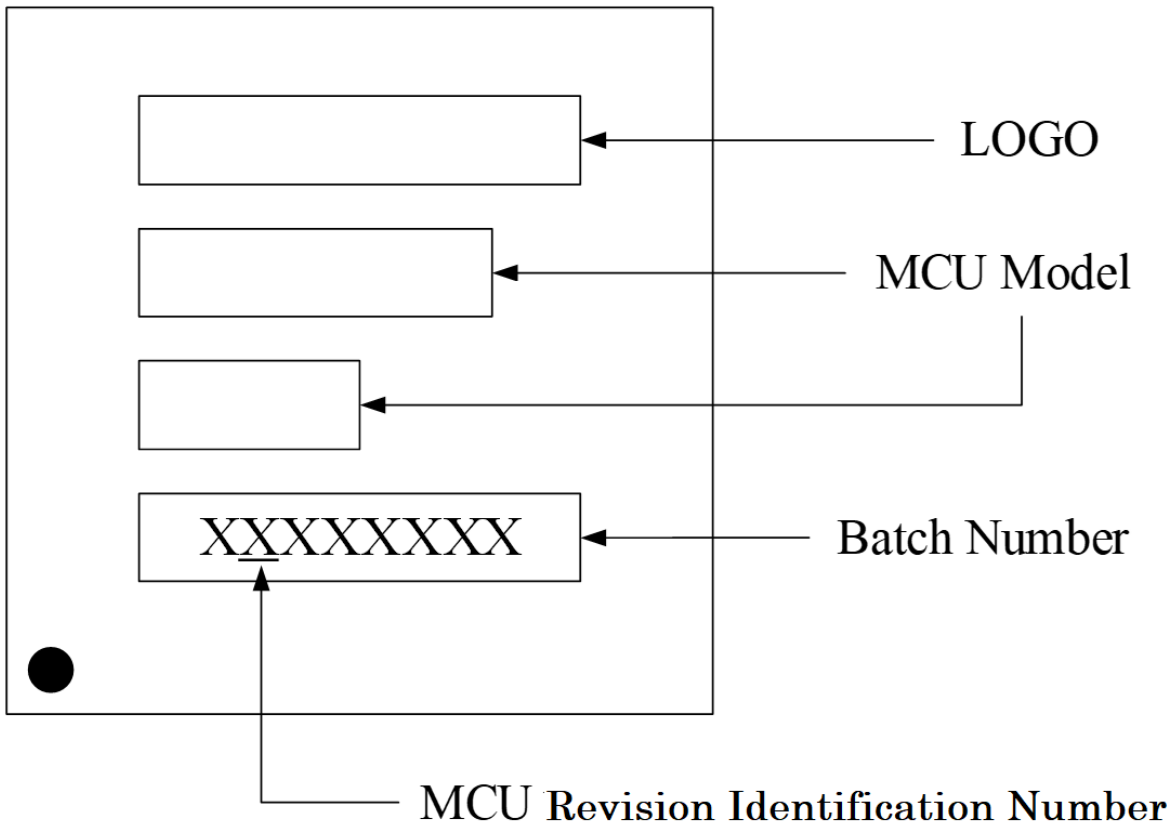
11 Chip Screen Printing and Version Description



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12 Version History

Version	Date	Changes
V1.2.0	2025.10.24	Initial release

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