N32H7xx series DSMU user guide

Introduction

This document is designed for users to quickly understand the basic functions and usage of the DSMU peripherals in N32H7xx series microcontrollers (MCUs), in order to guide users to easily use this product.

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Content

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1 Overview

The DSMU module is designed to interface with external ΣΔ modulators. It supports up to 8 external digital serial interfaces (channels) and includes up to 4 digital filters. Additionally, the DSMU can optionally accept parallel data stream input from internal ADC peripherals or device memory.

This document introduces the basic usage of the DSMU module in the N32H7xx series microcontrollers (MCUs). For detailed such as function descriptions, parameters, precautions, etc., please refer to the EN_UM_N32H7xx Series User Manual.

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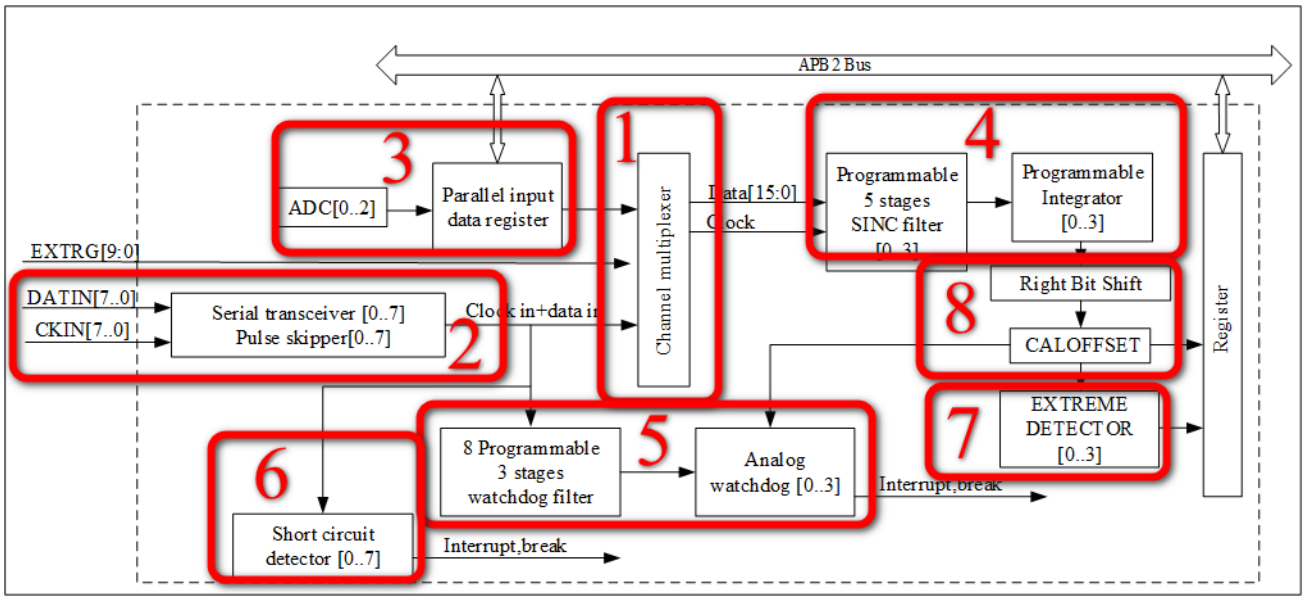
2 Introduction of DSMU

2.1 Brief introduction

DSMU stands for Delta Sigma Module Unit. It is primarily used to connect external Sigma-Delta ADC devices through a Sinc filter, performs a "moving average" calculation on the input serial data samples to obtain the desired filtered data. It also supports filtering of internal parallel data within the MCU (internal ADC conversion results, input data registers) and supports DMA.

2.2 DSMU Functional Block Diagram

The DSMU module structure diagram is shown below, and it can be roughly divided into 8 parts:



The functions of each component are as follows:

1) Channel Multiplexer:

   Supports 8 input channels, each channel can be independently configured as an external (serial) or internal (parallel) channel.

2) Serial Transceiver:

   External serial data interface, converting serial data to parallel data.

3) Parallel Input Data Register:

   16-bit data input register, which can be directly written by CPU or DMA, or connected to the MCU's built-in ADC via fixed channels: ADC1 connected to channel 0, ADC2 connected to channel 1, and ADC3 connected to channel 2.

4) SINC Filter + Integrator:

   Supports 4 data filters (sinc filter + integrator), which can be independently configured to connect to any input channels.

5) Analog Watchdog:

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Supports 4 analog watchdogs, which can monitor the serial data input from the external channel or the final output results.

When used to monitor the external channel input, each channel provides an additional sinc filter just for analog watchdog.

6) Short Circuit Detector:

Supports 8 short circuit detectors, monitoring the 1-bit data stream input from the external serial channel.

7) Extreme detector:

Supports 4 extreme value detectors, which performs simple analysis on the final result, and record the minimum and maximum values.

8) Right Bit Shift + CALOFFSET:

Supports 4 data post-processing units (right shift + correction), configurable for each input channel. They right-shift the data(0~31 bits) after the integrator, then add a configurable offset, and output the final result.

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3 DSMU Initialization

DSMU initialization can be divided into channel initialization and data filter initialization, which are described below.

3.1 DSMU Channel Initialization

The DSMU supports 8 input channels, each can be independently configured as an external serial data channel or an internal parallel data channel.

When configured as an external serial channel for connecting external devices, it can be configured as an SPI or Manchester interface, supporting short-circuit detection, clock loss detection, and analog watchdog functionality. The hardware supports the following two connection methods:

- When the external device requires a clock from the DSMU (e.g., Digital microphone), the DSMU is connected via the CKOUT and DATINy pins.
- When the external device does not require a clock from the DSMU (e.g., Some Sigma-Delta ADC such as AD7402), it is connected via the CKINy and DATINy pins.

Each serial input channel can be independently configured, such as follows:

- Analog watchdog filter:
  When a serial input channel is connected to an analog watchdog, the input data is processed by the analog watchdog filter and then output to the watchdog. The oversampling rate and filter order are configurable.
- Short-circuit detection:
  When the number of consecutive '1' or '0' data detected by the serial data interface reaches a threshold (configurable), a short-circuit event is triggered. A braking signal can also be output.
  Short-circuit detection is not included in the initialization and requires separate configuration.
- Clock Missing Detection:
  The clock input pin CKINy is detected based on the CKOUT signal (the signal source must be configured as the system clock). A clock missing event is generated when no SPI interface clock level change is detected for more than 8 CKOUT cycles, or no Manchester interface signal level change is detected for more than 2 CKOUT cycles.
  Clock missing detection is not included in the initialization and requires separate configuration.
- Additionally, each channel can be independently configured with data post-processing parameters:
  Data post-processing (right shift + correction) is applied to the data after integrator. When an input channel (serial or parallel) is connected to the data filter, the filtered data is further right-shifted and corrected before the final result is output. The right shift bits and correction values are configured in the corresponding input channels.

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The following introduction based on the channel initialization structure "DSMU_Channel_InitType".

```
typedef struct
{
  DSMU_Channel_OutputClockType      OutputClock;
  DSMU_Channel_InputType            Input;
  DSMU_Channel_SerialInterfaceType  SerialInterface;
  DSMU_Channel_AwdType              Awd;
  int32_t                           Offset;
  uint32_t                          RightBitShift;
} DSMU_Channel_InitType;
```

3.1.1 Clock Output Configuration: OutputClock

```
typedef struct
{
  FunctionalState  Activation;
  uint32_t         Selection;
  uint32_t         Divider;
}DSMU_Channel_OutputClockType;
```

The description of each parameter shows as follows:

- Activation:

  Clock output enable control. Some external devices (such as digital microphones) require a clock from the DSMU and must be set to ENABLE.
- Selection: Output clock source is selectable:
  - System Clock: DSMU module clock, refer to the function RCC_ConfigDSMUKerClk.
  - Audio Clock: Used only for clock output, refer to the function RCC_ConfigDSMUKerAClk.
- Divider:

  Output clock division factor (1~255), configured to 0 when disabled.
- Output to external devices via the CKOUT pin.
- Clock output can only be configured in the DSMU_CH0CFG1 register of the first input channel, and is valid for all channels.

3.1.2 Input Signal Configuration: Input

```
typedef struct
{
  uint32_t  Multiplexer;
  uint32_t  DataPacking;
  uint32_t  Pins;
}DSMU_Channel_InputType;
```

The description of each parameter shows as follows:

- Multiplexer:

  Input signal source selection: external pin, built-in ADC, input data register.
- DataPacking:

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The data format of input data register DSMU_CHyDATIN.

- Standard:

  One current channel data, stored in the lower 16 bits INDATAT0, the upper 16 bits INDATAT1 are invalid.

- Interleaved:

  Two current channel data, stored sequentially in INDATAT0 and INDATAT1.

- Dual:

  One current channel data stored in INDATAT0, and one next channel data stored in INDATAT1.

➢ Pins:

External channel data source, current channel or next channel.

- When a clock from the DSMU is required, connect the external device's serial clock pin via the CKOUT pin; CKINx is unused.
- When a clock from the DSMU is not required, connect the external device's serial clock pin via the CKINx pin; CKOUT is unused.

3.1.3 External Serial Interface Configuration: SerialInterface

```
typedef struct
{
  uint32_t  Type;
  uint32_t  SpiClock;
} DSMU_Channel_SerialInterfaceType;
```

The description of each parameter shows as follows:

➢ Type:

External serial data interface and clock edge configuration.

- Interface: SPI or Manchester.
- Sampling clock edge: Rising edge or falling edge.

➢ SpiClock: SPI interface clock configuration.

- Sampling clock source: CKIN or CKOUT.
- CKOUT sampling clock edge: Rising/falling edge, or the second rising/falling edge of each 2 clocks.

3.1.4 Analog Watchdog Filter Configuration: Awd

```
typedef struct
{
  uint32_t  FilterOrder;
  uint32_t  Oversampling;
} DSMU_Channel_AwdType;
```

The description of each parameter shows as follows:

➢ FilterOrder:

The order of the analog watchdog filter, can be configured as FastSinc, $Sinc^1$, $Sinc^2$, or $Sinc^3$.

➢ Oversampling:

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The oversampling rate of the analog watchdog filter, can be configured from 1 to 32.

- The analog watchdog filter is configured independently for each input channel, and is effective when the current channel is connected to the analog watchdog.
  - There are only 4 analog watchdogs, each can be independently configured and connected to any input channel.
  - When an input channel is connected to a watchdog, the input data is processed by the current channel's watchdog filter, and then output to the watchdog.

3.1.5 Data Post-processing Configuration: Offset, RightBitShift

The description of each parameter shows as follows:

- RightBitShift:
  The number of bits to right shift the data output of the data filter, 0~31 bits.
- Offset:
  The data filter output data correction amount, a 24-bit signed integer.
- Data right shift and correction are configured independently for each input channel and apply to the data filter output.
- There are only 4 data filters, each can be independently configured to connect to any input channel.
- The filter output data is first right-shifted and then corrected, and output the final result.
- When an input channel is connected to a data filter, the filter's post-processing parameters are configured on the connected input channel.

3.2 DSMU Data Filter Initialization

The DSMU supports four data filters, each consisting of one SINC filter and one integrator. These can be independently configured and connected to any input channel. Specifically:

- The SINC filter calculation is equivalent to a moving average (oversampling rate is configurable), and multiple moving averages (filter order) can be performed.
- The integrator is equivalent to accumulating the SINC filter results (oversampling rate is configurable).

Data filters process data using regular conversion or injected conversion:

- When configured for regular conversion, each filter can only be connected to one input channel.
- When configured for injected conversion, each filter can be connected to multiple input channels.

After the data filters output data, right shift and correction processing is required, and the final result is output after that. The right shift and correction parameters are independently configured by the channel connected to the filter.

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The following introduction based on the filter initialization structure " DSMU_Filter_InitType ".

```
typedef struct
{
   DSMU_Filter_RegularParamType RegularParam;
   DSMU_Filter_InjectedParamType InjectedParam;
   DSMU_Filter_FilterParamType    FilterParam;
} DSMU_Filter_InitType;
```

3.2.1 Regular Conversion Configuration: RegularParam

```
typedef struct
{
   uint32_t           Trigger;
   FunctionalState    FastMode;
   FunctionalState    DmaMode;
} DSMU_Filter_RegularParamType;
```

The description of each parameter shows as follows:

- Trigger:

  Regular conversion trigger type, software-triggered or synchronous-triggered.

  Used only as a condition during initialization and not written to registers.

- FastMode:

  Data filter fast conversion mode, applicable only to regular conversion.

- DmaMode:

  DMA read control for regular conversion results.

3.2.2 Injected Conversion Configuration: InjectedParam

```
typedef struct
{
   uint32_t           Trigger;
   FunctionalState    ScanMode;
   FunctionalState    DmaMode;
   uint32_t           ExtTrigger;
} DSMU_Filter_InjectedParamType;
```

The description of each parameter shows as follows:

- Trigger:

  Injected conversion trigger type: software trigger, synchronous trigger, or external trigger.

  Used only as a condition during initialization and not written to registers.

- ScanMode:

  Data filter scan mode control; only applicable to injected conversions.

- DmaMode:

  DMA read control for injected conversion results.

- ExtTrigger:

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External trigger source selection.

3.2.3 Filter parameter configuration: FilterParam

```
typedef struct
{
   uint32_t          SincOrder;
   uint32_t          Oversampling;
   uint32_t          IntOversampling;
} DSMU_Filter_FilterParamType;
```

The description of each parameter shows as follows:

- SincOrder:

  The order of the SINC filter, can be configured as FastSinc, $Sinc^1$, $Sinc^2$, $Sinc^3$, $Sinc^4$, $Sinc^5$.

- Oversampling:

  The oversampling rate of the SINC filter, can be configured from 1 to 1024.

- IntOversampling:

  The oversampling rate of the integrator, can be configured from 1 to 256.

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4 Additional functions for DSMU data filters

4.1 Analog Watchdog

Each data filter provides an analog watchdog to monitor in real time whether the serial input data or the final conversion result exceeds a specified range.

Each watchdog has independently configurable high and low thresholds. Exceeding the high or low threshold will generate independent events, and a braking signal can be output.

- When the analog watchdog is used to monitor the input data, the serial data is processed by the analog watchdog filter and then output to the watchdog.
- When the analog watchdog is used to monitor the final result, the data output by the data filter is right-shifted and corrected, and then output to the watchdog.

4.2 Extreme Detection

Extreme value detector records the maximum and minimum values of the final result in current data filter, which may be extreme values of one or multiple channels. User can read the extreme value register (maximum or minimum value) at any time. After reading, the extreme value register is reset to its default value and statistics restart.

4.3 Short-circuit and Clock absence Detection

Short circuit and clock absence detection operates on the input serial channels, and can be configured independently for each input channel. However, the status flag can only be queried in the status register DSMU_FLT0STS of the first data filter.

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5 DSMU Regular and Injected Conversion

5.1 Regular Conversion work flow

Rule conversion is only applicable to a single input channel. The following steps can be followed:

1) Initialize the DSMU channel and data filter.
2) Configure the rule channel and operating mode, referring to the function DSMU_FilterConfigRegChannel. Two operating modes are supported:
   - Single-time mode: Only one conversion is performed per trigger.
   - Continuous mode: Continuous conversion after triggering.
3) Configure additional functions as needed: short-circuit detection, clock absence detection, analog watchdog, extreme detection.
4) Start rule conversion, referring to the function DSMU_RegConvStart. Two triggering methods are supported:
   - Software trigger
   - Synchronous trigger

5.2 Injected Conversion work Flow

Injection conversion is applicable to multiple channels (injection conversion group). The following steps can be followed:

1) Initialize the DSMU channel and data filter.
2) Configure the injection channel group, referring to the function DSMU_FilterConfigInjChannel.
3) Configure additional functions as needed: short circuit detection, clock absence detection, simulated watchdog timer, extreme detection.
4) Start injected conversion, refer to the function DSMU_InjConvStart, supporting 3 triggering methods:
   - Software trigger
   - Synchronous trigger
   - External trigger
5) Injected conversion supports 2 working modes, configured during initialization:
   - Single-shot mode: Only one channel is converted per trigger.
   - Scan mode: After triggering, all channels in the injection group are converted sequentially according to the channel number from low to high.

5.3 Triggering Type Description

DSMU data conversion supports 3 triggering methods:

- Software trigger:
  Triggering ragular or injected conversion by writing 1 to the corresponding control bit in the data filter register.
- Synchronous trigger:

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Only applicable to the 2nd, 3rd, and 4th data filters. When the 1st filter DSMU_FLT0 starts conversion, the current data filter starts conversion synchronously.

- External trigger:

  Triggered by an external event, only applicable to injected conversion.

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6 Events, Interrupts, and DMA

- The DSMU supports the following events, all of them can be configured to generate interrupts:
  - Clock Absence Event
  - Short Circuit Event
  - Analog Watchdog Event
  - Regular Conversion Overload Event
  - Injected Conversion Overload Event
  - Regular Conversion Complete Event
  - Injected Conversion Complete Event
- Some events can be configured to output a break signal, connected to the timers such as ATIM1~3, GTIM8~10, and SHRTIM. Please refer the user manual for details:
  - Short Circuit Event
  - Analog Watchdog Event
- The internal parallel channel (the input data register), can be written by DMA.
- Regular or injected conversion results can be configured to be read via DMA respectively.

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7 Attention

7.1 DSMU Clocks

There are three clocks in DSMU:

- APB2 bus clock PCLK2: Register interface clock.
- DSMU Kernel clock:

  Module operating clock DSMU_CLK, the clock source can be configured as follows:
  - APB2 bus clock PCLK2.
  - System Bus clock divided by 1/2/4/8/16.
- DSMU Kernel A clock:

  Audio clock ACLK, used only for clock output, the clock source can be configured as follows:
  - APB2 bus clock PCLK2.
  - PLL1B/PLL2B/PLL3A.
  - Peripherals BUS clock.
  - Input clock from I2S CKIN pin.

7.2 Clock Frequency Requirements

In applications, the fequency of DSMU and external interface must meet the following requirements:

- DSMU_CLK >= PCLK2.
- When an input channel is configured as parallel data input:
  - Standard input mode: DSMU_CLK > (2 * input data rate).
  - Interleaved input mode: DSMU_CLK > (4 * input data rate).
- When an input channel is configured as a serial SPI interface, and the sampling clock is input from an external device:
  - The maximum sampling clock is 20MHz,
  - And the sampling clock must be also less than (DSMU_CLK/4).
- When an input channel is configured as a serial Manchester interface:
  - The maximum Manchester recovered clock is 10MHz,.
  - And the recovered clock must be less than (DSMU_CLK/6).
  - The output clock divider coefficient CLKOUTDIV must meet the following requirements:

  DSMU_CLK/(2*CLKOUTDIV) < Recovered Clock < DSMU_CLK/(CLKOUTDIV+1)

7.3 Sampling Rate

DSMU requires oversampling of the input data, which can greatly improve data accuracy, but will also reduce the output sampling rate:

- Output sampling rate = Input data sampling rate / Overall oversampling rate.

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- The overall oversampling rate is determined by the following three parameters:
  - SINC filter oversampling rate FOSR: FOSR bit field value + 1
  - Filter order FORD: FastSinc=4, $Sinc^1$, $Sinc^2$, $Sinc^3$, $Sinc^4$, $Sinc^5$=1~5.
  - Integrator oversampling rate IOSR: IOSR bit field value + 1.
- When performing regular conversion in fast mode:
  - The overall oversampling rate of first conversion is: FOSR * (FORD + IOSR-1) + 1
  - The overall oversampling rate of subsequent conversio is: FOSR * IOSR
- When performing injected conversion, or regular conversion without fast mode:
  - The overall oversampling rate is: FOSR * (FORD + IOSR-1) + 1

7.4 Valid Data Range

DSMU inputs and outputs are both signed integer data, within the following ranges:

- Maximum input resolution is 16 bits: $-2^{15} \sim (2^{15}-1)$.
- Maximum output resolution is 24 bits: $-2^{23} \sim (2^{23}-1)$.
- Maximum intermediate calculation result resolution is 32 bits: $-2^{31} \sim (2^{31}-1)$.

Therefore, when configuring data filter parameters, it is necessary to avoid data overflow:

- The number of valid bits in the output result cannot exceed 24 bits.
- The number of valid bits in the oversampled result (before the right shift operation) cannot exceed 32 bits.
- Data filter parameters can be evaluated using the following formulas:
  - When using FastSinc filtering: 2 * FOSR2 * IOSR <= 2^31
  - When using $Sinc^1$~$Sinc^5$ filtering: $FOSR^{FORD}$ * IOSR <= 2^31

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8 History versions

Version	Date	Notes
V1.0.1	2025.12.5	Initial version

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