User guide

N32H7xx Series USBHS User Guide

Introduction

The N32H7xx series microcontrollers built-in two high-speed USB 2.0 interfaces, supporting USB 2.0 High-Speed (480Mb/s), Full-Speed (12Mb/s), and Low-Speed (1.5Mb/s) Host modes, as well as USB 2.0 High-Speed (480Mb/s) and Full-Speed (12Mb/s) Device modes.

The N32H7xx USBHS has a built-in high-speed PHY, supporting high-speed mode without the need for an external PHY chip.

This document is intended to help users use USBHS correctly and improve the stability of its operation.

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1 N32H7xx USBHS brief introduction

1.1 USBHS Pin

The N32H7xx series USBHS1 and USBHS2 each have 5 pins. When USBHS is enabled, the corresponding pins need to be configured in multiplexed function mode.

Table 1-1 N32H7xx Series USBHS Pins

Pin Name	USBHS1	USBHS2	Pin Configuration
VBUS	PA9	PB13	Push-pull alternate output
ID	PA10	PB12	Push-pull alternate output
DP	PA12	PB15	Push-pull alternate output
DM	PA11	PB14	Push-pull alternate output
SOF	PA8	PA4	Push-pull alternate output

The SOF pin can be used or not used depending on user needs. When USBHS is as device, it outputs a pulse through the SOF pin when receiving a SOF frame from the host; when USBHS is as host, it outputs a pulse through the SOF pin when sending a SOF frame.

The VBUS power of USBHS is controlled by a switch chip. As shown in Figures 1-1 and 1-2, the 5V voltage on VBUS is controlled through the control signals USB1_CTRL and USB2_CTRL (users can choose the pins themselves). When operating in host mode, it is necessary to enable VBUS to provide 5V voltage externally.

Figure 1-1 USBHS1 VBUS Control Circuit

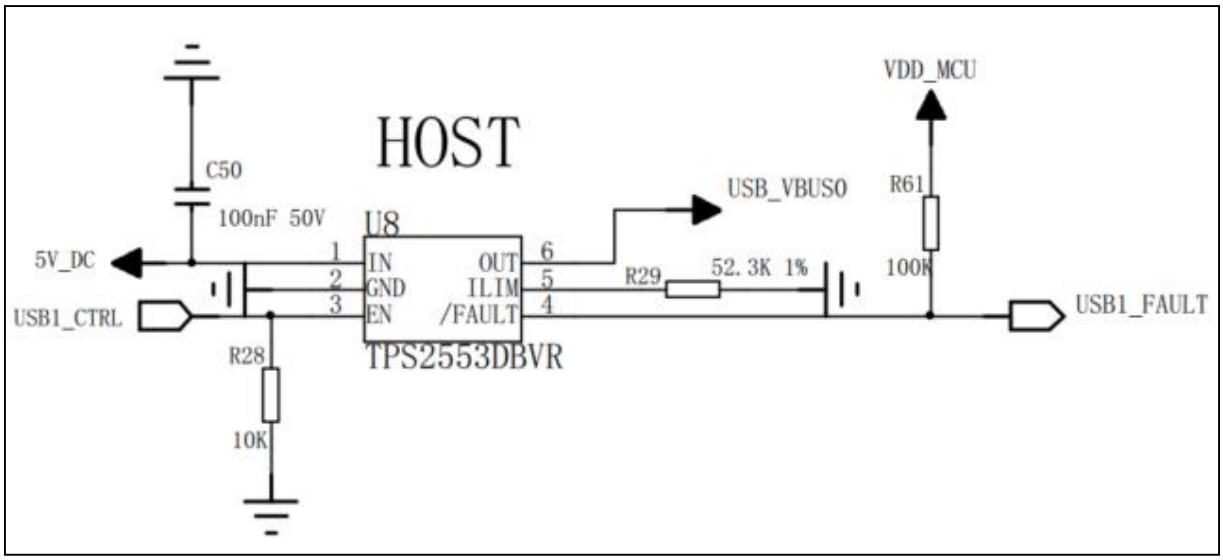

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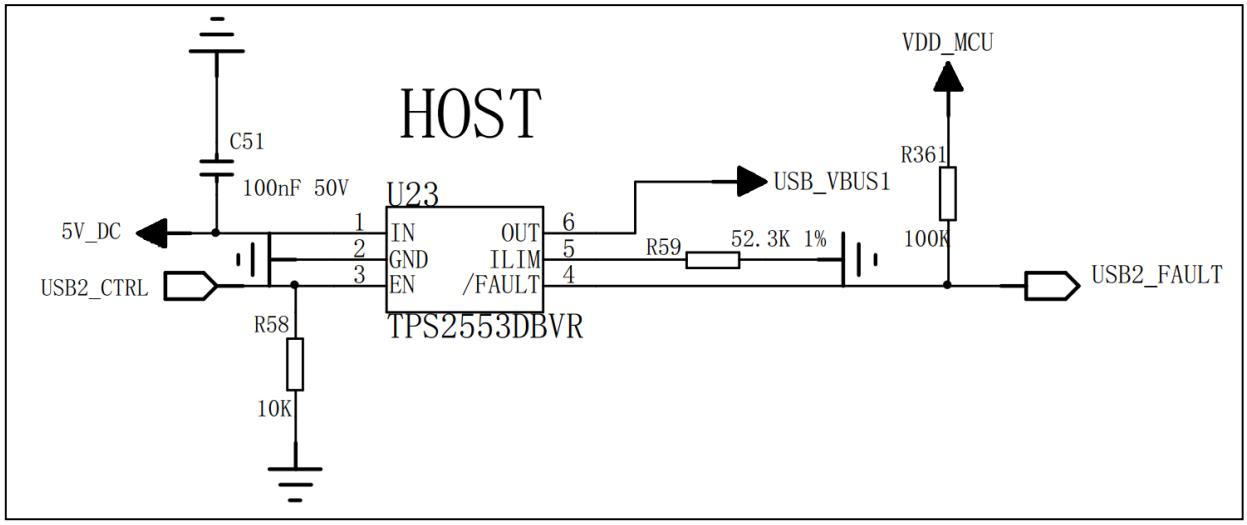
Figure 1-2 USBHS2 VBUS Control Circuit



1.2 USBHS Clock

When using the USBHS module, the USBHS clock source is selected as the external high-speed crystal (HSE), and the HSE crystal must be 10MHz, 12MHz, 19.2MHz, 24MHz, 25MHz, 27MHz, 30MHz, or 40MHz.

As shown in Figure 1-3, in the code, the HSE is configured as the clock source for USBHS, and the corresponding USB clock and power are enabled.

Figure 1-3 USBHS Clock Configuration

```
/**
*\*\name    USBHS_ConfigPLL.
*\*\fun     Configure USBHS clock.
*\*\param   none.
*\*\return  none.
*\*\
**/
static void USBHS_ConfigPLL(void)
{
    /* turn on HSE */
    RCC_ConfigHse(RCC_HSE_ENABLE);
    /* Select USB clock source */
    RCC_ConfigUSBRefClk(RCC_USBREFCLK_HSE_DIV1);
    /* Enable the PWR clock */
    RCC_EnableAHB5PeriphClk2(RCC_AHB5_PERIPHEN_PWR, ENABLE);
#ifdef USE_USBHS1
    /* Enale USBHS1 clock */
    RCC_EnableAHB2PeriphClk1(RCC_AHB2_PERIPHEN_M7_USB1, ENABLE);
    PWR_MoudlePowerEnable(HSC1_USB1_PWRCTRL, ENABLE);
#endif

#ifdef USE_USBHS2
    /* Enale USBHS2 clock */
    RCC_EnableAHB1PeriphClk1(RCC_AHB1_PERIPHEN_M7_USB2, ENABLE);
    PWR_MoudlePowerEnable(HSC2_USB2_PWRCTRL, ENABLE);
#endif
}
```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1.3 USBHS SDK

1.3.1 USBHS SDK Directory Structure

Figure 1-4 shows the USBHS driver directory in the SDK:

1. The device directory contains the core drivers and class drivers for device development. Class drivers include device class drivers such as audio, cdc, customhid, hid_keyboard, mouse, and msc.
2. The USBHS core driver under the driver directory; choose the corresponding driver based on whether it is a device or host.
3. The host directory contains the core drivers and class drivers when acting as a host. The class drivers include host class drivers such as CDC, HID, and MSC.

Figure 1-4 USBHS SDK Driver Directory

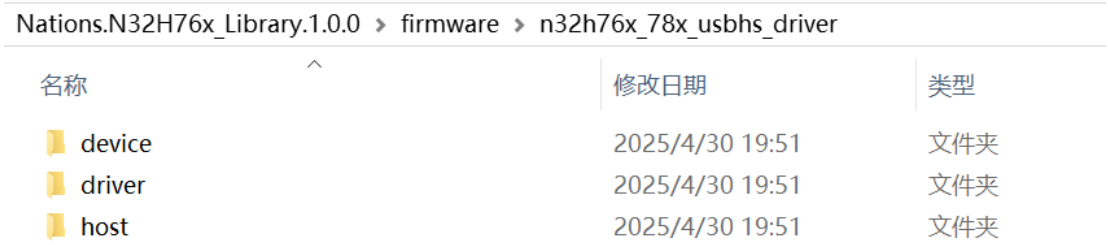
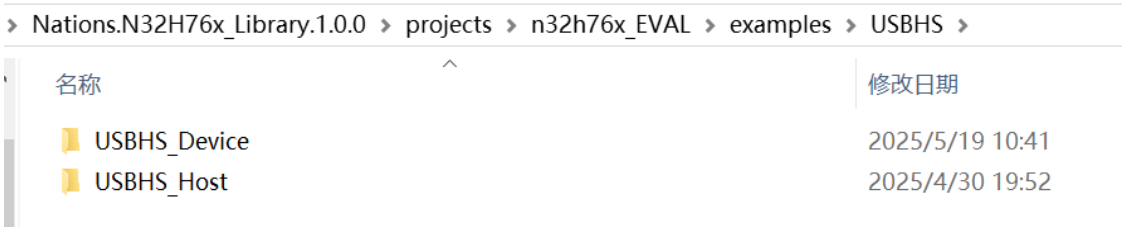


Figure 1-5 shows the USBHS DEMO directory in the SDK:

1. The USBHS_Device directory contains demos for USBHS devices, including CDC, HID_Customer, HID_Keyboard, HID_Mouse, MSC, and other device demos.
2. The USBHS_Host directory contains demos for USBHS host functionality, including CDC, HID, MSC, and other host demos.

Note: For specific usage of the demo, please refer to the readme in the demo.

Figure 1-5 USBHS SDK DEMO Directory



1.3.2 Notes on Using the USBHS Demo

1. Mode Switching: You can switch between full-speed or high-speed mode by change the USE_USB_HS_IN_FS or USE_USB_HS_IN_HS macro definitions.
2. SOF Pin Output: The SOF pin output function can be used by defining the USB_SOF_OUTPUT_ENABLED macro.

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2 USBHS Hardware Design

The hardware design considerations for the USBHS interface are as follows:

1. DP/DM traces need to have impedance control, with differential impedance at 90Ω ±10%
2. DP/DM traces require length matching, keeping the length difference of the differential pair within ±5 mils;
3. DP/DM traces should be routed symmetrically, avoiding right-angle turns to reduce impedance discontinuities;
4. Add ESD diodes near the connector on the DP/DM lines to prevent static damage;
5. Ensure a complete reference ground plane under the DP/DM differential lines, avoiding crossing splits to reduce return path interference;
6. DP/DM traces should avoid areas with high-frequency noise such as power and clock lines, and add shielded ground vias around the differential lines;
7. In some designs, a 22Ω resistor needs to be added in series at the end of the differential line to suppress reflections;
8. When using the USBHS module, an external HSE crystal must be used as the clock source, and the HSE frequency can only be 10MHz, 12MHz, 19.2MHz, 24MHz, 25MHz, 27MHz, 30MHz, or 40MHz.

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3 Version history

Date	Version	Modify
2025/12/26	V1.0.0	Initial version

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