N32G033xx Datasheet

N32G033 series based on Arm® Cortex®-M0, run up to 64MHz, supports fast FLASH execution of instructions, up to 64KB embedded Flash, 6KB SRAM, integrated analog interface, 1x12bit 1Msps ADC, 3x differential rail to rail operational amplifiers, 1x high-speed comparator, 1x NTC, 4x complementary electronic control TIM, integrated 3x UART, 2x I2C, 2x SPI communication interfaces, 1x 3-channel DMA.

Key features

- **Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - Run up to 64MHz
- **Encrypted memory**
  - Up to 64KByte embedded Flash memory, data 100,000 cycling and 10 years of data retention
  - SRAM of 6KB, STOP modes can be configured as retention
- **Low-power management**
  - Run mode: all peripherals configurable
  - STOP mode: TIM6, IWDG, UART3, COMP configurable operation, SRAM retention, all IO retention
- **Clock**
  - HSI_64M: Internal high-speed RC OSC 64MHz
  - LSI: Internal low-speed RC OSC 32KHz
  - MCO: Support 1-way clock output, configurable SYSCLK, HSI, and LSI clock output.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Support watchdog reset, Support software reset
- **Communication interface**
  - 3xUART, Supports asynchronous mode, multiprocessor communication mode, single-wire half-duplex mode, hardware 485 mode, UART3 supports low-power wake-up.
  - 2xSPI, up to 16 MHz
  - 2xI2C, up to 1 MHz, configurable master/slave mode
- **1xDMA, 3-channel, channel source address and destination address can be arbitrarily configurable**
- **Accelerator**
  - Supports 32-bit signed/unsigned dividers
  - Supports 32-bit unsigned Square root
- **Analog interface**
  - 1x12bit 1Msps ADC, up to 11 external single-ended input channels
  - 3 rail to rail differential operational amplifiers, built-in bias 1.8V, 1/2 VDDA, 1/4 VDDA, built-in maximum 32x programmable gain amplifier
  - 1 high-speed analog comparator with built-in 256 level adjustable comparison benchmark
  - Support internal NTC

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- Internal independent reference voltage reference source
- Internal integrated voltage inspection(PVD)

- **Supports up to 29 GPIos that support reuse functionality**
- **Timer counter**
  - 1x16-bit advanced timer counters, support input capture, complementary output, each timer support 7 independent channels. 4 channels support 8 complementary PWM outputs
  - 1x16-bit general purpose timer counters, 4 independent channels, supports input capture/output compare/PWM output
  - 1x32-bit general purpose timer counters, 3 independent channels, supports input capture/output compare/PWM output
  - 1x32-bit basic timer counters, supports low-power wake-up.
  - 1x24-bit SysTick
  - 1x14-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Security features**
  - Support write protection(WRP)
  - Support multiple read protection(RDP) levels (L0/L1/L2)
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 2.0V~5.5V
  - Operating Temperature Range: -40℃~105℃
- **Package**
  - QFN32(5 x 5mm)
  - QFN32 (4 x 4mm)
  - LQFP32
  - QFN20
  - QFN20-1
  - UFQFPN20
  - TSSOP20

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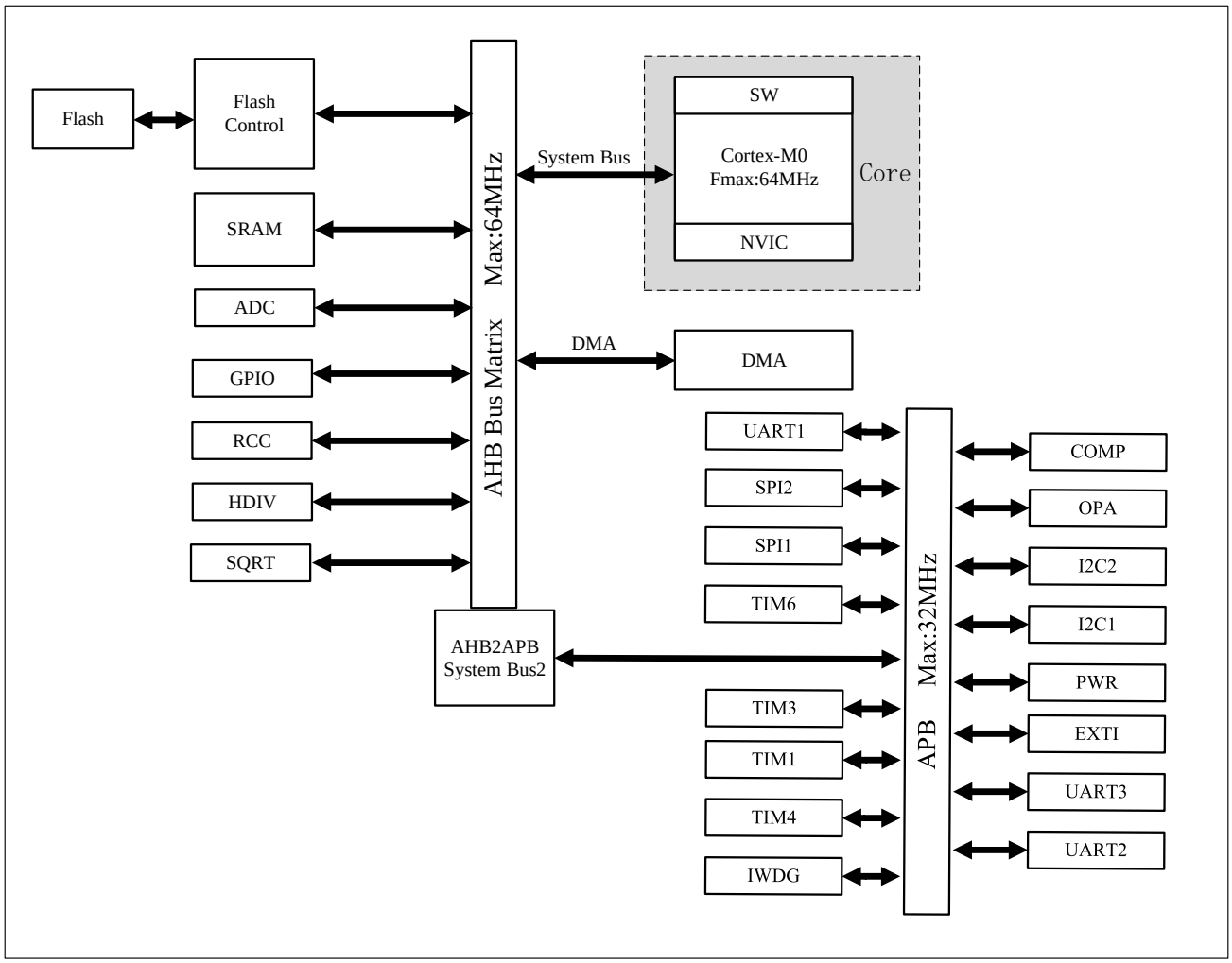
1 Product introduction

N32G033 family of microcontrollers features an ARM Cortex®-M0 core. Maximum operating main frequency 64MHz, integrated up to 64KB of in-chip encrypted storage Flash, maximum 6KB of embedded SRAM. It has an internal high speed AHB bus, a low speed peripherals clock bus APB and bus matrix. It supports up to 29 reusable I/Os and provides a rich array of high performance analog interfaces, including 1x 12-bit 1Msps ADC, up to 11 external input channels, and 3x differential rail to rail operational amplifier , 1 high-speed comparator, 4-channel complementary electronic control TIM, supporting 32-bit signed/unsigned dividers, supporting 32-bit unsigned Square root. At the same time, it provides a variety of digital communication interfaces, including 3x UART, 2x I2C, 2x SPI communication interface.

N32G033 series products can operate stably in a temperature range of -40 ℃ to +105 ℃, with a power supply voltage of 2.0V to 5.5V, including STOP power mode, meeting the requirements of low-power applications. This series of products offers different packaging forms with a maximum of 32 pins.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32G033 Block Diagram



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1.1 List of devices

Table 1-1 N32G033 Series devices features and peripheral list

Part Number		N32G033K8L7	N32G033K8Q7	N32G033K8Q7-1	N32G033F8Q7	N32G033F8Q7-1	N32G033F8S7	N32G033F8U7
Flash（KB）		64	64	64	64	64	64	64
SRAM（KB）		6	6	6	6	6	6	6
CPU frequency		ARM Cortex-M0 @64MHz						
Working environment		2.0~5.5V/-40~105℃						
Timer	Advanced	1						
	16 bit General	1						
	32 bit General	1						
	Basic	1						
Communication interface	SPI	2						
	I2C	2						
	UART	3						
GPIO		27	29	29	19	19	17	17
DMA		1x 3 Channel						
12bit ADC		1x 10Channel	1x 11Channel	1x 11Channel	1x 9Channel	1x 9Channel	1x 9Channel	1x 7Channel
COMP		1						
OPA		3	3	3	2	2	1	1
Security protection		Read/write protection(RDP/WRP)						
Package		LQFP32	QFN32(5x5 mm)	QFN32(4x4 mm)	QFN20	QFN20-1	TSSOP20	UFQFPN20

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2 Functional description

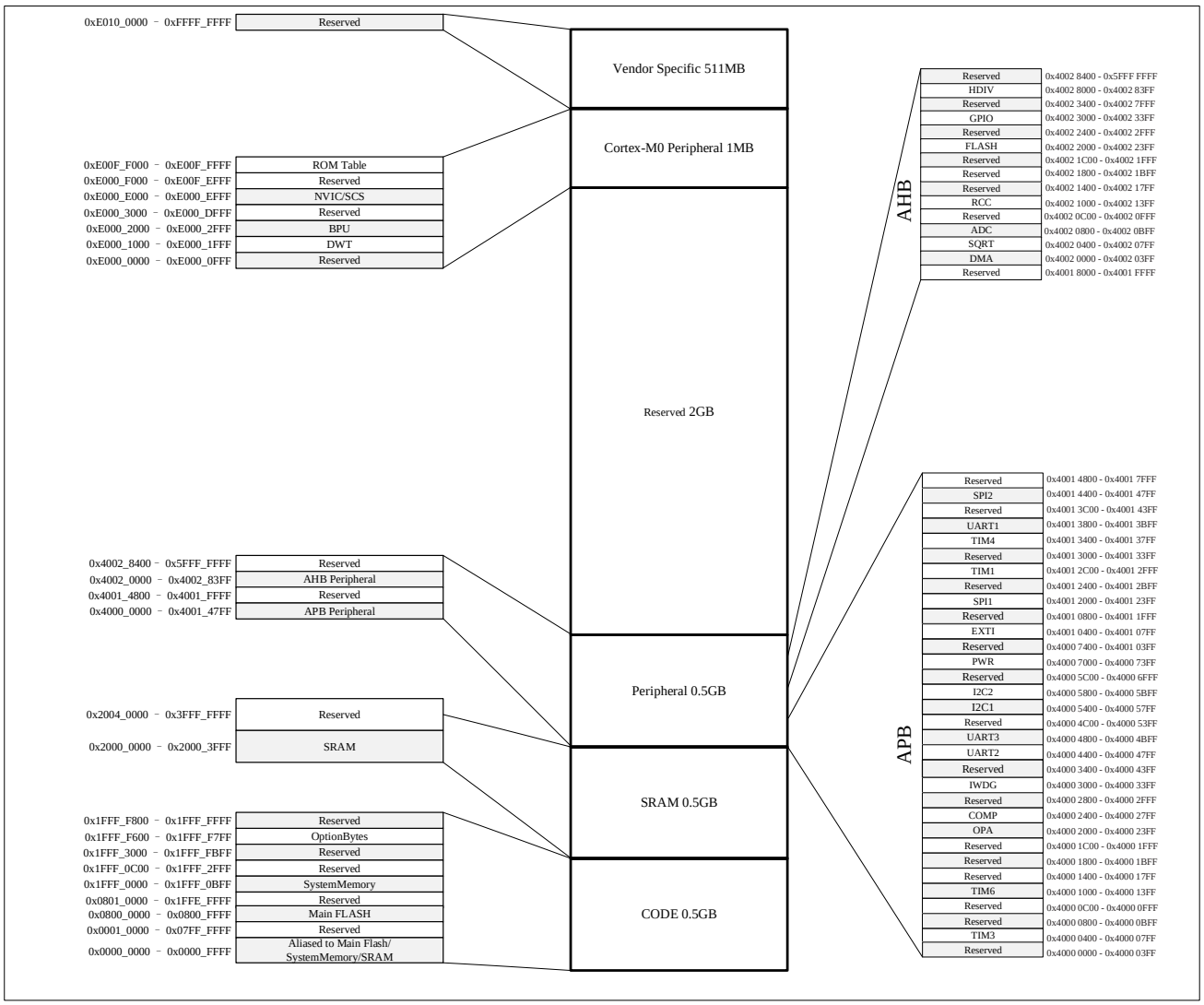
2.1 Processor core

N32G033 series integrates the latest generation of embedded ARM Cortex®-M0 processor

2.2 Storage

N32G033 series devices include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory address map



2.2.1 Embedded FLASH memory

Integrated up to 64K bytes embedded encryption FLASH, used to store programs and data, page size of 512byte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

2.2.2 Embedded SRAM

Integrated up to 6K bytes SRAM. In STOP mode, SRAM can hold data.

2.2.3 Nested vectored interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is tightly connected to the interface of the kernel, which can realize

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low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 21 maskable interrupt channels (not including 6 Cortex®-M0 interrupt lines)
- 4 programmable priority levels (using 2-bit interrupt priority levels)
- Low-latency exception and interrupt handling
- Power management control
- Realization of system control register

The module provides flexible interrupt management functions with minimal interrupt delay

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 11 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its triggering event (rising edge or falling edge or bilateral edge) and can be individually shielded. There is a suspended register that maintains the state of all interrupt requests. The corresponding bit of the suspend register can be cleared by writing '1'.

2.4 Clock system

The device provides a variety of clocks for users to choose from, including internal high speed RC oscillator HSI (64MHz), internal low speed clock LSI (32KHz).

Multiple prescaler are used to configure the AHB frequency and low speed APB regions. AHB has a maximum frequency of 64MHz, APB has a maximum frequency of 32MHz.

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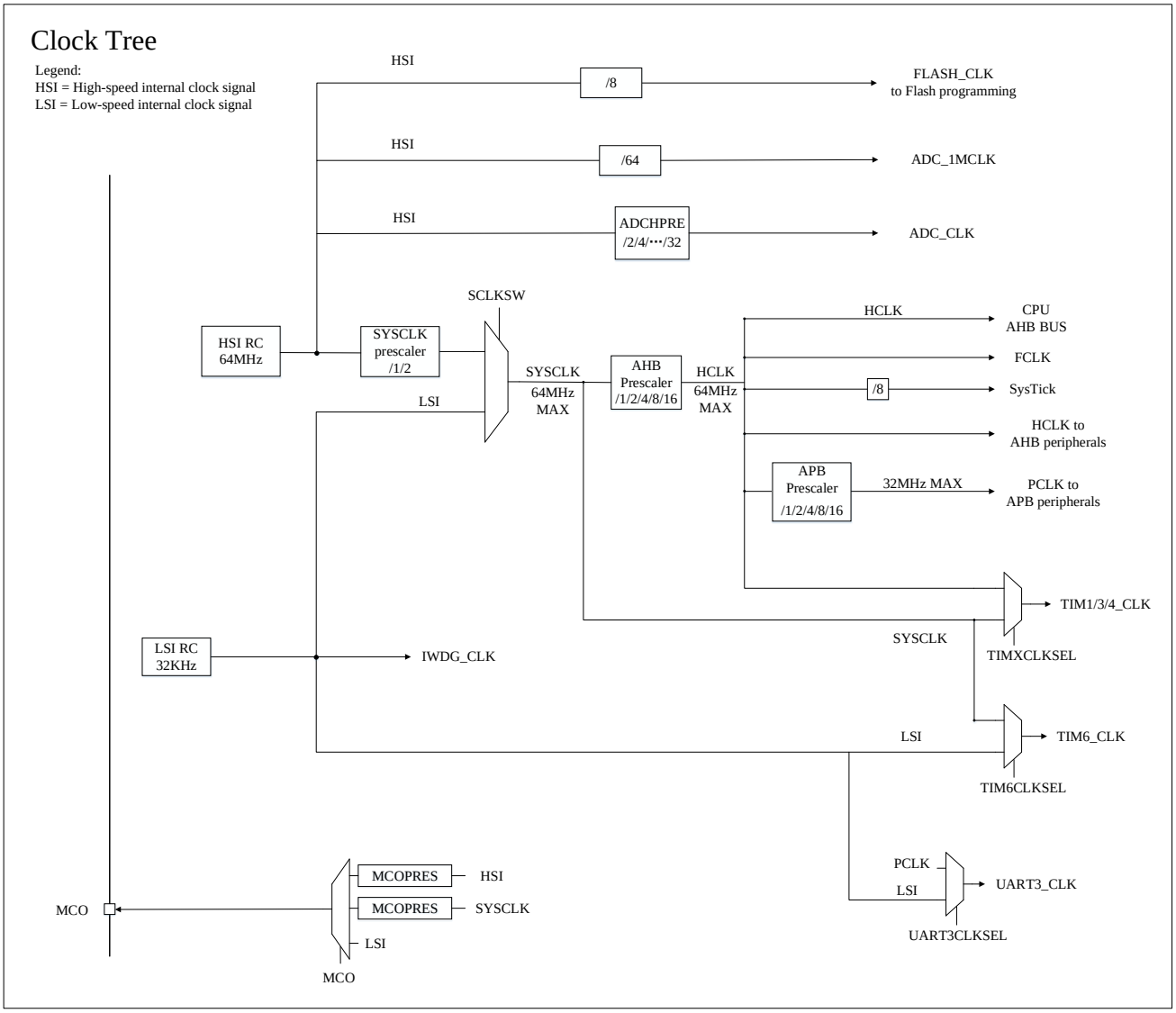
Figure 2-2 Clock Tree



2.5 Boot mode

At BOOT time, the BOOT mode after reset can be selected with the BOOT0 pin and option byte BOOT configuration (USER3).

- Boot from program FLASH Memory
- Boot from System Memory
- Boot from internal SRAM

The bootloader is stored in the system memory and can be programmed into the FLASH Memory/SRAM area through UART1. For specific instructions on using BOOT startup, please refer to the “CN-UG_N32G033 Series BOOT User Guide.pdf ”.

2.6 Power supply scheme

- VDD area: The voltage input range is 2.0V~5.5V, which mainly provides power input for Main Regulator, IO and clock reset system.
- VDDD area: The voltage regulator supplies power for the CPU, AHB, APB, SRAM, FLASH and most digital peripheral interfaces.

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PWR is the power control module of the entire device, its main function is to control N32G033 to enter different power modes and can be awakened by other events or interrupts. N32G033 supports RUN and STOP modes.

2.7 Programmable voltage detector

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 2.0V.

When V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is reset without the need for an external reset circuit.

The device has a programmable voltage detector (PVD), which monitors the V_{DD} power supply and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, it will generate an interrupt. The PVD function is turned on by software.

Table 4-6 is the value reference of $V_{POR/PDR}$ and V_{PVD}.

2.8 Low power mode

N32G033 is in RUN mode after system reset or power-on reset. When the CPU does not need to run, you can choose to enter a low power mode to save power.

N32G033 low power mode:

- STOP mode (most of the clocks are turned off, the voltage regulator is still running in low power mode)
- In addition, the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses

2.9 DMA

The device integrates a flexible general-purpose DMA controller that supports 3 DMA channels to manage data transfers from memory to memory, peripherals to memory, and memory to peripherals.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with peripherals: SPI, I2C, UART, TIMx (Advanced/General/Basic Timer).

2.10 Timer and watch dog

Up to 1 advanced control timer, 2 general-purpose timers and 1 basic timer, 1 watchdog timer and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low power timer:

Table 2-1 Timer function comparison

Timer	Counter resolution	Counter type	Prescaler	Capture/Compare channel	Complementary output
TIM1	16-bit	Up Down Up/Down	Any integer between 1~65536	4/7	support
TIM3	16-bit	Up Down Up/Down	Any integer between 1~65536	4	Unsupported

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TIM4	32-bit	Up Down Up/Down	Any integer between 1~65536	3	Unsupported
TIM6	32-bit	Up	Any integer between 1~65536	0	Unsupported

2.10.1 Advanced-control timers (TIM1)

The advanced control timers (TIM1) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and brake function. Suitable for motor control.

The main functions of advanced timers include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 7 channels
- 7 compare channels(CH1/2/3/4/5/6/7), the working modes are PWM output, Ouput compare, One-pulse mode output.
- 4 capture channels(CH1/2/3/4), the working mode is Input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with adjustable dead-time
  - For TIM1, channel 1,2,3,4 support this feature
- Timer can be controlled through external signals.
- Multiple timers are interconnected internally to achieve synchronization or linking of timers.
- TIM1_CC5 is used for COMP blanking
- TIM1 channels 1/2/3/4/5/6/7 and TRGO signals can trigger the ADC.
- Incremental (orthogonal) encoder interface: used to track the running trajectory and resolve the rotation direction.
- Hall sensor interface: used for three-phase motor control.

2.10.2 General-purpose timer (TIM3)

The general-purpose timers (TIM3) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.
The main functions of advanced timers include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)

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- TIM3 up to 4 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Multiple timers are interconnected internally to achieve synchronization or linking of timers.
- Incremental (orthogonal) encoder interface: used to track the running trajectory and resolve the rotation direction.
- Hall sensor interface: used for three-phase motor control.
- Support capturing internal comparator output signals.

2.10.3 General-purpose timer (TIM4)

The general-purpose timers (TIM4) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.
The main functions of advanced timers include:

- 32-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM4 up to 3 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Multiple timers are interconnected internally to achieve synchronization or linking of timers.
- Incremental (orthogonal), pulse+symbol, CCW/CW encoder interface: used to track the running trajectory and resolve the rotation direction.
- Hall sensor interface: used for three-phase motor control.
- Support capturing internal comparator output signals.

2.10.4 Basic timer -TIM6

The basic timer contains a 32-bit counter.

- 32-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- The events that generate the interrupt/DMA are as follows:
  - Update event
- Supports STOP mode wake-up: when the clock source is configured as LSI, STOP mode can be woken up by

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updating the interrupt (linked to EXTI9)

2.10.5 Systick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard decrement counter.

It has the following characteristics:

- 24 bit decrement counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.10.6 Watchdog (WDG)

Support independent watchdog (IWDG). The watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 14-bit decrepit counter and an 3-bit predivider. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

2.11 I2C bus interface (I2C)

The device integrates up to 2 independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus (SMBus), and Power Management Bus (PMBus).

The functions of the I2C interface are described as follows:

- This module can be used as master device or slave device;
- I2C master device function:
  - Generate a clock;
  - Generate start and stop signals;
- Function of I2C slave device
  - Programmable address detection;
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
  - Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and broadcast calls;
- Support different communication speeds;
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz);
  - Fast + (up to 1MHz);
- Status flags:
  - Transmitter/receiver mode flag;

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- Byte transmit complete flag;
- I2C bus busy flag;

- Error flags:
  - Arbitration is missing in Master Mode.
  - Acknowledge (ACK) error after address/data transfer;
  - Error start or stop condition detected
  - Overrun or underrun when disable extend clock function;
- Supported interrupt vectors: event interrupts and error interrupts
- Optional extend clock function
- Supports digital and analog filtering
- Generation or verification of configurable PEC(Packet error detection)
  - In transmit mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25 ms clock low
  - 10 ms accumulates low clock extension time of master device
  - 25 ms accumulates low clock extension time of slave device
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
- Compatible with the PMBus

2.12 Universal asynchronous transceiver (UART)

N32G033 series products integrate up to 3 universal asynchronous transceivers (UART1 / UART2 / UART3).

UART interface supports asynchronous communication mode, multiprocessor communication mode, single wire half duplex communication mode, etc.

Main features of UART are as follows:

- Full duplex, asynchronous communication
- Supports single-wire half-duplex communication
- Baud rate is configurable, up to 4Mbit/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- Hardware generated parity bit and parity bit checking
- Support TX/RX swap function
- DMA sending and receiving
- Support RS-485
- UART3 supports low-power wake-up
- Multiprocessor communication: if the address does not match, it enters silent mode, which can be awakened by idle bus detection or address identification.
- Serial Infrared Protocol (IrDA SIR) encoding and decoding, and provides two modes of operation: normal and

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low power consumption.

- supports LIN mode
- Multiple error detection: data overflow error, frame error, noise error, check error.
- Multiple interrupt requests:
  - ✧ send data register empty,
  - ✧ send complete,
  - ✧ data received,
  - ✧ bus idle,
  - ✧ data overflow,
  - ✧ frame error,
  - ✧ noise error,
  - ✧ Parity error
  - ✧ LIN mode break frame detection,
  - ✧ recevier timeout.

Mode configuration:

UART modes	UART1	UART2	UART3
Asynchronous mode	support	support	support
Multiprocessor communication	support	support	support
Half duplex (single wire mode)	support	support	support
IrDA	support	support	support
LIN	support	support	support
RS-485	support	support	support

2.13 Serial peripheral interface (SPI)

2x SPI interfaces. SPI allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCLK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-wire simplex synchronous transmission using a bidirectional data wire.

The main functions of SPI interfaces are as follows:

- 3-wire full-duplex synchronous transmission;
- two-wire simplex synchronous transmission with or without a third bidirectional data wire;
- 8 or 16 bit transmission frame format selection;
- Master or slave operations;
- Support multi-master mode;
- 8 master mode baud rate prescaling factors (up to $f_{PCLK}/2$);
- Slave mode frequency (max. $f_{PCLK}/2$);
- Fast communication between master mode and slave mode;
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes;
- Programmable clock polarity and phase;
- Programmable data order, MSB before or LSB before;

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- Dedicated send and receive flags that trigger interrupts;
- SPI bus busy flag;
- Hardware CRC for reliable communication;
  - In send mode, the CRC value can be sent as the last byte;
  - In full-duplex mode, CRC is automatically performed on the last byte received.
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum interface speed: 16Mbps

2.14 General purpose input/output (GPIO)

GPIO (General Purpose Input/Output) refers to general-purpose I/O, while AFIO (Alternate Function Input/Output) refers to multiplexed functional I/O. The chip supports up to 29 GPIO, which are divided into 3 groups (GPOA/GPIO B/GPIOF). Group A has 16 ports per group, Group B has 9 ports per group, and Group F has a total of 4 ports. GPIO ports share pins with other multiplexed peripherals, allowing users to flexibly configure according to their needs. Each GPIO pin can be independently configured as an output, input, or multiplexed peripheral functional port. Except for the analog input pin, all other GPIO pins have the ability to pass high currents.

GPIO ports have the following characteristics:

- Each GPIO port can be individually configured into multiple modes by software
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Push-pull output and pull-up/pull-down can be configured
  - Push-pull alternate function and pull-up/pull-down can be configured
  - Open-drain alternate function and pull-up/pull-down can be configured (Only I2C related multiplexing support)
- Individual bit set or bit clear function
- All IO supports external interrupt function
- All IO supports low power mode wake-up, rising or falling edge configurable
  - All EXTIs can be awakened, all GPIO can be configured to EXTI0~6, and 7 wake-up sources can be recorded (PA0~PA3: Group 1, PA4~PA7: Group 2, PA8~PA11: Group 3, PA12~PA15: Group 4, PB0~PB3: Group 5, PB4~PB8: Group 6, PF0~PF3: Group 7)
- Support software remapping I/O alternate function
- Support GPIO lock mechanism, reset the lock state to clear

Each I/O port bit can be programmed arbitrarily, but I/O port registers must be accessed as 32-bit words (16-bit half-word or 8-bit byte access is not allowed). The following figure shows the basic structure of an I/O port.

2.15 Analog/digital converter (ADC)

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. There are a total of 16 channels that can measure 11 external and 5 internal signal sources. The A/D conversion channels of each channel can be executed in single, continuous, and segment modes. The ADC conversion values are stored (left-aligned/right-aligned) in 16-bit data registers. An analog watchdog can be used to detect if the input voltage is within the user-defined high/low thresholds and the ADC's input clock has a maximum frequency of 32 MHz.

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The main features of the ADC are described below:

- Supports 12-bit resolution
- Only supports single ended input
- Interrupt generated when conversion ends and a simulated watchdog event occurs
- Conversion mode
  - Single conversion
  - Continuous conversion
- 10 result registers, channel numbers can be configured.
- 16 (11 external+5 internal) channel settings, sampling time can be individually configured.
- Single segment, double segment, three segment, and four segment custom sampling sequences can be sampled, and the number of sequences and channel numbers can be flexibly configured.
- Conversion completion interrupt: After each trigger source conversion is completed, a conversion completion flag is automatically generated, and the hardware setting software is reset to zero; Enable interrupt generation, including segment interrupt, any channel completion interrupt, all conversion completion interrupt, and watchdog interrupt
- Data alignment with embedded data consistency
- Rule conversion has internal and external triggering options
- Supports a maximum of 1MSPS
- Support ADC linkage: Supports 16 optional Trigger sources (including 14 TIM Trigger sources, EXTI, and software triggers), which can generate configurable length and specified channel conversions after triggering
- ADC power supply requirements: 2.4V to 5.5V.
- ADC input range: 0≤VIN≤VDDA.

2.16 Analog comparator (COMP)

Embedded with 1 comparators, it can be used as a stand-alone device (all ports of comparators lead to I/O) or combined with timers, which can be used in motor control applications to form cycle-by-cycle current control in conjunction with the PWM output from timers.

The main functions of the comparator are as follows:

- 1 independent comparator
- Internal reference input of independent 8-bit DAC
- Supports filtered clock
- Configurable high and low output polarity.
- Hysteresis configuration configurable none, low, medium, high
- Comparison results can be output to I/O ports or trigger timers for capturing events, OCREF_CLR events, braking events, generating interrupts
- Input channels can be re-selected for I/O ports, dedicated 8bit DAC
- COMP_CTRL register can be configured with read-only or read-write, and requires system reset or module reset to unlock when locked.
- Blanking support, Blanking source can be configured to generate Blanking.
- Configurable filter window size
- Configurable filter threshold size

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- Configurable sampling frequency for filtering

2.17 Operational amplifier (OPA)

The chip integrates three independent operational amplifiers with multiple operating modes, suitable for independent operational amplifier PGA and follower mode applications. The input range of OPAMP is 0V to VDDA, and the output range is 0.4V to VDDA-0.4V.

The main functions of the OPA are as follows:

- OPA1 supports independent operational amplifier mode, follower mode, differential PGA mode, and single ended PGA mode; OPA2, OPA3 differential PGA mode and following mode
- Support rail to rail input, input range is 0 to VDDA, output range is 0.4 to VDDA-0.4 programmable gain
- OPAMP can be configured as an instrument amplifier through external resistor connection
- Internal resistance feedback network configurable, 2% accuracy
- Programmable gain setting
- OPA1 single ended PGA gain: 2X, 4X, 8X, 16X, 32X times
- OPA1 differential PGA gain: 1X, 2X, 4X, 8X, 16X, 32X times
- OPA2, OPA3 differential PGA gain: 1X, 2X, 4X, 8X, 16X times
- Gain bandwidth: 5MHz
- Support independent write protectio

2.18 Temperature Sensors (TS)

The temperature sensor produces a voltage that varies linearly with temperature over a conversion range of 2.4V <VDDA< 5.5V. The temperature sensor is internally connected to the input channel of ADC_IN11, which is used to convert the output of the temperature sensor to a digital value.

2.19 HDIV and SQRT

Dividers (HDIV) and root mean square (SQRT) are mainly used in certain scenarios that require high computational energy efficiency, to partially supplement the computational shortcomings of microcontrollers. This divider and square root calculator can perform division or square root calculations on 32-bit integers.

The main properties of HDIV are as follows:

- Only supports 32-bit operations, with signed or unsigned operations
- Input: 32-bit dividend, 32-bit divisor
- Output: 32-bit quotient, 32-bit remainder
- Complete a signed/unsigned integer division operation in 8 clock cycles
- Dividing by zero, warning flag, data fixed return 0
- Support optional hardware auto enable (write divisor auto enable)
- Read quotient or remainder register, no need to query status, can be read immediately (enabled)

The main properties of SQRT are as follows:

- Only supports 32-bit operations
- Input: 32-bit unsigned square root integer
- Output: 16-bit root mean square
- Complete an unsigned integer square root operation in 8 clock cycles

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- Support optional hardware auto enable (write open square integer auto enable)
- Read result register, no need to query status, can be read immediately

2.20 Unique device serial number (UID)

The N32G033 series products have two built-in unique device serial numbers of different lengths, the 96-bit UID (Unique device ID) and the 128-bit UCID (Unique Customer ID), which are stored in the system configuration block of the flash memory, and the information they contain is written at the factory and is guaranteed to be unique to N32G033 series any one microcontroller in any case is unique, the user application or external devices can be read through the CPU or SWD interface, can not be modified.

UID is 96 bits, usually used as a serial number or as a password, when writing flash memory, this unique identifier is combined with software encryption and decryption algorithms to further improve the security of the code within the flash memory.

The UCID is 128 bits and complies with the National Technical Chip Serial Number Definition, which contains chip production and version related information.

2.21 Serial wire SWD debug port (SWD)

Embedded Arm SWD Interface.

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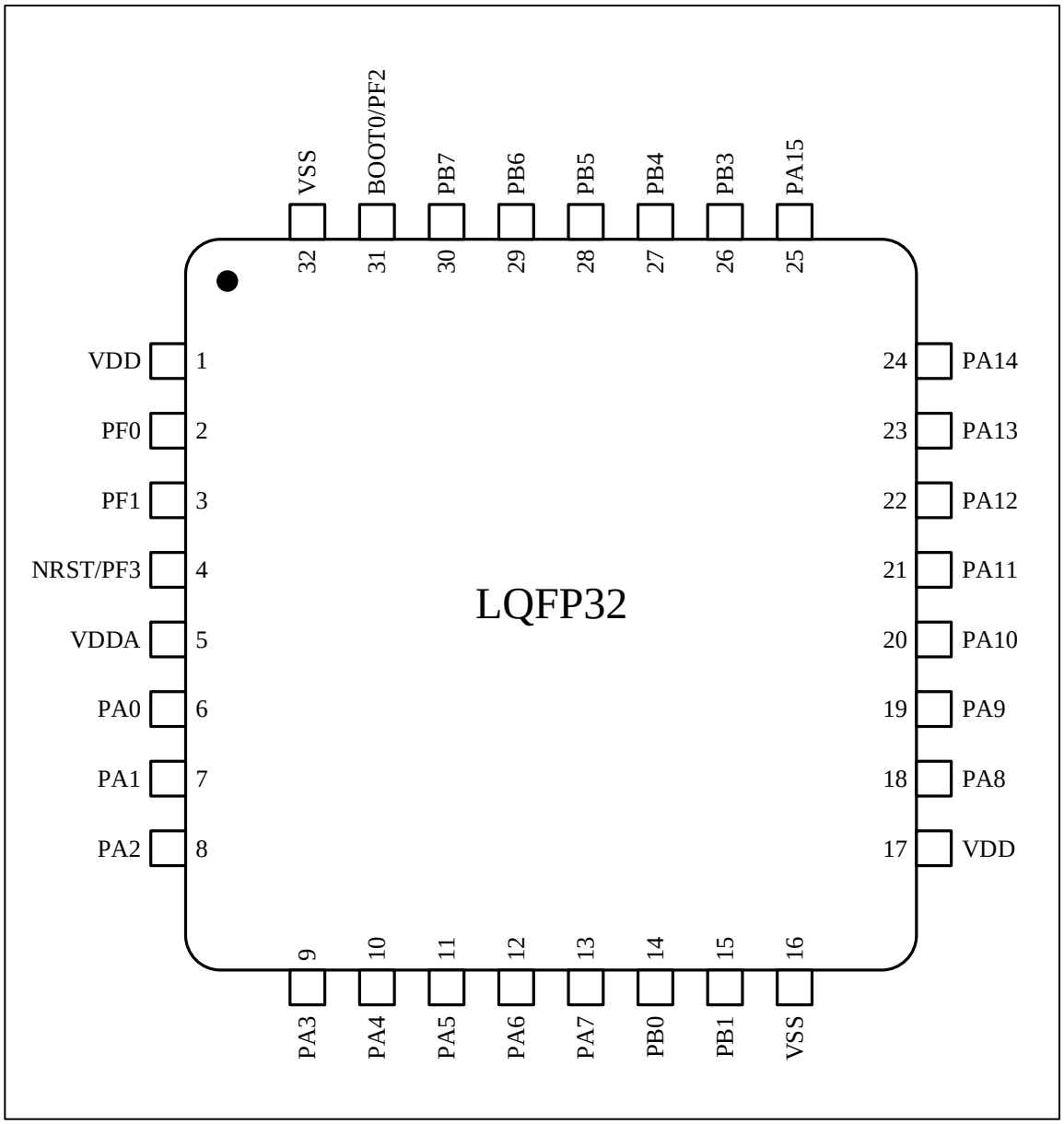
3 Pin descriptions

3.1 Pinouts

3.1.1 LQFP32

Figure 3-1 N32G033 Series LQFP32 pinouts



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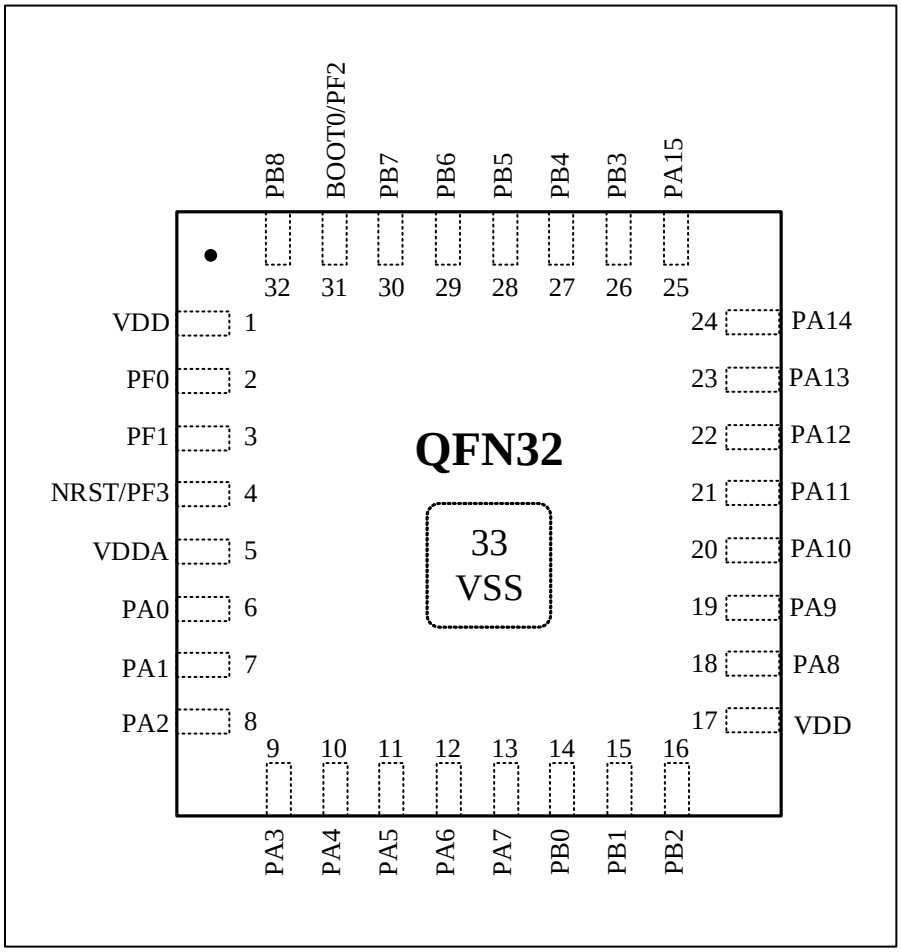
3.1.2 QFN32

Figure 3-2 N32G033 Series QFN32 pinouts



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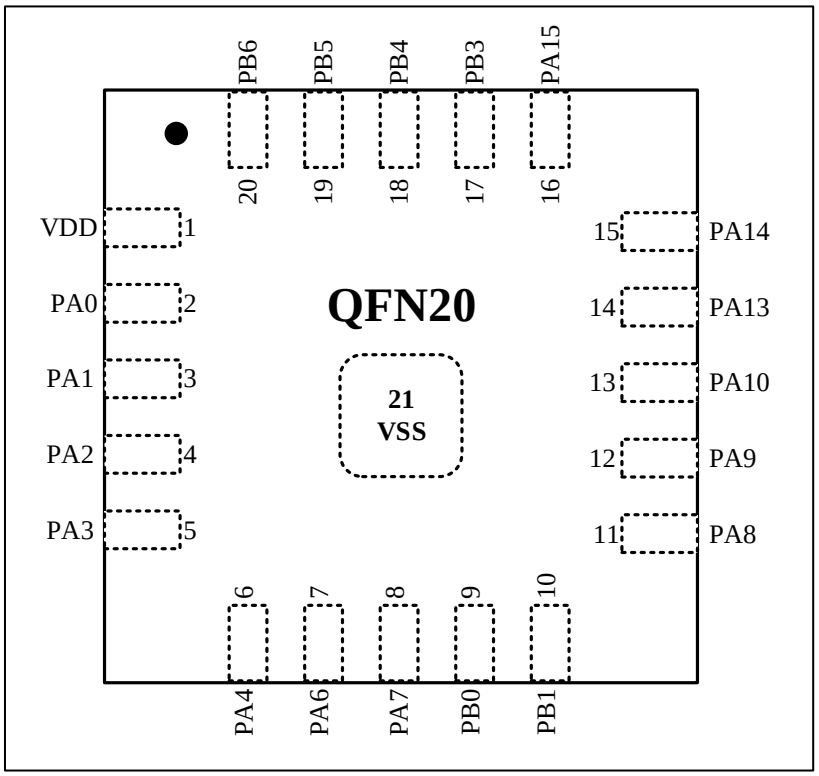
3.1.3 QFN20

Figure 3-3 N32G033 Series QFN20 pinouts



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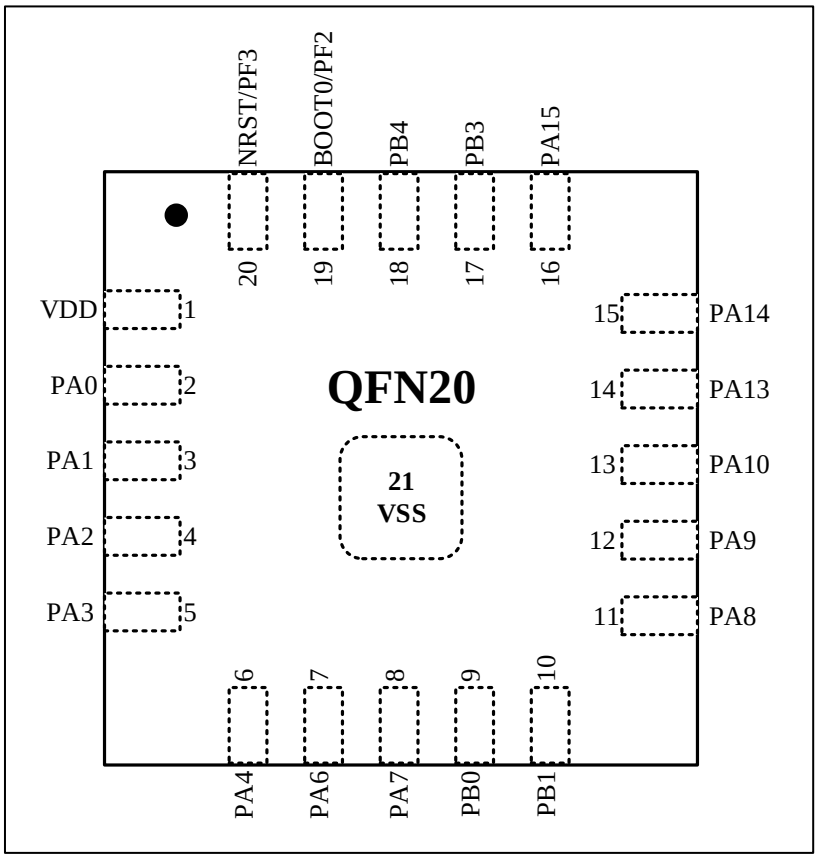
3.1.4 QFN20-1

Figure 3-4 N32G033 Series QFN20-1 pinouts



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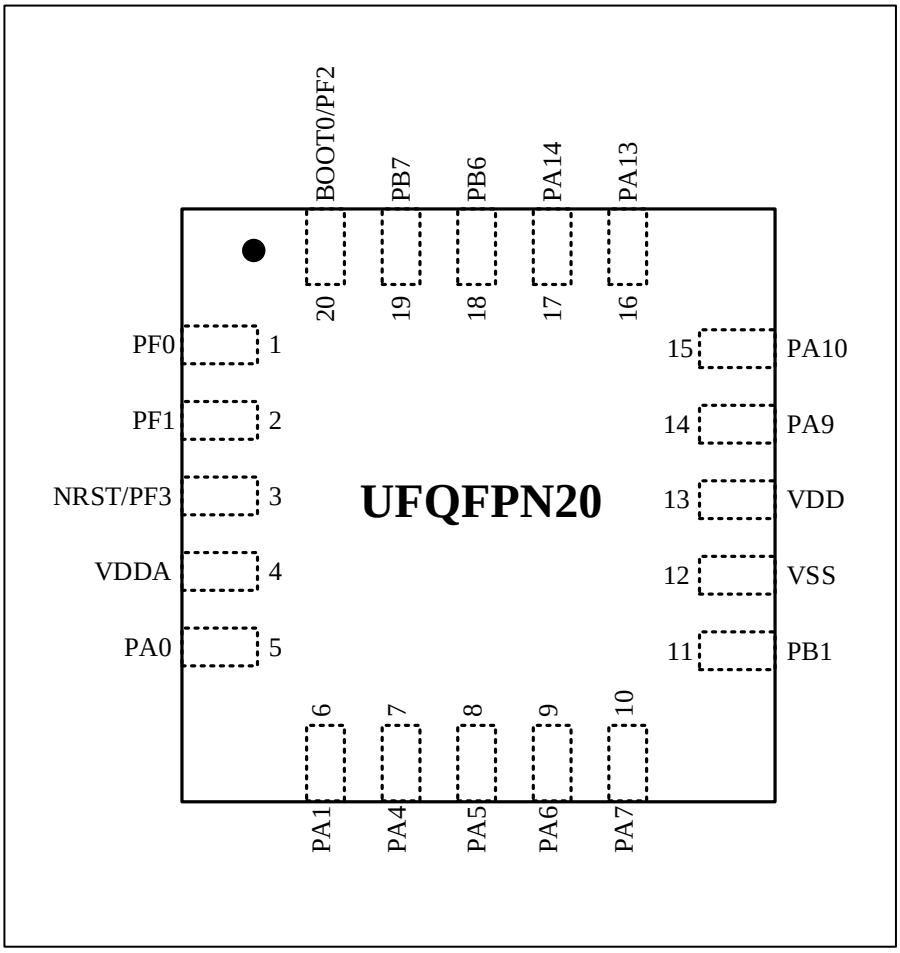
3.1.5 UFQFPN20

Figure 3-5 N32G033 Series UFQFPN20 pinouts



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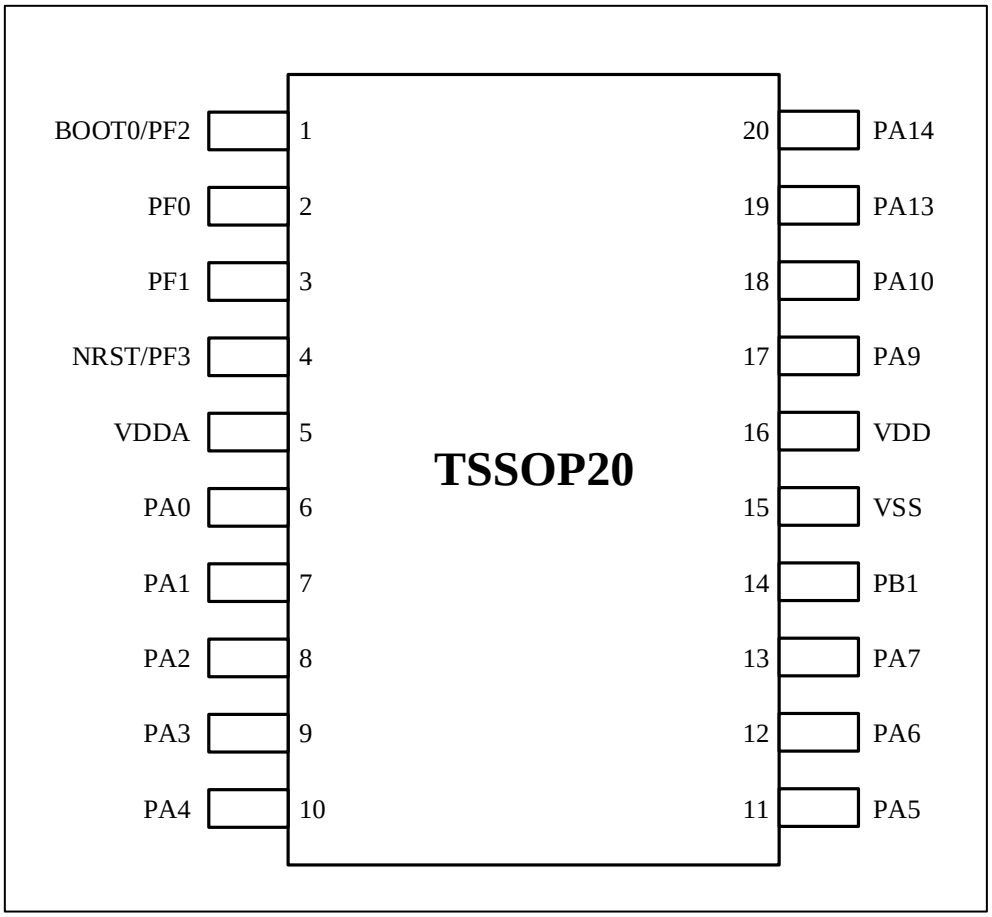
3.1.6 TSSOP20

Figure 3-6 N32G033 Series TSSOP20 pinouts



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3.2 Pin definitions

For details of alternate functions for IO, please refer to the "Alternate function" section within the "GPIO and AFIO" chapter of the User Manual.

Table 3-1 Pin definitions

Package						Pin name (function after reset)	Type(1)	I/O(2)	Alternate functions(3)	
LQFP32	QFN32	QFN20	QFN20-1	UFQFPN20	TSSOP20				Digital	Analog
1	1	1	1	-	-	VDD	S	TC	-	VDD
2	2	-	-	1	2	PF0	I/O	TC	I2C1_SDA, TIM3_CH1, UART1_TX, UART2_TX, UART3_TX, TIM3_ETR	OPAMP1_VINP
3	3	-	-	2	3	PF1	I/O	TC	I2C1_SCL, TIM3_CH2, UART1_RX, UART2_RX, UART3_RX, TIM4_ETR	OPAMP1_INM,
4	4	-	20	3	4	NRST/PF3(4)	I	RST	NRST	-
							I/O	TC	TIM3_CH3, TIM4_ETR, UART1_DE, UART2_DE, UART3_DE，	
5	5	-	-	4	5	VDDA	S	-	-	VDDA
6	6	2	2	5	6	PA0	I/O	TC	SPI1_SCK, UART2_RX, UART3_RX, TIM3_CH1, TIM1_CH5, TIM4_CH1, UART1_RX, COMP_OUT,	ADC_IN0, COMP_INM, OPAMP1_VINP
7	7	3	3	6	7	PA1	I/O	TC	EVENT_OUT, SPI1_NSS, I2C1_SMBA, TIM3_ETR, UART3_TX, TIM3_CH2, TIM1_CH6, TIM4_CH2, SPI1_MISO, UART2_TX, UART1_TX,	ADC_IN1, COMP_INP, OPAMP1_VINP
8	8	4	4	-	8	PA2	I/O	TC	UART1_TX, UART2_TX, SPI1_MOSI, TIM1_BKIN1, TIM3_CH3, TIM1_CH7, TIM4_CH3, UART3_TX,	ADC_IN2, OPAMP1_VINM

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9	9	5	5	-	9	PA3	I/O	TC	UART1_RX, UART2_RX, TIM1_CH2, SPI1_MISO, UART3_RX	ADC_IN3, COMP_INP
10	10	6	6	7	10	PA4	I/O	TC	SPI1_MISO, TIM3_CH1, TIM1_CH1, SPI1_NSS, I2C1_SCL, UART3_TX, UART1_DE, UART2_DE,	ADC_IN4, COMP_INM, OPAMP1_VINP
11	11	-	-	8	11	PA5	I/O	TC	SPI1_SCK, TIM1_CH2N, TIM1_CH3, SPI1_MOSI, I2C1_SDA,	ADC_IN5, COMP_INM, OPAMP1_VINM
12	12	7	7	9	12	PA6	I/O	TC	EVENT_OUT, SPI1_MISO, TIM3_CH1, TIM1_BKIN2, UART3_TX, I2C2_SCL, COMP_OUT,	ADC_IN6, OPAMP1_VOUT
13	13	8	8	10	13	PA7	I/O	TC	SPI1_MOSI, SPI2_NSS, TIM3_CH2, TIM1_CH1N, UART3_RX, I2C2_SDA,	ADC_IN7, COMP_INP, OPAMP1_VINP OPAMP1_VOUT_R
14	14	9	9	-	-	PB0	I/O	TC	TIM3_CH3, TIM1_CH2N, SPI2_SCK,	ADC_IN8, OPAMP1_VINP
15	15	10	10	11	14	PB1	I/O	TC	TIM3_CH3, TIM3_CH4, TIM1_CH3N, SPI2_MOSI, SPI1_MOSI,	ADC_IN9, OPAMP1_VINM
-	16	-	-	-	-	PB2	I/O	TC	I2C1_SMBA, I2C2_SMBA, TIM3_CH4,	ADC_IN10, OPAMP1_VINM
16	-	21	21	12	-	VSS	S	-	-	VSS
17	17	1	1	13	-	VDD	S	-	-	VDD
18	18	11	11	-	-	PA8	I/O	TC	TIM1_CH1, MCO, SPI2_NSS, UART1_DE, UART2_DE,	COMP_INP, OPAMP3_INP,
19	19	12	12	14	17	PA9	I/O	TC	UART1_TX, TIM1_CH2, I2C1_SCL, I2C2_SCL, SPI2_SCK, UART2_TX, MCO,	COMP_INP, OPAMP3_INM,
20	20	13	13	15	18	PA10	I/O	TC	UART1_RX, TIM1_CH3, I2C1_SDA, I2C2_SDA, SPI2_MISO, UART2_RX,	COMP_INP, OPAMP2_INM，

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21	21	-	-	-	-	PA11	I/O	TC	TIM1_CH4, I2C2_SCL, SPI2_MOSI, TIM1_BKIN3, COMP_OUT,	COMP_INM, OPAMP2_INP,
22	22	-	-	-	-	PA12	I/O	TC	EVENT_OUT, TIM1_ETR, I2C2_SDA, SPI2_MISO, TIM1_BKIN4， COMP_OUT,	COMP_INP,
23	23	14	14	16	19	PA13 (SWDIO)	I/O	TC	SWDIO, UART1_RX, UART2_RX, I2C1_SDA, SPI1_SCK, UART3_RX, TIM3_CH2, TIM4_CH2,	
24	24	15	15	17	20	PA14 (SWCLK)	I/O	TC	UART1_TX, UART2_TX, SWCLK, I2C1_SMBA, SPI1_MISO, UART3_TX, TIM3_CH1, TIM4_CH1,	-
25	25	16	16	-	-	PA15	I/O	TC	SPI1_NSS, UART1_RX, UART2_RX, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N, TIM4_CH1,	-
26	26	17	17	-	-	PB3	I/O	TC	SPI1_SCK, UART3_TX, TIM3_ETR, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N, TIM4_CH2,	-
27	27	18	18	-	-	PB4	I/O	TC	EVENT_OUT, SPI1_MISO, TIM3_CH1, UART3_RX, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N,	-

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28	28	19	-	-	-	PB5	I/O	TC	SPI1_MOSI, I2C1_SMBA, TIM3_CH2, UART3_TX, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N,	-
29	29	20	-	18	-	PB6	I/O	TC	I2C1_SCL, UART1_TX, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N, TIM3_CH3,	-
30	30	-	-	19	-	PB7	I/O	TC	I2C1_SDA, UART1_RX, UART3_RX, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N, TIM3_CH4,	-
31	31	-	19	20	1	BOOT0/PF2	I/O	TC	BOOT0, TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N,	-
-	32	-	-	-	-	PB8	I/O	TC	I2C1_SCL，TIM1_CH1, TIM1_CH1N, TIM1_CH2, TIM1_CH2N, TIM1_CH3, TIM1_CH3N, TIM1_CH4, TIM1_CH4N, TIM3_CH4	
32	-	-	-	-	15	VSS	S	-	-	VSS

1. *I = Input, O = Output, S = Power, HiZ = High Resistance*
2. *TC: Standard 5V I/O, RST: Bi-directional reset pin with embedded weak pull-up resistor.*
3. *This type of multiplexing function can be configured to other pins by software (if the corresponding package model has this pin), please refer to the Multiplexing I/O section and Debug Settings section of the N32G033 series User's Manual for more details.*
4. *Whether used as NRST or regular GPIO, it is recommended to pull up the PF3 pin externally to prevent the MCU from being in a reset state when powered on.*

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4 Electrical characteristics

4.1 Parameter conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions by testing performed on the production line with 100% of the product at an ambient temperature of T_A = 25 ℃.

Data stated in the notes below each table as having been obtained by characterization, design simulation and/or process characterization will not be tested on the production line; on the basis of characterization tests, minimum and maximum values are obtained by taking the average of the sample tests and adding or subtracting three times the standard distribution (mean $\pm 3\Sigma$).

4.1.2 Typical numerical values

Typical data is based on T_A = 25 ℃ and V_{DD} = 3.3V/5.0V (2.0V ≤ VDD ≤ 5.5V voltage range) unless otherwise noted. These data are for design guidance only and have not been tested.

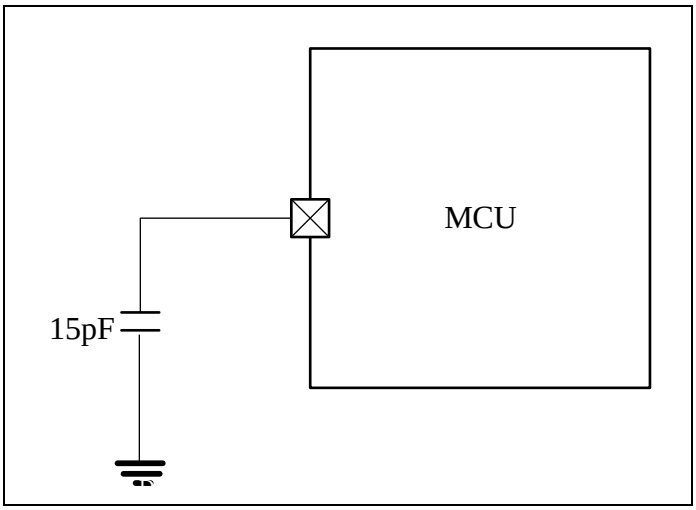
4.1.3 Typical curves

Typical curves are for design guidance only and are untested unless otherwise noted.

4.1.4 Loading capacitor

The load conditions when measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 pin loading conditions



4.1.5 Pin input voltage

The measurement method of the input voltage on the pin is shown in Figure 4-2.

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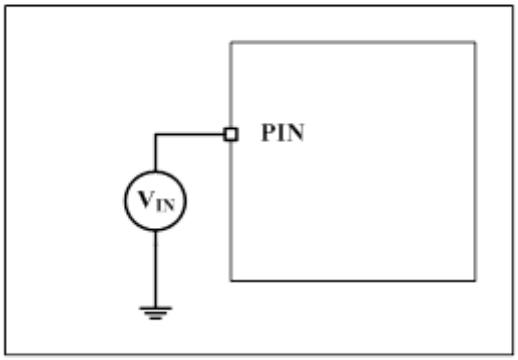
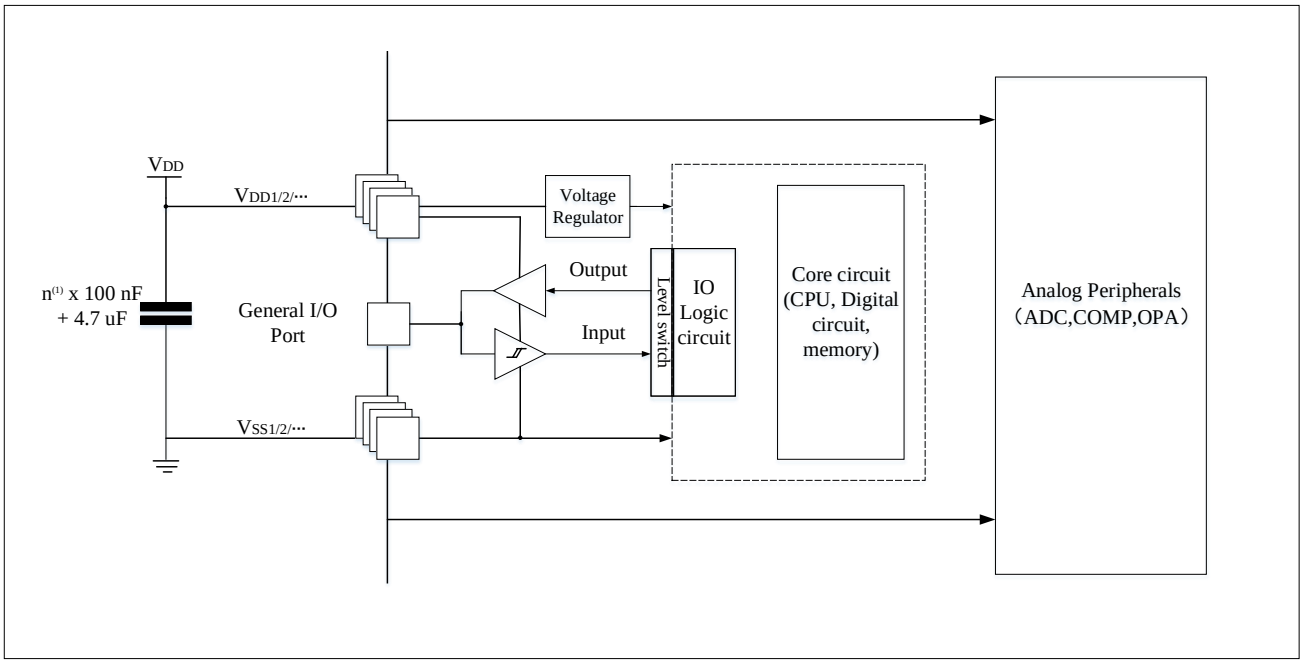
Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

Figure 4-3 Power supply scheme



1. n is the number of VDDs.

Note: Refer to the hardware design guide for capacitor connections

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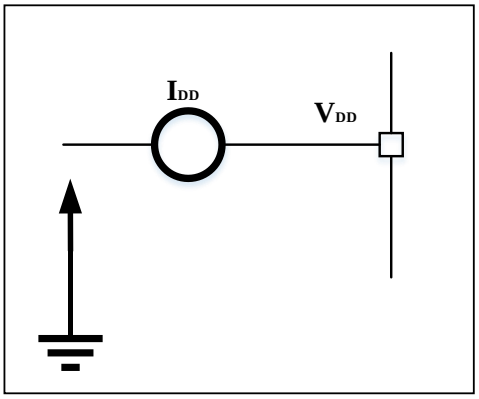
4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement



4.2 Absolute maximum ratings

Loads applied to the device in excess of the values given in the "Absolute Maximum Ratings" list (Table 4-1, Table 4-2, Table 4-3) may cause permanent damage to the device. The maximum loads that can be withstood are given here and do not imply that the functional operation of the device under these conditions is error-free. Prolonged operation of the device under maximum conditions will affect the reliability of the device.

Table 4-1 Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD} - V_{SS}	External mains supply voltage (V_{DD})(1)	-0.3	5.5	V
V_{IN}	Input voltage on arbitrary I/O and control pins(2)	V_{SS}-0.3	5.5	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic Discharge Voltage (Human Body Model)	See section 4.3.9		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external permissible range power supply system.
2. The $I_{INJ\ (PIN)}$ must never exceed its limit, i.e., it is guaranteed that V_{IN} does not exceed its maximum value. If it is not possible to guarantee that V_{IN} does not exceed its maximum value, also ensure that $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. There is a forward injection current when $V_{IN}>V_{DD}$ and a reverse injection current when $V_{IN}<V_{SS}$.

Table 4-2 Current characteristics

Symbol	Parameter	Max	Unit
I_{VDD}	Total current through V_{DD} power line (supply current) (1), test at VDD=5.0V	200	mA
I_{VSS}	Total current through V_{SS} ground (outgoing current) (1) , test at VDD=5.0V	200	
I_{IO}	Output potting current on arbitrary I/O and control pins, test at VDD=5.0V	16	
	Output current on arbitrary I/O and control pins, test at VDD=5.0V	-16	
$I_{INJ(PIN)}$(2)(3)	Injection current at the NRST pin, test at VDD=5.0V	0/-5	
	Injection current on other pins (4) , test at VDD=5.0V	+/-5	
$\sum I_{INJ(PIN)}$(2)	Total injected current on all I/O and control pins (4) , test at VDD=5.0V	+/-16	

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external permissible range of the power supply system.

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2. The $I_{INJ\ (PIN)}$ must never exceed its limit, i.e., it is guaranteed that V_{IN} does not exceed its maximum value. If it is not possible to guarantee that V_{IN} does not exceed its maximum value, also ensure that $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. There is a forward injection current when $V_{IN}>V_{DD}$ and a reverse injection current when $V_{IN}<V_{SS}$.

3. The reverse injection current interferes with the analog performance of the device.

4. When several I/O ports have injected currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the immediate absolute values of the forward injection current and the reverse injection current.

Table 4-3 Temperature characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-40 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	64	MHz
f_{PCLK}	Internal APB clock frequency	-	-	32	
V_{DD}	Standard operating voltage	-	2.0	5.5	V
	Operating voltage when using ADC section	Must be the same as VDD (1)	2.4	5.5	V
	Operating voltage when using OPA (Follow Mode/Single ended PGA Mode)	Must be the same as VDD (1)	2.4	5.5	V
	Operating voltage when using OPA (differential mode)	Must be the same as VDD (1)	2.8	5.5	V
	Working voltage when using COMP section	Must be the same as VDD (1)	2.2	5.5	V
T_A	Ambient Temperature	Suffix version 7	-40	105	℃
T_J	Junction temperature range	Suffix version 7	-40	125	℃

1. Use the same power supply to power VDD and VDDA. During power up and normal operation, a maximum difference of 300mV is allowed between VDD and VDDA.

4.3.2 Operating conditions at power-up and power-down

The parameters given in the following table are based on testing under the ambient temperature listed in Table 4-4.

Table 4-5 Operating conditions at power-up and power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rising time rate	From 0 to V_{DD}	20	∞	μs/V
	V_{DD} falling time rate	From V_{DD} to 0	80	∞	μs/V

4.3.3 Reset and power control module features

The parameters given in the following table are based on tests at ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Reset and power control module features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

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V_{PVD}	Rising	PVD[3:0]=0	Reserve			V
	Falling	PVD[3:0]=0				
	Rising	PVD[3:0]=1	2	2.08	2.16	
	Falling	PVD[3:0]=1	1.9	1.98	2.06	
	Rising	PVD[3:0]=2	2.2	2.28	2.36	
	Falling	PVD[3:0]=2	2.1	2.18	2.26	
	Rising	PVD[3:0]=3	2.4	2.48	2.56	
	Falling	PVD[3:0]=3	2.3	2.38	2.46	
	Rising	PVD[3:0]=4	2.6	2.68	2.76	
	Falling	PVD[3:0]=4	2.5	2.58	2.66	
	Rising	PVD[3:0]=5	2.8	2.88	2.96	
	Falling	PVD[3:0]=5	2.7	2.78	2.86	
	Rising	PVD[3:0]=6	3	3.08	3.16	
	Falling	PVD[3:0]=6	2.9	2.98	3.06	
	Rising	PVD[3:0]=7	3.2	3.28	3.36	
	Falling	PVD[3:0]=7	3.1	3.18	3.26	
	Rising	PVD[3:0]=8	3.4	3.48	3.56	
	Falling	PVD[3:0]=8	3.3	3.38	3.46	
	Rising	PVD[3:0]=9	3.6	3.68	3.76	
	Falling	PVD[3:0]=9	3.5	3.58	3.66	
	Rising	PVD[3:0]=10	3.8	3.88	3.96	
	Falling	PVD[3:0]=10	3.7	3.78	3.86	
	Rising	PVD[3:0]=11	4	4.08	4.16	
	Falling	PVD[3:0]=11	3.9	3.98	4.06	
	Rising	PVD[3:0]=12	4.2	4.28	4.36	
	Falling	PVD[3:0]=12	4.1	4.18	4.26	
	Rising	PVD[3:0]=13	4.4	4.48	4.56	
	Falling	PVD[3:0]=13	4.3	4.38	4.46	
	Rising	PVD[3:0]=14	4.6	4.68	4.76	
	Falling	PVD[3:0]=14	4.5	4.58	4.66	
	Rising	PVD[3:0]=15	4.8	4.88	4.96	
	Falling	PVD[3:0]=15	4.7	4.78	4.86	
$V_{PVDhyst}$(1)	PVD hysteresis	-	80	100	125	mV
$V_{POR/PDR}$	VDD power-up/down reset thresholds	Falling edge	-	1.65	-	V
		Rising edge	-	1.58	-	V
$V_{PDR/PORhyst}$(1)	POR/PDR hysteresis voltage	-	-	100	-	mV
$T_{RSTTEMPO}$(1)	Reset Duration	-	-	150	-	us

1. Guaranteed by design, not tested in production.

4.3.4 Internal reference voltage

The parameters given in the following table are based on tests at ambient temperature and V_{DD} supply voltage listed in Table 4-4.

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Table 4-7 Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REF1.2V}$	Internal reference voltage	-40℃< T_A< +105℃	1.176	1.2	1.224	V
$V_{REF1.8V}$	OPA Buffer output voltage	-40℃< T_A< +105℃	1.764	1.8	1.836	V
$V_{REF3.6V}$	ADC reference voltage	-40℃< T_A< +105℃	3.528	3.6	3.672	V
1/2VDDA	OPA Buffer output voltage	-40℃< TA< +105℃	0.49*VDDA	0.5*VDDA	0.51*VDDA	V
1/4VDDA	OPA Buffer output voltage	-40℃< TA< +105℃	0.245*VDDA	0.25*VDDA	0.255*VDDA	V
$T_{S\_vrefint}$(1)	When reading the internal reference voltage, the sampling time of the ADC	PLS[2:0]=001 (Rising edge) f_{ADC_CLK}=32M	16(2)	-	-	μs

1. The shortest sampling time is obtained by multiple cycles in the application.
2. Converted to ADC sampling period of 512 cycles.
3. Production calibration accuracy, excluding welding effects. The impact range of voltage deviation caused by welding is about ± 1%.

4.3.5 Power supply current characteristics

Current consumption is a combination of a number of parameters and factors that include operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, flip-flop rate of I/O pins, location of the program in memory, and code executed.

The current consumption measurements are described in detail in Figure 4-4.

All current consumption measurements given in this section for all modes of operation execute a condensed set of code.

4.3.5.1 Maximum current consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.
- Flash memory access time is adjusted to the frequency of f_{HCLK} (0 wait cycles for 0 < SYSCLK≤32MHz, and 1 wait cycles for 32MHz < SYSCLK≤64MHz).
- When peripheral is turned on: $f_{PCLK} = f_{HCLK}/2$.
- V_{DD} = 5.5V, ambient temperature equal to 105 ℃.

The parameters given in Table 4-8 is based on tests at ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-8 Typical current consumption in run mode with data processing code running from internal flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1)	Unit
				VDD=5.5V,T_A = 105℃	
I_{DD}	Supply current in operation mode	Internal clock. Enable all peripherals	64MHz	7.7	mA
			32MHz	4.4	
			16MHz	2.9	
			8MHz	2.2	
		Internal clock. Turn off all peripherals	64MHz	4.6	
			32MHz	2.85	
			16MHz	2.1	
			8MHz	1.7	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

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4.3.5.2 Typical current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level-V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.
- Flash memory access time is adjusted to the frequency of f_{HCLK} (0 wait cycles for 0 < SYSCLK≤32MHz, and 1 wait cycles for 32MHz < SYSCLK≤64MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-4.
- Instruction prefetch is on (Hint: This parameter must be set before setting the clock and bus divider).
- When the peripheral is turned on: $f_{PCLK} = f_{HCLK}/2$.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-9 Typical current consumption in run mode with data processing code running from internal flash memory (T_A=25 ℃, V_{DD}=5.0V)

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Enable all peripherals	Turn off all peripherals	
I_{DD}	Supply current in operation mode	Internal high-speed clock	64MHz	7.6	4.5	mA
			32MHz	4.3	2.8	
			16MHz	2.9	2.0	
			8MHz	2.1	1.7	

Table 4-10 Typical current consumption in run mode with data processing code running from internal flash memory (T_A=25℃、V_{DD}=3.3V)

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Enable all peripherals	Turn off all peripherals	
I_{DD}	Supply current in operation mode	Internal high-speed clock	64MHz	7.4	4.4	mA
			32MHz	4.25	2.7	
			16MHz	2.8	1.95	
			8MHz	2.05	1.58	

4.3.5.3 Low Power Current Consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VDD or VSS (no load).
- All peripherals are off unless otherwise noted.

Table 4-11 Typical consumption in stop and power-down mode (T_A=25℃、V_{DD}=3.3V)

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD_STOP}	Current in STOP mode	SRAM hold, all I/O status hold, BS TIM, independent watchdog off	1.81	-	uA

Table 4-12 Typical consumption in stop and power-down mode (T_A=25℃、V_{DD}=5.0V)

Symbol	Parameter	Conditions	Typ	Max	Unit

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I_{DD_STOP}	Current in STOP mode	SRAM hold, all I/O status hold, BS TIM, independent watchdog off	2.05	-	uA

4.3.6 Internal clock source characteristics

The characteristics given in the following table were measured using ambient temperatures and supply voltages in accordance with Table 4-4.

4.3.6.1 High-speed internal (HSI) RC oscillator

Table 4-13 HSI Oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	频率	VDD=5.0V，T_A = 25℃	-0.5(3)	64MHz	0.5(3)	%
ACC_{HSI}	HSI振荡器的频率(4)	VDD=2.0~5.5V，T_A = -40~105℃	-2(4)	64MHz	1.5(4)	%
		VDD=5.0V，T_A = 0~85℃	-1(4)	64MHz	1 (4)	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	-	10	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	400	600	μA

1. V_{DD} = 5.0V, T_A = -40 to 105 ℃ unless otherwise noted.
2. Guaranteed by design, not tested in production.
3. Production calibration accuracy, not including soldering effects. Frequency deviation due to soldering ranges from approximately ±1%.
4. Frequency deviation including soldering effects, data from sample testing, not tested in production.

4.3.6.2 Low-speed internal (LSI) RC oscillator

Table 4-14 LSI Oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	output frequency	VDD=5.0V，T_A = 25℃	-1	32KHz	+1	%
		VDD =2.0V ~5.5V, TA = -40~105℃	-5	32KHz	+5	%
$t_{SU(LSI)}$ (2)	LSI Oscillator Startup Time	TA = 25℃	-	30	80	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	TA = 25℃	-	0.3	-	μA

1. V_{DD} = 5.0V, T_A = -40 to 105 ℃ unless otherwise noted.
2. Guaranteed by design, not tested in production.

4.3.7 Low-power mode wake-up time

The wake-up times listed in Table 4-15 were measured during the wake-up phase of an 64MHz HSI RC oscillator. The clock source used for wake-up depends on the current operating mode:

- STOP mode: the clock source is the RC oscillator

All times are measured using the ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-15 Low-power mode wake-up time

Symbol	Parameter	Typ	Max	Unit
t_{WUSTOP}(1)	Wake up from STOP mode, VDD=VDDA=5V @ 25 °C, LSI turned on	35(1)	45	us

1. Wake-up time is measured from the start of the wake-up event until the user program reads the first instruction.

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4.3.8 FLASH characteristics

All characterization parameters were obtained at TA = -40~105 ℃ unless otherwise stated.

Table 4-16 FLASH characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
t_{PROG}	32-bit programming time	T_A = -40~105℃	-	75	-	μs
t_{ERASE}	Page (512 bytes) erase time	T_A = -40~105℃	-	2.5	-	ms
t_{ME}	Mass erase time	T_A = -40~105℃	-	35	-	ms
I_{DD}	Supply current (1)	Reading mode, f_{HCLK}=64MHz, V_{DD}=5.0V	-	4.5	6.0	mA
		Write mode, f_{HCLK}=64MHz, V_{DD}=5.0V	-	-	2	mA
		Erase mode, f_{HCLK}=64MHz, V_{DD}=5.0V	-	-	1.5	mA
		PD/STOP mode, V_{DD}=2.0~5.0V	-	0.3	15(2)	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Tested at T_A = 85 ℃.

Table 4-17 Flash memory life and data retention period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40~105 ℃	100	kcycles
t_{RET}	Data retention	T_A = 105 ℃, after 1000 erasing cycle(1)	10	years

1. Derived from characterization tests, not tested in production.

4.3.9 Absolute maximum value (electrical sensitivity)

Based on three different tests (ESD, LU), the chip is tested for strength to determine its performance in terms of electrical sensitivity, using specific measurement methods.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) was applied to all pins of all samples.

Table 4-18 ESD Absolute Maximum

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)(2)	T_A = +25 ℃, Complies with MIL-STD-883K Method 3015.9.	3A	±4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A = +25 ℃, Complies with ESDA/JEDEC JS-002-2018	C3	±2000	
V_{FESD}(3)	Voltage limitation applied to any I/O pin other than the power supply to cause functional interference	T_A=+25 °C, VDD=5.0V, HCLK=64MHz, compliant with lEC 61000-4-2	-	±1500	
	Voltage limitation applied to VDD/VSS pins to cause functional interference	T_A=+25 °C, VDD=5.0V, HCLK=64MHz, compliant with lEC 61000-4-2	-	±11000	
V_{EFTB}	Apply fast transient voltage burst restrictions on any I/O pin except for the power supply to cause functional interference	T_A=+25 °C, VDD=5.0V, HCLK=64MHz, compliant with lEC 61000-4-4	4A	±2000	
	Apply fast transient voltage burst limitation on VDD/VSS pins to cause	T_A=+25 °C, VDD=5.0V, HCLK=64MHz, compliant with lEC		±4000	

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	functional interference	61000-4-4			

1. Derived from characterization tests, not tested in production.
2. Test all pins except NRST. Please refer to the ESD-HBM test report for specific test results.
3. Chip level testing

Static latch-up

To evaluate latch-up performance, 2 complementary static latch-up tests on 6 samples are required:

- For each power supply pin, provide a supply voltage that exceeds the limit.
- Injects current on each input, output, and configurable I/O pin.

This test complies with the EIA/JESD78F IC bolting standard.

Table 4-19 Electrical sensitivity

Symbol	Parameter	Conditions	Maximum current
LU	Static latch-up	T_A = +125 ℃, complies with JESD78F standard	±300mA

4.3.10 I/O port characteristics

Generalized Input/Output Characteristics

Unless otherwise noted, the parameters listed in the following table were measured under the conditions of Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-20 I/O static characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
V_{IL}	Input Low Level Voltage	5	-	-	0.3×VDD	V
		3.3	-	-	0.8	
		2.0	-	-	0.2×VDD	
V_{IH}	Input High Level Voltage	5	-	0.7×VDD	-	
		3.3	-	2.15	-	
		2.0	-	0.8×VDD	-	
V_{hys}	Schmitt trigger voltage hysteresis(1)	5/3.3/2.0	-	0.1×VDD	-	V
I_{lkg}(2)	Input leakage current IIH	5/3.3/2.0	-	-	1	μA
	Input leakage current IIL	5/3.3/2.0	-	-1	-	
V_{OH}(3)	Output high level voltage	5	High driving Imin=16mA low driving Imin=12mA	VDD-0.8	-	V
		3.3	High driving Imin=8mA low driving Imin=4mA	2.4	-	
		2.0	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	-	
V_{OL}(3)	Output Low Voltage	5	High driving Imin=16mA low driving Imin=8mA	-	0.7	
		3.3	High driving Imin=8mA low driving Imin=4mA	-	0.45	
		2.0	High driving Imin=4mA low driving Imin=2mA	-	0.4	
R_{PU}	Weak pull-up equivalent resistance	5/3.3/2.0	-	40	100	kΩ
R_{PD}	Weak pull-down equivalent resistance	5/3.3/2.0	-	40	120	kΩ
C_{IO}	Capacitance of I/O pins	5/3.3/2.0	-	-	10	pF

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1. Hysteresis voltage for Schmitt trigger switching levels. Guaranteed by characterization tests, not tested in production.
2. Leakage current may be higher than maximum if there is reverse current back-up at adjacent pins.
3. PB3/PB4/PB5, which only serve as SPI functions, support driver capability switching.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their characteristics take into account most stringent CMOS process or TTL parameters:

Input and output AC characteristics

The definitions and values of the input and output AC characteristics are given in Table 4-4.

Unless otherwise stated, the parameters are measured using ambient temperatures and supply voltages in accordance with Table 4-4.

Table 4-21 PB3/4/5 AC Characteristics(1)

VDD	条件			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
5V(4.5~5.5)	Low (DR=1)	Slow (SR=1)	15	1.375	2.028	3.201	3.338	4.88	7.97
		Fast (SR=0)	15	1.103	1.658	2.65	2.846	4.187	6.92
	High (DR=0)	Slow (SR=1)	15	1.117	1.64	2.582	2.97	4.379	7.275
		Fast (SR=0)	15	0.86	1.29	2.05	2.7	4	6.6
3.3V(2.7~3.6)	Low (DR=1)	Slow (SR=1)	15	1.766	2.725	4.471	3.943	6.041	9.839
		Fast (SR=0)	15	1.446	2.261	3.731	3.429	5.263	8.577
	High (DR=0)	Slow (SR=1)	15	1.425	2.193	3.596	3.539	5.456	8.98
		Fast (SR=0)	15	1.125	1.755	2.899	3.257	4.996	8.127
2V(1.8~2.2)	Low (DR=1)	Slow (SR=1)	15	2.691	4.503	8.067	6.312	10.64	18.79
		Fast (SR=0)	15	2.242	3.803	6.996	5.451	9.177	16.14
	High (DR=0)	Slow (SR=1)	15	2.161	3.611	6.395	5.816	9.829	6.395
		Fast (SR=0)	15	1.739	2.943	5.261	5.188	8.726	15.3

1. Guaranteed by design, not tested in production

Table 4-22 Others pins(1) AC Characteristics(2)

VDD	条件			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
5V(4.5~5.5)	Low (DR=0)	Slow (SR=0)	15	1.322	1.938	3.192	3.012	4.54	7.601
3.3V(2.7~3.6)	Low (DR=0)	Slow (SR=0)	15	1.693	2.602	4.465	3.92	6.161	10.6
2V(1.8~2.2)	Low (DR=0)	Slow (SR=0)	15	2.597	4.339	8.147	6.627	11.52	21.38

1. Pins other than PB3/4/5.
2. Guaranteed by design, not tested in production.

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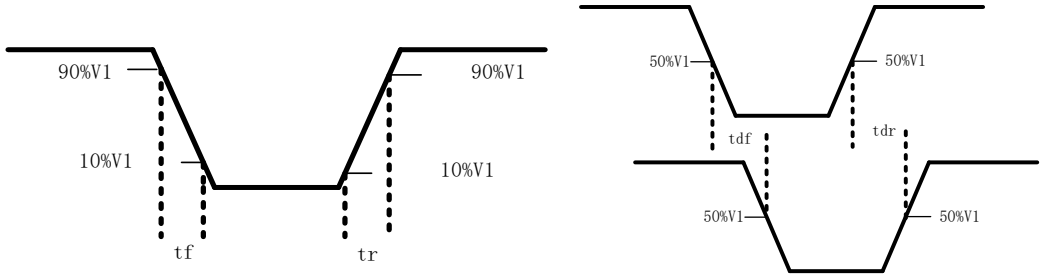
Figure 4-7 I/O AC characteristic definition



4.3.11 NRST pin characteristics

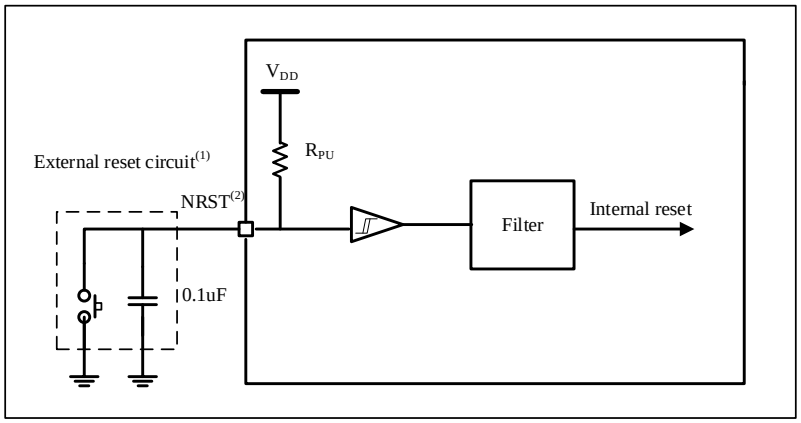
The NRST pin has an internal integrated pull-up resistor, and the parameters are measured using ambient temperature and supply voltage in accordance with Table 4-4, unless otherwise noted.

Table 4-23 NRST pin characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	2.0V~5.5V	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST input high voltage	2.0V~5.5V	0.7VDD	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	2.0V~5.5V	139	315	367	mV
R_{PU}	Weak pull-up equivalent resistance (2)	2.0V~5.5V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	2.0V~2.2V	-	-	203	ns
		3V~3.6V	-	-	119	
		4.5V~5.5V	-	-	83	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	2.0V~2.2V	490	-	-	ns
		3V~3.6V	301	-	-	
		4.5V~5.5V	199	-	-	

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a real resistor in series with a non-switchable PMOS implementation. The resistance of this PMOS switch is very small (about 10%).

Figure 4-8 Recommended NRST Pin Protection



1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin can be below the maximum VIL(NRST), otherwise the MCU cannot get reset.

4.3.12 TIM characteristics

The parameters listed are guaranteed by design

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Table 4-24 TIM characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer distinguishes time	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency for CH1 to CH4	-	0	$f_{TIMCLK}/2$	MHz
		f_{TIMCLK} = 64MHz	0	32	MHz
Res_{TIM}	TIM1/3: Timer Resolution	-	-	16	bits
	TIM4/6: Timer Resolution		-	32	bits
$t_{COUNTER}$	TIM1/3：16 bit counter	-	1	2^16	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	-	1024	μs
	TIM4：32 bit counter	-	1	2^32	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	-	67.109	s
	TIM6：32 bit counter	-	1	2^32	t_{TIMCLK}
		f_{TIMCLK} = 32MHz	-	134.218	s
t_{MAX_COUNT}(1)	TIM1/3：16 bit counter	-	1	2^32	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	-	67.109	s
	TIM4：32 bit counter	-	1	2^48	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	-	1221.68	h
	TIM6：32 bit counter	-	1	2^48	t_{TIMCLK}
		f_{TIMCLK} = 32MHz	-	2443.36	h

1. Refers to the maximum count that can be completed after dividing the TIM internally.

4.3.13 IWDG characteristics

Table 4-25 IWDG Maximum and minimum count reset times (LSI = 32KHz)

Prescaler divider	IWDG_PREDIV.PD[2:0]	Min(1) IWDG_RELV.REL[13:0]=0	Max(1) IWDG_RELV.REL[13:0]=0x3FFF	Unit
/4	000	0.125	2048	ms
/8	001	0.25	4096	
/16	010	0.5	8192	
/32	011	1	16384	
/64	100	2	32768	
/128	101	4	65536	
/256	11x	8	131072	

1. Guaranteed by design, not tested in production。

4.3.14 I2C characteristics

Unless otherwise specified, parameters are measured using ambient temperature, f_{PCLK} frequency and V_{DD} supply voltage in accordance with Table 4-4.

The I2C interface of the N32G033 products conforms to the standard I2C communication protocol with the following limitation: SDA and SCL are not "true" open-drain pins, and when configured as open-drain outputs, the PMOS tubes between the pin and VDD are turned off but still present.

The I2C interface characteristics are shown in the table below, and see Section 4.3.12 for details on the characteristics of the input/output multiplexing pins (SDA and SCL).

Table 4-26 I2C interface characteristics

Symbol	Parameter	Standard model		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	

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f_{SCL}	I2C Interface Frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.50	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{su(STA)}$	Repeat Start Condition Establishment Time	4.7	-	0.6	0.6	0.26	-	µs
$t_{h(SDA)}$	SDA data hold time	-	3.4	-	0.9	-	0.41	µs
$t_{su(SDA)}$	SDA build-up time	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1 C_b	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20+0.1 C_b	300	-	120	ns
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Stop condition to start condition time (bus idle)	4.7	-	1.3	-	0.50	-	µs
C_b	Capacitive load per bus	-	400	-	400	-	200	pf
t_{SP}	Spike pulse width suppressed by analog filter in standard and fast mode	-	-	0	50	0	50	ns
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	µs
$t_{v\,(ACK)}$	Answer validity time	-	3.45	-	0.9	-	0.45	µs

1. Guaranteed by design, not tested in production.
2. f_{PCLK} must be greater than 2MHz to achieve maximum frequency for standard mode I2C. f_{PCLK} must be greater than 4MHz to achieve maximum frequency for fast mode I2C.

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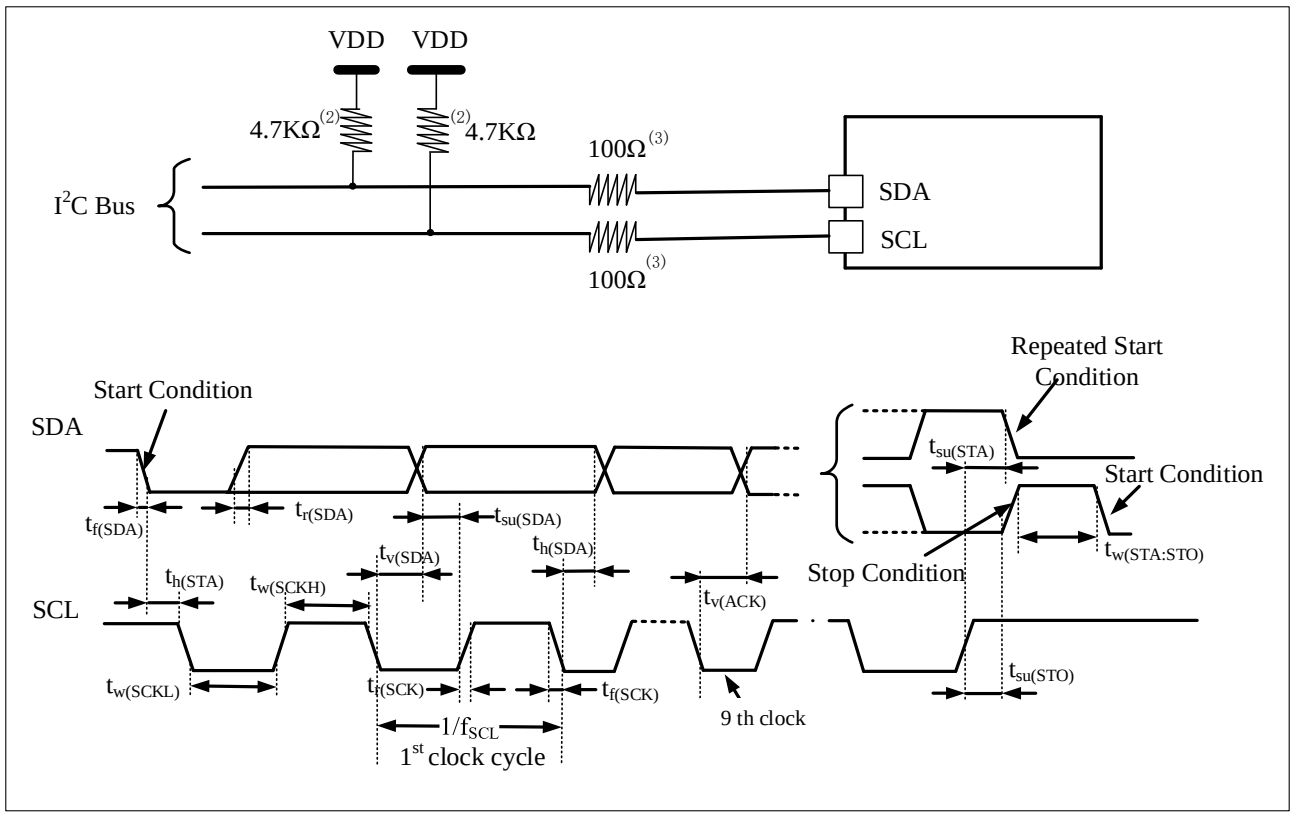
Figure 4-9 I2C bus AC waveform and measurement circuit (1)



1. The measurement points are set at $0.3V_{DD}$ and $0.7V_{DD}$.
2. Pull-up resistor resistance value depends on I2C interface speed.
3. The resistance value depends on the actual electrical characteristics. It is possible to leave the serial resistor unconnected and connect the signal line directly.

4.3.15 SPI characteristics

Unless otherwise noted, SPI parameters are measured using ambient temperature, f_{PCLK} frequency, and V_{DD} supply voltage conforming to the conditions in Table 4-4.

For details on the characteristics of the input-output multiplexing function pins (NSS, SCLK, MOSI, MISO of SPI), see Section 4.3.12.

Table 4-27 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI Clock Frequency	Master Mode	-	16	MHz
		Slave Mode	-	16	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall times	load capacitance ： C = 15pF	-	3	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI Slave Mode	45	55	%
$t_{su(NSS)}$ (1)	NSS Establishment Time	Slave Mode	$1t_{SYSCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS Hold Time	Slave Mode	$1t_{SYSCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master Mode	$t_{PCLK/BR}$-3	$t_{PCLK/BR}$+ 3	ns
$t_{su(MI)}$(1)	Data Input Establishment Time	Master Mode	4	-	ns

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$t_{su(SI)}^{(1)}$		Slave Mode	5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master Mode	4	-	ns
$t_{h(SI)}^{(1)}$		Slave Mode	5	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave Mode， f_{PCLK} = 20MHz	0	100	ns
$t_{dis(SO)}^{(1)(3)}$	Data output disable time	Slave Mode	2	24	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave Mode(After enabling edge)	-	28	ns
$t_{v(MO)}^{(1)}$		Master Mode(After enabling edge)	-	15	
$t_{h(SO)}^{(1)}$	Data output hold time	Slave Mode(After enabling edge)	6	-	ns
$t_{h(MO)}^{(1)}$		Master Mode(After enabling edge)	0	-	

1. Evaluated from a combination of VDD=3.3V/5V, load capacitance C=15pF, not tested in production.
2. Minimum value indicates the minimum time to drive the output, maximum value indicates the maximum time to get the data correctly.
3. Minimum value indicates the minimum time to turn off the output, maximum value indicates the maximum time to place the data line in a high resistance state.

Figure 4-5 SPI sequence diagram - slave mode and CPHA=0

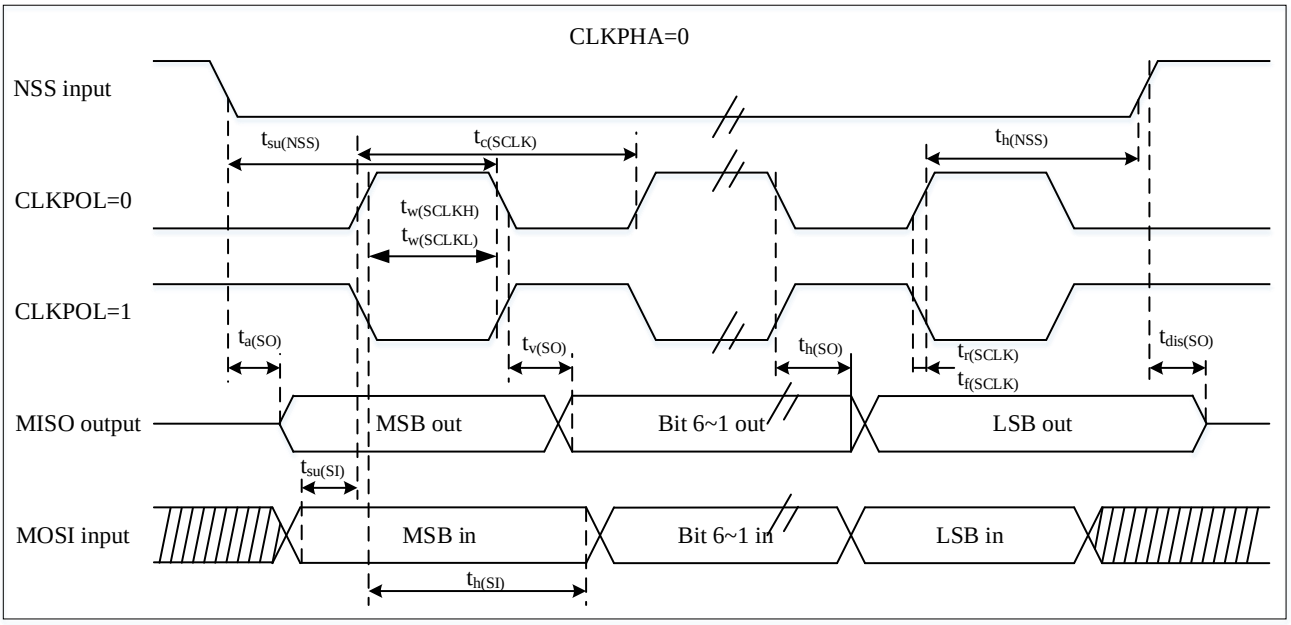

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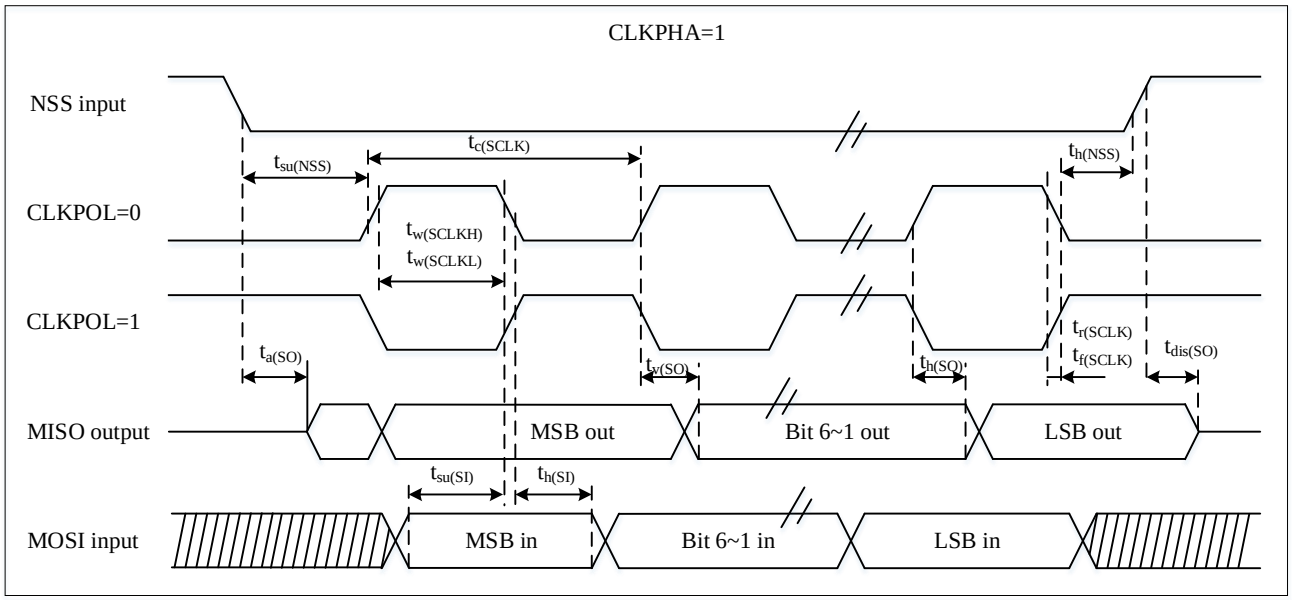
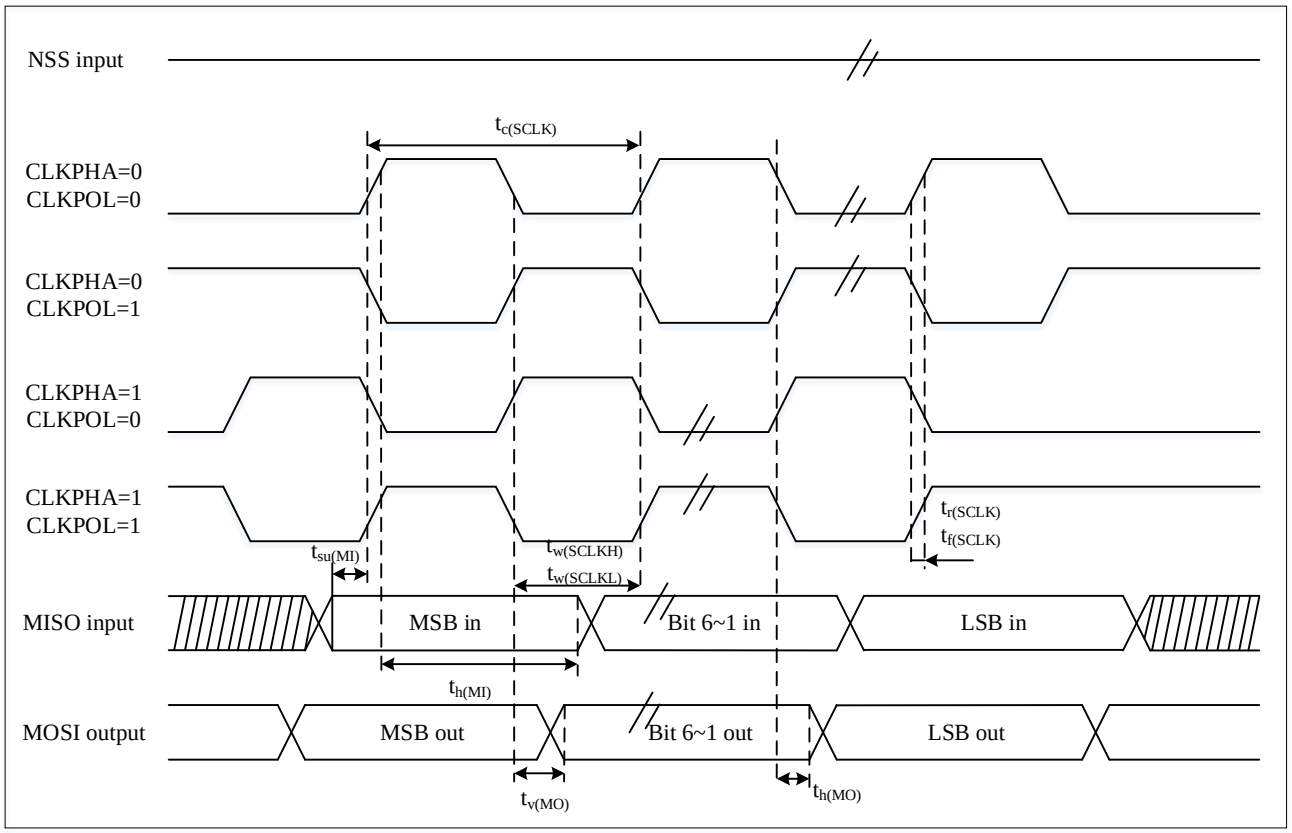
Figure 4-6 SPI sequence diagram - slave mode and CPHA=1(1)



1. The measurement points were set at the CMOS level of 0.3 V_{DD} and 0.7 V_{DD}.

Figure 4-7 SPI timing diagram-master mode (1)



1. The measurement points are set at CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

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4.3.16 12-bit ADC characteristics

Unless otherwise noted, the parameters of Table 4-4 are measured using an ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage that meet the conditions of Table 4-4.

Table 4-28 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}(1)	Supply Voltage	-	2.4(2)	-	5.5	V
V_{REF+}	Positive Reference Voltage	-	V_{DD}			V
f_{ADC}	ADC Clock Frequency	-	-	-	32	MHz
f_s(1)	Sampling Rate	-	0.03	-	1	Msps
V_{AIN}	Conversion Voltage Range	-	0 (VSSA or VREF- connected to ground)	-	V_{REF+}	V
R_{AIN}(1)	External Input Impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC Input Resistance	VDD=3.3V	-	1000.6	-	Ω
		VDD=5.0V	-	688.38		Ω
C_{ADC}(1)	Internal sample and hold capacitance	-	-	13	-	pF
SNDR	Signal-to-noise distortion	VDD=3.3V	-	63.4	-	dB
		VDD=5.0V	-	63.76	-	dB
T_S(1)	Number of Sampling Cycles	-	4	-	-	$1/f_{ADC}$
t_{STAB}(1)	Power-up time	-	48	-	-	$1/f_{ADC}$
t_{CONV}(1)	Conversion time	-	12			$1/f_{ADC}$
I_{ADC}	ADC current consumption	-	-	1.56	-	mA

1. Guaranteed by design, not tested in production.
2. ADC performance metrics degrade with 2.4V supply

Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above equation (Equation 1) is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. where N=12 (indicating 12-bit resolution).

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Table 4-29 ADC sampling time (1)

Resolution	Sample cycle@16M	Sampling Rate (MHz)	Minimum sampling time（ns）	Rin（kΩ）
12-bit	4	1.000	250	0.9
	6	0.889	375	1.9
	14	0.615	875	5.9
	20	0.500	1250	8.8
	30	0.381	1875	13.8
	42	0.296	2625	19.7
	56	0.235	3500	26.7
	72	0.190	4500	34.6
	88	0.160	5500	42.5
	120	0.121	7500	58.4
	182	0.082	11375	89.1
	240	0.063	15000	117.8
	300	0.051	18750	147.6
	400	0.039	25000	197.1
	480	0.033	30000	236.7
	600	0.026	37500	296.2
Resolution	Sample cycle@32M	Sampling Rate (MHz)	Minimum sampling time（ns）	Rin（kΩ）
12-bit	20	1.00	625	3.9
	30	0.76	937.5	6.4
	42	0.59	1312.5	9.3
	56	0.47	1750	12.8
	72	0.38	2250	16.8
	88	0.32	2750	20.7
	120	0.24	3750	28.7
	182	0.16	5687.5	44.0
	240	0.13	7500	58.4
	300	0.10	9375	73.2
	400	0.08	12500	98.0
	480	0.07	15000	117.8
	600	0.05	18750	147.6

1. Guaranteed by design, not tested in production.

Table 4-30 ADC accuracy (1)

Symbol	Parameter	Conditions	Typ	Max(2)	Unit
EO	Offset Error	f_{ADC} = 32 MHz, Sample rate=1M sps, V_{DDA} = 3.3V, T_A = 25 ℃	±2	-	LSB
ED	Differential Linearity Error		±0.6	2.85	
EL	Integral Linearity Error		±1.5	1.58	
EO	Offset Error	f_{ADC} = 32MHz, Sample rate=1M sps, V_{DDA} = 5.0V, T_A = 25 ℃	±2	-	
ED	Differential Linear Error		±0.6	3.25	
EL	Integral Linear Error		±1.5	1.98	
ENOB	Effective number of bits	f_{HCLK} = 64MHz, f_{ADC} = 32 MHz，sample rate=1M sps, T_A = 25 ℃	10.15	-	Bits

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1. ADC Accuracy vs. Reverse Current Injection: Reverse current injection on any standard analog input pin needs to be avoided, as it can significantly degrade the accuracy of a conversion being performed on another analog input pin. It is recommended that a Schottky diode be added to the standard analog pin (between the pin and ground) where the reverse injection current may be generated.
2. Guaranteed by characterization tests, not tested in production.

Figure 4-8 ADC Accuracy Characteristics

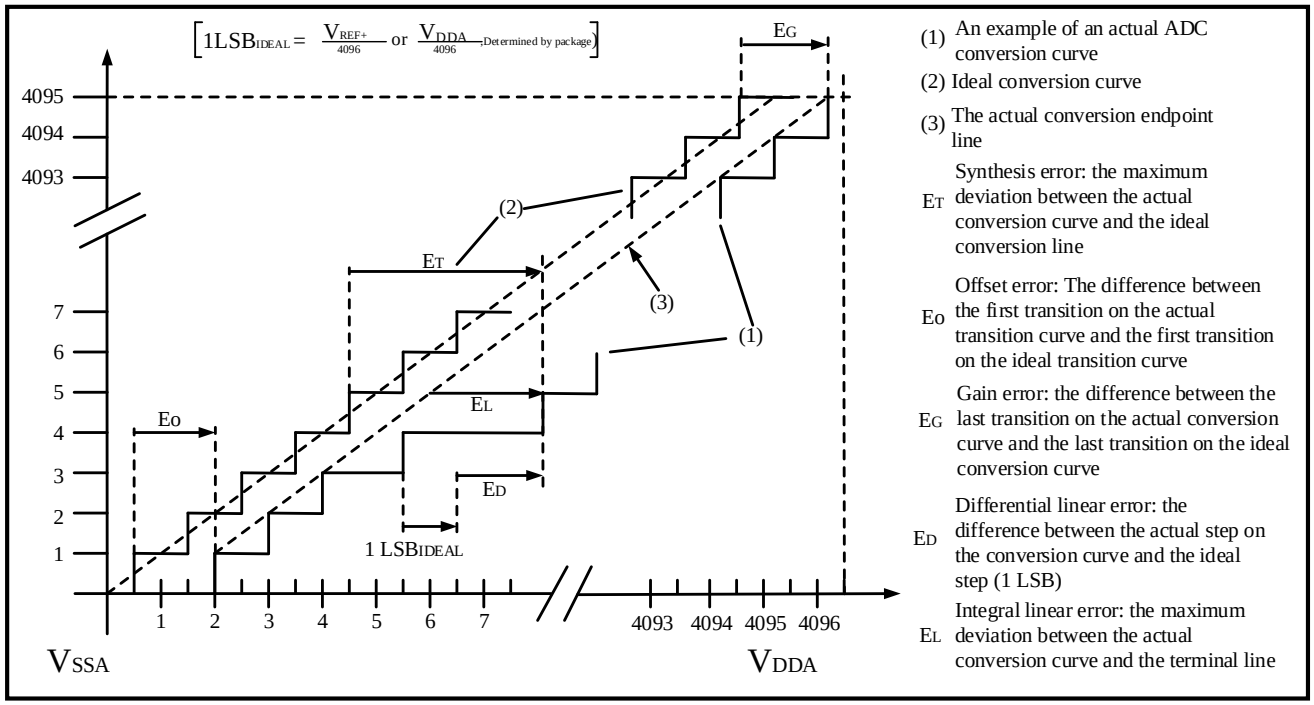
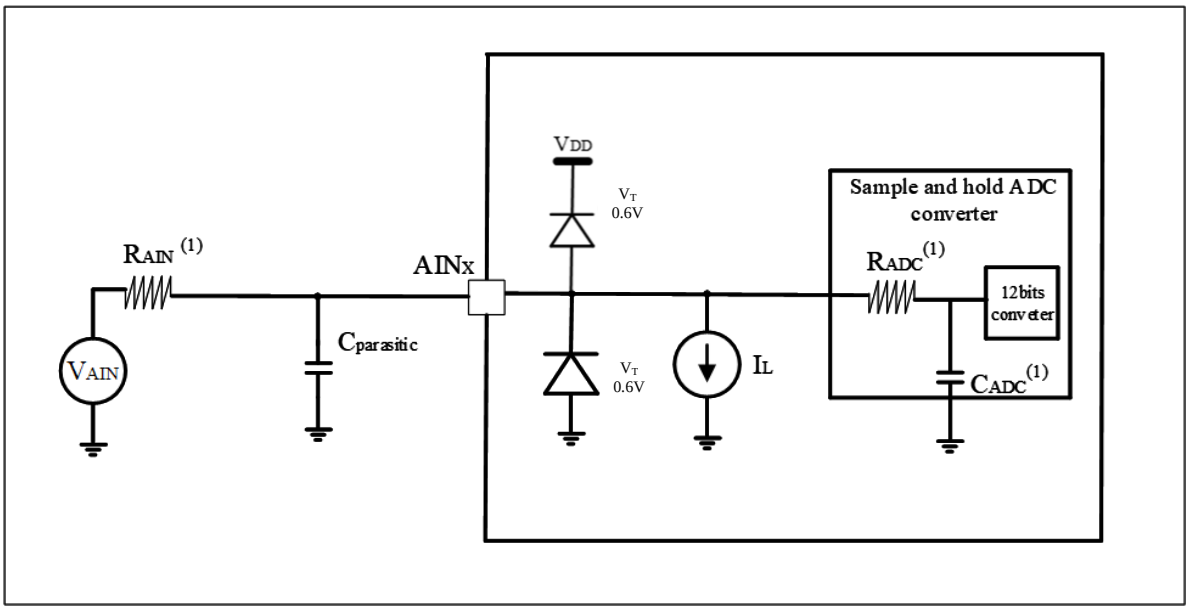


Figure 4-9 ADC typical connection diagram



1. See Table 4-28 for R_{AIN}, R_{ADC}, and C_{ADC} values.
2. Cparasitic represents the parasitic capacitance (approximately 7pF) on the PCB (related to soldering and PCB layout quality) and pads. Larger values of Cparasitic will reduce the accuracy of the conversion and the solution is to reduce the f_{ADC}.

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4.3.17 Built in Reference Source (V_{REFP}) characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-31 V_{REFP} characteristics(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	normal mode	4	-	5.5	V
V_{REFP}	Reference voltage output	Normal mode at 25℃	3.528(2)	3.6	3.672(2)	V
I_{DDA}(1)	Consumption from VDDA	Iload = 0 μA	-	800	-	μA
Load cap(1)	Load Capacitance	-	-	-	20	pF
t_{START}(1)	Startup time	-	-	-	5	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Production calibration accuracy, excluding welding effects. The impact range of voltage deviation caused by welding is about ± 1%.
3. Only supports application scenarios under 5V.

4.3.18 Operational amplifier (OPAMP) characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-32 OPAMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	analog supply voltage	Follow mode/Single ended PGA mode	2.4	-	5.5	V
		Differential mode	2.8	-	5.5	V
CMIR	Common mode voltage input range	-	0	-	VDDA	V
VIOFFSET	input offset voltage	-	-10	4	10	mV
ILOAD	drive current	-	-	0.5	-	mA
IDDA	Current consumption of operational amplifier	No load, quiescent mode	-	0.5	-	mA
CMMR	Common Mode Rejection Ratio	-	-	110	-	dB
PSRR	Power Supply Rejection Ratio	-	-	102	-	dB
GBW	gain bandwidth	-	-	5.5	-	MHz
SR	Slew rate	VDD=5.0V		6.16	-	V/us
		VDD=3.3V		5.68	-	V/us
RLOAD	Minimum impedance load	-	10	-	-	KΩ
CLOAD	Maximum capacitive load	-	-	-	25	pF
TSTARTUP	Start establishment time	CLOAD ≤ 25 pf, RLOAD ≥ 10 kΩ, Follower configuration	-	1.75	3	μs
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 25pF, Rload = 10 KΩ	-	1	-	MHz
		GA Gain = 4, Cload = 25pF, Rload = 10 KΩ	-	0.5	-	

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		GA Gain = 16, Cload = 25pF, Rload = 10 KΩ	-	0.125	-	
		GA Gain = 32, Cload = 25pF, Rload = 10 KΩ	-	0.0625	-	
Single PGA Gain error (opa1)	Programmable gain error	Input signal amplitude>100mV		+/-2		%

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.19 COMP characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-33 COMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Analog supply voltage	normal mode	2.2	3.3	5.5	V
V_{IN}	Input Voltage Range	VIN	0	-	VDD	
t_{START}(1)	Comparator start-up build-up time	Normal mode	-	-	1.7	us
		Low power mode	-	-	12	
t_d	Propagation delay for 200mV step with 100mV overdrive	Normal mode	-	100	-	ns
		Low power mode	-	500	-	
V_{OFFSET}	Comparator Input Offset Error	Full common mode range	-	±5	±20	mV
V_{hys}	Comparison Hysteresis Voltage (High speed)	No hysteresis	-	0	-	mV
		Low hysteresis	-	12	-	
		Medium hysteresis	-	31	-	
		High hysteresis	-	52	-	
	Comparison Hysteresis Voltage (Low power)	No hysteresis	-	0	-	
		Low hysteresis	-	10	-	
		Medium hysteresis	-	25	-	
		High hysteresis	-	41	-	
I_{DD}	Comparator Current Consumption (High speed)	Static	-	38.4	-	µA
		cmp With 50 kHz ±100 mV overdrive square signal	-	43	-	
		cmp static with 1* 6bit dac on	-	74	-	
I_{DD}	Comparator Current Consumption (Low power)	Static	-	6.1	-	µA
		cmp With 50 kHz ±100 mV overdrive square signal	-	6.7	-	µA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.20 Temperature sensor characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage that meet the conditions of Table 4-4.

Table 4-34 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with respect to temperature	-	±1	±5	℃
Avg_Slope(1)	Average Slope	-3.7	-4.07	-4.3	mV/℃
V_{25}(1)	Voltage at 25℃	-	1.247	-	V

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t_{START}(1)	Build-up time	4	-	10	μs
T_{S_temp}(2)(3)	ADC sampling time when reading temperature	8.2	-	17.1	μs

1. Guaranteed by characterization test results, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application program through multiple cycles.

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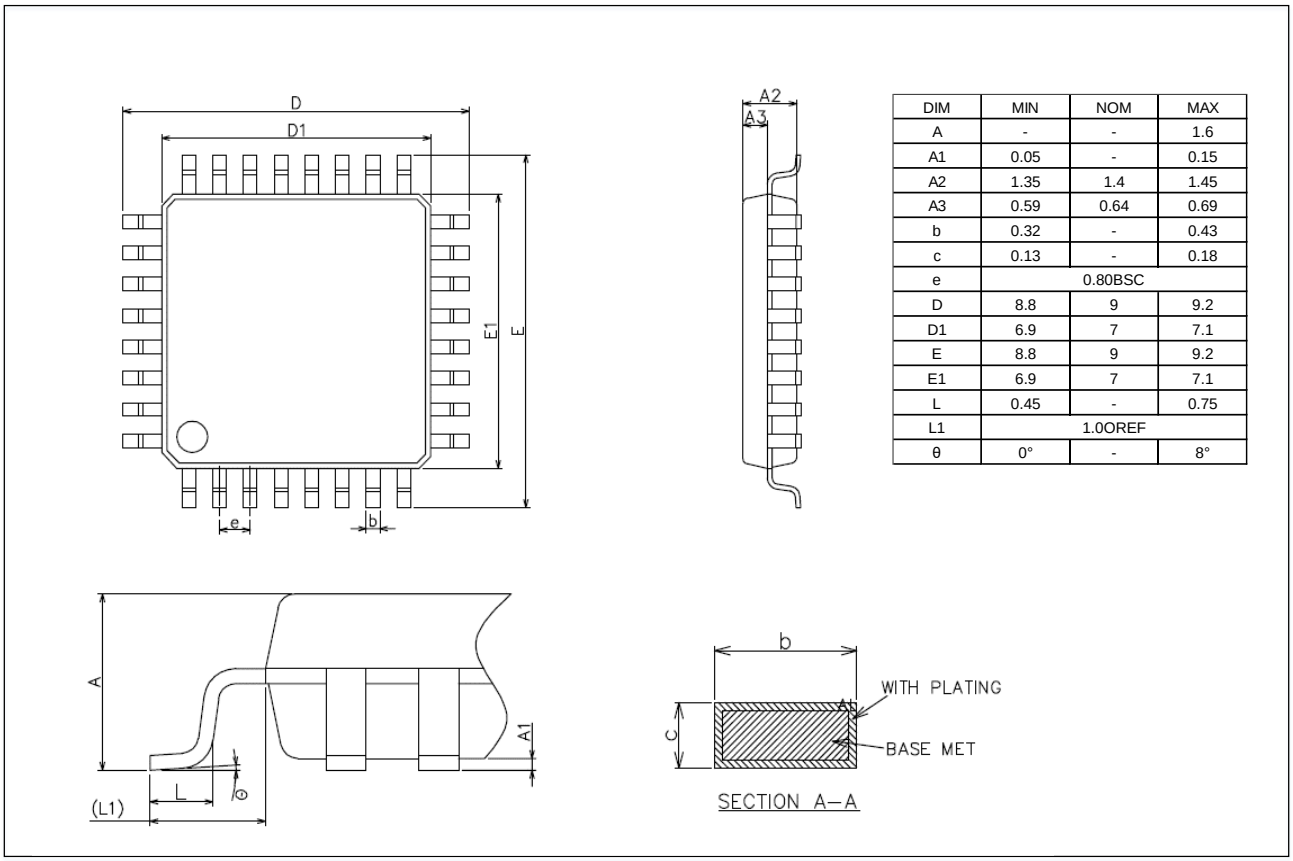
5 Package information

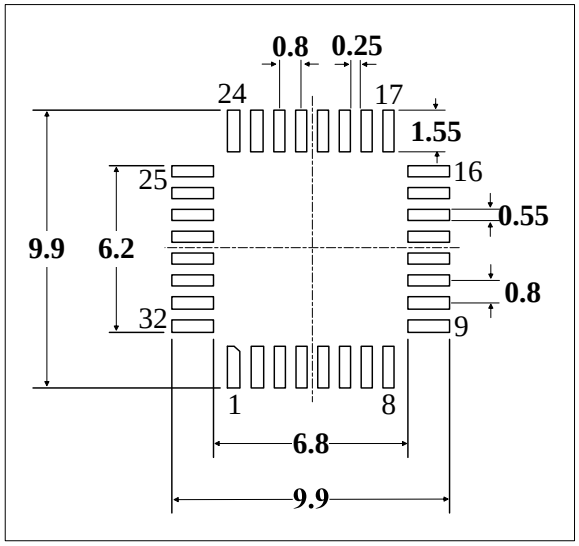
5.1 LQFP32

Figure 5-1 LQFP32 package outline



DIM	MIN	NOM	MAX
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
c	0.13	-	0.18
e	0.80BSC		
D	8.8	9	9.2
D1	6.9	7	7.1
E	8.8	9	9.2
E1	6.9	7	7.1
L	0.45	-	0.75
L1	1.0OREF		
θ	0°	-	8°

Figure 5-2 Suggestions for LQFP32 package solder pads(1)



1. The unit of measurement is millimeters

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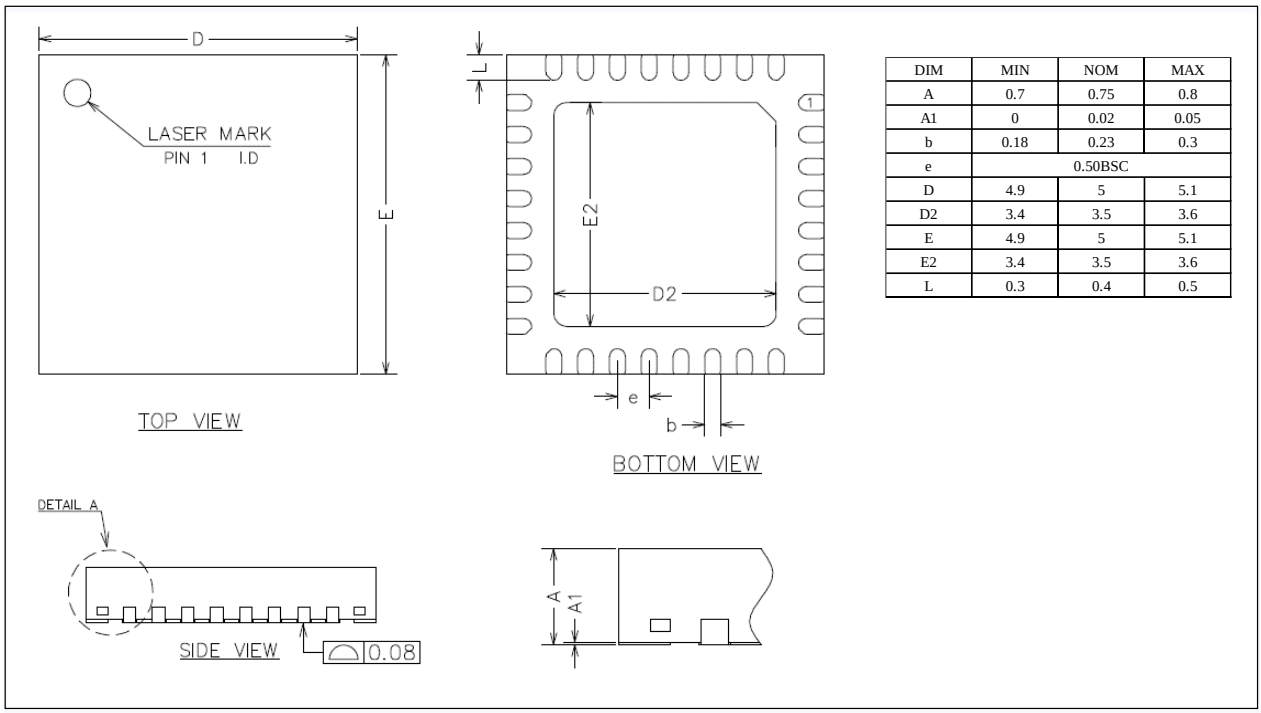
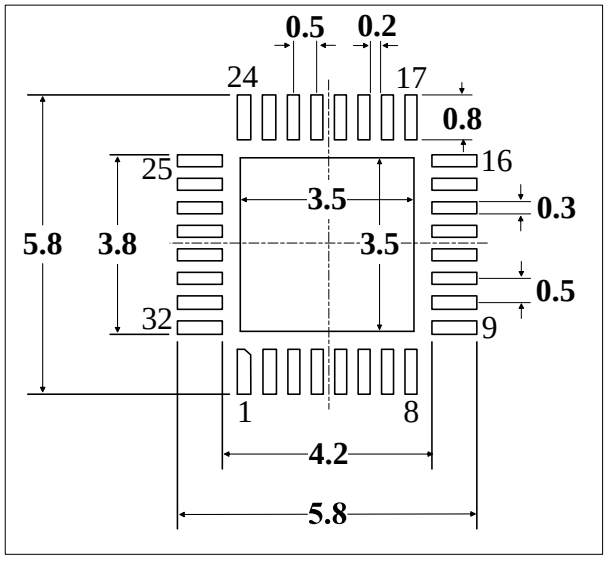
5.2 QFN32 (5x5mm)

Figure 5-3 QFN32 (5x5mm) package outline



DIM	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.18	0.23	0.3
e		0.50BSC	
D	4.9	5	5.1
D2	3.4	3.5	3.6
E	4.9	5	5.1
E2	3.4	3.5	3.6
L	0.3	0.4	0.5

Figure 5-4 Suggestions for QFN32 (5x5mm) package solder pads(1)



1. The unit of measurement is millimeters

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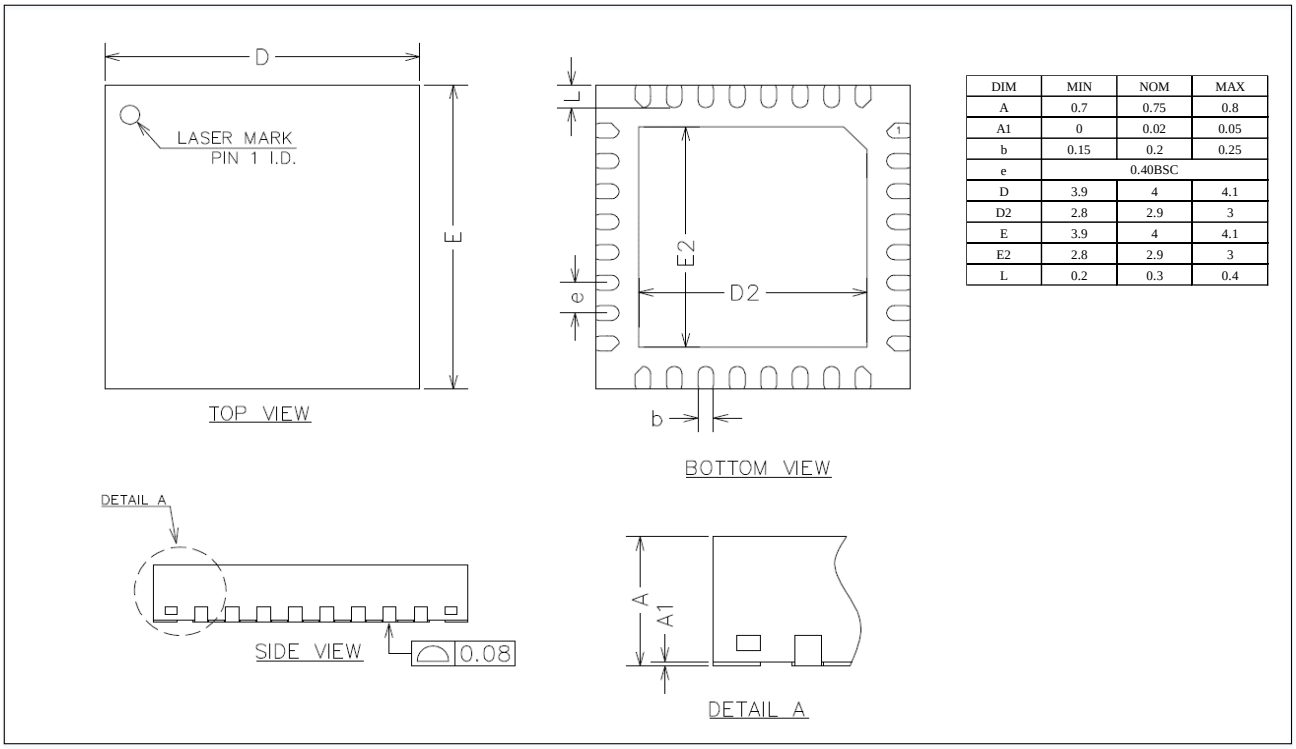
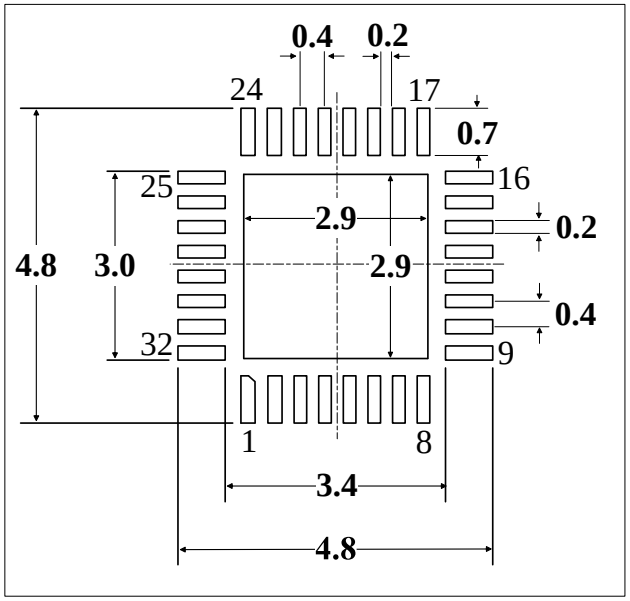
5.3 QFN32 (4x4mm)

Figure 5-5 QFN32 (4x4mm) package outline



DIM	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.15	0.2	0.25
e		0.40BSC	
D	3.9	4	4.1
D2	2.8	2.9	3
E	3.9	4	4.1
E2	2.8	2.9	3
L	0.2	0.3	0.4

Figure 5-6 Suggestions for QFN32 (4x4mm) package solder pads(1)



1. The unit of measurement is millimeters

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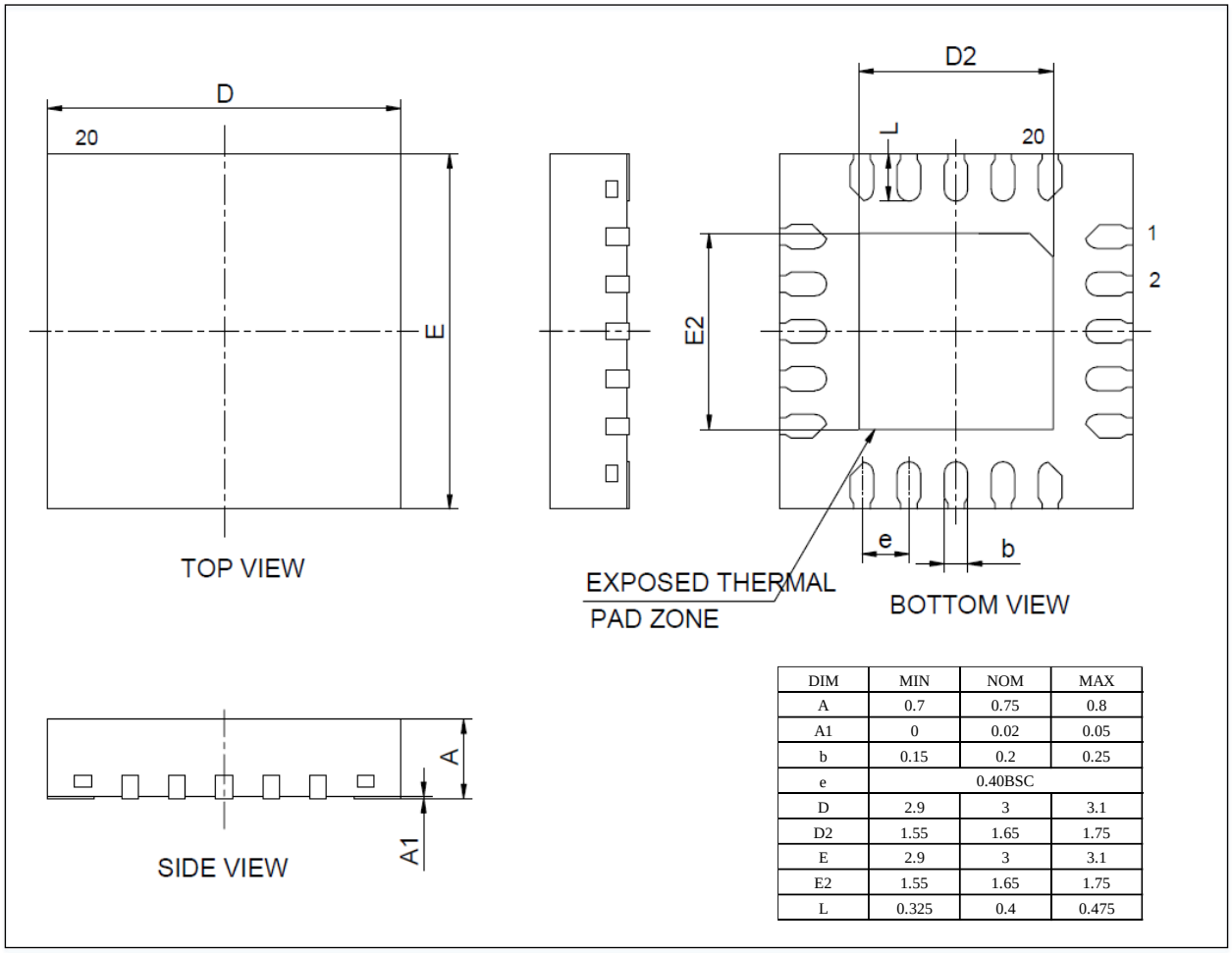
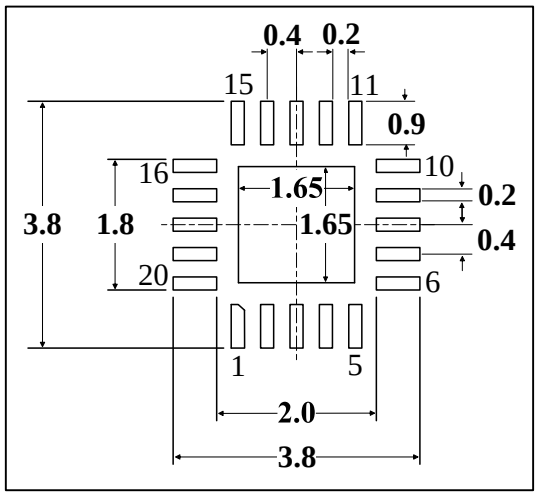
5.4 QFN20/QFN20-1

Figure 5-7 QFN20 package outline



DIM	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.15	0.2	0.25
e		0.40BSC	
D	2.9	3	3.1
D2	1.55	1.65	1.75
E	2.9	3	3.1
E2	1.55	1.65	1.75
L	0.325	0.4	0.475

Figure 5-8 Suggestions for QFN20 package solder pads(1)



1. The unit of measurement is millimeters

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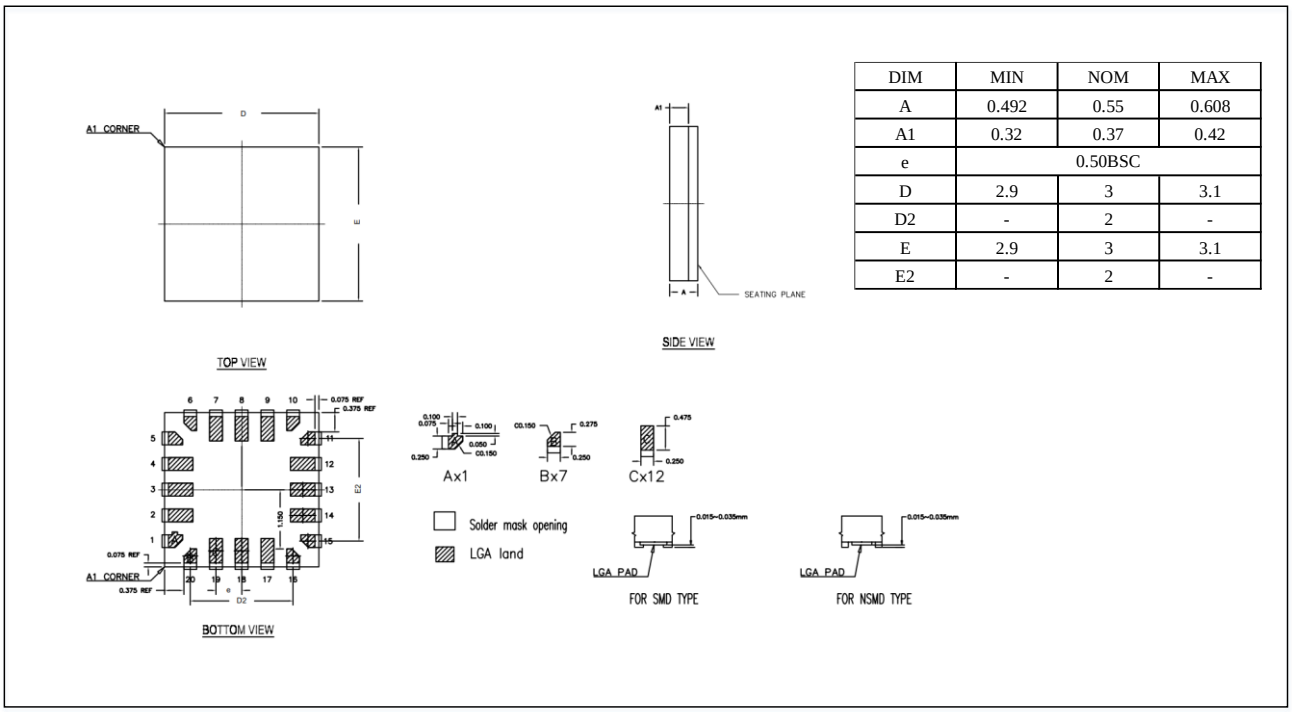
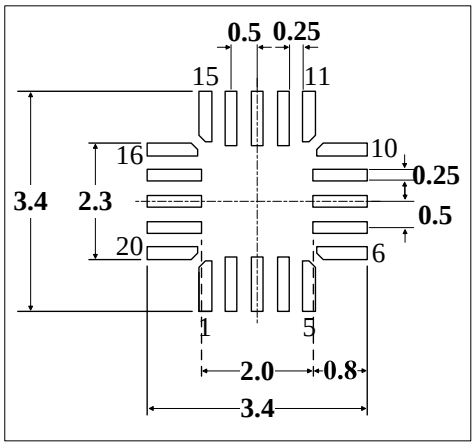
5.5 UFQFPN20

Figure 5-9 UFQFPN20 package outline



DIM	MIN	NOM	MAX
A	0.492	0.55	0.608
A1	0.32	0.37	0.42
e		0.50BSC	
D	2.9	3	3.1
D2	-	2	-
E	2.9	3	3.1
E2	-	2	-

Figure 5-10 Suggestions for UFQFPN20 package solder pads(1)



1. The unit of measurement is millimeters

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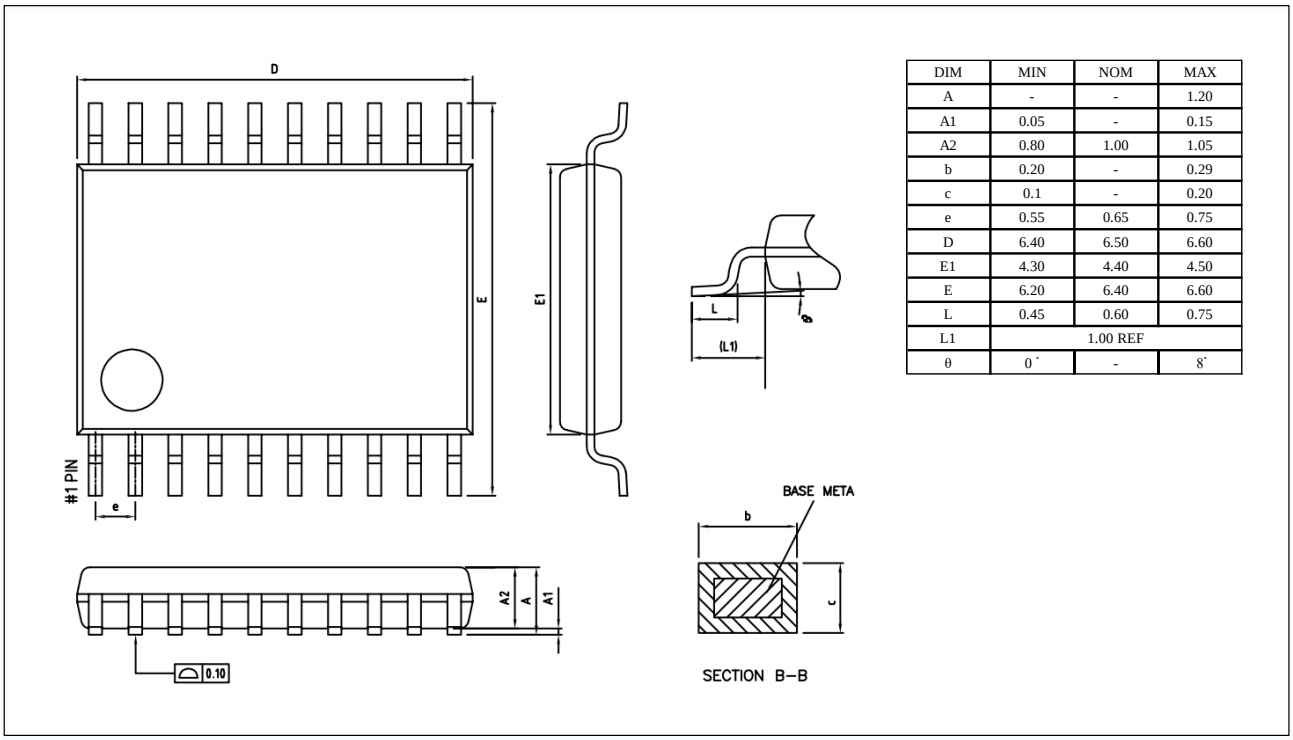
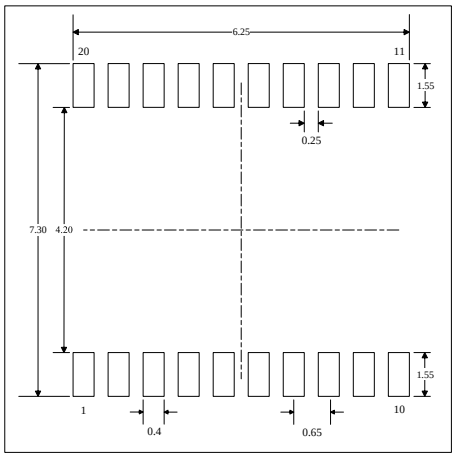
5.6 TSSOP20

Figure 5-11 TSSOP20 package outline



DIM	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.20	-	0.29
c	0.1	-	0.20
e	0.55	0.65	0.75
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	-	8°

Figure 5-12 Suggestions for TSSOP20 package solder pads(1)



1. The unit of measurement is millimeters

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5.7 Marking information

Figure 5-13 LQFP32/QFN32 (5mm*5mm) Marking information

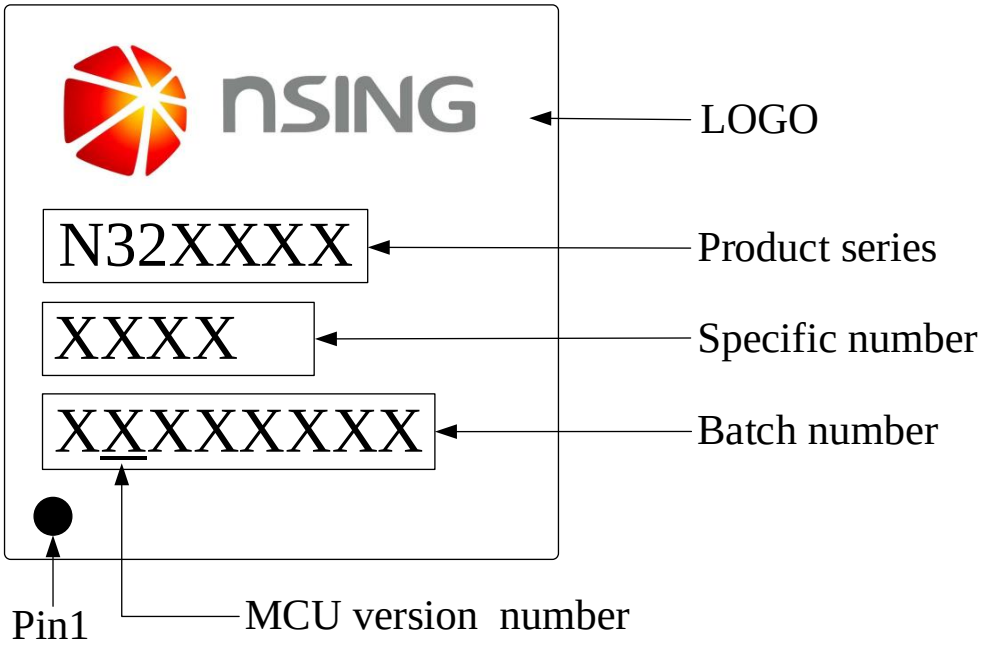

Figure 5-14 QFN32(4mm*4mm) Marking information

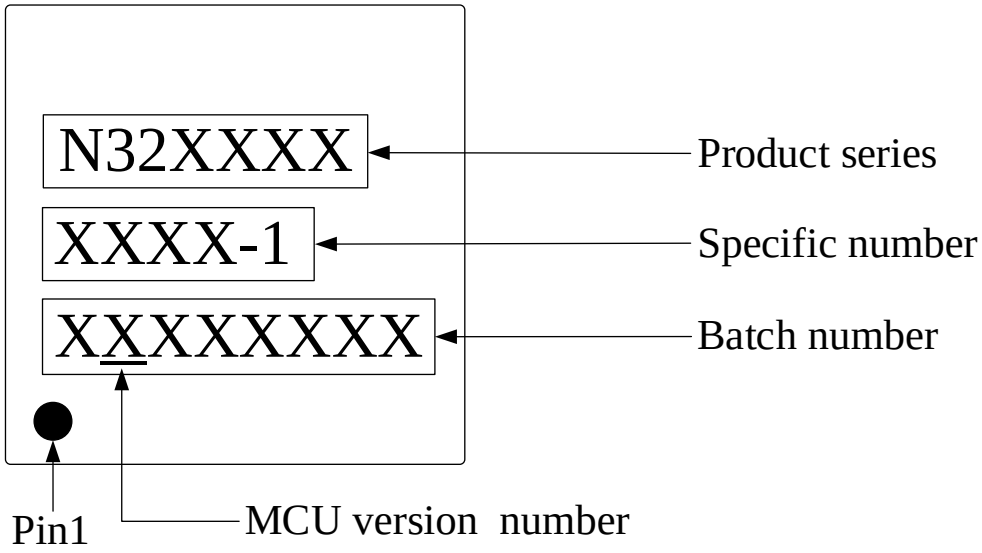

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Figure 5-15 UFQFPN20 Marking information

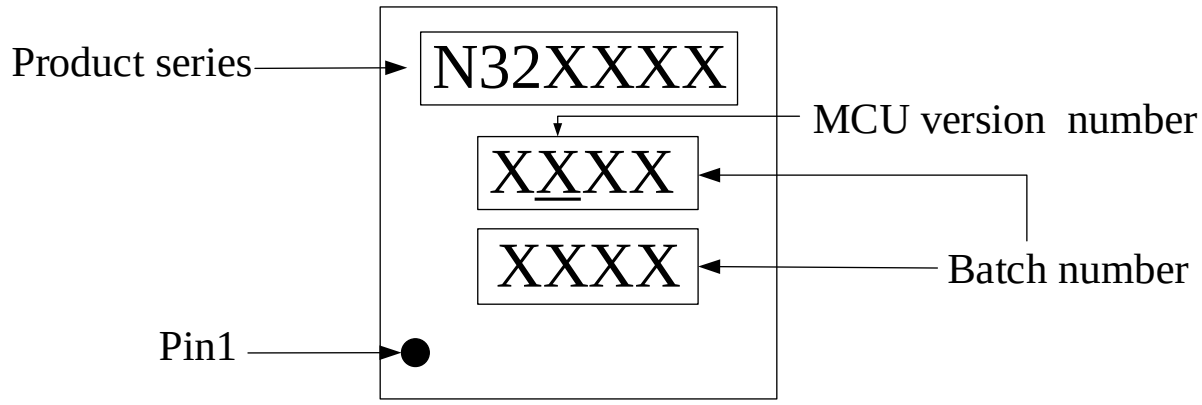

Figure 5-16 QFN20 Marking information

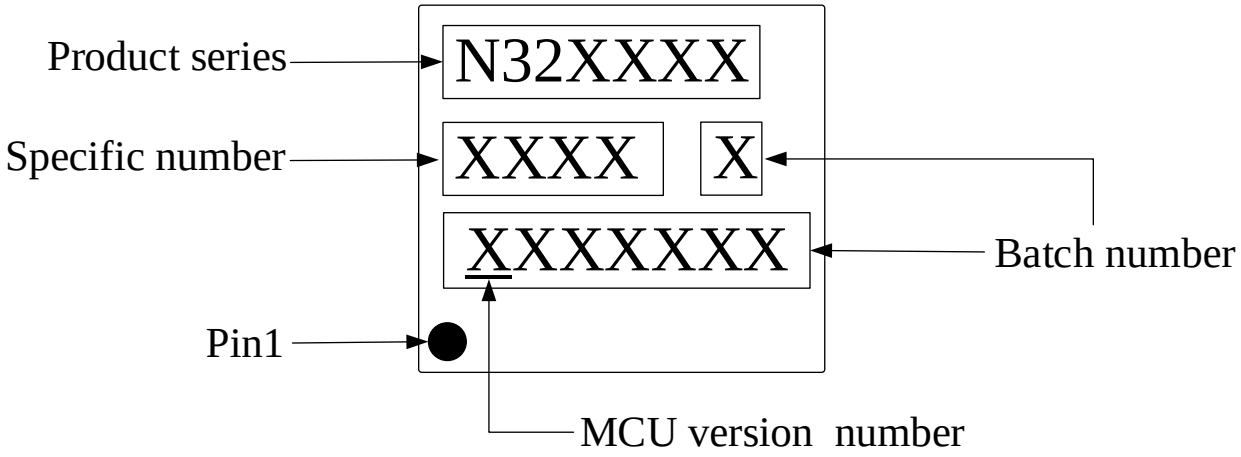

Figure 5-17 QFN20-1 Marking information

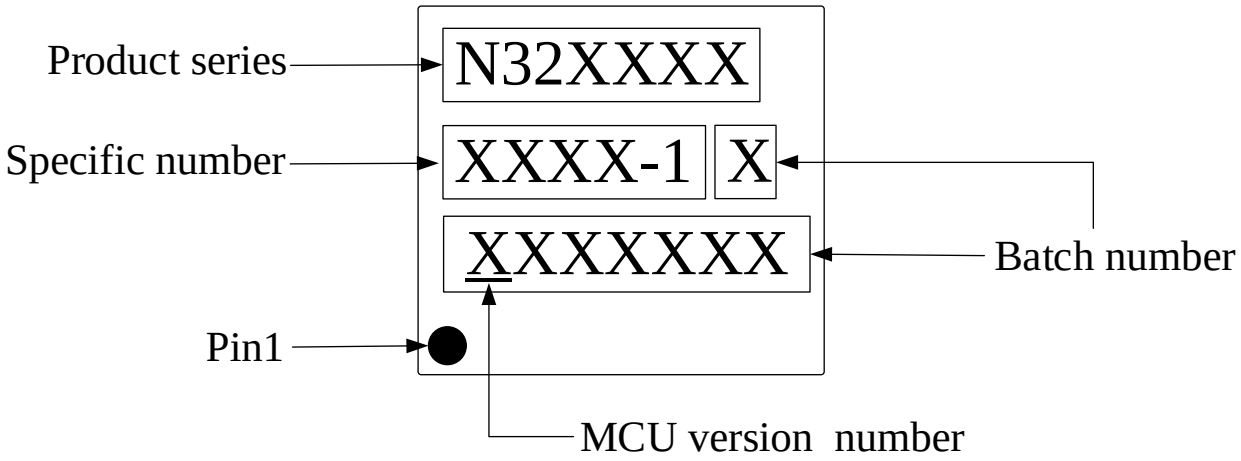

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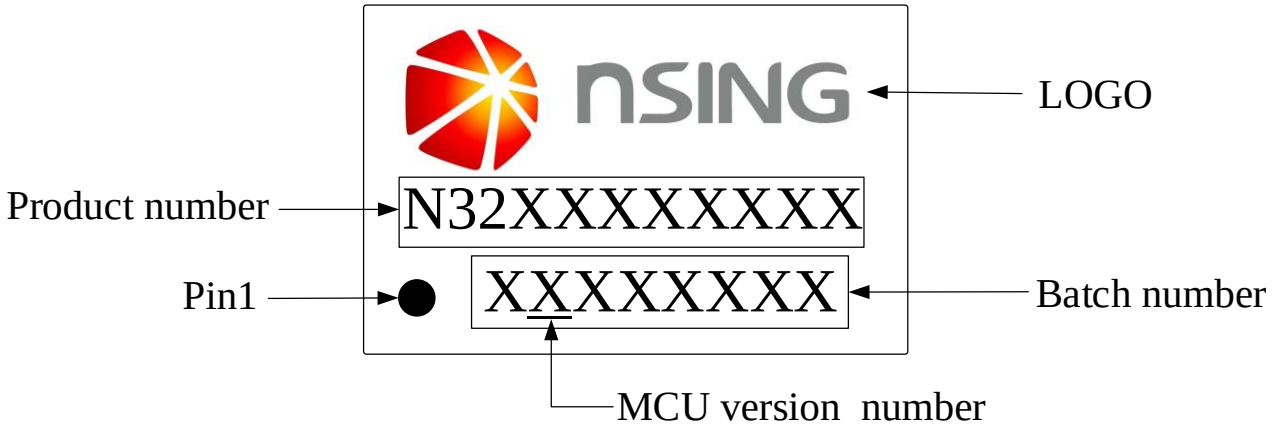
Figure 5-18 TSSOP20 Marking information



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6 Ordering Information

Figure 6-1 N32G033 series ordering code information diagram

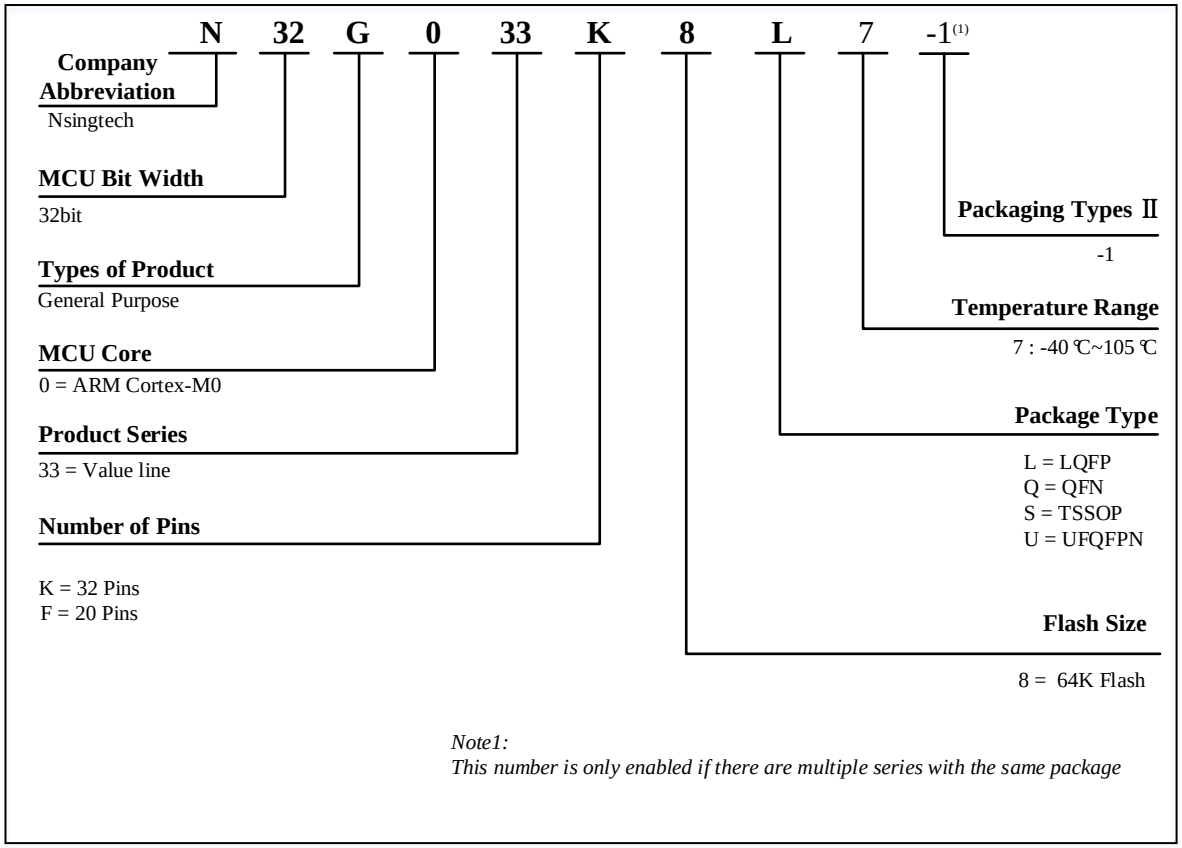

Table 6-1 N32G033 series ordering code information

Order Code(1)	Package	Package Size	Packaging(2)	SPQ(3)	temperature range
N32G033K8L7	LQFP32	7mm * 7mm	Tray	250	-40℃~105℃
N32G033K8Q7	QFN32	5mm *5mm	Tray	490	-40℃~105℃
			Reel	2500	
N32G033K8Q7-1	QFN32	4mm *4mm	Tray	490	-40℃~105℃
N32G033F8Q7	QFN20	3mm *3mm	Tray	490	-40℃~105℃
			Reel	5000	
N32G033F8Q7	QFN20	3mm *3mm	Tray	490	-40℃~105℃
			Reel	5000	
N32G033F8S7	TSSOP20	6.5mm *4.4mm	Tube	70	-40℃~105℃
			Reel	3500	
N32G033F8U7	UFQFPN20	3mm *3mm	Tray	490	-40℃~105℃
			Reel	5000	

1. For the latest detailed ordering information, please refer to the selection manual.
2. This packaging is the basic packaging. If you have any other requirements, please contact National Technology
3. Minimum packaging quantity

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7 Version history

Date	Version	Modify
2025.10.11	V1.0.0	1. Initial Beta version
2025.12.23	V1.1.0	1. Remove fail safe related descriptions from pin reuse definition, fail safe is not supported 2. In the definition of pin reuse, the reuse function column COMP_SUT is placed in the digital function column 3. TSSOP20 package size diagram update 4. N32G033F8S7 model adds Tube packaging 5. Update the ESD Absolute Maximum ESD value 6. Update the typical connection diagram using ADC 7. Update the maximum ED/EL value for ADC accuracy 8. Remove GPIO support for output open drain mode

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