Design Guidelines

N32G033 Series MCU Hardware Design Guide

Introduction

This document details the hardware design checklist for the N32G033 series MCUs to provide users with hardware design guidance.

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1. N32G033 Series MCU Hardware Design Checklist

1.1 Power Supply Introduction

The N32G033 series chips operate at a voltage (VDD) of 2.0V to 5.5V. The main pins are VDD and VDDA. Please refer to the relevant datasheet for details.

1.2 VDD power supply solution

VDD is the main power supply for the MCU and must be powered by a stable external power supply with a voltage range of 2.0V to 5.5V. Decoupling capacitors must be placed nearby on all VDD pins.

For LQFP32 and QFN32 packaged chips, a 4.7uF + 0.1uF decoupling capacitor should be placed near the VDD (pin 17) pin, and a 0.1uF capacitor should be placed near the other VDD pins;

For QFN20, UFQFPN20, and TSSOP20 packaged chips, a 4.7uF + 0.1uF decoupling capacitor should be placed near the VDD pin;

VDDA is the analog power supply, providing power to most analog peripherals. It is recommended to place a 0.1uF and a 1uF capacitor on the VDDA input pins.

1.3 External pin reset circuit

A low-level signal (external reset) on the NRST pin will trigger a system reset. The reference circuit for an external NRST pin reset is as follows.

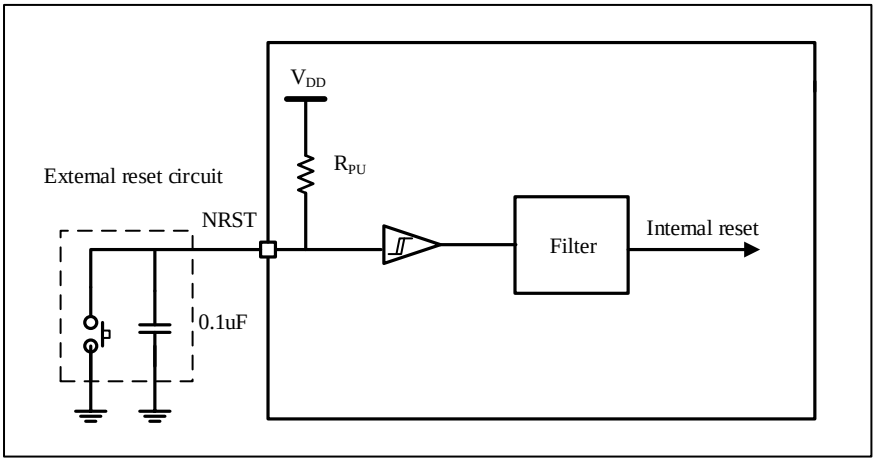

Figure 1-1 System Reset Diagram

Note: The reset pin NRST is designed with a typical reference value of 0.1uF external capacitor. If a faster reset time is required, an external pull-up resistor can be added to the NRST pin, with a typical value of 10K. Additionally, users can decide whether to add a reset button based on their product requirements.

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1.4 Clock circuit

The N32G033 series MCUs include two internal clocks: an internal high-speed RC oscillator HSI (64MHz) and an internal low-speed clock LSI (32kHz).

1.5 Start-up pin connection

The diagram below shows the external connections required when selecting the boot memory for the N32G033 series chips. Please refer to the relevant section of the datasheet for information on boot modes.

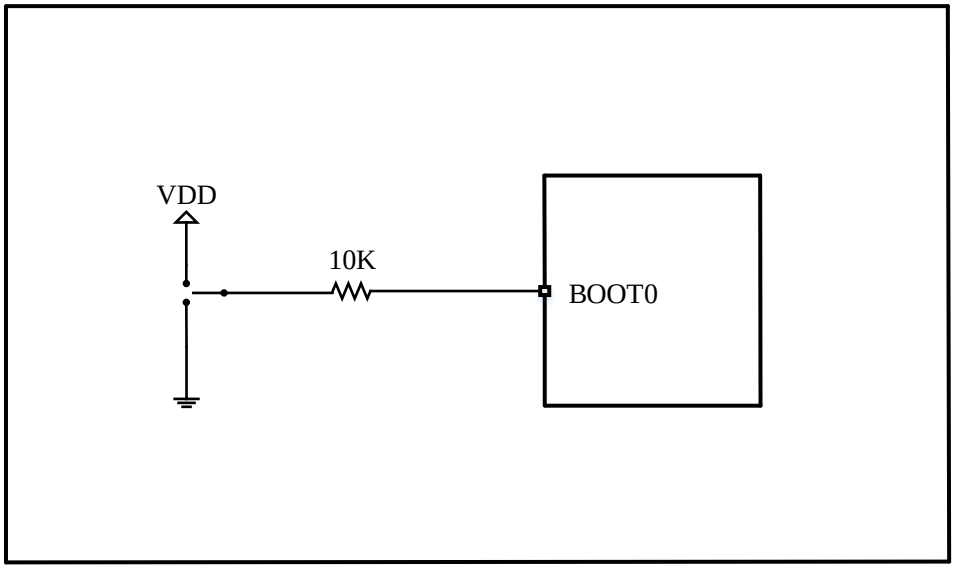

Figure 1-2 Startup mode implementation example

Note: The resistance values shown in the figure are given only as typical reference values.

1.6 Independent ADC converter

To improve conversion accuracy, the ADC has a pair of independent power supplies. A separate VDDA pin powers the ADC, while the VSSA pin serves as the ground for the analog power supply. This VSSA pin can be individually filtered and shielded before being used to power the ADC, reducing interference from PCB-level noise.

Regarding ADC circuit design, please note the following points:

1） When using ADC sampling, it is recommended to shorten the external trace distance of the ADC sampling channel;

2） It is recommended to keep the area around the ADC input signal away from high-frequency switching signals;

3） During ADC conversion, the chip does not support modifying the ADC configuration. If you need to modify

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the configuration, you must wait until the current conversion is completed or the ADC is turned off before you can configure it.

4） When using a particular ADC channel, a negative voltage (e.g., -0.2V) must not be applied to other unused ADC sampling channels. Applying this negative voltage will pull down the voltage of the normally sampling ADC channel, resulting in inaccurate sampled data.

5） When using a particular ADC channel, a high voltage (greater than VDD) must not be applied to other unused ADC sampling channels. Applying such a high voltage will pull up the voltage of the normally sampling ADC channel, resulting in inaccurate data readings.

6） When using an ADC, the maximum value of RAIN cannot be too large and must conform to the following formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

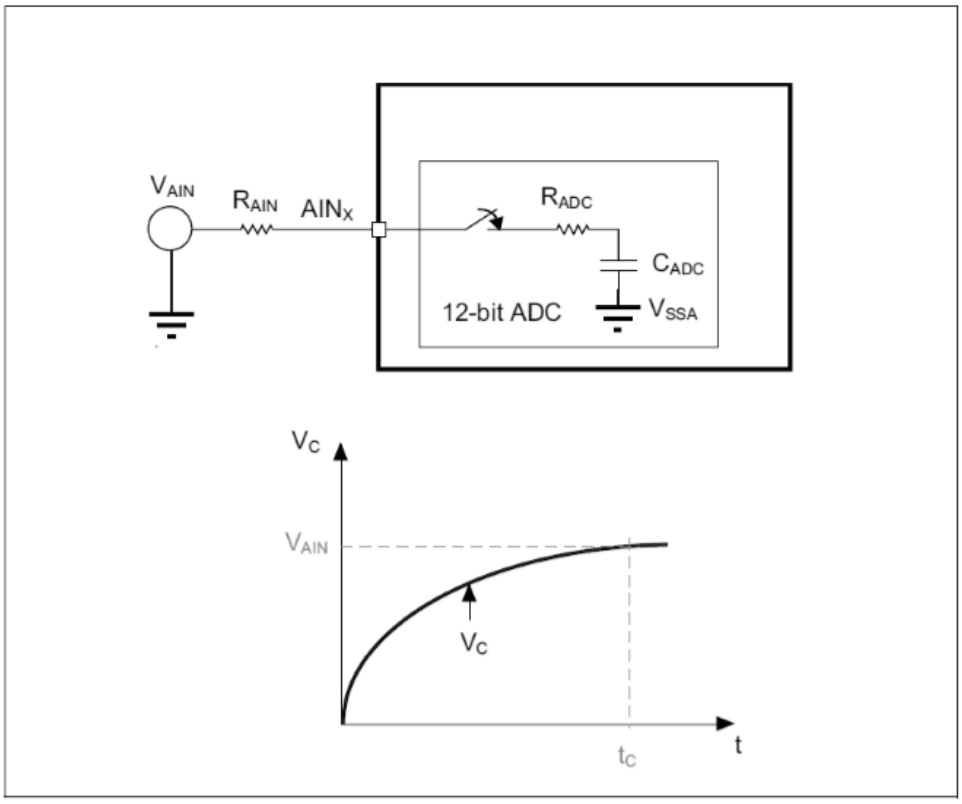

Figure 1-3 Effect of series resistance at ADC input port

The following table shows the relationship between external input impedance and sampling time: (Maximum

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permissible error = 1/4 LSB, 12-bit resolution, ADC clock frequency = 18MHz)

resolution	Sample cycle@16M	Sampling rate (MHz)	Minimum sampling time (ns)	Rin (kΩ)
12-bit	4	1.000	250	0.9
	6	0.889	375	1.9
	14	0.615	875	5.9
	20	0.500	1250	8.8
	30	0.381	1875	13.8
	42	0.296	2625	19.7
	56	0.235	3500	26.7
	72	0.190	4500	34.6
	88	0.160	5500	42.5
	120	0.121	7500	58.4
	182	0.082	11375	89.1
	240	0.063	15000	117.8
	300	0.051	18750	147.6
	400	0.039	25000	197.1
	480	0.033	30000	236.7
	600	0.026	37500	296.2
resolution	Sample cycle@32M	Sampling rate (MHz)	Minimum sampling time (ns)	Rin (kΩ)
12-bit	20	1.00	625	3.9
	30	0.76	937.5	6.4
	42	0.59	1312.5	9.3
	56	0.47	1750	12.8
	72	0.38	2250	16.8
	88	0.32	2750	20.7
	120	0.24	3750	28.7
	182	0.16	5687.5	44.0
	240	0.13	7500	58.4
	300	0.10	9375	73.2
	400	0.08	12500	98.0
	480	0.07	15000	117.8
	600	0.05	18750	147.6

Table 1-1 Table of ADC external input impedance and sampling time

1.7 IO withstand voltage

When using the chip, please pay attention to the withstand voltage of each I/O. In the I/O section of the datasheet, pin multiplexing definitions indicate TC: Standard 5V I/O.

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Package					Pin name (function after reset)	Type(1)	I/O(2)	Alternate functions(3)	
LQFP32	QFN32	QFN20	UFQFPN20	TSSOP20				Digital	Analog
1	1	1	-	-	VDD	S	TC	-	VDD
2	2	-	1	2	PF0	I/O	TC	I2C1_SDA, TIM3_CH1, UART1_TX, UART2_TX, UART3_TX, TIM3_ETR	OPAMP_VINP, PGA0_INP
3	3	-	2	3	PF1	I/O	TC	I2C1_SCL, TIM3_CH2, UART1_RX, UART2_RX, UART3_RX, TIM4_ETR	PGA0_INM,

Figure 1-4 Datasheet pin multiplexing defined I/O structure

Note : TC: Standard 5V IO; When using the chip, be aware of the impact of signals higher than 5V on the IO.

1.8 Anti-static design

1.8.1 PCB design

For standard two-layer PCB designs, it is recommended to surround signal lines with ground planes and also to cover the edges of the PCB with ground planes as much as possible. Where cost allows, four-layer or multi-layer PCB designs can be used. In multi-layer PCBs, the ground plane acts as an important charge source, which can counteract the charge on electrostatic discharge sources, thus reducing problems caused by electrostatic fields. The PCB ground plane can also act as a shield for signal lines (of course, the larger the opening of the ground plane, the lower its shielding effectiveness). Furthermore, in the event of a discharge, due to the large ground plane of the PCB, charge is easily injected into the ground plane rather than into the signal lines. This is beneficial for component protection, as the charge can dissipate before causing component damage.

1.8.2 ESD protection devices

In actual product design, the chip itself has a certain degree of electrostatic discharge (ESD) protection capability. The N32G033 series MCU has an ESD (HBM) rating of +/-4KV. However, if higher ESD protection levels are required, and some chip pins need to be directly connected as output or input ports, these pins are directly exposed on the outermost surface of the product and cannot be isolated using ground planes or similar methods. In such cases, external ESD protection devices are generally necessary. A TVS diode is a typical ESD protection device. Below is a typical connection example.

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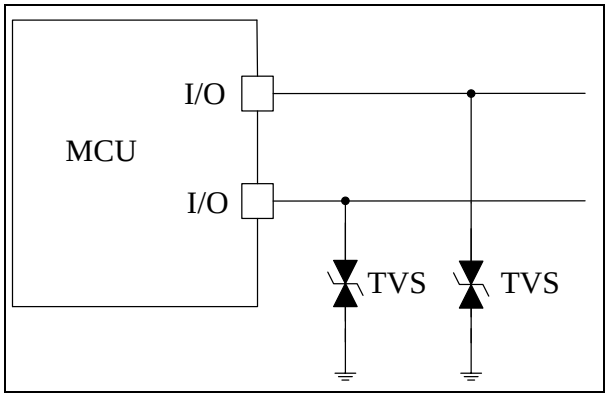

picture 1-5 TVS connection method on I/O pins

1.9 Debugging interface

The N32G033 series chips support a serial (SWD) debug interface. Please refer to the relevant user manual for detailed application information.

Debug signal	GPIO pins
SWDIO	PA13
SWCLK	PA14

Table 1-1 Debugging interface

1.10 BOOT serial port interface

The N32G033 series chips support BOOT serial communication. The serial port interfaces are shown in the table below:

BOOT serial port	GPIO pins
UART1_TX	PA9
UART1_RX	PA10

Table 1-2 Serial port interface

1.11 Module Design Considerations

If the MCU is used as the master, the following pins are recommended.

I2Cx	**SDA**	**SCL**
I2C1	PA5, PA10, PA13, PB7	PA4, PA9, PB6, PB8
I2C2	PA10	PA9, PA11

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2. Overall design recommendations

1） Printed circuit board

It is recommended to use a multilayer printed circuit board with a dedicated ground plane (VSS) and a dedicated power plane (VDD) to provide good coupling performance and shielding. In practical applications, if cost considerations prevent the use of a multilayer printed circuit board, then a good grounding and power supply structure must be ensured during circuit design.

2） Device location

In PCB design, different circuits need to be laid out separately based on their varying EMI impacts. For example, high-current circuits, low-voltage circuits, and high-frequency components should be separated. This reduces cross-coupling on the PCB.

3） Grounding and power supply (VSS, VDD)

Each module (analog circuits, digital circuits, and low-sensitivity circuits) should be grounded independently, with digital and analog grounds separated. All grounds should ultimately be connected together at a single point. Based on the PCB current, the power line width should be increased as much as possible to reduce loop resistance. Simultaneously, the routing of power and ground lines should be as consistent as possible with the current direction, and power lines should be placed as close as possible to ground lines to minimize loop areas. This helps enhance noise immunity. Areas on the PCB without components should be filled with ground to provide good shielding.

4） Decoupling

All power pins need to be properly connected to the power supply. These connections, including pads, traces, and vias, should have the lowest possible impedance. This is typically achieved by increasing trace width, and decoupling capacitors must be placed close to the chip for each VDD and VSS pin pair. The following diagram shows a typical layout for power/ground pins.

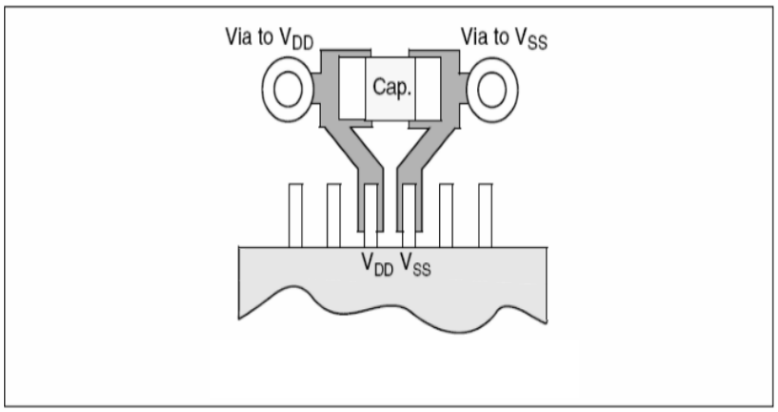

Figure 2-1 Typical layout of VDD/VSS pins

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3. PCB LAYOUT Reference

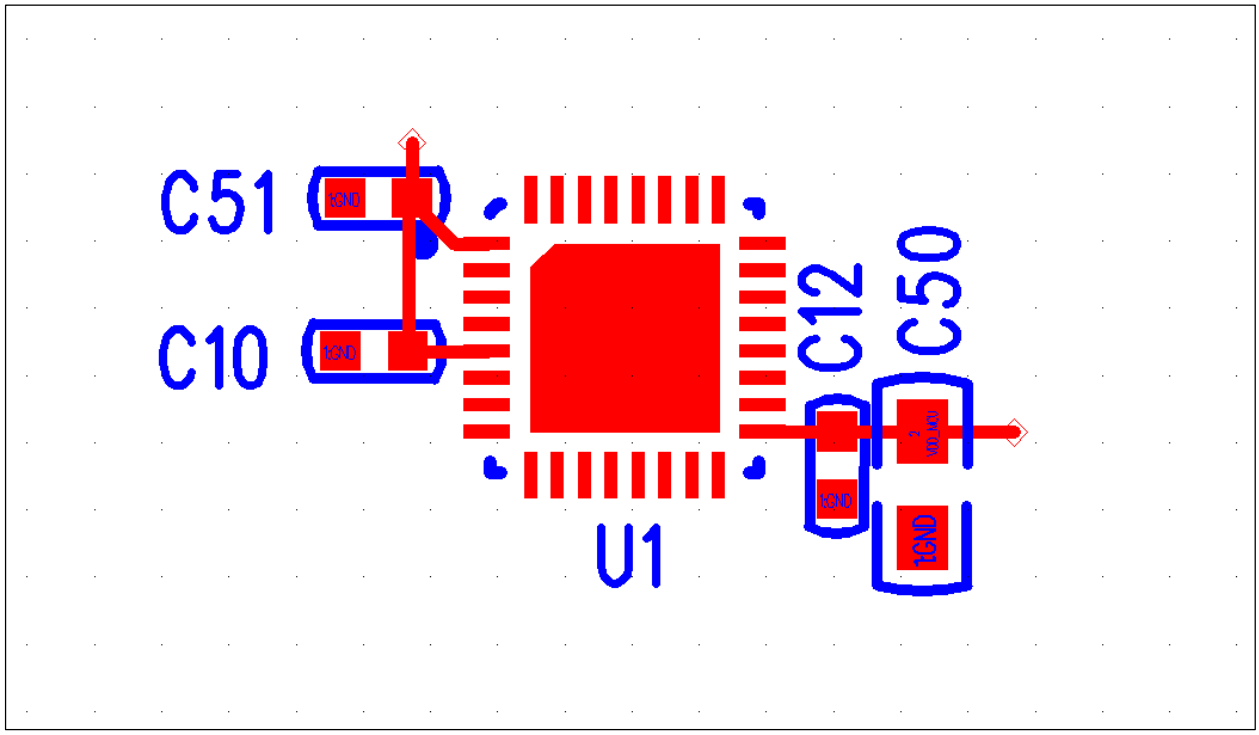

Figure 3-1 N32G033 Series QFN32 Package PCB LAYOUT Reference Diagram

When designing the PCB layout, a decoupling capacitor needs to be placed near each power pin.

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Version	date	Remark
V1.0.0	2025-8-26	Create document

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