User guide

UG_N32G033 Series MCU BOOT User Guide

Introduction

The usage guide mainly describes the BOOT interface instructions of N32G033 series MCU, which is easy to download and develop by using the Nations technology BOOT loader.

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Content

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1 BOOT brief introduction

The firmware program of the chip, namely BOOT, mainly provides user program download, API and other functions.

This document describes in detail the function, implementation and introduction of BOOT of N32G033 series chips. The maximum Main FLASH storage area of N32G033 series chips is 64KB.

1.1 BOOT function definition

- **User program download function**
  - Support UART (UART1, default PA9/PA10, can be configured as PA13/PA14, PF0/PF1, PA2/PA3 through option byte USER4 [1:0], baud rate negotiation);
  - Support download data CRC32 verification;
  - Support plaintext download
  - Supports power-on BOOT self-verification.
  - Support jumping to the Main flash/SRAM user area for execution
  - Support software reset chip operation.

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2 BOOT process and command processing

The firmware program BOOT of N32G033 series chips supports downloading user programs and data through the UART interface. The following describes the related command processing flow.

2.1 Commands and data structures

2.1.1 The list of commands

Table 2-1 Command definition

Name of the command	The key value	Description
CMD_SET_BR	0x01	Set the baud rate of the serial port (Valid only when serial ports are used)
CMD_GET_INF	0x10	Read chip model index, BOOT version number, chip ID
CMD_FLASH_ERASE	0x30	Erase FLASH
CMD_FLASH_DWNLD	0x31	Download user programs to FLASH
CMD_DATA_CRC_CHECK	0x32	CRC verification download user program
CMD_OPT_RW	0x40	Read/configure option bytes (including read protection level, FLASH page write protection, Data0/1 configuration)
CMD_SYS_RESET	0x50	The system reset
CMD_APP_GO	0x51	Jump to the user area to execute the program

2.1.2 The data structure

Here are some conventions explained below, where "<>" represents fields that must be included, and "()" represents fields that are included according to different parameters.

Upper and lower instruction data structures

1. Upper instruction structure:

<CMD_H + CMD_L + LEN + Par> + (DAT).

CMD_H represents the first-level command field, CMD_L represents the second-level command field; LEN represents the length of the transmitted data; Par represents the 4-byte command parameter; DAT represents the specific data sent by the upper layer command to the lower layer;

2. Lower level response structure：

< CMD_H + CMD_L + LEN > + (DAT) + <CR1+CR2>.

CMD_H represents the first-level command field, CMD_L represents the second-level command field, the lower-level command field is the same as the corresponding upper-level command field; LEN represents the length of the transmitted data; DAT represents the specific data that the lower layer responds to the upper layer; CR1+CR2 represents the return to the upper layer Command execution result, if the first-level and second-level command

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fields of the command sent by the upper layer do not belong to any command, BOOT replies with CR1=0xBB and CR2 = 0xCC.

Command data structures supported by the serial port:

1. The upper computer sends the upper-layer command:

STA1 + STA2 + {upper instruction structure} + XOR.

STA1 and STA2 are the starting bytes of the command sent by the serial port, STA1=0xAA, STA2=0x55. Used for the chip to identify the host computer to send the serial data stream.

XOR represents the XOR value of the previous command byte (STA1 + STA2 + {upper instruction structure}).

2. The upper computer receives the lower-layer response:

STA1 + STA2 + {lower response structure} + XOR.

STA1 and STA2 are the starting bytes of the command sent by the serial port, STA1=0xAA, STA2=0x55. Used for the host computer to identify the chip to send serial data stream

XOR represents the XOR value of the previous command byte (STA1 + STA2 + {lower response structure}).

2.1.3 Command Examples

The following table selects one command for each command type as an example for reference. For detailed instructions on commands, please refer to the Command Description section.

command name	Command Example	Command structure (2)							
		STA1	STA2	CMD_H	CMD_L	LEN[1:0]	Par[3:0]	DAT	XOR
CMD_SET_BR	Set serial port baud rate to 4800	AA	55	01	00	00,00	00,00,12, C0	empty (1)	2C
CMD_GET_INF	Read chip information	AA	55	10	00	00,00	00,00,00, 00	empty (1)	EF
CMD_FLASH_ERASE	Erase FLASH page 0	AA	55	30	00	00,00	00,00,01, 00	empty (1)	CE
CMD_FLASH_DWNLD	Download FLASH page 0 16 bytes	AA	55	31	00	24,00	00,00,00, 08	32 0x00，C8,22,2D,55	70
CMD_DATA_CRC_CHECK	CRC check FLASH page 0	AA	55	32	00	18,00	Actual CRC value of 4 bytes	16 0x00，00,00,00,08，00,02,00,00	XOR value based on CRC

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									value
CMD_OPT_RW	Get option bytes	AA	55	40	00	11,00	00,00,00,00	17 0x00	AE
CMD_SYS_RESET	Software reset boot program	AA	55	50	00	00,00	00,00,00,00	empty (1)	AF
CMD_APP_GO	Jump to Main FLASH	AA	55	51	00	00,00	00,00,00,00	empty (1)	AE

Note:

1. Empty means no data

2. For a detailed explanation of upper level instructions, please refer to the Command Description chapter

2.2 Command description

2.2.1 CMD_SET_BR

This command is used to modify the serial port baud rate.

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x01 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent: 0x00,0x00							
4~7(Par)	Par[0~3] : Set baud rate parameters							
(DAT)	None							

- Par[0~3], the serial port baud rate negotiation setting value can be set to the maximum, and the setting range is 2.4Kbps ~ 923.076Kbps, the default baud rate is 9600bps; baudrate = (Par[0] << 24) +(Par[1] << 16) + (Par[2] << 8) + Par[3].
- Reserved value: 0x00;

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x01 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent: 0x00,0x00							

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(DAT)	None
4(CR1)	Status byte 1
5(CR2)	Status byte 2

- Status bytes (CR1 and CR2) are divided into the following types according to command execution:
  1) Return success: status flag bit (0xA0, 0x00).
  2) Return failure: status flag bits (0xB0, 0x00).

The following are the baud rate values supported by baud rate negotiation (√ means supported, / means not supported):

Clock parameters	**Baud rate**											
(MHz)	**2400**	**4800**	**9600**	**14400**	**19200**	**38400**	**57600**	**115200**	**128000**	**256000**	**576000**	**923076**
HSI	√	√	√	√	√	√	√	√	√	√	√	√

2.2.2 CMD_GET_INF

The command reads the BOOT version number, chip model index, chip ID, and chip serialization information.

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x10 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3 (LEN)	Length of data sent							
4~7(Par)	Reserved							
(DAT)	None							

- Reserved value: 0x00.
- LEN send data length: 0x00(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] +(LEN[1]<<8).

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x10 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3 (LEN)	The length of the data							
4~54(DAT)	BOOT version, chip model index, and chip ID							

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55(CR1)	Status byte 1
56(CR2)	Status byte 2

- The procedure byte (CMD_H) corresponds to the upper instruction (CMD_H).
- LEN is the data length: 0x33(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- DAT[0] : 0x0B, chip model index
- DAT[1]: 0xXY, BOOT version number (BCD code)

  0x10: indicates the command set version used by BOOT, indicating that the command set version of V1.0 is used.
- DAT[2] : BOOT command set version
- DAT[3~50] 48Byte
  1) DAT[3~18] : 16Byte UCID (for details about the UCID, see the user manual).
  2) DAT[19-30] : 12Byte Chip ID(UID) (for details, see the user manual).
  3) DAT[31~34] : 4Byte DBGMCU_IDCODE (for details about DBGMCU_IDCODE, see the user manual).
  4) DAT[35~50] : 16Byte chip model.
- Status bytes (CR1 and CR2) are divided into the following types according to command execution:
  1) Return success: status flag bit (0xA0, 0x00).
  2) Return failure: status flag bits (0xB0, 0x00).

2.2.3 CMD_FLASH_ERASE

BOOT provides the function of erasing FLASH on a page by page basis, with the page address number and number provided by the user. The erased FLASH space cannot exceed the entire FLASH space, and at least one page (512Byte) must be erased.

Upper-level instructions:

Bit / Byte	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x30 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent (0)							
4~7(Par)	Page address number 2 bytes: 0~255 Page number 2 bytes :1~256							

- CMD_L: erases the partition number
  1) 0x00=Main FLASH
  2) 0x04=SRAM; Support address range 0x20000500~0x20017FF. The SRAM erase operation does not

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actually perform any operation and returns OK directly.

- LEN Send data length: 0x10(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- The erase address and range consist of four bytes in the Par field
  - Par[0~1] : page address number 2 bytes (0~255)

    Page address number = Par [0] + Par [1]<<8;
  - Par[2~3] : Page number 2 bytes (1~256)

    Page number = Par [2] + Par [3]<<8;
  - The header address of page 0 is 0x0800_0000. The number of subsequent pages is incremented by 1, and the header address is incremented by 0x200.

    Such as:

    The header address of page 1 is 0x0800_0000 + 1*0x200 = 0x0800_0200

    The header address of page 2 is 0x0800_0000 + 2*0x200 = 0x0800_0400
  - The entire address range erased

    For example: the page address number is 0x01, and the page number is 0x02

    Erasing address range:

    (0x0800_0000 + 1*0x200) ~ (0x0800_0000 + 1*0x200 + 2*0x200). That is (the header address of the page address number) ~ (the header address of the page address number + the number of pages * the size of the page)

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x30 Level-1 command field							
1(CMD_L)	Level-2 command field: Erase area							
2~3(LEN)	Length of data sent							
(DAT)	None							
4(CR1)	Status byte 1							
5(CR2)	Status byte 2							

- LEN Send data length: 0x00(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- Status bytes (CR1 and CR2) are divided into the following types according to command execution:

  1. Return success: status flag bit (0xA0, 0x00).
  2. Return failure: status flag bits (CR1, CR2).

     (1) (0xB0, 0x00) : Return failure;

     (2) (0xB0, 0x31) : The erased FLASH page is protected by WRP;

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(3) (0xB0, 0x34) : The FLASH address range is out of bounds (that is, it exceeds the size of the entire FLASH/SRAM);

(4) (0xB0, 0x37) : Failed to erase the FLASH.

2.2.4 CMD_FLASH_DWNLD

This command provides users with the ability to download code to a specified FLASH. The data length must be aligned with 16 bytes (if it is insufficient, 0x00 will be automatically added to the upper computer), all of which are provided by upper level commands. Write plaintext to FLASH.

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x31 Level-1 command field							
1(CMD_L)	Level-2 command field: Download partition number							
2~3(LEN)	Length of data sent							
4~7(Par)	Start address for downloading the FLASH							
8~23(DAT)	DAT[0:15] : 16 bytes Key authentication value for USER1/3 partition authentication							
24~(24+N)(DAT)	DAT[16~16+N] : Specific data to be downloaded							
(24+N+1)~(24+N+4)(DAT)	DAT[16+N+ 1-16 +N+4] : specifies the 4 byte CRC32 check value of data							

- CMD_L: download partition number
  1) 0x00= Main FLASH
  2) 0x04=SRAM; Support address range 0x20000500~0x20017FF.
- LEN send data length: 0xXX(LEN[0]), 0xXX(LEN[1]), LEN = LEN[0] + (LEN[1]<<8)
- Par [0 ~ 3] : download the starting address of the FLASH, synthetic rules to Address = Par[0] | Par[1]<<8 | Par[2]<<16 | Par[3]<<24.
- DAT[0~15] : reserve(0).
- DAT[16~16 +N] : download specific data, the total number of data is N+1
  1) USART: up to 128 bytes, 16<=N+1<=144. N+1 must be a multiple of 16.
- DAT[16+N+1~16+N+4] : 4Byte CRC32 check value of unencrypted data

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x31 Level-1 command field							
1(CMD_L)	Level-2 command field: Download partition number							

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2(LEN)	Length of data sent
(DAT)	None
3(CR1)	Status byte 1
4(CR2)	Status byte 2

- LEN Send data length: 0x00(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- Status bytes (CR1 and CR2) are divided into the following types according to command execution:
  1. Download success: status flag bit (0xA0, 0x00).
  2. Download failed: status flag bit (CR1, CR2).
     (1) (0xB0, 0x00) : Return failure;
     (2) (0xB0, 0x31) : The downloaded FLASH address is protected by WRP;
     (3) (0xB0, 0x34) : Download FLASH address range is out of bounds (refers to the size of the entire FLASH/SRAM);
     (4) (0xB0, 0x35) : Download FLASH start address is not 16 bytes aligned;
     (5) (0xB0, 0x36) : The downloaded FLASH data length is not a multiple of 16;
     (6) (0xB0, 0x37) : Programming FLASH fails;

2.2.5 CMD_DATA_CRC_CHECK

This command is used to verify whether the downloaded data is correct. Considering the factors of download speed and the relatively low probability of download failure, a unified CRC check is performed after the data download is completed. The upper level instructions need to provide the CRC value, start address, and length of the download data.

CRC verification cannot be performed under MMU sealing conditions.

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x32 Level-1 command field							
1(CMD_L)	Level-2 command field: Parity partition number							
2~3(LEN)	Length of data sent							
4~7(Par)	32-bit CRC check value							
8~23(DAT)	DAT[0~15] : 16 bytes Key authentication value of USER1/3 partition authentication							
24~27(DAT)	DAT[16 to 19] : Check start address							
28~31(DAT)	DAT[20~23] : Check length (unit: byte, minimum length 512B)							

- CMD_L: Check partition number

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1) 0x00=Main FLASH

2) 0x04=SRAM; Support address range 0x20000500~0x20017FF.

3) 0x05=FLASH+Option byte (After downloading the FLASH data, BOOT automatically writes the CRC32 checksum value of the FLASH download data to the corresponding position in the option byte (0x1FFFF61A~0x1FFFF621).

- LEN Send data length: 0x18(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8);
- Par [0~3] : 32 bit CRC check value, the synthetic rules for CRC32 = Par[0] | Par[1]<<8 | Par[2]<<16 | Par[3]<<24;
- DAT[0:15] : reserve(0);
- DAT [] 16 ~ 19: check the starting address, the synthesis rules to Address = DAT[16] | DAT[17]<<8 | DAT[18]<<16 | DAT[19]<<24, the Address is only within the scope of the FLASH;
- DAT [20 to 23] : check length, its synthesis rules for CRC_LEN = DAT[20] | DAT[21]<<8 | DAT[22]<<16 | DAT[23]<<24, CRC_LEN is only within the effective range, length is larger than 512B, and is a multiple of 16;

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x32 Level-1 command field							
1(CMD_L)	Level-2 command field: Parity partition number							
2~3(LEN)	Length of data sent							
(DAT)	None							
4(CR1)	Status byte 1							
5(CR2)	Status byte 2							

- LEN Send data length: 0x00(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- Status bytes (CR1 and CR2) are divided into the following types according to command execution:

1. Check succeeded: status flag bit (0xA0, 0x00).
2. Check failure: status flag bits (CR1, CR2)

(1) (0xB0, 0x00) : Return failure;

(2) (0xB0, 0x34) : CRC check address range is out of bounds (Refers to exceeding the entire FLASH size);

(3) (0xB0, 0x35) : CRC check address is not 16-byte alignment;

(4) (0xB0, 0x36) : the CRC check length is not a multiple of 16, or the CRC check length is less than 512B.

(5) (0xB0, 0x38) : CRC check fails;

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The CRC32 model is as follows:

The CRC software implementation code is as follows:

```
u32 CRC32_Calculate(u32* data,u32 len)
{
    u32 crc=0xffffffff, xbit=0,data0=0,i=0,j=0;
    u32 polynomial = 0x04c11db7;
    for(i=0;i<len;i++)
    {
        xbit = 0x80000000;
        data0 = *data++;
        for(j=0;j<32;j++)
        {
            if(crc & 0x80000000)
            {
                crc= (crc<<1)^polynomial;
            }
            else
            {
                crc<<=1;
            }

            if(data0 & xbit)
            {
                crc ^= polynomial;
            }
            xbit >>= 1;
        }
    }
    return crc;
}
```

2.2.6 CMD_OPT_RW

This command is used for option byte read and write (including read protection level, FLASH page write protection, Data0/1 configuration).

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x40 Level-1 command field							

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1(CMD_L)	Level-2 command field
2~3(LEN)	Length of data sent
4~7(Par)	Reserve(0)
8~20(DAT)	Option byte configures 13 bytes
21~24(CRC32)	CMD_L = 0 :CRC32: 4 bytes 0x00 CMD_L = 1/2: empty

- CMD_L Level-2 command field:
  1) 0x00: Gets option bytes + FLASH CRC32 Value.
  2) 0x01: Configuration option byte.
  3) 0x02: Configuration option byte, reset again.
- LEN Send data length: 0x10(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- DAT[0~12] : Option bytes configures 13bytes
  - RDP、USER4、USER0[7:0]、USER0[15:8]、USER1[7:0]、USER1[15:8]、USER2、USER3、Data0、Data1、WRP0、WRP1、RDP2;
    1) CMD_L = 0x00: all values are 0x00.
    2) CMD_L = 0x01/0x02: Configuration option bytes are the values to be written.
- CRC32[0~3]：

  CMD_L = 0: CRC32: 4 bytes 0x00

  CMD_L = 1/2: empty

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x40 Level-1 command field							
1(CMD_L)	Level-2 command field							
2~3(LEN)	Length of data sent							
4~16(DAT)	Option byte configures 13 bytes							
17~20(CRC32)	CMD_L = 0 ： CRC32: 4bytes CMD_L = 1/2： empty							
21(CR1)	Status byte 1							

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22(CR2)	Status byte 2

- LEN Send data length: 0x10(LEN[0]), 0x00(LEN[1]), LEN = LEN[0] + (LEN[1]<<8).
- DAT[0~12] : The current option byte configuration is 16 bytes
  - RDP、USER4、USER0[7:0]、USER0[15:8]、USER1[7:0]、USER1[15:8]、USER2、USER3、Data0、Data1、WRP0、WRP1、RDP2;
- CRC32[0~3]：

  CMD_L = 0 ： CRC32: 4bytes

  CMD_L = 1/2：empty

- Status bytes (CR1 and CR2) are divided into the following types according to command execution:
  1. Return success: status flag bit (0xA0, 0x00).
  2. Check failure: status flag bits (CR1, CR2)
     1) (0xB0, 0x00) : return failure;

2.2.7 CMD_SYS_RESET

This command is used to reset the BOOT program.

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x50 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent							
4~7(Par)	Reserved							
(DAT)	None							

- Reserved value: 0x00;

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x50 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent							
(DAT)	None							
4(CR1)	Status byte 1							

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5(CR2)	Status byte 2

- Status bytes (CR1 and CR2) are divided into the following types according to command execution:
  1) Return success: status flag bit (0xA0, 0x00).
  2) Return failure: status flag bits (0xB0, 0x00).

2.2.8 CMD_APP_GO

This command is used to jump to the FLASH reset program entry address (0x0800-0000) after BOOT downloads the application program to FLASH, or to jump to the SRAM reset program entry address (the entry address location is determined by the user's actual download) after BOOT downloads the application program to SRAM. SRAM supports user use of address range 0x20000500~0x20017FF.

Upper-level instructions:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x51 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent							
4~7(Par)	Reserved							
(DAT)	None							

- CMD_L：Jump partition number

1. 0x00 = Flash；
2. 0x01~0x03，Reserve
3. 0x04 = SRAM；Support address range 0x20000500~0x20017FF。

- LEN Sending data length：0x00(LEN[0])、0x00(LEN[1])，LEN = LEN[0] + (LEN[1]<<8)
- Par[0~3]：The starting address of the jump, the synthesis rule is Address = Par[0] | Par[1]<<8 | Par[2]<<16 | Par[3]<<24。
- Reserve：0x00；

Lower layer response:

Byte \ Bit	b7	b6	b5	b4	b3	b2	b1	b0
0(CMD_H)	0x51 Level-1 command field							
1(CMD_L)	0x00 Level-2 command field							
2~3(LEN)	Length of data sent							

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(DAT)	None
4(CR1)	Status byte 1
5(CR2)	Status byte 2

- Status bytes (CR1 and CR2) are divided into the following types according to command execution:
  1) Return success: status flag bit (0xA0, 0x00).
  2) Return failure: status flag bits (0xB0, 0x00).

2.3 Returns the status word description

2.3.1 Returns the success status word

Return success: status flag bit (0xA0, 0x00). Indicates that the command issued by the upper layer is executed successfully, and returns a success status word.

Contains the success return value of the read, update, configure, and other commands.

2.3.2 Returns the failure status word

Return failure: status flag bits (0xB0, 0x00). Indicates that the command issued by the upper layer fails to execute due to other reasons (command acceptance format error or timeout, etc.), and the failure status word is returned.

2.3.3 Return other status words

The following return status words also return failure. The second byte status word indicates a different error type.

(1) (0xB0, 0x30) : Erase/download FLASH page protected by RDP;

(2) (0xB0, 0x31) : Erased/downloaded FLASH page is protected by WRP;

(3) (0xB0, 0x34) : The address range of erase/download /CRC is out of bounds (refers to the size of the entire flash/sram);

(4) (0xB0, 0x35) : The start address of erase/download /CRC is not 16 bytes aligned;

(5) (0xB0, 0x36) : The length of the downloaded /CRC data is not a multiple of 16.Data length indicates the length of erasing flash/sram, or the length of downloading code to FLASH/SRAM, or the length of checking FLASH CRC values; The CRC check length in the code is less than 512B;

(6) (0xB0, 0x37) : Failed to erase/download FLASH/SRAM programming;

(7) (0xB0, 0x38) : CRC check failed.

(8) (0xB0, 0x43) : BOOT power on self verification error;

(9) (0xBB, 0xCC) : Upper-layer send commands Level-1 and level-2 command fields do not belong to any command.

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3 BOOT Instructions

3.1 Upper computer control process

The upper computer supports users to erase the FLASH area, download user codes, and verify the integrity of downloaded codes.

Download user code in plaintext on the upper computer.

The upper computer supports users to update option byte reading and modification.

The upper computer supports software reset commands and execution commands to jump to the FLASH/SRAM reset program entry address.

Enter BOOT: Enter BOOT, you can interact with PC TOOL through UART1 interface at this time.

Chip firmware integrity check: If you choose to start from the system storage area, BOOT automatically performs integrity self-checking. If the check fails, it will enter an infinite loop, and subsequent functions cannot be used..

Command set interaction: The PC TOOL sends different commands based on the command set supported by the BOOT to use corresponding functions.

1) Read BOOT version number, chip model index, chip ID;
2) Erase FLASH;
3) Download user programs to FLASH;
4) CRC check downloaded user program;
5) Read/configure option bytes (including read protection level, FLASH page write protection, Data0/1 configuration);
6) System reset, you can reset the BOOT program to run again;
7) Jump to the entry address of the reset program for Main Flash/SRAM, and then to the entry address of the reset program for downloading the Main Flash/SRAM partition code.

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4 Version history

Version	The revision date	Remark
V1.0.0	2025/8/21	Initial release

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