N32H7xx series Hardware Design user guide

Introduction

This document details the hardware design checklist for the N32H7xx series MCUs, so as to provide hardware design guidance for users.

Content

1 Hardware Design Checklist for N32H7xx Series MCU

1.1 Power Supply Overview

The operating voltage (VDD) of N32H7XX series chips ranges from 2.3V to 3.63V. The main external power supply pins include VDD, VDD33_USB, VCAP, VDDA, VREF and VBAT.

- VDD: The main chip power supply, primarily powering the power supply system, clock system and I/O ports.
- VDDA: The analog peripheral power supply, mainly powering analog peripherals.
- VDD33_USB: The dedicated power supply for USB modules.
- VCAP: The core power supply of the chip.
- VREF: Provides reference voltage for analog peripherals to ensure higher precision.
- VBAT: Connects to a battery and supplies power to the backup domain.

For detailed descriptions of the power supply pins, please refer to the relevant chip datasheet.
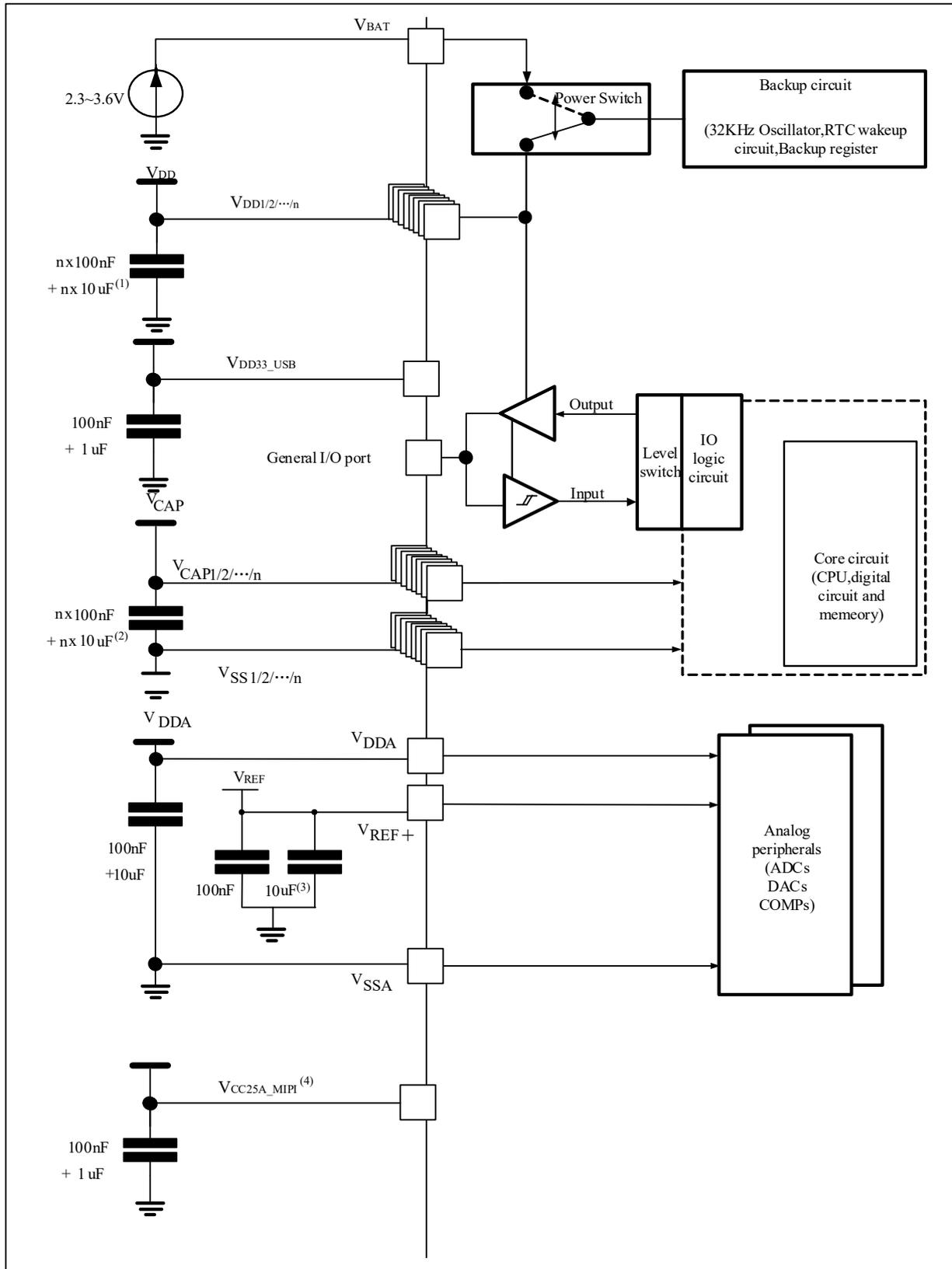
1.2 Power Supply Scheme

Figure 1-1 Power Supply Scheme

In Figure 1-1，the 10 μF capacitor in the power supply scheme must be connected to the specified VDD pins. For the specific designated VDD pins of each chip model, please refer to the table below:

Model	Package	VDD	VCAP
H730 H760	BGA100	Place a combination of 10uF + 0.1uF capacitor close to the chip, place a 0.1uF capacitor near each VDD pin	Place a 20uF + 0.1uF close to the chip, and place 0.1uF near each VCAP pin
	LQFP100	Place 10uF + 0.1uF at pin27 and pin75, and place 0.1uF at the remaining VDD pins.	Route the external power supply to Pin 48 and Pin 73 as a priority, and place a 10μF + 0.1μF capacitor near each respective pin..
	LQFP144	Place 10uF + 0.1uF at pin39 and pin108, and place 0.1uF at the remaining VDD pins.	Route the external power supply to Pin 71 and Pin 106 as a priority, and place a 10μF + 0.1μF capacitor near each respective pin.
H762	LQFP176	Place 10uF + 0.1uF at pin49 and pin127, and place 0.1uF at the remaining VDD pins.	Route the external power supply to Pin 81 and Pin 125 as a priority, and place a 10μF + 0.1μF capacitor near each respective pin
	BGA240+25	Place 10uF + 0.1uF close to the chip, and place 0.1uF near each VDD pin.	Place a 20μF + 0.1μF capacitor close to the chip first, and a 0.1μF capacitor near each VCAP pin.
H735 H735EC H765 H765EC	LQFP144_DCDC	Place 10uF + 0.1uF at pin42 and pin106, and place 0.1uF at the remaining VDD pins..	In addition to placing 2*10uF + 0.1uF at the output inductor position, also place 0.1uF at pin68, pin105 and pin140 respectively.
	LQFP176_DCDC	Place 10uF + 0.1uF at pin48 and pin136, and place 0.1uF at the remaining VDD pins	In addition to placing 2*10uF + 0.1uF at the output inductor position, also place 0.1uF at pin80, pin133 and pin172 respectively.
	BGA176+25	Place 10uF + 0.1uF close to the chip, and place 0.1uF near each VDD pin.	Place 2*10uF + 0.1uF at the output inductor position
H785 H785EC	LQFP176_DCDC	Place 10uF + 0.1uF at pin48 and pin136, and place 0.1uF at the remaining VDD pins..	In addition to placing 10uF + 0.1uF at the output inductor position, also place 10uF + 0.1uF at pin80, pin133 and pin172 respectively.
	BGA176+25	Place 10uF + 0.1uF close to the chip, and place 0.1uF near each VDD pin	Place 2*10uF + 0.1uF at the output inductor position
	BGA240+25	Place 10uF + 0.1uF close to the chip, and place 0.1uF near each VDD pin.	Place 2*10uF + 0.1uF at the output inductor position
H787	BGA240+25	Place 10uF + 0.1uF close to the chip, and place 0.1uF near each VDD pin.	Place 2*10uF + 0.1uF at the output inductor position

Table 1-1 Design Reference for Power Supply Decoupling Capacitors of Each Package

There are 4 power domains, which are powered by external power supplies respectively:

- VDD Domain: The voltage range is 2.3V~3.63V, mainly powering most GPIOs, HSE, HSI, PLL, POR/PDR, BOR and PVD.
- VDD33_USB Domain: The voltage range is 1.8V~3.6V, dedicated to powering the USB PHY.
- VDDA Domain: The voltage range is 2.3V~3.63V, mainly powering ADC, DAC, COMP, VREFBUF, TS and other peripherals.
- VCAP Domain: The voltage range is 0.9V~0.99V (including power supply ripple), mainly powering the CPU, AHB, APB, SRAM, FLASH, RCC, TRNG and most peripherals.

Note: When the VCAP domain is powered by an external LDO, it is required to ensure that the VDD voltage drops below 1V first before powering off the VCAP domain.

To ensure the power-off sequence of VDD and VCAP, the recommended power supply mode when VCAP is powered by an external LDO is as follows:

External 0.9V VCAP supply
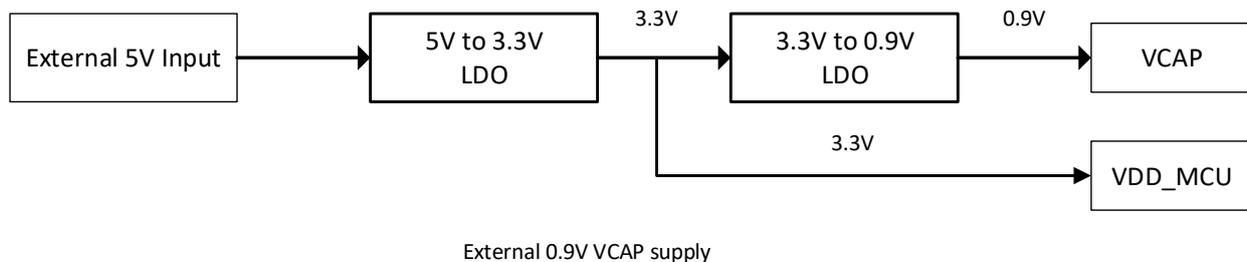
LDO Selection Requirements: 0.9V/1A (@25℃)

When the input voltage is 1.45V, it shall still output 0.9V with a current of at least 200mA.

At a high temperature of 105℃ @ 3.6V, the output current shall be at least 1A.

Recommended Model: RT2516GSP

For VCAP Powered by Internal DCDC, the Recommended Circuit is as Follows:
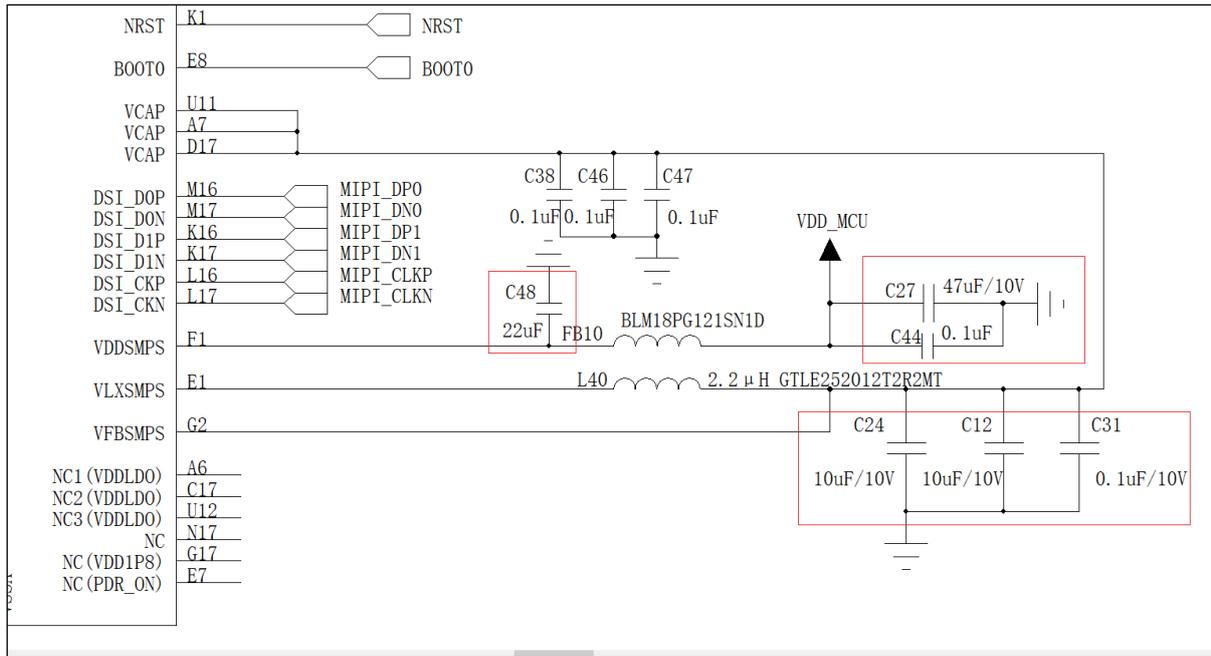
Note: The temperature coefficient of the input and output capacitors in the figure is recommended to be of the X7R type.

VDD is the main power supply of the MCU and must be powered by a stable external power source. Its voltage range is 2.3V~3.63V. A 0.1 µF decoupling capacitor must be placed close to each VDD pin; in addition, a 10 µF decoupling capacitor shall be added to the designated VDD pins. For specific designated VDD pins, please refer to Table 1-1 Design Reference for Power Supply Decoupling Capacitors of Each Package.

VDDA is the analog power supply. It is recommended to place a 0.1 µF capacitor and a 10 µF capacitor close to the VDDA input pin.

VREF+ is the reference voltage, providing reference level for ADC and DAC.When the built-in reference source VREFBUF is used for VREF+, it is recommended to place a 0.1 µF capacitor and a 1 µF capacitor close to the VREF+ pin.When VREF+ is powered by an external power source, it is recommended to place a 0.1 µF capacitor and a 10 µF capacitor close to the VREF+ pin.

The VBAT pin mainly supplies power to the backup domain (RTC, IWDG, Backup SRAM). When the main power supply (VDD) is turned off, the power switch can switch the power supply of the backup domain to the VBAT pin, so that the backup domain modules can still operate normally.

VCAP is the core power supply of the chip:

1.2.1 VCAP Power Supply for N32H735/N32H765/H78X Series Chips

（1） VCAP Powered by the Chip's Internal DCDC
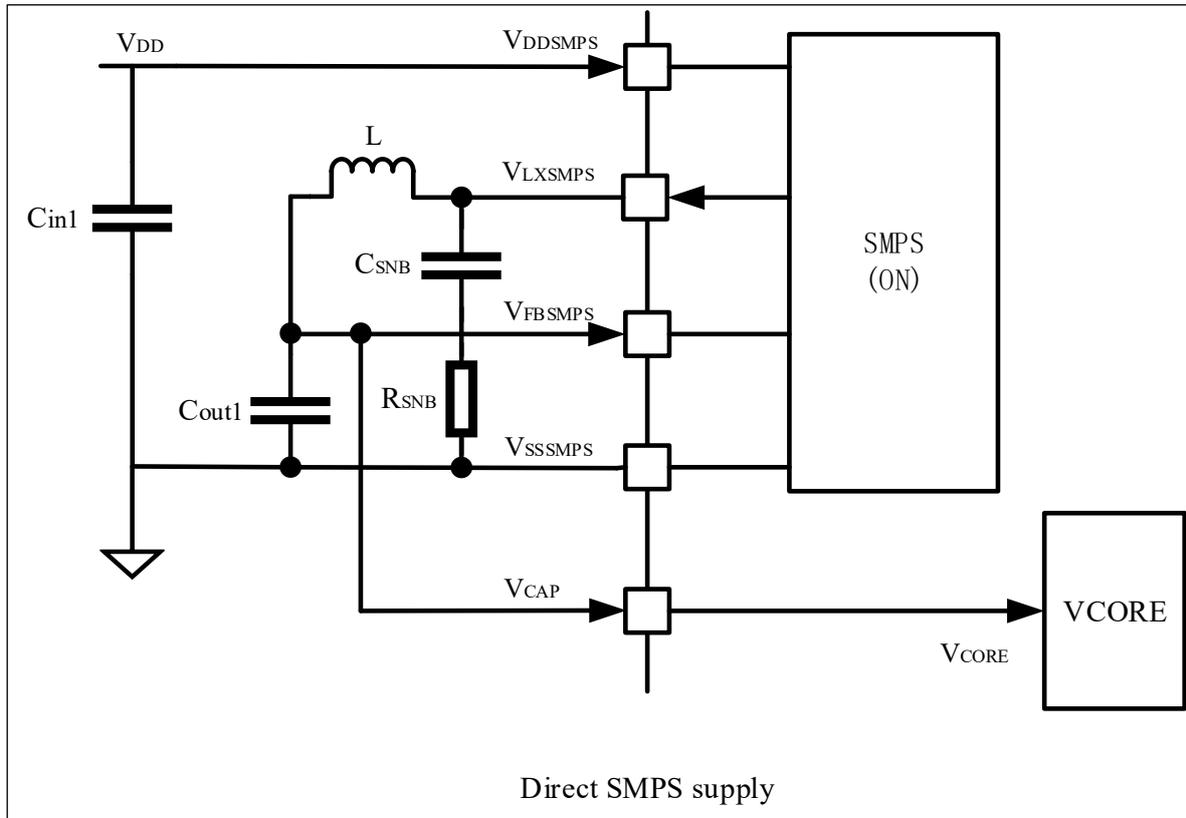
Figure 1-2 VCAP Powered by Internal LDO

Notes:

1. **Inductor L: inductance value = 2.2 µH, saturation current = 2~3 A.**

2. **C_{SNB} and R_{SNB} form an optional RC snubber circuit, which can reduce switching ringing and suppress EMI.**

（**2**）　**VCAP Powered by an External 0.9V Supply**
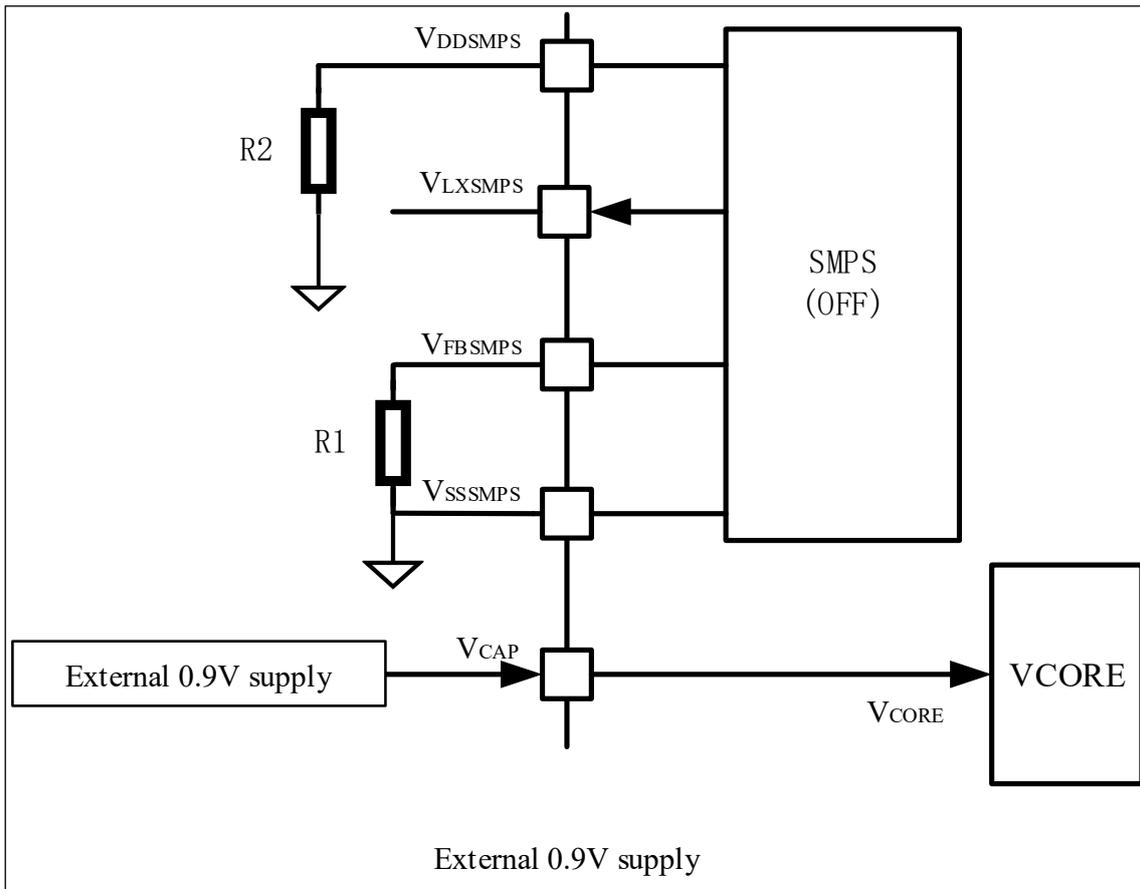
Figure 1-3 VCAP Powered by External LDO

Notes:

1. **When the DCDC power supply mode is not used, the VDDSMPS and VFBSMPS pins shall be pulled down to ground through 0Ω resistors to prevent leakage current.**

2. **For the scenario where VCAP is powered by an external power supply, the external power supply is required to stably output 0.9V when the input voltage is 1.45V or higher. The power supply voltage range of VCAP is 0.9V~0.99V (including power supply ripple).**

1.2.2 **VCAP Power Supply for N32H730/H760/H762 Series Chips**

（1） VCAP Powered by an External 0.9V Supply
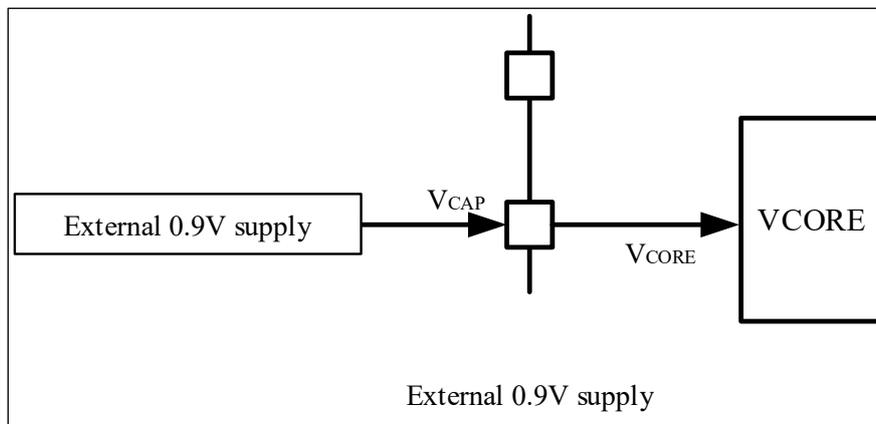
Figure 1-4 VCAP Powered by External Supply

Notes:

1. **For the scenario where VCAP is powered by an external supply, the external supply is required to stably output 0.9V when the input voltage is 1.45V or higher. The power supply voltage range of VCAP is 0.9V~0.99V (including power supply ripple).**

1.3 **Backup Battery**

The VBAT pin mainly supplies power to the backup domain (RTC, IWDG, Backup SRAM), ensuring that the backup domain modules can still operate normally when the main power supply (VDD) is turned off. If no external battery is used in the application, the VBAT pin must be externally connected to VDD.

1.4 **External Pin Reset Circuit**

A low level on the NRST pin (external reset) will trigger a system reset. The reference circuit for the external NRST pin reset is shown below.
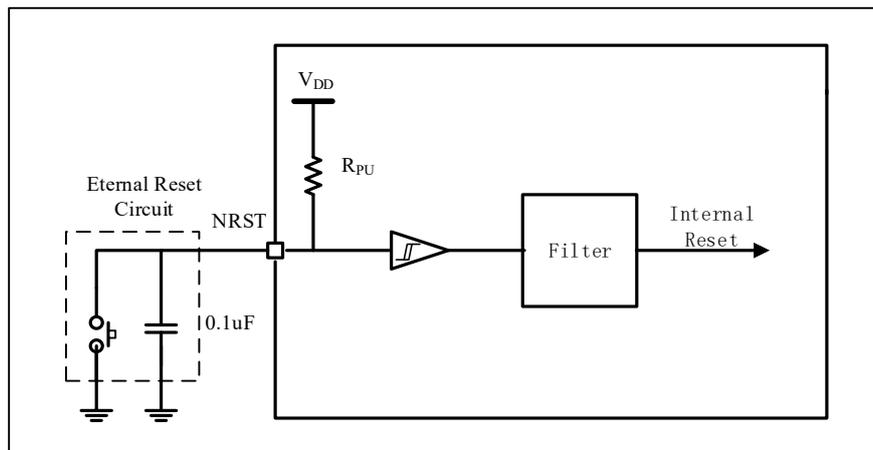
Figure 1-5 System Reset Diagram

Note: It is recommended that the reset pin NRST should not be left floating during design. An external 0.1 μF capacitor is provided as a typical reference value. If the reset time needs to be shortened, the NRST pin can be externally pulled up. In addition, users can decide whether to add a reset button according to the actual product requirements.

1.5 **External Clock Circuit**

The N32H7xx series MCUs include two external clocks: the High-Speed External Clock (HSE) (4MHz~48MHz) and the Low-Speed External Clock (LSE) (typically 32.768KHz).

Corresponding load capacitors for HSE and LSE shall be configured according to the crystal oscillator characteristics. For details, refer to the description of external clock characteristics in the relevant datasheet.

1.6 **Boot Pin Connection**

The figure below shows the external connections required for the N32H7xx series chips to select the boot memory. For details about the boot modes, refer to the relevant chapter in the user manual.
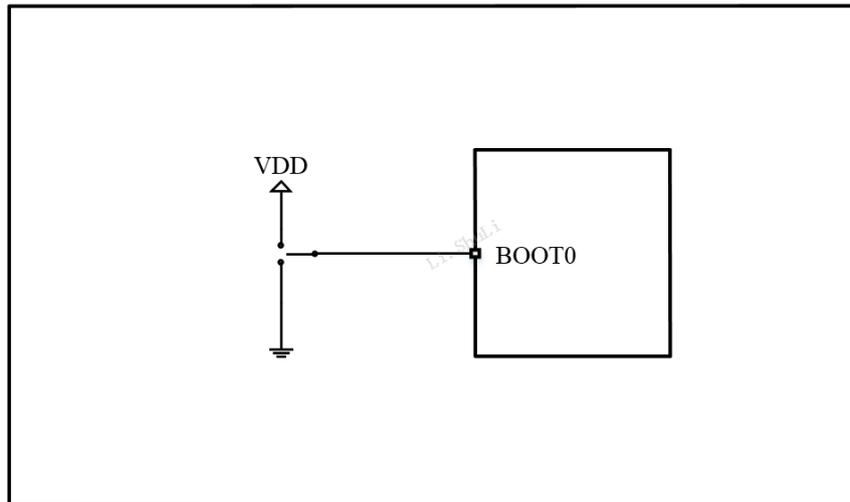
Figure 1-6 Implementation Example of Boot Modes

When the BOOT pin is pulled high, the chip boots from the BOOT area after reset; when the BOOT pin is pulled low, the chip boots from the user area after reset. For boot modes, refer to the BOOT Configuration chapter in the Software Development Guide.

1.7 ADC Converter

For the design of the ADC circuit, please note the following points:

1) When using ADC sampling, it is recommended to shorten the external trace length of the ADC sampling channels.

2) It is recommended to keep the ADC input signals away from high-frequency switching signals.

3) Pay attention to the maximum supported rate of the ADC sampling channels:

   For the N32H7xx series, when the ADC input clock is 20 MHz, the sampling rate of the ADC channels shall not exceed 5 Msps.

4) During ADC conversion, the chip does not support modifying the ADC configuration. If configuration modification is required, wait for the current conversion to complete or turn off the ADC before proceeding with the configuration.

5) When using a specific ADC channel, do not apply a negative voltage (e.g., -0.2 V) to other unused ADC sampling channels. Applying such a negative voltage will pull down the voltage of the normally sampling ADC channel, resulting in inaccurate read data.

6) When using a specific ADC channel, do not apply a high voltage (greater than the VDD voltage) to other unused ADC sampling channels. Applying such a high voltage will pull up the voltage of the normally sampling ADC channel, resulting in inaccurate read data.

7) When using the ADC, the sampling rate of the ADC is related to RAIN—the smaller the RAIN value, the faster the sampling rate. For details, refer to the table below.
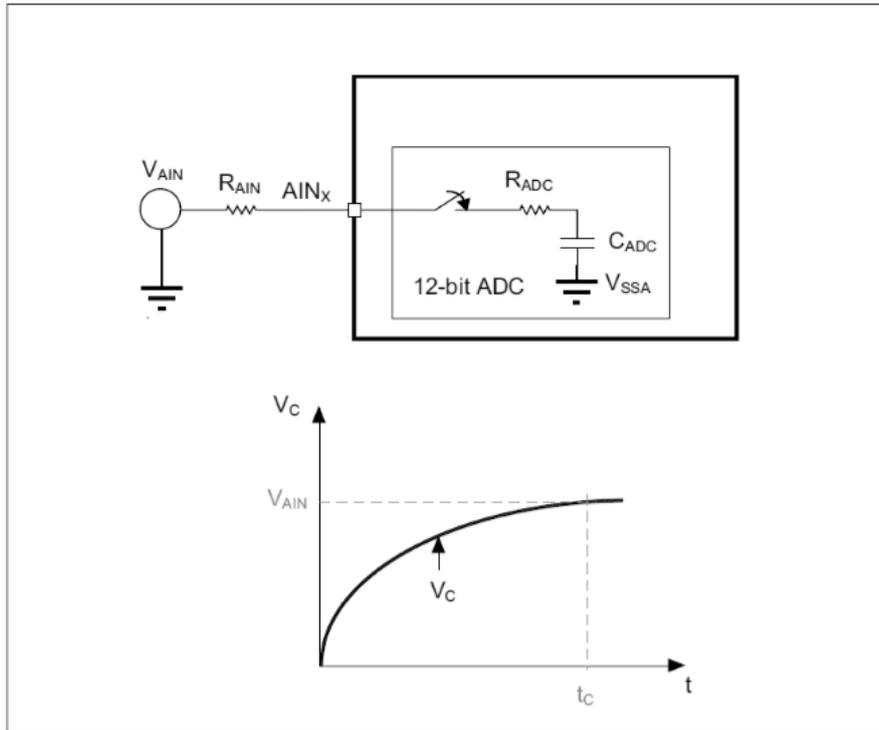
Figure 1-7 Impact of Series Resistors on ADC Input Pins

ADC Sampling Schedule:

Resolution	Rin（kΩ）	Minimum Sampling Time（ns）
12-bit	0	50
	0.45	100
	0.7	150
	0.95	200
	1.95	400
	2.95	600
	3.95	800
	4.95	1000
	9.95	2000

Table 1-2 ADC Sampling Schedule

Note: The sampling time shall be configured comprehensively based on the input clock and the optional sampling cycles of the ADC registers. In principle, the configured ADC sampling cycles should be greater than or equal to the minimum number of sampling cycles in the table.

1.8 Design Recommendations for High-Speed Communication Interfaces

1.8.1 USBHS Interface

1. The DPDM traces shall be impedance-controlled, with the differential impedance set to 90Ω±10%.

2. The DPDM traces require length matching, and the length difference of the differential pair shall be controlled within ±5 mil.

3. The DPDM traces shall be routed symmetrically; avoid right-angle bends to reduce impedance discontinuities.

4. Add an ESD diode near the connector on the DPDM lines to prevent electrostatic damage.

5. Ensure a continuous reference ground plane exists beneath the DPDM differential lines; avoid crossing ground splits to reduce return path interference.

6. Route the DPDM traces away from high-frequency noise sources such as power supplies and clock signals as much as possible, and add shielding ground vias around the differential lines.

7. When using the USBHS module, an external HSE crystal must be used as the clock source, and the HSE frequency shall be limited to 10MHz, 12MHz, 19.2MHz, 24MHz, 25MHz, 27MHz, 30MHz, or 40MHz.

1.8.2 MIPI Interface

1. The MIPI traces shall be impedance-controlled, with the differential impedance set to 100Ω±10%.

2. The MIPI traces require length matching: the length error within a differential pair shall be controlled within 5 mil, and the length error between differential pairs shall not exceed 10~20 mil; serpentine routing can be used for length adjustment.

3. The MIPI traces shall be routed symmetrically; avoid right-angle bends to reduce impedance discontinuities.

4. Ensure a continuous reference ground plane exists for the MIPI traces; avoid crossing ground splits to reduce return path interference.

5. Minimize the number of vias for MIPI traces (no more than 2 is recommended). When changing layers, drill vias symmetrically and add return ground vias nearby to optimize the signal return path; small-diameter vias are recommended to reduce the impact of parasitic capacitance.

6. Route the MIPI traces away from other high-speed signals as much as possible, maintaining a spacing of at least 3 times the trace width; avoid parallel routing, and add shielding ground vias around the differential lines.

7. Provide an independent power plane for the MIPI module, and add decoupling capacitors near the power pins to reduce power supply noise.

1.8.3 EtherCAT / ETH Interface

1. For the differential signal pairs (TXP/TXN, RXP/RXN), the differential impedance shall be controlled to 100Ω±10%, and the length difference within the same differential pair shall be controlled within 5 mil to maintain signal symmetry and reduce common-mode noise and timing deviations. The overall length difference between the transmit (TXP/TXN) and receive (RXP/RXN) differential pairs is recommended to be controlled within 50 mil to avoid inconsistent communication delays across nodes.

2. Length matching is required between the clock lines and data lines of the interface signals:
   - For the EtherCAT interface: TX_CLK and TX[3:0], RX_CLK and RXD[3:0] shall be length-matched

within their respective groups, with the length difference controlled within 50 mil.

- For the ETH GMII interface: TX_CLK and TX[7:0], RX_CLK and RXD[7:0] shall be length-matched within their respective groups, with the length difference controlled within 5 mil.

3. For the management interface signals (MDC and MDIO), the length difference is recommended to be ≤ 100 mil; pull-up resistors shall be added during use to avoid configuration timing anomalies.

4. The differential pair traces shall reference a continuous ground plane throughout the entire route; avoid crossing ground splits or changing layers.

5. Avoid right-angle routing to reduce impedance discontinuities; serpentine routing can be used for length adjustment.

6. Place the crystal oscillator as close to the PHY chip as possible, and route the clock signal with ground shielding to reduce radiation interference.

1.8.4 SDRAM Interface

1. For the chip select pins of SDRAM, it is recommended to prioritize SDRAM_NCE0 and SDRAM_CKE0; this configuration allows SDRAM to both run code and perform data read/write operations. When SDRAM_NCE1 and SDRAM_CKE1 are selected, only SDRAM data read/write operations are supported.

2. Keep the power plane as continuous as possible to reduce impedance. Add decoupling capacitors close to the power pins to lower power supply noise.

3. Route the clock signal CLK first to maintain the shortest path, and keep it away from other high-speed signals.

4. The data lines (DQ0~DQ15, LQDM, UDQM) shall be length-matched within the group, with the length difference controlled within 50 mil.

5. The address lines (A0~A12, BS0, BS1) shall be length-matched within the group, with the length difference controlled within 100 mil.

6. The control signal lines (CS/RAS/CAS/WE) shall be length-matched within the group, with the length difference controlled within 100 mil.

7. The length difference between the address/control lines and the CLK clock line shall be controlled within 100 mil.

8. Adopt a continuous ground plane, avoid crossing ground splits, and ensure a low-impedance return path.

9. A 22~33 Ω resistor can be terminated to the address lines, control lines, data lines and CLK signal to reduce signal reflection and improve signal integrity.

1.9 **Power-On Pulse Handling for I/O Pins**

During the power-on sequence, due to the high-impedance state of I/O pins and the coupling characteristics of internal circuits, a high-level pulse may occur on the I/O pins instantaneously (users are advised to measure the actual voltage value of the high pulse). If this pulse affects the application, it is recommended to connect an appropriate capacitor (1 nF~100 nF) or an external pull-down resistor (10 kΩ~100 kΩ) to the corresponding I/O pin for suppression.

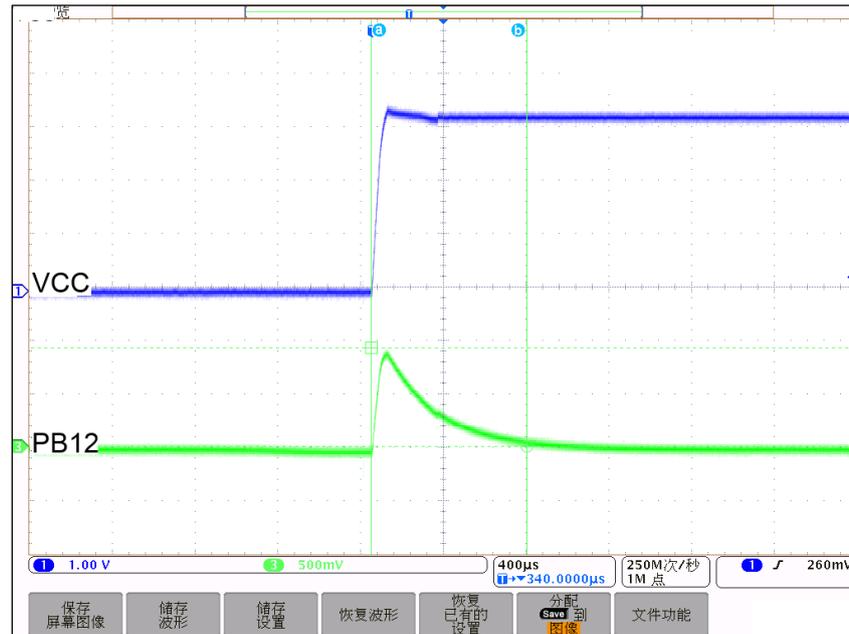The following figure shows the I/O (PB12) waveform during power-on of the development board N32H760VIB7_STB_V1.0:

Figure 1-8 I/O (PB12) Waveform During Power-On

The following figure shows the I/O (PB12) waveform after connecting a 10 kΩ pull-down resistor during power-on of the development board N32H760VIB7_STB_V1.0:
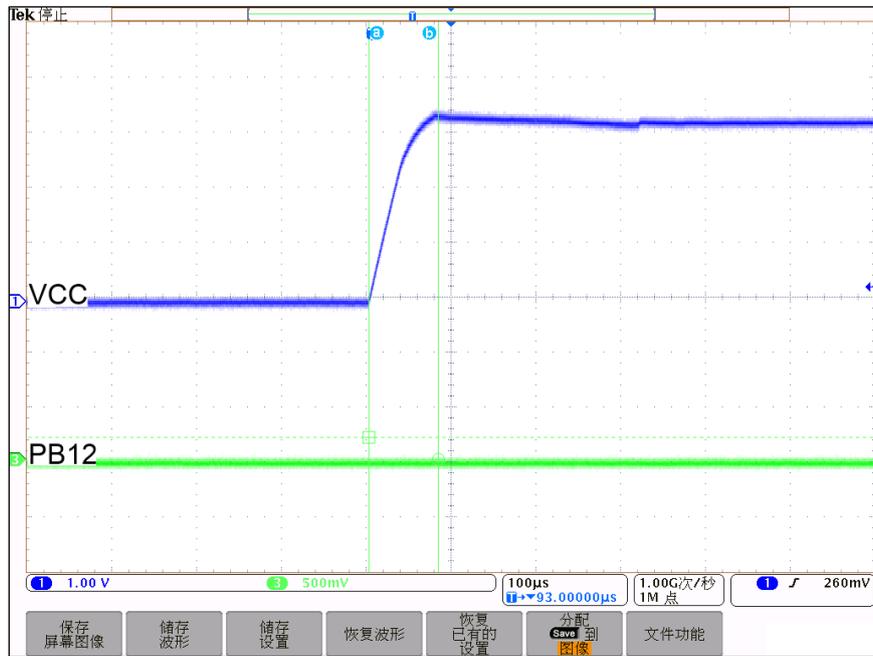
Figure 1-9 I/O (PB12) Waveform After External Pull-Down Resistor Treatment During Power-On

16

1.10 I/O Voltage Withstand Rating

When using the chip, please pay attention to the voltage withstand rating of each I/O pin. In the I/O Structure column of the pin multiplexing definition in the datasheet, the label FT: 5V tolerant IO is marked. For this type of I/O pin, level shifting is required when communicating with external I/O pins of different voltage domains.

Package			Pin Name	Type[1]	I/O Structure[2]	Fail-safe[3] Aternate Functions	Support Optional Multiplexed Functions	
LQFP144	TFBGA100	LQFP100					Aternate Functions	Additional Functions
1	A3	1	PE2	IO	TT	Yes	TRACECLK SPI6_SCK ETH1_MII_TXD3/ETH1_GMII_TXD3 GTIMB1_ETR DVP2_D0 FEMC_A23 USART5_RX FDCAN4_TX	-
2	B3	2	PE3	IO	TT	Yes	TRACED0 ETH1_MII_TXD2/ETH1_GMII_TXD2 GTIMB1_BRK DVP2_D1 FEMC_A19 USART5_TX FDCAN4_RX	-

Figure 1-10 I/O Structure in Pin Multiplexing Definition of Datasheet

Note: FT: 5V tolerant IO; TT: 3.3V standard IO. Please pay attention to the voltage withstand rating of the I/O pins when using the chip.

1.11 ESD Protection Design

1.11.1 PCB Design

For PCB design of standard two-layer boards, it is recommended to implement ground shielding around signal lines, and the board edges should be surrounded by ground planes as much as possible. If cost permits, four-layer or multi-layer PCBs are preferable for design. In multi-layer PCBs, the ground plane serves as a crucial charge sink that can neutralize charges from electrostatic discharge (ESD) sources, which helps mitigate issues caused by electrostatic fields. The PCB ground plane can also act as a shield for signal lines (note that the larger the opening in the ground plane, the lower its shielding effectiveness). In addition, if a discharge occurs, the large area of the PCB ground plane allows charges to be easily dissipated into the ground instead of coupling into signal lines. This helps protect components because charges can be discharged before they cause component damage.

1.11.2 ESD Protection Devices

In practical product design, the chip itself has a certain level of ESD immunity. The N32H7xx series MCUs have an ESD rating of ±4 kV under the Human Body Model (HBM). However, if a higher ESD protection level is required, and certain chip pins need to be directly connected externally as product I/O ports, these pins will be exposed on the

outermost part of the product and cannot be isolated by means such as ground planes. Under such circumstances, external ESD protection devices are generally required. The TVS diode is a typical ESD protection device, and a typical connection scheme is shown below.
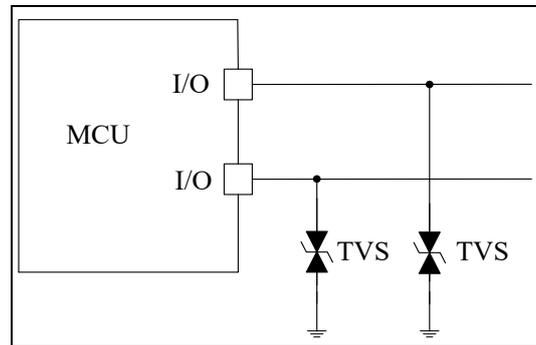
Figure 1-11 TVS Connection Method on I/O Pins

1.12 Debug Interface

The N32H7xx series chips support the Serial Wire Debug (SWD) and JTAG debug interfaces. For detailed application, please refer to the relevant user manual.

Debug Signal	GPIO Pin
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
JNTRST	PB4

Table 1-3 Debug Interface

1.13 BOOT UART Interface

The N32H7xx series chips support BOOT UART communication. The UART interface is shown in the table below:

BOOT USART	GPIO Pin
USART1_TX	PA9
USART1_RX	PA10

Table 1-4 USART Interface

1.14 Design Considerations for Each Module

1.14.1 SDRAM

For the chip select pins of SDRAM, it is recommended to prioritize SDRAM_NCE0 and SDRAM_CKE0; this configuration allows SDRAM to both run code and perform data read/write operations. When SDRAM_NCE1 and SDRAM_CKE1 are selected, only SDRAM data read/write operations are supported.

1.14.2 SDMMC

1) When using an SD card, it is necessary to design an NRST pin to power on/off the SD card via I/O pull-up and pull-down. This avoids I/O voltage mismatch between the MCU side and the card side caused by MCU reset without the card being powered off.

2) The CLKIN pin is mandatory. The design shall reserve this pin to form a loop with the CLK pin. There are two loop modes: external loop and internal loop. An external loop requires connecting the external pins together, while an internal loop can be enabled via the function AFIO_SDMMCClkSel.

1.14.3 USBHS

When using the USBHS module, an external HSE crystal must be used as the clock source, and the HSE frequency shall be limited to 10 MHz, 12 MHz, 19.2 MHz, 24 MHz, 25 MHz, 27 MHz, 30 MHz or 40 MHz.

1.14.4 VREFBUF

When the internal reference source VREFBUF is enabled, no external voltage shall be connected to the VREF+ pin.

1.14.5 I2C

When the VIH (Input High Voltage lower threshold) of the I2C device selected by the user is below 1.5V, the following I2C I/Os are recommended:

I2Cx	SDA	SCL
I2C1	PG4,PD5,PB7	PG5,PD4,PB6
I2C2	PF0,PH5,PB11	PF1, PB10
I2C3	-	PH7,PK0
I2C4	PF15,PH12,PD13,PB7	PF14, PD12,PB6
I2C5	PF0	PF1, PC11
I2C6	PF3,PF11,PE13	PF4,PF12
I2C7	PI12,PE7,PD8	PI13,PE8
I2C8	PD14, PG4,PI2	PG5,PI3
I2C9	PI10	PI11,PJ1, PH15
I2C10	PJ13,PK3,PK6	PI1, PK4,PK7,PI6

2 Overall Design Recommendations

1) Printed Circuit Board (PCB)

It is recommended to use a multi-layer PCB with a dedicated, independent ground plane (VSS) and a dedicated, independent power plane (VDD) to achieve excellent coupling performance and shielding effectiveness. In practical applications, if cost constraints preclude the use of a multi-layer PCB, the circuit design must ensure a robust grounding and power supply structure.

2) Component Placement

During PCB layout, circuits shall be separated according to the varying EMI impacts of different components—such as high-current circuits, low-voltage circuits, and high-frequency devices—to minimize cross-coupling on the PCB.

3) Grounding and Power Supply (VSS, VDD)

Each module (analog circuits, digital circuits, and low-sensitivity circuits) should have an independent ground connection. Digital grounds and analog grounds must be isolated and finally connected together at a single point.

Based on the current magnitude on the PCB, maximize the width of power supply traces as much as possible to reduce loop resistance. Meanwhile, the routing direction of power and ground traces should align with the current flow direction; power traces should be routed as close to ground traces as possible to minimize the area of current loops. This helps enhance noise immunity.

All empty areas on the PCB should be filled with ground planes to provide optimal shielding effectiveness.

4) Decoupling

All power pins must be properly connected to the power supply. These connections—including pads, traces, and vias—should be designed to have minimal impedance. This is typically achieved by increasing trace width. In addition, a decoupling capacitor must be placed close to the chip for each pair of VDD and VSS pins. The figure below shows a typical layout of power/ground pins.
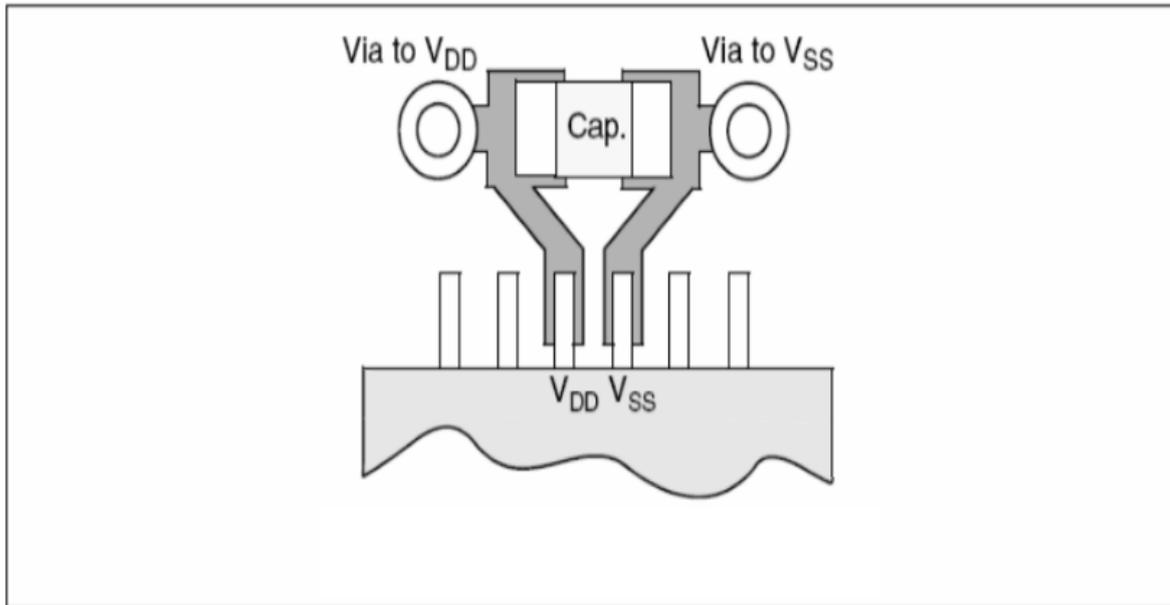
Figure 2-1 Typical Layout of VDD/VSS Pins

22

3 PCB Layout Reference

Figure 3-1 PCB Layout Reference Diagram for LQFP100 Package

Notes:

1. During PCB layout design, a decoupling capacitor must be placed close to each power pin.

2. For the external crystals and traces of HSE and LSE, ground shielding is recommended around them as much as possible. The area of the layer beneath the crystals, which is adjacent to the crystals, shall also be filled with a ground plane. No signal traces are allowed to pass through this area to prevent signal interference with the crystal signals.

3. When HSE and LSE are used as crystal oscillators, their traces should not be excessively long to avoid the antenna effect.

4 History versions

Version	Date	Notes
V1.2.0	2025-8-26	Initial version

5   Disclaimer

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD. (Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to NSING Technologies Inc. and NSING Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections. enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NSING has attempted to provide accurate and reliable information, NSING assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NSING be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product. NSING Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NSING and hold NSING harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NSING, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.