N32H497xG Datasheet

N32H497 series employs a 32-bit ARM Cortex-M4F core operating at a maximum frequency of 240MHz, supporting floating-point operations and DSP instructions. It integrates up to 1MB of embedded Flash, 576KB of SRAM (including 80KB of CCM SRAM) plus 4KB of Backup SRAM. The device incorporates three 12-bit 4.7Msps ADCs, two 12-bit DACs, and integrated communication interfaces including USB FS Device, USB HS Host/Device, U(S)ART, I2C, SPI, CAN-FD, and Ethernet. It supports DVP interfaces, SDIO, FEMC, xSPI, SDRAM high-speed memory interfaces, supports I2S audio interface, supports multiple advanced timers, general-purpose timers, basic timers, low-power timers, built-in cryptographic algorithm hardware acceleration engine, supports AES/TDES, SHA, SM3, SM4, MD5 algorithms, supports TRNG true random number generator, supports CRC16/32.

Key Features

- **CPU Core**
  - 32-bit ARM Cortex-M4F + FPU, single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
  - Built-in 8KB I-Cache (instruction cache) and 1KB D-Cache (data cache), supporting Flash Accelerator Unit for zero-wait program execution
  - Frequency up to 240 MHz, 300 DMIPS
- **Memories**
  - 1MByte on-chip Flash, dual-bank support, enabling secure storage, partition management and data protection, 10,000 erase/write cycles, 10-year data retention
  - 496KB general-purpose SRAM, configurable for ECC support; maximum capacity 448KB when ECC enabled
  - 80KB CCM SRAM, defaulted as general-purpose SRAM, configurable as CCM SRAM, configurable for ECC support, maximum capacity 64KB when ECC enabled
  - 4-KByte of Backup SRAM with ECC available in Standby mode
- **Power Modes**
  - Run mode: All peripherals configurable for operation
  - Sleep Mode: CPU halted, peripherals configurable for operation
  - Stop0 mode: SRAM and all registers can be configured to retention, RTC run
  - Standby mode: 6uA, all backup registers and Backup SRAM retained, all IOs retained, optional RTC run
  - VBAT mode: 4uA, all backup registers and Backup SRAM retained, optional RTC run
- **Clock**
  - HSE: 4MHz~32MHz high-speed external crystal oscillator
  - LSE: 32.768KHz low-speed external crystal oscillator
  - Built-in multiple high speed PLLs
  - MCO: Supports 2-channel clock outputs, which can be configured independently as clock output
  - HSI: High-speed internal RC 8MHz, -1.5% to +2% accuracy (full temperature range)
  - LSI: Low-speed internal RC 32KHz, +/-10% accuracy (full temperature range)

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- **Reset**
  - Supports power-on/brown-out/external pin reset
  - Supports watchdog reset
  - Supports programmable voltage detection
- **GPIOs**
  - Up to 118 GPIOs, PD6 to PD7 and PG9 to PG15 comprise nine I/O pins capable of supporting VDDIO input power supply operation.
- **Communication Interfaces**
  - 1x USB2.0 FS Device interface, built-in PHY, supports crystal-less mode
  - 1 USB High-Speed Host/Device interface, with integrated PHY
  - 6x SPI interfaces, 2x I2S interfaces, support half/full duplex mode, multiplexed with SPI interfaces
  - U(S)ART interfaces
    - 5x USART interfaces (support ISO7816, IrDA, LIN)
    - 5x UART interfaces
    - TX/RX of USART3/UART5/UART8 can be mapped to all pins
  - 4x I2C interfaces(Master/Slave) with speed up to 1 MHz where slave mode support dual address response
  - 3x CAN-FD bus interface, TX/RX can be mapped to all pins
  - 1x IEEE-802.3-2002 compatible Ethernet MAC interface, supports 10M/100M Ethernet, IEEE1588 synchronized Ethernet protocol
  - 1x DVP (Digital Video Port) supporting 8/10/12/16 bit data
- **High Performance Analog Interfaces**
  - 3x 12-bit 4.7 Msps ADCs, supporting 12-bit, 10-bit, 8-bit, and 6-bit sampling precision, with hardware oversampling capability up to 16-bit. ADC1 supports up to 16 external single-ended input channels, while ADC2 and ADC3 support up to 18 external single-ended input channels. Both single-ended and differential modes are supported.
  - 2x 12-bit DACs, each supporting one internal output channel and one external output channel. Sampling rate: 1 Msps. Supports buffered and unbuffered outputs. Capable of internal output, external output, or simultaneous internal and external output.
  - 1x temperature sensor
- **High Speed External Memory Interfaces**
  - 1x xSPI interface, supporting external SRAM, PSRAM and Flash, supporting XIP
  - 1x FEMC (Flexible External Memory Controller) interface, supporting external SRAM, PSRAM, NOR Flash and NAND Flash, 8/16-bit data bus width configurable
  - 1x SDIO interface, support SD/SDIO/MMC format
  - 1x SDRAM interface, configurable 8/16-bit data width
- **Mathematical hardware accelerator CORDIC for motor control functions**
- **Delta Sigma Module Unit (DSMU)**
- **DMA Controllers**

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- 2x DMA controller
- Each controller supports 8 channels
- Channel source address and destination address can be configured arbitrarily

- **RTC real-time clock**
  - Supports leap-year calendar, alarm event, periodic wake up
  - Supports internal and external clock calibration
- **Timers**
  - 3x 16-bit advanced timer/counters supporting input capture, complementary outputs, quadrature encoding inputs, etc., with a maximum control precision of 4.17ns; each timer features six independent channels, four of which support four pairs of complementary PWM outputs
  - 10x general-purpose timers (GTIM1–10):
    - GTIM2/3/5/6/7: 16-bit counters with a maximum control precision of 4.17 ns. Each timer features up to 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output.
    - GTIM1/4: 32-bit counters with maximum control precision of 4.17 ns. Each timer provides up to 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output;
    - GTIM8–10, 16-bit counters with a maximum control precision of 4.17 ns. Each timer features up to four independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output. Only Channel 1 supports complementary outputs with dead time and brake input capability.
  - 2x 32-bit basic timers
  - 2x 16-bit low-power timer, can operate in Stop0 and Standby mode.
  - 1x 24-bit SysTick timer.
  - 1x 14-bit Window Watchdog (WWDG)
  - 1x 12-bit Independent Watchdog (IWDG)
- **Programming Methods**
  - Support SWD/JTAG debugging interface.
  - Support UART and USB Bootloader
- **Security Features**
  - Flash encryption, multi-user partition management unit (SMPU)
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Built-in hardware acceleration engine for cryptographic algorithm
  - Supports AES/TDES, SHA, SM3, SM4, and MD5 algorithms
  - True random number generator(TRNG)
  - CRC16/32 operation
  - Supports secure boot, program encryption download, secure firmware update

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- Supports external clock failure detection, anti-tamper detection.

- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
- **Packages**
  - LQFP64(10mm x 10mm)
  - BGA64 (5mm x 5mm)
  - BGA72 (4.41mm x 3.76mm)
  - BGA81 (4.41mm x 3.76mm)
  - LQFP100(14mm x 14mm)
  - LQFP100-2(14mm x 14mm)
  - LQFP144(20mm x 20mm)

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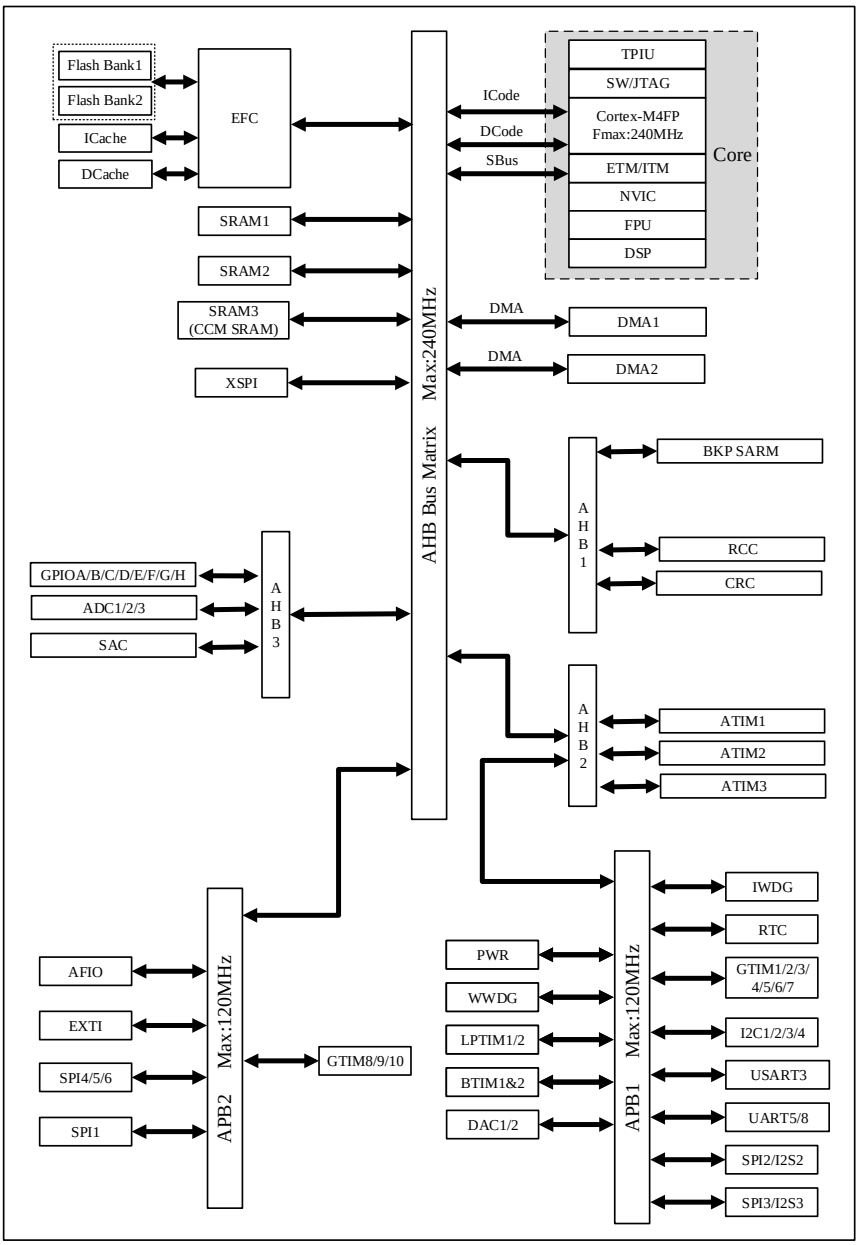
1 Introduction

The N32H497 series microcontrollers feature a 32-bit ARM Cortex®-M4F core, supporting single-precision floating-point operations and DSP instructions. Operating at a maximum frequency of 240MHz, they integrate up to 1MB of embedded Flash, 576KB of SRAM (including 80KB of CCM SRAM) plus 4KB of Backup SRAM. The devices incorporate three 12-bit 4.7Msps ADCs, two 12-bit DACs, and integrated communication interfaces including USB FS Device, USB HS Host/Device, U(S)ART, I2C, SPI, CAN-FD, and Ethernet. It supports DVP interfaces, SDIO, FEMC, xSPI, SDRAM high-speed memory interfaces, I2S audio interface, multiple advanced timers, general-purpose timers, basic timers, low-power timers, integrated cryptographic algorithm hardware acceleration engine supporting AES/TDES, SHA, SM3, SM4, MD5 algorithms, TRNG true random number generator, and CRC16/32.

The N32H497 series operates reliably within a temperature range of -40 ℃ to +105 ℃, with a supply voltage of 1.8V to 3.6V, and offers multiple power consumption modes.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32H497 Series Block Diagram



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1.1 Product Configurations

Table 1-1 N32H497 Series Product Configuration

Device		N32H497RGL7	N32H497RGB7	N32H497NGB7	N32H497MGB7	N32H497VGL7	N32H497VGL7C	N32H497ZGL7
Operating Condition		1.8~3.6V/-40~105°C						
CPU Frequency		ARM Cortex-M4F @240MHz, 300DMIPS						
Flash Capacity (KB)		1024	1024	1024	1024	1024	1024	1024
Total SRAM (KB)	General SRAM	496(1)						
	CCM SRAM(2)	80(3)						
	Backup SRAM	4						
Times	ATIM	3*16bit						
	GTIM	5*16bit						
		2*32bit(4)						
		3*16bit(5)						
	BTIM	2*32bit						
	LPTIM	2*16bit						
	SysTick timer	1						
	WWDG	1*14bit						
	IWDG	1*12bit						
	RTC	Yes						
Communication Interfaces	SPI/I2S	5(9)/2				6/2		
	I^2C	4						
	USART	5						
	UART	5						
	USB FS Device	Yes(6)						
	USB HS Host/Device	Yes(6)						
	FDCAN	3						

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	Ethernet	Yes						
Memory Expansion	XSPI	Yes						
	FEMC	No				Yes[7]		Yes
	SDIO	Yes						
	SDRAM	No						Yes
Human-computer interaction	DVP	Yes						
GPIO WKUP Pins		54 5	52 5	59 5	67 5	85 7	83 7	118 7
Nb of I/Os down to 1.8 V[8]		0	0	6	6	0	0	9
DMA Number of channels		2 16						
12bit ADC Number of channels		3 20	3 23	3 23	3 23	3 20	3 19	3 28
12bit DAC Number of channels		2 2						
Algorithm Support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM3、SM4、MD5、CRC16/CRC32						
TRNG		Yes						
Cordic		Yes						
DSMU Number of channels		1 8						
Security Protection		Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot						
Package		LQFP64	BGA64	BGA72	BGA81	LQFP100	LQFP100-2	LQFP144

Note:

1. *With ECC enabled, SRAM capacity is 448KB; without ECC enabled, SRAM capacity is 496KB. ECC is enabled by default.*
2. *Upon power-up, the default configuration is general-purpose SRAM; software can configure it as CCM SRAM.*
3. *With ECC enabled, SRAM capacity is 64KB; without ECC enabled, SRAM capacity is 80KB. ECC is enabled by default.*
4. *Only GTIM1 and GTIM4 support 32-bit timers;*
5. *Only GTIM8/9/10 support brake functionality, with channel 1 supporting complementary channel output;*
6. *For BGA81/71/64 packages, USB FS Device and USB HS Host/Device are mutually exclusive;*

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7. *Only supports lower 16-bit address and data multiplexing mode;*
8. *For BGA81 and BGA72 packages, pins PG9 to PG14 may support operation powered via the VDDIO input. For LQFP144 packages, pins PD6 to PD7 and PG9 to PG15 may support operation powered via the VDDIO input, with input voltage support ranging from 1.8V to 3.6V.*
9. *Supported SPI interfaces: SPI1 ~ SPI4 and SPI6*

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2 Functional Overview

2.1 Processor Core

The N32H497 series integrates the ARM Cortex™-M4F processor. It features a floating-point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 300 DMIPS. At the same time, its efficient signal processing capabilities combined with low power consumption, low cost, and ease of use advantages of the Cortex-M series processors. Make it suitable for applications that need a mix of control and signal processing capabilities in an easy-to-use manner.

The ARM Cortex™-M4F 32-bit reduced instruction set processor offers outstanding code efficiency.

2.2 Memories

The N32H497 series includes embedded encrypted Flash memory and embedded SRAM. The following diagram shows the memory address mapping.

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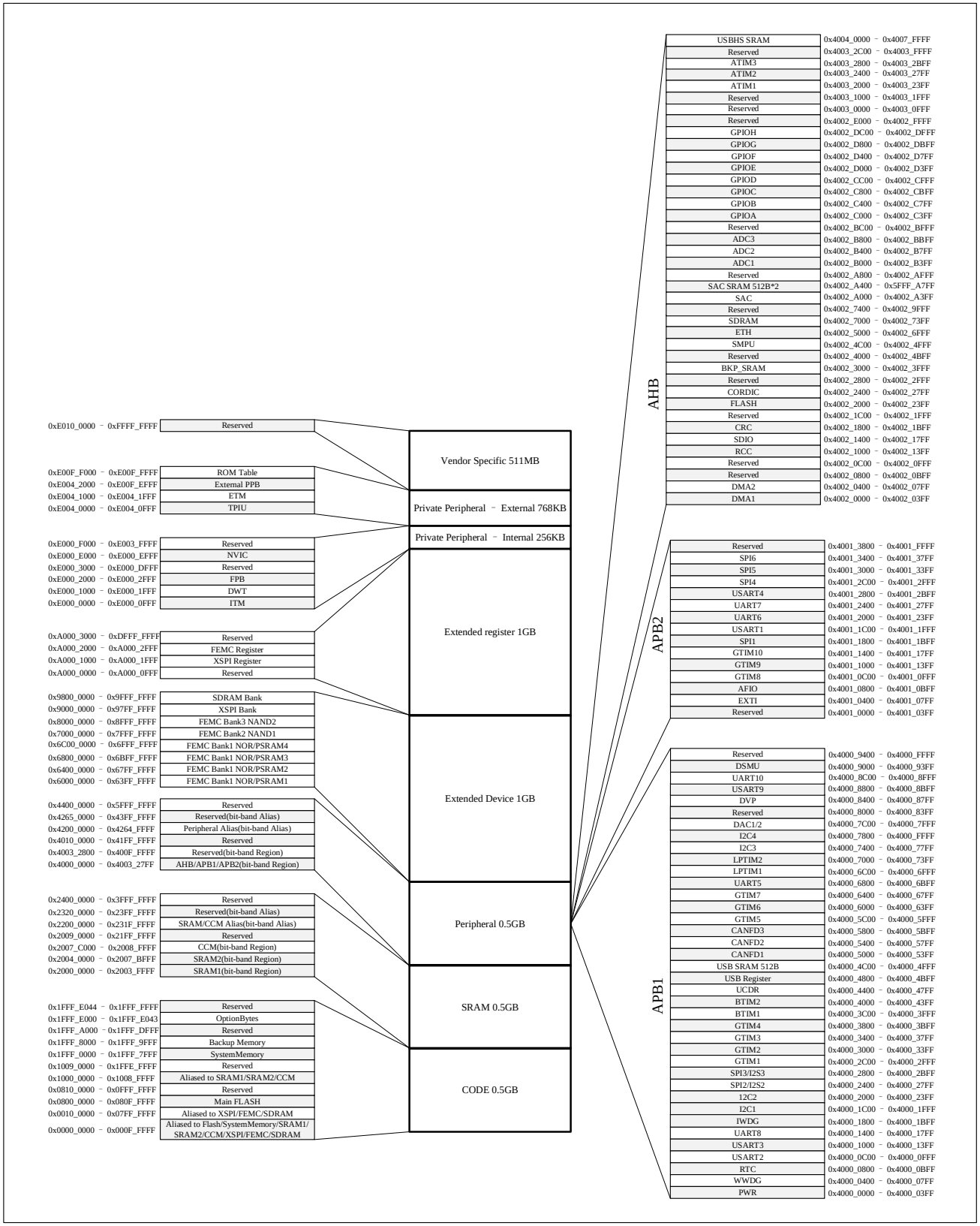
Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

The integrated encrypted Flash memory size is up to 1024 Kbytes, utilized for storing programs and data. The page size is 8Kbytes, supporting dual banks, supporting page erasing, double-word writing, word reading, half-word

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reading, and byte reading operations.

It supports storage encryption protection, enabling automatic encryption during writing and automatic decryption during reading (including program execution operation).

User partition management is supported, allowing for a maximum of 3 user partitions, different users cannot access each other's data (only executable code can be accessed).

2.2.2 Embedded SRAM

The chip integrates 576KB of SRAM (comprising 496KB of general-purpose SRAM and 80KB of CCM SRAM) alongside 4KB of Backup SRAM, detailed as follows:

496KB general-purpose SRAM, configurable to support ECC; when ECC is enabled, the maximum capacity is 448KB.

80KB CCM SRAM, defaulting as general-purpose SRAM, configurable as CCM SRAM. Supports ECC configuration, with a maximum capacity of 64KB when ECC is enabled.

4KB BKP SRAM capacity, supporting ECC. Data retention is optional in VBAT and Standby modes; data is retained normally in other operating modes (Run/Sleep/Stop0).

2.2.3 Nested Vector Interrupt Controller (NVIC)

Main features:

- Up to 112 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M4F)
- 16 programmable priority levels (four bits of interrupt priority used)
- Low-latency exception and interrupt handling
- Power management control
- Implementation of system control registers

The NVIC and the processor core interface are closely coupled, enabling low-latency interrupt processing and efficient processing of late arriving interrupts. All interrupts, including the core exceptions, are managed by the NVIC.

2.3 Extended Interrupt/Event Controller (EXTI)

The extended interrupt/event controller contains 25 edge detectors used for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. The pending register holds interrupt requests for the status lines, and the interrupt requests can be cleared by writing '1' to the corresponding bit in the pending register.

2.4 Clock System

The device offers various clock options for users to choose from, including:

- High speed internal RC oscillator (HSI) at 8 MHz
- Low speed internal RC oscillator (LSI) at 32 KHz
- High speed external crystal oscillator (HSE) ranging from 4 MHz to 32 MHz.
- Low speed external crystal oscillator (LSE) at 32.768 KHz.

The system clock source can be selected from HSI, HSE, PLL, EXTPLL, USBHS240M. Upon reset, the internal MSI clock is set as the default system clock, user can choose the external HSE clock with fail monitoring capabilites. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI. If interrupts are enabled, software can receive corresponding interrupts.

Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1)

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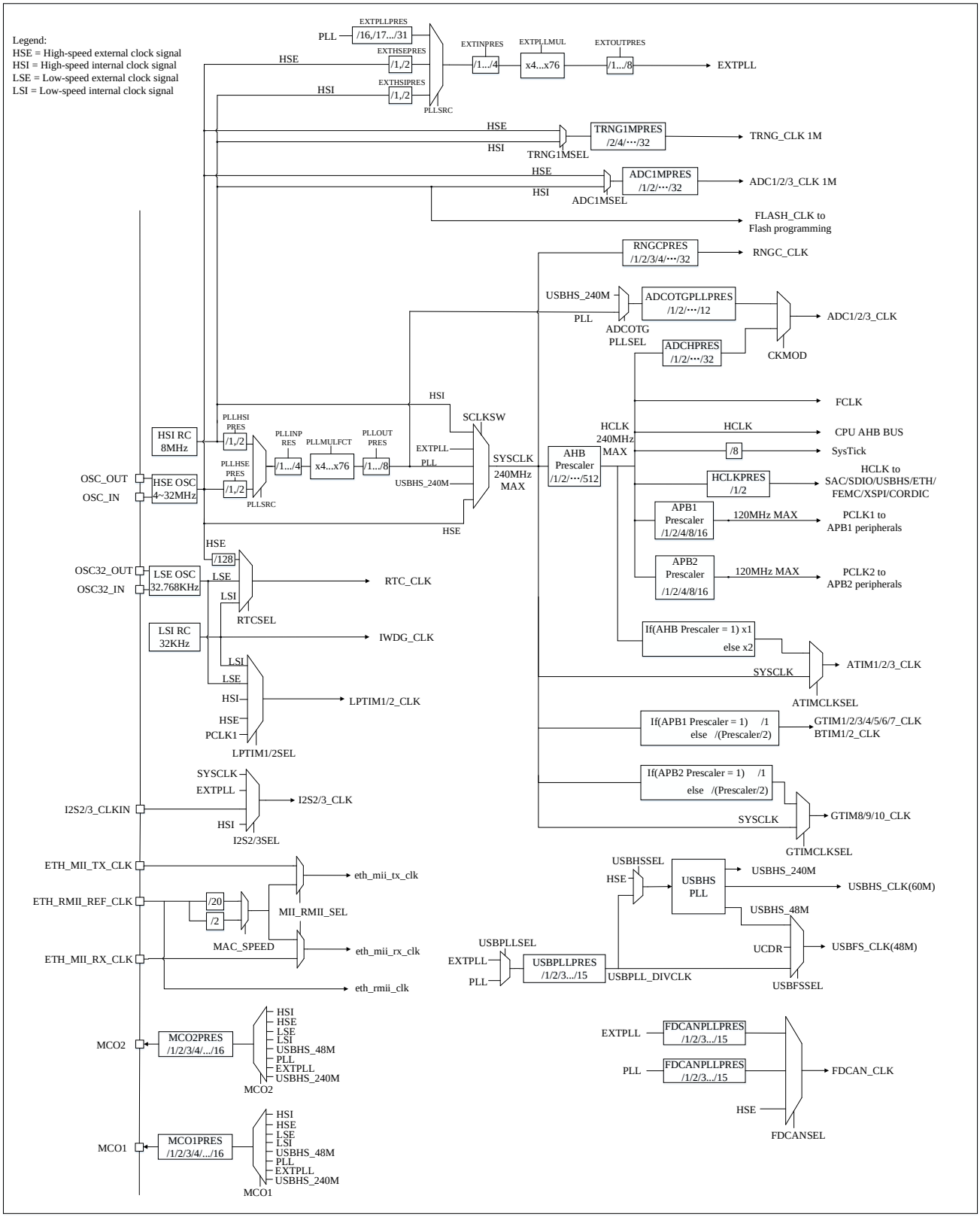
regions. The AHB has a maximum frequency of 240 MHz, APB2 has a maximum frequency of 120 MHz and APB1 has a maximum frequency of 120 MHz.

Refer to the clock tree diagram below.

Figure 2-2 Clock Tree



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2.5 Boot Modes

During startup, the BOOT mode after reset can be selected through the BOOT0 pin and option byte for BOOT configuration:

- Boot from Main Flash memory
- Boot from system memory
- Boot from embedded SRAM

Detailed start-up procedures are outlined in the table below:

Table 2-1 Single-BANK Mode Start-up

Option Byte				Pin	Boot mode	Starting address for accessing memory space in corresponding launch mode			
FLASH_BOOT	nBOOT1	nBOOT0	nSWBOOT0	BOOT0		Front half of Main Flash	Rear half of Main Flash	System Memory	SRAM
1	x	x	1	0	Main Flash front half boot	**0x0000_0000 0x0800_0000**	0x0808_0000(1)	0x1FFF_0000	0x1000_0000 0x2000_0000
1	x	1	0	x					
0	x	x	1	0	Main Flash rear half boot	0x0808_0000(1)	**0x0000_0000 0x0800_0000**	0x1FFF_0000	0x1000_0000 0x2000_0000
0	x	1	0	x					
x	1	x	1	1	SystemMemory boot	0x0800_0000	0x0808_0000	**0x0000_0000 0x1FFF_0000**	0x1000_0000 0x2000_0000
x	1	0	0	x					
x	0	x	1	1	SRAM boot	0x0800_0000	0x0808_0000	0x1FFF_0000	**0x0000_0000 0x1000_0000 0x2000_0000**
x	0	0	0	x					

Note 1. When the MCU's Flash capacity is 512KB, the starting address is 0x0804_0000; when the MCU's Flash capacity is 1MB, the starting address is 0x0808_0000.

Table 2-2 Dual-BANK Mode Start-up

Option Byte				Pin	Boot mode	Starting address for accessing memory space in corresponding launch mode			
FLASH_BOOT	nBOOT1	nBOOT0	nSWBOOT0	BOOT0		Main Flash BANK1	Main Flash BANK2	System Memory	SRAM
1	x	x	1	0	Main Flash BANK1 boot	**0x0000_0000 0x0800_0000**	0x0808_0000(1)	0x1FFF_0000	0x1000_0000 0x2000_0000
1	x	1	0	x					
0	x	x	1	0	Main Flash BANK2 boot	0x0808_0000(1)	**0x0000_0000 0x0800_0000**	0x1FFF_0000	0x1000_0000 0x2000_0000
0	x	1	0	x					
x	1	x	1	1	SystemMemory boot	0x0800_0000	0x0808_0000	**0x0000_0000 0x1FFF_0000**	0x1000_0000 0x2000_0000
x	1	0	0	x					
x	0	x	1	1	SRAM boot	0x0800_0000	0x0808_0000	0x1FFF_0000	**0x0000_0000 0x1000_0000 0x2000_0000**
x	0	0	0	x					

Note 1. When the MCU's Flash capacity is 512KB, the starting address is 0x0804_0000; when the MCU's Flash capacity is 1MB, the starting address is 0x0808_0000.

The Bootloader is stored in the system memory and can program the flash memory through USART1 or USB interface.

Address remapping for physical address 0 can also be achieved by configuring RCC_BOOTREMAP.REMAPSEL[2:0]:

- Boot from xSPI external memory through remap

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- Boot from FEMC external memory through remap
- Boot from SDRAM external memory through remap

2.6 Power Supply Scheme

There are five external power supplies: VDD, VDDIO, VDDA, VREF, VBAT. Among them, VDD is the chip power supply, mainly for the power supply system and clock system; VDDA is the analog peripheral power supply, mainly for the analog peripherals; VREF provides a reference power supply for the analog peripherals to provide higher accuracy. VBAT is connected to the battery to provide power for the backup domain.

There are five power domains, powered by external power supplies for different power domains:

- V_{DD} domain: 1.8 to 3.6V, mainly powering for MR, most GPIOs, HSE, HSI, PLL, POR/PDR, BOR, PVD, and USB PHY
- V_{DDIO} domain: Operating within a voltage range of 1.8 to 3.6 volts, it provides independent power supply to nine I/O pins: PD6 to PD7 and PG9 to PG15.
- V_{DDA} domain: 1.8 to 3.6V, mainly powering for ADC, DAC, TS, etc.
- V_{DDBK} domain: 1.8 to 3.6V, mainly powering for WKUP pin, NRST, PC13/14/15, LSE, LSI, etc.
- V_{DDD} domain: 1.1 V or 0.9 V, mainly powering for CPU, AHB, APB, SRAM, FLASH, RCC, TRNG, and most peripherals
- V_{DDDBK} domain: 0.9 V or 0.8 V, mainly powering for PWR, Backup SRAM (4KB), RTC, LPTIM, WKUP pin, NRST, PC13/14/15, backup IOM, IWDG, and RCC_BDCTRL register.

2.7 Reset

POR and BOR circuits are integrated inside the device. This part of the circuit ensures that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold ($V_{POR/BOR}$), the device goes into reset state without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See **Table 4-6** for values of $V_{POR/PDR}$ and V_{PVD}.

2.9 Low Power Mode

The N32H497 series supports four low-power modes.

- SLEEP mode

In SLEEP mode, only the CPU is stopped, all peripherals remain operational and can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

STOP0 mode is based on the Cortex-M4F deep sleep mode. Achieves the lowest power consumption, while retaining the content of SRAM and registers. Most clocks in the main power domain are stopped, such as PLL, HSE, HSI.

Wakeup: The device can be woken up from STOP0 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC timestamp, RTC alarm, etc.

- STANDBY Mode

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In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator. After entering STANDBY mode, most register contents will be lost, while the contents of backup registers will still be retained. The STANDBY circuitry continues to function.

Wakeup: External reset signal on NRST, IWDG reset, rising/falling edge on the WKUP pin, RTC alarm, RTC timestamp and LPTIM wake-up event can wake up the device from STANDBY mode.

- VBAT Mode

Whenever VDD power is lost, it will automatically enter VBAT mode. In VBAT mode, except for NRST, WKUP, PC13_TAMPER, PC14, and PC15, most I/O pins are in a high-impedance state.

Wakeup: VDD power up.

2.10 Direct Memory Access (DMA)

The DMA controller can access the following slaves: Flash, SRAM1, SRAM2, CCM SRAM3, FEMC, XSPI, CRC, SDIO, SDRAM, CORDIC, APB1, APB2, ATIM, ADC, DAC.

The DMA controller is controlled by the CPU to perform fast data transfers from source to destination. After configuring, data can be transferred without any CPU intervention. This keeps the CPU resources free for other operations or saves overall system power consumption.

The device integrates two DMA controllers (DMA1, DMA2), each DMA supports eight channels. Each channel is dedicated to servicing memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMAchannels.

The key features are as follows:

- 16 independently configurable channels (requests): Each DMA (DMA1, DMA2) supports 8 channels
- Support memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers
- Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Each DMA channel has a dedicated software priority level (DMA_CHCFGx.PRIOLVL[1:0] bits, corresponding to 4 priority levels) that can be individually configured. Channels with the same priority level will further compare the hardware index (channel number) to determine the final priority (the channel with the lower index number has higher priority).
- Configurable source and destination transfer size (byte, half word, word). Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) and 1 global interrupt flag (set by logical OR of the 3 events) for each channel
- Access to Flash, Sram1, Sram2, CCM Sram3, FEMC, XSPI, CRC, SDIO, SDRAM, CORDIC, APB1, APB2, ATIM, ADC, DAC
- Programmable number of data to be transferred: up to 65536
- Support burst transfers, burst length is configurable, can be set to 1/2/3/4/5/6/7/8 units.

2.11 Real Time Clock (RTC)

The RTC consists of continuously running counters integrated with a built-in calendar clock module that provides a perpetual calendar functionality, as well as alarm interrupts and periodic interrupt.

The key features are as follows:

- The Real-Time Clock (RTC) is an independent BCD (binary-coded decimal) timer/counter

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- Software supports daylight saving time compensation
- Programmable periodic automatic wake-up timer.
- Two 32-bit registers containing hours, minutes, seconds, year, month, date, and week day
- One independent 32-bit register containing sub-seconds
- Two programmable alarms
- Two 32-bit registers containing programmed hours, minutes, seconds, year, month, date, and week day
- Two independent 32-bit registers containing programmed sub-seconds
- Digital precision calibration function
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Three configurable filtering and internal pull-up intrusion detection events
- Timestamp functionality
- 20 backup registers that can retain data in low-power mode
- Multiple interrupt/event wake-up sources, including alarm A, alarm B, wake-up timer, timestamp, and tamper event
- As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, SLEEP mode, STOP0 mode and VBAT mode)
- The RTC provides various wake-up sources that can wake the MCU from all low-power modes (SLEEP mode, STOP0 mode, and STANDBY mode)

2.12 Timers and Watchdogs

The N32H497 series supports up to 3 advanced timers, 10 general timers, 2 basic timers, 2 low-power timers, as well as 1 independent watchdog timer, 1 window watchdog timer, and 1 SysTick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low-power timer:

Table 2-3 Comparison Of Timer Functions

Timer	Counter resolution	Counter type	Prescaler factor	Capture/compare channels	Complementary outputs	Maximum Interface Clock (MHz)	Maximum Timer Clock (MHz)
ATIM1~3	16	Up, down, up/down	Any integer between 1 and 65536	4	4	240	240
GTIM1 GTIM4	32	Up, down, up/down	Any integer between 1 and 65536	4	N	120	240
GTIM2~3 GTIM5~7	16	Up, down, up/down	Any integer between 1 and 65536	4	N	120	240
GTIM8~10	16	Up, down, up/down	Any integer between 1 and 65536	4	1	120	240
BTIM1~2	32	Up	Any integer between 1 and 65536	0	N	120	240
LPTIM1~2	16	Up	1、2、4、8、16、32、64、128	0	N	120	120

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2.12.1 Basic Timer (BTIM1~2)

Basic timers contain a 32-bit auto-reload counter.

Main features:

- 32-bit auto-reload up-counting counter
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- Event that generate the interrupt/DMA is as follows:
  - Update event

2.12.2 General-Purpose Timer (GTIM1~7)

The general-purpose timers (GTIM1/GTIM2/GTIM3/GTIM4/GTIM5/GTIM6/GTIM7) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-load counters (GTIM2/GTIM3/GTIM5/GTIM6/GTIM7) supporting up counting, down counting, and up/down counting.
- 32-bit auto-load counters (GTIM1/GTIM4) supporting up counting, down counting, and up/down counting.
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- GTIMx supports up to 4 channels
- Channel's working modes: PWM output, output compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signals

2.12.3 General-Purpose Timer (GTIM8~10)

The general-purpose timers (GTIMx) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. The general-purpose timer features complementary output, dead-time insertion, and break functions. It is suitable for motor control.

Main features:

- 16-bit auto-reload counters (Supports up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler (the prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- GTIMx supports up to 5 channels
- 4 capture/compare channels, operating modes include: PWM output, output compare, one-pulse mode output,

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input capture

- 1 break input signal supporting digital filtering, used to place the timer's output signal in a safe user-selectable configuration
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with programmable dead-time
  - For GTIMx, channel 1 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

2.12.4 Advanced Control Timer (ATIM1~3)

The advanced control timers (TIM1 and TIM8) is mainly used for the following purposes: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. Advanced timers have complementary output function with dead-time insertion and bracking functionality, making it suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- ATIMx supports up to 9 channels
- 4 capture/compare channels for:
  - PWM output
  - Output compare
  - One-pulse mode output
  - Input capture
- 2 break input signals supporting digital filtering
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input

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- Complementary outputs with programmable dead-time
  - For ATIMx, channel 1,2,3,4 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

2.12.5 Low Power Timer (LPTIM1~2)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes. LPTIM can run without internal clock source as a "Pulse Counter". Also, the LPTIM can wake up the system from low-power modes, to realize "Timeout functions" with extremely low power consumption.

Main features:

- 16-bit up counter
- 3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources:
  - Internal clock source: LSE, LSI, HSI, HSE or APB1 clock
  - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for Pulse Counter application)
- 16-bit auto-load register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or one-shot mode counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for glitch filtering
- Configurable output (PWM)
- Configurable IO polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.12.6 SysTick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reload function
- A maskable system interrupt is generated when the counter reaches 0
- Programmable clock source

2.12.7 Watchdog (WDG)

Built-in Independent Watchdog (IWDG) and Window Watchdog (WWDG) timers are used to detect issues caused by software errors. The watchdog timers are highly flexible, enhancing system security and the accuracy of timing control.

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Independent watchdog (IWDG)

The Independent Watchdog (IWDG) is driven by the low-speed internal clock (LSI clock) running at 32 kHz. It can continue to operate in the event of a deadlock or MCU freeze. This provides a higher level of security, timing accuracy, and watchdog flexibility. It can resolve system failures caused by software faults through a reset. The IWDG is best suited for applications where the watchdog needs to run as a completely independent process outside the main application but with lower timing accuracy constraints.
When the power control register PWR_CTRL2.IWDGRSTEN is set to '1', a system reset occurs when the IWDG counter reaches 0 (if this is set to '0', the IWDG counts but does not trigger a reset).

Main features:

- Independent 12-bit down-counter
- The RC oscillator provides an independent clock source that can operate in SLEEP, STOP0, and STANDBY modes
- Support reset and low-power wake-up
- When the down-counter reaches 0x000, the system resets (if the watchdog is activated)

Window watchdog (WWDG)

The clock of the Window Watchdog (WWDG) is derived by dividing the APB1 clock frequency by 4096. It detects abnormal program execution through the configuration of the time window. Therefore, WWDG is suitable for precise timing and is commonly used to monitor software faults that cause the application program to deviate from its normal operation sequence due to external interference or unforeseen logical conditions. When the WWDG decrementing counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0, a system reset occurs.

Main features:

- Programmable 14-bit independent down counter
- When the WWDG is enabled, a reset will occur under the following conditions:
  - The down-counter is less than 0x40
  - When the down counter value is greater than the value of the window register, reload will occur
- Early wake-up interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40

2.13 I^2C Bus Interface

The I^2C (Inter-Integrated Circuit) bus is a widely used bus structure that consists of only two bidirectional lines, namely the data line SDA and the clock line SCL. Through these two lines, all devices compatible with the I^2C bus can directly communicate with each other via the I^2C bus.

The I^2C interface connects the microcontroller and the serial I^2C bus, and can be used for communication between the MCU and external I^2C devices. The I^2C interface module implements the standard speed mode and fast mode of the I^2C protocol, with CRC calculation and verification functions, supports SMBus (System Management Bus) and PMBus (Power Management Bus). It controls all I^2C bus-specific sequencing, protocol, arbitration and timing. The I^2C interface module also supports DMA mode to effectively reduce the burden on the CPU.

Main features:

- This module can be used as master device or slave device
- Support 7-bit/10-bit addressing and general call
- As an I^2C master device, it can generate clock, start signal, and stop signal
- As an I^2C slave device, it has programmable I^2C address detection and stop bit detection functions
- Support Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz) and Fast-mode Plus (up to 1MHz)
- Supports interrupt vector, transfer complete interrupt, and error event interrupt

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- Optional extend clock function
- Support DMA
- Generation or verification of configurable PEC(Packet error checking)
- Compatible with the PMBus and SMBus 2.0
- Support FIFO

2.14 Universal Synchronous/Asynchronous Transceiver (USART)

Universal Synchronous Asynchronous Receiver Transmitter (USART) is a full-duplex serial data exchange interface that supports synchronous or asynchronous communication. It can be flexibly configured to facilitate full-duplex data exchange with a variety of external devices.

The USART interface allows configurable transmission and reception baud rates, and also supports continuous communication through DMA. USART also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smart card asynchronous protocol, IrDA SIR ENDEC function, as well as hardware flow control function.

Main features:

- Full duplex, asynchronous communication
- Single-wire half-duplex communications
- Programmable baud rate, up to 15 Mbit/s
- Configurable oversampling method by 16 or 8
- Programmable data word length (8 or 9 bits)
- Two internal FIFOs for transmit and receive data
- Configurable stop bits (1 or 2 stop bits)
- Support hardware-generated parity bit and parity bit checking
- Support hardware flow control: RTS, CTS
- Support transmission and reception via DMA
- Multiprocessor communications: If the address does not match, it enters mute mode. Wake-up from mute mode by idle line detection or address mark detection
- Support synchronous mode, allowing the user to control bidirectional synchronous serial communication in master mode
- Support asynchronous Smartcard protocol, compliant with ISO7816-3 standard
- Support IrDA (infrared data association) SIR ENDEC specifications, providing both normal and low power operation modes
- Support LIN mode
- Four error detection flags:Overflow error,Noise error,Frame error,Parity error
- Support multiple interrupt requests:Transmit data register empty,CTS flag,Transmission complete,Reception complete,Data overflow,Bus idle,Parity error,LIN mode break frame detection, and noise flags/overflow errors/frame errors in multi-buffer communications

Mode configuration:

USART modes	USART1	USART2	USART3	USART4	UART5	UART6	UART7	UART8	USART9	UART10
Asynchronous mode	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Multiprocessor communication	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

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USART modes	USART1	USART2	USART3	USART4	UART5	UART6	UART7	UART8	USART9	UART10
Synchronous mode	Y	Y	Y	Y	N	N	N	N	Y	N
Half duplex (Single wire mode)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Smartcard mode	Y	Y	Y	Y	N	N	N	N	Y	N
IrDA	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
DMA	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Hardware flow control	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Note: Y = supported; N = not supported.

2.15 Controller area network (FDCAN)

The N32H497 provides three FDCAN modules compliant with ISO 11898-1:2015, supporting CAN 2.0A/B and CAN FD protocols, and compatible with non-ISO standard Bosch protocols.

Furthermore, the FDCAN1 and FDCAN2 modules support Time-Triggered CAN (TTCAN) as defined in ISO 11898-4, encompassing event-synchronised time-triggered communication, Global System Time (GST), and clock drift compensation. FDCAN1 and FDCAN2 incorporate dedicated additional registers for time-triggered functionality. CANFD may optionally be used alongside event-triggered and time-triggered CAN communication.

Three FDCAN modules share a single message RAM region for receiving message filters, receive FIFOs, receive buffers, transmit buffers, transmit event FIFOs (and TTCAN triggers). The message RAM resides within the MCU's internal SRAM with a configurable starting address, allowing a maximum allocation of 4480 words (32-bit) per FDCAN module.

Main features:

- Complies with ISO 11898-1:2015 and ISO 11898-4 standards
- Support CANFD, data size up to 64 byte
- Supports fully hardware-implemented TTCAN Level 1 and Level 2 (FDCAN1/2 only)
- Support CAN error log record
- Support AUTOSRA standard
- Support SAE J1939 standard
- Enhanced receive filter
- Two configurable receive FIFOs
- Separate signal indication when receiving high-priority messages
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO or queue
- Configurable transmit event FIFO
- Support configurable message RAM shared by 3 FDCAN controllers
- Programmable loopback test mode
- Maskable module interrupt
- Two clock domains: CAN core clock and APB bus clock
- Support power-down mode

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2.16 Serial Peripheral Interface/inter-integrated sound interfaces (SPI/I²S)

The SPI protocol supports half-duplex, full-duplex and synchronous, serial communication with external devices. The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. It can be used for a variety of purposes, including simplex synchronous transfers on two lines with bidirectional data line, and also support hardware CRC check.

I²S is also a synchronous serial interface communication protocol. It supports four audio standards, including the Philips I²S standard, MSB and LSB alignment standards, and PCM standards. In half-duplex communication, it can operate in two modes: master and slave. When operating as a master device, it can provide clock signals to external slave devices via the interface.

The SPI main features are:

- Full-duplex and simplex synchronous transmission
- Support master, slave and multi-master mode
- 8 or 16 bit transmission frame format selection
- Programmable data order
- Hardware or software management of chip select signal
- Programmable clock polarity and phase
- Support hardware CRC calculation and check
- Support DMA transfer
- 8 bytes transmit/receive FIFO

The I²S main features are:

- Full-duplex and half-duplex synchronous transmission
- Support master, slave mode
- Supported I²S protocols:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard (with short and long frame synchronization)
- Configurable audio sampling frequency, ranging from 8KHz to 192KHz
- Programmable clock polarity (steady state)
- Data order is always MSB first
- Support DMA transfer
- Support multiple clock sources

2.17 Expanded Serial Peripheral Interface(xSPI)

xSPI is an interface used for communication with single/dual/quad/octal line SPI peripherals. It can operate in two modes: indirect and memory-mapped mode.

It supports indirect mode: all operations are performed using xSPI registers; memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory.

Main features:

- Configurable for 1/2/4/8-bit data

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- Support Single SPI/Normal SPI、DUAL SPI、QUAD SPI、Dual-QUAD、OCTAL SPI modes
- Support Motorola SPI:
  - Standard/Dual/Quad/Octal SPI
- Support SDR and DDR modes
- Support DDR transfer data mask
- Support clock stretching
- In indirect mode and memory-mapped mode, frame format and operation codes can be software configured
- Integrated FIFO for reception and transmission
- 8/16/32-bit data accesses allowed
- 16 words TX FIFO and 16 words RX FIFO
- Support DMA transfer
- Supports the Hyperbus protocol
- XIP mode supports SPI read and write, and supports serial NOR FLASH
  - Support continuous transfer mode
  - Support data prefetch
- Support automatic decryption of executed code, meaning that the xSPI peripheral stores encrypted code, reads the encrypted code during execution, and decrypts it to plaintext for CPU execution, without affecting the access speed to the peripheral storage. The decryption can be software configurable to enable/disable, and the root key is stored in the NVR area, inaccessible to the user
- Support serial NAND FLASH and PSRAM
- When xSPI accesses external memory for read and write, after xSPI initialization, there is no need for additional configuration of xSPI between writing to and reading from external storage, allowing direct memory access (via SRAM address) for reading and writing to external memory
- Support 2 external chip select output controls in master mode; Support 1 chip select input in slave mode. All IOs multiplexed as chip select outputs in master mode can be multiplexed as chip select inputs in slave mode
- Support multi-master arbitration function

2.18 Flexible External Memory Controller (FEMC)

The Flexible External Memory Controller (FEMC) is used to access various external memories, enabling easy expansion of different types of high-capacity static memories according to application needs. It can simultaneously expand multiple types of static memories without increasing external interfaces. All external memories share the address, data, and control signals output by the FEMC controller, and FEMC distinguishes different external devices through a unique chip select signal.

Main features:

- Support the following devices:
  - SRAM
  - PSRAM
  - ROM
  - NOR Flash
  - NAND Flash (SLC)
  - LCD (8080/6800)

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- Support two NAND flash blocks, hardware 1-bit ECC can detect up to 8K bytes of data
- Burst mode support for faster access to synchronous devices, such as NOR flash and PSRAM
- 8/16-bit data bus width
- Independent chip select control for each memory bank
- Support various different devices through timing programming
- Based on the data width of the external memory, it automatically converts 32-bit AHB access requests into consecutive 16-bit or 8-bit accesses, enabling communication with external 16-bit or 8-bit memory devices. It converts 32-bit AHB access requests into consecutive 16-bit or 8-bit accesses for accessing external 16-bit or 8-bit devices
- Write enable and byte lane select outputs for use with PSRAM and SRAM devices

2.19 SDRAM Controller

The principal features supported by SDRAM are as follows:

- Two SDRAM devices with independent configurations
- 8-bit and 16-bit data bus widths
- 13-bit row address, 11-bit column address, 4 internal banks: 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)
- Row addresses configurable to 11, 12, or 13 bits; column addresses configurable to 8, 9, 10, or 11 bits
- Word, half-word, and byte accesses
- Automatic row and bank boundary management
- Support for burst mode
- Write access protection
- Programmable timing parameters
- Supports software reset
- Software initialisation via SDRAM power-up
- CAS latency of 1, 2, 3
- Automatic refresh operation with programmable refresh rate
- Software suspend and wake via SDRAM

2.20 Secure Digital Input and Output Interface (SDIO)

The SDIO interface defines the host interface for SD cards, SD I/O cards, and MultiMediaCards (MMC). It provides data transfer between the AHB peripheral bus and MMC, SD storage cards, and SDIO cards. The MultiMediaCard system specifications are available through the MultiMediaCard Association website at www.mmca.org, published by the MMCA technical committee. SD memory card and SD I/O card system specifications are available through the SD card Association website at www.sdcard.org.

Main features:

- SD card: fully compatible with SD card specification version 2.0
- SD I/O: fully compatible with SD I/O card specification version 2.0, support two different data bus modes: 1-bit (default) and 4-bit
- MMC: fully compatible with MultiMediaCard system specification version 4.2 and earlier versions. Support three different data bus modes: 1-bit (default), 4-bit, and 8-bit
- Achieves a data transfer rate of up to 50MHz in 8-bit data bus mode

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- Support interrupts and DMA requests
- Data and command output enable signals used to control external bidirectional drivers

Notes:

(1) SDIO is not compatible with SPI communication mode.

(2) In the MultiMediaCard system specification version 2.11, it is defined that the SD storage card protocol only supports the I/O mode of the SD card or the I/O part of the composite card. It does not support many commands required in SD storage devices, such as erase commands that do not work in SD I/O devices, so SDIO does not support these commands. Additionally, some commands in SD storage cards and SD I/O cards are different, and SDIO does not support these commands.
SDIO supports only one SD/SDIO/MMC 4.2 card at a time, but can support multiple MMC version 4.1 or earlier cards.

2.21 Universal Serial Bus Full-Speed Device Interface (USB_FS_Device)

The Universal Serial Bus Full-Speed Device Interface (USB_FS_Device) module is a peripheral that complies with the USB 2.0 Full-Speed protocol. It includes the physical layer USB PHY and does not require an additional PHY chip. The USB_FS_Device supports four types of transfers defined in the USB 2.0 protocol: **control transfer**, **bulk transfer**, **interrupt transfer**, and **isochronous transfer.**

Main features:

- Comply with the technical specifications of USB2.0 full-speed equipment
- Configurable up to 8 USB endpoints
- Each endpoint supports the four types of transfer defined in the USB 2.0 protocol:
  - control transfer
  - bulk transfer
  - interrupt transfer
  - synchronous transfer
- Double buffer mechanism for bulk/isochronous endpoints
- Cyclic redundancy check (CRC) generation/checking, Non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing
- Support USB Suspend/Resume operation
- Frame locked clock pulse generation

2.22 Universal Serial Bus High-Speed Host/Device Interface (USB_HS_Host/Device)

USB High-Speed Dual Role Interface (USB HS Dual Role), hereinafter referred to as USBHS. The USBHS controller is designed to provide a standard interface for high-speed data transfer and connecting external devices. USBHS supports both host and device modes, it contains a full-speed USB PHY internal, which can be configured as high-speed or full-speed mode, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

Main features:

- Support USB 2.0 high-speed (480Mb/s) / full-speed (12Mb/s) / low-speed (1.5Mb/s) Host mode
- Support USB 2.0 high-speed (480Mb/s) / full-speed (12Mb/s) Device mode

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- Support all the four types of transfer: control transfer, bulk transfer, interrupt transfer and isochronous transfer
- USBHS contains a full-speed USB PHY internal, which supports high-speed, full-speed and low-speed operation, no more external PHY chip is needed
- Support HS SOF, FS SOF, and LS Keep-alive tokens
- SOF pulse can be output through PAD
- SOF pulse is connected internally to the timer (TIMx)
- Support A-B device identification (ID line)
- USBHS has embedded DMA, and can be software configured for AHB bulk transfer type
- Has power-saving functions, such as stopping the system during USB suspension, shutting down digital module clocks, and managing power for PHY and DFIFO
- 4 KB dedicated RAM
- Contain 16 host channels in Host mode, each channel supports any type of USB transfer
- Built-in hardware scheduler in Host mode:
  - Up to 16 interrupt and synchronous transfer requests in the periodic hardware queue
  - Up to 16 control and bulk transfer requests in the non-periodic hardware queue
- In Host mode, it contains one RX FIFO, one periodic transfer TX FIFO, and one non-periodic transfer TX FIFO
- In Device mode, it contains 1 bidirectional control endpoint 0, as well as 8 IN endpoints and 7 OUT endpoints. IN and OUT endpoints can be configured for bulk transfer, interrupt transfer, or isochronous transfer
- In Device mode, it contains a shared RX FIFO and a TX-OUT FIFO, as well as 9 dedicated TX-IN FIFOs
- Supports soft disconnect function

Note: USBHS requires the use of a 16MHz, 19.2MHz, 20MHz, 24MHz, 26MHz, or 32MHz external crystal as a clock source.

2.23 CORDIC Co-processor (CORDIC)

The CORDIC co-processor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications.

Main features:

- Support rotation and vectoring calculation modes
- Support circular and hyperbolic modes
- Once the calculation starts, any operation to read the result register will insert the bus into a waiting state until the calculation is completed. Therefore, the calculation result can be read out when it is completed without the need for polling or interrupts
- Support 10 functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Support fixed-point and floating-point input/output modes
- Support interrupt, polling, and DMA request read/write modes
- Programmable precision

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2.24 Digital filter for sigma delta modulators (DSMU)

The DSMU module is designed to interface with external ΣΔ modulators. It supports up to 8 external digital serial interfaces (channels) and includes up to 4 digital filters. These filters offer flexible Sigma Delta stream digital processing options, enabling up to 24-bit final ADC resolution. Additionally, the DSMU can optionally accept parallel data stream input from internal ADC peripherals or device memory.
The main features are as follows:

- Supports up to 8 multiplexed digital serial input channels:
  - Customizable SPI interface for various ΣΔ modulators connection
  - Customizable Manchester coded 1-wire interface support
  - Clock signal output for ΣΔ modulator(s)
- Supports up to 8 internal digital parallel channels:
  - Each input supporting up to 16-bit resolution
  - Internal sources from ADCs data or CPU/DMA write(memory) data
- Configurable digital signal processing:
  - Sinc^x filter: Adjustable order/type (1 to 5) and oversampling ratio (1 to 1024)
  - Integrator: Adjustable oversampling ratio (1 to 256)
- Support up to 24-bit output data resolution:
  - Right bit-shifter for final data (0 to 31 bits)
- Signed filter output data
- Automatic data offset correction (user-stored offset in register)
- Continuous or single conversion
- Start-of-conversion synchronization with:
  - Software trigger
  - Internal timers trigger
  - External events trigger
  - Start-of-conversion synchronize with first DSMU filter (DSMU_FLT0)
- Analog watchdog feature:
  - Low and high value threshold registers
  - Configurable Sinc^x digital filter (order = 1 to 3, oversampling ratio = 1 to 32)
  - Input from filter output data register or from serial channels (1 to 8)
  - Continuous monitoring independent of standard conversion
- Short-circuit detector for saturated analog input values (bottom and top ranges):
  - 8-bit counter to detect 1 to 256 consecutive 0’s or 1’s in the input data stream
  - Continuous monitoring of each channel (8 serial channel transceiver outputs)
- Break generation on analog watchdog or short-circuit detector event
- Extremes detector:
  - Store minimum and maximum output data values
  - Refreshed by software reading
- DMA support for reading converted data

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- Interrupts: End of conversion, overrun, analog watchdog, short-circuit, channel clock absence
- Two types of conversions:
  - Regular: Triggred by lesser priority software only, can be requested anytime or in continuous mode without affecting the timing of injected conversions
  - Injected: Higher priority, multiple trigger sources and precise timing.

2.25 General-Purpose Input/Output Interface (GPIO)

Up to 118 GPIOs, which can be divided into eight groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE/GPIOF/GPIOG/GPIOH). GPIO ports share pins with other multiplexed peripherals, allowing users to configure them flexibly according to requirements. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up or pull-down), or alternate peripheral function port. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up
  - Input pull down
  - Analog function
  - Open-drain output, pull-up and pull-down configurable
  - Push-pull output, pull-up and pull-down configurable
  - Push-pull alternate function, pull-up and pull-down configurable
  - Open-drain alternate function, pull-up and pull-down configurable
- Independent bit set or set functions
- All I/O support external interrupts
- All I/O support low-power mode wake-up, with configurable rising or falling edge:
  - 16 EXTI lines can be used for STOP0 mode wake-up, and all I/O can be multiplexed as EXTI
  - PA0/PA2/PC5/PC13/PE6/PD2/PD3 can be used to wake-up from STANDBY mode
- Support software configure alternate function selection
- Support GPIO lock mechanism, can only be cleared by reset once locked

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed in 32-bit words (16-bit half-word or 8-bit byte access is not allowed).

2.26 Analog/Digital Converter (ADC)

The 12-bit ADC employs a high-speed successive approximation method. Three ADCs are present: ADC1 and ADC2 may be configured as a dual ADC; ADC1, ADC2, and ADC3 may be configured as a triple ADC. ADC1 supports up to 16 multiplexed channels, while ADC2 and ADC3 support up to 18 multiplexed channels. Each A/D conversion channel may operate in single, continuous, scan, or intermittent modes. ADC conversion values are stored (left-aligned/right-aligned) in 16-bit data registers. Analogue watchdogs 1/2/3 can detect whether input voltages fall within user-defined high/low thresholds, and the maximum frequency of the ADC input clock is 80MHz.

Main features:

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- Support 3 ADCs, support single-ended or differential inputs
  - ADC1 is connected to 16 external channels and to 3 internal channels
  - ADC2 is connected to 18 external channels and to 1 internal channels
  - ADC3 is connected to 18 external channels
- Support 12/10/8/6-bits resolution configurable
  - The maximum sampling rate at 12bit resolution is 4.7 MSPS
  - The maximum sampling rate at 10bit resolution is 6 MSPS
  - The maximum sampling rate at 8bit resolution is 7.2 MSPS
  - The maximum sampling rate at 6bit resolution is 9 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 240 MHz
  - PLL or USBHS 240M can be configured as a sampling clock source, up to 80 MHZ, support 1, 2, 3, 4, 6, 8, 10, 12 frequency division
  - The AHB_CLK can be configured as the sampling clock source, up to 80 MHz, and supports frequency 1, 2, 3, 4, 6, 8, 10, 12, 16, 32
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports EXTI/TIMER trigger ADC sampling
- The sampling time interval for all channels can be programmed independently
- 3 analog watchdogs per ADC
- When the ADC is ready, sampling is completed, conversion is finished, or an analog watchdog 1/2/3 event occurs, an interrupt can be triggered
- Support 4 conversion modes:
  - Single conversion
  - Continuous conversion
  - Discontinuous mode
  - Scan mode
- Support self-calibration
- Data alignment with in-built data coherency
- Start-of-conversion can be initiated:
  - By software for both regular and injected conversions
  - By hardware triggers with configurable polarity (internal timers events or GPIO input events) for both regular and injected conversions
- Oversampling
  - 16-bit data register
  - Adjustable oversampling ratio, x2, x4, x8, x16, x32, x64, x128, x256
  - Programmable data right shift up to 8 bits
- Data preconditioning

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  - Support offset compensation
  - Support gain compensation
- Multi-ADC mode
  - Dual ADC mode: ADC1 and ADC2 combined
  - Triple ADC mode: ADC1, ADC2, and ADC3 combined
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$

2.27 Digital/Analog Converter (DAC)

The DAC is a digital-to-analogue converter, primarily accepting digital inputs and providing voltage outputs. DAC data operates in either 8-bit or 12-bit modes and supports DMA functionality. When configured for 12-bit mode, DAC data may be left-aligned or right-aligned; when set to 8-bit mode, DAC data is right-aligned. Each DAC possesses an independent converter capable of performing conversions autonomously. In dual-DAC mode, each DAC may convert independently, or both DACs (DAC1 and DAC2 may form a pair) may convert and update simultaneously. VREF+ is input via a pin as the DAC reference voltage, enhancing the precision of the DAC conversion data. The integrated VREFBUF may also serve as the DAC reference voltage. For details on the voltage reference buffer (VREFBUF), refer to the VREFBUF section.

When the DAC output is internally connected to on-chip peripherals, the DACx_OUT pin may function as a general-purpose input/output (GPIO). The DAC output buffer may be selectively enabled to achieve high drive output current.

Main features:

- Supports 2 DACs, each DAC has its own converter
- Supports 8-bit or 12-bit output, with left or right data aligned in 12-bit mode
- Dual DAC channel for independent or synchronous conversions
- Each DAC supports DMA functionality including DMA underrun error detection
- DMA double data mode can save bus bandwidth
- Generates Noise-wave, Triangular-wave and Sawtooth waveforms.
- Buffer offset calibration.
- Input voltage reference from V_{REF+} and internal VREFBUG.
- External triggers for conversion

2.28 Voltage Reference Buffer (VREFBUF)

The chip is equipped with a voltage reference buffer that can be used as a voltage reference for the ADC, 12-bit DAC. It can also serve as a voltage reference for external components through the VREF+ pin.

2.29 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated during the link-time and generating of the software.

Main features of CRC32:

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- CRC32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)
- 32-bit data to be checked and 32-bit output checksum
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- General-purpose 8-bit register
- Programmable CRC initial value

Main features of CRC16:

- CRC16 ($X^{16} + X^{15} + X^2 + 1$)
- 8-bit data to be checked and 16-bit output checksum
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- Configurable check initial value, and configurable endianness of the data to be checked
- Support 8-bit LRC checksum value generation
- Programmable CRC initial value

2.30 Secure Algorithm Co-processor (SAC)

The device features a secure algorithm co-processor, it supports a variety of international algorithms hash cryptography algorithm acceleration, which can greatly improve the speed of encryption and decryption compared with pure software algorithm.

The hardware supports the following algorithms:

- Support DES symmetric algorithms
  - DES and 3DES encryption and decryption operations are supported
  - TDES supports 2KEY and 3KEY mode
  - Support CBC and ECB mode
- Support the symmetric AES algorithm
  - Support 128bits, 192bits, or 256bits key length
  - Support CBC, ECB, and CTR mode
- Support the symmetric SM4 algorithm
  - Support CBC, ECB mode
- Support SHA hash algorithm
  - Support SHA1, SHA244, SHA256
- Support the MD5 digest algorithm
- Support SM3 hash algorithm
- Support random number generation

Note: The SAC module operating clock is up to 120MHz.

2.31 Ethernet (ETH)

N32H497 supports an Ethernet peripheral module, ETH contains a 10/100Mbps Ethernet MAC. The ETH module utilizes dedicated DMA to optimize the performance of sending and receiving data frames, supports standard

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interfaces for MII, RMII, and physical layer (PHY) communication, enabling the transmission and reception of Ethernet data frames.

The Ethernet module complies with the following standards:

- IEEE 802.3-2015 for Ethernet MAC and media independent interface (MII)
- IEEE 1588-2008 for precision networked clock synchronization (PTP)
- AMBA 2.0 for AHB master and AHB slave ports
- RMII specification version 1.2 from RMII consortium

Main features are as following:

2.31.1 MAC Features

MAC Tx and Rx common features

- Separate transmission, reception, and control interfaces to the application
- 10, 100 Mbps data transfer rates with the following PHY interfaces:
  - MII interface to communicate with an external Fast Ethernet PHY
  - RMII interface to communicate with an external Fast Ethernet PHY
- Half-duplex operation:
  - CSMA/CD protocol support
  - Flow control using backpressure
- 32-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- Network statistics with RMON or MIB counters (partial support of RFC2819/RFC2665)
- Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet)
- Flexibility to control pulse-per-second (PPS) output signal
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

MAC Tx features

- Preamble and start-of-frame data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-frame basis
- Programmable packet length to support Standard or Jumbo Ethernet packets of up to 16 Kbytes
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in Full-duplex mode)

MAC Rx features

- Automatic Pad and CRC stripping options
- Preamble and SFD deletion
- Programmable watchdog timeout limit
- Flexible address filtering modes:

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  - Four 48-bit perfect (DA) address filters with masks for each byte
  - Four 48-bit SA address comparison check with masks for each byte
  - 64 bit Hash filter for multicast and unicast (DA) addresses
- Option to pass all multicast addressed packets
- Promiscuous mode to pass all packets without any filtering for network monitoring
- Pass all incoming packets (as per filter) with a status report
- Additional packet filtering:
  - VLAN tag-based: Perfect match and Hash-based filtering based either on the outer or inner VLAN tag
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Detection of remote wake-up packets and AMD magic packets
- Optional forwarding of received Pause packets to the application (in Full-duplex mode)

2.31.2 Transaction Layer (MTL) Features

MTL Tx and Rx Common Features

- 32-bit Transaction Layer block (bridges the application and the MAC)
- Optimization for packet-oriented transfers with packets delimiters
- Single-port RAM based on synchronous FIFO controller
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the EQOS-MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)

MTL Tx features

- 2048-byte Transmit FIFO with programmable threshold capability
- Support a queue on the transmit path
- Store-and-forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Automatic retransmission of collision packets in Half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and underrun conditions with appropriate status
- Module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum on frames transmitted in Store-and-forward mode
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO
- Packet-level control for
  - Timestamp control
  - CRC and pad control

MTL Rx features

- 2048-byte Receive FIFO with configurable threshold
- Support a queue on the receive path
- Insert Rx status vector into Rx queue after EOP/EOF (threshold mode) and before SOP/SOF.
- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cutthrough) mode

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- Option to filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Option to forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level

2.31.3 DMA Block Features

- 32-bit data transfers
- Separate DMA in Transmit path and receive paths
- Optimization for packet-oriented DMA transfers with packet delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture allowing large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 Kbytes of data)
- Comprehensive status reporting normal operation and transfer errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host control (AHB) access and host data interface
- Independent port for host CSR (Control Status Register) access and host data interface

2.32 Digital Video Interface (DVP)

DVP is a flexible and powerful CMOS optical sensor interface, which can easily realize the customer's image acquisition requirements, and the entire acquisition process does not require CPU intervention.

This module is capable of receiving high-speed data from traditional or ITU-R BT.656 format CMOS image sensors. It also supports the data formats YCbCr422 and RGB565 progressive, as well as compressed data (JPEG).

Main features:

- Pure hardware acquisition method
- Pure input interface
- Support traditional synchronous parallel interfaces of 8-bit, 10-bit, 12-bit, and 16-bit
- Support 8-bit and 10-bit ITU-R BT.656 video formats
- Support 8-bit and 16-bit YCbCr, YUV, and RGB data formats
- Support 8-bit, 10-bit, and 16-bit Bayer data formats
- Support clock output (24MHz@typical) to provide clock for external CMOS chip

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- The input pixel clock DVP_PCLK, field sync signal DVP_VSYNC, and line sync signal DVP_HSYNC polarities can be independently configured
- 16x4 byte FIFO for receiving pixel data
- Support FIFO overflow protection
- Support DMA, image acquisition process without CPU intervention
- The image size must be a multiple of 4
- Support the inversion operation on the captured image
- Support a maximum of 1280*720@30Hz
- Support continuous mode and snapshot mode
- Support hardware cropping
- Support the following data formats:
- 8/10/12/14-bit progressive video: either monochrome or raw bayer
  - YCbCr422 progressive video
  - RGB 565 progressive video
  - Compressed data: JPEG

2.33 Unique Device Serial Number (UID)

The N32H497 series products have two built-in unique device serial numbers of different lengths, which are 96-bit unique device ID (UID) and 128-bit unique customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32H497 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory. It can also be used to activate Secure Bootloader with security functions.

The UCID is 128-bit, which complies with the definition of Nations technology chip serial number. It contains the information related to chip production and version.

2.34 Serial Single-Wire JTAG Debug Port (SWJ-DP)

The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

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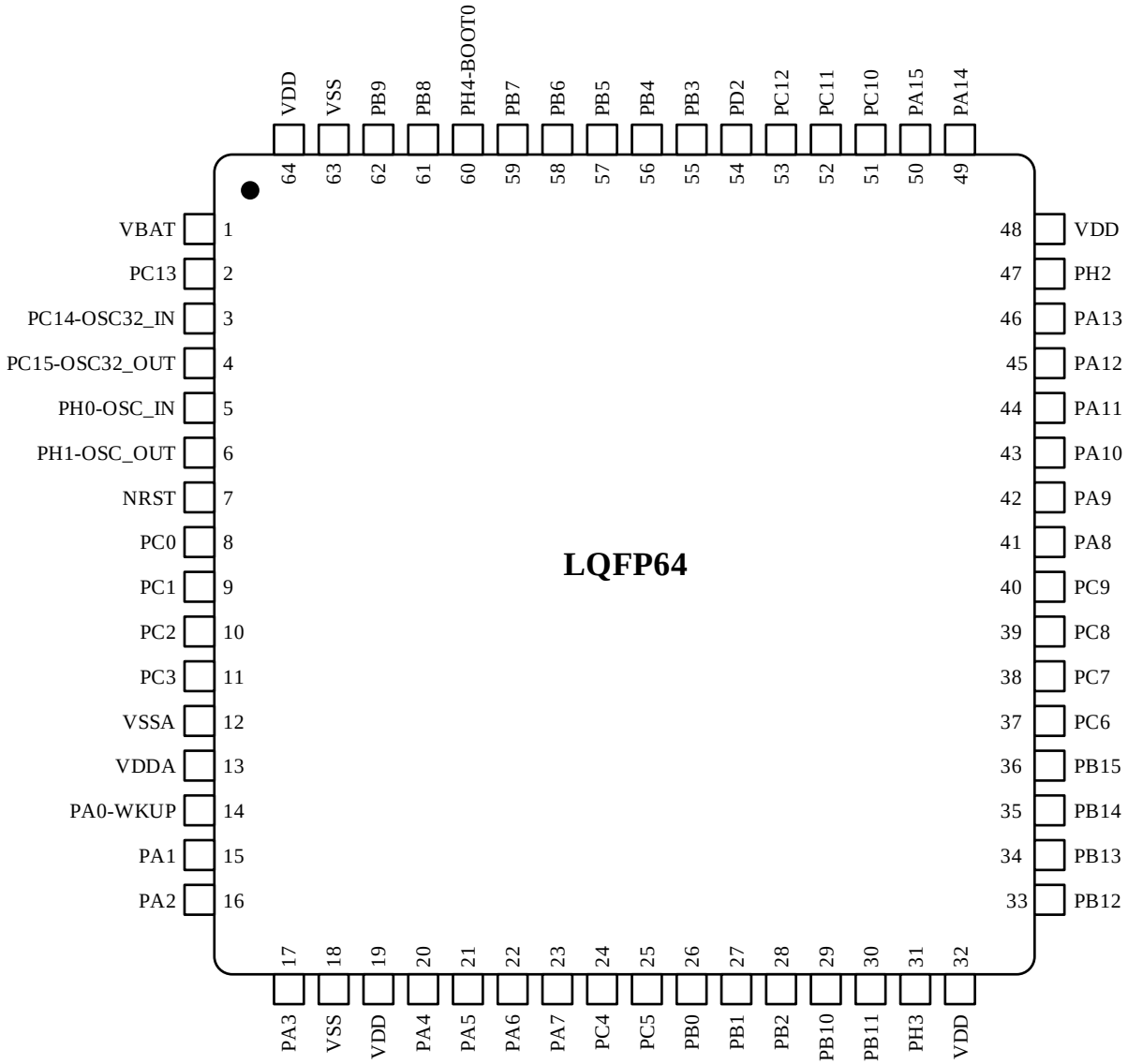
3 Pinouts and Pin Description

3.1 Pinouts

3.1.1 LQFP64

Figure 3-1 LQFP64 Pinout



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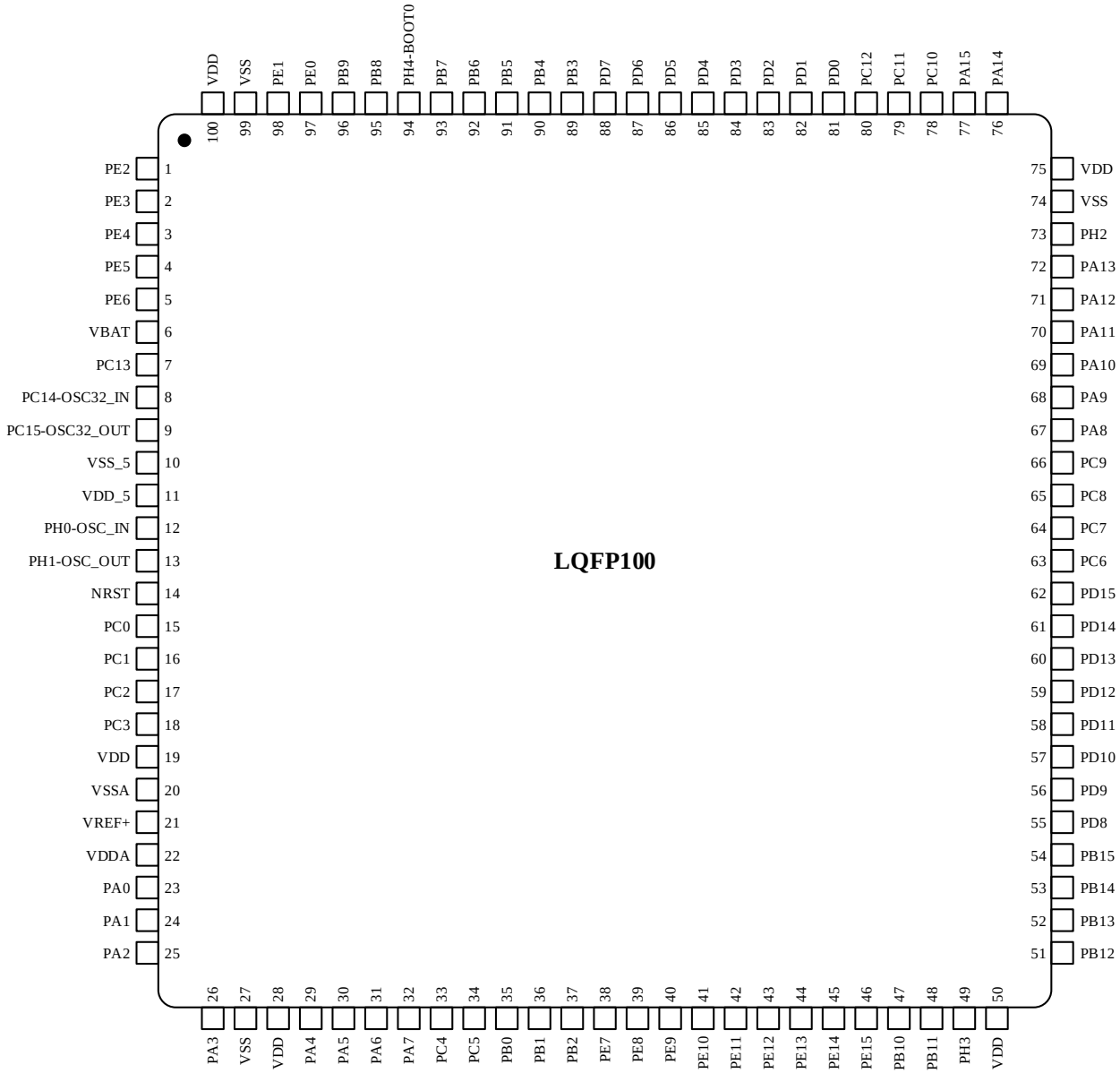
3.1.2 LQFP100

Figure 3-2 LQFP100 Pinout



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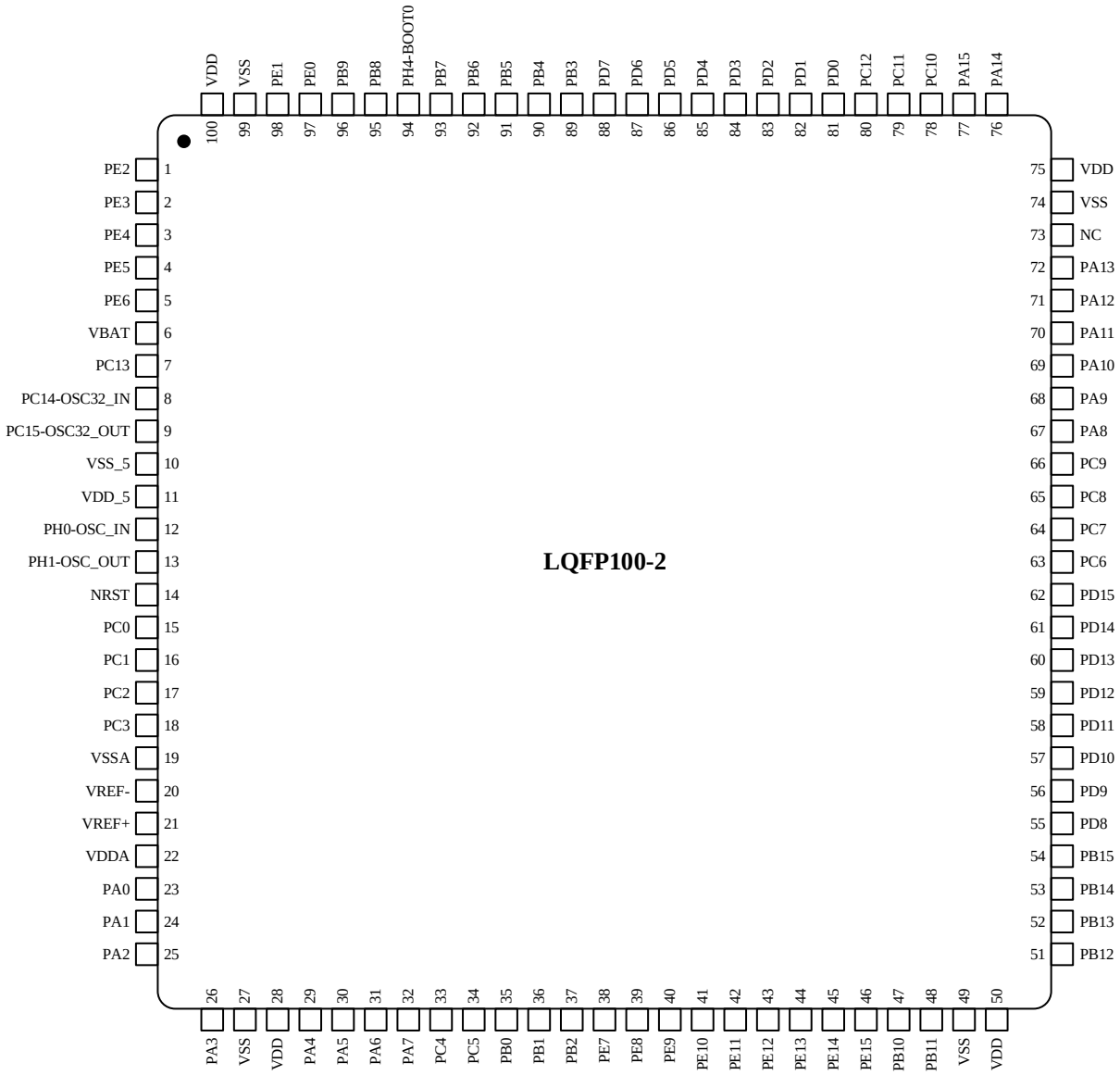
3.1.3 LQFP100-2

Figure 3-3 LQFP100-2 Pinout



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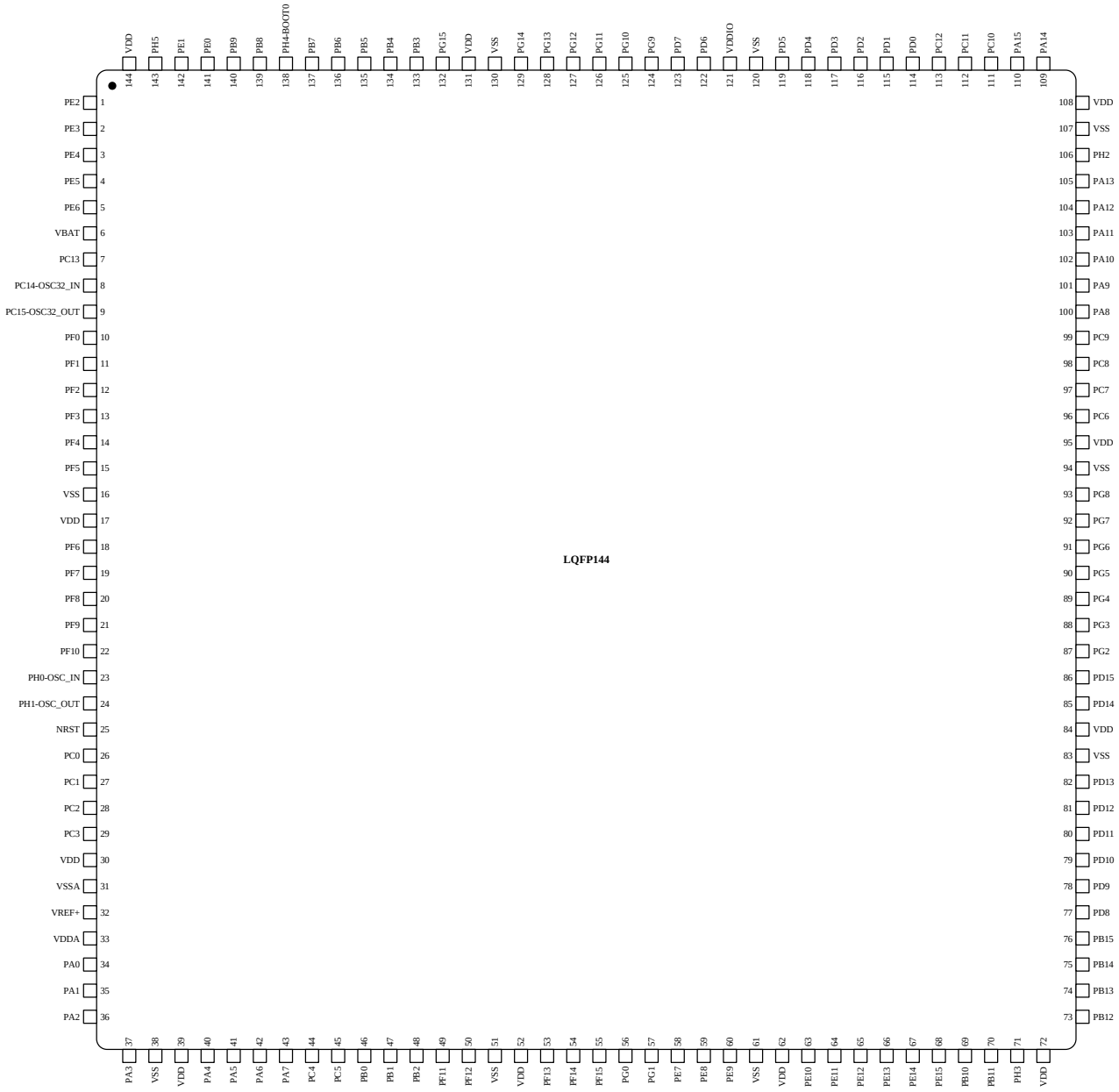
3.1.4 LQFP144

Figure 3-4 LQFP144 Pinout



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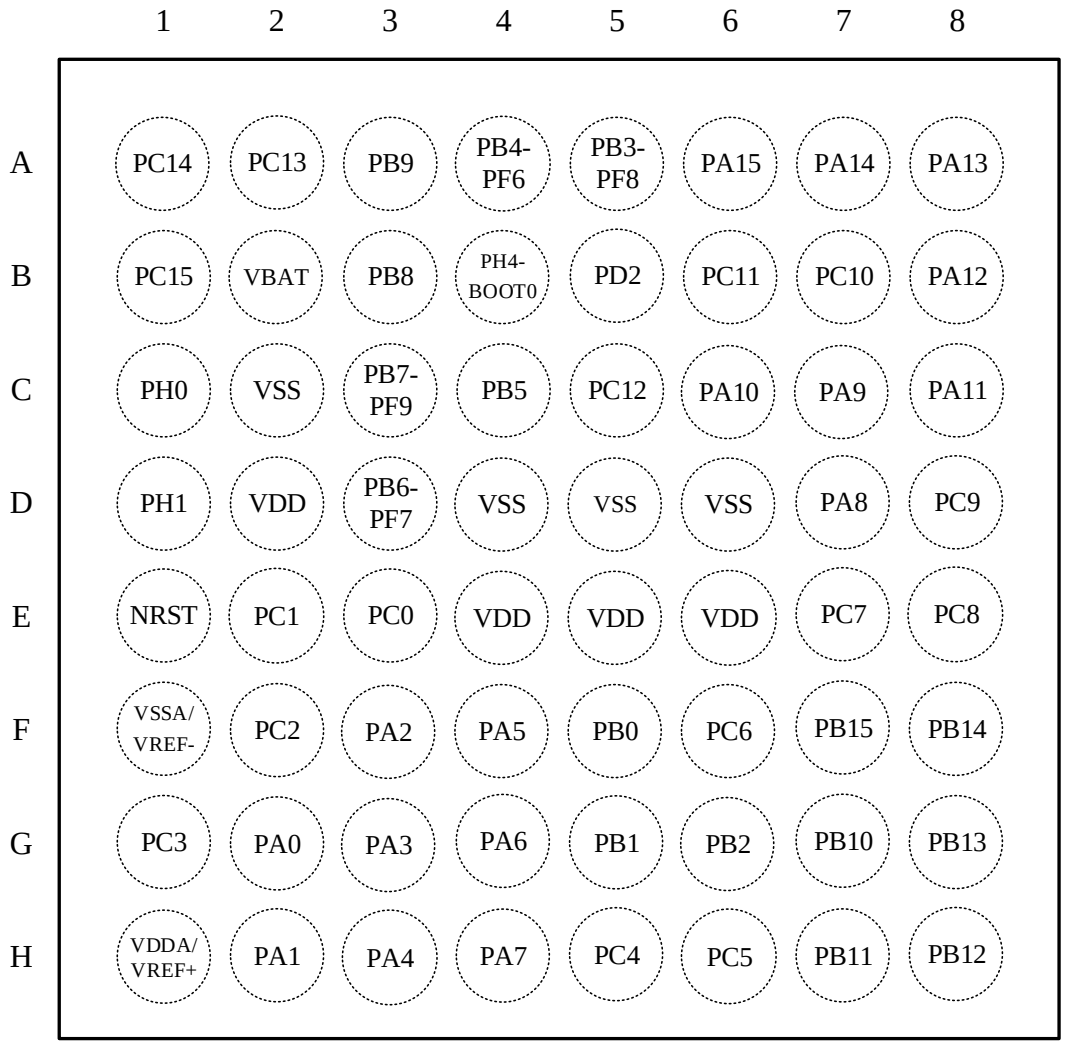
3.1.5 BGA64

Figure 3-5 BGA64 Pinout



Top view

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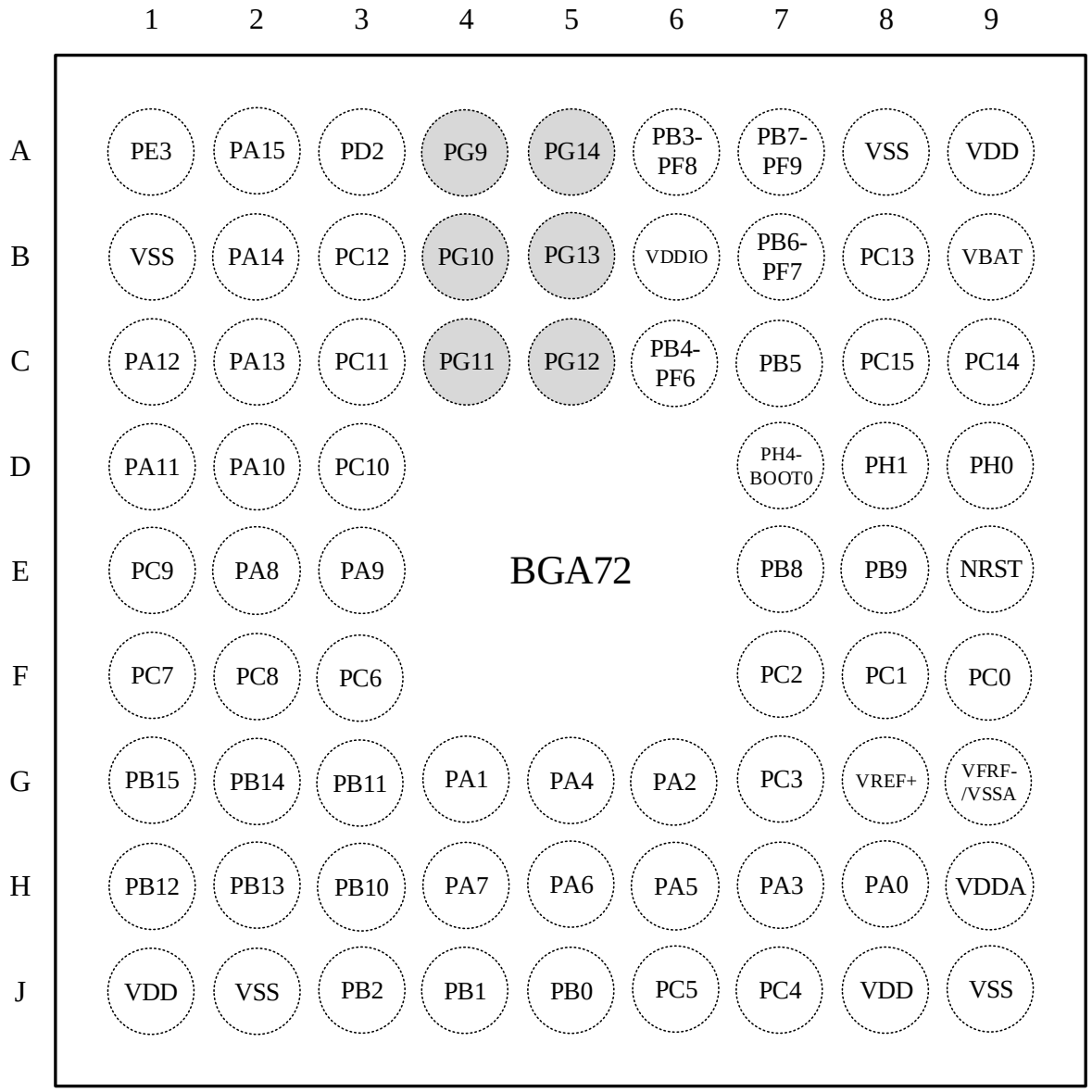
3.1.6 BGA72

Figure 3-6 BGA72 Pinout



Top view

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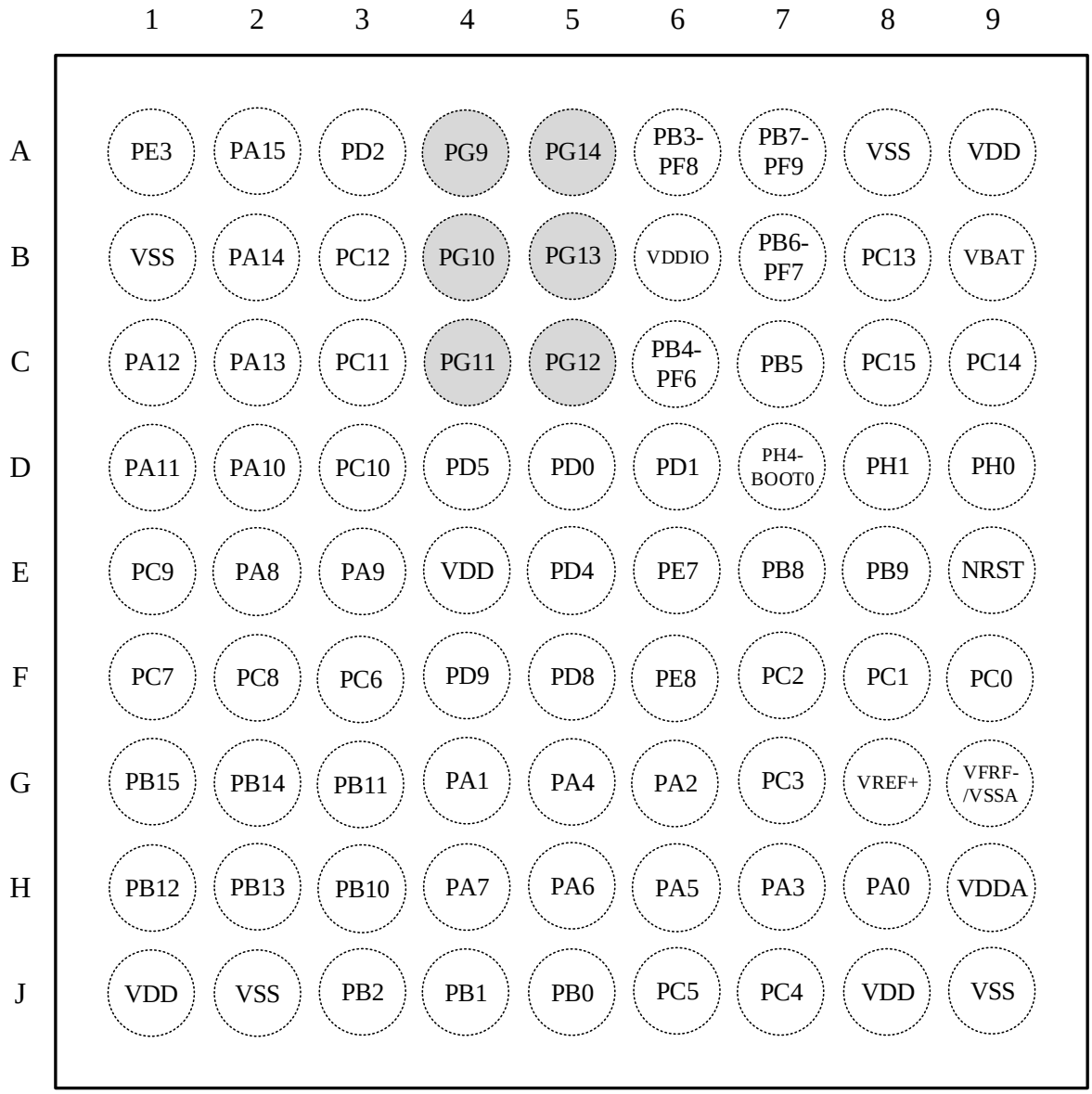
3.1.7 BGA81

Figure 3-7 BGA81 Pinout



Top view

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3.2 Pin Description

Table 3-1 Pin Description

Package							Pin name (function after reset)	Pin type(1)	I/O structure(2)	Fail-safe(3)	Alternate functions	Additional functions
LQFP64	BGA64	BGA72	BGA81	LQFP100	LQFP100-2	LQFP144						
-	-	-	-	1	1	1	PE2	I/O	FT	Y	FEMC_A23 ETH_MII_TX_D3 GTIM2_CH1_ETR SPI4_SCK ATIM3_CH1 USART4_TX DVP_HSYNC XSPI_IO2 DVP_D3 USART9_RX UART7_TX EVENTOUT	-
-	-	A1	A1	2	2	2	PE3	I/O	FT	Y	FEMC_A19 GTIM2_CH2 SPI4_NSS ATIM3_CH2 USART4_RX DVP_VSYNC GTIM8_BKIN USART9_TX GTIM2_CH1 EVENTOUT	-
-	-	-	-	3	3	3	PE4	I/O	FT	Y	FEMC_A20 DVP_D4 GTIM2_CH3 SPI4_NSS ATIM3_CH1N DVP_PIXCLK DSMU_DATIN3 GTIM8_CH1N GTIM2_CH2 EVENTOUT	-
-	-	-	-	4	4	4	PE5	I/O	FT	Y	FEMC_A21 GTIM5_CH1 DVP_D6 GTIM2_CH4 SPI4_MISO ATIM3_CH2N DVP_D0 DSMU_CKIN3 GTIM8_CH1 GTIM2_CH3 EVENTOUT	-
-	-	-	-	5	5	5	PE6	I/O	FT	Y	FEMC_A22 GTIM5_CH2 DVP_D7 SPI4_MOSI ATIM3_CH3N DVP_D1 LPTIM2_IN1 GTIM8_CH2 ATIM1_BKIN2 GTIM2_CH4 EVENTOUT	WKUP0 RTC_TAMP3
1	B2	B9	B9	6	6	6	VBAT	S	-	-	-	-

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2	A2	B8	B8	7	7	7	PC13	I/O	FT	Y	RTC_OUT1 ATIM1_CH1N ATIM1_BKIN ATIM2_CH4N LPTIM2_ETR XSPI_RXDS ATIM3_BKIN EVENTOUT	WKUP2 RTC_TAMP1
3	A1	C9	C9	8	8	8	PC14-OSC32_IN	I/O	FT	Y	GTIM7_CH3 EVENTOUT	OSC32_IN
4	B1	C8	C8	9	9	9	PC15-OSC32_OUT	I/O	FT	Y	GTIM7_CH4 EVENTOUT	OSC32_OUT
-	-	-	-	-	-	10	PF0	I/O	FT	Y	FEMC_A0 I2C2_SDA ATIM3_CH1 XSPI_NSS1 UART8_CTS SDRAM_A0 SDRAM_D10 ATIM2_CH1 EVENTOUT	-
-	-	-	-	-	-	11	PF1	I/O	FT	Y	FEMC_A1 I2C2_SCL ATIM3_CH2 XSPI_CLK SDRAM_A1 SDRAM_D11 ATIM2_CH1N ATIM2_CH2 EVENTOUT	-
-	-	-	-	-	-	12	PF2	I/O	FT	Y	FEMC_A2 I2C2_SMBA ATIM3_CH3 XSPI_IO0 SDRAM_A2 USART3_CK UART10_TX SDRAM_D12 ATIM2_CH3 EVENTOUT	-
-	-	-	-	-	-	13	PF3	I/O	FTa	Y	FEMC_A3 ATIM3_CH4 I2C3_SCL XSPI_IO1 SDRAM_A3 SDRAM_D13 ATIM2_CH3N ATIM2_CH4 EVENTOUT	ADC3_IN9
-	-	-	-	-	-	14	PF4	I/O	FTa	Y	FEMC_A4 ATIM3_CH1N I2C3_SDA XSPI_IO2 GTIM5_CH1 I2C3_SCL SDRAM_A4 SDRAM_D14 ATIM3_CH2 GTIM9_ETR EVENTOUT	ADC3_IN14
-	-	-	-	-	-	15	PF5	I/O	FTa	Y	FEMC_A5 ATIM3_CH2N XSPI_IO3 GTIM5_CH2 I2C3_SDA SDRAM_A5	ADC3_IN15

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											I2C4_SCL USART3_CTS UART10_RX SDRAM_D15 GTIM9_ETR EVENTOUT	
-	C2	-	-	10	10	16	VSS	S	-	-	-	-
-	D2	-	-	11	11	17	VDD	S	-	-	-	-
-	A4	C6	C6	-	-	18	PF6	I/O	FTa	Y	GTIM6_CH1 GTIM4_ETR GTIM3_CH4 I2C2_SCL GTIM4_CH1 XSPI_IO3 SPI5_NSS UART7_RX DVP_D14 ATIM1_BKIN2 GTIM9_CH1 SDRAM_D0 EVENTOUT	ADC3_IN4
-	D3	B7	B7	-	-	19	PF7	I/O	FTa	Y	GTIM7_CH1 ATIM3_BKIN GTIM4_CH2 XSPI_IO2 FEMC_A1 SPI5_SCK UART7_TX GTIM8_ETR GTIM10_CH1 SDRAM_A1 SDRAM_D1 EVENTOUT	ADC3_IN5
-	A5	A6	A6	-	-	20	PF8	I/O	FTa	Y	GTIM9_CH1 ATIM3_BKIN2 GTIM4_CH3 XSPI_IO0 FEMC_A24 SPI5_MISO GTIM9_CH1N GTIM6_CH1 SDRAMM_D2 ATIM2_CH1N ATIM2_CH2 EVENTOUT	ADC3_IN6
-	C3	A7	A7	-	-	21	PF9	I/O	FTa	Y	GTIM10_CH1 ATIM3_BKIN GTIM8_CH1 SPI2_SCK/I2S2_CK GTIM4_CH4 XSPI_IO1 FEMC_A25 SPI5_MOSI DVP_D15 UART8_CTS GTIM10_CH1N GTIM7_CH1 SDRAM_D3 EVENTOUT	ADC3_IN7
-	-	-	-	-	-	22	PF10	I/O	FTa	Y	ATIM3_BKIN2 GTIM8_CH2 SPI2_SCK/I2S2_CK XSPI_CLK FEMC_A0 DVP_D11 GTIM9_BKIN SDRAM_A0	ADC3_IN8

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											SDRAM_D4 ATIM2_CH2N EVENTOUT	
5	C1	D9	D9	12	12	23	PH0-OSC_IN	I/O	FT	Y	I2C2_SDA SPI2_NSS/I2S2_WS ATIM1_CH3N USART2_RX GTIM5_CH3 ATIM3_CH1N XSPI_IO4 EVENTOUT	OSC_IN
6	D1	D8	D8	13	13	24	PH1-OSC_OUT	I/O	FT	Y	I2C2_SCL SPI2_SCK/I2S2_CK USART2_TX GTIM5_CH4 ATIM3_CH2N XSPI_NSS0 EVENTOUT	OSC_OUT
7	E1	E9	E9	14	14	25	NRST	I/O	RST	Y	-	-
8	E3	F9	F9	15	15	26	PC0	I/O	FTa	Y	LPTIM1_IN1 ATIM1_CH1 UART7_RX I2C3_SCL DVP_D2 USART4_TX XSPI_RXDS DVP_D15 GTIM10_CH1 SDRAM_NWE DSMU_CKIN0 DSMU_DATIN4 XSPI_IO7 FEMC_A25 GTIM9_BKIN EVENTOUT	ADC123_IN10
9	E2	F8	F8	16	16	27	PC1	I/O	FTa	Y	ETH_MDC LPTIM1_OUT ATIM1_CH2 UART7_TX XSPI_IO4 SPI3_MOSI/I2S3_SD SPI2_MOSI/I2S2_SD I2C3_SDA USART4_RX GTIM10_CH2 DSMU_DATIN0 DSMU_CKIN4 EVENTOUT	ADC123_IN11
10	F2	F7	F7	17	17	28	PC2	I/O	FTa	Y	SPI2_MISO/I2S2_AUX_SD ETH_MII_TX_D2 LPTIM1_IN2 ATIM1_CH3 ATIM3_CH2 XSPI_IO5 SPI3_NSS/I2S3_WS GTIM10_CH3 UART7_TX SDRAM_NE0 DSMU_CKIN1 XSPI_IO2 GTIM3_CH4 GTIM10_CH1 DSMU_CKOUT EVENTOUT	ADC123_IN12
11	G1	G7	G7	18	18	29	PC3	I/O	FTa	Y	SPI2_MOSI/I2S2_SD ETH_MII_TX_CLK	ADC123_IN13

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											LPTIM1_ETR ATIM1_CH4 ATIM1_BKIN2 XSPI_IO6 SPI3_SCK/I2S3_CK GTIM10_CH4 UART7_RX SDRAM_CKE0 DSMU_DATIN1 XSPI_IO0 LPTIM2_ETR EVENTOUT	
-	-	-	-	19	-	30	VDD	S	-	-	-	-
12	F1	G9	G9	20	19	31	VSSA	S	-	-	-	-
12	F1	G9	G9	20	20	31	VREF-	S	-	-	-	-
13	H1	G8	G8	21	21	32	VREF+	S	-	-	-	-
13	H1	H9	H9	22	22	33	VDDA	S	-	-	-	-
14	G2	H8	H8	23	23	34	PA0-WKUP1	I/O	FTa	Y	USART2_CTS UART6_TX ETH_MII_CRS GTIM1_CH1_ETR GTIM4_CH1 ATIM2_ETR ATIM2_BKIN SPI3_MISO/I2S3_AUX_SD ATIM3_CH3N SPI6_NSS GTIM8_BKIN EVENTOUT	ADC123_IN0 WKUP1 RTC_TAMP2
15	H2	G4	G4	24	24	35	PA1	I/O	FTa	Y	USART2_RTS_DE UART6_RX ETH_RMII_REF_CLK/ETH_MII_RX_CLK GTIM4_CH2 GTIM1_CH2 RTC_REFIN GTIM8_CH1N SPI4_MOSI DVP_HSYNC SPI3_MOSI/I2S3_SD SPI6_SCK ATIM3_CH4N XSPI_IO3 XSPI_RXDS EVENTOUT	ADC123_IN1
16	F3	G6	G6	25	25	36	PA2	I/O	FTa	Y	USART2_TX GTIM4_CH3 GTIM5_CH1 GTIM1_CH3 ETH_MDIO GTIM8_CH1_ETR XSPI_NSS0 UART7_TX I2S_CKIN DVP_VSYNC SPI6_NSS DSMU_CKIN7 LPTIM1_IN2 EVENTOUT	ADC123_IN2 WKUP3 LSCO
17	G3	H7	H7	26	26	37	PA3	I/O	FTa	Y	USART2_RX GTIM4_CH4 GTIM5_CH2 GTIM1_CH4 ETH_MII_COL GTIM8_CH2 XSPI_CLK UART7_RX	ADC123_IN3

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											I2S2_MCK DVP_PIXCLK MCO2 DSMU_DATIN7 EVENTOUT	
18	D4	J9	J9	27	27	38	VSS	S	-	-	-	-
19	E4	J8	J8	28	28	39	VDD	S	-	-	-	-
20	H3	G5	G5	29	29	40	PA4	I/O	TTa	Y	SPI1_NSS SPI3_NSS/I2S3_WS USART2_CK DVP_HSYNC USB_HS_SOF GTIM2_CH2 DVP_D0 XSPI_NSS1 I2C2_SCL SPI6_MISO GTIM7_CH1 LPTIM2_IN2 USART1_TX SPI6_NSS EVENTOUT	ADC12_IN4 DAC1_OUT
21	F4	H6	H6	30	30	41	PA5	I/O	TTa	Y	SPI1_SCK GTIM1_CH1_ETR ATIM2_CH1N DVP_D1 XSPI_CLK I2C2_SDA SPI6_MOSI USART1_RX XSPI_IO0 GTIM7_CH2 SPI6_SCK ETH_MII_TX_EN/ETH_RMII_TX_EN LPTIM2_ETR EVENTOUT	ADC12_IN5 DAC2_OUT
22	G4	H5	H5	31	31	42	PA6	I/O	FTa	Y	SPI1_MISO ATIM2_BKIN GTIM9_CH1 DVP_PIXCLK GTIM2_CH1 ATIM1_BKIN XSPI_IO3 UART7_CTS I2S2_MCK SDIO_CMD DVP_D2 XSPI_IO0 SPI6_MISO GTIM6_CH1 EVENTOUT	ADC12_IN6
23	H4	H4	H4	32	32	43	PA7	I/O	FTa	Y	SPI1_MOSI ATIM2_CH1N GTIM7_CH1 GTIM2_CH2 ETH_MII_RX_DV/ETH_RMII_CRS_DV ATIM1_CH1N GTIM10_CH1 XSPI_IO2 DVP_D3 XSPI_IO1 MCO1 GTIM9_CH2 FEMC_NWE SDRAM_NWE SPI6_MOSI EVENTOUT	ADC12_IN7

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24	H5	J7	J7	33	33	44	PC4	I/O	FTa	Y	ETH_RMII_RX_D0/ETH_MII_RX_D0 ATIM1_ETR I2C2_SCL USART1_TX XSPI_IO7 DVP_D4 XSPI_IO2 UART7_TX I2C3_SCL LPTIM2_OUT ATIM3_CH3N DSMU_CKIN2 SDRAM_NE0 GTIM1_CH4 EVENTOUT	ADC12_IN14
25	H6	J6	J6	34	34	45	PC5	I/O	FTa	Y	ETH_RMII_RX_D1/ETH_MII_RX_D1 GTIM8_BKIN ATIM1_CH4N USART1_RX DVP_D5 XSPI_IO3 UART7_RX I2C3_SDA GTIM5_ETR DSMU_DATIN2 XSPI_RXDS SDRAM_CKE0 UART10_RTS_DE EVENTOUT	ADC12_IN15 WKUP4
26	F5	J5	J5	35	35	46	PB0	I/O	FTa	Y	GTIM2_CH3 ATIM2_CH2N ETH_MII_RX_D2 ATIM1_CH2N XSPI_IO1 SPI5_SCK SPI3_MOSI/I2S3_SD SDIO_D1 DVP_D6 USART4_TX DSMU_CKOUT UART6_CTS USART3_CK EVENTOUT	ADC12_IN8
27	G5	J4	J4	36	36	47	PB1	I/O	FTa	Y	GTIM2_CH4 ATIM2_CH3N ETH_MII_RX_D3 ATIM1_CH3N XSPI_IO0 UART7_RTS_DE SPI5_NSS SDIO_D2 DVP_D7 USART4_RX DSMU_DATIN1 LPTIM2_IN1 EVENTOUT	ADC12_IN9
28	G6	J3	J3	37	37	48	PB2	I/O	FTa	Y	RTC_OUT2 LPTIM1_OUT GTIM4_CH1 ATIM3_CH1 I2C3_SMBA XSPI_IO5 GTIM1_CH4 SPI3_MOSI/I2S3_SD SDIO_CLK DVP_D3 UART6_TX	ADC3_IN16

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											SPI1_NSS GTIM6_ETR DSMU_CKIN1 EVENTOUT	
-	-	-	-	-	-	49	PF11	I/O	FT	Y	DVP_D12 ATIM3_ETR FEMC_NE4 SPI5_MOSI SDRAM_NRAS XSPI_CLK SDRAM_D7 ATIM1_CH3N ATIM1_CH4 EVENTOUT	-
-	-	-	-	-	-	50	PF12	I/O	FT	Y	FEMC_A6 ATIM3_CH1 DVP_D4 SDRAM_A6 SDRAM_BA0 SDRAM_A11 EVENTOUT	-
-	D5	J2	J2	-	-	51	VSS	S	-	-	-	-
-	E5	J1	J1	-	-	52	VDD	S	-	-	-	-
-	-	-	-	-	-	53	PF13	I/O	FT	Y	FEMC_A7 ATIM3_CH2 I2C4_SMBA DVP_D5 MCO1 SDRAM_A7 DSMU_DATIN6 SDRAM_NE0 XSPI_IO4 ATIM3_CH1N EVENTOUT	-
-	-	-	-	-	-	54	PF14	I/O	FT	Y	FEMC_A8 ATIM3_CH3 I2C4_SCL DVP_D6 MCO2 SDRAM_A8 DSMU_CKIN6 SDRAM_NRAS XSPI_IO5 ATIM2_CH1 EVENTOUT	-
-	-	-	-	-	-	55	PF15	I/O	FT	Y	FEMC_A9 ATIM3_CH4 I2C4_SDA DVP_D7 SDRAM_A9 SDRAM_NCAS XSPI_IO6 ATIM2_CH2 ATIM3_CH3N EVENTOUT	-
-	-	-	-	-	-	56	PG0	I/O	FT	Y	FEMC_A10 ATIM3_CH1N UART7_TX GTIM7_CH2 SDRAM_A10 SDRAM_NWE XSPI_IO7 GTIM9_CH3 EVENTOUT	-
-	-	-	-	-	-	57	PG1	I/O	FT	Y	FEMC_A11 ATIM3_CH2N	-

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											UART7_RX GTIM7_CH3 SDRAM_A11 SPI2_MOSI/I2S2_SD SDRAM_NBL0 GTIM9_CH4 EVENTOUT	
-	-	-	E6	38	38	58	PE7	I/O	FT	Y	FEMC_D4 ATIM1_ETR UART7_RX UART6_RX SPI1_SCK GTIM4_CH2 GTIM9_CH4 SDRAM_D4 DSMU_DATIN2 XSPI_IO4 UART10_RTS_DE EVENTOUT	-
-	-	-	F6	39	39	59	PE8	I/O	FT	Y	FEMC_D5 ATIM1_CH1N GTIM4_CH3 UART7_TX SDIO_D0 SPI1_MISO SDRAM_D5 DSMU_CKIN2 UART10_CTS XSPI_IO5 EVENTOUT	-
-	-	-	-	40	40	60	PE9	I/O	FT	Y	FEMC_D6 ATIM1_CH1 GTIM4_CH4 SDIO_D1 SPI1_MOSI SDRAM_D6 DSMU_CKOUT XSPI_IO6 UART10_RX EVENTOUT	-
-	-	-	-	-	-	61	VSS	S	-	-	-	-
-	-	-	-	-	-	62	VDD	S	-	-	-	-
-	-	-	-	41	41	63	PE10	I/O	FT	Y	FEMC_D7 ATIM1_CH2N XSPI_CLK SDIO_D2 SPI2_NSS/I2S2_WS ATIM1_CH1N GTIM2_CH1 GTIM9_CH1 USART4_TX SDRAM_D7 DSMU_DATIN4 UART8_CTS XSPI_IO7 UART10_TX EVENTOUT	-
-	-	-	-	42	42	64	PE11	I/O	FT	Y	FEMC_D8 ATIM1_CH2 SPI4_NSS XSPI_NSS0 SPI5_NSS SDIO_D3 SPI2_SCK/I2S2_CK USART4_RX SDRAM_D8 DSMU_CKIN4	-

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											EVENTOUT	
-	-	-	-	43	43	65	PE12	I/O	FT	Y	FEMC_D9 ATIM1_CH3N SPI4_SCK XSPI_IO0 SPI5_SCK SDIO_CLK SPI2_MISO/I2S2_AUX_SD GTIM7_CH4 SDRAM_D9 DSMU_DATIN5 SPI1_NSS EVENTOUT	-
-	-	-	-	44	44	66	PE13	I/O	FT	Y	FEMC_D10 ATIM1_CH3 SPI4_MISO XSPI_IO1 SPI5_MISO SPI2_MOSI/I2S2_SD SDIO_CMD SDRAM_D10 DSMU_CKIN5 SPI1_SCK EVENTOUT	-
-	-	-	-	45	45	67	PE14	I/O	FT	Y	FEMC_D11 ATIM1_CH4 SPI4_MOSI ATIM1_BKIN2 XSPI_IO2 SPI5_MOSI SDRAM_D11 SPI1_MISO EVENTOUT	-
-	-	-	-	46	46	68	PE15	I/O	FT	Y	FEMC_D12 ATIM1_BKIN ATIM1_CH4N XSPI_IO3 I2C1_SDA USART4_RX GTIM10_CH1 SDRAM_D12 USART9_CK SPI1_MOSI EVENTOUT	-
29	G7	H3	H3	47	47	69	PB10	I/O	FTa	Y	SPI2_SCK/I2S2_CK I2C2_SCL ETH_MII_RX_ER GTIM1_CH3 UART7_RX XSPI_CLK ATIM1_BKIN SDIO_D7 FEMC_D11 DVP_D4 ATIM3_CH2 DSMU_DATIN7 XSPI_NSS1 SDRAM_D11 EVENTOUT	ADC3_IN17
30	H7	G3	G3	48	48	70	PB11	I/O	FTa	Y	I2C2_SDA ETH_RMII_TX_EN/ETH_MII_TX_EN GTIM1_CH4 UART7_TX XSPI_NSS0 I2S_CKIN FEMC_D12 DVP_D5	ADC2_IN16

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											ATIM3_CH3 DSMU_CKIN7 FEMC_NBL1 SDRAM_NBL1 SDRAM_D12 EVENTOUT	
31	-	-	-	49	-	71	PH3	I/O	FTa	Y	LPTIM2_IN1 UART8_CTS ATIM3_BKIN ATIM2_CH4N DVP_D12 GTIM5_CH1 DSMU_DATIN4 XSPI_IO5 EVENTOUT	ADC2_IN17
-	-	-	-	-	49	-	VSS	S	-	-	-	-
32	-	-	-	50	50	72	VDD	S	-	-	-	-
33	H8	H1	H1	51	51	73	PB12	I/O	FT	Y	SPI2_NSS/I2S2_WS I2C2_SMBA USART3_CK ATIM1_BKIN ETH_RMII_TX_D0/ETH_MII_TX_D0 USB_HS_ID GTIM4_ETR UART7_RTS_DE SPI4_NSS GTIM9_CH3 ATIM3_CH4 DSMU_DATIN1 XSPI_CLK I2C2_SDA EVENTOUT	-
34	G8	H2	H2	52	52	74	PB13	I/O	FT	Y	SPI2_SCK/I2S2_CK USART3_CTS ATIM1_CH1N ETH_RMII_TX_D1/ETH_MII_TX_D1 UART7_CTS SPI4_SCK ATIM1_CH2 GTIM10_CH2 GTIM9_CH4 DSMU_CKIN1 I2C2_SMBA SDIO_D0 UART8_CTS EVENTOUT	USB_HS_VBUS
35	F8	G2	G2	53	53	75	PB14	I/O	FT	N	SPI2_MISO/I2S2_AUX_SD ATIM1_CH2N GTIM8_CH1 ATIM2_CH2N GTIM9_CH2 USART4_CK DVP_D13 DSMU_DATIN2 USART1_TX UART6_RTS_DE GTIM5_CH1 EVENTOUT	USB_HS_DM
36	F7	G1	G1	54	54	76	PB15	I/O	FT	N	RTC_REFIN SPI2_MOSI/I2S2_SD ATIM1_CH3N ATIM2_CH3N GTIM8_CH2 GTIM8_CH1N ATIM2_CH4 UART8_CTS DVP_D14	USB_HS_DP

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											DSMU_CKIN2 USART1_RX XSPI_CLK ETH_MII_TX_D1/ETH_RMII_TX_D1 USART3_CTS EVENTOUT	
-	-	-	F5	55	55	77	PD8	I/O	FT	Y	FEMC_D13 ETH_MII_RX_DV ETH_RMII_CRS_DV SPI3_NSS/I2S3_WS ATIM1_CH3 GTIM10_CH1 SDRAM_D13 DSMU_CKIN3 EVENTOUT	-
-	-	-	F4	56	56	78	PD9	I/O	FT	Y	FEMC_D14 ETH_MII_RX_D0 ETH_RMII_RX_D0 SPI3_SCK/I2S3_CK ATIM1_CH3N GTIM9_CH3 GTIM7_ETR GTIM10_CH2 SDRAM_D14 DSMU_DATIN3 EVENTOUT	-
-	-	-	-	57	57	79	PD10	I/O	FT	Y	FEMC_D15 USART3_CK ETH_MII_RX_D1 ETH_RMII_RX_D1 ATIM1_CH4 ATIM3_ETR SDRAM_D15 DSMU_CKOUT EVENTOUT	-
-	-	-	-	58	58	80	PD11	I/O	FT	Y	FEMC_CLE/FEMC_A16 USART3_CTS GTIM4_ETR I2C4_SMBA ETH_MII_RX_D2 SPI3_MISO/I2S3_AUX_SD USART4_TX I2C1_SCL GTIM10_CH3 UART6_RX XSPI_IO0 LPTIM2_IN2 LPTIM2_ETR EVENTOUT	-
-	-	-	-	59	59	81	PD12	I/O	FT	Y	FEMC_ALE/FEMC_A17 GTIM3_CH1 ETH_MII_RX_D3 SPI3_MOSI/I2S3_SD GTIM6_CH1 UART6_TX I2C4_SCL I2C3_SCL XSPI_IO1 DVP_D12 LPTIM1_IN1 LPTIM2_IN1 EVENTOUT	-
-	-	-	-	60	60	82	PD13	I/O	FT	Y	FEMC_A18 GTIM3_CH2 XSPI_RXDS GTIM6_CH2 I2C4_SDA	-

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											I2C3_SDA XSPI_IO3 DVP_D13 LPTIM1_IN1 LPTIM2_IN2 LPTIM2_OUT EVENTOUT	
-	-	-	-	-	-	83	VSS	S	-	-	-	-
-	-	-	-	-	-	84	VDD	S	-	-	-	-
-	-	-	-	61	61	85	PD14	I/O	FT	Y	FEMC_D0 GTIM3_CH3 I2C4_SCL ATIM2_CH1 GTIM10_CH4 GTIM6_CH3 SDRAM_D0 UART7_CTS EVENTOUT	-
-	-	-	-	62	62	86	PD15	I/O	FT	Y	FEMC_D1 GTIM3_CH4 SPI2_NSS/I2S2_WS I2C4_SDA ATIM2_CH2 ATIM2_CH1N GTIM8_CH1 GTIM6_CH4 SDRAM_D1 UART7_RTS_DE EVENTOUT	-
-	-	-	-	-	-	87	PG2	I/O	FT	Y	FEMC_A12 ATIM3_CH3N SPI1_SCK I2C2_SCL GTIM5_ETR SDRAM_A12 ATIM2_BKIN UART10_RX SDRAM_BA1 ATIM3_CH4 EVENTOUT	-
-	-	-	-	-	-	88	PG3	I/O	FT	Y	FEMC_A13 ATIM3_BKIN I2C4_SCL SPI1_MISO ATIM3_CH4N I2C2_SDA ATIM2_BKIN2 UART10_TX SDRAM_A10 GTIM8_CH3 EVENTOUT	-
-	-	-	-	-	-	89	PG4	I/O	FT	Y	FEMC_A14 ATIM3_BKIN2 I2C4_SDA SPI1_MOSI GTIM6_ETR SDRAM_BA0 ATIM1_BKIN2 SDRAM_A0 GTIM8_CH4 EVENTOUT	-
-	-	-	-	-	-	90	PG5	I/O	FT	Y	FEMC_A15 ATIM3_ETR SPI1_NSS UART7_CTS SDRAM_BA1	-

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											ATIM1_ETR SDRAM_A1 ATIM2_CH3N EVENTOUT	
-	-	-	-	-	-	91	PG6	I/O	FT	Y	FEMC_INT2 ATIM3_BKIN I2C3_SMBA UART7_RTS_DE DVP_D12 I2C4_SDA I2C3_SDA XSPI_NSS0 FEMC_NE3 GTIM10_BKIN SDRAM_A2 EVENTOUT	-
-	-	-	-	-	-	92	PG7	I/O	FT	Y	FEMC_INT3 USART4_CK I2C3_SCL UART7_TX DVP_D13 I2C4_SCL SDRAM_A3 ATIM1_CH1N ATIM1_CH2 GTIM9_CH2 EVENTOUT	-
-	-	-	-	-	-	93	PG8	I/O	FT	Y	USART4_RTS_DE ETH_PPS_OUT I2C3_SDA UART7_RX FEMC_NE3 XSPI_NSS1 SDRAM_CLK SPI6_NSS ATIM2_ETR SDRAM_A4 ATIM1_CH2N GTIM9_CH3 EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	E4	-	-	95	VDD	S	-	-	-	-
37	F6	F3	F3	63	63	96	PC6	I/O	FT	Y	I2S2_MCK ATIM2_CH1 SDIO_D6 USART4_TX DVP_D0 GTIM2_CH1 I2C4_SCL SPI2_NSS/I2S2_WS USART2_CTS FEMC_A16/FEMC_CLE ATIM2_CH2 DSMU_CKIN3 XSPI_IO5 FEMC_NWAIT EVENTOUT	-
38	E7	F1	F1	64	64	97	PC7	I/O	FT	Y	I2S3_MCK ATIM2_CH2 SDIO_D7 USART4_RX DVP_D1 GTIM2_CH2 I2C4_SDA SPI2_SCK/I2S2_CK USART2_RTS_DE FEMC_A17/ALE	-

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											ATIM2_CH2N GTIM8_CH2 DSMU_DATIN3 XSPI_IO6 FEMC_NE1/FEMC_NCE2 EVENTOUT	
39	E8	F2	F2	65	65	98	PC8	I/O	FT	Y	ATIM2_CH3 SDIO_D0 GTIM2_CH3 USART4_CK DVP_D2 ATIM3_CH3 I2C3_SCL SPI2_MISO/I2S2_AUX_SD USART2_TX FEMC_INT2 FEMC_ALE/FEMC_A17 FEMC_NE2/FEMC_NCE3 EVENTOUT	-
40	D8	E1	E1	66	66	99	PC9	I/O	FT	Y	I2S_CKIN MCO2 ATIM2_CH4 SDIO_D1 I2C3_SDA DVP_D3 GTIM2_CH4 ATIM2_BKIN2 SPI2_MOSI/I2S2_SD USART2_RX FEMC_NOE ATIM2_CH3N GTIM8_CH3 UART5_CTS XSPI_IO0 EVENTOUT	-
41	D7	E2	E2	67	67	100	PA8	I/O	FT	Y	MCO1 USART1_CK ATIM1_CH1 I2C3_SCL I2C2_SDA I2S2_MCK I2C2_SMBA GTIM3_ETR SDIO_D1 DSMU_DATIN6 FEMC_NOE ATIM2_BKIN2 DVP_D3 LPTIM2_OUT EVENTOUT	-
42	C7	E3	E3	68	68	101	PA9	I/O	FT	Y	USART1_TX ATIM1_CH2 I2C3_SMBA DVP_D0 I2C2_SCL I2S3_MCK GTIM8_BKIN GTIM1_CH3 SPI2_SCK/I2S2_CK SDIO_D2 I2C4_SCL I2C1_SCL DSMU_CKIN6 ETH_MII_TX_ER FEMC_NWE EVENTOUT	-
43	C6	D2	D2	69	69	102	PA10	I/O	FT	Y	USART1_RX	PVD_IN

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											ATIM1_CH3 DVP_D1 GTIM10_BKIN I2C2_SMBA SPI2_MISO/I2S2_AUX_SD GTIM1_CH4 ATIM2_BKIN I2C2_SDA SPI5_MOSI I2C4_SDA FEMC_NWE DSMU_DATIN0 SDIO_D0 EVENTOUT	
44	C8	D1	D1	70	70	103	PA11	I/O	FT	Y	USART1_CTS ATIM1_CH4 USB_FS_DM SPI2_MOSI/I2S2_SD ATIM1_CH1N GTIM3_CH1 ATIM1_BKIN2 SPI4_MISO USART4_TX ATIM2_CH3N DSMU_CKIN0 UART6_RX SPI2_NSS/I2S2_WS EVENTOUT	-
45	B8	C1	C1	71	71	104	PA12	I/O	FT	Y	USART1_RTS_DE ATIM1_ETR USB_FS_DP GTIM9_CH1 I2S_CKIN ATIM1_CH2N GTIM3_CH2 SPI4_MOSI USART4_RX SPI2_NSS/I2S2_WS ATIM2_BKIN UART6_TX SPI2_SCK/I2S2_CK EVENTOUT	-
46	A8	C2	C2	72	72	105	PA13	I/O	FT	Y	JTMS-SWDIO GTIM9_CH1N I2C4_SCL I2C1_SCL IR_OUT USART3_CTS GTIM3_CH3 UART6_TX GTIM8_CH3 EVENTOUT	IR-OUT
47	-	-	-	73	-	106	PH2	I/O	FT	Y	USART4_RTS_DE USART1_RX GTIM3_CH4 GTIM9_CH3 DVP_D13 ATIM3_BKIN2 DSMU_CKIN4 XSPI_NSS1 XSPI_IO7 SDRAM_NE1 EVENTOUT	-
-	-	-	-	-	73	-	NC	-	-	-	-	-
-	-	B1	B1	74	74	107	VSS	S	-	-	-	-
48	-	-	-	75	75	108	VDD	S	-	-	-	-

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49	A7	B2	B2	76	76	109	PA14	I/O	FT	Y	JTCK-SWCLK LPTIM1_OUT I2C4_SMBA I2C1_SDA ATIM2_CH2 ATIM1_BKIN USART2_TX UART6_RX GTIM8_CH4 EVENTOUT	-
50	A6	A2	A2	77	77	110	PA15	I/O	FT	Y	JTDI SPI3_NSS/I2S3_WS GTIM1_CH1_ETR SPI1_NSS ATIM2_CH1 I2C1_SCL USART2_RX UART6_RTS_DE ATIM1_BKIN USART1_TX USART2_CTS ATIM2_CH1N ATIM3_ETR FEMC_NBL1 SDRAM_NBL1 EVENTOUT	-
51	B7	D3	D3	78	78	111	PC10	I/O	FT	Y	SPI3_SCK/I2S3_CK UART6_TX SDIO_D2 DVP_D8 ATIM2_CH1N XSPI_NSS1 GTIM9_CH4 DSMU_CKIN5 XSPI_IO1 ETH_MII_TX_D0/ETH_RMII_TX_D0 EVENTOUT	-
52	B6	C3	C3	79	79	112	PC11	I/O	FT	Y	UART6_RX SPI3_MISO/I2S3_AUX_SD SDIO_D3 DVP_D4 ATIM2_CH2N I2C3_SDA XSPI_CLK GTIM10_ETR ATIM3_CH2 DSMU_DATIN5 XSPI_NSS0 EVENTOUT	-
53	C5	B3	B3	80	80	113	PC12	I/O	FT	Y	SDIO_CLK DVP_D9 SPI3_MOSI/I2S3_SD USART3_CK GTIM4_CH2 ATIM2_CH3N I2C2_SDA XSPI_IO0 ATIM2_CH2N ATIM3_CH3 SPI6_SCK GTIM8_CH1 EVENTOUT	-
-	-	-	D5	81	81	114	PD0	I/O	FT	Y	FEMC_D2 ATIM2_CH4N SPI4_MISO SPI3_MOSI UART6_TX	-

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											XSPI_IO1 ATIM3_CH4 SDRAM_D2 DSMU_CKIN6 DSMU_DATIN7 UART5_CTS SPI2_NSS/I2S2_WS I2C1_SCL EVENTOUT	
-	-	-	D6	82	82	115	PD1	I/O	FT	Y	FEMC_D3 ATIM2_CH4 ATIM2_BKIN2 SPI2_NSS/I2S2_WS UART6_RX XSPI_IO2 I2C1_SDA SDRAM_D3 DSMU_DATIN6 DSMU_CKIN7 SPI2_SCK/I2S2_CK USART9_CK EVENTOUT	-
54	B5	A3	A3	83	83	116	PD2	I/O	FT	Y	GTIM2_ETR SDIO_CMD DVP_D11 ATIM2_BKIN SPI3_NSS/I2S3_WS XSPI_IO3 ATIM2_CH3N SPI2_MOSI/I2S2_SD ATIM1_CH4 ATIM2_CH4N ATIM3_CH4 GTIM5_CH2 GTIM8_BKIN EVENTOUT	WKUP5
-	-	-	-	84	84	117	PD3	I/O	FT	Y	FEMC_CLK USART2_CTS GTIM1_CH1_ETR XSPI_NSS0 SPI2_SCK/I2S2_CK DVP_D5 DSMU_CKOUT DSMU_DATIN0 SPI2_MISO/I2S2_AUX_SD EVENTOUT	WKUP6
-	-	-	E5	85	85	118	PD4	I/O	FT	Y	FEMC_NOE USART2_RTS_DE GTIM1_CH2 XSPI_IO4 DSMU_CKIN0 SPI2_MOSI/I2S2_SD EVENTOUT	-
-	-	-	D4	86	86	119	PD5	I/O	FT	Y	FEMC_NWE USART2_TX XSPI_IO5 GTIM6_CH1 ATIM1_CH4N EVENTOUT	-
-	-	-	-	-	-	120	VSS	S	-	-	-	-
-	-	B6	B6	-	-	121	VDDIO(6)	S	-	-	-	-
-	-	-	-	87	87	122	PD6	I/O	FT	Y	FEMC_NWAIT USART2_RX GTIM1_CH4 XSPI_IO6 SPI3_MOSI/I2S3_SD	-

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											DVP_D0 GTIM9_ETR DSMU_CKIN4 DSMU_DATIN1 DVP_D10 I2C1_SCL EVENTOUT	
-	-	-	-	88	88	123	PD7	I/O	FT	Y	USART2_CK FEMC_NE1/FEMC_NCE2 GTIM1_CH3 XSPI_IO7 DSMU_DATIN4 DSMU_CKIN1 SPI1_MOSI I2C1_SDA SPI3_NSS/I2S3_WS EVENTOUT	-
-	-	A4	A4	-	-	124	PG9	I/O	FT	Y	USART4_RX FEMC_NE2/FEMC_NCE3 SPI3_SCK/I2S3_CK USART1_TX GTIM8_CH1N DVP_VSYNC SPI2_MOSI/I2S2_SD GTIM6_CH2 SPI2_MISO/I2S2_AUX_SD SPI1_MISO XSPI_IO6 XSPI_IO5 I2C1_SMBA I2C4_SMBA SDRAM_NBL1 EVENTOUT	-
-	-	B4	B4	-	-	125	PG10	I/O	FT	Y	FEMC_NE3 XSPI_IO2 DVP_D2 GTIM7_CH1 SPI1_NSS SPI3_MISO/I2S3_AUX_SD USART1_RX LPTIM1_IN1 GTIM8_CH1 I2C4_SCL SDRAM_CLK ATIM1_CH4N EVENTOUT	-
-	-	C4	C4	-	-	126	PG11	I/O	FT	Y	ETH_MII_TX_EN/ETH_RMII_TX_EN XSPI_IO3 SPI4_SCK DVP_D3 GTIM7_CH2 SPI1_SCK SPI3_MOSI USART1_CTS USART9_RX LPTIM1_IN2 GTIM8_CH2 I2C4_SDA SDRAM_CKE0 EVENTOUT	-
-	-	C5	C5	-	-	127	PG12	I/O	FT	Y	FEMC_NE4 USART4_RTS_DE XSPI_IO1 SPI4_MISO GTIM7_CH3 SPI6_MISO ETH_MII_TX_D1/ETH_RMII_TX_D1	-

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											DVP_D11 SPI3_NSS/I2S3_WS USART1_RTS_DE USART9_TX LPTIM1_ETR LPTIM1_IN1 SDRAM_A11 EVENTOUT	
-	-	B5	B5	-	-	128	PG13	I/O	FT	Y	FEMC_A24 USART4_CTS ETH_MII_TX_D0/ETH_RMII_TX_D0 XSPI_CLK SPI4_MOSI GTIM7_CH4 USART9_CTS SPI6_SCK I2C1_SDA USART1_CK LPTIM1_IN2 SDRAM_A9 EVENTOUT	-
-	-	A5	A5	-	-	129	PG14	I/O	FT	Y	FEMC_A25 USART4_TX ETH_MII_TX_D1/ETH_RMII_TX_D1 XSPI_IO0 SPI4_NSS SPI2_MISO/I2S2_AUX_SD I2C1_SCL GTIM6_CH3 ATIM2_CH4 USART9_RTS_DE SPI6_MOSI XSPI_IO7 LPTIM1_ETR LPTIM1_IN1 SDRAM_A8 EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	-	131	VDD	S	-	-	-	-
-	-	-	-	-	-	132	PG15	I/O	FT	Y	USART4_CTS DVP_D13 GTIM6_CH4 I2C1_SDA SPI6_NSS ATIM2_CH4N USART1_RX SDRAM_NCAS USART9_CK XSPI_NSS1 I2C1_SMBA I2C4_SDA LPTIM1_OUT SDRAM_A6 EVENTOUT	-
55	A5	A6	A6	89	89	133	PB3	I/O	FT	Y	JTDO SPI3_SCK/I2S3_CK GTIM1_CH2 SPI1_SCK GTIM3_ETR ATIM2_CH1N USART2_TX GTIM2_ETR USART1_RX I2C2_SDA USART2_RTS_DE ATIM2_BKIN UART10_CTS	-

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											EVENTOUT	
56	A4	C6	C6	90	90	134	PB4	I/O	FT	Y	NJTRST SPI3_MISO/I2S3_AUX_SD GTIM2_CH1 SPI1_MISO GTIM9_CH1_ETR ATIM2_CH2N USART2_RX GTIM10_BKIN I2C3_SDA SDIO_D0 ATIM2_ETR LPTIM2_IN1 USART2_TX XSPI_CLK EVENTOUT	-
57	C4	C7	C7	91	91	135	PB5	I/O	FT	Y	I2C1_SMBA ETH_PPS_OUT GTIM2_CH2 SPI1_MOSI SPI3_MOSI/I2S3_SD DVP_D10 GTIM9_BKIN ATIM2_CH3N USART2_CK I2C3_SDA GTIM10_CH1 LPTIM1_IN1 UART5_CTS USART2_RX SDRAM_CKE1 EVENTOUT	-
58	D3	B7	B7	92	92	136	PB6	I/O	FT	Y	I2C1_SCL GTIM3_CH1 DVP_D5 USART1_TX GTIM9_CH1N ATIM2_CH1 ATIM2_ETR ATIM2_BKIN2 LPTIM1_ETR ETH_PPS_OUT FEMC_NE2/FEMC_NCE3 ATIM3_CH1N SDRAM_NE1 DSMU_DATIN5 I2C4_SCL EVENTOUT	-
59	C3	A7	A7	93	93	137	PB7	I/O	FT	Y	I2C1_SDA FEMC_NADV DVP_VSYNC USART1_RX GTIM3_CH2 GTIM10_CH1N ATIM2_BKIN GTIM2_CH4 I2C4_SDA LPTIM1_IN2 ETH_MII_TX_D3 UART6_CTS ATIM3_CH2N DSMU_CKIN5 EVENTOUT	PVD_IN
60	B4	D7	D7	94	94	138	PH4-BOOT0	I/O	FT	Y	GTIM4_CH1 GTIM10_CH1N USART1_TX SDRAM_NE1	-

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											XSPI_IO4 EVENTOUT	
61	B3	E7	E7	95	95	139	PB8	I/O	FT	Y	GTIM3_CH3 SDIO_D4 GTIM6_CH1 DVP_D6 ETH_MII_TX_D3 I2C1_SCL GTIM9_CH1 ATIM2_CH2 ATIM1_BKIN SPI5_MOSI GTIM9_CH4 ATIM3_CH3N DSMU_CKIN7 UART6_RX EVENTOUT	-
62	A3	E8	E8	96	96	140	PB9	I/O	FT	Y	SPI2_NSS/I2S2_WS GTIM3_CH4 GTIM7_CH1 SDIO_D5 DVP_D7 I2C1_SDA GTIM10_CH1 ATIM2_CH3 ATIM1_CH3N FEMC_NE1/FEMC_NCE2 ATIM3_CH4N DSMU_DATIN7 UART6_TX EVENTOUT	IR-OUT
-	-	-	-	97	97	141	PE0	I/O	FT	Y	GTIM3_ETR FEMC_NBL0 DVP_D2 ATIM3_ETR ATIM3_CH4N GTIM9_CH1 USART1_TX SDRAM_NBL0 UART7_RX LPTIM1_ETR LPTIM2_ETR LPTIM2_IN1 EVENTOUT	-
-	-	-	-	98	98	142	PE1	I/O	FT	Y	FEMC_NBL1 DVP_D3 GTIM10_CH1 ATIM3_CH4 USART1_RX SDRAM_NBL1 UART7_TX EVENTOUT	-
-	-	-	-	-	-	143	PH5	I/O	FT	Y	DVP_D11 SDRAM_D8 XSPI_IO6 I2C2_SMBA I2C3_SMBA ATIM2_CH4 GTIM10_CH4 EVENTOUT	-
63	D6	A8	A8	99	99	-	VSS	S	-	-	-	-
64	E6	A9	A9	100	100	144	VDD	S	-	-	-	-

Notes:

1. *I = input, O = output, S = power supply.*
2. *FT: 5V toleran; FTa: 5V tolerant, support analog peripherals; TTa: 3.3V tolerant, support analog peripherals.*

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3. *Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.*
4. *The RTS_DE, TX, and RX signals of USART3, UART5 and UART8 can be mapped to any IO.*
5. *The TX, and RX signals of FDCAN1, FDCAN2 and FDCAN3 can be mapped to any IO.*
6. *The BGA81 and BGA72 packages (PG9 to PG14) support operation via the VDDIO input, whilst the LQFP144 package (PD6 to PD7, PG9 to PG15) supports operation via the VDDIO input, accommodating 1.8 to 3.6V input.*

The ADC12_INx mentioned in the pin name annotations in the table indicates that this pin can be either ADC1_INx or ADC2_INx. For example, ADC12_IN9 means that this pin can be configured as ADC1_IN9 or ADC2_IN9.

Similarly, the ADC34_INx mentioned in the pin name annotations in the table indicates that this pin can be either ADC3_INx or ADC4_INx.

In the pin PA0 of the table, the multiplexing function GTIM1_CH1_ETR means that this function can be configured as GTIM1_TI1 or GTIM1_ETR. Similarly, for PA15, the remapping multiplexing function name GTIM1_CH1_ETR has the same meaning.

For the FT ports in the table, it is necessary to ensure that the voltage difference between the IO voltage and the power supply voltage is less than 3.6V.

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4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and Maximum Values

The minimum and maximum values in the Beta version are based on design simulations.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3∑).

4.1.2 Typical Values

Unless otherwise specified, typical data are based on T_A = 25 ℃ and V_{DD} = 3.3V (for the 1.8V ≤ V_{DD} ≤ 3.6V voltage range). These data are for design guidance only and not tested.

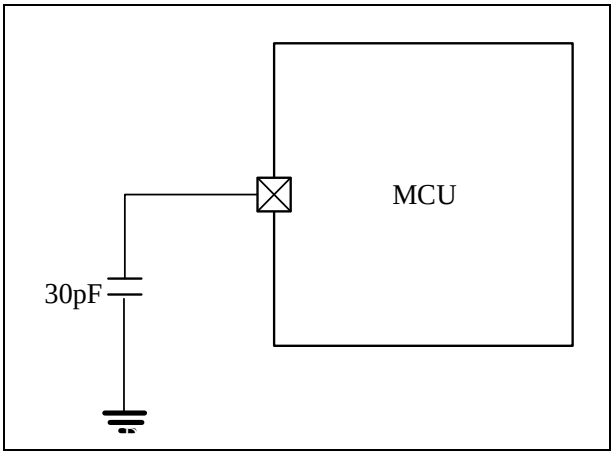
4.1.3 Typical Curves

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading Capacitor

The load conditions for measuring pin parameters are shown Figure 4-1:

Figure 4-1 Load Conditions Of Pins



4.1.5 Pin Input Voltage

The measurement of the input voltage on the pin is shown Figure 4-2:

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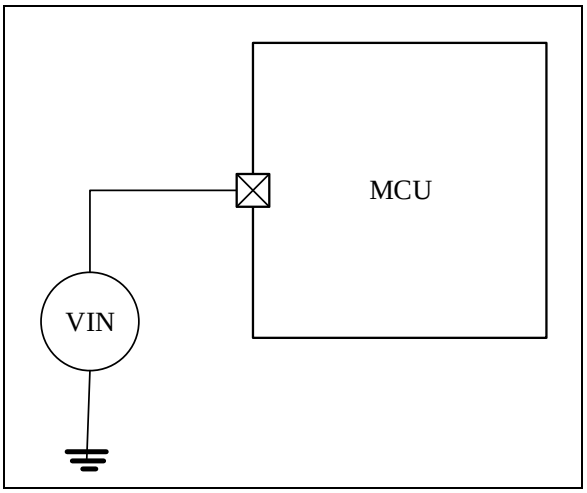
Figure 4-2 Pin Input Voltage



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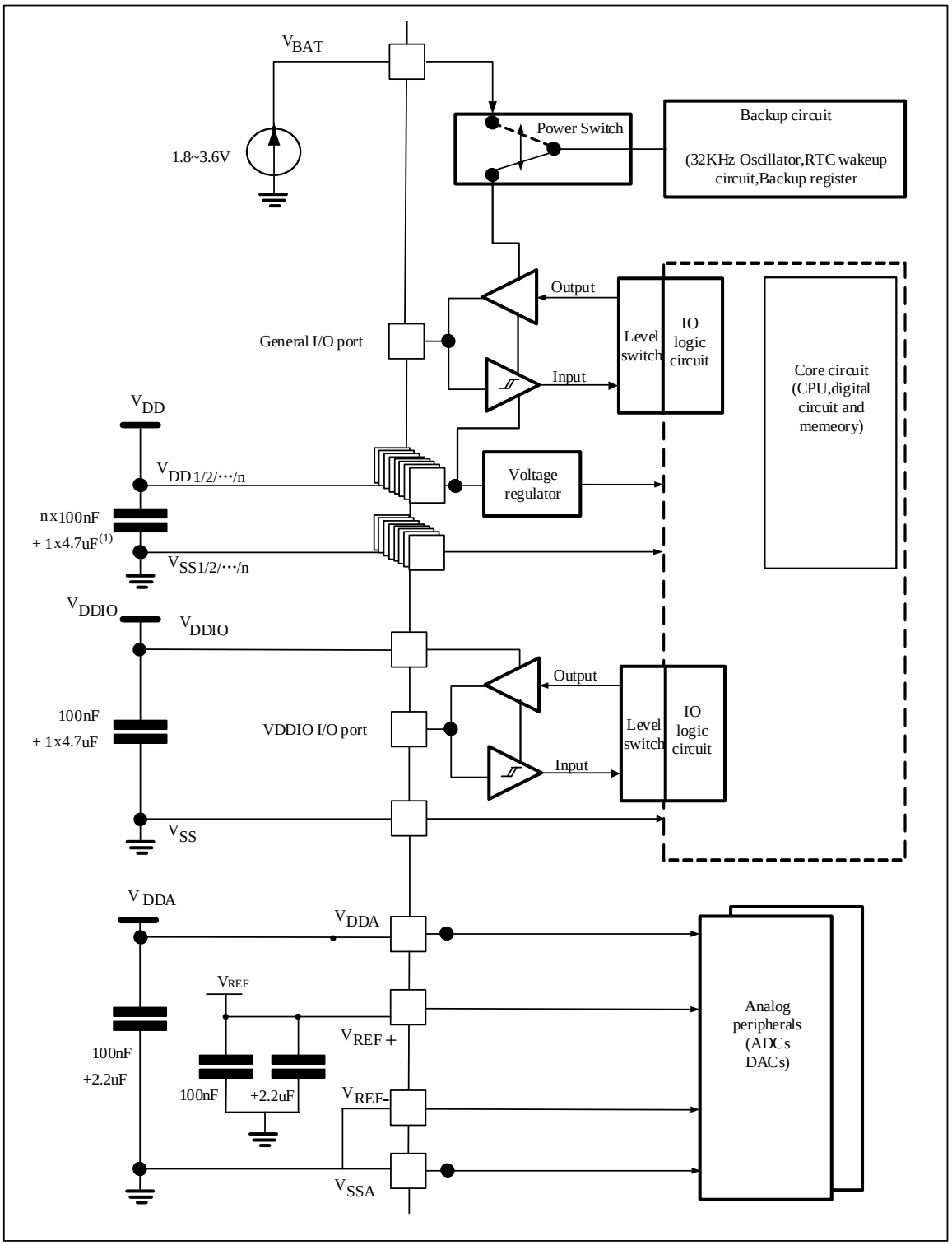
4.1.6 Power Supply Scheme

Figure 4-3 Power Supply Scheme



Note:

(1) The 4.7μF capacitor shown in the diagram must be connected to the designated main VDD pin: Pin 64 for LQFP64, Pin 100 for LQFP100, Pin 144 for LQFP144, and Pin A9 for BGA81/BGA72.

(2) For BGA81 and BGA72 packages, the pins supporting independent VDDIO power supply are PG9 to PG14, For LQFP144 packages, the pins supporting independent VDDIO power supply are PD6~PD7, PG9~PG15.

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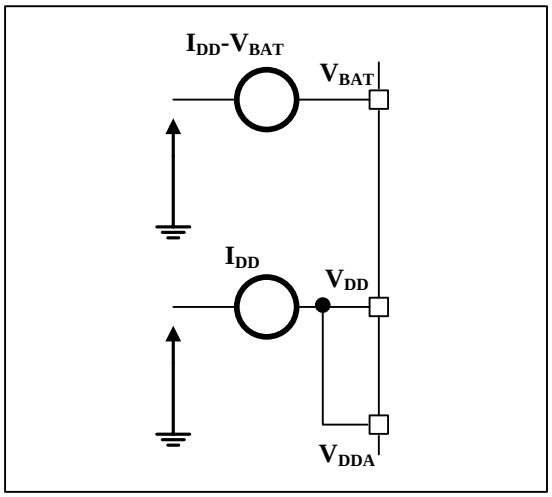
4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins(3)	V_{SS} - 0.3	5.5	
	Input voltage on other pins(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		-

Notes:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

(2) V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

(3) When a 5V tolerant pin inputs 5.5V, VDD cannot be lower than 2.25V.

Table 4-2 Current Characteristics

Symbol	Describe	Max (1)	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1) (4)	400	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1) (4)	400	
I_{IO}	Output current sunk by I/O and control pins	12	
	Output current source by I/O and control pins	-12	
$I_{INJ(PIN)}$(2)(3)	Injection current on NRST pin	-5/0	
	Injection current on other pins	+/-5	

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Notes:

(1) All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

(2) When $V_{IN}>V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Refer to Table 4-1 for voltage characteristics.

(3) Reverse injection current can interfere with the analog performance of the device. See section 4.3.2526.

(4) When the maximum current occurs, the maximum allowable voltage drop of VDD is 0.1VDD.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	- 65 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	240	MHz
f_{PCLK}	Internal APB1/2 clock frequency	-	0	180	
V_{DDA}	Analog operating of working voltage	Must be the same potential as V_{DD}(1)	1.8	3.6	V
V_{BAT}	Backup domain supply voltage	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃
T_J	Junction temperature range	7 suffix version	-40	125	℃

(1) It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

4.3.2 Operating Conditions at Power-on and Power-down

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating Conditions At Power-On And Power-Down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	20	∞	μs/V
	V_{DD} fall time rate		80	∞	

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-6 Features Of Embedded Reset And Power Control Modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (MSB of PWR_CTRL	PRS[2:0]=000 (rising edge)	-	2.18	-	V
		PRS[2:0]=000 (falling edge)	-	2.08	-	V
		PRS[2:0]=001 (rising edge)	-	2.28	-	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	is 0)	PRS[2:0]=001 (falling edge)	-	2.18	-	V
		PRS[2:0]=010 (rising edge)	-	2.38	-	V
		PRS[2:0]=010 (falling edge)	-	2.28	-	V
		PRS[2:0]=011 (rising edge)	-	2.48	-	V
		PRS[2:0]=011 (falling edge)	-	2.38	-	V
		PRS[2:0]=100 (rising edge)	-	2.58	-	V
		PRS[2:0]=100 (falling edge)	-	2.48	-	V
		PRS[2:0]=101 (rising edge)	-	2.68	-	V
		PRS[2:0]=101 (falling edge)	-	2.58	-	V
		PRS[2:0]=110 (rising edge)	-	2.78	-	V
		PRS[2:0]=110 (falling edge)	-	2.68	-	V
		PRS[2:0]=111 (rising edge)	-	2.88	-	V
		PRS[2:0]=111 (falling edge)	-	2.78	-	V
	Programmable voltage detector level selection (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	-	1.78	-	V
		PRS[2:0]=000 (falling edge)	-	1.68	-	V
		PRS[2:0]=001 (rising edge)	-	1.88	-	V
		PRS[2:0]=001 (falling edge)	-	1.78	-	V
		PRS[2:0]=010 (rising edge)	-	1.98	-	V
		PRS[2:0]=010 (falling edge)	-	1.88	-	V
		PRS[2:0]=011 (rising edge)	-	2.08	-	V
		PRS[2:0]=011 (falling edge)	-	1.98	-	V
		PRS[2:0]=100 (rising edge)	-	3.28	-	V
		PRS[2:0]=100 (falling edge)	-	3.18	-	V
		PRS[2:0]=101 (rising edge)	-	3.38	-	V
		PRS[2:0]=101 (falling edge)	-	3.28	-	V
		PRS[2:0]=110 (rising edge)	-	3.48	-	V
		PRS[2:0]=110 (falling edge)	-	3.38	-	V
		PRS[2:0]=111 (rising edge)	-	3.58	-	V
		PRS[2:0]=111 (falling edge)	-	3.48	-	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
V_{POR}	VDD power on/power down reset threshold	-	-	1.66/1.58	-	V
V_{BOR}	BOR power on/off reset threshold	BOR_LVL[2:0]=000 (rising edge)	-	1.66	-	V
		BOR_LVL[2:0]=000 (falling edge)	-	1.62	-	V
		BOR_LVL[2:0]=001 (rising edge)	-	2.1	-	V
		BOR_LVL[2:0]=001 (falling edge)	-	2	-	V
		BOR_LVL[2:0]=010 (rising edge)	-	2.3	-	V
		BOR_LVL[2:0]=010 (falling edge)	-	2.2	-	V
		BOR_LVL[2:0]=011 (rising edge)	-	2.6	-	V
		BOR_LVL[2:0]=011 (falling edge)	-	2.5	-	V
		BOR_LVL[2:0]=100 (rising edge)	-	2.9	-	V
		BOR_LVL[2:0]=100 (falling edge)	-	2.8	-	V
$T_{RSTTEMPO}$(1)	Reset duration	-	-	0.8	4	ms

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(1) Guaranteed by design, not tested in production.

4.3.4 Embedded Reference Voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in **Table 4-4**.

Table 4-7 Internal Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃< T_A< +105℃	1.164	1.2	1.236	V
$T_{S\_vrefint}$(1)	The sampling time of the ADC when reading the internal reference voltage	-	-	5.1	17.1(2)	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	VDD = 3.3V -40℃< T_A< +105℃	-14	-	14	mV

Notes:

(1) The shortest sampling time is obtained through multiple loops in the application.

(2) Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, toggle rate of I/O pins, program location in memory, and executed code.

The measurement method of current consumption is described in **Figure 4-4**.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum Current Consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting period from 0 to 48 MHz, 1 waiting period from 48 to 96 MHz, 2 waiting periods from 96 to 144 MHz, 3 waiting periods from 144 to 192 MHz, 4 waiting periods from 192 to 240 MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$.
- VDD is 3.63V, ambient temperature is 105℃

The parameters given in Table 4-8 and Table 4-9 are based on tests at the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Maximum Current Consumption In Operating Mode Where Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)				Unit
				T_A = -40℃	T_A = 25℃	T_A = 85℃	T_A = 105℃	
I_{DD}	Supply current in operation mode	External clock(2), enable all peripherals	240MHz	87.4	90.6	104.3	113.7	mA
			180MHz	66.4	69.3	82.3	91.6	
			120MHz	49.2	51.8	63.9	72.8	
			60MHz	27.7	30	41.1	50	

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		External clock(2), disable all peripherals	240MHz	27.3	29.7	41.1	50.2	
			180MHz	21.7	24	35.1	44	
			120MHz	16.9	18.2	29.5	38.1	
			60MHz	10.1	12.1	22.6	31.3	

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) Enable PLL when f_{HCLK} > 8MHz.

Table 4-9 Maximum Current Consumption In Sleep Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ (1)				Unit
				T_A = -40℃	T_A = 25℃	T_A = 85℃	T_A = 105℃	
I_{DD}	Supply current in sleep mode	External clock(2), enable all peripherals	240MHz	77.4	80.5	93.6	103.2	mA
			180MHz	60.2	63.1	75.5	84.8	
			120MHz	45	47.6	59.3	68.3	
			60MHz	25.6	27.8	38.7	47.6	
		External clock(2), disable all peripherals	240MHz	18.9	21.2	31.9	40.8	
			180MHz	15.2	17.4	28	36.8	
			120MHz	12.3	13.4	24.4	31	
			60MHz	7.8	9.8	20.1	28.7	

Notes:

(1) Based on comprehensive evaluation result, not tested in production.

(2) Enable PLL when f_{HCLK} > 8MHz.

4.3.5.2 Current consumption in Low-Power Mode

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disable unless otherwise noted.

Table 4-10 Typical Current Consumption In Low Power Mode

Symbol	Parameter	Conditions	Typ (1)				Unit
			T_A = -40℃	T_A =25℃	T_A =85℃	T_A =105℃	
I_{DD}	Supply current in STOP0 mode	Regulator in run mode, LSE on, RTC on, IWDG off, Backup SRAM hold	1.5	2.9	12.3	20.7	mA
		Regulator in LP mode, LSE on, RTC on, IWDG off, Backup SRAM hold	1	1.7	7.3	13.9	
I_{DD}	Supply current in STANDBY mode	LSE on, RTC on, IWDG off, BackupSRAM hold	1.98	3.75	20.8	39	uA
		LSE on, RTC off, IWDG off, BackupSRAM hold	1.98	3.75	20.49	39.05	
		LSE on, RTC off, IWDG off, BackupSRAM not holding	1.98	3.76	20.13	38.01	

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I_{DD_VBAT}	Supply current in VBAT mode	LSE on, RTC on, IWDG off, Backup SRAM hold	1.13	2.71	16.8	30.82	uA

(1) Based on comprehensive evaluation result, not tested in production.

4.3.5.3 Peripheral current consumption

Table 4-11 Peripheral current consumption

Bus	Peripheral	Typ	Unit
AHB	ETH	13.01	μA/MHz
	DMA1	4.37	
	DMA2	4.37	
	FEMC	6.01	
	XSPI	11.67	
	SDRAM	4.84	
	USBHS	13.96	
AHB1	BKP SRAM	0.41	μA/MHz
	CORDIC	0.51	
	CRC	0.2	
	SDIO	3.59	
AHB2	ATIM1	9.05	μA/MHz
	ATIM2	9.12	
	ATIM3	8.55	
AHB3	GPIOA	14.01	μA/MHz
	GPIOB	14.2	
	GPIOC	14.34	
	GPIOD	14.28	
	GPIOE	14.12	
	GPIOF	14.66	
	GPIOG	14.31	
	GPIOH	13.78	
	ADC1	10.04	
	ADC2	8.16	
	ADC3	7.81	
	SAC	1.83	
APB1	DVP	1.33	μA/MHz
	DAC1/2	1.71	
	I2C1	2.72	
	I2C2	2.72	
	I2C3	2.72	
	I2C4	2.72	

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	LPTIM1	2.27	
	LPTIM2	2.27	
	UART5	2.51	
	UART8	2.51	
	UART10	2.51	
	GTIM1	7.03	
	GTIM2	4.86	
	GTIM3	4.75	
	GTIM4	6.79	
	GTIM5	5.47	
	GTIM6	4.49	
	GTIM7	4.68	
	CANFD1	11.35	
	CANFD2	12.37	
	CANFD3	3.84	
	UCDR	22.17	
	USBFS	20.21	
	BTIM1	0.22	
	BTIM2	0.22	
	SPI2/I2S2	2.69	
	SPI3/I2S3	2.69	
	USART2	2.82	
	USART3	2.82	
	USART9	2.82	
	RTC	3.52	
	WWDG	0.28	
	DSMU	47.53	
	PWR	1.94	
APB2	SPI1	1.46	µA/MHz
	SPI4	1.32	
	SPI5	1.82	
	SPI6	1.33	
	USART1	0.46	
	USART4	2.38	
	UART6	2.38	
	UART7	2.89	
	GTIM8	2.51	
	GTIM9	13.61	
	GTIM10	13.34	

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4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Source (HSE)

The characteristic parameters given in the following table are measured using a high-speed external clock source (Bypass mode), and the ambient temperature and supply voltage meet the conditions specified in **Table 4-4.**

Table 4-12 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	1	8	50	MHz
V_{HSEH}	OSC_IN Input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HSE)}$	Time when OSC_IN is high or low(1)		16	-	-	ns
$t_{r(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$t_{f(HSE)}$						
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-1	-	+1	μA

(1) Guaranteed by design, not tested in production.

4.3.6.2 Low-Speed External Clock Source (LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source (Bypass mode), and the ambient temperature and supply voltage meet the conditions specified in **Table 4-4.**

Table 4-13 Low-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency(1)	-	8.8	32.768	1000	KHz
V_{LSEH}	OSC32_IN Input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN Input pin low level voltage		V_{SS}	-	0.3VDD	mV
$t_{w(LSE)}$	OSC32_IN High or low time(1)		450	-	-	ns
$t_{w(LSE)}$						
$t_{r(LSE)}$	OSC32_IN Rise or fall time(1)		-	-	50	
$t_{f(LSE)}$						
$DuCy_{(LSE)}$	Duty ratio		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

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Figure 4-5 AC Timing Diagram Of An External High Speed Clock Source

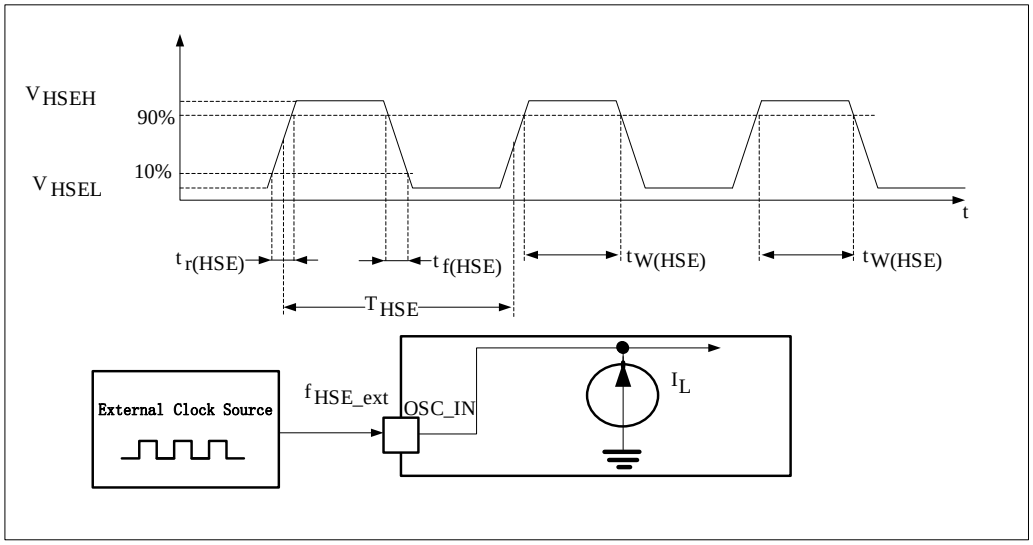
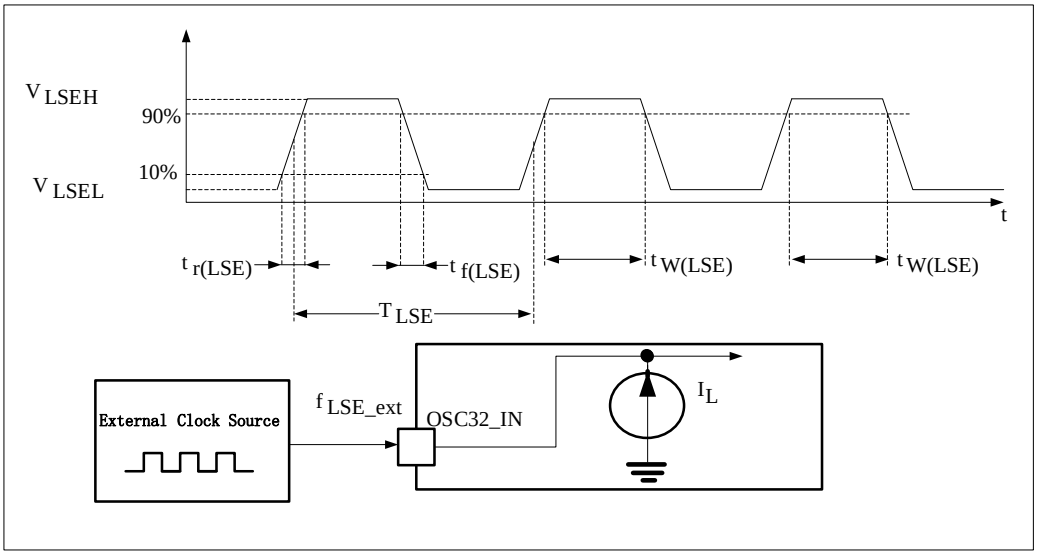


Figure 4-6 AC Timing Diagram Of An External Low Speed Clock Source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Table 4-14 HSE 4~32MHz Oscillator Characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	380	-	kΩ
i_2	HSE drive current	V_{DD} = 3.3V, V_{IN} = V_{SS} 30 pf load	-	1.8	-	mA
g_m	Transconductance of the oscillator	Start	-	10	-	mA/V
$t_{SU(HSE)}$(3)	Startup time (8M crystal)	V_{DD} is stabilized	-	10	-	mA/V

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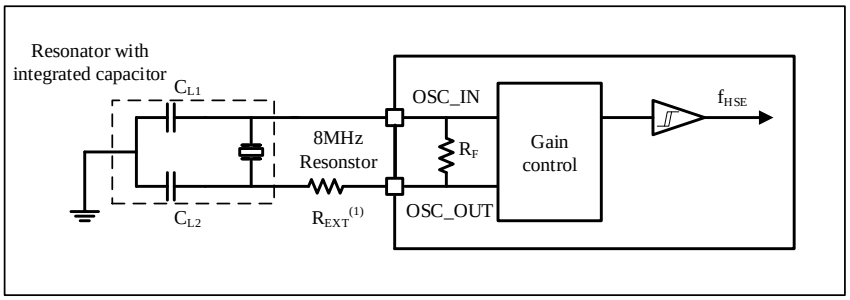
Notes:

(1) The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2) Guaranteed by characterization results, not tested in production.

(3) $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-7 Typical Application Using 8 MHz Crystal



(1) The R_{EXT} value depends on the properties of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric containers, and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}.

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example: If a resonator with load capacitance C_L = 6pF is selected and C_{stray} = 2pF, then $C_{L1} = C_{L2}$ = 8pF.

Table 4-15 LSE Oscillator Characteristics (F_{LSE} = 32.768KHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
I2	LSE drive current	Low drive capability	-	300	-	nA
		Medium drive capability	-	750	-	
		High drive capability	-	1000	-	
g_m	Maximum transconductance	Low drive capability	-	9	-	μA/V
		Medium drive capability	-	12	-	
		High drive capability	-	27	-	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stabilized	-	2	-	s

Notes:

(1) Guaranteed by design, not tested in production.

(2) $t_{SU(LSE)}$ is the starting time, which is the period from the LSE enabled by the software to the stable 32.768 khz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

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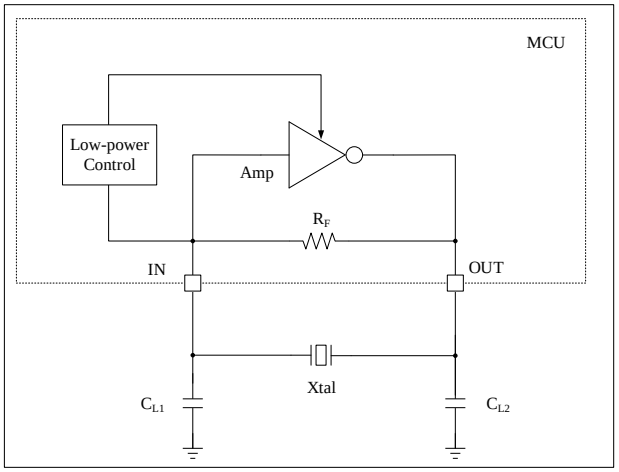
Figure 4-8 Typical Application Of 32.768KHz Crystal



4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

4.3.7.1 High Speed Internal (HSI) RC Oscillator

Table 4-16 HSI Oscillator Characteristics (1) (2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	V_{DD}=3.3V, T_A = 25℃, after calibration	7.96(3)	8	8.04(3)	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	V_{DD}=3.3V, T_A = -40~105℃	-1.5	-	2	%
		V_{DD}=3.3V, T_A = -10~85℃	-0.8	-	1.5	%
		V_{DD}=3.3V, T_A = 0~70℃	-0.5	-	1.3	%
$t_{SU(HSI)}$	HSI oscillator start time	-	-	-	6	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	120	μA

Notes:

(1) V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.

(2) Guaranteed by design, not tested in production.

(3) Production calibration accuracy, excluding soldering effects. Soldering introduces a frequency deviation range of approximately ±1%.

(4) Frequency deviation includes the effects of soldering, data is from sample testing, not tested in production.

4.3.7.2 Low Speed Internal (LSI) RC Oscillator

Table 4-17 LSI Oscillator Characteristics (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25℃ calibration, V_{DD} = 3.3V	-	32	-	KHz
		V_{DD} = 1.8 V to 3.6 V, T_A = - 40 ~ 105 ℃	28.8	32	35.2	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time	-	-	60	84	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.6	-	μA

Notes:

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(1) V_{DD} = 3.3V, T_A = -40~105℃ unless otherwise specified.

(2) Guaranteed by characterization results, not tested in production.

4.3.8 Wake Up Time from Low Power Mode

The wake-up time listed in **Table 4-18** is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP0 or STANDBY mode: clock source is RC oscillator
- SLEEP mode: The clock source is the clock used to enter SLEEP mode

All times were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-18 Wake Time In Low Power Mode

Symbol	Parameter	Typ(1)	Unit
$t_{WUSLEEP}$	Wake up from SLEEP mode	6	Cycles
$t_{WUSTOP0}$	Wake up from STOP0 mode (regulator in run mode)	20	μs
	Wake up from STOP0 mode (regulator in low power mode)	22	μs
$t_{WUSTDBY}$	Wake up from STANDBY mode	100	μs

(1) The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.

4.3.9 PLL Characteristics

The parameters listed in **Table 4-19** are measured when the ambient temperature and power supply voltage meet the conditions in **Table 4-4**

Table 4-19 PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
f_{PLL_IN}	PLL PFD input clock(2)	4	8	50	MHz
	PLL Input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL output clock(2)	32	-	240	MHz
t_{LOCK}	PLL Ready indicates signal output time(3)	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @240MHz	-	5	-	ps
I_{PLL}	Operating Current of PLL @240MHz VCO frequency.	-	-	1500	uA

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) The correct configuration coefficients need to be used so that the f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

4.3.10 FLASH Memory Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105℃.

Table 4-20 Flash Memory Characteristics

Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
tprog	64-bit programming time	T_A = - 40 ~ 105 ℃, double word mode	-	40	-	μs
		T_A = - 40 ~ 105 ℃, buffer program mode	-	19	-	
t_{ERASE}	Page (16K byte) erase time, single-bank mode	T_A = -40~105℃	-	24	40	ms

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Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
	Page (8K byte) erase time, dual-bank mode	T_A = -40~105℃	-	12	20	ms
t_{ME}	Mass erase time, single-bank mode	T_A = -40~105℃	-	28	40	ms
	Mass erase time (bank1 + bank2), dual-bank mode	TA = -40~105℃	-	28	40	ms
I_{DD}	The power supply current	Read mode, f_{HCLK} = 240 MHz, 4 waiting cycles, V_{DD} = 3.3V	-	4.2	5.45	mA
		Write mode, f_{HCLK} = 240 MHz, V_{DD} = 3.3V	-	6.5	-	mA
		Erase mode, f_{HCLK} = 240 MHz, V_{DD} = 3.3V	-	4.5	-	mA
		Power-down/stop mode, V_{DD} = 3.3~3.6V	-	0.05	4.65	μA
Vprog	Programming voltage	-	1.8	3	3.6	V

Note:

(1) Guaranteed by design, not tested in production.

Table 4-21 Flash Endurance And Data Retention Life

Symbol	Parameter	Condition	Min (1)	Unit
N_{END}	Endurance (note: erasure times)	T_A = -40~105 ℃, Flash size is 512 KB	10	Kcycle
t_{RET}	Data retention period	10 kcycle(2) at T_A = 85 ℃	20	Years
		10 kcycle(2) at T_A = 105 ℃	15	
		10 kcycle(2) at T_A = 125 ℃	10	

(1) Based on comprehensive evaluation, not tested in production.

4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD， ES， LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-22 Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Max (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$(2)	Electrostatic discharge voltage (charging device model)	T_A = +25 ℃, In accordance with ESDA/JEDEC JS-002-2018	C3	1000	

(1) Based on comprehensive evaluation, not tested in production.

(2) LQFP144 VBAT pin voltage maximum 500V

Electromagnetic susceptibility (EMS)

Table 4-23 EMS Features

Symbol	Parameter	Condition	Level

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V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD = 3.3V, LQFP144,TA = 25℃, HCLK = 240MHz, conforms to IEC 61000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	VDD = 3.3V, LQFP144,TA = 25℃, HCLK = 240MHz, conforms to IEC 61000-4-4	4A
	Fast transient voltage burst and capacitively coupled clamping limits to be applied on I/O pins to induce a functional disturbance	VDD = 3.3V, LQFP144,TA = 25℃, HCLK = 240MHz, conforms to IEC 61000-4-4	4A

Static latch-up (LU)

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78A IC latch standard.

Table 4-24 Static Latch-Up

Symbol	Parameter	Condition	Type	Min
LU(1)	Static lock-up class	T_A= +125 ℃, in accordance with JESD 78E	II class A	±100mA, 1.5*VDDMAX

(1) Pins PA4 and PA5 meet I class A standards, passing tests at ±200mA at 25 ℃ and ±80mA at 85 ℃.

4.3.12 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in **Table 4-4**. All I/O ports are CMOS and TTL compatible.

Table 4-25 I/O Static Characteristics

Symbol	Parameter	Condition	Min (1)	Typ (1)	Max (1)	Unit
V_{IL}	Input low level voltage	V_{DD}=3.3V	Vss	-	0.8	V
		V_{DD}=2.5V	Vss	-	0.7	
		V_{DD}=1.8V	Vss	-	0.3*V_{DD}	
V_{IH}	Input high level voltage	V_{DD}=3.3V	2	-	V_{DD}	
		V_{DD}=2.5V	1.7	-	V_{DD}	
		V_{DD}=1.8V	0.7*V_{DD}	-	V_{DD}	
Vhys	Schmidt trigger voltage hysteresis (1)	V_{DD}=3.3V	200	-	-	mV
		V_{DD}=2.5V	200	-	-	
		V_{DD}=1.8V	0.1*V_{DD}(2)	-	-	
I_{lkg}	Input leakage current(3)	V_{DD}=Maximum	-1	-	1	μA
		V_{PAD}=0 or V_{PAD}=V_{DD}(5)				
R_{PU}	Weak pull-up equivalent resistor (4)	VDD=3.3v,V_{IN}= Vss	80	-	220	kΩ
		VDD=1.8~3.3v,V_{IN}= Vss	60	-	500	kΩ
R_{PD}	Weak pull-down equivalent resistor (4)	VDD=3.3v,V_{IN}= VDD	80	-	220	kΩ
		VDD=1.8~3.3v,VIN= VDD	60	-	500	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Notes:

(1) The hysteresis voltage of Schmitt trigger switching level. Based on comprehensive evaluation, not tested in production.

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(2) At least 100mV.

(3) If there is reverse current injection from adjacent pins, the leakage current may be higher than the maximum value.

(4) Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

(5) V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

Output driving current

GPIO (universal input/output port) can absorb or output up to +/-12mA current. In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in Section 4.2.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating value I_{VDD} (Table 4-2)
- The sum of the currents sourced by all the I/Os on Vss, plus the maximum consumption of the MCU sourced on Vss, cannot exceed the absolute maximum rating value I_{VSS} (Table 4-2)

Output voltage

Unless otherwise specified, the parameters listed in **Table 4-27** were measured using ambient temperature and V_{DD} supply voltage in accordance with **Table 4-4**. All I/O ports are CMOS and TTL compatible

Table 4-26 IO Output Drive Capability Characteristics(1)

Drive Capability	I_{OH}, VDD=3.3V	I_{OL}, VDD=3.3V	I_{OH}, VDD=2.5V	I_{OL}, VDD=2.5V	I_{OH}, VDD=1.8V	I_{OL}, VDD=1.8V	Unit
2	-2	2	-1.5	1.5	-1	1	mA
4	-4	4	-3	3	-2	2	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7	8	mA

(1) Guaranteed by design, not tested in production.

Table 4-27 Output Voltage Characteristics(3)

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD}=3.3V，I_{OL}(4)= 2/4/8/12	V_{SS}	0.4	V
		V_{DD}=2.5V，I_{OL}(4)= 2/4/8/12	V_{SS}	0.4	
		V_{DD}=1.8V，I_{OL}(4)= 2/4/8/12	V_{SS}	0.2*V_{DD}	
V_{OH}(2)	Output high level	V_{DD}=3.3V，I_{OH}(4)= 2/4/8/12	2.4(5)	V_{DD}	
		V_{DD}=2.5V，I_{OH}(4)= 2/4/8/12	1.8(5)	V_{DD}	
		V_{DD}=1.8V，I_{OH}(4)= 2/4/8/12	0.8*V_{DD}	V_{DD}	

Notes:

(1) The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.

(2) The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.

(3) Data based on characterization results, not tested in production

(4) Actual drive capability see Table 4-26.

(5) PC13, PC14, PC15 are not within this range.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in **Figure 4-9** and **Table 4-28** respectively.

Unless otherwise specified, the parameters listed in **Table 4-28** were measured using ambient temperature and supply

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voltage in accordance with **Table 4-4**.

Table 4-28 Input/Output AC Characteristics (1)

DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=5pF,V_{DD}=3.3V	-	75	MHz
			C_L=5pF,V_{DD}=2.5V	-	50	
			C_L=5pF,V_{DD}=1.8V	-	30	
	$t_{(IO)out}$	Output delay	C_L=5pF,V_{DD}=3.3V	-	3.7	ns
			C_L=5pF,V_{DD}=2.5V	-	4.8	
			C_L=5pF,V_{DD}=1.8V	-	7.2	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns
10 (4mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=10pF,V_{DD}=3.3V	-	90	MHz
			C_L=10pF,V_{DD}=2.5V	-	60	
			C_L=10pF,V_{DD}=1.8V	-	40	
	$t_{(IO)out}$	Output delay	C_L=10pF,V_{DD}=3.3V	-	3.5	ns
			C_L=10pF,V_{DD}=2.5V	-	4.5	
			C_L=10pF,V_{DD}=1.8V	-	6.8	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
01 (8mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=20pF,V_{DD}=3.3V	-	100	MHz
			C_L=20pF,V_{DD}=2.5V	-	75	
			C_L=20pF,V_{DD}=1.8V	-	50	
	$t_{(IO)out}$	Output delay	C_L=20pF,V_{DD}=3.3V	-	3.5	ns
			C_L=20pF,V_{DD}=2.5V	-	4.8	
			C_L=20pF,V_{DD}=1.8V	-	6.6	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
11 (12mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=30pF,V_{DD}=3.3V	-	120	MHz
			C_L=30pF,V_{DD}=2.5V	-	90	
			C_L=30pF,V_{DD}=1.8V	-	60	
	$t_{(IO)out}$	Output delay	C_L=30pF,V_{DD}=3.3V	-	3.4	ns
			C_L=30pF,V_{DD}=2.5V	-	4.3	
			C_L=30pF,V_{DD}=1.8V	-	6.4	
	$t_{(IO)in}$	Input delay	CL=50fF,VDD=2.97V,VDDD=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	

Notes:

(1) The speed of the I/O port can be configured via PMODEy [1:0]. Refer to the N32H497 user manual for instructions on configuring registers for GPIO ports.

*(2) The maximum frequency is defined in **Figure 4-9**.*

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Figure 4-9 Definition Of Input/Output AC Characteristics

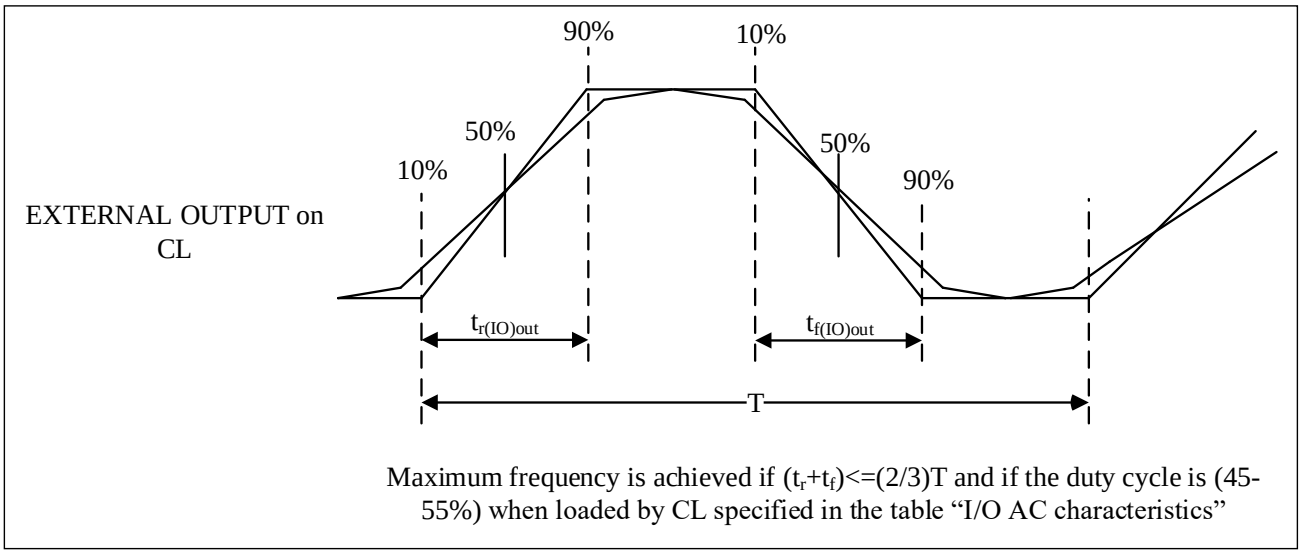
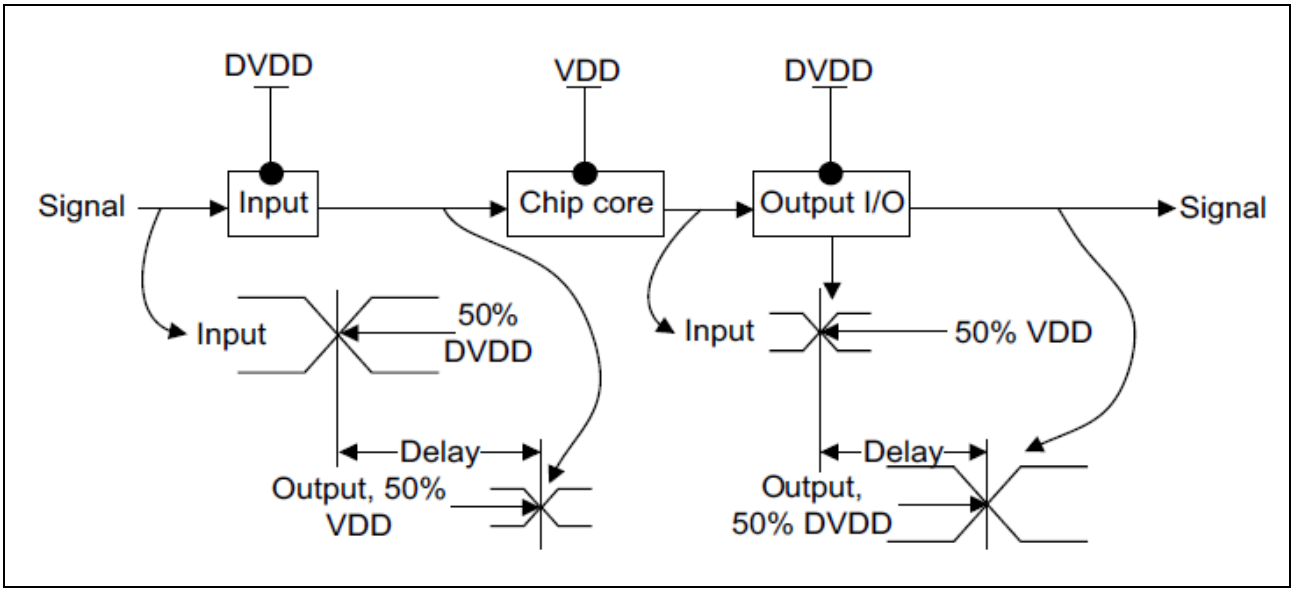


Figure 4-10 Transmission Delay



4.3.13 NRST Pin Characteristics

The NRST pin input driver uses the CMOS process, which is connected to an unbreakable pull-up resistor, R_{PU} (see **Table 4-29**). Unless otherwise specified, the parameters listed in **Table 4-29** were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-29 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	V_{SS}	-	0.3*V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.7*V_{DD}	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance(2)	V_{IN}= V_{SS}	30	50	80	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	VDD=3.3V	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	VDD=3.3V	300	-	-	ns

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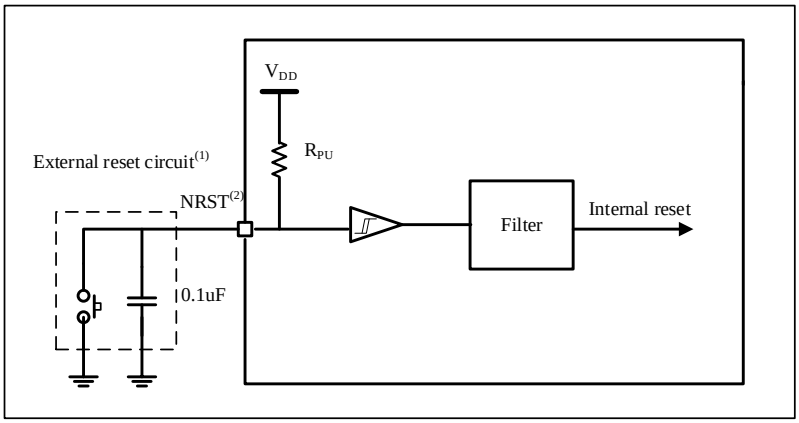
Notes:

(1) Guaranteed by design, not tested in production.

(2) The pull-up resistor is designed as a real resistor in series for a switchable PMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-11 Recommended NRST Pin Protection



Notes:

(1) Acts as a filter.

*(2) The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in **Table 4-29**, otherwise the MCU cannot be reset.*

4.3.14 Timer Characteristics

The parameters listed in **Table 4-30**, **Table 4-31**, **Table 4-32**, **Table 4-33** are guaranteed by design, not tested in production.

See section 4.3.12 for details on the features of the I/O alternate function pins (output comparison, input capture, external clock, PWM output).

Table 4-30 ATIM1/2/3 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	4.16	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 240MHz	0	120	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	0.00416	273	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	-	17.9	s

(1) Guaranteed by design, not tested in production.

Table 4-31 GTIM1/2/3/4/5/6/7 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	8.33	-	ns
		$f_{TIMxCLK}$= 180MHz	5.56	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 120MHz	0	60	MHz

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Symbol	Parameter	Condition	Min	Max	Unit
		$f_{TIMxCLK}$= 180MHz	0	90	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	0.00833	546	µs
		$f_{TIMxCLK}$= 180MHz	0.00556	364	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	-	35.8	s
		$f_{TIMxCLK}$= 180MHz	-	23.9	s

(1) Guaranteed by design, not tested in production.

Table 4-32 GTIM8/9/10 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	4.16	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 240MHz	0	120	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	0.00416	273	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 240MHz	-	17.9	s

(1) Guaranteed by design, not tested in production.

Table 4-33 LPTIMER1/2 Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Maximum possible count	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	8.33	-	ns
f_{EXT}	Maximum possible count	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 120MHz	0	60	MHz
Res_{TIM}	Maximum possible count	-	-	16	bit
$t_{COUNTER}$	Maximum possible count	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	0.00833	546	µs
t_{MAX_COUNT}	Maximum possible count	-	-	128x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 120MHz	-	69.9	ms

(1) Guaranteed by design, not tested in production.

4.3.15 Watchdog Characteristics

Table 4-34 IWDG Counting Maximum And Minimum Reset Time (LSI = 32 Khz)

Prescaler	PD[2:0]	Min timeout RL[11:0] = 0	Max timeout RL[11:0] = 0xFFF	Unit
/4	000	0.125	512	ms
/8	001	0.25	1024	
/16	010	0.5	2048	

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/32	011	1.0	4096	
/64	100	2.0	8192	
/128	101	4.0	16384	
/256	11x	8.0	32768	

(1) Guaranteed by design, not tested in production.

Table 4-35 WWDG Counting Maximum And Minimum Reset Time (PCLK1 = 120 Mhz)

Prescaler	TIMERB[1:0]	Min timeout	Max timeout	Unit
/1	0	0.0341	556.92	ms
/2	1	0.0682	1113.84	
/3	2	0.136	2227.68	
/4	3	0.273	4455.36	

(1) Guaranteed by design, not tested in production.

4.3.16 I²C Interface Characteristics

Unless otherwise specified, the parameters listed in **Table 4-36** were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

The I²C interface of the N32H497 product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open-drain pins, and when configured for open-drain output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in **Table 4-36**. See Section 4.3.12 for details about the features of the input/output alternate function pins (SDA and SCL).

Table 4-36 I²C Interface Characteristics(1)

Symbol	Parameter	Standard mode		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{su(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	µs
$t_{h(SDA)}$	SDA data hold time	300	-	300	-	0	-	µs
$t_{su(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	µs
Cb	Capacitive load per bus	-	400	-	400	-	550	pf
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	µs
$t_{v\,(ACK)}$	Response time	-	3.45	-	0.9	-	0.45	µs

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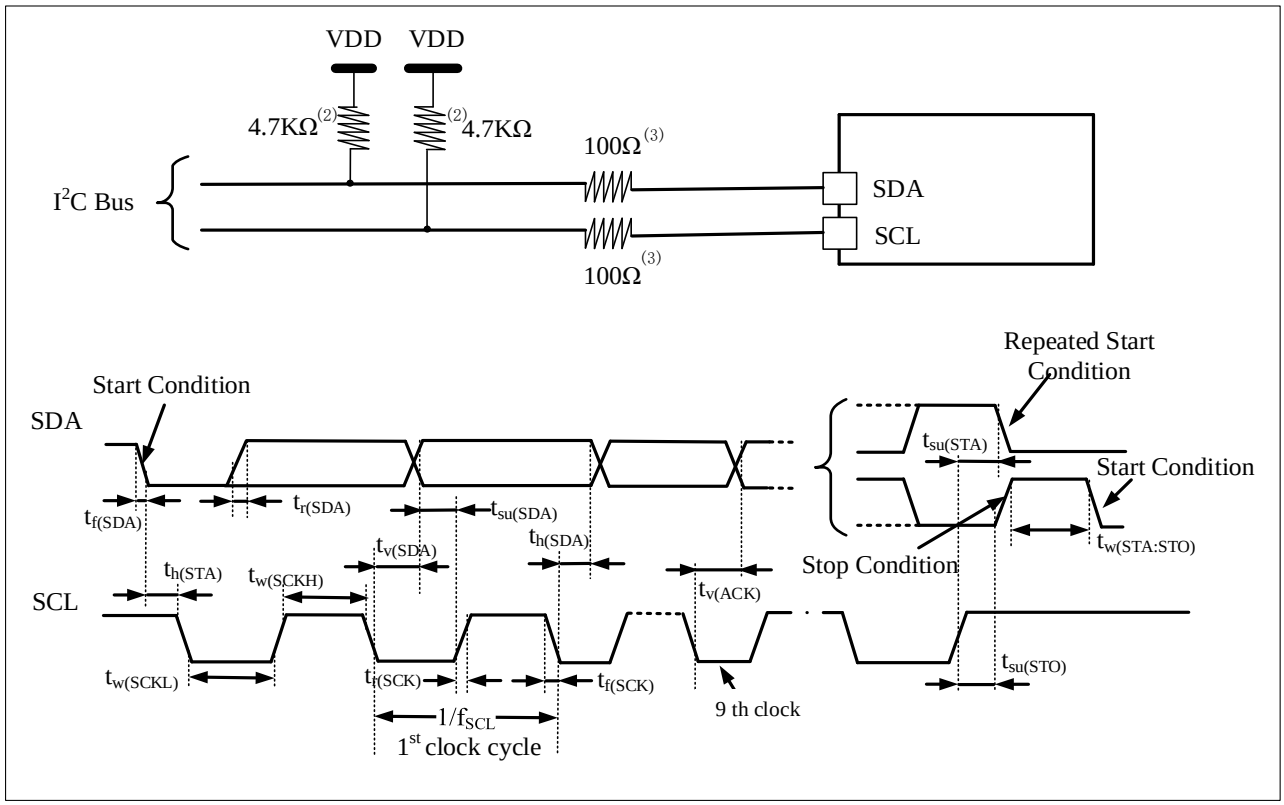
Symbol	Parameter	Standard mode		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
t_{SP}	Spike pulse width to be suppressed by the input filter	-	-	0	50	0	50	ns

(1) Guaranteed by design, not tested in production.

Figure 4-12 I²C Bus AC Waveform And Measuring Circuit (1)



Notes:

(1) The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

(2) The pull-up resistance depends on the I²C interface speed.

(3) The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.17 SPI/I²S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in **Table 4-37** and the I²S parameters listed in **Table 4-38** are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with **Table 4-4.**

See Section 4.3.12 for details on the characteristics of the I/O multiplexed pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

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Table 4-37 SPI Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	-	60	MHz
		Slave mode	-	-	40	
DuCy(SCK)	SPI from the input clock duty cycle	SPI slave mode	45	50	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Master mode	$t_{SCLK}/2$	-	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$t_{SCLK}/2$	-	-	
$t_{w(SCLKH)}$ (1) $t_{w(SCLKL)}$ (1)	SCLK high and low time	Master mode	$t_{SCLK}/2$ - 1	$t_{SCLK}/2$	$t_{SCLK}/2$ + 1	
$t_{su(MI)}$ (1)	Data entry setup time	Master mode	3	-	-	
$t_{su(SI)}$ (1)		Slave mode	3	-	-	
$t_{h(MI)}$ (1)	Data entry hold time	Master mode	2.5	-	-	
$t_{h(SI)}$ (1)		Slave mode	2	-	-	
$t_{a(SO)}$ (1)(2)	Data entry hold time	Slave mode	9	-	$2*t_{SCLK}/2$	
$t_{dis(SO)}$ (1)(3)	Data entry hold time	Slave mode	9	-	16	
$t_{v(SO)}$ (1)	Valid time of data output	Slave mode (after enable edge)	-	9	13	
$t_{v(MO)}$ (1)		Master mode (after enable edge)	-	3	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	5	-	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	0	-	-	

Notes:

(1) Guaranteed by design, not tested in production.

(2) The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.

(3) The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-13 SPI Timing Diagram-Slave Mode And CPHA=0

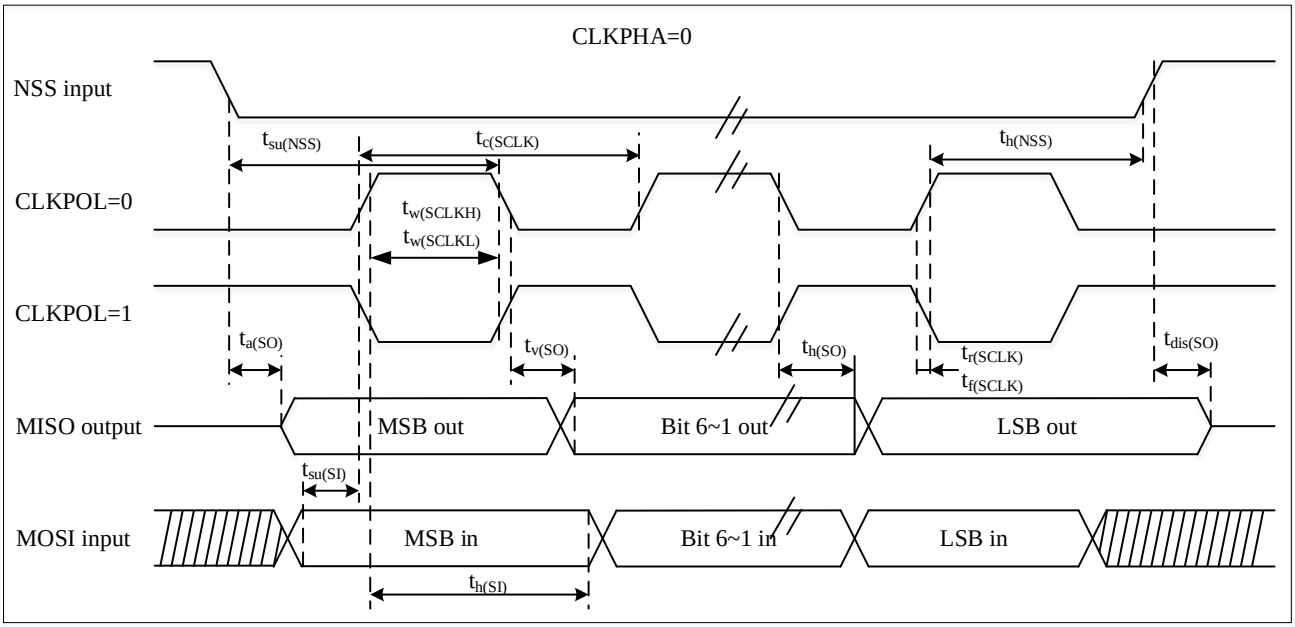

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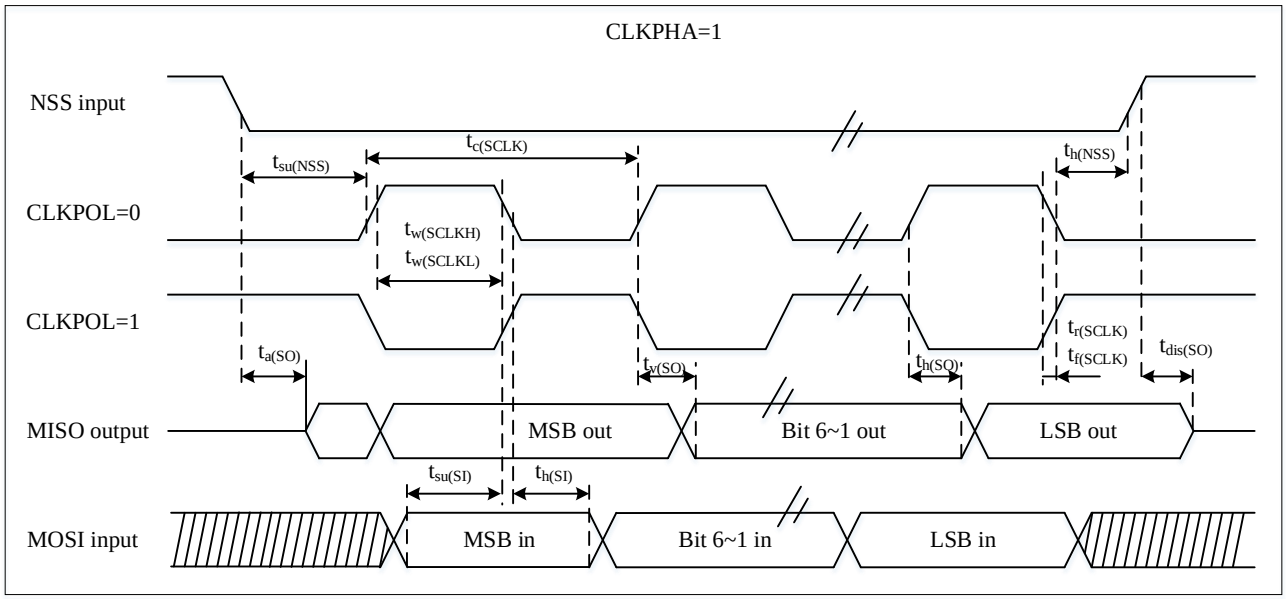
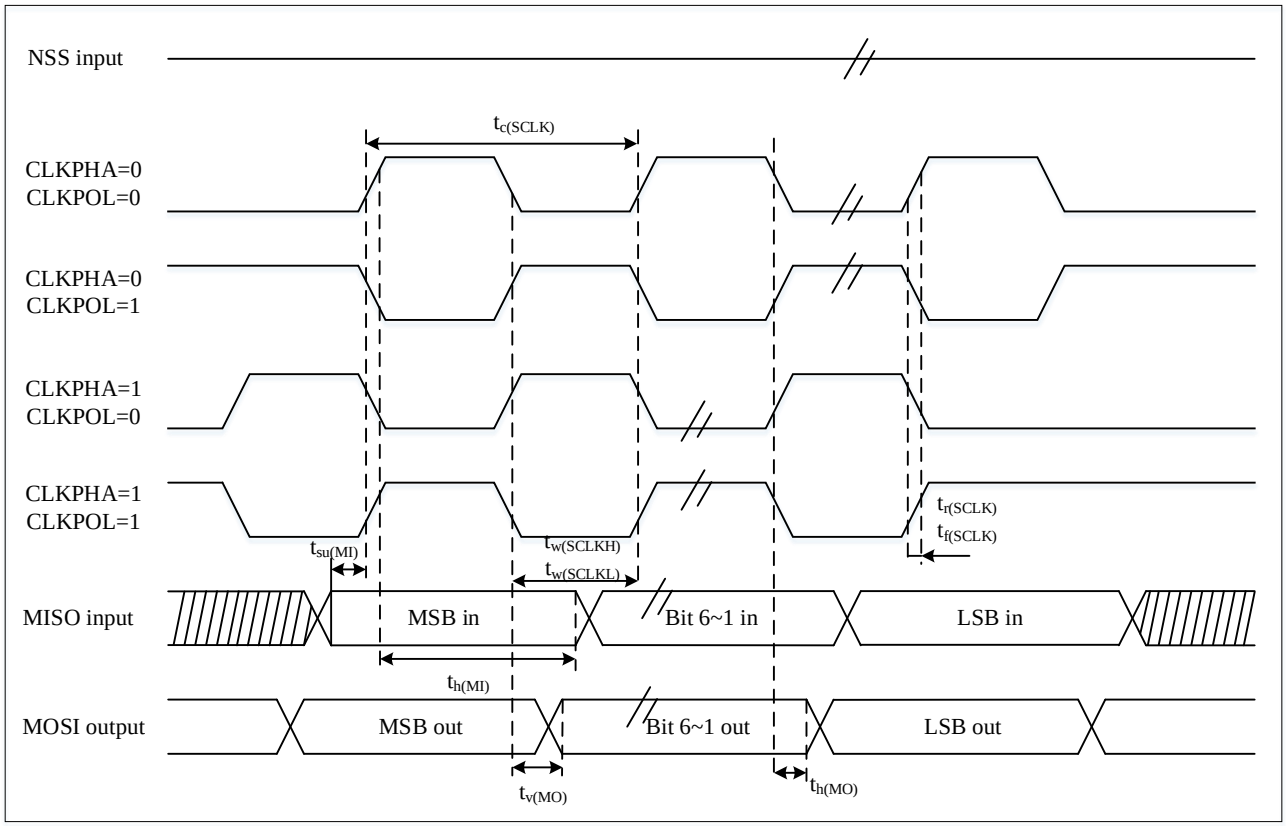
Figure 4-14 SPI Timing Diagram-Slave Mode And CPHA=1 (1)



(1) The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-15 SPI Timing Diagram-Master Mode (1)



(1) The measuring point is set at the CMOS level: 0.3V and $0.7V_{DD}$.

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Table 4-38 I²S Characteristics (1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{MCLK}	I²S main clock frequency	Master mode		256x8K	256Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I²S clock frequency	Master mode (32 bit)		-	64Fs(3)	
		Slave mode (32 bit)		-	64Fs(3)	
DuCy(SCK)	I²S input clock duty cycle	I²S slave mode		30	70	%
$t_{v(WS)}$ (1)	WS valid time	Master mode	I2S2	-	6	
			I2S3	-	6	
$t_{h(WS)}$(1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	2		
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	7	-	
			I2S3	7	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I2S2	0	-	
			I2S3	0	-	
$t_{w(CLKH)}$(1)	CLK high and low times	Master mode, f_{PCLK} = 16MHz, audio 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	I2S2	6	-	
			I2S3	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S2	7	-	
			I2S3	7	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	I2S2	0	-	
			I2S3	0		
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S2	1	-	
			I2S3	1		
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	I²S2	-	15	
			I²S3	-	15	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	I²S2	4	-	
			I²S3	4	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	6	
			I2S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge))	I2S2	0	-	
			I2S3	0	-	

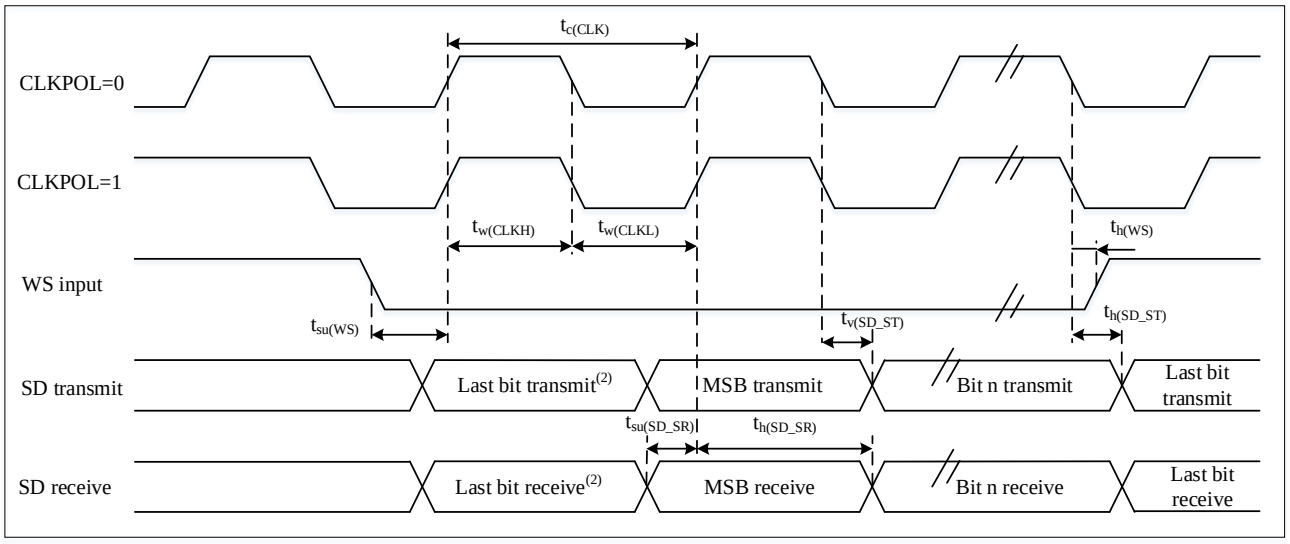
Notes:

(1) Guaranteed by design, not tested in production.

(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK}=1/f_{PCLK} =125ns.

(3) Audio signal sampling frequency.

Figure 4-16 I²S Slave Mode Timing Diagram (Philips Protocol) (1)



Notes:

(1) The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

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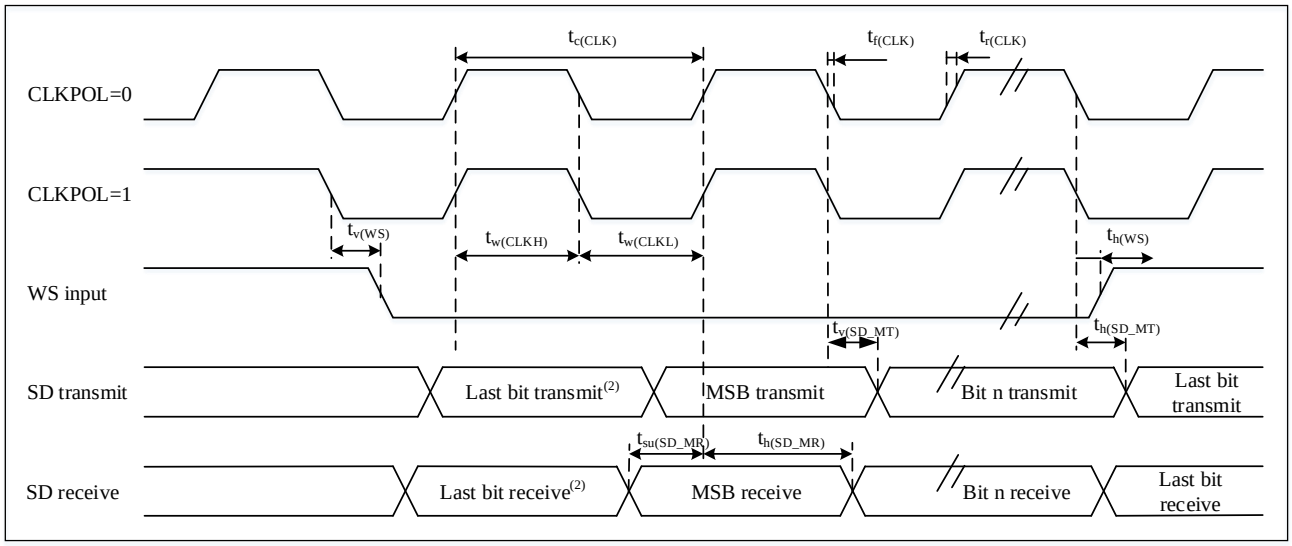
(2) Transmit/receive of the last byte.There is no least significant transmit/receive before the first byte.

Figure 4-17 I²s Master Mode Timing Diagram (Philips Protocol) (1)



Notes:

(1) The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

(2) Send/receive of the last byte. There is no least significant send/receive before the first byte.

4.3.18 xSPI Characteristics

Table 4-39 Characteristics Of XSPI In SDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$		$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	
$t_{s(IN)}$	Data input setup time	2.5	-	-	ns
$t_{h(IN)}$	Data input hold time	5.5	-	-	ns
$t_{v(OUT)}$	Data output valid time	-	2.5	3.5	ns
$t_{h(OUT)}$	Data output hold time	2.5	-	-	ns

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Figure 4-18 Timing Of XSPI In SDR Mode

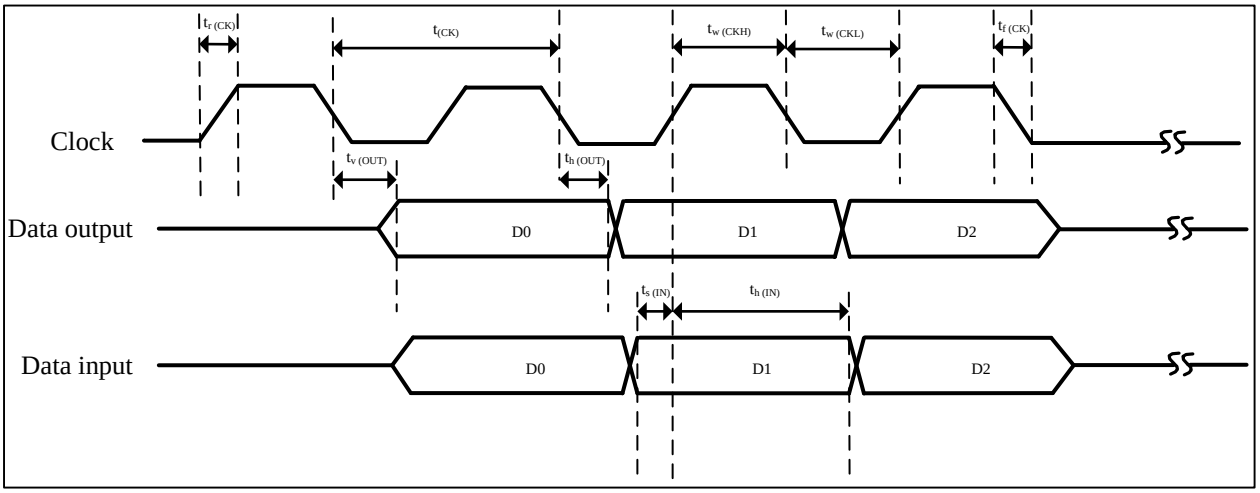

Table 4-40 Features Of XSPI In DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$		$t_{(CK)}$/2-0.5	-	$t_{(CK)}$/2	ns
$t_{sf(IN)}$	Data input setup time	3	-	-	ns
$t_{sr(IN)}$		5	-	-	ns
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time	2	-	-	ns
$t_{vf(OUT)}$;$t_{vr(OUT)}$	Data output valid time	-	-	7	ns
$t_{hf(OUT)}$;$t_{hr(OUT)}$	Data output hold time	4	-	-	ns

Figure 4-19 Timing Of XSPI In DDR Mode

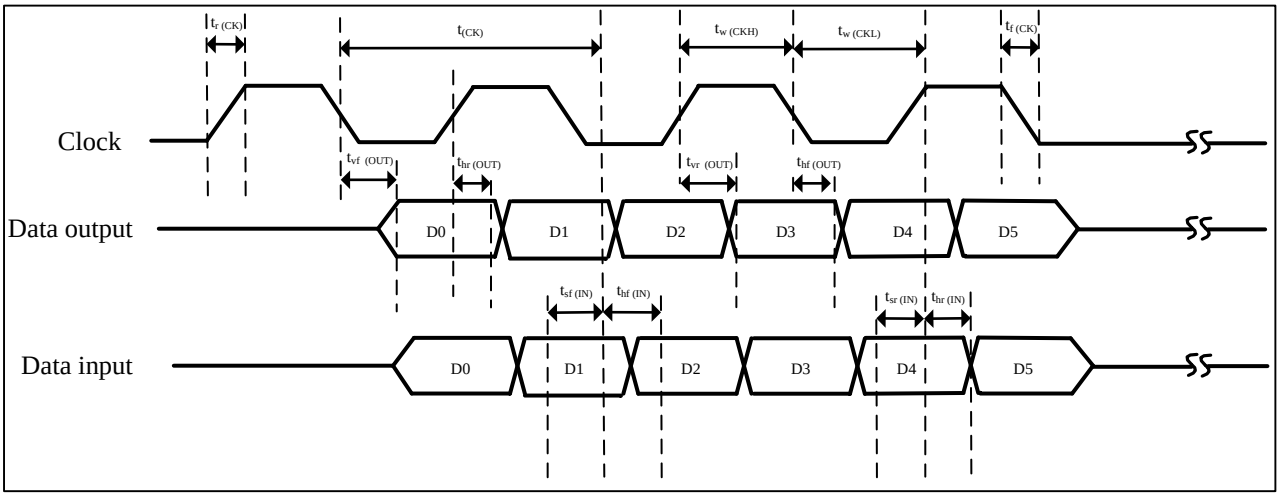

Table 4-41 Features Of XSPI In RXDS Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	t(CK)/2-0.5	-	t(CK)/2	ns
$t_{w(CKL)}$		t(CK)/2-0.5	-	t(CK)/2	
$t_{v(CLK)}$	clock valid time	-	-	t(CK)+2	

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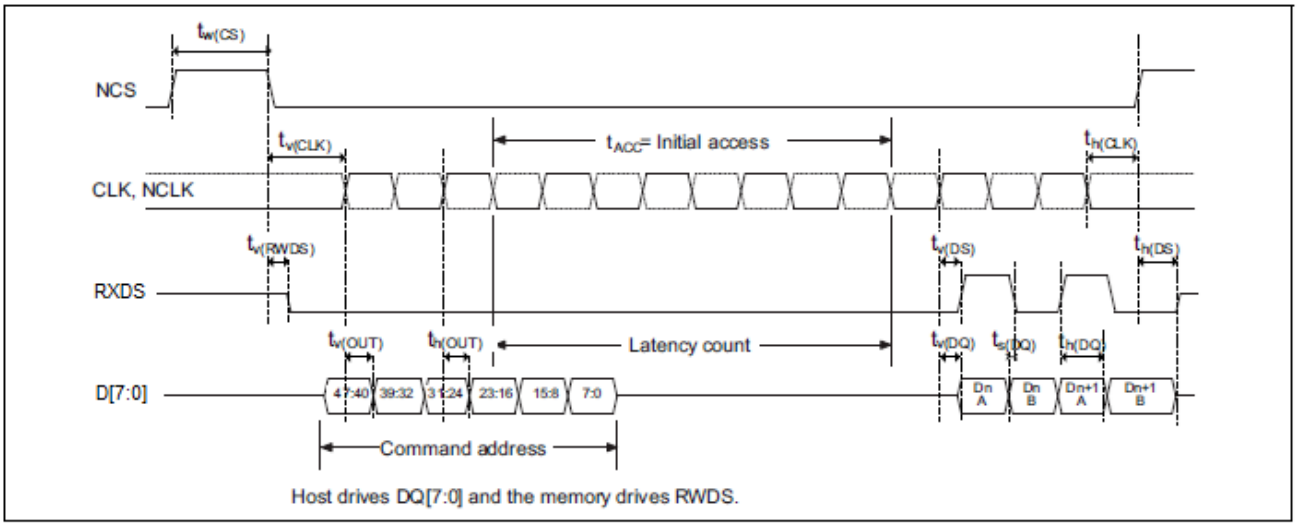
$t_{h(CLK)}$	clock high time	t(CK)+0.5	-	-	
$t_{w(CS)}$	chip select high time	3*t(CK)	-	-	
$t_{v(DQ)}$	Data input valid time	0	-	-	
$t_{v(DS)}$	Data selection input valid time	0	-	-	
$t_{h(DS)}$	Data selection input hold time	0	-	-	
$t_{v(RWDS)}$	Data selection output valid time	-	-	3*t(CK)	
$t_{sf(DQ)};t_{sr(DQ)}$	Input data setup time	3	-	-	ns
$t_{hf(DQ)}$; $t_{hr(DQ)}$	Input data hold time	4	-	-	ns
$t_{vf(OUT)};t_{vr(OUT)}$	Output data setup time	-	6	7	ns
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Output data hold time	3.5	-	-	ns

Figure 4-20 Timing Of XSPI In RXDS Mode



4.3.19 FEMC Characteristics

Synchronous waveforms and timings

Figure 4-21 through **Figure 4-24** represent synchronous waveforms and **Table 4-42** through **Table 4-45** provide the corresponding timings. The results shown in these tables are obtained with the following FEMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

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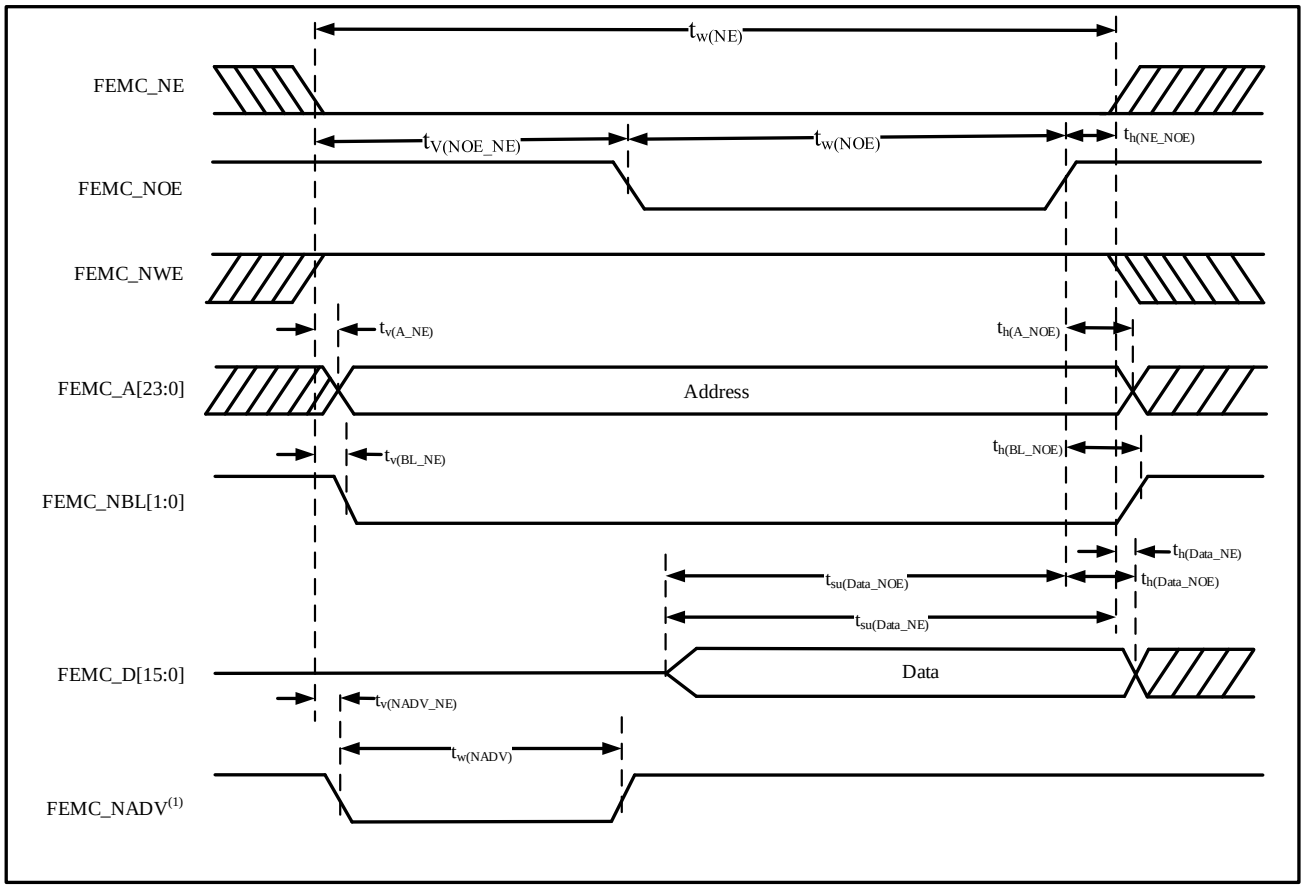
Figure 4-21 Asynchronous Non-Multiplexed SRAM/PSRAM/NOR Read Waveforms



Note:

(1) Only suitable for modes 2/B, C, and D. In mode 1, FEMC_NADV is not used.

Table 4-42 Asynchronous Non-Multiplexed SRAM/PSRAM/NOR Read Timings(1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE low time	$5t_{HCLK} – 0.5$	$5t_{HCLK} + 1$	ns
$t_{v(NOE\_NE)}$	FEMC_NEx low to FEMC_NOE low	0.5	2	ns
$t_{w(NOE)}$	FEMC_NOE low time	$5t_{HCLK} – 0.5$	$5t_{HCLK} + 1$	ns
$t_{h(NE\_NOE)}$	FEMC_NOE high to FEMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FEMC_NEx low to FEMC_A valid	-	3	ns
$t_{h(A\_NOE)}$	Address hold time after FEMC_NOE high	4	-	ns
$t_{v(BL\_NE)}$	FEMC_NEx low to FEMC_BL valid	-	1.5	ns
$t_{h(BL\_NOE)}$	FEMC_BL hold time after FEMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FEMC_NEx high setup time	$2t_{HCLK} + 3$	-	ns
$t_{su(Data\_NOE)}$	Data to FEMC_NOEx high setup time	$2t_{HCLK} + 3$	-	ns
$t_{h(Data\_NOE)}$	Data to FEMC_NOEx high hold time	0	-	ns
$t_{h(Data\_NE)}$	Data to FEMC_NOEx high hold time	0	-	ns
$t_{v(NADV\_NE)}$	FEMC_NEx low to FEMC_NADV low	-	2	ns
$t_{w(NADV)}$	FEMC_NADV low time	-	$2t_{HCLK}$	ns

Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

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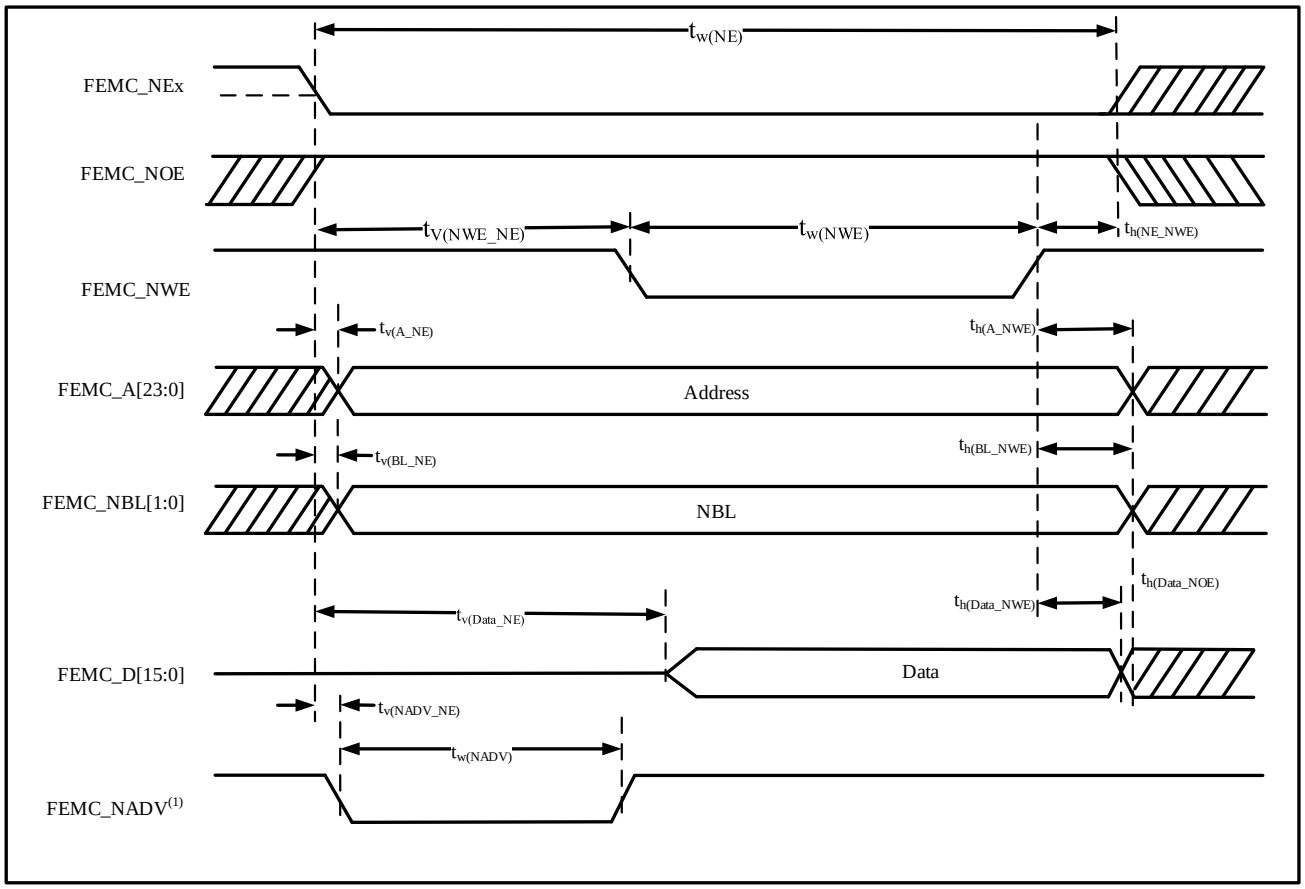
(2) Measurement point set at CMOS level: 0.5VDD

(3) t_{HCLK} >= 1/120MHz

Figure 4-22 Asynchronous Non-Multiplexed SRAM/PSRAM/NOR Write Waveforms



Note:

(1) Only suitable for modes 2/B, C, and D. In mode 1, FEMC_NADV is not used.

Table 4-43 Asynchronous Non-Multiplexed SRAM/PSRAM/NOR Write Timings(1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE low time	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1$	ns
$t_{v(NWE\_NE)}$	FEMC_NEx low to FEMC_NWE low	$1t_{HCLK} - 0.5$	$1t_{HCLK} + 0.5$	ns
$t_{w(NWE)}$	FEMC_NWE low time	$1t_{HCLK} - 0.5$	$1t_{HCLK} + 1$	ns
$t_{h(NE\_NWE)}$	FEMC_NWE high to FEMC_NE high hold time	$1t_{HCLK}$	-	ns
$t_{v(A\_NE)}$	FEMC_NEx low to FEMC_A valid	-	3	ns
$t_{h(A\_NWE)}$	Address hold time after FEMC_NWE high	$1t_{HCLK}$	-	ns
$t_{v(BL\_NE)}$	FEMC_NEx low to FEMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FEMC_BL hold time after FEMC_NWE high	$1t_{HCLK} - 0.5$	-	ns
$t_{v(Data\_NE)}$	FEMC_NEx low to data valid	-	$1t_{HCLK} + 3$	ns
$t_{h(Data\_NWE)}$	Date hold time after FEMC_NWE high	$1t_{HCLK}-1$	-	ns
$t_{v(NADV\_NE)}$	FEMC_NEx low to FEMC_NADV valid	-	2	ns
$t_{w(NADV)}$	FEMC_NADV low time	-	$1t_{HCLK} + 1$	ns

Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

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(2) Measurement point set at CMOS level: 0.5VDD

(3) t_{HCLK} >= 1/120MHz

Figure 4-23 Asynchronous Multiplexed PSRAM /NOR Read Waveforms

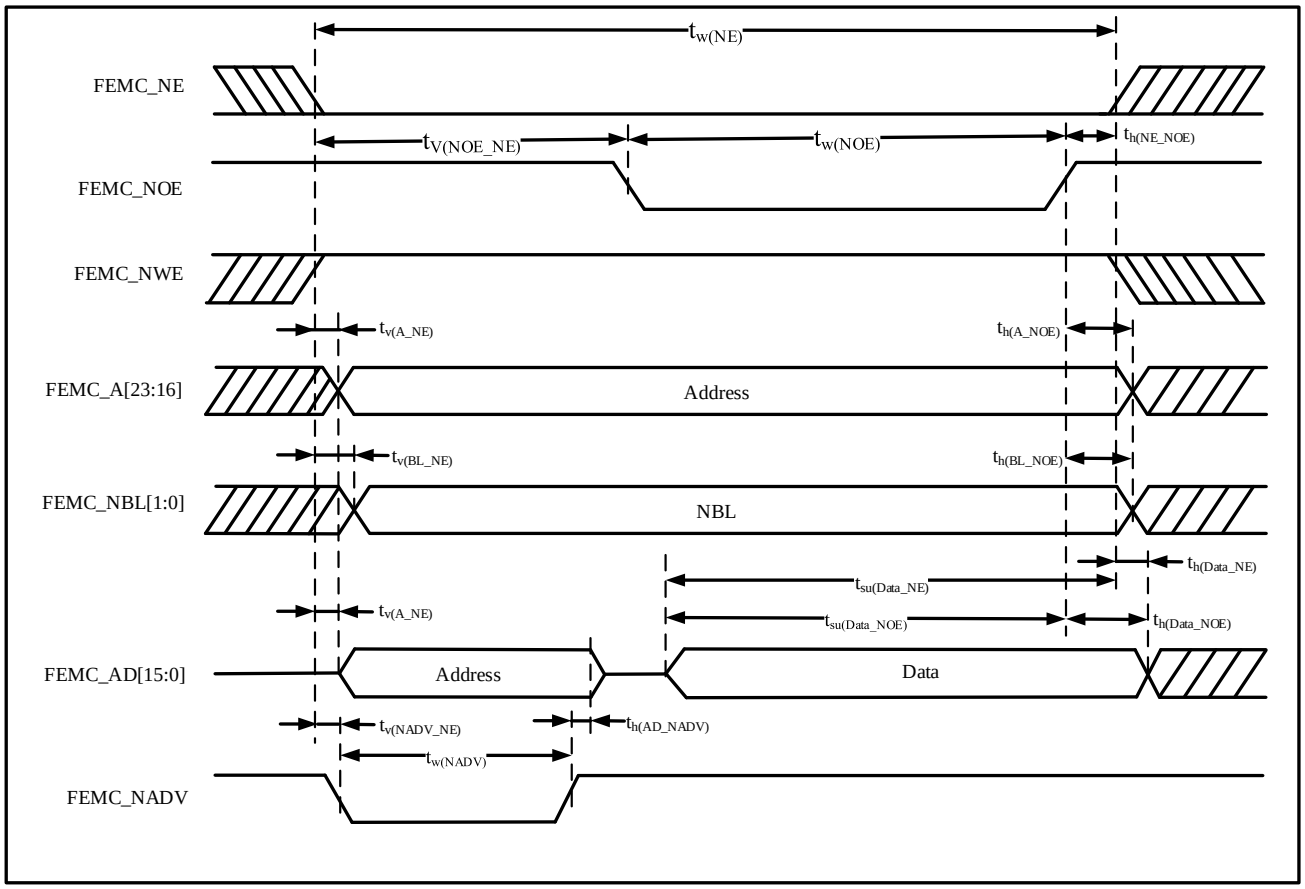

Table 4-44 Asynchronous Multiplexed PSRAM/NOR Write Timings(1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE low time	$7t_{HCLK} - 1$	$7t_{HCLK} + 1$	ns
$t_{v(NOE\_NE)}$	FEMC_NEx low to FEMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1$	ns
$t_{w(NOE)}$	FEMC_NOE low time	$4t_{HCLK} - 0.5$	$4t_{HCLK} + 1$	ns
$t_{h(NE\_NOE)}$	FEMC_NOE high to FEMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FEMC_NEx low to FEMC_A valid	-	3	ns
$t_{v(NADV\_NE)}$	FEMC_NEx low to FEMC_NADV low	1	2	ns
$t_{w(NADV)}$	FEMC_NADV low time	$t_{HCLK} - 1.5$	$t_{HCLK} + 1.5$	ns
$t_{h(AD\_NADV)}$	FEMC_A valid hold time after FEMC_NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	FEMC_A hold time after FEMC_NOE high	$t_{HCLK} - 1$	-	ns
$t_{h(BL\_NOE)}$	FEMC_BL hold time after FEMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FEMC_NEx low to FEMC_BL valid	-	1.5	ns
$t_{su(Data\_NE)}$	Data to FEMC_NEx high setup time	$1t_{HCLK} + 3$	-	ns
$t_{su(Data\_NOE)}$	Data to FEMC_NOE high hold time	$1t_{HCLK} + 3$	-	ns
$t_{h(Data\_NE)}$	Data hold time after FEMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FEMC_NOE high	0	-	ns

Notes:

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(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

(2) Measurement point set at CMOS level: 0.5VDD

(3) t_{HCLK} >= 1/120MHz

Figure 4-24 Asynchronous Multiplexed PSRAM/NOR Write Waveforms

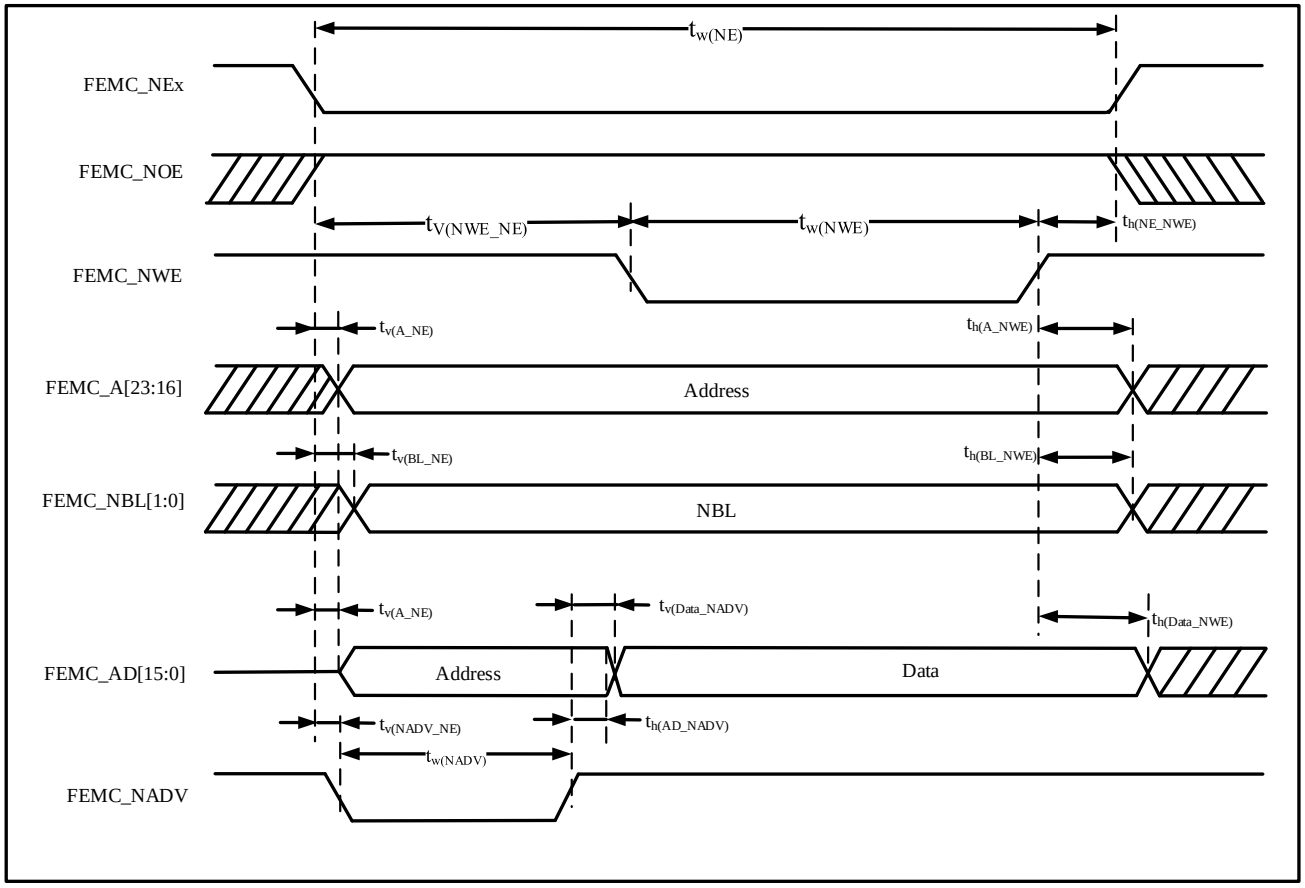

Table 4-45 Asynchronous Multiplexed PSRAM/NOR Write Timings(1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE low time	$5t_{HCLK} - 1$	$5t_{HCLK} + 1$	ns
$t_{v(NWE\_NE)}$	FEMC_NEx low to FEMC_NWE low	$2t_{HCLK}$	$2t_{HCLK} + 1$	ns
$t_{w(NWE)}$	FEMC_NWE low time	$2t_{HCLK} - 0.5$	$2t_{HCLK} + 1$	ns
$t_{h(NE\_NWE)}$	FEMC_NWE high to FEMC_NE high hold time	$t_{HCLK} - 1$	-	ns
$t_{v(A\_NE)}$	FEMC_NEx low to FEMC_A valid	-	3	ns
$t_{v(NADV\_NE)}$	FEMC_NEx low to FEMC_NADV low	1	2	ns
$t_{w(NADV)}$	FEMC_NADV low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	ns
$t_{h(AD\_NADV)}$	FEMC_A valid hold time after FEMC_NADV high	$t_{HCLK} - 1$	-	ns
$t_{h(A\_NWE)}$	FEMC_A hold time after FEMC_NWE high	$4t_{HCLK}$	-	ns
$t_{v(BL\_NE)}$	FEMC_BL hold time after FEMC_NWE high	-	1.5	ns
$t_{h(BL\_NWE)}$	FEMC_NWE low to FEMC_BL valid	$t_{HCLK} - 1$	-	ns
$t_{v(Data\_NADV)}$	Data hold time after FEMC_NADV high	-	$t_{HCLK} + 1$	ns
$t_{h(Data\_NWE)}$	Data hold time after FEMC_NWE high	t_{HCLK}	-	ns

Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

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(2) Measurement point set at CMOS level: 0.5VDD

(3) t_{HCLK} >= 1/120MHz

Synchronous waveforms and timings

Figure 4-25 through **Figure 4-28** represent synchronous waveforms and **Table 4-46** hrough **Table 4-49** provide the corresponding timings. The results shown in these tables are obtained with the following FEMC configuration:

- BurstAccMode = FEMC_NOR_SRAM_BURST_MODE_ENABLE, enable burst mode
- MemoryType = FEMC_MEM_TYPE_PSRAM, memory type is PSRAM
- WriteBurst = FEMC_NOR_SRAM_BURST_WRITE_ENABLE, enable burst write operation
- CLKDiv = 1, (1 memory cycle = 2 HCLK cycles) (Note: ClkDiv is the CLKDIV bit in the FEMC_SNTCFGx register)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

(Note: DataLatency is the DATAHLD bit in the FEMC_SNTCFGx register)

Figure 4-25 Synchronous Non-Multiplexed PSRAM/NOR Read Waveforms

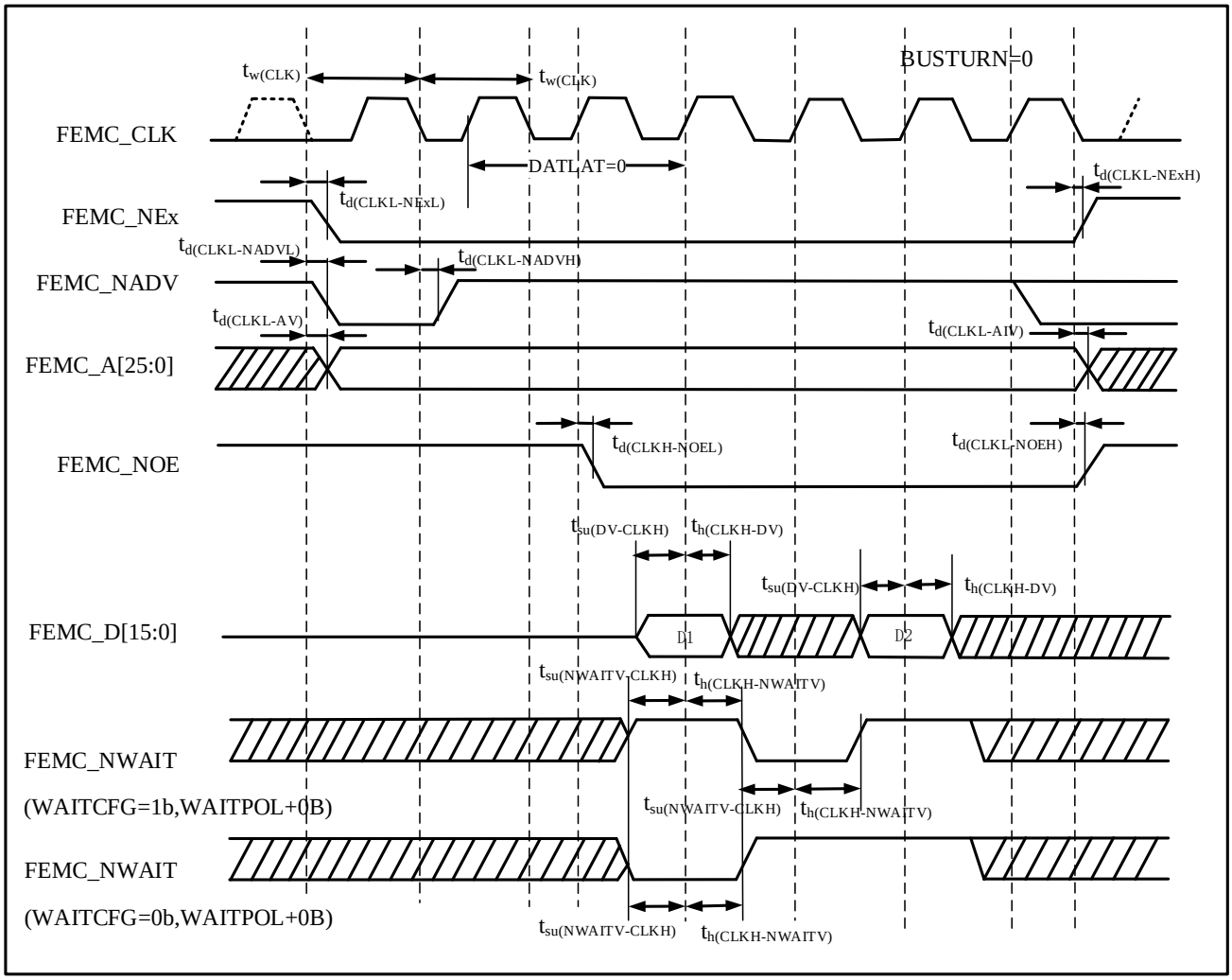

Table 4-46 Synchronous Non-Multiplexed PSRAM/NOR Read Timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	16.67	-	ns

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$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low	-	1	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high	0	-	ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FEMC_CLK low to FEMC_Ax valid	-	2	ns
$t_{d(CLKL-AIV)}$	FEMC_CLK low to FEMC_Ax invalid	2	-	ns
$t_{d(CLKL-NOEL)}$	FEMC_CLK low to FEMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FEMC_CLK low to FEMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FEMC_D[15:0] valid before FEMC_CLK high	3	-	ns
$t_{h(CLKH-DV)}$	FEMC_D[15:0] valid after FEMC_CLK high	2	-	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid before FEMC_CLK high	3	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid after FEMC_CLK high	2	-	ns

Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

(2) Measurement point set at CMOS level: 0.5VDD

Figure 4-26 Synchronous Non-Multiplexed PSRAM Write Waveforms

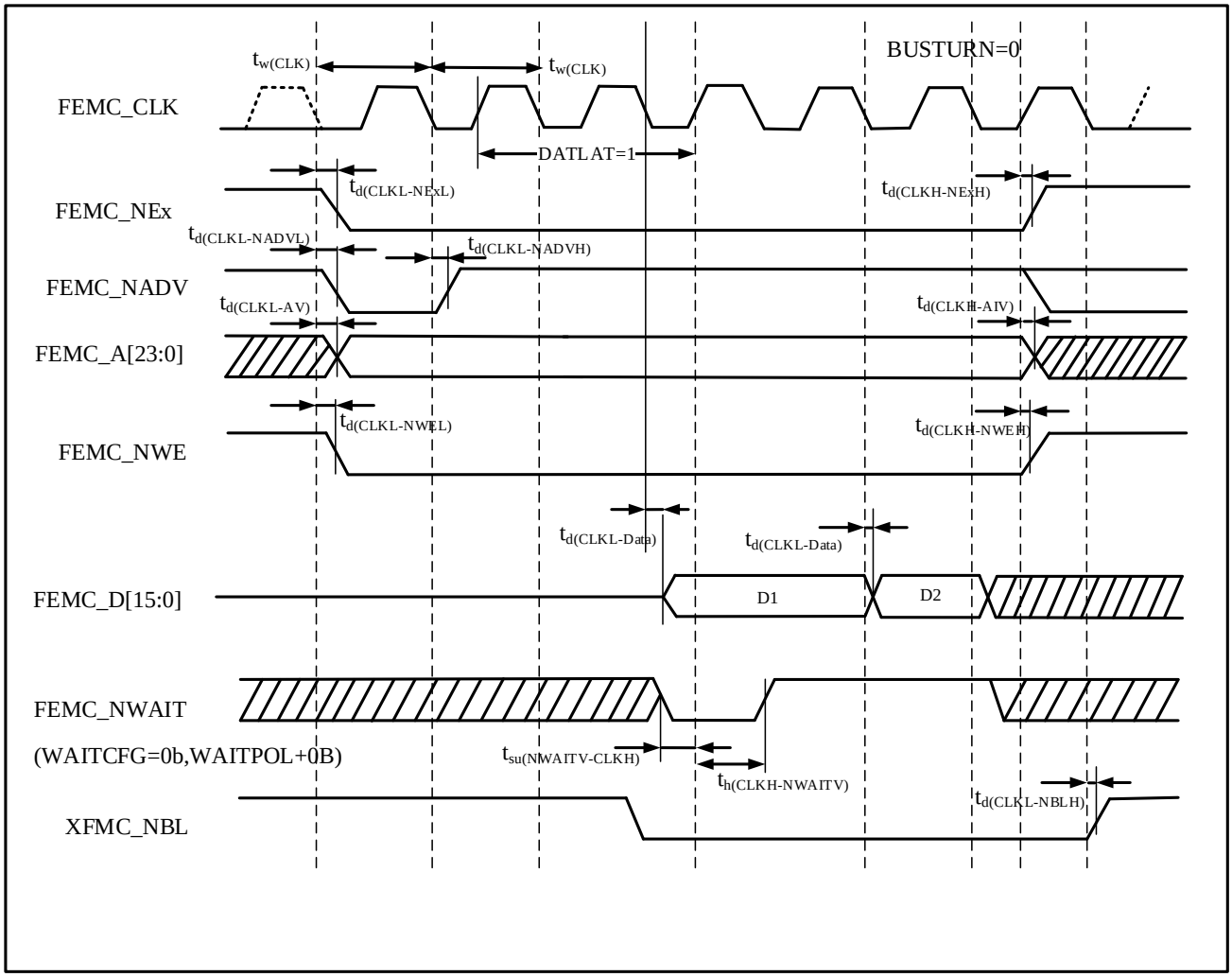

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Table 4-47 Synchronous Non-Multiplexed PSRAM Write Timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	16.67	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low	-	1	ns
$t_{d(CLKH-NExH)}$	FEMC_CLK low to FEMC_NEx high	1	-	ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FEMC_CLK low to FEMC_Ax valid	-	3	ns
$t_{d(CLKH-AIV)}$	FEMC_CLK low to FEMC_Ax invalid	2	-	ns
$t_{d(CLKL-NWEL)}$	FEMC_CLK low to FEMC_NWE low	-	1	ns
$t_{d(CLKH-NWEH)}$	FEMC_CLK low to FEMC_NWE high	1.5	-	ns
$t_{d(CLKL-Data)}$	FEMC_D[15:0] valid after FEMC_CLK high	-	3	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid before FEMC_CLK high	2	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid after FEMC_CLK high	3	-	ns
$t_{d(CLKL-NBLH)}$	FEMC_CLK low to FEMC_NBL high	2	-	ns

Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

(2) Measurement point set at CMOS level: 0.5VDD

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Figure 4-27 Synchronous Multiplexed NOR/PSRAM Write Waveforms

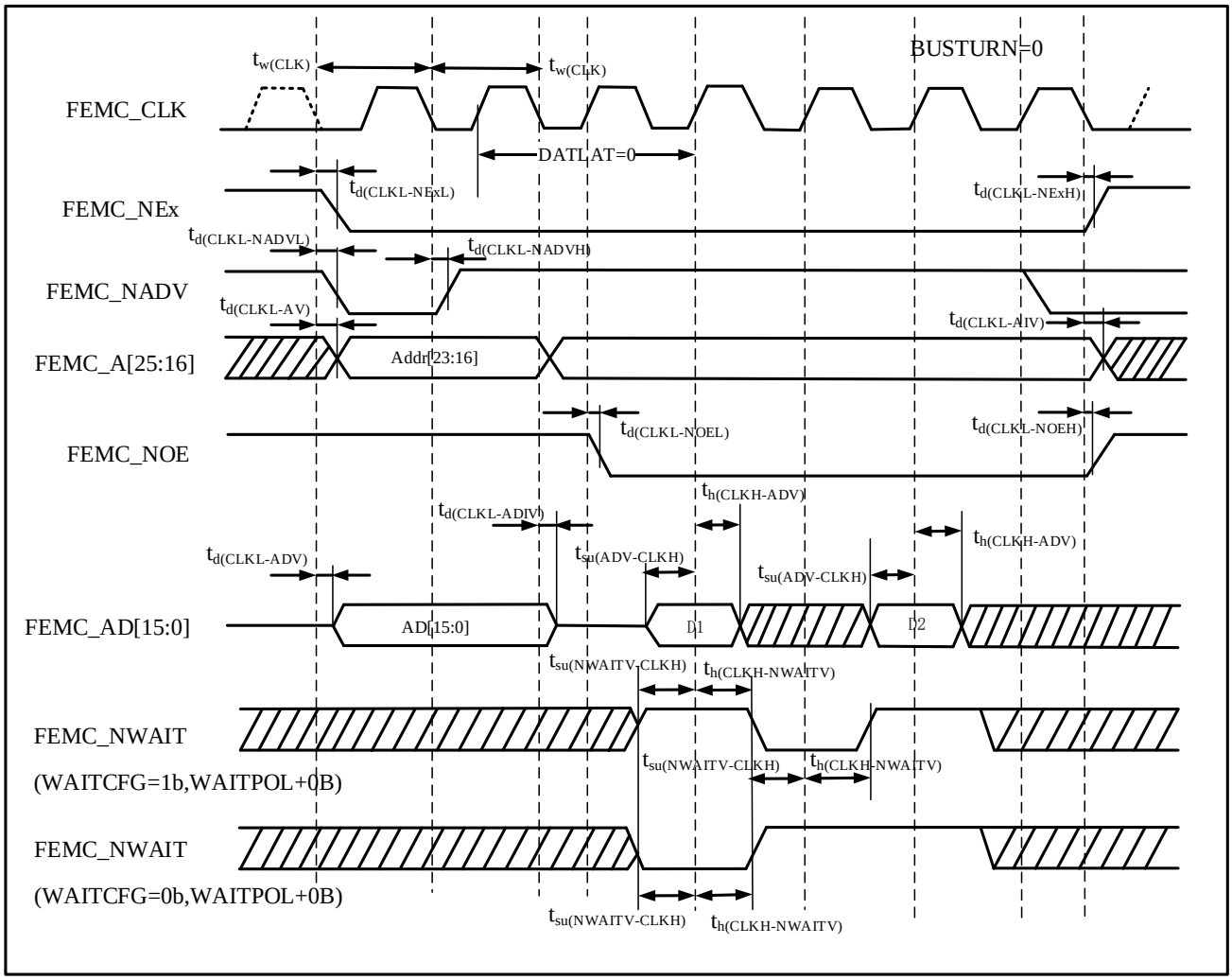

Table 4-48 Synchronous Multiplexed NOR/PSRAM Write Timings(1)(2)

Symbol	Parameter	Min(3)	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	$4t_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low	-	1.5	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high	2	-	ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FEMC_CLK low to FEMC_Ax valid	-	2	ns
$t_{d(CLKL-AIV)}$	FEMC_CLK low to FEMC_Ax invalid	2	-	ns
$t_{d(CLKL-NOEL)}$	FEMC_CLK low to FEMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FEMC_CLK low to FEMC_NOE high	1.5	-	ns
$t_{d(CLKL-ADV)}$	FEMC_CLK low to FEMC_AD[15:0] valid	-	3	ns
$t_{d(CLKL-ADIV)}$	FEMC_CLK low to FEMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FEMC_AD[15:0] valid before FEMC_CLK high	3	-	ns
$t_{h(CLKH-ADV)}$	FEMC_AD[15:0] valid after FEMC_CLK high	2	-	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid before FEMC_CLK high	3	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid after FEMC_CLK high	3	-	ns

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Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

(2) Measurement point set at CMOS level: 0.5VDD

(3) t_{HCLK} >= 1/120MHz

Figure 4-28 Synchronous Multiplexed PSRAM Write Waveforms

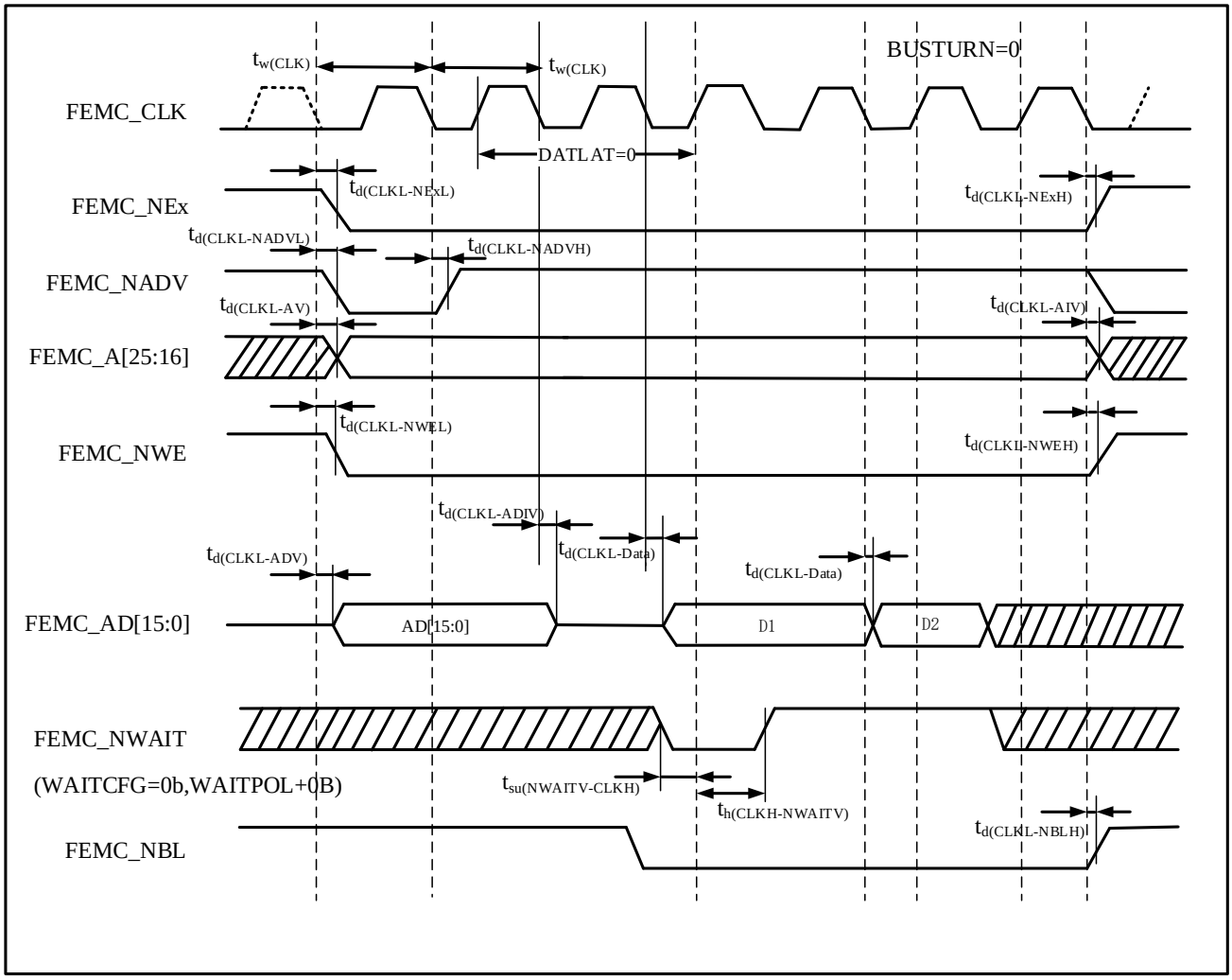

Table 4-49 Synchronous Multiplexed NOR/PSRAM Write Timings(1)(2)

Symbol	Parameter	Min(3)	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	$4t_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low	-	1.5	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high	2	-	ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FEMC_CLK low to FEMC_Ax valid	-	3	ns
$t_{d(CLKL-AIV)}$	FEMC_CLK low to FEMC_Ax invalid	2	-	ns
$t_{d(CLKL-NWEL)}$	FEMC_CLK low to FEMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FEMC_CLK low to FEMC_NWE high	1.5	-	ns
$t_{d(CLKL-ADV)}$	FEMC_CLK low to FEMC_AD[15:0] valid	-	3	ns
$t_{d(CLKL-ADIV)}$	FEMC_CLK low to FEMC_AD[15:0] invalid	0	-	ns

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$t_{d(CLKL-Data)}$	FEMC_AD[15:0] valid after FEMC_CLK low	-	3	ns
$t_{d(CLKL-NBLH)}$	FEMC_CLK low to FEMC_NBL high	2	-	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid before FEMC_CLK high	3	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid after FEMC_CLK high	3	-	ns

Notes:

(1) IO drive capacity is 8 mA, Capacitive load = 30 pF

(2) Measurement point set at CMOS level: 0.5VDD

(3) t_{HCLK} >= 1/120MHz

NAND controller waveforms and timings

Figure 4-29 through **Figure 4-32** represent synchronous waveforms, and **Table 4-50** provides the corresponding timings. The results shown in these tables are obtained with the following FEMC configuration:

- COM.FEMC_SetupTime = 0x01; (Note: SET of FEMC_NCMEMTM, x = 2…3)
- COM.FEMC_WaitSetupTime = 0x03; (Note: WAIT of FEMC_NCMEMTMxx, x = 2…3)
- COM.FEMC_HoldSetupTime = 0x02; (Note: HLD of FEMC_NCMEMTMxx, x = 2…3)
- COM.FEMC_HiZSetupTime = 0x01; (Note: HIZ of FEMC_NCMEMTMxx, x = 2…3)
- ATT.FEMC_SetupTime = 0x01; (Note: SET of FEMC_NATTMEMTMx, x = 2…3)
- ATT.FEMC_WaitSetupTime = 0x03; (Note: WAIT of FEMC_NATTMEMTMx, x = 2…3)
- ATT.FEMC_HoldSetupTime = 0x02; (Note: HLD of FEMC_NATTMEMTMx, x = 2…3)
- ATT.FEMC_HiZSetupTime = 0x01; (Note: HIZ of FEMC_NATTMEMTMx, x = 2…3)
- Bank =FEMC_Bank_NAND;
- MemoryDataWidth = FEMC_NAND_BUS_WIDTH_16B; (Note: Memory data width = 16)
- ECC = FEMC_NAND_ECC_ENABLE; (Note: Enable ECC)
- ECCPageSize = FEMC_NAND_ECC_PAGE_512BYTES; (Note: ECC page size = 512 kB)
- TCLRSetupTime = 0; (Note: CRDLY of FEMC_NCTRLx)
- TARSetupTime = 0; (Note: ARDLY of FEMC_NCTRLx)

Figure 4-29 NAND Controller Waveforms For Read Access

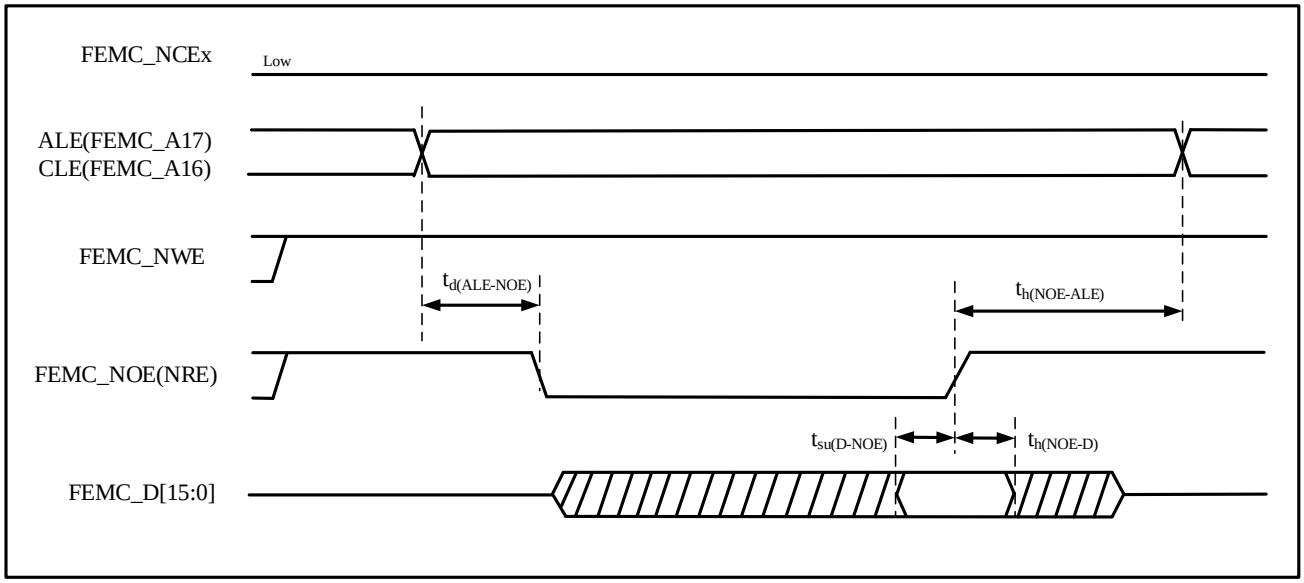

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Figure 4-30 NAND Controller Waveforms For Write Access

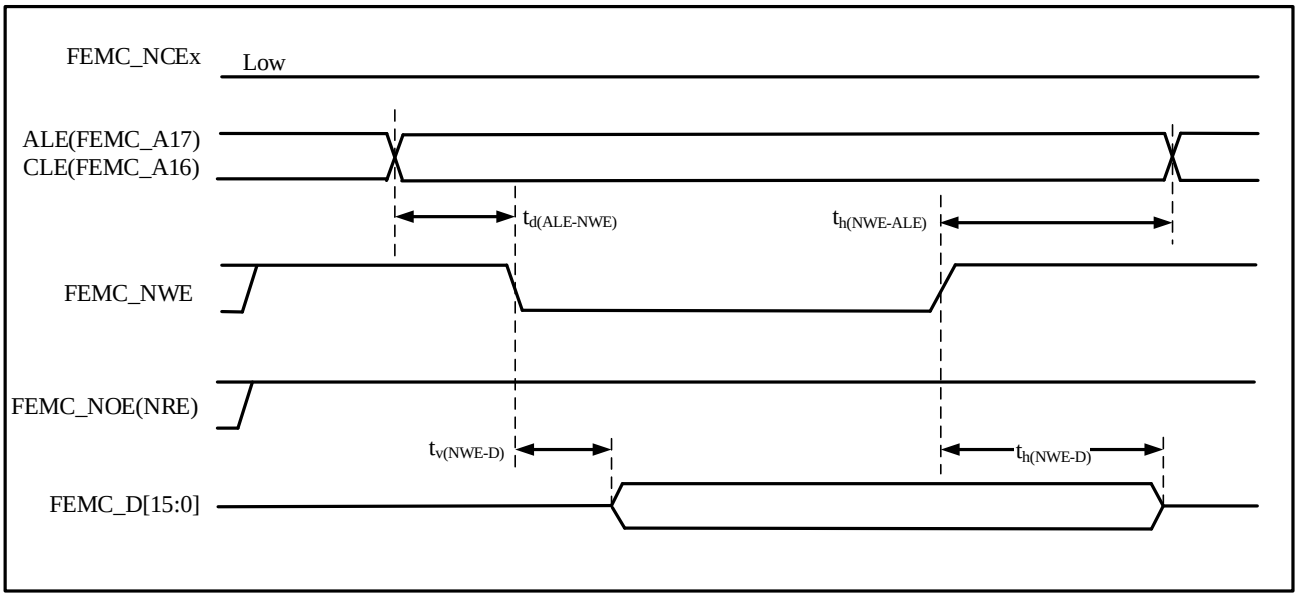

Figure 4-31 NAND Controller Waveforms For Common Memory Read Access

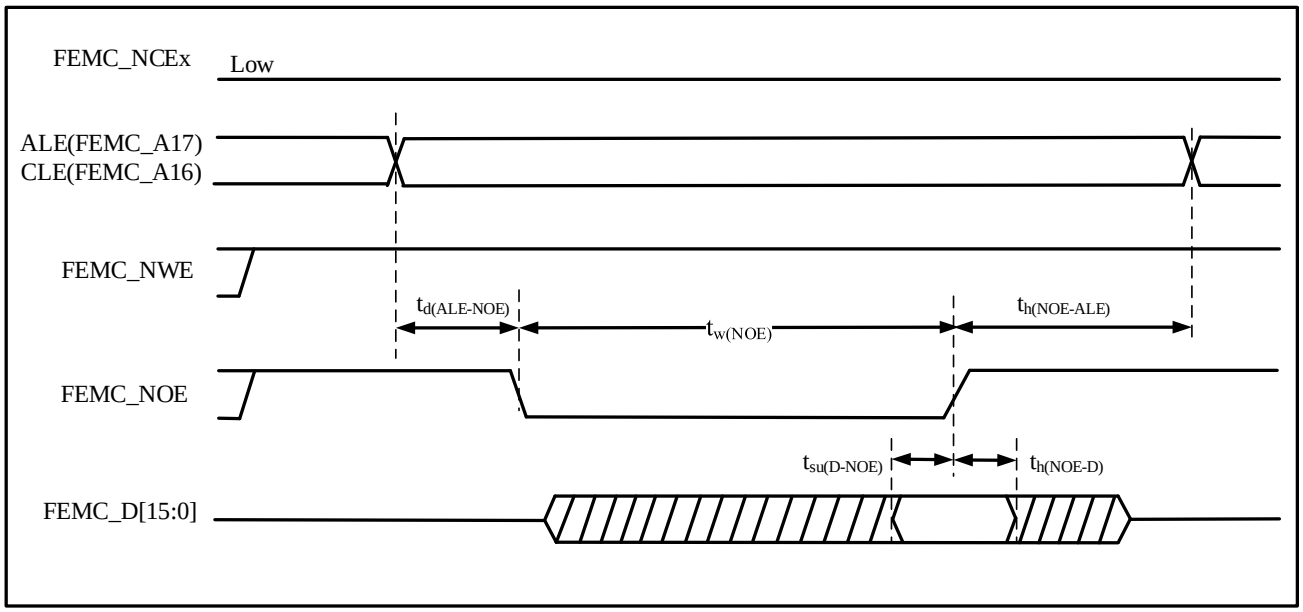

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Figure 4-32 NAND Controller Waveforms For Common Memory Write Access

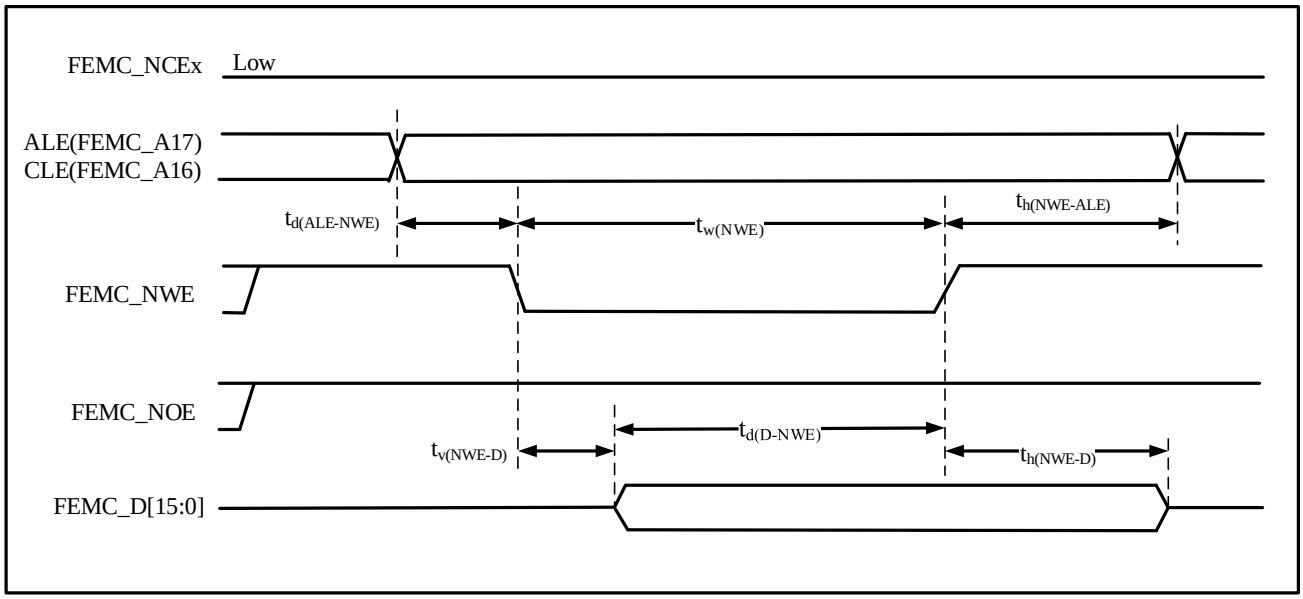

Table 4-50 Timing Characteristics Of NAND Flash Read/Write Cycles (1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$	Before FEMC_NWE high to FEMC_D[15:0] data valid	$5t_{HCLK}$ + 2	-	ns
$t_{w(NOE)}$	FEMC_NOE low time	$4t_{HCLK}$-1.5	$4t_{HCLK}$+1.5	ns
$t_{su(D-NOE)}$	Before FEMC_NOE high to FEMC_D[15:0] data valid	6	-	ns
$t_{h(NOE-D)}$	After FEMC_NOE high to FEMC_D[15:0] data valid	2	-	ns
$t_{w(NWE)}$	FEMC_NWE low time	$4t_{HCLK}$-1	$4t_{HCLK}$+1	ns
$t_{v(NWE-D)}$	FEMC_NWE low to FEMC_D[15:0] data valid	-	0	ns
$t_{h(NWE-D)}$	FEMC_NWE high to FEMC_D[15:0] data invalid	$2t_{HCLK}$ + 3	-	ns
$t_{d(ALE-NWE)}$	FEMC_NWE low to FEMC_ALE valid	-	$3t_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$	FEMC_NWE high to FEMC_ALE invalid	$3t_{HCLK}$ + 2	-	ns
$t_{d(ALE-NOE)}$	Before FEMC_NOE low to FEMC_ALE valid	-	$3t_{HCLK}$+ 2	ns
$t_{h(NOE-ALE)}$	FEMC_NOE high to FEMC_ALE invalid	$3t_{HCLK}$+ 3	-	ns

Note:

(1) Capacitive load = 15 pF.

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4.3.20 SDRAM Characteristics

Figure 4-33 SDRAM Read Timing Diagram

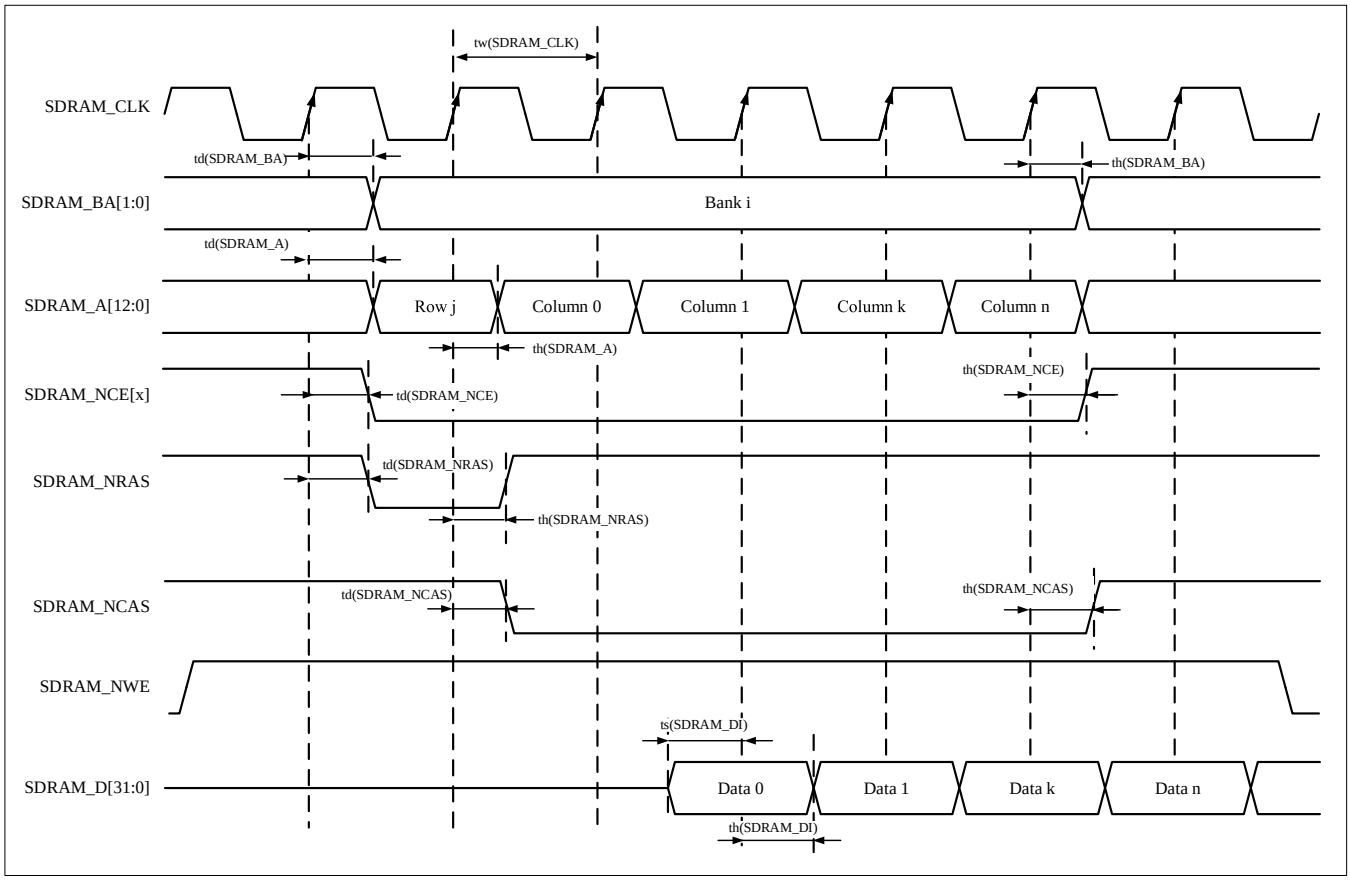

Table 4-51 SDRAM Read Timing (1)

Symbol	Parameter	Min	Max	Unit
t_w(SDRAM_CLK)	SDRAM_CLK Period	8.3(120M)	-	ns
t_d(SDRAM_BA)	Bank Address Valid Time	-	6.17	
t_h(SDRAM_BA)	Bank Address Hold Time	2.0	-	
t_d(SDRAM_A)	Address (Row/Column) Valid Time	-	6.17	
t_h(SDRAM_A)	Address (Row/Column) Hold Time	2.0	-	
t_d(SDRAM_NCE)	Chip Select Valid Time	-	6.17	
t_h(SDRAM_NCE)	Chip Select Hold Time	2.0	-	
t_d(SDRAM_NRAS)	SDRAM_NRAS Valid Time	-	6.17	
t_h(SDRAM_NRAS)	SDRAM_NRAS Hold Time	2.0	-	
t_d(SDRAM_NCAS)	SDRAM_NCAS Valid Time	-	6.17	
t_h(SDRAM_NCAS)	SDRAM_NCAS Hold Time	2.0	-	
t_s(SDRAM_DI)	Data Input Setup Time	-	3.0	
th(SDRAM_DI)	Data Input Hold Time	2.0	-	

(1) Guaranteed by design, not tested in production.

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Figure 4-34 SDRAM Write Timing Diagram

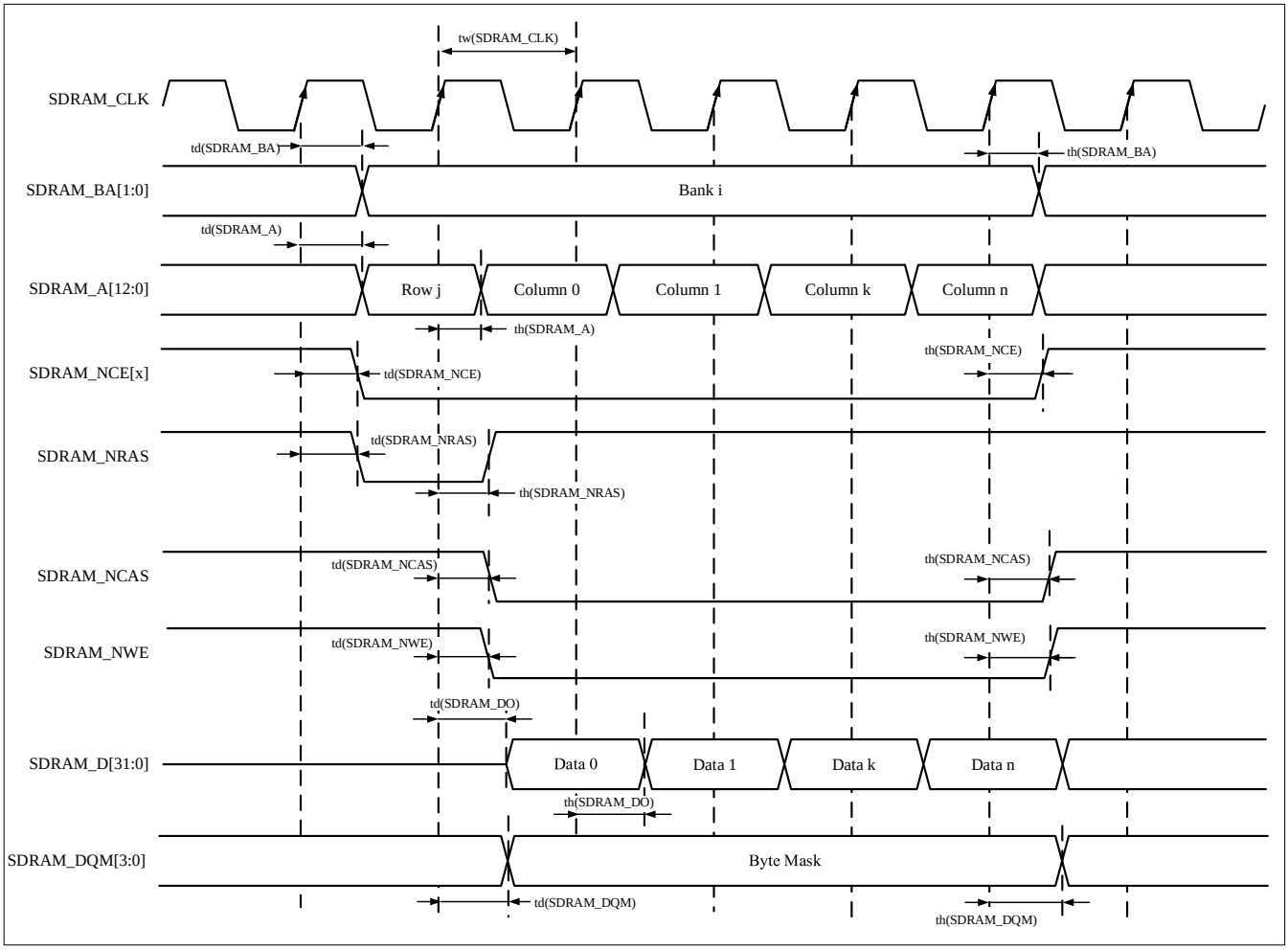

Table 4-52 SDRAM Write Timing (1)

Symbol	Parameter	Min	Max	Unit
t_w(SDRAM_CLK)	SDRAM_CLK Period	8.3(120M)	-	ns
t_d(SDRAM_BA)	Bank Address Valid Time	-	6.17	
t_h(SDRAM_BA)	Bank Address Hold Time	2.0	-	
t_d(SDRAM_A)	Address (Row/Column) Valid Time	-	6.17	
t_h(SDRAM_A)	Address (Row/Column) Hold Time	2.0	-	
t_d(SDRAM_NCE)	Chip Select Valid Time	-	6.17	
t_h(SDRAM_NCE)	Chip Select Hold Time	2.0	-	
t_d(SDRAM_NRAS)	SDRAM_NRAS Valid Time	-	6.17	
t_h(SDRAM_NRAS)	SDRAM_NRAS Hold Time	2.0	-	
t_d(SDRAM_NCAS)	SDRAM_NCAS Valid Time	-	6.17	
t_h(SDRAM_NCAS)	SDRAM_NCAS Hold Time	2.0	-	
t_d(SDRAM_NWE)	Write Enable Valid Time	-	6.17	
t_h(SDRAM_NWE)	Write Enable Hold Time	2.0	-	
t_d(SDRAM_DO)	Data Output Valid Time	-	3.0	
t_h(SDRAM_DO)	Data Output Hold Time	2.0	-	
t_d(SDRAM_DQM)	Output Byte Mask Valid Time	-	6.17	
t_h(SDRAM_DQM)	Output Byte Mask Hold Time	2.0	-	

(1) Guaranteed by design, not tested in production.

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4.3.21 DSMU Characteristics

Unless otherwise specified, the Parameters in Table 4-53 are measured under the environmental conditions (ambient temperature 25 °C, fHCLK frequency, and VDD supply voltage) conforming to Table 4-4. Additional test conditions are as follows:

- Port switching speed configuration: DSy[1:0] = 2b10, SRy = 1b0
- Load capacitance CL = 30 pF
- Reference CMOS level standards, I/O measurement point at 0.5 VDD

For more details on the characteristics of ports (DSMU_CKINx, DSMU_DATINx, DSMU_CKOUT), please refer to the I/O Port Characteristics section 4.3.12.

Table 4-53 DSMU Timing Parameters

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{DSMU} ($1/T_{DSMU}$)	DSMU clock	2.3V < VDD < 3.63V		-	-	240	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		-	-	20	
		2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), internal clock mode (SPICLKSEL[1:0] ≠ 0)		-	-	20	
f_{CKOUT}	Output clock frequency	2.3V < VDD < 3.63V		-	-	20	
$Duty_{CKOUT}$	Output clock duty cycle	2.3V < VDD < 3.63V	Even division CKOUTDIV = n(1,3,5…)	45	50	55	%
			Odd division CKOUTDIV = n(2,4,6…)	(((n/2+1)/(n+1)) *100)-5	((n/2+1)/(n+1)) *100	(((n/2+1)/(n+1)) *100)+5	
t_{wh}(CKIN) t_{wl}(CKIN)	Input clock high/low pulse width	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		-	Tclk/2	-	ns
t_{su}	Input data setup time	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		3.5	-	-	
t_h	Input data hold time	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		4.3	-	-	
$T_{Manchester}$	Manchester data period (self-recovery clock period)	2.3V < VDD < 3.63V, Manchester interface (SITP[1:0] = 2,3), internal clock mode (SPICLKSEL[1:0] ≠ 0)		(CKOUTDIV+1) *$T_{DSMUCLK}$	-	(2*CKOUTDIV) *$T_{DSMUCLK}$	

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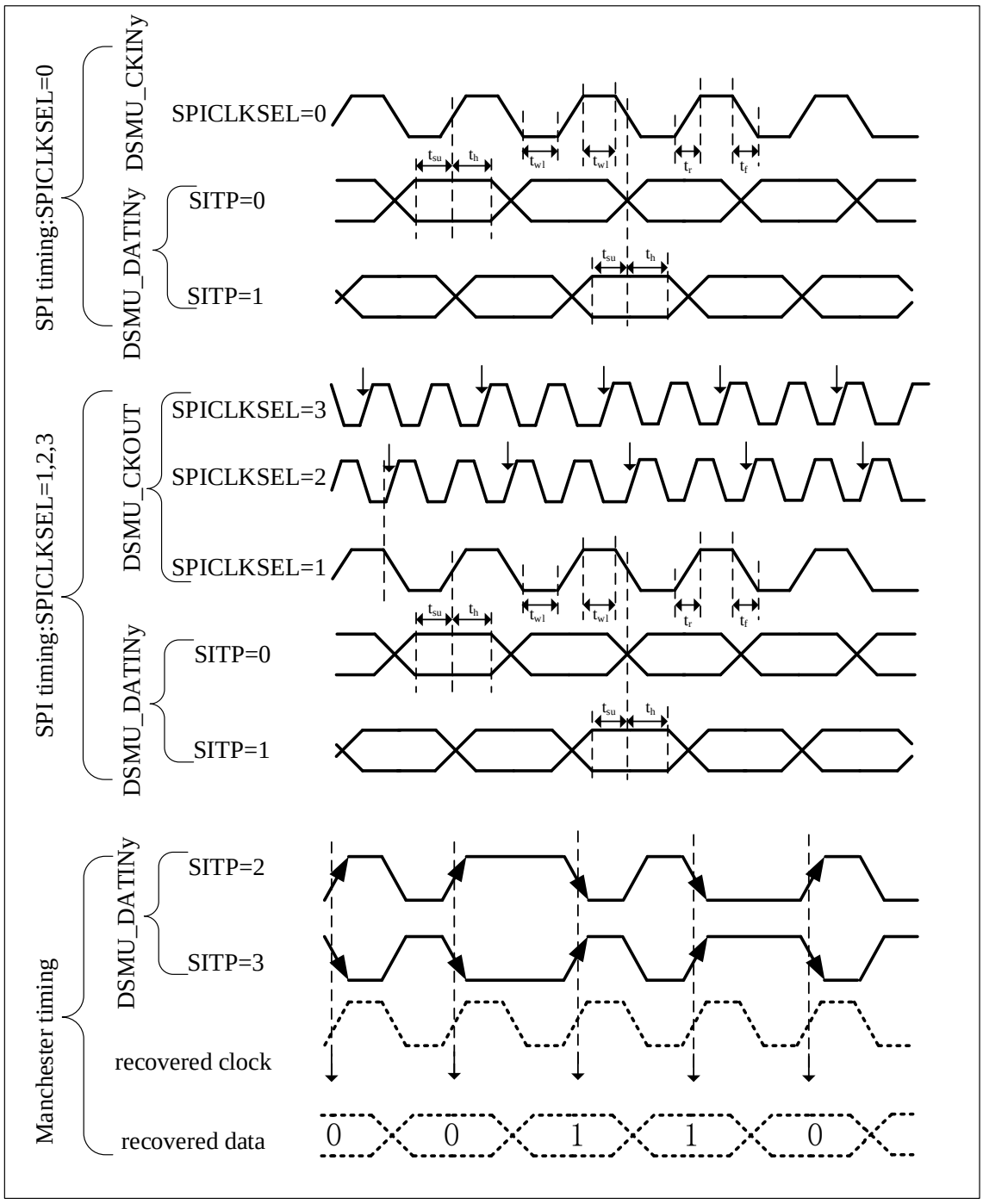
Figure 4-35 DSMU Channel Transceiver Timing Diagram



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4.3.22 USB_FS_Device Characteristics

USB (full speed) interface is certified by the USB-IF.

Table 4-54 USBFS Startup Time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 4-55 USBFS DC Characteristics

Symbol	Parameter	Condition	Min (1)	Max (1)	Unit
Input level					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I (USBDP and USBDM)	0.2	-	V
V_{CM}(4)	Differential common model range	Contains V_{DI} ranges	0.8	2.5	
V_{SE}(4)	Single-end receiver threshold	-	1.3	2.0	
Output level					
V_{OL}	Static output low level	1.5KΩ RL is connected to 3.6V(5) (6)	-	0.3	V
V_{OH}	Static output high level	15KΩ RL is connected to V_{SS}(6)	2.8	3.6	

Notes:

(1) All voltage measurements are based on the ground cable at the device end.

(2) USB operating voltage is 3.0~3.6V in order to be compatible with USB2.0 full speed electrical specification.

(3) The correct USB function of the N32H497 series products can be guaranteed at 2.7V, instead of dropping the electrical characteristics in the 2.7-3.0V voltage range.

(4) Based on comprehensive evaluation, not tested in production.

(5) The chip has a built-in 1.5kΩ pull-up resistor, which is optional for the user.

(6) R_L is the load attached to the USB drive.

Figure 4-36 USB Timing: Definition Of Rise And Fall Time Of Data Signal

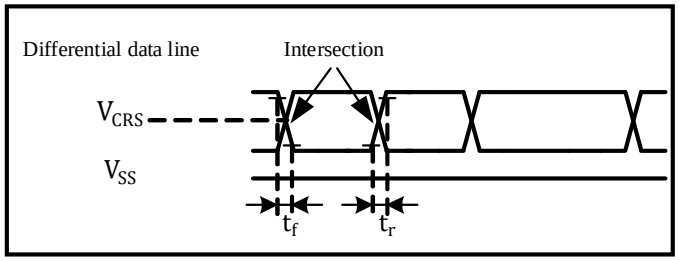

Table 4-56 Full Speed Of USB Electrical Characteristics

Symbol	Parameter	Condition	Min (1)	Max (1)	Unit
t_r	Rise time(2)	CL ≤ 50pF	4	20	ns
t_f	Fall time(2)	CL ≤ 50pF	4	20	ns
t_{rfm}	Rise and fall times match	t_r / t_f	90	110	%
V_{CRS}	Output signal crosstalk(3)	-	1.3	2.0	V

Notes:

(1) Guaranteed by design, not tested in production.

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(2) Measured data signal from 10% to 90%.For more details, see Chapter 7 (version 2.0) of the USB specification.

(3) External terminal series resistors are not required on USB_PD (D+) and USB_DM (D-); matching impedance is included in the embedded driver.

4.3.23 USB_HS_Host/Device Characteristics

Table 4-57 USBHS DC Electrical Characteristics

Symbol		Parameter	Condition	Min	Typ	Max	Unit
VDD (1)		USB operating voltage	-	3	-	3.6	V
LS/FS FUNCTIONALITY							
Input levels(1)	VDIFS	Differential input sensitivity (FS/LS)	-	0.2	-	-	V
	VCMFS	Differential common mode range (FS/LS)	Includes V_{DI} range	0.8	-	2.5	
	VILSE	Single ended receive low voltage(FS/LS)	-	-	-	0.8	
	VIHSE	Single ended receive high voltage(FS/LS)	-	2.0	-	-	
Output levels(1)	VOLFS	Static output level low (FS/LS)	RL of 1.5kΩ to 3.6V	-	-	0.3	
	VOHFS	Static output level high (FS/LS)	RL of 15 kΩ to VSS	2.8	3.3	3.6	
RPD(1)		USBHS_DM/DP	VIN = VDD	-	15	-	kΩ
RPU(1)		USBHS_DM/DP	VIN = VSS	-	1.5	-	
ZHSDRV(1)		Driver output impedance	Steady-state driving	-	45	-	Ω
HS FUNCTIONALITY							
Input levels(1)	DIHS	Differential input sensitivity (HS)	-	0.1	-	-	V
	VCMHS	Differential common mode range (HS)	-	-50	-	500	mV
	VHSSQ	HS overshoot detection threshold	-	100	-	150	
	VHSDSC	HS dropout threshold	-	525	-	625	
Output levels(1)	VOLHS	High-speed low-level output voltage	45Ω	-10	-	10	
	VOHHS	High-speed high-level output voltage	45Ω	360	400	440	

Notes:

(1) Guaranteed by design, not tested in production.

Table 4-58 USB Dynamic Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{FR}	Rising time (FS/LS)	C_L = 50 pF	4	-	20	ns
T_{HSR}	Differential rising time (HS)	-	500	-	-	ps
T_{FF}	Falling time (FS/LS)	C_L = 50 pF	4	-	20	ns
T_{HSF}	Differential falling time (HS)	-	500	-	-	ps
v_{CRS}	Output single-ended crosstalk voltage (FS/LS)	-	1.3	-	2	V

Notes:

(1) Guaranteed by design, not tested in production.

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4.3.24 Controller Area Network (CAN) Interface Characteristics

See Section 4.3.12 for details on the features of the input/output alternate function pins (CAN_TX and CAN_RX).

4.3.25 SDIO Interface Characteristics

Unless otherwise specified, the parameters listed in **Table 4-59** are measured under the conditions of environmental temperature, f_{PCLKx} frequency, and V_{DD} supply voltage as specified in**Table 4-4**. For details on the characteristics of the input/output multiplexed function pins (D[7:0], CMD, CK), refer to section 4.3.12.

Figure 4-37 SDIO High Speed Mode

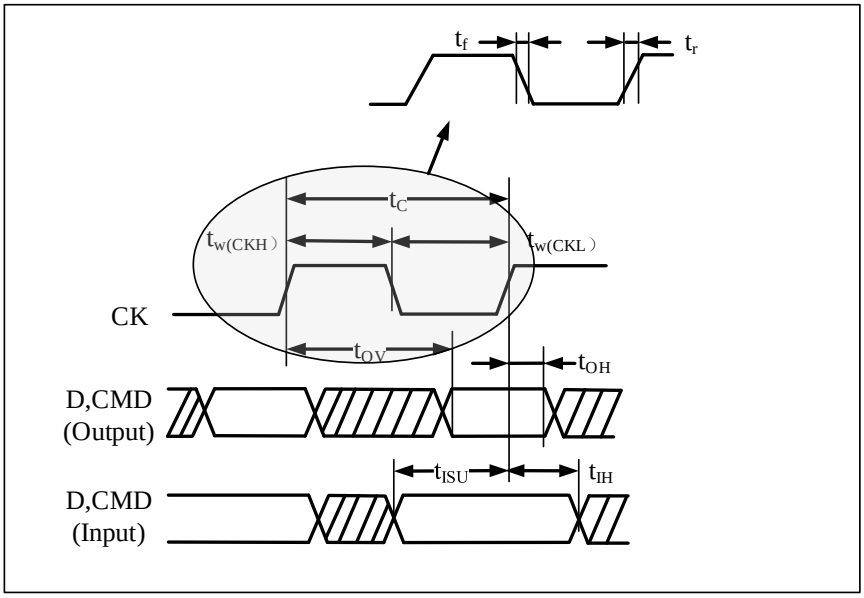

Figure 4-38 SDIO Default Mode

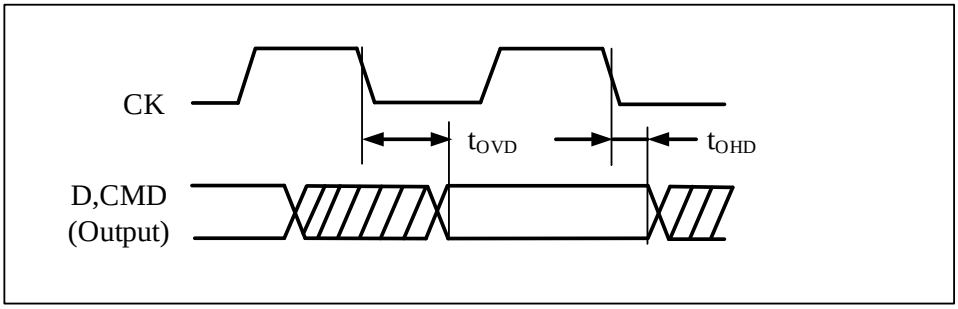

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Table 4-59 SD/MMC Interface Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	CL ≤ 30pF	0	50	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 48MHz	CL ≤ 30pF	8.5	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 48MHz	CL ≤ 30pF	6	-	
t_r	Clock rising time	CL ≤ 30pF	-	5	
t_f	Clock falling time	CL ≤ 30pF	-	5	
CMD、D inputs(referenced to CK)					
t_{ISU}	Input setup time	CL ≤ 30pF	5	-	ns
t_{IH}	Input hold time	CL ≤ 30pF	1	-	
CMD、D outputs in MMC and SD HS mode (referenced to CK)					
t_{OV}	Output valid time	CL ≤ 30pF	-	6	ns
t_{OH}	Output hold time	CL ≤ 30pF	0	-	
CMD、D outputs in SD default mode (referenced to CK)					
t_{OVD}	Output valid default time	CL ≤ 30pF	-	7	ns
t_{OHD}	Output hold default time	CL ≤ 30pF	0.5	-	

Note:

(1) Refer to SDIO_CLKCR, the SDI clock control register, to control the CK output.

4.3.26 Ethernet Interface Characteristics

Table 4-60 shows the Ethernet operating voltages.

Table 4-60 Ethernet DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}	Ethernet operating voltage	3.0	3.6	V

Note:

(1) All voltage measurements are referenced to the device ground.

Table 4-61 provides the SMI signal list for the Ethernet MAC, and **Figure 4-39** shows the related timing.

Figure 4-39 Ethernet SMI Timing Diagram

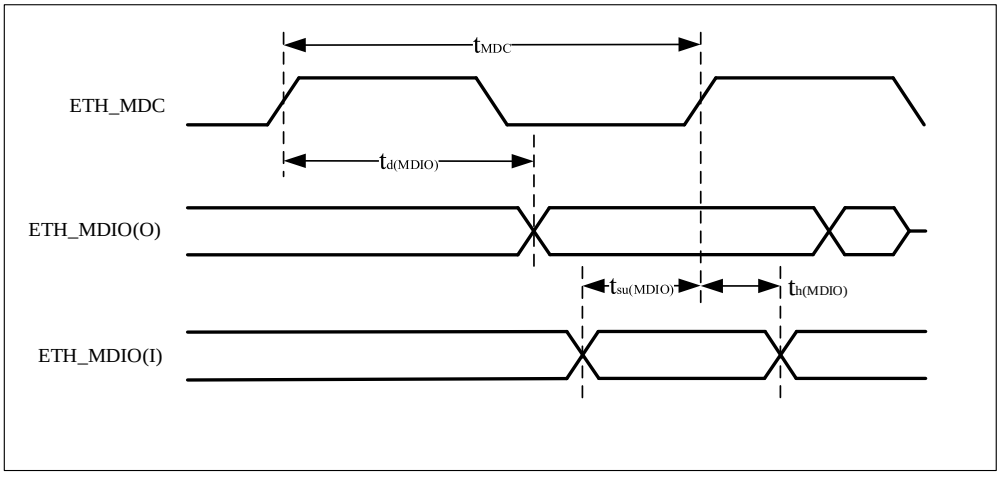

Table 4-61 Ethernet SMI Signal Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC clock period time (2.35MHz)	420	425	430	ns
$t_{d(MDIO)}$	MDC write data valid time	6	10	13	ns
$t_{su(MDIO)}$	Read data setup time	12	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

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Table 4-62 shows the RMII signals for the Ethernet MAC, and **Figure 4-40** displays the relevant timing.

Figure 4-40 Ethernet RMII Timing Diagram

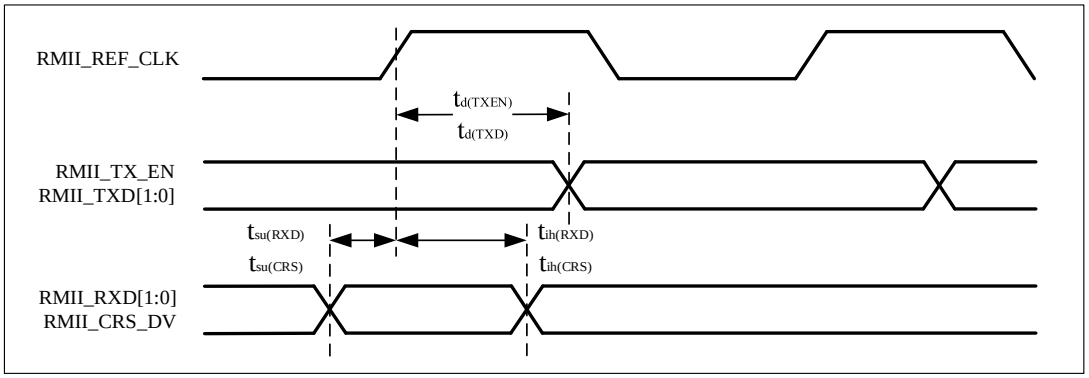

Table 4-62 Ethernet RMII Signal Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	3.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2.6	-	-	ns
$t_{su(CRS)}$	Carrier sense setup time	3.5	-	-	ns
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	5.5	6.5	12	ns
$t_{d(TXD)}$	Transmit data valid delay time	6	6.5	12	ns

Table 4-63 shows the MII signals for the Ethernet MAC, and **Figure 4-41** displays the relevant timing.

Figure 4-41 Ethernet MII Timing Diagram

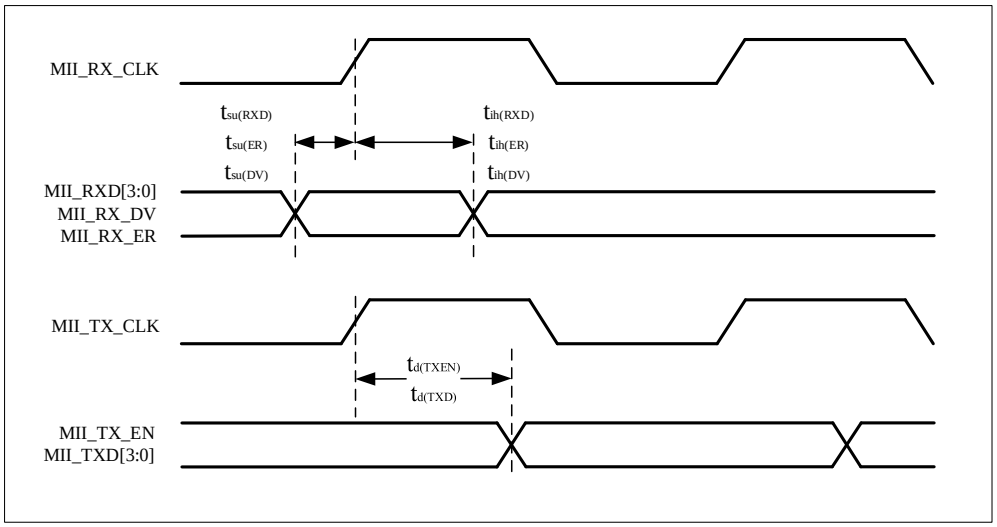

Table 4-63 Ethernet MII Signal Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	10	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	10	-	-	ns
$t_{su(DV)}$	Carrier sense setup time	10	-	-	ns
$t_{ih(DV)}$	Carrier sense hold time	10	-	-	ns
$t_{su(ER)}$	Error setup time	10	-	-	ns
$t_{ih(ER)}$	Error hold time	10	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	0	10	14	ns
$t_{d(TXD)}$	Transmit data valid delay time	0	10	14	ns

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4.3.27 Digital Video Port (DVP) Interface Characteristics

Table 4-64 shows the characteristics of the DVP interface signals, and **Figure 4-42** displays the relevant timing.

Figure 4-42 Ethernet MII Timing Diagram

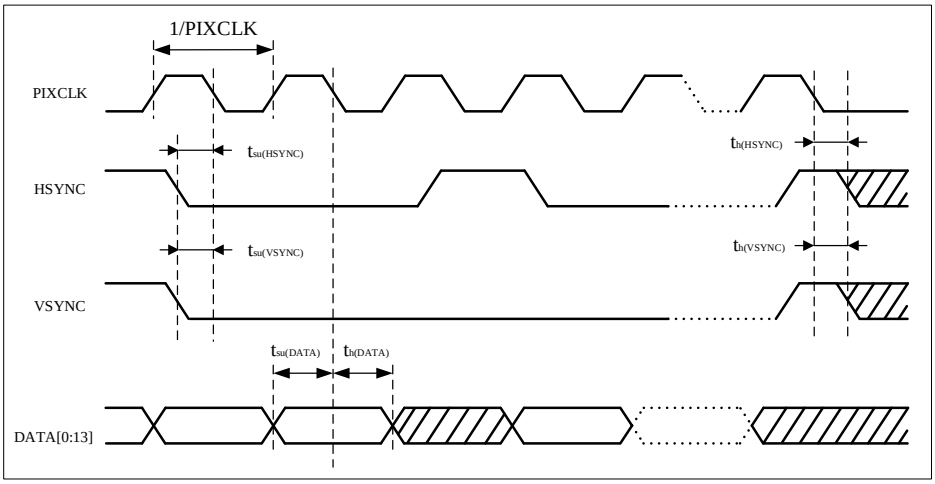

Table 4-64 Dynamic Characteristics Of DVP Signals

Symbol	Parameter	Min	Typ	Max	Unit
PCLK	Pixel clock input	-	0	60	MHz
Dpixel	Pixel clock input duty cycle	-	30%	70%	-
$t_{su(DATA)}$	Data input setup time	-	5	-	ns
$t_{h(DATA)}$	Data hold time	-	2.5	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	HSYNC/VSYNC input setup time	-	5	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	HSYNC/VSYNC input hold time	-	2.5	-	

4.3.28 Electrical Parameters of 12 bit Analog-to-Digital Converter (ADC)

Unless otherwise specified, the parameters in **Table 4-65** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Note: It is recommended to perform a calibration at each power-on.

Table 4-65 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	The power supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	-	-	80	MHz
f_s	Sampling rate(1)	VDDA ≥ 2.4V	-	-	4.7	Msps
		1.8V ≤ VDDA < 2.4V	-	-	4	
V_{AIN}	Switching voltage range(2)	-	0 (V_{SSA} or V_{REF-} Connect to ground)	-	V_{REF+}	V
R_{ADC}	Sampling switch resistance	2.4~3.3V	-	-	300	ohm
		1.8~2.4V	-	-	480	
C_{ADC}	Internal sampling and holding capacitors	-	-	5	-	pF
SNDR	Singal noise distortion ration	-	-	65	-	dBFS
T_{cal}	The calibration time	-	82			$1/f_{ADC}$
t_S	Sampling time	fADC = 80 MHz(fast channel)	0.0563	-	7.52	μs

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Symbol	Parameter	Condition	Min	Typ	Max	Unit
		fADC = 80 MHz(slow channel)	0.0625		8.35	
Ts(1)	Sampling cycles	fADC = 80 MHz(fast channel)	0.0938	-	7.52	1/f_{ADC}
		fADC = 80 MHz(slow channel)	4.5	-	601.5	
Ts	Power on time	-	4.5	-	601.5	μs
t_{CONV}(2)	Total conversion time (including sampling time)	-	8~614 (Sampling T_S + 6.5/8.5/10.5/12.5 for successive approximation)			1/f_{ADC}

Notes:

(1) Guaranteed by design, not tested in production.

(2) According to different packages, V_{REF+} connected to V_{DDA} internally, and V_{REF-} connected to V_{SSA} internally.

(3) Sampling time/sampling rate is related to the input impedance Rin. The correspondence between the maximum input impedance Rin and the sampling time is shown in Table 4-66.

Table 4-66 ADC Sampling Time(1)

Resolution	Rin（kΩ）	Minimum Sampling Time (ns)			
		Vdda=2.4V to 3.6V , Vddd=1.1 V, selrange_ldo=L, Tjunction=125℃, fclk=80 MHz		Vdda=1.8V to 2.4V, Vddd=1.1 V, selrange_ldo=L, Tjunction=125℃, fclk=80 MHz.	
		Fast Channel	Slow Channel	Fast Channel	Slow Channel
12-bit	0.14	45.0	73.0	79.0	103.0
	0.6	79.0	103.0	300.0	345.0
	4.6	300.0	345.0	576.0	651.0
	9.5	576.0	651.0	1131.0	1257.0
	19	1131.0	1257.0	2776.0	3051.0
	48	2776.0	3051.0	5475.0	5982.0
10-bit	0.14	39.0	61.0	64.0	88.0
	0.6	64.0	88.0	250.0	357.0
	4.6	250.0	357.0	478.0	540.0
	9.5	478.0	540.0	935.0	1040.0
	19	935.0	1040.0	2294.0	2526.0
	48	2294.0	2526.0	4532.0	4963.0
8-bit	0.14	33.0	50.0	52.0	71.0
	0.6	52.0	71.0	202.0	234.0
	4.6	202.0	234.0	391.0	457.0
	9.5	391.0	457.0	800.0	1012.0
	19	800.0	1012.0	1838.0	2027.0
	48	1838.0	2027.0	3632.0	3984.0
6-bit	0.14	27.0	40.0	41.0	56.0
	0.6	41.0	56.0	153.0	177.0
	4.6	153.0	177.0	292.0	330.0
	9.5	292.0	330.0	569.0	642.0
	19	569.0	642.0	1435.0	1666.0
	48	1435.0	1666.0	3001.0	3919.0

Notes:

(1) Guaranteed by design, not tested in production.

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Table 4-67 ADC Accuracy-Limited Test Conditions [1] [2]

Symbol	Parameter	Condition	Typ	Max [3]	Unit
ET[4]	Comprehensive error	f_{HCLK} = 240MHz, f_{ADC} = 240MHz, sample Rate = 1.75M SPS, V_{DDA} = 3.3V, T_A = 25 ℃ Measurements are made after the ADC is calibrated $V_{REF+} = V_{DDA}$	1.3	5	LSB
EO[4]	Offset error		1	3	
ED	Differential linear error		1	2.2	
EL	Integral linear error		2	3	

Notes:

(1) The DC accuracy of the ADC is measured after internal calibration.

(2) ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin.It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current.

*(3) The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in **Table 4-2***

(4) Based on comprehensive evaluation, not tested in production.

Figure 4-43 ADC Precision Characteristics

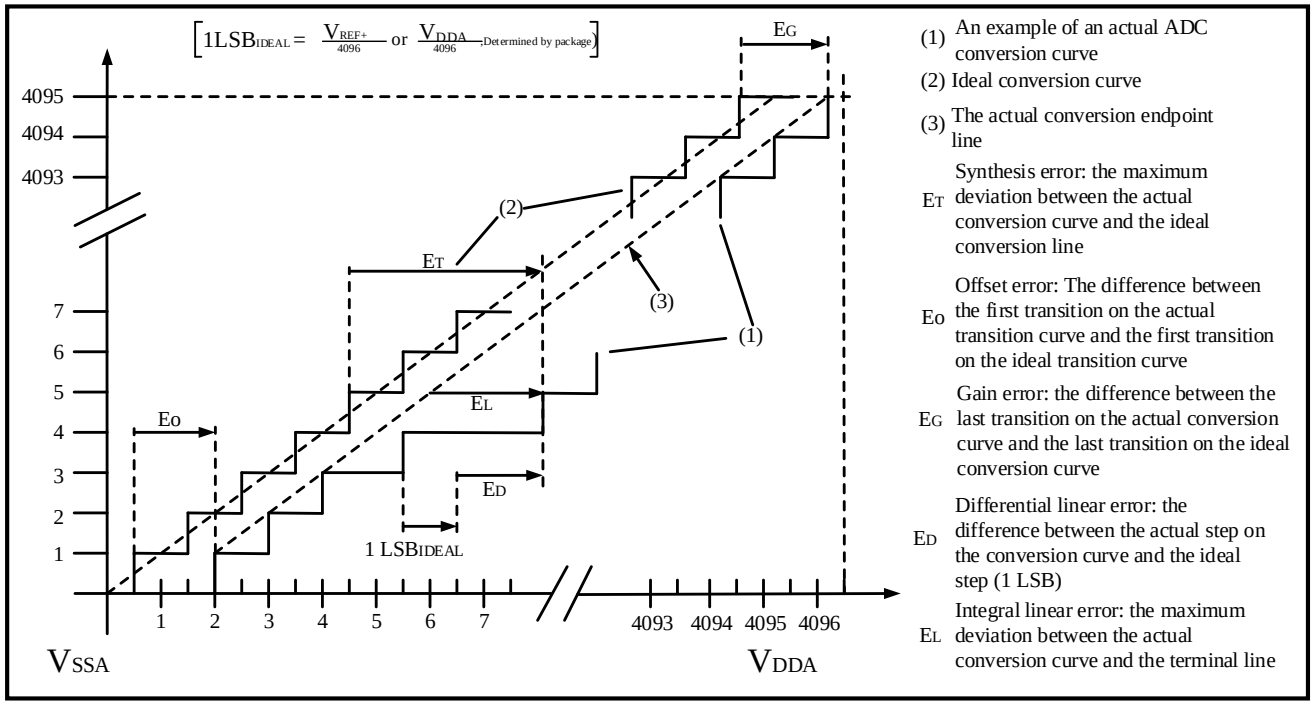

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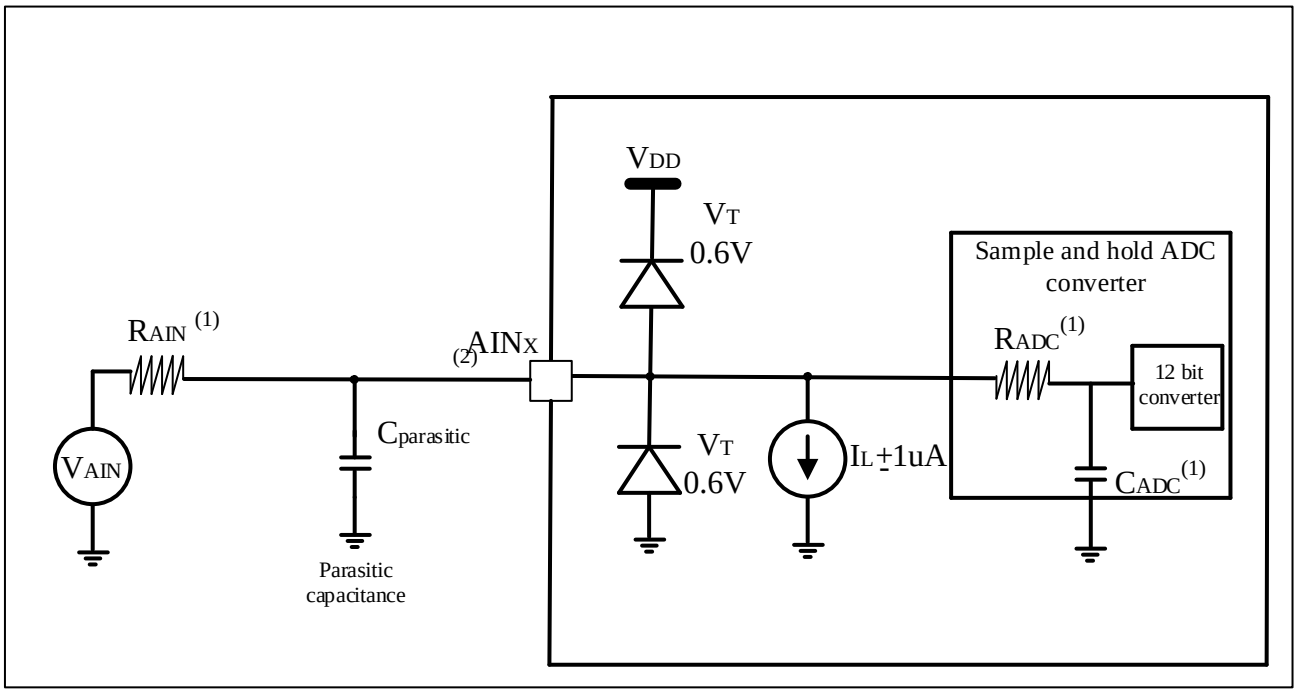
Figure 4-44 Typical Connection Diagram Using ADC



Notes:

(1) For values of R_{AIN}, R_{ADC}, and C_{ADC}, see Table 4-65.

(2) $C_{parasitic}$ indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF).A larger $C_{parasitic}$ value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC} from medine.

4.3.29 12-bit DAC Electrical Parameters

Unless otherwise specified, the parameters of **Table 4-68** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions of **Table 4-4**.

Table 4-68 DAC 1MSPS Characteristics(1)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	DAC output buffer disabled, output only internally connected		2.4	-	3.6	V
V_{REF+}	Positive reference voltage	DAC output buffer disabled, output only internally connected		2.4	-	VDDA	
V_{REF-}	Negative reference voltage	-		VSSA			
R_L	Resistive load with buffer enable	DAC output Buffer enable	Connected to VSSA	5	-	-	kΩ
			Connected to VDDA	25	-	-	
Ro	Impedance output	DAC output buffer disable		10.3	12.3	15.7	kΩ
C_L	Capacitive load	-		-	-	50	pF
DAC_OUT	DAC_OUT output voltage	Output buffer enable		0.2	-	V_{REF+} - 0.2	V
		Output buffer disable		0	-	V_{REF+}	-
I_{DD}	Static mode (standby mode)	-		-	180	230	μA

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	DAC DC consumption ($V_{DDD+}V_{DDA+}V_{REF+}$)	-	-	400	610	μA
$t_{SETTLING}$	Settling time (full range: 12-bit input code transitioning from minimum value to maximum value, DAC_OUT reaching its final value within ±1 LSB)	DAC buffer enable, CL ≤ 50 pF,RL ≥ 5 kΩ	-	3	4.1	μs
		DAC buffer disable	-	2.1	2.6	
t_{WAKEUP}	Wake-up time from shutdown state (from enabling DAC to DAC_OUT reaching its final value within ±1 LSB)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ	-	4	7	μs
		DAC buffer disable, CL ≤ 10 pF	-	2	4	
PSRR	Power supply rejection ratio (relative to $V_{DD}33A$) (static DC measurement)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ	-	-85	-30	dB
TW_to_W	The minimum time between two consecutive writes to the DACx_DATO register to ensure that small changes in the input code result in the correct DAC_OUT(1 LSB)。DACxy_CTRL.EXOUT = 1, DACxy_CTRL. BxEN = 1	CL ≤ 50 pF, RL ≥ 5 kΩ	1	-	-	μs
	DACxy_CTRL.EXOUT = 1, DACxy_CTRL. BxEN = 0 or DACxy_CTRL.INOUT = 1, DACxy_CTRL. BxEN = 0	CL ≤ 10 pF	1.4	-	-	
Voffset	Middle code offset for 1 trim code step	VREF+ =3.6V	-	-	1500	μV
$I_{DDA(DAC)}$	DAC consumption from VDDA	DAC buffer enable, No load, input mid-value 0x800	-	250	400	μA
		DAC buffer enable, No load, input max-value 0xF1C	-	450	670	
		DAC buffer disable, No load, input mid-value 0x800	-	-	0.25	
$I_{DDV(DAC)}$	DAC consumption from VREF+	DAC buffer enable, No load, input mid-value 0x800	-	180	240	μA
		DAC buffer enable, No load, input max-value 0xF1C	-	320	400	
		DAC buffer disable, No load, input mid-value 0x800	-	155	200	
DNL	Nonlinear distortion (deviation between two consecutive codes)	-	-2	-	+2	LSB
INL	Nonlinear accumulation (deviation measured at code i from the line connecting code 0 and code 4095)	-	-6	-	+6	LSB
Offset	Offset error (value measured at code 0x800)	Output buffer enable,CL ≤ 50 pF,RL ≥ 5 kΩ, VREF+ =3.6V	-16	-	+8	LSB
		Output buffer enable,CL ≤ 50 pF,RL ≥ 5 kΩ, VREF+ =1.8V	-20	-	+20	
		Output buffer disable,CL ≤ 50 pF, noRL	-8	-	+6	
Gain Error	Gain error	-	-	±0.5	-	%

(1) Guaranteed by design, not tested in production.

4.3.30 Voltage Reference Buffer (VREFBUF) Characteristics

Unless otherwise specified, the parameters in **Table 4-69** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4.**

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Table 4-69 VREFBUF Characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V_{REFBUF_OUT}	Voltage reference output	VRS= 00，T_A=25℃	2.044	2.048	2.052	
		VRS= 01，T_A=25℃	2.496	2.5	2.504	
		VRS= 10，T_A=25℃	2.896	2.9	2.904	
TRIM	Trim step resolution	-	-	±0.05	±0.1	%
CL	Load capacitor	-	0.5	1	2	μF
PSRR	Power supply rejection	DC	48.9	74.7	-	dB
		100KHz	25	40	-	
t_{START}	Start-up time	CL =1 μF	-	500	650	μs
$I_{DDA(VREFBUF)}$	VREFBUF consumption from VDDA	Iload <= 10 mA	-	45	80	μA

Note: (1)Guaranteed by design, not tested in production.

4.3.31 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in **Table 4-70** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Table 4-70 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±3	℃
Avg_Slope(1)	Average slope	-3.7	-4	-4.3	mV/℃
V_{25}(1)	Voltage at 25℃	-	1.32	-	V
t_{START}(1)	Startup time	4	-	10	μs
T_{S_temp}(2)(3)	ADC sampling time when reading the tempearture	-	-	3	μs

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Shortest sampling time can be determined in the application by multiple iterations.

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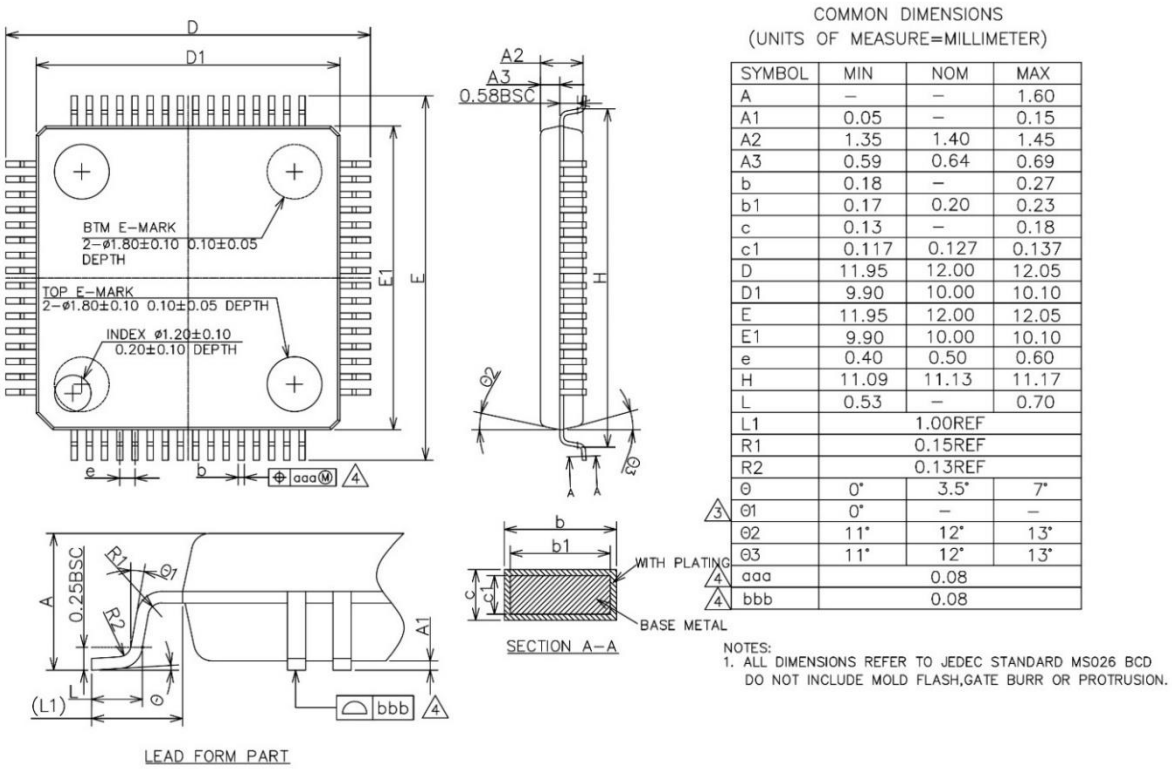
5 Packages

5.1 LQFP64

Figure 5-1 LQFP64 Package Dimensions

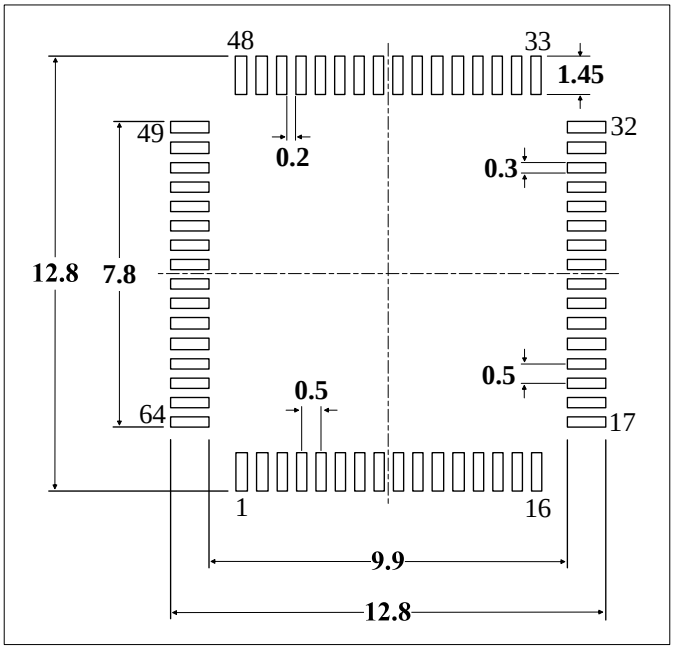


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
3 θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°
4 aaa	0.08		
4 bbb	0.08		

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

Figure 5-2 LQFN64 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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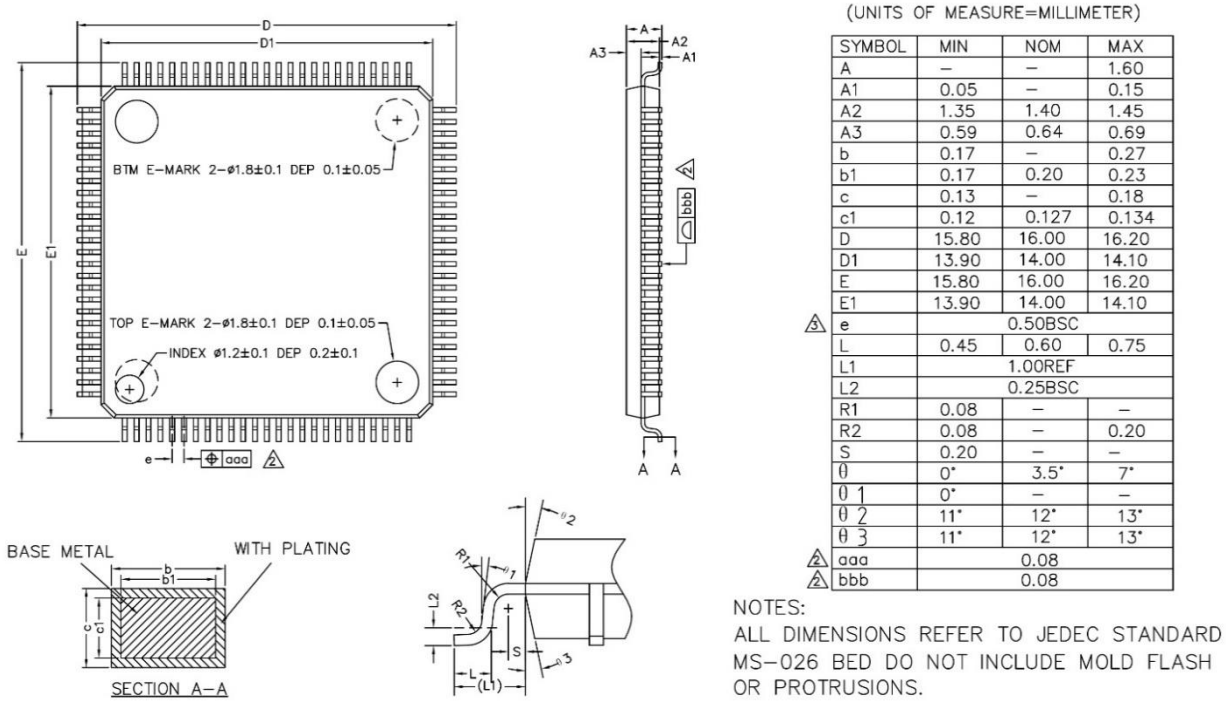
5.2 LQFP100/LQFP100-2

Figure 5-3 LQFP100/LQFP100-2 Package Dimensions

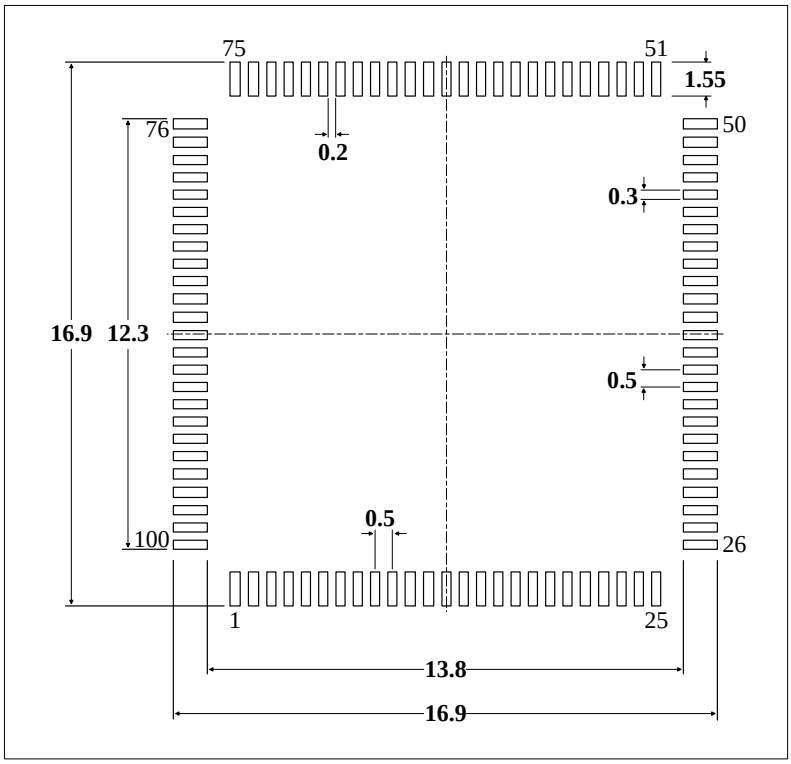


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
3 e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°
2 aaa		0.08	
2 bbb		0.08	

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BED DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 5-4 LQFN100/LQFP100-2 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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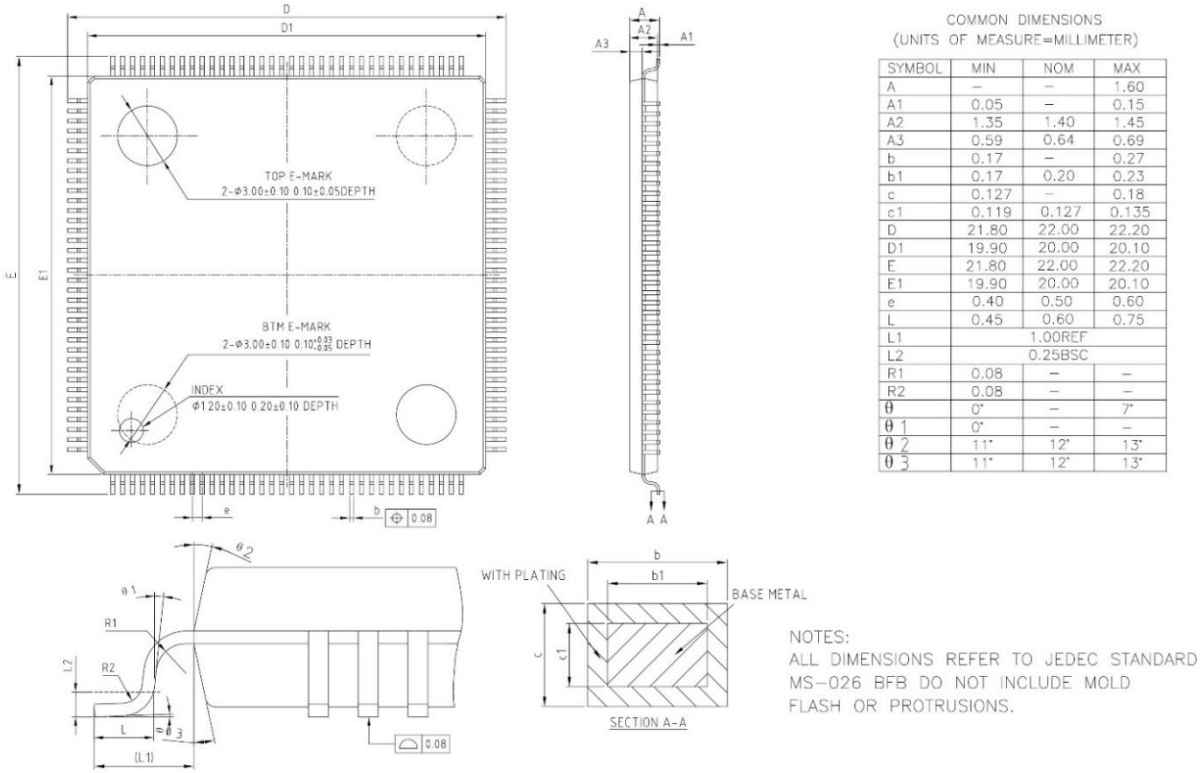
5.3 LQFP144

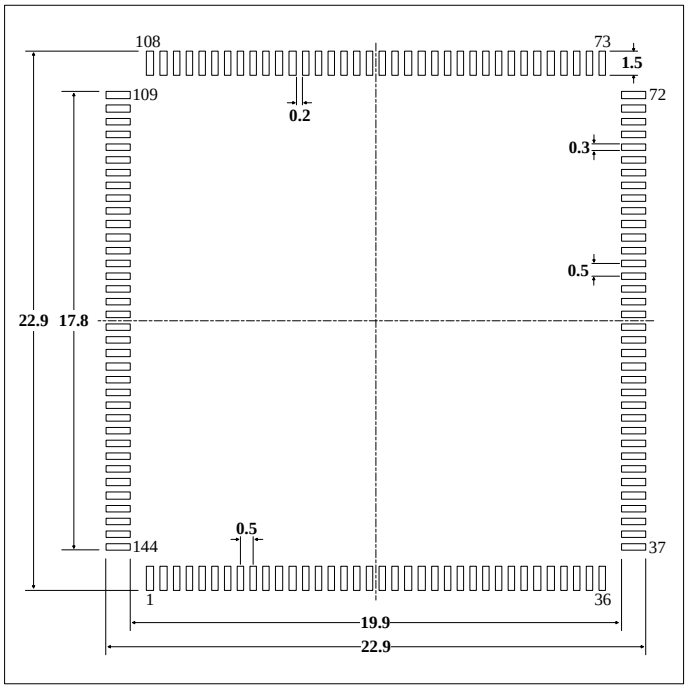
Figure 5-5 LQFP144 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.127	–	0.18
c1	0.119	0.127	0.135
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	–
θ	0°	–	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

Figure 5-6 LQFN144 Recommended Footprint(1)



1. Dimensions are expressed in millimeters

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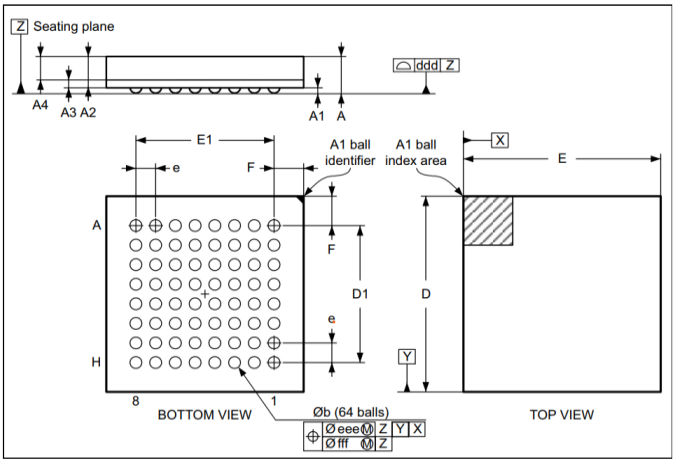
5.4 BGA64

Figure 5-7 BGA64 Package Dimensions



Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

Figure 5-8 BGA64 Recommended Footprint

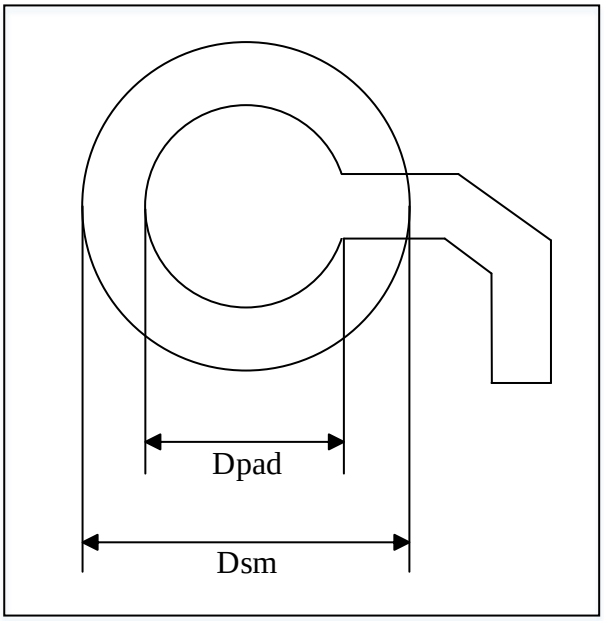


Figure 5-9 BGA64 Recommended PCB design rules

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Pad trace width	0.100 mm

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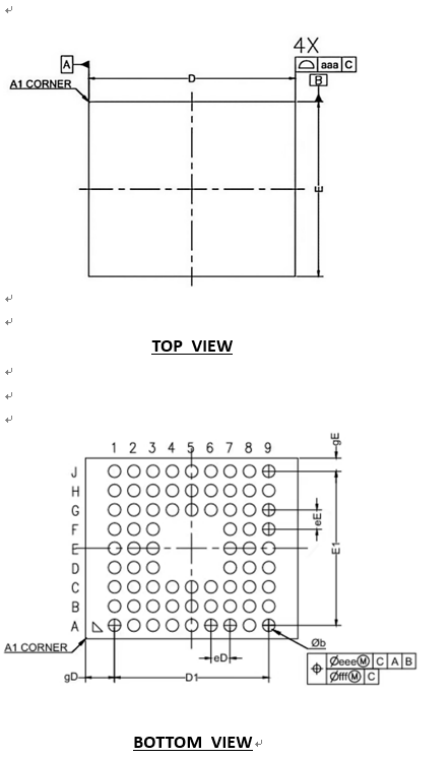
5.5 BGA72

Figure 5-10 BGA72 Package Dimensions



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

ITEM		SYMBOL	COMMON DIMENSIONS		
			MIN.	NOM.	MAX
Body Size	X	D	4.300	4.400	4.500
	Y	E	3.660	3.760	3.860
Ball Pitch	X	eD		0.400	
	Y	eE		0.400	
Total Thickness		A	0.662	0.733	0.804
Ball Stand Off		A1	0.138	0.188	0.238
Mold+Substrate		A2	0.495	0.545	0.595
Mold Thickness		A3	0.325	0.365	0.405
Substrate Thickness		A5	0.150	0.180	0.210
Ball Size		b	0.208	0.258	0.308
Package Edge Tolerance		aaa		0.100	
Mold Flatness		ccc		0.200	
Coplanarity		ddd		0.080	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.050	
Ball Count		n		72	
Edge Ball Center to Center	X	D1		3.200	
	Y	E1		3.200	
Edge Ball Center to Package Edge	X	gD		0.600	
	Y	gE		0.280	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSITIONS DESIGNATION PER JESD 95.

Figure 5-11 BGA72 Recommended Footprint

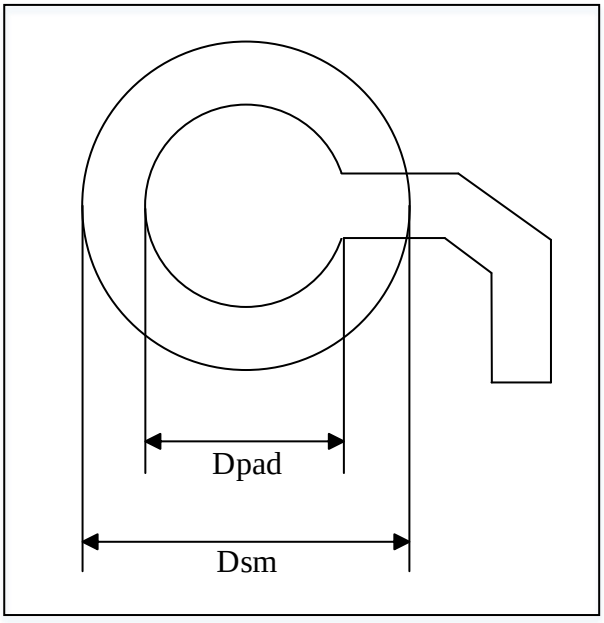


Figure 5-12 BGA72 Recommended PCB design rules

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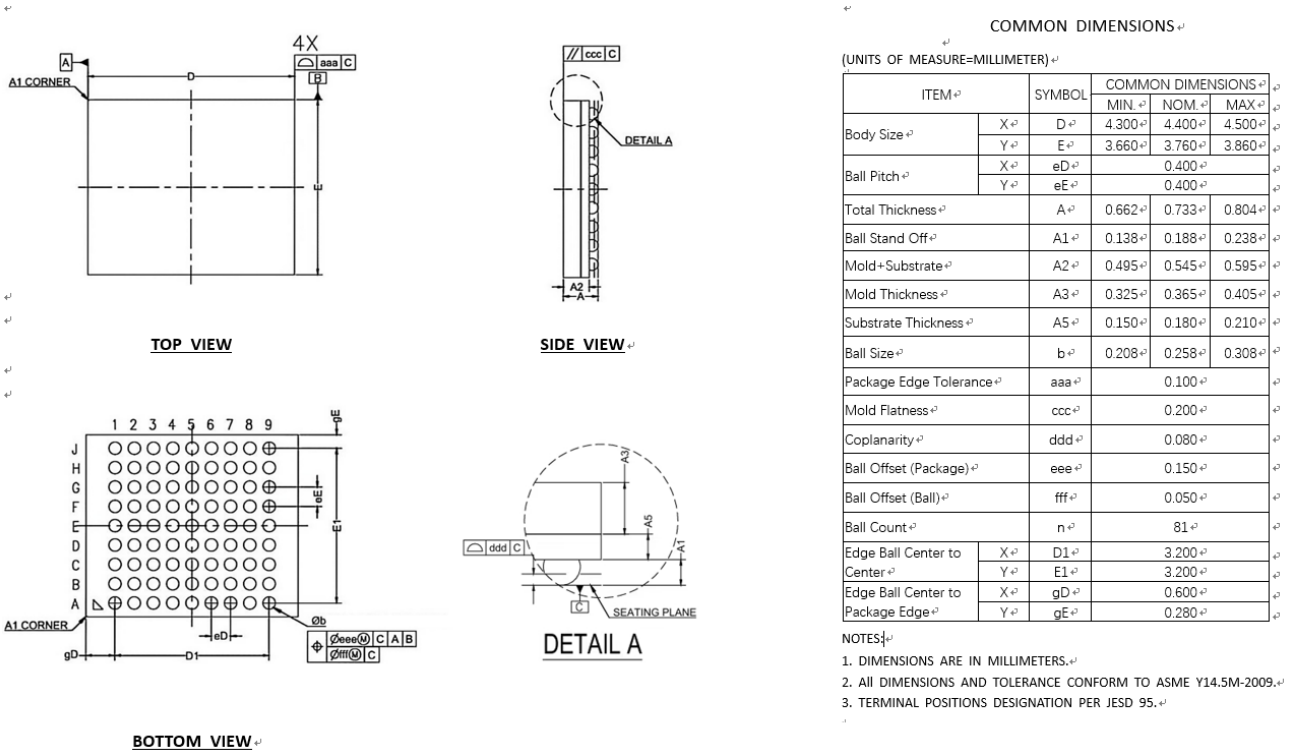
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.220 mm
Dsm	0.310 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

5.6 BGA81

Figure 5-13 BGA81 Package Dimensions



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

ITEM		SYMBOL	COMMON DIMENSIONS		
			MIN.	NOM.	MAX
Body Size	X	D	4.300	4.400	4.500
	Y	E	3.660	3.760	3.860
Ball Pitch	X	eD		0.400	
	Y	eE		0.400	
Total Thickness		A	0.662	0.733	0.804
Ball Stand Off		A1	0.138	0.188	0.238
Mold+Substrate		A2	0.495	0.545	0.595
Mold Thickness		A3	0.325	0.365	0.405
Substrate Thickness		A5	0.150	0.180	0.210
Ball Size		b	0.208	0.258	0.308
Package Edge Tolerance		aaa		0.100	
Mold Flatness		ccc		0.200	
Coplanarity		ddd		0.080	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.050	
Ball Count		n		81	
Edge Ball Center to Center	X	D1		3.200	
	Y	E1		3.200	
Edge Ball Center to Package Edge	X	gD		0.600	
	Y	gE		0.280	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSITIONS DESIGNATION PER JESD 95.

Figure 5-14 BGA81 Recommended Footprint

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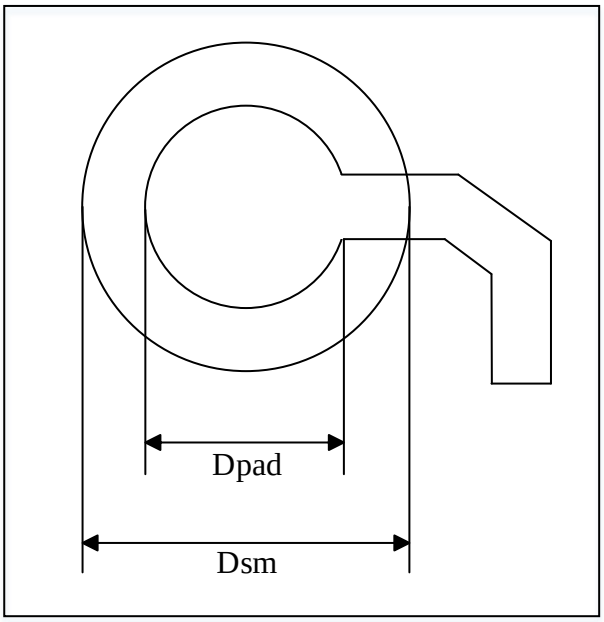

Figure 5-15 BGA81 Recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.220 mm
Dsm	0.310 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

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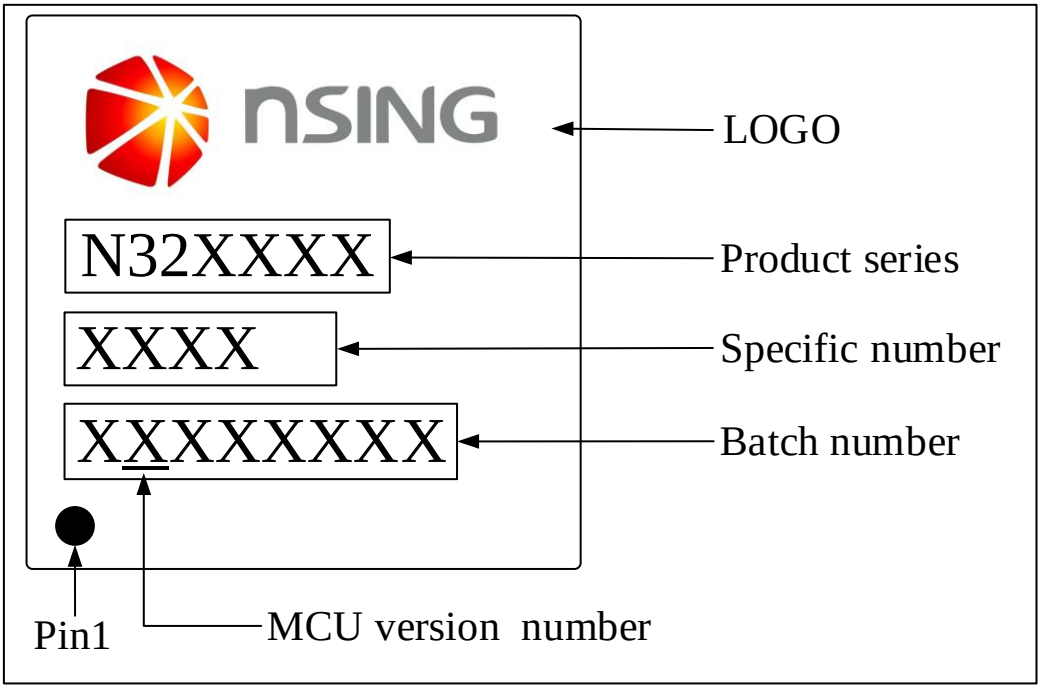
6 Marking Information

Figure 6-1 Marking Information



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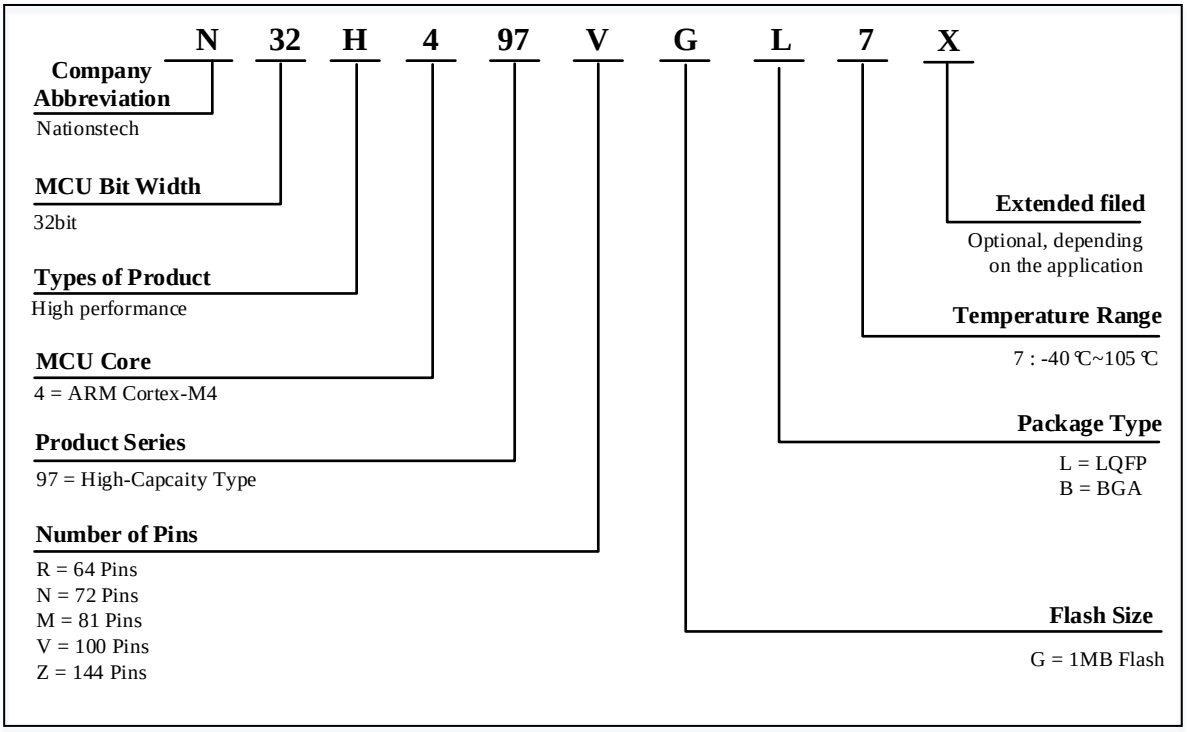
7 Ordering Information

7.1 Naming Convention

Figure 7-1 N32H497 Series Part Number Information



7.2 Ordering code

Table 7-1 N32H497 Series Ordering Code

Ordering Code(1)	Package	Size	Packaging(2)	SPQ(3)	Temperature range
N32H497RGL7	LQFP64	10mm x 10mm	Tray	160	-40℃～105℃
N32H497VGL7	LQFP100	14mm x 14mm	Tray	90	-40℃～105℃
N32H497VGL7G	LQFP100-2	14mm x 14mm	Tray	90	-40℃～105℃
N32H497ZGL7	LQFP144	20mm x 20mm	Tray	60	-40℃～105℃
N32H497RGB7	BGA64	5mm x 5mm	TBD	TBD	-40℃～105℃
N32H497NGB7	BGA72	4.41mm x 3.76mm	TBD	TBD	-40℃～105℃
N32H497MGB7	BGA81	4.41mm x 3.76mm	TBD	TBD	-40℃～105℃

1. For the latest detailed-ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
3. Minimum packaging quantity.

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8 Version History

Date	Version	Changes
2026.1.22	V1.0.0	Initial release.

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