

N32H493 xE/xG

Datasheet

N32H493 series employs a 32-bit ARM Cortex-M4F core operating at a maximum frequency of 240MHz, supporting floating-point operations and DSP instructions. It integrates up to 1MB of embedded Flash, 256KB of SRAM (including 64KB of CCM SRAM) plus 4KB of Backup SRAM, three 12-bit 4.7Msps ADCs, two 12-bit DACs, and integrated communication interfaces including U(S)ART, I²C, and SPI. It supports the xSPI high-speed memory interface, multiple advanced timers, general-purpose timers, basic timers, and low-power timers. The device incorporates a hardware acceleration engine for cryptographic algorithms, supporting AES/TDES, SHA, SM3, SM4, and MD5 algorithms. Supports TRNG true random number generator and CRC16/32.

Key Features

● CPU Core

- 32-bit ARM Cortex-M4F + FPU, single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
- Built-in 8KB I-Cache (instruction cache) and 1KB D-Cache (data cache), supporting Flash Accelerator Unit for zero-wait program execution
- Frequency up to 240 MHz, 300 DMIPS

● Memories

- 1MByte on-chip Flash, dual-bank support, enabling secure storage, partition management and data protection, 10,000 erase/write cycles, 10-year data retention
- 192KB general-purpose SRAM, configurable for ECC support
- 64KB CCM SRAM, defaulted as general-purpose SRAM, configurable as CCM SRAM, configurable for ECC support
- 4-KByte of Backup SRAM with ECC available in Standby mode

● Power Modes

- Run mode: All peripherals configurable for operation
- Sleep Mode: CPU halted, peripherals configurable for operation
- Stop0 mode: SRAM and all registers can be configured to retention, RTC run
- Standby mode: 6uA, all backup registers and Backup SRAM retained, all IOs retained, optional RTC run
- VBAT mode: 4uA, all backup registers and Backup SRAM retained, optional RTC run

● Clock

- HSE: 4MHz~32MHz high-speed external crystal oscillator
- LSE: 32.768KHz low-speed external crystal oscillator
- Built-in multiple high speed PLLs
- MCO: Supports 2-channel clock outputs, which can be configured independently as clock output
- HSI: High-speed internal RC 8MHz, -1.5% to +2% accuracy (full temperature range)
- LSI: Low-speed internal RC 32KHz, +/-10% accuracy (full temperature range)

● Reset

- Supports power-on/brown-out/external pin reset

- Supports watchdog reset
- Supports programmable voltage detection
- **GPIOs**
 - Up to 67 GPIOs, PG9 to PG14 comprise 6 I/O pins capable of supporting VDDIO input power supply operation.
- **Communication Interfaces**
 - 6x SPI interfaces, support half/full duplex mode
 - U(S)ART interfaces
 - ◆ 1x USART interfaces (support ISO7816, IrDA, LIN)
 - ◆ 2x UART interfaces
 - ◆ TX/RX can be mapped to all pins
 - 4x I2C interfaces(Master/Slave) with speed up to 1 MHz where slave mode support dual address response
- **High Performance Analog Interfaces**
 - 3x 12-bit 4.7 Msps ADCs, supporting 12-bit, 10-bit, 8-bit, and 6-bit sampling precision, with hardware oversampling capability up to 16 bits. ADC1 supports up to 16 external single-ended input channels, ADC2 supports up to 17 external single-ended input channels, and ADC3 supports up to 10 external single-ended input channels. Both single-ended and differential modes are supported.
 - 2x 12-bit DACs, each supporting one internal output channel and one external output channel. Sampling rate: 1 Msps. Supports buffered and unbuffered outputs. Capable of internal output, external output, or simultaneous internal and external output.
 - 1x temperature sensor
- **High Speed External Memory Interfaces**
 - 1x xSPI interface, supporting external SRAM, PSRAM and Flash, supporting XIP
- **DMA Controllers**
 - 2x DMA controller
 - Each controller supports 8 channels
 - Channel source address and destination address can be configured arbitrarily
- **RTC real-time clock**
 - Supports leap-year calendar, alarm event, periodic wake up
 - Supports internal and external clock calibration
- **Timers**
 - 3x 16-bit advanced timer/counters supporting input capture, complementary outputs, quadrature encoding inputs, etc., with a maximum control precision of 4.17ns; each timer features six independent channels, four of which support four pairs of complementary PWM outputs
 - 10x general-purpose timers (GTIM1–10):

- GTIM2/3/5/6/7: 16-bit counters with a maximum control precision of 4.17 ns. Each timer features up to 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output.
- GTIM1/4: 32-bit counters with maximum control precision of 4.17 ns. Each timer provides up to 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output;
- GTIM8–10, 16-bit counters with a maximum control precision of 4.17 ns. Each timer features up to four independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output. Only Channel 1 supports complementary outputs with dead time and brake input capability.
- 2x 32-bit basic timers
- 2x 16-bit low-power timer, can operate in Stop0 and Standby mode.
- 1x 24-bit SysTick timer.
- 1x 14-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)
- **Programming Methods**
 - Support SWD/JTAG debugging interface.
 - Support UART and I2C Bootloader
- **Security Features**
 - Flash encryption, multi-user partition management unit (SMPU)
 - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
 - Built-in hardware acceleration engine for cryptographic algorithm
 - Supports AES/TDES, SHA, SM3, SM4, and MD5 algorithms
 - True random number generator(TRNG)
 - CRC16/32 operation
 - Supports secure boot, program encryption download, secure firmware update
 - Supports external clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
 - Operating voltage range: 1.8V~3.6V
 - Operating temperature range: -40°C ~ 105°C
- **Packages**
 - BGA64 (5mm x 5mm)
 - BGA72 (4.41mm x 3.76mm)
 - BGA81 (4.41mm x 3.76mm)

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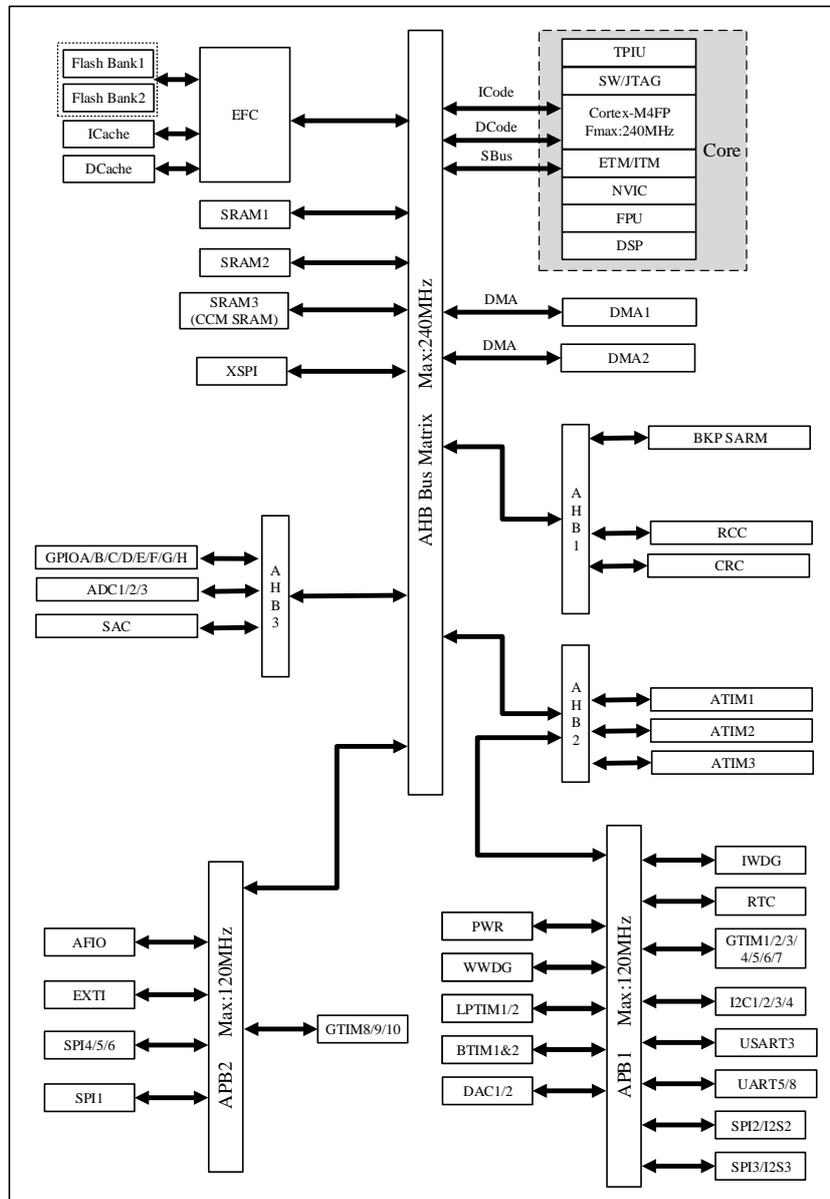
1 Introduction

The N32H493 series microcontrollers feature a 32-bit ARM Cortex®-M4F core, supporting single-precision floating-point operations and DSP instructions. Operating at a maximum frequency of 240MHz, they integrate up to 1MB of embedded Flash, 256KB SRAM (including 64KB CCM SRAM) + 4KB Backup SRAM. The devices incorporate three 12-bit 4.7Msps ADCs, two 12-bit DACs, and integrated communication interfaces including U(S)ART, I²C, and SPI. It supports the xSPI high-speed memory interface, multiple advanced timers, general-purpose timers, basic timers, and low-power timers. The device incorporates a hardware acceleration engine for cryptographic algorithms, supporting AES/TDES, SHA, SM3, SM4, and MD5 algorithms. Supports TRNG true random number generator and CRC16/32.

The N32H493 series operates reliably within a temperature range of -40 °C to +105 °C, with a supply voltage of 1.8V to 3.6V, and offers multiple power consumption modes.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32H493 Series Block Diagram



1.1 Product Configurations

Table 1-1 N32H493 Series Product Configuration

Device		N32H493ME/MGB7		N32H493NE/NGB7		N32H493RE/RGB7	
Operating Condition		1.8~3.6V/-40~105°C					
CPU Frequency		ARM Cortex-M4F @240MHz, 300DMIPS					
Flash Capacity (KB)		512	1024	512	1024	512	1024
Total SRAM (KB)	General SRAM	192	192	192	192	192	192
	CCM SRAM ⁽¹⁾	64					
	Backup SRAM	4					
Times	ATIM	3*16bit					
	GTIM	5*16bit					
		2*32bit ⁽²⁾					
		3*16bit ⁽³⁾					
	BTIM	2*32bit					
	LPTIM	2*16bit					
	SysTick timer	1					
	WWDG	1*14bit					
	IWDG	1*12bit					
RTC	Yes						
Communication Interfaces	SPI	6					
	I ² C	4					
	USART	1 ⁽⁴⁾					
	UART	2 ⁽⁵⁾					
Memory Expansion	XSPI	Yes					
GPIO		67		59		52	
WKUP Pins		5		5		5	
Nb of I/Os down to 1.8 V ⁽⁶⁾		6		6		0	

DMA Number of channels	2 16		
12bit ADC Number of channels	3 23	3 23	3 23
12bit DAC Number of channels	2 2		
Algorithm Support	DES/3DES、AES、SHA1/SHA224/SHA256、SM3、SM4、 MD5、CRC16/CRC32		
TRNG	Yes		
Security Protection	Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot		
Package	BGA81	BGA72	BGA64

Note:

1. *Power-on default is general-purpose SRAM; software configurable as CCM SRAM;*
2. *Only GTIM1 and GTIM4 support 32-bit timers;*
3. *Only GTIM8/9/10 support braking; channel 1 supports complementary channel output;*
4. *USART interface is USART3; TX, RX, RTS_DE support full pin mapping;*
5. *UART interfaces are UART5 and UART8, with TX, RX, and RTS_DE supporting full pin mapping;*
6. *The PG9 to PG14 pins on the BGA81 and BGA72 packages support operation via VDDIO input, accommodating 1.8 to 3.6V input..*

2 Functional Overview

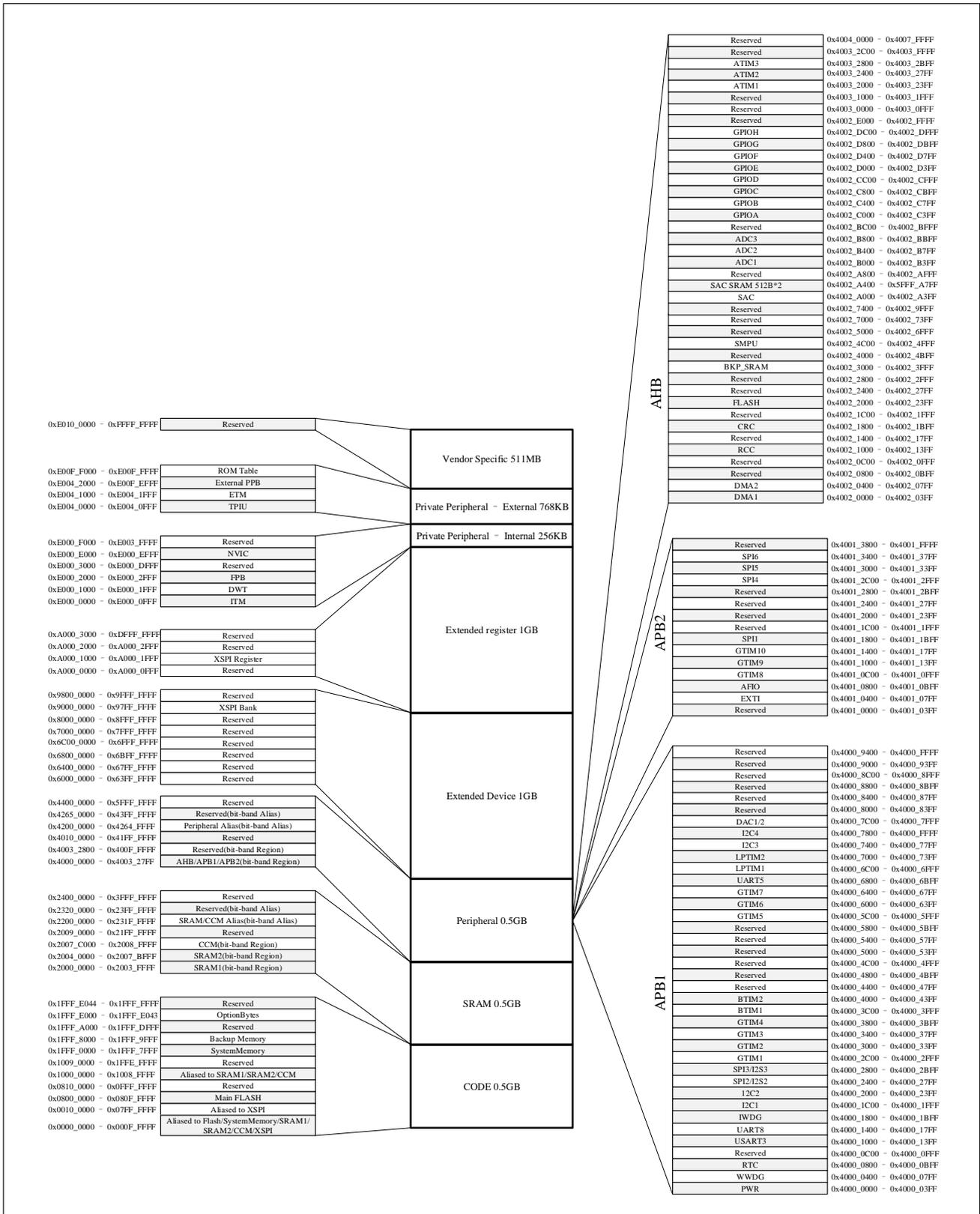
2.1 Processor Core

The N32H493 series integrates the ARM Cortex™-M4F processor. It features a floating-point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 300 DMIPS. At the same time, its efficient signal processing capabilities combined with low power consumption, low cost, and ease of use advantages of the Cortex-M series processors. Make it suitable for applications that need a mix of control and signal processing capabilities in an easy-to-use manner.

The ARM Cortex™-M4F 32-bit reduced instruction set processor offers outstanding code efficiency.

2.2 Memories

The N32H493 series includes embedded encrypted Flash memory and embedded SRAM. The following diagram shows the memory address mapping.

Figure 2-1 Memory Map


2.2.1 Embedded FLASH Memory

The integrated encrypted Flash memory size is up to 1024 Kbytes, utilized for storing programs and data. The page size is 8Kbytes, supporting dual banks, supporting page erasing, double-word writing, word reading, half-word

reading, and byte reading operations.

It supports storage encryption protection, enabling automatic encryption during writing and automatic decryption during reading (including program execution operation).

User partition management is supported, allowing for a maximum of 3 user partitions, different users cannot access each other's data (only executable code can be accessed).

2.2.2 Embedded SRAM

The chip integrates 256KB of SRAM (comprising 192KB of general-purpose SRAM and 64KB of CCM SRAM) alongside 4KB of Backup SRAM, detailed as follows:

192KB general-purpose SRAM, configurable to support ECC.

64KB CCM SRAM, defaulting as general-purpose SRAM, configurable as CCM SRAM. Supports ECC configuration.

4KB BKP SRAM capacity, supporting ECC. Data retention is optional in Standby modes.

2.2.3 Nested Vector Interrupt Controller (NVIC)

Main features:

- Up to 112 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M4F)
- 16 programmable priority levels (four bits of interrupt priority used)
- Low-latency exception and interrupt handling
- Power management control
- Implementation of system control registers

The NVIC and the processor core interface are closely coupled, enabling low-latency interrupt processing and efficient processing of late arriving interrupts. All interrupts, including the core exceptions, are managed by the NVIC.

2.3 Extended Interrupt/Event Controller (EXTI)

The extended interrupt/event controller contains 25 edge detectors used for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. The pending register holds interrupt requests for the status lines, and the interrupt requests can be cleared by writing '1' to the corresponding bit in the pending register.

2.4 Clock System

The device offers various clock options for users to choose from, including:

- High speed internal RC oscillator (HSI) at 8 MHz
- Low speed internal RC oscillator (LSI) at 32 KHz
- High speed external crystal oscillator (HSE) ranging from 4 MHz to 32 MHz.
- Low speed external crystal oscillator (LSE) at 32.768 KHz.

The system clock source can be selected from HSI, HSE, PLL, EXTPLL. Upon reset, the internal MSI clock is set as the default system clock, user can choose the external HSE clock with fail monitoring capabilities. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI. If interrupts are enabled, software can receive corresponding interrupts.

Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. The AHB has a maximum frequency of 240 MHz, APB2 has a maximum frequency of 120 MHz and APB1 has a maximum frequency of 120 MHz.

- Boot from Main Flash memory
- Boot from system memory
- Boot from embedded SRAM

Detailed start-up procedures are outlined in the table below:

Table 2-1 Single-BANK Mode Start-up

Option Byte				Pin	Boot mode	Starting address for accessing memory space in corresponding launch mode			
FLASH_BOOT	nBOOT1	nBOOT0	nSWBOOT0	BOOT0		Front half of Main Flash	Rear half of Main Flash	System Memory	SRAM
1	x	x	1	0	Main Flash front half boot	0x0000_0000	0x0808_0000 ⁽¹⁾	0x1FFF_0000	0x1000_0000
1	x	1	0	x		0x0800_0000			0x2000_0000
0	x	x	1	0	Main Flash rear half boot	0x0808_0000 ⁽¹⁾	0x0000_0000	0x1FFF_0000	0x1000_0000
0	x	1	0	x		0x0800_0000			0x2000_0000
x	1	x	1	1	SystemMemory boot	0x0800_0000	0x0808_0000	0x0000_0000	0x1000_0000
x	1	0	0	x				0x1FFF_0000	0x2000_0000
x	0	x	1	1	SRAM boot	0x0800_0000	0x0808_0000	0x1FFF_0000	0x0000_0000
x	0	0	0	x					0x1000_0000
									0x2000_0000

Note 1. When the MCU's Flash capacity is 512KB, the starting address is 0x0804_0000; when the MCU's Flash capacity is 1MB, the starting address is 0x0808_0000.

Table 2-2 Dual-BANK Mode Start-up

Option Byte				Pin	Boot mode	Starting address for accessing memory space in corresponding launch mode			
FLASH_BOOT	nBOOT1	nBOOT0	nSWBOOT0	BOOT0		Main Flash BANK1	Main Flash BANK2	System Memory	SRAM
1	x	x	1	0	Main Flash BANK1 boot	0x0000_0000	0x0808_0000 ⁽¹⁾	0x1FFF_0000	0x1000_0000
1	x	1	0	x		0x0800_0000			0x2000_0000
0	x	x	1	0	Main Flash BANK2 boot	0x0808_0000 ⁽¹⁾	0x0000_0000	0x1FFF_0000	0x1000_0000
0	x	1	0	x		0x0800_0000			0x2000_0000
x	1	x	1	1	SystemMemory boot	0x0800_0000	0x0808_0000	0x0000_0000	0x1000_0000
x	1	0	0	x				0x1FFF_0000	0x2000_0000
x	0	x	1	1	SRAM boot	0x0800_0000	0x0808_0000	0x1FFF_0000	0x0000_0000
x	0	0	0	x					0x1000_0000
									0x2000_0000

Note 1. When the MCU's Flash capacity is 512KB, the starting address is 0x0804_0000; when the MCU's Flash capacity is 1MB, the starting address is 0x0808_0000.

The Bootloader is stored in the system memory and can program the flash memory through USART1 or USB interface.

Address remapping for physical address 0 can also be achieved by configuring RCC_BOOTREMAP.REMAPSEL[2:0]:

- Boot from xSPI external memory through remap
- Boot from FEMC external memory through remap
- Boot from SDRAM external memory through remap

2.6 Power Supply Scheme

There are five external power supplies: VDD, VDDIO, VDDA, VREF, VBAT. Among them, VDD is the chip power supply, mainly for the power supply system and clock system; VDDA is the analog peripheral power supply, mainly for the analog peripherals; VREF provides a reference power supply for the analog peripherals to provide higher accuracy. VBAT is connected to the battery to provide power for the backup domain.

There are five power domains, powered by external power supplies for different power domains:

- V_{DD} domain: 1.8 to 3.6V, mainly powering for MR, most GPIOs, HSE, HSI, PLL, POR/PDR, BOR, PVD, and USB PHY
- V_{DDIO} domain: Operating within a voltage range of 1.8 to 3.6 volts, it provides independent power supply to 6 I/O pins: PG9 to PG14.
- V_{DDA} domain: 1.8 to 3.6V, mainly powering for ADC, DAC, TS, etc.
- V_{DDBK} domain: 1.8 to 3.6V, mainly powering for WKUP pin, NRST, PC13/14/15, LSE, LSI, etc.
- V_{DDD} domain: 1.1 V or 0.9 V, mainly powering for CPU, AHB, APB, SRAM, FLASH, RCC, TRNG, and most peripherals
- V_{DDDBK} domain: 0.9 V or 0.8 V, mainly powering for PWR, Backup SRAM (4KB), RTC, LPTIM, WKUP pin, NRST, PC13/14/15, backup IOM, IWDG, and RCC_BDCTRL register.

2.7 Reset

POR and BOR circuits are integrated inside the device. This part of the circuit ensures that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold (V_{POR/BOR}), the device goes into reset state without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See Table 4-6 for values of V_{POR/PDR} and V_{PVD}.

2.9 Low Power Mode

The N32H493 series supports four low-power modes.

- SLEEP mode

In SLEEP mode, only the CPU is stopped, all peripherals remain operational and can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

STOP0 mode is based on the Cortex-M4F deep sleep mode. Achieves the lowest power consumption, while retaining the content of SRAM and registers. Most clocks in the main power domain are stopped, such as PLL, HSE, HSI.

Wakeup: The device can be woken up from STOP0 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC timestamp, RTC alarm, etc.

- STANDBY Mode

In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator. After entering STANDBY mode, most register contents will be lost, while the contents of backup registers will still be retained. The STANDBY circuitry continues to function.

Wakeup: External reset signal on NRST, IWDG reset, rising/falling edge on the WKUP pin, RTC alarm, RTC

timestamp and LPTIM wake-up event can wake up the device from STANDBY mode.

- VBAT Mode

Whenever VDD power is lost, it will automatically enter VBAT mode. In VBAT mode, except for NRST, WKUP, PC13_TAMPER, PC14, and PC15, most I/O pins are in a high-impedance state.

Wakeup: VDD power up.

2.10 Direct Memory Access (DMA)

The DMA controller can access the following slaves: Flash, SRAM1, SRAM2, CCM SRAM3, XSPI, CRC, APB1, APB2, ATIM, ADC, DAC.

The DMA controller is controlled by the CPU to perform fast data transfers from source to destination. After configuring, data can be transferred without any CPU intervention. This keeps the CPU resources free for other operations or saves overall system power consumption.

The device integrates two DMA controllers (DMA1, DMA2), each DMA supports eight channels. Each channel is dedicated to servicing memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA channels.

The key features are as follows:

- 16 independently configurable channels (requests): Each DMA (DMA1, DMA2) supports 8 channels
- Support memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers
- Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Each DMA channel has a dedicated software priority level (DMA_CHCFGx.PRIOLVL[1:0] bits, corresponding to 4 priority levels) that can be individually configured. Channels with the same priority level will further compare the hardware index (channel number) to determine the final priority (the channel with the lower index number has higher priority).
- Configurable source and destination transfer size (byte, half word, word). Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) and 1 global interrupt flag (set by logical OR of the 3 events) for each channel
- Access to Flash, Sram1, Sram2, CCM Sram3, XSPI, CRC, APB1, APB2, ATIM, ADC, DAC
- Programmable number of data to be transferred: up to 65536
- Support burst transfers, burst length is configurable, can be set to 1/2/3/4/5/6/7/8 units.

2.11 Real Time Clock (RTC)

The RTC consists of continuously running counters integrated with a built-in calendar clock module that provides a perpetual calendar functionality, as well as alarm interrupts and periodic interrupt.

The key features are as follows:

- The Real-Time Clock (RTC) is an independent BCD (binary-coded decimal) timer/counter
- Software supports daylight saving time compensation
- Programmable periodic automatic wake-up timer.
- Two 32-bit registers containing hours, minutes, seconds, year, month, date, and week day
- One independent 32-bit register containing sub-seconds
- Two programmable alarms

- Two 32-bit registers containing programmed hours, minutes, seconds, year, month, date, and week day
- Two independent 32-bit registers containing programmed sub-seconds
- Digital precision calibration function
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Three configurable filtering and internal pull-up intrusion detection events
- Timestamp functionality
- 20 backup registers that can retain data in low-power mode
- Multiple interrupt/event wake-up sources, including alarm A, alarm B, wake-up timer, timestamp, and tamper event
- As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, SLEEP mode, STOP0 mode and VBAT mode)
- The RTC provides various wake-up sources that can wake the MCU from all low-power modes (SLEEP mode, STOP0 mode, and STANDBY mode)

2.12 Timers and Watchdogs

The N32H493 series supports up to 3 advanced timers, 10 general timers, 2 basic timers, 2 low-power timers, as well as 1 independent watchdog timer, 1 window watchdog timer, and 1 SysTick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low-power timer:

Table 2-3 Comparison Of Timer Functions

Timer	Counter resolution	Counter type	Prescaler factor	Capture/compare channels	Complementary outputs	Maximum Interface Clock (MHz)	Maximum Timer Clock (MHz)
ATIM1~3	16	Up, down, up/down	Any integer between 1 and 65536	4	4	240	240
GTIM1 GTIM4	32	Up, down, up/down	Any integer between 1 and 65536	4	N	120	240
GTIM2~3 GTIM5~7	16	Up, down, up/down	Any integer between 1 and 65536	4	N	120	240
GTIM8~10	16	Up, down, up/down	Any integer between 1 and 65536	4	1	120	240
BTIM1~2	32	Up	Any integer between 1 and 65536	0	N	120	240
LPTIM1~2	16	Up	1, 2, 4, 8, 16, 32, 64, 128	0	N	120	120

2.12.1 Basic Timer (BTIM1~2)

Basic timers contain a 32-bit auto-reload counter.

Main features:

- 32-bit auto-reload up-counting counter
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- Event that generate the interrupt/DMA is as follows:

- Update event

2.12.2 General-Purpose Timer (GTIM1~7)

The general-purpose timers (GTIM1/GTIM2/GTIM3/GTIM4/GTIM5/GTIM6/GTIM7) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-load counters (GTIM2/GTIM3/GTIM5/GTIM6/GTIM7) supporting up counting, down counting, and up/down counting.
- 32-bit auto-load counters (GTIM1/GTIM4) supporting up counting, down counting, and up/down counting.
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- GTIMx supports up to 4 channels
- Channel's working modes: PWM output, output compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event
 - Input capture
 - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signals

2.12.3 General-Purpose Timer (GTIM8~10)

The general-purpose timers (GTIMx) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. The general-purpose timer features complementary output, dead-time insertion, and break functions. It is suitable for motor control.

Main features:

- 16-bit auto-reload counters (Supports up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler (the prescaler factor can be configured with any value between 1 and 65536)
- Programmable repetition counter
- GTIMx supports up to 5 channels
- 4 capture/compare channels, operating modes include: PWM output, output compare, one-pulse mode output, input capture
- 1 break input signal supporting digital filtering, used to place the timer's output signal in a safe user-selectable configuration
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event

- Input capture
- Output compare
- Break input
- Complementary outputs with programmable dead-time
 - For GTIMx, channel 1 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

2.12.4 Advanced Control Timer (ATIM1~3)

The advanced control timers (TIM1 and TIM8) is mainly used for the following purposes: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc. Advanced timers have complementary output function with dead-time insertion and bracking functionality, making it suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- ATIMx supports up to 9 channels
- 4 capture/compare channels for:
 - PWM output
 - Output compare
 - One-pulse mode output
 - Input capture
- 2 break input signals supporting digital filtering
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event
 - Input capture
 - Output compare
 - Break input
- Complementary outputs with programmable dead-time
 - For ATIMx, channel 1,2,3,4 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position

- Hall sensor interface: used to do three-phase motor control
- Trigger input as an external clock or for per-cycle current management

2.12.5 Low Power Timer (LPTIM1~2)

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes. LPTIM can run without internal clock source as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extremely low power consumption.

Main features:

- 16-bit up counter
- 3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources:
 - Internal clock source: LSE, LSI, HSI, HSE or APB1 clock
 - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for Pulse Counter application)
- 16-bit auto-load register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or one-shot mode counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for glitch filtering
- Configurable output (PWM)
- Configurable IO polarity
- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.12.6 SysTick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reload function
- A maskable system interrupt is generated when the counter reaches 0
- Programmable clock source

2.12.7 Watchdog (WDG)

Built-in Independent Watchdog (IWDG) and Window Watchdog (WWDG) timers are used to detect issues caused by software errors. The watchdog timers are highly flexible, enhancing system security and the accuracy of timing control.

Independent watchdog (IWDG)

The Independent Watchdog (IWDG) is driven by the low-speed internal clock (LSI clock) running at 32 kHz. It can continue to operate in the event of a deadlock or MCU freeze. This provides a higher level of security, timing accuracy, and watchdog flexibility. It can resolve system failures caused by software faults through a reset. The IWDG is best suited for applications where the watchdog needs to run as a completely independent process outside the main application but with lower timing accuracy constraints.

When the power control register PWR_CTRL2.IWDGRSTEN is set to '1', a system reset occurs when the IWDG

counter reaches 0 (if this is set to '0', the IWDG counts but does not trigger a reset).

Main features:

- Independent 12-bit down-counter
- The RC oscillator provides an independent clock source that can operate in SLEEP, STOP0, and STANDBY modes
- Support reset and low-power wake-up
- When the down-counter reaches 0x000, the system resets (if the watchdog is activated)

Window watchdog (WWDG)

The clock of the Window Watchdog (WWDG) is derived by dividing the APB1 clock frequency by 4096. It detects abnormal program execution through the configuration of the time window. Therefore, WWDG is suitable for precise timing and is commonly used to monitor software faults that cause the application program to deviate from its normal operation sequence due to external interference or unforeseen logical conditions. When the WWDG decrementing counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0, a system reset occurs.

Main features:

- Programmable 14-bit independent down counter
- When the WWDG is enabled, a reset will occur under the following conditions:
 - The down-counter is less than 0x40
 - When the down counter value is greater than the value of the window register, reload will occur
- Early wake-up interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40

2.13 I²C Bus Interface

The I²C (Inter-Integrated Circuit) bus is a widely used bus structure that consists of only two bidirectional lines, namely the data line SDA and the clock line SCL. Through these two lines, all devices compatible with the I²C bus can directly communicate with each other via the I²C bus.

The I²C interface connects the microcontroller and the serial I²C bus, and can be used for communication between the MCU and external I²C devices. The I²C interface module implements the standard speed mode and fast mode of the I²C protocol, with CRC calculation and verification functions, supports SMBus (System Management Bus) and PMBus (Power Management Bus). It controls all I²C bus-specific sequencing, protocol, arbitration and timing. The I²C interface module also supports DMA mode to effectively reduce the burden on the CPU.

Main features:

- This module can be used as master device or slave device
- Support 7-bit/10-bit addressing and general call
- As an I²C master device, it can generate clock, start signal, and stop signal
- As an I²C slave device, it has programmable I²C address detection and stop bit detection functions
- Support Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz) and Fast-mode Plus (up to 1MHz)
- Supports interrupt vector, transfer complete interrupt, and error event interrupt
- Optional extend clock function
- Support DMA
- Generation or verification of configurable PEC(Packet error checking)
- Compatible with the PMBus and SMBus 2.0
- Support FIFO

2.14 Universal Synchronous/Asynchronous Transceiver (USART)

Universal Synchronous Asynchronous Receiver Transmitter (USART) is a full-duplex serial data exchange interface that supports synchronous or asynchronous communication. It can be flexibly configured to facilitate full-duplex data exchange with a variety of external devices.

The USART interface allows configurable transmission and reception baud rates, and also supports continuous communication through DMA. USART also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smart card asynchronous protocol, IrDA SIR ENDEC function, as well as hardware flow control function.

Main features:

- Full duplex, asynchronous communication
- Single-wire half-duplex communications
- Programmable baud rate, up to 15 Mbit/s
- Configurable oversampling method by 16 or 8
- Programmable data word length (8 or 9 bits)
- Two internal FIFOs for transmit and receive data
- Configurable stop bits (1 or 2 stop bits)
- Support hardware-generated parity bit and parity bit checking
- Support hardware flow control: RTS, CTS
- Support transmission and reception via DMA
- Multiprocessor communications: If the address does not match, it enters mute mode. Wake-up from mute mode by idle line detection or address mark detection
- Support synchronous mode, allowing the user to control bidirectional synchronous serial communication in master mode
- Support asynchronous Smartcard protocol, compliant with ISO7816-3 standard
- Support IrDA (infrared data association) SIR ENDEC specifications, providing both normal and low power operation modes
- Support LIN mode
- Four error detection flags: Overflow error, Noise error, Frame error, Parity error
- Support multiple interrupt requests: Transmit data register empty, CTS flag, Transmission complete, Reception complete, Data overflow, Bus idle, Parity error, LIN mode break frame detection, and noise flags/overflow errors/frame errors in multi-buffer communications

Mode configuration:

USART modes	USART3	UART5	UART8
Asynchronous mode	Y	Y	Y
Multiprocessor communication	Y	Y	Y
LIN	Y	Y	Y
Synchronous mode	Y	N	N
Half duplex (Single wire mode)	Y	Y	Y
Smartcard mode	Y	N	N
IrDA	Y	Y	Y
DMA	Y	Y	Y
Hardware flow control	Y	Y	Y

Note: Y = supported; N = not supported.

2.15 Serial Peripheral Interface (SPI)

The SPI protocol supports half-duplex, full-duplex and synchronous, serial communication with external devices. The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. It can be used for a variety of purposes, including simplex synchronous transfers on two lines with bidirectional data line, and also support hardware CRC check.

The SPI main features are:

- Full-duplex and simplex synchronous transmission
- Support master, slave and multi-master mode
- 8 or 16 bit transmission frame format selection
- Programmable data order
- Hardware or software management of chip select signal
- Programmable clock polarity and phase
- Support hardware CRC calculation and check
- Support DMA transfer
- 8 bytes transmit/receive FIFO

2.16 Expanded Serial Peripheral Interface(xSPI)

xSPI is an interface used for communication with single/dual/quad/octal line SPI peripherals. It can operate in two modes: indirect and memory-mapped mode.

It supports indirect mode: all operations are performed using xSPI registers; memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory.

Main features:

- Configurable for 1/2/4/8-bit data
- Support Single SPI/Normal SPI、 DUAL SPI、 QUAD SPI、 Dual-QUAD、 OCTAL SPI modes
- Support Motorola SPI:
 - Standard/Dual/Quad/Octal SPI
- Support SDR and DDR modes
- Support DDR transfer data mask
- Support clock stretching
- In indirect mode and memory-mapped mode, frame format and operation codes can be software configured
- Integrated FIFO for reception and transmission
- 8/16/32-bit data accesses allowed
- 16 words TX FIFO and 16 words RX FIFO
- Support DMA transfer
- Supports the Hyperbus protocol
- XIP mode supports SPI read and write, and supports serial NOR FLASH
 - Support continuous transfer mode
 - Support data prefetch

- Support automatic decryption of executed code, meaning that the xSPI peripheral stores encrypted code, reads the encrypted code during execution, and decrypts it to plaintext for CPU execution, without affecting the access speed to the peripheral storage. The decryption can be software configurable to enable/disable, and the root key is stored in the NVR area, inaccessible to the user
- Support serial NAND FLASH and PSRAM
- When xSPI accesses external memory for read and write, after xSPI initialization, there is no need for additional configuration of xSPI between writing to and reading from external storage, allowing direct memory access (via SRAM address) for reading and writing to external memory
- Support 2 external chip select output controls in master mode; Support 1 chip select input in slave mode. All IOs multiplexed as chip select outputs in master mode can be multiplexed as chip select inputs in slave mode
- Support multi-master arbitration function

2.17 General-Purpose Input/Output Interface (GPIO)

Up to 67 GPIOs, which can be divided into 7 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE/GPIOG/ GPIOH). GPIO ports share pins with other multiplexed peripherals, allowing users to configure them flexibly according to requirements. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up or pull-down), or alternate peripheral function port. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
 - Input floating
 - Input pull up
 - Input pull down
 - Analog function
 - Open-drain output, pull-up and pull-down configurable
 - Push-pull output, pull-up and pull-down configurable
 - Push-pull alternate function, pull-up and pull-down configurable
 - Open-drain alternate function, pull-up and pull-down configurable
- Independent bit set or set functions
- All I/O support external interrupts
- All I/O support low-power mode wake-up, with configurable rising or falling edge:
 - 16 EXTI lines can be used for STOP0 mode wake-up, and all I/O can be multiplexed as EXTI
 - PA0/PA2/PC5/PC13/PE6/PD2/PD3 can be used to wake-up from STANDBY mode
- Support software configure alternate function selection
- Support GPIO lock mechanism, can only be cleared by reset once locked

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed in 32-bit words (16-bit half-word or 8-bit byte access is not allowed).

2.18 Analog/Digital Converter (ADC)

The 12-bit ADC employs a high-speed successive approximation method. Three ADCs are present: ADC1 and ADC2 may be configured as a dual ADC; ADC1, ADC2, and ADC3 may be configured as a triple ADC. ADC1

supports up to 16 multiplexed channels, ADC2 supports up to 17 multiplexed channels, ADC3 supports up to 10 multiplexed channels. Each A/D conversion channel may operate in single, continuous, scan, or intermittent modes. ADC conversion values are stored (left-aligned/right-aligned) in 16-bit data registers. Analogue watchdogs 1/2/3 can detect whether input voltages fall within user-defined high/low thresholds, and the maximum frequency of the ADC input clock is 80MHz.

Main features:

- Support 3 ADCs, support single-ended or differential inputs
 - ADC1 is connected to 16 external channels and to 3 internal channels
 - ADC2 is connected to 17 external channels and to 1 internal channels
 - ADC3 is connected to 10 external channels
- Support 12/10/8/6-bits resolution configurable
 - The maximum sampling rate at 12bit resolution is 4.7 MSPS
 - The maximum sampling rate at 10bit resolution is 6 MSPS
 - The maximum sampling rate at 8bit resolution is 7.2 MSPS
 - The maximum sampling rate at 6bit resolution is 9 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
 - AHB_CLK can be configured as the working clock source, up to 240 MHz
 - PLL or USBHS 240M can be configured as a sampling clock source, up to 80 MHz, support 1, 2, 3, 4, 6, 8, 10, 12 frequency division
 - The AHB_CLK can be configured as the sampling clock source, up to 80 MHz, and supports frequency 1, 2, 3, 4, 6, 8, 10, 12, 16, 32
 - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports EXTI/TIMER trigger ADC sampling
- The sampling time interval for all channels can be programmed independently
- 3 analog watchdogs per ADC
- When the ADC is ready, sampling is completed, conversion is finished, or an analog watchdog 1/2/3 event occurs, an interrupt can be triggered
- Support 4 conversion modes:
 - Single conversion
 - Continuous conversion
 - Discontinuous mode
 - Scan mode
- Support self-calibration
- Data alignment with in-built data coherency
- Start-of-conversion can be initiated:
 - By software for both regular and injected conversions
 - By hardware triggers with configurable polarity (internal timers events or GPIO input events) for both

regular and injected conversions

- Oversampling
 - 16-bit data register
 - Adjustable oversampling ratio, x2, x4, x8, x16, x32, x64, x128, x256
 - Programmable data right shift up to 8 bits
- Data preconditioning
 - Support offset compensation
 - Support gain compensation
- Multi-ADC mode
 - Dual ADC mode: ADC1 and ADC2 combined
 - Triple ADC mode: ADC1, ADC2, and ADC3 combined
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$

2.19 Digital/Analog Converter (DAC)

The DAC is a digital-to-analogue converter, primarily accepting digital inputs and providing voltage outputs. DAC data operates in either 8-bit or 12-bit modes and supports DMA functionality. When configured for 12-bit mode, DAC data may be left-aligned or right-aligned; when set to 8-bit mode, DAC data is right-aligned. Each DAC possesses an independent converter capable of performing conversions autonomously. In dual-DAC mode, each DAC may convert independently, or both DACs (DAC1 and DAC2 may form a pair) may convert and update simultaneously. V_{REF+} is input via a pin as the DAC reference voltage, enhancing the precision of the DAC conversion data. The integrated V_{REFBUF} may also serve as the DAC reference voltage. For details on the voltage reference buffer (V_{REFBUF}), refer to the V_{REFBUF} section.

When the DAC output is internally connected to on-chip peripherals, the $DACx_OUT$ pin may function as a general-purpose input/output (GPIO). The DAC output buffer may be selectively enabled to achieve high drive output current.

Main features:

- Supports 2 DACs, each DAC has its own converter
- Supports 8-bit or 12-bit output, with left or right data aligned in 12-bit mode
- Dual DAC channel for independent or synchronous conversions
- Each DAC supports DMA functionality including DMA underrun error detection
- DMA double data mode can save bus bandwidth
- Generates Noise-wave, Triangular-wave and Sawtooth waveforms.
- Buffer offset calibration.
- Input voltage reference from V_{REF+} and internal V_{REFBUG} .
- External triggers for conversion

2.20 Voltage Reference Buffer (V_{REFBUF})

The chip is equipped with a voltage reference buffer that can be used as a voltage reference for the ADC, 12-bit DAC. It can also serve as a voltage reference for external components through the V_{REF+} pin.

2.21 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated during the link-time and generating of the software.

Main features of CRC32:

- CRC32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)
- 32-bit data to be checked and 32-bit output checksum
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- General-purpose 8-bit register
- Programmable CRC initial value

Main features of CRC16:

- CRC16 ($X^{16} + X^{15} + X^2 + 1$)
- 8-bit data to be checked and 16-bit output checksum
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- Configurable check initial value, and configurable endianness of the data to be checked
- Support 8-bit LRC checksum value generation
- Programmable CRC initial value

2.22 Secure Algorithm Co-processor (SAC)

The device features a secure algorithm co-processor, it supports a variety of international algorithms hash cryptography algorithm acceleration, which can greatly improve the speed of encryption and decryption compared with pure software algorithm.

The hardware supports the following algorithms:

- Support DES symmetric algorithms
 - DES and 3DES encryption and decryption operations are supported
 - TDES supports 2KEY and 3KEY mode
 - Support CBC and ECB mode
- Support the symmetric AES algorithm
 - Support 128bits, 192bits, or 256bits key length
 - Support CBC, ECB, and CTR mode
- Support the symmetric SM4 algorithm
 - Support CBC, ECB mode
- Support SHA hash algorithm
 - Support SHA1, SHA244, SHA256
- Support the MD5 digest algorithm

- Support SM3 hash algorithm
- Support random number generation

Note: The SAC module operating clock is up to 120MHz.

2.23 Unique Device Serial Number (UID)

The N32H493 series products have two built-in unique device serial numbers of different lengths, which are 96-bit unique device ID (UID) and 128-bit unique customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32H493 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory. It can also be used to activate Secure Bootloader with security functions.

The UCID is 128-bit, which complies with the definition of Nations technology chip serial number. It contains the information related to chip production and version.

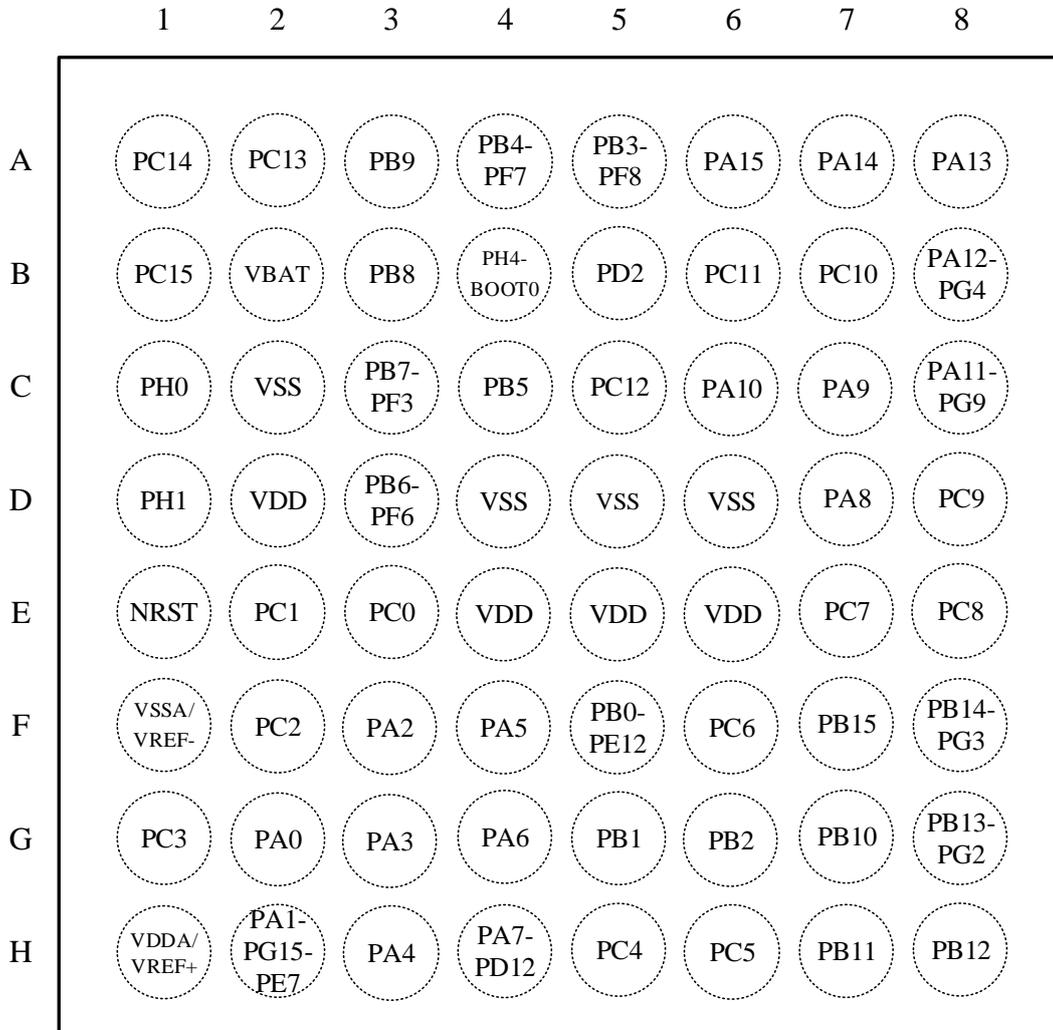
2.24 Serial Single-Wire JTAG Debug Port (SWJ-DP)

The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and Pin Description

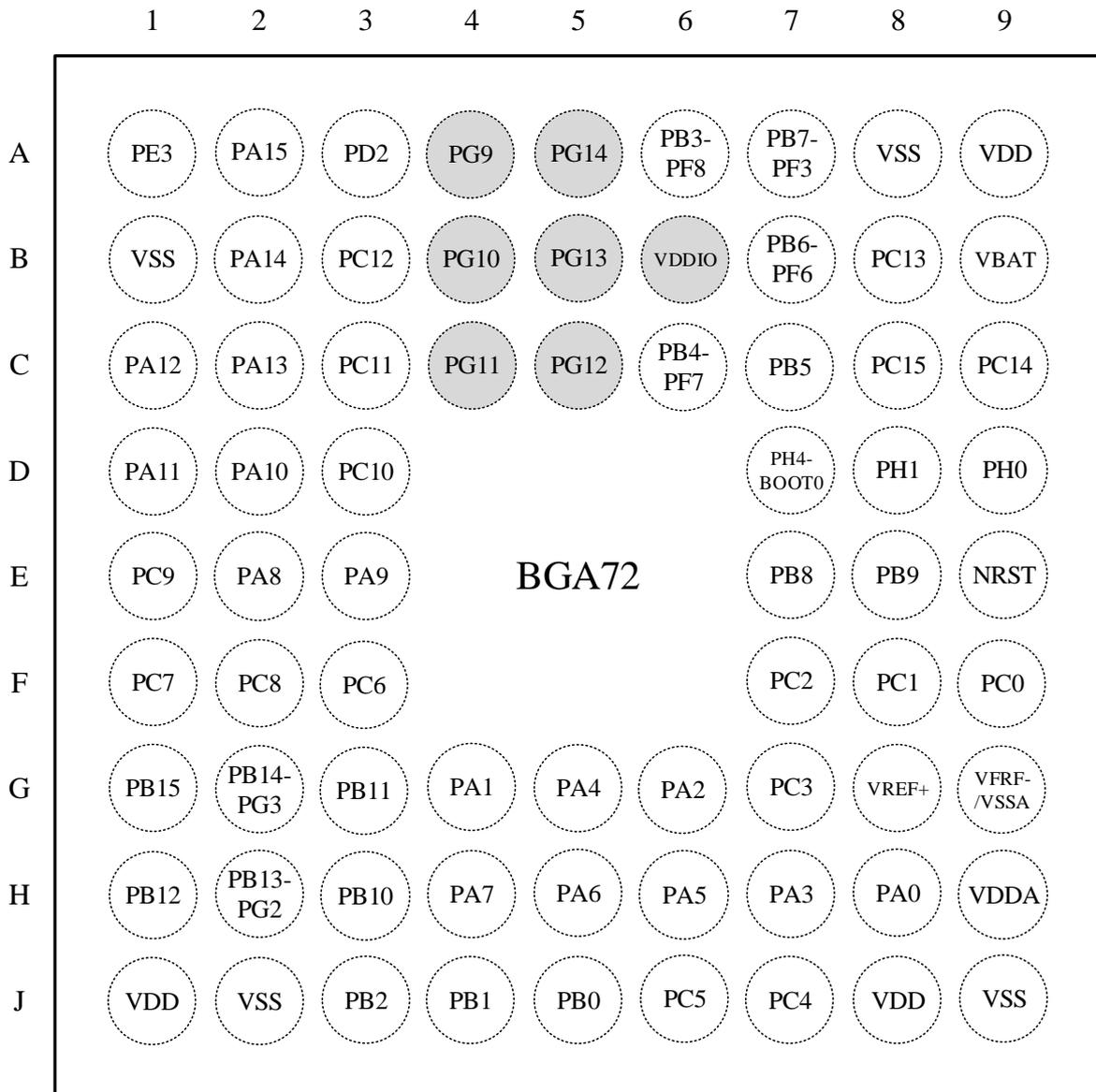
3.1 Pinouts

3.1.1 BGA64

Figure 3-1 BGA64 Pinout


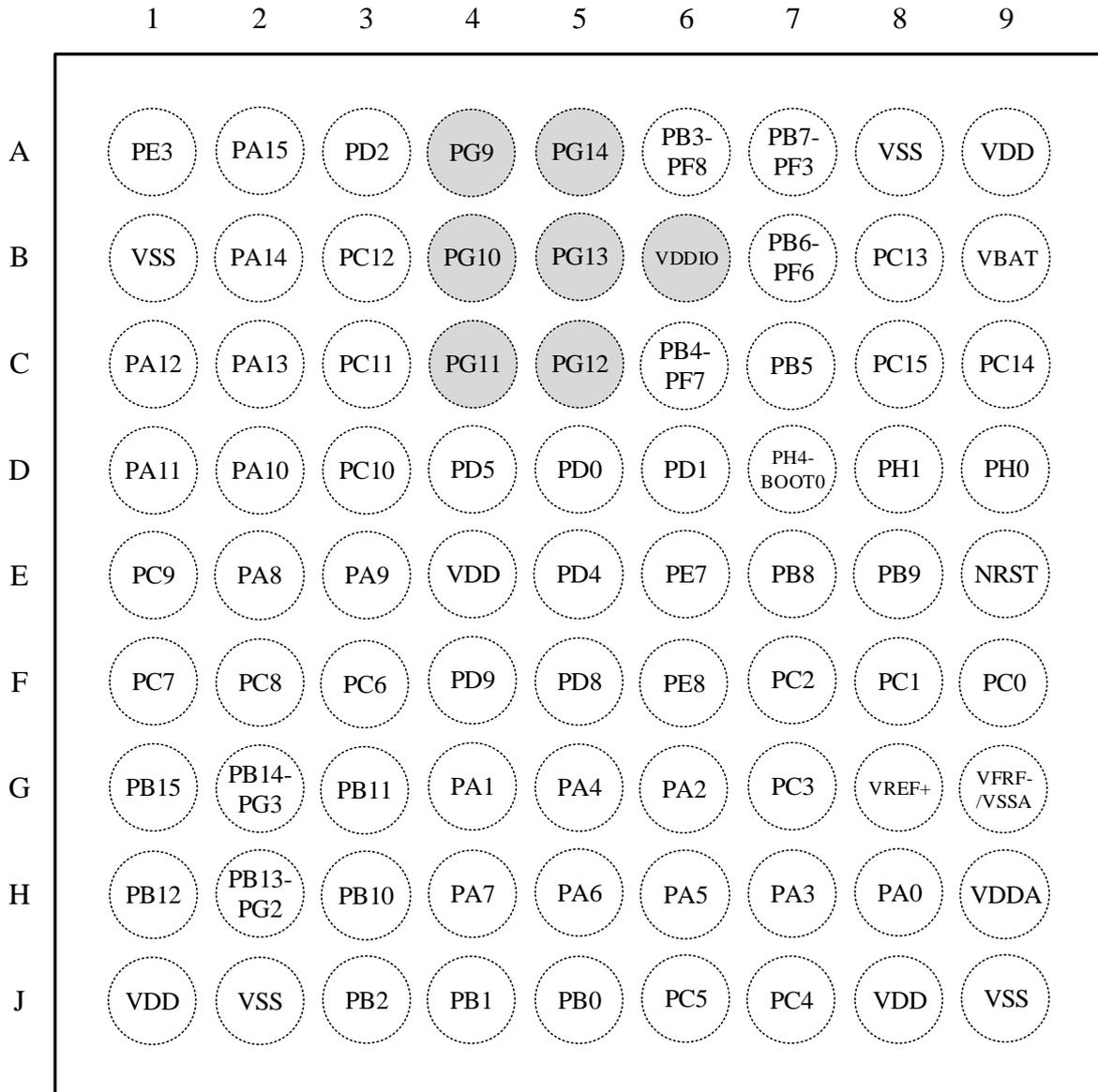
Top view

3.1.2 BGA72

Figure 3-2 BGA72 Pinout


Top view

3.1.3 BGA81

Figure 3-3 BGA81 Pinout


Top view

3.2 Pin Description

Table 3-1 Pin Description

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
-	A1	A1	PE3	I/O	FT	Y	PE3	GTIM2_CH2 SPI4_NSS ATIM3_CH2 GTIM8_BKIN GTIM2_CH1 EVENTOUT	-
B2	B9	B9	VBAT	S	-	-	VBAT	-	-
A2	B8	B8	PC13	I/O	FT	Y	PC13	RTC_OUT1 ATIM1_CH1N ATIM1_BKIN ATIM2_CH4N LPTIM2_ETR XSPI_RXDS ATIM3_BKIN EVENTOUT	WKUP2 RTC_TAMP1
A1	C9	C9	PC14-OSC32_IN	I/O	FT	Y	PC14- OSC32_IN	GTIM7_CH3 EVENTOUT	OSC32_IN
B1	C8	C8	PC15- OSC32_OUT	I/O	FT	Y	PC15- OSC32_OUT	GTIM7_CH4 EVENTOUT	OSC32_OUT
C2	-	-	VSS	S	-	-	VSS	-	-
D2	-	-	VDD	S	-	-	VDD	-	-
C1	D9	D9	PH0-OSC_IN	I/O	FT	Y	PH0-OSC_IN	I2C2_SDA SPI2_NSS ATIM1_CH3N GTIM5_CH3 ATIM3_CH1N XSPI_IO4 EVENTOUT	OSC_IN
D1	D8	D8	PH1-OSC_OUT	I/O	FT	Y	PH1-OSC_OUT	I2C2_SCL SPI2_SCK GTIM5_CH4 ATIM3_CH2N XSPI_NSS0 EVENTOUT	OSC_OUT
E1	E9	E9	NRST	I/O	RST	Y	NRST	-	-
E3	F9	F9	PC0	I/O	FTa	Y	PC0	LPTIM1_IN1 ATIM1_CH1 I2C3_SCL XSPI_RXDS GTIM10_CH1 XSPI_IO7 GTIM9_BKIN EVENTOUT	ADC123_IN10
E2	F8	F8	PC1	I/O	FTa	Y	PC1	LPTIM1_OUT ATIM1_CH2 XSPI_IO4 SPI3_MOSI SPI2_MOSI I2C3_SDA	ADC123_IN11

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								GTIM10_CH2 EVENTOUT	
F2	F7	F7	PC2	I/O	FTa	Y	PC2	SPI2_MISO LPTIM1_IN2 ATIM1_CH3 ATIM3_CH2 XSPI_IO5 SPI3_NSS GTIM10_CH3 XSPI_IO2 GTIM3_CH4 GTIM10_CH1 EVENTOUT	ADC123_IN12
G1	G7	G7	PC3	I/O	FTa	Y	PC3	SPI2_MOSI LPTIM1_ETR ATIM1_CH4 ATIM1_BKIN2 XSPI_IO6 SPI3_SCK GTIM10_CH4 XSPI_IO0 LPTIM2_ETR EVENTOUT	ADC123_IN13
F1	G9	G9	VSSA	S	-	-	VSSA	-	-
F1	G9	G9	VREF-	S	-	-	VREF-	-	-
H1	G8	G8	VREF+	S	-	-	VREF+	-	-
H1	H9	H9	VDDA	S	-	-	VDDA	-	-
G2	H8	H8	PA0-WKUP1	I/O	FTa	Y	PA0-WKUP1	GTIM1_CH1_ETR GTIM4_CH1 ATIM2_ETR ATIM2_BKIN SPI3_MISO ATIM3_CH3N SPI6_NSS GTIM8_BKIN EVENTOUT	ADC123_IN0 WKUP1 RTC_TAMP2
H2	G4	G4	PA1	I/O	FTa	Y	PA1	GTIM4_CH2 GTIM1_CH2 RTC_REFIN GTIM8_CH1N SPI4_MOSI SPI3_MOSI SPI6_SCK ATIM3_CH4N XSPI_IO3 XSPI_RXDS EVENTOUT	ADC123_IN1
H2	-	-	PE7	I/O	FT	Y	PE7	ATIM1_ETR SPI1_SCK GTIM4_CH2 GTIM9_CH4 XSPI_IO4 EVENTOUT	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
H2	-	-	PG15	I/O	FT	Y	PG15	GTIM6_CH4 I2C1_SDA SPI6_NSS ATIM2_CH4N XSPI_NSS1 I2C1_SMBA I2C4_SDA LPTIM1_OUT EVENTOUT	-
F3	G6	G6	PA2	I/O	FTa	Y	PA2	GTIM4_CH3 GTIM5_CH1 GTIM1_CH3 GTIM8_CH1_ETR XSPI_NSS0 SPI6_NSS LPTIM1_IN2 EVENTOUT	ADC123_IN2 WKUP3 LSCO
G3	H7	H7	PA3	I/O	FTa	Y	PA3	GTIM4_CH4 GTIM5_CH2 GTIM1_CH4 GTIM8_CH2 XSPI_CLK MCO2 EVENTOUT	ADC123_IN3
D4	J9	J9	VSS	S	-	-	VSS	-	-
E4	J8	J8	VDD	S	-	-	VDD	-	-
H3	G5	G5	PA4	I/O	TTa	Y	PA4	SPI1_NSS SPI3_NSS GTIM2_CH2 XSPI_NSS1 I2C2_SCL SPI6_MISO GTIM7_CH1 LPTIM2_IN2 SPI6_NSS EVENTOUT	ADC12_IN4 DAC1_OUT
F4	H6	H6	PA5	I/O	TTa	Y	PA5	SPI1_SCK GTIM1_CH1_ETR ATIM2_CH1N XSPI_CLK I2C2_SDA SPI6_MOSI XSPI_IO0 GTIM7_CH2 SPI6_SCK LPTIM2_ETR EVENTOUT	ADC12_IN5 DAC2_OUT
G4	H5	H5	PA6	I/O	FTa	Y	PA6	SPI1_MISO ATIM2_BKIN GTIM9_CH1 GTIM2_CH1 ATIM1_BKIN XSPI_IO3 XSPI_IO0	ADC12_IN6

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								SPI6_MISO GTIM6_CH1 EVENTOUT	
H4	H4	H4	PA7	I/O	FTa	Y	PA7	SPI1_MOSI ATIM2_CH1N GTIM7_CH1 GTIM2_CH2 ATIM1_CH1N GTIM10_CH1 XSPI_IO2 XSPI_IO1 MCO1 GTIM9_CH2 SPI6_MOSI EVENTOUT	ADC12_IN7
H4	-	-	PD12	I/O	FT	Y	PD12	GTIM3_CH1 SPI3_MOSI GTIM6_CH1 I2C4_SCL I2C3_SCL XSPI_IO1 LPTIM1_IN1 LPTIM2_IN1 EVENTOUT	-
H5	J7	J7	PC4	I/O	FTa	Y	PC4	ATIM1_ETR I2C2_SCL XSPI_IO7 XSPI_IO2 I2C3_SCL LPTIM2_OUT ATIM3_CH3N GTIM1_CH4 EVENTOUT	ADC12_IN14
H6	J6	J6	PC5	I/O	FTa	Y	PC5	GTIM8_BKIN ATIM1_CH4N XSPI_IO3 I2C3_SDA GTIM5_ETR XSPI_RXDS EVENTOUT	ADC12_IN15 WKUP4
F5	J5	J5	PB0	I/O	FTa	Y	PB0	GTIM2_CH3 ATIM2_CH2N ATIM1_CH2N XSPI_IO1 SPI5_SCK SPI3_MOSI EVENTOUT	ADC12_IN8
F5	-	-	PE12	I/O	FT	Y	PE12	ATIM1_CH3N SPI4_SCK XSPI_IO0 SPI2_MISO GTIM7_CH4 SPI1_NSS SPI5_SCK	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								EVENTOUT	
G5	J4	J4	PB1	I/O	FTa	Y	PB1	GTIM2_CH4 ATIM2_CH3N ATIM1_CH3N XSPI_IO0 SPI5_NSS LPTIM2_IN1 EVENTOUT	ADC12_IN9
G6	J3	J3	PB2	I/O	FTa	Y	PB2	RTC_OUT2 LPTIM1_OUT GTIM4_CH1 ATIM3_CH1 I2C3_SMBA XSPI_IO5 GTIM1_CH4 SPI3_MOSI SPI1_NSS GTIM6_ETR EVENTOUT	ADC3_IN16
D5	J2	J2	VSS	S	-	-	VSS	-	-
E5	J1	J1	VDD	S	-	-	VDD	-	-
-	-	E6	PE7	I/O	FT	Y	PE7	ATIM1_ETR SPI1_SCK GTIM4_CH2 GTIM9_CH4 XSPI_IO4 EVENTOUT	-
-	-	F6	PE8	I/O	FT	Y	PE8	ATIM1_CH1N GTIM4_CH3 SPI1_MISO XSPI_IO5 EVENTOUT	-
G7	H3	H3	PB10	I/O	FTa	Y	PB10	SPI2_SCK I2C2_SCL GTIM1_CH3 XSPI_CLK ATIM1_BKIN ATIM3_CH2 XSPI_NSS1 EVENTOUT	ADC3_IN17
H7	G3	G3	PB11	I/O	FTa	Y	PB11	I2C2_SDA GTIM1_CH4 XSPI_NSS0 ATIM3_CH3 EVENTOUT	ADC2_IN16
H8	H1	H1	PB12	I/O	FT	Y	PB12	SPI2_NSS I2C2_SMBA ATIM1_BKIN GTIM4_ETR SPI4_NSS GTIM9_CH3 ATIM3_CH4 XSPI_CLK	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								I2C2_SDA EVENTOUT	
G8	H2	H2	PB13	I/O	FT	Y	PB13	SPI2_SCK ATIM1_CH1N SPI4_SCK ATIM1_CH2 GTIM10_CH2 GTIM9_CH4 I2C2_SMBA EVENTOUT	-
G8	H2	H2	PG2	I/O	FT	Y	PG2	ATIM3_CH3N SPI1_SCK I2C2_SCL GTIM5_ETR ATIM2_BKIN ATIM3_CH4 EVENTOUT	-
F8	G2	G2	PB14	I/O	FT	Y	PB14	SPI2_MISO ATIM1_CH2N GTIM8_CH1 ATIM2_CH2N GTIM9_CH2 GTIM5_CH1 EVENTOUT	-
F8	G2	G2	PG3	I/O	FT	Y	PG3	ATIM3_BKIN I2C4_SCL SPI1_MISO ATIM3_CH4N I2C2_SDA ATIM2_BKIN2 SDRAM_A10 GTIM8_CH3 EVENTOUT	-
F7	G1	G1	PB15	I/O	FT	Y	PB15	RTC_REFIN SPI2_MOSI ATIM1_CH3N ATIM2_CH3N GTIM8_CH2 GTIM8_CH1N ATIM2_CH4 XSPI_CLK EVENTOUT	-
-	-	F5	PD8	I/O	FT	Y	PD8	SPI3_NSS ATIM1_CH3 GTIM10_CH1 EVENTOUT	-
-	-	F4	PD9	I/O	FT	Y	PD9	SPI3_SCK ATIM1_CH3N GTIM9_CH3 GTIM7_ETR GTIM10_CH2 EVENTOUT	-
-	-	E4	VDD	S	-	-	VDD	-	-
F6	F3	F3	PC6	I/O	FT	Y	PC6	ATIM2_CH1	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								GTIM2_CH1 I2C4_SCL SPI2_NSS ATIM2_CH2 XSPI_IO5 EVENTOUT	
E7	F1	F1	PC7	I/O	FT	Y	PC7	ATIM2_CH2 GTIM2_CH2 I2C4_SDA SPI2_SCK ATIM2_CH2N GTIM8_CH2 XSPI_IO6 EVENTOUT	-
E8	F2	F2	PC8	I/O	FT	Y	PC8	ATIM2_CH3 GTIM2_CH3 ATIM3_CH3 I2C3_SCL SPI2_MISO EVENTOUT	-
D8	E1	E1	PC9	I/O	FT	Y	PC9	MCO2 ATIM2_CH4 I2C3_SDA GTIM2_CH4 ATIM2_BKIN2 SPI2_MOSI ATIM2_CH3N GTIM8_CH3 XSPI_IO0 EVENTOUT	-
D7	E2	E2	PA8	I/O	FT	Y	PA8	MCO1 ATIM1_CH1 I2C3_SCL I2C2_SDA I2C2_SMBA GTIM3_ETR ATIM2_BKIN2 LPTIM2_OUT EVENTOUT	-
C7	E3	E3	PA9	I/O	FT	Y	PA9	ATIM1_CH2 I2C3_SMBA I2C2_SCL GTIM8_BKIN GTIM1_CH3 SPI2_SCK I2C4_SCL I2C1_SCL EVENTOUT	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
C6	D2	D2	PA10	I/O	FT	Y	PA10	ATIM1_CH3 GTIM10_BKIN I2C2_SMBA SPI2_MISO SPI5_MOSI GTIM1_CH4 ATIM2_BKIN I2C2_SDA I2C4_SDA EVENTOUT	PVD_IN
C8	D1	D1	PA11	I/O	FT	Y	PA11	ATIM1_CH4 SPI2_MOSI ATIM1_CH1N GTIM3_CH1 ATIM1_BKIN2 SPI4_MISO ATIM2_CH3N SPI2_NSS EVENTOUT	-
C8	-	-	PG9	I/O	FT	Y	PG9	SPI3_SCK GTIM8_CH1N SPI2_MOSI GTIM6_CH2 SPI2_MISO SPI1_MISO XSPI_IO6 XSPI_IO5 I2C1_SMBA I2C4_SMBA EVENTOUT	-
B8	C1	C1	PA12	I/O	FT	Y	PA12	ATIM1_ETR GTIM9_CH1 ATIM1_CH2N GTIM3_CH2 SPI4_MOSI SPI2_NSS ATIM2_BKIN SPI2_SCK EVENTOUT	-
B8	-	-	PG4	I/O	FT	Y	PG4	ATIM3_BKIN2 I2C4_SDA SPI1_MOSI GTIM6_ETR ATIM1_BKIN2 GTIM8_CH4 EVENTOUT	-
A8	C2	C2	PA13	I/O	FT	Y	PA13	JTMS-SWDIO GTIM9_CH1N I2C4_SCL I2C1_SCL GTIM3_CH3 GTIM8_CH3 EVENTOUT	IR-OUT
-	B1	B1	VSS	S	-	-	VSS	-	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
A7	B2	B2	PA14	I/O	FT	Y	PA14	JTCK-SWCLK LPTIM1_OUT I2C4_SMBA I2C1_SDA ATIM2_CH2 ATIM1_BKIN GTIM8_CH4 EVENTOUT	-
A6	A2	A2	PA15	I/O	FT	Y	PA15	JTDI SPI3_NSS GTIM1_CH1_ETR SPI1_NSS ATIM2_CH1 I2C1_SCL ATIM1_BKIN ATIM2_CH1N ATIM3_ETR EVENTOUT	-
B7	D3	D3	PC10	I/O	FT	Y	PC10	SPI3_SCK ATIM2_CH1N XSPI_NSS1 GTIM9_CH4 XSPI_IO1 EVENTOUT	-
B6	C3	C3	PC11	I/O	FT	Y	PC11	SPI3_MISO ATIM2_CH2N I2C3_SDA XSPI_CLK GTIM10_ETR ATIM3_CH2 XSPI_NSS0 EVENTOUT	-
C5	B3	B3	PC12	I/O	FT	Y	PC12	SPI3_MOSI GTIM4_CH2 ATIM2_CH3N I2C2_SDA XSPI_IO0 ATIM2_CH2N ATIM3_CH3 SPI6_SCK GTIM8_CH1 EVENTOUT	-
-	-	D5	PD0	I/O	FT	Y	PD0	ATIM2_CH4N SPI4_MISO SPI3_MOSI XSPI_IO1 ATIM3_CH4 SPI2_NSS I2C1_SCL EVENTOUT	-
-	-	D6	PD1	I/O	FT	Y	PD1	ATIM2_CH4 ATIM2_BKIN2 SPI2_NSS XSPI_IO2	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								I2C1_SDA SPI2_SCK EVENTOUT	
B5	A3	A3	PD2	I/O	FT	Y	PD2	GTIM2_ETR ATIM2_BKIN SPI3_NSS XSPI_IO3 ATIM2_CH3N SPI2_MOSI ATIM1_CH4 ATIM2_CH4N ATIM3_CH4 GTIM5_CH2 GTIM8_BKIN EVENTOUT	WKUP5
-	-	E5	PD4	I/O	FT	Y	PD4	GTIM1_CH2 XSPI_IO4 SPI2_MOSI EVENTOUT	-
-	-	D4	PD5	I/O	FT	Y	PD5	XSPI_IO5 GTIM6_CH1 ATIM1_CH4N EVENTOUT	-
-	B6	B6	VDDIO	S	-	-	VDDIO ⁽⁶⁾	-	-
-	A4	A4	PG9	I/O	FT	Y	PG9	SPI3_SCK GTIM8_CH1N SPI2_MOSI GTIM6_CH2 SPI2_MISO SPI1_MISO XSPI_IO6 XSPI_IO5 I2C1_SMBA I2C4_SMBA EVENTOUT	-
-	B4	B4	PG10	I/O	FT	Y	PG10	XSPI_IO2 GTIM7_CH1 SPI1_NSS SPI3_MISO LPTIM1_IN1 GTIM8_CH1 I2C4_SCL ATIM1_CH4N EVENTOUT	-
-	C4	C4	PG11	I/O	FT	Y	PG11	XSPI_IO3 SPI4_SCK GTIM7_CH2 SPI1_SCK SPI3_MOSI LPTIM1_IN2 GTIM8_CH2 I2C4_SDA EVENTOUT	-
-	C5	C5	PG12	I/O	FT	Y	PG12	XSPI_IO1	-

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								SPI4_MISO GTIM7_CH3 SPI6_MISO SPI3_NSS LPTIM1_ETR LPTIM1_IN1 EVENTOUT	
-	B5	B5	PG13	I/O	FT	Y	PG13	XSPI_CLK SPI4_MOSI GTIM7_CH4 SPI6_SCK I2C1_SDA LPTIM1_IN2 EVENTOUT	-
-	A5	A5	PG14	I/O	FT	Y	PG14	XSPI_IO0 SPI4_NSS SPI2_MISO I2C1_SCL GTIM6_CH3 ATIM2_CH4 SPI6_MOSI XSPI_IO7 LPTIM1_ETR LPTIM1_IN1 EVENTOUT	-
A5	A6	A6	PB3	I/O	FT	Y	PB3	JTDO SPI3_SCK GTIM1_CH2 SPI1_SCK GTIM3_ETR ATIM2_CH1N GTIM2_ETR I2C2_SDA ATIM2_BKIN EVENTOUT	-
A5	A6	A6	PF8	I/O	FTa	Y	PF8	GTIM9_CH1 ATIM3_BKIN2 GTIM4_CH3 XSPI_IO0 SPI5_MISO GTIM9_CH1N GTIM6_CH1 ATIM2_CH1N ATIM2_CH2 EVENTOUT	ADC3_IN6

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
A4	C6	C6	PB4	I/O	FT	Y	PB4	NJTRST SPI3_MISO GTIM2_CH1 SPI1_MISO GTIM9_CH1_ETR ATIM2_CH2N GTIM10_BKIN I2C3_SDA ATIM2_ETR LPTIM2_IN1 XSPI_CLK EVENTOUT	-
A4	C6	C6	PF7	I/O	FTa	Y	PF7	GTIM7_CH1 ATIM3_BKIN GTIM4_CH2 XSPI_IO2 SPI5_SCK GTIM8_ETR GTIM10_CH1 EVENTOUT	ADC3_IN5
C4	C7	C7	PB5	I/O	FT	Y	PB5	I2C1_SMBA GTIM2_CH2 SPI1_MOSI SPI3_MOSI GTIM9_BKIN ATIM2_CH3N I2C3_SDA GTIM10_CH1 LPTIM1_IN1 EVENTOUT	-
D3	B7	B7	PB6	I/O	FT	Y	PB6	I2C1_SCL GTIM3_CH1 GTIM9_CH1N ATIM2_CH1 ATIM2_ETR ATIM2_BKIN2 LPTIM1_ETR ATIM3_CH1N I2C4_SCL EVENTOUT	-
D3	B7	B7	PF6	I/O	FTa	Y	PF6	GTIM6_CH1 GTIM4_ETR GTIM3_CH4 I2C2_SCL GTIM4_CH1 XSPI_IO3 SPI5_NSS ATIM1_BKIN2 GTIM9_CH1 EVENTOUT	ADC3_IN4
C3	A7	A7	PB7	I/O	FT	Y	PB7	I2C1_SDA GTIM3_CH2 GTIM10_CH1N ATIM2_BKIN	PVD_IN

Package			Pin name	Pin type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽³⁾	Main Function (After reset)	Optional multiplexed function	
BGA64	BGA72	BGA81						Alternate functions	Additional functions
								GTIM2_CH4 I2C4_SDA LPTIM1_IN2 ATIM3_CH2N EVENTOUT	
C3	A7	A7	PF3	I/O	FTa	Y	PF3	ATIM3_CH4 I2C3_SCL XSPI_IO1 ATIM2_CH3N ATIM2_CH4 EVENTOUT	ADC3_IN9
B4	D7	D7	PH4-BOOT0	I/O	FT	Y	PH4-BOOT0	GTIM4_CH1 GTIM10_CH1N XSPI_IO4 EVENTOUT	-
B3	E7	E7	PB8	I/O	FT	Y	PB8	GTIM3_CH3 GTIM6_CH1 I2C1_SCL SPI5_MOSI GTIM9_CH1 ATIM2_CH2 ATIM1_BKIN GTIM9_CH4 ATIM3_CH3N EVENTOUT	-
A3	E8	E8	PB9	I/O	FT	Y	PB9	SPI2_NSS GTIM3_CH4 GTIM7_CH1 I2C1_SDA GTIM10_CH1 ATIM2_CH3 ATIM1_CH3N ATIM3_CH4N EVENTOUT	IR-OUT
D6	A8	A8	VSS	S	-	-	VSS	-	-
E6	A9	A9	VDD	S	-	-	VDD	-	-

Notes:

1. I = input, O = output, S = power supply.
2. FT: 5V toleran; FTa: 5V tolerant, support analog peripherals; TTa: 3.3V tolerant, support analog peripherals.
3. Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.
4. The RTS_DE, TX, and RX signals of USART3, UART5 and UART8 can be mapped to any IO.
5. The BGA81 and BGA72 packages (PG9 to PG14) support operation via the VDDIO input, accommodating 1.8 to 3.6V input.

The ADC12_INx mentioned in the pin name annotations in the table indicates that this pin can be either ADC1_INx or ADC2_INx. For example, ADC12_IN9 means that this pin can be configured as ADC1_IN9 or ADC2_IN9.

Similarly, the ADC34_INx mentioned in the pin name annotations in the table indicates that this pin can be either ADC3_INx or ADC4_INx.

In the pin PA0 of the table, the multiplexing function GTIM1_CH1_ETR means that this function can be configured as GTIM1_TII or GTIM1_ETR. Similarly, for PA15, the remapping multiplexing function name GTIM1_CH1_ETR has the same meaning.

For the FT ports in the table, it is necessary to ensure that the voltage difference between the IO voltage and the power supply voltage is less than 3.6V.

4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and Maximum Values

The minimum and maximum values in the Beta version are based on design simulations.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean $\pm 3\Sigma$).

4.1.2 Typical Values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^\circ\text{C}$ and $V_{DD} = 3.3\text{V}$ (for the $1.8\text{V} \leq V_{DD} \leq 3.6\text{V}$ voltage range). These data are for design guidance only and not tested.

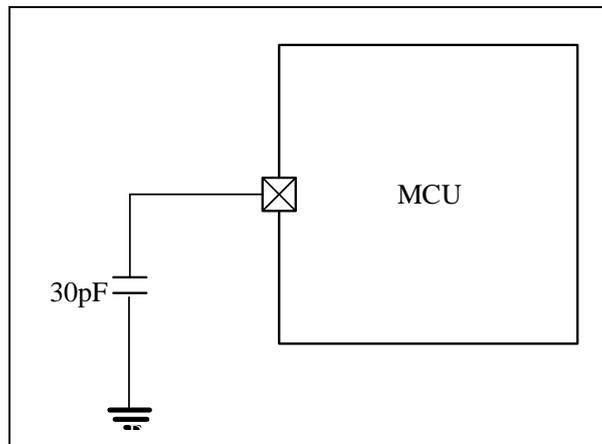
4.1.3 Typical Curves

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading Capacitor

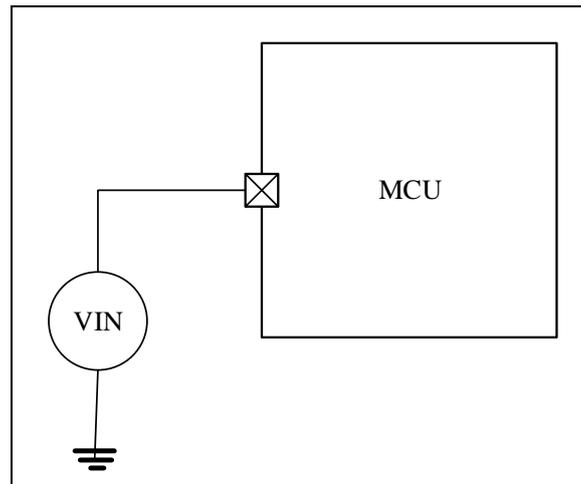
The load conditions for measuring pin parameters are shown Figure 4-1:

Figure 4-1 Load Conditions Of Pins



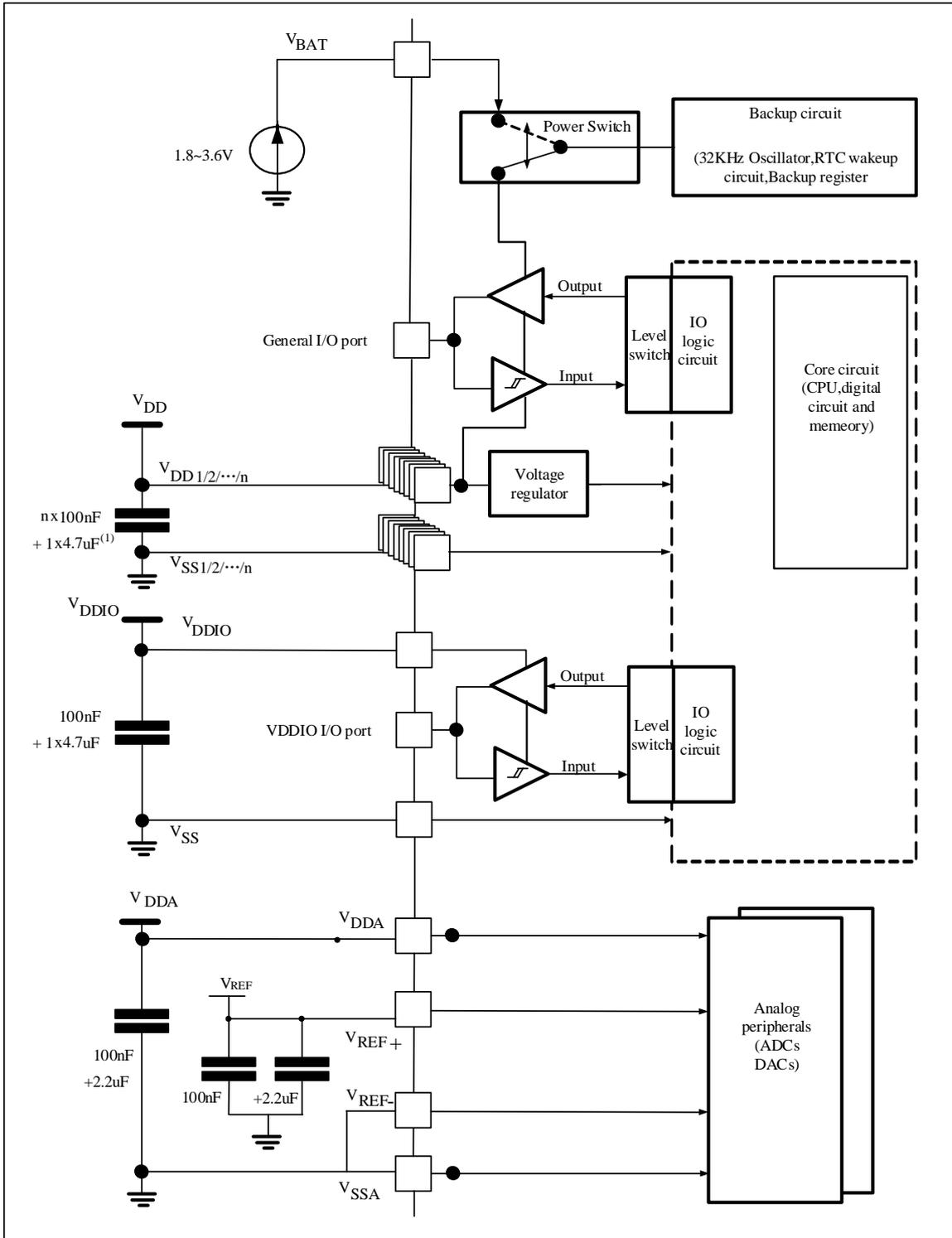
4.1.5 Pin Input Voltage

The measurement of the input voltage on the pin is shown Figure 4-2:

Figure 4-2 Pin Input Voltage

4.1.6 Power Supply Scheme

Figure 4-3 Power Supply Scheme

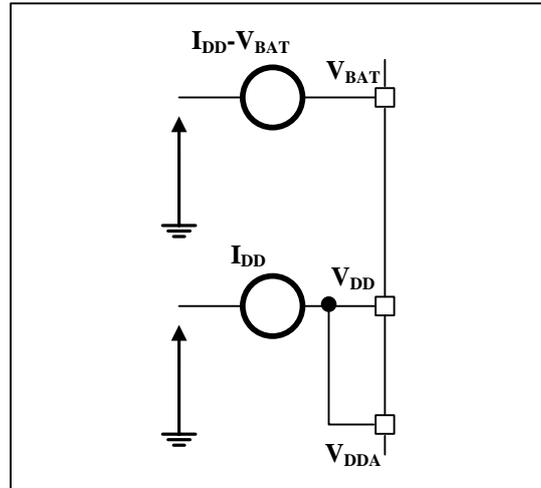


Note:

- (1) The $4.7\mu\text{F}$ capacitor shown in the diagram must be connected to the designated main V_{DD} pin.
- (2) For BGA81 and BGA72 packages, the pins supporting independent V_{DDIO} power supply are PG9 to PG14, For LQFP144 packages, the pins supporting independent V_{DDIO} power supply are PD6~PD7, PG9~PG15.

4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins ⁽³⁾	$V_{SS} - 0.3$	5.5	
	Input voltage on other pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
$ \Delta V_{DDx} $	Voltage difference between different supply pins	-	50	mV
$ V_{SSx} - V_{SS} $	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		-

Notes:

- (1) All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
- (2) V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.
- (3) When a 5V tolerant pin inputs 5.5V, V_{DD} cannot be lower than 2.25V.

Table 4-2 Current Characteristics

Symbol	Describe	Max ⁽¹⁾	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) ⁽¹⁾⁽⁴⁾	400	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) ⁽¹⁾⁽⁴⁾	400	
I_{IO}	Output current sunk by I/O and control pins	12	
	Output current source by I/O and control pins	-12	
$I_{IN(PIN)}^{(2)(3)}$	Injection current on NRST pin	-5/0	
	Injection current on other pins	+/-5	

Notes:

- (1) All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
- (2) When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current. $I_{IN(PIN)}$ should not exceed its maximum value. Refer to Table 4-1 for voltage characteristics.
- (3) Reverse injection current can interfere with the analog performance of the device. See section 4.3.1926.
- (4) When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is $0.1V_{DD}$.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	- 65 ~ + 150	°C
T_J	Maximum junction temperature	125	°C

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	240	MHz
f_{PCLK}	Internal APB1/2 clock frequency	-	0	180	
V_{DDA}	Analog operating of working voltage	Must be the same potential as $V_{DD}^{(1)}$	1.8	3.6	V
V_{BAT}	Backup domain supply voltage	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	°C
T_J	Junction temperature range	7 suffix version	-40	125	°C

(1) It is recommended that the same power supply be used to power the V_{DD} and V_{DDA} . During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA} .

4.3.2 Operating Conditions at Power-on and Power-down

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating Conditions At Power-On And Power-Down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	20	∞	$\mu\text{s}/\text{V}$
	V_{DD} fall time rate		80	∞	

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Features Of Embedded Reset And Power Control Modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (MSB of PWR_CTRL)	PRS[2:0]=000 (rising edge)	-	2.18	-	V
		PRS[2:0]=000 (falling edge)	-	2.08	-	V
		PRS[2:0]=001 (rising edge)	-	2.28	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	is 0)	PRS[2:0]=001 (falling edge)	-	2.18	-	V
		PRS[2:0]=010 (rising edge)	-	2.38	-	V
		PRS[2:0]=010 (falling edge)	-	2.28	-	V
		PRS[2:0]=011 (rising edge)	-	2.48	-	V
		PRS[2:0]=011 (falling edge)	-	2.38	-	V
		PRS[2:0]=100 (rising edge)	-	2.58	-	V
		PRS[2:0]=100 (falling edge)	-	2.48	-	V
		PRS[2:0]=101 (rising edge)	-	2.68	-	V
		PRS[2:0]=101 (falling edge)	-	2.58	-	V
		PRS[2:0]=110 (rising edge)	-	2.78	-	V
		PRS[2:0]=110 (falling edge)	-	2.68	-	V
		PRS[2:0]=111 (rising edge)	-	2.88	-	V
		PRS[2:0]=111 (falling edge)	-	2.78	-	V
		Programmable voltage detector level selection (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	-	1.78	-
	PRS[2:0]=000 (falling edge)		-	1.68	-	V
	PRS[2:0]=001 (rising edge)		-	1.88	-	V
	PRS[2:0]=001 (falling edge)		-	1.78	-	V
	PRS[2:0]=010 (rising edge)		-	1.98	-	V
	PRS[2:0]=010 (falling edge)		-	1.88	-	V
	PRS[2:0]=011 (rising edge)		-	2.08	-	V
	PRS[2:0]=011 (falling edge)		-	1.98	-	V
	PRS[2:0]=100 (rising edge)		-	3.28	-	V
	PRS[2:0]=100 (falling edge)		-	3.18	-	V
	PRS[2:0]=101 (rising edge)		-	3.38	-	V
	PRS[2:0]=101 (falling edge)		-	3.28	-	V
	PRS[2:0]=110 (rising edge)	-	3.48	-	V	
PRS[2:0]=110 (falling edge)	-	3.38	-	V		
PRS[2:0]=111 (rising edge)	-	3.58	-	V		
PRS[2:0]=111 (falling edge)	-	3.48	-	V		
V _{PVDhyst} ⁽¹⁾	PVD hysteresis	-	-	100	-	mV
V _{POR}	VDD power on/power down reset threshold	-	-	1.66/1.58	-	V
V _{BOR}	BOR power on/off reset threshold	BOR_LVL[2:0]=000 (rising edge)	-	1.66	-	V
		BOR_LVL[2:0]=000 (falling edge)	-	1.62	-	V
		BOR_LVL[2:0]=001 (rising edge)	-	2.1	-	V
		BOR_LVL[2:0]=001 (falling edge)	-	2	-	V
		BOR_LVL[2:0]=010 (rising edge)	-	2.3	-	V
		BOR_LVL[2:0]=010 (falling edge)	-	2.2	-	V
		BOR_LVL[2:0]=011 (rising edge)	-	2.6	-	V
		BOR_LVL[2:0]=011 (falling edge)	-	2.5	-	V
		BOR_LVL[2:0]=100 (rising edge)	-	2.9	-	V
		BOR_LVL[2:0]=100 (falling edge)	-	2.8	-	V
TRSTTEMPO ⁽¹⁾	Reset duration	-	-	0.8	4	ms

(1) Guaranteed by design, not tested in production.

4.3.4 Embedded Reference Voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Internal Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$	1.164	1.2	1.236	V
$T_{S_vrefint}^{(1)}$	The sampling time of the ADC when reading the internal reference voltage	-	-	5.1	17.1 ⁽²⁾	μs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DD} = 3.3\text{V}$ $-40^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$	-14	-	14	mV

Notes:

(1) The shortest sampling time is obtained through multiple loops in the application.

(2) Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, toggle rate of I/O pins, program location in memory, and executed code.

The measurement method of current consumption is described in **Figure 4-4**.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum Current Consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting period from 0 to 48 MHz, 1 waiting period from 48 to 96 MHz, 2 waiting periods from 96 to 144 MHz, 3 waiting periods from 144 to 192 MHz, 4 waiting periods from 192 to 240 MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$.
- V_{DD} is 3.63V, ambient temperature is 105°C

The parameters given in Table 4-8 and Table 4-9 are based on tests at the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Maximum Current Consumption In Operating Mode Where Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ ⁽¹⁾				Unit
				$T_A = -40^{\circ}\text{C}$	$T_A = 25^{\circ}\text{C}$	$T_A = 85^{\circ}\text{C}$	$T_A = 105^{\circ}\text{C}$	
I_{DD}	Supply current in operation mode	External clock ⁽²⁾ , enable all peripherals	240MHz	63.8	67	80.7	103.8	mA
			180MHz	47.8	50.7	63.7	86	
			120MHz	33.93	36.53	48.63	69.63	
			60MHz	20.25	22.55	33.65	53.65	

	External clock ⁽²⁾ , disable all peripherals	240MHz	27.3	29.7	41.1	50.2
		180MHz	21.7	24	35.1	44
		120MHz	16.9	18.2	29.5	38.1
		60MHz	10.1	12.1	22.6	31.3

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) Enable PLL when $f_{HCLK} > 8MHz$.

Table 4-9 Maximum Current Consumption In Sleep Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ ⁽¹⁾				Unit
				$T_A = -40^\circ C$	$T_A = 25^\circ C$	$T_A = 85^\circ C$	$T_A = 105^\circ C$	
I_{DD}	Supply current in sleep mode	External clock ⁽²⁾ , enable all peripherals	240MHz	55.9	59	72.1	94.8	mA
			180MHz	43.4	46.3	58.7	80.4	
			120MHz	33.25	35.85	47.55	68.25	
			60MHz	19.1	21.3	32.2	52	
		External clock ⁽²⁾ , disable all peripherals	240MHz	18.9	21.2	31.9	40.8	
			180MHz	15.2	17.4	28	36.8	
			120MHz	12.3	13.4	24.4	31	
			60MHz	7.8	9.8	20.1	28.7	

Notes:

(1) Based on comprehensive evaluation result, not tested in production.

(2) Enable PLL when $f_{HCLK} > 8MHz$.

4.3.5.2 Current consumption in Low-Power Mode

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disable unless otherwise noted.

Table 4-10 Typical Current Consumption In Low Power Mode

Symbol	Parameter	Conditions	Typ ⁽¹⁾				Unit
			$T_A = -40^\circ C$	$T_A = 25^\circ C$	$T_A = 85^\circ C$	$T_A = 105^\circ C$	
I_{DD}	Supply current in STOP0 mode	Regulator in run mode, LSE on, RTC on, IWDG off, Backup SRAM hold	1.5	2.9	12.3	20.7	mA
		Regulator in LP mode, LSE on, RTC on, IWDG off, Backup SRAM hold	1	1.7	7.3	13.9	
I_{DD}	Supply current in STANDBY mode	LSE on, RTC on, IWDG off, BackupSRAM hold	1.98	3.75	20.8	39	uA
		LSE on, RTC off, IWDG off, BackupSRAM hold	1.98	3.75	20.49	39.05	
		LSE on, RTC off, IWDG off, BackupSRAM not holding	1.98	3.76	20.13	38.01	

I _{DD_VBAT}	Supply current in VBAT mode	LSE on, RTC on, IWDG off, Backup SRAM hold	1.13	2.71	16.8	30.82	uA
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(1) Based on comprehensive evaluation result, not tested in production.

4.3.5.3 Peripheral current consumption

Table 4-11 Peripheral current consumption

Bus	Peripheral	Typ	Unit
AHB	DMA1	4.37	μA/MHz
	DMA2	4.37	
	FEMC	6.01	
	XSPI	11.67	
AHB1	BKP SRAM	0.41	μA/MHz
	CRC	0.2	
AHB2	ATIM1	9.05	μA/MHz
	ATIM2	9.12	
	ATIM3	8.55	
AHB3	GPIOA	14.01	μA/MHz
	GPIOB	14.2	
	GPIOC	14.34	
	GIOD	14.28	
	GPIOE	14.12	
	GPIOF	14.66	
	GPIOG	14.31	
	GPIOH	13.78	
	ADC1	10.04	
	ADC2	8.16	
	ADC3	7.81	
	SAC	1.83	
	APB1	DAC1/2	
I2C1		2.72	
I2C2		2.72	
I2C3		2.72	
I2C4		2.72	
LPTIM1		2.27	
LPTIM2		2.27	
UART5		2.51	
UART8		2.51	
GTIM1		7.03	
GTIM2		4.86	

	GTIM3	4.75	
	GTIM4	6.79	
	GTIM5	5.47	
	GTIM6	4.49	
	GTIM7	4.68	
	BTIM1	0.22	
	BTIM2	0.22	
	SPI2	2.69	
	SPI3	2.69	
	USART3	2.82	
	RTC	3.52	
	WWDG	0.28	
	PWR	1.94	
APB2	SPI1	1.46	$\mu\text{A}/\text{MHz}$
	SPI4	1.32	
	SPI6	1.33	
	GTIM8	2.51	
	GTIM9	13.61	
	GTIM10	13.34	

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Source (HSE)

The characteristic parameters given in the following table are measured using a high-speed external clock source (Bypass mode), and the ambient temperature and supply voltage meet the conditions specified in **Table 4-4**.

Table 4-12 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSE_ext}}$	User external clock frequency ⁽¹⁾	-	1	8	50	MHz
V_{HSEH}	OSC_IN Input pin high level voltage		$0.7V_{\text{DD}}$	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage		V_{SS}	-	$0.3V_{\text{DD}}$	
$t_{\text{w(HSE)}}$	Time when OSC_IN is high or low ⁽¹⁾		16	-	-	ns
$t_{\text{r(HSE)}}$	OSC_IN rise or fall time ⁽¹⁾		-	-	20	
$t_{\text{f(HSE)}}$						
DuCy _(HSE)	Duty cycle		-	45	-	55
I_{L}	OSC_IN Input leakage current	$V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}}$	-1	-	+1	μA

(1) Guaranteed by design, not tested in production.

4.3.6.2 Low-Speed External Clock Source (LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source

(Bypass mode), and the ambient temperature and supply voltage meet the conditions specified in Table 4-4.

Table 4-13 Low-Speed External User Clock Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency ⁽¹⁾	-	8.8	32.768	1000	KHz
V_{LSEH}	OSC32_IN Input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN Input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	mV
$t_{w(LSE)}$	OSC32_IN High or low time ⁽¹⁾		450	-	-	ns
$t_{w(LSE)}$						
$t_{r(LSE)}$	OSC32_IN Rise or fall time ⁽¹⁾		-	-	50	ns
$t_{f(LSE)}$						
$DuCy_{(LSE)}$	Duty ratio		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

(1) Guaranteed by design, not tested in production.

Figure 4-5 AC Timing Diagram Of An External High Speed Clock Source

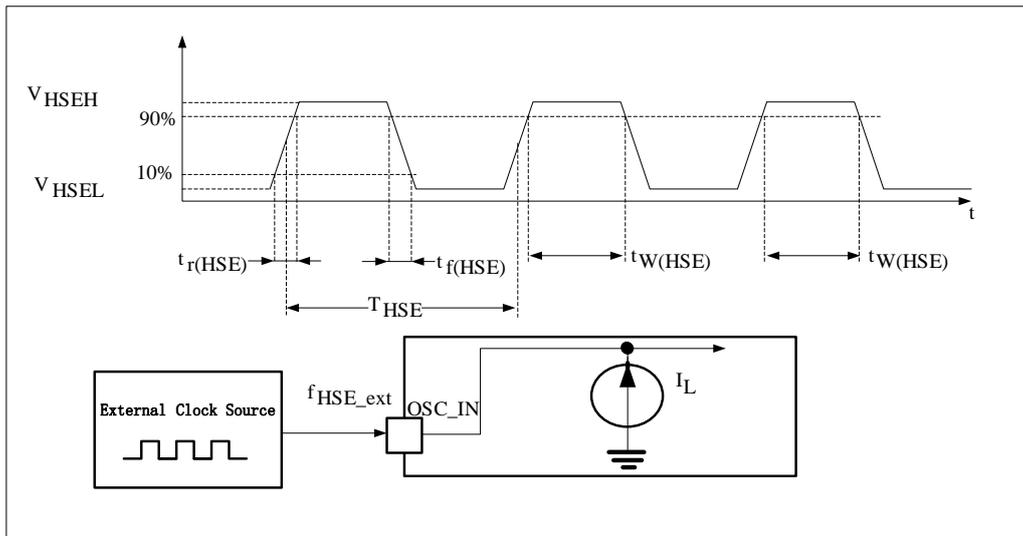
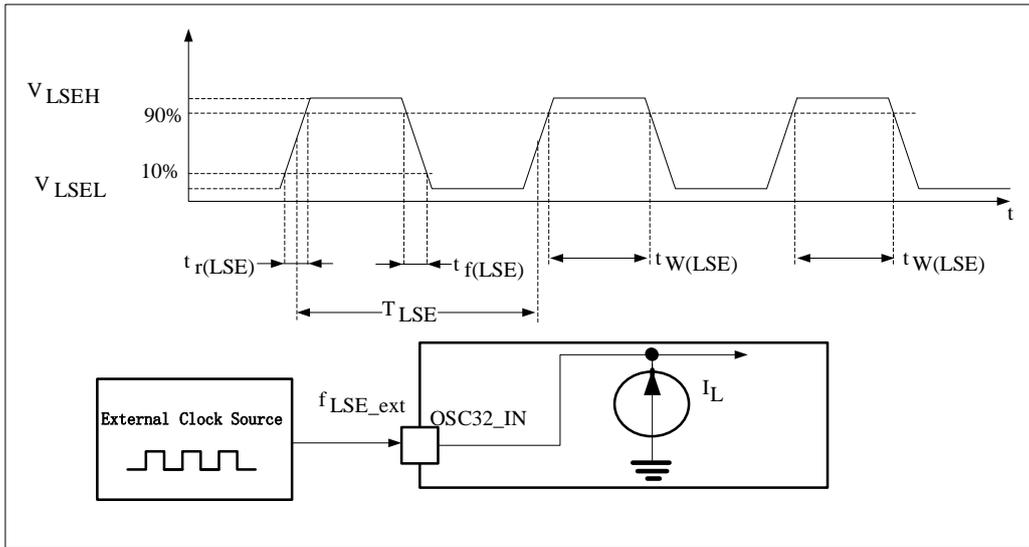


Figure 4-6 AC Timing Diagram Of An External Low Speed Clock Source


High-speed external clock generated using a crystal/ceramic resonator

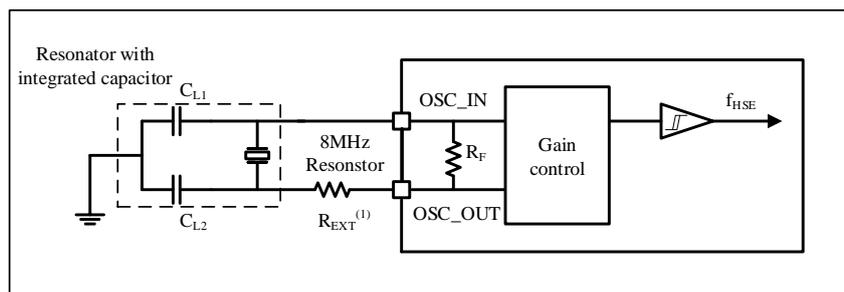
High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Table 4-14 HSE 4~32MHz Oscillator Characteristics ^{(1) (2)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	380	-	k Ω
i_2	HSE drive current	$V_{DD} = 3.3V$, $V_{IN} = V_{SS}$ 30 pf load	-	1.8	-	mA
g_m	Transconductance of the oscillator	Start	-	10	-	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time (8M crystal)	V_{DD} is stabilized	-	10	-	mA/V

Notes:

- (1) The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
- (2) Guaranteed by characterization results, not tested in production.
- (3) $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-7 Typical Application Using 8 MHz Crystal


(1) The R_{EXT} value depends on the properties of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2} , it is recommended to use high quality ceramic dielectric containers, and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2} .

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example: If a resonator with load capacitance $C_L = 6pF$ is selected and $C_{stray} = 2pF$, then $C_{L1} = C_{L2} = 8pF$.

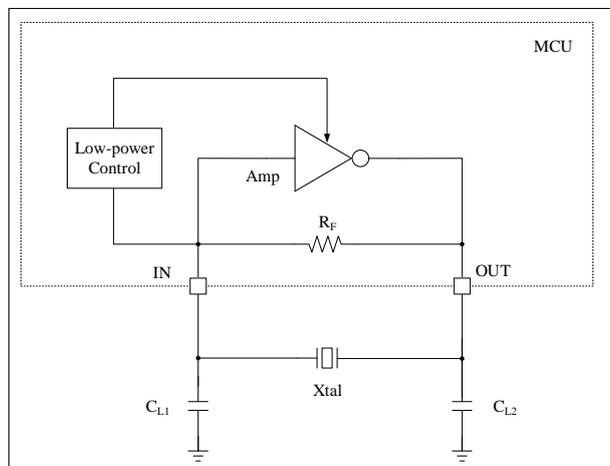
Table 4-15 LSE Oscillator Characteristics ($F_{LSE} = 32.768KHz$)⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
I_2	LSE drive current	Low drive capability	-	300	-	nA
		Medium drive capability	-	750	-	
		High drive capability	-	1000	-	
g_m	Maximum transconductance	Low drive capability	-	9	-	μA/V
		Medium drive capability	-	12	-	
		High drive capability	-	27	-	
$t_{SU(LSE)}^{(2)}$	Startup time	V_{DD} is stabilized	-	2	-	s

Notes:

- (1) Guaranteed by design, not tested in production.
- (2) $t_{SU(LSE)}$ is the starting time, which is the period from the LSE enabled by the software to the stable 32.768 khz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-8 Typical Application Of 32.768KHz Crystal



4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-4.

4.3.7.1 High Speed Internal (HSI) RC Oscillator

Table 4-16 HSI Oscillator Characteristics ^{(1) (2)}

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$, after calibration	7.96 ⁽³⁾	8	8.04 ⁽³⁾	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$	-1.5	-	2	%
		$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = -10\sim 85^{\circ}\text{C}$	-0.8	-	1.5	%
		$V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}} = 0\sim 70^{\circ}\text{C}$	-0.5	-	1.3	%
$t_{\text{SU(HSI)}}$	HSI oscillator start time	-	-	-	6	μs
$I_{\text{DD(HSI)}}$	HSI oscillator power consumption	-	-	100	120	μA

Notes:

(1) $V_{\text{DD}} = 3.3\text{V}$, $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$ unless otherwise specified.

(2) Guaranteed by design, not tested in production.

(3) Production calibration accuracy, excluding soldering effects. Soldering introduces a frequency deviation range of approximately $\pm 1\%$.

(4) Frequency deviation includes the effects of soldering, data is from sample testing, not tested in production.

4.3.7.2 Low Speed Internal (LSI) RC Oscillator

Table 4-17 LSI Oscillator Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{LSI}}^{(2)}$	Output frequency	25 $^{\circ}\text{C}$ calibration, $V_{\text{DD}} = 3.3\text{V}$	-	32	-	KHz
		$V_{\text{DD}} = 1.8\text{V}$ to 3.6V , $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$	28.8	32	35.2	KHz
$t_{\text{SU(LSI)}}^{(2)}$	LSI oscillator startup time	-	-	60	84	μs
$I_{\text{DD(LSI)}}^{(2)}$	LSI oscillator power consumption	-	-	0.6	-	μA

Notes:

(1) $V_{\text{DD}} = 3.3\text{V}$, $T_{\text{A}} = -40\sim 105^{\circ}\text{C}$ unless otherwise specified.

(2) Guaranteed by characterization results, not tested in production.

4.3.8 Wake Up Time from Low Power Mode

The wake-up time listed in Table 4-18 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP0 or STANDBY mode: clock source is RC oscillator
- SLEEP mode: The clock source is the clock used to enter SLEEP mode

All times were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-18 Wake Time In Low Power Mode

Symbol	Parameter	Typ ⁽¹⁾	Unit
--------	-----------	--------------------	------

twUSLEEP	Wake up from SLEEP mode	6	Cycles
twUSTOPO	Wake up from STOP0 mode (regulator in run mode)	20	μs
	Wake up from STOP0 mode (regulator in low power mode)	22	μs
twUSTDBY	Wake up from STANDBY mode	100	μs

(1) The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.

4.3.9 PLL Characteristics

The parameters listed in Table 4-19 are measured when the ambient temperature and power supply voltage meet the conditions in Table 4-4

Table 4-19 PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f _{PLL_IN}	PLL PFD input clock ⁽²⁾	4	8	50	MHz
	PLL Input clock duty cycle	40	50	60	%
f _{PLL_OUT}	PLL output clock ⁽²⁾	32	-	240	MHz
t _{LOCK}	PLL Ready indicates signal output time ⁽³⁾	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @240MHz	-	5	-	ps
I _{PLL}	Operating Current of PLL @240MHz VCO frequency.	-	-	1500	uA

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) The correct configuration coefficients need to be used so that the f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

4.3.10 FLASH Memory Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105°C.

Table 4-20 Flash Memory Characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
t _{prog}	64-bit programming time	T _A = -40 ~ 105 °C, double word mode	-	40	-	μs
		T _A = -40 ~ 105 °C, buffer program mode	-	19	-	
t _{ERASE}	Page (16K byte) erase time, single-bank mode	T _A = -40~105°C	-	24	40	ms
	Page (8K byte) erase time, dual-bank mode	T _A = -40~105°C	-	12	20	ms
t _{ME}	Mass erase time, single-bank mode	T _A = -40~105°C	-	28	40	ms
	Mass erase time (bank1 + bank2), dual-bank mode	T _A = -40~105°C	-	28	40	ms
I _{DD}	The power supply current	Read mode, f _{HCLK} = 240 MHz, 4 waiting cycles, V _{DD} = 3.3V	-	4.2	5.45	mA
		Write mode, f _{HCLK} = 240 MHz, V _{DD} = 3.3V	-	6.5	-	mA
		Erase mode, f _{HCLK} = 240 MHz, V _{DD} = 3.3V	-	4.5	-	mA
		Power-down/stop mode, V _{DD} = 3.3~3.6V	-	0.05	4.65	μA

Symbol	Parameter	Condition	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
V _{prog}	Programming voltage	-	1.8	3	3.6	V

Note:

(1) Guaranteed by design, not tested in production.

Table 4-21 Flash Endurance And Data Retention Life

Symbol	Parameter	Condition	Min ⁽¹⁾	Unit
N _{END}	Endurance (note: erasure times)	T _A = -40~105 °C, Flash size is 512 KB	10	Kcycle
t _{RET}	Data retention period	10 kcycle ⁽²⁾ at T _A = 85 °C	20	Years
		10 kcycle ⁽²⁾ at T _A = 105 °C	15	
		10 kcycle ⁽²⁾ at T _A = 125 °C	10	

(1) Based on comprehensive evaluation, not tested in production.

4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, ES, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-22 Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Max ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
V _{ESD(CDM)⁽²⁾}	Electrostatic discharge voltage (charging device model)	T _A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	C3	1000	

(1) Based on comprehensive evaluation, not tested in production.

(2) LQFP144 VBAT pin voltage maximum 500V

Electromagnetic susceptibility (EMS)

Table 4-23 EMS Features

Symbol	Parameter	Condition	Level
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD = 3.3V, LQFP144, T _A = 25 °C, HCLK = 240MHz, conforms to IEC 61000-4-2	4A
V _{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	VDD = 3.3V, LQFP144, T _A = 25 °C, HCLK = 240MHz, conforms to IEC 61000-4-4	4A
	Fast transient voltage burst and capacitively coupled clamping limits to be applied on I/O pins to induce a functional disturbance	VDD = 3.3V, LQFP144, T _A = 25 °C, HCLK = 240MHz, conforms to IEC 61000-4-4	4A

Static latch-up (LU)

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78A IC latch standard.

Table 4-24 Static Latch-Up

Symbol	Parameter	Condition	Type	Min
LU ⁽¹⁾	Static lock-up class	T _A = +125 °C, in accordance with JESD 78E	II class A	±100mA, 1.5*VDDMAX

(1) Pins PA4 and PA5 meet I class A standards, passing tests at ±200mA at 25 °C and ±80mA at 85 °C.

4.3.12 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-25 I/O Static Characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
V _{IL}	Input low level voltage	V _{DD} =3.3V	V _{SS}	-	0.8	V
		V _{DD} =2.5V	V _{SS}	-	0.7	
		V _{DD} =1.8V	V _{SS}	-	0.3*V _{DD}	
V _{IH}	Input high level voltage	V _{DD} =3.3V	2	-	V _{DD}	V
		V _{DD} =2.5V	1.7	-	V _{DD}	
		V _{DD} =1.8V	0.7*V _{DD}	-	V _{DD}	
V _{hys}	Schmidt trigger voltage hysteresis ⁽¹⁾	V _{DD} =3.3V	200	-	-	mV
		V _{DD} =2.5V	200	-	-	
		V _{DD} =1.8V	0.1*V _{DD} ⁽²⁾	-	-	
I _{lkg}	Input leakage current ⁽³⁾	V _{DD} =Maximum	-1	-	1	μA
		V _{PAD} =0 or V _{PAD} =V _{DD} ⁽⁵⁾				
R _{PU}	Weak pull-up equivalent resistor ⁽⁴⁾	V _{DD} =3.3V, V _{IN} = V _{SS}	80	-	220	kΩ
		V _{DD} =1.8~3.3V, V _{IN} = V _{SS}	60	-	500	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽⁴⁾	V _{DD} =3.3V, V _{IN} = V _{DD}	80	-	220	kΩ
		V _{DD} =1.8~3.3V, V _{IN} = V _{DD}	60	-	500	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

Notes:

(1) The hysteresis voltage of Schmitt trigger switching level. Based on comprehensive evaluation, not tested in production.

(2) At least 100mV.

(3) If there is reverse current injection from adjacent pins, the leakage current may be higher than the maximum value.

(4) Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

(5) V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

Output driving current

GPIO (universal input/output port) can absorb or output up to +/-12mA current. In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in Section 4.2.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating value I_{VDD} (Table 4-2)
- The sum of the currents sourced by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sourced

on V_{SS} , cannot exceed the absolute maximum rating value I_{VSS} (Table 4-2)

Output voltage

Unless otherwise specified, the parameters listed in Table 4-27 were measured using ambient temperature and V_{DD} supply voltage in accordance with Table 4-4. All I/O ports are CMOS and TTL compatible

Table 4-26 IO Output Drive Capability Characteristics⁽¹⁾

Drive Capability	I_{OH} , VDD=3.3V	I_{OL} , VDD=3.3V	I_{OH} , VDD=2.5V	I_{OL} , VDD=2.5V	I_{OH} , VDD=1.8V	I_{OL} , VDD=1.8V	Unit
2	-2	2	-1.5	1.5	-1	1	mA
4	-4	4	-3	3	-2	2	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7	8	mA

(1) Guaranteed by design, not tested in production.

Table 4-27 Output Voltage Characteristics⁽³⁾

Symbol	Parameter	Condition	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level	$V_{DD}=3.3V, I_{OL}^{(4)}=2/4/8/12$	V_{SS}	0.4	V
		$V_{DD}=2.5V, I_{OL}^{(4)}=2/4/8/12$	V_{SS}	0.4	
		$V_{DD}=1.8V, I_{OL}^{(4)}=2/4/8/12$	V_{SS}	$0.2 \cdot V_{DD}$	
$V_{OH}^{(2)}$	Output high level	$V_{DD}=3.3V, I_{OH}^{(4)}=2/4/8/12$	$2.4^{(5)}$	V_{DD}	V
		$V_{DD}=2.5V, I_{OH}^{(4)}=2/4/8/12$	$1.8^{(5)}$	V_{DD}	
		$V_{DD}=1.8V, I_{OH}^{(4)}=2/4/8/12$	$0.8 \cdot V_{DD}$	V_{DD}	

Notes:

- (1) The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS} .
- (2) The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD} .
- (3) Data based on characterization results, not tested in production
- (4) Actual drive capability see Table 4-26.
- (5) PC13, PC14, PC15 are not within this range.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in Figure 4-9 and Table 4-28 respectively.

Unless otherwise specified, the parameters listed in Table 4-28 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-28 Input/Output AC Characteristics⁽¹⁾

DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	$f_{\max(1O)out}$	Maximum frequency ⁽²⁾	$C_L=5pF, V_{DD}=3.3V$	-	75	MHz
			$C_L=5pF, V_{DD}=2.5V$	-	50	
			$C_L=5pF, V_{DD}=1.8V$	-	30	
	$t_{(1O)out}$	Output delay	$C_L=5pF, V_{DD}=3.3V$	-	3.7	ns
			$C_L=5pF, V_{DD}=2.5V$	-	4.8	
			$C_L=5pF, V_{DD}=1.8V$	-	7.2	
$t_{(1O)in}$	Input delay	$CL=50fF, V_{DD}=2.97V, V_{DDD}=0.81V$ input characteristics at 1.8V and 2.5V are derated	-	2	ns	
10 (4mA)	$f_{\max(1O)out}$	Maximum frequency ⁽²⁾	$C_L=10pF, V_{DD}=3.3V$	-	90	MHz
			$C_L=10pF, V_{DD}=2.5V$	-	60	

DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
	$t_{(IO)out}$	Output delay	$C_L=10pF, V_{DD}=1.8V$	-	40	ns
			$C_L=10pF, V_{DD}=3.3V$	-	3.5	
			$C_L=10pF, V_{DD}=2.5V$	-	4.5	
			$C_L=10pF, V_{DD}=1.8V$	-	6.8	
	$t_{(IO)in}$	Input delay	$CL=50fF, V_{DD}=2.97V, V_{DDD}=0.81V$ input characteristics at 1.8V and 2.5V are derated	-	2	
01 (8mA)	$f_{max(IO)out}$	Maximum frequency ⁽²⁾	$C_L=20pF, V_{DD}=3.3V$	-	100	MHz
			$C_L=20pF, V_{DD}=2.5V$	-	75	
			$C_L=20pF, V_{DD}=1.8V$	-	50	
	$t_{(IO)out}$	Output delay	$C_L=20pF, V_{DD}=3.3V$	-	3.5	ns
			$C_L=20pF, V_{DD}=2.5V$	-	4.8	
			$C_L=20pF, V_{DD}=1.8V$	-	6.6	
	$t_{(IO)in}$	Input delay	$CL=50fF, V_{DD}=2.97V, V_{DDD}=0.81V$ input characteristics at 1.8V and 2.5V are derated	-	2	
11 (12mA)	$f_{max(IO)out}$	Maximum frequency ⁽²⁾	$C_L=30pF, V_{DD}=3.3V$	-	120	MHz
			$C_L=30pF, V_{DD}=2.5V$	-	90	
			$C_L=30pF, V_{DD}=1.8V$	-	60	
	$t_{(IO)out}$	Output delay	$C_L=30pF, V_{DD}=3.3V$	-	3.4	ns
			$C_L=30pF, V_{DD}=2.5V$	-	4.3	
			$C_L=30pF, V_{DD}=1.8V$	-	6.4	
	$t_{(IO)in}$	Input delay	$CL=50fF, V_{DD}=2.97V, V_{DDD}=0.81V$ input characteristics at 1.8V and 2.5V are derated	-	2	

Notes:

- (1) The speed of the I/O port can be configured via PMODEy [1:0]. Refer to the N32H493 user manual for instructions on configuring registers for GPIO ports.
- (2) The maximum frequency is defined in **Figure 4-9**.

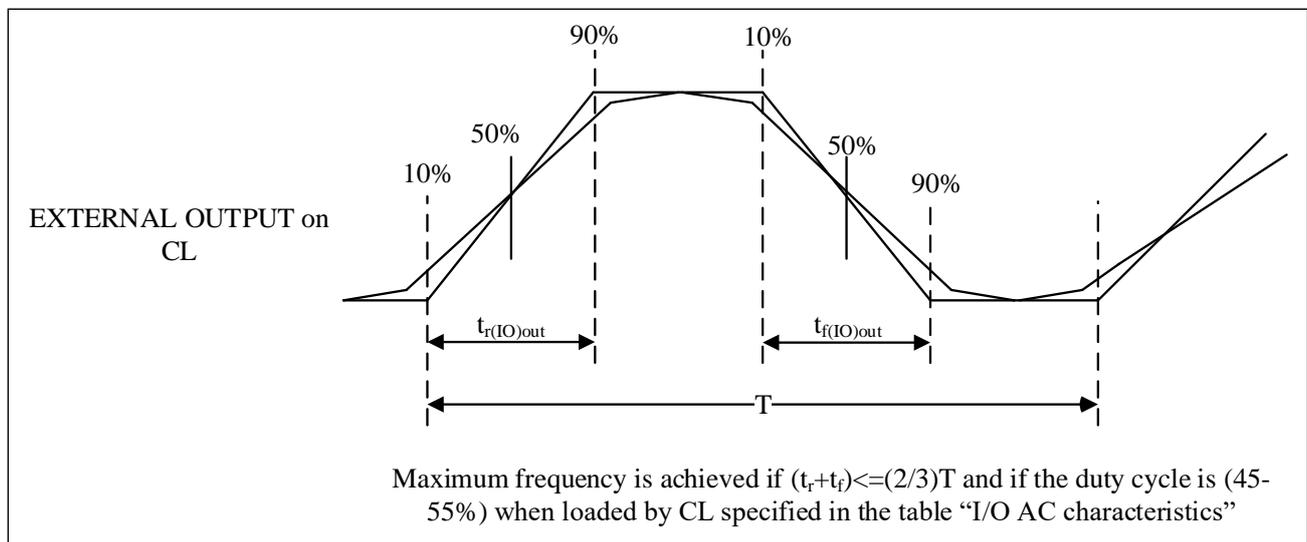
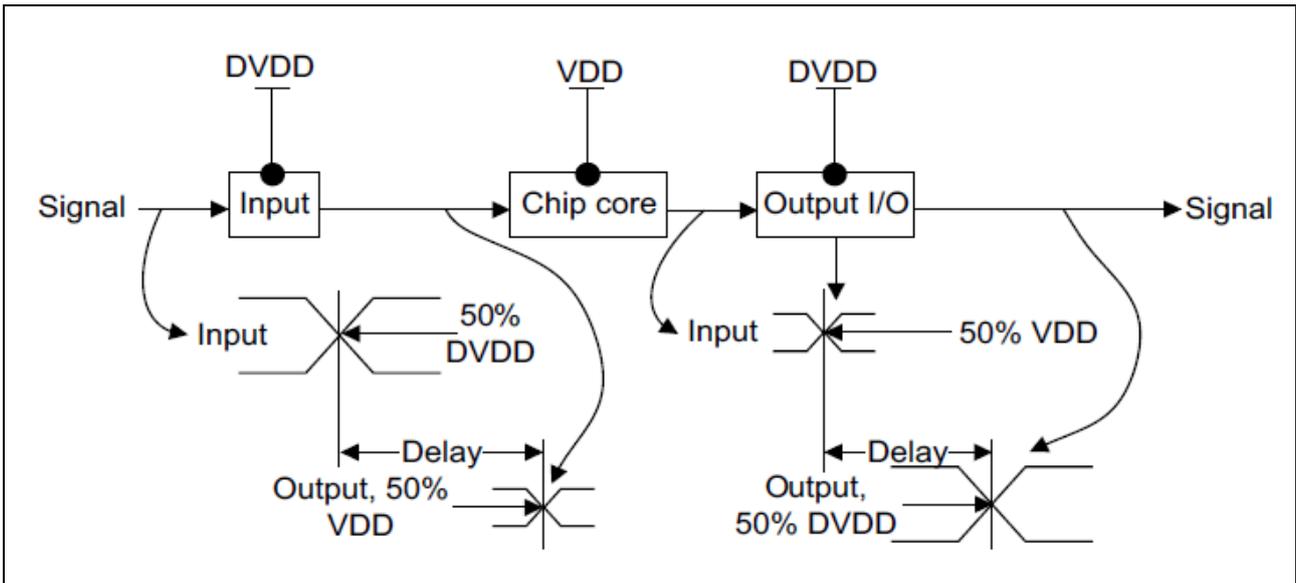
Figure 4-9 Definition Of Input/Output AC Characteristics


Figure 4-10 Transmission Delay


4.3.13 NRST Pin Characteristics

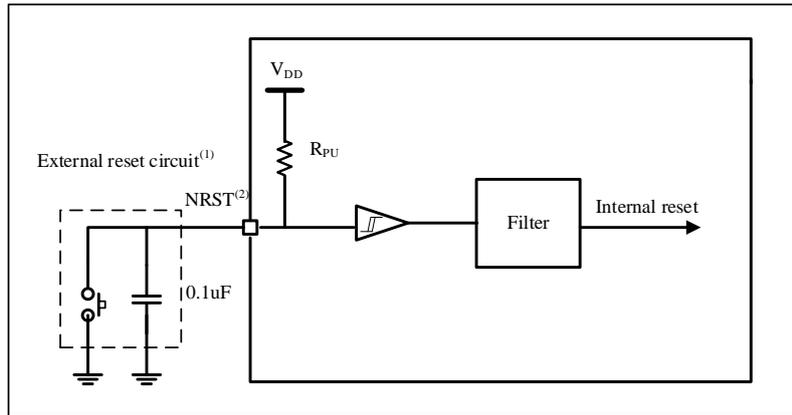
The NRST pin input driver uses the CMOS process, which is connected to an unbreakable pull-up resistor, R_{PU} (see **Table 4-29**). Unless otherwise specified, the parameters listed in **Table 4-29** were measured using ambient temperature and supply voltage in accordance with **Table 4-4**.

Table 4-29 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage	-	V_{SS}	-	$0.3 \cdot V_{DD}$	V
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage	-	$0.7 \cdot V_{DD}$	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance ⁽²⁾	$V_{IN} = V_{SS}$	30	50	80	k Ω
$V_{F(NRST)}^{(1)}$	NRST input filter pulse	$V_{DD} = 3.3V$	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST input unfiltered pulse	$V_{DD} = 3.3V$	300	-	-	ns

Notes:

- (1) *Guaranteed by design, not tested in production.*
- (2) *The pull-up resistor is designed as a real resistor in series for a switchable PMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).*

Figure 4-11 Recommended NRST Pin Protection


Notes:

(1) Acts as a filter.

(2) The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in **Table 4-29**, otherwise the MCU cannot be reset.

4.3.14 Timer Characteristics

The parameters listed in **Table 4-30**, **Table 4-31**, **Table 4-32**, **Table 4-33** are guaranteed by design, not tested in production.

See section 4.3.12 for details on the features of the I/O alternate function pins (output comparison, input capture, external clock, PWM output).

Table 4-30 ATIM1/2/3 Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 240MHz$	4.16	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 240MHz$	0	120	MHz
Restim	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 240MHz$	0.00416	273	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 240MHz$	-	17.9	s

(1) Guaranteed by design, not tested in production.

Table 4-31 GTIM1/2/3/4/5/6/7 Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 120MHz$	8.33	-	ns
		$f_{TIMxCLK} = 180MHz$	5.56	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 120MHz$	0	60	MHz
		$f_{TIMxCLK} = 180MHz$	0	90	MHz
Restim	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 120MHz$	0.00833	546	μs

Symbol	Parameter	Condition	Min	Max	Unit
		f _{TIMxCLK} = 180MHz	0.00556	364	μs
t _{MAX_COUNT}	Maximum possible count	-	-	65536x65536	t _{TIMxCLK}
		f _{TIMxCLK} = 120MHz	-	35.8	s
		f _{TIMxCLK} = 180MHz	-	23.9	s

(1) Guaranteed by design, not tested in production.

Table 4-32 GTIM8/9/10 Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit
t _{res(TIM)}	Timer resolution time	-	1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 240MHz	4.16	-	ns
f _{EXT}	Timer external clock frequency on CH1 to CH4	-	0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 240MHz	0	120	MHz
Re _{TIM}	Timer resolution	-	-	16	bit
t _{COUNTER}	16 bit counter clock cycle when internal clock is selected	-	1	65536	t _{TIMxCLK}
		f _{TIMxCLK} = 240MHz	0.00416	273	μs
t _{MAX_COUNT}	Maximum possible count	-	-	65536x65536	t _{TIMxCLK}
		f _{TIMxCLK} = 240MHz	-	17.9	s

(1) Guaranteed by design, not tested in production.

Table 4-33 LPTIMER1/2 Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t _{res(TIM)}	Maximum possible count	-	1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 120MHz	8.33	-	ns
f _{EXT}	Maximum possible count	-	0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 120MHz	0	60	MHz
Re _{TIM}	Maximum possible count	-	-	16	bit
t _{COUNTER}	Maximum possible count	-	1	65536	t _{TIMxCLK}
		f _{TIMxCLK} = 120MHz	0.00833	546	μs
t _{MAX_COUNT}	Maximum possible count	-	-	128x65536	t _{TIMxCLK}
		f _{TIMxCLK} = 120MHz	-	69.9	ms

(1) Guaranteed by design, not tested in production.

4.3.15 Watchdog Characteristics

Table 4-34 IWDG Counting Maximum And Minimum Reset Time (LSI = 32 KHz)

Prescaler	PD[2:0]	Min timeout RL[11:0] = 0	Max timeout RL[11:0] = 0xFFFF	Unit
/4	000	0.125	512	ms
/8	001	0.25	1024	
/16	010	0.5	2048	
/32	011	1.0	4096	
/64	100	2.0	8192	
/128	101	4.0	16384	

/256	11x	8.0	32768	
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(1) Guaranteed by design, not tested in production.

Table 4-35 WWDG Counting Maximum And Minimum Reset Time (PCLK1 = 120 Mhz)

Prescaler	TIMERB[1:0]	Min timeout	Max timeout	Unit
/1	0	0.0341	556.92	ms
/2	1	0.0682	1113.84	
/3	2	0.136	2227.68	
/4	3	0.273	4455.36	

(1) Guaranteed by design, not tested in production.

4.3.16 I²C Interface Characteristics

Unless otherwise specified, the parameters listed in **Table 4-36** were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

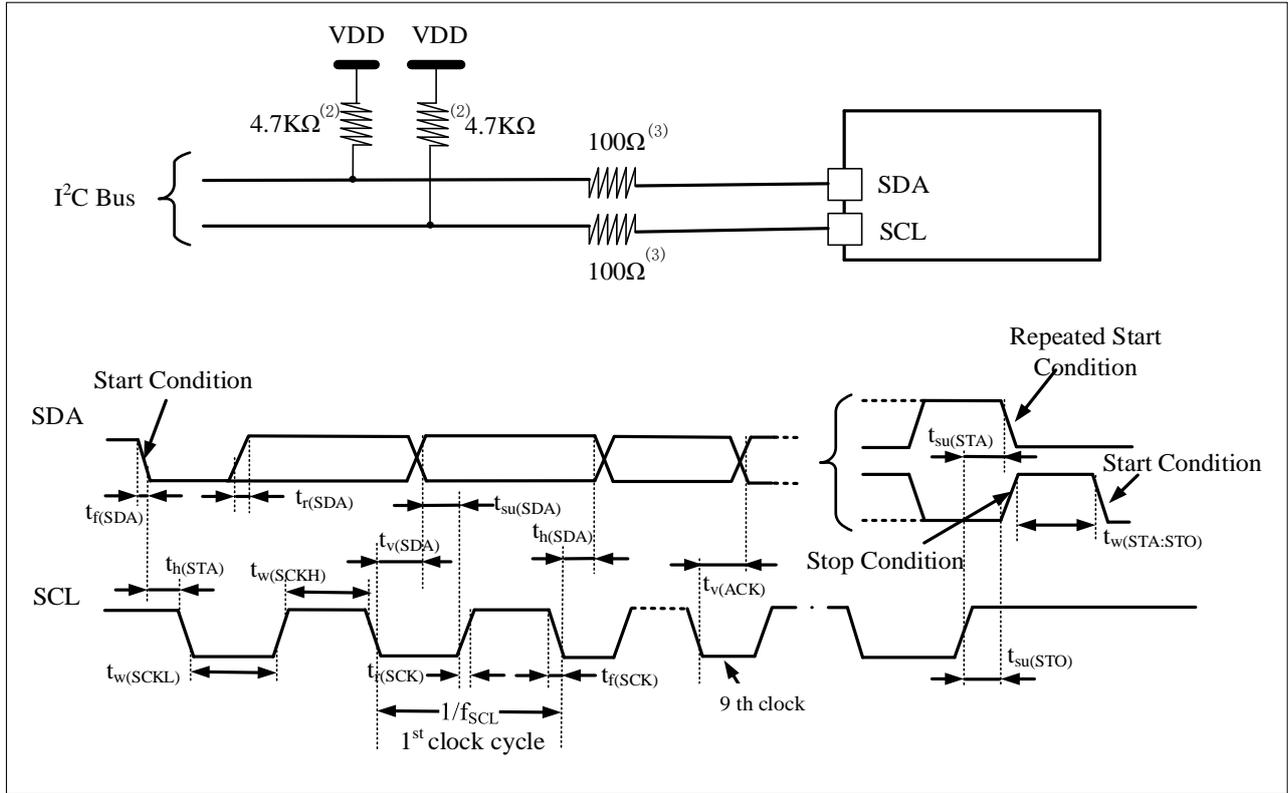
The I²C interface of the N32H493 product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open-drain pins, and when configured for open-drain output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in **Table 4-36**. See Section 4.3.12 for details about the features of the input/output alternate function pins (SDA and SCL).

Table 4-36 I²C Interface Characteristics⁽¹⁾

Symbol	Parameter	Standard mode		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{H(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	μ s
$t_{W(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	μ s
$t_{W(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	μ s
$t_{SU(STA)}$	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	μ s
$t_{H(SDA)}$	SDA data hold time	300	-	300	-	0	-	μ s
$t_{SU(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns
$t_{R(SDA)}$ $t_{R(SCL)}$	SDA and SCL rise time	-	1000	20	300	-	120	ns
$t_{F(SDA)}$ $t_{F(SCL)}$	SDA and SCL fall time	-	300	-	300	-	120	ns
$t_{SU(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	μ s
$t_{W(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	μ s
C_b	Capacitive load per bus	-	400	-	400	-	550	pf
$t_V(SDA)$	Data validity time	-	3.45	-	0.9	-	0.45	μ s
$t_V(ACK)$	Response time	-	3.45	-	0.9	-	0.45	μ s
t_{SP}	Spike pulse width to be suppressed by the input filter	-	-	0	50	0	50	ns

(1) Guaranteed by design, not tested in production.

Figure 4-12 I²C Bus AC Waveform And Measuring Circuit ⁽¹⁾

Notes:

- (1) The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.
- (2) The pull-up resistance depends on the I²C interface speed.
- (3) The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.17 SPI Interface Characteristics

Unless otherwise specified, the SPI parameters listed in **Table 4-37** are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with **Table 4-4**.

See Section 4.3.12 for details on the characteristics of the I/O multiplexed pins (NSS, SCLK, MOSI, MISO for SPI).

Table 4-37 SPI Characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	-	60	MHz
		Slave mode	-	-	40	
DuCy(SCK)	SPI from the input clock duty cycle	SPI slave mode	45	50	55	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Master mode	$t_{SCLK}/2$	-	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	$t_{SCLK}/2$	-	-	
$t_{w(SCLKH)}^{(1)}$ $t_{w(SCLKL)}^{(1)}$	SCLK high and low time	Master mode	$t_{SCLK}/2 - 1$	$t_{SCLK}/2$	$t_{SCLK}/2 + 1$	
$t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$	Data entry setup time	Master mode	3	-	-	
$t_{su(SI)}^{(1)}$		Slave mode	3	-	-	
$t_{h(MI)}^{(1)}$ $t_{h(SI)}^{(1)}$	Data entry hold time	Master mode	2.5	-	-	
$t_{h(SI)}^{(1)}$		Slave mode	2	-	-	
$t_{a(SO)}^{(1)(2)}$	Data entry hold time	Slave mode	9	-	$2 * t_{SCLK}/2$	
$t_{dis(SO)}^{(1)(3)}$	Data entry hold time	Slave mode	9	-	16	
$t_{v(SO)}^{(1)}$	Valid time of data output	Slave mode (after enable edge)	-	9	13	
$t_{v(MO)}^{(1)}$		Master mode (after enable edge)	-	3	5	
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	5	-	-	
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	0	-	-	

Notes:

- (1) Guaranteed by design, not tested in production.
- (2) The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.
- (3) The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

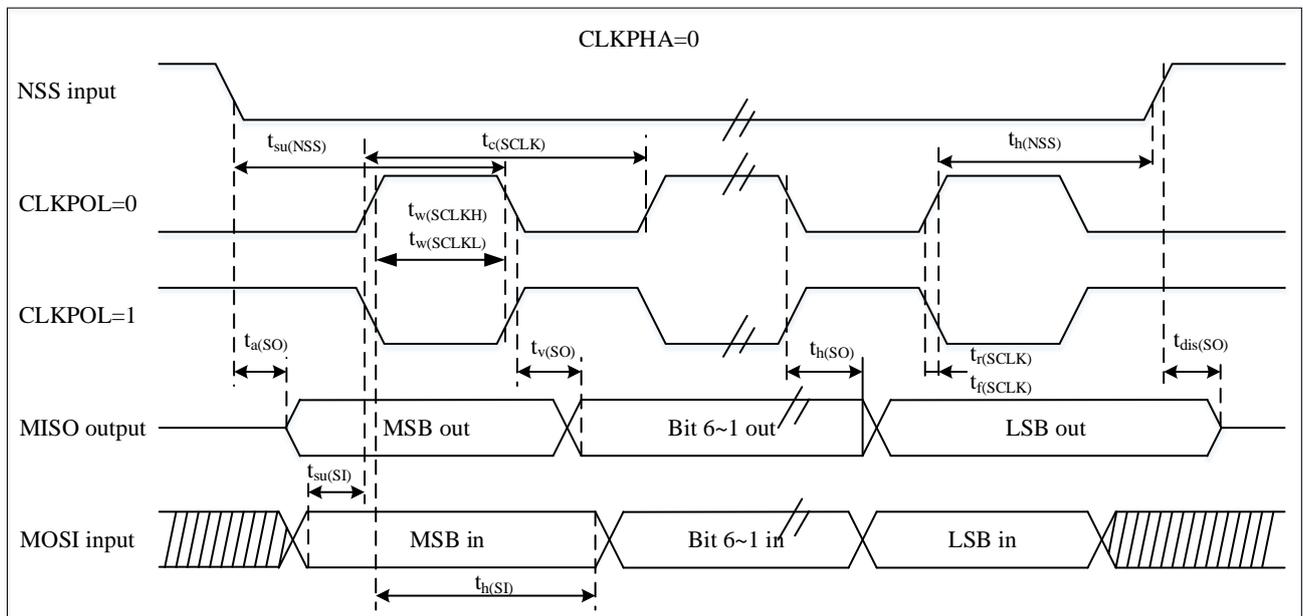
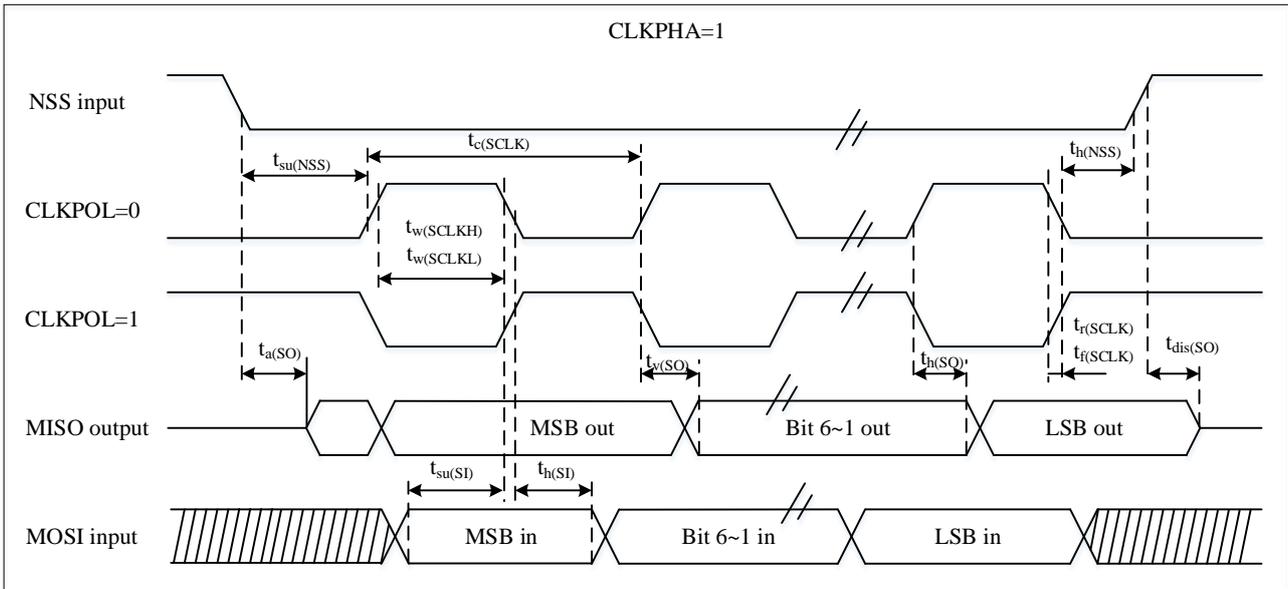
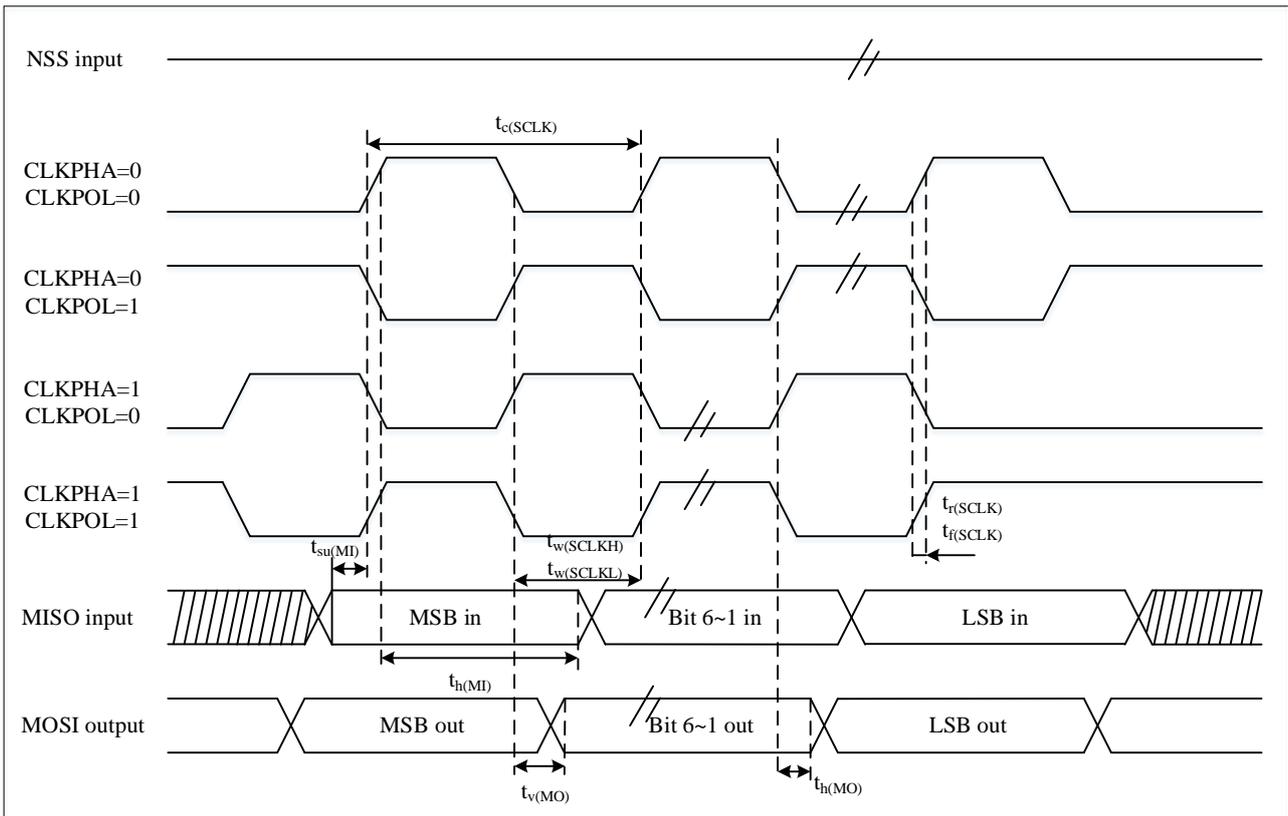
Figure 4-13 SPI Timing Diagram-Slave Mode And CPHA=0


Figure 4-14 SPI Timing Diagram-Slave Mode And CPHA=1⁽¹⁾


(1) The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

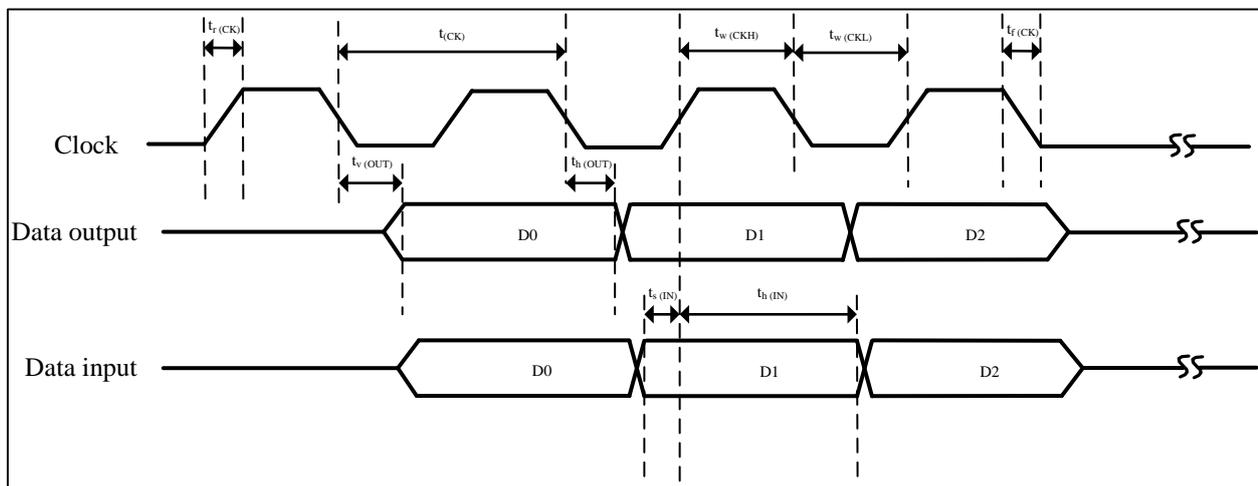
Figure 4-15 SPI Timing Diagram-Master Mode⁽¹⁾


(1) The measuring point is set at the CMOS level: $0.3V$ and $0.7V_{DD}$.

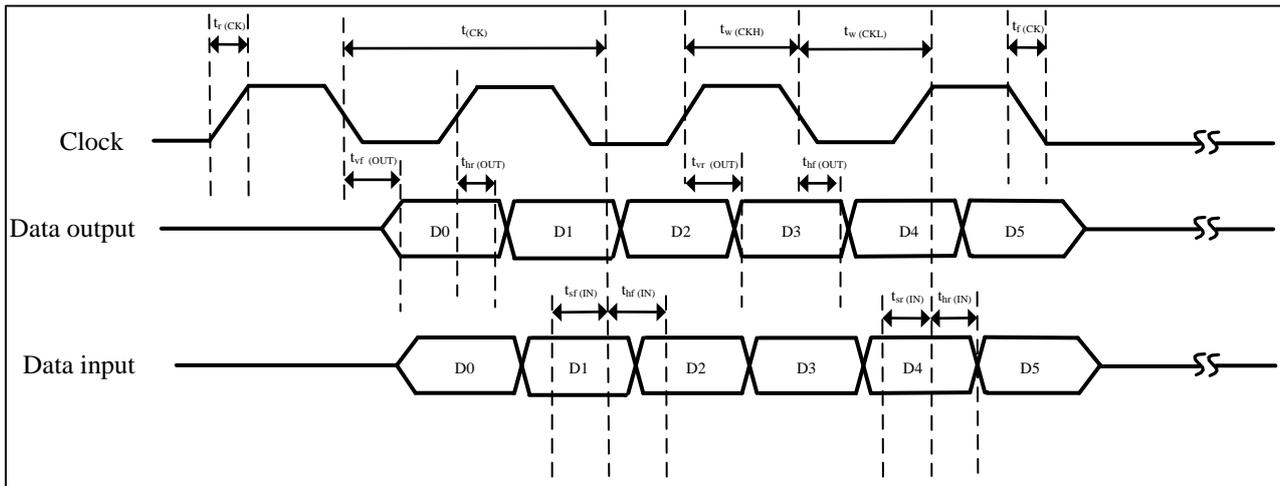
4.3.18 xSPI Characteristics

Table 4-38 Characteristics Of XSPI In SDR Mode

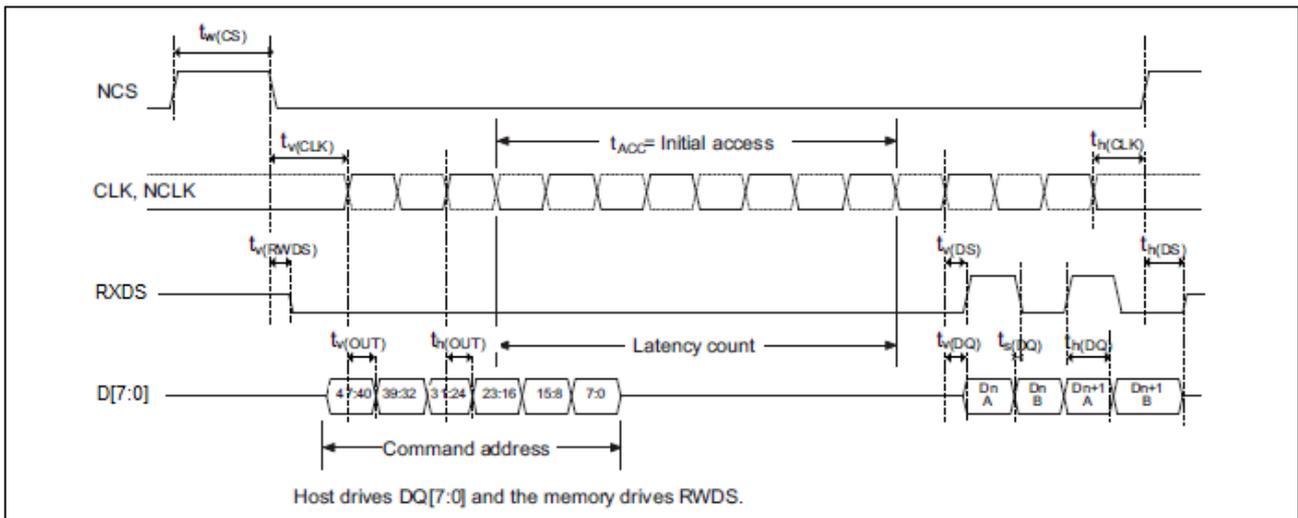
Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{CK}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{CK}/2-0.5$	-	$t_{CK}/2$	ns
$t_{w(CKL)}$		$t_{CK}/2-0.5$	-	$t_{CK}/2$	
$t_{s(IN)}$	Data input setup time	2.5	-	-	ns
$t_{h(IN)}$	Data input hold time	5.5	-	-	ns
$t_{v(OUT)}$	Data output valid time	-	2.5	3.5	ns
$t_{h(OUT)}$	Data output hold time	2.5	-	-	ns

Figure 4-16 Timing Of XSPI In SDR Mode

Table 4-39 Features Of XSPI In DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{CK}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{CK}/2-0.5$	-	$t_{CK}/2$	ns
$t_{w(CKL)}$		$t_{CK}/2-0.5$	-	$t_{CK}/2$	
$t_{sf(IN)}$	Data input setup time	3	-	-	ns
$t_{sr(IN)}$		5	-	-	
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time	2	-	-	ns
$t_{vf(OUT)}$; $t_{vr(OUT)}$	Data output valid time	-	-	7	ns
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Data output hold time	4	-	-	ns

Figure 4-17 Timing Of XSPI In DDR Mode

Table 4-40 Features Of XSPI In RXDS Mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{CK} $1/t_{(CK)}$	xSPI clock frequency	-	-	60	MHz
$t_{w(CKH)}$	SCK high/low time	$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2$	
$t_{v(CK)}$	clock valid time	-	-	$t_{(CK)}+2$	
$t_{h(CK)}$	clock high time	$t_{(CK)}+0.5$	-	-	
$t_{w(CS)}$	chip select high time	$3*t_{(CK)}$	-	-	
$t_{v(DQ)}$	Data input valid time	0	-	-	
$t_{v(DS)}$	Data selection input valid time	0	-	-	
$t_{h(DS)}$	Data selection input hold time	0	-	-	
$t_{v(RWDS)}$	Data selection output valid time	-	-	$3*t_{(CK)}$	
$t_{sf(DQ)}; t_{sr(DQ)}$	Input data setup time	3	-	-	ns
$t_{hf(DQ)}; t_{hr(DQ)}$	Input data hold time	4	-	-	ns
$t_{vf(OUT)}; t_{vr(OUT)}$	Output data setup time	-	6	7	ns
$t_{hf(OUT)}; t_{hr(OUT)}$	Output data hold time	3.5	-	-	ns

Figure 4-18 Timing Of XSPI In RXDS Mode


4.3.19 Electrical Parameters of 12 bit Analog-to-Digital Converter (ADC)

Unless otherwise specified, the parameters in **Table 4-41** are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in **Table 4-4**.

Note: It is recommended to perform a calibration at each power-on.

Table 4-41 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	The power supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	-	-	80	MHz
f_s	Sampling rate ⁽¹⁾	$V_{DDA} \geq 2.4V$	-	-	4.7	MSPS
		$1.8V \leq V_{DDA} < 2.4V$	-	-	4	
V_{AIN}	Switching voltage range ⁽²⁾	-	0 (V_{SSA} or V_{REF-} Connect to ground)		V_{REF+}	V
R_{ADC}	Sampling switch resistance	2.4~3.3V	-	-	300	ohm
		1.8~2.4V	-	-	480	
C_{ADC}	Internal sampling and holding capacitors	-	-	5	-	pF
SNDR	Singal noise distortion ration	-	-	65	-	dBFS
T_{cal}	The calibration time	-	82			$1/f_{ADC}$
t_s	Sampling time	$f_{ADC} = 80$ MHz(fast channel)	0.0563	-	7.52	μs
		$f_{ADC} = 80$ MHz(slow channel)	0.0625	-	8.35	
$T_s^{(1)}$	Sampling cycles	$f_{ADC} = 80$ MHz(fast channel)	0.0938	-	7.52	$1/f_{ADC}$
		$f_{ADC} = 80$ MHz(slow channel)	4.5	-	601.5	
T_s	Power on time	-	4.5	-	601.5	μs
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	-	8~614 (Sampling $T_s + 6.5/8.5/10.5/12.5$ for successive approximation)			$1/f_{ADC}$

Notes:

(1) *Guaranteed by design, not tested in production.*

(2) *According to different packages, V_{REF+} connected to V_{DDA} internally, and V_{REF-} connected to V_{SSA} internally.*

(3) *Sampling time/sampling rate is related to the input impedance R_{in} . The correspondence between the maximum input impedance R_{in} and the sampling time is shown in Table 4-42.*

Table 4-42 ADC Sampling Time⁽¹⁾

Resolution	Rin (kΩ)	Minimum Sampling Time (ns)			
		Vdda=2.4V to 3.6V, Vddd=1.1 V, selrange_Ido=L, Tjunction=125 °C, fclk=80 MHz		Vdda=1.8V to 2.4V, Vddd=1.1 V, selrange_Ido=L, Tjunction=125 °C, fclk=80 MHz.	
		Fast Channel	Slow Channel	Fast Channel	Slow Channel
12-bit	0.14	45.0	73.0	79.0	103.0
	0.6	79.0	103.0	300.0	345.0
	4.6	300.0	345.0	576.0	651.0
	9.5	576.0	651.0	1131.0	1257.0
	19	1131.0	1257.0	2776.0	3051.0
	48	2776.0	3051.0	5475.0	5982.0
10-bit	0.14	39.0	61.0	64.0	88.0
	0.6	64.0	88.0	250.0	357.0
	4.6	250.0	357.0	478.0	540.0
	9.5	478.0	540.0	935.0	1040.0
	19	935.0	1040.0	2294.0	2526.0
	48	2294.0	2526.0	4532.0	4963.0
8-bit	0.14	33.0	50.0	52.0	71.0
	0.6	52.0	71.0	202.0	234.0
	4.6	202.0	234.0	391.0	457.0
	9.5	391.0	457.0	800.0	1012.0
	19	800.0	1012.0	1838.0	2027.0
	48	1838.0	2027.0	3632.0	3984.0
6-bit	0.14	27.0	40.0	41.0	56.0
	0.6	41.0	56.0	153.0	177.0
	4.6	153.0	177.0	292.0	330.0
	9.5	292.0	330.0	569.0	642.0
	19	569.0	642.0	1435.0	1666.0
	48	1435.0	1666.0	3001.0	3919.0

Notes:

(1) Guaranteed by design, not tested in production.

Table 4-43 ADC Accuracy-Limited Test Conditions^{(1) (2)}

Symbol	Parameter	Condition	Typ	Max ⁽³⁾	Unit
ET ⁽⁴⁾	Comprehensive error	f _{HCLK} = 240MHz, f _{ADC} = 240MHz, sample Rate = 1.75M SPS, V _{DDA} = 3.3V, T _A = 25 °C Measurements are made after the ADC is calibrated V _{REF+} = V _{DDA}	1.3	5	LSB
EO ⁽⁴⁾	Offset error		1	3	
ED	Differential linear error		1	2.2	
EL	Integral linear error		2	3	

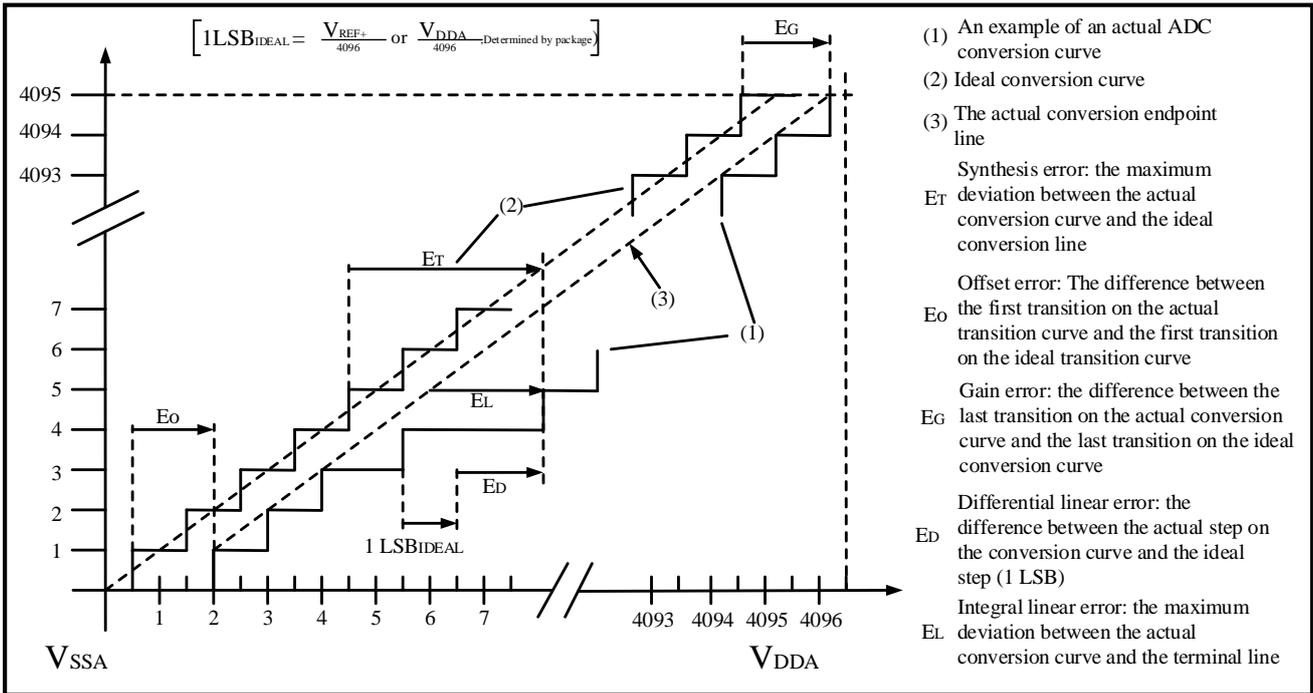
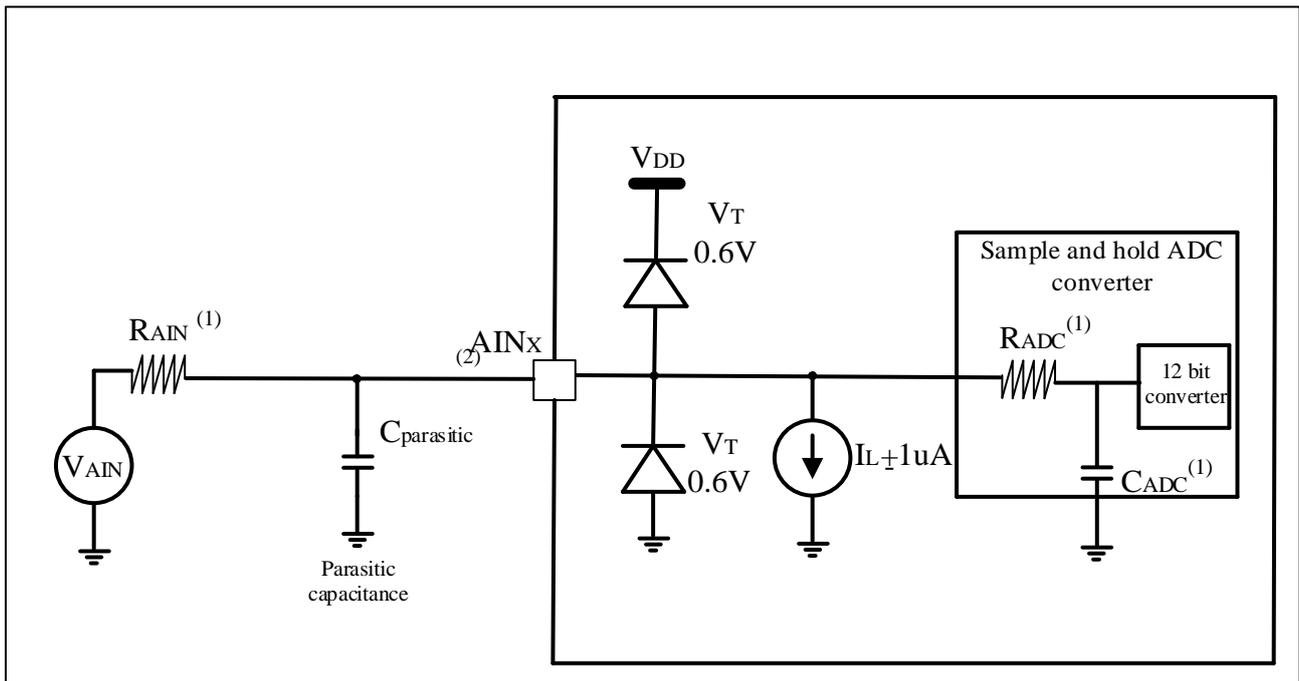
Notes:

(1) The DC accuracy of the ADC is measured after internal calibration.

(2) ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin. It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current.

(3) The forward injection current does not affect the ADC accuracy as long as it is within the range of I_{INJ(PIN)} and ΣI_{INJ(PIN)} given in **Table 4-2**

(4) Based on comprehensive evaluation, not tested in production.

Figure 4-19 ADC Precision Characteristics

Figure 4-20 Typical Connection Diagram Using ADC


Notes:

(1) For values of R_{AIN} , R_{ADC} , and C_{ADC} , see Table 4-41.

(2) $C_{\text{parasitic}}$ indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF). A larger $C_{\text{parasitic}}$ value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC} from medine.

4.3.20 12-bit DAC Electrical Parameters

Unless otherwise specified, the parameters of Table 4-44 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions of Table 4-4.

Table 4-44 DAC 1MSPS Characteristics⁽¹⁾

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	DAC output buffer disabled, output only internally connected		2.4	-	3.6	V
V _{REF+}	Positive reference voltage	DAC output buffer disabled, output only internally connected		2.4	-	V _{DDA}	
V _{REF-}	Negative reference voltage	-		V _{SSA}			
R _L	Resistive load with buffer enable	DAC output Buffer enable	Connected to V _{SSA}	5	-	-	kΩ
			Connected to V _{DDA}	25	-	-	
R _o	Impedance output	DAC output buffer disable		10.3	12.3	15.7	kΩ
C _L	Capacitive load	-		-	-	50	pF
DAC _{OUT}	DAC_OUT output voltage	Output buffer enable		0.2	-	V _{REF+} - 0.2	V
		Output buffer disable		0	-	V _{REF+}	-
I _{DD}	Static mode (standby mode) DAC DC consumption (V _{DD} +V _{DDA} +V _{REF+})	-		-	180	230	μA
		-		-	400	610	μA
t _{SETTLING}	Settling time (full range: 12-bit input code transitioning from minimum value to maximum value, DAC_OUT reaching its final value within ±1 LSB)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ		-	3	4.1	μs
		DAC buffer disable		-	2.1	2.6	
t _{WAKEUP}	Wake-up time from shutdown state (from enabling DAC to DAC_OUT reaching its final value within ±1 LSB)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ		-	4	7	μs
		DAC buffer disable, CL ≤ 10 pF		-	2	4	
PSRR	Power supply rejection ratio (relative to V _{DD33A}) (static DC measurement)	DAC buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ		-	-85	-30	dB
TW _{to_W}	The minimum time between two consecutive writes to the DAC _x _DATO register to ensure that small changes in the input code result in the correct DAC_OUT(1 LSB). DAC _{xy} _CTRL.EXOUT = 1, DAC _{xy} _CTRL.BxEN = 1 DAC _{xy} _CTRL.EXOUT = 1, DAC _{xy} _CTRL.BxEN = 0 or DAC _{xy} _CTRL.INOUT = 1, DAC _{xy} _CTRL.BxEN = 0	CL ≤ 50 pF, RL ≥ 5 kΩ		1	-	-	μs
		CL ≤ 10 pF		1.4	-	-	
V _{offset}	Middle code offset for 1 trim code step	V _{REF+} = 3.6V		-	-	1500	μV
I _{DDA(DAC)}	DAC consumption from V _{DDA}	DAC buffer enable	No load, input mid-value 0x800	-	250	400	μA
			No load, input max-value 0xF1C	-	450	670	
		DAC buffer disable	No load, input mid-value 0x800	-	-	0.25	

I _{DDV(DAC)}	DAC consumption from VREF+	DAC buffer enable	No load, input mid-value 0x800	-	180	240	μA
			No load, input max-value 0xF1C	-	320	400	
		DAC buffer disable	No load, input mid-value 0x800	-	155	200	
DNL	Nonlinear distortion (deviation between two consecutive codes)	-	-2	-	+2	LSB	
INL	Nonlinear accumulation (deviation measured at code i from the line connecting code 0 and code 4095)	-	-6	-	+6	LSB	
Offset	Offset error (value measured at code 0x800)	Output buffer enable, CL ≤ 50 pF, RL ≥ 5 kΩ	VREF+ = 3.6V	-16	-	+8	LSB
			VREF+ = 1.8V	-20	-	+20	
		Output buffer disable, CL ≤ 50 pF, noRL	-8	-	+6		
Gain Error	Gain error	-	-	±0.5	-	%	

(1) Guaranteed by design, not tested in production.

4.3.21 Voltage Reference Buffer (VREFBUF) Characteristics

Unless otherwise specified, the parameters in Table 4-45 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-45 VREFBUF Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V _{REFBUF_OUT}	Voltage reference output	VRS= 00, T _A =25°C	2.044	2.048	2.052	
		VRS= 01, T _A =25°C	2.496	2.5	2.504	
		VRS= 10, T _A =25°C	2.896	2.9	2.904	
TRIM	Trim step resolution	-	-	±0.05	±0.1	%
CL	Load capacitor	-	0.5	1	2	μF
PSRR	Power supply rejection	DC	48.9	74.7	-	dB
		100KHz	25	40	-	
t _{START}	Start-up time	CL = 1 μF	-	500	650	μs
I _{DDA(VREFBUF)}	VREFBUF consumption from VDDA	I _{load} ≤ 10 mA	-	45	80	μA

Note: (1) Guaranteed by design, not tested in production.

4.3.22 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in Table 4-46 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-46 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	±1	±3	°C
Avg_Slope ⁽¹⁾	Average slope	-3.7	-4	-4.3	mV/°C

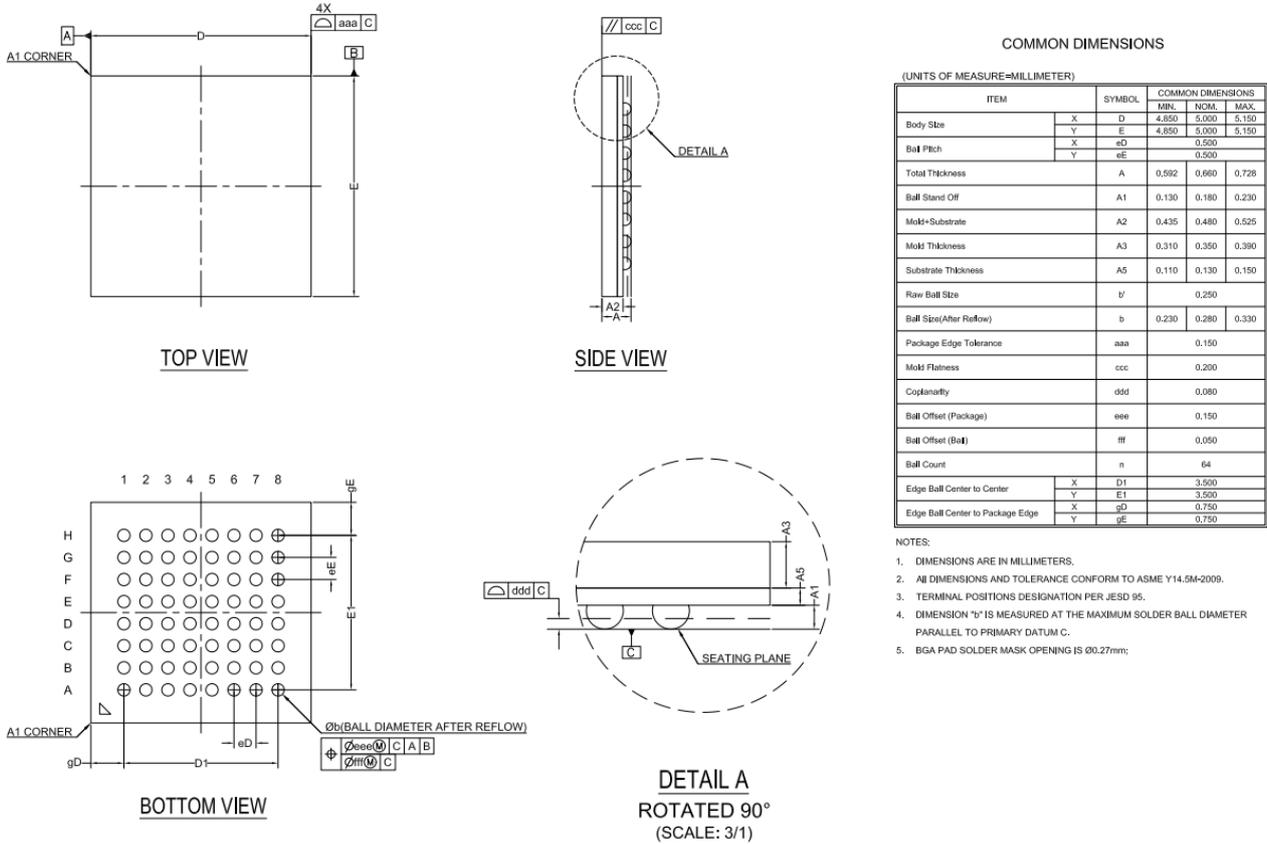
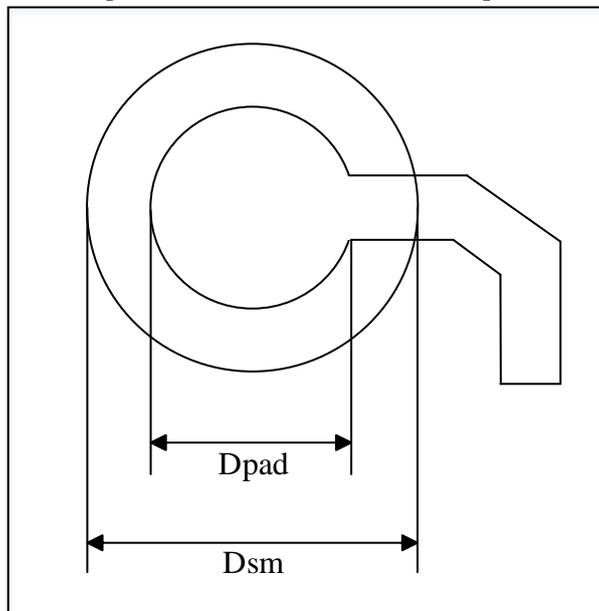
Symbol	Parameter	Min	Typ	Max	Unit
$V_{25}^{(1)}$	Voltage at 25 °C	-	1.32	-	V
$t_{START}^{(1)}$	Startup time	4	-	10	μ s
$T_{S_temp}^{(2)(3)}$	ADC sampling time when reading the temperature	-	-	3	μ s

Notes:

- (1) Based on comprehensive evaluation, not tested in production.*
- (2) Guaranteed by design, not tested in production.*
- (3) Shortest sampling time can be determined in the application by multiple iterations.*

5 Packages

5.1 BGA64

Figure 5-1 BGA64 Package Dimensions

Figure 5-2 BGA64 Recommended Footprint

Figure 5-3 BGA64 Recommended PCB design rules

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Pad trace width	0.100 mm

5.2 BGA72

Figure 5-4 BGA72 Package Dimensions

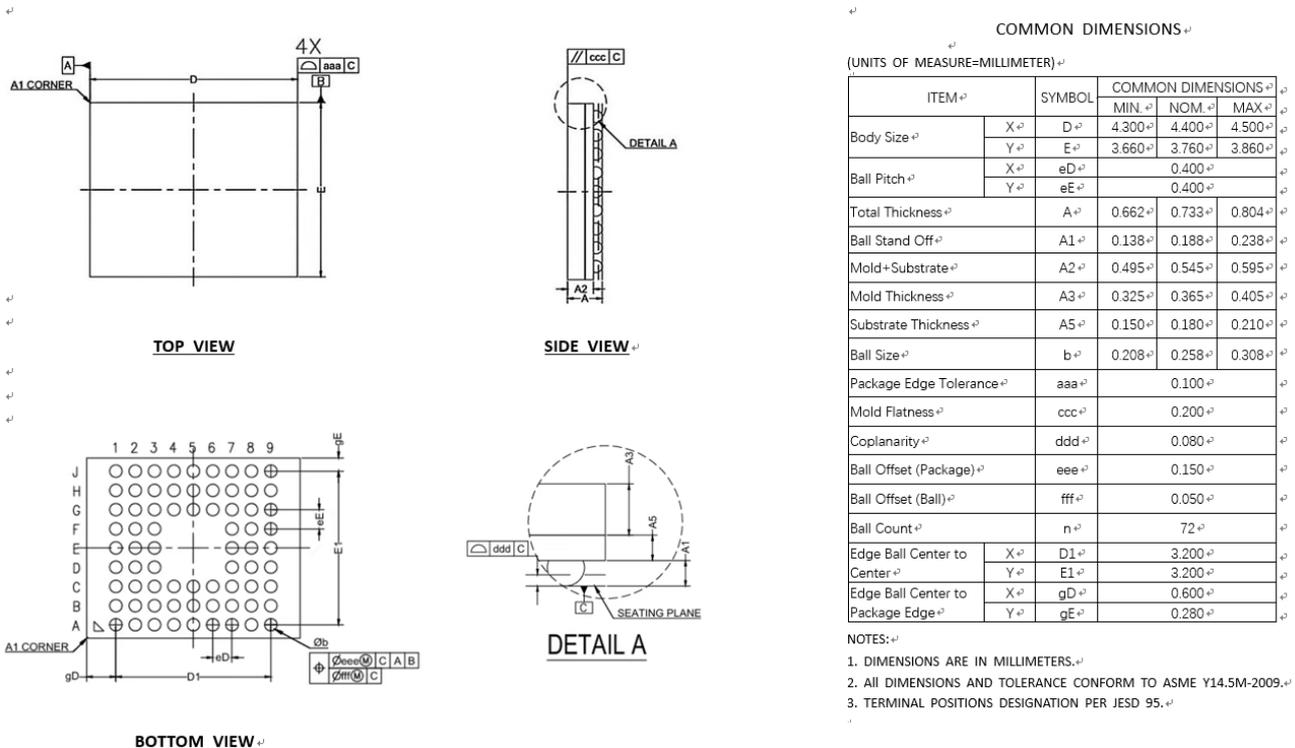


Figure 5-5 BGA72 Recommended Footprint

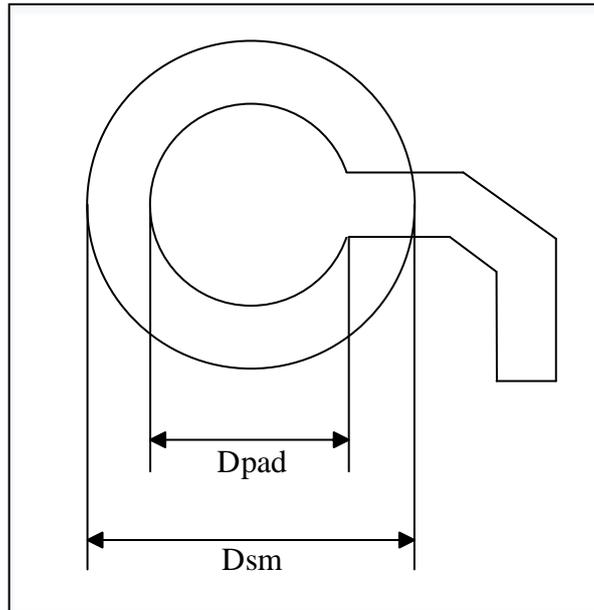
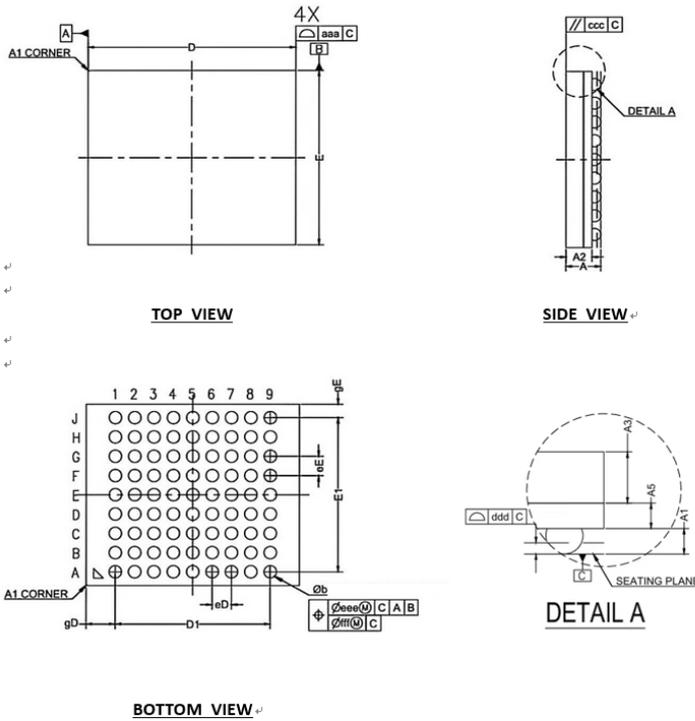


Figure 5-6 BGA72 Recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
D_{pad}	0.220 mm
D_{sm}	0.310 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

5.3 BGA81

Figure 5-7 BGA81 Package Dimensions



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

ITEM	SYMBOL	COMMON DIMENSIONS		
		MIN	NOM	MAX
Body Size	X	4.300	4.400	4.500
	Y	3.660	3.760	3.860
Ball Pitch	X	0.400		
	Y	0.400		
Total Thickness	A	0.662	0.733	0.804
Ball Stand Off	A1	0.138	0.188	0.238
Mold+Substrate	A2	0.495	0.545	0.595
Mold Thickness	A3	0.325	0.365	0.405
Substrate Thickness	A5	0.150	0.180	0.210
Ball Size	b	0.208	0.258	0.308
Package Edge Tolerance	aaa	0.100		
Mold Flatness	ccc	0.200		
Coplanarity	ddd	0.080		
Ball Offset (Package)	eee	0.150		
Ball Offset (Ball)	fff	0.050		
Ball Count	n	81		
Edge Ball Center to Center	X	D1	3.200	
	Y	E1	3.200	
Edge Ball Center to Package Edge	X	gD	0.600	
	Y	gE	0.280	

- NOTES
1. DIMENSIONS ARE IN MILLIMETERS.
 2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
 3. TERMINAL POSITIONS DESIGNATION PER JESD 95.

Figure 5-8 BGA81 Recommended Footprint

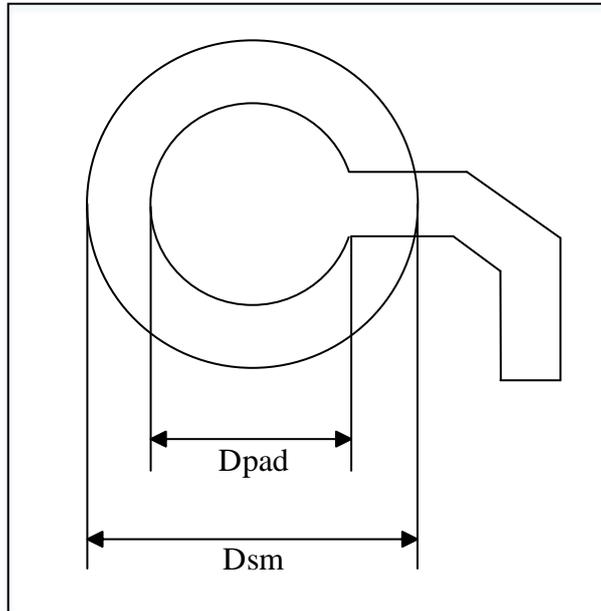
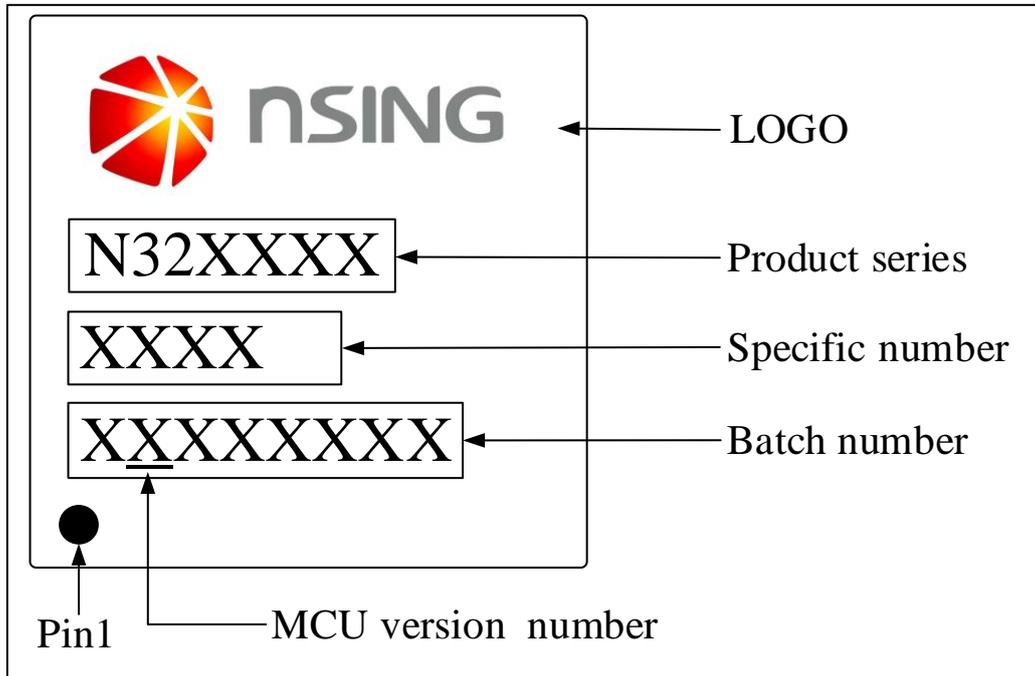


Figure 5-9 BGA81 Recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.220 mm
Dsm	0.310 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

6 Marking Information

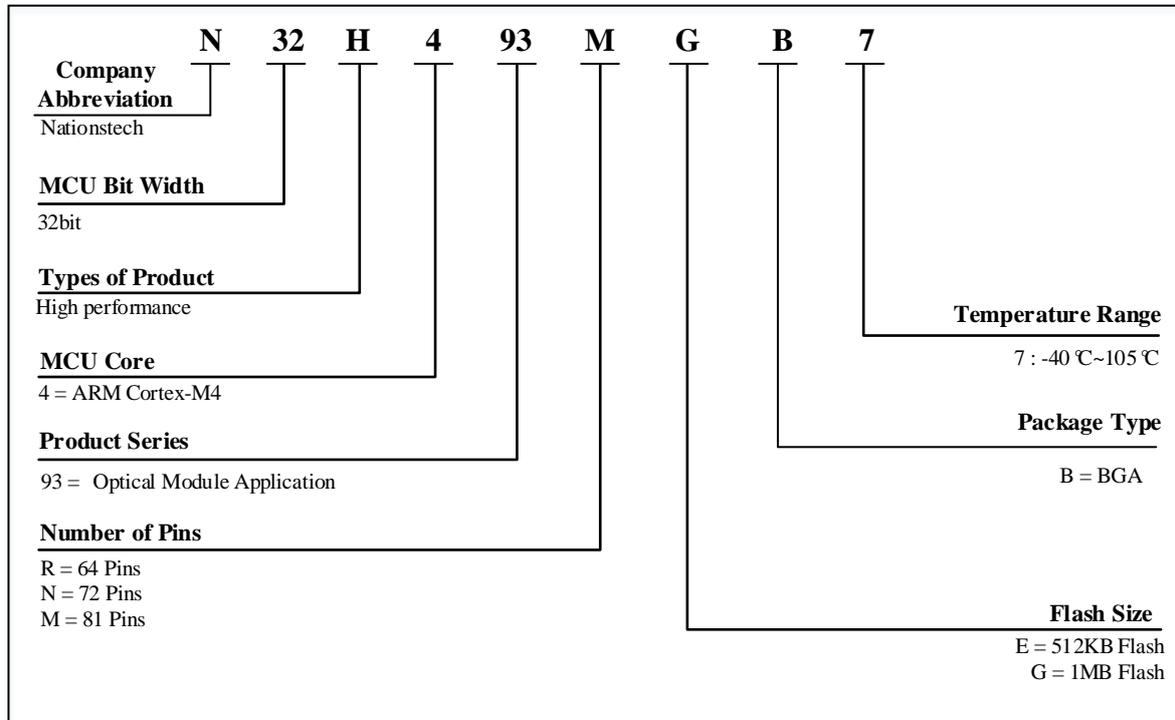
Figure 6-1 Marking Information



7 Ordering Information

7.1 Naming Convention

Figure 7-1 N32H493 Series Part Number Information



7.2 Ordering code

Table 7-1 N32H493 Series Ordering Code

Ordering Code ⁽¹⁾	Package	Size	Packaging ⁽²⁾	SPQ ⁽³⁾	Temperature range
N32H493REB7	BGA64	5mm x 5mm	TBD	TBD	-40°C~105°C
N32H493RGB7	BGA64	5mm x 5mm	TBD	TBD	-40°C~105°C
N32H493NEB7	BGA72	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H493NGB7	BGA72	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H493MEB7	BGA81	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H493MGB7	BGA81	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C

- For the latest detailed-ordering information, please refer to the Selection Guide.
- The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
- Minimum packaging quantity.

8 Version History

Date	Version	Changes
2026.1.22	V1.0.0	Initial release.

9 Disclaimer

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