Design Guidelines

N32H49X Series Hardware Design Guide

Introduction

This document details the hardware design checklist for the N32H49X series MCUs to provide users with hardware design guidance.

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1. N32H49X Series MCU Hardware Design Checklist

1.1 Power Supply Introduction

The N32H49X series chips operate at a voltage (VDD) of 1.8V to 3.6V. The main pins are: VDD, VDDIO, VDDA, VREF, and VBAT. Please refer to the relevant datasheet for details.

1.2 Power supply scheme

VDD is the main power supply for the MCU and must be powered by a stable external power source. The voltage range is 1.8V to 3.6V. A 0.1uF decoupling capacitor must be placed near all VDD pins, and an additional 4.7uF decoupling capacitor is required for one of the VDD pins. For detailed design instructions on the decoupling capacitors, please refer to the minimum system reference design schematics for each package in Chapter 3.

VDDIO supplies power to specific IO pins (BGA81/BGA72: PG9 to PG14; LQFP144: PD6 to PD7, PG9 to PG15) independently of VDD. It is recommended to place a 0.1uF and a 1uF capacitor on the VDDIO input pin.

VDDA is an analog power supply that provides power to the ADC, DAC, COMP, and PGA. It is recommended to place a 0.1uF and a 2.2uF capacitor on the VDDA input pins.

VREF+ is the reference voltage, providing a reference level for the ADC and DAC. When VERF+ uses the built-in reference source VREFBUF, it is recommended to place a 0.1uF and a 1uF capacitor near the VREF+ pin. When VERF+ is externally powered, it is recommended to place a 0.1uF and a 2.2uF capacitor near the VREF+ pin.

Note: VREFBUF strictly prohibits enabling external input while in internal output mode; only one of the output or external input modes can be selected at a time.

1.3 backup battery

The VBAT pin primarily supplies power to the backup power domain (RTC, LPTIM, Backup SRAM), enabling the backup power domain modules to continue operating normally when the main power supply (VDD) is turned off.

1.4 External pin reset circuit

A low-level signal (external reset) on the NRST pin will trigger a system reset. The reference circuit for an external NRST pin reset is as follows.

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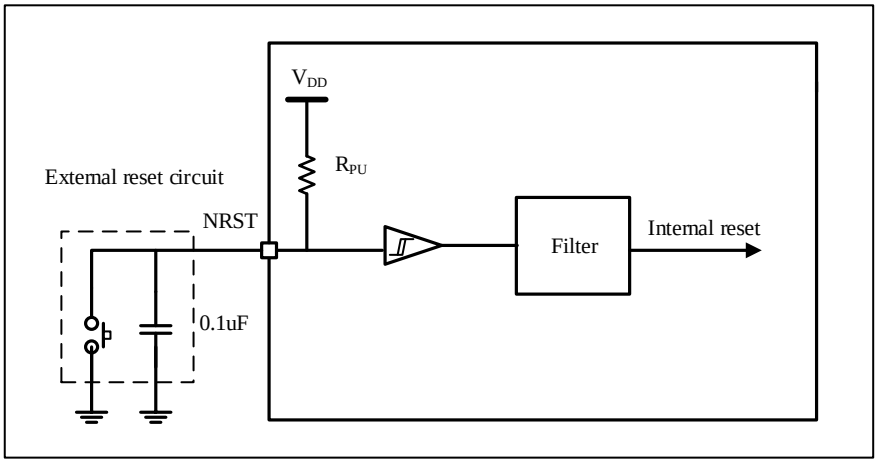

Figure 1-1 System Reset Diagram

Note: It is recommended that the reset pin NRST not be left floating during design. A typical reference value is given for an external capacitor of 0.1uF. If a faster reset time is required, an external pull-up capacitor can be added to the NRST pin. In addition, users can decide whether to add a reset button according to the actual needs of the product.

1.5 External clock circuit

The N32H49X series MCUs include two external clocks: an external high-speed clock HSE (4MHz~32MHz) and an external low-speed clock LSE (typically 32.768KHz).
HSE and LSE are configured with appropriate load capacitors based on the crystal oscillator characteristics. Please refer to the external clock characteristic description in the relevant datasheet for details..

1.6 Start-up pin connection

The diagram below shows the external connections required when selecting the boot memory for the N32H49X series chips. Please refer to the relevant section of the user manual for information on boot modes.

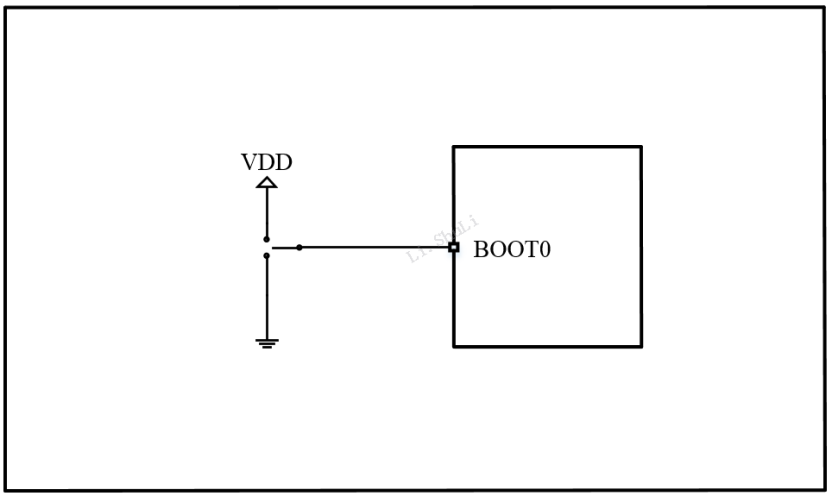

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Figure 1-2 Startup mode implementation example

When the BOOT pin is pulled high, the chip resets and boots from the BOOT area; when the BOOT pin is pulled low, the chip resets and boots from the user area.

1.7 ADC converter

Regarding ADC circuit design, please note the following points:

1） When using ADC sampling, it is recommended to shorten the external trace distance of the ADC sampling channel;

2） It is recommended to keep the area around the ADC input signal away from high-frequency switching signals;

3） Note the maximum supported speeds for the slow and fast channels :

With an ADC input clock of 80MHz, the N32H49X series should maintain an ADC fast channel sampling rate of no more than 4.7Msps and a slow channel sampling rate of no more than 2.5Msps.

4） During ADC conversion, the chip does not support modifying the ADC configuration. If you need to modify the configuration, you must wait until the current conversion is completed or the ADC is turned off before you can configure it.

5） When using a particular ADC channel, a negative voltage (For example, -0.2V) must not be applied to other unused ADC sampling channels. Applying this negative voltage will pull down the voltage of the normally sampling ADC channel, resulting in inaccurate data readings.

6） When using a particular ADC channel, a high voltage (greater than VDD) must not be applied to other unused ADC sampling channels. Applying such a high voltage will pull up the voltage of the normally sampling ADC channel, resulting in inaccurate data readings.

7） When using an ADC, the sampling rate is related to the RAIN; the smaller the RAIN, the faster the sampling rate. See the table below for details:

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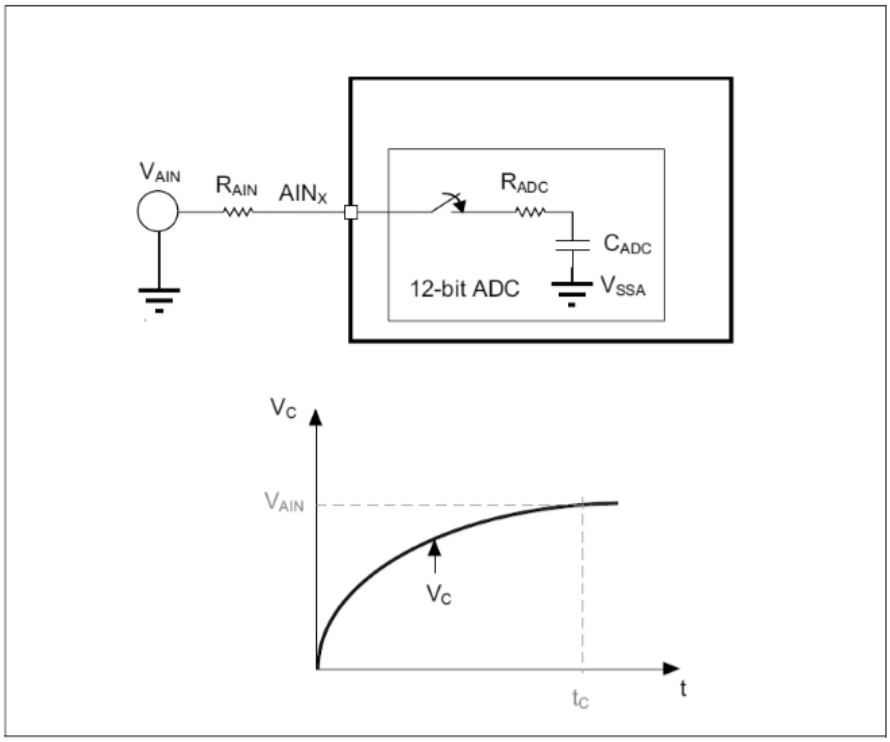

Figure 1-3 Effect of series resistance at ADC input port

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ADC sampling schedule:

resolution	RAIN (kΩ)	Minimum sampling time (ns)	
		Fast Track	Slow lane
12-bit	0.14	45.0	73.0
	0.6	79.0	103.0
	4.6	300.0	345.0
	9.5	576.0	651.0
	19	1131.0	1257.0
	48	2776.0	3051.0
10-bit	0.14	39.0	61.0
	0.6	64.0	88.0
	4.6	250.0	357.0
	9.5	478.0	540.0
	19	935.0	1040.0
	48	2294.0	2526.0
8-bit	0.14	33.0	50.0
	0.6	52.0	71.0
	4.6	202.0	234.0
	9.5	391.0	457.0
	19	800.0	1012.0
	48	1838.0	2027.0
6-bit	0.14	27.0	40.0
	0.6	41.0	56.0
	4.6	153.0	177.0

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	9.5	292.0	330.0
	19	569.0	642.0
	48	1435.0	1666.0

Table 1-1 ADC sampling schedule

Note : The sampling time needs to be configured based on the input clock and the selectable sampling period of the ADC register. In principle, the ADC sampling period configuration should be greater than or equal to the minimum number of sampling periods in the table.

1.8 Design Recommendations for High-Speed Communication Interfaces

Note: Relevant schematic diagrams may be referenced in the《N32H497ZGL7_EVB》full-function board design.

1.8.1 USBHS Interface

1）Impedance control is required for DPDM traces, and the differential impedance shall be 90Ω±10%.

2）Length matching shall be implemented for DPDM traces, and the length difference of the differential pair shall be controlled within ±5 mil.

3）DPDM traces shall be routed symmetrically, right-angle bends shall be avoided, and impedance discontinuities shall be minimized.

4）Add ESD diodes close to the connectors on the DPDM traces to prevent electrostatic damage.

5）Ensure a complete reference ground plane is present beneath the DPDM differential traces, avoid crossing ground splits, and minimize interference from return current paths.

6）DPDM traces shall be routed away from high-frequency noise areas such as power supplies and clock circuits as much as possible, and shielding ground vias shall be added around the differential traces.

1.8.2 SDRAM Interface

1）The power plane shall be kept as intact as possible to minimize impedance; decoupling capacitors shall be added close to the power pins to reduce power supply noise.

2）The clock signal CLK shall be routed with priority, kept with the shortest path, and routed away from other high-speed signals.

3）The traces of data lines (DQ0~DQ15, LQDM, UDQM) shall be length-matched within the same group, with the length difference controlled within 50 mils.

4）The traces of address lines (A0~A12, BS0, BS1) shall be length-matched within the same group, with the length difference controlled within 100 mils.

5）The traces of control signal lines (CS/RAS/CAS/WE) shall be length-matched within the same group, with the length difference controlled within 100 mils.

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6） The length difference between the groups of address lines, control lines, and data lines relative to the CLK clock line shall be controlled within 100 mils.

7） Adopt a complete ground plane, avoid crossing splits, and ensure a low-impedance return path.

8） The address lines, control lines, data lines and CLK signal can be terminated with a 22~33Ω resistor to reduce signal reflection and improve signal integrity.

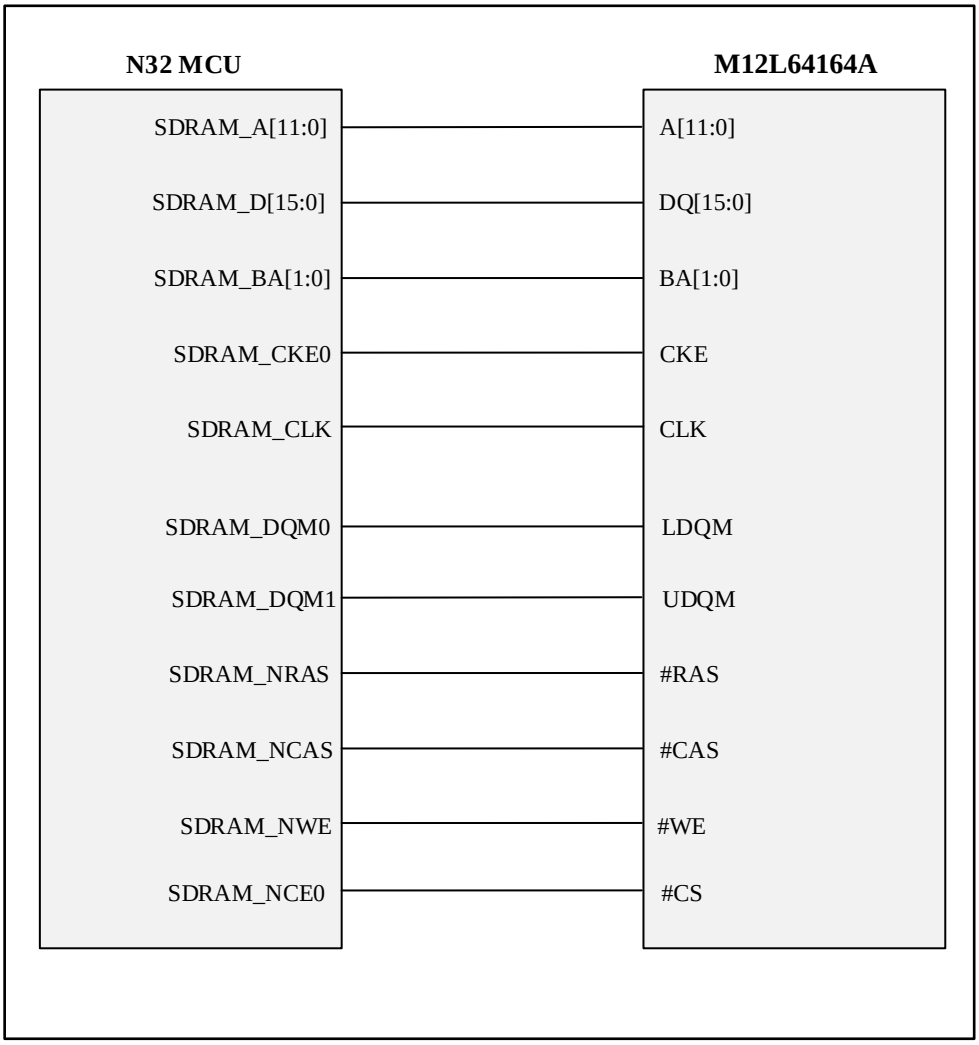

Figure 1-4 SDRAM Pin connection

1.8.3 XSPI Interface

1） Data lines (XSPI_IO0~XSPI_IO7), XSPI_CLK, XSPI_NSS, and XSPI_RXDS must be routed with equal lengths, and the length difference must be controlled within 100mil.

2） A pull-up resistor needs to be added when designing the XSPI_NSS signal;

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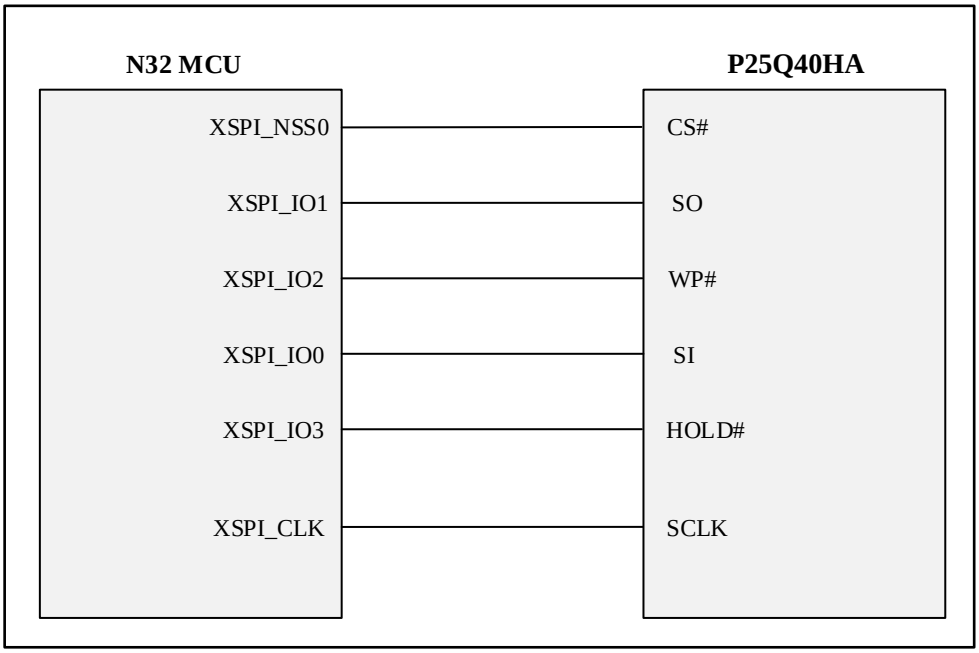

Figure 1-5 XSPI Pin connection

1.8.4 ETH Interface

Note: The following recommendations are based on the DM9162EP as the PHY.

1） For TXP/TXN and RXP/RXN differential signal pairs, the differential impedance should be controlled at 100Ω ± 10%, and the length difference of the same differential line pair should be controlled within 5mil to maintain signal symmetry and reduce common-mode noise and timing deviation. The overall length difference between the transmitting (TXP/TXN) and receiving (RXP/RXN) differential pairs is recommended to be controlled within 50mil to avoid inconsistent communication delays across nodes.

2） The interface signal clock and data lines must be of equal length. TX_CLK, TXD0, and TXD1 must be of equal length within the same group, and RX_CLK, RXD0, and RXD1 must be of equal length within the same group. The length difference must be controlled within 50mil.

3） To avoid right-angle routing and reduce impedance abrupt changes, the routing length can be adjusted using serpentine routing.

4） The crystal oscillator should be placed as close as possible to the PHY chip, and the clock signal should be grounded to reduce radiation interference.

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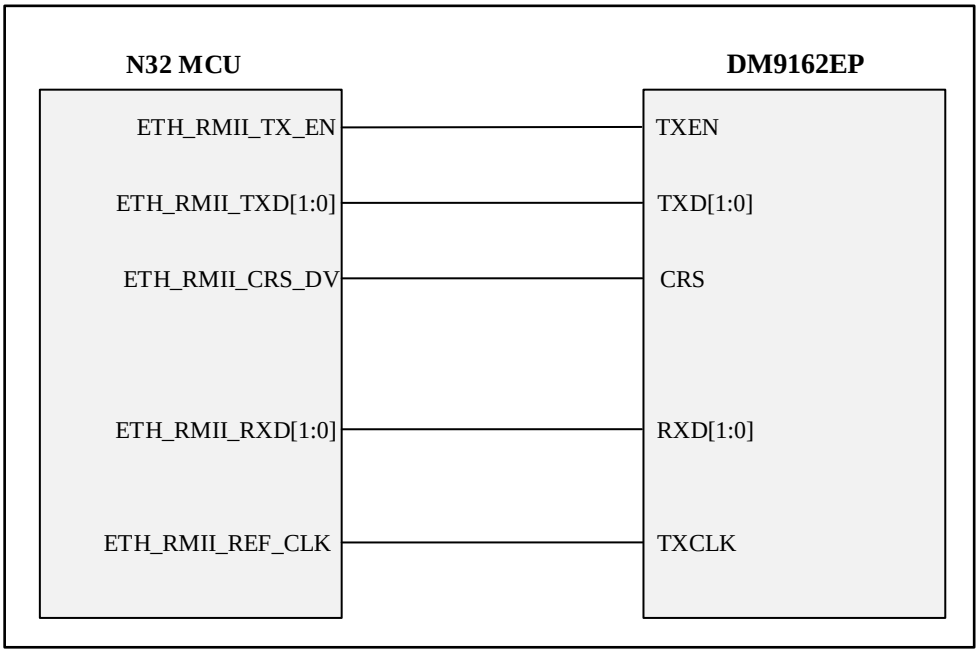

Figure 1-6 ETH Pin connection

1.9 IO power-on pulse processing

During power-up, due to the high impedance state of the I/O pin and the coupling characteristics of its internal circuitry, a high-level pulse will appear on the I/O pin momentarily upon power-up (the actual high-pulse voltage value should be measured by the user). If this pulse affects its application, it is recommended to connect an appropriate capacitor (1nF~100nF) or add an appropriate pull-down resistor (10K~100K) to the corresponding I/O pin.

The following figure shows the I/O (PB12) waveform during the power-on process of the N32H497ZGL7_STB_V1.0 development board:

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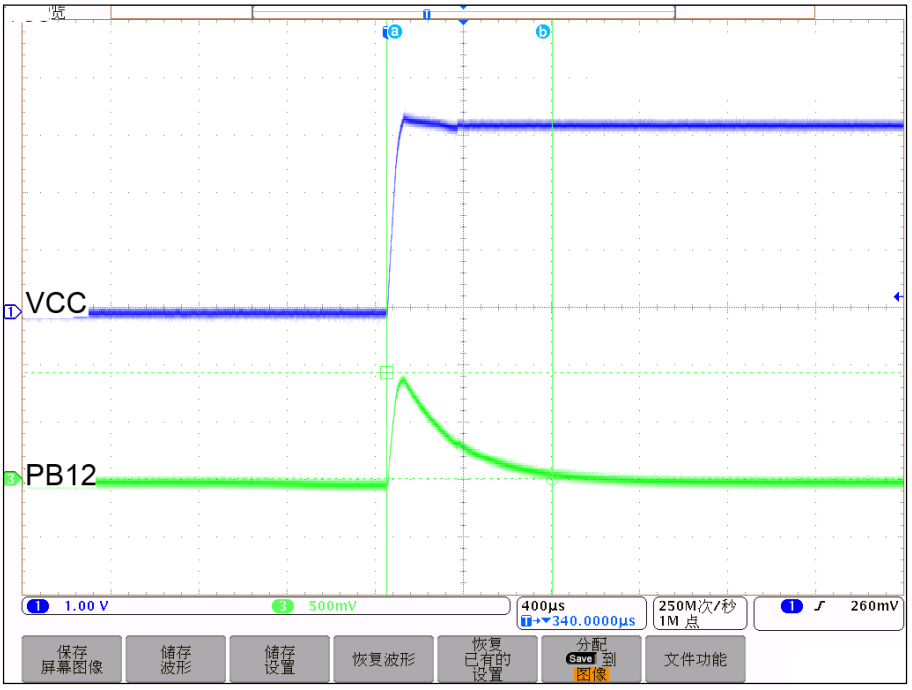

Figure 1-7 Power-on process IO (PB12) waveform

The following image shows the waveform of the N32H97ZGL7_STB_V1.0 development board after a 10K pull-down resistor is added to I/O (PB12) during power-up.:

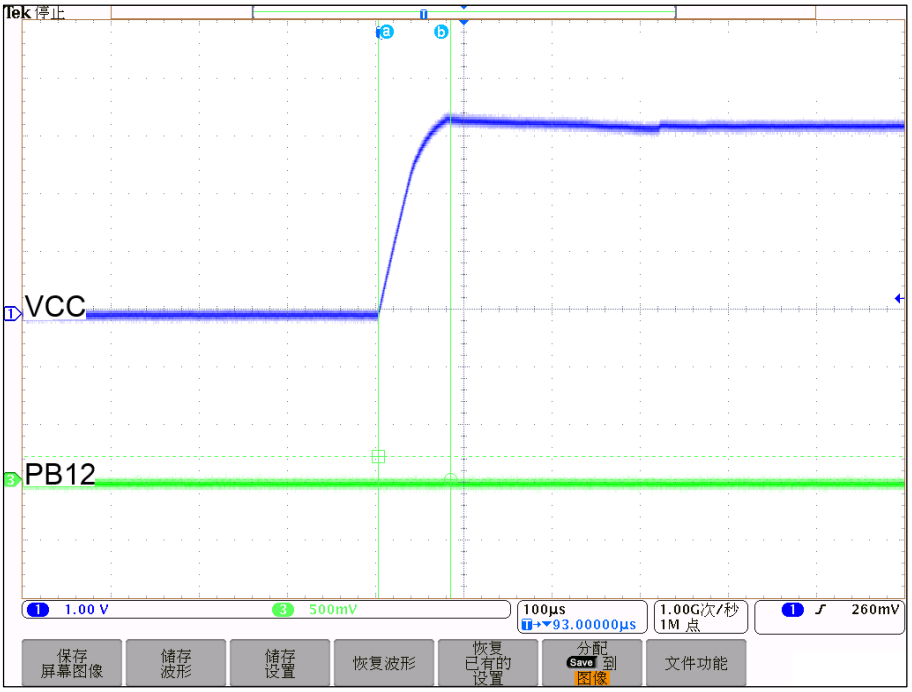

Figure 1-8 Waveform after power-on process I/O (PB12) with external pull-down resistor processing

1.10 IO withstand voltage

When using the chip, please pay attention to the withstand voltage of each I/O. In the I/O structure section of the

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datasheet, which defines pin multiplexing, it is marked FT: 5V tolerant IO. This type of IO requires level conversion when communicating with other external IOs in different voltage domains.

Packaging							Pin name (function after reset)	Pin type(1)	I/O structure(2)	Fail-safe(3)	Alternate functions	Additional functions
LQFP64	BGA64	BGA72	BGA81	LQFP100	BGA100	LQFP144						
-	-	-	-	1	B2	1	PE2	I/O	FT	Y	FEMC_A23 ETH_MII_TX_D3 GTIM2_CH1_ETR SPI4_SCK ATIM3_CH1 USART4_TX DVP_HSYNC XSPI_IO2 DVP_D3 USART9_RX UART7_TX EVENTOUT	-
-	-	A1	A1	2	A1	2	PE3	I/O	FT	Y	FEMC_A19 GTIM2_CH2 SPI4_NSS ATIM3_CH2 USART4_RX DVP_VSYNC GTIM8_BKIN USART9_TX GTIM2_CH1 EVENTOUT	-

Figure 1-9 Datasheet pin multiplexing defined I/O structure

Note : FT: 5V tolerance; FTa: 5V tolerance, supports analog peripherals; TTa: 3.3V standard I/O. When using the chip, pay attention to the I/O voltage tolerance.

1.11 Anti-static design

1.11.1 PCB design

For standard two-layer PCB designs, it is recommended to surround signal lines with ground planes and also to cover the edges of the PCB with ground planes as much as possible. Where cost allows, four-layer or multi-layer PCB designs can be used. In multi-layer PCBs, the ground plane acts as an important charge source, which can counteract the charge on electrostatic discharge sources, thus reducing problems caused by electrostatic fields. The PCB ground plane can also act as a shield for signal lines (of course, the larger the opening of the ground plane, the lower its shielding effectiveness). Furthermore, in the event of a discharge, due to the large ground plane of the PCB, charge is easily injected into the ground plane rather than into the signal lines. This is beneficial for component protection, as the charge can dissipate before causing component damage.

1.11.2 ESD protection devices

In actual product design, the chip itself has a certain degree of electrostatic discharge (ESD) protection capability. The N32H49X series MCU has an ESD (HBM) rating of +/-4KV. However, if higher ESD protection levels are required, and some chip pins need to be directly connected as output or input ports, then the chip pins are directly exposed on the outermost surface of the product and cannot be isolated by grounding or other methods. Under these conditions, external ESD protection devices are generally necessary. A TVS diode is a typical ESD

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protection device. Below is a typical connection example.

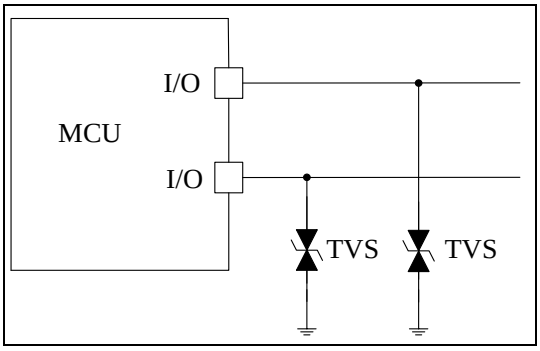

Figure 1-10 TVS connection method on I/O pins

1.12 Debugging interface

The N32H49X series chips support serial interface (SWD) and JTAG debug interface. Please refer to the relevant user manual for detailed application information.

Debug signal	GPIO pins
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
JNTRST	PB4

Table 1-1 Debugging interface

1.13 BOOT serial port interface

The N32H49X series chips support BOOT serial communication. The serial port interfaces are shown in the table below.:

BOOT serial port	GPIO pins
USART1_TX	PA9
USART1_RX	PA10

Table 1-2 Serial port interface

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2. Overall design recommendations

1） Printed circuit board

It is recommended to use a multilayer printed circuit board with a dedicated ground plane (VSS) and a dedicated power plane (VDD) to provide good coupling performance and shielding. In practical applications, if cost considerations prevent the use of a multilayer printed circuit board, then a good grounding and power supply structure must be ensured during circuit design.

2） Device location

In PCB design, different circuits need to be laid out separately based on their varying EMI impacts. For example, high-current circuits, low-voltage circuits, and high-frequency components should be separated. This reduces cross-coupling on the PCB.

3） Grounding and power supply (VSS, VDD)

Each module (analog circuits, digital circuits, and low-sensitivity circuits) should be grounded independently, with digital and analog grounds separated. All grounds should ultimately be connected together at a single point. Based on the PCB current, the power line width should be increased as much as possible to reduce loop resistance. Simultaneously, the routing of power and ground lines should be as consistent as possible with the current direction, and power lines should be placed as close as possible to ground lines to minimize loop areas. This helps enhance noise immunity. Areas on the PCB without components should be filled with ground to provide good shielding.

4） Decoupling

All power pins need to be properly connected to the power supply. These connections, including pads, traces, and vias, should have the lowest possible impedance. This is typically achieved by increasing trace width, and decoupling capacitors must be placed close to the chip for each VDD and VSS pin pair. The following diagram shows a typical layout for power/ground pins.

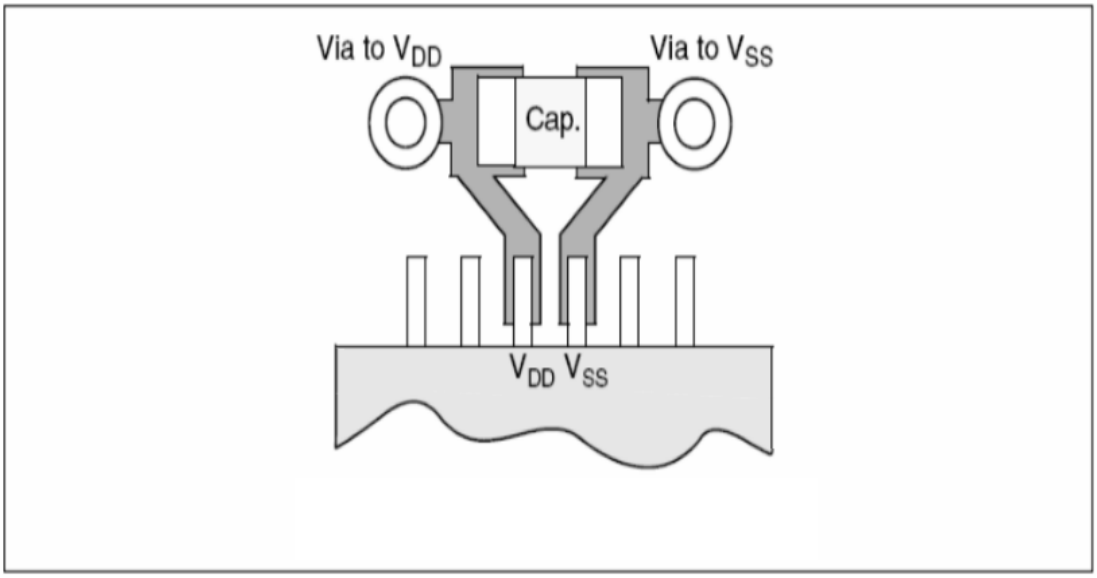

Figure 2-1 Typical layout of VDD/VSS pins

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3. Minimum System Reference Design Schematic

3.1 LQFP64-N32H497RGL7

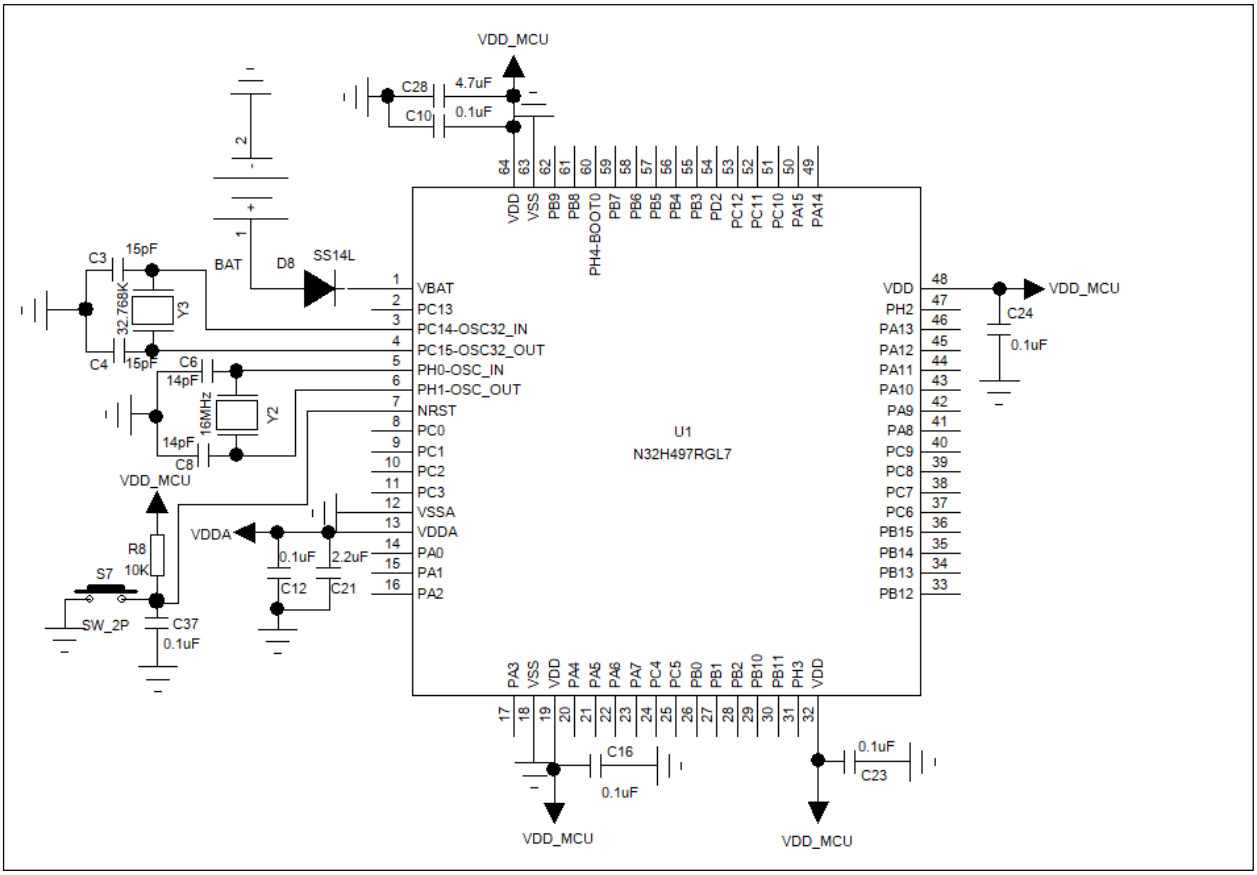

Figure 3-1 LQFP64 package minimum system reference design schematic

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3.2 LQFP100-N32H497VGL7

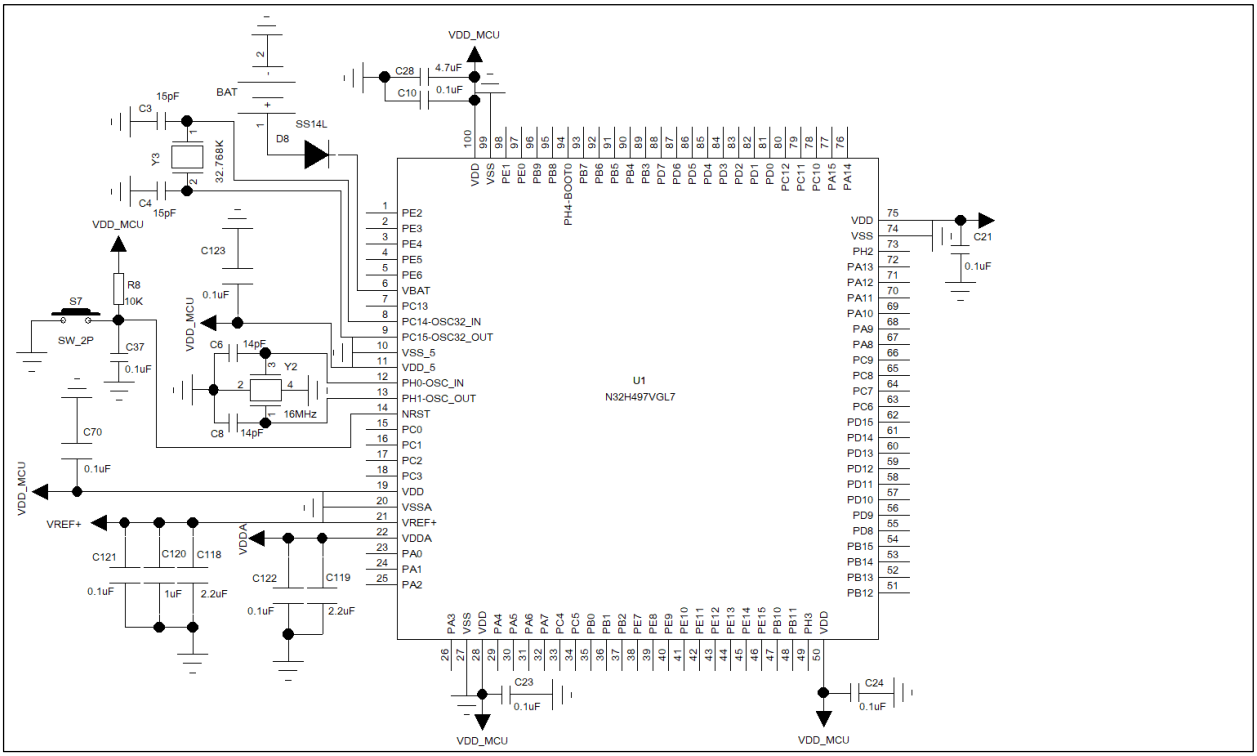

Figure 3-2 LQFP100 package minimum system reference design schematic

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3.3 LQFP100-2-N32H497VGL7C

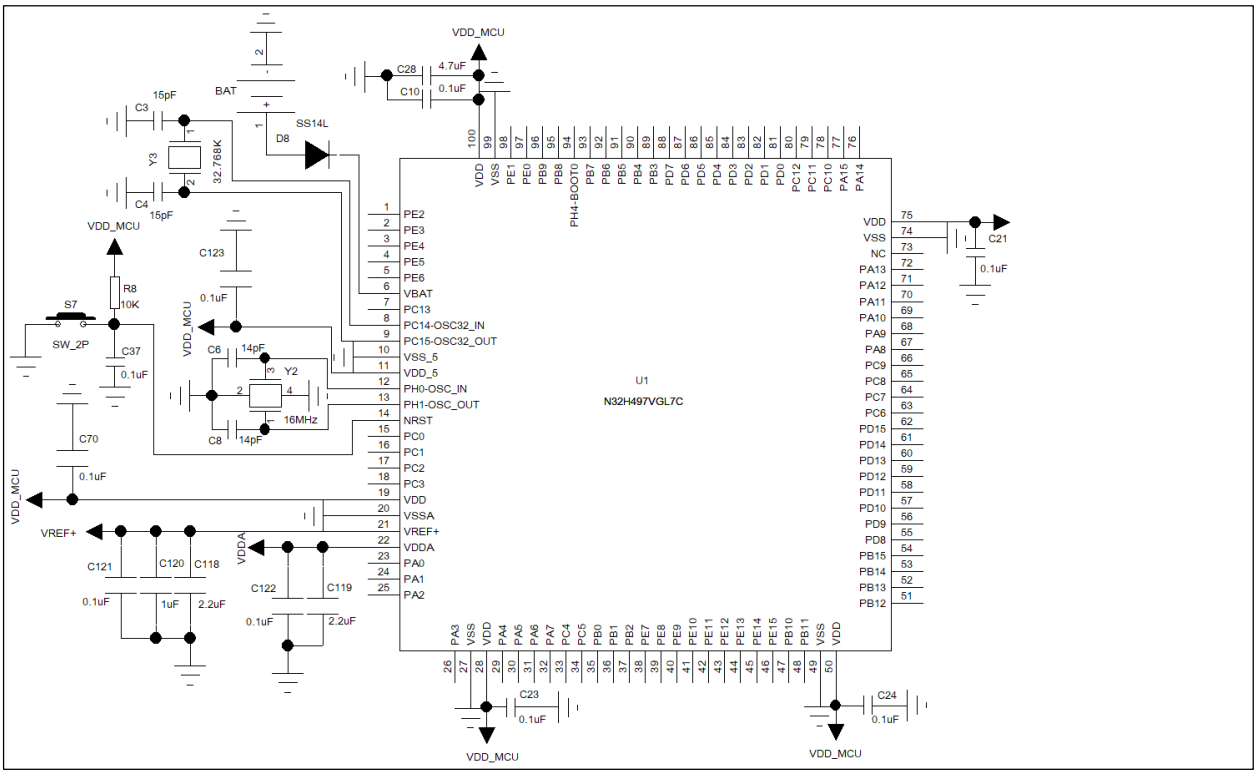

Figure 3-3 LQFP100-2 package minimum system reference design schematic

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3.4 LQFP144-N32H497ZGL7

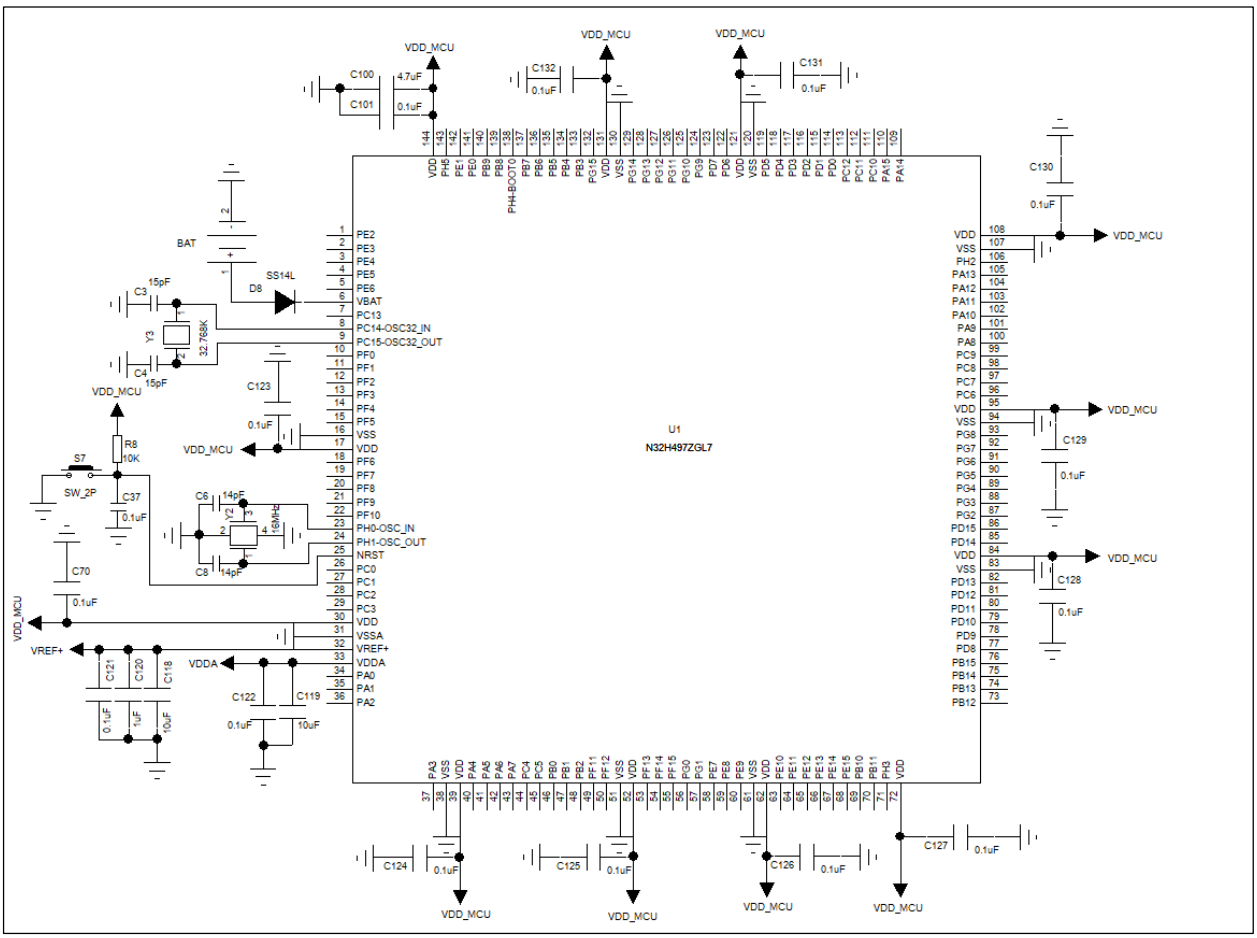

Figure 3-4 LQFP144 package minimum system reference design schematic

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3.5 BGA64-N32H497RGB7

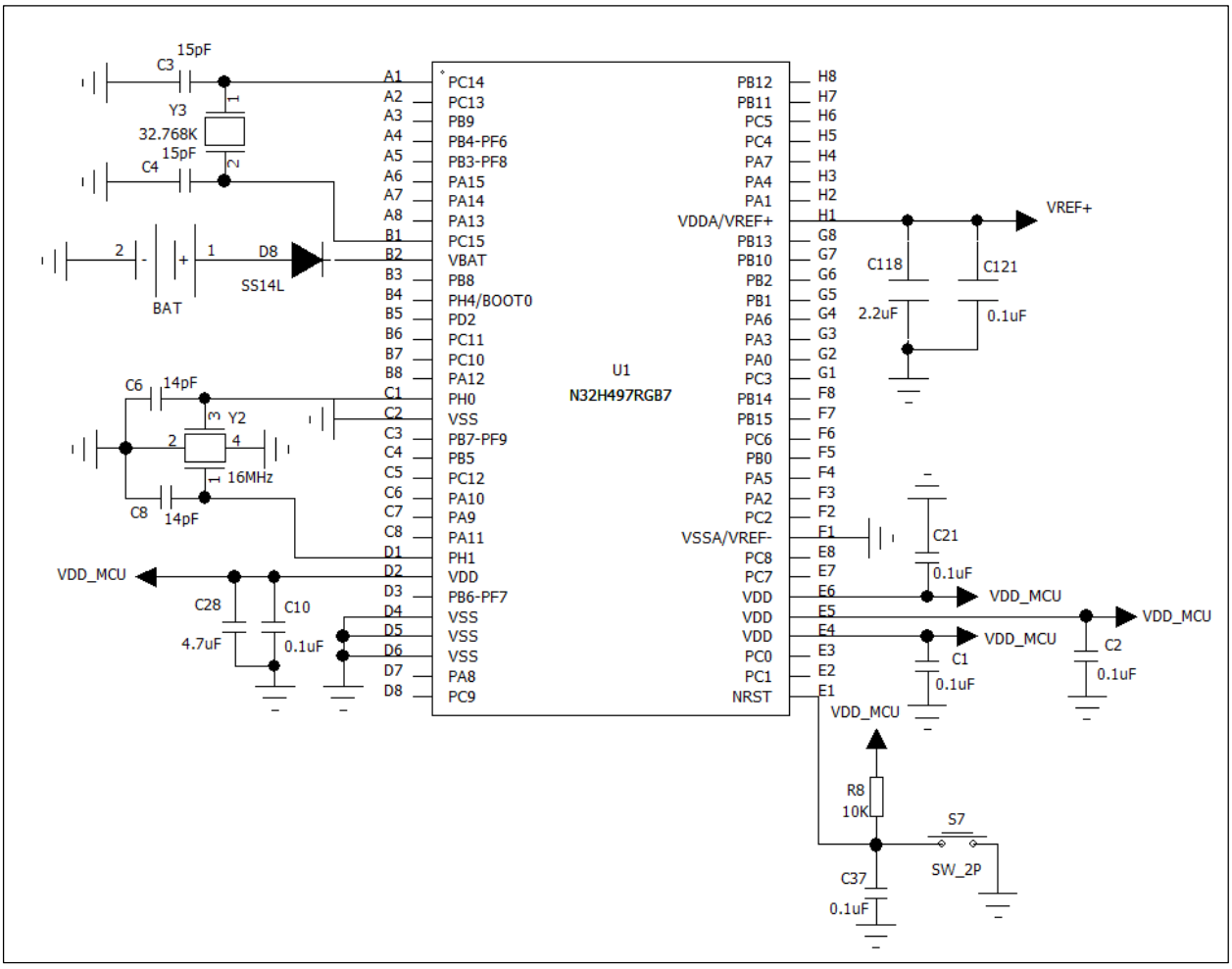

Figure 3-5 BGA64 package minimum system reference design schematic

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3.6 BGA72-N32H497NGB7

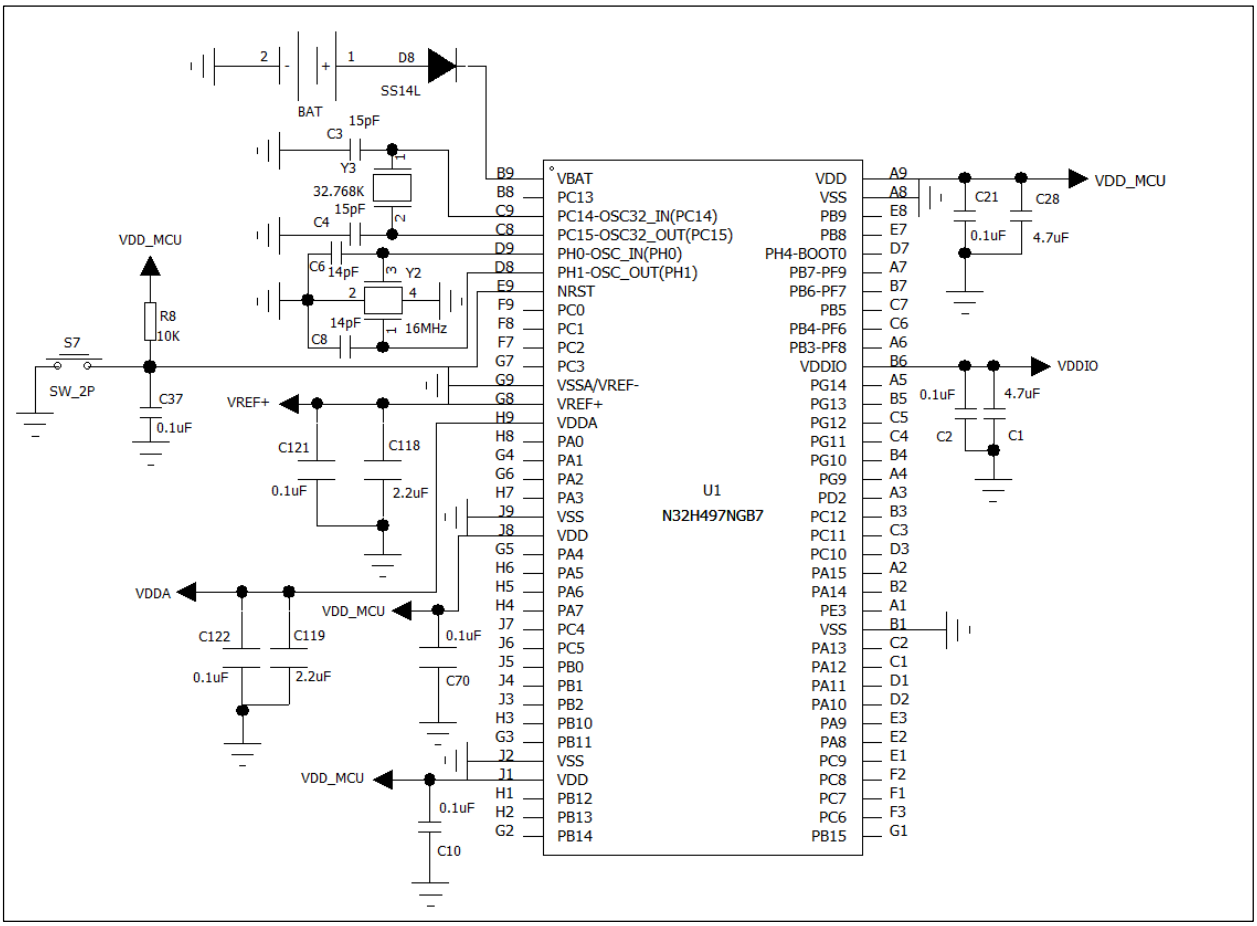

Figure 3-6 BGA72 package minimum system reference design schematic

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3.7 BGA81-N32H497MGB7

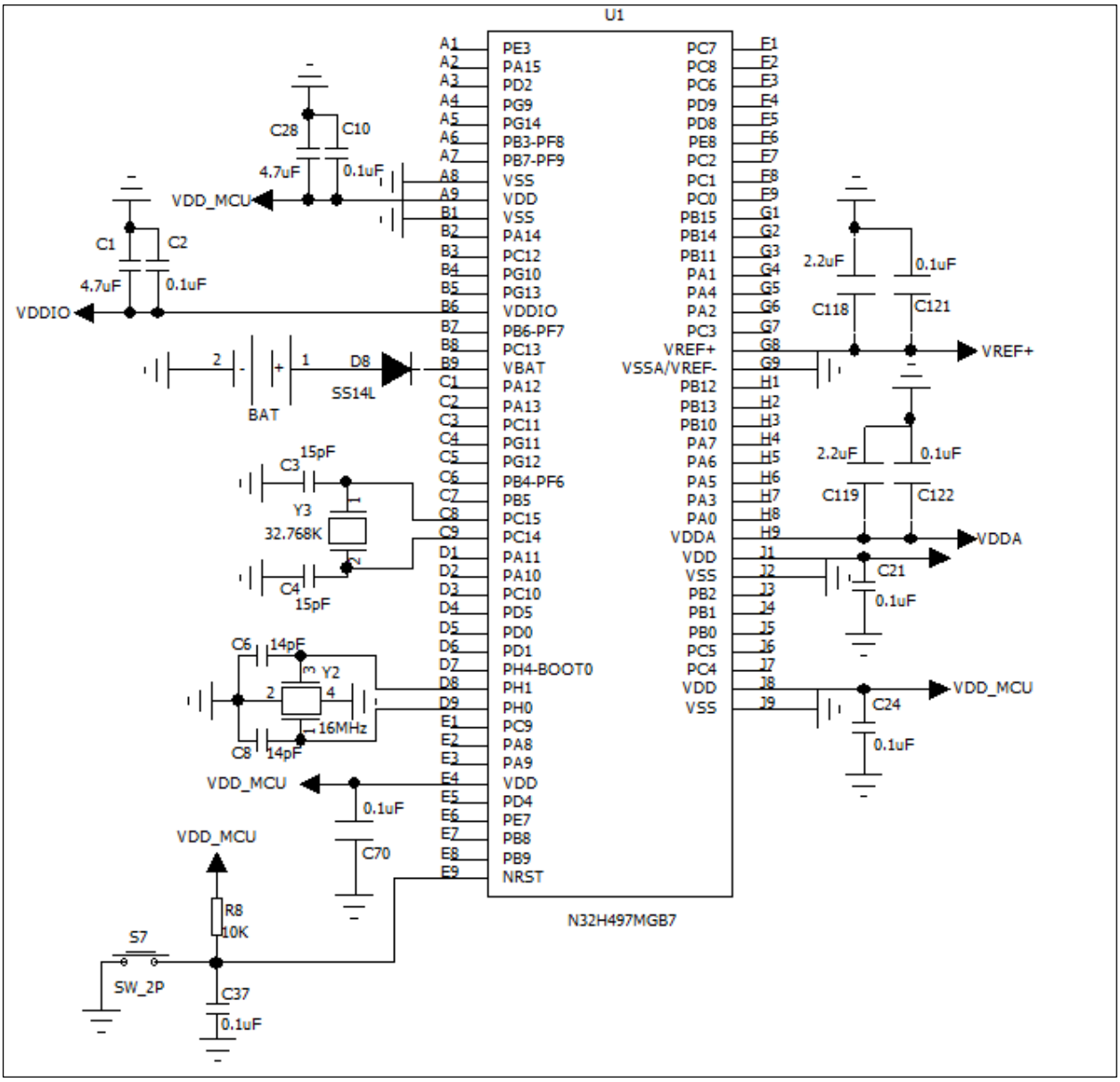

Figure 3-7 BGA81 package minimum system reference design schematic

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3.8 LQFP64-N32H492RGL7

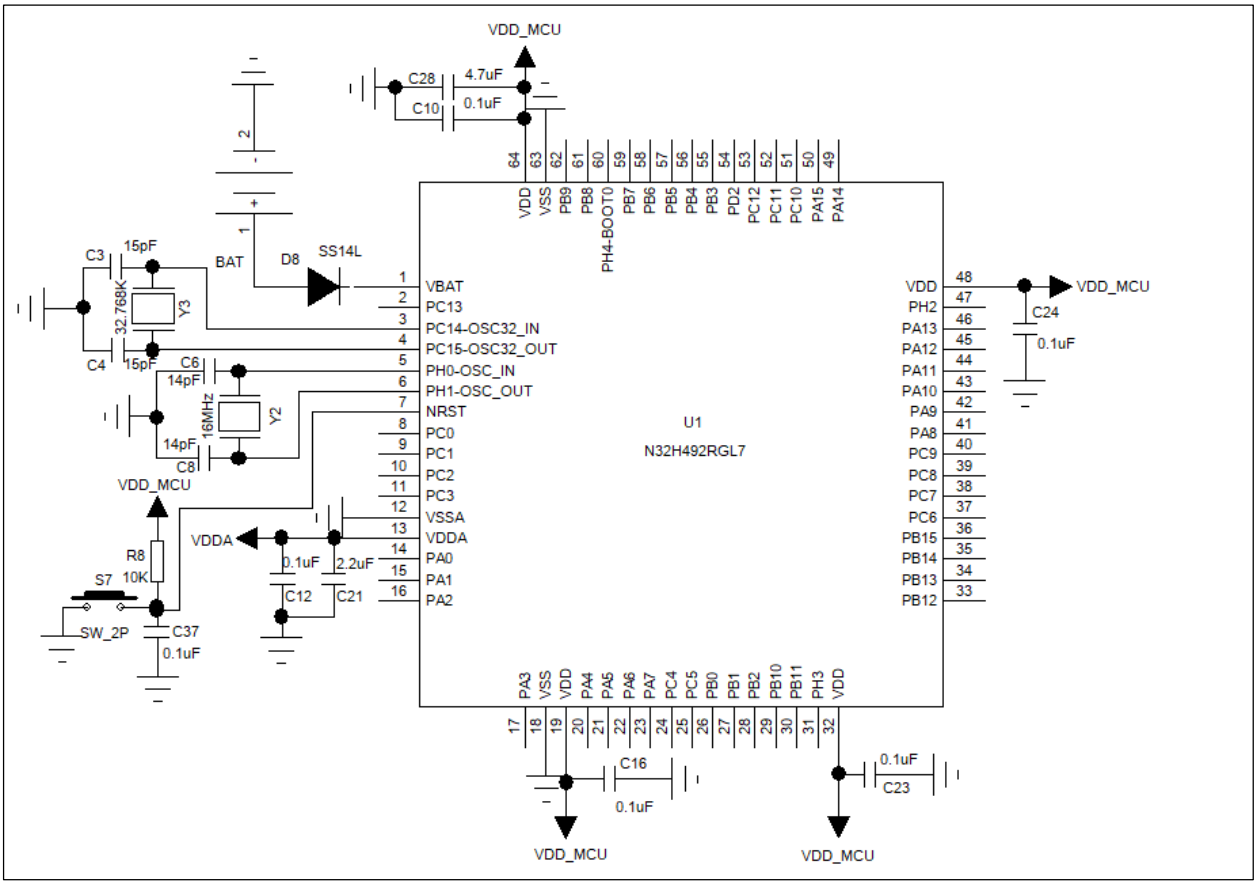

Figure 3-8 LQFP64 package minimum system reference design schematic

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3.9 LQFP100-N32H492VGL7

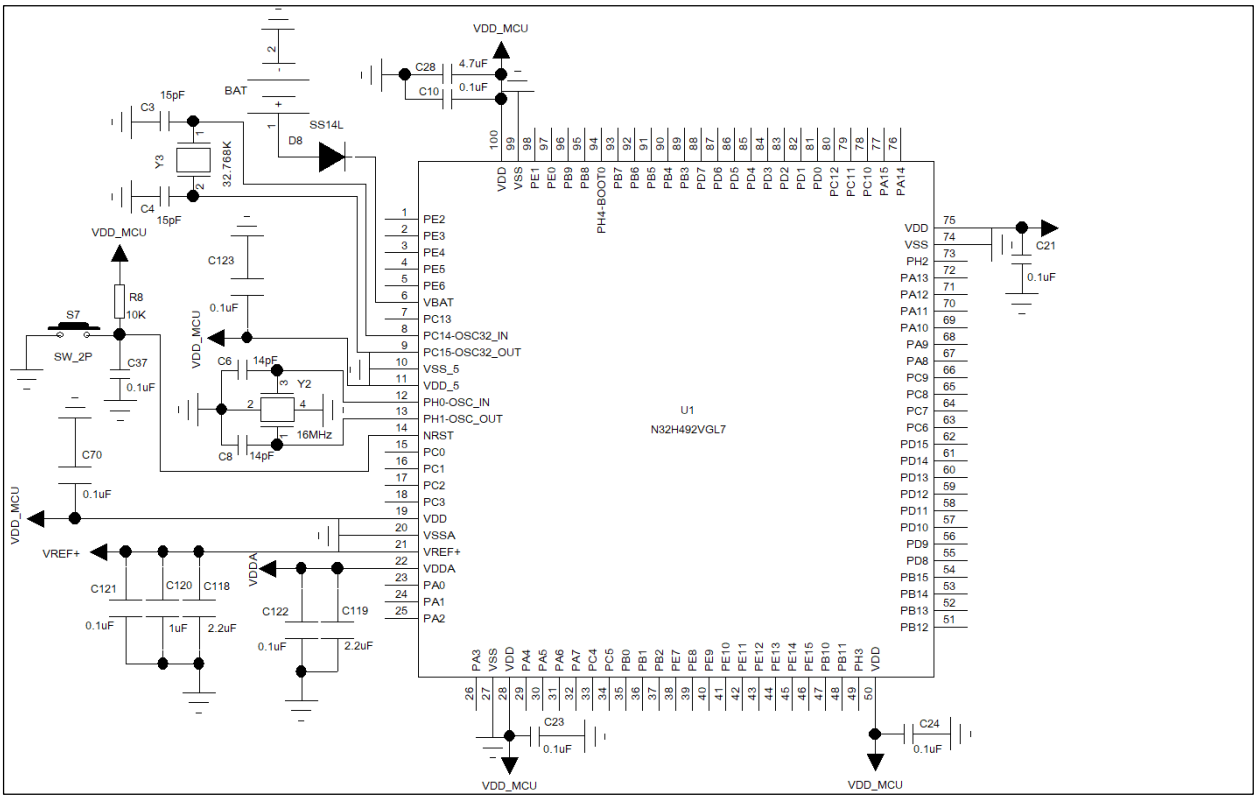

Figure 3-9 LQFP100 package minimum system reference design schematic

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3.10 LQFP144-N32H492ZGL7

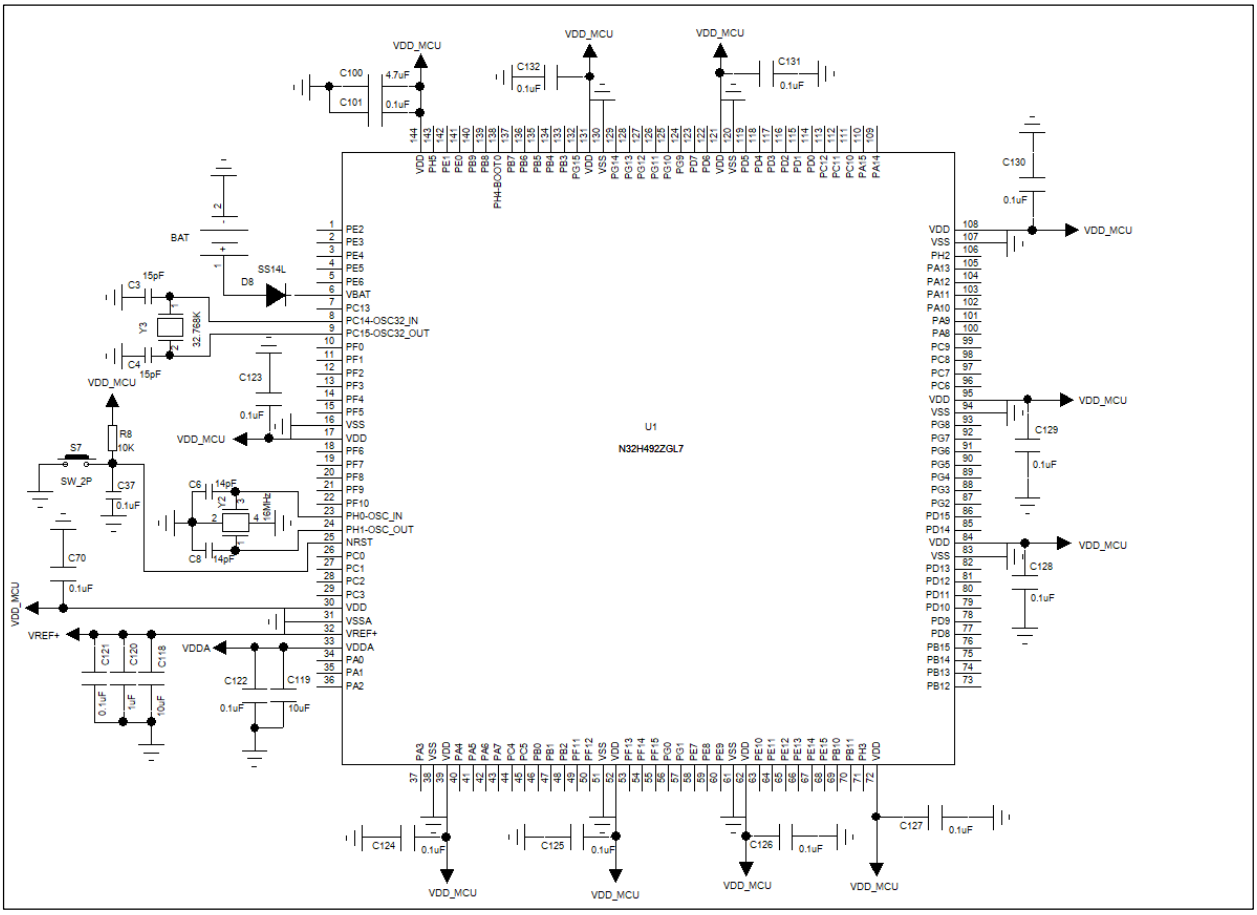

Figure 3-10 LQFP144 package minimum system reference design schematic

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3.11 BGA64-N32H492RGB7

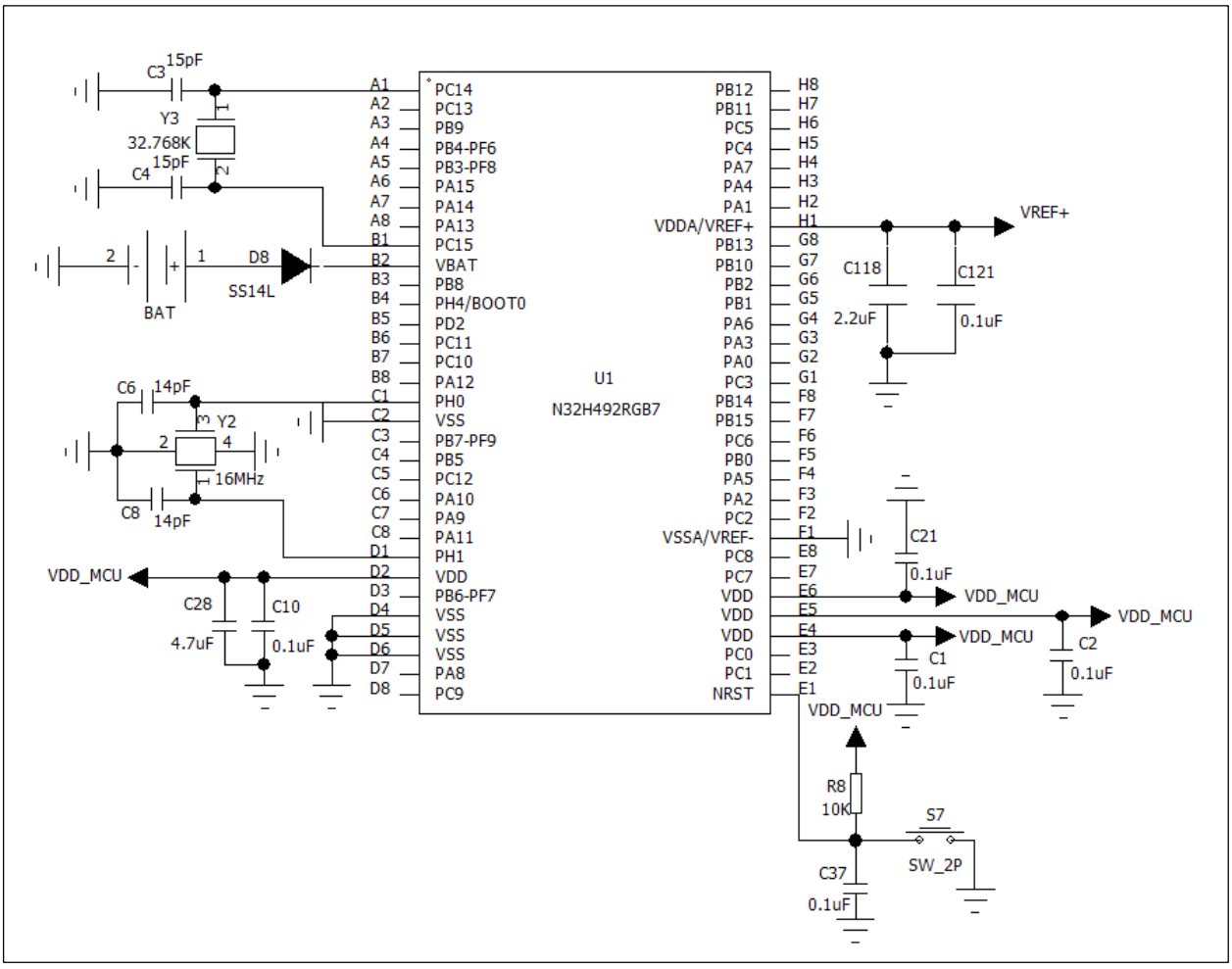

Figure 3-11 BGA64 package minimum system reference design schematic

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3.12 BGA72-N32H492NGB7

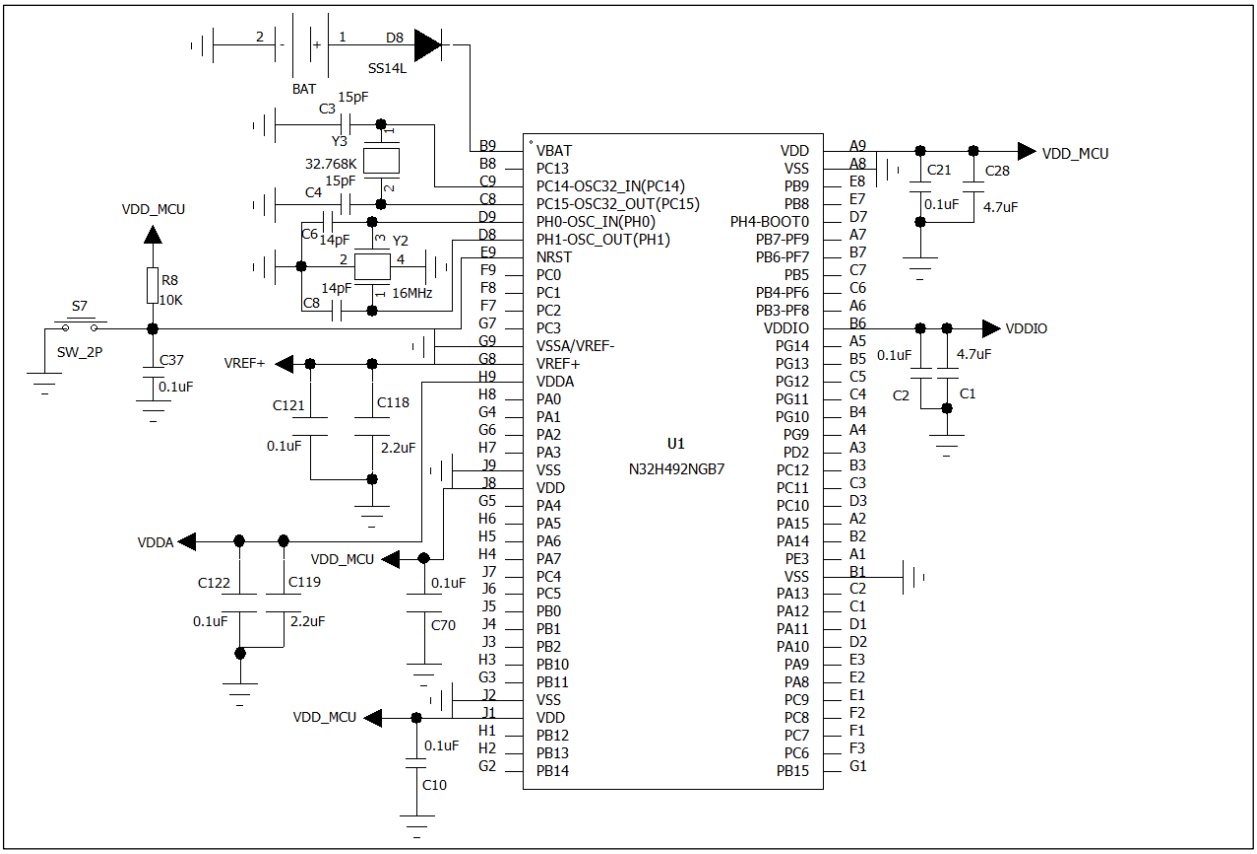

Figure 3-12 BGA72 package minimum system reference design schematic

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3.13 BGA81-N32H492MGB7

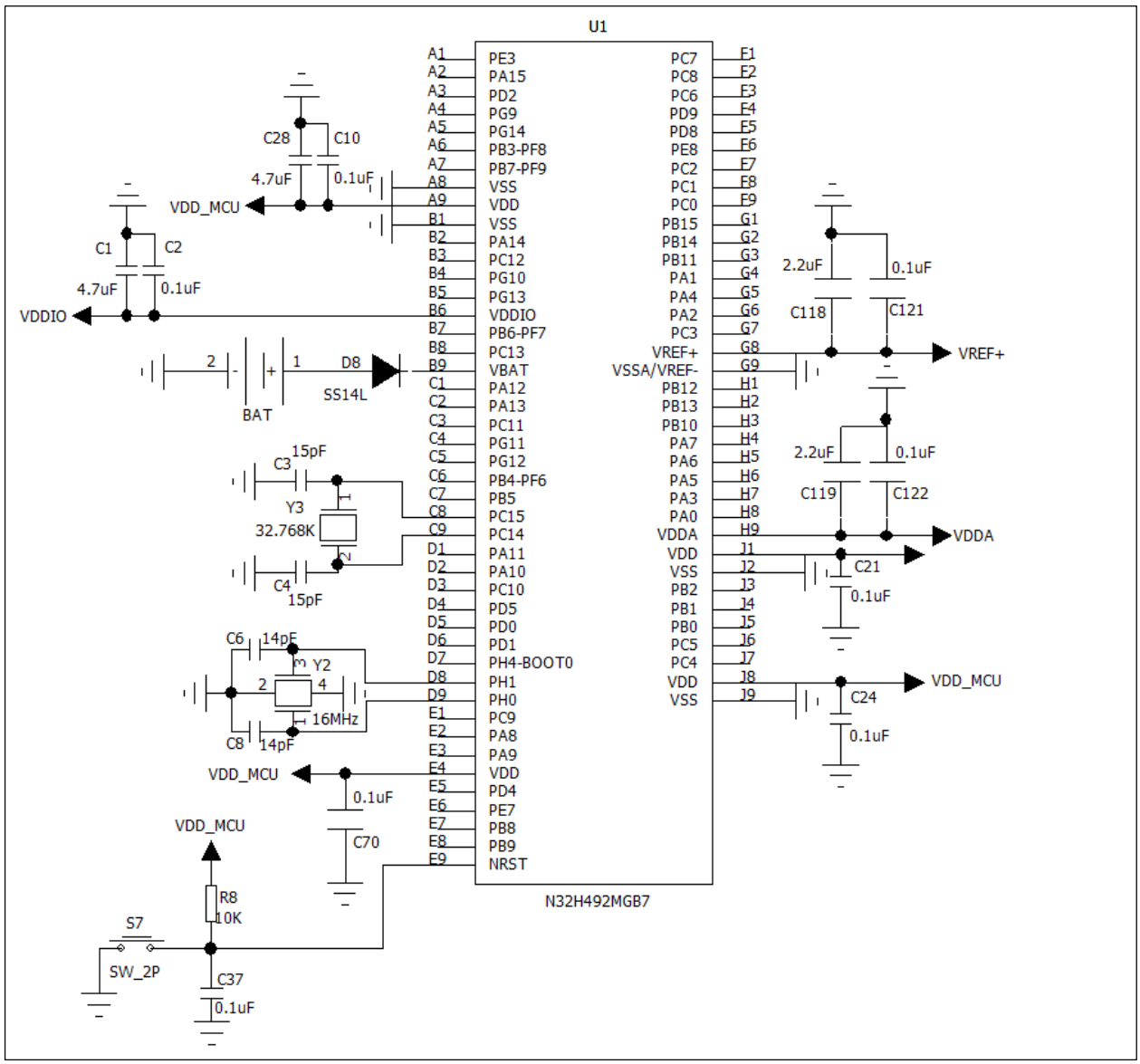

Figure 3-13 BGA81 package minimum system reference design schematic

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3.14 BGA64-N32H493RGB7

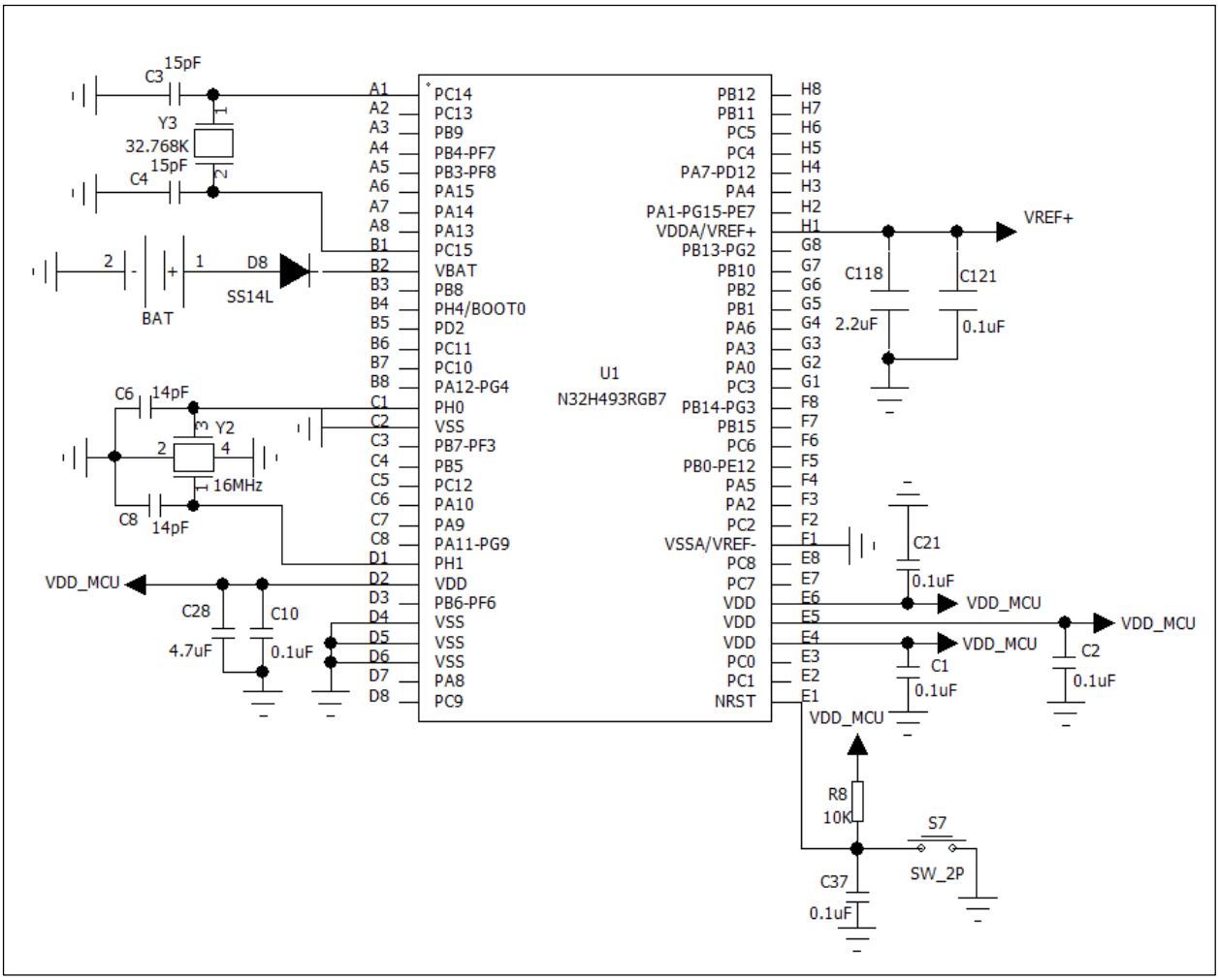

Figure 3-14 BGA64 package minimum system reference design schematic

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3.15 BGA72-N32H493NGB7

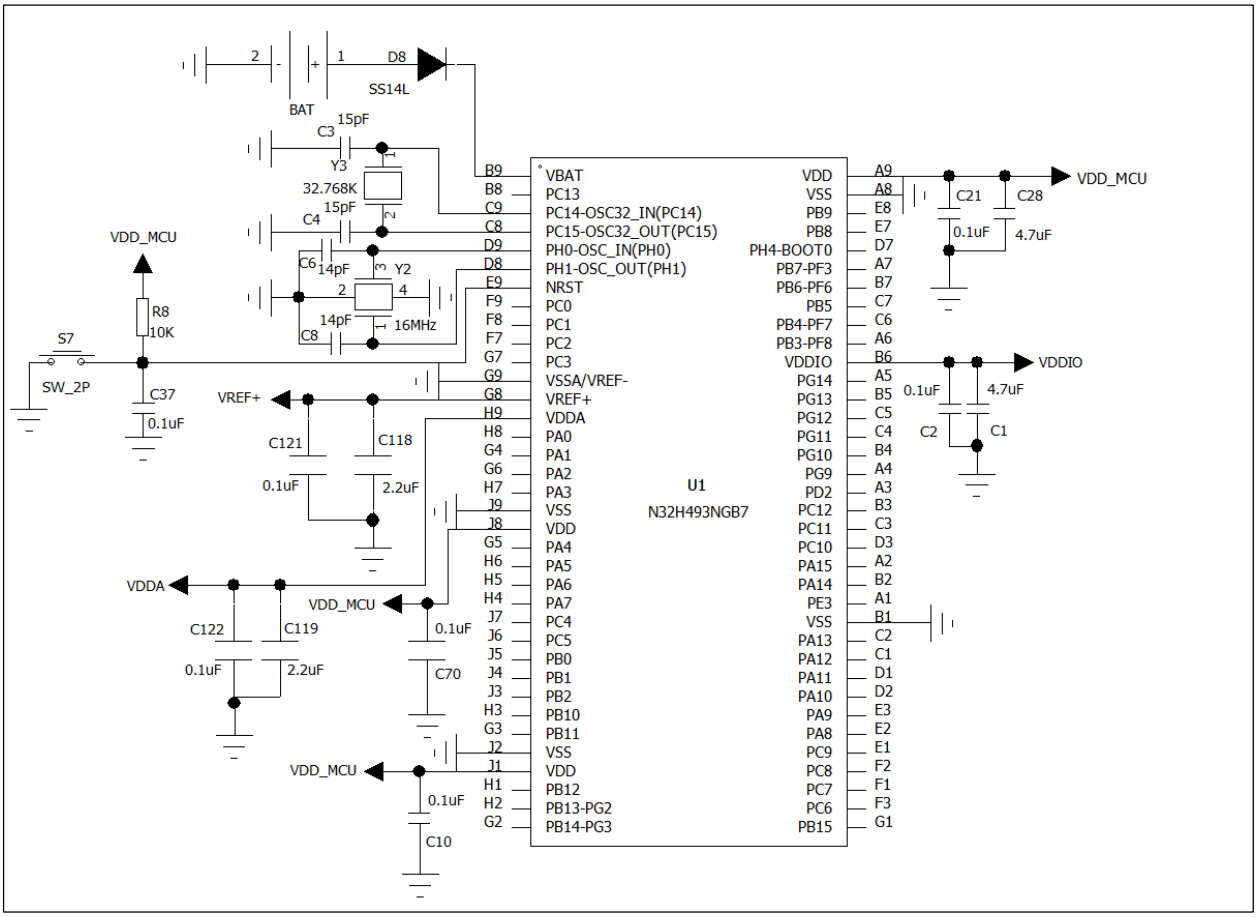

Figure 3-15 BGA72 package minimum system reference design schematic

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3.16 BGA81-N32H493MGB7

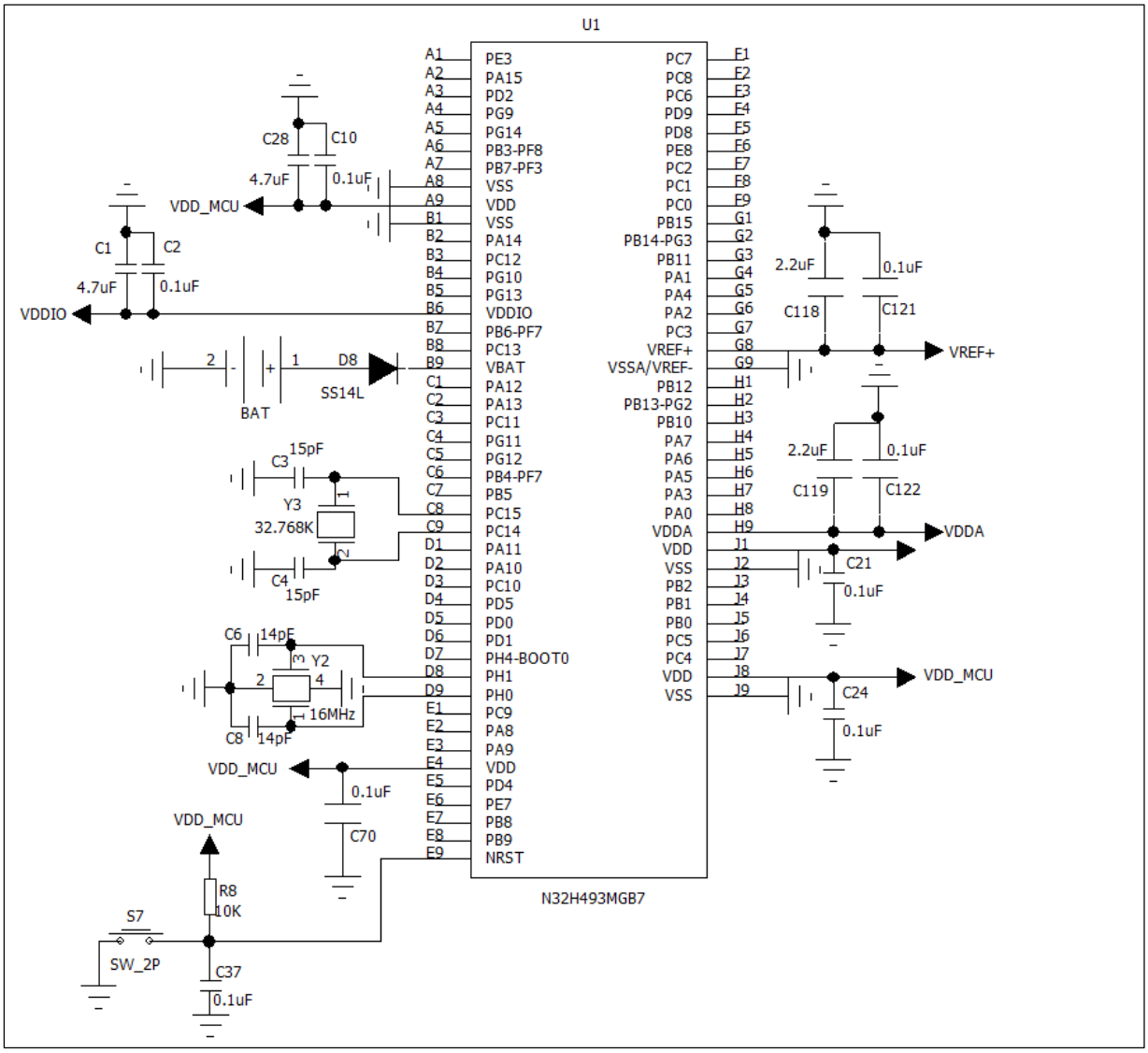

Figure 3-16 BGA81 package minimum system reference design schematic

The above are reference design schematics for minimum systems in different packages, mainly showing the design of power supply decoupling capacitors, clock, reset circuits, etc.

The clock circuit and backup battery depend on the user's design;

The chip supports both internal high-speed and low-speed clocks, allowing users to choose the appropriate one.

The analog power supply VDDA is recommended to be powered by an external stable power supply. If it is directly connected to VDD, appropriate filtering is required.

For N32H492/7 series chips:

When VERF+ uses the built-in reference source VREFBUF, it is recommended to place a 0.1uF and a 1uF capacitor near the VREF+ pin. When VERF+ is externally powered, it is recommended to place a 0.1uF and a 2.2uF capacitor near the VREF+ pin.

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4. PCB LAYOUT Reference

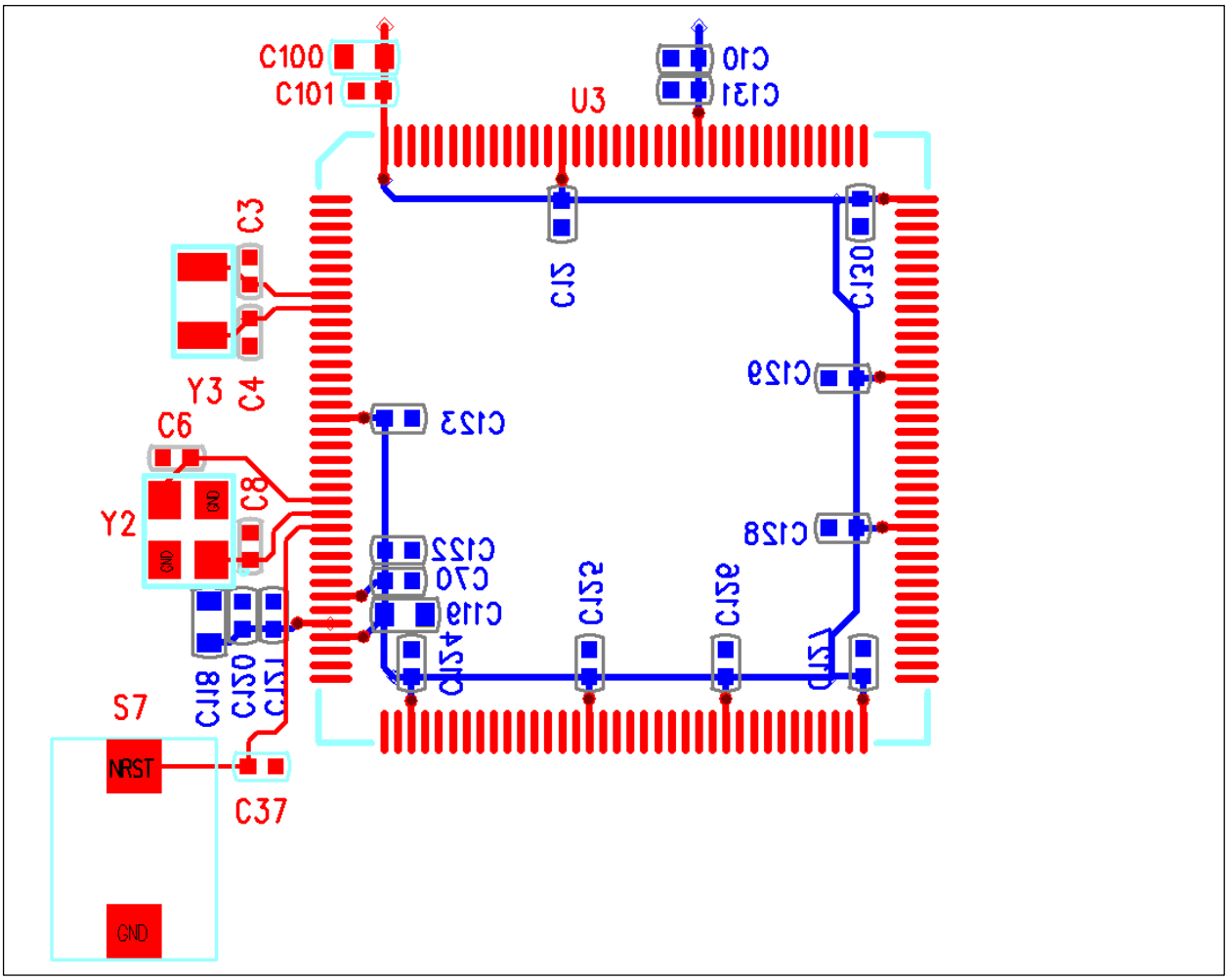

Figure 4-1 LQFP144 package PCB layout reference diagram

Note :

1. When designing the PCB layout, a decoupling capacitor needs to be placed near each power pin;
2. The external crystals and traces of HSE and LSE should be surrounded by ground plane as much as possible. The area on the layer below the crystal close to the crystal also needs to be grounded, and no signal lines should pass through it to prevent signal lines from interfering with the crystal signal.
3. When HSE and LSE are used as crystal oscillators, the traces should not be too long to avoid antenna effects.

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5. Historical versions

Version	date	Remark
V0.6.0	2025-10-28	Create document
V1.0.0	2025-12-26	1、 Add a new chapter "Design Recommendations for High-Speed Communication Interfaces" 2、 Supplement the minimum system reference design schematics for all packages of the 492/493/497 series chips.

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6. statement

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