

# N32H492xE/xG

# Product Brief

N32H492 series employs a 32-bit ARM Cortex-M4F core operating at a maximum frequency of 240MHz, supporting floating-point operations and DSP instructions. It integrates up to 1MB of embedded Flash, 320KB of SRAM (including 80KB of CCM SRAM) plus 4KB of Backup SRAM. The device incorporates three 12-bit 4.7Msps ADCs, two 12-bit DACs, and integrated communication interfaces including USB FS Device, USB HS Host/Device, U(S)ART, I2C, SPI, CAN-FD, and Ethernet. It supports SDIO, FEMC, xSPI, SDRAM high-speed memory interfaces, supports I2S audio interface, supports multiple advanced timers, general-purpose timers, basic timers, low-power timers, built-in cryptographic algorithm hardware acceleration engine, supports AES/TDES, SHA, SM3, SM4, MD5 algorithms, supports TRNG true random number generator, supports CRC16/32.

## Key Features

### ● CPU Core

- 32-bit ARM Cortex-M4F + FPU, single-cycle hardware multiplication and division instruction, support DSP instruction and MPU
- Built-in 8KB I-Cache (instruction cache) and 1KB D-Cache (data cache), supporting Flash Accelerator Unit for zero-wait program execution
- Frequency up to 240 MHz, 300 DMIPS

### ● Memories

- 1MByte on-chip Flash, dual-bank support, enabling secure storage, partition management and data protection, 10,000 erase/write cycles, 10-year data retention
- 240KB general-purpose SRAM, configurable for ECC support; maximum capacity 192KB when ECC enabled
- 80KB CCM SRAM, defaulted as general-purpose SRAM, configurable as CCM SRAM, configurable for ECC support, maximum capacity 64KB when ECC enabled
- 4-KByte of Backup SRAM with ECC available in Standby mode

### ● Power Modes

- Run mode: All peripherals configurable for operation
- Sleep Mode: CPU halted, peripherals configurable for operation
- Stop0 mode: SRAM and all registers can be configured to retention, RTC run
- Standby mode: 6uA, all backup registers and Backup SRAM retained, all IOs retained, optional RTC run
- VBAT mode: 4uA, all backup registers and Backup SRAM retained, optional RTC run

### ● Clock

- HSE: 4MHz~32MHz high-speed external crystal oscillator
- LSE: 32.768KHz low-speed external crystal oscillator
- Built-in multiple high speed PLLs
- MCO: Supports 2-channel clock outputs, which can be configured independently as clock output
- HSI: High-speed internal RC 8MHz, -1.5% to +2% accuracy (full temperature range)
- LSI: Low-speed internal RC 32KHz, +/-10% accuracy (full temperature range)

### ● Reset

- Supports power-on/brown-out/external pin reset
- Supports watchdog reset
- Supports programmable voltage detection
- **GPIOs**
  - Up to 118 GPIOs, PD6 to PD7 and PG9 to PG15 comprise nine I/O pins capable of supporting VDDIO input power supply operation.
- **Communication Interfaces**
  - 1x USB2.0 FS Device interface, built-in PHY, supports crystal-less mode
  - 1 USB High-Speed Host/Device interface, with integrated PHY
  - 6x SPI interfaces, 2x I2S interfaces, support half/full duplex mode, multiplexed with SPI interfaces
  - U(S)ART interfaces
    - ◆ 5x USART interfaces (support ISO7816, IrDA, LIN)
    - ◆ 5x UART interfaces
    - ◆ TX/RX of USART3/UART5/UART8 can be mapped to all pins
  - 4x I2C interfaces(Master/Slave) with speed up to 1 MHz where slave mode support dual address response
  - 3x CAN-FD bus interface, TX/RX can be mapped to all pins
  - 1x IEEE-802.3-2002 compatible Ethernet MAC interface, supports 10M/100M Ethernet, IEEE1588 synchronized Ethernet protocol
  - 1x DVP (Digital Video Port) supporting 8/10/12/16 bit data
- **High Performance Analog Interfaces**
  - 3x 12-bit 4.7 Msps ADCs, supporting 12-bit, 10-bit, 8-bit, and 6-bit sampling precision, with hardware oversampling capability up to 16-bit. ADC1 supports up to 16 external single-ended input channels, while ADC2 and ADC3 support up to 18 external single-ended input channels. Both single-ended and differential modes are supported.
  - 2x 12-bit DACs, each supporting one internal output channel and one external output channel. Sampling rate: 1 Msps. Supports buffered and unbuffered outputs. Capable of internal output, external output, or simultaneous internal and external output.
  - 1x temperature sensor
- **High Speed External Memory Interfaces**
  - 1x xSPI interface, supporting external SRAM, PSRAM and Flash, supporting XIP
  - 1x FEMC (Flexible External Memory Controller) interface, supporting external SRAM, PSRAM, NOR Flash and NAND Flash, 8/16-bit data bus width configurable
  - 1x SDIO interface, support SD/SDIO/MMC format
  - 1x SDRAM interface, configurable 8/16-bit data width
- **Mathematical hardware accelerator CORDIC for motor control functions**
- **Delta Sigma Module Unit (DSMU)**
- **DMA Controllers**
  - 2x DMA controller

- Each controller supports 8 channels
- Channel source address and destination address can be configured arbitrarily
- **RTC real-time clock**
  - Supports leap-year calendar, alarm event, periodic wake up
  - Supports internal and external clock calibration
- **Timers**
  - 3x 16-bit advanced timer/counters supporting input capture, complementary outputs, quadrature encoding inputs, etc., with a maximum control precision of 4.17ns; each timer features six independent channels, four of which support four pairs of complementary PWM outputs
  - 10x general-purpose timers (GTIM1–10):
    - GTIM2/3/5/6/7: 16-bit counters with a maximum control precision of 4.17 ns. Each timer features up to 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output.
    - GTIM1/4: 32-bit counters with maximum control precision of 4.17 ns. Each timer provides up to 4 independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output;
    - GTIM8–10, 16-bit counters with a maximum control precision of 4.17 ns. Each timer features up to four independent channels, each supporting input capture, output compare, PWM generation, and single-pulse mode output. Only Channel 1 supports complementary outputs with dead time and brake input capability.
  - 2x 32-bit basic timers
  - 2x 16-bit low-power timer, can operate in Stop0 and Standby mode.
  - 1x 24-bit SysTick timer.
  - 1x 14-bit Window Watchdog (WWDG)
  - 1x 12-bit Independent Watchdog (IWDG)
- **Programming Methods**
  - Support SWD/JTAG debugging interface.
  - Support UART and USB Bootloader
- **Security Features**
  - Flash encryption, multi-user partition management unit (SMPU)
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Built-in hardware acceleration engine for cryptographic algorithm
  - Supports AES/TDES, SHA, SM3, SM4, and MD5 algorithms
  - True random number generator(TRNG)
  - CRC16/32 operation
  - Supports secure boot, program encryption download, secure firmware update
  - Supports external clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**

- **Operating Conditions**

- Operating voltage range: 1.8V~3.6V
- Operating temperature range: -40°C ~ 105°C

- **Packages**

- LQFP64(10mm x 10mm)
- BGA64 (5mm x 5mm)
- BGA72 (4.41mm x 3.76mm)
- BGA81 (4.41mm x 3.76mm)
- LQFP100(14mm x 14mm)
- LQFP144(20mm x 20mm)

# 1 Ordering Information

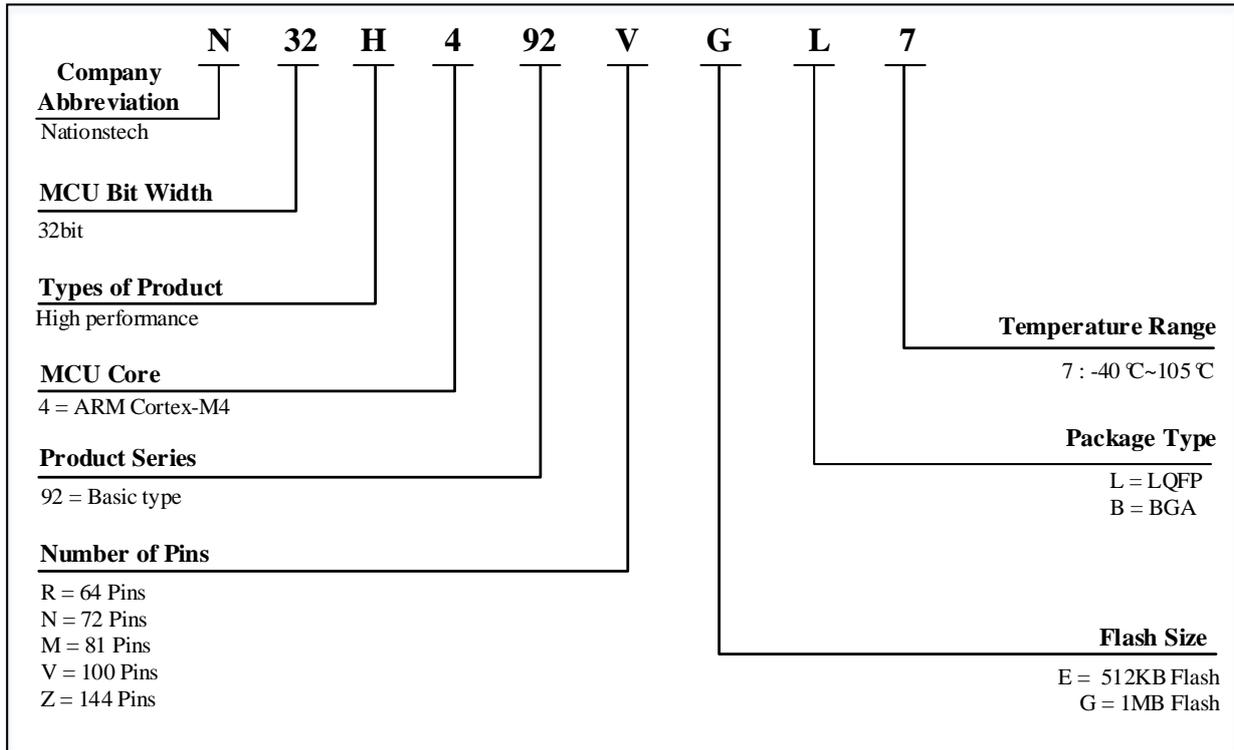


Table 1-1 N32H492 Series Ordering Code

Ordering Code <sup>(1)</sup>	Package	Size	Packaging <sup>(2)</sup>	SPQ <sup>(3)</sup>	Temperature range
N32H492RGL7	LQFP64	10mm x 10mm	Tray	160	-40°C~105°C
N32H492RGB7	BGA64	5mm x 5mm	TBD	TBD	-40°C~105°C
N32H492NGB7	BGA72	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H492MGB7	BGA81	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H492VGL7	LQFP100	14mm x 14mm	Tray	90	-40°C~105°C
N32H492ZGL7	LQFP144	20mm x 20mm	Tray	60	-40°C~105°C
N32H492REL7	LQFP64	10mm x 10mm	Tray	160	-40°C~105°C
N32H492REB7	BGA64	5mm x 5mm	TBD	TBD	-40°C~105°C
N32H492NEB7	BGA72	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H492MEB7	BGA81	4.41mm x 3.76mm	TBD	TBD	-40°C~105°C
N32H492VEL7	LQFP100	14mm x 14mm	Tray	90	-40°C~105°C
N32H492ZEL7	LQFP144	20mm x 20mm	Tray	60	-40°C~105°C

1. For the latest detailed-ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact Naitons.
3. Minimum packaging quantity.

## 2 Product Configurations

**Table 2-1 N32H492 Series Product Configuration**

Device		N32H492RE/RGL7	N32H492RE/RGB7	N32H492NE/NGB7	N32H492ME/MGB7	N32H492VE/VGL7	N32H492ZE/ZGL7						
Operating Condition		1.8~3.6V/-40~105°C											
CPU Frequency		ARM Cortex-M4F @240MHz, 300DMIPS											
Flash Capacity (KB)		512	1024	512	1024	512	1024	512	1024	512	1024	512	1024
Total SRAM (KB)	General SRAM	240 <sup>(1)</sup>											
	CCM SRAM <sup>(2)</sup>	80 <sup>(3)</sup>											
	Backup SRAM	4											
Times	ATIM	3*16bit											
	GTIM	5*16bit											
		2*32bit <sup>(4)</sup>											
		3*16bit <sup>(5)</sup>											
	BTIM	2*32bit											
	LPTIM	2*16bit											
	SysTick timer	1											
	WWDG	1*14bit											
	IWDG	1*12bit											
RTC	Yes												
Communication Interfaces	SPI/I2S	5/2					6/2						
	I <sup>2</sup> C	4											
	USART	5											
	UART	5											
	USB FS Device	Yes <sup>(6)</sup>											
	USB HS DualRole	Yes <sup>(6)</sup>											
	FDCAN	3											
	Ethernet	Yes											
Memory	XSPI	Yes											

Expansion	FEMC	No				Yes <sup>(7)</sup>	Yes
	SDIO	Yes					
	SDRAM	No				Yes	
Human-computer interaction	DVP	Yes					
GPIO		54	52	59	67	85	118
WKUP Pins		5	5	5	5	7	7
Nb of I/Os down to 1.8 V <sup>(8)</sup>		0	0	6	6	0	9
DMA		2					
Number of channels		16					
12bit ADC		3	3	3	3	3	3
Number of channels		20	23	23	23	20	28
12bit DAC		2					
Number of channels		2					
Algorithm Support		DES/3DES、AES、SHA1/SHA224/SHA256、SM3、SM4、MD5、CRC16/CRC32					
TRNG		Yes					
Cordic		Yes					
DSMU		1					
Number of channels		8					
Security Protection		Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot					
Package		LQFP64	BGA64	BGA72	BGA81	LQFP100	LQFP144

**Note:**

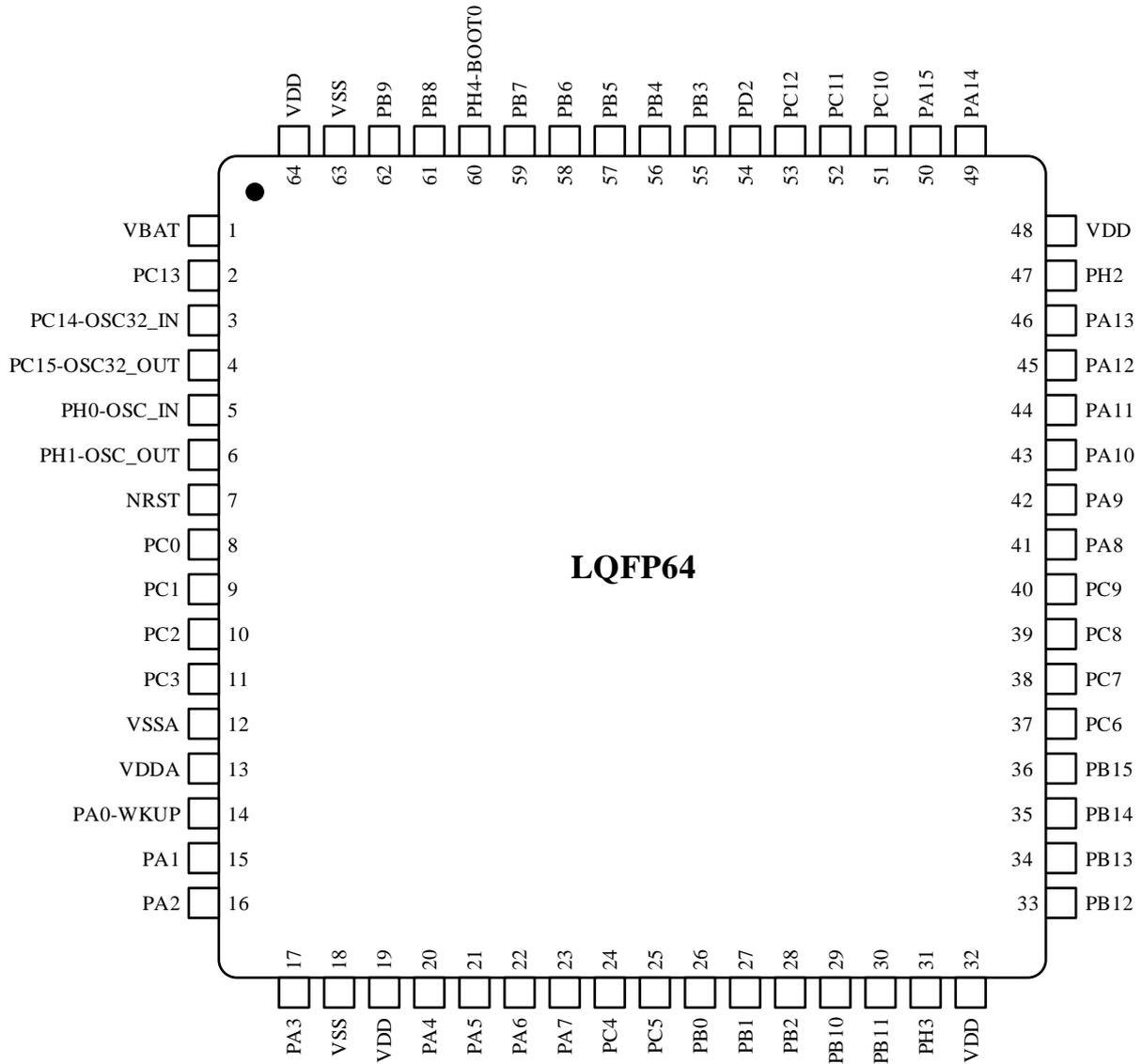
1. With ECC enabled, SRAM capacity is 192KB; without ECC enabled, SRAM capacity is 240KB. ECC is enabled by default.
2. Upon power-up, the default configuration is general-purpose SRAM; software can configure it as CCM SRAM.
3. With ECC enabled, SRAM capacity is 64KB; without ECC enabled, SRAM capacity is 80KB. ECC is enabled by default.
4. Only GTIM1 and GTIM4 support 32-bit timers;
5. Only GTIM8/9/10 support brake functionality, with channel 1 supporting complementary channel output;
6. For BGA81/71/64 packages, USB FS Device and USB HS Host/Device are mutually exclusive;
7. Only supports lower 16-bit address and data multiplexing mode;

8. *For BGA81 and BGA72 packages, pins PG9 to PG14 may support operation powered via the VDDIO input. For LQFP144 packages, pins PD6 to PD7 and PG9 to PG15 may support operation powered via the VDDIO input, with input voltage support ranging from 1.8V to 3.6V.*

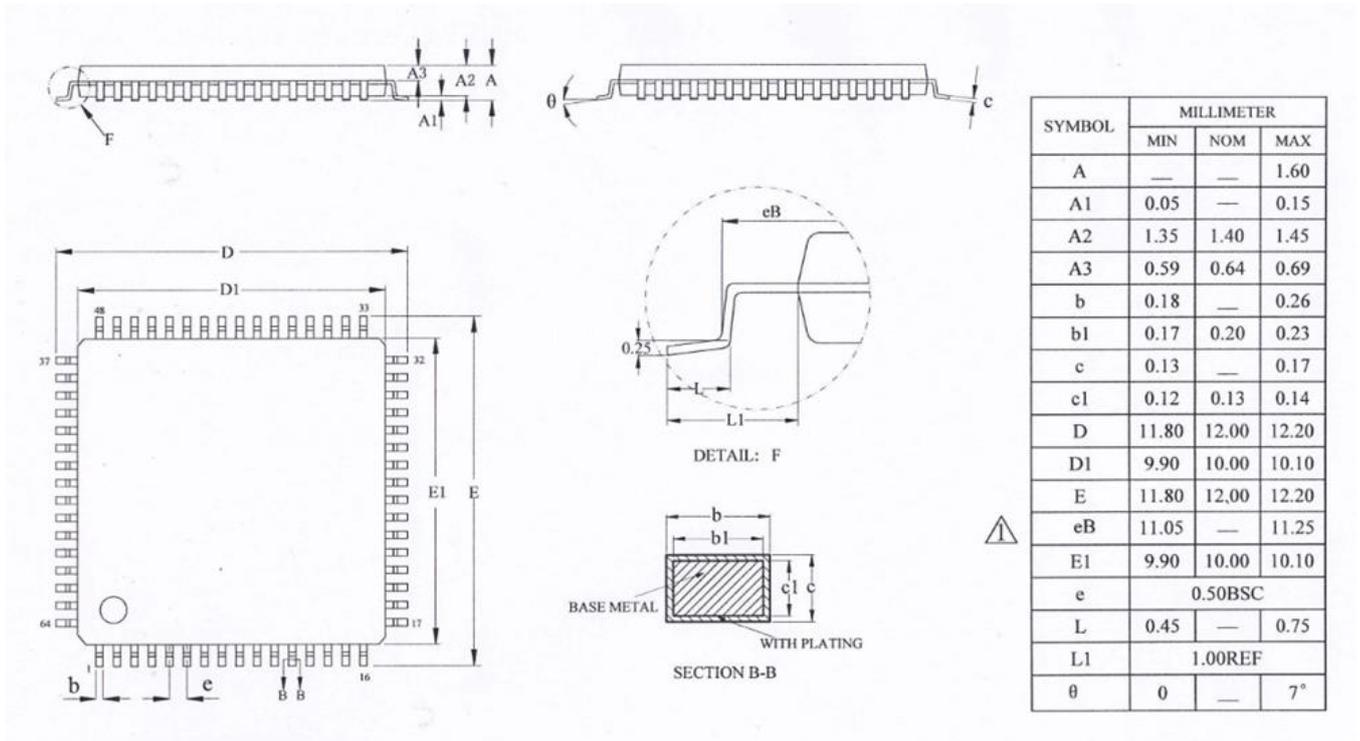
### 3 Package

#### 3.1 LQFP64

##### 3.1.1 LQFP64 Pinout

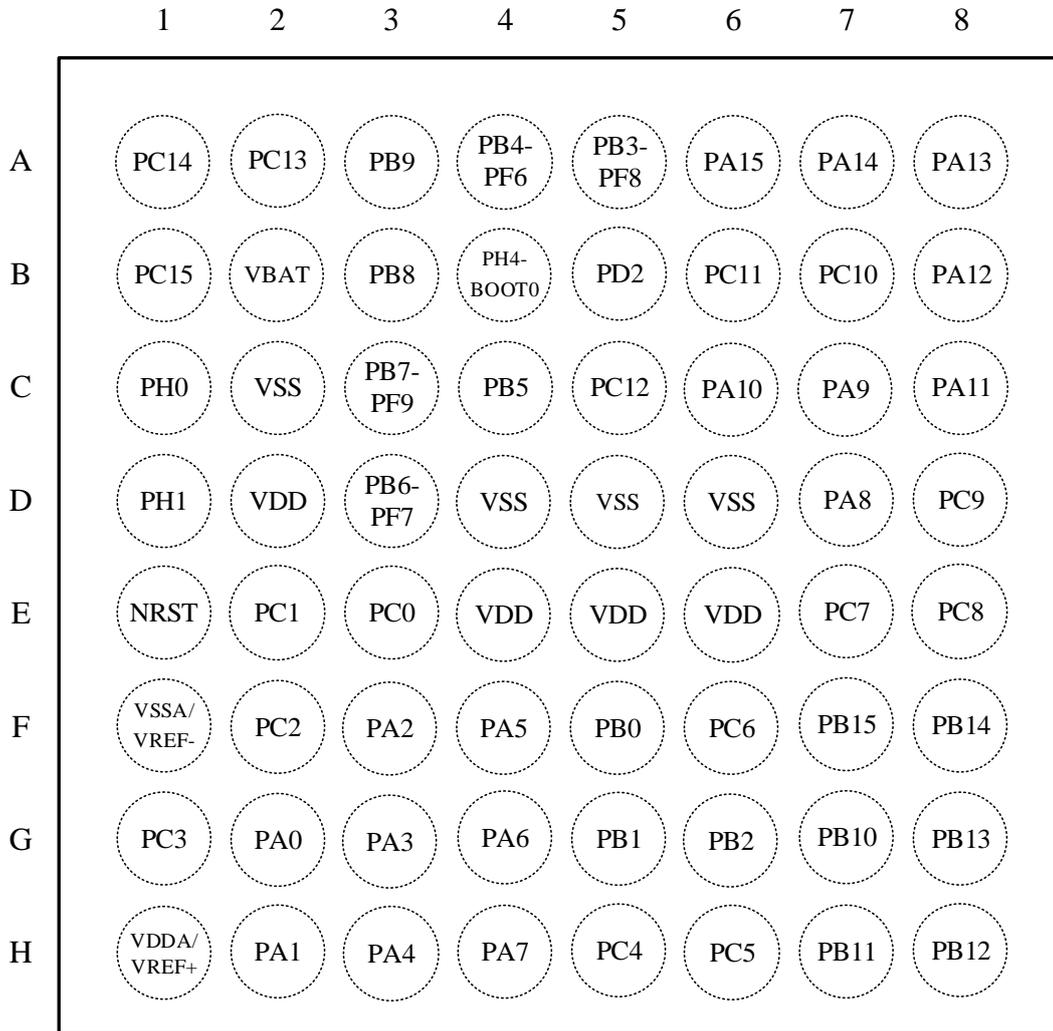


### 3.1.2 LQFP64 Package



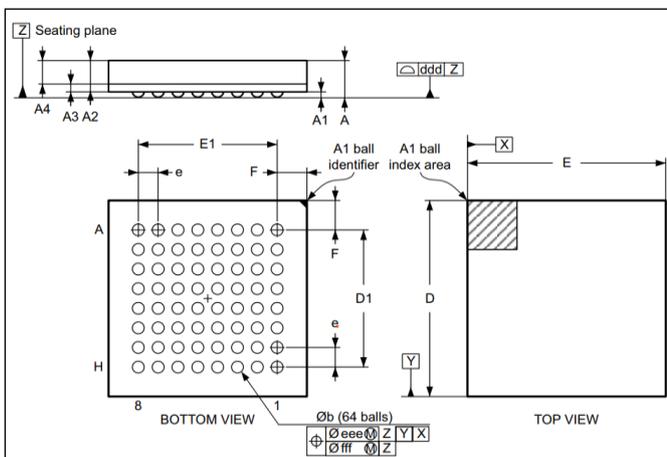
### 3.2 BGA64

#### 3.2.1 BAG64 Pinout



Top view

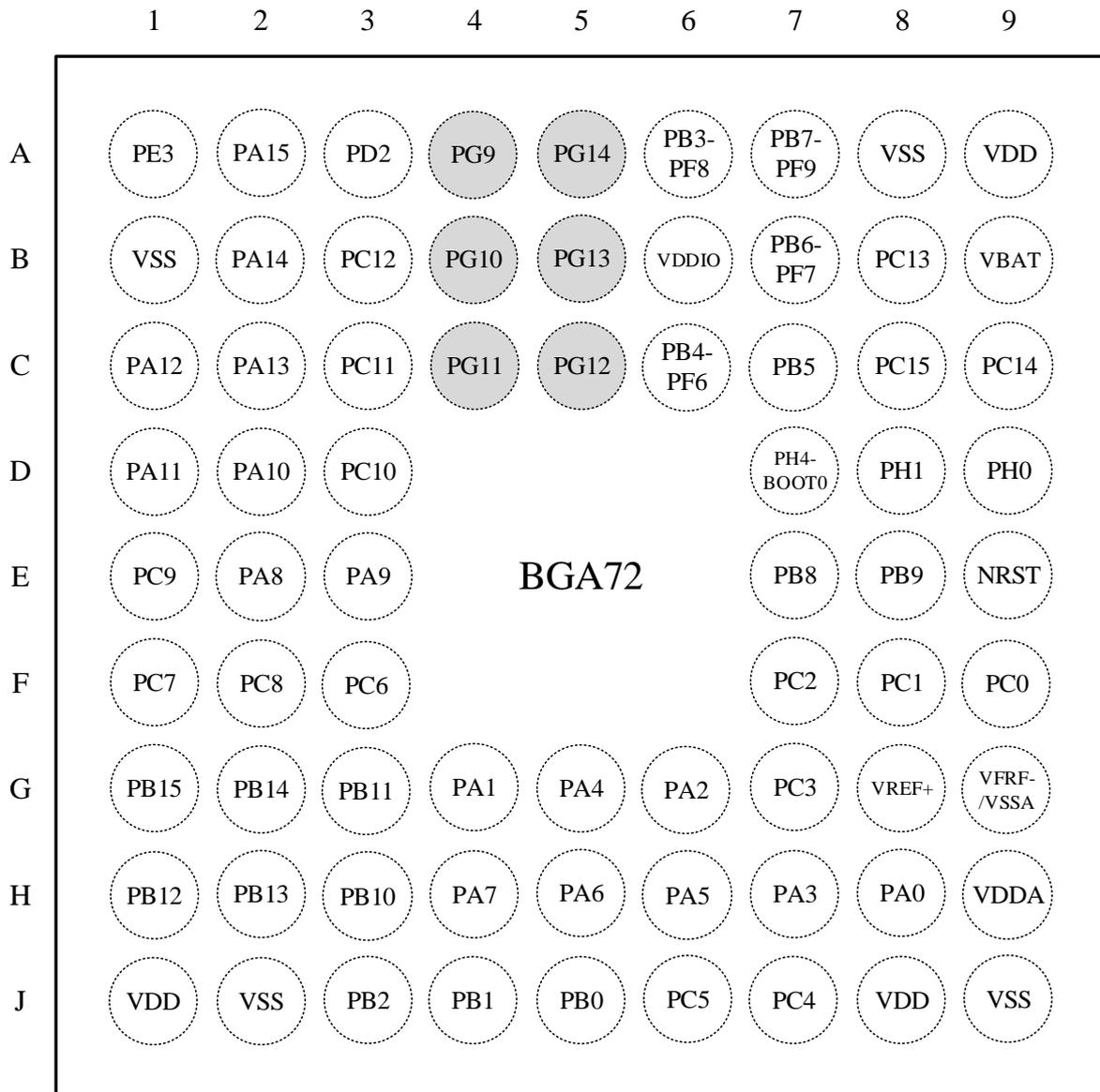
#### 3.2.2 BGA64 Package



Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

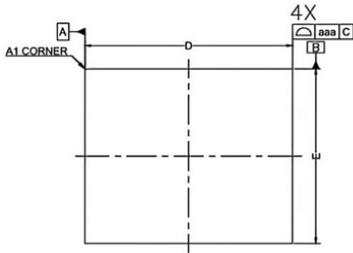
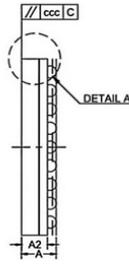
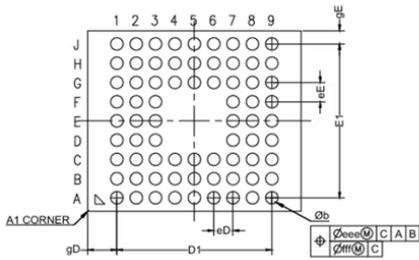
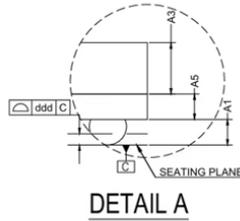
### 3.3 BGA72

#### 3.3.1 BGA72 Pinout



Top view

### 3.3.2 BGA72 Package


**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

**DETAIL A**
**COMMON DIMENSIONS**

(UNITS OF MEASURE=MILLIMETER)

ITEM	SYMBOL	COMMON DIMENSIONS			
		MIN.	NOM.	MAX.	
Body Size	X	D	4.300	4.400	4.500
	Y	E	3.660	3.760	3.860
Ball Pitch	X	eD	0.400		
	Y	eE	0.400		
Total Thickness	A	0.662	0.733	0.804	
Ball Stand Off	A1	0.138	0.188	0.238	
Mold+Substrate	A2	0.495	0.545	0.595	
Mold Thickness	A3	0.325	0.365	0.405	
Substrate Thickness	A5	0.150	0.180	0.210	
Ball Size	b	0.208	0.258	0.308	
Package Edge Tolerance	aaa	0.100			
Mold Flatness	ccc	0.200			
Coplanarity	ddd	0.080			
Ball Offset (Package)	eee	0.150			
Ball Offset (Ball)	fff	0.050			
Ball Count	n	72			
Edge Ball Center to Center	X	D1	3.200		
	Y	E1	3.200		
Edge Ball Center to Package Edge	X	gD	0.600		
	Y	gE	0.280		

**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSITIONS DESIGNATION PER JESD 95.

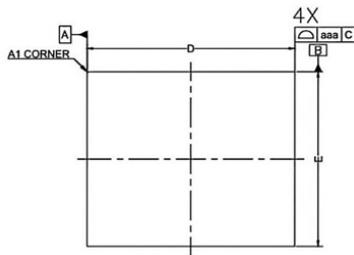
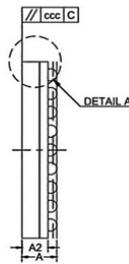
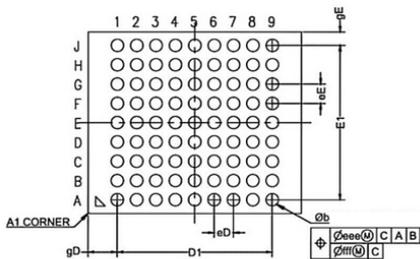
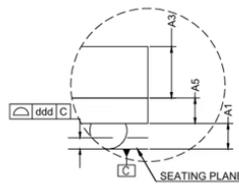
## 3.4 BGA81

### 3.4.1 BGA81 Pinout

	1	2	3	4	5	6	7	8	9
A	PE3	PA15	PD2	PG9	PG14	PB3-PF8	PB7-PF9	VSS	VDD
B	VSS	PA14	PC12	PG10	PG13	VDDIO	PB6-PF7	PC13	VBAT
C	PA12	PA13	PC11	PG11	PG12	PB4-PF6	PB5	PC15	PC14
D	PA11	PA10	PC10	PD5	PD0	PD1	PH4-BOOT0	PH1	PH0
E	PC9	PA8	PA9	VDD	PD4	PE7	PB8	PB9	NRST
F	PC7	PC8	PC6	PD9	PD8	PE8	PC2	PC1	PC0
G	PB15	PB14	PB11	PA1	PA4	PA2	PC3	VREF+	VFRF-/VSSA
H	PB12	PB13	PB10	PA7	PA6	PA5	PA3	PA0	VDDA
J	VDD	VSS	PB2	PB1	PB0	PC5	PC4	VDD	VSS

Top view

### 3.4.2 BGA81 Package


**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

**DETAIL A**
**COMMON DIMENSIONS**

(UNITS OF MEASURE=MILLIMETER)

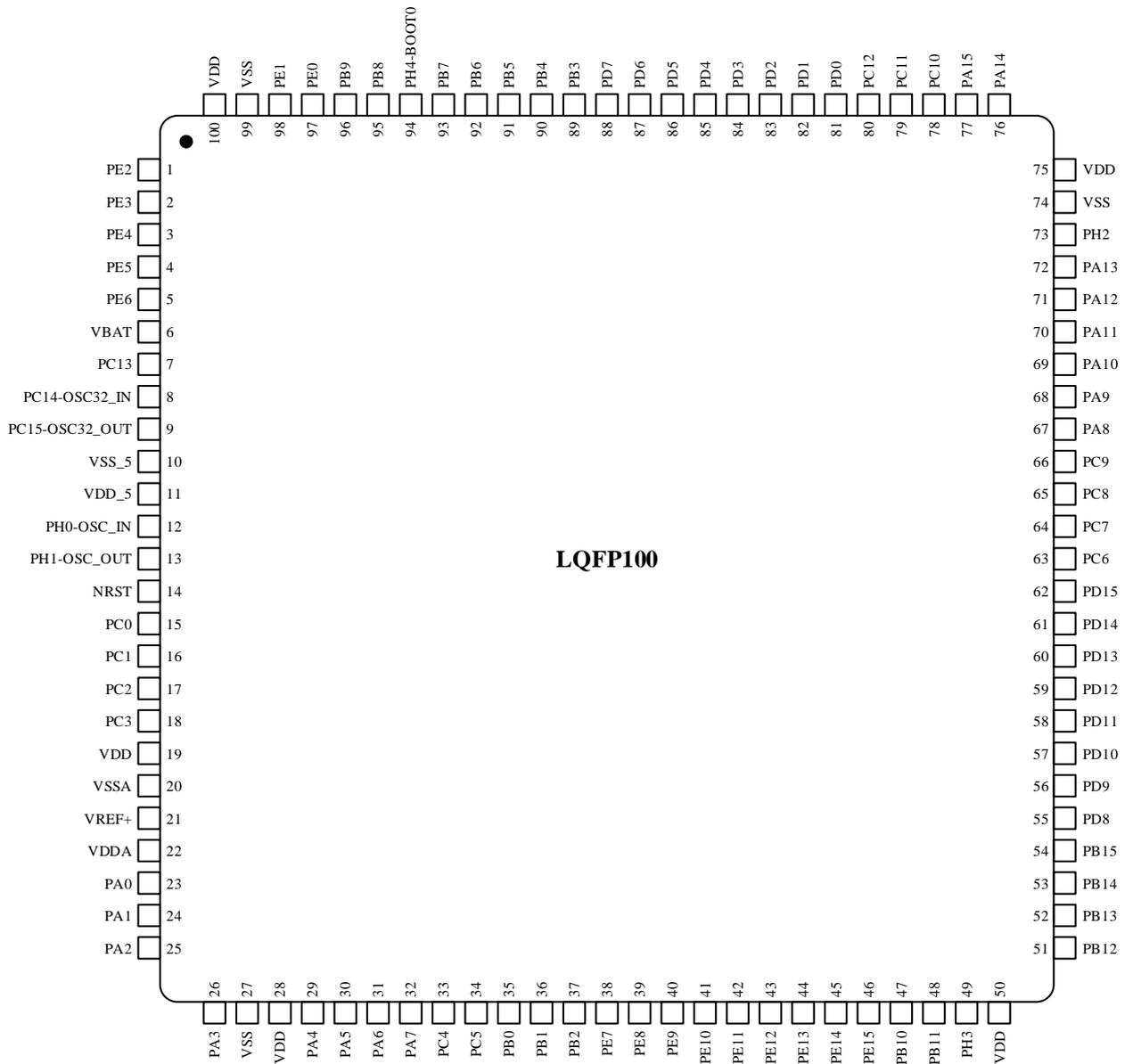
ITEM	SYMBOL	COMMON DIMENSIONS			
		MIN.	NOM.	MAX.	
Body Size	X	D	4.300	4.400	4.500
	Y	E	3.660	3.760	3.860
Ball Pitch	X	eD	0.400		
	Y	eE	0.400		
Total Thickness	A	0.662	0.733	0.804	
Ball Stand Off	A1	0.138	0.188	0.238	
Mold+Substrate	A2	0.495	0.545	0.595	
Mold Thickness	A3	0.325	0.365	0.405	
Substrate Thickness	A5	0.150	0.180	0.210	
Ball Size	b	0.208	0.258	0.308	
Package Edge Tolerance	aaa	0.100			
Mold Flatness	ccc	0.200			
Coplanarity	ddd	0.080			
Ball Offset (Package)	eee	0.150			
Ball Offset (Ball)	fff	0.050			
Ball Count	n	81			
Edge Ball Center to Center	X	D1	3.200		
	Y	E1	3.200		
Edge Ball Center to Package Edge	X	gD	0.600		
	Y	gE	0.280		

**NOTES**

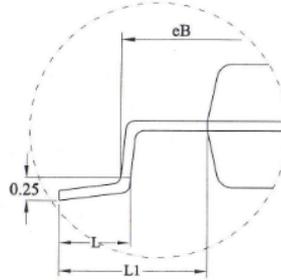
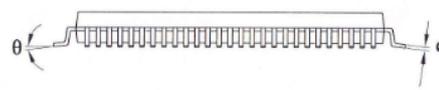
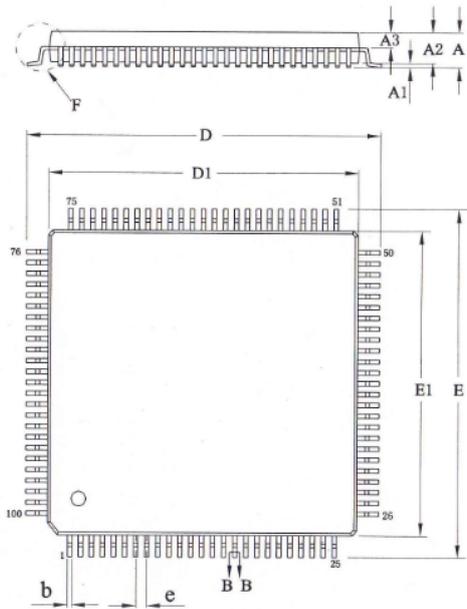
1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSITIONS DESIGNATION PER JESD 95.

## 3.5 LQFP100

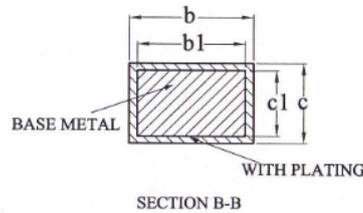
### 3.5.1 LQFP100 Pinout



### 3.5.2 LQFP100 Package



DETAIL: F

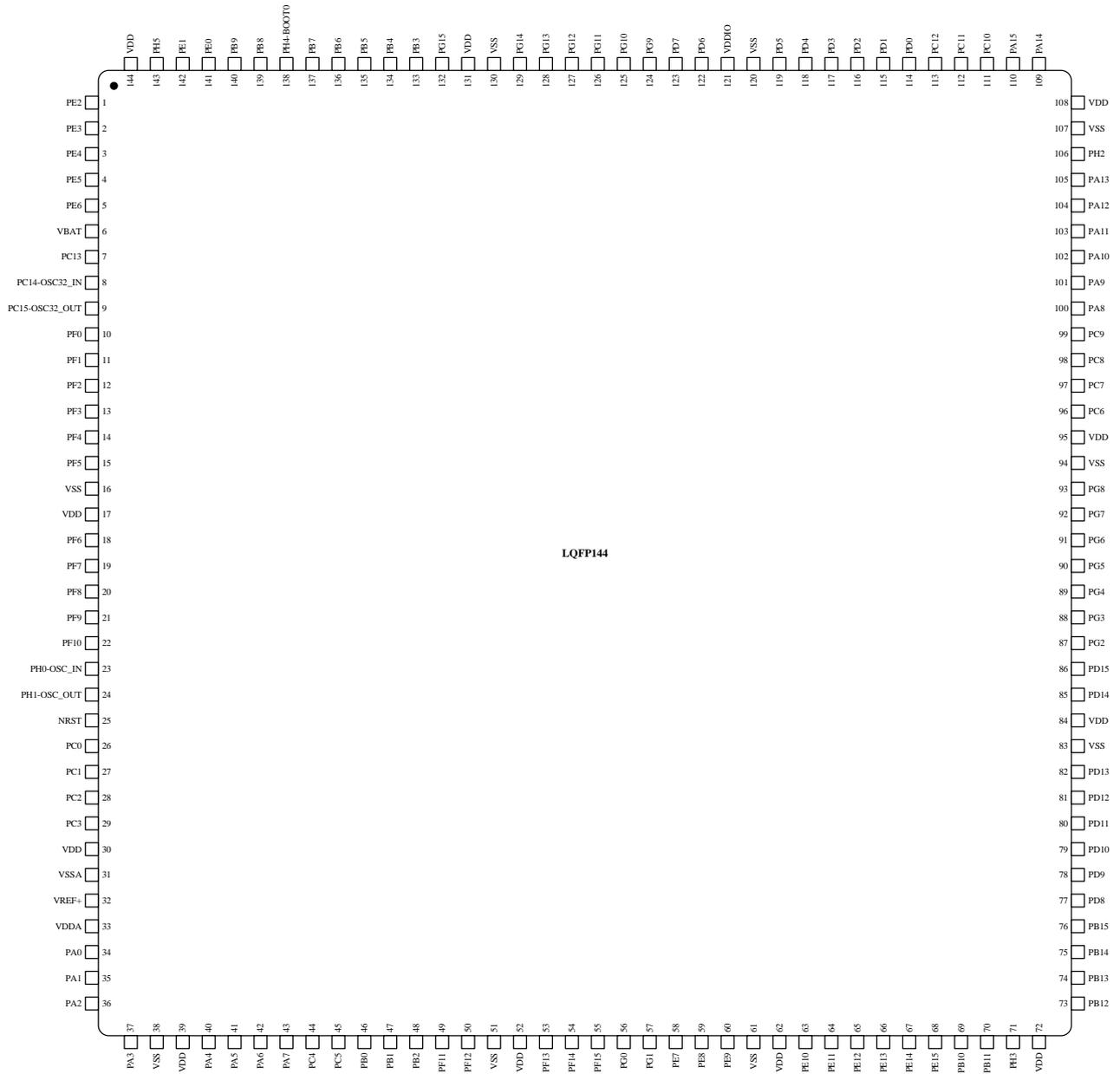


SECTION B-B

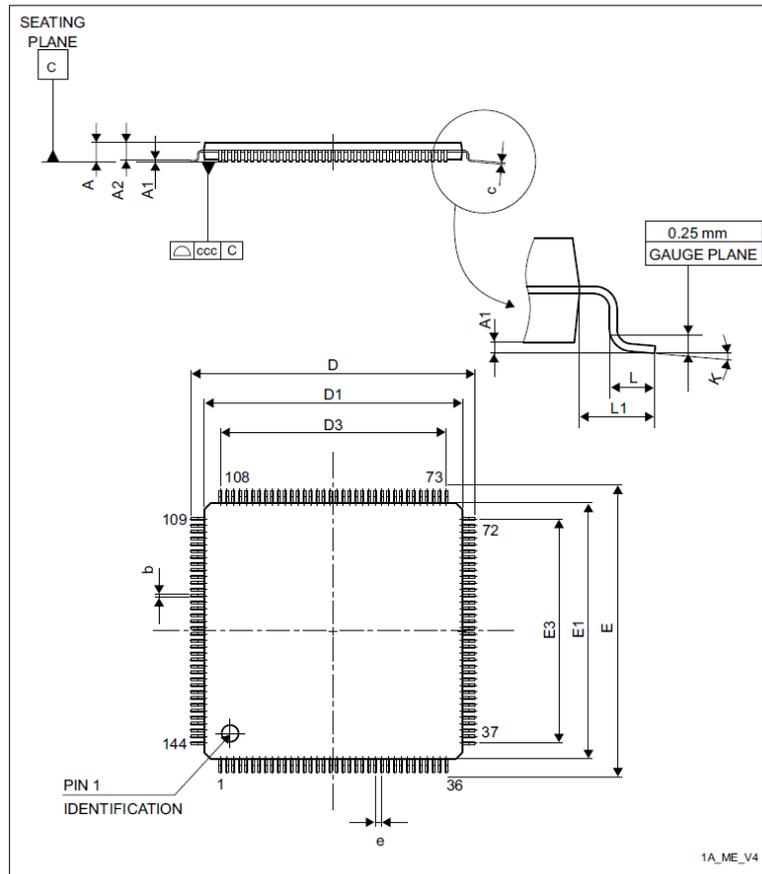
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7

## 3.6 LQFP144

### 3.6.1 LQFP144 Pinout



### 3.6.2 LQFP144 Package



Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

## 4 Version History

Date	Version	Changes
2026.1.22	V1.0.0	Initial release.

## 5 Disclaimer

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