N32A052xx Product Brief

N32A052 series based on Arm® Cortex®-M0, run up to 64MHz, up to 128KB embedded Flash, 8KB data Flash, 16KB SRAM, integrated analog interface, 1x12bit 1Msps ADC, 4x Comparator, 1x8/12bit 1Msps DAC, integrated multi-channel UART, I2C, SPI, CAN and other digital communication interfaces, Segment LCD Driver Interface, built-in password algorithm hardware acceleration engine.

Key features

- **Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - Run up to 64MHz
- **Encrypted memory**
  - Up to 128KByte embedded Flash memory, 8KByte embedded Data Flash memory, supports encrypted storage, supports hardware ECC verification, data 100,000 cycling and 10 years of data retention
  - SRAM of 16KB, STOP modes can be configured as retention, supporting hardware parity
- **Low-power management**
  - Run mode: all peripherals configurable
  - SLEEP mode: all peripherals configurable
  - STOP mode: TIM6, IWDG, RTC configurable operation, 16KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode: support NRST, PA0_WKUP0, PA2_WKUP1 wakeup
- **Clock**
  - HSE: 8MHz~16MHz external high-speed crystal
  - HSI: Internal high-speed RC OSC 8MHz
  - HSI_24MHz: Internal high-speed RC OSC 24MHz, available only as an ADC sample clock source option
  - LSI: Internal low-speed RC OSC 32KHz
  - Built-in high-speed PLL
  - MCO: Support 1-way clock output, configurable SYSCLK, HSI, HSE, LSI, and PLL clock output that can be divided.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Supports programmable low voltage detection reset(LVR)
  - Support watchdog reset, Support software reset
- **Communication interface**
  - 5xUART, Supports asynchronous mode, multiprocessor communication mode, single-wire half-duplex mode
  - 3xSPI, up to 16 MHz

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- 2xI2C, up to 1 MHz, configurable master/slave mode
- 1xCAN 2.0A/B bus interface, up to 1Mbps

- **1xDMA, 5-channel, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **Segment LCD display driver, support up to 44 segments (4x11) or 26 segments (2x13)**
- **Analog interface**
  - 1x12bit 1Msps ADC , up to 8 external single-ended input channels
  - 4xCOMP (Comparator has an internal independent 6bit DAC)
  - 1x 12bit DAC, sampling rate 1Msps
  - Internal 1.2V independent reference voltage reference source
  - Internal integrated low voltage check unit
- **Up to 29 GPIOs**
- **1xBeeper, 16mA output drive capacity**
- **Timer counter**
  - 1x16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, each timer support 5 independent channels. 4 channels support 8 complementary PWM outputs
  - 4x16-bit general purpose timer counters, 4 independent channels, supports input capture/output compare/PWM output
  - 1x16-bit basic timer counters, supports STOP wake-up low-power mode.
  - 1x24-bit SysTick
  - 1x14-bit Window Watchdog (WWDG)
  - 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Security features**
  - CRC16 calculation
  - Flash storage encryption, multi-user partition management (MMU)
  - Support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 2.0V~5.5V
  - Operating Temperature Range:
    - ✧ Temperature coefficient 8, -40 ℃~125 ℃, certified by AEC-Q100-G1
    - ✧ Temperature coefficient 7, -40 ℃~105 ℃, certified by AEC-Q100-G2

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- **Package**
  - QFN32(5mm x5mm, 0.5mm pitch)

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1 Ordering Information

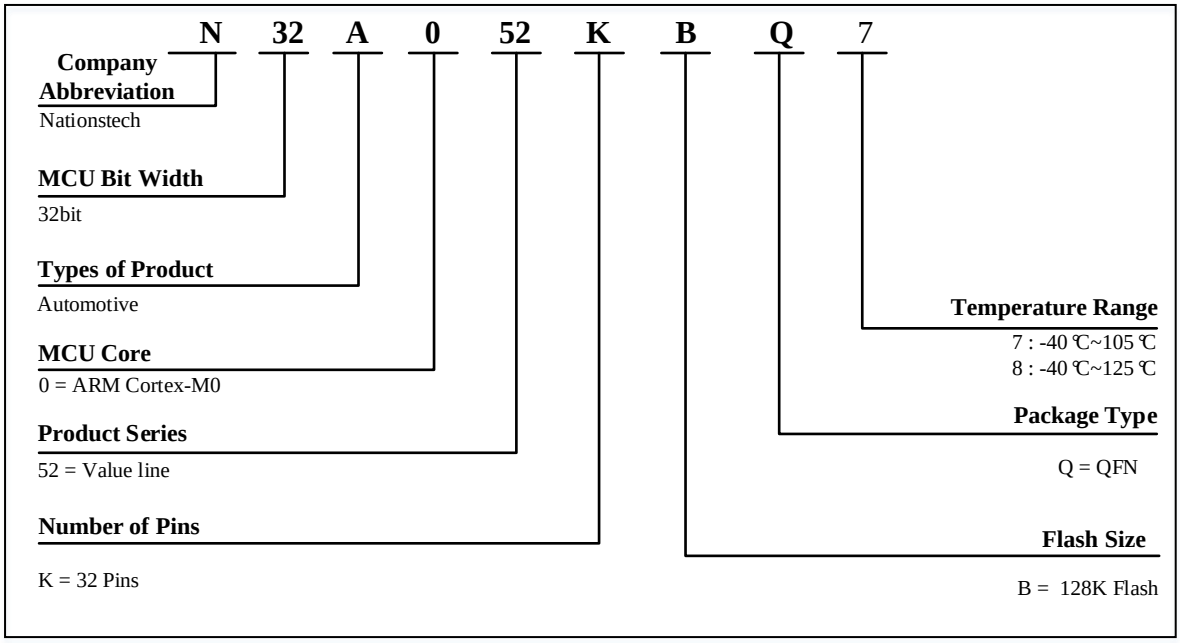

Table 1-1 N32A052 series ordering code information

Order Code(1)	Package	Package Size	Packaging(2)	SPQ(3)	temperature range
N32A052KBQ8	QFN32	5*5mm	Tray	490	-40℃~125℃
			Reel	2500	
N32A052KBQ7	QFN32	5*5mm	Tray	490	-40℃~105℃
			Reel	2500	

1. For the latest detailed ordering information, please refer to the selection manual.
2. This packaging is the basic packaging. If you have any other requirements, please contact Nsing Technology
3. Minimum packaging quantity

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2 Product Model Resource Configuration

Table 2-1 N32A052 series resource configuration

Part Number		N32A052KBQ7	N32A052KBQ8
Flash（KB）		128	128
DATA flash(KB)		8	8
SRAM（KB）		16	16
CPU frequency		ARM Cortex-M0 @64MHz	ARM Cortex-M0 @64MHz
Working environment		2.0~5.5V/-40~105℃	2.0~5.5V/-40~125℃
Timer	Advanced	1	1
	General	4	4
	Basic	1	1
	Beeper	1	1
Communication interface	SPI	3	3
	I2C	2	2
	UART	5	5
	CAN	1	1
GPIO		29	29
DMA		1x 5 Channel	1x 5 Channel
RTC		1	1
12bit ADC		1x 8Channel	1x 8Channel
12bit DAC		1x 1Channel	1x 1Channel
COMP		3	3
Segment LCD		4*11/2*13	4*11/2*13
Algorithm support		CRC16	CRC16
Security protection		Read/write protection (RDP/WRP)	Read/write protection (RDP/WRP)
Package		QFN32(5*5mm, 0.5mm pitch)	QFN32(5*5mm, 0.5mm pitch)

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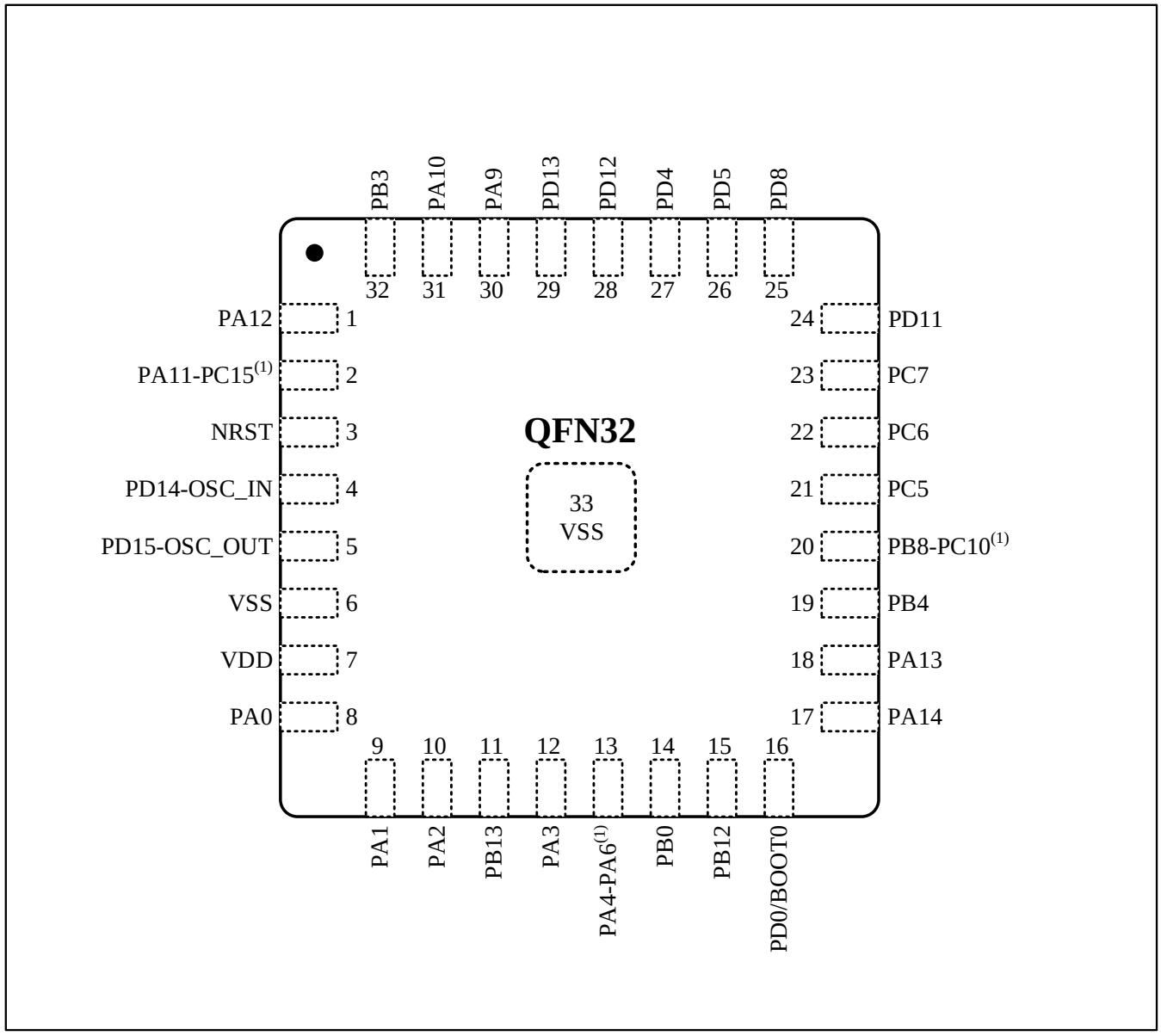
3 Package

3.1 QFN32

3.1.1 QFN32 pinouts



1. *pin-2, pin-13 and pin-20 are combination IOs, where pin-2 is a combination of PA11 and PC15, where pin-13 is a combination of PA4 and PA6, and where pin-20 is a combination of PB8 and PC10; Only one of the IOs can be used at the same time, and other IOs on the same pin must be configured in analogue mode, so as not to affect the IOs being used. IOs in use.*

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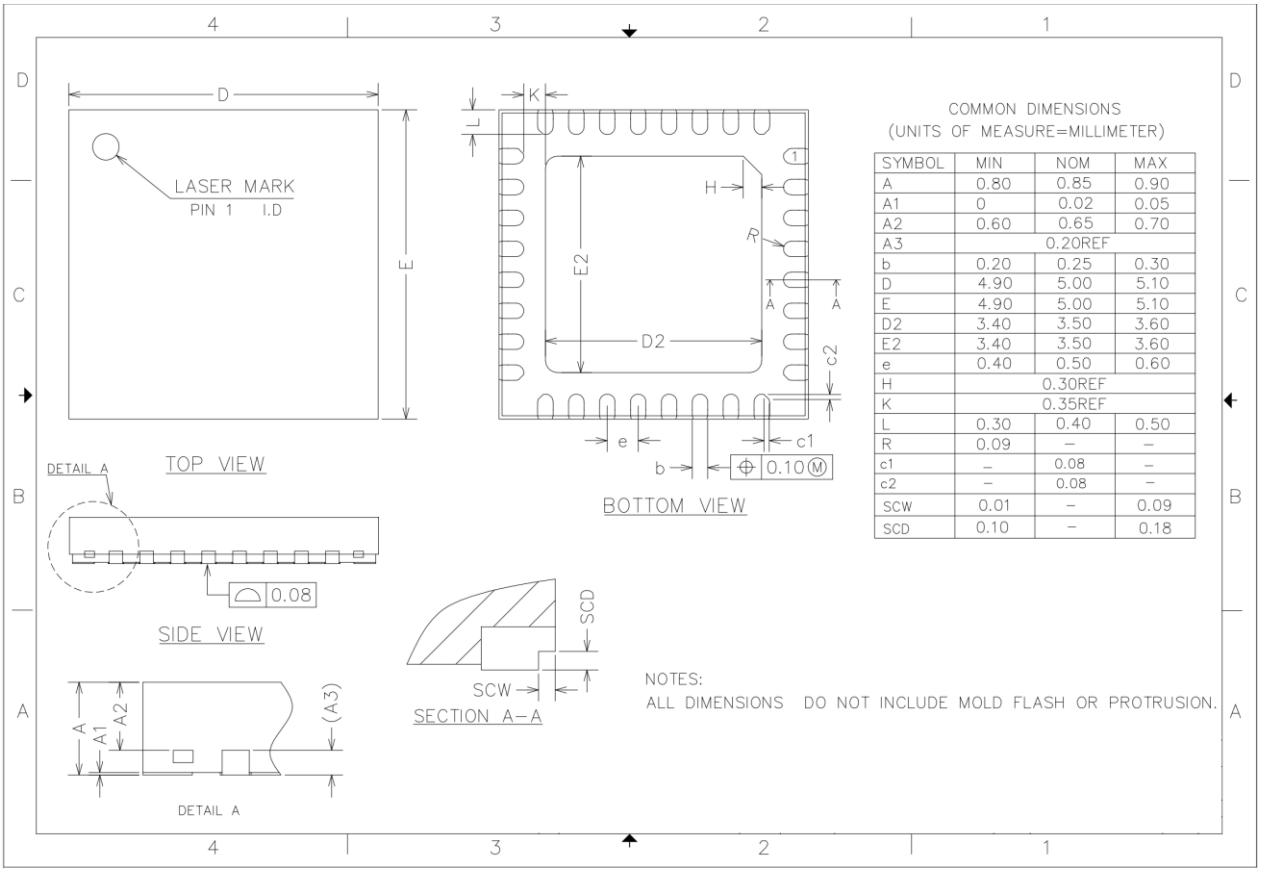
3.1.2 QFN32 (5x5mm) Package Size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e	0.40	0.50	0.60
H		0.30REF	
K		0.35REF	
L	0.30	0.40	0.50
R	0.09	–	–
c1	–	0.08	–
c2	–	0.08	–
SCW	0.01	–	0.09
SCD	0.10	–	0.18

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4 Version history

Date	Version	Modify
V1.0.0	2026.2.24	Initial version

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5 Notice

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