N32A052xx Datasheet

N32A052 series adopts a 32-bit ARM Cortex-M0 core, with a maximum operating frequency of 64MHz. It integrates up to 128KB of embedded encrypted Flash, 8KB of data Flash, 16KB of SRAM, and rich high-performance analog devices. It has a built-in 12 bit 1Msps ADC, 4 rail to rail comparators, 1 12 bit 1Msps DAC, up to 44 segments of Segment LCD driver, and multiple digital communication interfaces such as UART, I2C, SPI, CAN, etc.

Key features

- **Core**
  - A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
  - Run up to 64MHz
- **Encrypted memory**
  - Up to 128KByte embedded Flash memory, 8KByte embedded Data Flash memory, supports encrypted storage, supports hardware ECC verification, data 100,000 cycling and 10 years of data retention
  - SRAM of 16KB, STOP modes can be configured as retention, supporting hardware parity
- **Low-power management**
  - Run mode: all peripherals configurable
  - SLEEP mode: all peripherals configurable
  - STOP mode: TIM6, IWDG, RTC configurable operation, 16KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode: support NRST, PA0_WKUP0, PA2_WKUP1 wakeup
- **Clock**
  - HSE: 8MHz~16MHz external high-speed crystal
  - HSI: Internal high-speed RC OSC 8MHz
  - HSI_24MHz: Internal high-speed RC OSC 24MHz, available only as an ADC sample clock source option
  - LSI: Internal low-speed RC OSC 32KHz
  - Built-in high-speed PLL
  - MCO: Support 1-way clock output, configurable SYSCLK, HSI, HSE, LSI, and PLL clock output that can be divided.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Supports programmable low voltage detection reset(LVR)
  - Support watchdog reset, Support software reset
- **Communication interface**
  - 5xUART, Supports asynchronous mode, multiprocessor communication mode, single-wire half-duplex mode
  - 3xSPI, up to 16 MHz
  - 2xI2C, up to 1 MHz, configurable master/slave mode
  - 1xCAN 2.0A/B bus interface, up to 1Mbps
- **1xDMA, 5-channel, channel source address and destination address can be arbitrarily configurable**

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- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **Segment LCD display driver, support up to 44 segments (4x11) or 26 segments (2x13)**
- **Analog interface**
  - 1x12bit 1Msps ADC , up to 8 external single-ended input channels
  - 4xCOMP (Comparator has an internal independent 6bit DAC)
  - 1x 12bit DAC, sampling rate 1Msps
  - Internal 1.2V independent reference voltage reference source
  - Internal integrated low voltage check unit
- **Up to 29 GPIOs**
- **1xBeeper, 16mA output drive capacity**
- **Timer counter**
  - 1x16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, each timer support 5 independent channels. 4 channels support 8 complementary PWM outputs
  - 4x16-bit general purpose timer counters, 4 independent channels, supports input capture/output compare/PWM output
  - 1x16-bit basic timer counters, supports STOP wake-up low-power mode.
  - 1x24-bit SysTick
  - 1x14-bit Window Watchdog (WWDG)
  - 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Security features**
  - CRC16 calculation
  - Flash storage encryption, multi-user partition management (MMU)
  - Support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 2.0V~5.5V
  - Operating Temperature Range:
    - Temperature coefficient 8, -40 ℃~125 ℃, certified by AEC-Q100-G1
    - Temperature coefficient 7, -40 ℃~105 ℃, certified by AEC-Q100-G2
- **Package**
  - QFN32(5mm x5mm, 0.5mm pitch)

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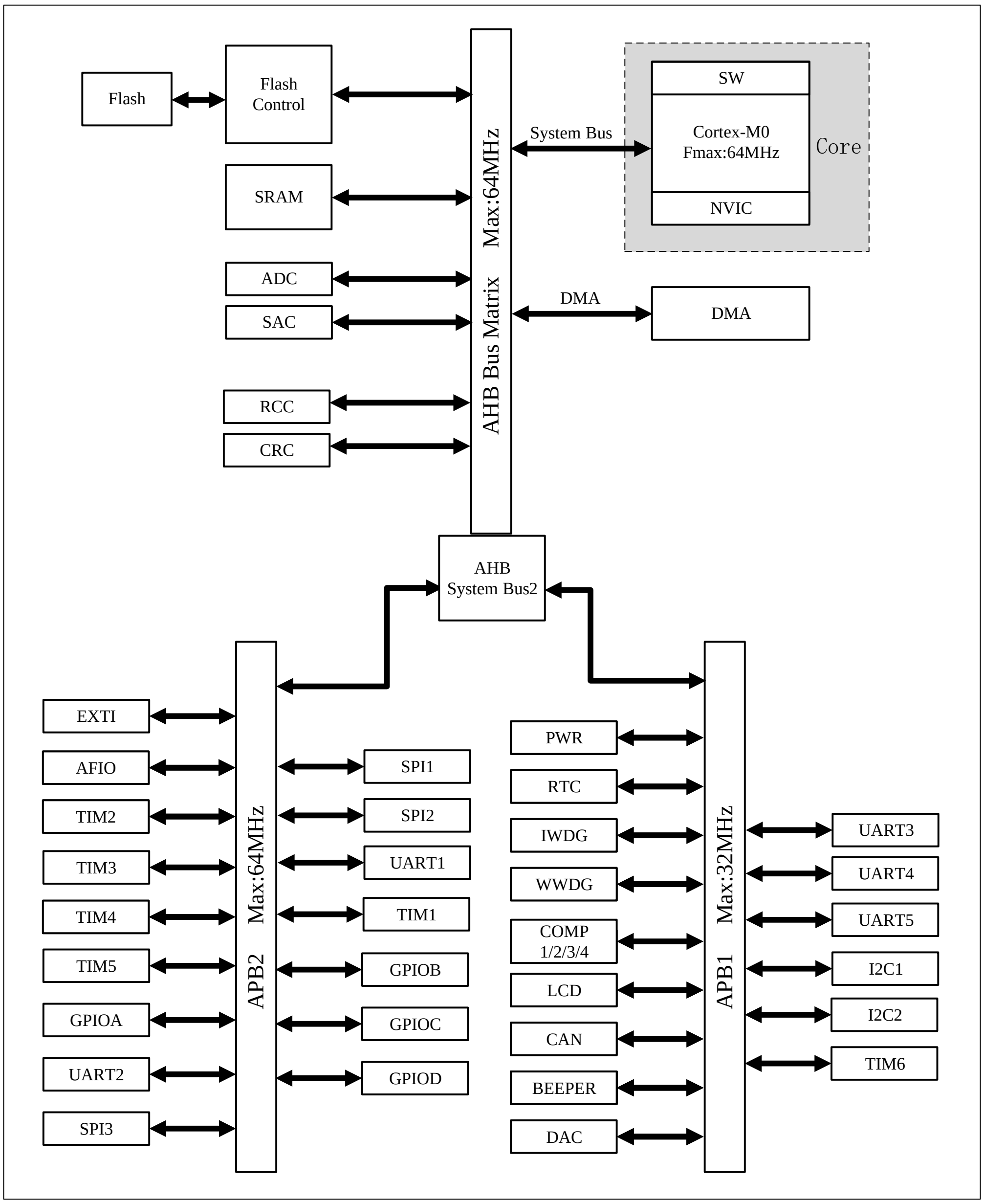
1 Product introduction

N32A052 family of microcontrollers features an ARM Cortex®-M0 core. Maximum operating main frequency 64MHz, integrated up to128KB of in-chip encrypted storage Flash, 8KB DataFlash, maximum 16KB of embedded SRAM. It has an internal high speed AHB bus, two low speed peripherals clock bus APB and bus matrix. It supports up to 29 reusable I/ Os and provides a rich array of high performance analog interfaces, including 1x 12-bit 1Msps ADC, up to 8 external input channels, and 4 high-speed comparator, 1x 12-bit 1Msps DAC, integrated Segment LCD driver with up to 44 segments. At the same time, it provides a variety of digital communication interfaces, including 5x UART, 2x I2C, 3x SPI, 1x CAN2.0A/B communication interface.

N32A052 series products can work stably in the temperature range of -40 ℃ to +125 ℃, supply voltage from 2.0V to 5.5V, provide a variety of power modes for users to choose, meet the requirements of low-power applications.

Figure 1-1 shows the bus block diagram of this series of products.

Figure 1-1 N32A052 Block Diagram



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1.1 List of devices

Table 1-1 N32A052 Series devices features and peripheral list

Part Number		N32A052KBQ7	N32A052KBQ8
Flash（KB）		128	128
DATA flash(KB)		8	8
SRAM（KB）		16	16
CPU frequency		ARM Cortex-M0 @64MHz	ARM Cortex-M0 @64MHz
Working environment		2.0~5.5V/-40~105℃	2.0~5.5V/-40~125℃
Timer	Advanced	1	1
	General	4	4
	Basic	1	1
	Beeper	1	1
Communication interface	SPI	3	3
	I2C	2	2
	UART	5	5
	CAN	1	1
GPIO		29	29
DMA		1x 5 Channel	1x 5 Channel
RTC		1	1
12bit ADC		1x 8Channel	1x 8Channel
12bit DAC		1x 1Channel	1x 1Channel
COMP		3	3
Segment LCD		4*11/2*13	4*11/2*13
Algorithm support		CRC16	CRC16
Security protection		Read/write protection (RDP/WRP)	Read/write protection (RDP/WRP)
Package		QFN32(5*5mm, 0.5mm pitch)	QFN32(5*5mm, 0.5mm pitch)

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2 Functional description

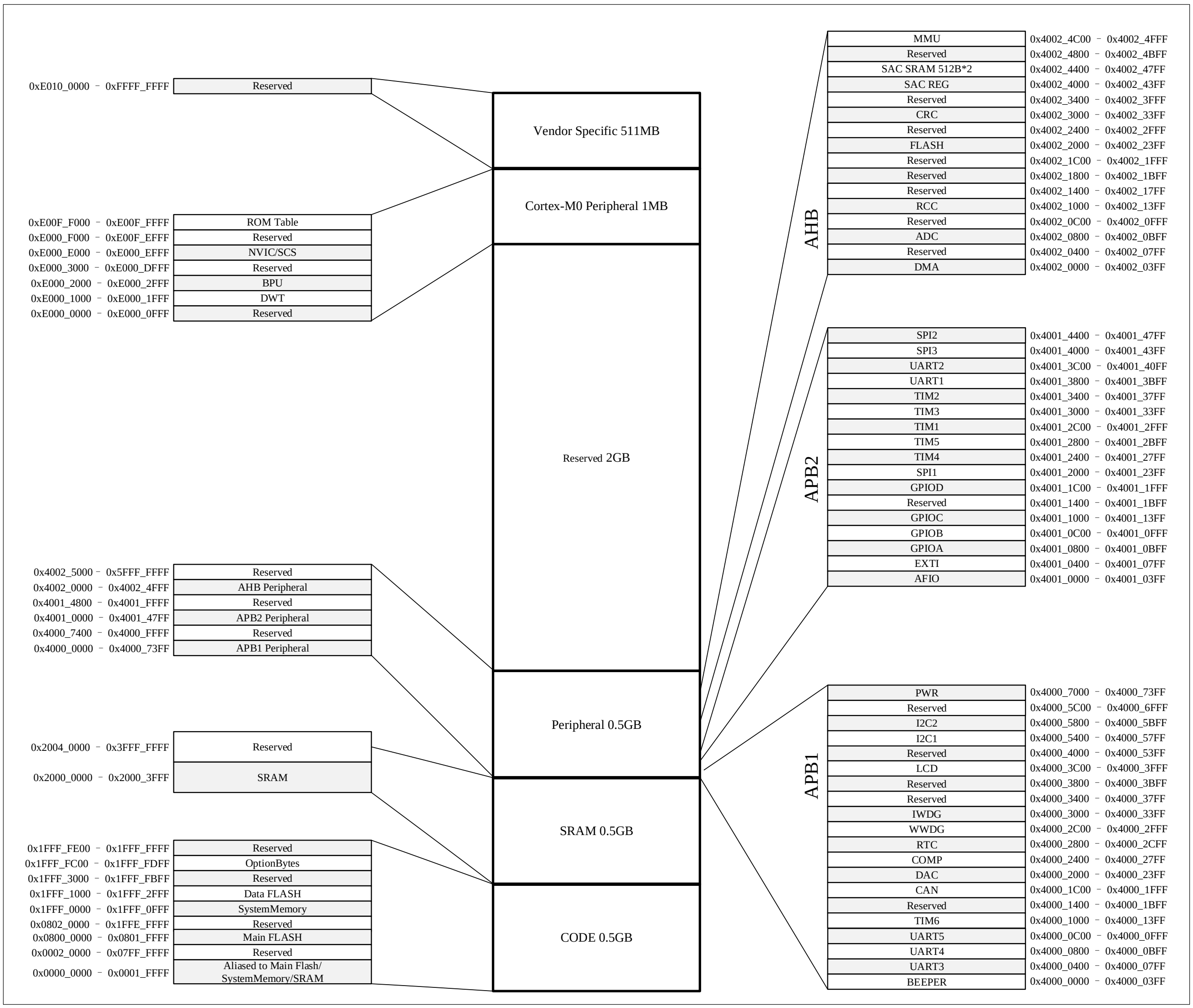
2.1 Processor core

N32A052 series integrates the latest generation of embedded ARM Cortex®-M0 processor

2.2 Storage

N32A052 series devices include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory address map



2.2.1 Embedded FLASH memory

Integrated up to 128K bytes embedded encryption FLASH, used to store programs and data, page size of 512byte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Integrated 8K bytes embedded encryption Data FLASH, used to store data, page size of 512byte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program

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execution operation).

2.2.2 Embedded SRAM

Integrated up to 16K bytes SRAM. In STOP mode, SRAM can hold data.

2.2.3 Nested vectored interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is tightly connected to the interface of the kernel, which can realize low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 32 maskable interrupt channels (not including 16 Cortex®-M0 interrupt lines)
- 4 programmable priority levels (using 2-bit interrupt priority levels)
- Low-latency exception and interrupt handling
- Power management control
- Realization of system control register

The module provides flexible interrupt management functions with minimal interrupt delay

2.3 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 21 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its triggering event (rising edge or falling edge or bilateral edge) and can be individually shielded. There is a suspended register that maintains the state of all interrupt requests. The corresponding bit of the suspend register can be cleared by writing '1'.

2.4 Clock system

The device provides a variety of clocks for users to choose from, including internal high speed RC oscillator HSI (8MHz), internal low speed clock LSI (32KHz), external high speed clock HSE (8MHz~16MHz), PLL.

During reset, the internal HSI clock is set as the default CPU clock, and then the user can choose the external HSE clock with failure monitoring function. When HSE failure is detected, it will be isolated, the system will automatically switch to HSI, and if interrupts are enabled, the software can receive the corresponding interrupt. Also, security interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

Multiple prescaler are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. AHB has a maximum frequency of 64MHz, APB2 has a maximum frequency of 64MHz and APB1 has a maximum frequency of 32MHz.

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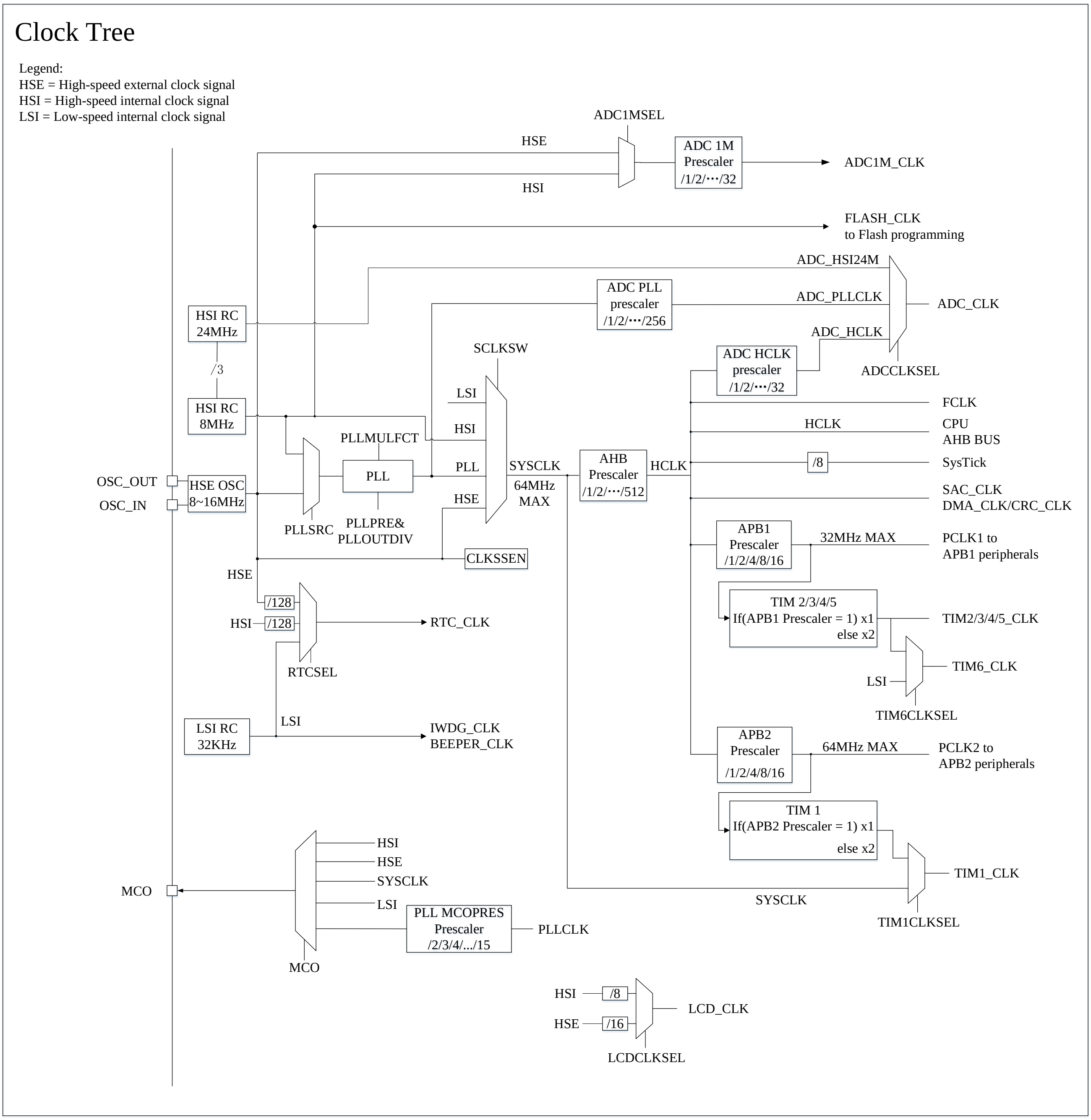
Figure 2-2 Clock Tree



2.5 Boot mode

At BOOT time, the BOOT mode after reset can be selected with the BOOT0 pin and option byte BOOT configuration (USER2).

- Boot from program FLASH Memory
- Boot from System Memory
- Boot from internal SRAM

The bootloader is stored in the system memory and can be programmed into the FLASH Memory/SRAM area through UART1. For specific instructions on using BOOT startup, please refer to the "CN-UG_N32A052 Series BOOT User Guide.pdf ".

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2.6 Boot Swap

This function can be used to update the secondary boot, to avoid directly updating the secondary boot because of temporary power failure or other reasons leading to the failure of updating the code of the secondary boot area, and the loss of the original secondary boot code leads to the program can not work properly, boot swap function can effectively avoid this problem.

2.7 Power supply scheme

- VDD area: The voltage input range is 2.0V~5.5V, which mainly provides power input for Main Regulator, IO and clock reset system.
- VDDD area: The voltage regulator supplies power for the CPU, AHB, APB, SRAM, FLASH and most digital peripheral interfaces.

PWR is the power control module of the entire device, its main function is to control N32A052 to enter different power modes and can be awakened by other events or interrupts. N32A052 supports RUN, SLEEP, STOP and PD modes.

2.8 Programmable voltage detector

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 2.0V.

When V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device remains in the reset state.

The device has a programmable voltage detector (PVD), which monitors the V_{DD} power supply and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, it will generate an interrupt. The PVD function is turned on by software.

The device has a programmable voltage detector (LVR), which monitors the V_{DD} power supply and compares it with the threshold V_{LVR}. When V_{DD} is lower or higher than the threshold V_{LVR}, it will generate Reset. The LVR function is turned on by software.

Table 4-6 is the value reference of $V_{POR}/_{PDR}$ and $V_{PVD/LVR}$.

2.9 Low power mode

N32A052 is in RUN mode after system reset or power-on reset. When the CPU does not need to run, you can choose to enter a low power mode to save power.

N32A052 has the following four low power modes:

- SLEEP mode (the core is stopped, all peripherals including Cortex®-M0 core peripherals (such as NVIC, SysTick) are still running)
- STOP mode (most of the clocks are turned off, the voltage regulator is still running in low power mode)
- PD mode (V_{DDD} power down mode, V_{DD} retention, 2 WAKEUP IO and NRST can wake up)
- In addition, the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses

2.10 DMA

The device integrates a flexible general-purpose DMA controller that supports 5 DMA channels to manage data transfers from memory to memory, peripherals to memory, and memory to peripherals.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The

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transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, UART, TIMx (Advanced/General/Basic Timer), DAC, ADC.

2.11 Real time clock (RTC)

The RTC is a set of continuously running counters with a built-in calendar clock module that provides perpetual calendar functionality, as well as an alarm interrupt and periodic interrupt (minimum 2 clock cycles).

The RTC will not be reset by a system reset, nor will it be reset when woken up from STOP mode.

The RTC's drive clock can be selected from any of the clock sources: an internal low-power 32KHz RC oscillator, a high-speed internal clock divided by 128, or a high-speed external clock divided by 128. The RTC drive clock can be selected from an internal low-power 32KHz RC oscillator, a high-speed internal clock divided by 128, or a high-speed external clock divided by 128.

To compensate for clock deviations, the RTC clock can be calibrated by outputting a 256 Hz signal.The RTC has a 22-bit prescaler for the time base clock, which generates a 1-second long time reference. Additionally the RTC can be used to trigger a wake-up in a low-power state.

2.12 Timer and watch dog

Up to 1 advanced control timers, 4 general-purpose timers and 1 basic timers, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer, basic timer and low power timer:

Table 2-1 Timer function comparison

Timer	Counter resolution	Counter type	Prescaler	Capture/Compare channel	Complementary output
TIM1	16-bit	Up Down Up/Down	Any integer between 1~65536	4/5	support
TIM2 ~ TIM5	16-bit	Up Down Up/Down	Any integer between 1~65536	4	Unsupported
TIM6	16-bit	Up	Any integer between 1~65536	0	Unsupported

2.12.1 Advanced-control timers (TIM1)

The advanced control timers (TIM1 and TIM8) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and brake function. Suitable for motor control.

The main functions of advanced timers include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 5 channels
- 4 capture/compare channels, the working modes are PWM output, Ouput compare, One-pulse mode output, Input capture

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- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with adjustable dead-time
  - For TIM1, channel 1,2,3,4 support this feature
- TIM1_CC5 is used for COMP blanking
- Supports PWM-triggered ADC sampling
- Timer can be controlled by external signal
- Repeat counter that allows the timer register to be updated after a specified number of counter cycles

2.12.2 General-purpose timer (TIMx)

The general-purpose timers (TIM2/TIM3/TIM4/TIM5) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.
The main functions of advanced timers include:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIMx up to 4 channels
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Supports incremental (quadrature) encoder and Hall sensor circuits for positioning
- TIM2 support for internal capture HSE, HSI_8M, LSI
- Input channels support digital filtering

2.12.3 Basic timer -TIM6

The basic timer contains a 16-bit counter.

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- The events that generate the interrupt/DMA are as follows:
  - Update event
- Supports STOP mode wake-up: when the clock source is configured as LSI, STOP mode can be woken up by updating the interrupt (linked to EXTI20)

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2.12.4 Systick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard decrement counter.

It has the following characteristics:

- 24 bit decrement counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.12.5 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit decrepit counter and an 3-bit predivider. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the decline counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 14-bit decrement counter value (in the control register) is flushed before the decrement counter reaches the window register value, then an MCU reset will also occur. This indicates that the decrement counter needs to be refreshed in a finite time window.

Main features:

- WWDG is driven by the clock generated after the APB1 clock is divided.
- Programmable free-running decrement counter.
- Conditional reset:
  - When the decrement counter is less than 0x40, a reset occurs (if the watchdog is started);
  - A reset occurs when the decrement counter is reloaded outside the window (if the watchdog is started);
- If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the decrement counter equals 0x40, which can be used to reload the counter to avoid WWDG reset.

2.13 I2C bus interface (I2C)

The device integrates up to 2 independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus (SMBus), and Power Management Bus (PMBus).

The functions of the I2C interface are described as follows:

- This module can be used as master device or slave device;
- I2C master device function:
  - Generate a clock;
  - Generate start and stop signals;

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- Function of I2C slave device
  - Programmable address detection;
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
  - Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and broadcast calls;
- Support different communication speeds;
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz);
  - Fast + (up to 1MHz);
- Status flags:
  - Transmitter/receiver mode flag;
  - Byte transmit complete flag;
  - I2C bus busy flag;
- Error flags:
  - Arbitration is missing in Master Mode.
  - Acknowledge (ACK) error after address/data transfer;
  - Error start or stop condition detected
  - Overrun or underrun when disable extend clock function;
- Supported interrupt vectors: event interrupts and error interrupts
- Optional extend clock function
- Supports digital and analog filtering
- Generation or verification of configurable PEC(Packet error detection)
  - In transmit mode, the PEC value can be transmitted as the last byte
  - PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25 ms clock low
  - 10 ms accumulates low clock extension time of master device
  - 25 ms accumulates low clock extension time of slave device
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
- Compatible with the PMBus

2.14 Universal asynchronous transceiver (UART)

N32A052 series products integrate up to 5 universal asynchronous transceivers (UART1 / UART2 / UART3 / UART4 / UART5).

UART interface sends and receives at configurable baud rates and also supports continuous communication via DMA. UART supports multiprocessor communication, LIN mode, single-wire half-duplex communication, and IrDA SIR ENDEC functions.

Main features of UART are as follows:

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- Full duplex, asynchronous communication
- Supports single-wire half-duplex communication
- Baud rate is configurable, up to 4Mbit/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- Hardware generated parity bit and parity bit checking
- DMA sending and receiving
- Multiprocessor communication: if the address does not match, it enters silent mode, which can be awakened by idle bus detection or address identification.
- Serial Infrared Protocol (IrDA SIR) encoding and decoding, and provides two modes of operation: normal and low power consumption.
- supports LIN mode
- Multiple error detection: data overflow error, frame error, noise error, check error.
- Multiple interrupt requests: send data register empty, send complete, data received, data overflow, bus idle, check error, LIN mode break frame detection, and noise flag/overflow error/frame error in multi-buffer communication.

Mode configuration:

UART modes	UART1	UART2	UART3	UART4	UART5
Asynchronous mode	support	support	support	support	support
Multiprocessor communication	support	support	support	support	support
Half duplex (single wire mode)	support	support	support	support	support
IrDA	support	support	support	support	support
LIN	support	support	support	support	support

2.15 Serial peripheral interface (SPI)

3x SPI interfaces. SPI allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCLK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-wire simplex synchronous transmission using a bidirectional data wire.

The main functions of SPI interfaces are as follows:

- 3-wire full-duplex synchronous transmission;
- two-wire simplex synchronous transmission with or without a third bidirectional data wire;
- 8 or 16 bit transmission frame format selection;
- Master or slave operations;
- Support multi-master mode;
- 8 master mode baud rate prescaling factors (up to $f_{PCLK}/2$);
- Slave mode frequency (max. $f_{PCLK}/2$);
- Fast communication between master mode and slave mode;
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes;
- Programmable clock polarity and phase;

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- Programmable data order, MSB before or LSB before;
- Dedicated send and receive flags that trigger interrupts;
- SPI bus busy flag;
- Hardware CRC for reliable communication;
  - In send mode, the CRC value can be sent as the last byte;
  - In full-duplex mode, CRC is automatically performed on the last byte received.
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum interface speed: 16Mbps

2.16 Controller area network (CAN)

1x CAN bus interface compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode;
- Baud rate up to 1Mbps;
- Supports time-triggered communication
- Send
  - Three sending mailboxes
  - The priority of sent packets can be configured by software
  - Records the timestamp of the time when the SOF was sent
- Receive
  - Level 3 depth of 2 receiving FIFO
  - Variable filter group:
  - There are 14 filter groups
  - Identifier list
  - The FIFO overflow processing mode is configurable
  - Record the time stamp of the receipt of the SOF
- Time-triggered communication mode
  - Disable automatic retransmission mode
  - 16-bit free run timer
  - Timestamp can be sent in the last 2 bytes of data
- Management
  - Interrupt masking
  - The mailbox occupies a separate address space to improve software efficiency

2.17 General purpose input/output (GPIO)

Up to 29 GPIO, divided into 4 groups (GPIOA/GPIOB/GPIOC/ GPIOF), GPIOA have 12pins, GPIOB have 6 pins, GPIOC have 5 pins, GPIOD has 9 pins. Each GPIO pin can be configured by software as output (push-pull or open

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drain), input (with or without pull-up or pull-down) or alternate peripheral function ports (output/input), most GPIO pins are shared with digital or analog reuse peripherals, some IO pins are also reused with clock pins. Except for ports with analog input function, all GPIO pins have the ability to pass through a large current.

GPIO ports have the following characteristics:

- Each GPIO port can be individually configured into multiple modes by software
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Open drain output and pull-up/pull-down can be configured
  - Push-pull output and pull-up/pull-down can be configured
  - Push-pull alternate function and pull-up/pull-down can be configured
  - Open-drain alternate function and pull-up/pull-down can be configured
- Individual bit set or bit clear function
- All IO supports external interrupt function
- All IO supports low power mode wake-up, rising or falling edge configurable
  - 16 EXTIs can be used to wake up from SLEEP or STOP mode, and all I/Os can be reused as EXTIs
  - NRST/PA0/ PA2 three wake-up IO can be used for PD mode wake-up, the maximum I/O filter time is 1us
- Support software remapping I/O alternate function
- Support GPIO lock mechanism, reset the lock state to clear

Each I/O port bit can be programmed arbitrarily, but I/O port registers must be accessed as 32-bit words (16-bit half-word or 8-bit byte access is not allowed). The following figure shows the basic structure of an I/O port.

2.18 Analog/digital converter (ADC)

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. There are a total of 10 channels that can measure 8 external and 2 internal signal sources. The A/D conversion channels of each channel can be executed in single, continuous, and sweep modes.The ADC conversion values are stored (left-aligned/right-aligned) in 16-bit data registers. An analog watchdog can be used to detect if the input voltage is within the user-defined high/low thresholds and the ADC's input clock has a maximum frequency of 24 MHz.

The main features of the ADC are described below:

- Supports 1 ADC, supports single-ended inputs, and can measure up to 8 external and 2 internal signal sources
- Supports 12-bit resolution and a maximum sampling rate of 1MSPS
- ADC clock source is divided into working clock source and timing clock source
  - HSI, PLL, AHB as ADC_CLK working clock source, up to 24M
  - HSI or HSE as ADC_1MCLK timing clock source, used for internal timing function, frequency must be configured to 1MHz
- Timer-triggered sampling support
- Interrupt can be triggered when conversion is completed or analog watchdog event.
- Conversion mode
  - Single conversion
  - Continuous conversion

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◆ Scan mode

- Scan mode supports up to any 5 channels, each with a separate result data register.
- Sampling intervals can be programmed uniformly for all channels.
- Can be externally triggered for rule-based conversion.
- The ADC operates with voltages between 2.4V and 5.5V.
- ADC supports conversion between 0 and V_{DD}.
- ADC supports DMA operation

2.19 Digital/Analog converter (DAC)

DAC is a digital/analog converter, mainly digital input, voltage output.DAC data has two modes, 8bit or 12bit, and supports DMA function. When the DAC is configured in 12bit mode, the DAC data can be left-aligned or right-aligned; when the DAC is configured in 8bit mode, the DAC data can be right-aligned.There are 1 DAC output channels with independent converters.AVREFP(PB2) is input through the pins as the DAC reference voltage, which makes the converted data of the DAC more accurate.

- 1 independent DAC converter corresponding to 1 output channel
- Monotonic output
- Supports 8-bit or 12-bit output, with right-aligned and left-aligned data in 12-bit mode.
- Synchronized update
- Support DMA function
- Noise wave and triangle waveform generation
- Input reference voltage AVREFP
- External event triggered conversion

2.20 Analog comparator (COMP)

Embedded with 4 comparators, it can be used as a stand-alone device (all ports of comparators lead to I/O) or combined with timers, which can be used in motor control applications to form cycle-by-cycle current control in conjunction with the PWM output from timers.

The main functions of the comparator are as follows:

- Shares the internal reference inputs of two independent 6bit DACs
- Supports filtered clock, filtered reset
- Configurable high and low output polarity.
- Hysteresis configuration configurable none, low, medium, high
- Comparison results can be output to I/O ports or trigger timers for capturing events, OCREF_CLR events, braking events, generating interrupts
- Input channels can be re-selected for I/O ports, dedicated 6bit DAC, channel outputs for general purpose 12bit DACs
- Read-only or read-write configurable, requires reset to unlock in case of locking.
- Blanking support, Blanking source can be configured to generate Blanking.
- COMP1/COMP2, COMP3/COMP4 can form a window comparator.
- Wake up the system from Sleep mode by generating an interrupt.
- Configurable filter window size

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- Configurable filter threshold size

2.21 Segment LCD Driver (Segment LCD)

The LCD controller is suitable for monochrome passive segmented liquid crystal displays (Segment LCD) with up to 4 common terminals (COM) and 11 segment terminals (SEG), the exact number of terminals depends on the pinout of the different packages, which can be referred to in the datasheet.The Segment LCD consists of a number of segments, which can be either illuminated or extinguished. Each segment contains a layer of liquid crystal molecules aligned between two electrodes. When a voltage above the threshold voltage is applied to the liquid crystal, the corresponding segment is visible. To avoid electrophoretic effects in the liquid crystal, the zone voltage must be AC.

Key Features:

- Frame rate is configurable.
- Duty Cycle Configurable: Supports static, 1/2, 1/3, 1/4 and 1/8 duty cycles.
- Voltage bias is configurable: supports static, 1/2, 1/3, and 1/4 bias.
- Double buffering mechanism allows the user to update the data in the display memory registers (pixel active/inactive information) at any time.
- LCD clock source selectable: HSE/16 or HSI_8M/8.
- Two contrast control methods: Adjust the dead time of up to 7 phase cycles between frames; Adjust the VLCD to vary in the range of VLCDmin~VLCDmax (only when using the internal boost converter).
- Built-in resistor network is used to generate LCD intermediate voltage, which can be configured via software to match capacitive loads on the LCD panel.
- Built-in voltage output buffer
- Built-in phase inversion to reduce electromagnetic interference (EMI) and power consumption.
- Supports blinking function: 1, 2, 3, 4, 8 or all pixels can be configured to blink at a specified frequency (0.5Hz, 1Hz, 2Hz or 4Hz)
- Pins used for SEG and COM functions should be configured as corresponding AFIOs.

2.22 Temperature Sensors (TS)

The temperature sensor produces a voltage that varies linearly with temperature over a conversion range of 2.4V <VDDA< 5.5V. The temperature sensor is internally connected to the input channel of ADC_IN15, which is used to convert the output of the temperature sensor to a digital value.

2.23 BEEPER

The BEEPER module supports complementary outputs that can generate periodic signals to drive an external passive buzzer. It is used to generate beeps or alarm audible sounds.

2.24 Cyclic redundancy check calculation unit (CRC)

Integrating the CRC16 function, the cyclic redundancy check (CRC) computation unit is based on a fixed generating polynomial to get the result of any CRC computation. In numerous applications, CRC-based techniques are used to verify the consistency of data transmission or storage.

The main properties of CRC are as follows:

- CRC16: supports polynomials $X^{16}+X^{15}+X^{2}+X^{0}$
- CRC16 calculation time: 1 AHB clock cycle (HCLK)
- Initial value of cyclic redundancy calculation is configurable

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- Supports DMA mode

2.25 Unique device serial number (UID)

The N32A052 series products have two built-in unique device serial numbers of different lengths, the 96-bit UID (Unique device ID) and the 128-bit UCID (Unique Customer ID), which are stored in the system configuration block of the flash memory, and the information they contain is written at the factory and is guaranteed to be unique to N32A052 series any one microcontroller in any case is unique, the user application or external devices can be read through the CPU or SWD interface, can not be modified.

UID is 96 bits, usually used as a serial number or as a password, when writing flash memory, this unique identifier is combined with software encryption and decryption algorithms to further improve the security of the code within the flash memory.

The UCID is 128 bits and complies with the National Technical Chip Serial Number Definition, which contains chip production and version related information.

2.26 Serial wire SWD debug port (SWD)

Embedded Arm SWD Interface.

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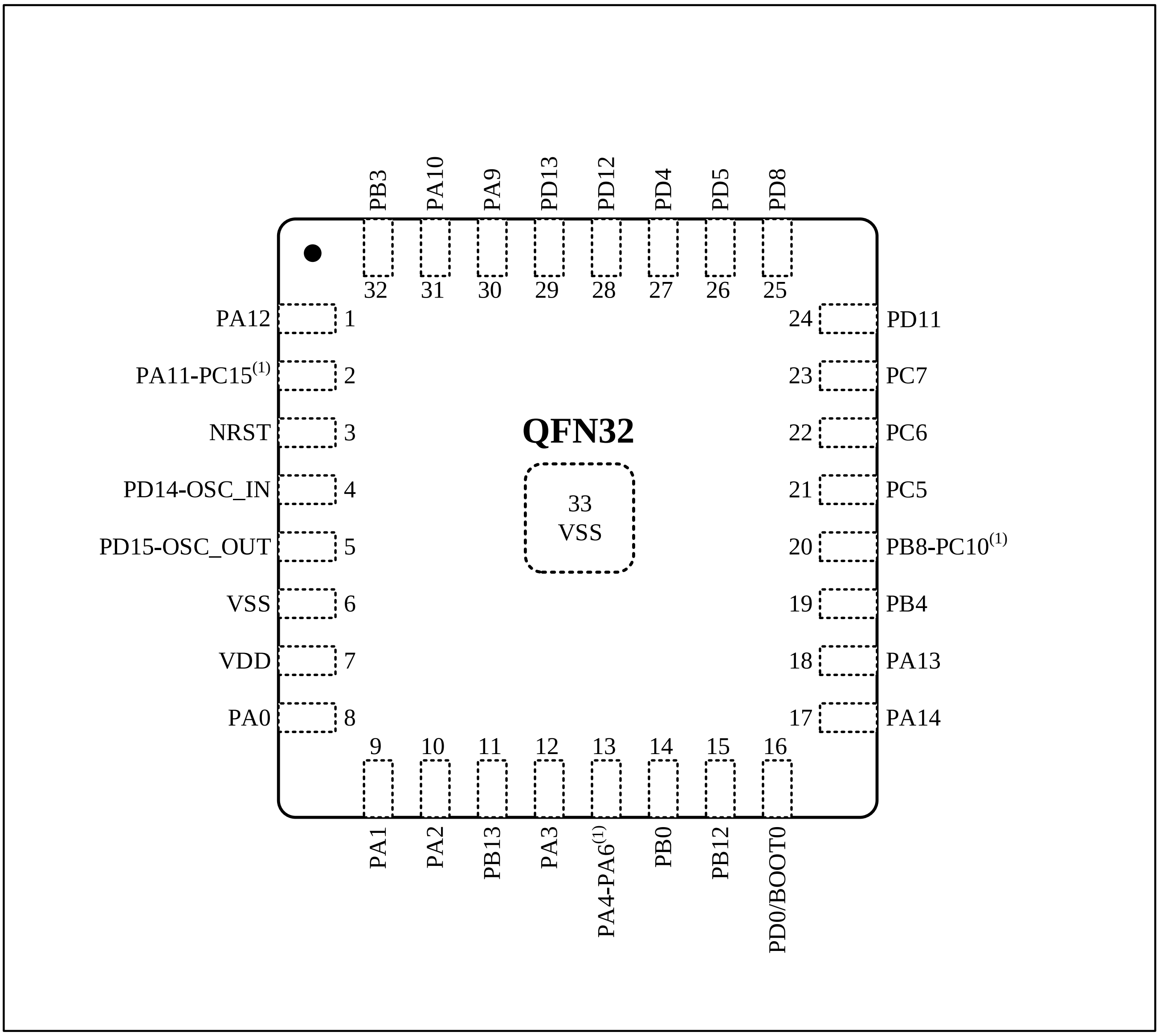
3 Pin descriptions

3.1 Pinouts

3.1.1 QFN32

Figure 3-1 N32A052 Series QFN32 pinouts



1. *pin-2, pin-13 and pin-20 are combination IOs, where pin-2 is a combination of PA11 and PC15, where pin-13 is a combination of PA4 and PA6, and where pin-20 is a combination of PB8 and PC10; Only one of the IOs can be used at the same time, and other IOs on the same pin must be configured in analogue mode, so as not to affect the IOs being used. IOs in use.*

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3.2 Pin definitions

For details of alternate functions for IO, please refer to the "Alternate function" section within the "GPIO and AFIO" chapter of the User Manual.

Table 3-1 Pin definitions

Package	Pin name (function after reset)	Type(1)	IO(2)	Fail-safe(4)	Alternate functions(3)	
QFN32					Digital	Analog
14	PB0	I/O	TC	N	LCD_SEG0 TIM2_CH1 EVENTOUT	ADC_IN8 COMP1_INM
15	PB12	I/O	TC	N	LCD_SEG5 TIM1_CH4N TIM2_CH3 SPI1_SCK SPI1_MISO SPI2_MISO SPI3_MISO UART2_TX EVENTOUT	ADC_IN13
16	PD0	I/O	TC	N	LCD_SEG6 TIM2_CH2 SPI1_NSS BOOT0	-
17	PA14	I/O	TC	N	LCD_SEG7 TIM1_ETR TIM1_CH4N TIM2_CH1 UART4_TX SWCLK	-
18	PA13	I/O	TC	N	LCD_SEG8 TIM1_CH4 TIM2_CH4 I2C2_SMBA UART4_RX SWDIO Beeper_OUT MCO	-
19	PB4	I/O	TC	N	LCD_SEG13 TIM5_CH4 TIM5_CH3 UART2_TX EVENTOUT COMP3_OUT	-

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20(5)	PB8	I/O	TC	N	LCD_SEG16 TIM4_CH4 TIM4_CH3 I2C1_SCL I2C2_SCL UART3_TX UART5_TX RTC_TAMP3 COMP1_OUT	-
20(5)	PC10	I/O	TC	N	LCD_SEG21 I2C2_SCL UART3_TX COMP4_OUT	-
21	PC5	I/O	TC	N	LCD_SEG23 TIM3_ETR I2C1_SCL I2C2_SCL SPI1_SCK SPI2_SCK SPI3_SCK COMP4_OUT	-
22	PC6	I/O	TC	N	LCD_SEG24 TIM3_CH1 I2C1_SCL I2C2_SCL I2C1_SDA I2C2_SDA SPI1_MOSI SPI2_MOSI SPI3_MOSI	-
23	PC7	I/O	TC	N	LCD_SEG25 TIM3_CH2 I2C1_SDA I2C2_SDA SPI1_MISO SPI2_MISO SPI3_MISO	-
24	PD11	I/O	TC	N	LCD_COM7 LCD_SEG32 TIM4_CH1 I2C1_SDA I2C2_SDA SPI2_MOSI UART1_RX UART4_RX	-
25	PD8	I/O	TC	N	LCD_COM4 LCD_SEG35 TIM1_CH3 UART5_TX CAN_RX	-

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26	PD5	I/O	TC	N	LCD_COM1 TIM1_CH1N TIM3_CH3 TIM3_CH4 SPI1_MISO UART4_TX UART5_RX EVENTOUT	COMP4_INP
27	PD4	I/O	TC	N	LCD_COM0 TIM1_CH1 TIM1_CH3 TIM1_CH4 I2C1_SMBA SPI1_MOSI UART4_RX EVENTOUT	COMP4_INM
28	PD12	I/O	TC	N	TIM1_CH4N TIM3_CH3 TIM3_CH4 I2C1_SCL I2C2_SCL SPI3_NSS	-
29	PD13	I/O	TC	N	TIM4_CH3 TIM5_CH3 TIM5_CH4 I2C1_SDA I2C2_SDA SPI3_MISO UART3_TX UART3_RX	-
30	PA9	I/O	TC	N	TIM1_CH1 TIM1_CH2 TIM1_CH3N SPI1_MISO SPI3_MOSI UART3_TX UART1_TX UART4_TX	COMP3_INM
31	PA10	I/O	TC	N	TIM1_CH4 TIM2_CH1 TIM4_CH1 TIM4_CH2 I2C1_SDA I2C2_SDA SPI1_MOSI UART1_RX UART4_RX COMP3_OUT	COMP3_INP

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1	PA12	I/O	TC	N	TIM1_ETR TIM2_CH3 TIM5_CH1 TIM5_CH2 I2C1_SCL I2C2_SCL SPI1_SCK CAN_RX EVENTOUT	COMP4_INP
2(5)	PA11	I/O	TC	N	TIM1_BKIN TIM1_CH3 TIM1_CH4N TIM2_CH2 CAN_TX EVENTOUT	COMP4_INM
32	PB3	I/O	TC	N	CAN_TX EVENTOUT MCO	ADC_IN14
2(5)	PC15	I/O	TC	N	-	-
3	NRST	I/O	RST	N	NRST	-
4	PD14-OSC_IN	I/O	TC	N	TIM2_CH4 TIM4_CH4 I2C1_SDA	OSC_IN
5	PD15-OSC_OUT	I/O	TC	N	I2C1_SCL	OSC_OUT
6	VSS	S	TC	-	-	VSS
7	VDD	S	TC	-	-	VDD
8	PA0	I/O	TC	N	TIM5_CH1 SPI3_MOSI RTC_TAMP2 WAKUP0	ADC_IN0
9	PA1	I/O	TC	N	TIM1_BKIN TIM5_CH2 SPI3_MISO RTC_REFCLKIN EVENTOUT	ADC_IN1
10	PA2	I/O	TC	N	TIM5_CH3 I2C1_SMBA UART1_TX WAKUP1	ADC_IN2 COMP1_INP COMP1_INM
11	PB13	I/O	TC	N	TIM1_CH1N I2C2_SMBA	DAC_OUT
12	PA3	I/O	TC	N	TIM5_CH4 I2C1_SDA UART1_RX CAN_RX	ADC_IN3 COMP1_INP COMP2_INM

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13(5)	PA4	I/O	TC	N	TIM1_CH1 TIM1_CH3N I2C1_SCL CAN_TX	ADC_IN4 COMP2_INM
13(5)	PA6	I/O	TC	N	TIM1_CH2 TIM1_CH2N UART2_TX EVENTOUT	ADC_IN6 COMP2_INP

1. *I = Input, O = Output, S = Power, HiZ = High Resistance*
2. *TC: Standard 5V I/O, RST: Bi-directional reset pin with embedded weak pull-up resistor.*
3. *This type of multiplexing function can be configured to other pins by software (if the corresponding package model has this pin), please refer to the Multiplexing I/O section and Debug Settings section of the N32A052 series User's Manual for more details.*
4. *Fail-safe refers to adding input high level on IO when there is no power input to the chip, there will be no input high level poured into the chip, which will lead to a certain voltage on the power supply and consume current.*
5. *Combined IO, only one of the IO functions can be used at the same time, and other IOs on the same pin must be configured in analogue mode so as not to affect the IO being used.*

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4 Electrical characteristics

4.1 Parameter conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions by testing performed on the production line with 100% of the product at an ambient temperature of T_A = 25 ℃.

Data stated in the notes below each table as having been obtained by characterization, design simulation and/or process characterization will not be tested on the production line; on the basis of characterization tests, minimum and maximum values are obtained by taking the average of the sample tests and adding or subtracting three times the standard distribution (mean ± 3∑).

4.1.2 Typical numerical values

Typical data is based on T_A = 25 ℃ and V_{DD} = 3.3V/5.0V (2.0V ≤ VDD ≤ 5.5V voltage range) unless otherwise noted. These data are for design guidance only and have not been tested.

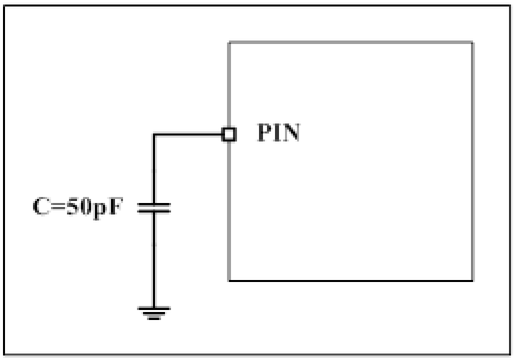
4.1.3 Typical curves

Typical curves are for design guidance only and are untested unless otherwise noted.

4.1.4 Loading capacitor

The load conditions when measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 pin loading conditions



4.1.5 Pin input voltage

The measurement method of the input voltage on the pin is shown in Figure 4-2.

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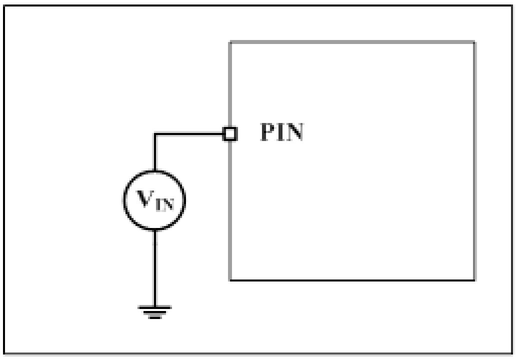
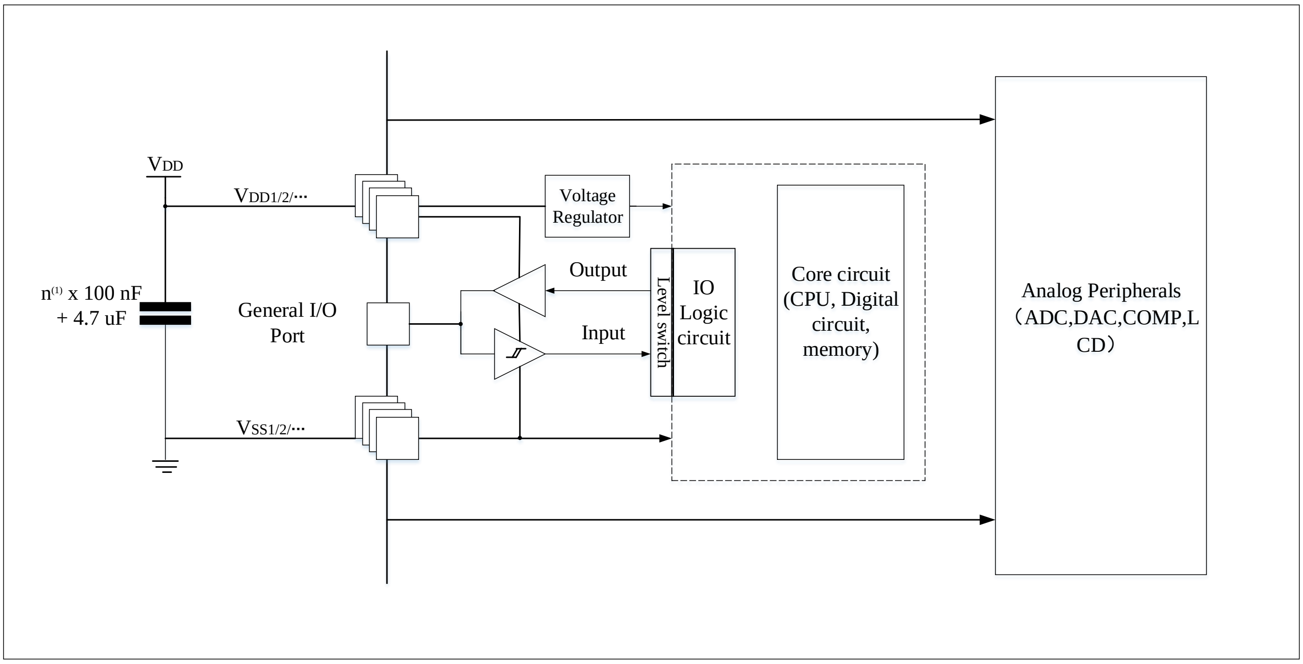
Figure 4-2 Pin input voltage



4.1.6 Power supply scheme

Figure 4-3 Power supply scheme



1. n is the number of VDDs.
2. When PB2 is multiplexed into the AVREFP function, an external 100nF+1uF capacitor is recommended.

Note: Refer to the hardware design guide for capacitor connections

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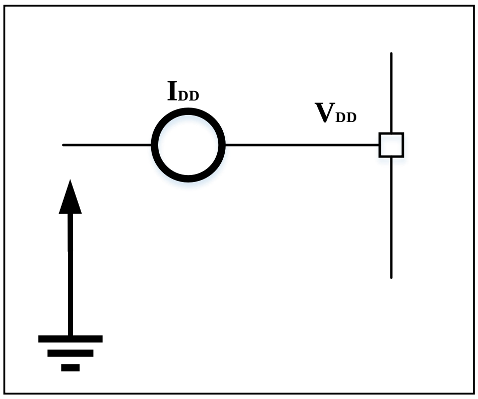
4.1.7 Current consumption measurement

Figure 4-4 Current consumption measurement



4.2 Absolute maximum ratings

Loads applied to the device in excess of the values given in the "Absolute Maximum Ratings" list (Table 4 1, Table 4 2, Table 4 3) may cause permanent damage to the device. The maximum loads that can be withstood are given here and do not imply that the functional operation of the device under these conditions is error-free. Prolonged operation of the device under maximum conditions will affect the reliability of the device.

Table 4-1 Voltage characteristics[1]

Symbol	Parameter	Min	Max	Unit
V_{DD} - V_{SS}	External mains supply voltage (V_{DD})[1]	-0.3	6.5	V
V_{IN}	Input voltage on arbitrary I/O and control pins	-0.3	Min (V_{DD} + 0.3, 6.5)	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply pins	0	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage difference between different ground pins	0	50	
$V_{ESD(HBM)}$	ESD Electrostatic Discharge Voltage (Human Body Model)	See section 4.3.11		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external permissible range power supply system.

Table 4-2 Current characteristics

Symbol	Parameter	Max	Unit
I_{VDD}	Total current through V_{DD} power line (supply current) [1]	200	mA
I_{VSS}	Total current through V_{SS} ground (outgoing current) [1]	200	
I_{IO}	Output potting current on arbitrary I/O and control pins	16	
	Output current on arbitrary I/O and control pins	-16	
$I_{INJ(PIN)}$[2][3]	Injection current at the NRST pin	0/-5	
	Injection current on other pins [4]	+/-5	
$\sum I_{INJ(PIN)}$[2]	Total injected current on all I/O and control pins [4]	+/-25	

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external permissible range of the power supply system.

2. The $I_{INJ\ (PIN)}$ must never exceed its limit, i.e., it is guaranteed that V_{IN} does not exceed its maximum value. If it is not possible to guarantee that V_{IN} does not exceed its maximum value, also ensure that $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. There is a forward injection current when $V_{IN}>V_{DD}$ and a reverse injection current when $V_{IN}<V_{SS}$.

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3. The reverse injection current interferes with the analog performance of the device. Refer to Section 4.3.19.

4. When several I/O ports have injected currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the immediate absolute values of the forward injection current and the reverse injection current.

Table 4-3 Temperature characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Junction temperature	+150	℃
	Junction temperature	+135	℃

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0.032	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0.032	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0.032	64	
V_{DD}	Standard operating voltage	-	2.0	5.5	V
	Operating voltage when using ADC, COMP section	-	2.4	5.5	V
	Operating voltage when using DAC section	-	2.97	5.5	V
	Operating voltage when using LCD section	-	4.5	5.5	V
T_A	Ambient Temperature	Suffix version 8	-40	125	℃
	Ambient Temperature	Suffix version 7	-40	105	℃
T_J	Junction temperature range	Suffix version 8	-40	135	℃
	Junction temperaturerange	Suffix version 7	-40	125	℃

1. Guaranteed by design, not tested during production.

4.3.2 Operating conditions at power-up and power-down

The parameters given in the following table are based on testing under the ambient temperature listed in Table 4-4.

Table 4-5 Operating conditions at power-up and power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rising time rate	From 0 to V_{DD}	20	10^6	µs/V
	V_{DD} falling time rate	From V_{DD} to 0	50	∞	µs/V

1. Guaranteed by design, not tested during production.

4.3.3 Reset and power control module features

The parameters given in the following table are based on tests at ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Reset and power control module features(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Rising	PVD[3:0]=0	Reserve			V

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	Falling	PVD[3:0]=0				
	Rising	PVD[3:0]=1	2	2.08	2.16	
	Falling	PVD[3:0]=1	1.9	1.98	2.06	
	Rising	PVD[3:0]=2	2.2	2.28	2.36	
	Falling	PVD[3:0]=2	2.1	2.18	2.26	
	Rising	PVD[3:0]=3	2.4	2.48	2.56	
	Falling	PVD[3:0]=3	2.3	2.38	2.46	
	Rising	PVD[3:0]=4	2.6	2.68	2.76	
	Falling	PVD[3:0]=4	2.5	2.58	2.66	
	Rising	PVD[3:0]=5	2.8	2.88	2.96	
	Falling	PVD[3:0]=5	2.7	2.78	2.86	
	Rising	PVD[3:0]=6	3	3.08	3.16	
	Falling	PVD[3:0]=6	2.9	2.98	3.06	
	Rising	PVD[3:0]=7	3.2	3.28	3.36	
	Falling	PVD[3:0]=7	3.1	3.18	3.26	
	Rising	PVD[3:0]=8	3.4	3.48	3.56	
	Falling	PVD[3:0]=8	3.3	3.38	3.46	
	Rising	PVD[3:0]=9	3.6	3.68	3.76	
	Falling	PVD[3:0]=9	3.5	3.58	3.66	
	Rising	PVD[3:0]=10	3.8	3.88	3.96	
	Falling	PVD[3:0]=10	3.7	3.78	3.86	
	Rising	PVD[3:0]=11	4	4.08	4.16	
	Falling	PVD[3:0]=11	3.9	3.98	4.06	
	Rising	PVD[3:0]=12	4.2	4.28	4.36	
	Falling	PVD[3:0]=12	4.1	4.18	4.26	
	Rising	PVD[3:0]=13	4.4	4.48	4.56	
	Falling	PVD[3:0]=13	4.3	4.38	4.46	
	Rising	PVD[3:0]=14	4.6	4.68	4.76	
	Falling	PVD[3:0]=14	4.5	4.58	4.66	
	Rising	PVD[3:0]=15	4.8	4.88	4.96	
	Falling	PVD[3:0]=15	4.7	4.78	4.86	
$V_{PVDhyst}$(1)	PVD hysteresis	-	80	100	125	mV
V_{LVR}	Rising	LVR[3:0]=0	Reserve			V
	Falling	LVR[3:0]=0				
	Rising	LVR[3:0]=1	2	2.08	2.16	
	Falling	LVR[3:0]=1	1.9	1.98	2.06	
	Rising	LVR[3:0]=2	2.2	2.28	2.36	
	Falling	LVR[3:0]=2	2.1	2.18	2.26	
	Rising	LVR[3:0]=3	2.4	2.48	2.56	
	Falling	LVR[3:0]=3	2.3	2.38	2.46	
	Rising	LVR[3:0]=4	2.6	2.68	2.76	
	Falling	LVR[3:0]=4	2.5	2.58	2.66	
	Rising	LVR[3:0]=5	2.8	2.88	2.96	

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	Falling	LVR[3:0]=5	2.7	2.78	2.86	
	Rising	LVR[3:0]=6	3	3.08	3.16	
	Falling	LVR[3:0]=6	2.9	2.98	3.06	
	Rising	LVR[3:0]=7	3.2	3.28	3.36	
	Falling	LVR[3:0]=7	3.1	3.18	3.26	
	Rising	LVR[3:0]=8	3.4	3.48	3.56	
	Falling	LVR[3:0]=8	3.3	3.38	3.46	
	Rising	LVR[3:0]=9	3.6	3.68	3.76	
	Falling	LVR[3:0]=9	3.5	3.58	3.66	
	Rising	LVR[3:0]=10	3.8	3.88	3.96	
	Falling	LVR[3:0]=10	3.7	3.78	3.86	
	Rising	LVR[3:0]=11	4	4.08	4.16	
	Falling	LVR[3:0]=11	3.9	3.98	4.06	
	Rising	LVR[3:0]=12	4.2	4.28	4.36	
	Falling	LVR[3:0]=12	4.1	4.18	4.26	
	Rising	LVR[3:0]=13	4.4	4.48	4.56	
	Falling	LVR[3:0]=13	4.3	4.38	4.46	
	Rising	LVR[3:0]=14	4.6	4.68	4.76	
	Falling	LVR[3:0]=14	4.5	4.58	4.66	
	Rising	LVR[3:0]=15	4.8	4.88	4.96	
	Falling	LVR[3:0]=15	4.7	4.78	4.86	
$V_{LVRhyst}$(1)	LVR hysteresis	-	80	100	125	mV
$V_{POR/PDR}$	VDD power-up/down reset thresholds	Falling edge	1.65	1.7	1.74	V
		Rising edge	1.77	1.8	1.95	V
$V_{PDR/PORhyst}$(1)	POR/PDR hysteresis voltage	-	50	100	150	mV
$T_{PVDresp}$	PVD response time	-	-	2	-	us
$T_{RSTTEMPO}$(1)	Reset Duration	-	76	150	250	us

1. Guaranteed by design, not tested in production.

4.3.4 Internal reference voltage

The parameters given in the following table are based on tests at ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-Temperature drift characteristics at 40 ℃<TA<+105 ℃(2)	-	-	60	mV
		-Temperature drift characteristics at 40 ℃<TA<+125 ℃(2)	-	-	65	mV
		T_A = 25℃，VDD=5.0V(3)	1.14	1.2	1.26	V
$T_{S\_vrefint}$(1) (2)	When reading the internal reference voltage, the sampling time of the ADC	PLS[2:0]=001 (Rising edge) f_{ADC_CLK}=24M	15.8	-	126.7	µs

1. The shortest sampling time is obtained through multiple cycles in the application, with the minimum value converted to an ADC sampling period of 380 cycles and the maximum value converted to an ADC sampling period of 3040 cycles.

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2. Guaranteed by design, not tested in production.

3. Tested in production.

4.3.5 Power supply current characteristics

Current consumption is a combination of a number of parameters and factors that include operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, flip-flop rate of I/O pins, location of the program in memory, and code executed.

The current consumption measurements are described in detail in Figure 4-4.

All current consumption measurements given in this section for all modes of operation execute a condensed set of code.

4.3.5.1 Maximum current consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.
- Flash memory access time is adjusted to the frequency of SYSCLK (0 wait cycles for 0 to 24 MHz, 1 wait cycle for 24 to 48 MHz, and 2 wait cycles above 48 MHz).
- Instruction prefetch is on (Hint: this parameter must be set before setting the clock and bus divider).
- When peripheral is turned on: $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$.

The parameters given in Table 4-8 and Table 4-9 are based on tests at ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-8 Typical current consumption in run mode with data processing code running from internal flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) VDD=5.5V,T_A = 105°C	Typ (1) VDD=5.5V,T_A = 125°C	Unit
I_{DD}	Supply current in operation mode	External clock. Enable all peripherals	64MHz	20.23	20.38	mA
			32MHz	11.23	15.30	
			16MHz	6.72	6.84	
			8MHz	4.40	4.52	
		External clock. Turn off all peripherals	64MHz	13.58	13.72	
			32MHz	7.77	7.90	
			16MHz	4.88	5.00	
			8MHz	3.38	3.49	
I_{DD}	Supply current in operation mode	Internal clock. Enable all peripherals	64MHz	20.04	20.15	mA
			32MHz	11.13	11.24	
			16MHz	6.67	6.78	
			8MHz	3.41	3.46	
		Internal clock. Turn off all peripherals	64MHz	13.45	13.57	
			32MHz	7.70	7.82	
			16MHz	4.84	4.96	
			8MHz	2.39	2.45	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Table 4-9 Typical current consumption in sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ (1) VDD=5.5V,T_A = 105°C	Typ (1) VDD=5.5V,T_A = 125°C	Unit

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I_{DD}	Supply current in sleep mode	External clock. Enable all peripherals	64MHz	15.82	15.95	mA
			32MHz	8.93	9.05	
			16MHz	5.45	5.56	
			8MHz	3.35	3.46	
		External clock. Turn off all peripherals	64MHz	8.43	8.54	
			32MHz	5.10	5.21	
			16MHz	3.43	3.53	
			8MHz	2.24	2.34	
I_{DD}	Supply current in sleep mode	Internal clock. Enable all peripherals	64MHz	15.67	15.48	mA
			32MHz	8.86	8.96	
			16MHz	5.41	5.51	
			8MHz	2.37	2.41	
		Internal clock. Turn off all peripherals	64MHz	8.35	8.45	
			32MHz	5.07	5.17	
			16MHz	3.41	3.51	
			8MHz	1.26	1.31	

1. Guaranteed by design and comprehensive evaluation, Tested in production with maximal V_{DD} and maximal f_{HCLK}.

4.3.5.2 Typical current consumption

The chip test conditions are as follows:

- All I/O pins are in input mode and connected to a static level-V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.
- Flash memory access time is adjusted to the frequency of SYSCLK (0 wait cycle for 0 to 24 MHz, 1 wait cycle for 24 to 48 MHz, and 2 wait cycles above 48 MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-4.
- Instruction prefetch is on (Hint: This parameter must be set before setting the clock and bus divider).
- When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$.

The parameter test conditions in the following table are based on Table 4-4.

Table 4-10 Typical current consumption in run mode with data processing code running from internal flash memory (T_A=25 ℃, V_{DD}=5.0V)

Symbol	Parameter	Conditions	f_{HCLK}	Typ(2)		Max	Unit
				Enable all peripherals	Turn off all peripherals	Turn off all peripherals	
I_{DD}	Supply current in operation mode	External High Speed Clock	64MHz	19.90	13.22	-	mA
			32MHz	10.92	7.45	-	
			16MHz	6.42	4.57	-	
			8MHz	4.10	3.07	-	
I_{DD}	Supply current in operation mode	Internal high-speed clock	64MHz	19.90	13.21	15(1)	mA
			32MHz	10.91	7.45	-	
			16MHz	6.42	4.57	-	
			8MHz	3.40	2.37	-	

1. Tested in production.
2. Guaranteed by design and comprehensive evaluation, not tested in production.

Table 4-11 Typical current consumption in run mode with data processing code running from internal flash memory

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(T_A=25°C、V_{DD}=3.3V) (1)

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Enable all peripherals	Turn off all peripherals	
I_{DD}	Supply current in operation mode	External High Speed Clock	64MHz	19.74	13.06	mA
			32MHz	10.77	7.30	
			16MHz	6.28	4.43	
			8MHz	3.96	2.93	
I_{DD}	Supply current in operation mode	Internal high-speed clock	64MHz	19.73	13.06	mA
			32MHz	10.76	7.30	
			16MHz	6.27	4.43	
			8MHz	3.39	2.37	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Table 4-12 Typical current consumption in sleep mode (T_A=25°C、V_{DD}=5.0V)

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Max	Unit
				Enable all peripherals	Turn off all peripherals	Turn off all peripherals	
I_{DD}	Supply current in sleep mode	External High Speed Clock	64MHz	15.53	8.12	-	mA
			32MHz	8.64	4.80	-	
			16MHz	5.15	3.13	-	
			8MHz	3.06	1.94	-	
I_{DD}	Supply current in sleep mode	Internal high-speed clock	64MHz	15.53	8.12	10(2)	mA
			32MHz	8.63	4.80		
			16MHz	5.15	3.13	-	
			8MHz	2.36	1.24	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Tested in production.

Table 4-13 Typical current consumption in sleep mode (T_A=25°C、V_{DD}=3.3V)

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals	Turn off all peripherals	
I_{DD}	Supply current in sleep mode	External High Speed Clock	64MHz	15.37	7.98	mA
			32MHz	8.49	4.66	
			16MHz	5.01	2.99	
			8MHz	2.92	1.80	
I_{DD}	Supply current in sleep mode	Internal high-speed clock	64MHz	15.36	7.97	mA
			32MHz	8.48	4.66	
			16MHz	5.01	2.98	
			8MHz	2.35	1.24	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.5.3 Low Power Current Consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VDD or VSS (no load).
- All peripherals are off unless otherwise noted.

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Table 4-14 Typical consumption in stop and power-down mode (T_A=25°C、V_{DD}=3.3V)

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			T_A=25°C	T_A=105°C	T_A=125°C		
I_{DD_STOP}	Current in STOP mode	SRAM hold, all I/O status hold, BS TIM, independent watchdog off	2.96	24.97	55.84	-	uA
I_{DD_PD}	Current in PD mode	All power supplies are turned off, only the wake-up pin, NRST required circuits are retained for operation	0.95	3.48	8.11	-	uA

Table 4-15 Typical consumption in stop and power-down mode (T_A=25°C、V_{DD}=5.0V)

Symbol	Parameter	Conditions	Typ(1)			Max(2)	Unit
			T_A=25°C	T_A=105°C	T_A=125°C	T_A=25°C	
I_{DD_STOP}	Current in STOP mode	SRAM hold, all I/O status hold, BS TIM, independent watchdog off	3.75	26.57	58.67	10	uA
I_{DD_PD}	Current in PD mode	All power supplies are turned off, only the wake-up pin, NRST required circuits are retained for operation	1.76	5.06	10.86	3	uA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Tested in production.

4.3.6 External clock source characteristics

4.3.6.1 High-speed external clock generated by external oscillator

The characteristic parameters given in the following table were measured using ambient temperatures and supply voltages in accordance with Table 4-4.

Table 4-16 High-speed external clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User External Clock Frequency (1)	T_A=25°C	1	8	16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	15(2)	
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Calculated at HSE=16MHz

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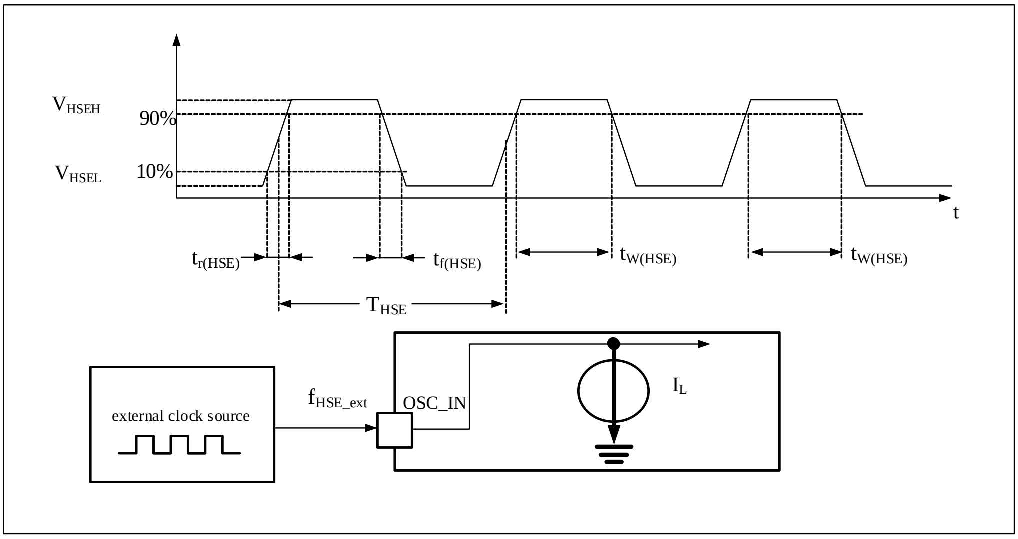
Figure 4-5 AC timing diagram of external high-speed clock source



High-Speed External Clock Generation Using a Crystal/Ceramic Resonator

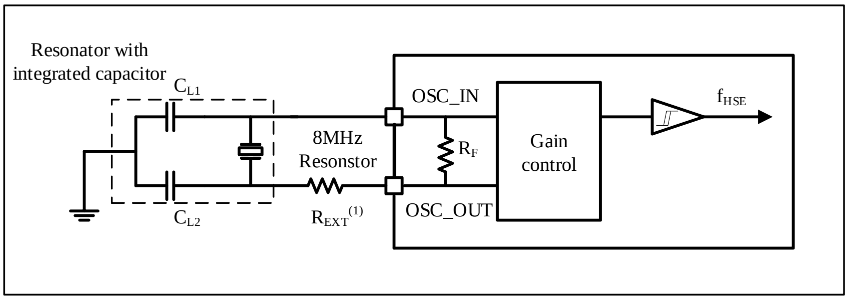
High-speed external clocks (HSE) can be generated using an oscillator consisting of a crystal/ceramic resonator from 8 to 16 MHz. The information given in this section is based on a comprehensive characterization using typical external components listed in the table below. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the appropriate manufacturer. (The crystal resonator mentioned here is what we usually refer to as passive crystal oscillator)

Table 4-17 HSE 8~16MHz Oscillator Characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	oscillator frequency	-	8	-	16	MHz
C_{L1} C_{L2}(3)	Recommended load capacitance with corresponding crystal serial impedance (R_{EXT})	$R_{EXT} = 30\Omega$	-	12	25	pF
$t_{SU(HSE)}$(3)	Start-up time (8M crystal)	V_{DD} is stable	-	3	-	ms

1. Resonator characteristics are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the start-up time, which is measured from the time the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

Figure 4-6 Typical application using 8MHz crystal



1. R_{EXT} value is determined by the characteristics of the crystal.

4.3.7 Internal clock source characteristics

The characteristics given in the following table were measured using ambient temperatures and supply voltages in accordance with Table 4-4.

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4.3.7.1 High-speed internal (HSI) RC oscillator

Table 4-18 HSI Oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI_8M}	Frequency	VDD=5.0V, T_A = 25°C, post-calibration	7.96(3)	8	8.04(3)	MHz
f_{HSI_24M}	Frequency	VDD=5.0V, T_A = 25°C, post-calibration	23.88(3)	24	24.12(3)	MHz
ACC_{HSI}	Temperature drift of HSI oscillator(4)	VDD=5.0V, T_A = -40~125°C, Temperature drift	-2.1	-	2.1	%
		VDD=5.0V, T_A = -40~105°C, Temperature drift	-2	-	2	%
		VDD=5.0V, T_A = -20~85°C, Temperature drift	-1.5	-	1.5	%
		VDD=5.0V, T_A = 0~70°C, Temperature drift	-1	-	1	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	1.5	2.5	4	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	140	250	330	µA

1. V_{DD} = 5.0V, T_A = -40 to 125 ℃ unless otherwise noted.
2. Guaranteed by design, not tested in production.
3. Production calibration accuracy, not including soldering effects. Frequency deviation due to soldering ranges from approximately ±1%.
4. Frequency deviation including soldering effects, data from sample testing, not tested in production.

4.3.7.2 Low-speed internal (LSI) RC oscillator

Table 4-19 LSI Oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	output frequency	25 ℃ Calibration, V_{DD}=5.0V(3)	31	32	33	KHz
		V_{DD} =2.0V ~ 5.5V, T_A = -40 ~ 105°C Real-time calibration based on temperature changes via software	28.8	32	35.2	KHz
		V_{DD} =2.0V ~ 5.5V, T_A = -40 ~ 125°C Real-time calibration based on temperature changes via software	27.2	32	36.8	KHz
$t_{SU(LSI)}$ (2)	LSI Oscillator Startup Time	-	-	30	80	µs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.3	0.7	µA

1. V_{DD} = 5.0V, T_A = -40 to 125 ℃ unless otherwise noted.
2. Guaranteed by design, not tested in production.
3. Tested in production.

4.3.8 Low-power mode wake-up time

The wake-up times listed in Table 4-20 were measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used for wake-up depends on the current operating mode:

- STOP/PD mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times are measured using the ambient temperature and supply voltage in accordance with Table 4-4.

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Table 4-20 Low-power mode wake-up time

Symbol	Parameter	Typ	Max	Unit
$t_{WUSLEEP}$(1)	Wake-up from SLEEP mode	-	16	HCLK
t_{WUSTOP}(1)	Fast wake-up from STOP mode	31	62	us
	Normal wake-up from STOP mode	41	82	
t_{WUPD}(1)	Wake-up from PD mode	100	200	

1. Wake-up time is measured from the start of the wake-up event until the user program reads the first instruction.

4.3.9 PLL characteristics

The parameters listed in Table 4-20 are measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-21 PLL characteristics(1)

Symbol	Parameter	Num			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL Input Clock	4	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_IN}/N	PLL input clock after N-division	4	-	16	MHz
f_{PLL_OUT}	PLL multiplier output clock(2)	48	-	72	MHz
t_{LOCK}	PLL Ready indication signal output time	-	-	20	µs
Jitter	TIE RMS Jitter	-	40	121	pS
Ipll	Operating Current of PLL @64MHz VCO frequency. (1)	-	300	500	uA

1. Guaranteed by design, not tested in production.
2. Care needs to be taken to use the correct multiplication factor so that f_{PLL_OUT} is within the allowable range based on the PLL input clock frequency.

4.3.10 FLASH characteristics

All characterization parameters were obtained at TA = -40~125 ℃ unless otherwise stated.

Table 4-22 FLASH characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
t_{PROG}	64-bit programming time	T_A = -40~125°C	144.5	175	185	µs
t_{ERASE}	Page (512 bytes) erase time	T_A = -40~125°C	2	-	3	ms
t_{ME}	Mass erase time	T_A = -40~125°C	30	35	40	ms
I_{DD}	Supply current (1)	Reading mode, f_{HCLK}=64MHz, V_{DD}=5.0V	-	4.5	6.0	mA
		Write mode, f_{HCLK}=64MHz, V_{DD}=5.0V	-	-	2	mA
		Erase mode, f_{HCLK}=64MHz, V_{DD}=5.0V	-	-	1.5	mA
		PD/STOP mode, V_{DD}=2.0~5.0V	-	0.3	15(2)	µA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Tested at T_A = 85 ℃.

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Table 4-23 Flash memory life and data retention period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40~125 ℃	100	kcycles
t_{RET}	Data retention	T_A = 125 ℃, after 1000 erasing cycle(1)	10	years
		T_A = 85 ℃, after 1000 erasing cycle(1)	20	years

1. Derived from characterization tests, not tested in production.

4.3.11 Absolute maximum value (electrical sensitivity)

Based on three different tests (ESD, LU), the chip is tested for strength to determine its performance in terms of electrical sensitivity, using specific measurement methods.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) was applied to all pins of all samples.

Table 4-24 ESD Absolute Maximum

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, Conforming to AEC-Q100-002	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A = +25 ℃, Conforming to AEC-Q100-011	750	

1. Derived from characterization tests, not tested in production.

Static Peg-Lock

To evaluate bolting performance, 2 complementary static bolting tests on 6 samples are required:

- For each power supply pin, provide a supply voltage that exceeds the limit.
- Injects current on each input, output, and configurable I/O pin.

This test complies with the EIA/JESD78F IC bolting standard.

Table 4-25 Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static bolts and locks	T_A = +125 ℃, complies with JESD78F standard	II level A

4.3.12 I/O port characteristics

Generalized Input/Output Characteristics

Unless otherwise noted, the parameters listed in the following table were measured under the conditions of Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-26 I/O static characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
V_{IL}(1)	Input Low Level Voltage	5	-	-	0.3×VDD	V
		3.3	-	-	0.8	
		2.0	-	-	0.2×VDD	
V_{IH}(1)	Input High Level Voltage	5	-	0.7×VDD	-	
		3.3	-	2.037	-	

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		2.0	-	0.8×VDD	-	
V_{hys}(1)	Schmitt trigger voltage hysteresis(1)	5/3.3/2.0	-	0.1×VDD	-	V
I_{lkg}(1) (2)	Input leakage current IIH	5/3.3/2.0	-	-	1	µA
	Input leakage current IIL	5/3.3/2.0	-	1	-	
V_{OH}	Output high level voltage	5(3)	High driving Imin=16mA low driving Imin=8mA	VDD-0.7	VDD*1.005	V
		3.3(1)	High driving Imin=8mA low driving Imin=4mA	2.4	-	
		2.0(1)	High driving Imin=4mA low driving Imin=2mA	VDD-0.45	-	
V_{OL}	Output Low Voltage	5(3)	High driving Imin=16mA low driving Imin=8mA	0.1	0.4	
		3.3(1)	High driving Imin=8mA low driving Imin=4mA	-	0.45	
		2.0(1)	High driving Imin=4mA low driving Imin=2mA	-	0.4	
R_{PU}(3)	Weak pull-up equivalent resistance	5/3.3/2.0	-	20	120	kΩ
R_{PD}(3)	Weak pull-down equivalent resistance	5/3.3/2.0	-	20	120	kΩ
C_{IO}(1)	Capacitance of I/O pins	5/3.3/2.0	-	-	10	pF

1. Hysteresis voltage for Schmitt trigger switching levels. Guaranteed by characterization tests, not tested in production.
2. Leakage current may be higher than maximum if there is reverse current back-up at adjacent pins.
3. Tested in production.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their characteristics take into account most stringent CMOS process or TTL parameters:

Output driving current

GPIO (General Purpose Input/Output Port) can absorb or output up to+/-16mA current. In user applications, the number of I/O pins must ensure that the driving current does not exceed the absolute maximum rated value given in section 4.2:

The total current obtained by all I/O ports from VDD, plus the maximum operating current obtained by the MCU on VDD, must not exceed the absolute maximum rated value IVDD (Table 4-2).

The total current absorbed by all I/O ports and flowing out of VSS, plus the maximum operating current flowing out of the MCU on VSS, must not exceed the absolute maximum rated value IVSS (Table 4-2).

Input and output AC characteristics

The definitions and values of the input and output AC characteristics are given in Table 4-4.

Unless otherwise stated, the parameters are measured using ambient temperatures and supply voltages in accordance with Table 4-4.

Table 4-27 I/O AC Characteristics

VDD	Conditions			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	CLoading(pf)	Min	Typ	Max	Min	Typ	Max
5V(4.5~5.5)	Low (DR=1)	Slow (SR=1)	25	2.493	3.509	5.393	4.351	6.296	10.13
			50	4.109	5.81	9.086	5.289	7.597	12.11
			100	7.498	10.65	16.63	7.036	10.04	15.83
		Fast (SR=0)	25	2.173	3.062	4.793	3.751	5.486	8.93
			50	3.865	5.427	8.521	4.615	6.698	10.78

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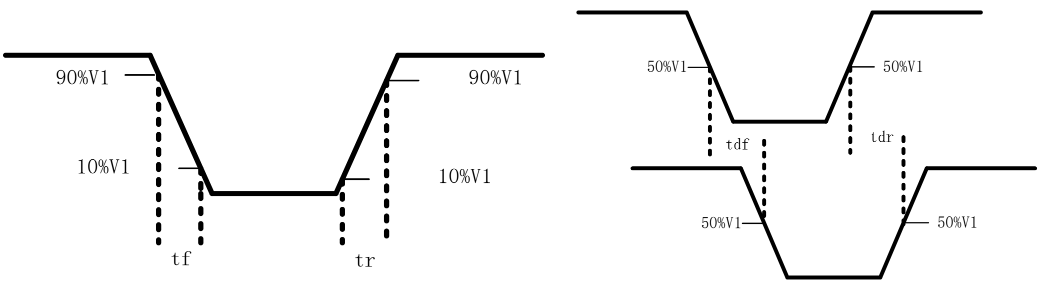
			100	7.295	10.34	16.12	6.331	9.1	14.43
	High (DR=0)	Slow (SR=1)	25	1.627	2.276	3.513	3.855	5.623	9.126
			50	2.454	3.442	5.349	4.421	6.405	10.32
			100	4.095	5.779	8.891	5.375	7.728	12.33
		Fast (SR=0)	25	1.344	1.892	2.957	3.356	4.943	8.115
			50	2.157	3.023	4.721	3.825	5.6	9.126
			100	3.833	5.372	8.369	4.698	6.82	10.99
3.3V(2.7~3.6)	Low (DR=1)	Slow (SR=1)	25	3.215	4.727	8.585	5.309	7.923	14.38
			50	5.357	7.964	14.47	6.524	9.695	17.54
			100	9.718	14.47	26.42	8.8	13.03	23.5
		Fast (SR=0)	25	2.819	4.168	7.648	4.522	6.811	12.43
			50	5.008	7.455	13.54	5.646	8.46	15.39
			100	9.49	14.05	25.86	7.875	11.74	21.25
	High (DR=0)	Slow (SR=1)	25	2.095	3.063	5.522	4.67	7.017	12.8
			50	3.176	4.66	8.4	5.403	8.075	14.67
			100	5.311	7.816	14.12	6.636	9.868	17.88
		Fast (SR=0)	25	1.729	2.546	4.659	3.999	6.059	11.12
			50	2.784	4.124	7.503	4.612	6.956	12.73
			100	4.97	7.338	13.33	5.75	8.623	15.73
2V(1.8~2.2)	Low (DR=1)	Slow (SR=1)	25	5.641	9.338	16.84	9.428	15.96	28.85
			50	9.431	15.81	28.57	11.66	19.58	35.32
			100	17.25	28.99	52.5	15.78	26.51	47.71
		Fast (SR=0)	25	5.027	8.341	15.1	8.015	13.6	24.73
			50	8.92	14.98	27.03	10.06	17.03	30.88
			100	16.9	28.5	51.08	14.13	23.89	43.09
	High (DR=0)	Slow (SR=1)	25	3.642	6.019	10.83	8.458	14.31	25.88
			50	5.54	9.139	16.52	9.741	16.42	29.64
			100	9.372	15.49	28.08	11.94	20.07	36.18
		Fast (SR=0)	25	3.044	5.064	9.218	7.162	12.21	22.24
			50	4.941	8.194	14.88	8.272	14.05	25.55
			100	8.829	14.62	26.53	10.34	17.51	31.74

1. Guaranteed by design, not tested in production

Figure 4-7 I/O AC characteristic definition



4.3.13 NRST pin characteristics

The NRST pin has an internal integrated pull-up resistor, and the parameters are measured using ambient temperature and supply voltage in accordance with Table 4-4, unless otherwise noted.

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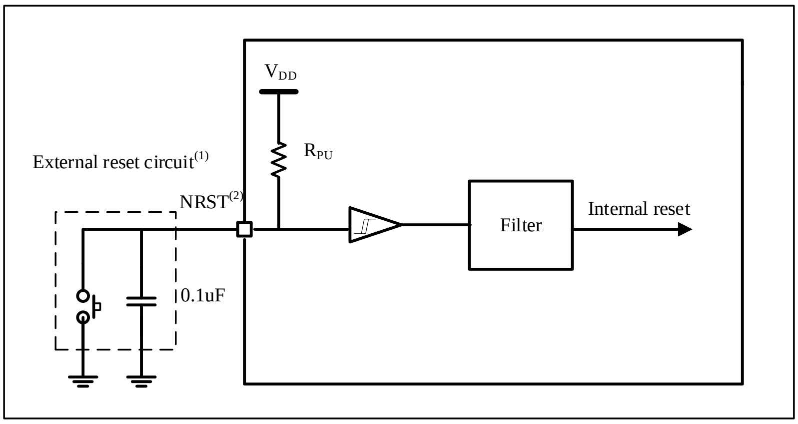
Table 4-28 NRST pin characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	2.0V~5.5V	-	-	0.3VDD	V
$V_{IH(NRST)}$(1)	NRST input high voltage	2.0V~5.5V	0.7VDD	-	-	
$V_{hys(NRST)}$ (1)	NRST Schmitt trigger voltage hysteresis	2.0V~5.5V	115	220	315	mV
R_{PU}(1)	Weak pull-up equivalent resistance (2)	2.0V~5.5V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	2.0V~2.2V	-	-	196	ns
		3V~3.6V	-	-	115	
		4.5V~5.5V	-	-	81	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	2.0V~2.2V	540	-	-	ns
		3V~3.6V	287	-	-	
		4.5V~5.5V	191	-	-	

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a real resistor in series with a non-switchable PMOS implementation. The resistance of this PMOS switch is very small (about 10%).

Figure 4-8 Recommended NRST Pin Protection



1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin can be below the maximum VIL(NRST), otherwise the MCU cannot get reset.

4.3.14 TIM characteristics

The parameters listed are guaranteed by design

Table 4-29 TIM characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency for CH1 to CH4	-	0	f_{TIMCLK}/2	MHz
		f_{TIMCLK} = 64MHz	0	32	MHz
Res_{TIM}	Timer Resolution	-	-	16	bits
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	0.015625	1024	µs
	Maximum possible count	-	-	65536x65536	t_{TIMCLK}

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t_{MAX_COUNT}		f_{TIMCLK} = 64MHz	-	67.109	s

Table 4-30 TIM2/3/4/5 characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency for CH1 to CH4	-	0	$f_{TIMCLK}/2$	MHz
		f_{TIMCLK} = 64MHz	0	32	MHz
Res_{TIM}	Timer Resolution	-	-	16	bits
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	0.015625	1024	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	-	67.109	s

Table 4-31 TIM6 characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	15.625	-	ns
Res_{TIM}	Timer Resolution	-	-	16	bits
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	0.015625	1024	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536x65536	t_{TIMCLK}
		f_{TIMCLK} = 64MHz	-	67.109	s

4.3.15 IWDG characteristics

Table 4-32 IWDG Maximum and minimum count reset times (LSI = 32KHz)

Prescaler divider	IWDG_PREDIV.PD[2:0]	Min(1) IWDG_RELV.REL[11:0]=0	Max(1) IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.125	512	ms
/8	001	0.25	1024	
/16	010	0.5	2048	
/32	011	1	4096	
/64	100	2	8192	
/128	101	4	16384	
/256	11x	8	32768	

1. Guaranteed by design, not tested in production。

4.3.16 WWDG characteristics

Table 4-33 WWDG Maximum and Minimum Count Reset Time (APB1 PCLK1 = 32MHz)

Prescaler divider	WWDG_CFG.TIMERB[1:0]	Min(1) WWDG_CGF.W[13:0]=0x3F	Max(1) WWDG_CFG.W[13:0]=0x3FFF	Unit
/1	00	0.128	2089	ms
/2	01	0.256	4178	
/4	10	0.512	8356	
/8	11	1.024	16712	

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1. Guaranteed by design, not tested in production。

4.3.17 I2C characteristics

Unless otherwise specified, parameters are measured using ambient temperature, f_{PCLK} frequency and V_{DD} supply voltage in accordance with Table 4-4.

The I2C interface of the N32A052 products conforms to the standard I2C communication protocol with the following limitation: SDA and SCL are not "true" open-drain pins, and when configured as open-drain outputs, the PMOS tubes between the pin and VDD are turned off but still present.

The I2C interface characteristics are shown in the table below, and see Section 4.3.12 for details on the characteristics of the input/output multiplexing pins (SDA and SCL).

Table 4-34 I2C interface characteristics

Symbol	Parameter	Standard model		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C Interface Frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.50	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{su(STA)}$	Repeat Start Condition Establishment Time	4.7	-	0.6	-	0.26	-	µs
$t_{h(SDA)}$	SDA data hold time	-	3.45	-	0.9	-	0.4	µs
$t_{su(SDA)}$	SDA build-up time	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1 C_b	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20+0.1 C_b	300	-	120	ns
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Stop condition to start condition time (bus idle)	4.7	-	1.3	-	0.50	-	µs
C_b	Capacitive load per bus	-	400	-	400	-	550	pf
t_{SP}	Spike pulse width suppressed by analog filter in standard and fast mode	-	-	0	50	0	50	ns
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	µs
$t_{v (ACK)}$	Answer validity time	-	3.45	-	0.9	-	0.45	µs

1. Guaranteed by design, not tested in production.
2. f_{PCLK} must be greater than 2MHz to achieve maximum frequency for standard mode I2C. f_{PCLK} must be greater than 4MHz to achieve maximum frequency for fast mode I2C.

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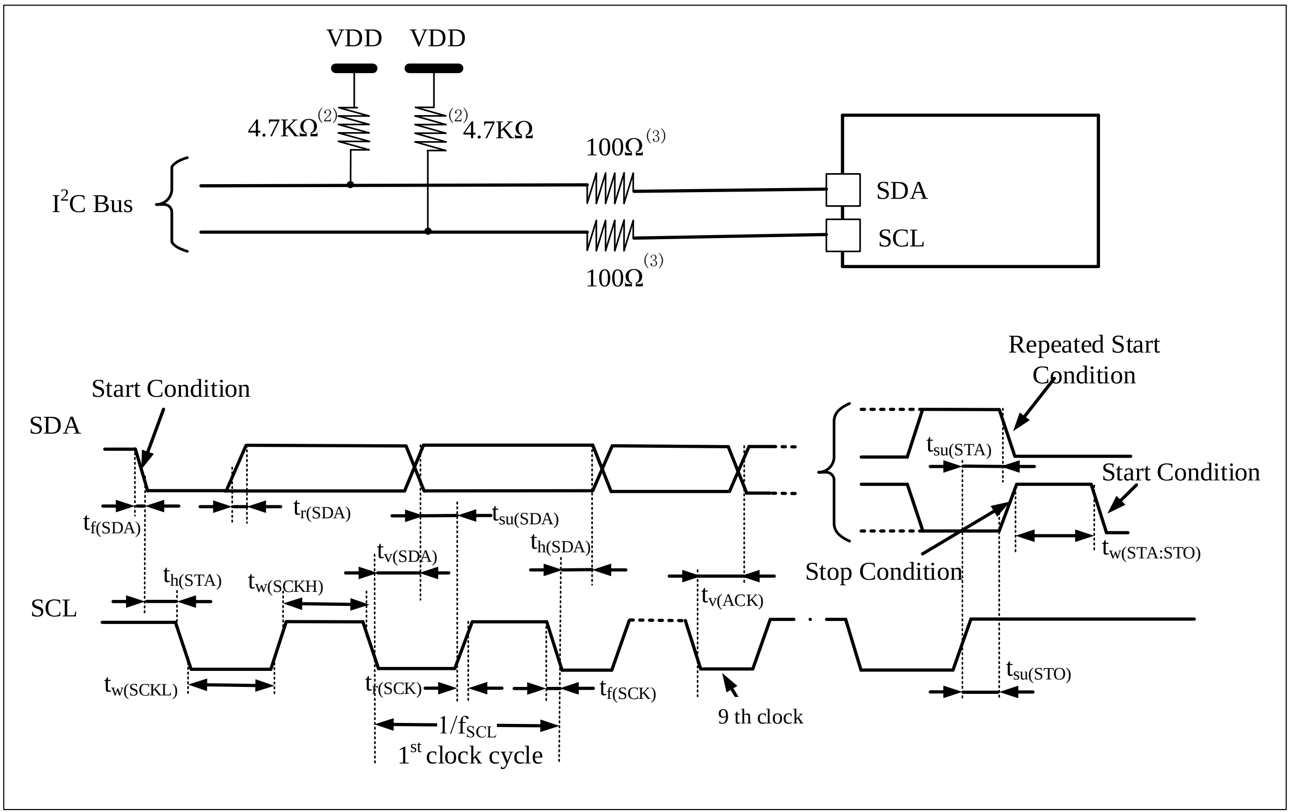
Figure 4-9 I2C bus AC waveform and measurement circuit (1)



1. The measurement points are set at $0.3V_{DD}$ and $0.7V_{DD}$.
2. Pull-up resistor resistance value depends on I2C interface speed.
3. The resistance value depends on the actual electrical characteristics. It is possible to leave the serial resistor unconnected and connect the signal line directly.

4.3.18 SPI characteristics

Unless otherwise noted, SPI parameters are measured using ambient temperature, f_{PCLK} frequency, and V_{DD} supply voltage conforming to the conditions in Table 4-4.

For details on the characteristics of the input-output multiplexing function pins (NSS, SCLK, MOSI, MISO of SPI), see Section 4.3.12.

Table 4-35 SPI characteristics (4)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$(1)	SPI Clock Frequency	Master Mode	-	16	MHz
		Slave Mode	-	12	
$t_{r(SCLK)}t_{f(SCLK)}$(1)	SPI clock rise and fall times	load capacitance ： C = 30pF	-	11	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	SPI Slave Mode	35	70	%
$t_{su(NSS)}$ (1)	NSS Establishment Time	Slave Mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS Hold Time	Slave Mode	$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master Mode	$t_{PCLK/BR}-2$	$t_{PCLK/BR}+2$	ns
$t_{su(MI)}$(1)	Data Input Establishment Time	Master Mode	5	-	ns

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$t_{su(SI)}$ (1)		Slave Mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master Mode	5	-	ns
$t_{h(SI)}$ (1)		Slave Mode	6	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave Mode, f_{PCLK} = 20MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave Mode	2	10	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave Mode(After enabling edge)	-	31	ns
$t_{v(MO)}$ (1)		Master Mode(After enabling edge)	-	15	
$t_{h(SO)}$ (1)	Data output hold time	Slave Mode(After enabling edge)	7	-	ns
$t_{h(MO)}$ (1)		Master Mode(After enabling edge)	0	-	

1. Simulation test results obtained under VDD=3.3V/5V and load capacitance C=20pF, not tested in production.
2. Minimum value indicates the minimum time to drive the output, maximum value indicates the maximum time to get the data correctly.
3. Minimum value indicates the minimum time to turn off the output, maximum value indicates the maximum time to place the data line in a high resistance state.

Figure 4-6 SPI sequence diagram - slave mode and CPHA=0

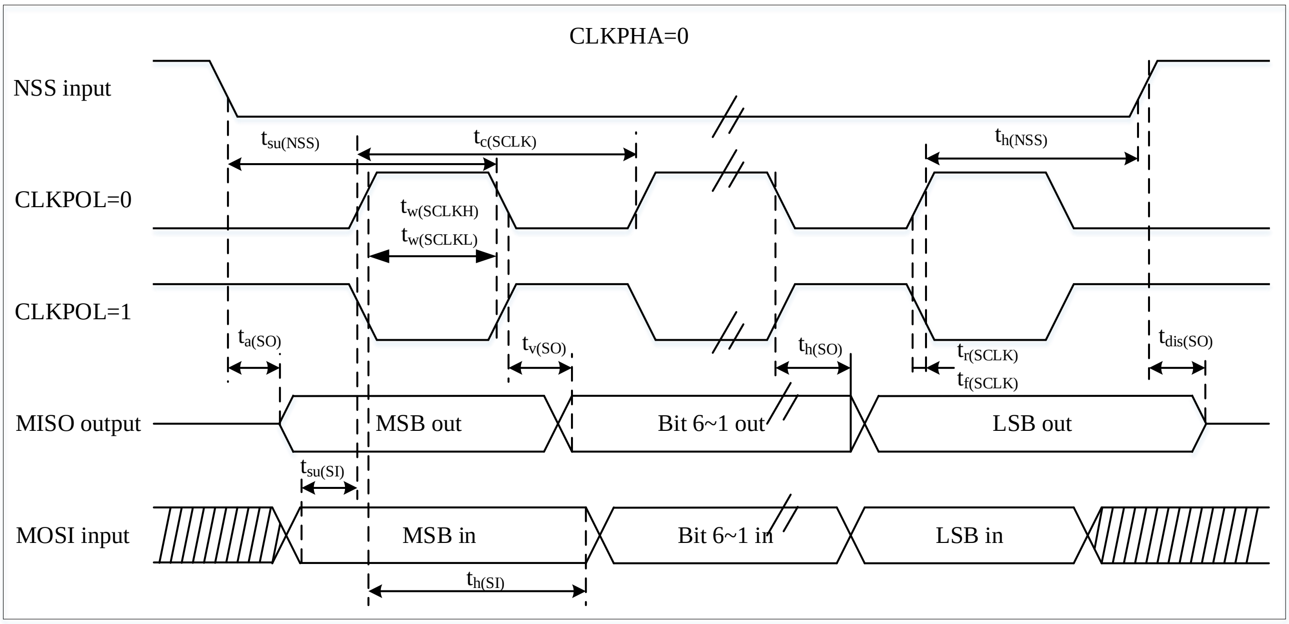

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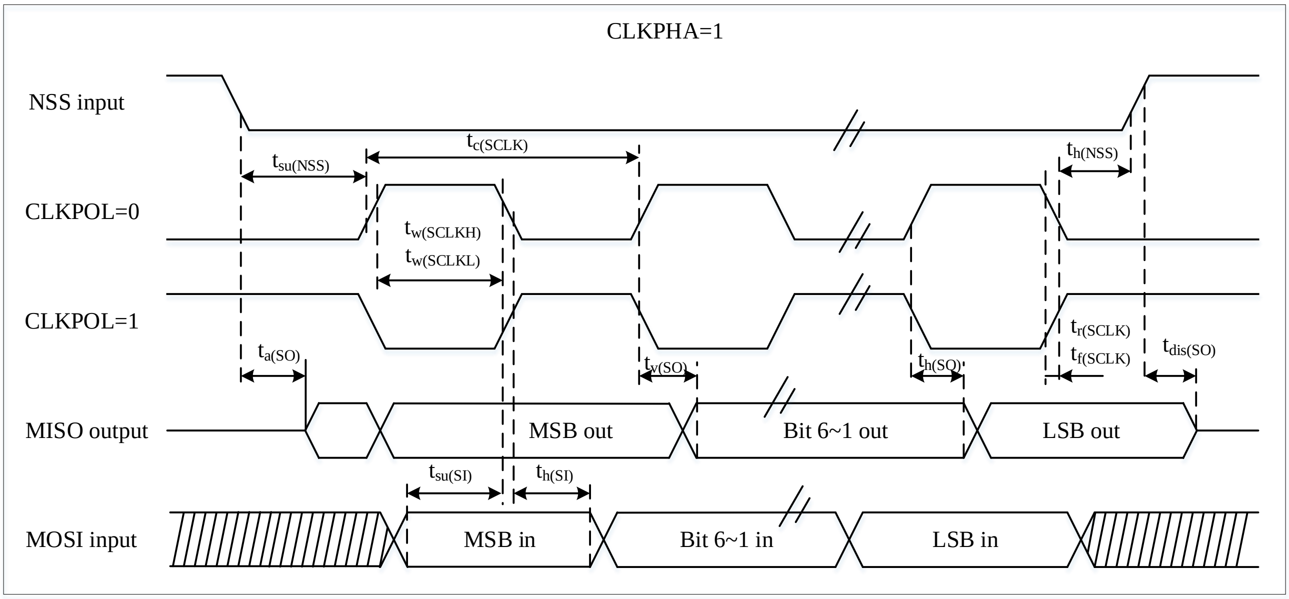
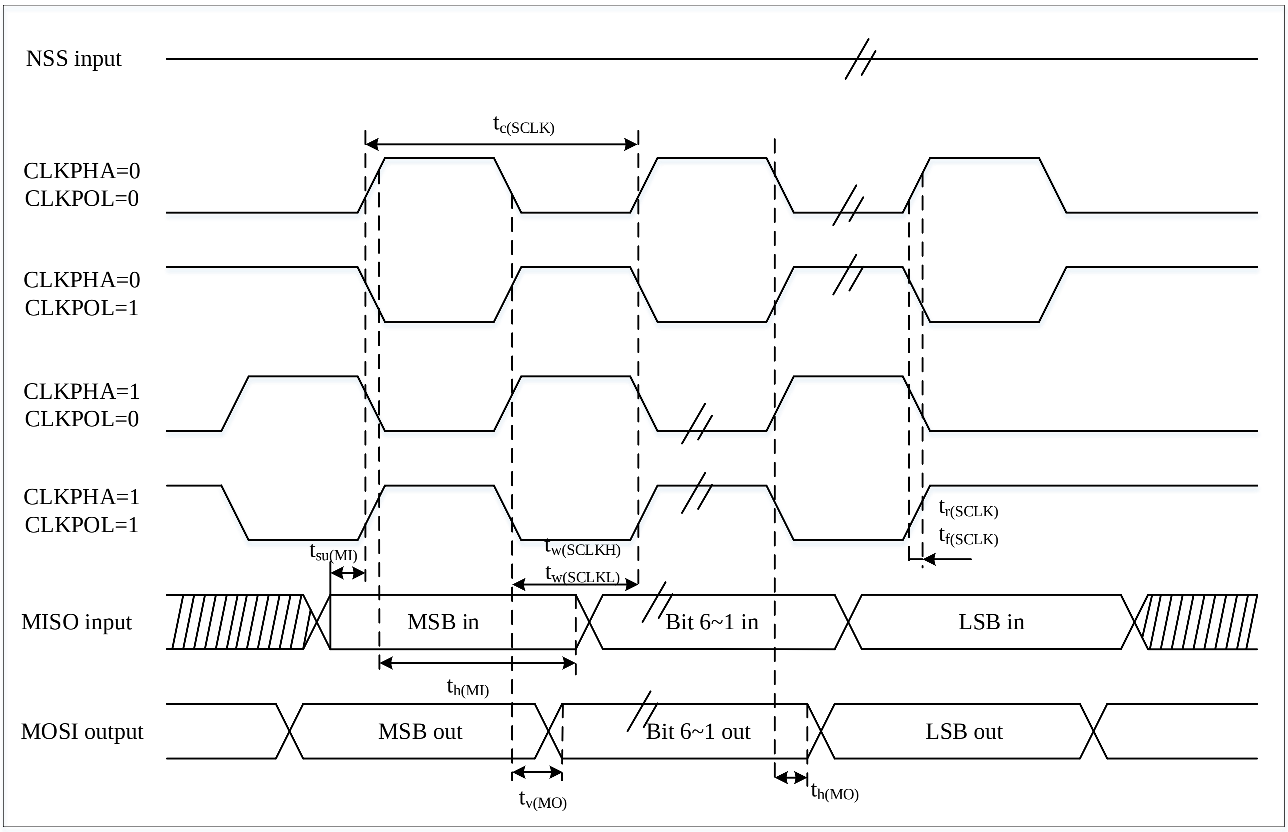
Figure 4-7 SPI sequence diagram - slave mode and CPHA=1(1)



1. The measurement points were set at the CMOS level of 0.3 V_{DD} and 0.7 V_{DD}.

Figure 4-8 SPI timing diagram-master mode (1)



1. The measurement points are set at CMOS level: 0.3 V_{DD} and 0.7 V_{DD}.

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4.3.19 CAN Interface Characteristics

For details on the characteristics of the input/output multiplexing function pins (CAN_TX and CAN_RX), see Section 4.3.12.

It is recommended to use HSE as the clock source for CAN.

4.3.20 12-bit ADC electrical parameters

Unless otherwise noted, the parameters of Table 4-4 are measured using an ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage that meet the conditions of Table 4-4.

Table 4-36 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}(1)	Supply Voltage	-	2.4(2)	-	5.5	V
V_{REF+}	Positive Reference Voltage	-	V_{DD}			V
f_{ADC}	ADC Clock Frequency	-	-	-	24	MHz
f_s(1)	Sampling Rate	-	0.03	-	1	Msps
V_{AIN}	Conversion Voltage Range	-	0 (VSSA or VREF- connected to ground)	-	V_{REF+}	V
R_{AIN}(1)	External Input Impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC Input Resistance	VDD=3.3V	600	750	975	Ω
		VDD=5.0V	360	450	585	Ω
C_{ADC}(1)	Internal sample and hold capacitance	-	22	26	30	pF
SNDR	Signal-to-noise distortion	VDD=3.3V	57	58.5	73	dB
		VDD=5.0V	57.7	58.9	74	dB
T_S(1)	Number of Sampling Cycles	-	6	-	3040	$1/f_{ADC}$
t_{STAB}(1)	Power-up time	-	48	-	-	$1/f_{ADC}$
t_{CONV}(1)	Conversion time	-	12			$1/f_{ADC}$
I_{ADC}	ADC current consumption	-	-	1.47	5.88	mA

1. Guaranteed by design, not tested in production.
2. ADC performance metrics degrade with 2.4V supply

Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above equation (Equation 1) is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. where N=12 (indicating 12-bit resolution).

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Table 4-37 ADC sampling time (VDD = 3.3V) (1)

Resolution	Rin（kΩ）	Minimum sampling time（ns）
12-bit	0.9	500
	1.2	583
	2.2	833
	3.8	1250
	8.1	2333
	10.8	3000
	18.7	5000
	28.9	7583
	38.5	10000
	61.6	15833

1. Guaranteed by design, not tested in production.

Table 4-38 ADC sampling time(VDD = 5.0V) (1)

Resolution	Rin（kΩ）	Minimum sampling time（ns）
12-bit	0.6	500
	0.9	583
	1.9	833
	3.5	1250
	7.8	2333
	10.5	3000
	18.4	5000
	28.6	7583
	38.2	10000
	61.3	15833

1. Guaranteed by design, not tested in production.

Table 4-39 ADC accuracy (1)

Symbol	Parameter	Conditions	Typ	Max(2)	Unit
EO	Offset Error	f_{ADC} = 24 MHz, Sample rate=1M sps, V_{DDA} = 3.3V, T_A = 25 ℃	±2	±5	LSB
ED	Differential Linearity Error		±0.6	±5	
EL	Integral Linearity Error		±1.5	±2	
EO	Offset Error	f_{ADC} = 24 MHz, Sample rate=1M sps, V_{DDA} = 5.0V, T_A = 25 ℃	±2	±5	
ED	Differential Linear Error		±0.6	1.5	
EL	Integral Linear Error		±1.5	2.5	
ENOB	Effective number of bits	f_{HCLK} = 64MHz(clock source HSI_8M), f_{ADC} = 24 MHz， sample rate=1M sps, T_A = 25 ℃	10.3	-	Bits
		f_{HCLK} =48MHz(clock source HSE), f_{ADC} = 24MHz， sample rate=1M sps, T_A = 25 ℃	10.5	-	

1. ADC Accuracy vs. Reverse Current Injection: Reverse current injection on any standard analog input pin needs to be avoided, as it can significantly degrade the accuracy of a conversion being performed on another analog input pin. It is recommended that a Schottky diode be added to the standard analog pin (between the pin and ground) where the reverse injection current may be generated.

2. Guaranteed by characterization tests, not tested in production.

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Figure 4-9 ADC Accuracy Characteristics

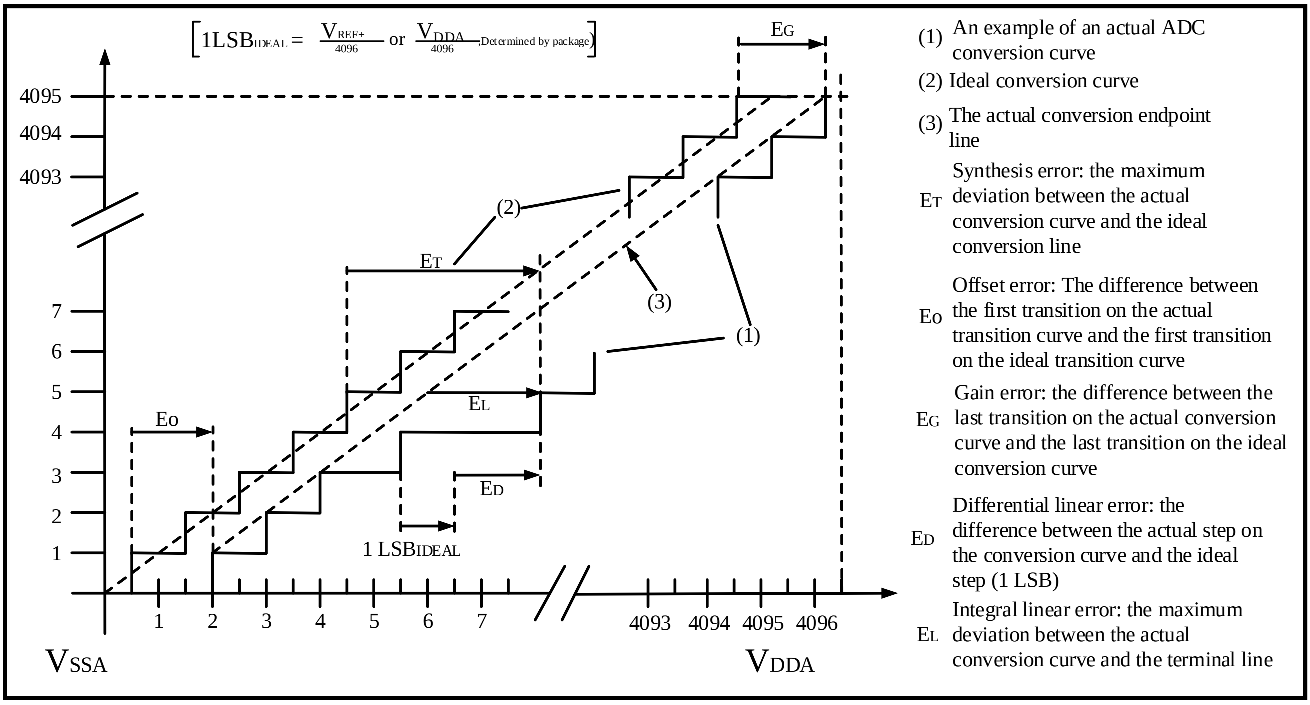
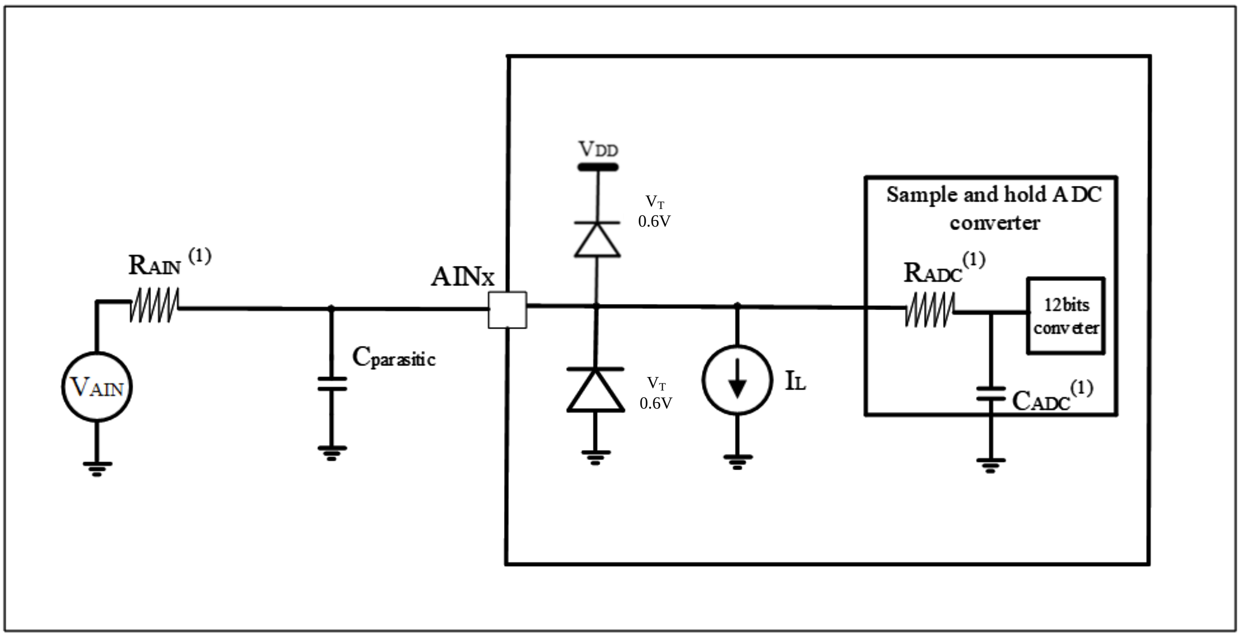


Figure 4-10 ADC typical connection diagram



1. See Table 4-36 for R_{AIN}, R_{ADC}, and C_{ADC} values.
2. Cparasitic represents the parasitic capacitance (approximately 7pF) on the PCB (related to soldering and PCB layout quality) and pads. Larger values of Cparasitic will reduce the accuracy of the conversion and the solution is to reduce the f_{ADC}.

4.3.21 12-bit DAC Electrical Parameters

Unless otherwise noted, the parameters in Table 4-39 DAC Characteristics are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage that meet the conditions in Table 4-4.

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Table 4-40 V_{REFP} characteristics

Symbol	Parameter	Min	Typ	Max	Unit	marginal notes
V_{DDA}	Analog Supply Voltage	2.97	-	5.5	V	-
V_{REF+}	Reference Voltage	2.97	-	5.5	V	V_{REF+} must always be lower than V_{DDA}
R_L	Load resistance with buffer on	5	-	-	kΩ	Minimum load resistance between DAC_OUT and V_{SSA}
C_L	Load capacitance	-	-	50	pF	Maximum capacitance on the DAC_OUT pin
DAC_OUT Min	DAC_OUT voltage with buffer on	0.2	-	-	V	The maximum DAC output span is given When VREF+=5.5V corresponds to 12-bit input values 0x095~0xF6B. When VREF+=2.97V corresponds to 12-bit input values 0x114~0xEEC.
DAC_OUT Max	DAC_OUT voltage with buffer on	-	-	V_{REF+} - 0.2	V	
	DAC_OUT voltage when buffer is off	-	-	V_{REF+} – 5LSB		
I_{DD}	In standstill mode (standby mode) DAC DC consumption (V_{DDD}+V_{DDA}+V_{REF+})	-	900	1500	µA	No load, input median 0x800
		-	1400	1600		No load, input maximum when VREF+ = 5.5V
I_{DDQ}	In power-down mode DAC DC consumption (V_{DDD}+V_{DDA}+V_{REF+})	-	10	2200	nA	unloaded
	In power-down mode DAC DC consumption (V_{DDA}+V_{REF+})	-	10	2200		
DNL	Nonlinear distortion (deviation between 2 consecutive codes)	-	-	±2.4	LSB	DAC configured to 10 bits (always B1=B0=0)
INL	Nonlinear accumulation (deviation between the value measured at code i and the line between code 0 and code 4095)	-	-	±6	LSB	DAC configured for 12-bit
misalignment	Offset error (deviation between the measured value at code 0x800 and the ideal value V_{REF+}/2)	-	-	±12	mV	DAC configured for 12-bit
		-	-	±12	LSB	When V_{REF+}=3.3V, the DAC is configured to 12 bits.
gain error	gain error	-	-	±0.6	%	DAC configured for 12-bit
Amplifier Gain	Amplifier gain with open loop	50	85	87.5	dB	5kΩ load (maximum load)
$t_{SETTLING}$	Setup time (full range: 10-bit input code changes from minimum to maximum value, DAC_OUT reaches ±1 LSB of its final value)	2	3	4	µs	$C_{LOAD} \leq 50pF$ $R_{LOAD} \geq 5k\Omega$
refresh rate	The maximum frequency of the correct DAC_OUT is obtained when the input code is a small change (from the value i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50pF$ $R_{LOAD} \geq 5k\Omega$

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t_{WAKEUP}	Wake-up time from off state (PDV18 changes from 1 to 0)	2	6.5	10	µs	$C_{LOAD} \leq$ 50pF， $R_{LOAD} \geq$ 5kΩ Input code between minimum and maximum possible values
PSRR+	Supply rejection ratio (relative to V_{DD}33A) (static DC measurement)	-72	-60	-40	dB	No R_{LOAD}， $C_{LOAD} \leq$ 50pF

1. Guaranteed by design, not tested in production.

4.3.22 COMP characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and VDD supply voltage in accordance with the conditions in Table 4-4.

Table 4-41 COMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Analog supply voltage	normal mode	2.4	3.3	5.5	V
V_{IN}	Input Voltage Range	VIN	0	-	VDD	
t_{START}(1)	Comparator start-up build-up time	-	-	-	7	us
t_d	Propagation delay for 200mV step with 100mV overdrive	Falling edge	70	110	150	ns
		Rising edge	64	102	135	
V_{OFFSET}	Comparator Input Offset Error	VIN	-	±5	±20	mV
V_{hys}	Comparison Hysteresis Voltage	No hysteresis	-	0	-	mV
		Low hysteresis	4.5	7	34	
		Medium hysteresis	15	17	64	
		High hysteresis	17.5	32	94	
I_{DD}	Comparator Current Consumption	Static	-	167	219	µA
		cmp With 50 kHz ±100 mV overdrive square signal	-	168	220	
		cmp static with 1* 6bit dac on	-	207	416	
		cmp static with 2* 6bit dac on	-	247	483	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.23 Segment LCD characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and VDD supply voltage in accordance with the conditions in Table 4-4.

Table 4-42 LCD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	5.0	5.5	V
I_{LCD}	Supply current from V_{DD} at V_{DD} = 5.0 V	Buffer off + only high resistance on	-	4.5	6.75	µA
		Buffer off + both high and low resistance on	-	24.7	30	µA
I_{VLCD}	Supply current from V_{LCD} (V_{LCD} = 5.0V)+ high resistance turn on	Buffer on（BUFEN = 1, 1/2 Bias）	-	7.2	10.8	µA
		Buffer on（BUFEN = 1, 1/3 Bias）	-	12.86	19.29	

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		Buffer on（BUFEN = 1, 1/4 Bias）	-	12.86	19.29	
R_{HN}	Total High Resistance Value of Low Driving Resistor Network		0.75	1	1.25	MΩ
R_{LN}	Total low resistance value of high driving resistance network		150	200	250	KΩ
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		2.375(2)	3/4 V_{LCD}	2.575(2)	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage		1.55(2)	1/2 V_{LCD}	1.75(2)	
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		0.725(2)	1/4 V_{LCD}	0.925(2)	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design, not tested in production.
2. VDD = 3.3V，tested in production.

Table 4-43 LCD Adjustable contrast(1)

gear level	VLCD(HR)			VLCD(LR)		
	Min	Typ	Max	Min	Typ	Max
0	Typ*0.94	1.00 * VCC	Typ*1.06	Typ*0.94	1.00 * VCC	Typ*1.06
1	Typ*0.94	0.97* VCC	Typ*1.06	Typ*0.94	0.96 * VCC	Typ*1.06
2	Typ*0.94	0.94 * VCC	Typ*1.06	Typ*0.94	0.92* VCC	Typ*1.06
3	Typ*0.94	0.9* VCC	Typ*1.06	Typ*0.94	0.88* VCC	Typ*1.06
4	Typ*0.94	0.87* VCC	Typ*1.06	Typ*0.94	0.84 * VCC	Typ*1.06
5	Typ*0.94	0.84* VCC	Typ*1.06	Typ*0.94	0.8* VCC	Typ*1.06
6	Typ*0.94	0.8 * VCC	Typ*1.06	Typ*0.94	0.76 * VCC	Typ*1.06
7	Typ*0.94	0.77* VCC	Typ*1.06	Typ*0.94	0.73 * VCC	Typ*1.06
8	Typ*0.94	0.74 * VCC	Typ*1.06	Typ*0.94	0.7* VCC	Typ*1.06
9	Typ*0.94	0.7* VCC	Typ*1.06	Typ*0.94	0.66* VCC	Typ*1.06
10	Typ*0.94	0.67* VCC	Typ*1.06	Typ*0.94	0.63 * VCC	Typ*1.06
11	Typ*0.94	0.64* VCC	Typ*1.06	Typ*0.94	0.6 * VCC	Typ*1.06
12	Typ*0.94	0.61 * VCC	Typ*1.06	Typ*0.94	0.57* VCC	Typ*1.06
13	Typ*0.94	0.58 * VCC	Typ*1.06	Typ*0.94	0.53* VCC	Typ*1.06
14	Typ*0.94	0.54* VCC	Typ*1.06	Typ*0.94	0.5* VCC	Typ*1.06
15	Typ*0.94	0.5 * VCC	Typ*1.06	Typ*0.94	0.47 * VCC	Typ*1.06

1. Guaranteed by design and comprehensive evaluation, not tested in production.

4.3.24 Temperature sensor characteristics

Unless otherwise noted, parameters are measured using ambient temperature, f_{HCLK} frequency, and VDD supply voltage that meet the conditions of Table 4-4.

Table 4-44 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with respect to temperature	-	±1	±5	℃
Avg_Slope(1)	Average Slope	-3.7	-3.9	-4.3	mV/℃

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V_{25}(1)	Voltage at 25 ℃	1.3	1.32	1.34	V
t_{START}(1)	Build-up time	4	-	10	µs
T_{S_temp}(2)(3)	ADC sampling time when reading temperature	8.2	-	17.1	µs

1. Guaranteed by characterization test results, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application program through multiple cycles.

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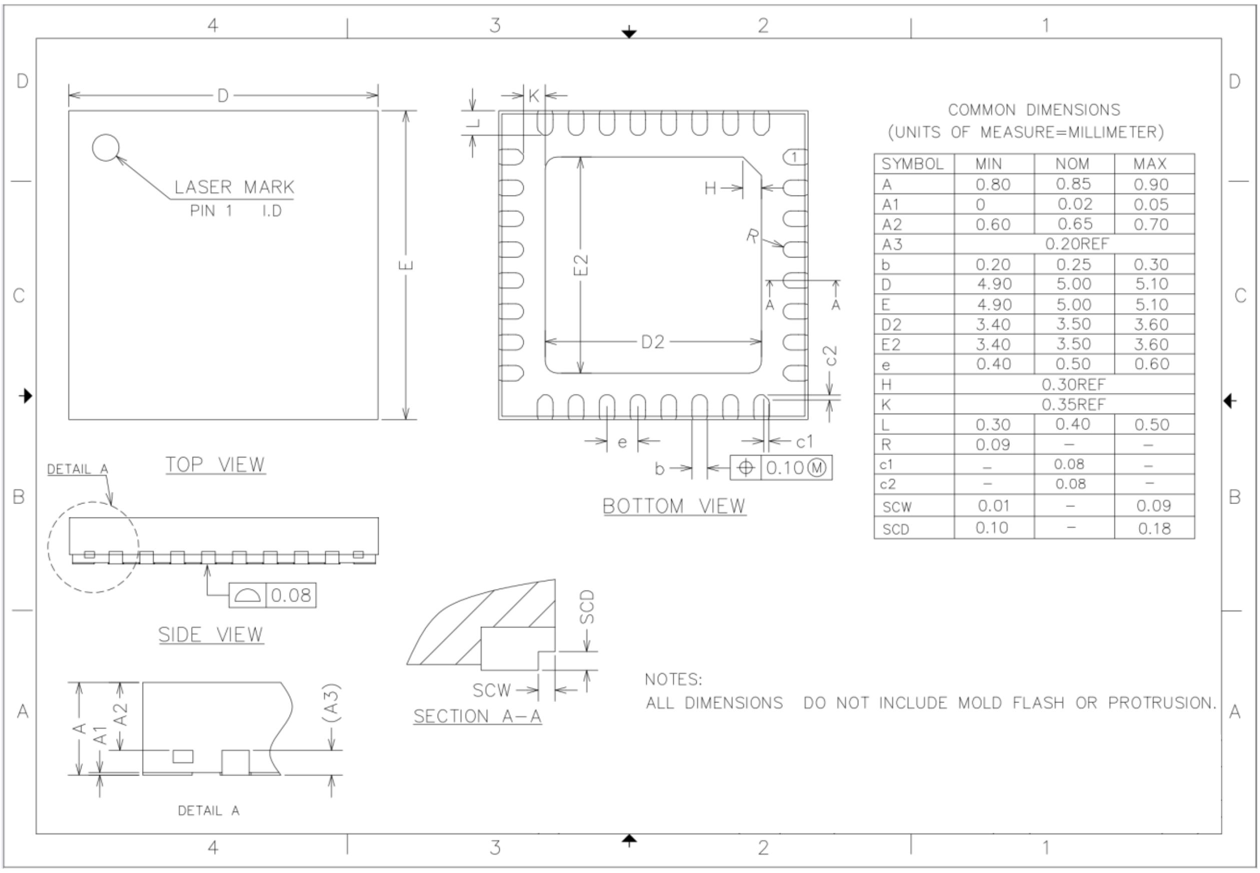
5 Package information

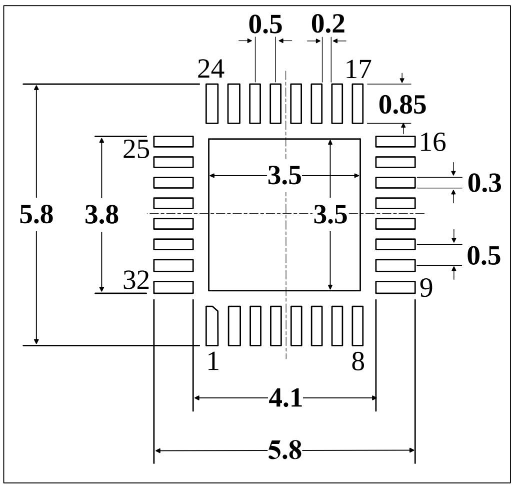
5.1 QFN32 (5x5mm)

Figure 5-1 N32A052KBQ7 package outline



SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e	0.40	0.50	0.60
H		0.30REF	
K		0.35REF	
L	0.30	0.40	0.50
R	0.09	–	–
c1	–	0.08	–
c2	–	0.08	–
SCW	0.01	–	0.09
SCD	0.10	–	0.18

Figure 5-2 Suggestions for QFN32(5x5mm) package solder pads(1)



1. The unit of measurement is millimeters

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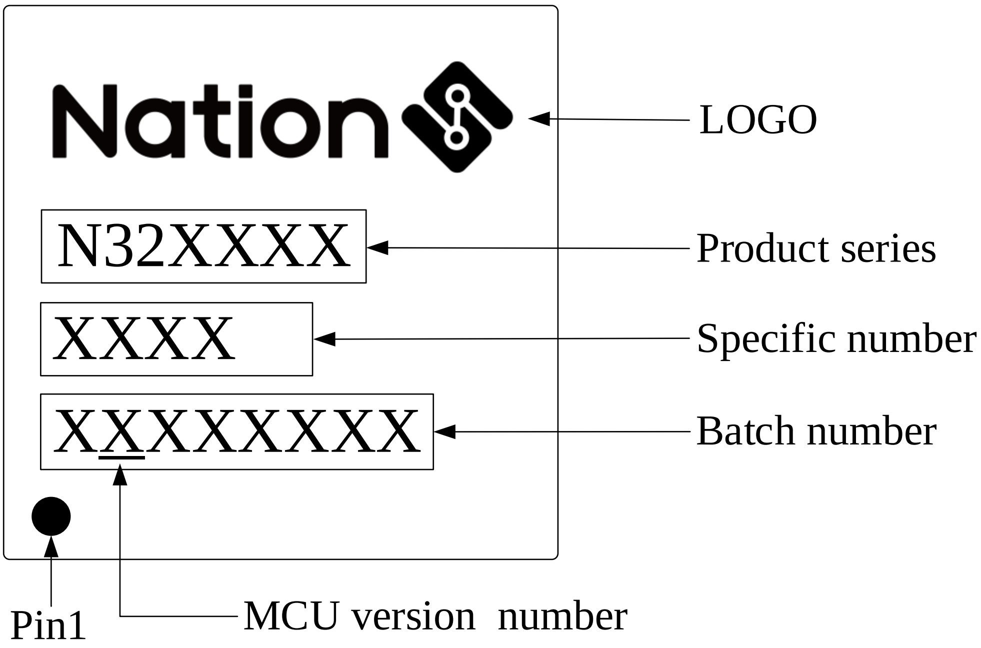
5.2 Marking information

Figure 5-3 Marking information



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6 Ordering Information

Figure 6-1 N32A052 series ordering code information diagram

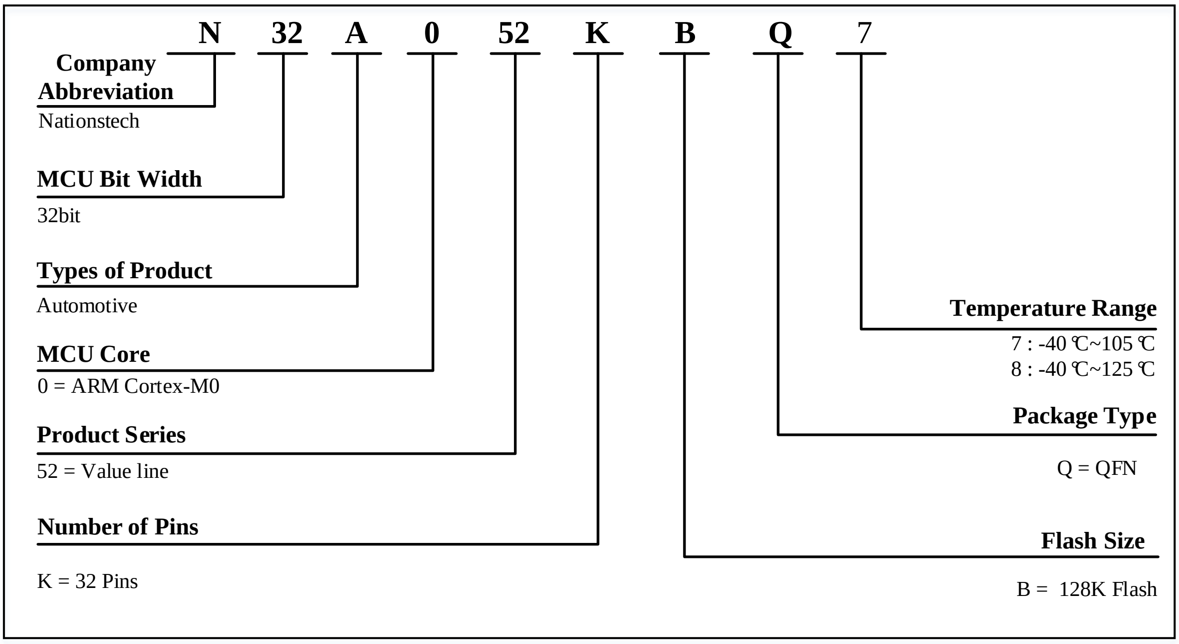

Table 6-1 N32A052 series ordering code information

Order Code(1)	Package	Package Size	Packaging(2)	SPQ(3)	temperature range
N32A052KBQ8	QFN32	5*5mm	Tray	490	-40°C~125°C
			Reel	2500	
N32A052KBQ7	QFN32	5*5mm	Tray	490	-40°C~105°C
			Reel	2500	

1. For the latest detailed ordering information, please refer to the selection manual.
2. This packaging is the basic packaging. If you have any other requirements, please contact Nsing Technology
3. Minimum packaging quantity

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7 Version history

Date	Version	Modify
2026.3.3	V1.0.0	Initial version

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