N32G05x Series Errata Manual V1.2.0

Content

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1 Errata List

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chapter 5: I2C interface	chapter 5.1: STOP establishment time exceeds the minimum limit in standard mode	●
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●：There is this issue

-：There is no such issue

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2 Reset and clock control（RCC）

2.1 HSE not fully started up, HSE_ready bit ready issue

Description

After enabling HSE, HSE did not fully vibrate, but HSE READY was set.

Solution

1. Capture the HSE/128 clock using TIM2_CH4, determine that HSE is fully oscillating, and add this code to the SDK. The maximum waiting time for determining whether HSE has fully started oscillating is 200ms. If it exceeds 200ms, HSI will be used as the system clock.

2.2 LSI ready bit ready issue

Question 1:

Description

The LSI ready bit cannot clear the issue in RUN mode.

Reason

1. In RUN mode, the LSI remains in the enabled state, the LSI enable bit is invalid, and the LSI remains in the ready state.

Question 2:

Description

When the MCU operates at a voltage of 2.0V, there is a small probability that the LSI read bit cannot be set properly.

Solution

1. Increase the operating voltage of MCU to 2.4V.

3 Real Time Clock(RTC)

3.1 Tamper interrupt does not meet expectations

Description

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RTC intrusion pin rising/falling edge triggering tamper interrupt does not meet expectations, and there may be situations where it cannot be triggered or triggered incorrectly.

Solution

The RTC intrusion pin requires adding up/down resistors to the outer board level circuit.

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4 Analog to Digital Conversion(ADC)

4.1 When the ENDC flag is set, immediately read the ADC data register value for abnormal issues

Description

After ENDC is set, immediately read the ADC data register, which may read the result of the previous conversion.

Solution

1. After the ENDC flag is set, delay by 8 ADC_CK clocks before reading the ADC data register;
2. In some scenarios, the ENDCA flag is used instead of the ENDC flag.

5 I2C interface

5.1 STOP establishment time exceeds the minimum limit in standard mode

Description

In host mode: When the communication rate is 100K and the clock extension of the slave is triggered, the STOP establishment time will be less than 4us.

Solution

Suggest reducing the communication speed to 50K or below according to the timing requirements of the slave peripheral devices.

6 Timer

6.1 Timer 0% or 100% duty cycle PWM output mode switching

Description

When TIM switches to PWM1/2 mode in other modes (except for freeze mode), if the PWM duty cycle is 100% or 0%, it cannot be successfully switched to PWM1/2 mode. At this time, when the PWM duty cycle is modified to non-100% or 0%, it can be successfully switched to PWM1/2 mode output.

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Solution

When switching between the forced valid/forced invalid/channel matching valid/channel matching invalid mode and the PWM 1/2 mode with 100% or 0% duty cycle, achieve 100% or 0% duty cycle by modifying CCxP.

Switching from flipping mode to PWM 1/2 mode with 100% or 0% duty cycle, no solution available.

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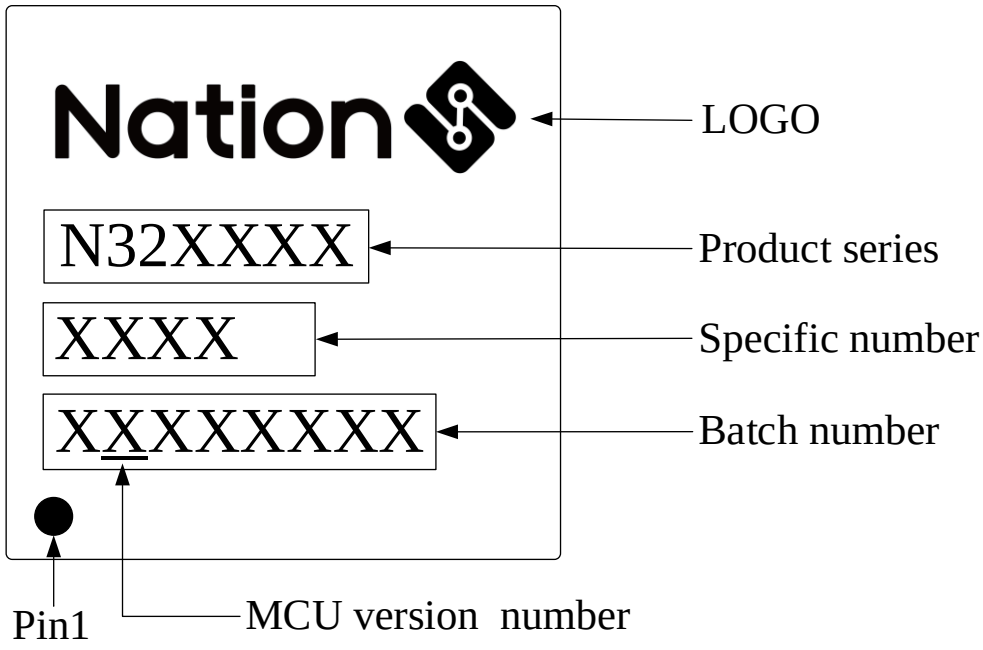
7 Chip Marking Information and Version Description



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8 Version history

Data	Version	Notes
2026.3.3	V1.0.0	Initial version

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