N32G430 series crystal selection guide

Introduction

This document details the crystal selection guide for N32G430 series MCUs to provide users reference.

Contents

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1. Description for crystal selection

1.1 Application circuit for crystal

Figure 1-1 is the typical application circuit for crystal， feedback resistor(R_F) is embedded in the oscillator circuitry， No external resistance is required.

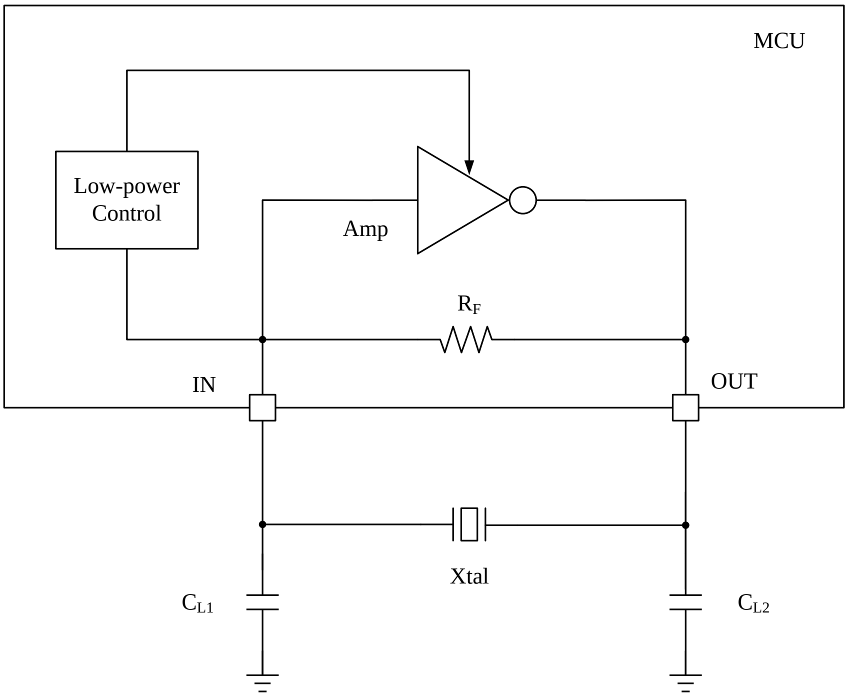

Figure 1-1 Typical application with a 32.768 kHz crystal

1.2 Selection of Capacitors

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors to match the requirements of the crystal, C_{L1} and C_{L2}, are usually the same value.

Load capacitance CL has the following formula: $CL = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + Cstray$ where Cstray is the pin capacitance and board or trace PCB-related capacitance.

Example: if you choose a crystal with a load capacitance of CL =7 pF, and Cstray = 2 pF, then $C_{L1} = C_{L2} = 10$ pF.

1.3 Crystal test

1.3.1 LSE parameter configuration

When using the LSE external crystal， call the void RCC_LSE_Config (uint32_t RCC_LSE, uint16_t LSE_Trim) function,and configure the LSE parameters through the input parameter uint16_t LSE_Trim. For details, see the following code example:

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```
/**
*\*\name    RCC_LSE_Config.
*\*\fun     Configures the External Low Speed oscillator (LSE).
*\*\param   RCC_LSE(the new state of the LSE):
*\*\          - RCC_LSE_DISABLE    LSE oscillator OFF
*\*\          - RCC_LSE_ENABLE     LSE oscillator ON
*\*\          - RCC_LSE_BYPASS     LSE oscillator bypassed with external clock
*\*\param   LSE_Trim(LSE Driver Trim Level):
*\*\          - 0x00~0x1FF
*\*\return  none
**/
void RCC_LSE_Config(uint32_t RCC_LSE,uint16_t LSE_Trim)
{
    /* Enable PWR Clock */
    RCC_APB1_Peripheral_Clock_Enable(RCC_APB1_PERIPH_PWR);
    /* PWR DBKP set 1 */
    PWR->CTRL |=  PWR_CTRL_DBKP;

    /* Reset LSEEN LSEBP bits before configuring the LSE */
    *(__IO uint32_t*)RCC_BDCTRL_ADDR &= (~(RCC_LSE_ENABLE | RCC_LSE_BYPASS));
    /* Configure LSE (RCC_LSE_DISABLE is already covered by the code section above) */
    switch (RCC_LSE)
    {
        case RCC_LSE_ENABLE:
            /* Set LSEON bit */
            *(__IO uint32_t*)RCC_BDCTRL_ADDR |= RCC_LSE_ENABLE;
            RCC_LSE_Trim_Config(LSE_Trim);
            break;
        case RCC_LSE_BYPASS:
            /* Set LSEBYP and LSEON bits */
            *(__IO uint32_t*)RCC_BDCTRL_ADDR |= (RCC_LSE_BYPASS | RCC_LSE_ENABLE);
            break;
        default:
            break;
    }
}
```

Different configuration values have a great influence on the characteristics of the final crystal. The recommended LSE configuration parameter value is 0x1FA.

1.3.2 Crystal frequency test

1.3.2.1 Crystal frequency test @ 25℃

Referring to the peripheral hardware design in Figure 1-1, select a crystal and connect an external capacitor to test the crystal frequency. The crystal signal can be output to a frequency meter or other frequency testing instruments through the MCO.

- Example：

The selected crystal load capacitance CL=7pF, and the frequency tolerance is ±20ppm. Cstray is calculated by 3pF, then C_{L1}=C_{L2}=8pF.

（The value of Cstray is related to different test board hardware, the user can fine-tune C_{L1} and C_{L2} according to the test frequency value）

Refer to Figure 1-2 for the output frequency value of the normal temperature (25℃)when the LSE configuration parameter value is 0x1FA.

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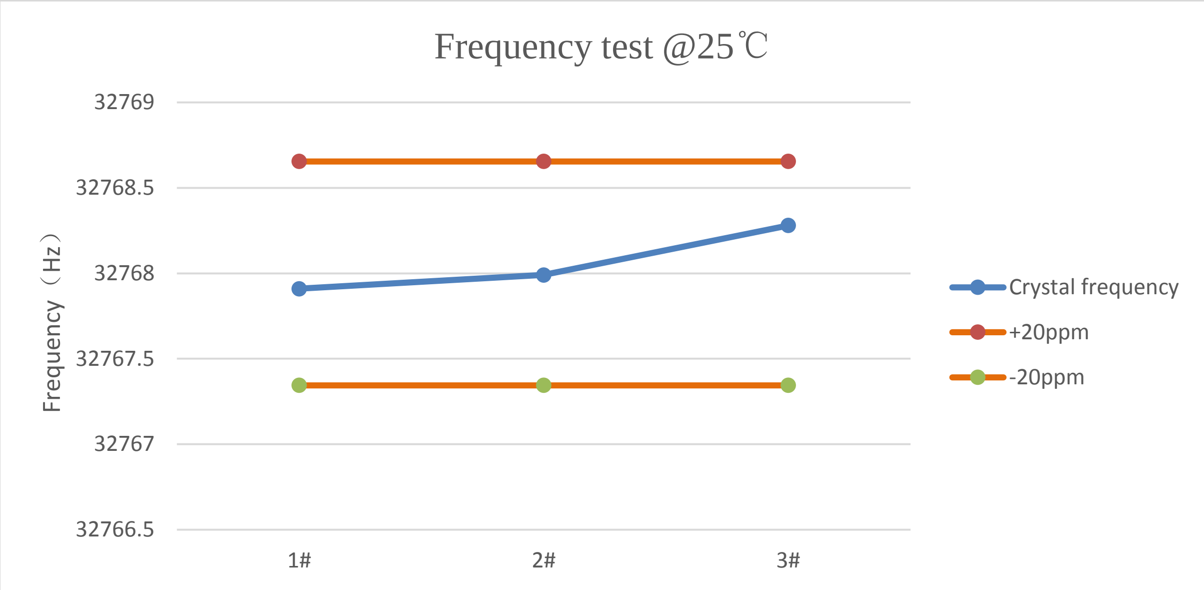

Figure 1-2 25℃， $C_{L1}=C_{L2}$=8pF， LSE configuration parameter=0x1FA, crystal output frequency

As can be seen from Figure 1-2, under normal temperature conditions, the output frequencies of the three test boards are all within ±20ppm.

1.3.2.2 Crystal frequency test @-40~85℃

Referring to Figure 1-3, for the output frequency value of the crystal operation temperature (-40~85℃)when the LSE configuration parameter value is 0x1FA.

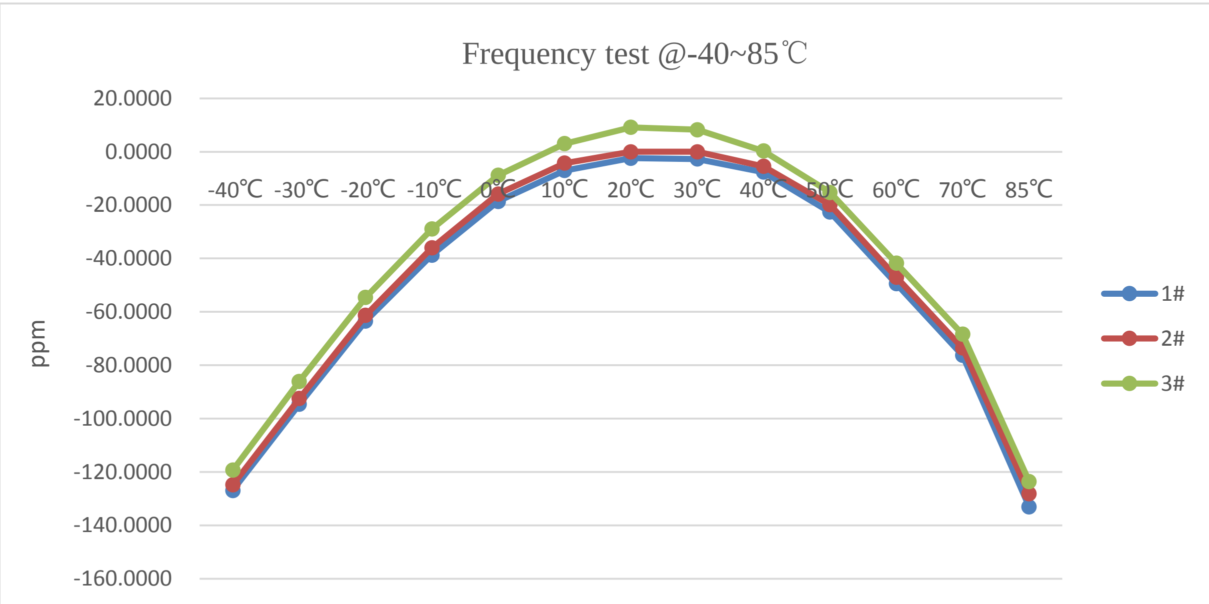

Figure 1-3 -40~85℃， $C_{L1}=C_{L2}$=8pF， LSE configuration parameter=0x1FA, crystal output frequency

1. 3. 3 Crystal Compatibility test

When selecting an external 32.768KHz crystal for the N32G430 chip, it should be noted that the selected crystal can work in the full operating temperature range。

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The LSE configuration parameters are different, and the crystal models that can be adapted are also different. Refer to Table 1-1 for the crystal full temperature test compatibility list. The LSE configuration parameter is 0x1FA.

Table 1-1 crystal compatibility list

No.	Product name/Part Number	Package	Manufacturer	CL (pF)	C0 (pF)	ESR(max) (kΩ)	Temp Range (℃)
1	TFX-04-32.768K(7PF)	1610	RIVER	7	1.3	90	-40~85
2	TFX-04-32.768K			12.5	1.3	90	
3	1TJH090DR1A0086		KDS	9	1.3	90	
4	DST1610A 32.768KHz			12.5	1.3	90	
5	X1A0001210005		EPSON	12.5	1.2	90	
6	SC-16S 32.768kHz 20PPM 12.5pF		SEIKO	12.5	1.2	90	
7	ABS06-32.768KHZ-T	2012	ABRACON	12.5		90	
8	SC-20S,32.768kHz,20PPM,7pF		SEIKO	7	1.3	90	
9	FC-12M 32.768000 kHz 7.0+20.0-20.0/X1A0000610006		EPSON	7	1.3	90	
10	TJXM32768K2TGDCNT2T		TAE	12.5		70	
11	1TJG125DR1A0019		KDS	12.5	1.3	80	
12	FC-135R 32.768KHz 9PF 20PPM/ X1A0001410002	3215	EPSON	9	1.1	50	
13	FC-135 32.768KHz 9PF 20PPM/ Q13FC13500003			9	1	70	
14	FC-135 32.768KHz 7PF 20PPM/ Q13FC13500002			7	1	70	
15	FC-135 32.768kHz 6PF 20PPM/ Q13FC1350004900			6	1	70	
16	FC-135 32.768KHz 12.5PF 20PPM/Q13FC13500004			12.5	1.2	70	
17	FC-135 32.768KHz 9PF 20PPM			9	1	70	
18	SC-32S 32.768kHz 7pF 20ppm		SEIKO	7	1	70	
19	SC-32S 32.768kHz 12.5pF 20ppm			12.5	1	70	
20	SC-32S 32.768kHz 9pF 20ppm			9	1	70	
21	SC-32S 32.768kHz 6pF 20ppm			6	1	70	
22	1TJF125DP1A000A		KDS	12.5	1.3	80	
23	SF32WK32768D71T005		TKD	7	1.1	70	
24	SF32WK32768D61T002			6	1.1	70	
25	FC31M2-32.768-NTLLLDT		HCI	12.5	1.5	70	
26	FC31M2-32.768-N09LLDT			9	1.5	70	
27	X321532768KGD2SI		YXC	12.5	1.2	70	
28	ETST00327000JE		HOSONIC	12.5	2	70	
29	TCXM32768K2NGDCZT2T		TAE	12.5	2	80	
30	XDMCZLNDDF-0.032768MHZ		TAITIEN	12.5			
31	KFC3276812520		KYX	12.5	1.2	70	

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32	F3K232768PWQAC		JYJE	12.5		70	
33	MC-146 32.768KHz 9PF 20PPM/ Q13MC14610004	MC-146	EPSON	9	0.8	65	
34	MC-146 32.768KHz 12.5PF 20PPM/Q13MC14620002			12.5	0.8	65	
35	SSP-T7-F 32.768kHz 20PPM 12.5pF		SEIKO	12.5	0.8	65	
36	FR07S4-32.768-N07LLDT		HCI	7	0.8	65	
37	FR07S4-32.768-NTLLLDT			12.5	0.8	65	
38	TSXM32768K4KGDCZT3T		TAE	12.5	0.8	65	
39	7MC32768F12UC		SJK	12.5	1.2	70	
40	M132768PWPAC		JYJE	12.5		65	
41	6LC32768F12UC	MC-306	SJK	12.5	1.2	50	
42	CD01K032768ACNBAEAE	DT26	TKD	12.5	1.4	40	-20~70
43	CD01K032768DGRBAEAE			6	1.4	40	
44	Y26003271C2040DYJY		JGHC	12.5		40	
45	X206032768KGB2SC		YXC	12.5		40	
46	WTL2T45292LZ		WTL	12.5	1.5	40	
47	7L032768NW2	MC-146	HD	12.5	0.8	65	
48	X308032768KGB2SC	DT38	YXC	12.5		40	
49	CD02K032768AEPBAEAE		TKD	12.5	1.8	30	
50	38-32.768-12.5-10/A		LIMING	12.5			
51	S3132768092070	3215	JGHC	9	1	65	-10~60
52	SMD31327681252090			12.5	1	65	
53	S3132768072070		JGHC	7	1	65	
54	DT-26-32.768K 6pF 20PPM	DT26	KDS	6	1.1	40	
55	DT-26 32.768KHz			12.5	1.1	40	
56	DT-38 32.768KHz	DT38	KDS	12.5	1.3	30	
57	Y308327681252075		JGHC	12.5	1.1	40	

Note:

1. The chip power supply voltage for the above crystal compatibility test is VDD=3.3V.
2. If the crystal model used is not in the compatibility list, please contact Nations Technologies Inc.

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2. Version history

Version	Date	Modify
V1.0	2022-05-19	Initial version.

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