Design guide

N32G430 series hardware design guide

Introduction

This document details the hardware design checklist for N32G430 series MCUs to provide users with hardware design guidance.

CONTENS

1. N32G430 Series MCU Hardware Design Checklist

1.1 Introduction to Power Supply

The operating voltage (VDD) of N32G430 series chips is 2.4V~3.6V. Mainly: VDD, VDDA pins. For details, please refer to the relevant datasheet.

1.2 VDD power supply scheme

VDD is the main power supply of MCU, which must be powered by a stable external power supply, the voltage range is 2.4V~3.6V, all VDD pins need to place a 0.1uF decoupling capacitor nearby, and one VDD pin needs to add a 4.7uF decoupling capacitors. For the specific design of the decoupling capacitor, please refer to the reference design schematic diagram of the minimum system of each package in Chapter 3.

VDDA is an analog power supply, which provides power for analog modules such as ADC and COMP. It is recommended to place a 0.1uF and a 1uF capacitor on the VDDA input pin.

1.3 External pin reset circuit

A system reset occurs when a low level (external reset) occurs on the NRST pin. The external NRST pin reset reference circuit is as follows.
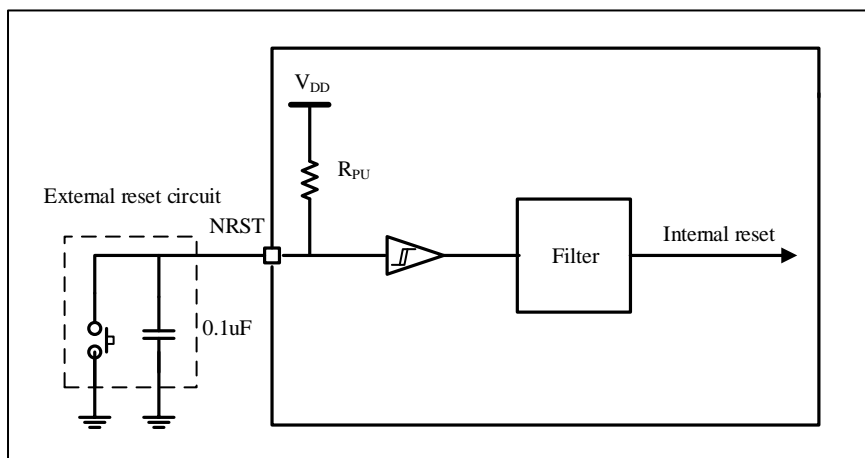
Figure 1-1 System reset diagram

Note: The reset pin NRST cannot be left floating during design, and the external capacitor 0.1uF is given as a typical reference value. If the reset time needs to be accelerated, the NRST pin can be pulled up externally, and the typical value of the pull-up resistor is 10K. In addition, the user can decide whether to add a reset button according to the actual needs of the product

1.4 External clock circuit

N32G430 series MCU contains 2 external clocks: external high-speed clock HSE (4MHz~32MHz) and external low-speed clock LSE (usually 32.768KHz).

HSE and LSE configure the corresponding load capacitance according to the characteristics of the crystal oscillator. For details, please refer to the description of the external clock characteristics in the relevant datasheet.

1.5 Boot Pin Connection

The figure below shows the external connections required for the N32G430 series chip to select the boot memory. Please refer to the relevant section of the datasheet for the startup mode.
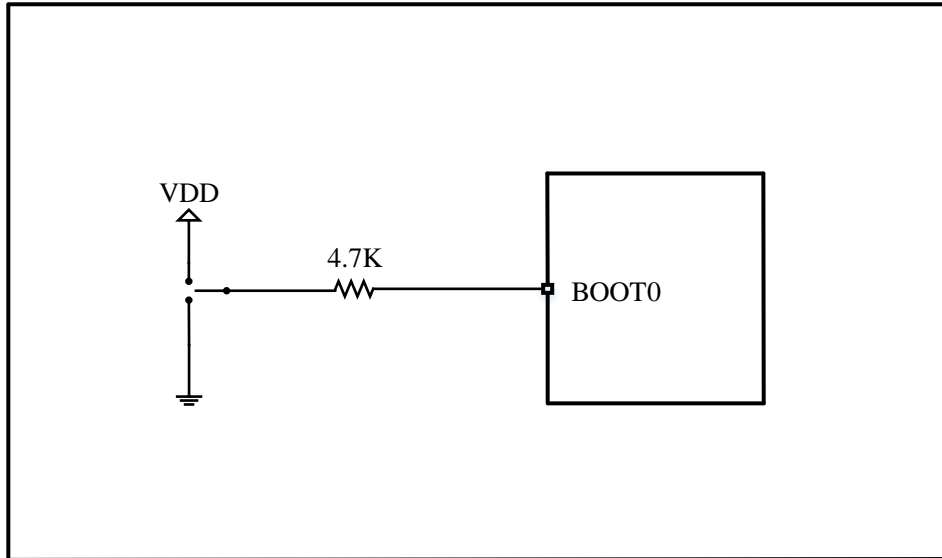

Figure 1-2 Implementation example of startup mode

The BOOT pin is pulled high, and the chip is started from the BOOT area after reset; the BOOT pin is pulled low, and the chip is started from the user area after reset.

Note: The resistance values in the figure are given as typical reference values only.

1.6 Independent ADC Converter

In order to improve the conversion accuracy, the ADC has a pair of independent power supplies, an independent VDDA pin powers the ADC, and the VSSA pin is used as the ground terminal of the analog power supply. It can be separately filtered and shielded from noise on the PCB to power the ADC.

Regarding the ADC circuit design, please pay attention to the following points:

1）When using ADC sampling, it is recommended to shorten the external wiring distance;

2）It is recommended to keep away from some high frequency inversion signals around the input signal of ADC;

3）Note the maximum supported rates for slow and fast channels:

The sampling rate of the ADC fast channel should not exceed 4.7Msps, and the sampling rate of the ADC slow channel should not exceed 2.5Msps;

4）During ADC conversion, the chip does not support modifying the ADC configuration. If you need to

modify the configuration, you need to wait for the current conversion to end or turn off the ADC before configuring;

5）When a certain ADC channel is used, negative voltage (such as -0.2V) cannot be applied to other unused ADC sampling channels. If this negative voltage is applied, the voltage of the normally sampled ADC channel will be pulled down, resulting in sampling. data is inaccurate;

6）When using ADC, the maximum value of RAIN cannot be too large, and it needs to comply with the following formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$
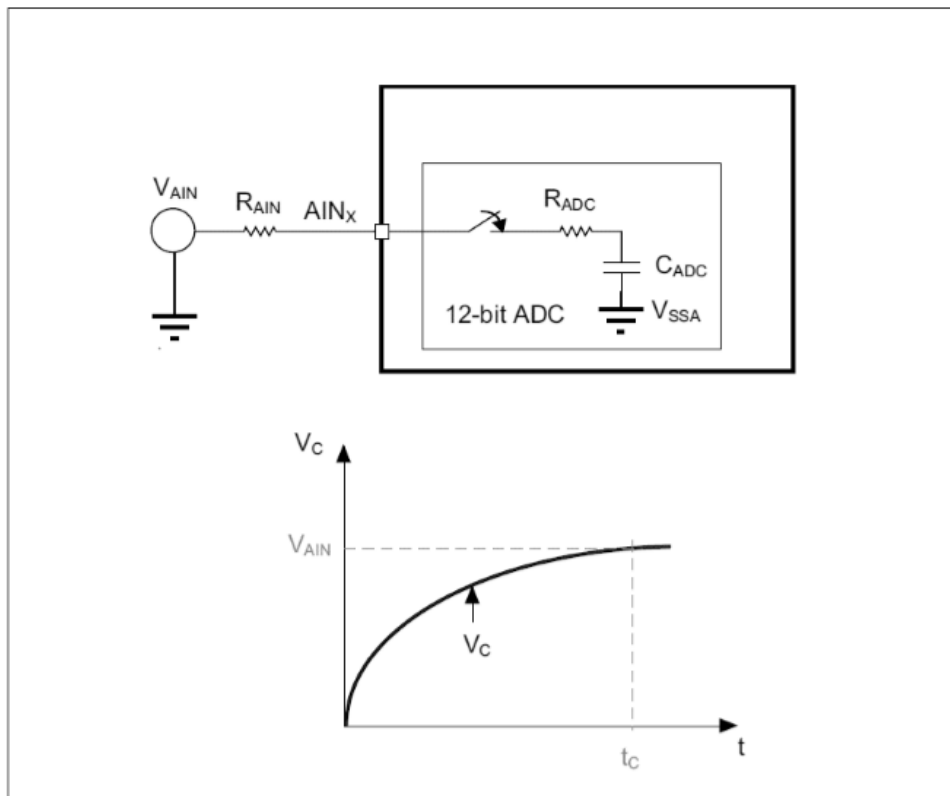
Figure 1-3 Influence of series resistance of ADC input port

Input	Resolution	Rin (kΩ)	Min sampling time （ns）	Input	Resolution	Rin (kΩ)	Min sampling time （ns）
fast channel	12-bit	0	31.1	slow channel	12-bit	0	48.1
		0.05	34.9			0.05	52.0
		0.1	38.8			0.1	55.9
		0.2	46.6			0.2	63.7
		0.5	69.9			0.5	86.9
		1	108.7			1	125.8
		10	807.4			10	824.5
		20	1583.7			20	1600.8
		50	3912.7			50	3929.8
		100	7794.3			100	7811.4
fast channel	10-bit	0	26.6	slow channel	10-bit	0	41.3
		0.05	29.9			0.05	44.6
		0.1	33.3			0.1	47.9
		0.2	39.9			0.2	54.6
		0.5	59.9			0.5	74.5
		1	93.2			1	107.8
		10	692.0			10	706.7
		20	1357.5			20	1372.1
		50	3353.7			50	3368.4
		100	6680.8			100	6695.5
fast channel	8-bit	0	22.2	slow channel	8-bit	0	34.4
		0.05	25.0			0.05	37.2
		0.1	27.7			0.1	39.9
		0.2	33.3			0.2	45.5
		0.5	49.9			0.5	62.1
		1	77.6			1	89.8
		10	576.7			10	588.9
		20	1131.2			20	1143.4
		50	2794.8			50	2807.0
		100	5567.4			100	5579.6
fast channel	6-bit	0	17.7	slow channel	6-bit	0	27.5
		0.05	20.0			0.05	29.7
		0.1	22.2			0.1	31.9
		0.2	26.6			0.2	36.4
		0.5	39.9			0.5	49.7
		1	62.1			1	71.9
		10	461.4			10	471.1
		20	905.0			20	914.7
		50	2235.8			50	2245.6
		100	4453.9			100	4463.6

Figure 1-4 ADC sampling schedule

1.7 IO power-on pulse processing

During the power-on process, because the IO is in a high-impedance state and the internal circuit coupling characteristics, a high-level pulse will appear on the IO at the moment of power-on (the actual high-pulse voltage value should be measured by the user). If the pulse will affect its application, it is recommended to add an appropriate capacitor (1nF~100nF) or an appropriate pull-down resistor (10K~100K) on the corresponding IO.

The following picture shows the waveform of IO (PA9) during the power-on process of the development board N32G430C8L7-STB 1.0:

Figure 1-5 IO (PA9) waveform during power-on

The following figure shows the waveform of the development board N32G430C8L7-STB 1.0 after the IO (PA9) is added with a 10K pull-down resistor during the power-on process:
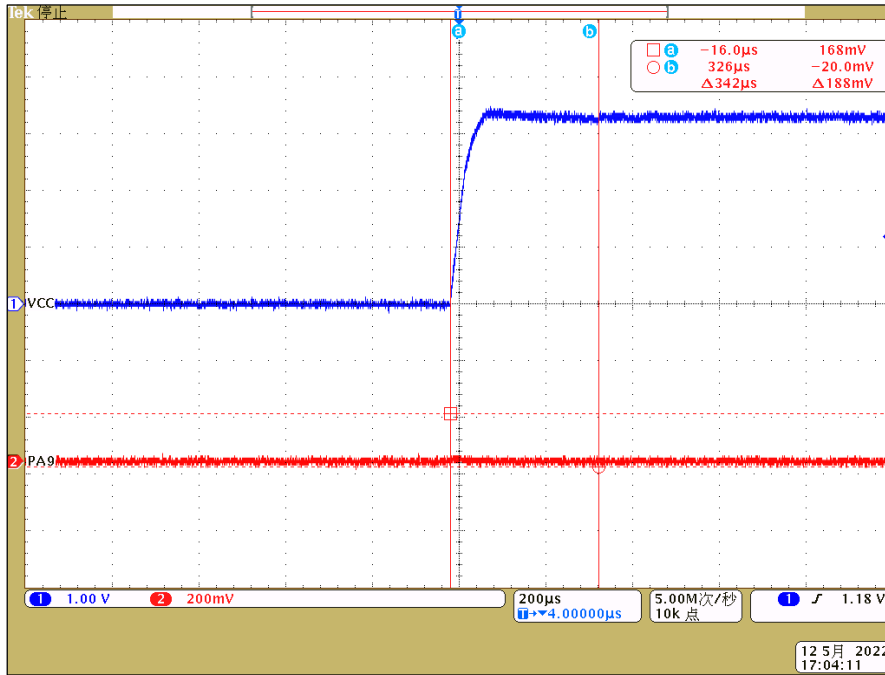
Figure 1-6 Waveform after IO (PA9) plus pull-down resistor during power-on process

1.8 IO withstand voltage

When using the chip, please pay attention to the withstand voltage value of each IO. In the I/O column defined by pin multiplexing in the datasheet, mark FT: 5V tolerant IO.

TSSOP20	QFN20	QFN28	QFN32 LQFP32	QFN48 LQFP48	Pin name (function after reset)	Type[1]	I/O[2]	Fail-safe[5]	Alternate functions[3]	Additional functions
-	-	-	1	1	VDD	S	-	-	-	-
-	-	-	-	2	PC13_TAMPER-RTC[4]	I/O	FT	Y	TIM1_CH1N EVENTOUT	RTC-TAMP1 RTC_OUT WKUP2
-	1	-	-	3	PC14-OSC32_IN[4]	I/O	FT	Y	-	OSC32_IN
-	2	-	-	4	PC15-OSC32_OUT[4]	I/O	FT	Y	-	OSC32_OUT

Figure 1-7 I/O structure defined by pin multiplexing in the datasheet

Note: FT: 5V tolerant IO; when using the chip, pay attention to the impact of signals higher than 5V on IO.

1.9 Anti-static design

1.9.1 PCB Design

For the PCB design of ordinary two-layer boards, it is recommended to do wrapping around the signal lines, and try to cover the edges of the PCB as much as possible. If the cost allows, it can be designed with a four-layer board or a multi-layer board. In a multi-layer PCB, the ground plane acts as an important charge source, which can offset the charge on the electrostatic discharge source, which is conducive to reducing the electrostatic field band. The ground

plane of the PCB can also be used as a shield for the signal line (of course, the larger the opening of the ground plane, the lower the shielding effectiveness). In addition, if a discharge occurs, since the ground plane of the PCB board is large, the charge is easily injected into the ground plane, rather than into the signal line. This will help protect the component, because the charge can be drained before causing component damage.

1.9.2 ESD Protection Devices

In the actual product design, the chip itself has a certain anti-static ability. The static level of N32G430 series MCU ESD (HBM) mode is +/-4KV, but if there is a higher ESD protection level requirement, and the pins of the chip need Direct external connection is used as the output or input port of the product. At this time, the pins of the chip are directly exposed to the outermost part of the product, and cannot be isolated by laying the ground or other means. Under this condition, it is generally necessary to consider an external ESD protection device. TVS diode is a typical ESD protection device. The following is an example of a typical connection method.
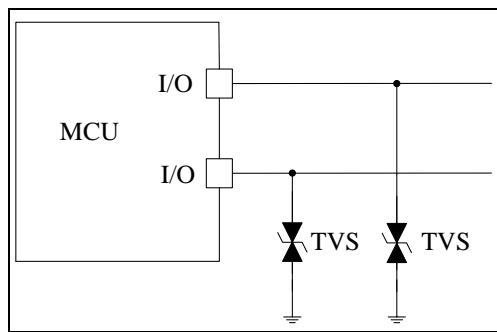
Figure 1-8 TVS connection on I/O pins

1.10 Debug Interface

N32G430 series chips support serial interface (SWD) and JTAG debug interface, please refer to the relevant user manual for detailed application.

Debug Signal	GPIO Pins
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
JNTRST	PB4

Table 1-1 Debug Interface

1.11 BOOT serial interface

N32G430 series chips support BOOT serial communication. The serial interface is as follows:

BOOT Serial Port	GPIO Pins
USART1_TX	PA9
USART1_RX	PA10

Table 1-2 Serial port interface

2. Overall Design Suggestions

1）Printed circuit board

It is recommended to use a multi-layer printed circuit board with a dedicated independent ground plane (VSS) and a dedicated independent power supply plane (VDD), which can provide good coupling performance and shielding effect. In practical applications, if a multi-layer printed circuit board cannot be used considering the economical reason, a good grounding and power supply structure must be ensured when designing the circuit.

2）Component layout

In PCB design, different circuits need to be laid out separately according to the different effects of each device on EMI. For example, high-current circuits, low-voltage circuits, and high-frequency devices. Thereby reducing cross-coupling on the PCB.

3）ground and Power (VSS, VDD)

Each module (analog circuit, digital circuit, low-sensitivity circuit) should be grounded separately, the digital ground and the analog ground should be separated, and all the grounds should be connected together at one point eventually. According to the size of the printed circuit board current, try to increase the width of the power line to reduce the loop resistance. At the same time, the direction of the power wire and the ground wire and the direction of the current should be as consistent as possible, and the power supply should be as close to the ground wire as possible to reduce the area of the loop. This helps to enhance noise immunity. The area on the PCB without devices needs to be filled with ground to provide good shielding effect.

4）Decoupling

All power pins need to be properly connected to power. These connections, including pads, wires, and vias, should have as low impedance as possible. The method of increasing the wiring width is usually adopted, and decoupling capacitors must be placed close to the chip for each pair of VDD and VSS pins. The figure below shows a typical layout of the power/ground pins.
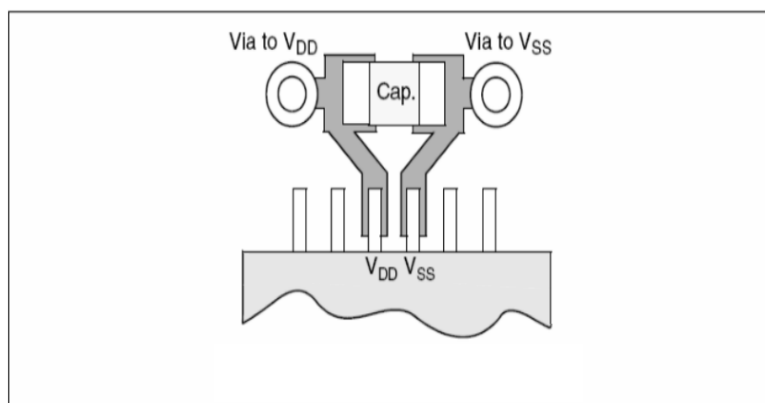
Figure 2-1 Typical layout of VDD/VSS pins

3. Minimum System Reference Design Schematic

3.1 LQFP48
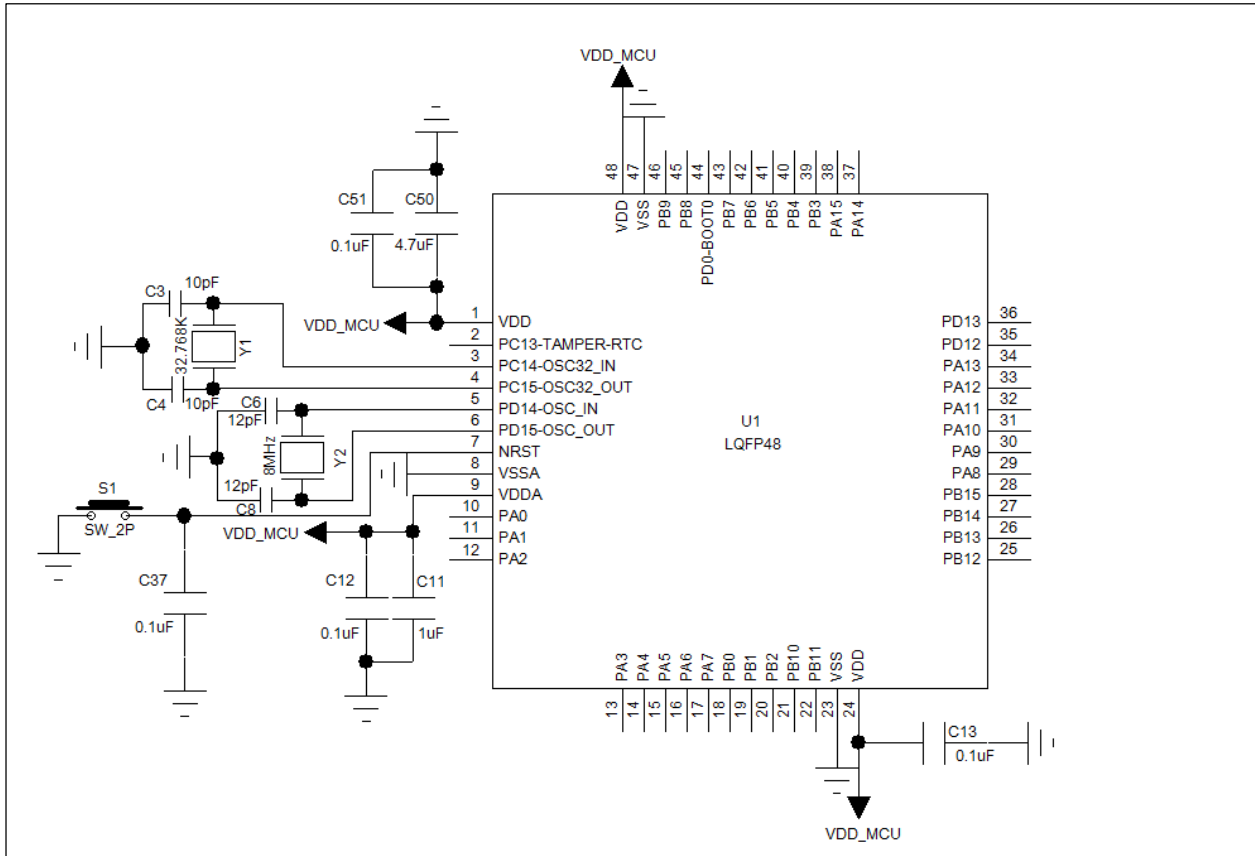
Figure 3-1 N32G430 Series LQFP48 Package Minimum System Reference Design Schematic

3.2 LQFP32
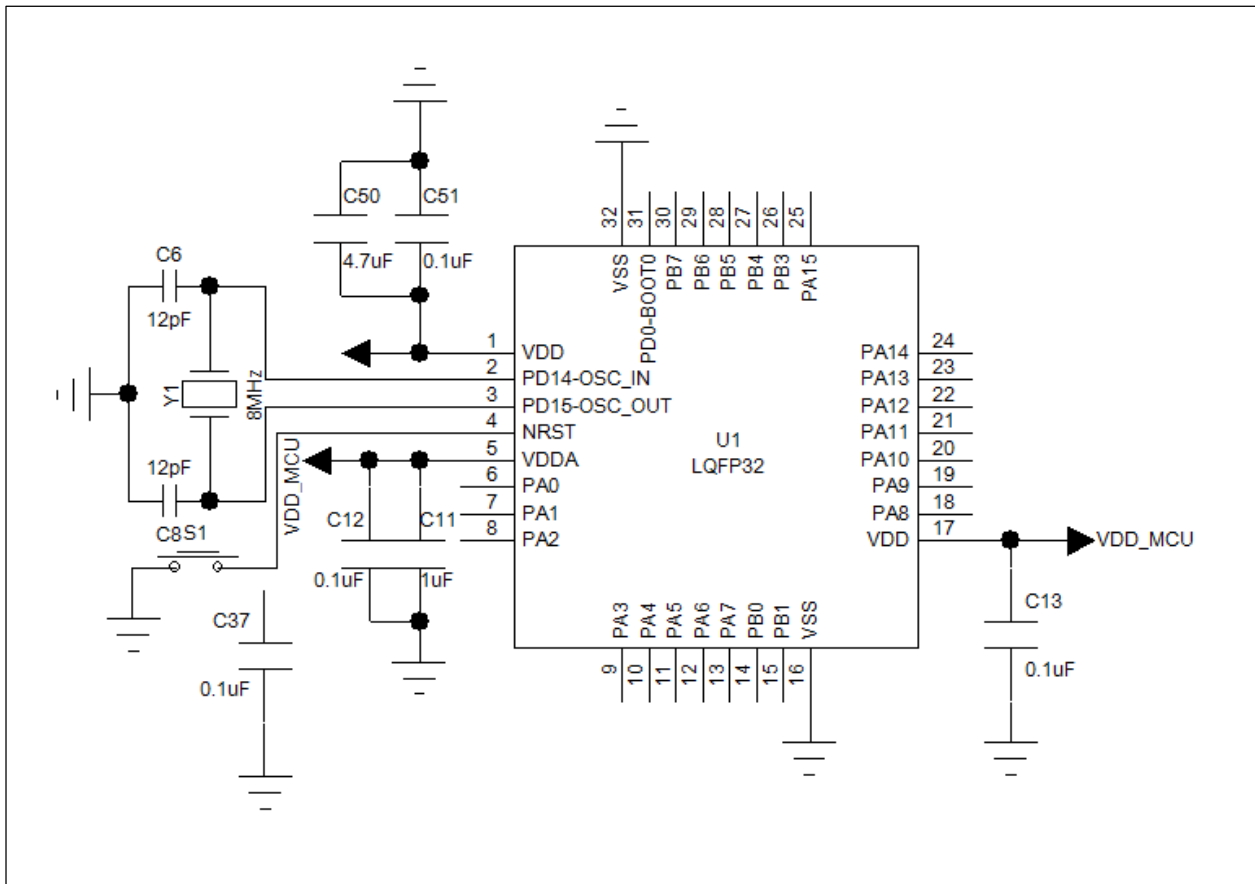
Figure 3-2 N32G430 Series LQFP32 Package Minimum System Reference Design Schematic

3.3 QFN20
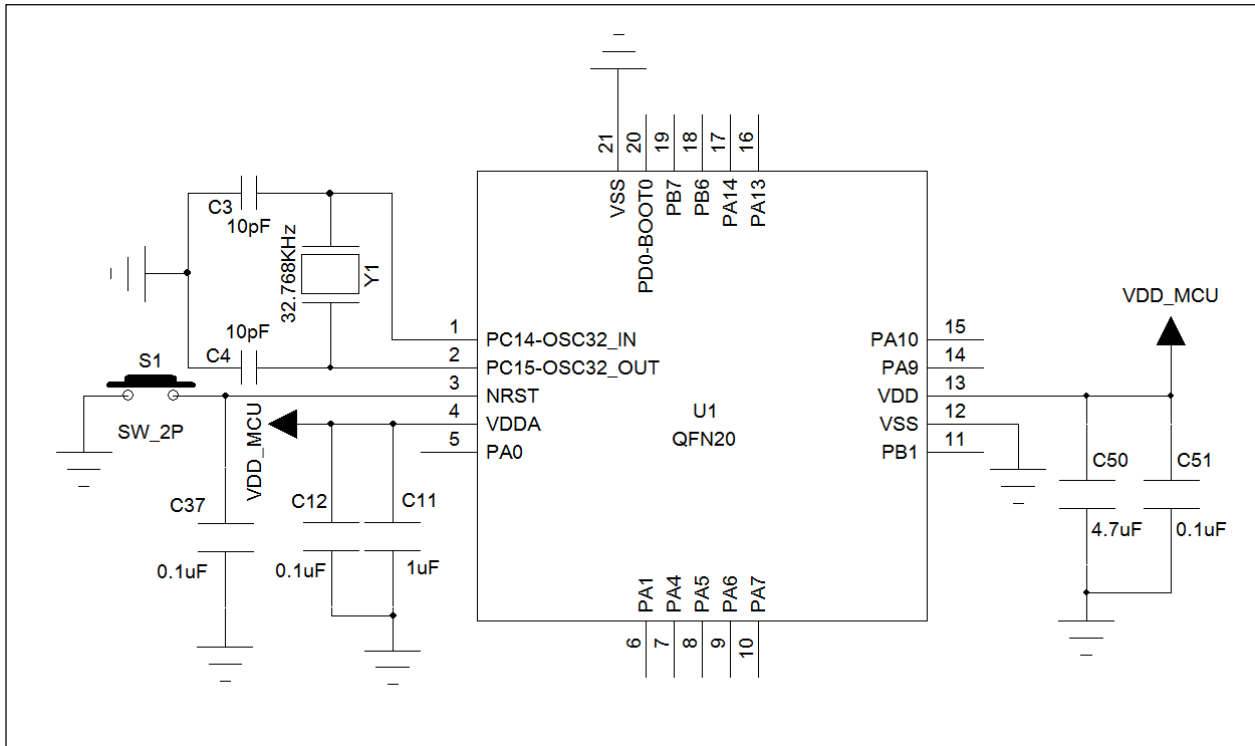
Figure 3-3 N32G430 Series QFN20 Package Minimum System Reference Design Schematic

3.4 QFN28
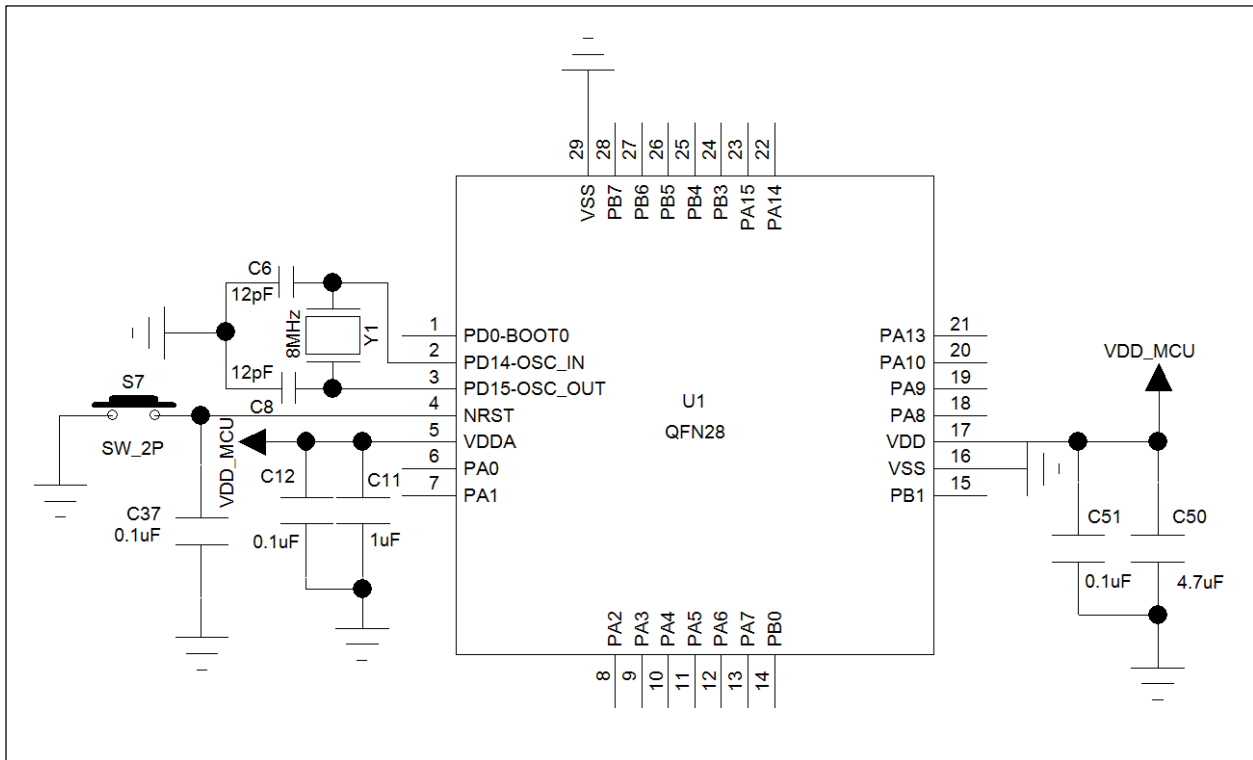
Figure 3-4 N32G430 Series QFN28 Package Minimum System Reference Design Schematic

3.5 QFN32
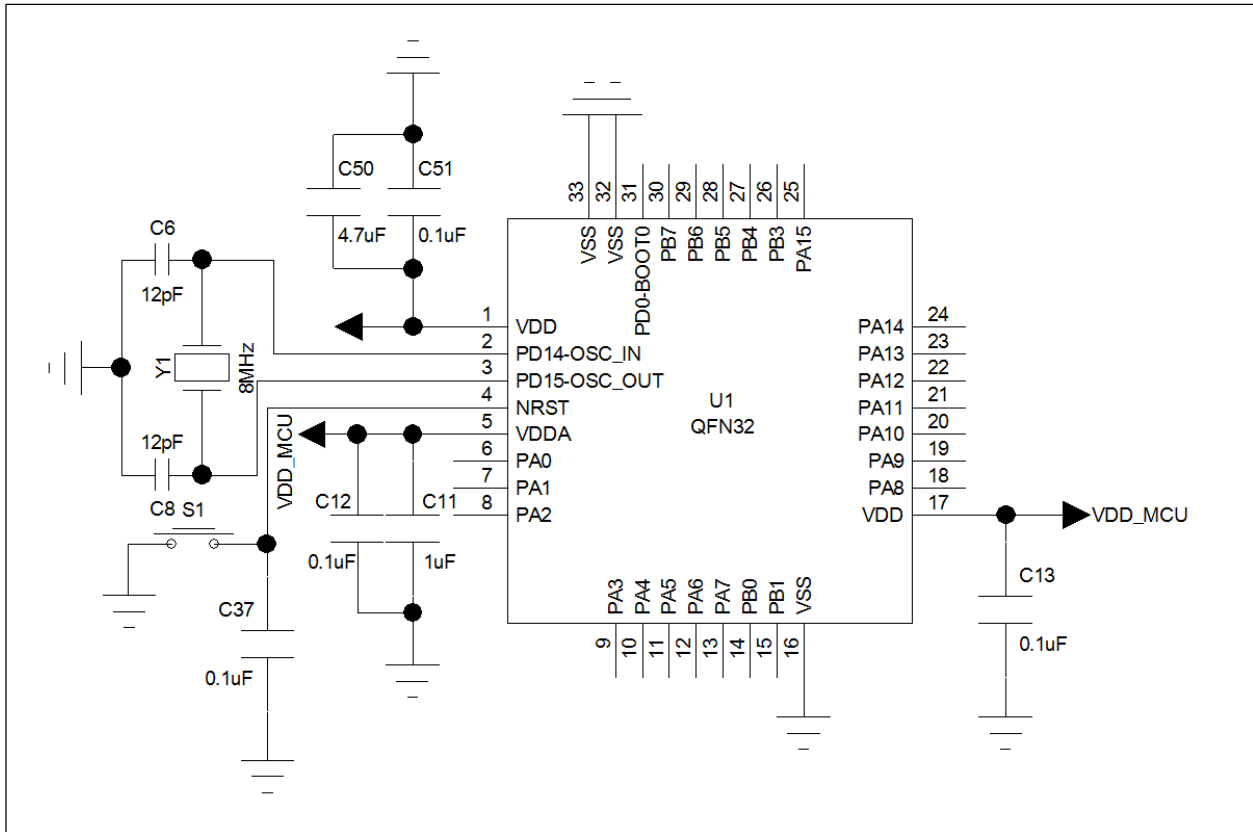
Figure 3-5 N32G430 Series QFN32 Package Minimum System Reference Design Schematic

3.6 QFN48
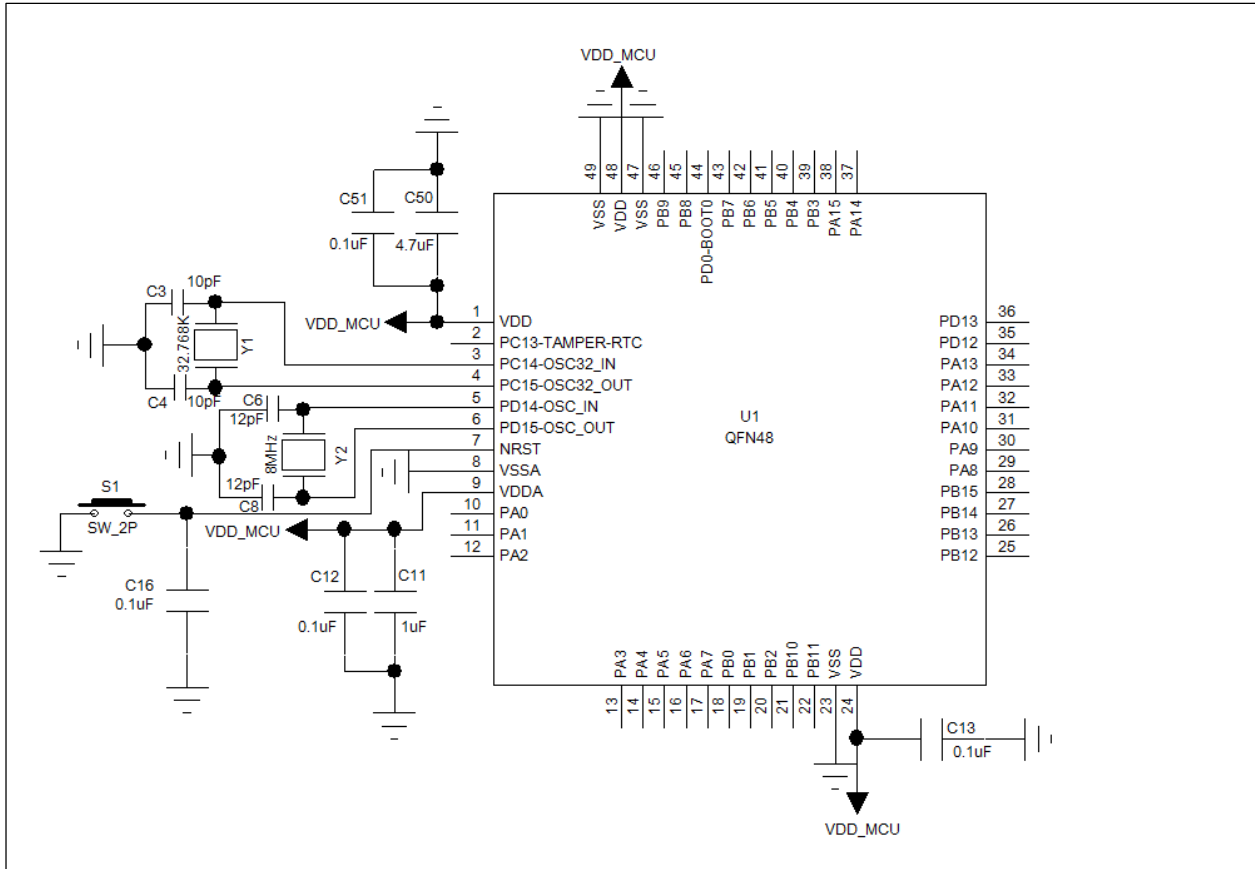
Figure 3-6 N32G430 Series QFN48 Package Minimum System Reference Design Schematic

3.7 TSSOP20
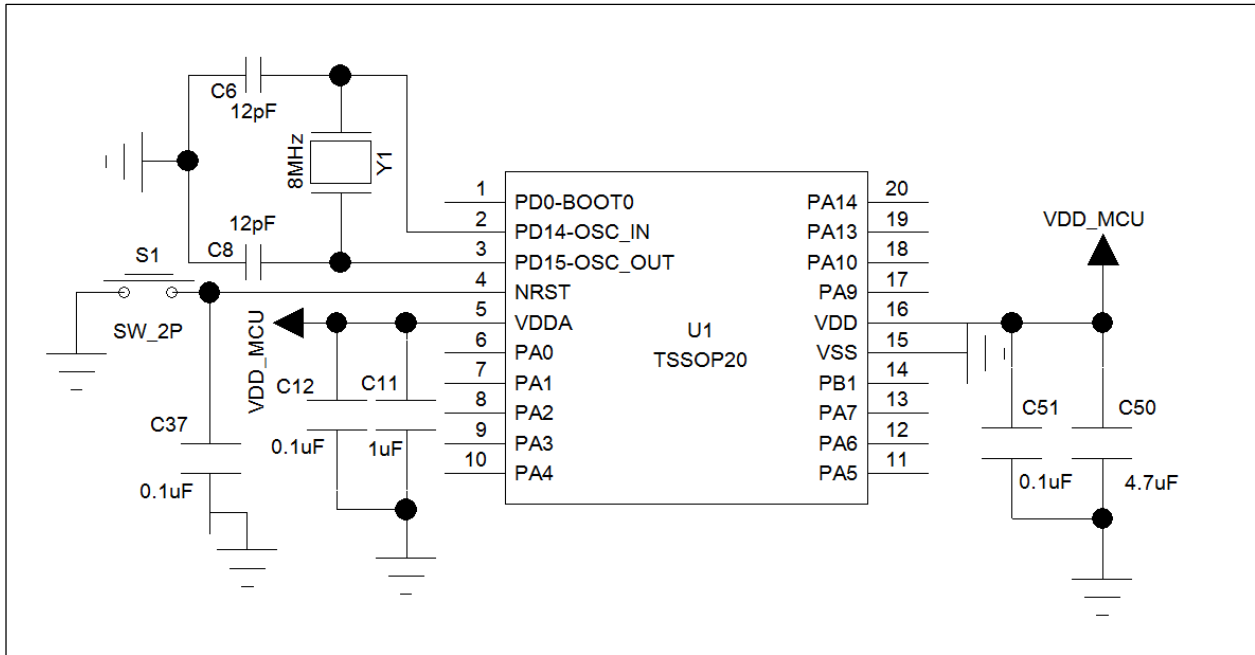
Figure 3-7 N32G430 Series TSSOP20 Package Minimum System Reference Design Schematic

Figure 3-1 to Figure 3-7 are the schematic diagrams of the minimum system reference design of each package of the N32G430 series, which mainly reflect the design of power supply decoupling capacitors, clocks, reset circuits, etc. The clock circuit depends on the user's design, and the chip supports internal high-speed and low-speed clocks available to the user for selection.

4. PCB LAYOUT Reference
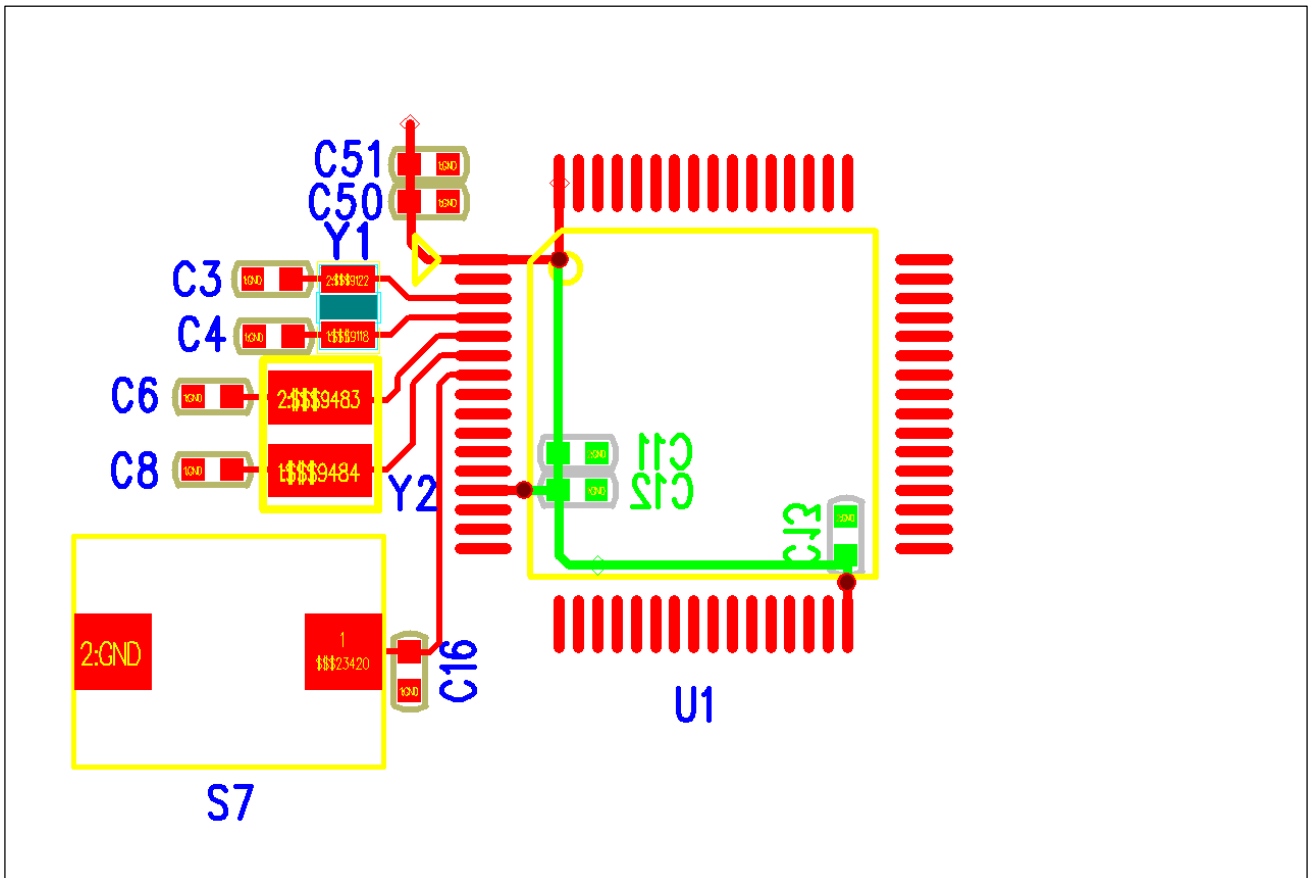
Figure 4-1 N32G430 series PCB LAYOUT reference diagram

During PCB LAYOUT design, decoupling capacitors need to be placed near each power pin. The external crystals and traces of the HSE and LSE should be grounded as much as possible. The area below the crystals close to the crystals also needs to be grounded, and no signal lines can pass through them to prevent the signal lines from interfering with the crystal signals.

5. Typical failure analysis

The common problems and analysis methods encountered by customers in the process of using the chip are described as follows.

5.1.1 Short circuit between power pins and ground

Problem Description:

The VDD pin of the chip is short-circuited with the GND test, and the chip is abnormally hot after power-on.

Problem check:

1) Whether the VDD decoupling capacitor has insufficient withstand voltage to cause the capacitor to break down and short circuit.

2) When the product starts up, whether the VDD voltage exceeds the specified maximum value.

3) Whether there is an overshoot voltage exceeding the maximum value of VDD during the operation of the product.

4) In the process of production and use, whether there is static electricity that causes chip damage.

5.1.2 GPIO damage

Problem Description:

The chip GPIO cannot output a high level or a low level normally, the GPIO is used as an input to detect the level error, the VIH or VIL test value is abnormal, and the pin impedance is abnormal.

Problem check:

1) Whether the external input voltage to the chip GPIO exceeds the maximum value, such as the 5V-tolerant I/O input voltage exceeding 5V.

2) In the process of product production and testing, whether there is a high voltage input to the GPIO port.

3) In product design, whether there is a high-voltage signal near the GPIO trace coupled to the GPIO input port.

4) In the process of production and use, whether there is static electricity that causes chip damage.

5.1.3 ADC sampling inaccurate

Problem Description:

When sampling the voltage at the ADC input port of the chip, the sampling voltage is inaccurate.

Problem check:

Refer to Section 1.6 to confirm whether the hardware and software settings meet the requirements of ADC

considerations.

6. Version history

Version	Date	Modify
V1.0	2022-4-6	Initial version

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