N32G031x Series Errata Sheet

V1.1

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2 RCC

2.1 LSE is affected by toggling of adjacent pins

Description

LSE is affected by toggling of adjacent pins.

Resolution

Avoid toggling of adjacent pins of LSE

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3 GPIO and AFIO

3.1 GPIO analog function

Description

When the 4 GPIOs PA1/PA2/PA3/PA4 are in the high-level output state, when they switch to the analog function, there will be a short output voltage drop of about 30mv during the switching process.

Resolution

Avoid the above methods of use.

3.2 IO reverse current

Description

If the IO that does not support failsafe is powered on before VDD, an exception may occur at this time, and the external pin reset cannot return to normal after the exception.

Resolution

It is recommended that customers use the power-on of VDD prior to the power-on of IO.

4 ADC

4.1 When the injection channel is triggered, the regular channel is also triggered

Description

The ADC converts continuously, and the external trigger of the regular channel is disabled. When the software or hardware trigger injection channel conversion, the regular channel may be converted, and the corresponding status bit of the regular channel conversion will be set.

Resolution

Ignore the status bit and data generated by the regular channel.

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5 SPI&I2S

5.1 SPI

5.1.1 SPI baud rate setting

Description

In SPI master mode and the CRC check function is enabled, when the SPI clock frequency is greater than 14MHz, the CRC check is abnormal.

Resolution

In SPI master mode and CRC check function is enabled, the SPI clock frequency is not greater than 14MHz.

5.1.2 Slave mode CRC check

Description

SPI works in slave mode and CRC check has been enabled, even if the NSS pin is high level, as long as the SPI receives the clock signal, the CRC calculation will still be performed

Resolution

Before using the CRC check, clear the CRC data register so that the CRC check of the master and slave devices can be synchronized

The steps to clear are as follows：

1. SPI enable bit reset (set 0)
2. CRC check bit reset (set 0)
3. CRC check bit set (set 1)
4. SPI enable bit set (set 1)

5.2 I2S

5.2.1 PCM long frame mode

Description

When I2S works in master mode, PCM long frame mode, and the data format is "32bit" or "16bit extended to 32bit", the WS signal is one cycle per 16bit instead of 32bit.

Resolution

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When I2S is the master mode and the long frame mode must be used, the 16bit data mode should be used.

6 I2C

6.1 A software event that must be managed before the current byte is transferred.

Description

When EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3 events occur, the events must be processed before the current byte is transferred, otherwise there may be a problem of reading an extra byte, reading duplicate data, or losing data. If the software does not read the N-1th byte before the stop signal is generated, the Nth byte in the shift register is corrupted (shifted one bit to the left).

Resolution

1. When using I2C to transfer more than one byte, try to use DMA mode
2. When using I2C interrupt, adjust the interrupt priority to the highest priority of the application
3. When the read data reaches the N-1th byte:
   a) Detect BSF as 1
   b) Configure SCL as GPIO open-drain output and set it to 0
   c) Set STOPGEN as 1
   d) Read the N-1th byte
   e) Configure SCL as I2C multiplexing function open-drain output mode
   f) read the last byte

6.2 Attentions when reading a single byte at time

Description

In the master read mode, when the length of the read byte is a single byte, a read data error may occur.

Resolution

When read single byte：

a) After receive ADDRF
b) Set ACKEN bit as 0
c) Clear ADDRF bit（Cleared by reading STS1 and then STS2）

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d) Set STOPGEN as 1

e) Read last byte。

7 USART

7.1 Parity error flag

Description

During the reception of one byte of data, before the stop bit is received, a parity error is detected, and the parity error flag is set. During this period, the parity error flag cannot be cleared by software (reading the status register and then reading the data register). If the parity error interrupt is enabled, the parity error interrupt handler will be entered multiple times.

Resolution

After the read data buffer flag is set, after receiving the data, the operation of clearing the parity error flag is performed. If the parity error interrupt is enabled, in order to avoid entering the interrupt processing function multiple times, when the parity error interrupt is entered for the first time, the parity error interrupt is turned off, and after the data is received, the parity error interrupt is turned on again.

7.2 RTS hardware flow control

Description

Enable RTS hardware flow control. When the USART receives data, the RTS signal will be automatically pulled high. If the byte data is not read from the data register in time, and a new byte is sent to the USART (violating the flow control protocol), the RTS signal will be pulled low again. USART waits again to receive the next frame of data.

Resolution

Before the next new data is received, the data is read out from the data register in time.

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8 TIM

8.1 TIM overcapture

Description

When reading the capture data register data (under normal circumstances, the read data register operation will cause the capture flag to be cleared), a trigger capture is generated externally, even if the previous capture has been correctly read and the new capture data is also is sent to the register exactly, but the overcapture flag is still detected. The system is critical for overcapture, but no capture data is lost.

Resolution

None

8.2 ADTIM and GPTIM cannot generate compare events under certain circumstances

Description

In edge-aligned mode, in up-counting PWM1 mode, when the current PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the next PWM cycle is 0. At the moment when the PWM cycle counter is 0, although the counter value = CCDATx shadow register value = 0 and OCxREF = 0, but still no compare event is generated.

Resolution

If it is not required that "the compare event is generated at the time when the counter value = CCDATx shadow register value =0", the compare event generated through another channel can replace the compare event that is not generated.

9 RTC

9.1 RTC subsecond match

Description

The RTC programmable alarm clock function does not enable matching of date, hour, minute and second, but only enables matching of sub-seconds (that is, an alarm interrupt is generated when sub-seconds match in every second). The alarm interrupt cannot be generated in the first sub-second match after the alarm function is enabled, and the alarm interrupt is generated for each sub-second match after that.

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Resolution

None

9.2 RTC second match

Description

When the alarm clock configuration second matches, the chip enters the SLEEP mode. When the alarm interrupt is generated to wake up the chip from SLEEP, and the interrupt processing function is executed (only the operation of clearing the interrupt flag bit is performed), it immediately enters the STOP mode. The next alarm interrupt cannot wake the chip from STOP mode.

Resolution

Before setting the RTC time, you need to enter the RTC initialization mode. Before entering the RTC initialization mode, you need to wait for the value of the sub-second register to be less than the synchronous prescaler value and cannot be 0.

9.3 RTC calendar function cannot be initialized multiple times within 1 second

Description

The RTC calendar function is initialized multiple times within 1 second, so that the RTC alarm clock interrupt cannot be generated.

Resolution

The interval between two initializations of the RTC calendar function is more than 1 second.

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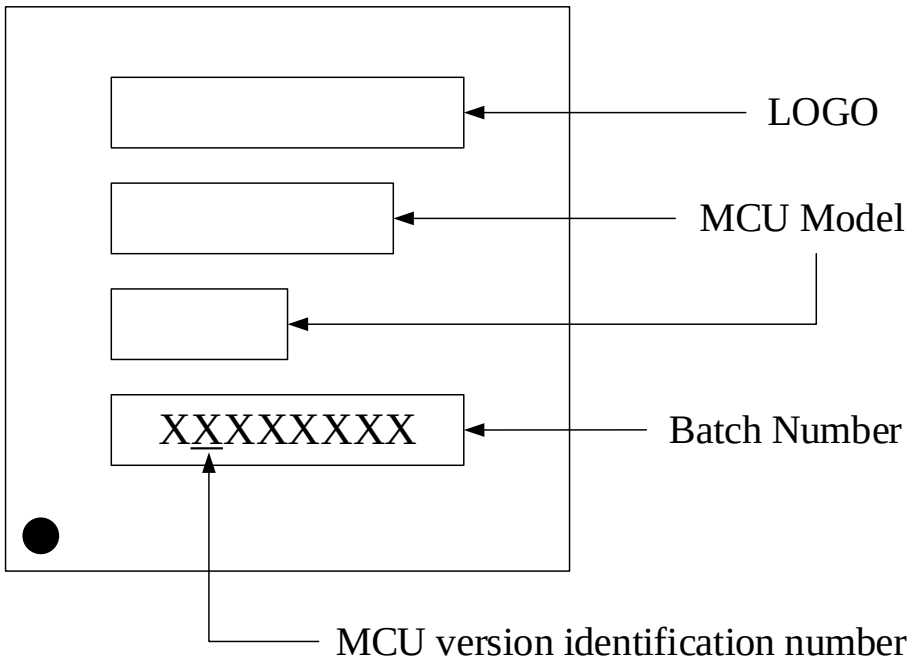
10 Marking information



11 Version history

Date	Version	Description
2022.6.14	V1.1	Initial version

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