

N32L40xx8/xB

Product Brief

N32L40x series uses 32-bit ARM Cortex-M4F core, maximum working frequency 64MHz, support floating point operation and DSP instructions, integrated up to 128KB embedded encryption Flash, 24KB SRAM, integrated with rich high-performance analog interface, Built-in one 12bit 4.5Msps ADC, two independent rail-to-rail operational amplifiers, two high-speed comparators, one 1Msps 12bit DAC, Integrated multi-channel U(S)ART, I2C, SPI, USB, CAN and other digital communication interfaces, Segment LCD Driver Interface ,built-in password algorithm hardware acceleration engine

Main features

- **CPU core**
 - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply and divide instructions, support DSP instructions and MPU.
 - Built-in 2KB instruction Cache, support Flash acceleration unit execution program 0 wait
 - The highest frequency is 64MHz, 80DMIPS
- **Cryptographic memory**
 - Up to 128KByte in-chip Flash, support encrypted storage, partition management and data protection, support hardware ECC verification, 100,000 erasing times, 10 years of data retention
 - Up to 24KByte in-chip SRAM, including 16Kbyte SRAM1(Stop2 mode can be configured as retention) and 8 Kbyte SRAM2(both Standby and Stop2 modes can be configured as retention), supporting hardware parity check
- **Low power management**
 - Support Run, Sleep, LP Run, LP Sleep, Stop2, Standby mode
- **High-performance analog interface**
 - One 12bit 4.5Msps ADC with a variety of precision configurable, sampling rate up to 8Msps in 6bit mode, up to 16 external single-ended input channels, supporting differential mode
 - Two rail-to-rail operational amplifiers with built-in programmable gain amplifier up to 32 times
 - Two high-speed analog comparators with built-in 64-level adjustable comparison reference, COMP1 support working in STOP2 mode
 - One 12bit DAC, sampling rate 1Msps
 - Internal 2.048V independent reference voltage reference source
 - All analog interfaces support full voltage from 1.8 to 3.6V
- **Clock**
 - 4MHz~32MHz external high-speed crystal
 - 32.768KHz External low-speed crystal
 - Internal high-speed RC(HSI) 16MHz
 - Internal multi-speed RC(MSI) 100K~4MHz
 - Internal low-speed RC(LSI) 40KHz
 - Built-in high-speed PLL
 - Supports one clock output, which can be configured as low-speed or high-speed clock output
- **Reset**

- Support power-on, brown-out, and external pin reset
- Support watchdog reset, software reset
- **Support up to 64 GPIOs.**
- **Communication interface**
 - Five U(S)ART interfaces, including three USART interfaces (support 1xISO7816, 1xIrDA, LIN) and two UART interfaces
 - One LPUART, support STOP2 to wake up MCU in low power consumption state
 - Two SPI interfaces, the rate is up to 16 Mbps, support I2S communication
 - Two I2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
 - One USB2.0 FS Device interface
 - One CAN 2.0A/B bus interface
- **Segment LCD driver interface**
 - Supports up to 320 segments (8x40) or 176 segments (4x44) monochrome passive LCD display
 - Flexible LCD refresh rate support (30~102Hz)
 - Support static, 1/2, 1/3, 1/4, 1/8 duty cycle
 - Support static, 1/2, 1/3, 1/4 bias
 - Support normal display in Stop2 mode
- **One high-speed DMA controller, each controller supports 8 channels, channel source address and destination address can be configured arbitrarily**
- **RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **Timer counter**
 - Two 16bit advanced timer counters, support input capture, complementary output, quadrature encoding input, the highest control accuracy is 9.25ns, each timer has four independent channels, three of which support six-channel complementary PWM output
 - Five 16bit general purpose timer counters, each timer has 4 independent channels, support input capture/output comparison /PWM output
 - Two 16bit basic timer counters
 - One 16bit low power timer counter, support quadrature encoding and double pulse counting function, can work in STOP2 mode
 - 1x 24bit SysTick
 - 1x 7bit window Watchdog (WWDG)
 - 1x 12bit independent Watchdog (IWDG)
- **Programming method**
 - Support SWD/JTAG online debugging interface
 - Support UART and USB Bootloader
- **Security features**
 - Built-in cryptographic algorithm hardware acceleration engine
 - Support AES, DES, TDES, SHA1/224/256, SM1, SM3, SM4, and SM7 algorithms
 - Flash storage encryption, multi-user partition management (MMU)

- TRNG true random number generator
- CRC16/32 calculation
- Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Support security start, program encryption download, security update
- Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
 - Operating voltage range: 1.8V~3.6V
 - Operating temperature range: -40°C ~ 105°C
 - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
 - QFN32(4mm x 4mm)
 - QFN32(5mm x 5mm)
 - QFN48 (6mm x 6mm)
 - LQFP48(7mm x 7mm)
 - QFN64 (8mm x 8mm)
 - LQFP64(10mm x 10mm)
 - LQFP80(12mm x 12mm)

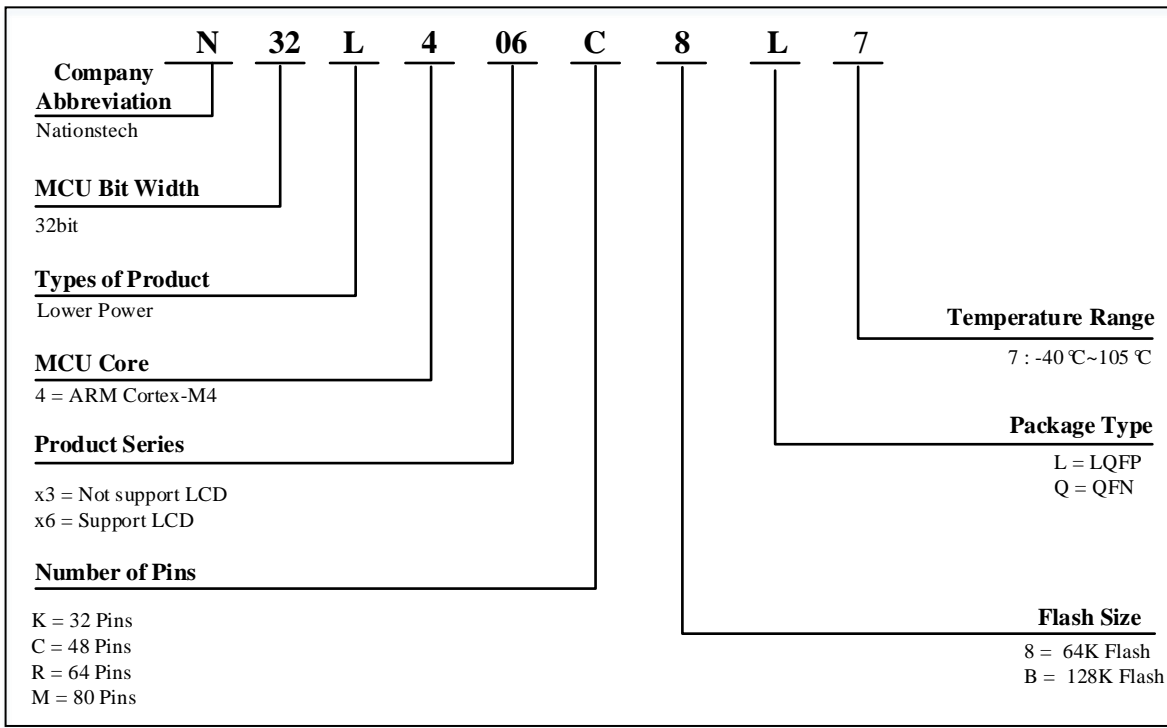
● **Order model**

Type	Model
N32L402	N32L402C8Q7, N32L402C8L7, N32L402R8L7, N32L402CBQ7, N32L402CBL7, N32L402RBL7
N32L403	N32L403K8Q7, N32L403KBQ7, N32L403KBQ7-1 ⁽¹⁾
N32L406	N32L406C8Q7, N32L406R8Q7, N32L406CBL7, N32L406RBL7, N32L406MBL7

Note:

(1):The package is QFN32(5mm x 5mm)

1 Naming rules



2 Product model resource configuration

Table 2-1 N32L40x series resource configuration

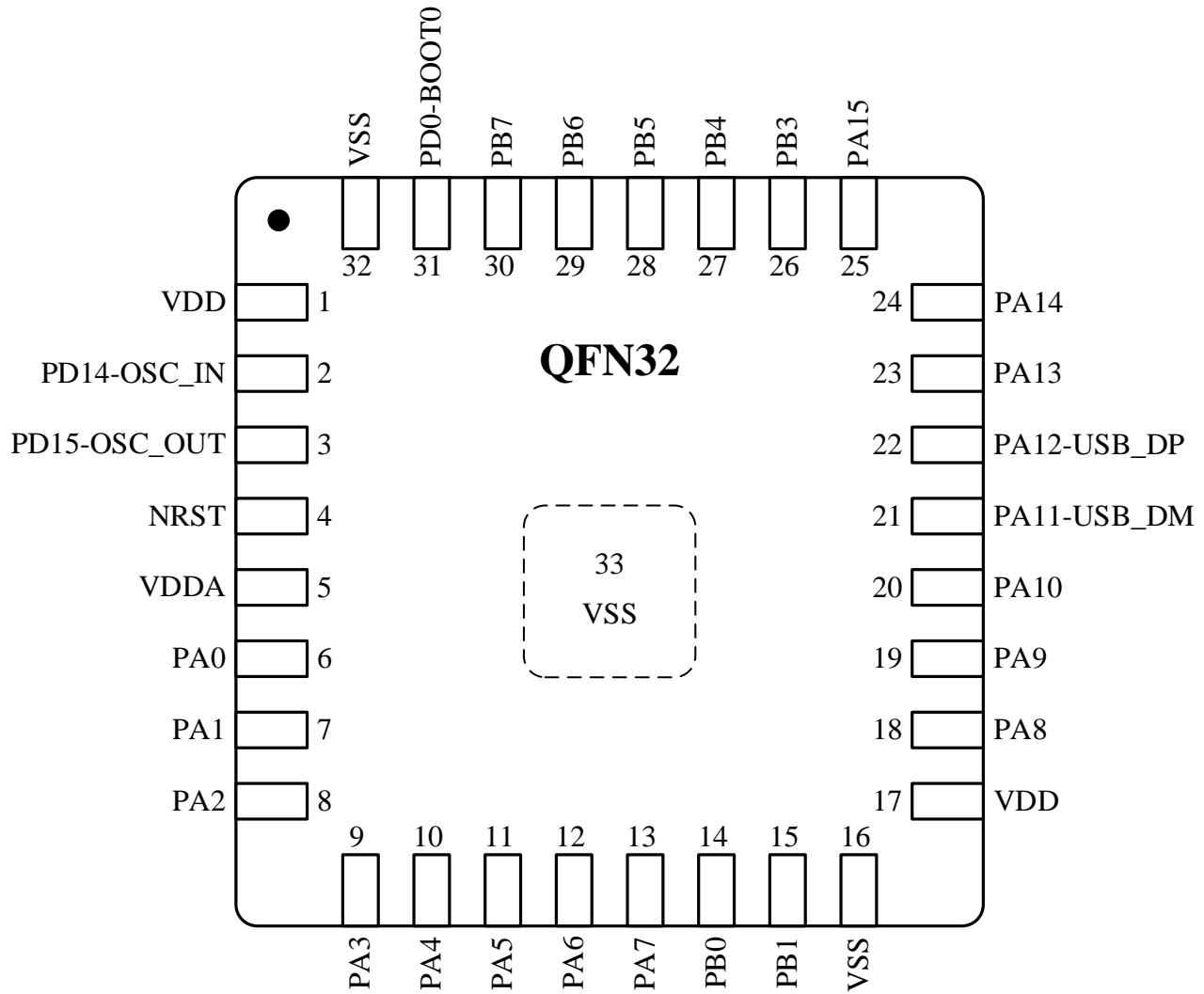
Part Number	N32L402C8/B		N32L402R8/B		N32L403K8/BQ7		N32L403 KBQ7-1 ⁽⁵⁾	N32L406C8/B		N32L406R8/B		N32L406MB	
	Flash (KB)	64	128	64	128	64		128	128	64	128		64
SRAM (KB)	16	16	16	16	16	24	24	16	24	16	24	24	
CPU frequency	ARM Cortex-M4 @ 64MHz, 80DMIPS												
Working environment	1.8~3.6V/-40~105°C												
Timer	General	5											
	Advanced	2											
	Basic	2											
	LPTIM	1											
Communication interface	SPI ⁽¹⁾	2	2	2	2	1	2	2	2	2	2	2	
	I2S ⁽¹⁾	2	2	2	2	1	2	2	2	2	2	2	
	I2C	2											
	UART	2											
	USART	3	3	2	2	2	3	3	3	3	3	3	
	LPUART	1											
	USB	1					No	1	1	1	1	1	1
	CAN	No	No	1									
GPIO	38	52	26	29	38	52	64						
DMA	1x												
Number of Channels	8 Channel												
12bit ADC	1x	1x	1x	1x	1x	1x	1x	1x	1x	1x	1x	1x	
Number of Channels	10Channel	16Channel	10Channel	10Channel	10Channel	10Channel	10Channel	10Channel	16Channel	16Channel	16Channel	16Channel	
12bit DAC	1x												
Number of Channels	1 Channel												
OPAMP/COMP	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	
Segment LCD	4x20	4x34/8x30 ⁽²⁾⁽³⁾	No					4x20	4x34/8x30 ⁽²⁾⁽³⁾	4x44/8x40 ⁽³⁾			
Algorithm support	DES/TDES, AES, SHA1/SHA224/SHA256, SM1, SM3, SM4, SM7, CRC16/CRC32, TRNG												
Security protection	Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot												
Package	LQFP48/QFN48	LQFP64	QFN32 ⁽⁴⁾	QFN32 ⁽⁵⁾	LQFP48/QFN48	LQFP64/QFN64	LQFP80						

1. SPI1 and SPI2 interfaces have the flexibility to switch between SPI mode and I2S audio mode.
2. LQFP64/QFN64 package version B chips do not support LCD 1/8 duty cycle mode (8x30).
3. In 1/8 duty cycle mode, B and C chip LCDs do not support 1/4 bias.
4. The package size is QFN32(4mm x 4mm)
5. The package size is QFN32(5mm x 5mm)

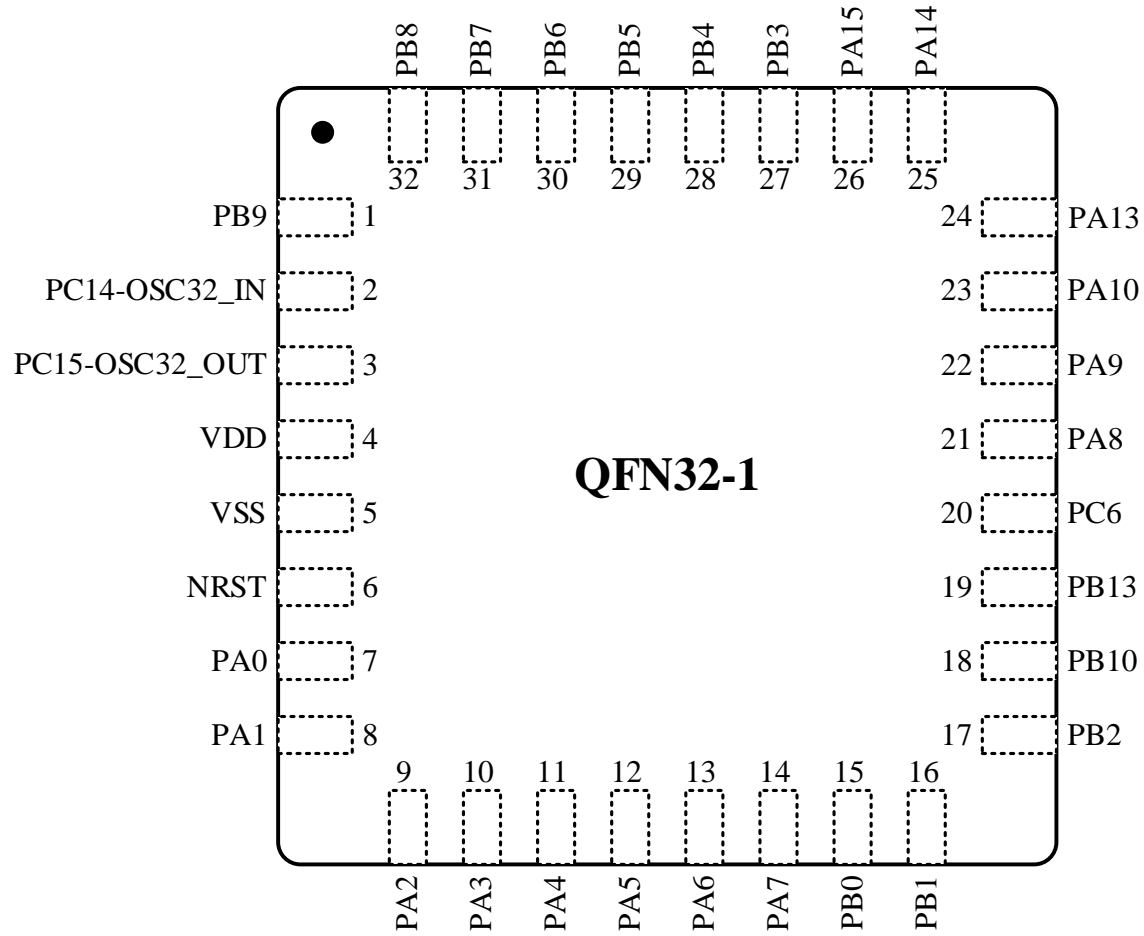
3 Package

3.1 QFN32package

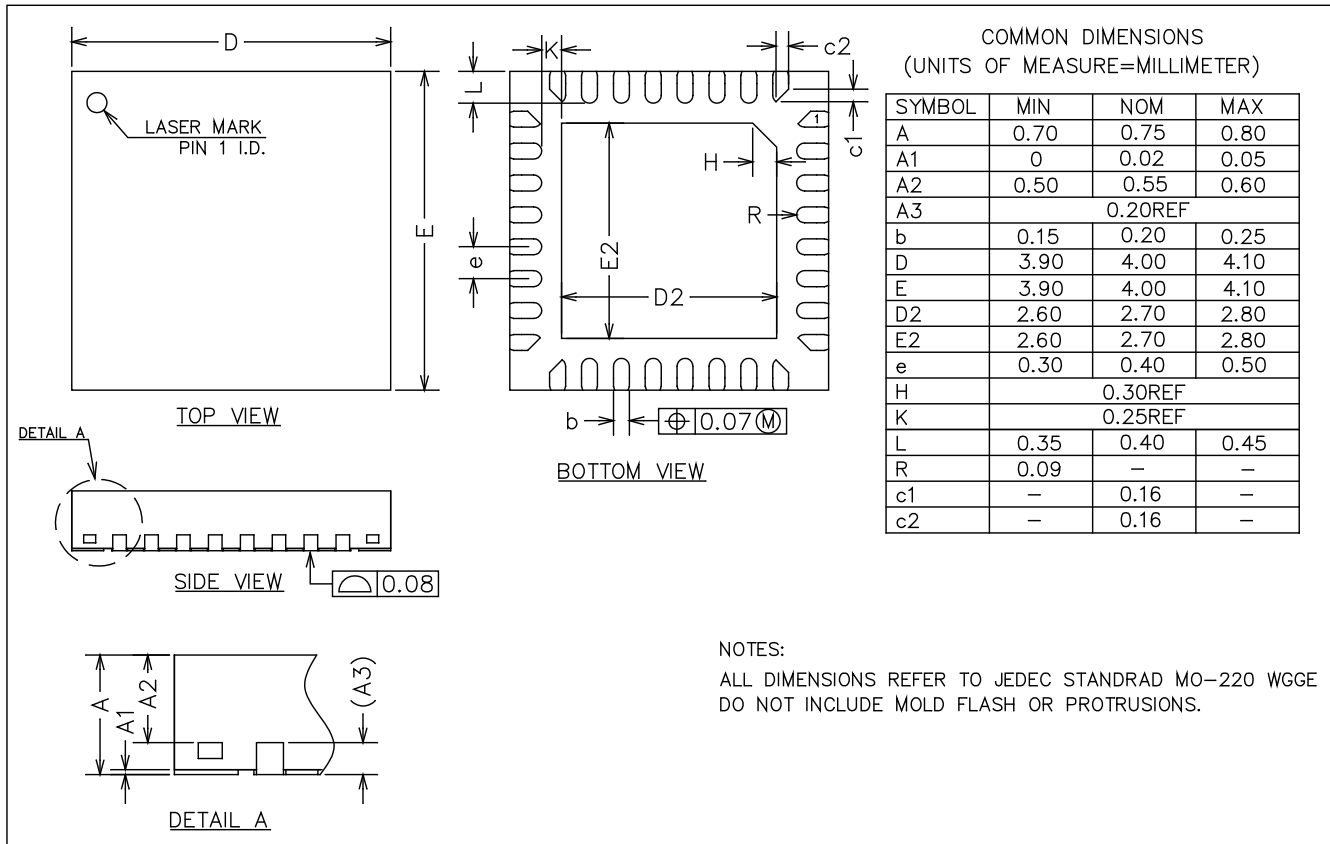
3.1.1 QFN32 (4mm x 4mm)pinout



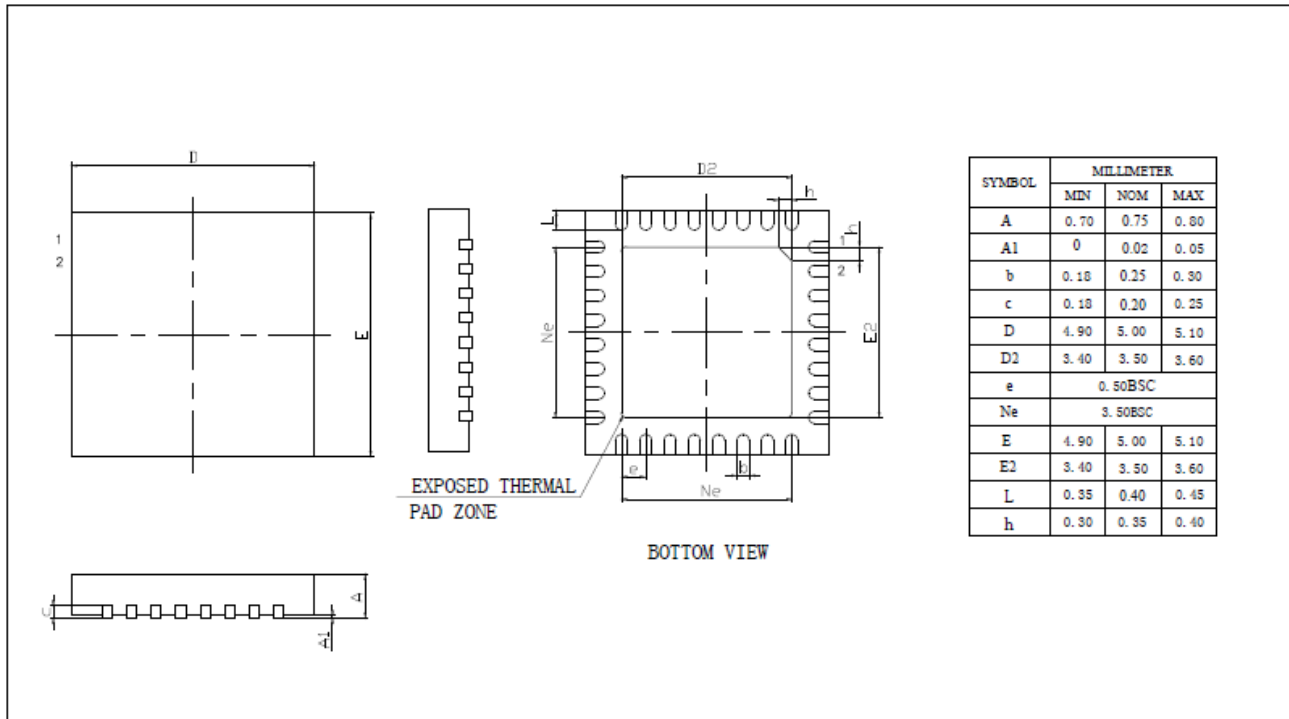
3.1.2 QFN32 (5mm x 5mm)pinout



3.1.3 QFN32 (4mm x 4mm) package

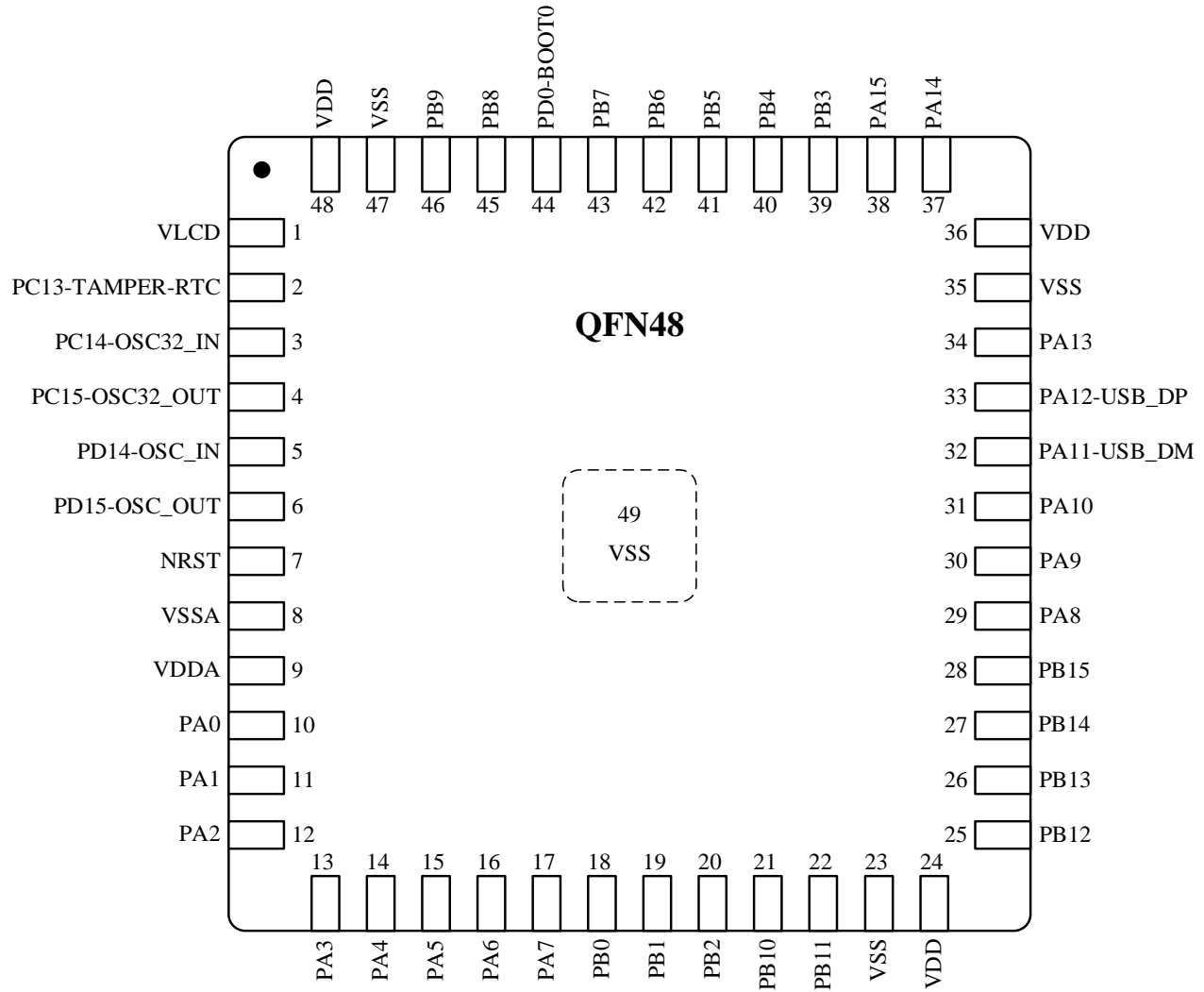


3.1.4 QFN32 (5mm x 5mm) package

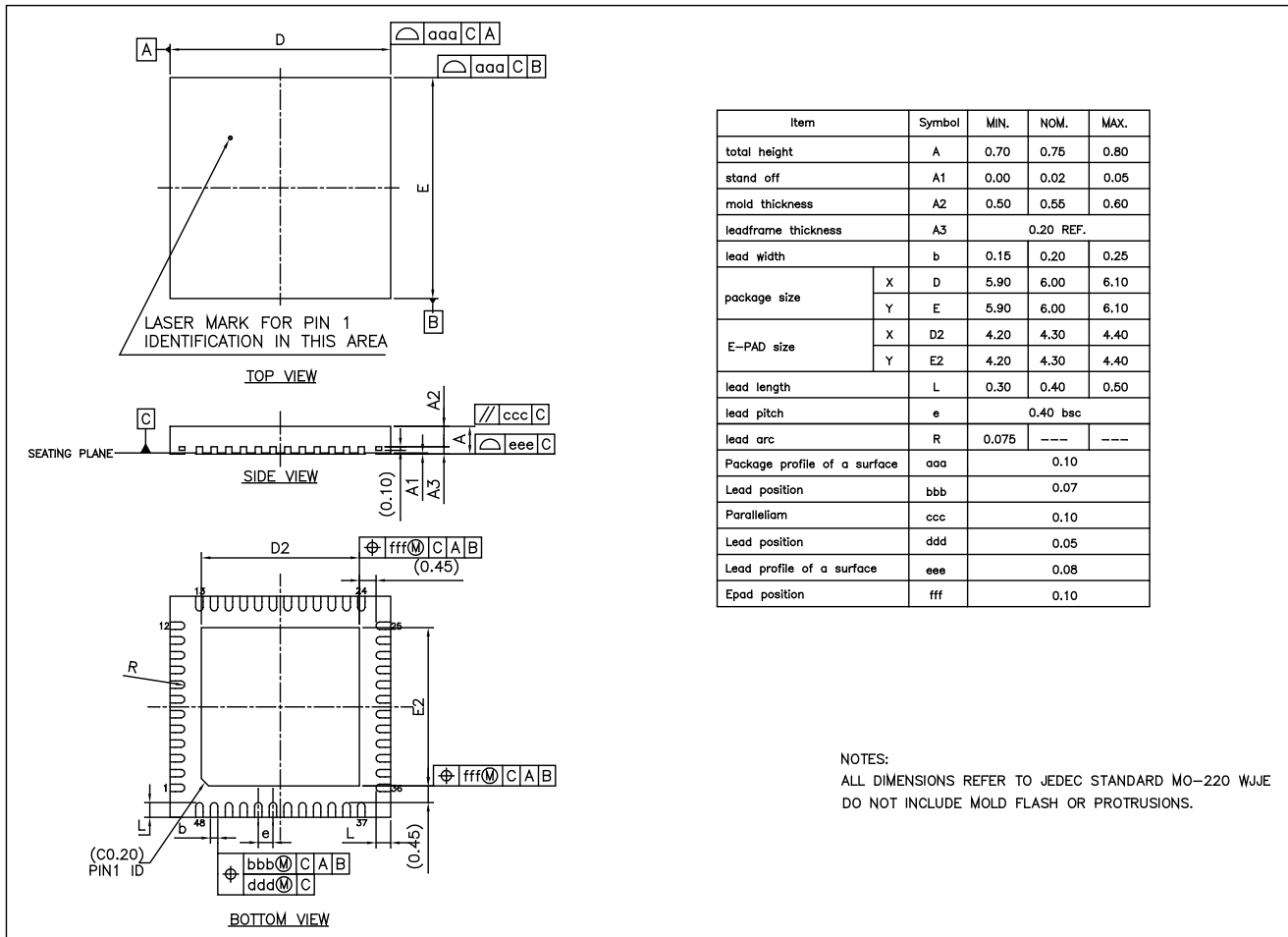


3.2 QFN48 package

3.2.1 QFN48(with LCD) pinout

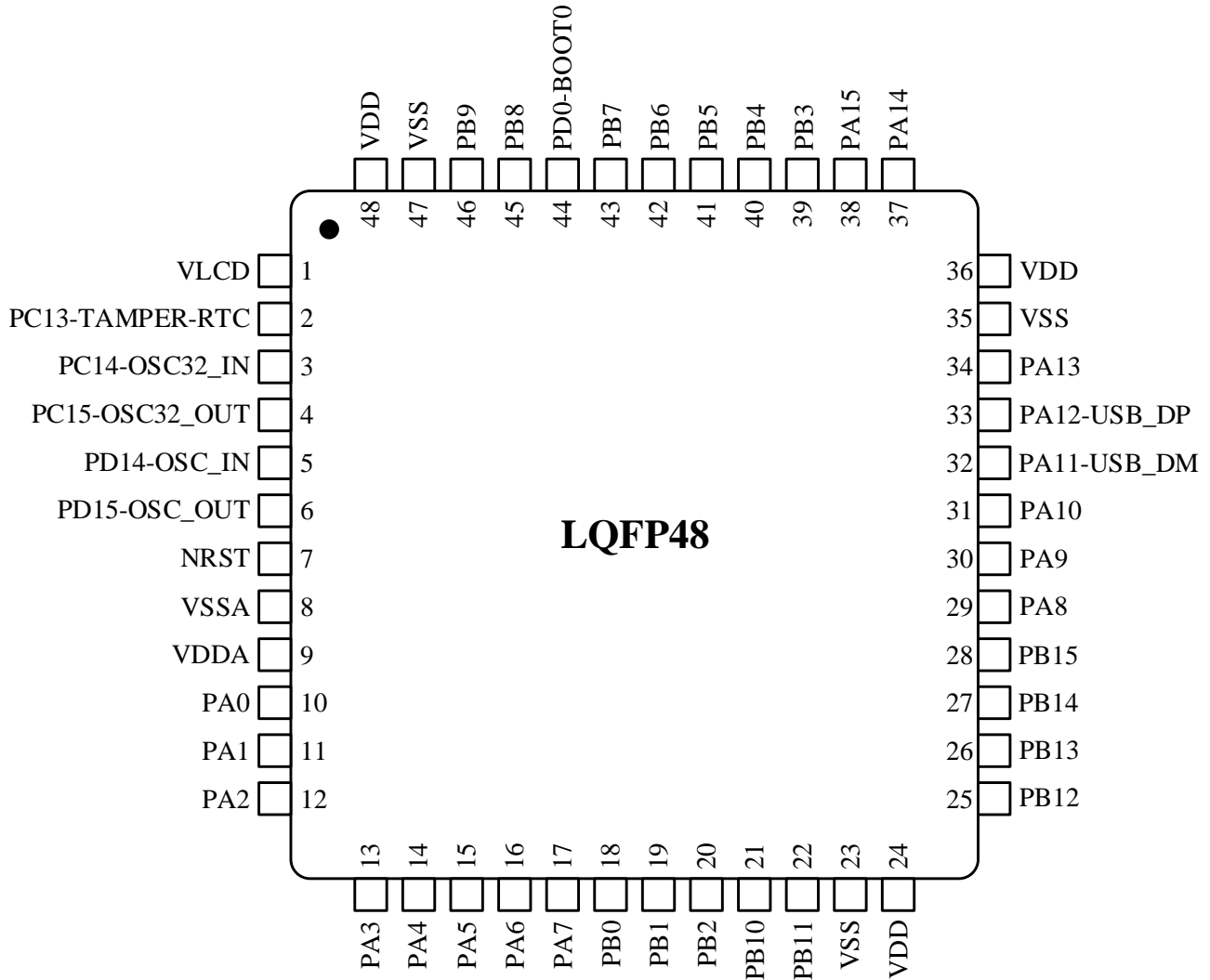


3.2.2 QFN48 (6mm x 6mm) package

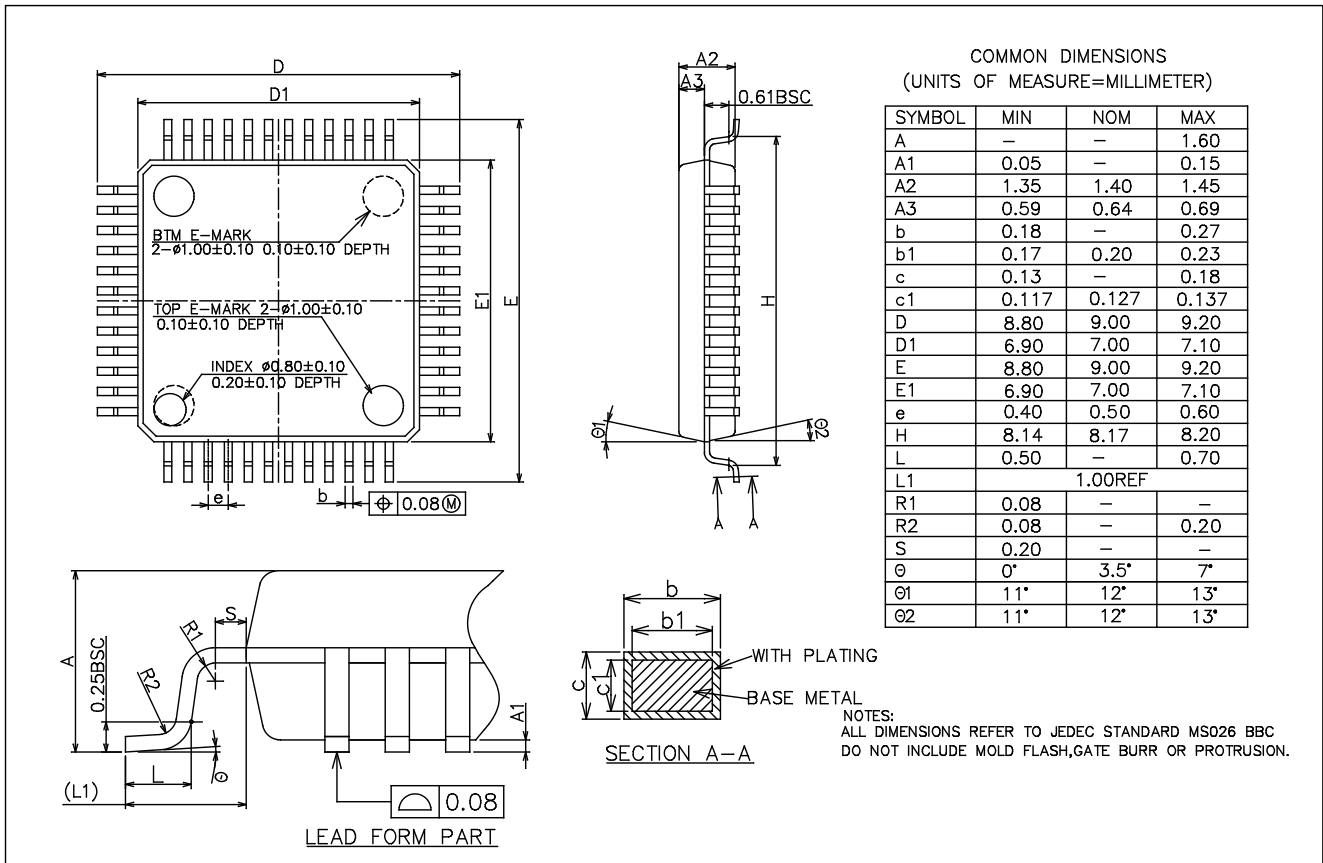


3.3 LQFP48 package

3.3.1 LQFP48(with LCD) pinout

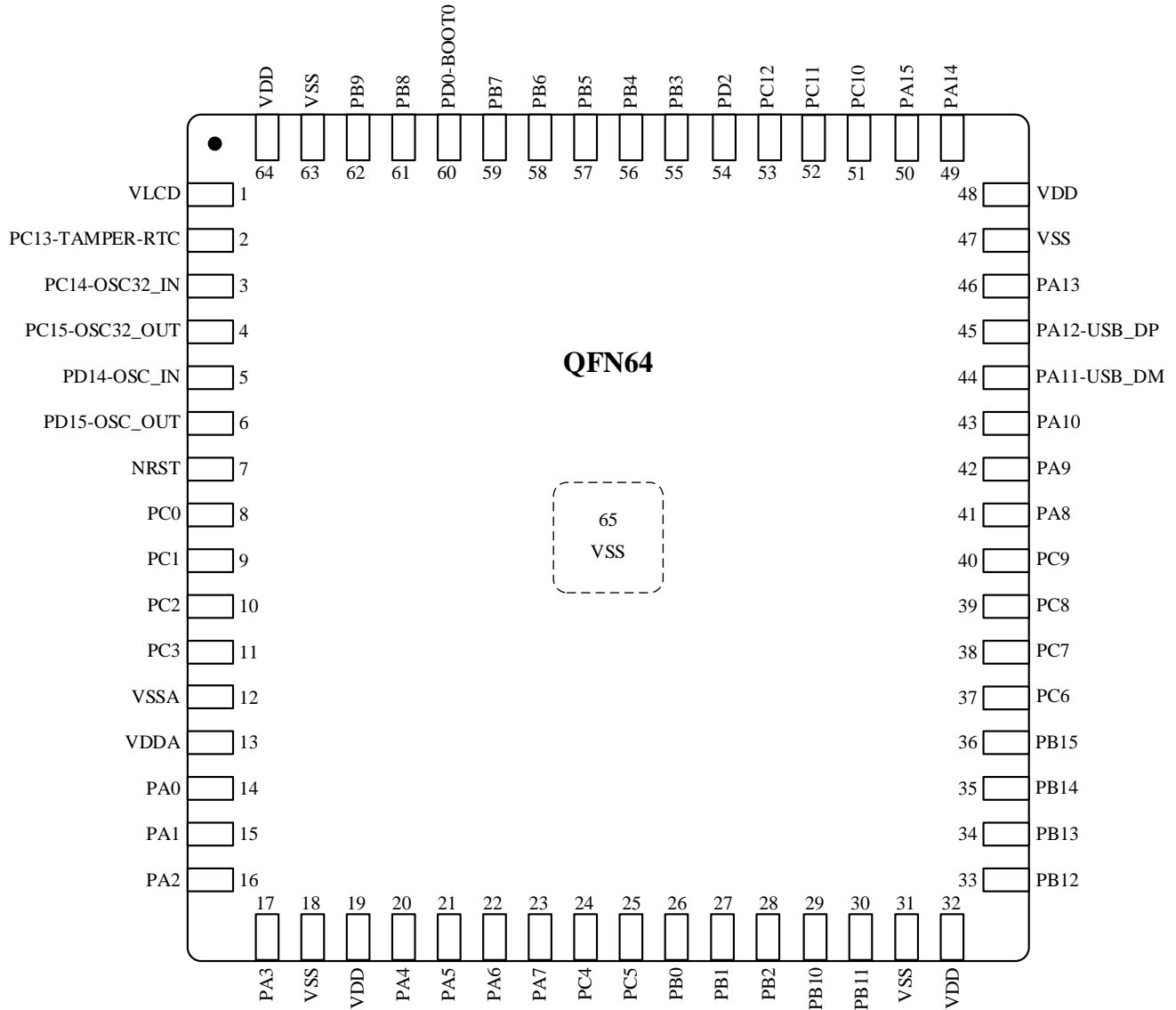


3.3.2 LQFP48 (7mm x 7mm)package

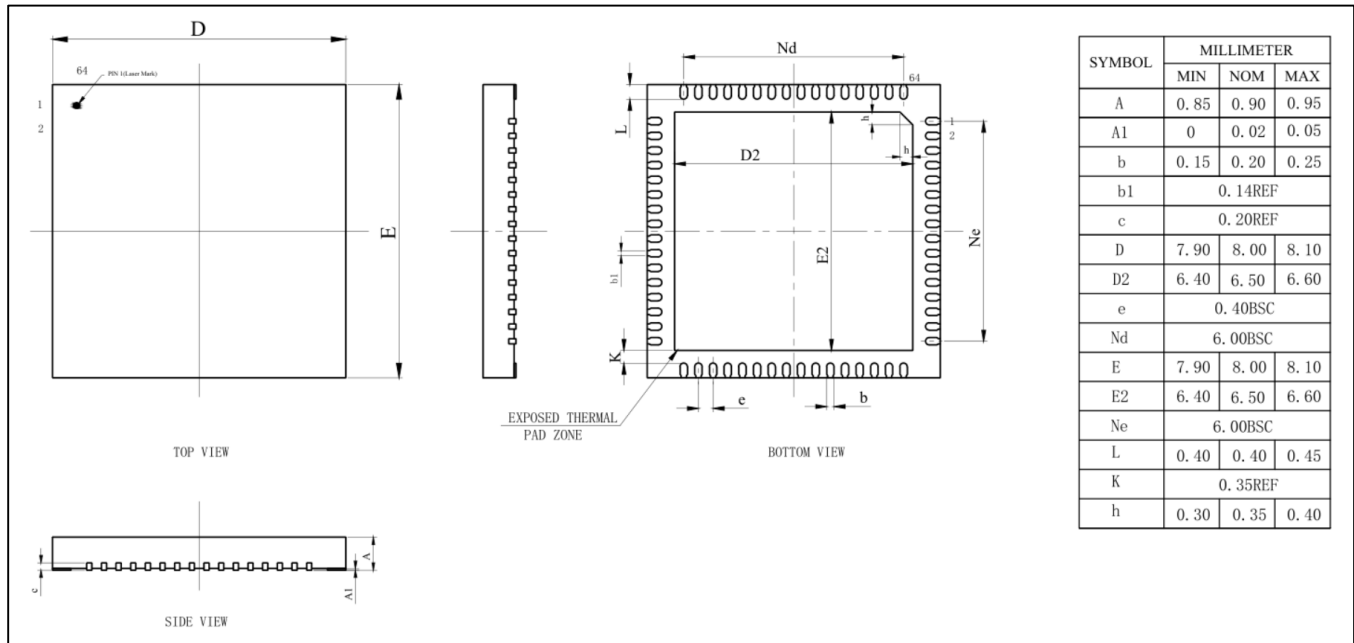


3.4 QFN64 package

3.4.1 QFN64 pinout

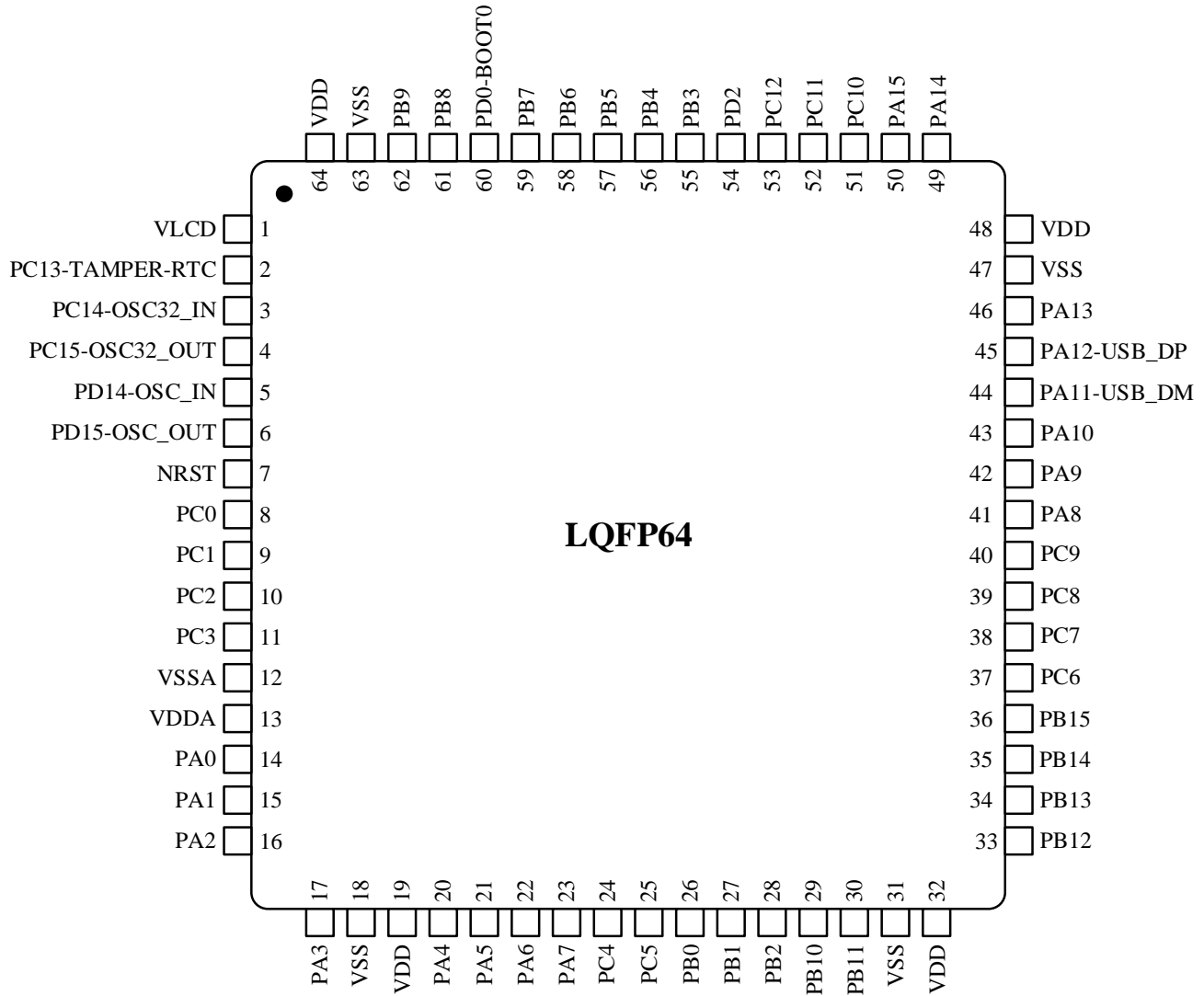


3.4.2 QFN64 (8mm x 8mm)package

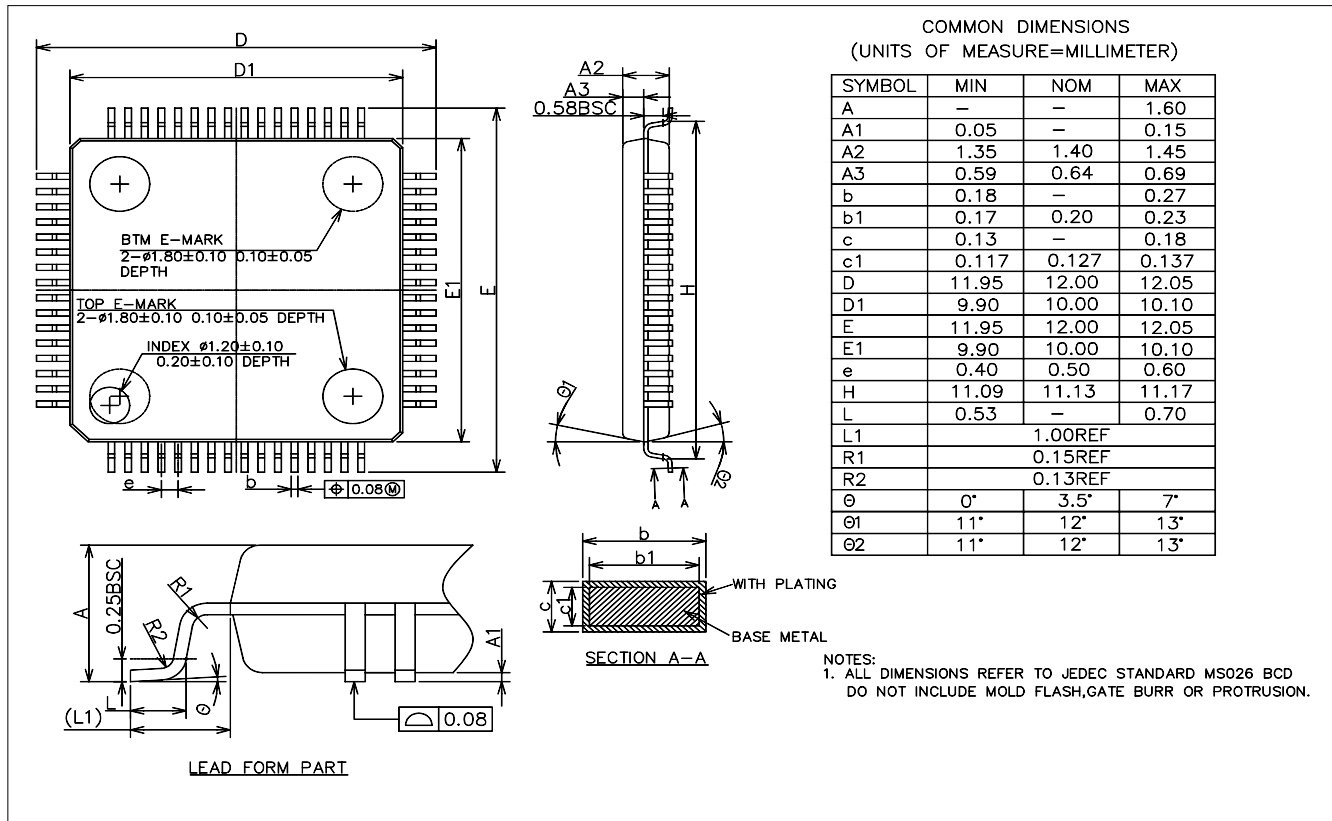


3.5 LQFP64 package

3.5.1 LQFP64 pinout

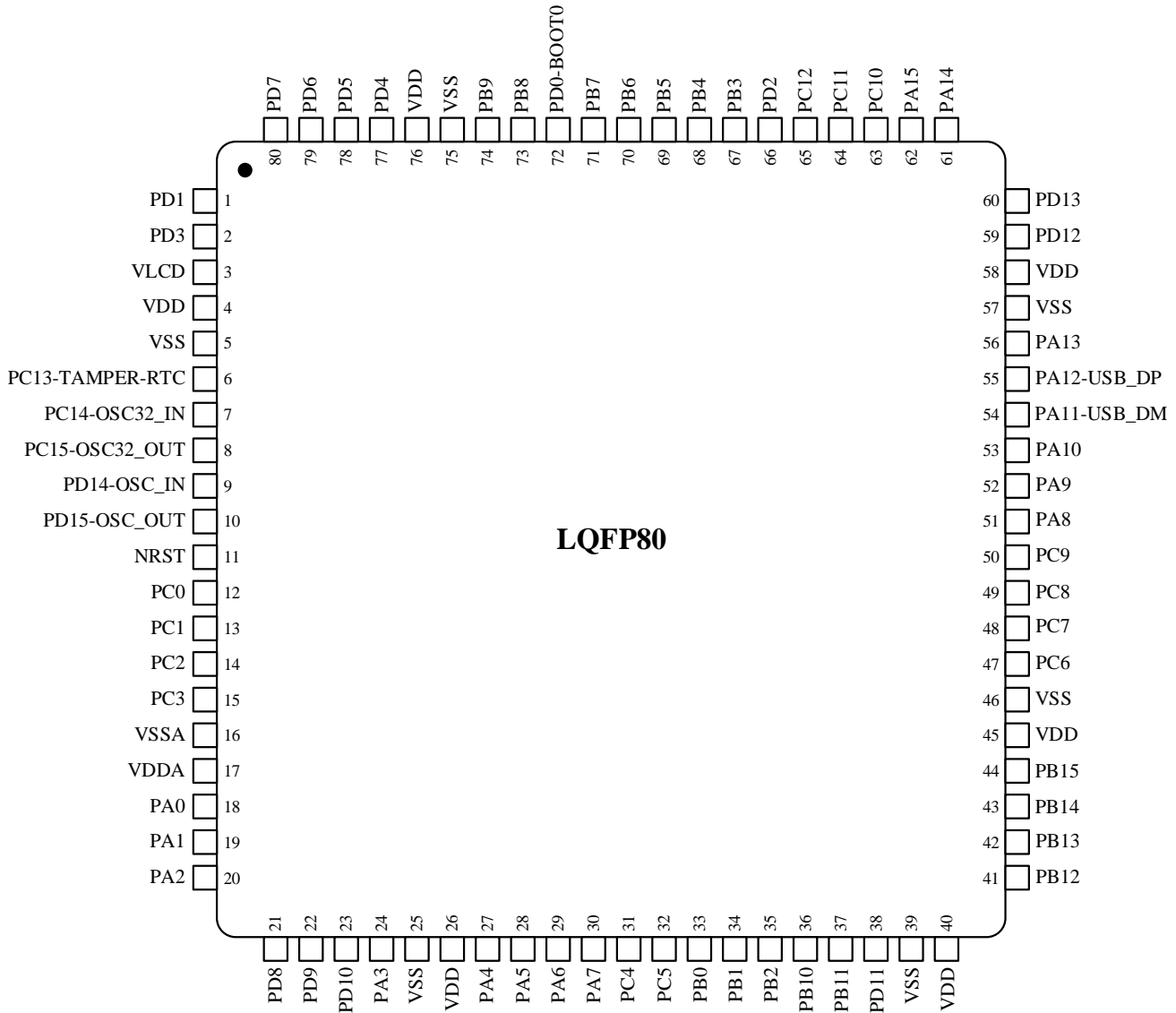


3.5.2 LQFP64 (10mm x 10mm) package

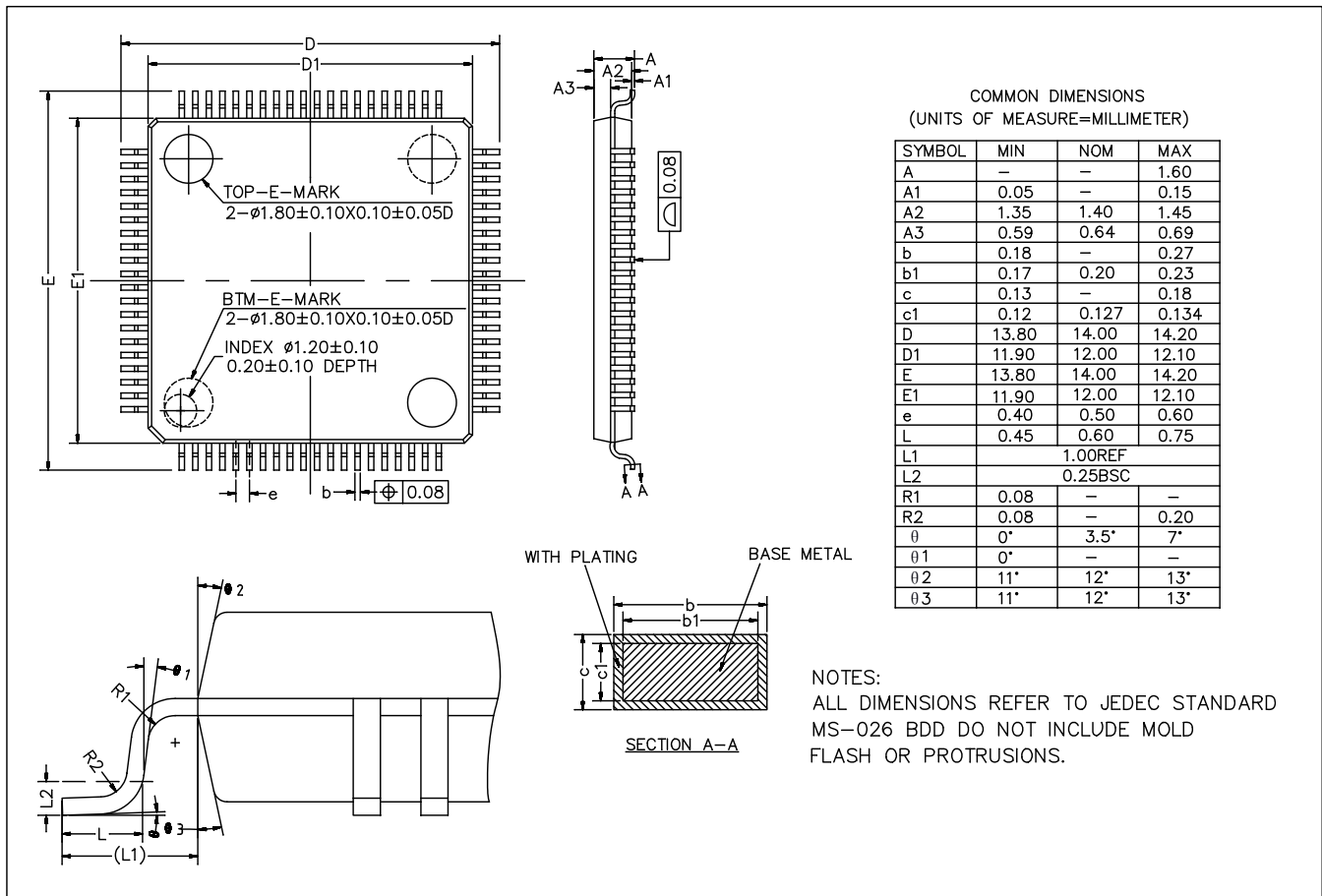


3.6 LQFP80 package

3.6.1 LQFP80 pinout



3.6.2 LQFP80 (12mm x 12mm) package



4 Version history

Version	Date	Note
V1.0	2020.7.1	New document
V1.2	2021.4.14	<ol style="list-style-type: none"> 1. Added N32L401x 2. Updated LCD version difference description, add the precautions for LCD 1/8 duty cycle mode
V1.3	2022.7.6	<ol style="list-style-type: none"> 1. Modify the description of low power 2. Delete N32L401x 3. Modify the description of time counter 4. Modify reset description
V1.4	2022.9.5	<ol style="list-style-type: none"> 1. Add the type N32L403KBQ7-1⁽¹⁾ 2. Modify the number of DAC channels in the resource configuration table 2-1 3. Modify the PB8 pin number of QFN64 pinout 4. Add N32L402 series type 5. Modify LQFP packages size description

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