N32L43x series

32-bit ARM® Cortex®-M4F microcontroller

User manual V2.2

Contents

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1 Abbreviations in the text

1.1 Describes the list of abbreviations used in the register table

The following abbreviations are used in the description of registers:

read/write(rw)	Software can read and write this bit.
read-only(r)	Software can only read this bit.
write-only(w)	Software can only write this bit, and reading this bit will return the reset value.
read/clear(rc_w1)	Software can read this bit or clear it by writing' 1', and writing' 0' has no effect on this bit.
read/clear(rc_w0)	Software can read this bit or clear it by writing' 0', and writing' 1' has no effect on this bit.
read/clear by read(rc_r)	Software can read this bit. Reading this bit will automatically clear it to' 0'. Writing' 0' has no effect on this bit.
read/set(rs)	Software can read or set this bit. Writing' 0' has no effect on this bit.
read-only write trigger(rt_w)	Software can read this bit and write' 0' or' 1' to trigger an event, but it has no effect on this bit value.
toggle(t)	Software can only flip this bit by writing' 1', and writing' 0' has no effect on this bit.
Reserved(Res.)	Reserved bits, the default value must be kept unchanged.

1.2 Available peripherals

For all models of N32L43x microcontroller series, the existence and number of a peripheral, please refer to the data sheet of the corresponding model.

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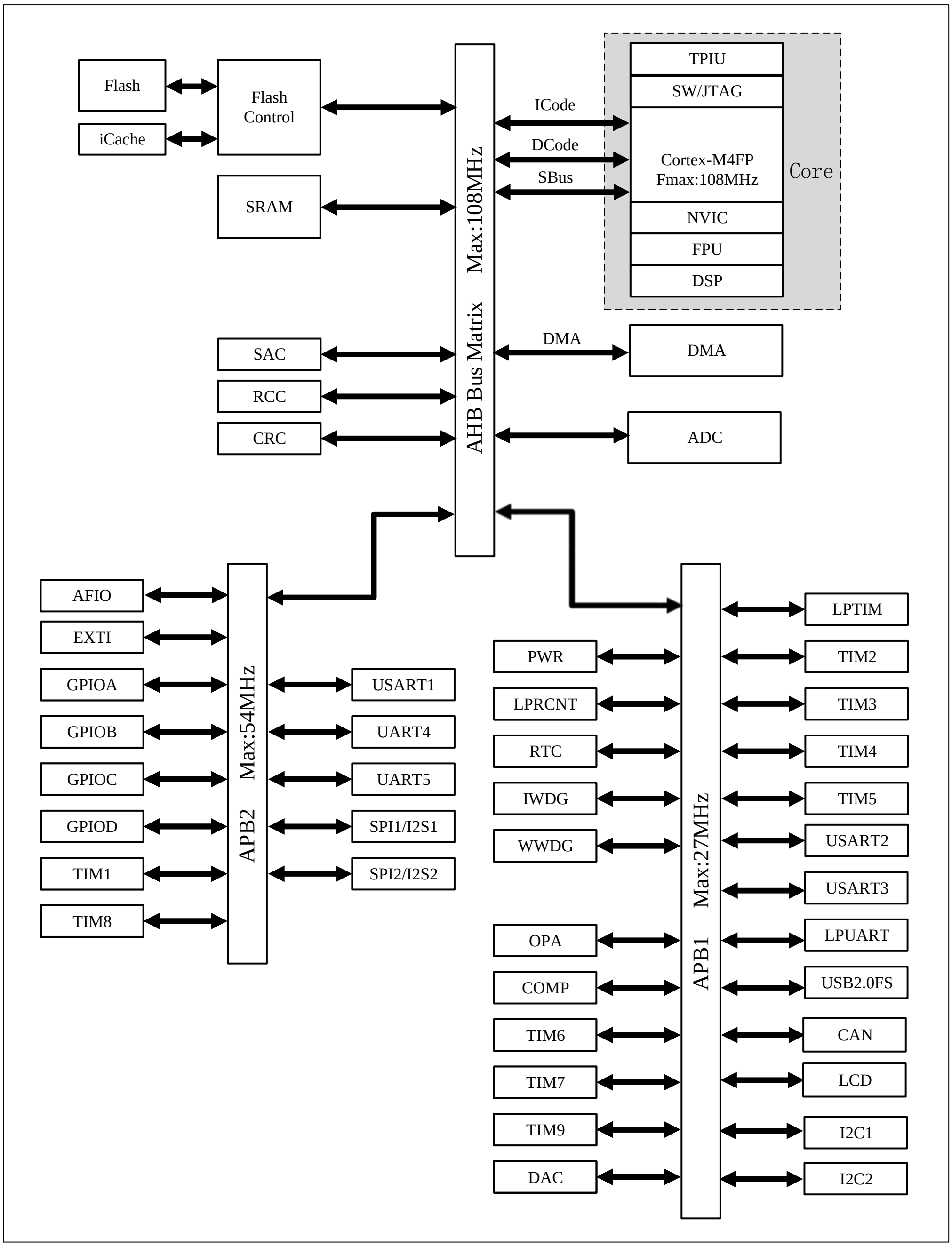
2 Memory and bus architecture

2.1 System architecture

2.1.1 Bus architecture

Figure 2-1 Bus architecture



■ ICode bus: Connect the ICode bus of Cortex™-M4FP core with the flash instruction interface. Instruction prefetching is completed on this bus.

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- The DCode bus connects the DCode bus of Cortex™-M4FP core with the data interface of flash memory (constant loading and debugging access).
- SBus bus connects the SBus bus (peripheral bus) of Cortex™-M4FP core to the bus matrix, which coordinates the access between the core and DMA.
- SAC/CRC has designed matrix interconnection, which supports DMA transmission by software triggering.
- The system consists of two AHB2APB Bridges, i.e. AHB2APB1 and AHB2APB2. The maximum speed of APB1 PCLK is 27MHz; the maximum speed of APB2 PCLK is 54MHz.

2.1.2 Bus address mapping

The address mapping includes all AHB and APB peripherals: AHB peripherals, APB1 peripherals, APB2 peripherals, Flash, SRAM, System Memory, etc. And the address space of SRAM is located in the bit-band Region of SRAM, and atomic accesses can be made through the bit-band Alias to performed read-modify-write operations on the target bits of the bit-band region. The address spaces of all APB and AHB peripherals are located in the bit-band Region of the peripherals. Atomic accesses can be made through the bit-band Alias to performed read-modify-write operations on the target bits of the bit-band region. The specific mapping is as follows:

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Figure 2-2 Bus address map

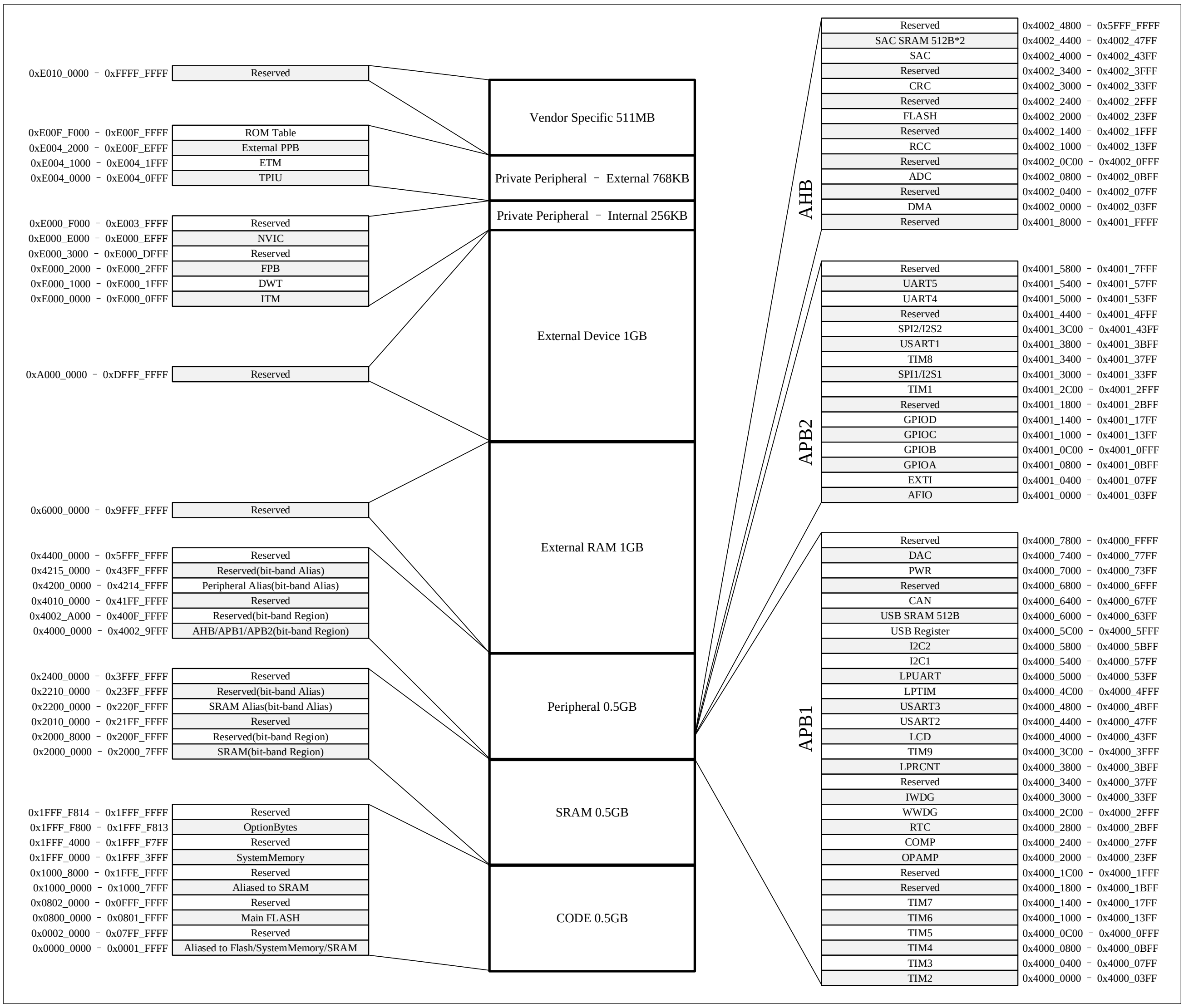

Table 2-1 List of peripheral register addresses

Address range	Peripherals	Bus
0x4002_4800 – 0x5FFF_FFFF	Reserved	AHB
0x4002_4400 – 0x4002_47FF	SAC SRAM 512B*2	
0x4002_4000 – 0x4002_43FF	SAC	
0x4002_3400 – 0x4002_3FFF	Reserved	
0x4002_3000 – 0x4002_33FF	CRC	
0x4002_2400 – 0x4002_2FFF	Reserved	
0x4002_2000 – 0x4002_23FF	FLASH	
0x4002_1400 – 0x4002_1FFF	Reserved	
0x4002_1000 – 0x4002_13FF	RCC	
0x4002_0C00 – 0x4002_0FFF	Reserved	
0x4002_0800 – 0x4002_0BFF	ADC	

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Address range	Peripherals	Bus
0x4002_0400 – 0x4002_07FF	Reserved	
0x4002_0000 – 0x4002_03FF	DMA	
0x4001_8000 – 0x4001_FFFF	Reserved	
0x4001_5800 – 0x4001_7FFF	Reserved	APB2
0x4001_5400 – 0x4001_57FF	UART5	
0x4001_5000 – 0x4001_53FF	UART4	
0x4001_4400 – 0x4001_4FFF	Reserved	
0x4001_3C00 – 0x4001_43FF	SPI2/I2S2	
0x4001_3800 – 0x4001_3BFF	USART1	
0x4001_3400 – 0x4001_37FF	TIM8	
0x4001_3000 – 0x4001_33FF	SPI1/I2S1	
0x4001_2C00 – 0x4001_2FFF	TIM1	
0x4001_1800 – 0x4001_2BFF	Reserved	
0x4001_1400 – 0x4001_17FF	GPIOD	
0x4001_1000 – 0x4001_13FF	GPIOC	
0x4001_0C00 – 0x4001_0FFF	GPIOB	
0x4001_0800 – 0x4001_0BFF	GPIOA	
0x4001_0400 – 0x4001_07FF	EXTI	
0x4001_0000 – 0x4001_03FF	AFIO	
0x4000_7800 – 0x4000_FFFF	Reserved	APB1
0x4000_7400 – 0x4000_77FF	DAC	
0x4000_7000 – 0x4000_73FF	PWR	
0x4000_6800 – 0x4000_6FFF	Reserved	
0x4000_6400 – 0x4000_67FF	CAN	
0x4000_6000 – 0x4000_63FF	USB SRAM 512B	
0x4000_5C00 – 0x4000_5FFF	USB Register	
0x4000_5800 – 0x4000_5BFF	I2C2	
0x4000_5400 – 0x4000_57FF	I2C1	
0x4000_5000 – 0x4000_53FF	LPUART	
0x4000_4C00 – 0x4000_4FFF	LPTIM	
0x4000_4800 – 0x4000_4BFF	USART3	
0x4000_4400 – 0x4000_47FF	USART2	
0x4000_4000 – 0x4000_43FF	Reserved	
0x4000_3C00 – 0x4000_3FFF	TIM9	
0x4000_3800 – 0x4000_3BFF	Reserved	
0x4000_3400 – 0x4000_37FF	Reserved	
0x4000_3000 – 0x4000_33FF	IWDG	
0x4000_2C00 – 0x4000_2FFF	WWDG	
0x4000_2800 – 0x4000_2BFF	RTC	
0x4000_2400 – 0x4000_27FF	COMP	

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Address range	Peripherals	Bus
0x4000_2000 – 0x4000_23FF	OPAMP	
0x4000_1C00 – 0x4000_1FFF	Reserved	
0x4000_1800 – 0x4000_1BFF	Reserved	
0x4000_1400 – 0x4000_17FF	TIM7	
0x4000_1000 – 0x4000_13FF	TIM6	
0x4000_0C00 – 0x4000_0FFF	TIM5	
0x4000_0800 – 0x4000_0BFF	TIM4	
0x4000_0400 – 0x4000_07FF	TIM3	
0x4000_0000 – 0x4000_03FF	TIM2	

2.1.2.1 Bit banding

Cortex™-M4FP memory image includes two bit-band areas. These two bit-band areas map each word in the alias memory area to a bit in the bit-band memory area. When writing a word in the alias area, it is equivalent to performing a read-modify-write operation on the target bits of the bit segment area.

Both the peripheral registers and SRAM are mapped into a bit-band area, which allows a single bit-band area write and read operation to be performed.

The following mapping formula shows how each byte in the alias area corresponds to the corresponding bit in the bit band area:

bitband_ byte _addr = bitband _base + (byte_offset×32) + (bit_number×4)

In which:

bitband_byte_addr is the address of the byte in the alias memory area, which is mapped to a certain target bit;

bitband _base is the starting address of alias area;

byte_offset is the serial number of the byte containing the target bit in the bit-band;

bit_number is the position of the target bit (0-7).

For example:

The following example shows how to map bit 4 in bytes with SRAM address 0x20000400 in alias area:

0x22008010 = 0x22000000 + (0x400×32) + (4×4).

Writing to address 0x22008010 has the same effect as reading-modify-writing to bit 4 of address 0x20000400 bytes in SRAM.

Reading 0x22008010 address returns the value of bit 4 (0x01 or 0x00) of address 0x20000400 bytes in SRAM. Please refer to “Cortex™-M4 Technical Reference Manual” for more information about bit-banding.

2.1.3 Boot management

2.1.3.1 Boot address

During system startup, you can select the BOOT mode after the reset through the BOOT0 pin and the user option

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byte BOOT configuration. After a system reset or exit from standby mode, the value of the BOOT pin will be re-latched and the option byte boot configuration (USER2) will be re-read. After a startup delay, the CPU gets the address at the top of the stack from address 0x0000_0000 and executes the code from the reset vector address indicated by address 0x0000_0004.Because of the Cortex™-M4 always gets the stack top pointer and reset vector from addresses 0x0000_0000 and 0x0000_0004, so boot is only suitable for starting from the CODE area, and address remapping is designed for boot space. There are three boot modes to choose from:

- Boot from Main Flash:
  - Main flash memory is mapped to the boot space (0x0000_0000);
  - Main flash memory is accessible in two address areas, 0x0000_0000 or 0x0800_0000 （ICode/DCode/DMA）;
- Boot from System Memory:
  - System memory is mapped to boot space (0x0000_0000);
  - System memory can be accessed in two address areas, 0x0000_0000 or 0x1FFF_0000 （ICode/DCode/DMA）;
- Boot from the built-in SRAM:
  - The built-in SRAM is mapped to boot space (0x0000_0000);
  - The built-in SRAM is accessible in two address areas, 0x0000_0000 or 0x2000_0000 （ICode/DCode/SBus/DMA）;

2.1.3.2 Boot configuration

In addition, SRAM can also be accessed through virtual address segment 0x1000_0000, which makes the CPU jump to SRAM to run programs through ICode/DCode after starting from Main Flash or System Memory (note that programs are not started from SRAM and do not belong to startup mode). In addition to the BOOT pin configuration boot program, there are two ways to run the program in SRAM:

- Jump directly to the physical address segment 0x2000_0000 of SRAM to run the program. At this time, the program will be run through SBus.
- Jump to the virtual address segment 0x1000_0000 of SRAM, and internally remap to the physical address segment 0x2000_0000 to run the program. At this time, the program will run efficiently through ICode/DCode.

Table 2-2 List of boot mode

Boot mode select pin				**Boot mode**	**Specifies the start address for accessing memory space in boot mode**		
nBOOT1	nBOOT0	BOOT0 pin	nSWBOOT0		Main Flash	System Memory	SRAM
X	X	0	1	Main Flash start	0x0000_0000 0x0800_0000	0x1FFF_0000	0x2000 0000 0x1000 0000
X	1	X	0				
1	X	1	1	System Memory Start	0x08000000	0x0000_0000 0x1FFF_0000	0x2000 0000 0x1000 0000
1	0	X	0				

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Boot mode select pin				Boot mode	Specifies the start address for accessing memory space in boot mode		
nBOOT1	nBOOT0	BOOT0 pin	nSWBOOT0		Main Flash	System Memory	SRAM
0	X	1	1	SRAM start	0x08000000	0x1FFF_0000	0x0000_0000 0x2000 0000 0x1000 0000
0	0	X	0				

2.1.3.3 Embedded boot loader

Embedded boot loader program is stored in the system memory System Memory and is used to reprogram the flash memory through the USART1 or USB-FS interface (full-speed USB device, DFU protocol). The USB-FS interface can only be run when the external clock (HSE) of 4MHz, 6MHz, 8MHz, 12MHz, 16MHz, 18MHz, 24MHz and 32MHz is used. In addition to the above-mentioned 8-frequency external clock (HSE), the USART1 interface can also rely on the internal 16MHz oscillator (HSI) to run.

2.2 Memory system

The program memory, data memory, registers and I/O ports are organized in the same 4GB linear address space. Data bytes are stored in the memory in little endian format. The lowest address byte in a word is regarded as the least significant byte of the word, while the highest address byte is the most significant byte. The specifications of program memory and data memory are as follows.

2.2.1 FLASH specification

Flash consists of a main storage area and an information area, which are described separately below: (Capacity values in the following description do not include ECC)

- The maximum main memory area is 128KB, also known as main flash memory, which contains 64 Page for storing and running user programs and storing data.
- The information area is 20KB, including 10 Page, and consists of system storage area (16KB), system configuration area (2KB) and option byte area (2KB).
  - The System Memory area is 16KB, which contains 8 Page, also known as System Memory, and is used to store and run the BOOT program.
  - The system configuration area is 2KB, including 1 Page.
  - The Option Byte area is 2KB, containing 1 Page, also known as Option Byte, and the effective space is 20B, BOOT programs and user programs can be read, written or erased.

2.2.1.1 Flash memory module organization

Bus address space is allocated to the main storage area and the information area.

Table 2-3 Flash bus address list

Memory area	Page name	Address range	Size
Main memory area	Page 0	0x0800_0000 – 0x0800_07FF	2KB

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Memory area	Page name	Address range	Size
	Page 1	0x0800_0800 – 0x0800_0FFF	2KB
	Page 2	0x0800_1000 – 0x0800_17FF	2KB
	⋮	⋮	⋮
	Page 63	0x0801_F800 – 0x0801_FFFF	2KB
Information area	System memory area	0x1FFF_0000 – 0x1FFF_3FFF	16KB
	System configuration area	0x1FFF_F000 – 0x1FFF_F7FF	2KB
	Option byte area	0x1FFF_F800 – 0x1FFF_F813	20B
Memory area interface register	FLASH_AC	0x4002_2000 – 0x4002_2003	4B
	FLASH_KEY	0x4002_2004 – 0x4002_2007	4B
	FLASH_OPTKEY	0x4002_2008 – 0x4002_200B	4B
	FLASH_STS	0x4002_200C – 0x4002_200F	4B
	FLASH_CTRL	0x4002_2010 – 0x4002_2013	4B
	FLASH_ADD	0x4002_2014 – 0x4002_2017	4B
	FLASH_OB2	0x4002_2018 – 0x4002_201B	4B
	FLASH_OB	0x4002_201C – 0x4002_201F	4B
	FLASH_WRP	0x4002_2020 – 0x4002_2023	4B
	FLASH_ECC	0x4002_2024 – 0x4002_2027	4B
	Reserved	0x4002_2028 – 0x4002_202F	8B
	FLASH_CAHR	0x4002_2030 – 0x4002_2033	4B

Flash memory is organized into 32-bit wide memory units, which can store codes and data constants.

Information is divided into three parts:

- The system memory area is used for storing a boot program for boot loader mode of the system memory. The boot program uses USART1 and USB (DFU) serial interface to program the flash memory.
- System configuration area, which contains basic information of the chip.
- Option byte area, writing to main memory and information block is managed by embedded flash programming/erasing controller.

There are two ways to protect flash memory from illegal access (read, write and erase):

- Page write protection (WRP)
- Read protection (RDP)

When the flash memory write operation is executed, any read operation to the flash memory will lock the bus, and the read operation can only be carried out correctly after the write operation is completed. That is, when writing or erasing, cannot have any read access to the code or data.

The internal RC oscillator (HSI) must be turned on when the flash memory is programmed (written or erased).

Note: In the low power consumption mode, all flash memory operations are suspended.

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2.2.1.2 Read and write operation

The Flash operation only supports 32-bit operation, and the Flash should be erased before the write operation, and the minimum block size for erasing is one Page 2KB. Write operation is divided into programming and erasing phases.

When reading Flash, the number of waiting cycles for reading can be configured by the register. When using, it needs to be calculated in combination with the clock frequency of AHB interface. For example, when HCLK<=32MHz, the minimum number of waiting periods is 0; When 32MHz<HCLK<=64MHz, the minimum number of waiting is 1; When 64MHz<HCLK<=96MHz, the minimum number of waiting periods is 2; When 96MHz<HCLK<=108MHz, the minimum number of waiting periods is 3.

Note: Enable prefetch buffer whether number of wait periods is not zero can improve overall efficiency.

Flash has two low-power operating modes:

- *Low Voltage Mode, configure the FLASH_CTRL.LVMEN bit to enable this mode. Before enabling the low voltage operation mode, it must be ensured that FLASH_CTRL.LATENCY must be greater than 2 (at least 3 wait periods).*
- *Sleep Mode, configure the FLASH_CTRL.SLMEN bit to enable this mode. In sleep mode, code cannot be run in Flash, only in SRAM.*

2.2.1.3 Unlock Flash

After reset, the Flash module is protected and cannot be written into the FLASH_CTRL register to prevent accidental operation of Flash due to electrical interference and other reasons. By writing a specific sequence of key values into the FLASH_KEY register, you can open the operation authority of the FLASH_CTRL register. The specific sequence is: Firstly, writing KEY1 = 0x45670123 in the FLASH_KEY register. Secondly, write KEY2 = 0xCDEF89AB in the FLASH_KEY register.

If there is an error in sequence or key value, a bus error will be returned and the FLASH_CTRL register will be locked until the next reset. The software can check whether the Flash has been unlocked by looking at the FLASH_CTRL.LOCK bit. If normal lock setting is needed, it can be realized by setting the FLASH_CTRL.LOCK bit to 1 by software. After that, you can unlock the Flash by writing the correct key value series in FLASH_KEY.

2.2.1.4 Erase and program

2.2.1.4.1 Erase of main memory area

The main memory area can be erased page by page or whole.

Page Erase

Page Erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Set the FLASH_CTRL.PER bit to' 1';
- Select the page to be erased with the FLASH_ADD register;
- Set the FLASH_CTRL.START bit to' 1';
- Wait for the FLASH_ STS.BUSY bit to change to' 0';

- Read out the erased page and verify it.

Mass Erase

Mass Erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Set the FLASH_CTRL.MER bit to' 1';
- Set the FLASH_CTRL.START bit to' 1';
- Wait for the FLASH_ STS.BUSY bit to change to' 0';
- Read out all pages and verify.

2.2.1.4.2 Main memory area programming

The main memory area can be programmed with 32 bits at a time. When the FLASH_CTRL.PG bit is' 1', writing a word in a flash address will start programming once; Writing any half word of data will result in a bus error. During the programming process (the FLASH_ STS.BUSY bit is' 1'), any operation of reading or writing the flash memory will cause the CPU to pause until the end of the flash programming.

Main memory programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Set the FLASH_CTRL.PG bit to '1';
- Write the word to be programmed at the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

Note: When the FLASH_STS.BUSY bit is '1', you cannot write to any register.

2.2.1.4.3 Option byte erase and programming

The option byte area is programmed differently from the main storage area. The number of option bytes is only 10 bytes (4 bytes for write protection, 2 bytes for read protection, 2 byte for configuration and 2 bytes for storing user data). After unlocking the Flash, you must write KEY1 and KEY2 respectively (see2.2.1.3) to the FLASH_OPTKEY register, and then set the FLASH_CTRL.OPTWE bit to' 1'. At this time, the option byte area can be programmed: set the FLASH_CTRL.OPTPG bit to' 1' and then write the word to the specified address.

When programming the word in the option byte area, use the low byte in the half-word and automatically calculate the high byte (the high byte is the complement of the low byte), and start the programming operation, which will ensure that the option byte and its complement are always correct.

Option byte erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTER bit to '1';
- Set the FLASH_CTRL.START bit to '1';

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- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the erased option byte and verify it.

Option byte area programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTPG bit to '1';
- Writing the word to be programmed to the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

2.2.1.5 ECC function

The Flash module supports the ECC function to realize 1-bit error detection and 1-bit error correction. ECC encoding and decoding (error correction, error detection) are automatically performed by hardware. If an error is detected, the error bit is set and an interrupt is generated.

2.2.1.6 Instruction prefetching

The instruction prefetch function of Flash module supports the prefetch Buffer of 16B. Through instruction prefetching, the instruction execution efficiency of CPU can be improved. The instruction prefetch function can be configured to be enabled or disabled through the register, and it is enabled by default.

2.2.1.7 Option byte

Option byte block is mainly used to configure read-write protection, software/hardware watchdog configuration, boot management, BOR gear selection and reset options when the system is in standby/stop2 mode, and bus address space is allocated for read-write access. They consist of byte with 10 options: 4 byte for write protection, 2 bytes for read protection, 2 byte for configuration option, 2 bytes defined by user, These 10 bytes need to be written through the bus. The option byte block also contains the complement codes corresponding to these 10 option bytes. These complement codes need to be automatically calculated by hardware when the option bytes are written in the bus, and written into Flash together, and used for verification when the option bytes are read.

By default, the option byte block is always readable and write-protected. To write (program/erase) the option byte block, first unlock the Flash, then unlock the option byte: write the correct key-value sequence (KEY1 = 0x45670123, KEY2 = 0xCDEF89AB) in the FLASH_OPTKEY, and then write the option byte block will be allowed. If the sequence is wrong or the key value is wrong, a bus error will be returned and the option byte will be locked until the next reset. If it is necessary to set the lock normally, it can be realized by writing 0 to the FLASH_CTRL.OPTWE bit by software, and then the option byte can be unlocked by writing the correct key-value series in the FLASH_OPTKEY.

After each system reset, the option byte data is read out from the option byte block of Flash and stored in the option byte register (FLASH_OB/FLASH_WRP) with read-only property. At the same time, the option byte complement data read out together will be used to verify whether the option byte data is correct. If it does not match, an option byte error flag (FLASH_OB.OBERR) will be generated. When an option byte error occurs, the corresponding option byte is forced to 0xFF. When the option byte and its complement are both 0xFF (the state after erasing), the above

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verification steps are skipped and verification is not required.

Table 2-4 Option byte list

Address	[31:24] Corresponding complement code	[23:16] Option byte	[15:8] Corresponding complement code	[7:0] Option byte
0x1FFF_F800	nUSER	USER	nRDP1	RDP1
0x1FFF_F804	nData1	Data1	nData0	Data0
0x1FFF_F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF_F80C	nWRP3	WRP3	nWRP2	WRP2
0x1FFF_F810	nUSER2	USER2	nRDP2	RDP2

- Read protection L1 level option byte: RDP1
  - Protect the code stored in the flash memory;
  - When the correct value is written, it will be forbidden to read the flash memory;
  - The result of whether RDP1 is turned on or not can be inquired through FLASH_OB[1];
- User configuration options: USER
  - USER[7:3]：Reserved
  - USER[2]：nRST_STDBY configuration options, read through FLASH_OB [4]

    0：Reset when entering standby mode

    1：No reset occurs when entering standby mode
  - USER[1]：nRST_STOP2, read through FLASH_OB[3]

    0：Reset occurs when entering stop2 mode

    1：No reset occurs when entering stop2 mode
  - USER[0]：WDG_SW configuration options, read through FLASH_OB[2]

    0：Hardware watchdog

    1：Software watchdog
- 2 bytes of user data: Datax
  - Data1 (stored in FLASH_OB[25:18]);
  - Data0 (stored in FLASH_OB [17:10]);
- Write protection option byte: WRP0 ~ 3, which can be written through the register FLASH _WRP[31:0] query
  - WRP0: write protection of pages 0-15, bit [0] corresponds to Page0 / 1,., bit [7] corresponds to page14 / 15;
  - WRP1: write protection on pages 16-31, bit [0] corresponds to Page16 / 17,., bit [7] corresponds to Page30 / 31;

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- WRP2: write protection on pages 32-47 bit [0] corresponds to Page32 / 33,., bit [7] corresponds to Page46 / 47;
- WRP3: write protection on pages 48-63, bit [0] corresponds to Page48 /49., bit [7] corresponds to Page62 / 63;

- Read protection L2 level option byte: RDP2
  - Add protection function on the basis of L1, see 2.2.1.9 detailed description of read protection;
  - Whether RDP2 is turned on or not can be determined by FLASH_OB [31] query;
- User Configuration 2：USER2
  - USER2 [7]：Reserved
  - USER2[6:4]：BOR_LEV[2:0], , read out through FLASH_OB2[10:8],default is 0
  - USER2 [3]：Reserved
  - USER2[2] : nSWBOOT0, read out through FLASH_OB2[26],default is 1
  - USER2[1]: nBOOT1, read out through FLASH_OB2[23], default is 1
  - USER2[0]: nBOOT0, read out through FLASH_OB2[27], default is 1

2.2.1.8 Write protect

Write protection can be configured for all pages in the flash main storage area (maximum 128KB) to prevent accidental write operations caused by program runaway or electrical interference. The basic unit of write protection is: for Page0 ~ 63, every 2 pages is a basic protection unit. Write protection can be configured by setting WRP0 ~ 3 in the option byte block; After each configuration, A system reset is required for the configured value to be reloaded to take effect. If an attempt is made to program or erase a protected page, a protection error flag will be returned in the FLASH_STS.

The system memory block (16KB) in the system information area stores the boot program and cannot be changed.

The system configuration block (2KB) in the system information area stores the basic information of the chip and cannot be changed.

The option byte block (2KB) in the system information area stores the user-configurable option byte information. The write protection of the option byte block is achieved by writing 0 to the FLASH_CTRL.OPTWE bit by software, and after that, you can write the correct key value series in FLASH_OPTKEY to release the write protection of the option byte.

2.2.1.9 Read protection

The user code in flash can be protected from illegal reading by setting read protection. Read protection is mainly aimed at protecting the access operation of main memory area and option byte block after chip sealing operation. Read protection is set by configuring RDP bytes in the option byte block. Three different read protection levels can be configured, as shown in the following Table

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Table 2-5 Read protection configuration list

Read protection status	RDP1	nRDP1	nRDP2	RDP2
L1 level	0xFF	0xFF	RDP2! = 0xCC ‖ nRDP2! = 0x33	
Unprotected	0xA5	0x5A	RDP2! = 0xCC ‖ nRDP2! = 0x33	
L2 level	0xXX	0xXX	0x33	0xCC
L1 level	Not the above three configurations			

- L0 level:
  - In unprotected state, corresponding (RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33);
  - The main memory area and option byte block can be read arbitrarily;
  - The write protection property of each page can be configured for programming and erasing;
- L1 level:
  - The corresponding ~(((RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33)) | (RDP2 == 0xCC & nRDP2 == 0x33));
  - Only the read operation of the main storage area from the user code is allowed, that is, when the program is started from the main flash memory in non debugging mode, the read operation of the main storage area is allowed;
  - Pages 0~1 are automatically write-protected；
  - Other pages can be programmed by the code executed in the main flash memory (realizing IAP or data storage and other functions);
  - All pages are not allowed to write or erase in debug mode or after booting from internal SRAM (except for mass erase);
  - All functions of loading code into the built-in SRAM through JTAG/SWD and then execute it are still valid, or they can be started from the built-in SRAM through JTAG/SWD, which can be used to remove read protection;
  - When the read-protected option byte is rewritten to the unprotected L0 level, all the main storage areas will be automatically erased, and the process is as follows: (Erasing the option byte block will not result in automatic whole erasing operation, because the result of erasing is 0xFF, which is equivalent to still being in the protection state of L1 level)
    - Write the correct key value sequence to unlock the option byte area in FLASH_OPTKEY;
    - The bus initiates a command to erase the entire option byte area (Page erase);
    - Bus write 0xA5 to read protection option byte;
    - Automatically erase all main storage areas internally;
    - Automatically write 0xA5 to read protection option byte internally;
    - When the system is reset (such as software reset, etc.), the option byte block (including the new

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RDP value 0xA5) will be reloaded into the system, and the read protection will be released;

- The following access operations to the flash memory will be prohibited:
  - Access main flash memory from built-in SRAM start execution code (including using DMA);
  - Access the main flash memory by JTAG, SWV (serial line observer), SWD (serial line debugging) and boundary scanning;

- L2 level: Except that SRAM boot disabled, debug mode disabled, option byte write/page erase disabled and the protection level cannot be modified (irreversible), other features are the same as L1 level. The L2 level is realized by configuring another option byte, RDP2. No matter what the value of RDP1 is, as long as it satisfies (RDP2==0xCC & nRDP2==0x33), it is L2 level.

Table 2-6 Flash read-write-erase(1) permission control table

protect level	Boot mode	Main Flash				Changing a Protection Level
	Perform user / Access area	JTAG/ SWD	Main Flash	System Memory	SRAM	
L0 level	Before 4KB of flash main memory area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Change to L1 or L2 is allowed
	After 4KB of flash main memory area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	prohibit	prohibit	Read-Write-Erase	prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Before 4KB of flash main memory area	Prohibit	Read-only	Read-only	Read-only	L0 or L2 is allowed. When changed to L0, the main memory area is automatically erased.
	After 4KB of flash main memory area	Prohibit	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	

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	Flash option byte area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Before 4KB of flash main memory area	JTAG/SWD interface is disabled.	Read-only	Read-only	Read-only	No modification is allowed.
	After 4KB of flash main memory area		Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase		Allow	Allow	Allow	
	Flash option byte area		Read-only	Read-only	Read-only	
	Flash system memory area		Prohibit	Read-write-erase	Prohibit	
	SRAM (All)		Read and write	Read and write	Read and write	
protect level	Boot mode	SRAM				Changing a Protection Level
	Perform user / Access to areas	JTAG/SWD	Main Flash	System Memory	SRAM	
L0 level	Before 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	Change to L1 or L2 is allowed
	After 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	

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	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Before 4KB of flash main memory area	Prohibit	Read-only	Read-only	Prohibit	L0 or L2 is allowed. When changed to L0, the main memory area is automatically erased.
	After 4KB of flash main memory area	Prohibit	Read-write-erase	Read-write-erase	Prohibit	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Prohibit	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Before 4KB of flash main memory area	L2 protection level, cannot boot from SRAM				No modification is allowed. JTAG/SWD is banned.
	After 4KB of flash main memory area					
	Flash main memory area mass erase					
	Flash option byte area					
	Flash system memory area					
	SRAM (All)					

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protect level	Boot mode / Perform user / Access to areas	System Memory				Changing a Protection Level
		JTAG/SWD	Main Flash	System Memory	SRAM	
L0 level	Before 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	Change to L1 or L2 is allowed
	After 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Before 4KB of flash main memory area	Prohibit	Read-only	Read-only	Read-only	L0 or L2 is allowed. When changed to L0, the main memory area is automatically erased.
	After 4KB of flash main memory area	Prohibit	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Before 4KB of flash main memory area	JTAG/SWD interface is	Read-only	Read-only	Read-only	No modification allowed

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	After 4KB of flash main memory area	disabled.	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase		Allow	Allow	Allow	
	Flash option byte area		Read-only	Read-only	Read-only	
	Flash system memory area		Prohibit	Read-write-erase	Prohibit	
	SRAM (All)		Read and write	Read and write	Read and write	

Note: 1. Erase here refers to flash page erase;

2.2.2 iCache

In order to achieve higher system performance, an instruction buffer needs to be added between the high-speed CPU and the low-speed Flash to improve the instruction execution efficiency. Because of the existence of the instruction buffer, the CPU will be able to work at a higher frequency. When the instruction requested by the CPU is in the instruction buffer, the CPU can obtain the instruction without delay and realize zero waiting for execution. When the current instruction sequence, instruction prefetch sequence and instruction buffer all miss, Flash will be re-read and the Cache will be backfilled and updated. Accordingly, it is equivalent to storing only the jump header of the program in the Cache.

The main features of the instruction buffer are as follows:

- 2KB iCache。
- Support connection mode: 4WAY.

2.2.2.1 Software interface

- Enable
  - Provide configuration for software to enable/disable iCache. There is no limit to the switching conditions (see the FLASH_AC.ICAHEN bit).
- Reset
  - Provide software to clear the iCache interface, which must be initiated when iCache is closed. Reset and switching cannot be switched at the same time. First, turn off FLASH_AC.ICAHEN, then write 1 to FLASH_AC.ICAHRST, and then turn on FLASH_AC.ICAHEN.
- Lock
  - Cache locking mechanism is supported, and the software configuration puts the program into its designated way. When all the ways are locked, the new data will not be written into the cache. After the software resets the cache, the lock state is automatically cleared.

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- Additional remarks
  - Selection of Cache replacement algorithm is not supported.
  - When using icache, there is no WB/WT selection when the CPU writes operation.

2.2.2.2 Register description

FLASH_AC.ICAHEN and FLASH_AC.ICAHRST are the iCache enable switch and iCache data clear switch respectively.

FLASH_CAHR.LOCKSTRT and FLASH_CAHR.LOCKSTOP are the start latch and stop latch of iCache corresponding mode lock, respectively. After iCache is reset, the FLASH_CAHR register automatically returns to the reset value. See for detailed usage method of 2.2.2.3.3 ICache locking.

2.2.2.3 Operating process

2.2.2.3.1 iCache enable and disable

Users can turn on and switch off iCache at any time. If the user program needs to jump between the main memory area and other memory areas, the iCache must be closed and the data of the iCache must be cleared, otherwise, the instruction acquisition error will occur.

2.2.2.3.2 iCache data refresh

The iCache is designed as instruction cache. When the instruction is updated by application software or the instruction jumps between the main memory area and other memory areas, the software must set the FLASH_AC.ICAHRST bit to 1 to clear the data in the instruction cache.

Note: FLASH_AC.ICAHRST bit is a write-only bit, and it returns to 0 when read.

2.2.2.3.3 iCache locking

The software controls the FLASH_CAHR register to lock some repeatedly used codes in iCache to improve the efficiency of code execution. iCache module has four latch channels, and the size of each channel is 1/4 of the whole cache. When using a single channel, you must ensure that the amount of code to latch is less than the size of each channel. Otherwise need to use more channels to latch the code. The latch function can be used according to the following control flow:

1. Set FLASH_CAHR.LOCKSTRT[0] to 1;
2. Execute function 1 that needs to be locked in channel 0 (the code amount of function 1 should be less than the size of a single channel);
3. Set FLASH_CAHR.LOCKSTOP[0] to 1 after the function 1 is executed;
4. Then set FLASH_CAHR.LOCKSTRT[1] to 1;
5. Execute function 2 that needs to be locked in channel 1 (the code amount of function 2 should be less than the size of a single channel);
6. After the function 2 is executed, set FLASH_CAHR.LOCKSTOP[1] to 1;

Attention: 1. when the channel is latched, the register operation must follow a fixed process -First set FLASH_CAHR.LOCKSTRT then set FLASH_CAHR.LOCKSTOP;

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2. The order of channel latch must be 0~3, otherwise it will reduce the execution efficiency.

2.2.3 SRAM

SRAM is mainly used for code operation to store variables and data or stacks during program execution. The maximum capacity is 32KB， it is divided into SRAM1 and SRAM2, of which SRAM1 is up to 24K bytes and SRAM2 is 8K bytes(SRAM2 supports parity check and needs to be initialized before use).

SRAM supports read-write access of byte, half-word and word.

SRAM supports code running (supports access of SBus, ICode and DCode), and can run programs at full speed in SRAM. The maximum address range of SRAM is 0x2000 0000~0x2000 7FFF.

In Stop2 mode, SRAM1 and SRAM2 data optional retention; in STANDBY mode， only SRAM2 data optional rentention.

The main features are as follows:

- The maximum capacity is 32KB in total.
- Support byte/half-word/word reading and writing
- I/D/S/DMA can be accessed.
- I/D BUS can run programs at full speed from Remap to SRAM.

2.2.4 FLASH register description

These peripheral registers must be operated as words (32 bits).

2.2.4.1 FLASH register overview

Table 2-7 FLASH register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	FLASH_AC	Reserved																				SLMEN	SLMF	LVMEN	LVMF	ICAHEN	ICAHRST	PRFTBFS	PRFTBFE	Reserved	LATENCY		
	Reset Value																					0	0	0	0	0	0	1	1		0	0	0
004h	FLASH_KEY	FKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	FLASH_OPTKEY	OPTKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	FLASH_STS	Reserved																								ECCERR	EVERR	EOP	WRPERR	PVERR	PGERR	Reserved	BUSY
	Reset Value																									0	0	0	0	0	0		0
010h	FLASH_CTRL	Reserved																		ECCERRITE	EOPITE	FERRITE	ERRITE	OPTWE	SMPSEL	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
	Reset Value																			0	0	0	0	0	0	1	0	0	0		0	0	0
014h	FLASH_ADD	FADD																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
018h	FLASH_OB2	Reserved				nBOOT0	nSWBOOT0	Reserved		nBOOT1	Reserved												BOR_LEV			Reserved							
	Reset Value					1	1			1													0	0	0								
01Ch	FLASH_OB	RDPRT2	Reserved					Data1								Data0								Not Used					nRST_STDBY	nRST_STOP2	WDG_SW	RDPRT1	OBERR
	Reset Value	0						1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
020h	FLASH_WRP	WRPT																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
024h	FLASH_ECC	Reserved																		ECCHW						Reserved		ECCLW					
	Reset Value																			0	0	0	0	0	0			0	0	0	0	0	0
028h ~ 02Ch	Reserved																																
030h	FLASH_CAHR	Reserved																								LOCKSTOP				LOCKSTRT			
	Reset Value																									0	0	0	0	0	0	0	0

2.2.4.2 FLASH control and status register

See for abbreviations in register descriptions 1.1 section.

2.2.4.2.1 The FLASH access control register (FLASH_AC)

Address offset: 0x00

Reset value: 0x0000 0030

31 … 16
Reserved

15 … 12	11	10	9	8	7	6	5	4	3	2 … 0
Reserved	SLMEN	SLMF	LVMEN	LVMF	ICAHEN	ICAHRST	PRFTBFS	PRFTBFE	Reserved	LATENCY
	rw	r	rw	r	rw	w	r	rw		rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	SLMEN	FLASH Sleep Mode Enable 0：Turn off FLASH sleep mode; 1：Enable FLASH sleep mode.
10	SLMF	FLASH sleep mode flag 0：FLASH not working in sleep mode; 1：FLASH working in sleep mode.
9	LVMEN	FLASH low-voltage working mode enable 0: Turn off FLASH low-voltage working mode;

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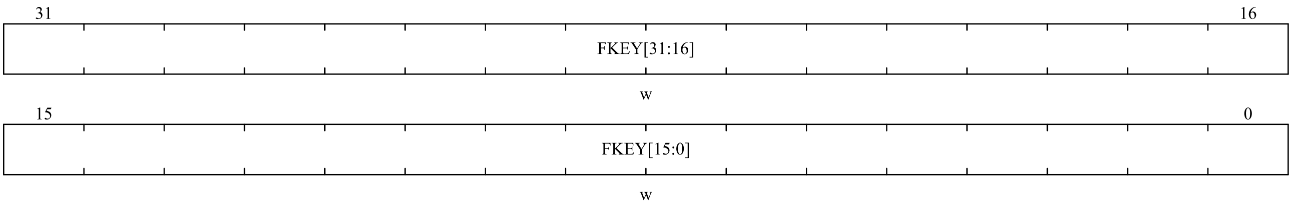
Bit field	Name	Description
		1: Enable FLASH low-voltage working mode. *Note: FLASH_AC.LATENCY must be greater than 0x02 to enable FLASH low voltage operation mode.*
8	LVMF	FLASH low voltage working mode flag 0: FLASH is not working in low voltage working mode; 1: FLASH works in low voltage working mode.
7	ICAHEN	iCache enable 0: turn off iCache; 1: enable iCache.
6	ICAHRST	iCache reset 0: writing '0' is invalid; 1: write '1' to reset.
5	PRFTBFS	Prefetch buffer status This bit indicates the status of the prefetch buffer 0: The prefetch buffer is closed; 1: The prefetch buffer is open.
4	PRFTBFE	Prefetch buffer enable 0: Close the prefetch buffer; 1: Enable prefetch buffer.
3	Reserved	Reserved, the reset value must be maintained.
2:0	LATENCY	time delay These bits represent the ratio of SYSCLK (system clock) period to flash memory access time. 000: zero period delay, when 0 < SYSCLK <=32MHz 001: one cycle delay, when 32MHz < SYSCLK <=64MHz 010: two cycle delay, when 64MHz < SYSCLK <=96MHz 011: three cycle delay, when 96MHz < SYSCLK <= 108MHz Other values: reserved

2.2.4.2.2 The FLASH key register (FLASH_KEY)

Address offset: 0x04

Reset value: 0xXXXX XXXX



Bit field	Name	Description
31:0	FKEY	Used to unlock the FLASH_CTRL.LOCK bit.

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2.2.4.2.3 The FLASH OPTKEY register (FLASH_OPTKEY)

Address offset: 0x08

Reset value: 0xXXXX XXXX

31–16
OPTKEY[31:16]
w

15–0
OPTKEY[15:0]
w

Bit field	Name	Description
31:0	OPTKEY	Used to unlock the FLASH_CTRL.OPTWE bit.

2.2.4.2.4 The FLASH status register (FLASH_STS)

Address offset: 0x0C

Reset value: 0x0000 0000

31–16
Reserved

15–8	7	6	5	4	3	2	1	0
Reserved	ECCERR	EVERR	EOP	WRPERR	PVERR	PGERR	Reserved	BUSY
	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1		r

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	ECCERR	ECC error Read FLASH error, hardware set this bit to '1', write '1' to clear this state.
6	EVERR	Erase check error When the page is erased and the check reports an error, the hardware sets this bit to '1', and writing '1' can clear this state.
5	EOP	End of operation When the flash operation (programming/erasing) is completed, the hardware sets this bit to '1', and writing '1' can clear this bit status. *Note: Every successful programming or erasing will set the EOP state.*
4	WRPERR	Write protection error When trying to program a write-protected flash address, the hardware sets this bit to '1', and writing '1' can clear this bit.
3	PVERR	programming verification error When an error is reported during verification after programming, the hardware sets this bit to '1', and writing '1' can clear this state.
2	PGERR	Programming error When trying to program an address whose content is not '0xFFFF_FFFF', the

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Bit field	Name	Description
		hardware sets this bit to '1', and writing '1' can clear this state. *Note: Before programming, the FLASH_CTRL.START bit must be cleared.*
1	Reserved	Reserved, the reset value must be maintained.
0	BUSY	Busy This bit indicates that a flash operation is in progress. At the beginning of flash operation, this bit is set to '1'; This bit is cleared to '0' when the operation ends or an error occurs.

2.2.4.2.5 The FLASH control register (FLASH_CTRL)

Address offset: 0x10

Reset value: 0x0000 0080

31:16
Reserved

15:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ECERRITE	EOPITE	FERRITE	ERRITE	OPTWE	SMPSEL	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	ECERRITE	ECC error interrupt This bit allows an interrupt to be generated when the FLASH_STS.ECCERR bit goes to '1'. 0: Interrupt generation is prohibited; 1: Enable interrupt generation.
12	EOPITE	Allow operation completion interrupt. This bit allows an interrupt to be generated when the FLASH_STS.EOP bit becomes '1'. 0: interrupt generation is prohibited; 1: interrupt generation is allowed.
11	FERRITE	Erase/Program Verify Error Interrupt This bit allows an interrupt to be generated when the FLASH_STS.EVERR/PVERR bit goes to '1'. 0: Interrupt generation is prohibited; 1: Enable interrupt generation.
10	ERRITE	Error status interrupt allowed This bit allows an interrupt to be generated when a Flash error occurs (when FLASH_STS.PGERR/ FLASH_STS.WRPERR is set to '1'). 0: interrupt generation is prohibited; 1: interrupt generation is allowed.
9	OPTWE	Allow write option byte

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Bit field	Name	Description
		When this bit is '1', the option byte is allowed to be programmed. When the correct key sequence is written in the FLASH_OPTKEY register, this bit is set to '1'. Software can clear this bit.
8	SMPSEL	Flash programming mode options 0: SMP1 mode. Before programming, you need to read the content of the address where the programming is located, and check whether it has been erased. If it has not been erased, the programming operation will not be performed, and the FLASH_STS.PGERR warning bit will be set; 1: SMP2 mode. Before programming, it will not judge whether the content of the address where the programming is located has been erased, and the Flash will directly start programming. If the programming address has been written with data before, only the same data can be written when programming the address in SMP2 mode, otherwise the data cannot be guaranteed to be written correctly.
7	LOCK	Lock You can only write '1'. When this bit is '1', Flash and FLASH_CTRL are locked. After detecting the correct unlocking sequence, hardware clears this bit to '0'. After an unsuccessful unlocking operation, this bit cannot be changed until the next system reset.
6	START	Start When this bit is '1', an erase operation will be triggered. This bit can only be set to '1' by software and cleared to '0' when FLASH_STS.BUSY becomes '1'.
5	OPTER	Erase option bytes. 0: Disable option bytes erase mode; 1: Enable option bytes erase mode.
4	OPTPG	Program option bytes. 0: Disable option bytes program mode; 1: Enable option bytes program mode.
3	Reserved	Reserved, the reset value must be maintained.
2	MER	Mass erase. 0: disable mass erase mode; 1: enable mass erase mode.
1	PER	Page erase. 0: disable page erase mode; 1: enable page erase mode
0	PG	Program. 0: disable program mode; 1: enable program mode.

Note: Please refer to section 2.2.1.4 for programming and erasing.

2.2.4.2.6 The FLASH address register (FLASH_ADD)

Address offset: 0x14

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Reset value: 0x0000 0000

31–16
FADD[31:16]
w

15–0
FADD[15:0]
w

Bit field	Name	Description
31:0	FADD	Flash address Select the address to be programmed when programming, and select the page to be erased when page erasing. *Note: When the FLASH_STS.BUSY bit is '1', this register cannot be written.*

2.2.4.2.7 The FLASH Option byte register 2 (FLASH_OB2)

Address offset: 0x18

Reset value: 0x0c800000

31–28	27	26	25–24	23	22–16
Reserved	nBOOT0	nSW BOOT0	Reserved	nBOOT1	Reserved
	r	r		r	

15–11	10–8	7–0
Reserved	BOR_LEV[2:0]	Reserved
	r	

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
27	nBOOT0	nBOOT0 *Note: This bit is read-only.*
26	nSWBOOT0	nSWBOOT0 *Note: This bit is read-only.*
25:24	Reserved	Reserved, the reset value must be maintained.
23	nBOOT1	nBOOT1 *Note: This bit is read-only.*
22:11	Reserved	Reserved, the reset value must be maintained.
10:8	BOR_LEV[2:0]	BOR reset level 000：1.64V 001：2.10V 010：2.30V 011：2.60V 100：2.90V Other: reserved
7:0	Reserved	Reserved, the reset value must be maintained.

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Note: For the specific combined functions of nBOOT0, nSWBOOT0, and nBOOT1, see chapter 2.1.3 boot Management.

2.2.4.2.8 Option byte register (FLASH_OB)

Address offset: 0x1C

Reset value: 0x03FF FFFC

31	30–26	25–18	17–16
RDPRT2	Reserved	Data1	Data0
r		r	r

15–10	9–5	4	3	2	1	0
Data0	Not_Used	nRST_STDBY	nRST_STOP2	WDG_SW	RDPRT1	OBERR
r	r	r	r	r	r	r

Bit field	Name	Description
31	RDPRT2	Read protection L2 level protection 0: Read protection L2 level is not enabled; 1: Read protection L2 level is enabled. *Note: This bit is read-only.*
30:26	Reserved	Reserved, the reset value must be maintained.
25:18	Data1[7:0]	Data1 *Note: This bit is read-only.*
17:10	Data0[7:0]	Data0 *Note: This bit is read-only.*
9:5	Reserved	Not used, the hardware remains at 1.
4	nRST_STDBY	Enter Standby mode reset configuration. 0: Reset immediately after entering Standby mode; 1: No reset occurs after entering Standby mode. *Note: This bit is read-only.*
3	nRST_STOP2	Enter STOP2 mode reset configuration. 0: Reset occurs immediately after entering STOP2 mode; 1: No reset occurs after entering the STOP2 mode. *Note: This bit is read-only.*
2	WDG_SW	Set watchdog 0: hardware watchdog; 1: Software watchdog. *Note: This bit is read-only.*
1	RDPRT1	Read protection L1 level protection 0: Read protection L1 level is not enabled; 1: read protection L1 level is enabled. *Note: This bit is read-only.*
0	OBERR	Option byte error When this bit is '1', it means that the option byte does not match its complement.

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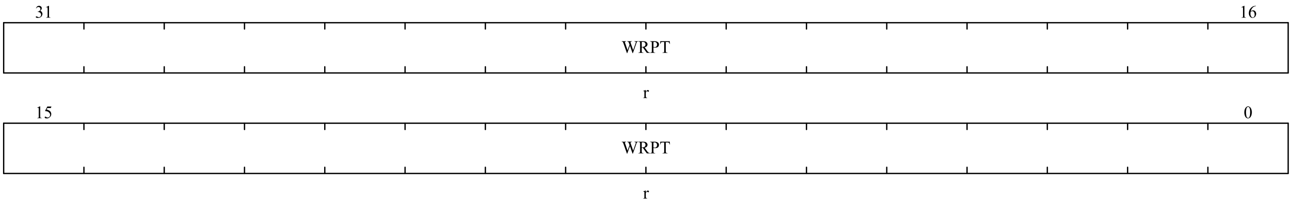
Bit field	Name	Description
		Note: This bit is read-only.

2.2.4.2.9 Write protection register (FLASH_WRP)

Address offset: 0x20

Reset value: 0xFFFF FFFF

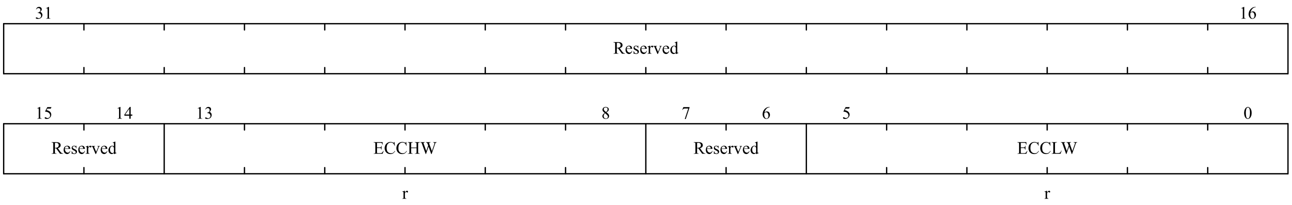


Bit field	Name	Description
31:0	WRPT	Write protect This register contains the write protection option byte loaded by option byte area. 0: write protection takes effect; 1: Write protection is invalid. *Note: These bits are read-only.*

2.2.4.2.10 ECC register（FLASH_ECC）

Address offset: 0x24

Reset value: 0x0000 0000



Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:8	ECCHW	After writing a word to a 32-bit Flash address, the corresponding higher 6-bit ECC value.
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	ECCLW	After writing a word to a 32-bit Flash address, the corresponding lower 6-bit ECC value.

2.2.4.2.11 CAHR register (FLASH_CAHR)

Address offset: 0x30

Reset value: 0x0000 0000

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31	16
Reserved	

15-8	7-4	3-0
Reserved	LOCKSTOP	LOCKSTRT
	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:4	LOCKSTOP[3:0]	iCache lock stop (see for detailed operation instructions 2.2.2.3.3 iCache locking Chapter). 0: disable 1: enable
3:0	LOCKSTRT[3:0]	iCache lock start. 0: disable 1: enable

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3 Power control (PWR)

3.1 General description

PWR is power management unit to control status of different modules in different power modes. Its major function is to control MCU to enter different power modes and wakeup when events or interrupts happen. MCU supports RUN, LOW-POWER RUN, SLEEP, LOW-POWER SLEEP, STOP2 and STANDBY mode.

3.1.1 Power supply

- ✧ The PWR module mainly consists of the following independent power domains: V_{DD}, V_{DDA}, V_{LCD}, V_{REF+}, V_{REF-}. For details, please refer to Figure 3-1 power supply block diagram. In order to illustrate the functions of different power domains, some power domains will be introduced below. This document will introduce the digital part of the power domain in the following chapters.
  - V_{DD} domain: The voltage input range is 1.8V~3.6V, mainly for MR, LPR, COMP, HSE, HSI, PLL, BOR, PVD, TRNG, USB PHY and most digital peripheral interfaces power supply.
  - V_{DDA} domain: The voltage input range is 1.8V~3.6V, which mainly supplies power for most analog peripherals. A/D, D/A, TS (Temperature Sensor) and OPAMP are in this power domain. This independent analog power supply is powered by VSSA, which can filter and shield noise separately, and improve the conversion accuracy performance of analog modules such as A/D and D/A.
  - V_{LCD} domain: The voltage input range is 2.58V~3.6V, V_{LCD} can be used to control the contrast of LCD. The V_{LCD} pin can be used in the following two situations:
    - ➢ It can receive the maximum voltage provided by external circuit (supply voltage for Segment and Common lines LCD through MCU).
    - ➢ It can also be connected to an external capacitor for the boost converter of the MCU. This boost converter is software controlled and provides voltage for Segment and Common lines LCD.

    The voltage supplied to the Segment and Common lines LCD determines the contrast ratio of the LCD. The user reduces contrast by controlling its duty cycle or dead-time.
    - ➢ When an external voltage provides voltage for V_{LCD}, its voltage range should be: 2.58V~3.6V, and independent of V_{DD}.
    - ➢ When the LCD is based on an internal boost converter, V_{LCD} should be connected to a capacitor.
  - V_{REF+} or V_{REF-} domain:
    - ➢ External V_{REF}: V_{REF+} is the input reference voltage for ADC and DAC. When enabled, it is also the output of the internal voltage reference buffer. V_{REF-} must always be equal to V_{SSA}.
    - ➢ Internal V_{REF}: Connected to $V_{REFBUFF}$, the voltage is 2.048V, and V_{DDA} is required not to be lower than 2.4V.
- ✧ The PWR module consists of a main regulator (MR) and a low power regulator (LPR). Two embedded linear regulators power all digital circuits. The regulator is always enabled after reset.

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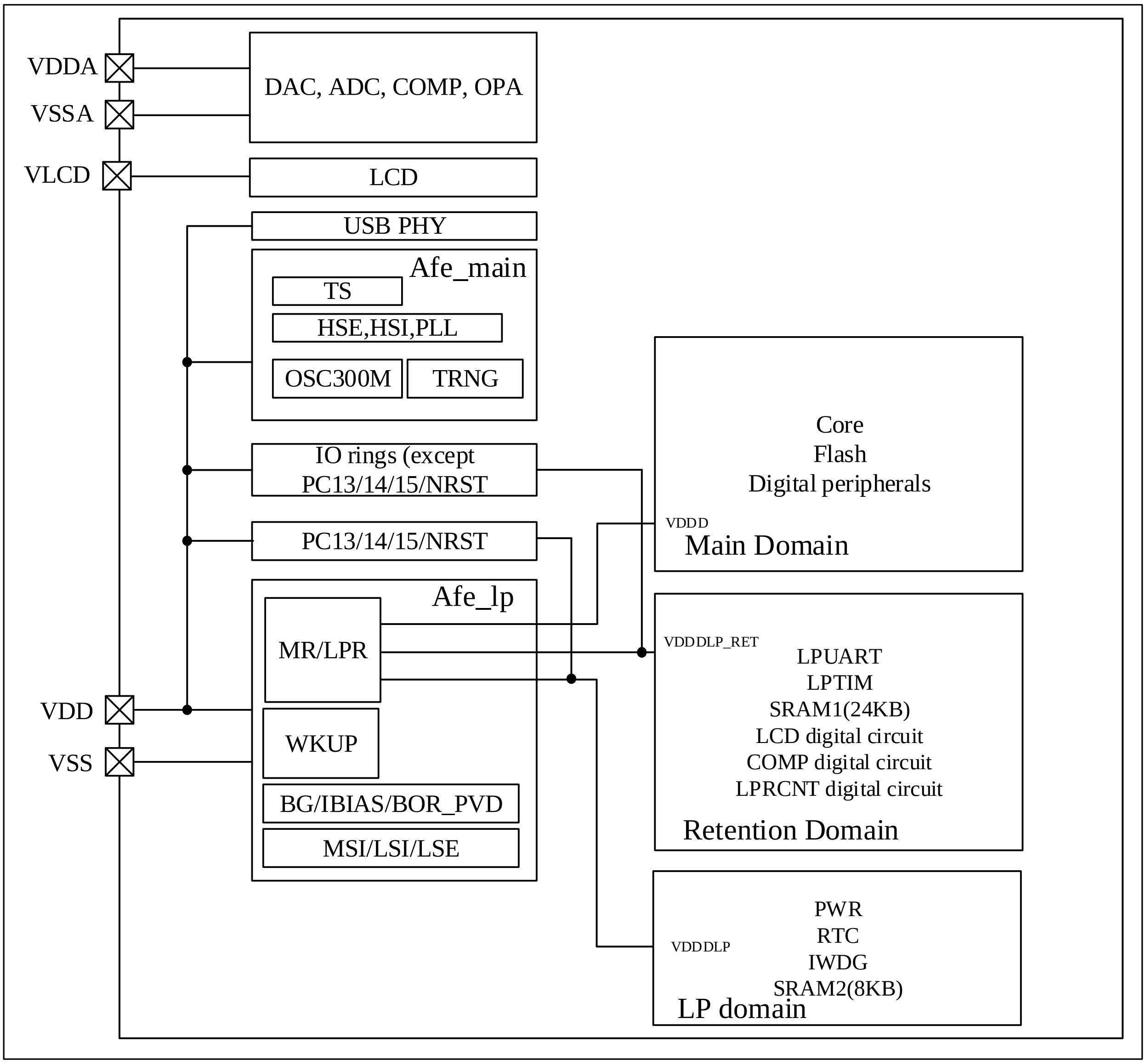
- **MR**

  The output voltage range of MR can be adjusted by PWR_CTRL1.MRSEL[1:0]. It is mainly used in RUN mode and SLEEP mode of MCU. MR is disabled when MCU is in LOW-POWER RUN, LOW-POWER SLEEP, STOP2, STANDBY mode.

- **LPR**

  LPR is used in LOW-POWER RUN mode, LOW-POWER SLEEP mode, STOP2 mode and STANDBY mode. In STOP2 mode, it powers the retention power domain (RET) and the low-power power domain.

Figure 3-1 Power supply block diagram



3.1.2 Power supply supervisor

3.1.2.1 Power on reset (POR) and brown out reset (BOR)

Power-on reset (POR) and brown-out reset (BOR) circuits are integrated inside the chip. BOR is active in all power

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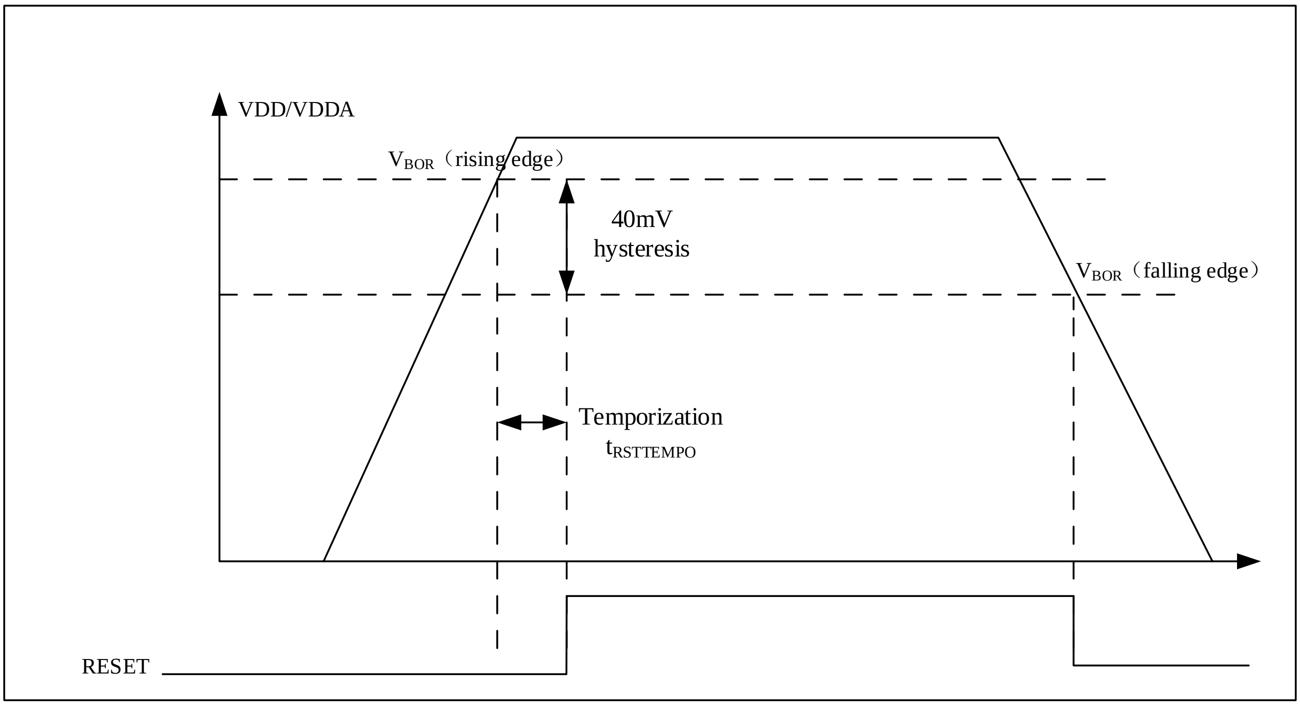
modes and cannot be disabled. Five BOR thresholds can be selected via the option byte.

During power-on, the BOR will hold the chip in reset until the supply voltage (V_{DD}) reaches the specified threshold. When V_{DD} falls below the selected threshold, the chip will be reset. For more information on switching power supply reset thresholds, see the Electrical Characteristics section of the relevant data sheet.

Figure 3-2 Brown-out reset (BOR) waveform



Note: The reset temporization $t_{RSTTEMPO}$ exists only based on the BOR minimum threshold (V_{BOR0}).

3.1.2.2 Programmable voltage detector (PVD)

PVD monitors the power supply by comparing the V_{DD} voltage with the relevant bits in the Power Control Register 2 (PWR_CTRL2). PWR_CTRL2.PLS[2:0] select the threshold for the monitored voltage. Enable PVD by setting PWR_CTRL2.PVDEN.

The PWR_STS2.PVDO flag is used to indicate whether the V_{DD} is above/below the PVD voltage threshold. This event is connected internally to the 16th line of the external interrupt and produces an interrupt if the interrupt is enabled in the external interrupt register. A PVD interrupt occurs when the VDD drops below the PVD threshold and/or when the VDD rises above the PVD threshold, according to the rise/fall edge trigger setting of the external interrupt line 16. For example, this feature can be used to perform emergency shutdown tasks.

PVD can also be configured to monitor the external analog voltage PVD_IN (PB7) (compared to the internal VREFINT (about 1.2V)).

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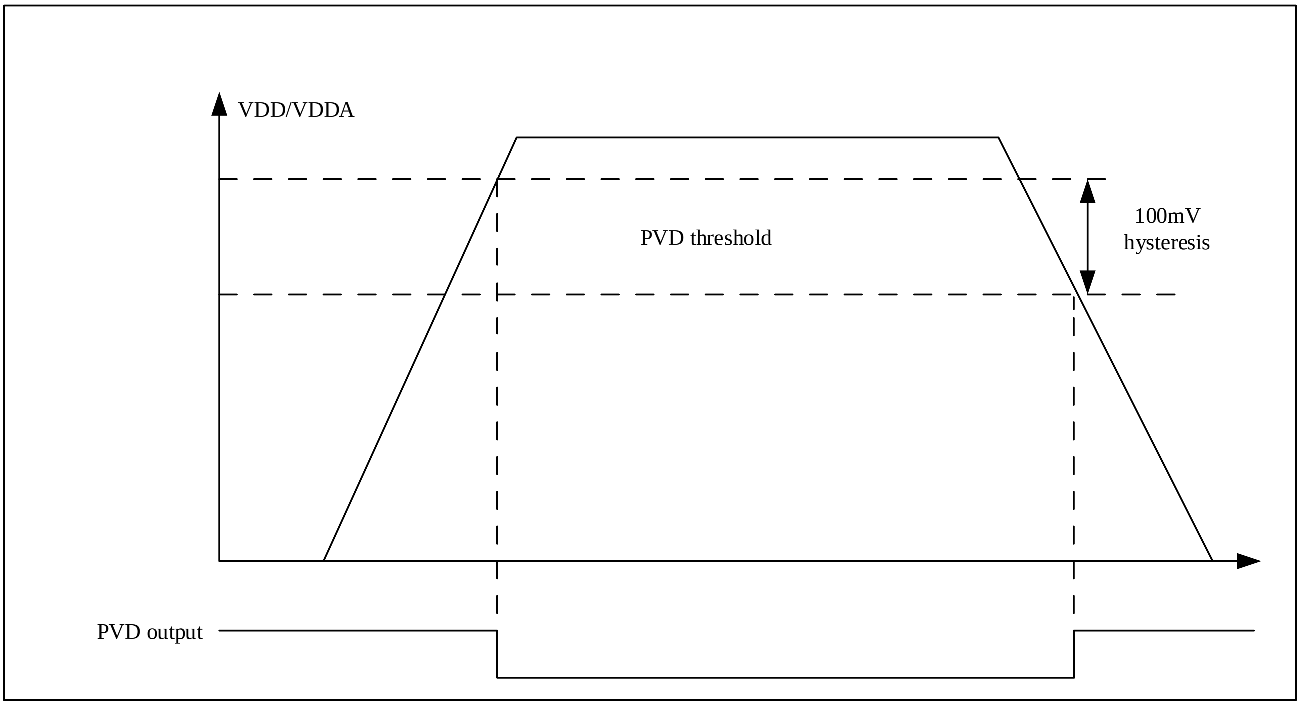
Figure 3-3 PVD threshold waveform



3.2 Power modes

Overall MCU has 6 power modes: RUN, SLEEP, LOW POWER RUN, LOW POWER SLEEP, STOP2 and STANDBY. Different mode has different performance and power consumption. A summary of MCU power modes is shown below.

Table 3-1 Power modes

Mode	Regulator	Enter	Exit	Wakeup state
RUN	MR	Power on, system reset, low power wake-up	Enter another power mode	Code execution continues without peripheral reconfiguration
SLEEP	MR	1) WFI returned from ISR 2) WFE	any interrupt or wake-up event	Code execution continues without peripheral reconfiguration
LOW POWER RUN	LPR	By configuring PWRCTRL1.LPREN bit	Clear PWRCTRL1.LPREN bit or system reset	Code execution continues without peripheral reconfiguration
LOW POWER SLEEP	LPR	To enter LOW POWER RUN first 1) WFI returned from ISR 2) WFE	any interrupt or wake-up event	Code execution continues without peripheral reconfiguration
STOP2	LPR	WFI/WFE： 1）SCB_SCR.SLEEPDEEP = 1 2）PWR_CTRL1.LPMSEL = “000/010”	System reset and all EXTI	Continue to execute the code, peripherals that the user chooses to keep do not need to be

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Mode	Regulator	Enter	Exit	Wakeup state
				reconfigured, USB, CAN need to be reconfigured, MSI = 4M
STANDBY	LPR	WFI/WFE： 1）SCB_SCR.SLEEPDEEP = 1 2）PWR_CTRL1.LPMSEL = “011”	3 WKUP IO rising/falling edges, RTC alarm rising edge, NRST reset, IWDG reset, RTC timestamp, tamper detection	System reset

Note:

1. *STOP2 mode, after wake-up, the code can continue running from the stop position. The RCC configuration is retained, and the SPI/UART2/UART3/UART4/UART5/I2C1/I2C2/WWDG configuration is retained.*
2. *Please refer to the corresponding data sheet for the low power wake-up time.*

The running enable conditions of different modules in different power consumption modes are shown in the following table:

Table 3-2 Blocks running state

Main Blocks	Run	Sleep	Low power run	Low power sleep	Stop2		Standby	
					-	Wakeup capability	-	Wakeup capability
CPU	Y	-	Y	-	-	-	-	-
MMU	O	O	O	O	-	-	-	-
DMA	O	O	O	O	-	-	-	-
FLASH	O	O	O	O	-	-	-	-
SRAM1	Y	Y	Y	Y	O	-	-	-
SRAM2	Y	Y	Y	Y	O	-	O	-
BOR	Y	Y	Y	Y	Y	Y	Y	Y
PVD	O	O	O	O	O	Y	O	-
HSE	O	O	-	-	-	-	-	-
HSI	O	O	-	-	-	-	-	-
LSE	O	O	O	O	O	-	O	-
LSI	O	O	O	O	O	-	O	-
MSI	O	O	Y	Y	O	-	-	-
CSS for HSE	O	O	O	O	-	-	-	-
CSS for LSE	O	O	O	O	O	O	O	O
PLL	O	O	-	-	-	-	-	-
RTC	O	O	O	O	O	Y	O	Y
Tamper	3	3	3	3	3	O	3	O
IWDG	O	O	O	O	O	Y	O	Y
EXTI	Y	Y	Y	Y	Y	-	-	-

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Main Blocks	Run	Sleep	Low power run	Low power sleep	Stop2		Standby	
					-	Wakeup capability	-	Wakeup capability
LPTIM	O	O	O	O	O	Y	-	-
LPUART	O	O	O	O	O	Y	-	-
TIM1/8	O	O	O	O	-	-	-	-
TIM2/3/4/5	O	O	O	O	-	-	-	-
TIM6/7	O	O	O	O	-	-	-	-
WWDG	O	O	O	O	-	-	-	-
USART1/2/3	O	O	O	O	-	-	-	-
UART4/5	O	O	O	O	-	-	-	-
I2C1/2	O	O	O	O	-	-	-	-
SPI1/2	O	O	O	O	-	-	-	-
USB	O	O	-	-	-	-	-	-
UCDR	O	O	-	-	-	-	-	-
CAN	O	O	O	O	-	-	-	-
SAC	O	O	-	-	-	-	-	-
CRC	O	O	O	O	-	-	-	-
DAC	O	O	O	O	-	-	-	-
ADC	O	O	O	O	-	-	-	-
TempSensor	O	O	O	O	-	-	-	-
OPAMP	O	O	O	O	-	-	-	-
COMP	O	O	O	O	O	Y	-	-
TRNG	O	O	-	-	-	-	-	-
LCD	O	O	O	O	O	Y	-	-
GPIOs	O	O	O	O	O	Y	O	3 pins

Note:

1. *Y: Yes (Enable), O: Option, -: Not available.*
2. *Only COMP1 support STOP2 mode*
3. *3 pins represent three wake-up IOs, PA8, PA0 and PC13.*

3.2.1 RUN mode

RUN mode is the normal operation mode of the MCU. The speed of the system clock can be reduced by configuring the RCC register to achieve the purpose of reducing energy consumption, or the peripheral clock can be turned off to reduce power consumption. To further reduce dynamic power consumption, MR output voltage can also be adjusted via PWR_CTRL1.MRSEL. In addition, if the FLASH is not used, the software can write the FLASH_AC.SLMEN bit to put the FLASH into sleep mode to reduce power consumption, and the FLASH_AC.SLMEN bit can also restore the current state of the FLASH.

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3.2.1.1 Dynamic Voltage Regulation (MR)

Steps to enter MR 1.0V:

- Make sure the system clock is at most 72MHz. Note that if the current operating mode is LP RUN, then the maximum system clock is up to 4MHz;
- Configure the FLASH read cycle to be greater than or equal to 2. This step is to avoid entering the low-voltage mode FLASH timing problem;
- Set FLASH_AC.LVMEN to 1, and wait for FLASH_AC.LVMF to be 1, indicating that FLASH has entered the low-voltage mode;
- Reconfigure the FLASH read cycle, the configuration cycle is related to the system clock, and ensure that the read FLASH wait time is greater than 30ns. If the system clock is 72MHz, the period needs to be configured as 2;
- Set SRAM to work in normal mode;
- Configure PWR_CTRL1.MRSEL[1:0] = 0x2, then poll to wait for PWR_STS2.MRF to be pulled low and then pulled high. It takes about 100us to pull down PWR_STS2.MRF.

Steps for MR1.0V → MR 1.1V:

- Configure PWR_CTRL1.MRSEL[1:0] = 0x3, then poll and wait for PWR_STS2.MRF to be pulled low and then pulled high. It takes about 100us to pull down PWR_STS2.MRF;
- Configure the FLASH read cycle to be greater than or equal to 2. This step is to avoid entering the low-voltage mode FLASH timing problem;
- Clear the FLASH_AC.LVMEN bit and wait for the FLASH_AC.LVMF bit to be 0, indicating that the FLASH has exited the low-voltage mode;
- Increase the system clock;
- Configure the FLASH read cycle according to the system clock, and ensure that the read wait time is greater than or equal to 20ns (if it is less than 50MHz, it can be configured to 0).

3.2.2 SLEEP mode

The CPU stops and all peripherals including peripherals around the Cortex®-M4F core (such as NVIC, SysTick, etc.) can run and wake up the CPU when an interrupt or event occurs. In SLEEP mode, all I/O pins maintain the same state/function as in RUN mode.

3.2.2.1 Enter SLEEP mode

Enter SLEEP mode by executing WFI (wait for interrupt) or WFE (wait for event) instruction with SCB_SCR.SLEEPDEEP = 0. Depending on the SCB_SCR.SLEEPONEXIT, there are two options for SLEEP mode entry:

- SLEEP-NOW: If SCB_SCR.SLEEPONEXIT = 0, then WFI or WFE instruction is executed immediately, and the system enters sleep mode immediately.

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- SLEEP-ON-EXIT: If SCB_SCR.SLEEPONEXIT = 1, the system immediately enters sleep mode when exiting from the lowest priority ISR.

3.2.2.2 Exit SLEEP mode

If WFI instruction is used to enter the SLEEP mode, any NVIC interrupts can wake up the device from the SLEEP mode.

If the WFE instruction is used to enter the SLEEP mode, MCU will exit the SLEEP mode immediately when the event occurs. Wake-up events can be generated in the following ways:

- Enable an interrupt in the peripheral control register instead of NVIC, and enable the SCB_SCR.SEVONPEND. When MCU wakes up by WFE, the peripheral interrupt suspend bit and the peripheral NVIC interrupt channel suspend bit (in NVIC interrupt clear suspend register) must be cleared.
- Configure an external or internal EXTI event mode. When the MCU wakes up, it is not necessary to clear the peripheral interrupt suspend bit and the peripheral NVIC interrupt channel suspend bit (in the NVIC interrupt clear suspend register) because the suspend bit corresponding to the event line is not set. This mode provides the shortest wake-up time because there is no time spent on interrupt entry or exit.

3.2.3 LOW POWER RUN mode

In LOW POWER RUN mode, the entire core logic is provided by LPR and MR is disabled. The system clock comes from MSI, the frequency is up to 4MHz, and the PLL is turned off. Executing programs in FLASH or SRAM, all peripherals can be configured to work as required, except USB/ SAC disabled.

3.2.3.1 Enter LOW POWER RUN mode

LOW POWER RUN mode can be entered from RUN mode, or wake-up from LOW POWER SLEEP mode.

Do the following to enter LOW POWER RUN mode:

- Turn off modules that do not support LPRUN, such as USB, algorithm (SAC), etc.;
- Ensure that the system clock is up to 4MHz;
- Configure the FLASH read cycle to be greater than or equal to 2. This step is to avoid entering the low-voltage mode flash timing problem;
- Set the FLASH_AC.LVMEN bit to 1, and wait for the FLASH_AC.LVMF bit to be 1, indicating that the flash has entered the low-voltage mode;
- Reconfigure the FLASH read cycle to 0;
- Set SRAM to work in low voltage mode;
- Configure PWR_CTRL3.BGTLPR = 0 and PWR_CTRL3.PBDTLPR = 0, configure BANDGAP/PVD/BOR to be normally open;
- PWR_CTRL1.LPREN bit is set to 1, use while to wait for PWR_STS2.LPRUNF to be 1. The use of while is to avoid CPU access to SRAM and prevent SRAM timing problems.

Additional steps can be taken to further reduce power consumption:

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- Adjust the LPR output to meet different power or frequency requirements;
- Turn on or off the digital peripheral clock according to actual needs;
- Turn off unnecessary analog peripherals;
- If FLASH is not used, in order to further reduce power consumption, user can configure FLASH_AC.SLMEN = 1 to put FLASH into sleep mode. Configuring FLASH_AC.SLMEN = 0 will restore the current state of FLASH.

It should be noted that LP RUN can switch to LP SLEEP mode, STOP2 mode, STANDBY mode and RUN mode, and can also return from LP SLEEP or STOP2. A system reset also exits LP RUN to RUN mode.

3.2.3.2 Exit LOW POWER RUN mode

The LOW POWER RUN mode can be exited by the following steps:

- Clear PWR_CTRL1.LPREN and wait until PWR_STS2.LPRUNF is set to 1;
- Set the FLASH read delay to greater than 2;
- Clear FLASH_AC.LVMEN and ensure that the FLASH low voltage mode is canceled by polling the FLASH_AC.LVMF bit;
- Restore the system clock to the required state;
- Configure the FLASH read cycle according to the system clock, and ensure that the read wait time is greater than or equal to 20ns (for example, <50MHz, it can be configured to 0).

3.2.4 LOW POWER SLEEP mode

In LOW POWER SLEEP mode, all I/O pins remain in the same state as in RUN mode.

3.2.4.1 Enter LOW POWER SLEEP mode

To enter LOW POWER SLEEP mode, first need to enter LOW POWER RUN mode, and then enter SLEEP mode. The specific steps to enter LOW POWER RUN mode and SLEEP mode are described in Section 3.2.3.1 and Section 3.2.2.1.

3.2.4.2 Exit LOW POWER SLEEP mode

Exiting LOW POWER SLEEP mode is the same as exiting SLEEP mode, any interrupt or event can wake the device from LOW POWER SLEEP mode. For details, see Section 3.2.2.2. It should be noted that the chip will return to LOW POWER RUN mode after waking up from LOW POWER SLEEP mode.

3.2.5 STOP2 mode

STOP2 mode is based on Cortex®-M4F deep sleep mode, all core digital logic areas are powered off. Main voltage regulator (MR) off, HSE/HSI/PLL off, MSI/LSE/LSI optional operation. CPU registers, 80-byte backup registers, RCC, SPI1/2, UART4/5, USART2/3, I2C1/2 and WWDG register retention. The RET domain and the low-power power domain are still functioning normally.

SRAM1/2 can be configured to be retained in STOP2 mode via PWR_CTRL3.RAM1RET and

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PWR_CTRL3.RAM2RET. All I/O pins except PC13/14/15 are in retention state by default, PC13/14/15 can be configured to retention the same state as run mode.

3.2.5.1 Enter STOP2 mode

To enter STOP2 mode, should be configured: SCB_SCR.SLEEPDEEP = 1, PWR_CTRL1.LPMSEL = "000~010".

In STOP2 mode, if FLASH is being operated, the time to enter STOP2 mode will be delayed until the memory access is completed.

If the access to the APB area is in progress, the time to enter the STOP2 mode will be delayed until the APB access is completed.

In STOP2 mode, the following peripherals are available:

- Independent Watchdog (IWDG) optional: Once enabled, it will keep counting until a reset is generated.
- RTC optional: It can be turned on by RCC_LDCTRL.RTCEN.
- Internal RC oscillator (LSI RC) optional: It can be turned on by RCC_CTRLSTS.LSIEN.
- External 32.768kHz crystal oscillator (LSE OSC) optional: It can be turned on by RCC_LDCTRL.LSEEN bit.
- Other peripherals that can choose to hold or work such as GPIO, COMP, EXTI, LPUART, LPTIMER, LCD, LPRCNT.
- IO can be configured to retention or high-Z state.

Unneeded analog peripherals such as ADC and DAC can be disabled when entering STOP2 mode to avoid unnecessary power consumption.

3.2.5.2 Exit STOP2 mode

When the STOP2 mode is exited by an interrupt or a wake-up event via the EXTI line, the system clock will be restored to its previous state, and the code execution will continue from where it left off. System reset (NRST, IWDG) can also exit STOP2 mode.

Note: When a system reset occurs, the CPU will run from address 0.

3.2.6 STANDBY mode

STANDBY mode is a Cortex®-M4 based Deep-Sleep mode. The core domain is completely turned off, the PLL, HSI, HSE are turned off, and the LSI and LSE are optionally run. SRAM2 optional retention, RTC and IWDG optional work. All GPIO pin states are selectable as retention or high-Z.

Note: The GPIO pin state will change to the system default state upon exit.

3.2.6.1 Enter STANDBY mode

Enter STANDBY mode by executing WFI/WFE and setting SCB_SCR.SLEEPDEEP = 1 and PWR_CTRL1.LPMSEL = "011".

If FLASH is being operated, the time to enter STANDBY mode will be delayed until the memory access is completed.

If the access to the APB area is in progress, the time to enter the STANDBY mode will be delayed until the APB

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access is completed.

In STANDBY mode, the following peripherals are available:

- Independent Watchdog (IWDG) optional: Once enabled, it will keep counting until a reset is generated.
- RTC optional: It can be turned on by RCC_LDCTRL.RTCEN.
- Internal RC oscillator (LSI RC) optional: It can be turned on by RCC_CTRLSTS.LSIEN.
- External 32.768kHz crystal oscillator (LSE OSC) optional: It can be turned on by RCC_LDCTRL.LSEEN bit.

Unneeded analog peripherals such as ADC and DAC can be disabled when entering STANDBY mode to avoid unnecessary power consumption.

3.2.6.2 Exit STANDBY mode

MCU exits STANDBY mode when external reset (NRST pin), IWDG reset, rising/falling edge of WKUP pin or RTC alarm event, timestamp event, tamper event occurs. Except for the power status registers (PWR_STS1/2), all registers are reset after waking up from STANDBY state.

After waking up from STANDBY mode, code execution is the same as reset (detecting BOOT pin, getting reset vector, etc.). The PWR_STS1.STBYF flag indicates that the MCU exits STANDBY mode.

3.3 Low-power auto-wakeup (AWU) mode

In automatic wake-up mode, the RTC can be used to wake up from different low-power modes without relying on external interrupts. The RTC provides a programmable clock reference for timed wake-up from SLEEP, STOP2 and STANDBY modes. To do this, two of the three optional RTC clock sources can be selected by software programming RCC_LDCTRL.RTCSEL[1:0] as follows:

- 32.768kHz external crystal clock (LSE OSC)

  This clock source provides an accurate clock reference with very low power consumption.

- RC internal crystal clock (LSI RC)

  This clock source has the advantage of saving the cost of the 32.768 kHz crystal, but the clock accuracy is worse than the LSE.

To wake up from STOP2 mode using the RTC alarm event, you need:

- Configure EXTI 18 rising edge trigger.
- Configure RTC to enable RTC alarm event.

To wake up from STANDBY mode using RTC alarm event, EXTI 18 does not need to be configured. PWR_CTRL3.IWKUPLEN needs to be configured.

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3.4 PWR registers

3.4.1 PWR register overview

Table 3-3 PWR register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	PWR_CTRL1	Reserved																	LPREN	Reserved			MRSEL[1:0]		DRBP	Reserved					LPMSEL[2:0]		
	Reset Value																		0				1	1	1						0	0	0
004h	PWR_CTRL2	Reserved																											PVDFLTEN	PLS[2:0]			PVDEN
	Reset Value																												0	0	0	0	0
008h	PWR_CTRL3	Reserved										PSTSTP2	PSTSTBY	Reserved	PBDTSTBY	PBDTSTP2	PBDTLPR	Reserved	IWKUPLEN	RAM2RET	RAM1RET	Reserved	BGDTSTBY	BGDTSTP2	BGDTLPR	Reserved	WKUP2PS	WKUP1PS	WKUP0PS	Reserved	WKUP2EN	WKUP1EN	WKUP0EN
	Reset Value											0	0		1	1	1		0	0	0		1	1	1		0	0	0		0	0	0
00Ch	PWR_STS1	Reserved																IWKUPF	Reserved						STBYF	Reserved					WKUPF2	WKUPF1	WKUPF0
	Reset Value																	0							0						0	0	0
010h	PWR_STS2	Reserved																													PVDO	MRF	LPRUNF
	Reset Value																														0	1	1
014h	PWR_STSCLR	Reserved																							CLRSTBY	Reserved					CLRWKUP2	CLRWKUP1	CLRWKUP0
	Reset Value																								0						0	0	0

3.4.2 Power control register 1 (PWR_CTRL1)

Address offset: 0x00

Reset value: 0x0000 0700 (reset by wakeup from STANDBY mode)

31:16
Reserved

15	14	13:11	10:9	8	7:3	2:0
Reserved	LPREN	Reserved	MRSEL[1:0]	DRBP	Reserved	LPMSEL[2:0]
	rw		rw	rw		rw

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
14	LPREN	LOW POWER RUN mode enable bit. When this bit is set, the MR is turned off and the LPR will be used to power the main power domain. Note: This bit is affected by system reset.
13:11	Reserved	Reserved, the reset value must be maintained.
10:9	MRSEL[1:0]	Main voltage regulator voltage configuration level selection. 01: Reserved 10: 1.0V (Rang1) 11: 1.1V (Rang0)
8	DRBP	Disable RTC, backup registers and write protection of RCC_LDCTRL register. In the reset state, the RTC, backup registers and RCC_LDCTRL registers are protected from illegal writes. This bit must be set to enable write access to these registers. 0: Disable access to RTC, backup registers and RCC_LDCTRL 1: Enable access to RTC, backup registers and RCC_LDCTRL Note: This bit must remain 1 if HSE is divided by 32 as the RTC clock.
7:3	Reserved	Reserved, the reset value must be maintained.
2:0	LPMSEL [2:0]	Low power mode selection bits. These bits select the low power mode the CPU enters. 000-010: STOP2 mode 011: STANDBY mode

3.4.3 Power control register 2 (PWR_CTRL2)

Address offset: 0x04

Reset value: 0x0000 0000 (reset by wakeup from STANDBY mode or system reset)

31–16
Reserved

15–5	4	3–1	0
Reserved	PVDFLTEN	PLS[2:0]	PVDEN
	rw	rw	rw

Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained.
4	PVDFLTEN	PVD filter enable bit. 0: Disable PVD filtering 1: Enable PVD filtering
3:1	PLS[2:0]	PVD threshold. PLS[2:0] / Voltage 000 / 2.1v 001 / 2.25v

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Bit field	Name	Description
		010 2.4v 011 2.55v 100 2.7v 101 2.85v 110 2.95v 111 （1） *Remarks: (1) is the external input analog voltage PVD_IN (internally compared with VREFINT)*
0	PVDEN	Programmable Voltage Detector (PVD) enable bit. 0: Disable PVD 1: Enable PVD

3.4.4 Power control register 3 (PWR_CTRL3)

Address offset: 0x08

Reset value: 0x0007 0700 (reset by wakeup from STANDBY mode)

31:22	21	20	19	18	17	16
Reserved	PSTSTP2	PSTSTBY	Reserved	PBDT STBY	PBDT STP2	PBDT LPR
	rw	rw		rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	IWKUPL EN	RAM2R ET	RAM1R ET	Reserved	BGDT STBY	BGDT STP2	BGDT LPR	Reserved	WKUP2 PS	WKUP1 PS	WKUP0 PS	Reserved	WKUP2 EN	WKUP1 EN	WKUP0 EN
	rw	rw	rw		rw	rw	rw		rw	rw	rw		rw	rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	PSTSTP2	Pin state bit in STOP2 mode. 0: Pin in retention state 1: Pin in high-Z state
20	PSTSTBY	Pin state bit in STANDBY mode. 0: Pin in retention state 1: Pin in high-Z state
19	Reserved	Reserved, the reset value must be maintained.
18	PBDTSTBY	PVDBOR state bit in STANDBY mode. 0: Normal mode 1: Duty on mode
17	PBDTSTP2	PVDBOR state bit in STOP2 mode. 0: Normal mode 1: Duty on mode
16	PBDTLPR	PVDBOR state bit in LP RUN mode. 0: Normal mode 1: Duty on mode

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Bit field	Name	Description
15	Reserved	Reserved, the reset value must be maintained.
14	IWKUPLEN	Internal wake-up line enable bit. 0: Disable internal wake-up line 1: Enable internal wake-up line
13	RAM2RET	SRAM2 retention bit. SRAM2 supports selection of retention in STANDBY or STOP2 mode. 0: No retention 1: Retention
12	RAM1RET	SRAM1 retention bit. SRAM1 only supports selection of retention in STOP2 mode. 0: No retention 1: Retention
11	Reserved	Reserved, the reset value must be maintained.
10	BGDTSTBY	BANDGAP/BG_Buffer/IBIAS idle state bit in STANDBY mode. 0: Always on 1: Duty on
9	BGDTSTP2	BANDGAP/BG_Buffer/IBIAS idle state bit in STOP2 mode. 0: Always on 1: Duty on
8	BGDTLPR	BANDGAP/BG_Buffer/IBIAS idle state bit in LP RUN mode. 0: Always on 1: Duty on
7	Reserved	Reserved, the reset value must be maintained.
6	WKUP2PS	WKUP2 wake-up pin polarity selection bit. Use rising or falling edge to wake up STANDBY mode. Make sure the corresponding wakeup pins are disabled before changing polarity. 0: Rising edge 1: Falling edge
5	WKUP1PS	WKUP1 wake-up pin polarity selection bit. Use rising or falling edge to wake up STANDBY mode. Make sure the corresponding wakeup pins are disabled before changing polarity. 0: Rising edge 1: Falling edge
4	WKUP0PS	WKUP0 wake-up pin polarity selection bit. Use rising or falling edge to wake up STANDBY mode. Make sure the corresponding wakeup pins are disabled before changing polarity. 0: Rising edge 1: Falling edge
3	Reserved	Reserved, the reset value must be maintained.
2	WKUP2EN	Enable WKUP2 pin. Software can set and clear this bit.

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Bit field	Name	Description
		0: WKUP pin is used for general purpose I/O. An event on the WKUP pin will not wake the device from STANDBY mode. 1: WKUP pin is used to wake up STANDBY mode.
1	WKUP1EN	Enable WKUP1 pin. Software can set and clear this bit. 0: WKUP pin is used for general purpose I/O. An event on the WKUP pin will not wake the device from STANDBY mode. 1: WKUP pin is used to wake up STANDBY mode.
0	WKUP0EN	Enable WKUP0 pin. Software can set and clear this bit. 0: WKUP pin is used for general purpose I/O. An event on the WKUP pin will not wake the device from STANDBY mode. 1: WKUP pin is used to wake up STANDBY mode.

3.4.5 Power status register 1 (PWR_STS1)

Address offset: 0x0C

Reset value: 0x0000 0000 (Power-on reset or PWR soft reset clear)

31:16
Reserved

15	14:9	8	7:3	2	1	0
IWKUPF	Reserved	STBYF	Reserved	WKUPF2	WKUPF1	WKUPF0
r		r		r	r	r

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	IWKUPF	Internal wake-up flag. This bit is set and cleared by hardware. 0: All internal wakeup sources have been cleared 1: Device wakes up from STANDBY mode by internal wakeup source
14:9	Reserved	Reserved, the reset value must be maintained.
8	STBYF	STANDBY flag bit. This bit is set by hardware when the device enters STANDBY mode and cleared by software by setting PWR_STSCLR.CLRSTBY or by a power-on reset. 0: The device has never entered STANDBY mode 1: The device has ever entered STANDBY mode Note: A system reset will not clear this bit.
7:3	Reserved	Reserved, the reset value must be maintained.
2	WKUPF2	WKUP2 pin wakeup flag. This bit is set by hardware. Can be cleared by software setting

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Bit field	Name	Description
		PWR_STSCLR.CLRWKUP2. 0: No wakeup event occurred 1: Wakeup event received from WKUP pin
1	WKUPF1	WKUP1 pin wakeup flag. This bit is set by hardware. Can be cleared by software setting PWR_STSCLR.CLRWKUP1. 0: No wakeup event occurred 1: Wakeup event received from WKUP pin
0	WKUPF0	WKUP0 pin wakeup flag. This bit is set by hardware. Can be cleared by software setting PWR_STSCLR.CLRWKUP0. 0: No wakeup event occurred 1: Wakeup event received from WKUP pin

3.4.6 Power status register 1 (PWR_STS1)

Address offset: 0x10

Reset value: 0x0000 0003 (Power-on reset or PWR soft reset clear)

31–16
Reserved

15–3	2	1	0
Reserved	PVDO	MRF	LPRUNF
	r	r	r

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	PVDO	PVD output. This bit is set and cleared by hardware. Only valid when PWR_CTRL2.PVDEN = 1. 0: VDD/VDDA is above the PVD threshold selected using PWR_CTRL2.PLS[2:0]. 1: VDD/VDDA is below the PVD threshold selected using PWR_CTRL2.PLS[2:0].
1	MRF	Voltage adjustment flag. 0: Voltage adjustment is in progress 1: Voltage adjustment is completed
0	LPRUNF	Low power voltage regulator flag. This bit is cleared by hardware when MCU is in LOW POWER RUN mode. This bit remains 0 when MCU exits LOW POWER RUN mode and is set to 1 by hardware until the voltage regulator is ready in master mode. This bit must be polled before increasing the frequency. 0: MCU is in LOW POWER RUN mode 1: MCU is in RUN mode

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3.4.7 Power status clear register (PWR_STSCLR)

Address offset: 0x14

Reset value: 0x0000 0000

31:16
Reserved

15:9	8	7:3	2	1	0
Reserved	CLRSTBY	Reserved	CLR WKUP2	CLR WKUP1	CLR WKUP0
	w		w	w	w

Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	CLRSTBY	Clear STANDBY flag. This bit always reads as 0. 0: No effect. 1: Clear PWR_STS1.STBYF flag.
7:3	Reserved	Reserved, the reset value must be maintained.
2	CLRWKUP2	Clear WKUP2 wakeup flag. This bit always reads as 0. 0: No effect. 1: Clear wakeup flag PWR_STS1.WKUPF2.
1	CLRWKUP1	Clear WKUP1 wakeup flag. This bit always reads as 0. 0: No effect. 1: Clear wakeup flag PWR_STS1.WKUPF1.
0	CLRWKUP0	Clear WKUP0 wakeup flag. This bit always reads as 0. 0: No effect. 1: Clear wakeup flag PWR_STS1.WKUPF0.

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4 Reset and clock control (RCC)

4.1 Reset Control Unit

Supports the following three types of reset:

- Power Reset
- System Reset
- Low power domain Reset

4.1.1 Power reset

A Power reset occurs in the following circumstances:

- Power-on reset (POR reset).
- Brown-out reset(BOR reset).
- When exiting STANDBY mode.

When returning from STANDBY mode, resets all registers except low-power domains.

Other generated power resets will reset all registers (see Figure 3-1).

The reset source in the figure will finally act on the NRST pin and remain low during the reset process.

4.1.2 System reset

Except the reset flags in the Control/Status Register (RCC_CTRLSTS)and the registers in the low power domain (see Figure 3-1), a system reset sets all registers to their reset values.

A system reset is generated when one of the following events occurs:

- A low level on the NRST pin (external reset)
- Window watchdog end of count condition (WWDG reset)
- Independent watchdog end of count condition (IWDG reset)
- Software reset (SW reset)
- Low power management reset
- MMU protection reset
- RAM parity error reset
- EMC reset

The reset source can be identified by checking the reset flags in the Control/Status Register (RCC_CTRLSTS) and Low Power Domain Control Register(RCC_LDCTRL).

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4.1.2.1 Software reset

A software reset can be generated by setting the SYSRESETREQ bit in Cortex™-M4 Application Interrupt and Reset Control Register. Refer to Cortex™-M4 technical reference manual for further information.

4.1.2.2 Low-power management reset

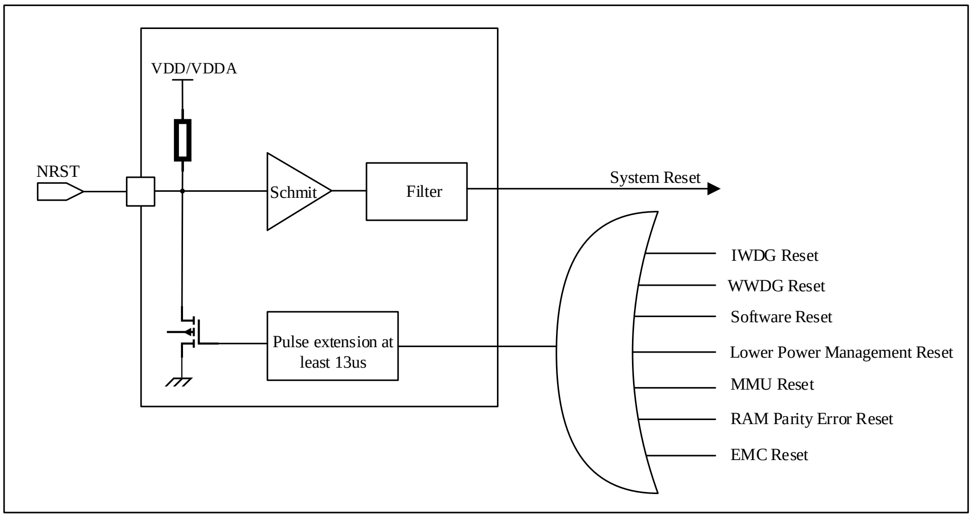
Low-power management reset can be generated by using the following methods:

- Generate low power management reset when entering STANDBY mode: This reset is enabled by setting the nRST_STDBY bit in the user option byte. At this time, even if the procedure to enter STANDBY mode is performed, the system will be reset instead of entering STANDBY mode.
- Generate low power management reset when entering STOP2 mode: This reset is enabled by setting the nRST_STOP2 bit in the user option byte. At this time, even if the process to enter STOP2 mode is performed, the system will be reset instead of entering STOP2 mode.

The system reset signal provided to the chip is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 13μs for each reset source (external or internal). For external reset, the reset pulse is generated while the NRST pin is asserted low.

The Figure below shows the system reset generation circuit.

Figure 4-1 System reset generation



4.1.3 Low power domain reset

A low power domain reset is generated when one of the following events occurs:

- Software reset: The low power domain reset can be generated by setting the RCC_LDCTRL.LDSFTRST bit.
- VDD power up/down will cause a low power domain reset.

4.2 Clock control unit

Four different clock sources can be used to drive the system clock (SYSCLK):

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- HSI oscillator clock,16MHz;
- HSE oscillator clock, 4~32MHz;
- MSI oscillator clock:

  The frequency can be configured to 100KHz/200KHz/400KHz/800KHz/1MHz/2MHz/4MHz, the default is 4MHz;

  Automatically enable the clock after power-on reset, system reset or wake-up from Standby mode;

  Configurable clock source for low power mode;
- PLL clock, Up to 108MHz;

After booting from reset, MSI is used as system clock source, configured as 4 MHz.

The devices have the following two secondary clock sources:

- LSI: 40 kHz low-speed internal RC which drives independent watchdog (IWDG) can be selected by software to drive RTC/LPTIMER.
- LSE: 32.768 kHz low-speed external crystal can also be selected by software to drive RTC/LPTIMER/LPUART.

Each clock source can be turned on or off independently when it is not used to optimize power consumption.

Several prescalers can be used to configure the frequencies of the AHB, the high-speed APB (APB2), and the low-speed APB (APB1) domains. The maximum frequencies of the AHB, APB2, and APB domains are 108MHz, 54MHz, and 27MHz respectively.

RCC provides the Cortex System Timer (SysTick) external clock with the AHB clock (HCLK) divided by 8. This clock or Cortex clock(HCLK) can be selected to drive the SysTick by programming the SysTick Control and Status Register. The ADC clock is generated by dividing the AHB clock or PLL clock.

The clock frequencies of timers are automatically set by hardware. There are two scenarios:

- If the APB prescaler is 1, the timer clock frequencies are set to the same frequency as that of the APB domain to which the timers are connected.
- Otherwise, they are set to twice the frequency of the APB domain to which the timers are connected.

FCLK is the free-running clock of Cortex™-M4F. For more details, refer to the ARM Cortex™-M4 technical reference manual.

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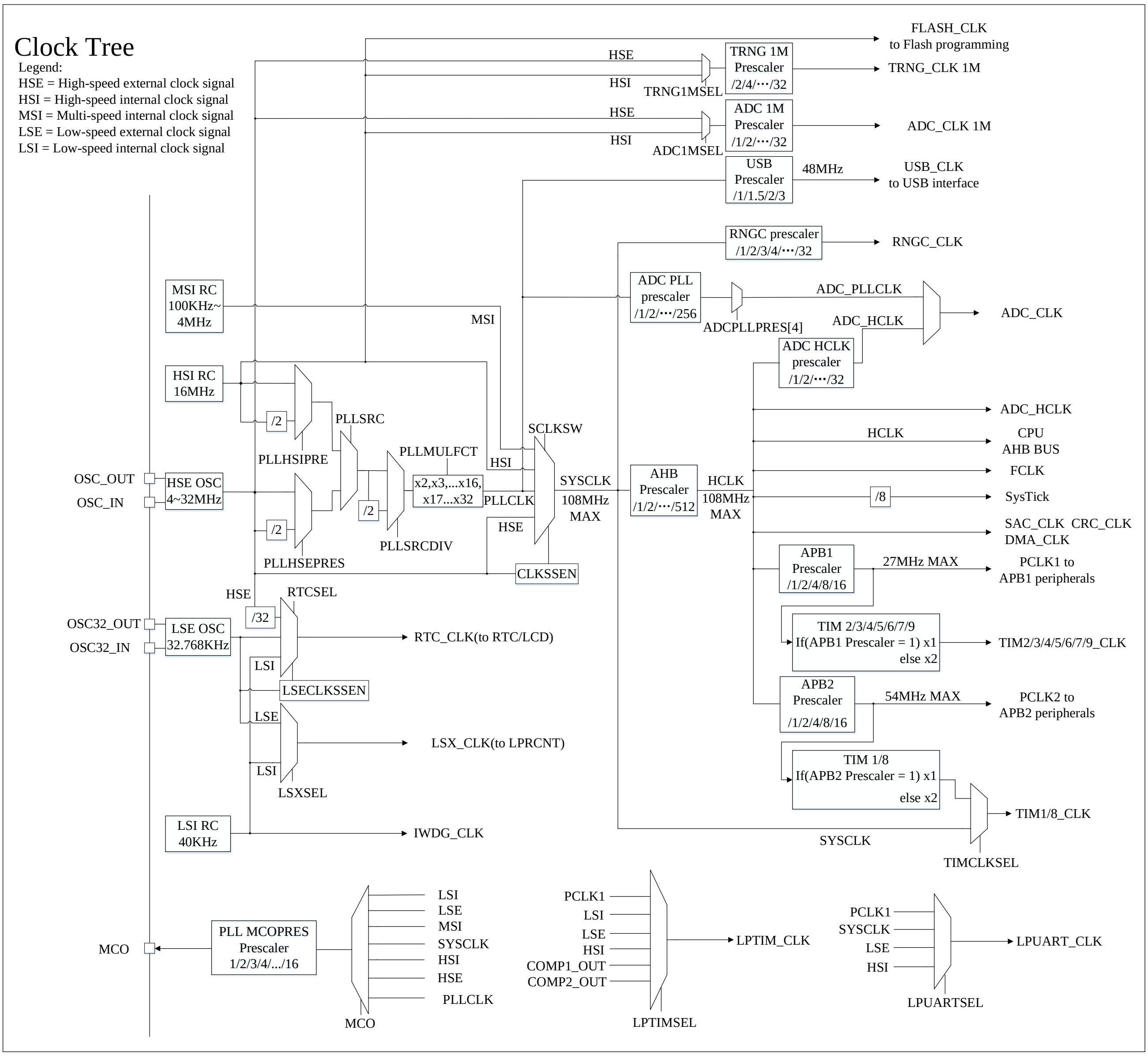
4.2.1 Clock Tree Diagram

Figure 4-2 Clock Tree



1. The maximum frequency available for the system clock is 108MHz.
2. For more details about the internal and external clock source characteristics, please refer to the "Electrical Characteristics" section in the product datasheet.
3. When PLL is selected as system clock source, PLL minimum clock output is 32MHz.

4.2.2 HSE clock

The high-speed external clock signal (HSE) can be generated from the following two clock sources:

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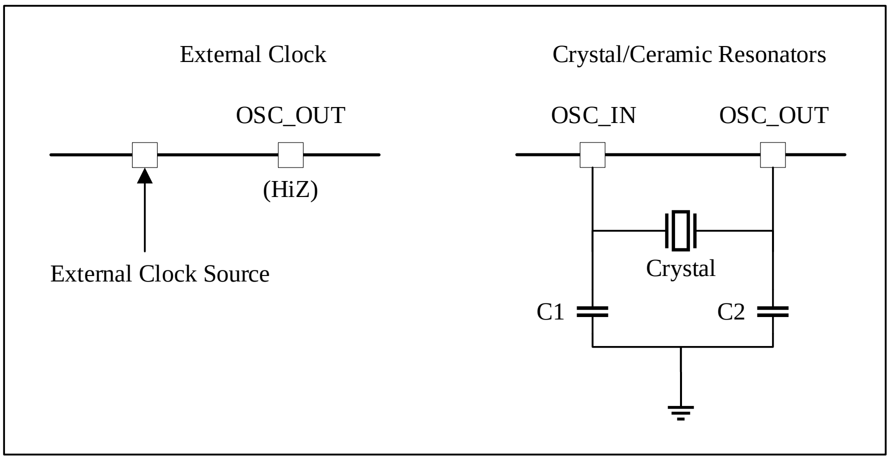
- HSE external crystal/ceramic resonator
- HSE user external clock

To reduce distortion of the clock output and shorten the start-up Stablize time, the crystal/ceramic resonator and load capacitor must be placed as close as possible to the oscillator pins. The load capacitance value must be adjusted according to the chosen oscillator.

Figure 4-3 HSE/LSE clock source



4.2.2.1 External clock source (HSE bypass)

In this mode, an external clock source must be provided. Its frequency can be up to 32MHz. Users can select this mode by setting the RCC_CTRL.HSEBP and RCC_CTRL.HSEEN bits. The external clock signal(50% duty cycle square, sine or triangle wave) must be connected to the OSC_IN pin while the OSC_OUT pin must be left floating (Hi-Z). See Figure 4-3.

The RCC_CTRL.HSERDF bit is used to indicate whether the external clock is stable. At startup, until this bit is set by hardware, the clock was released.

4.2.2.2 External crystal/ceramic resonator (HSE crystal)

The 4 to 32 MHz external oscillator has the advantage of producing a more accurate master clock for the system. The associated hardware configuration is shown in See Figure 4-3. For more details, please refer to the electrical characteristics section of the datasheet.

The RCC_CTRL.HSERDF bit indicates whether the high-speed external oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock Interrupt Register (RCC_CLKINT).

HSE clock can be switched on and off by setting the RCC_CTRL.HSEEN bit.

4.2.3 HSI clock

The HSI (High Speed Internal) clock signal is generated by an internal 16MHz RC oscillator and can be used directly as system clock or as PLL input after dividing by 1 or 2 (selected by RCC_PLLHSIPRE.PLLHSIPRE bit to divide by 1 or 2). The HSI RC oscillator can provide a clock source without any external devices. It also has a shorter startup

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time than the HSE crystal oscillator. However, its frequency is less accurate even with calibration.

The HSI clock frequency of each chip has been calibrated to 1% (25 ℃) before leaving the factory. After the system reset, the factory calibration value is loaded into the RCC_CTRL.HSICAL[8:0] bits.

If the user application is subject to voltage or temperature variations, this may affect the accuracy of the RC oscillator. The HSI frequency can be trimmed by using the RCC_CTRL.HSITRIM[4:0] bits.

The RCC_CTRL.HSIRDF bit flag indicates if the HSI RC oscillator is stable. At startup, the HSI RC output clock is not released until this bit is set by hardware. HSI clock can be switched on and off using the RCC_CTRL.HSIEN bit.

Note:

1. *HSI after Reflow, the frequency will drift,Refer to the HSI oscillator characteristics table in the datasheet for detailed electrical parameters of HSI。*

4.2.4 MSI clock

The MSI (Multi Speed Internal) clock signal is generated from the internal RC oscillator. The frequency range can be selected by software using the RCC_CTRLSTS.MSIRANGE[3:0] bits. There are 7 frequency ranges available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default).

After power-on reset, system reset or wake-up from STANDBY mode, the MSI clock is used as the system clock and the MSI frequency is set to its default value of 4 MHz.

The RCC_CTRLSTS.MSIRD bit indicates whether the MSI is stable. The MSI output clock cannot be used until the hardware sets this bit to 1 at startup. MSI can be turned on or off with the RCC_CTRLSTS.MSIEN bit.

If the HSE crystal oscillator fails, the MSI clock will be used as a backup clock source for the system clock. Refer to Section 4.2.9 Clock Security System.

Note:

1. *MSI after Reflow, the frequency will drift,Refer to the MSI oscillator characteristics table in the datasheet for detailed electrical parameters of MSI。*

4.2.5 PLL clock

The internal PLL can be used to multiply the HSI or the HSE clock frequency. Refer to Figure 4-2 Clock Tree,The PLL configuration (selection of PLL input clock (HSI/HSE and divider) and multiplication factor) must be done before enabling PLL. Once the PLL is enabled, these parameters cannot be changed. The PLL can be configured using control bits in RCC_CTRL and RCC_CFG registers.

After selecting HSI or HSE (both can be divided by 1 or 2) as the clock source, you can continue to select the frequency divided by 1 or 2 as the final PLL input clock, see Figure 4-4

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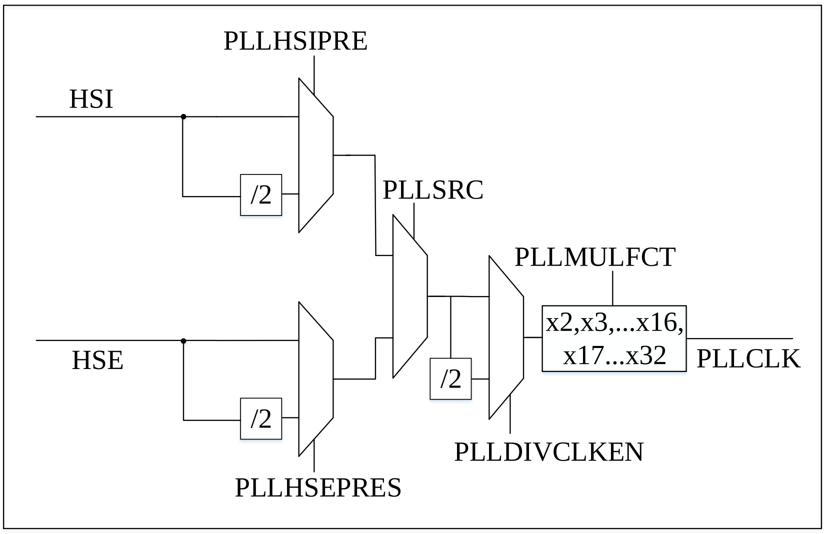
Figure 4-4 PLL clock source selection



If the PLL interrupt is enabled in the clock interrupt register, an interrupt request can be generated when the PLL is ready.

If the USB interface needs to be used in the application, the PLL must be set to output 48, 72, 96MHz clocks to provide the 48MHz USBCLK clock.

4.2.6 LSE clock

The LSE crystal is a 32.768KHz low speed external crystal or ceramic resonator. It provides a low-power and accurate clock source for the real-time clock or other timing functions.

The LSE clock is enabled and disabled by the RCC_LDCTRL.LSEEN bit.

The RCC_LDCTRL.LSERD bit indicates whether the LSE clock is stable. During the startup phase, the LSE clock signal is not released until this bit is set by hardware. If enabled in the clock interrupt register, an interrupt request can be generated.To turn off LSE,you need to waif for 3 LSE clocks to turn it off completely.LSE enabled by repeat switch needs to wait for 1024 LSE clocks RCC_LDCTRL.LSEEN bit to set.

4.2.6.1 LSE external clock source(LSE bypass)

In this mode, an external clock source with a frequency of up to 1 MHz can be provided. Users can select this mode by setting the RCC_LDCTRL.LSEBP and RCC_LDCTRL.LSEEN bits. The external clock signal(square, sine or triangle wave) with 50% duty cycle must be connected to the OSC32_IN pin while the OSC32_OUT pin must be left floating (Hi-Z).

4.2.7 LSI clock

The LSI RC can clock the IWDG and AWU in STOP2 and STANDBY modes. The LSI clock frequency is about 40kHz. For further information please refer to the Electrical Characteristics section of the data sheet.

The LSI clock can be turned on or off using the RCC_CTRLSTS.LSIEN bit.

The RCC_CTRLSTS.LSIRD bit flag indicates if the LSI clock is stable. At startup, the clock is not released until this

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bit is set by hardware. An interrupt can be generated if enabled in the Clock Interrupt Register (RCC_CLKINT).

4.2.7.1 LSI calibration

The internal low-speed oscillator LSI can be calibrated to compensate for its frequency offset to obtain an RTC time base with acceptable accuracy, and an independent watchdog (IWDG) timeout (when these peripherals are clocked from the LSI).

Calibration can be achieved by measuring the LSI clock frequency using the TIM9's input clock (TIM9_CLK). The measurement is guaranteed by the accuracy of the HSE. The software can obtain the accurate RTC clock base by adjusting the 20 bit prescaler of the RTC, and obtain the accurate independent watchdog (IWDG) timeout time by calculation.

The LSI calibration steps are as follows:

1. Turn on TIM9 and set channel 3 to input capture mode;

2. Set the TIM9_CTRL1.C3SEL bit to 1, and connect the LSI to channel 3 of TIM9 internally;

3. Measure LSI clock frequency through TIM9 capture/compare 3 events or interrupts;

4. Set the 20 bit prescaler based on the measurement results and the desired RTC time base and independent watchdog timeout.

4.2.8 System clock (SYSCLK) selection

The system clock (SYSCLK) has four clock sources: MSI, HSI, HSE, PLL.

The maximum frequency of the system clock is 108 MHz. After a system reset, the MSI oscillator (with a reset frequency of 4MHz) is selected as the system clock. It cannot be stopped when the clock source is used directly or indirectly through the PLL as the system clock.

Switching from one clock source to another will only occur when the target clock source is ready (either after a delay to start the stabilization phase or PLL stabilization). When the selected clock source is not ready, the switching of the system clock will not occur until the target clock source is ready.

4.2.9 Clock security system (CLKSS)

Clock security system can be activated by software by setting the RCC_CTRL.CLKSSEN bit. Once activated, the clock detector is enabled after the startup delay of the HSE oscillator, and disabled when the HSE clock is turned off.

If the HSE clock fails, the HSE oscillator will be automatically turned off, and a clock failure event will be sent to the break input of the advanced timers (TIM1 and TIM8), and the Clock Security System Interrupt CLKSSIF will be generated, allowing the software to execute rescue operations. The CLKSSIF interrupt is connected to the NMI (Non-Maskable Interrupt) interrupt of the Cortex™-M4.

Once the CSS is activated and the HSE clock fails, the CSS interrupt is generated and the NMI is automatically generated. The NMI will be executed continuously until the CSS interrupt pending bit is cleared. Therefore, it is necessary to clear the CSS interrupt by setting the RCC_CLKINT.CLKSSICLR bit in the NMI handler.

If the HSE oscillator is directly or indirectly used as the system clock (indirectly means: it is used as the PLL input

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clock, and the PLL clock is used as the system clock), the clock failure will cause a switch of the system clock to the MSI oscillator and the disabling of the external HSE oscillator. If HSE clock (divided or not) is selected as PLL input clock then upon HSE clock failure, the PLL will be turned off.

4.2.10 LSE Clock security system (LSECSS)

The LSE clock security system is activated by enabling the RCC_LDCTRL.LSECLKSSEN bit. The RCC_LDCTRL.LSECLKSSEN bit can be cleared by a hardware reset or RTC software reset or after detection of an LSE fault. When LSE and LSI are enabled and ready, the RCC_LDCTRL.LSECLKSSEN bit must be enabled after configuring the RCC_LDCTRL.RTCSEL to select the RTC clock source.

If an LSE failure is detected, no more LSE will be provided to the RTC, but the RCC_LDCTRL.RTCSEL bits will not be modified by hardware to switch the RTC clock source.

In Standby mode, an LSE clock failure triggers a wake-up. In other modes, an interrupt can be generated to wake up, and then the software can clear the RCC_LDCTRL.LSECLKSSEN bit and turn off the LSE, and change the RTC clock source and other measures to ensure the safety of the application.

The frequency of the LSE oscillator must be higher than 30KHz to avoid false detection of LSECSS.

4.2.11 RTC clock

By programming RCC_LDCTRL.RTCSEL[1:0] bits, the RTCCLK clock source can be either the HSE/32, LSE, or LSI clocks. This selection cannot be changed unless the low power domain is reset.

Before configuring the RTC clock source, the PWR_CTRL1.DRBP bit must be set to 1 to cancel the write protection.

The LSE and LSI clocks are in the low power domain, but the HSE clocks are not. therefore:

- If LSE or LSI is selected as RTC clock:
  - If the V_{DD} supply is switched off, the RTC cannot continue to work
- If the HSE clock divided by 32 is used as the RTC clock:
  - When in Stop2 or Standby mode, the RTC state is indeterminate.

4.2.12 Watchdog clock

If the IWDG is started by either hardware option or software access, the LSI oscillator will be forced ON and cannot be disabled. After the LSI oscillator is stabilized, the clock is provided to the IWDG.

4.2.13 Clock output(MCO)

The microcontroller clock output (MCO) capability allows the clock signal to be output onto the external MCO pin.

The corresponding GPIO port register must be configured for the corresponding function.The following 7 clock signals can be selected as the MCO clock:

- SYSCLK

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- HSI
- HSE
- PLL
- LSI
- LSE(1)
- MSI

The clock selection is controlled by RCC_CFG.MCO[2:0] bits.

The MCO output clock frequency division selection is realized by configuring the RCC_CFG.MCOPRES[3:0] bits.

Note:

2. MCO outputs LSE with a duty cycle of about of 50%±10%

4.3 RCC Registers

The RCC registers are accessible through AHB bus. The register description is as follows.

4.3.1 RCC register overview

Table 4-1 RCC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RCC_CTRL	Reserved						PLLRDF	PLLEN	Reserved				CLKSSEN	HSEBP	HSERDF	HSEEN	HSICAL[8:0]									HSITRIM[4:0]					HSIRDF	HSIEN
	Reset Value							0	0					0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0
004h	RCC_CFG	MCOPRES[3:0]				PLLMULFCT[4]	MCO[2:0]			USBPRES[1:0]		PLLMULFCT [3:0]				PLLHSEPRES	PLLSRC	Reserved		APB2PRES[2:0]			APB1PRES[2:0]			AHBPRES[3:0]				SCLKSTS[1:0]		SCLKSW[1:0]	
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	RCC_CLKINT	Reserved					LSESSICLR	LSESSIEN	LSESSIF	CLKSSICLR	Reserved	BORICLR	PLLRDICLR	HSERDICLR	HSIRDICLR	LSERDICLR	LSIRDICLR	MSIRDICLR	MSIRDIEN	BORIEN	PLLRDIEN	HSERDIEN	HSIRDIEN	LSERDIEN	LSIRDIEN	CLKSSIF	MSIRDIF	BORIF	PLLRDIF	HSERDIF	HSIRDIF	LSERDIF	LSIRDIF
	Reset Value						0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	RCC_APB2PRST	Reserved												SPI2RST	UART5RST	UART4RST	Reserved		USART1RST	TIM8RST	SPI1RST	TIM1RST	Reserved					IOPDRST	IOPCRST	IOPBRST	IOPAMPRST	Reserved	AFIORST
	Reset Value													0	0	0			0	0	0	0						0	0	0	0		0
010h	RCC_APB1PRST	OPAMPRST	Reserved	DACRST	PWRRST	Reserved		CANRST	UCDRRST	USBRST	I2C2RST	I2C1RST	Reserved		USART3RST	USART2RST	Reserved					WWDGRST	Reserved	TIM9RST	Reserved		COMPRST	TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
	Reset Value	0		0	0			0	0	0	0	0			0	0						0		0			0	0	0	0	0	0	0
014h	RCC_AHBPCLKEN	Reserved																			ADCEN	SACEN	Reserved	RNGCEN	Reserved		CRCEN	Reserved	FLITFEN	Reserved	SRAMEN	Reserved	DMAEN
	Reset Value																				0	0		0			0		1		1		0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
018h	RCC_APB2PCLKEN	Reserved												SPI2EN	UART5EN	UART4EN	Reserved		USART1EN	TIM8EN	SPI1EN	TIM1EN	Reserved					IOPDEN	IOPCEN	IOPBEN	IOPAMPEN	Reserved	AFIOEN
	Reset Value													0	0	0			0	0	0	0						0	0	0	0		0
01Ch	RCC_APB1PCLKEN	OPAMPEN	Reserved	DACEN	PWREN	Reserved		CANEN	Reserved	USBEN	I2C2EN	I2C1EN	Reserved		USART3EN	USART2EN	Reserved					WWDGEN	Reserved	TIM9EN	Reserved	COMPFILTEN	COMPEN	TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
	Reset Value	0		0	0			0		0	0	0			0	0						0		0		0	0	0	0	0	0	0	0
020h	RCC_LDCTRL	Reserved	LDEMCRSTF	Reserved	BDRRSTF	Reserved											LDSFTRST	RTCEN	Reserved					RTCSEL[1:0]		Reserved		LSXSEL	LSECLKSSF	LSECLKSSEN	LSEBP	LSERD	LSEEN
	Reset Value		0		0												0	0						0	0			0	0	0	0	0	0
024h	RCC_CTRLSTS	LPWRRSTF	WWDGRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	MMURSTF	RMRSTF	RAMRSTF	MSITRIM[7:0]								MSICAL[7:0]								MSIRANGE [2:0]			MSIRD	MSIEN	LSIRD	LSIEN
	Reset Value	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0
028h	RCC_AHBPRST	Reserved																		ADCRST	SACRST	Reserved	RNGCRST	Reserved									
	Reset Value																			0	0		0										
02Ch	RCC_CFG2	Reserved		TIMCLKSEL	RNGCPRES[4:0]					Reserved						ADC1MSEL	ADC1MPRES[4:0]					Reserved			ADCPLLPRES[4:0]					ADCHPRES [3:0]			
	Reset Value			0	0	0	0	0	0							0	0	0	1	1	1				0	0	0	0	0	0	0	0	0
030h	RCC_CFG3	Reserved													TRNG1MEN	TRNG1MSEL	Reserved	TRNG1MPRES[4:0]					Reserved	UCDR300MSEL	USBXTALESS	UCDREN	Reserved						
	Reset Value														0	0		0	0	1	1	1		0	0	0							
034h	RCC_RDCTRL	Reserved																		LPRCNTRST	LCDRST	LPUARTRST	LPTIMRST	LPRCNTEN	LCDEN	LPUARTEN	LPTIMEN	Reserved	LPUARTSEL [1:0]		LPTIMSEL [2:0]		
	Reset Value																			0	0	0	0	0	0	0	0		0	0	0	0	0
038h	Reserved																																
03Ch	Reserved																																
040h	RCC_PLLHSIPRE	Reserved																														PLLSRCDIV	PLLHSIPRE
	Reset Value																															0	0
044h	SRAM_PARITY _CTRLSTS	Reserved																										ERR2STS	ERR2RSTEN	ERR2IEN	ERR1STS	ERR1RSTEN	ERR1IEN
	Reset Value																											0	0	0	0	0	0

4.3.2 Clock Control Register (RCC_CTRL)

Address offset: 0x00

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Reset value: 0x0000 0040

31:26	25	24	23:20	19	18	17	16
Reserved	PLLRDF	PLLEN	Reserved	CLKSSEN	HSEBP	HSERDF	HSEEN
	r	rw		rw	rw	r	rw

15:7	6:2	1	0
HSICAL[8:0]	HSITRIM[4:0]	HSIRDF	HSIEN
r	rw	r	rw

Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	PLLRDF	PLL clock ready flag Set by hardware once PLL is ready. 0: PLL is not ready 1: PLL is ready
24	PLLEN	PLL enable Set and cleared by software. When entering the stop2 mode, it is cleared by hardware. This bit cannot be cleared when PLL is used as the system clock. When the HSI/HSE is used as the clock source for the PLL, the PLL will not be turned on until the HSI/HSE clock is ready. 0: Disable PLL 1: Enable PLL
23:20	Reserved	Reserved, the reset value must be maintained.
19	CLKSSEN	Clock security system enable Set and cleared by software. 0: Disable the clock detector 1: Enable the clock detector if the HSE oscillator is ready
18	HSEBP	External high-speed clock bypass enable Set and cleared by software. This bit can only be written when the HSE oscillator is disabled. 0: Disable the bypass function of HSE oscillator 1: Enable the bypass function of HSE oscillator
17	HSERDF	External high-speed clock ready flag Set by hardware once HSE is ready. This bit takes 6 HSE clock cycles to clear after the HSEEN bit is cleared. 0: HSE is not ready 1: HSE is ready
16	HSEEN	External high-speed clock enable Set and cleared by software. When entering the stop2 or standby mode, it is cleared by hardware. This bit cannot be cleared when HSE is used directly or indirectly as the system clock. 0: Disable HSE oscillator 1: Enable HSE oscillator
15:7	HSICAL[8:0]	Internal high-speed clock calibration value

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Bit Field	Name	Description
		These bits are automatically initialized at startup.
6:2	HSITRIM[4:0]	Internal high-speed clock correction value Written by software. The values of these bits will be added to the HSICAL[8:0] bits in order to form the final value for calibrating the frequency of the internal HSI RC oscillator. The trimming step is around 28 kHz between two consecutive HSICAL steps, and the default value is 16, which can adjust the HSI to 16 MHz ±1%.
1	HSIRDF	Internal high-speed clock ready flag Set by hardware once HSI is stable. After the HSIEN bit is cleared, it takes 6 internal 16 MHz oscillator clock cycles to go low. 0: HSI is not ready 1: HSI is ready
0	HSIEN	Internal high-speed clock enable Set and cleared by software. This bit cannot be cleared when HSI is used as the system clock. When returning from stop2 or standby mode or HSE failure occurs, set by hardware to enable the HSI oscillator. This bit cannot be reset if the HSI is used directly or indirectly as system clock. 0: Disable HSI oscillator 1: Enable HSI oscillator

4.3.3 Clock Configuration Register (RCC_CFG)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCOPRES[3:0]				PLLMULFCT[4]	MCO[2:0]			USBPRES[1:0]		PLLMULFCT[3:0]				PLLHSEPRES	PLLSRC
rw				rw	rw			rw		rw				rw	rw
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		APB2PRES[2:0]			APB1PRES[2:0]			AHBPRES[3:0]				SCLKSTS[1:0]		SCLKSW[1:0]	
		rw			rw			rw				r		rw	

Bit Field	Name	Description
31:28	MCOPRES[3:0]	MCO prescaler Set and cleared by software. 0000: MCO clock divided by 1, the duty cycle is the same as clock source 0001: MCO clock divided by 2, duty cycle 1/(frequency division factor * 2) 0010: MCO clock divided by 3, duty cycle 1/(frequency division factor * 2) 0011: MCO clock divided by 4, duty cycle 1/(frequency division factor * 2) 0100: MCO clock divided by 5, duty cycle 1/(frequency division factor * 2) 0101: MCO clock divided by 6, duty cycle 1/(frequency division factor * 2) 0110: MCO clock divided by 7, duty cycle 1/(frequency division factor * 2) 0111: MCO clock divided by 8, duty cycle 1/(frequency division factor * 2)

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Bit Field	Name	Description
		1000: MCO clock divided by 2, duty cycle 50% 1001: MCO clock divided by 4, duty cycle 50% 1010: MCO clock divided by 6, duty cycle 50% 1011: MCO clock divided by 8, duty cycle 50% 1100: MCO clock divided by 10, duty cycle 50% 1101: MCO clock divided by 12, duty cycle 50% 1110: MCO clock divided by 14, duty cycle 50% 1111: MCO clock divided by 16, duty cycle 50%
27	PLLMULFCT[4]	This bit is combined with bit[21:18] to form a PLL multiplication factor. Please refer to PLLMULFCT[3:0].
26:24	MCO[2:0]	Microcontroller clock output selection Set and cleared by software. 0xx: no clock output 001: select internal low-speed clock (LSI) output 010: Select external low-speed clock (LSE) output 011: Select internal multi-speed clock (MSI) output 100: Select system clock (SYSCLK) output 101: select internal high-speed clock (HSI) output 110: select external high-speed clock (HSE) output 111: Select PLL clock output *Notice: This clock output may be truncated when starting and switching the MCO clock source.* *When the system clock is output to the MCO pin, the output clock frequency should not exceed 50MHz (the highest frequency of the I/O port).*
23:22	USBPRES[1:0]	USB prescaler. Set or cleared by software to generate a 48MHz USB clock. The values of these bits must be valid before enabling the USB clock in the RCC_APB1PCLKEN register. 00: Divide the PLL clock by 1.5 as the USB clock 01: The PLL clock is directly used as the USB clock 10: Divide the PLL clock by 2 as the USB clock 11: Divide the PLL clock by 3 as the USB clock
21:18	PLLMULFCT[3:0]	PLL multiplication factor (including bit 27) Written by software to define PLL multiplication factor. These bits can only be written when the PLL is disabled. The PLL output frequency must not exceed 108MHz. 00000: PLL input clock ×2 00001: PLL input clock ×3 00010: PLL input clock ×4 00011: PLL input clock ×5 00100: PLL input clock ×6

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Bit Field	Name	Description
		00101: PLL input clock ×7 00110: PLL input clock ×8 00111: PLL input clock ×9 01000: PLL input clock ×10 01001: PLL input clock ×11 01010: PLL input clock ×12 01011: PLL input clock ×13 01100: PLL input clock ×14 01101: PLL input clock ×15 01110: PLL input clock ×16 01111: PLL input clock ×16 10000: PLL input clock ×17 10001: PLL input clock ×18 10010: PLL input clock ×19 10011: PLL input clock ×20 10100: PLL input clock ×21 10101: PLL input clock ×22 10110: PLL input clock ×23 10111: PLL input clock ×24 11000: PLL input clock ×25 11001: PLL input clock ×26 11010: PLL input clock ×27 11011: PLL input clock ×28 11100: PLL input clock ×29 11101: PLL input clock ×30 11110: PLL input clock ×31 11111: PLL input clock ×32
17	PLLHSEPRES	HSE prescaler for PLL input Set and cleared by software to divide HSE before PLL entry. This bit can only be written when PLL is disabled. 0: HSE clock not divided 1: HSE divided by 2
16	PLLSRC	PLL clock source Set and cleared by software to select PLL clock source. This bit can only be written when PLL is disabled. 0: HSI clock selected as PLL input clock 1: HSE clock selected as PLL input clock
15:14	Reserved	Reserved, the reset value must be maintained.
13:11	APB2PRES[2:0]	APB high-speed (APB2) prescaler Set and cleared by software to configure the division factor of APB2 clock (PCLK2). Make sure that PCLK2 does not exceed 54MHz.

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Bit Field	Name	Description
		0xx: HCLK not divided 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
10:8	APB1PRES[2:0]	APB low-speed (APB1) prescaler Set and cleared by software to configure the division factor of APB1 clock (PCLK1). Make sure that PCLK1 does not exceed 27MHz. 0xx: HCLK not divided 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
7:4	AHBPRES[3:0]	AHB prescaler Set and cleared by software to configure the division factor of the AHB clock (HCLK). 0xxx: SYSCLK not divided 1000: SYSCLK divided by 2 1001: SYSCLK divided by 4 1010: SYSCLK divided by 8 1011: SYSCLK divided by 16 1100: SYSCLK divided by 64 1101: SYSCLK divided by 128 1110: SYSCLK divided by 256 1111: SYSCLK divided by 512
3:2	SCLKSTS[1:0]	System clock switching status Set and cleared by hardware to indicate which clock source is used as system clock 00: The system clock comes from MSI 01: The system clock comes from HSI 10: The system clock comes from HSE 11: The system clock comes from the PLL output
1:0	SCLKSW[1:0]	System clock switch Set and cleared by software to select the system clock source. Set by hardware to force HSI selection when exiting from the stop2 or standby mode, or when the HSE oscillator fails (RCC_CTRL.CLKSSEN is enabled). 00: Select MSI as system clock 01: Select HSI as system clock 10: Select HSE as system clock 11: Select PLL output as system clock

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4.3.4 Clock Interrupt Register (RCC_CLKINT)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					LSESSI CLR	LSESSI EN	LSESSIF	CLKSSI CLR	Reserved	BORICLR	PLLRDI CLR	HSERDI CLR	HSIRDI CLR	LSERDI CLR	LSIRDI CLR
					w	rw	r	w		w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSIRDI CLR	MSIRDI EN	BORIEN	PLLRDI EN	HSERDI EN	HSIRDI EN	LSERDI EN	LSIRDI EN	CLKSSIF	MSIRDIF	BORIF	PLLRDIF	HSERDIF	HSIRDIF	LSERDIF	LSIRDIF
w	rw	rw	rw	rw	rw	rw	rw	r	r	r	r	r	r	r	r

Bit Field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26	LSESSICLR	LSE Clock security system interrupt clear. This bit is set by software to clear the LSESSIF flag. 0: No effect 1: Clear LSESSIF flag
25	LSESSIEN	LSE Clock Security System (CSS) interrupt enable Set and cleared by software to enable/disable interrupt caused by LSE CSS detection. 0: LSE CSS interrupt disabled 1: LSE CSS interrupt enabled
24	LSESSIF	Clock security system interrupt flag Set by hardware when a failure is detected in the LSE. Cleared by software setting the LSESSICLR bit. 0: No clock security interrupt caused by LSE clock failure 1: Clock security interrupt caused by LSE clock failure
23	CLKSSICLR	Clock security system interrupt clear Set by the software to clear the CLKSSIF flag. 0: No effect 1: Clear the CLKSSIF flag
22	Reserved	Reserved, the reset value must be maintained.
21	BORICLR	BOR interrupt clear This bit is set by software to clear the BORIF flag. 0: No effect 1: BORIF cleared
20	PLLRDICLR	PLL ready interrupt clear Set by the software to clear the PLLRDIF flag. 0: No effect 1: Clear the PLLRDIF flag
19	HSERDICLR	HSE ready interrupt clear Set by the software to clear the HSERDIF flag.

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Bit Field	Name	Description
		0: Not used 1: Clear HSERDIF flag
18	HSIRDICLR	HSI ready interrupt clear Set by the software to clear the HSIRDIF flag. 0: Not used 1: Clear the HSIRDIF flag
17	LSERDICLR	LSE ready interrupt clear Set by the software to clear the LSERDIF flag. 0: Not used 1: Clear LSERDIF flag
16	LSIRDICLR	LSI ready interrupt clear Set by software to clear the LSIRDIF flag. 0: Not used 1: Clear the LSIRDIF flag
15	MSIRDICLR	MSI ready interrupt clear bit. Set by software to clear the MSIRDIF flag. 0: not used 1: Clear the MSIRDIF interrupt flag bit
14	MSIRDIEN	MSI ready interrupt enable bit. Set or cleared by software to enable or disable the MSI ready interrupt. 0: Disable MSI ready interrupt 1: Enable MSI ready interrupt MSIRDF triggers interrupt
13	BORIEN	BOR interrupt enable Set and cleared by software to enable/disable interrupt caused by BOR. 0: BOR interrupt disabled 1: BOR interrupt enabled
12	PLLRDIEN	PLL ready interrupt enable Set and cleared by software to enable and disable PLL ready interrupt 0: Disable PLL ready interrupt 1: Enable PLL ready interrupt
11	HSERDIEN	HSE ready interrupt enable Set and cleared by software to enable and disable HSE ready interrupt. 0: Disable HSE ready interrupt 1: Enable HSE Ready Interrupt
10	HSIRDIEN	HSI ready interrupt enable Set and cleared by software to enable and disable HSI ready interrupt. 0: Disable HSI ready interrupt 1: Enable HSI ready interrupt
9	LSERDIEN	LSE ready interrupt enable Set and cleared by software to enable and disable LSE ready interrupt.

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Bit Field	Name	Description
		0: Disable LSE ready interrupt 1: Enable LSE ready interrupt
8	LSIRDIEN	LSI ready interrupt enable Set and cleared by software to enable and disable LSI ready interrupt. 0: Disable LSI ready interrupt 1: Enable LSI ready interrupt
7	CLKSSIF	Clock security system interrupt flag Set by hardware when a failure is detected in the external HSE oscillator. 0: No clock security system interrupt caused by HSE clock failure 1: Clock security system interrupt caused by HSE clock failure
6	MSIRDIF	MSI ready interrupt flag. Hardware sets this bit when MSIRDIEN is set and the MSI clock is ready. This bit is cleared by software by setting the MSIRDICLR bit. 0: No clock ready interrupt from MSI oscillator 1: MSI oscillator has generated a clock ready interrupt
5	BORIF	BOR interrupt flag This bit is set by hardware when BORIEN is set and the BOR falling edge is triggered. This bit is cleared by software by setting the BORICLR bit. 0: No BOR generates an interrupt 1: BOR generates an interrupt
4	PLLRDIF	PLL ready interrupt flag This bit is set by hardware when PLLRDIEN is set and PLL clock is ready. This bit is cleared by software by setting the PLLRDICLR bit. 0: No clock ready interrupt caused by PLL lock 1: Clock ready interrupt caused by PLL lock
3	HSERDIF	HSE ready interrupt flag Set by hardware when HSERDIEN is set and the HSE clock is ready. This bit is cleared by software by setting the HSERDICLR bit. 0: No clock ready interrupt caused by HSE oscillator 1: Clock ready interrupt caused by HSE oscillator
2	HSIRDIF	HSI ready interrupt flag Set by hardware when HSIRDIEN is set and the HSI clock is ready. This bit is cleared by software by setting the HSERDICLR bit. 0: No clock ready interrupt caused by HSI oscillator 1: Clock ready interrupt caused by HSI oscillator
1	LSERDIF	LSE ready interrupt flag Set by hardware when LSERDIEN is set and the LSE clock is ready. This bit is cleared by the software by setting the LSERDICLR bit. 0: No clock ready interrupt caused by LSE oscillator 1: Clock ready interrupt caused by LSE oscillator

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Bit Field	Name	Description
0	LSIRDIF	LSI ready interrupt flag Set by the hardware when LSIRDIEN is set and the LSI clock is ready. This bit is cleared by software by setting the LSIRDICLR bit. 0: No clock ready interrupt caused by LSI oscillator 1: Clock ready interrupt caused by LSI oscillator

4.3.5 APB2 Peripheral Reset Register (RCC_APB2PRST)

Address offset: 0x0c

Reset value: 0x0000 0000

31:20	19	18	17	16
Reserved	SPI2RST	UART5 RST	UART4 RST	Reserved
	rw	rw	rw	

15	14	13	12	11	10:6	5	4	3	2	1	0
Reserved	USART1 RST	TIM8RST	SPI1RST	TIM1RST	Reserved	IOPDRST	IOPCRST	IOPBRST	IOPARST	Reserved	AFIORST
	rw	rw	rw	rw		rw	rw	rw	rw		rw

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19	SPI2RST	SPI2 reset Set and cleared by software. 0: Clear the reset 1: Reset SPI2
18	UART5RST	UART5 reset Set and cleared by software. 0: Clear the reset 1: Reset UART5
17	UART4RST	UART4 reset Set and cleared by software. 0: Clear the reset 1: Reset UART4
16:15	Reserved	Reserved, the reset value must be maintained.
14	USART1RST	USART1 reset Set and cleared by software. 0: Clear the reset 1: Reset USART1
13	TIM8RST	TIM8 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM8 timer

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Bit Field	Name	Description
12	SPI1RST	SPI1 reset Set and cleared by software. 0: Clear the reset 1: Reset SPI1
11	TIM1RST	TIM1 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM1 timer
10:6	Reserved	Reserved, the reset value must be maintained.
5	IOPDRST	GPIO port D reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port D
4	IOPCRST	GPIO port C reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port C
3	IOPBRST	GPIO port B reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port B
2	IOPAMPRST	GPIO port A reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port A
1	Reserved	Reserved, the reset value must be maintained.
0	AFIORST	Alternate function IO reset Set and cleared by software. 0: Clear the reset 1: Reset Alternate Function

4.3.6 APB1 Peripheral Reset Register (RCC_APB1PRST)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPAMP RST	Reserved	DACRST	PWRRST	Reserved		CANRST	UCDRRST	USBRST	I2C2RST	I2C1RST	Reserved		USART3 RST	USART2 RST	Reserved
rw		rw	rw			rw	rw	rw	rw	rw			rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WWDG RST	Reserved	TIM9RST	Reserved		COMPRST	TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
				rw		rw			rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31	OPAMPRST	OPAMP interface reset. Set or cleared by software. 0: Clear the reset 1: Reset the OPAMP interface
30	Reserved	Reserved, the reset value must be maintained.
29	DACRST	DAC interface reset. Set or cleared by software. 0: Clear the reset 1: Reset the DAC interface
28	PWRRST	Power interface reset Set and cleared by software. 0: Clear the reset 1: Reset the power interface
27:26	Reserved	Reserved, the reset value must be maintained.
25	CANRST	CAN reset Set or cleared by software. 0: Clear the reset 1: Reset CAN
24	UCDRRST	UCDR reset. Set or cleared by software. 0: clear the reset 1: Reset UCDR
23	USBRST	USB reset. Set or cleared by software. 0: clear the reset 1: Reset USB
22	I2C2RST	I2C2 reset Set and cleared by software. 0: Clear the reset 1: Reset I2C2
21	I2C1RST	I2C1 reset Set and cleared by software. 0: Clear the reset 1: Reset I2C1
20:19	Reserved	Reserved, the reset value must be maintained.
18	USART3RST	USART3 reset. Set or cleared by software. 0: clear the reset 1: Reset USART3
17	USART2RST	USART2 reset Set and cleared by software.

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Bit Field	Name	Description
		0: Clear the reset 1: Reset USART2
16:12	Reserved	Reserved, the reset value must be maintained.
11	WWDGRST	Window watchdog reset Set and cleared by software. 0: Clear the reset 1: Reset window watchdog
10	Reserved	Reserved, the reset value must be maintained.
9	TIM9RST	TIM9 reset. Set or cleared by software. 0: clear the reset 1: Reset TIM9
8:7	Reserved	Reserved, the reset value must be maintained.
6	COMPRST	COMP reset Set and cleared by software. 0: Clear the reset 1: Reset COMP
5	TIM7RST	TIM7 timer reset. Set or cleared by software. 0: clear the reset 1: Reset the TIM7 timer
4	TIM6RST	TIM6 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM6 timer
3	TIM5RST	TIM5 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM5 timer
2	TIM4RST	TIM4 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM4 timer
1	TIM3RST	TIM3 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM3 timer
0	TIM2RST	TIM2 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM2 timer

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4.3.7 AHB Peripheral Clock Enable Register (RCC_AHBPCLKEN)

Address offset: 0x14

Reset value: 0x0000 0014

31–16
Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			ADCEN	SACEN	Reserved	RNGCEN	Reserved		CRCEN	Reserved	FLITFEN	Reserved	SRAMEN	Reserved	DMAEN
			rw	rw		rw			rw		rw		rw		rw

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCEN	ADC clock enable Set and cleared by software. 0: ADC clock disabled 1: ADC clock enabled
11	SACEN	SAC clock enable Set and cleared by software. 0: SAC clock disabled 1: SAC clock enabled
10	Reserved	Reserved, the reset value must be maintained.
9	RNGCEN	RNGC clock enable Set and cleared by software. 0: RNGC clock disabled 1: RNGC clock enabled
8:7	Reserved	Reserved, the reset value must be maintained.
6	CRCEN	CRC clock enable Set and cleared by software. 0: CRC clock disabled 1: CRC clock enabled
5	Reserved	Reserved, the reset value must be maintained.
4	FLITFEN	Flash interface circuit clock enable. Set or cleared by software. 0: Disable the clock of the flash interface circuit 1: Enable the clock of the flash interface circuit
3	Reserved	Reserved
2	SRAMEN	SRAM interface clock enable Set and cleared by software to disable/enable SRAM interface clock during Sleep mode. 0: SRAM interface clock disabled during Sleep mode. 1: SRAM interface clock enabled during Sleep mode

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Bit Field	Name	Description
1	Reserved	Reserved, the reset value must be maintained.
0	DMAEN	DMA clock enable Set and cleared by software. 0: DMA clock disabled 1: DMA clock enabled

4.3.8 APB2 Peripheral Clock Enable Register (RCC_APB2PCLKEN)

Address offset: 0x18

Reset value: 0x0000 0000

31:20	19	18	17	16
Reserved	SPI2EN	UART5EN	UART4EN	Reserved
	rw	rw	rw	

15	14	13	12	11	10:6	5	4	3	2	1	0
Reserved	USART1EN	TIM8EN	SPI1EN	TIM1EN	Reserved	IOPDEN	IOPCEN	IOPBEN	IOPAEN	Reserved	AFIOEN
	rw	rw	rw	rw		rw	rw	rw	rw		rw

Bit Field	Name	Description
31:20	Reserved	Reserved, the reset value must be maintained.
19	SPI2EN	SPI2 clock enable Set and cleared by software. 0: SPI2 clock disabled 1: SPI2 clock enabled
18	UART5EN	UART5clock enable Set and cleared by software. 0: UART5 clock disabled 1: UART5 clock enabled
17	UART4EN	UART4 clock enable Set and cleared by software. 0: UART4 clock disabled 1: UART4 clock enabled
16:15	Reserved	Reserved, the reset value must be maintained.
14	USART1EN	USART1 clock enable Set and cleared by software. 0: USART1 clock disabled 1: USART1 clock enabled
13	TIM8EN	TIM8 Timer clock enable Set and cleared by software. 0: TIM8 timer clock disabled 1: TIM8 timer clock enabled

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Bit Field	Name	Description
12	SPI1EN	SPI1 clock enable Set and cleared by software. 0: SPI1 clock disabled 1: SPI1 clock enabled
11	TIM1EN	TIM1 timer clock enable Set and cleared by software. 0: TIM1 timer clock disabled 1: TIM1 timer clock enabled
10:6	Reserved	Reserved, the reset value must be maintained.
5	IOPDEN	IO Port D clock enable Set and cleared by software. 0: IO Port D clock disabled 1: IO Port D clock enabled
4	IOPCEN	IO Port C clock enable Set and cleared by software. 0: IO Port C clock disabled 1: IO Port C clock enabled
3	IOPBEN	IO Port B clock enable Set and cleared by software. 0: IO Port B clock disabled 1: IO Port B clock enabled
2	IOPAEN	IO Port A clock enable Set and cleared by software. 0: IO Port A clock disabled 1: IO Port A clock enabled
1	Reserved	Reserved, the reset value must be maintained.
0	AFIOEN	Alternate function IO clock enable Set and cleared by software. 0: Alternate Function IO clock disabled 1: Alternate Function IO clock enabled

4.3.9 APB1 Peripheral Clock Enable Register (RCC_APB1PCLKEN)

Address offset: 0x1c

Reset value: 0x0000 0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPAMPEN	Reserved	DACEN	PWREN	Reserved		CANEN	Reserved	USBEN	I2C2EN	I2C1EN	Reserved		USART3 EN	USART2 EN	Reserved
rw		rw	rw			rw		rw	rw	rw			rw	rw	

15			12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WWDG EN	Reserved	TIM9EN	Reserved	COMP FILTEN	COMPEN	TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
				rw		rw		rw	rw	rw	rw	rw	rw	rw	rw

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Bit Field	Name	Description
31	OPAMPEN	OPAMP clock enable. Set or cleared by software. 0: Disable OPAMP clock 1: Enable OPAMP clock
30	Reserved	Reserved, the reset value must be maintained.
29	DACEN	DAC interface clock enable Set and cleared by software. 0: DAC interface clock disabled 1: DAC interface clock enable
28	PWREN	Power interface clock enable Set and cleared by software. 0: Power interface clock disabled 1: Power interface clock enable
27:26	Reserved	Reserved, the reset value must be maintained.
25	CANEN	CAN clock enable Set and cleared by software. 0: CAN clock disabled 1: CAN clock enabled
24	Reserved	Reserved, the reset value must be maintained.
23	USBEN	USB clock enable Set and cleared by software. 0: USB clock disabled 1: USB clock enabled
22	I2C2EN	I2C2 clock enable Set and cleared by software. 0: I2C2 clock disabled 1: I2C2 clock enabled
21	I2C1EN	I2C1 clock enable Set and cleared by software. 0: I2C1 clock disabled 1: I2C1 clock enabled
20:19	Reserved	Reserved, the reset value must be maintained.
18	USART3EN	USART3 clock enable Set and cleared by software. 0: USART3 clock disabled 1: USART3 clock enabled
17	USART2EN	USART2 clock enable Set and cleared by software. 0: USART2 clock disabled 1: USART2 clock enabled
16:12	Reserved	Reserved, the reset value must be maintained.

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Bit Field	Name	Description
11	WWDGEN	Window watchdog clock enable Set and cleared by software. 0: Window watchdog clock disabled 1: Window watchdog clock enabled
10	Reserved	Reserved, the reset value must be maintained.
9	TIM9EN	TIM9 clock enable Set and cleared by software. 0: TIM9 clock disabled 1: TIM9 clock enabled
8	Reserved	Reserved, the reset value must be maintained.
7	COMPFILTEN	COMP Filter clock enable Set and cleared by software. 0: COMP Filter clock disabled 1: COMP Filter clock enabled
6	COMPEN	COMP clock enable Set and cleared by software. 0: COMP clock disabled 1: COMP clock enabled
5	TIM7EN	TIM7 timer clock enable Set and cleared by software. 0: TIM7 clock disabled 1: TIM7 clock enabled
4	TIM6EN	TIM6 timer clock enable Set and cleared by software. 0: TIM6 clock disabled 1: TIM6 clock enabled
3	TIM5EN	TIM5 timer clock enable Set and cleared by software. 0: TIM5 clock disabled 1: TIM5 clock enabled
2	TIM4EN	TIM4 timer clock enable Set and cleared by software. 0: TIM4 clock disabled 1: TIM4 clock enabled
1	TIM3EN	TIM3 timer clock enable Set and cleared by software. 0: TIM3 clock disabled 1: TIM3 clock enabled
0	TIM2EN	TIM2 timer clock enable Set and cleared by software.

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Bit Field	Name	Description
		0: TIM2 clock disabled 1: TIM2 clock enabled

4.3.10 LOW POWER Domain Control Register (RCC_LDCTRL)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29	28	27:17	16
Reserved	LDEMCRSTF	Reserved	BDRRSTF	Reserved	LDSFTRST
	r		r		rw

15	14:10	9:8	7:6	5	4	3	2	1	0
RTCEN	Reserved	RTCSEL[1:0]	Reserved	LSXSEL	LSECLKSSF	LSECLKSSEN	LSEBP	LSERD	LSEEN
rw		rw		rw	r	rw	rw	rw	rw

Bit Field	Name	Description
31	Reserved	Reserved, the reset value must be maintained.
30	LDEMCRSTF	Low power domain EMC reset flag. Set by hardware when a low-power domain EMC reset occurs, and cleared by software by writing the RCC_CTRLSTS.RMRSTF bit. 0: No low power domain EMC reset occurred 1: A low power domain EMC reset has occurred
29	Reserved	Reserved, the reset value must be maintained.
28	BORRSTF	BOR reset flag. Set by hardware when a BOR reset occurs and cleared by software by writing to the RCC_CTRLSTS.RMRSTF bit. 0: No BOR reset occurred 1: A BOR reset has occurred
27:17	Reserved	Reserved, the reset value must be maintained.
16	LDSFTRST	Low power domain software reset. Set or cleared by software. 0: No effect 1: Reset the entire low-power domain
15	RTCEN	RTC clock enable Set and cleared by software. 0: Disable RTC clock 1: Enable RTC clock
14:10	Reserved	Reserved, the reset value must be maintained.
9:8	RTCSEL[1:0]	RTC clock source selection Set by software to select RTC clock source. Once the RTC clock source is selected, it cannot be changed until the next low power domain is reset. These bits can be reset by setting the LDSFTRST bit.

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Bit Field	Name	Description
		00: No clock 01: LSE oscillator selected as RTC clock 10: LSI oscillator selected as RTC clock 11: HSE oscillator divided by 32 selected as RTC clock
7:6	Reserved	Reserved, the reset value must be maintained.
5	LSXSEL	LPRCNT low-speed clock source selection. Cleared by system reset. 0: Select LSI oscillator as clock source (LSI needs to be enabled in advance) 1: Select the LSE oscillator as the clock source (LSE needs to be enabled in advance)
4	LSECLKSSF	LSE clock security system status. 0: No LSE failure detected 1: LSE failure detected
3	LSECLKSSEN	LSE clock security system enable bit. Set or cleared by software. 0: Disable LSE clock detector 1: If LSE is ready, enable LSE clock detector
2	LSEBP	External low-speed oscillator bypass In debug mode, set and cleared by software to bypass oscillator. This bit can only be written when the external low-speed oscillator is disabled. 0: LSE oscillator not bypassed 1: LSE oscillator bypassed
1	LSERD	External low-speed clock oscillator ready Set and cleared by hardware to indicate if the LSE oscillator is ready. After the LSEEN bit is cleared, LSERD goes low after 6 cycles of the LSE clock. 0: External low-speed oscillator not ready 1: External low-speed oscillator ready
0	LSEEN	External low-speed clock oscillator enable Set and cleared by software. 0: Disable the external low-speed oscillator 1: Enable the external low-speed oscillator.

Note: The RCC_LDCTRL.LSEEN, RCC_LDCTRL.LSEBP, RCC_LDCTRL.RTCSEL and RCC_LDCTRL.RTCEN bits are in the low power domain. Therefore, these bits are write-protected after reset and can only be changed after the PWR_CTRL1.DRBP bit is set. These bits can only be cleared by a low-power domain reset. Any internal or external reset will not affect these bits.

4.3.11 Clock Control/Status Register (RCC_CTRLSTS)

Address offset: 0x24

Reset value: 0x0C00246C

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31	30	29	28	27	26	25	24	23	22–16
LPWR RSTF	WWDG RSTF	IWDG RSTF	SFT RSTF	POR RSTF	PINRSTF	MMU RSTF	RMRSTF	RAM RSTF	MSITRIM [7:1]
r	r	r	r	r	r	r	rw	r	rw

15	14–7	6–4	3	2	1	0
MSITRIM [0]	MSICAL[7:0]	MSIRANGE[2:0]	MSIRD	MSIEN	LSIRD	LSIEN
rw	r	rw	r	rw	r	rw

Bit Field	Name	Description
31	LPWRRSTF	Low power reset flag Set by hardware when a low-power management reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No low-power management reset occurred 1: A low-power management reset occurred
30	WWDGRSTF	Window watchdog reset flag Set by hardware when a window watchdog reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No windowed watchdog reset occurred 1: Window watchdog reset occurred
29	IWDGRSTF	Independent watchdog reset flag Set by hardware when an independent watchdog reset occurs Cleared by software by writing to the RMRSTF bit. 0: No independent watchdog reset occurred 1: Independent watchdog reset occurred
28	SFTRSTF	Software reset flag Set by hardware when a software reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No software reset occurred 1: Software reset occurred
27	PORRSTF	Power-on/power-down reset flag Set by hardware when a power-on/power-down reset occurs Cleared by software by writing to the RMRSTF bit. 0: No power on/power off reset occurred 1: Power-on/power-off reset occurred
26	PINRSTF	External pin reset flag Set by hardware when a reset from the NRST pin occurs. Cleared by software by writing to the RMRSTF bit. 0: No NRST pin reset occurred 1: NRST pin reset occurred
25	MMURSTF	MMU reset flag Set by hardware when MMU reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No MMU reset occurred 1: MMU reset occurred

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Bit Field	Name	Description
24	RMRSTF	Clear the reset flag Set by the software to clear the reset flag. 0: No effect 1: Clear the reset flag
23	RAMRSTF	RAM reset flag. Set by hardware when a RAM reset occurs and cleared by software by writing to the RMRSTF bit. 0: No RAM reset occurred 1: A RAM reset has occurred
22:15	MSITRIM[7:0]	Internal multi-speed clock correction value. Written by software. The value of these bits will be added to MSICAL[7:0] to form the final calibration value used to calibrate the frequency of the internal MSI RC oscillator.
14:7	MSICAL[7:0]	Internal multi-speed clock calibration value. The value of these bits is automatically initialized when the system is powered on.
6:4	MSIRANGE[2:0]	MSI frequency range selection. A total of 7 frequencies are available for software selection 000: 100kHz 001: 200kHz 010: 400kHz 011: 800kHz 100: 1MHz 101: 2MHz 110: 4MHz (default)
3	MSIRD	The internal multi-speed clock is ready. Hardware will be set to 1 after MSI is stable. This bit takes 6 internal MSI oscillator clock cycles to clear after the MSIEN bit is cleared. 0: MSI not ready 1: MSI is ready
2	MSIEN	Internal multi-speed clock enable bit. Set or cleared by software. This bit cannot be cleared when the MSI is directly or indirectly used as the system clock; when returning from Stop2 or Standby mode or when the HSE fails, the hardware will set it to 1 to start the MSI oscillator. 0: Disable the MSI oscillator 1: Enable the MSI oscillator
1	LSIRD	Internal low-speed oscillator ready Set and cleared by hardware to indicate if the internal RC 40 KHz oscillator is ready. After LSIEN is cleared, LSIRD goes low after 3 internal RC 40 KHz oscillator clock cycles. 0: Internal 40KHz RC oscillator clock not ready 1: Internal 40KHz RC oscillator clock ready

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Bit Field	Name	Description
0	LSIEN	Internal low-speed oscillator enable Set and cleared by software. 0: Disable the internal RC 40 kHz oscillator 1: Enable the internal RC 40 kHz oscillator

4.3.12 AHB Peripheral Reset Register (RCC_AHBPRST)

Address offset: 0x28

Reset value: 0x0000 0000

31:16
Reserved

15:13	12	11	10	9	8:0
Reserved	ADCRST	SACRST	Reserved	RNGCRST	Reserved
	rw	rw		rw	

Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	ADCRST	ADC reset Set and cleared by software. 0: Clear the reset 1: Reset ADC
11	SACRST	SAC reset Set and cleared by software. 0: Clear the reset 1: Reset SAC
10	Reserved	Reserved, the reset value must be maintained.
9	RNGCRST	RNGC reset Set and cleared by software. 0: Clear the reset 1: Reset RNGC
8:0	Reserved	Reserved, the reset value must be maintained.

4.3.13 Clock Configuration Register 2 (RCC_CFG2)

Address offset: 0x2c

Reset value: 0x0000 7000

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31:30	29	28:24	23:18	17	16
Reserved	TIMCLK SEL	RNGCPRES[4:0]	Reserved	ADC1M SEL	ADC1M PRES[4]
	rw	rw		rw	rw

15:12	11:9	8:4	3:0
ADC1M PRES[3:0]	Reserved	ADCPLLPRES[4:0]	ADCHPRES[3:0]
rw		rw	rw

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	TIMCLKSEL	TIM1/8 clock source selection Set and cleared by software. 0: PCLK2 is selected as TIM1/8 clock source if APB2 prescaler is 1. Otherwise, PCLK2 ×2 is selected. 1: SYSCLK input clock is selected as TIM1/8 clock source.
28:24	RNGCPRES[4:0]	RNGC prescaler. Software sets or clears these bits to configure the prescale factor for the RNGC clock. 00000: SYSCLK is not divided 00001: SYSCLK divided by 2 00010: SYSCLK divided by 3 ... 11110: SYSCLK divided by 31 11111: SYSCLK divided by 32
23:18	Reserved	Reserved, the reset value must be maintained.
17	ADC1MSEL	ADC 1M clock source selection. Set or cleared by software. 0: Select HSI oscillator clock as the input clock of ADC 1M 1: Select HSE oscillator clock as the input clock of ADC 1M
16:12	ADC1MPRES[4:0]	ADC 1M clock prescaler Set and cleared by software to configure the division factor of ADC 1M clock source. 00000: ADC 1M clock source not divided 00001: ADC 1M clock source divided by 2 00010: ADC 1M clock source divided by 3 ... 11110: ADC 1M clock source divided by 31 11111: ADC 1M clock source divided by 32 *Note: ADC clock must be configured to 1M*
11:9	Reserved	Reserved, the reset value must be maintained.
8:4	ADCPLLPRES[4:0]	ADC PLL prescaler Set and cleared by software to configure the division factor from the PLL clock to the ADC. 0xxxx: ADC PLL clock is disabled

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Bit Field	Name	Description
		10000: PLL clock not divided 10001: PLL clock divided by 2 10010: PLL clock divided by 4 10011: PLL clock divided by 6 10100: PLL clock divided by 8 10101: PLL clock divided by 10 10110: PLL clock divided by 12 10111: PLL clock divided by 16 11000: PLL clock divided by 32 11001: PLL clock divided by 64 11010: PLL clock divided by 128 11011: PLL clock divided by 256 Others: PLL clock divided by 256
3:0	ADCHPRES[3:0]	ADC HCLK prescaler Set and cleared by software to configure the division factor from the HCLK clock to the ADC. 0000: HCLK clock not divided 0001: HCLK clock divided by 2 0010: HCLK clock divided by 4 0011: HCLK clock divided by 6 0100: HCLK clock divided by 8 0101: HCLK clock divided by 10 0110: HCLK clock divided by 12 0111: HCLK clock divided by 16 1000: HCLK clock divided by 32 Others: HCLK clock divided by 32

4.3.14 Clock Configuration Register 3 (RCC_CFG3)

Address offset: 0x30

Reset value: 0x0000 3800

31:19	18	17	16
Reserved	TRNG1MEN	TRNG1MSEL	Reserved
	rw	rw	

15:11	10	9	8	7	6:0
TRNG1MPRES[4:0]	Reserved	UCDR300MSEL	USBXTALESS	UCDREN	Reserved
rw		rw	rw	rw	

Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	TRNG1MEN	TRNG analog interface clock enable. Set or cleared by software.

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Bit Field	Name	Description
		0: Disable TRNG analog interface clock 1: Enable TRNG analog interface clock
17	TRNG1MSEL	TRNG 1M clock selection. Set or cleared by software. 0: Select HSI oscillator as TRNG 1M input clock 1: Select HSE oscillator as TRNG 1M input clock
16	Reserved	Reserved, the reset value must be maintained.
15:11	TRNG1MPRES[4:0]	TRNG 1M clock prescaler. Software sets or clears these bits to generate the TRNG 1M clock. 00000: Reserved 00001: TRNG 1M clock source divided by 2, HSE must be selected as TRNG 1M input clock 00010: TRNG 1M clock source divided by 4 00011: TRNG 1M clock source divided by 6 00100: TRNG 1M clock source divided by 8 ... 11111: TRNG 1M clock source divided by 62 *Notes: TRNG clock should be less than or equal to 4M after frequency division*
10	Reserved	Reserved, the reset value must be maintained.
9	UCDR300MSEL	UCDR 300M clock source selection 0: OSC300M 1: PLL VCO clock (288M)
8	USBXTALESS	USB external crystal oscillator selection mode 0: USB has external crystal oscillator mode 1: USB without external crystal oscillator mode
7	UCDREN	UCDR enable 0: UCDR bypass 1: UCDR enable
6:0	Reserved	Reserved, the reset value must be maintained.

4.3.15 Retention Domain Control Register (RCC_RDCTRL)

Address offset: 0x34

Reset value: 0x0000 0000

31:16
Reserved

15:14	13	12	11	10	9	8	7	6	5	4:3	2:0
Reserved	LPRCNTRST	LCDRST	LPUARTRST	LPTIMRST	LPRCNTEN	LCDEN	LPUARTEN	LPTIMEN	Reserved	LPUARTSEL[1:0]	LPTIMSEL[2:0]
	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

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Bit Field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	LPRCNTRST	LPRCNT reset. Set or cleared by software. 0: clear reset 1: Reset LPRCNT
12	LCDRST	LCD reset. Set or cleared by software. 0: clear reset 1: Reset LCD
11	LPUARTRST	LPUART reset. Set or cleared by software. 0: clear reset 1: Reset LPUART
10	LPTIMRST	LPTIM reset. Set or cleared by software. 0: clear reset 1: Reset LPTIM
9	LPRCNTEN	LPRCNT clock enable. Set or cleared by software. 0: Disable LPRCNT clock 1: Enable LPRCNT clock
8	LCDEN	LCD clock enable. Set or cleared by software. 0: Disable LCD clock 1: Enable LCD clock
7	LPUARTEN	LPUART clock enable. Set or cleared by software. 0: Disable LPUART clock 1: Enable LPUART clock
6	LPTIMEN	LPTIM clock enable. Set or cleared by software. 0: Disable LPTIM clock 1: Enable LPTIM clock
5	Reserved	Reserved, the reset value must be maintained.
4:3	LPUARTSEL	LPUART clock source selection. Set or cleared by software. 00: Select APB as input clock 01: Select the system clock as the input clock 10: Select HSI (16MHz) as input clock 11: Select LSE as input clock
2:0	LPTIMSEL	LPTIM clock source selection.

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Bit Field	Name	Description
		Set or cleared by software. 000: select PCLK1 as input clock 001: Select LSI as input clock 010: Select HSI (16MHz) as input clock 011: Select LSE as input clock 100: Select COMP1 output as input clock 101: Select COMP2 output as input clock Other values: Configuration not allowed *Notice:* *When switching the clock source from COMP1/2 to other clock sources, it is recommended to turn off COMP1/2 before switching.*

4.3.16 PLL and HSI Configuration Register (RCC_PLLHSIPRE)

Address offset: 0x40

Reset value: 0x0000 0000

31–16
Reserved

15–2	1	0
Reserved	PLLSRC DIV	PLLHSI PRE
	rw	rw

Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	PLLSRCDIV	PLL clock source frequency division selection 0: No frequency division 1: 2 frequency division
0	PLLHSIPRE	HSI prescaler for PLL input Set and cleared by software to divide HSI before PLL entry. This bit can be written only when PLL is disabled. 0: HSI clock not divided 1: HSI clock divided by 2

4.3.17 SRAM Control/Status Register (RCC_SRAM_CTRLSTS)

Address offset: 0x44

Reset value: 0x0000 0000

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31–16
Reserved

15–6	5	4	3	2	1	0
Reserved	ERR2STS	ERR2 RSTEN	ERR2IEN	ERR1STS	ERR1 RSTEN	ERR1IEN
	rc_w1	rw	rw	rc_w1	rw	rw

Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	ERR2STS	SRAM2 parity error status bit. Software writes 1 to clear. 0: No parity error 1: There is a parity error
4	ERR2RSTEN	SRAM2 parity error reset enable bit. 0: System reset when parity error detected 1: No system reset when parity error is detected
3	ERR2IEN	SRAM2 parity error interrupt enable bit. 0: Trigger an interrupt when a parity error is detected 1: Not trigger an interrupt when a parity error is detected
2	ERR1STS	SRAM1 parity error status bit. Software writes 1 to clear. 0: no parity error 1: There is a parity error
1	ERR1RSTEN	SRAM1 parity error reset enable bit. 0: System reset when parity error detected 1: No system reset when parity error is detected
0	ERR1IEN	SRAM1 parity error interrupt enable bit. 0: Trigger an interrupt when a parity error is detected 1: Not trigger an interrupt when a parity error is detected

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5 GPIO and AFIO

5.1 Summary

GPIO (General purpose input/output) is general purpose I/O, and AFIO (Alternate-function input/output) is alternate function I/O. The chip supports up to 64 GPIOs, which are divided into 4 groups (GPIOA/GPIOB/GPIOC/GPIOD). GPIO ports share pins with other alternate peripherals, and users can configure them flexibly according to their needs. Each GPIO pin can be independently configured as an output, input or alternate peripheral function port. Except for the analog pins, other GPIO pins have high current capacity.

GPIO ports have the following characteristics:

- Each GPIO port can be individually configured into multiple modes by software
  - Input floating
  - Input pull-up
  - Input pull-down
  - Analog function
  - Open-drain output and pull-up/pull-down can be configured
  - Push-pull output and pull-up/pull-down can be configured
  - Push-pull alternate function and pull-up/pull-down can be configured
  - Open-drain alternate function and pull-up/pull-down can be configured
- Individual bit set or bit clear function
- All I/O supports external interrupt function
- All I/O supports low power mode wake-up, rising or falling edge configurable
  - 16 EXTI can be used to wake up from Stop2 mode, and all I/O can be reused as EXTI
  - PA8/PA0/PC13 can be used to wake up in Standby mode, the maximum I/O filter time is 5us
- Support software remapping I/O alternate function
- Support GPIO lock mechanism, reset the lock state to clear

Each I/O port bit can be programmed arbitrarily, but the I/O port registers must be accessed as 32-bit words (16-bit half-word or 8-bit byte access is not allowed). The figure below shows the basic structure of an I/O port.

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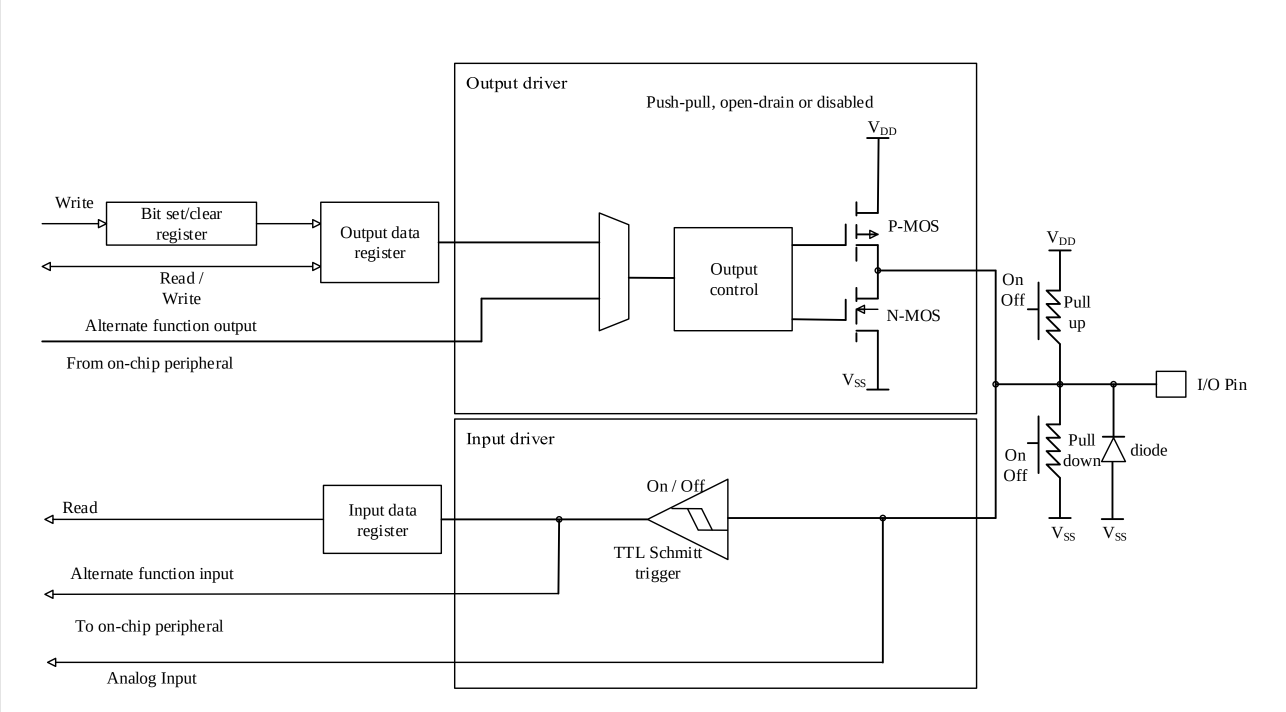
Figure 5-1 Basic structure of I/O port



5.2 I/O function description

5.2.1 I/O mode configuration

The I/O port mode can be configured through the registers GPIOx_PMODE, GPIOx_POTYPE and GPIOx_PUPD (x= A,B,C,D). The I/O configurations in different operation modes are shown in the following table:

Table 5-1 I/O port configuration table

PMODE[1:0]	POTYPE	PUPD[1:0]		I/O configuration
01	0	0	0	General-purpose output push-pull
	0	0	1	General-purpose output push-pull + pull-up
	0	1	0	General-purpose output push-pull + pull-down
	0	1	1	Reserved
	1	0	0	General-purpose output open-drain
	1	0	1	General-purpose output open-drain + pull-up
	1	1	0	General-purpose output open-drain + pull-down
	1	1	1	Reserved
10	0	0	0	Alternate function push-pull
	0	0	1	Alternate function push-pull + pull-up
	0	1	0	Alternate function push-pull + pull-down
	0	1	1	Reserved
	1	0	0	Alternate function open-drain

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PMODE[1:0]	POTYPE	PUPD[1:0]		I/O configuration
	1	0	1	Alternate function open-drain + pull-up
	1	1	0	Alternate function open-drain + pull-down
	1	1	1	Reserved
00	x	0	0	Input floating
	x	0	1	Input pull-up
	x	1	0	Input pull-down
	x	1	1	Reserved
11	x	0	0	Analog
	x	0	1	Reserved
	x	1	0	
	x	1	1	

The input and output characteristics of I/O under different configurations are shown in the following table：

Table 5-2 Input and output characteristics of different configurations

Feature	GPIO Input	GPIO Output	Analog	Alternate function
Output buffer	Disabled	Enabled	Disabled	Configure according to peripheral functions
Schmitt trigger	Enabled	Enabled	Disabled，Output is forced to 0	Enabled
PULL UP/DOWN/FLOAT	Configurable	Configurable	Disabled	Configurable
OPEN DRAIN	Disabled	Configurable, GPIO outputs 0 when the output data is "0", and GPIO high impedance when "1"	Disabled	Configurable, GPIO outputs 0 when the output data is "0", and GPIO high impedance when "1"
PUSH PULL MODE	Disabled	Configurable, when the output data is "0", the GPIO outputs 0, and when the output data is "1", the GPIO outputs 1	Disabled	Configurable, GPIO outputs 0 when the output data is "0", and GPIO high impedance when "1"
Input data register (I/O status)	Readable	Readable	Reads out 0	Readable
Output data register(Output value)	Invalid	Readable and writable	Invalid	Readable

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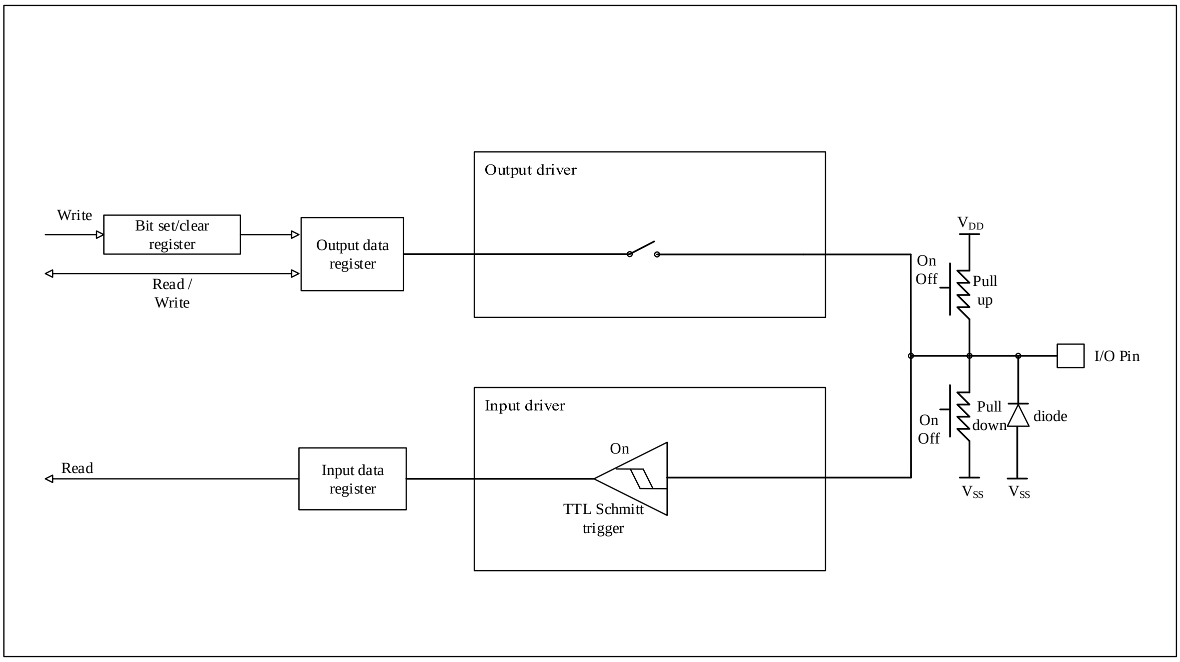
5.2.1.1 Input mode

When I/O port is configured in input mode:

- Schmitt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- Output buffer is disabled
- The data appearing on the I/O pin is sampled into the input data register
- Get I/O status by read access to data register

Figure 5-2 Input floating/pull-up/pull-down configuration



5.2.1.2 Output mode

When I/O port is configured as output mode:

- Schmidt trigger input is activated
- Whether the pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- Output buffer is activated
  - Open-drain mode: '0' on the output data register activates N-MOS, and the pin outputs low level.
    The '1' port on the output data register is placed in a high impedance state (P-MOS is never activated)
  - Push-pull mode: '0' on the output data register activates N-MOS, and the pin outputs low level.
    '1' on the output data register activates P-MOS, and the pin outputs high level.

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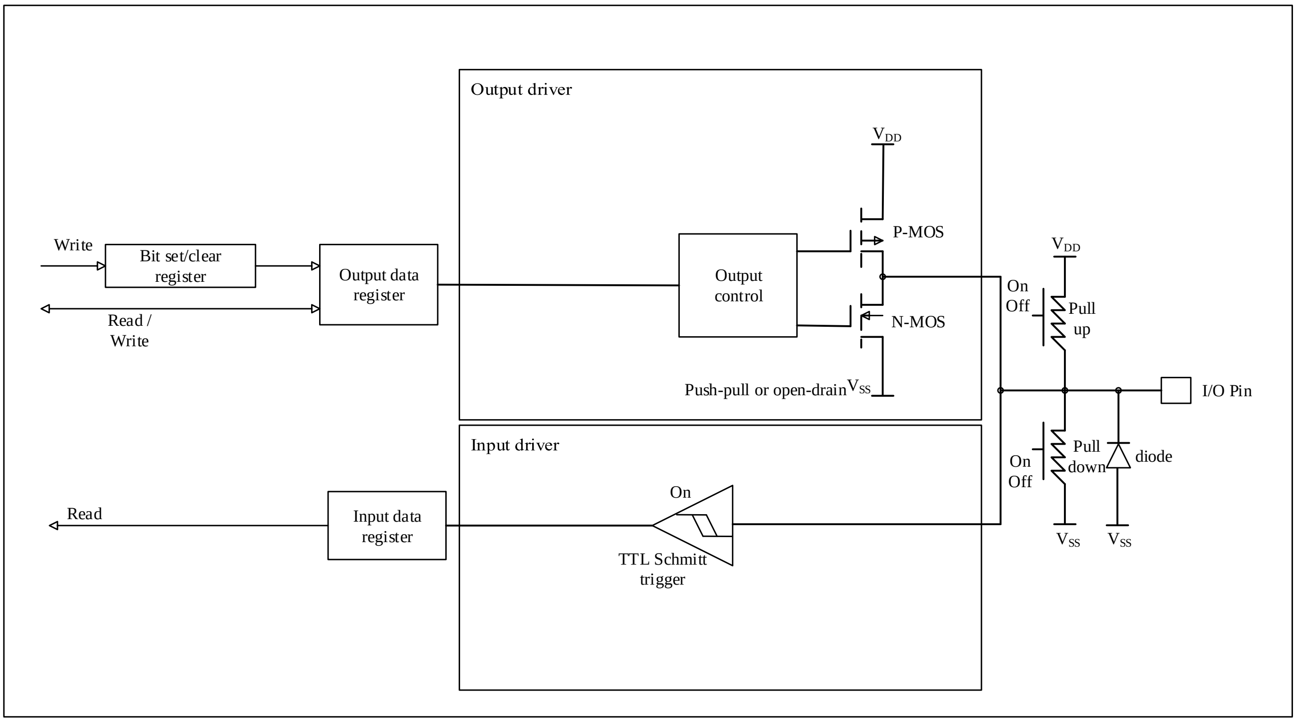
- The data appearing on the I/O pin is sampled into the input data register
- Read access to input data register for I/O status
- The read access to the output data register gets the last written value

Figure 5-3 Output mode configuration



5.2.1.3 Alternate function mode

When the I/O port is configured as alternate function mode:

- Schmidt trigger input is activated
- Whether the weak pull-up and pull-down resistors are connected depends on the configuration of the GPIOx_PUPD register
- In open-drain or push-pull configuration, the output buffer is controlled by the peripheral
- Signal-driven output buffer with built-in peripherals
- The data appearing on the I/O pin is sampled into the input data register
- Read access to input data register for I/O status

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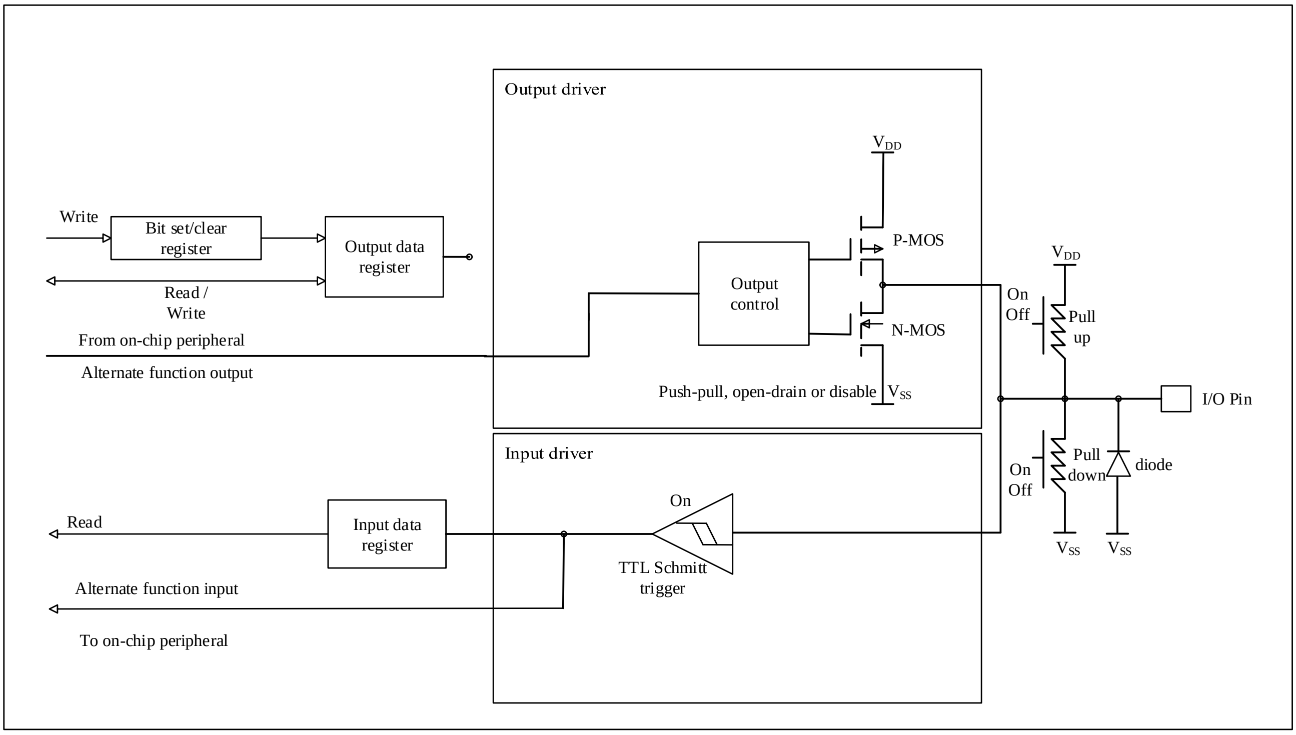
Figure 5-4 Alternate function configuration



5.2.1.4 Analog mode

When the I/O Port is programmed as analog mode：

- Schmitt trigger input is disabled and output value is forced to '0' (achieving zero consumption on each analog I/O pin)
- Pull-up and pull-down resistors are disabled
- When reading the input data register, the value is '0'
- Output buffer is disabled

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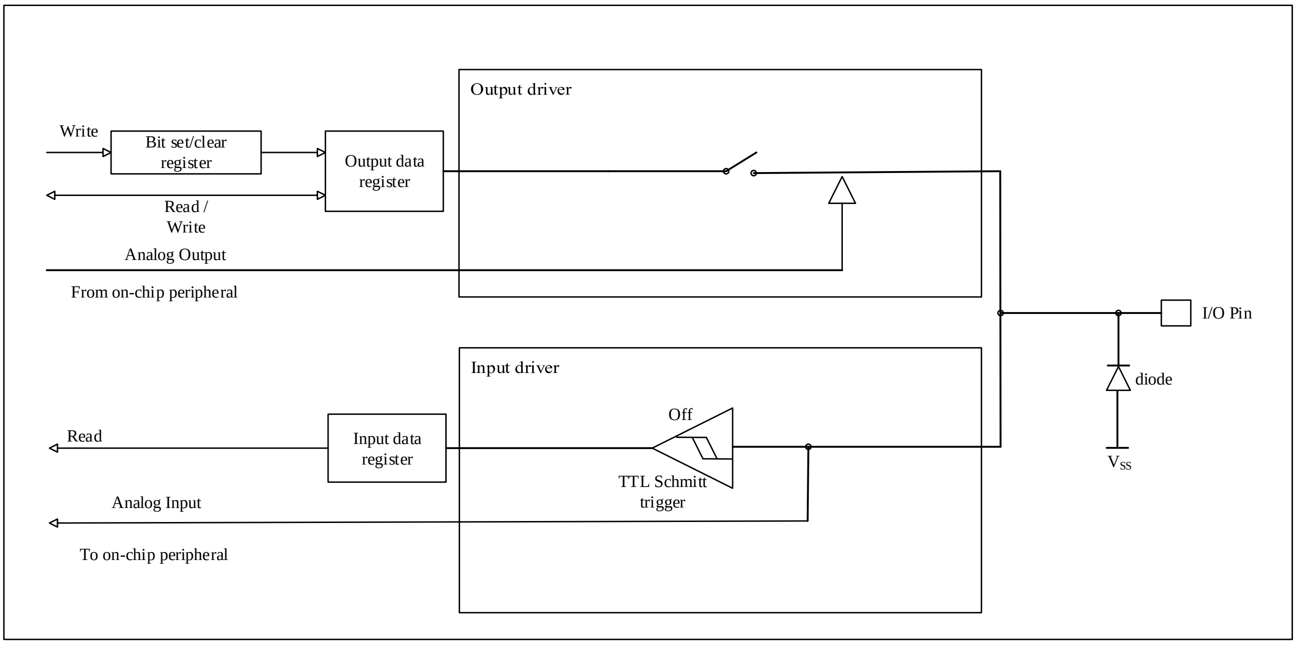
Figure 5-5 High impedance analog mode configuration



5.2.2 Status after reset

During and after reset, the alternate function is not turned on, and the I / O port is configured to analog function mode (GPIOx_PMODE.PMODEx[1:0]=11b). But there are several exceptional signals:

- NRST has no GPIO function by default, analog pins, no digital control
- The default input pull-down of BOOT0 pin
- After reset, start SWD_JTAG when debugging system related pins by default, and put JTAG pin into input pull-up or pull-down mode
  - PA15: JTDI in input pull-up mode
  - PA14: JTCK in input pull-down mode
  - PA13: JTMS in input pull-up mode
  - PB4: NJTRST in input pull-up mode
  - ◆ PB3[(1)]: JTD0 is placed in push-pull output without pull-up/pull-down (low level)
- PC13、PC14、PC15：
  - ◆ PC13~15 are three IOs in the LPR domain, and the default is analog mode when powered on for the first time

Note 1:Start Debug mode,PB3 outputs high level by default.

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5.2.3 Individual bit setting and bit clearing

By writing '1' to the bit to be changed in the "set register (GPIOx_PBSC) and reset register (GPIOx_PBC)", the individual bit operation of the data register (GPIOx_POD) can be realized, and one or more bits can be set. The bit written with '1' is set or cleared accordingly, and the bit not written with '1' will not be changed. The software does not need interrupt disable, and is completed in a single APB2 write operation.

5.2.4 External interrupt/wake-up line

All ports have external interrupt capability, which can be configured in the EXTI module, and the port must be configured in input mode.

5.2.5 Alternate function

When the I/O port is configured in alternate function mode. The port bit configuration register (GPIOx_AFL/ GPIOx_AFH) and output type register (GPIOx_POTYPE configuration push-pull or open-drain) must be programmed before use, alternate input or output is determined by the peripheral.

5.2.5.1 Clock output MCO

The microcontroller allows to output the clock signal to the external MCO pin (PA8). PA8 must be configured for alternate push-pull output function mode.

5.2.5.2 LPR domain PC13/PC14/PC15 function remapping

The mode of PC14/PC15 is determined according to the following priority order:

- When LSE is enabled (RCC_LDCTRL.LSEEN is set), PC14/PC15 pins will be forced to analog mode. If LSE is configured in external clock mode (RCC_LDCTRL.LSEBP is set), PC14 is forced to analog mode, OSC32_OUT (PC15) can also be used for other purposes
- If LSE is not enabled, RTC timestamp is enabled (RTC_CTRL.TSEN is set), and when PC14/PC15 is used as timestamp input (corresponding to register bit GPIOC_AFH.AFSEL= AF9), PC14/PC15 is forced to input floating mode, and enter the timestamp for the RTC
- In standby mode, PC14/PC15 automatically becomes input pull-down mode
- In the above three cases, PC14/PC15 is used as GPIO

When PC13 is used as the RTC pin, please refer to 14.3.8 chapter for specific configuration. If it is not used as an RTC pin, PC13 automatically becomes input pull-down mode in standby mode, otherwise it is used as GPIO normally.

5.2.5.3 HSE/LSE pins used as GPIO ports

OSC_IN and OSC_OUT of HSE are mapped to PD14 and PD15 respectively, and OSC32_IN and OSC32_OUT of LSE are mapped to PC14 and PC15 respectively. If HSE or LSE is off, the corresponding pin can be used as GPIO. If HSE or LSE is on, the corresponding pin goes into analog mode and bypasses the GPIO configuration.

The crystal oscillator is configured as user external clock mode, the pin remains as clock input, and OSC_OUT or OSC32_OUT can still be used as normal GPIO.

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5.2.5.4 JTAG/SWD alternate function remapping

The SWD-JTAG debug interface is enabled by default when the chip is powered on, and the debug interface is mapped to the GPIO port, as shown in the following table.

Alternate function	GPIO port	Remap
JTMS/SWDIO	PA13	AF0
JTCK/SWCLK	PA14	AF0
JTDI	PA15	AF0
JTDO	PB3	AF0
NJTRST	PB4	AF0

If you need to use its GPIO function during debugging, you can change the above remapping configuration by setting the alternate remapping and debugging I/O configuration registers (GPIOx_AFL or GPIOx_AFH). See the table below.

Table 5-3 Debug port image

Possible debug ports	SWD_JTAG I/O pin allocation				
	PA13/ JTMS/ SWDIO	PA14/ JTCK/ SWCLK	PA15/ JTDI	PB3/ JTDO	PB4/ NJTRST
Complete SWD-JTAG (JTAG-DP+SW-DP) (reset state)	I/O is not available	I/O is not available	I/O is not available	I/O is not available	I/O is not available
Complete SWD-JTAG (JTAG-DP+SW-DP) But there is no NJTRST.	I/O is not available	I/O is not available	I/O is not available	I/O is not available	I/O available
Turn off JTAG-DP and enable SW-DP.	I/O is not available	I/O is not available	I/O available	I/O available	I/O available
Turn off JTAG-DP and SW-DP.	I/O available	I/O available	I/O available	I/O available	I/O available

Since the JTAG pin is directly connected to the internal debug register (JTCK/SWCLK is directly connected to the clock terminal), it must be ensured that the JTAG input pin cannot be in a floating state. In order to avoid any uncontrolled I/O levels, the input pins of JTAG are fixed with internal pull-up/pull-down:

- NJTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- JTCK/SWCLK: internal pull-down

5.2.5.5 ADC external trigger alternate function remapping

The external trigger source of injection conversion and regular conversion of ADC supports remapping. See alternate remapping and debug I/O configuration register (AFIO_RMP_CFG).

Table 5-4 ADC external trigger injection conversion alternate function remapping

Alternate function	ADC_ETRI = 0	ADC_ETRI = 1

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ADC external trigger injection conversion	ADC external trigger injection conversion is connected to EXTI (0 - 15).	ADC external trigger injection conversion and TIM8_CH4 connection.

Table 5-5 ADC external trigger regular conversion alternate function remapping

Alternate function	ADC_ETRR = 0	ADC_ETRR = 1
ADC external trigger rule conversion	ADC external trigger regular conversion is connected to EXTI (0 - 15).	ADC external trigger regular conversion and TIM8_TRGO connection.

5.2.5.6 TIMx alternate function remapping

5.2.5.6.1 TIM1 alternate function remapping

Table 5-6 TIM1 alternate function remapping

Alternate function	**Pin**	**Remap**
TIM1_ETR	PA12	AF2
TIM1_CH1	PA8	AF2
TIM1_CH2	PA9	AF2
TIM1_CH3	PA10	AF2
TIM1_CH4	PA11	AF2
TIM1_BKIN	PA6	AF5
	PB12	AF5
TIM1_CH1N	PB13	AF2
	PA7	AF5
	PC13	AF2
TIM1_CH2N	PB14	AF2
	PB0	AF5
	PB6	AF7
TIM1_CH3N	PB15	AF2
	PB1	AF5
	PD14	AF2

5.2.5.6.2 TIM2 alternate function remapping

Table 5-7 TIM2 alternate function remapping

Alternate function	**Pin**	**Remap**
TIM2_ETR	PA0	AF5
	PA15	AF2
TIM2_CH1	PA0	AF2
	PA15	AF5
TIM2_CH2	PA1	AF2
	PB3	AF2
TIM2_CH3	PA2	AF2
	PB10	AF2
TIM2_CH4	PB11	AF2

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5.2.5.6.3 TIM3 alternate function remapping

Table 5-8 TIM3 alternate function remapping

Alternate function	Pin	Remap
TIM3_ETR	PD2	AF2
TIM3_CH1	PA6	AF2
	PB4	AF2
	PC6	AF2
TIM3_CH2	PA7	AF2
	PB5	AF4
	PC7	AF2
TIM3_CH3	PB0	AF2
	PC8	AF2
TIM3_CH4	PB1	AF2
	PC9	AF2

5.2.5.6.4 TIM4 alternate function remapping

Table 5-9 TIM4 alternate function remapping

Alternate function	Pin	Remap
TIM4_CH1	PB6	AF2
TIM4_CH2	PB7	AF2
TIM4_CH3	PB8	AF2
TIM4_CH4	PB9	AF2

5.2.5.6.5 TIM5 alternate function remapping

Table 5-10 TIM5 alternate function remapping

Alternate function	Pin	Remap
TIM5_CH1	PA0	AF1
TIM5_CH2	PA1	AF7
TIM5_CH3	PA2	AF6
TIM5_CH4	PA3	AF7

5.2.5.6.6 TIM8 alternate function remapping

Table 5-11 TIM8 alternate function remapping

Alternate function	Pin	Remap
TIM8_ETR	PA0	AF7
TIM8_CH1	PC6	AF6
TIM8_CH2	PC7	AF6
TIM8_CH3	PC8	AF6
TIM8_CH4	PC9	AF6
TIM8_BKIN	PA6	AF6

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Alternate function	Pin	Remap
TIM8_CH1N	PA7	AF6
TIM8_CH2N	PB0	AF7
TIM8_CH3N	PB1	AF0

5.2.5.6.7 TIM9 alternate function remapping

Table 5-12 TIM9 alternate function remapping

Alternate function	Pin	Remap
TIM9_ETR	PB2	AF1
TIM9_CH1	PB12	AF1
TIM9_CH2	PB13	AF1
TIM9_CH3	PB14	AF1
TIM9_CH4	PB15	AF1

5.2.5.7 LPTIM alternate function remapping

Table 5-13 LPTIM alternate function remapping

Alternate function	Pin	Remap
LPTIM_IN1	PB5	AF2
	PC0	AF0
LPTIM_IN2	PB7	AF5
	PC2	AF2
LPTIM_OUT	PB2	AF2
	PC1	AF0
LPTIM_ETR	PB6	AF8
	PC3	AF0

5.2.5.8 CAN alternate function remapping

CAN signals can be mapped to port A and port B as shown in the table below.

Table 5-14 CAN alternate function remapping

Alternate function	Pin	Remap
CAN_RX	PA11	AF1
	PB8	AF5
CAN_TX	PA12	AF1
	PB9	AF5

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5.2.5.9 USARTx alternate function remapping

5.2.5.9.1 USART1 alternate function remapping

Table 5-15 USART1 alternate function remapping

Alternate function	Pin	Remap
USART1_CTS	PA11	AF4
USART1_RTS	PA12	AF4
USART1_TX	PA4	AF1
	PA9	AF4
	PB6	AF0
	PB8	AF0
USART1_RX	PA5	AF4
	PA10	AF4
	PB7	AF0
USART1_CK	PA8	AF4

5.2.5.9.2 USART2 alternate function remapping

Table 5-16 USART2 alternate function remapping

Alternate function	Pin	Remap
USART2_CTS	PA0	AF4
	PA15	AF6
	PD3	AF0
USART2_RTS	PA1	AF4
	PB3	AF4
USART2_TX	PA2	AF4
	PB4	AF4
	PD14	AF4
USART2_RX	PA3	AF4
	PB5	AF6
	PD15	AF4
USART2_CK	PA4	AF4
	PA14	AF4

5.2.5.9.3 USART3 alternate function remapping

Table 5-17 USART3 alternate function remapping

Alternate function	Pin	Remap
USART3_CTS	PB13	AF7
USART3_RTS	PB14	AF7
USART3_TX	PB10	AF0
	PC10	AF5
USART3_RX	PB11	AF5

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Alternate function	Pin	Remap
USART3_CTS	PB13	AF7
USART3_RTS	PB14	AF7
	PC11	AF5
USART3_CK	PB12	AF4
	PC12	AF5

5.2.5.10 UARTx alternate function remapping

5.2.5.10.1 UART4 alternate function remapping

Table 5-18 UART4 alternate function remapping

Alternate function	Pin	Remap
UART4_TX	PB0	AF6
	PB14	AF6
	PC10	AF6
	PD13	AF6
UART4_RX	PB1	AF6
	PB15	AF6
	PC11	AF6
	PD12	AF6

5.2.5.10.2 UART5 alternate function remapping

Table 5-19 UART5 alternate function remapping

Alternate function	Pin	Remap
UART5_TX	PB4	AF6
	PB8	AF6
	PC12	AF6
UART5_RX	PB5	AF7
	PB9	AF6
	PD2	AF6

5.2.5.11 LPUART alternate function remapping

Table 5-20 LPUART alternate function remapping

Alternate function	Pin	Remap
LPUART_CTS	PA6	AF4
	PB13	AF4
LPUART_RTS	PB1	AF7
	PB12	AF2
	PB14	AF4
	PD2	AF0
LPUART_TX	PA1	AF6
	PA4	AF6

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Alternate function	Pin	Remap
LPUART_CTS	PA6	AF4
	PB13	AF4
LPUART_RTS	PB1	AF7
	PB12	AF2
	PB14	AF4
	PD2	AF0
	PB6	AF6
	PB10	AF4
	PC4	AF2
	PC10	AF0
LPUART_RX	PA0	AF6
	PA3	AF6
	PB7	AF6
	PB11	AF4
	PC5	AF2
	PC11	AF0

5.2.5.12 I2C alternate function remapping

5.2.5.12.1 I2C1 alternate function remapping

Table 5-21 I2C1 alternate function remapping

Alternate function	Pin	Remap
I2C1_SCL	PA4	AF7
	PA15	AF7
	PB6	AF1
	PB8	AF4
	PC0	AF7
	PC4	AF7
	PD13	AF7
I2C1_SDA	PA5	AF7
	PA14	AF7
	PB7	AF1
	PB9	AF4
	PC1	AF7
	PC5	AF7
	PD12	AF7
I2C1_SMBA	PB5	AF1

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5.2.5.12.2 I2C2 alternate function remapping

Table 5-22 I2C2 alternate function remapping

Alternate function	Pin	Remap
I2C2_SCL	PA3	AF5
	PA9	AF6
	PB10	AF6
	PB13	AF5
	PD15	AF6
I2C2_SDA	PA2	AF5
	PA8	AF6
	PA10	AF6
	PB11	AF6
	PB14	AF5
	PD14	AF6
I2C2_SMBA	PA8	AF1
	PB12	AF8

5.2.5.13 SPI/I2S alternate function remapping

5.2.5.13.1 SPI1 alternate function remapping

Table 5-23 SPI1 alternate function remapping

Alternate function	Pin	Remap
SPI1_I2S1_NSS_WS	PA4	AF0
	PA8	AF5
	PB6	AF4
	PD7	AF6
SPI1_I2S1_SCK_CK	PA5	AF0
	PA10	AF0
	PB3	AF1
	PD4	AF5
SPI1_I2S1_MISO_MCK	PA0	AF0
	PA6	AF0
	PB4	AF1
	PD5	AF5
SPI1_I2S1_MOSI_SD	PA7	AF0
	PB5	AF0
	PD6	AF5

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5.2.5.13.2 SPI2/I2S2 alternate function remapping

Table 5-24 SPI2/I2S2 alternate function remapping

Alternate function	Pin	Remap
SPI2_I2S2_NSS_WS	PA13	AF5
	PA15	AF1
	PB12	AF0
	PC6	AF5
SPI2_I2S2_SCK_CK	PA10	AF5
	PB6	AF5
	PB13	AF0
	PC7	AF5
	PD12	AF5
SPI2_I2S2_MISO_MCK	PA11	AF0
	PB14	AF0
	PC8	AF5
SPI2_I2S2_MOSI_SD	PA12	AF0
	PB15	AF0
	PC9	AF5

5.2.5.14 COMP alternate function remapping

5.2.5.14.1 COMP1 alternate function remapping

Table 5-25 COMP1 alternate function remapping

Alternate function	Pin	Remap
COMP1_OUT	PA0	AF8
	PA11	AF7
	PB6	AF9
	PB8	AF7

5.2.5.14.2 COMP2 alternate function remapping

Table 5-26 COMP2 alternate function remapping

Alternate function	Pin	Remap
COMP2_OUT	PA2	AF7
	PA6	AF7
	PA7	AF7
	PA12	AF7
	PA14	AF8
	PB9	AF7

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5.2.5.15 EVENTOUT alternate function remapping

Table 5-27 EVENTOUT alternate function remapping

Alternate function	Pin	Remap
EVENTOUT	PA0~PA13	AF3
	PA15	AF3
	PB0~PB15	AF3
	PC0~PC7	AF3
	PC9~PC13	AF3
	PD2	AF3
	PD12~PD13	AF3

5.2.5.16 RTC alternate function remapping

Table 5-28 RTC alternate function remapping

Alternate function	Pin	Remap
RTC_REFIN	PB15	AF9

5.2.5.17 LCD alternate function remapping

Table 5-29 LCD alternate function remapping

Alternate function	Pin	Remap
COM0	PA8	AF10
COM1	PA9	AF10
COM2	PA10	AF10
COM3	PA15	AF11
	PB9	AF10
COM4(1)	PD4(1)	AF10
	PC10(1)	AF10
COM5(1)	PD5(1)	AF10
	PC11(1)	AF10
COM6(1)	PD6(1)	AF10
	PC12(1)	AF10
COM7(1)	PD7(1)	AF10
	PD2(1)	AF10
SEG0~SEG2	PA1~PA3	AF10
SEG3~SEG4	PA6~PA7	AF10
SEG5~SEG6	PB0~PB1	AF10
SEG7~SEG9	PB3~PB5	AF10
SEG10~SEG15	PB10~PB15	AF10
SEG16	PB8	AF10
SEG17	PA15	AF10
SEG18~SEG27	PC0~PC9	AF10

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Alternate function	Pin	Remap
SEG28~SEG30(1)	PC10~PC12(1)	AF10
	PD4~PD6(1)	AF10
SEG31(1)	PD2(1)	AF10
	PD7(1)	AF10
SEG32~SEG33	PD0~PD1	AF10
SEG34	PD3	AF10
SEG35	PC13	AF10
SEG36~SEG39	PD8~PD11	AF10
SEG40~SEG42(1)	PD4~PD6(1)	AF10
	PC10~PC12(1)	AF10
SEG43(1)	PD7(1)	AF10
	PD2(1)	AF10

1. Due to the difference of the chip version, the corresponding pins of COM4~COM7, SEG28~SEG31, SEG40~SEG43 are different. It can be judged according to the second character of the 8-bit code in the last line of the chip silk screen:

Table 5-30 LCD pin mapping function distinction

Pin name	***Version B***	***Version C/Version D***
COM4	*PD4*	*PC10*
COM5	*PD5*	*PC11*
COM6	*PD6*	*PC12*
COM7	*PD7*	*PD2*
SEG28	*PC10*	*PD4*
SEG29	*PC11*	*PD5*
SEG30	*PC12*	*PD6*
SEG31	*PD2*	*PD7*
SEG40	*PD4*	*PC10*
SEG41	*PD5*	*PC11*
SEG42	*PD6*	*PC12*
SEG43	*PD7*	*PD2*

5.2.6 I/O configuration of peripherals

Table 5-31 ADC/DAC

ADC/DAC pin	GPIO configuration
ADC	Analog mode
DAC	Analog mode

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Table 5-32 TIM1/TIM8

TIM1/TIM8 pin	configuration	PAD configuration mode
TIM1/8_CHx	Input capture channel x	Input floating
	Output channel x	Push-pull alternate output
TIM1/8_CHxN	Complementary output channel x	Push-pull alternate output
TIM1/8_BKIN	Brake input	Input floating
TIM1/8_ETR	External trigger clock input	Input floating

Table 5-33 TIM2/3/4/5/9

TIM2/3/4/5/9 pin	configuration	PAD configuration mode
TIM2/3/4/5/9_CHx	Input capture channel x	Input floating
	Output channel x	Push-pull alternate output
TIM2/3/4/5/9_ETR	External trigger clock input	Input floating

Table 5-34 LPTIM

LPTIM pin	PAD configuration mode
LPTIM_INx	Input floating
LPTIM_OUT	Push-pull alternate output
LPTIM_ETR	Input floating

Table 5-35 CAN

CAN pin	GPIO configuration
CAN_TX	Push-pull alternate output
CAN_RX	Input floating or input pull-up

Table 5-36 USART

USART pin	configuration	GPIO configuration
USARTx_TX	full duplex transmissions	Push-pull alternate output
	Half duplex synchronous mode	Push-pull alternate output
USARTx_RX	full duplex transmissions	Input floating or input pull-up
	Half duplex synchronous mode	Unused, can be used as general I/O.
USARTx_CK	Synchronous mode	Push-pull alternate output
USARTx_RTS	Hardware flow control	Push-pull alternate output
USARTx_CTS	Hardware flow control	Input floating or input pull-up

Table 5-37 UART

USAR pin	configuration	GPIO configuration
UARTx_TX	full duplex transmissions	Push-pull alternate output
	Half duplex synchronous mode	Push-pull alternate output
UARTx_RX	full duplex transmissions	Input floating or input pull-up
	Half duplex synchronous mode	Unused, can be used as general I/O.

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Table 5-38 LPUART

LPUSART pin	configuration	GPIO configuration
LPUART_TX	Digital output	Push-pull alternate output
LPUART_RX	Digital input	Push-pull alternate output
LPUART _CTS	Hardware flow control	Input floating or input pull-up
LPUART _RTS	Hardware flow control	Push-pull alternate output

Table 5-39 I2C

I2C pin	configuration	GPIO configuration
I2Cx_SCL	I2C clock	Open-drain alternate output
I2Cx_SDA	I2C data	Open-drain alternate output
I2Cx_SMBA	SMBA data	Push-pull alternate output

Table 5-40 SPI-I2S

SPI-I2S pin	configuration	GPIO configuration
SPIx_I2Sx_MOSI_SD	Master mode	Push-pull alternate output
	Slave mode	Input floating or input pull-up or push-pull alternate output
SPIx_I2Sx_MISO_MCK	Master mode	Input floating or input pull-up or push-pull alternate output
	Slave mode	Push-pull alternate output
SPIx_I2Sx_NSS_WS	Master mode	Push-pull alternate output
	Slave mode	Push-pull alternate output
SPIx_I2Sx_SCK_CK	Master mode	Push-pull alternate output
	Slave mode	Push-pull alternate output

Table 5-41 USB

USB pin	GPIO configuration
USB_DM USB_DP	Once the USB module is enabled, these pins are automatically connected to the internal USB transceiver

Table 5-42 JTAG/SWD

JTAG/SWD pin	configuration	GPIO configuration
JTMS/SWDIO	Input pull-up	Push-pull alternate output + pull-up
JTCK/SWCLK	Pull-down output	Push-pull alternate output + pull-up
JTDI	Input pull-up	Push-pull alternate output + pull-up
JTDO	Output	Push-pull alternate output
NJTRST	Input pull-up	Push-pull alternate output + pull-up

Table 5-43 Other

pin	Alternate function	GPIO configuration
EVENT_OUT	EVENT OUT	Push-pull alternate output

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pin	Alternate function	GPIO configuration
COMPx_OUT	COMP	Push-pull alternate output
MCO	clock output	Push-pull alternate output
LCD_COMx	LCD common output	Analog mode
LCD_SEGx	LCD segment output	Analog mode
EXTI Input Line	External interrupt input	Input floating or input pull-up or input pull-down

5.2.7 GPIO locking mechanism

The locking mechanism is used to freeze the I/O configuration to prevent accidental changes. When a lock (LOCK) procedure is performed on a port bit, the configuration of the port cannot be changed until the next reset, refer to the port configuration lock register GPIOx_PLOCK.

- PLOCKK, that is, GPIOx_PLOCK [16], becomes 1 only after the correct sequence w1-> w0-> w1-> r0 (r0 here is also a must). After that, it becomes 0 only if the system reset is performed. GPIOx_PLOCK.PLOCK[15:0] can only be modified at GPIOx_PLOCK.PLOCKK=0.
- The lock sequence to set GPIOx_PLOCK.PLOCKK bit, w1-> w0-> w1-> r0 will be valid only if the value (1 or 0) in GPIOx_PLOCK.PLOCK [15:0] does not change during this sequence.The GPIOx_PLOCK.PLOCKK bit will not be set if the value in GPIOx_PLOCK.PLOCK [15:0] changes during this sequence.
- As long as GPIOx_PLOCK.PLOCKK=0 and GPIOx_PLOCK.PLOCKx=0 or 1, all configuration and alternate function bits can be modified. When GPIOx_PLOCK.PLOCKK=1 but GPIOx_PLOCK.PLOCK[x]=0, the corresponding configuration and alternate function bits corresponding to GPIOx_PLOCK.PLOCK[x]=0 can be modified.
- Only when GPIOx_PLOCK.PLOCKK=1 and GPIOx_PLOCK.PLOCK[x]=1, the configurations corresponding to GPIOx_PLOCK.PLOCK[x]=1 are locked and can not be modified.
- If the lock sequence operation is wrong, then it must be redone (w1-> w0-> w1-> r0) to initiate the lock operation again.

5.3 GPIO register

These peripheral registers must be operated as 32-bit words.

5.3.1 GPIO register overview

GPIOA base address: 0x40010800

GPIOB base address: 0x40010C00

GPIOC base address: 0x40011000

GPIOD base address: 0x40011400

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Table 5-44 GPIO register overview

Offset	Register		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	GPIOx_PMODE		PMODE15[1:0]		PMODE14[1:0]		PMODE13[1:0]		PMODE12[1:0]		PMODE11[1:0]		PMODE10[1:0]		PMODE9[1:0]		PMODE8[1:0]		PMODE07[1:0]		PMODE6[1:0]		PMODE05[1:0]		PMODE4[1:0]		PMODE03[1:0]		PMODE2[1:0]		PMODE01[1:0]		PMODE0[1:0]	
	Reset Value	x=A	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		x=B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1
		x=C	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		x=D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
004h	GPIOx_POTYPE		Reserved																POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	GPIOx_SR		Reserved																SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
	Reset Value																		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
00Ch	GPIOx_PUPD		PUPD15[1:0]		PUPD14[1:0]		PUPD13[1:0]		PUPD12[1:0]		PUPD11[1:0]		PUPD10[1:0]		PUPD9[1:0]		PUPD8[1:0]		PUPD7[1:0]		PUPD6[1:0]		PUPD5[1:0]		PUPD4[1:0]		PUPD3[1:0]		PUPD2[1:0]		PUPD1[1:0]		PUPD0[1:0]	
	Reset Value	x=A	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		x=B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		x=C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		x=D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
010h	GPIOx_PID		Reserved																PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
	Reset Value																		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
014h	GPIOx_POD		Reserved																POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	GPIOx_PBSC		PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0	PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	GPIOx_PLOCK		Reserved															PLOCKK	PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	GPIOx_AFL		AFSEL7[3:0]				AFSEL6[3:0]				AFSEL5[3:0]				AFSEL4[3:0]				AFSEL3[3:0]				AFSEL2[3:0]				AFSEL1[3:0]				AFSEL0[3:0]			
	Reset Value	x=A,C,D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		x=B	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
024h	GPIOx_AFH		AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]				AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
	Reset Value	x=A	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		x= B,C,D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
028h	GPIOx_PBC		Reserved																PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
02Ch	GPIOx_DS	DS15[1:0]		DS14[1:0]		DS13[1:0]		DS12[1:0]		DS11[1:0]		DS10[1:0]		DS9[1:0]		DS8[1:0]		DS7[1:0]		DS6[1:0]		DS5[1:0]		DS4[1:0]		DS3[1:0]		DS2[1:0]		DS1[1:0]		DS0[1:0]	
	Reset Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

5.3.2 GPIO mode description register (GPIOx_PMODE)

Address: 0x00

Reset value: 0xABFF FFFF（x=A）; 0xFFFF FEBF（x=B）; 0xFFFF FFFF（x=C）; 0xFFFF FFFC（x=D）

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
PMODE15[1:0]	PMODE14[1:0]	PMODE13[1:0]	PMODE12[1:0]	PMODE11[1:0]	PMODE10[1:0]	PMODE9[1:0]	PMODE8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PMODE7[1:0]	PMODE6[1:0]	PMODE5[1:0]	PMODE4[1:0]	PMODE3[1:0]	PMODE2[1:0]	PMODE1[1:0]	PMODE0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	PMODEy[1:0]	Mode bits for port x (y = 0…15) 00: Input mode 01: General output mode 10: Alternate function mode 11: Analog function mode (state after reset)

5.3.3 GPIO type definition (GPIOx_POTYPE)

Address: 0x04

Reset value: 0x0000 0000（x= A,B,C,D）

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31															16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POT15	POT14	POT13	POT12	POT11	POT10	POT9	POT8	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	**Name**	**Description**
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	POTy	Output mode bits for port x (y = 0…15) 0: Output push-pull mode (state after reset) 1: Output open-drain mode

5.3.4 GPIO port slew rate configuration register (GPIOx_SR)

Address: 0x08

Reset value: 0x0000 FFFF（x= A,B,C,D）

31															16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	**Name**	**Description**
31:16	Reserved	Reserved,the reset value must be maintained.
15:0	SRy	Toggle rate configuration bits y for port GPIOx (y = 0…15) These bits can only be read or written as 16-bit words. 0：Fast slew rate 1：Slow slew rate

5.3.5 GPIO pull-up/pull-down description register (GPIOx_PUPD)

Address: 0x0C

Reset value: 0x6400 0000（x=A）；0x0000 0100（x=B）；0x0000 0000（x=C）；0x0000 0002（x=D）

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
PUPD15[1:0]	PUPD14[1:0]	PUPD13[1:0]	PUPD12[1:0]	PUPD11[1:0]	PUPD10[1:0]	PUPD9[1:0]	PUPD8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PUPD7[1:0]	PUPD6[1:0]	PUPD5[1:0]	PUPD4[1:0]	PUPD3[1:0]	PUPD2[1:0]	PUPD1[1:0]	PUPD0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	PUPDy[1:0]	Mode bits for port x (y = 0…15) 00: No pull-up, pull-down 01: Pull-up 10: Pull-down 11: Reserved

5.3.6 GPIO input data register (GPIOx_PID)

Address: 0x10

Reset value: 0x0000 0000（x=A,B,C,D）

31															16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained.
15:0	PIDy	Port input data (y = 0…15) These bits are read-only and can only be read in the form of 16-bit words, and the read value is the state of the corresponding I/O port.

5.3.7 GPIO output data register (GPIOx_POD)

Address: 0x14

Reset value: 0x0000 0000（x=A,B,C,D）

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31															16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved,the reset value must be maintained.
15:0	PODy	Port output data (y = 0…15) These bits can only be read or written as 16-bit words. For GPIOx_PBSC (x = A…D), the corresponding POD bits can be independently set/cleared.

5.3.8 GPIO bit set/clear register (GPIOx_PBSC)

Address: 0x18

Reset value: 0x0000 0000（x=A,B,C,D）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit field	Name	Description
31:16	PBCy	Clear bit y of port GPIOx (y = 0…15) These bits can only be written and operated as words (16 bits). 0: Does not affect the corresponding PODy bit 1: Clear the corresponding PODy bit to 0 *Note: if the corresponding bits of PBSy and PBCy are set at the same time, the PBSy bit works.*
15:0	PBSy	Set bit y of port GPIOx (y = 0…15) These bits can only be written and operated as words (16 bits). 0: Does not affect the corresponding PODy bit 1: Set the corresponding PODy bit to 1

5.3.9 GPIO configuration lock register (GPIOx_PLOCK)

Address: 0x1C

Reset value: 0x0000 0000（x=A,B,C,D）

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31–17	16
Reserved	PLOCKK
	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLOCK15	PLOCK14	PLOCK13	PLOCK12	PLOCK11	PLOCK10	PLOCK9	PLOCK8	PLOCK7	PLOCK6	PLOCK5	PLOCK4	PLOCK3	PLOCK2	PLOCK1	PLOCK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:17	Reserved	Reserved,the reset value must be maintained.
16	PLOCKK	Lock key. This bit can be read at any time, and it can only be modified by the key lock write sequence. 0: Port configuration lock key is activated 1: The port configuration lock key is activated, and the GPIOx_PLOCK register is locked before the next system reset. The write sequence of the lock key: Write 1 -> write 0 -> write 1 -> read 0 -> read 1 The last reading can be omitted, but it can be used to confirm that the lock key has been activated. *Note: the value of PLOCK[15:0] cannot be changed when the writing sequence of lock key is operated. Any error in the operation key writing sequence will not activate the key.*
15:0	PLOCKy	Configuration lock bit y of port GPIOx (y = 0…15) These bits are readable and writable but can only be written when the PLOCKK bit is 0. 0: Do not lock the configuration of the port 1: Lock the configuration of the port

5.3.10 GPIO alternate function low register (GPIOx_AFL)

Address: 0x20

Reset value: 0xFFFF FFFF（x=A,C,D）; 0xFFF0 0FFF（x=B）

31–28	27–24	23–20	19–16
AFSEL7[3:0]	AFSEL6[3:0]	AFSEL5[3:0]	AFSEL4[3:0]
rw	rw	rw	rw

15–12	11–8	7–4	3–0
AFSEL3[3:0]	AFSEL2[3:0]	AFSEL1[3:0]	AFSEL0[3:0]
rw	rw	rw	rw

Bit field	Name	Description
31:28 27:24 23:20 19:16 15:12	AFSELy[3:0]	Alternate function configuration bits y for port GPIOx (y = 0…7) 0000：AF0 0001：AF1 0010：AF2 0011：AF3

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Bit field	Name	Description
11:8 7:4 3:0		0100：AF4 0101：AF5 0110：AF6 0111：AF7 1000：AF8 1001：AF9 1010：AF10 1011：AF11 1100：AF12 1101：AF13 1110：AF14 1111：AF15 (No alternate function)

5.3.11 GPIO alternate function High register (GPIOx_AFH)

Address: 0x24

Reset value: 0x000F FFFF（x=A）；0xFFFF FFFF（x=B,C,D）

31 … 28	27 … 24	23 … 20	19 … 16
AFSEL15[3:0]	AFSEL14[3:0]	AFSEL13[3:0]	AFSEL12[3:0]
rw	rw	rw	rw
15 … 12	**11 … 8**	**7 … 4**	**3 … 0**
AFSEL11[3:0]	AFSEL10[3:0]	AFSEL9[3:0]	AFSEL8[3:0]
rw	rw	rw	rw

Bit field	Name	Description
31:28 27:24 23:20 19:16 15:12 11:8 7:4 3:0	AFSELy[3:0]	Alternate function configuration bits y for port GPIOx（y = 8…15） 0000：AF0 0001：AF1 0010：AF2 0011：AF3 0100：AF4 0101：AF5 0110：AF6 0111：AF7 1000：AF8 1001：AF9 1010：AF10 1011：AF11 1100：AF12 1101：AF13 1110：AF14 1111：AF15 (No alternate function)

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5.3.12 GPIO bit clear register (GPIOx_PBC)

Address: 0x28

Reset value: 0x0000 0000（x=A,B,C,D）

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PBCy	Clear bit y of port GPIOx (y = 0...15) These bits can only be written and operated as words (16 bits). 0: Does not affect the corresponding PODy bit 1: Clear the corresponding PODy bit to 0

5.3.13 GPIO driver strength configuration register (GPIOx_DS)

Address: 0x2C

Reset value: 0x5555 5555（x=A,B,C,D）

31:30	29:28	27:26	25:24	23:22	21:20	19:18	17:16
DS15[1:0]	DS14[1:0]	DS13[1:0]	DS12[1:0]	DS11[1:0]	DS10[1:0]	DS9[1:0]	DS8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
DS7[1:0]	DS6[1:0]	DS5[1:0]	DS4[1:0]	DS3[1:0]	DS2[1:0]	DS1[1:0]	DS0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:30 29:28 27:26 25:24 23:22 21:20 19:18 17:16 15:14 13:12 11:10 9:8	DSy[1:0]	Port GPIOx drive capability configuration bits y (y = 0…15) 00：2mA 01：8mA 10：4mA 11：12mA

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Bit field	Name	Description
7:6 5:4 3:2 1:0		

5.4 AFIO register

5.4.1 AFIO register overview

AFIO base address: 0x40010000

Table 5-45 AFIO register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	AFIO_RMP_CFG	Reserved																				SPI1_NSS	SPI2_NSS	ADC_ETRI	ADC_ETRR	EXTI_ETRI[3:0]				EXTI_ETRR[3:0]			
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
004h	AFIO_EXTI_CFG1	Reserved																		EXTI3[1:0]		Reserved		EXTI2[1:0]		Reserved		EXTI1[1:0]		Reserved		EXTI0[1:0]	
	Reset Value																			0	0			0	0			0	0			0	0
008h	AFIO_EXTI_CFG2	Reserved																		EXTI7[1:0]		Reserved		EXTI6[1:0]		Reserved		EXTI5[1:0]		Reserved		EXTI4[1:0]	
	Reset Value																			0	0			0	0			0	0			0	0
00Ch	AFIO_EXTI_CFG3	Reserved																		EXTI11[1:0]		Reserved		EXTI10[1:0]		Reserved		EXTI9[1:0]		Reserved		EXTI8[1:0]	
	Reset Value																			0	0			0	0			0	0			0	0
010h	AFIO_EXTI_CFG4	Reserved																		EXTI15[1:0]		Reserved		EXTI14[1:0]		Reserved		EXTI13[1:0]		Reserved		EXTI12[1:0]	
	Reset Value																			0	0			0	0			0	0			0	0

5.4.2 AFIO mapping configuration control register (AFIO_RMP_CFG)

Address: 0x00

Reset value: 0x0000 0000

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31–16
Reserved

15–12	11	10	9	8	7–4	3–0
Reserved	SPI1_NSS	SPI2_NSS	ADC _ETRI	ADC _ETRR	EXTI_ETRI[3:0]	EXTI_ETRR[3:0]
	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	SPI1_NSS	NSS mode selection bit of SPI1 (NSS is configured in AFIO push-pull mode) 0: NSS is in a high-impedance state when idle 1: NSS is high when idle
10	SPI2_NSS	NSS mode selection bit of SPI2 (NSS is configured in AFIO push-pull mode) 0: NSS is in a high-impedance state when idle 1: NSS is high when idle
9	ADC_ETRI	ADC injection conversion external trigger remapping This bit can be set to '1' or '0' by software. It controls the trigger input connected to the external trigger for ADC injection conversion. 0: ADC injection conversion external trigger is connected to EXTI (0-15) 1: ADC injection conversion external trigger is connected to TIM8_CH4.
8	ADC_ETRR	ADC rule conversion external trigger remapping This bit can be set to '1' or '0' by software. It controls the trigger input connected to the ADC regular conversion external trigger. 0: ADC regular conversion external trigger is connected to EXTI (0-15) 1: ADC regular conversion external trigger is connected to TIM8_TAGO
7:4	EXTI_ETRI[3:0]	Select interrupt line injection to convert external trigger remapping
3:0	EXTI_ETRR[3:0]	Select interrupt line regular to convert external trigger remapping

5.4.3 AFIO external interrupt configuration register 1(AFIO_EXTI_CFG1)

Address: 0x04

Reset value: 0x0000 0000

31–16
Reserved

15–14	13–12	11–10	9–8	7–6	5–4	3–2	1–0
Reserved	EXTI3_CFG[1:0]	Reserved	EXTI2_CFG[1:0]	Reserved	EXTI1_CFG[1:0]	Reserved	EXTI0_CFG[1:0]
	rw		rw		rw		rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:12	EXTI3[1:0]	00：PA3 pin 01：PB3 pin

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Bit field	Name	Description
		10：PC3 pin 11：PD3 pin
11:10	Reserved	Reserved, the reset value must be maintained.
9:8	EXTI2[1:0]	00：PA2 pin 01：PB2 pin 10：PC2 pin 11：PD2 pin
7:6	Reserved	Reserved, the reset value must be maintained.
5:4	EXTI1[1:0]	00：PA1 pin 01：PB1 pin 10：PC1 pin 11：PD1 pin
3:2	Reserved	Reserved, the reset value must be maintained.
1:0	EXTI0[1:0]	00：PA0 pin 01：PB0 pin 10：PC0 pin 11：PD0 pin

5.4.4 AFIO external interrupt configuration register 2(AFIO_EXTI_CFG2)

Address: 0x08

Reset value: 0x0000 0000

31 … 16
Reserved

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved	EXTI7_CFG[1:0]	Reserved	EXTI6_CFG[1:0]	Reserved	EXTI5_CFG[1:0]	Reserved	EXTI4_CFG[1:0]
	rw		rw		rw		rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:12	EXTI7[1:0]	00：PA7 pin 01：PB7 pin 10：PC7 pin 11：PD7 pin
11:10	Reserved	Reserved, the reset value must be maintained.
9:8	EXTI6[1:0]	00：PA6 pin 01：PB6 pin 10：PC6 pin 11：PD6 pin
7:6	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
5:4	EXTI5[1:0]	00：PA5 pin 01：PB5 pin 10：PC5 pin 11：PD5 pin
3:2	Reserved	Reserved, the reset value must be maintained.
1:0	EXTI4[1:0]	00：PA4 pin 01：PB4 pin 10：PC4 pin 11：PD4 pin

5.4.5 AFIO external interrupt configuration register 3(AFIO_EXTI_CFG3)

Address: 0x0C

Reset value: 0x0000 0000

31–16
Reserved

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved	EXTI11_CFG[1:0]	Reserved	EXTI10_CFG[1:0]	Reserved	EXTI9_CFG[1:0]	Reserved	EXTI8_CFG[1:0]
	rw		rw		rw		rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:12	EXTI11[1:0]	00：PA11 pin 01：PB11 pin 10：PC11 pin 11：PD11 pin
11:10	Reserved	Reserved, the reset value must be maintained.
9:8	EXTI10[1:0]	00：PA10 pin 01：PB10 pin 10：PC10 pin 11：PD10 pin
7:6	Reserved	Reserved, the reset value must be maintained.
5:4	EXTI9[1:0]	00：PA9 pin 01：PB9 pin 10：PC9 pin 11：PD9 pin
3:2	Reserved	Reserved, the reset value must be maintained
1:0	EXTI8[1:0]	00：PA8 pin 01：PB8 pin 10：PC8 pin

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Bit field	Name	Description
		11：PD8 pin

5.4.6 AFIO external interrupt configuration register 4(AFIO_EXTI_CFG4)

Address: 0x10

Reset value: 0x0000 0000

31–16
Reserved

15–14	13–12	11–10	9–8	7–6	5–4	3–2	1–0
Reserved	EXTI15_CFG[1:0]	Reserved	EXTI14_CFG[1:0]	Reserved	EXTI13_CFG[1:0]	Reserved	EXTI12_CFG[1:0]
	rw		rw		rw		rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:12	EXTI15[1:0]	00：PA15 pin 01：PB15 pin 10：PC15 pin 11：PD15 pin
11:10	Reserved	Reserved, the reset value must be maintained.
9:8	EXTI14[1:0]	00：PA14 pin 01：PB14 pin 10：PC14 pin 11：PD14 pin
7:6	Reserved	Reserved, the reset value must be maintained.
5:4	EXTI13[1:0]	00：PA13 pin 01：PB13 pin 10：PC13 pin 11：PD13 pin
3:2	Reserved	Reserved, the reset value must be maintained.
1:0	EXTI12[1:0]	00：PA12 pin 01：PB12 pin 10：PC12 pin 11：PD12 pin

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6 Interrupts and events

6.1 Nested vector interrupt register

Features

- 66 maskable interrupt channels (excluding 16 Cortex-M4 interrupt lines).
- 16 programmable priority levels (using 4-bit interrupt priority);
- Low-latency exception and interrupt handling;
- Power management control;
- Implementation of system control registers;

The nested vector interrupt Controller (NVIC) is closely linked to the processor core, enabling low latency interrupt processing and efficient processing of late interrupts. The nested vector interrupt controller manages interrupts including core exceptions.

6.1.1 SysTick calibration value register

The system tick calibration value is fixed at 13500. When the system tick clock is set to 13.5MHz (the maximum value of HCLK/8), 1ms time reference is generated.

6.1.2 Interrupt and exception vectors

Table 6-1 Vector table

Position	Priority	Priority type	Name	Description	Address
-	-	-	-	Reserved	0x0000_0000
-	-3	Fixed	Reset	Reset	0x0000_0004
-	-2	Fixed	NMI	Non-maskable interrupt. RCC clock security system (CSS) is connected to NMI vector.	0x0000_0008
-	-1	Fixed	HardFault	All types of errors (fault)	0x0000_000C
-	0	Settable	MemManage	Memory management	0x0000_0010
-	1	Settable	BusFault	Prefetch means failure. Memory access failed	0x0000_0014
-	2	Settable	UsageFault	Undefined instruction or illegal status	0x0000_0018
-	-	-	-	Reserved	0x0000_001C ~0x0000_002B
-	3	Settable	SVCall	System services invoked by SWI directives	0x0000_002C
-	4	Settable	DebugMonitor	Debug monitor	0x0000_0030

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Position	Priority	Priority type	Name	Description	Address
-	-	-	-	Reserved	0x0000_0034
-	5	Settable	PendSV	System services that can be suspended	0x0000_0038
-	6	Settable	SysTick	System tick timer	0x0000_003C
0	7	Settable	WWDG	Window timer interrupt	0x0000_0040
1	8	Settable	PVD	Power supply voltage detection (PVD) interrupt connected to EXTI line 16	0x0000_0044
2	9	Settable	RTC_TAMPER_STAMP	RTC timestamp interrupt connected to EXTI line 19	0x0000_0048
3	10	Settable	RTC_WKUP	Real time clock (RTC) wake up interrupt connected to EXTI line 20	0x0000_004C
4	11	Settable	FLASH	Flash global interrupt	0x0000_0050
5	12	Settable	RCC	Reset and clock control (RCC) interrupt	0x0000_0054
6	13	Settable	EXTI0	EXTI line 0 interrupt	0x0000_0058
7	14	Settable	EXTI1	EXTI line 1 interrupt	0x0000_005C
8	15	Settable	EXTI2	EXTI line 2 interrupt	0x0000_0060
9	16	Settable	EXTI3	EXTI line 3 interrupt	0x0000_0064
10	17	Settable	EXTI4	EXTI line 4 interrupt	0x0000_0068
11	18	Settable	The DMA channel 1	DMA channel 1 global interrupt	0x0000_006C
12	19	Settable	The DMA channel 2	DMA channel 2 global interrupt	0x0000_0070
13	20	Settable	The DMA channel 3	DMA channel 3 global interrupt	0x0000_0074
14	21	Settable	The DMA channel 4	DMA channel 4 global interrupt	0x0000_0078
15	22	Settable	The DMA channel 5	DMA channel 5 global interrupt	0x0000_007C
16	23	Settable	The DMA channel 6	DMA channel 6 global interrupt	0x0000_0080
17	24	Settable	The DMA channel 7	DMA channel 7 global interrupt	0x0000_0084
18	25	Settable	The DMA channel 8	DMA channel 8 global interrupt	0x0000_0088
19	26	Settable	ADC	ADC global interrupt	0x0000_008C
20	27	Settable	USB_HP	USB high priority interrupt	0x0000_0090
21	28	Settable	USB_LP	USB low priority interrupt	0x0000_0094
22	29	Settable	COMP	COMP1/COMP2 interrupt connected to EXTI line 21/22	0x0000_0098
23	30	Settable	EXTI9_5	EXTI line [9:5] interrupt	0x0000_009C
24	31	Settable	TIM1_BRK	TIM1 brake interrupt	0x0000_00A0
25	32	Settable	TIM1_UP	TIM1 update interrupt	0x0000_00A4
26	33	Settable	TIM1_TRG_COM	TIM1 triggers and communication interrupt	0x0000_00A8
27	34	Settable	TIM1_CC	TIM1 capture comparison interrupt	0x0000_00AC
28	35	Settable	TIM2	TIM2 global interrupt	0x0000_00B0
29	36	Settable	TIM3	TIM3 global interrupt	0x0000_00B4
30	37	Settable	TIM4	TIM4 global interrupt	0x0000_00B8

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Position	Priority	Priority type	Name	Description	Address
31	38	Settable	I2C1_EV	I2C1 event interrupt	0x0000_00BC
32	39	Settable	I2C1_ER	I2C1 error interrupt	0x0000_00C0
33	40	Settable	I2C2_EV	I2C2 event interrupt	0x0000_00C4
34	41	Settable	I2C2_ER	I2C2 error interrupt	0x0000_00C8
35	42	Settable	SPI1	SPI1 global interrupt	0x0000_00CC
36	43	Settable	SPI2	SPI2 global interrupt	0x0000_00D0
37	44	Settable	USART1	USART1 global interrupt	0x0000_00D4
38	45	Settable	USART2	USART2 global interrupt	0x0000_00D8
39	46	Settable	USART3	USART3 global interrupt	0x0000_00DC
40	47	Settable	EXTI15_10	EXTI line [15:10] interrupt	0x0000_00E0
41	48	Settable	RTC Alarm	RTC alarm interrupt connected to EXTI line 18	0x0000_00E4
42	49	Settable	USBWKUP	USB wake up failure interrupt connected to EXTI line 17	0x0000_00E8
43	50	Settable	TIM8_BRK	TIM8 brake failure	0x0000_00EC
44	51	Settable	TIM8_UP	TIM8 update interrupt	0x0000_00F0
45	52	Settable	TIM8_TRG_COM	TIM8 triggers and communication interrupt	0x0000_00F4
46	53	Settable	TIM8_CC	TIM8 capture comparison interrupt	0x0000_00F8
47	54	Settable	UART4	UART4 global interrupt	0x0000_00FC
48	55	Settable	UART5	UART5 global interrupt	0x0000_0100
49	56	Settable	LPUART	LPUART global interrupt	0x0000_0104
50	57	Settable	TIM5	TIM5 global interrupt	0x0000_0108
51	58	Settable	TIM6	TIM6 global interrupt	0x0000_0118
52	59	Settable	TIM7	TIM7 global interrupt	0x0000_011C
53	60	Settable	CAN_TX	CAN send interrupt	0x0000_0120
54	61	Settable	CAN_RX0	CAN receives 0 interrupt	0x0000_0124
55	62	Settable	CAN_RX1	CAN receive 1 interrupt	0x0000_0128
56	63	Settable	CAN_SCE	CAN SCE interrupt	0x0000_012C
57	64	Settable	LPUART_WKUP	LPUART wake up interrupt connected to EXTI line 23	0x0000_0130
58	65	Settable	LPTIM_WKUP	LPTIM wake up interrupt connected to EXTI line 24	0x0000_0134
59	66	Settable	LCD	LCD global interrupt connected to EXTI line 26	0x0000_0138
60	67	Settable	SAC	SAC global interrupt	0x0000_013C
61	68	Settable	MMU	MMU golbal interrupt	0x0000_0140
62	69	Settable	Reserved	Reserved	0x0000_0144
63	70	Settable	RAMC_PERR	RAM verification error interrupt	0x0000_0148

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Position	Priority	Priority type	Name	Description	Address
64	71	Settable	TIM9	TIM9 global interrupt	0x0000_014C
65	72	Settable	UCDR	UCDR error interrupt	0x0000_0150

6.2 External interrupt/event controller (EXTI)

6.2.1 Introduction

The external interrupt/event controller contains 27 edge detection circuits that generate interrupt/event triggers. Each input line can be independently configured with pulse or pending input types, and 3 trigger event types including rising edge, falling edge or double edge, which can also be independently shielded. Interrupt requests that hold the state line in the pending register can be cleared by writing '1' in the corresponding bit of the pending register.

6.2.2 Main features

The main features of EXTI controller are as follows:

- Support 27 software interrupt/event requests.
- Interrupts/events corresponding to each input line can be configured to trigger or mask independently.
- Each interrupt line has an independent state bit.
- Support for pulse or pending input types.
- 3 trigger events are supported: rising edge, falling edge, and double edge.
- Can wake up to exit low power mode.

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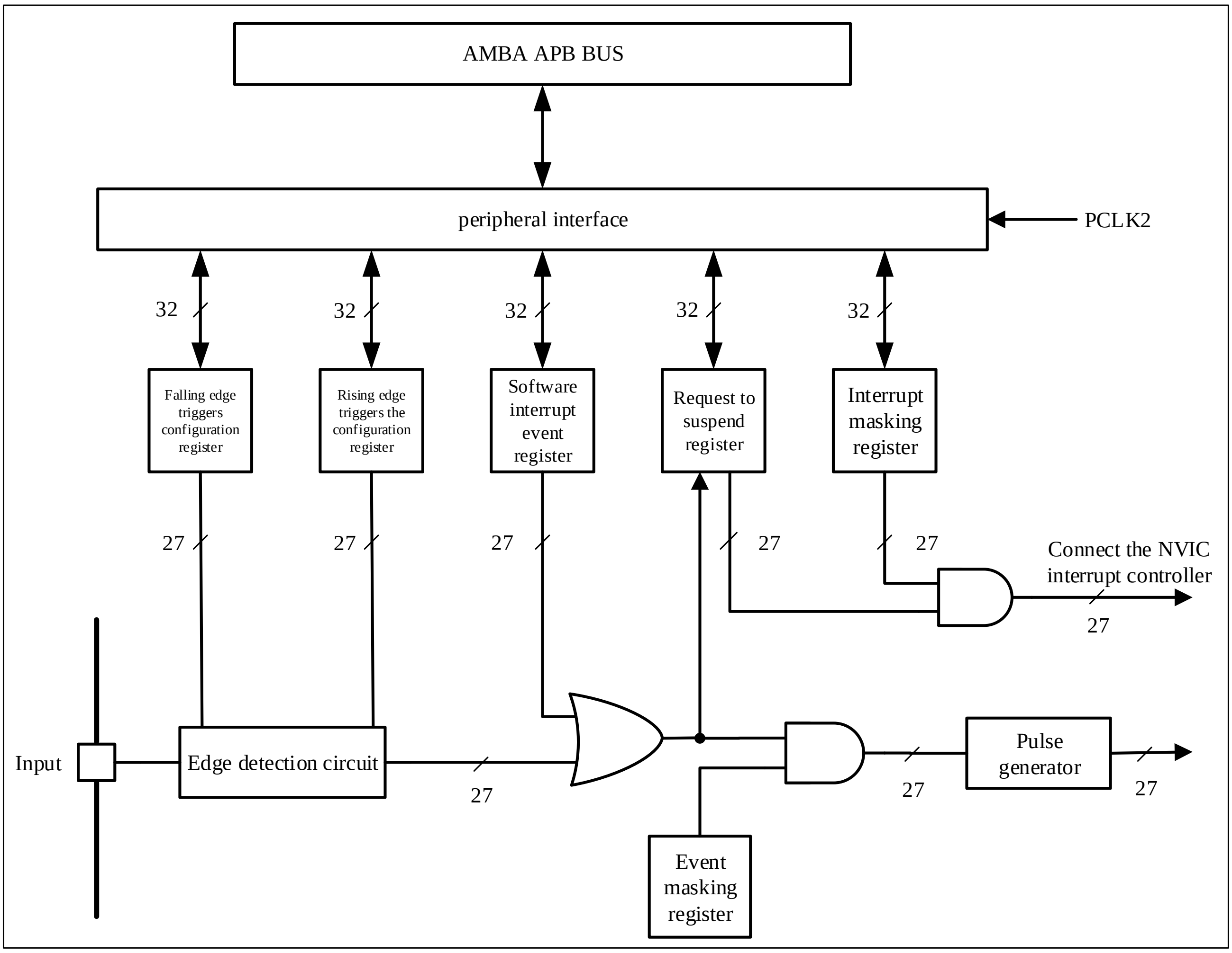
Figure 6-1 External interrupt/event controller block diagram



6.2.3 Functional description

EXTI contains 27 interrupts, 16 from I/O pins and 11 from internal modules. To generate interrupts, the NVIC interrupt channel of the external interrupt controller must be configured to enable the appropriate interrupt line. Select rising edge, falling edge, or double edge trigger event types by edge trigger configuration registers EXTI_RT_CFG and EXTI_FT_CFG, and write '1' to the corresponding bit of interrupt masking register EXTI_IMASK to allow interrupt requests. When a preset edge trigger polarity is detected on the external interrupt line, an interrupt request is generated and the corresponding pending bit is set to '1'. Writing '1' to the corresponding bit of the pending register clears the interrupt request.

To generate events, the corresponding event line must be configured and enabled. According to the desired edge detection polarity, set up the rise/fall edge trigger configuration register, while writing '1' in the corresponding bit of the event masking register to allow interrupt requests. When a preset edge occurs on an event line, an event request pulse is generated and the corresponding pending bit is not set to '1'.

In addition, interrupt/event requests can also be generated by software by writing a '1' in the software interrupt/event register.

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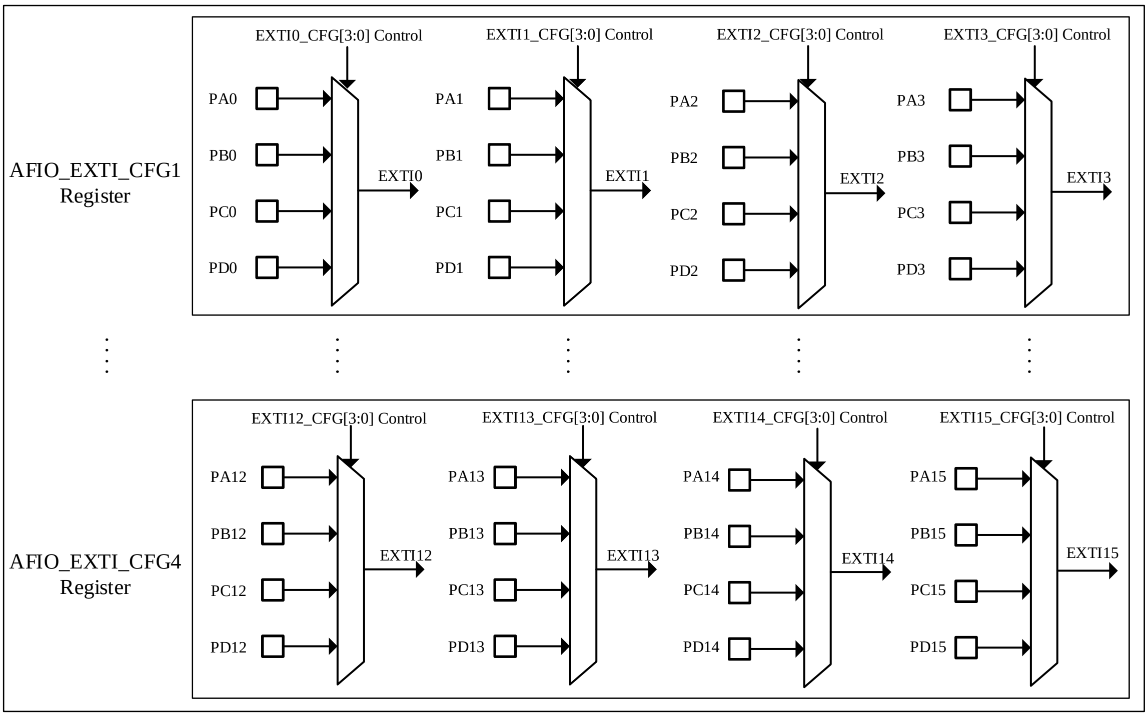
- Hardware interrupt configuration, select and configure 27 lines as interrupt sources as required:
  - Configure the mask bit (EXTI_IMASK) for 27 interrupt lines.
  - Configure the selected disconnection trigger configuration bits (EXTI_RT_CFG and EXTI_FT_CFG);
  - Configure the enable and mask bits of the NVIC interrupt channel corresponding to the external interrupt controller so that the requests in the 27 interrupt lines can be correctly responded to.
- Hardware event configuration: Select 27 lines as event sources as required:
  - Configure the mask bit (EXTI_EMASK) for 27 event lines.
  - Configure the trigger configuration bits for the selected event line (EXTI_RT_CFG and EXTI_FT_CFG).
- Software interrupt/event configuration, select 27 lines as software interrupt/event lines as required:
  - Configure 27 interrupt/event line mask bits (EXTI_IMASK and EXTI_EMASK).
  - Configure the request bit of the software interrupt event register (EXTI_SWIE).

6.2.4 EXTI line maping

Figure 6-2 External interrupt generic I/O mapping



To configure external interrupts/events on the GPIO line using AFIO_EXTI_CFGy, the AFIO clock must be enabled first. Universal I/O ports are connected to 16 external interrupt/event lines as shown above. The connection mode of the other 11 EXTI lines is as follows:

- EXTI line 16 is connected to the PVD output
- EXTI line 17 is connected to the USB wake up event

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- EXTI line 18 is connected to the RTC alarm
- EXTI line 19 is connected to the RTC timestamp event
- EXTI line 20 is connected to the RTC Wake up event
- EXTI line 21 is connected to the COMP1 output
- EXTI line 22 is connected to the COMP2 output
- EXTI line 23 is connected to the LPUART wake up interrupt
- EXTI line 24 is connected to the LPTIM wake up interrupt
- EXTI line 25 is Reserved
- EXTI line 26 is connected to the LCD global interrupt

6.3 EXTI registers

EXTI base address: 0x40010400

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6.3.1 EXTI register overview

Table 6-2 EXTI register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	EXTI_IMASK	Reserved					IMASK26	Reserved	IMASK[24:0]																								
	Reset Value						0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	EXTI_EMASK	Reserved					EMASK26	Reserved	EMASK[24:0]																								
	Reset Value						0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	EXTI_RT_CFG	Reserved					RT_CFG26	Reserved	RT_CFG[24:0]																								
	Reset Value						0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	EXTI_FT_CFG	Reserved					FT_CFG26	Reserved	FT_CFG[24:0]																								
	Reset Value						0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	EXTI_SWIE	Reserved					SWIE26	Reserved	SWIE[24:0]																								
	Reset Value						0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	EXTI_PEND	Reserved					PEND26	Reserved	PEND24	PEND23	PEND22	PEND21	PEND20	PEND19	PEND18	PEND17	PEND16	PEND15	PEND14	PEND13	PEND12	PEND11	PEND10	PEND9	PEND8	PEND7	PEND6	PEND5	PEND4	PEND3	PEND2	PEND1	PEND0
	Reset Value						0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	EXTI_TS_SEL	Reserved																												TSSEL[3:0]			
	Reset Value																													0	0	0	0

6.3.2 EXTI interrupt mask register (EXTI_IMASK)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					IMASK26	Reserved	IMASK24	IMASK23	IMASK22	IMASK21	IMASK20	IMASK19	IMASK18	IMASK17	IMASK16
					rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMASK15	IMASK14	IMASK13	IMASK12	IMASK11	IMASK10	IMASK9	IMASK8	IMASK7	IMASK6	IMASK5	IMASK4	IMASK3	IMASK2	IMASK1	IMASK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained.
26	IMASK26	Interrupt mask on line 26

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Bit Field	Name	Description
		0: Masking the interrupt requests from line 26. 1: Not masking the interrupt requests from line 26.
25	Reserved	Reserved,the reset value must be maintained.
24:0	IMASKx	Interrupt mask on line x(x is 0,1,2,3…23,24) 0: Masking the interrupt requests from line x. 1: Not masking the interrupt requests from line x.

6.3.3 EXTI event mask register (EXTI_EMASK)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					EMASK26	Reserved	EMASK24	EMASK23	EMASK22	EMASK21	EMASK20	EMASK19	EMASK18	EMASK17	EMASK16
					rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMASK15	EMASK14	EMASK13	EMASK12	EMASK11	EMASK10	EMASK9	EMASK8	EMASK7	EMASK6	EMASK5	EMASK4	EMASK3	EMASK2	EMASK1	EMASK0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained.
26	EMASK26	Event mask on line 26 0: Masking the event requests from line 26. 1: Not masking the event requests from line 26.
25	Reserved	Reserved,the reset value must be maintained.
24:0	EMASKx	Event mask on line x(x is 0,1,2,3…23,24) 0: Masking the event requests from line x. 1: Not masking the event requests from line x.

6.3.4 EXTI rising edge trigger configuration register (EXTI_RT_CFG)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					RT_CFG26	Reserved	RT_CFG24	RT_CFG23	RT_CFG22	RT_CFG21	RT_CFG20	RT_CFG19	RT_CFG18	RT_CFG17	RT_CFG16
					rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RT_CFG15	RT_CFG14	RT_CFG13	RT_CFG12	RT_CFG11	RT_CFG10	RT_CFG9	RT_CFG8	RT_CFG7	RT_CFG6	RT_CFG5	RT_CFG4	RT_CFG3	RT_CFG2	RT_CFG1	RT_CFG0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained.
26	RT_CFG26	The rising edge on line 26 triggers the configuration bit 0: Disable rising edge triggering (interrupts and events) on input line 26.

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Bit Field	Name	Description
		1: Enable rising edge triggering (interrupts and events) on input line 26.
25	Reserved	Reserved,the reset value must be maintained.
24:0	RT_CFGx	The rising edge on line x triggers the configuration bit.(x is 0,1,2,3…23,24) 0: Disable rising edge triggering (interrupts and events) on input line x 1: Enable rising edge triggering (interrupts and events) on input line x

6.3.5 EXTI falling edge trigger configuration register (EXTI_FT_CFG)

Address offset: 0x0C

Reset value: 0x0000 0000

31:27	26	25	24	23	22	21	20	19	18	17	16
Reserved	FT_CFG26	Reserved	FT_CFG24	FT_CFG23	FT_CFG22	FT_CFG21	FT_CFG20	FT_CFG19	FT_CFG18	FT_CFG17	FT_CFG16
	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FT_CFG15	FT_CFG14	FT_CFG13	FT_CFG12	FT_CFG11	FT_CFG10	FT_CFG9	FT_CFG8	FT_CFG7	FT_CFG6	FT_CFG5	FT_CFG4	FT_CFG3	FT_CFG2	FT_CFG1	FT_CFG0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained.
26	FT_CFG26	The falling edge on line 26 triggers the configuration bit 0: Disable falling edge triggering (interrupts and events) on input line 26. 1: Enable falling edge triggering (interrupts and events) on input line 26.
25	Reserved	Reserved,the reset value must be maintained.
24:0	FT_CFGx	The falling edge on line x triggers the configuration bit. (x is 0,1,2,3…23,24) 0: Disable falling edge triggering (interrupts and events) on input line x. 1: Enable falling edge triggering (interrupts and events) on input line x.

6.3.6 EXTI software interrupt event register (EXTI_SWIE)

Address offset: 0x10

Reset value: 0x0000 0000

31:27	26	25	24	23	22	21	20	19	18	17	16
Reserved	SWIE26	Reserved	SWIE24	SWIE23	SWIE22	SWIE21	SWIE20	SWIE19	SWIE18	SWIE17	SWIE16
	rc_w1		rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWIE15	SWIE14	SWIE13	SWIE12	SWIE11	SWIE10	SWIE9	SWIE8	SWIE7	SWIE6	SWIE5	SWIE4	SWIE3	SWIE2	SWIE1	SWIE0
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained.
26	SWIE26	Software interrupt on line 26 When the bit is' 0 ', writing '1' sets the corresponding pending bit in EXTI_PEND. If this interrupt is allowed in EXTI_IMASK and EXTI_EMASK, an interrupt will be

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Bit Field	Name	Description
		generated. *Note: This bit can be cleared to '0' by writing '1' to clear the corresponding bit of EXTI_PEND.*
25	Reserved	Reserved,the reset value must be maintained.
24:0	SWIEx	Software interrupt on line x. (x is 0,1,2,3…23,24) When the bit is' 0 ', writing '1' sets the corresponding pending bit in EXTI_PEND. If this interrupt is allowed in EXTI_IMASK and EXTI_EMASK, an interrupt will be generated. *Note: This bit can be cleared to '0' by writing '1' to clear the corresponding bit of EXTI_PEND.*

6.3.7 EXTI pending register (EXTI_PEND)

Address offset: 0x14

Reset value: 0x0000 0000

31				27	26	25	24	23	22	21	20	19	18	17	16
Reserved					PEND26	Reserved	PEND24	PEND23	PEND22	PEND21	PEND20	PEND19	PEND18	PEND17	PEND16
					rc_w1		rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEND15	PEND14	PEND13	PEND12	PEND11	PEND10	PEND9	PEND8	PEND7	PEND6	PEND5	PEND4	PEND3	PEND2	PEND1	PEND0
rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31:27	Reserved	Reserved,the reset value must be maintained.
26	PEND26	Pending bit on line 26 0: No pending request has occurred 1: A pending trigger request occurred This bit is set to '1' when a selected edge trigger event occurs on the external interrupt line. It can be cleared by writing '1' to the bit, or by changing the polarity of the edge detection.
25	Reserved	Reserved,the reset value must be maintained.
24:0	PENDx	Pending bit on line x. (x is 0,1,2,3…23,24) 0: No pending request has occurred 1: A pending trigger request occurred This bit is set to '1' when a selected edge trigger event occurs on the external interrupt line. It can be cleared by writing '1' to the bit, or by changing the polarity of the edge detection.

6.3.8 EXTI timestamp trigger source selection register (EXTI_TS_SEL)

Address offset: 0x18

Reset value: 0x0000 0000

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31–16
Reserved

15–4	3–0
Reserved	TSSEL[3:0]
	rw

Bit Field	Name	Description
31:4	Reserved	Reserved,the reset value must be maintained.
3:0	TSSEL[3:0]	Select the external interrupt input as the trigger source for the timestamp event 0000: Select EXTI0 as the trigger source of the timestamp event; 0001: Select EXTI1 as the trigger source of the timestamp event. ... 1111: Select EXTI15 as the trigger source for the timestamp event.

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7 DMA controller

7.1 Introduction

The DMA controller can access totally 5 AHB slaves: Flash, SRAM, ADC, ABP1 and APB2. DMA Controller is controlled by CPU to perform fast data movement from source to destination. After configuration, data can be transferred without CPU intervention. Thus, CPU can be released for other computation/control tasks or save overall system power consumption.

MCU's main backbone is a multi-layer AHB-Lite bus structure with round-robin arbitration scheme. DMA and CPU core can access different slaves in parallel or same slaves sequentially.

DMA controller has 8 logic channels. Each logic channel is to serve memory access requests from single or multiple peripherals. Internal arbiter controls the priority of different DMA channels.

7.2 Main features

DMA main features:

- 8 DMA channels which can be configured independently.
- Each DMA channel supports hardware requests and software triggers to initiate transfer, and is configured by software.
- Each DMA channel has dedicated software priority level (DMA_CHCFGx.PRIOLVL [1:0] bits, corresponding to 4 levels of priority) which can be configured individually. Channels with the same software priority level will further compare hardware index (channel number) to decide final priority (lower index number channel will has higher priority).
- Configurable source and destination size. Address setting should correspond to data size.
- Configurable circular transfer mode for each channel.
- Each channel has 3 independent event flags and interrupts (Transfer complete, Half transfer, Transfer error), and 1 global interrupt flag (set by logical OR of 3 events).
- Support three transfer types which are Memory-to-Memory, Memory-to-Peripheral and Peripheral-to-Memory.
- Access totally 5 AHB slaves: Flash, SRAM, ADC, APB1 and APB2.
- Configurable data transmit number (0~65535).

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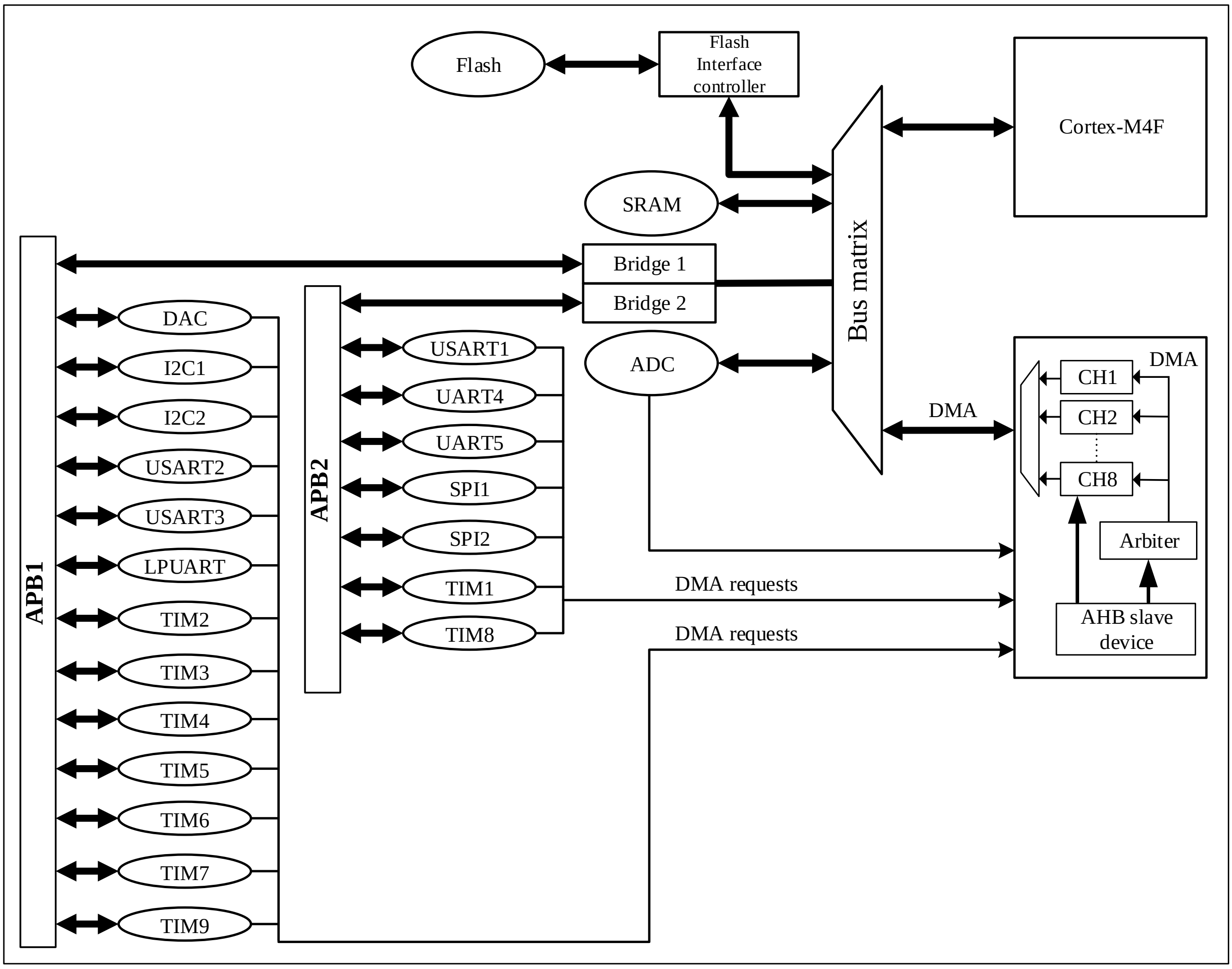
7.3 Block diagram

Figure 7-1 DMA block diagram



7.4 Function description

DMA controller and Cortex™-M4F core share the same system data bus. When CPU and DMA access the same target (RAM or peripheral) at the same time, DMA request will suspend CPU from accessing the system bus for several cycles, and the bus arbiter will perform cyclic scheduling. This allows the CPU to get at least half of the system bus (memory or peripheral) bandwidth.

7.4.1 DMA operation

A DMA request can be triggered by hardware peripherals or software, and the DMA controller processes the request according to the priority level of the channel. The data is read from the source address according to the configured transfer address and bit width, and then the read data is stored in the destination address space. After one operation, the controller calculates the number of remaining transfers and updates the source address and the destination address

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of the next transfer.

Each DMA data transfer consists of three operations:

- Data access: determine the source address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and read data from the source address.
- Data storage: determine the destination address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and store the read data into the destination address space.
- Calculate the number of outstanding operations, perform a decrement operation of the DMA_TXNUMx register, and update the source and destination addresses of the next operation.

7.4.2 Channel priority and arbitration

The DMA uses an arbitration strategy to handle multiple requests from different channels. The priority of each channel is programmable in the channel control register (DMA_CHCFGx).

4 levels of priority:

- Very high priority
- High priority
- Medium priority
- Low priority

By default, channel with lower index has higher priority if the programmed priority is the same.

For memory to memory transfer, re-arbitration is carried on after 4 transfer operations.

For transfer related to periphery, re-arbitration is carried on after each transfer operation.

7.4.3 DMA channels and number of transfers

Each channel can perform DMA transfer between the peripheral register at the specified address and the memory address. The number of data transferred by DMA is programmable, and the maximum supported value is 65535. The DMA_TXNUM register is decremented after each transfer.

7.4.4 Programmable data bit width, alignment and endians

Peripheral and memory transfer data bit width supports byte, half-word and word, which can be programmed through DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE.

When DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE are different, the DMA module aligns the data according to the Table 7-1 below.

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Table 7-1 Programmable data width and endian operation (when PINC = MINC = 1)

Source width (bit)	Destination width (bit)	Number of transfer (bit)	Source: Address / data	Transfer operations (R: Read, W: Write)	Destination: Address / data
8	8	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W B0 [7:0] @0x0 2: R B1 [7:0] @0x1, W B1 [7:0] @0x1 3: R B2 [7:0] @0x2, W B2 [7:0] @0x2 4: R B3 [7:0] @0x3, W B3 [7:0] @0x3	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3
8	16	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W 00B0 [15:0] @0x0 2: R B1 [7:0] @0x1, W 00B1 [15:0] @0x2 3: R B2 [7:0] @0x2, W 00B2 [15:0] @0x4 4: R B3 [7:0] @0x3, W 00B3 [15:0] @0x6	0x0 / 00B0 0x2 / 00B1 0x4 / 00B2 0x6 / 00B3
8	32	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W 000000B0 [31:0] @0x0 2: R B1 [7:0] @0x1, W 000000B1 [31:0] @0x4 3: R B2 [7:0] @0x2, W 000000B2 [31:0] @0x8 4: R B3 [7:0] @0x3, W 000000B3 [31:0] @0xC	0x0 / 000000B0 0x4 / 000000B1 0x8 / 000000B2 0xC / 000000B3
16	8	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W B0 [7:0] @0x0 2: R B3B2 [15:0] @0x2, W B2 [7:0] @0x1 3: R B5B4 [15:0] @0x4, W B4 [7:0] @0x2 4: R B7B6 [15:0] @0x6, W B6 [7:0] @0x3	0x0 / B0 0x1 / B2 0x2 / B4 0x3 / B6
16	16	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W B1B0 [15:0] @0x0 2: R B3B2 [15:0] @0x2, W B3B2 [15:0] @0x2 3: R B5B4 [15:0] @0x4, W B5B4 [15:0] @0x4 4: R B7B6 [15:0] @0x6, W B7B6 [15:0] @0x6	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6
16	32	4	0x0 / B1B0 0x2 / B3B2 0x4 / B5B4 0x6 / B7B6	1: R B1B0 [15:0] @0x0, W 0000B1B0 [31:0] @0x0 2: R B3B2 [15:0] @0x2, W 0000B3B2 [31:0] @0x4 3: R B5B4 [15:0] @0x4, W 0000B5B4 [31:0] @0x8 4: R B7B6 [15:0] @0x6, W 0000B7B6 [31:0] @0xC	0x0 / 0000B1B0 0x4 / 0000B3B2 0x8 / 0000B5B4 0xC / 0000B7B6
32	8	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B0 [7:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B4 [7:0] @0x1 3: R BBBAB9B8 [31:0] @0x8, W B8 [7:0] @0x2 4: R BFBEBDBC [31:0] @0xC, W BC [7:0] @0x3	0x0 / B0 0x1 / B4 0x2 / B8 0x3 / BC
32	16	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B1B0 [15:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B5B4 [15:0] @0x2 3: R BBBAB9B8 [31:0] @0x8, W B9B8 [15:0] @0x4 4: R BFBEBDBC [31:0] @0xC, W BDBC [15:0] @0x6	0x0 / B1B0 0x2 / B5B4 0x4 / B9B8 0x6 / BDBC
32	32	4	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC	1: R B3B2B1B0 [31:0] @0x0, W B3B2B1B0 [31:0] @0x0 2: R B7B6B5B4 [31:0] @0x4, W B7B6B5B4 [31:0] @0x4 3: R BBBAB9B8 [31:0] @0x8, W BBBAB9B8 [31:0] @0x8 4: R BFBEBDBC [31:0] @0xC, W BFBEBDBC [31:0] @0xC	0x0 / B3B2B1B0 0x4 / B7B6B5B4 0x8 / BBBAB9B8 0xC / BFBEBDBC

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DMA always provide full 32-bits data to HWDATA[31:0] no matter what destination size it is (HSIZE still follows destination size setting for device supports byte/half-word operation). The HWDATA[31:0] it provides follow rules as follow:

- When source size is smaller than destination size, DMA pads the MSB with 0 until their sizes match and duplicates it to be 32 bits. E.g., source is 8 bits data 0x55 and destination size is 16 bits. DMA pads the source data with 0 to make it 16 bits and become 0x0055, then duplicate it to 32-bit data 0x0055_0055 and provide to HWDATA[31:0]; (if destination size is 32-bit then DMA will only pad source data with 0).
- When source size is larger or equal to destination size and smaller than 32 bits, DMA duplicates source data to 32 bits data. E.g., source data is 8 bits data 0x1F, HWDATA[31:0] = 0x1F1F_1F1F. If source data is 16 bits data 0x2345, then HWDATA[31:0] = 0x2345_2345.

This guarantees peripherals that only support word operation won't generate bus error and the desired data can still move to the place we want with extra bits i.e. 0 padding. If user wants to configure an 8-bit register but is aligned to a 32-bit address boundary, the source size should be set to 8 bits and destination to 32 bits so extra bits will be padded with 0.

7.4.5 Peripheral/Memory address incrementation

DMA_CHCFGx.PINC and DMA_CHCFGx.MINC respectively control whether the peripheral address and memory address are enabled in auto-increment mode. The software cannot (can read) write the address register during transfer.

- In auto-increment mode, the next address to be transferred is automatically increased according to the data bit width (1, 2 or 4) after each transfer. The address of the first transfer is stored in DMA_PADDRx or DMA_MADDRx register.
- In fixed mode, the address is always fixed to the initial address.

At the end of transfer (i.e. the transfer count changes to 0), different processes will be carried out according to whether the current work is under circular mode or not.

- In acyclic mode, DMA stops after the transfer is completed. To start a new DMA transfer, need to rewrite the transfer number in the DMA_TXNUMx register with the DMA channel disabled.
- In circular mode, at the end of a transfer, the content of the DMA_TXNUMx register will be automatically reloaded to its initial value, and the current internal peripheral or memory address register will also be reloaded to the initial base address set by the DMA_PADDRx or DMA_MADDRx register.

7.4.6 Channel configuration procedure

The detail configuration flow is as below：

1. Configure interrupt mask bits, 1: enable interrupts, 0 disable interrupts.
2. Configure channel peripheral address and memory address and transfer direction.
3. Configure channel priority, 0: lowest, 3: highest.
4. Configure peripheral and memory address increment.

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5. Configure channel transfer block size.
6. If necessary, configure circular mode.
7. If it is memory to memory, configure MEM2MEM mode (Note: to configure DMA to work in M2M mode, user needs to set corresponding channel select value to reserved value, e.g., 63).
8. Repeat step 1~8 on channel 1~8 and finally.
9. Enable corresponding channel.

If software is used to serve interrupt, software must enquire interrupt status register to check which interrupt occurred (software needs to write 1 to interrupt flag clear bit to clear the corresponding interrupt). Before enable channel, all interrupts corresponding to the channel should be cleared.

If the interrupt is transfer complete interrupt, software can configure the next transfer, or report to user this channel transformation is done.

7.4.7 Flow control

Three major flow controls are supported:

- Memory to memory
- Memory to peripheral
- Peripheral to memory

Flow control is controlled by two register bits in each DMA channel configuration register. Flow control is used to control source/destination and direction of DMA channel.

Table 7-2 Flow control table

DMA_CHCFGx.MEM2MEM	DMA_CHCFGx.DIR	Source	Destination	Transfer
1	x	Memory	Memory	AHB read to AHB write, can do back2back transfer
0	1	Memory	AHB Peripheral	AHB read to AHB write, single transfer
			APB Peripheral	AHB read to APB write, single transfer
0	0	AHB Peripheral	Memory	AHB read to AHB write, single transfer
		APB Peripheral		APB read to AHB write, single transfer

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7.4.8 Circular mode

The circular mode is used to process circular buffers and continuous data transmission (such as ADC scan mode). The DMA_CHCFGx.CIRC is used to enable this function. When the cyclic mode is activated, if the number of data to be transferred becomes 0, it will automatically be restored to the initial value when configuring the channel, and the DMA operation will continue.

If the user wants to turn off the circular mode, the user needs to write 0 to DMA_CHCFGx.CHEN to disable the DMA channel, and then write 0 to DMA_CHCFGx.CIRC (when DMA_CHCFGx.CHEN is 1, other bits in the DMA_CHCFGx register cannot be rewritten).

7.4.9 Error management

DMA access to a reserved address area will cause DMA transmission errors. When an error occurs, the transfer error flag is set, and the hardware automatically clears the current DMA channel enable bit (DMA_CHCFGx.CHEN), and the channel operation is stopped. If the transfer error interrupt enable bit is set in the DMA_CHCFGx register, an interrupt will be generated.

7.4.10 Interrupt

- Transfer complete interrupt:

  An interrupt is generated when channel data transfer is complete. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. interrupt status bit is cleared when interrupt flag clear bit is set.

- Half transfer interrupt:

  An interrupt is generated when half of the channel data is transferred. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. interrupt status bit is cleared when interrupt flag clear bit is set.

- Transfer error interrupt:

  An interrupt is generated when bus returned error. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. interrupt status bit is cleared when interrupt flag clear bit is set.

Table 7-3 DMA interrupt request

Interrupt event	Event flag bit	Enable control bit
Half transfer	HTXF	HTXIE
Transfer complete	TXCF	TXCIE
Transfer error	ERRF	ERRIE

7.4.11 DMA request mapping

Totally there are 63 DMA requests from all the peripherals. To have better support with full flexibility, register bits

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can be used to select which DMA request is mapped to which DMA channel. The table blow show the mapping scheme of peripherals' DMA request to DMA controller's DMA channels.

Table 7-4 DMA request mapping

DMA channel select	Peripheral DMA request
Sel = 0	ADC_DMA
Sel = 1	USART1_TX
Sel = 2	USART1_RX
Sel = 3	USART2_TX
Sel = 4	USART2_RX
Sel = 5	USART3_TX
Sel = 6	USART3_RX
Sel = 7	UART4_TX
Sel = 8	UART4_RX
Sel = 9	UART5_TX
Sel = 10	UART5_RX
Sel = 11	LPUART_TX
Sel = 12	LPUART_RX
Sel = 13	SPI1_TX
Sel = 14	SPI1_RX
Sel = 15	SPI2_TX
Sel = 16	SPI2_RX
Sel = 17	I2C1_TX
Sel = 18	I2C1_RX
Sel = 19	I2C2_TX
Sel = 20	I2C2_RX
Sel = 21	DAC
Sel = 22	TIM1_CH1
Sel = 23	TIM1_CH2
Sel = 24	TIM1_CH3
Sel = 25	TIM1_CH4
Sel = 26	TIM1_COM
Sel = 27	TIM1_UP
Sel = 28	TIM1_TRIG
Sel = 29	TIM2_CH1
Sel = 30	TIM2_CH2
Sel = 31	TIM2_CH3
Sel = 32	TIM2_CH4
Sel = 33	TIM2_UP
Sel = 34	TIM3_CH1
Sel = 35	TIM3_CH3

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DMA channel select	Peripheral DMA request
Sel = 36	TIM3_CH4
Sel = 37	TIM3_UP
Sel = 38	TIM3_TRIG
Sel = 39	TIM4_CH1
Sel = 40	TIM4_CH2
Sel = 41	TIM4_CH3
Sel = 42	TIM4_UP
Sel = 43	TIM5_CH1
Sel = 44	TIM5_CH2
Sel = 45	TIM5_CH3
Sel = 46	TIM5_CH4
Sel = 47	TIM5_UP
Sel = 48	TIM5_TRIG
Sel = 49	TIM6
Sel = 50	TIM7
Sel = 51	TIM8_CH1
Sel = 52	TIM8_CH2
Sel = 53	TIM8_CH3
Sel = 54	TIM8_CH4
Sel = 55	TIM8_COM
Sel = 56	TIM8_UP
Sel = 57	TIM8_TRIG
Sel = 58	TIM9_CH1
Sel = 59	TIM9_TRIG
Sel = 60	TIM9_CH3
Sel = 61	TIM9_CH4
Sel = 62	TIM9_UP

7.5 DMA registers

7.5.1 DMA register overview

Table 7-5 DMA register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DMA_INTSTS	ERRF8	HTXF8	TXCF8	GLBF8	ERRF7	HTXF7	TXCF7	GLBF7	ERRF6	HTXF6	TXCF6	GLBF6	ERRF5	HTXF5	TXCF5	GLBF5	ERRF4	HTXF4	TXCF4	GLBF4	ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	DMA_INTCLR	CERRF8	CHTXF8	CTXCF8	CGLBF8	CERRF7	CHTXF7	CTXCF7	CGLBF7	CERRF6	CHTXF6	CTXCF6	CGLBF6	CERRF5	CHTXF5	CTXCF5	CGLBF5	CERRF4	CHTXF4	CTXCF4	CGLBF4	CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	DMA_CHCFG1	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	DMA_TXNUM1	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	DMA_PADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	DMA_MADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	DMA_CHSEL1	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
01Ch	DMA_CHCFG2	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	DMA_TXNUM2	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	DMA_PADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	DMA_MADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	DMA_CHSEL2	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
030h	DMA_CHCFG3	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	DMA_TXNUM3	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	DMA_PADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	DMA_MADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	DMA_CHSEL3	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
044h	DMA_CHCFG4	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	DMA_TXNUM4	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	DMA_PADDR4	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	DMA_MADDR4	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	DMA_CHSEL4	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
058h	DMA_CHCFG5	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05Ch	DMA_TXNUM5	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
060h	DMA_PADDR5	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
064h	DMA_MADDR5	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
068h	DMA_CHSEL5	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
06Ch	DMA_CHCFG6	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
070h	DMA_TXNUM6	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
074h	DMA_PADDR6	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
078h	DMA_MADDR6	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07Ch	DMA_CHSEL6	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
080h	DMA_CHCFG7	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
084h	DMA_TXNUM7	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
088h	DMA_PADDR7	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08Ch	DMA_MADDR7	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
090h	DMA_CHSEL7	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
094h	DMA_CHCFG8	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
098h	DMA_TXNUM8	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
09Ch	DMA_PADDR8	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A0h	DMA_MADDR8	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A4h	DMA_CHSEL8	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0

7.5.2 DMA interrupt status register (DMA_INTSTS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERRF8	HTXF8	TXCF8	GLBF8	ERRF7	HTXF7	TXCF7	GLBF7	ERRF6	HTXF6	TXCF6	GLBF6	ERRF5	HTXF5	TXCF5	GLBF5
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRF4	HTXF4	TXCF4	GLBF4	ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31/27/23/19/15/11/7/3	ERRFx	Transfer error flag for channel x (x=1…8). Hardware sets this bit when transfer error happen. This bit is cleared by software by writing '1' to DMA_INTCLR.CERRFx bit. 0: Transfer error no happened on channel x. 1: Transfer error happened on channel x.
30/26/22/18/14/10/6/2	HTXFx	Half transfer flag for channel x (x=1…8). Hardware sets this bit when half transfer is done. This bit is cleared by software by writing '1' to DMA_INTCLR.CHTXFx bit. 0: Half transfer not yet done on channel x. 1: Half transfer was done on channel x.
29/25/21/17/13/9/5/1	TXCFx	Transfer complete flag for channel x (x=1…8). Hardware sets this bit when transfer is done. This bit is cleared by software by writing '1' to DMA_INTCLR.CTXCFx bit. 0: Transfer not yet done on channel x. 1: Transfer was done on channel x.
28/24/20/16/12/8/4/0	GLBFx	Global flag for channel x (x=1…8). Hardware sets this bit when any interrupt events happen in this channel. This bit is

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Bit field	Name	Description
		cleared by software by writing '1' to DMA_INTCLR.CGLBFx bit. 0: No transfer error, half transfer or transfer done event happen on channel x. 1: One of transfer error, half transfer or transfer done event happen on channel x.

7.5.3 DMA interrupt flag clear register (DMA_INTCLR)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CERRF8	CHTXF8	CTXCF8	CGLBF8	CERRF7	CHTXF7	CTXCF7	CGLBF7	CERRF6	CHTXF6	CTXCF6	CGLBF6	CERRF5	CHTXF5	CTXCF5	CGLBF5
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CERRF4	CHTXF4	CTXCF4	CGLBF4	CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bit field	Name	Description
31/27/23/19/15/11/7/3	CERRFx	Clear transfer error flag for channel x (x=1…8). Software can set this bit to clear ERRF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.ERRF bit of corresponding channel.
30/26/22/18/14/10/6/2	CHTXFx	Clear half transfer flag for channel x (x=1…8). Software can set this bit to clear HTXF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.HTXF bit of corresponding channel.
29/25/21/17/13/9/5/1	CTXCFx	Clear transfer complete flag for channel x (x=1…8). Software can set this bit to clear TXCF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.TXCF bit of corresponding channel.
28/24/20/16/12/8/4/0	CGLBFx	Clear global event flag for channel x (x=1…8). Software can set this bit to clear GLBF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.GLBF bit of corresponding channel.

7.5.4 DMA channel x configuration register (DMA_CHCFGx)

Note：The x is channel number, x = 1…8

Address offset: 0x08+20 * (x–1)

Reset value: 0x0000 0000

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31															16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	rw	rw		rw		rw		rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	MEM2MEM	Memory to memory mode. Software can configure this channel to memory to memory transfer when it is not yet enabled. 0: Channel transfer between memory and peripheral. 1: Channel set to memory to memory transfer.
13:12	PRIOLVL[1:0]	Channel priority. Software can program channel priority when channel is not enable. 00: Low 01: Medium 10: High 11: Very high
11:10	MSIZE[1:0]	Memory data size. Software can configure data size read/write from/to memory address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
9:8	PSIZE[1:0]	Peripheral data size. Software can configure data size read/write from/to peripheral address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
7	MINC	Memory increment mode. Software can enable/disable memory address increment mode. 0: Memory address won't increase with each transfer. 1: Memory address increase with each transfer.
6	PINC	Peripheral increment mode. Software can enable/disable peripheral address increment mode. 0: Peripheral address won't increase with each transfer. 1: Peripheral address increase with each transfer.
5	CIRC	Circular mode. Software can set/clear this bit. 0: Channel will stop after one round of transfer.

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Bit field	Name	Description
		1: Channel configure as circular mode.
4	DIR	Data transfer direction Software can set/clear this bit. 0: Data transfer from Peripheral to Memory 1: Data transfer from Memory to Peripheral.
3	ERRIE	Transfer error interrupt enable. Software can enable/disable transfer error interrupt. 0: Disable transfer error interrupt of channel x. 1: Enable transfer error interrupt of channel x.
2	HTXIE	Half transfer interrupt enable. Software can enable/disable half transfer interrupt. 0: Disable half transfer interrupt of channel x. 1: Enable half transfer interrupt of channel x.
1	TXCIE	Transfer complete interrupt enable. Software can enable/disable transfer complete interrupt. 0: Disable transfer complete interrupt of channel x. 1: Enable transfer complete interrupt of channel x.
0	CHEN	Channel enable. Software can set/reset this bit. 0: Disable channel. 1: Enable channel.

7.5.5 DMA channel x transfer number register (DMA_TXNUMx)

Note：The x is channel number, x = 1…8

Address offset: 0x0c+20 * (x–1)

Reset value: 0x0000 0000

31 … 16
Reserved

15 … 0
NDTX[15:0]
rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	NDTX	Number of data to transfer. Number of data to be transferred (0～65535). Software can read/write the number of transfers when channel is disable and it will be read only after channel enable. Every successful transfer of corresponding DMA channel will decrease this register by 1. If circular mode is enable, it will automatically reload pre-set value when it reach zero.

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Bit field	Name	Description
		Otherwise it will keep at zero and reset channel enable.

7.5.6 DMA channel x peripheral address register (DMA_PADDRx)

Note：The x is channel number, x = 1…8

Address offset: 0x10+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

31 … 16
ADDR[31:0]
rw

15 … 0
ADDR[31:0]
rw

Bit field	Name	Description
31:0	ADDR	Peripheral address. Peripheral starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.PSIZE. With DMA_CHCFGx.PSIZE equal to 01, DMA ignores bit 0 of PADDR and if DMA_CHCFGx.PSIZE equal to 10 DMA will ignore bit [1:0] of PADDR.

7.5.7 DMA channel x memory address register (DMA_MADDRx)

Note：The x is channel number, x = 1…8

Address offset: 0x14+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

31 … 16
ADDR[31:0]
rw

15 … 0
ADDR[31:0]
rw

Bit field	Name	Description
31:0	ADDR	ADDR Memory address. Memory starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.MSIZE. With DMA_CHCFGx.MSIZE equal to 01, DMA ignores bit 0 of MADDR and if

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Bit field	Name	Description
		DMA_CHCFGx.MSIZE equal to 10 DMA will ignore bit [1:0] of MADDR.

7.5.8 DMA channel x channel request select register (DMA_CHSELx)

Note：The x is channel number, x = 1…8

Address offset: 0x18+20 * (x–1)

Reset value: 0x0000 0000

31–16
Reserved

15–6	5–0
Reserved	CH_SEL[5:0]
	rw

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	CH_SEL[5:0]	DMA channel request selection 0x00：ADC_DMA 0x01：USART1_TX 0x02：USART1_RX 0x03：USART2_TX 0x04：USART2_RX 0x05：USART3_TX 0x06：USART3_RX 0x07：UART4_TX 0x08：UART4_RX 0x09：UART5_TX 0x0A：UART5_RX 0x0B：LPUART_TX 0x0C：LPUART_RX 0x0D：SPI1_TX 0x0E：SPI1_RX 0x0F：SPI2_TX 0x10：SPI2_RX 0x11：I2C1_TX 0x12：I2C1_RX 0x13：I2C2_TX 0x14：I2C2_RX 0x15：DAC 0x16：TIM1_CH1 0x17：TIM1_CH2

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Bit field	Name	Description
		0x18：TIM1_CH3 0x19：TIM1_CH4 0x1A：TIM1_COM 0x1B：TIM1_UP 0x1C：TIM1_TRIG 0x1D：TIM2_CH1 0x1E：TIM2_CH2 0x1F：TIM2_CH3 0x20：TIM2_CH4 0x21：TIM2_UP 0x22：TIM3_CH1 0x23：TIM3_CH3 0x24：TIM3_CH4 0x25：TIM3_UP 0x26：TIM3_TRIG 0x27：TIM4_CH1 0x28：TIM4_CH2 0x29：TIM4_CH3 0x2A：TIM4_UP 0x2B：TIM5_CH1 0x2C：TIM5_CH2 0x2D：TIM5_CH3 0x2E：TIM5_CH4 0x2F：TIM5_UP 0x30：TIM5_TRIG 0x31：TIM6 0x32：TIM7 0x33：TIM8_CH1 0x34：TIM8_CH2 0x35：TIM8_CH3 0x36：TIM8_CH4 0x37：TIM8_COM 0x38：TIM8_UP 0x39：TIM8_TRIG 0x3A：TIM9_CH1 0x3B：TIM9_TRIG 0x3C：TIM9_CH3 0x3D：TIM9_CH4 0x3E：TIM9_UP

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8 CRC calculation unit

8.1 CRC introduction

This module integrates the functions of CRC32 and CRC16, and the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. EN/IEC 60335-1 provides a method to verify the integrity of flash memory. CRC calculation unit can calculate the identifier of the software when the program is running, then compare it with the reference identifier generated during connection, and then store it in the specified memory space.

8.2 CRC main features

8.2.1 CRC32 module

- CRC32($X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$)
- 32 bits of data to be checked and 32 bits of output check code.
- CRC calculation time: 1 AHB clock cycles (HCLK)
- General-purpose 8-bit register (can be used to store temporary data)

8.2.2 CRC16 module

- CRC16($X^{16}+X^{15}+X^{2}+1$)
- There are 8 bits of data to be checked and 16 bits of output check code.
- CRC calculation time: 1 AHB clock cycle (HCLK)
- The verification initial value can be configured, and the size end of the data to be verified can be configured.
- Support 8bit LRC check value generation

The following figure is the block diagram of CRC unit.

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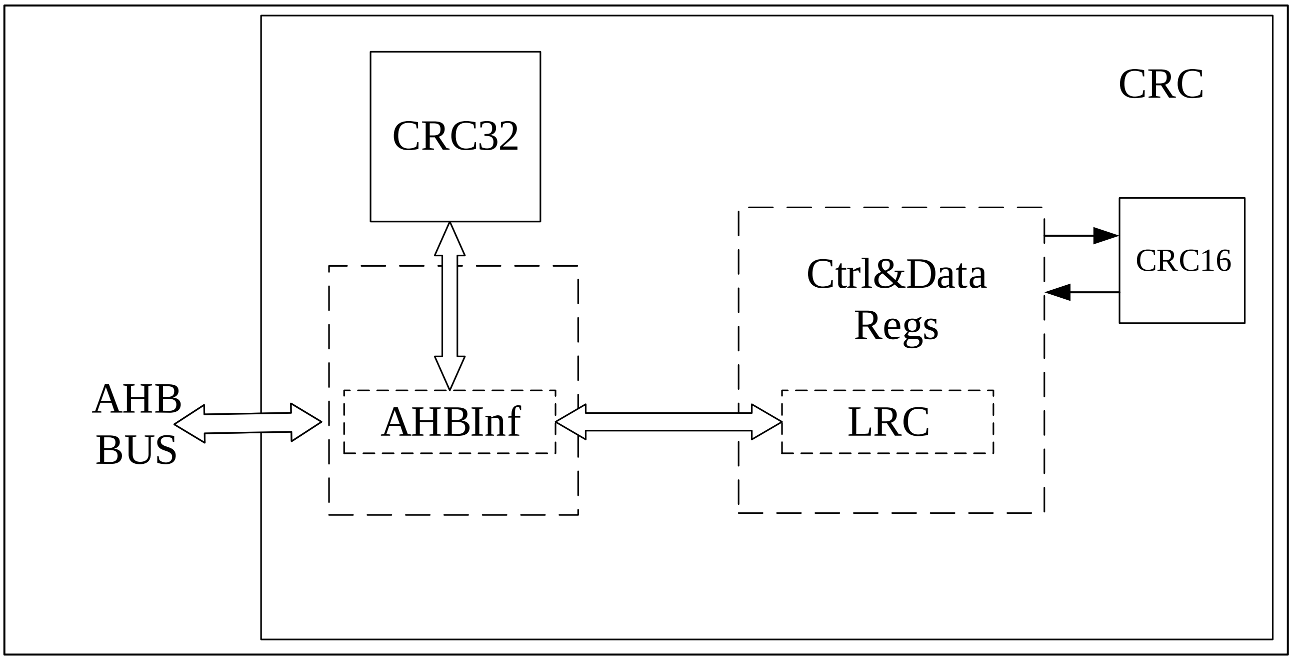
Figure 8-1 CRC calculation unit block diagram



8.3 CRC function description

8.3.1 CRC32

CRC unit contains one 32-bit data register:

- Writing this register to input CRC data.
- Reading this register to get the calculated CRC result.

Every writing operation of this data register triggers the calculation of this new data with the previous calculation result (CRC calculation is performed on the whole 32-bit word rather than byte by byte).

Support back-to-back writes or sequential write-read operations.

CRC_CRC32DAT can be re-initialized to 0xFFFFFFFF by setting CRC_CRC32CTRL.RESET. This operation does not affect the data in register CRC_CRC32IDAT.

8.3.2 CRC16

CRC_CRC16CTRL.ENDHL controls little endian or big endian.

To clear the result of the last CRC operation, set CRC_CRC16CTRL.CLR to 1 or CRC_CRC16D to 0.

The initial value of CRC calculation can be configured by writing the CRC_CRC16D register. By default, the initial value is the result of the last calculation.

LRC calculation is the same as CRC calculation. Both are carried out at the same time. CRC or LRC can be read out depending on needs. If the initial value needs to be set, the LRC register should be configured first.

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8.4 CRC registers

8.4.1 CRC register overview

The following table lists the registers and reset values of CRC.

Table 8-1 CRC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	CRC32DAT	CRC32DAT[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
004h	CRC32IDAT	Reserved																								CRC32IDAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
008h	CRC32CTRL	Reserved																															RESET
	Reset Value																																0
00Ch	CRC16CTRL	Reserved																													CLR	ENDHL	Reserved
	Reset Value																														0	0	
010h	CRC16DAT	Reserved																								CRC16DAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	CRC16D	Reserved																CRC16D[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LRC	Reserved																								LRCDAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0

8.4.2 CRC32 data register (CRC_CRC32DAT)

Address offset: 0x00

Reset value: 0xFFFF FFFF

31 … 16
CRC32DAT[31:0]
rw

15 … 0
CRC32DAT[31:0]
rw

Bit field	Name	Description
31:0	CRC32DAT[31:0]	CRC32 Data register. The written data is the CRC value to be checked. The read data is the CRC calculation result. Only 32-bit operations are supported.

8.4.3 CRC32 independent data register (CRC_CRC32IDAT)

Address offset: 0x04

Reset value: 0x0000 0000

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31–16
Reserved

15–8	7–0
Reserved	CRC32IDAT[7:0]
	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CRC32IDAT[7:0]	Independent 8-bit data register. General 8 bits data register. It is for temporary stored 1-byte data. CRC_ CRC32CTRL.RESET reset signal will not impact this register.

Note: This register is not a part of CRC calculation and can be used to store any data.

8.4.4 CRC32 control register (CRC_CRC32CTRL)

Address offset: 0x08

Reset value: 0x0000 0000

31–16
Reserved

15–1	0
Reserved	RESET
	w

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	RESET	RESET signal. It can reset CRC32 module and set data register to be 0xFFFF_FFFF. This reset can only write 1, and hardware will clear to 0 automatically.

8.4.5 CRC16 control register (CRC_CRC16CTRL)

Address offset: 0x0C

Reset value: 0x0000 0000

31–16
Reserved

15–3	2	1	0
Reserved	CLR	ENDHL	Reserved
	w	rw	

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Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2	CLR	Clear CRC16 results. 0: Not clear. 1: Clear to default value 0x0000. Set this bit to 1 will only maintain 1 clock cycle, hardware will clear automatically. (Software read always 0).
1	ENDHL	Data to be verified start to calculate from MSB or LSB(configured endian). 0: From MSB to LSB 1: From LSB to MSB This bit is only for data to be verified.
0	Reserved	Reserved, the reset value must be maintained.

Note: 8-bits, 16-bits and 32-bits operations are supported.

8.4.6 CRC16 input data register (CRC_CRC16DAT)

Address offset: 0x10

Reset value: 0x0000 0000

31–16
Reserved

15–8	7–0
Reserved	CRC16DAT[7:0]
	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CRC16DAT[7:0]	Data to be verified.

Note: 8-bits, 16-bits and 32-bits operations are supported.

8.4.7 CRC cyclic redundancy check code register (CRC_CRC16D)

Address offset: 0x14

Reset value: 0x0000 0000

31–16
Reserved

15–0
CRC16D[15:0]
rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.

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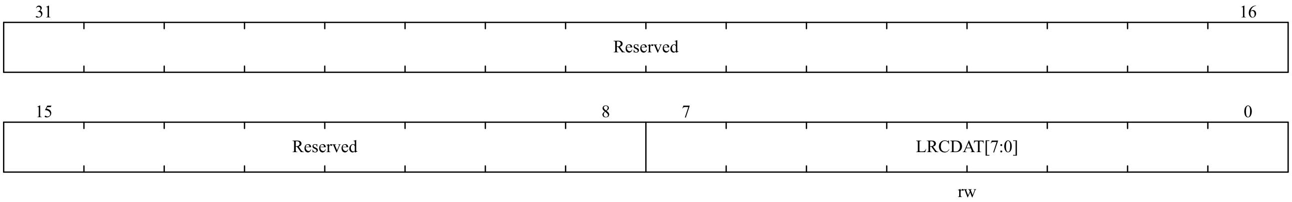
Bit field	Name	Description
15:0	CRC16D[15:0]	16-bit value of cyclic redundancy result data. Every time the software writes the CRC16DAT register, the 16-bit calculated data from CRC16 is updated in this register.

Note: 8-bits, 16-bits and 32-bits operations are supported (8-bit operations must be performed twice in a row to ensure that 16-bit initial values are configured properly)

8.4.8 LRC result register (CRC_LRC)

Address offset: 0x18

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	LRCDAT[7:0]	LRC check value register. Software need to write initial value before use. And then each writing data to CRC_CRC16DAT will be XOR with CRC_LCR register value. The result will be stored in CRC_LRC. Software read the result. It should be cleared before next use.

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9 Cryptographic algorithm hardware acceleration engine (SAC)

Embedded algorithm hardware acceleration engine supports a variety of international algorithms and national cryptographic symmetric algorithms and hash cryptographic algorithm acceleration, which can greatly improve the encryption and decryption speed compared with pure software algorithms.

Algorithms supported by hardware are as follows:

- Support DES symmetric algorithm
  - Support DES and 3DES encryption and decryption operations
  - TDES supports 2KEY and 3KEY modes
  - Support CBC and ECB mode
- Support AES symmetric algorithm
  - Support 128bit/192bit/ 256bit key length
  - Support CBC, ECB, CTR mode
- Support SHA hash algorithm
  - Support SHA1/SHA224/SHA256
- Support MD5 digest algorithm
- Support symmetric national cryptographic SM1, SM4, SM7 algorithm and SM3 hash algorithm

Note: For the performance and use of the cryptographic algorithm, please contact Nations Technologies sales staff

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10 Advanced-control timers (TIM1 and TIM8)

10.1 TIM1 and TIM8 introduction

The advanced control timers (TIM1 and TIM8) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

10.2 Main features of TIM1 and TIM8

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 6 channels, TIM8 up to 6 channels.
- 4 capture/compare channels, the working modes are PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with adjustable dead-time.
  - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timer can be controlled by external signal
- Timers are linked internally for timer synchronization or chaining
- TIM1_CC5 and TIM8_CC5 for COMP blanking.
- TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 can switch the input channel of OPAMP2
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

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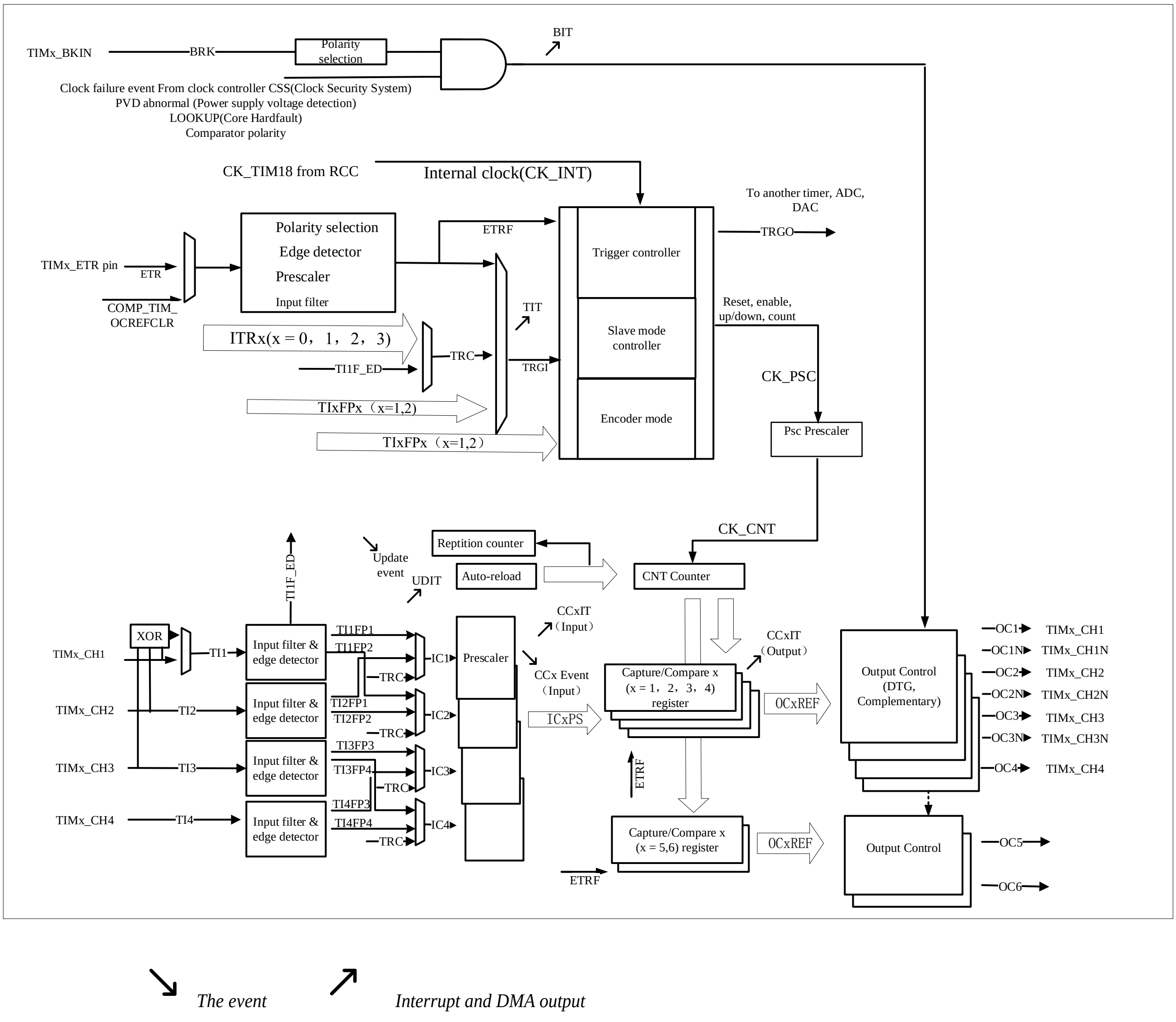
Figure 10-1 Block diagram of TIM1 and TIM8



The capture channel 1 input can come from IOM or comparator output

10.3 TIM1 and TIM8 function description

10.3.1 Time-base unit

The advanced-control's time-base unit mainly includes: prescaler, counter, auto-reload and repetition counter. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter

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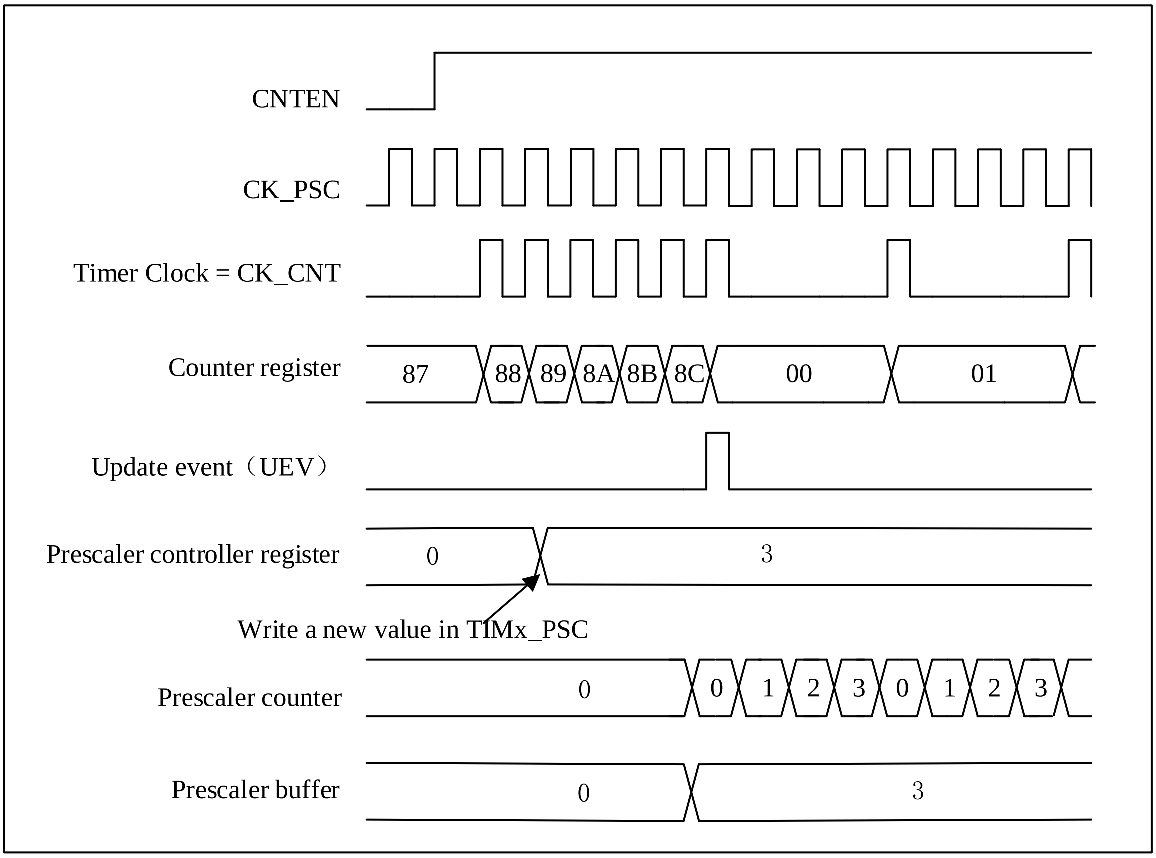
starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

10.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 10-2 Counter timing diagram with prescaler division change from 1 to 4



10.3.2 Counter mode

10.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate. And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS, When an update event occurs, the TIMx_STS.UDITF is set, all registers are updated:

- The repetition counter reloads the contents of the TIMx_REPCNT

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- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 10-3 Timing diagram of up-counting. The internal clock divider factor = 2/N

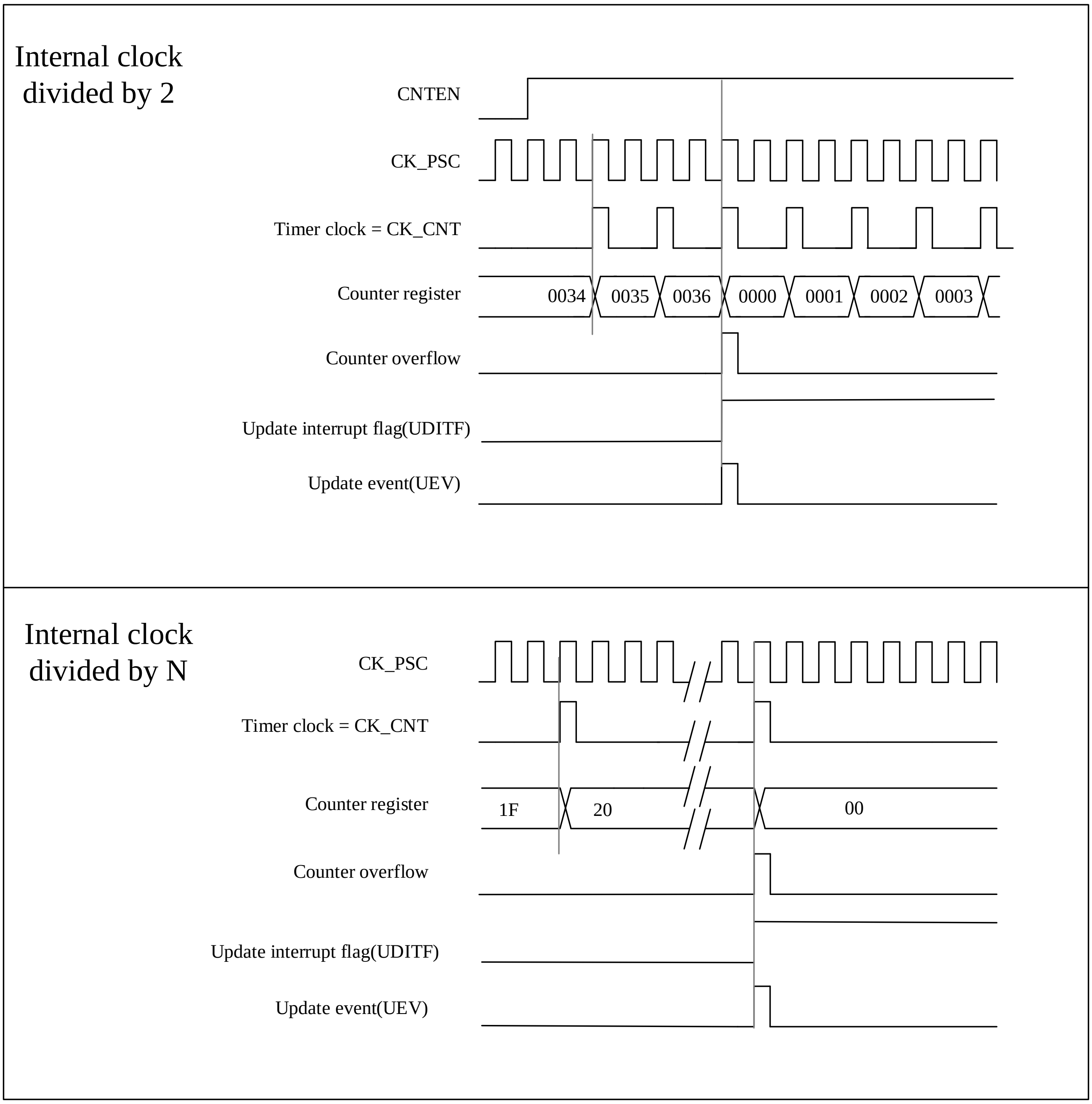

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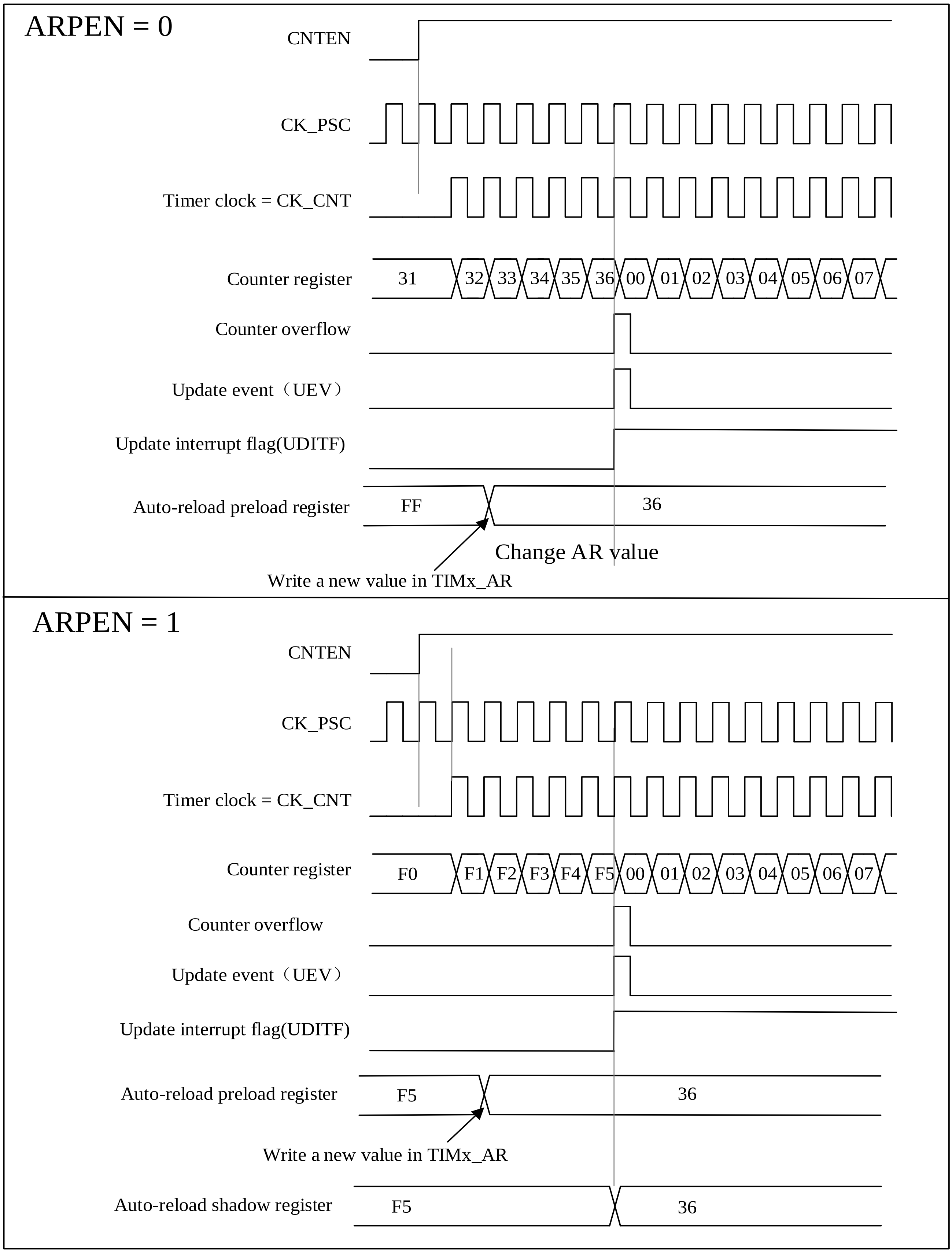
Figure 10-4 Timing diagram of the up-counting, update event when ARPEN=0/1



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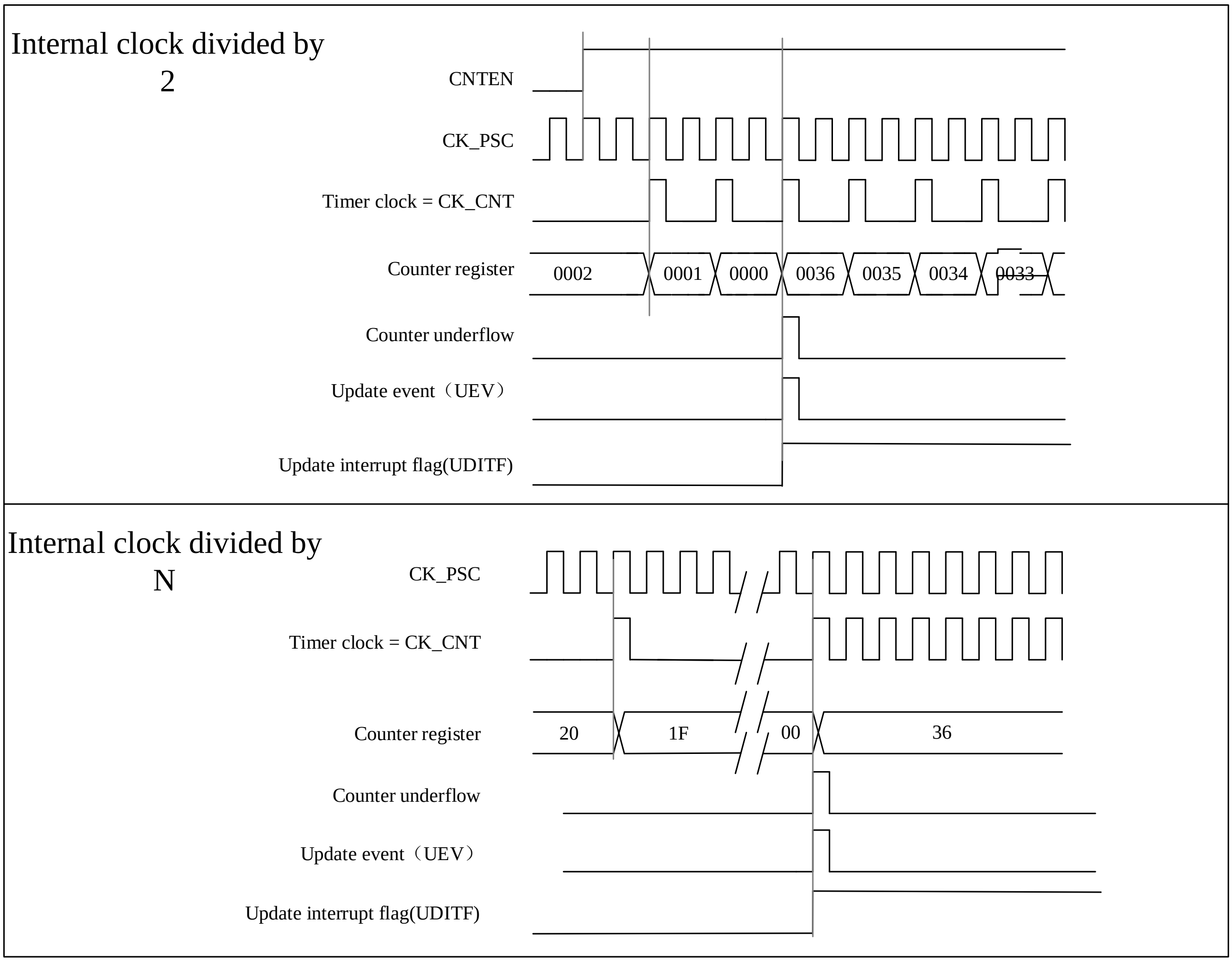
10.3.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see 10.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 10-5 Timing diagram of the down-counting, internal clock divided factor = 2/N



10.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

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The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Please note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 10-6 Timing diagram of the Center-aligned, internal clock divided factor =2/N

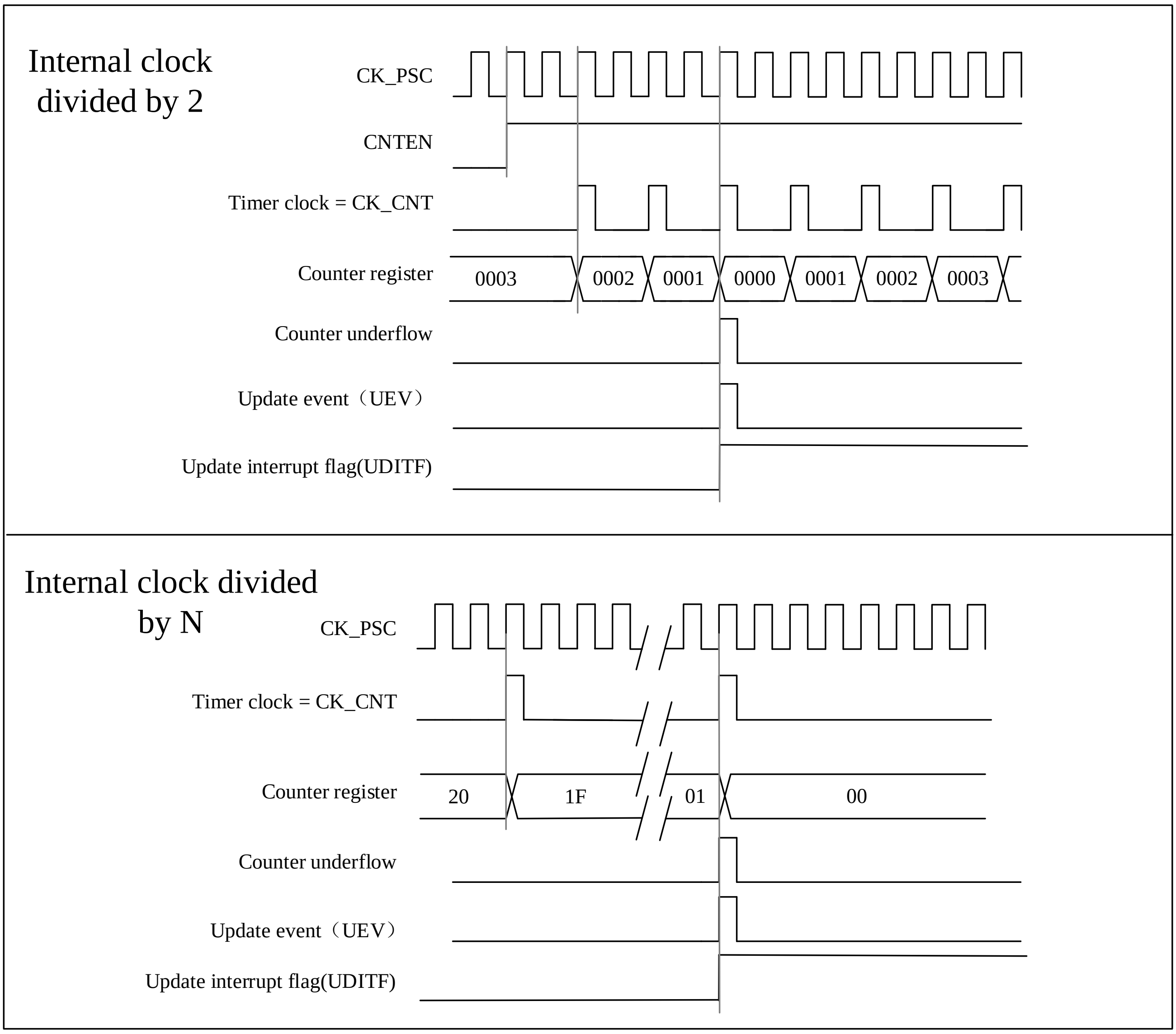

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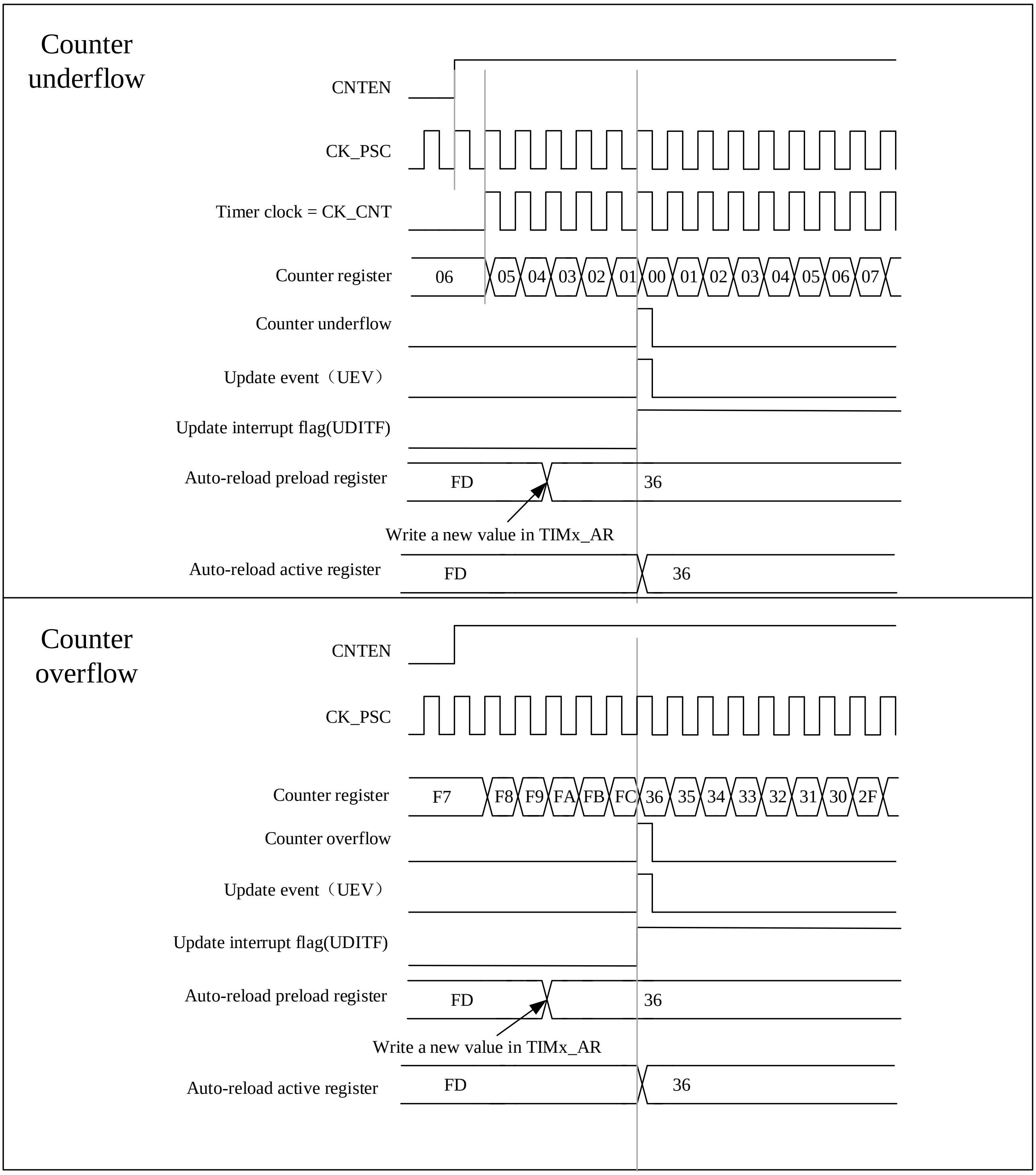
Figure 10-7 A center-aligned sequence diagram that includes counter overflows and underflows (ARPEN = 1)



10.3.3 Repetition counter

The basic unit of Section 10.3.1 describes the conditions for generating an update event (UEV). An update event (UEV) is actually only generated when the repeat counter reaches zero, which is valuable for generating PWM signals.

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This means that data is transferred from the preload registers to the shadow registers every N+1 counter overflow or underflow, where N is the value in the TIMx_REPCNT.

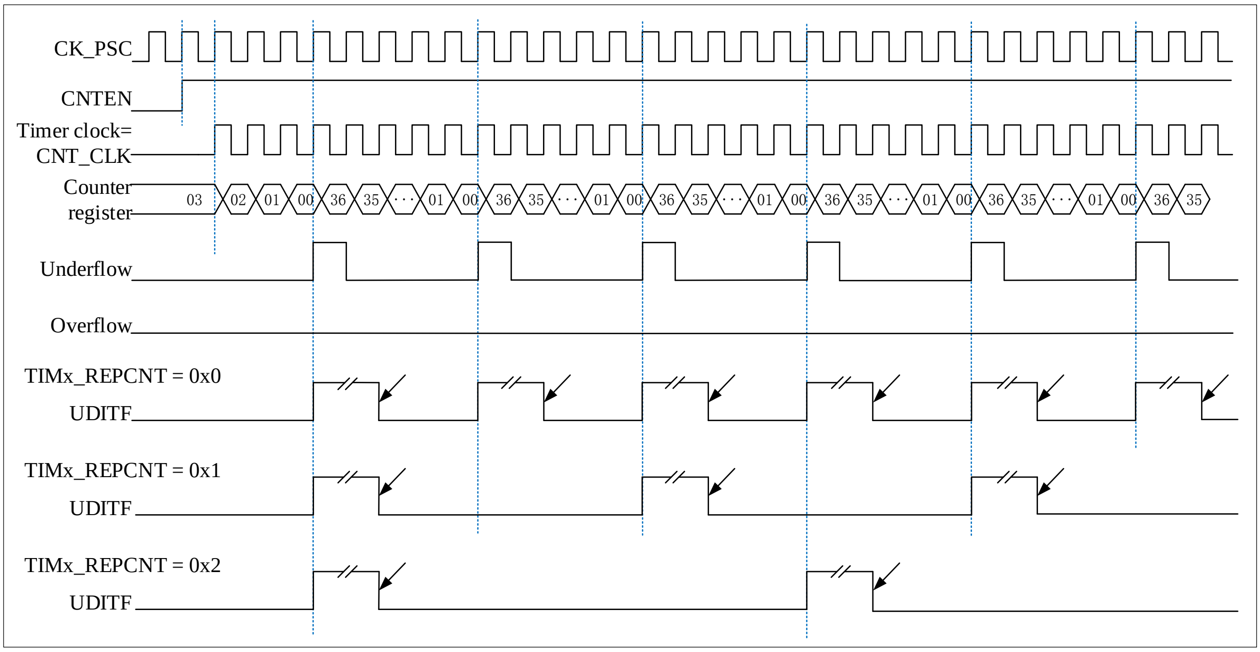
The repetition counter is decremented:

- In the up-counting mode, each time the counter reaches the maximum value, an overflow occurs.
- In down-counting mode, each time the counter decrements to the minimum value, an underflow occurs.
- In center-aligned mode, each time the counter overflows or underflows.

Its repetition rate is defined by the value of the TIMx_REPCNT register.

Repetition counters feature automatic reloading. The update event (generated by setting TIMx_EVTGEN.UDGN or hardware through slave mode controller) occurs immediately, regardless of the value of the repeat counter.

Figure 10-8 Repeat count sequence diagram in down-counting mode



Software clear

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Figure 10-9 Repeat count sequence diagram in up-counting mode

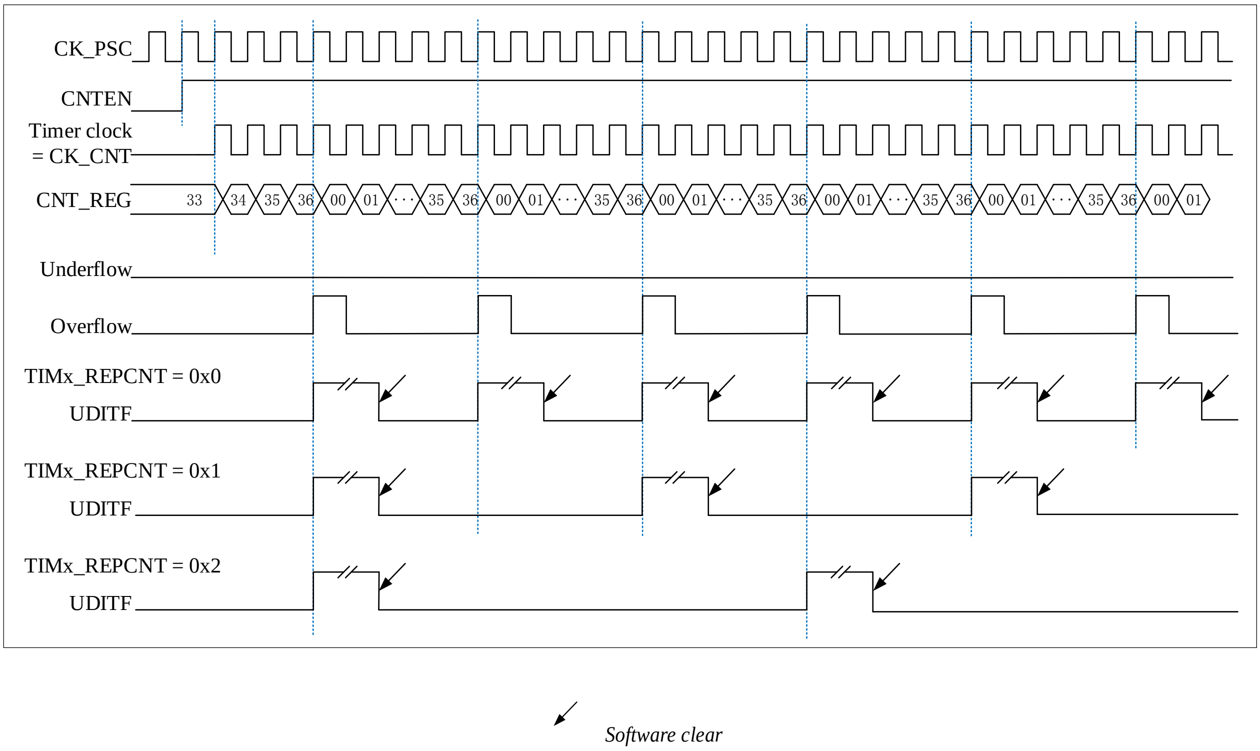
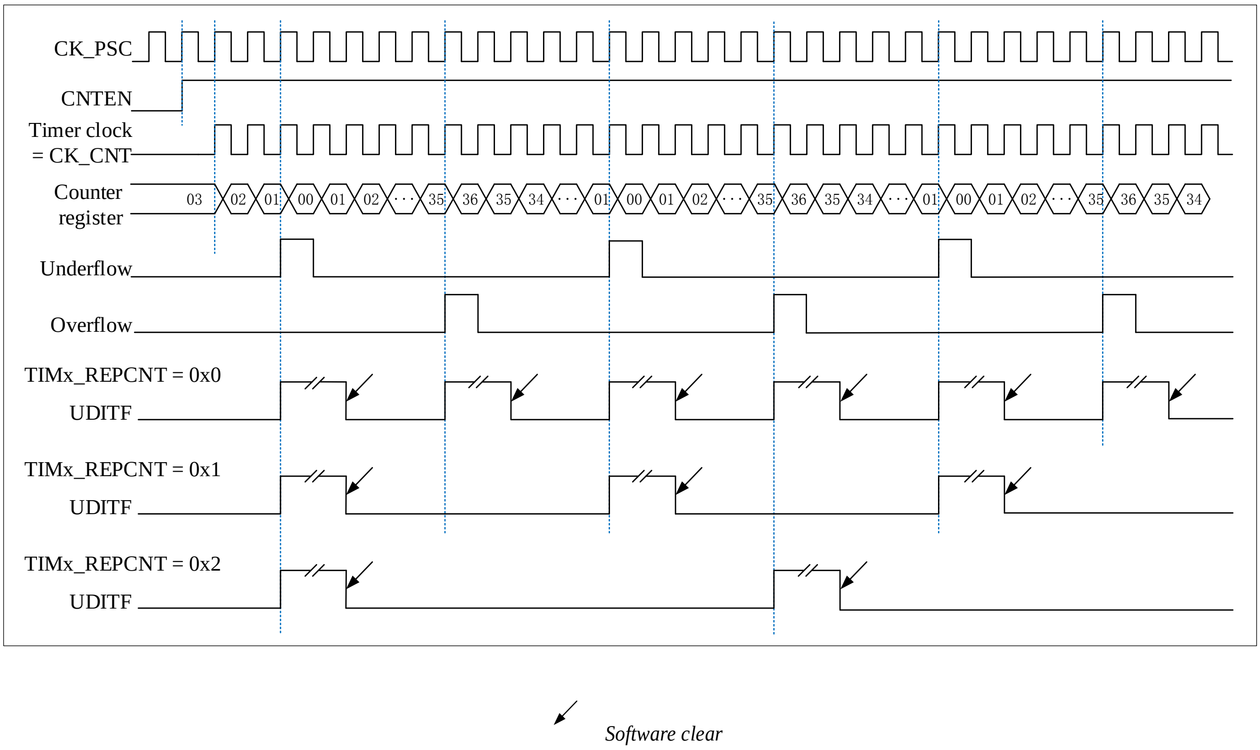


Figure 10-10 Repeat count sequence diagram in center-aligned mode



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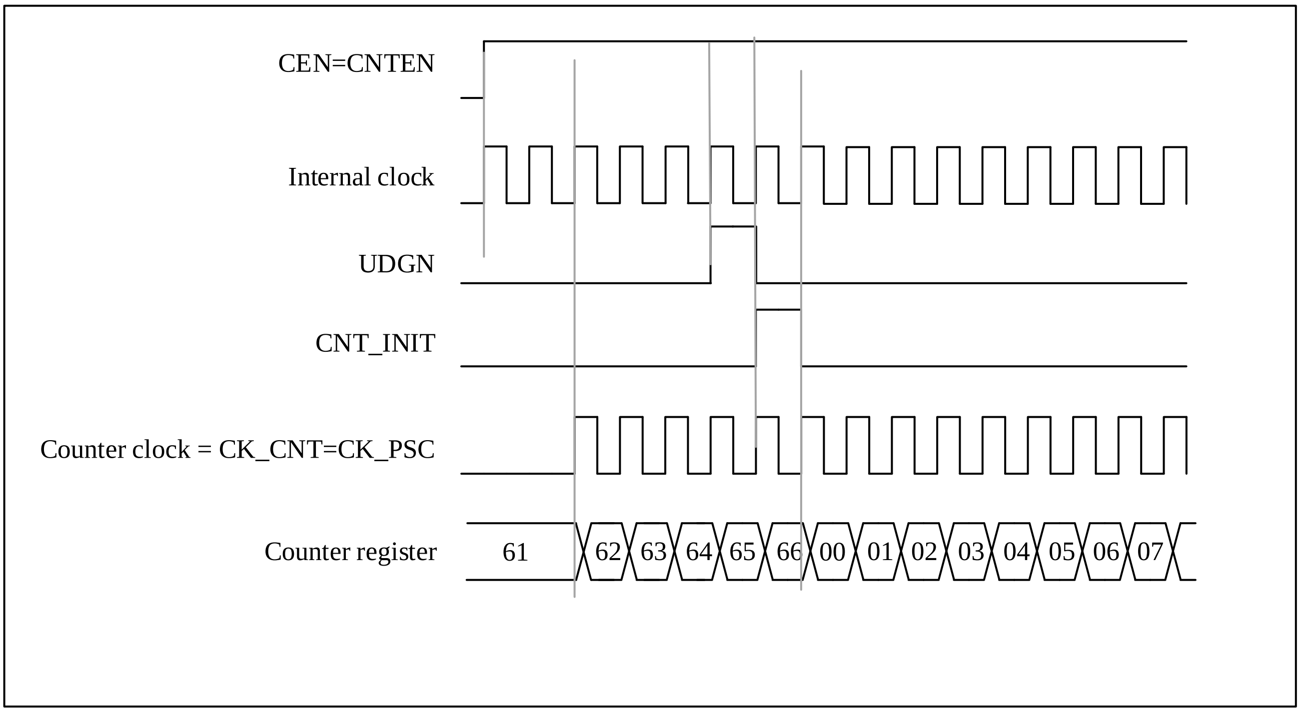
10.3.4 Clock selection

- The internal clock of Advanced-control timers: CK_INT
- Two kinds of external clock mode :
  - external input pin
  - external trigger input ETR
- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

10.3.4.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1.DIR、TIMx_EVTGEN.UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by soft, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 10-11 Control circuit in normal mode, internal clock divided by 1



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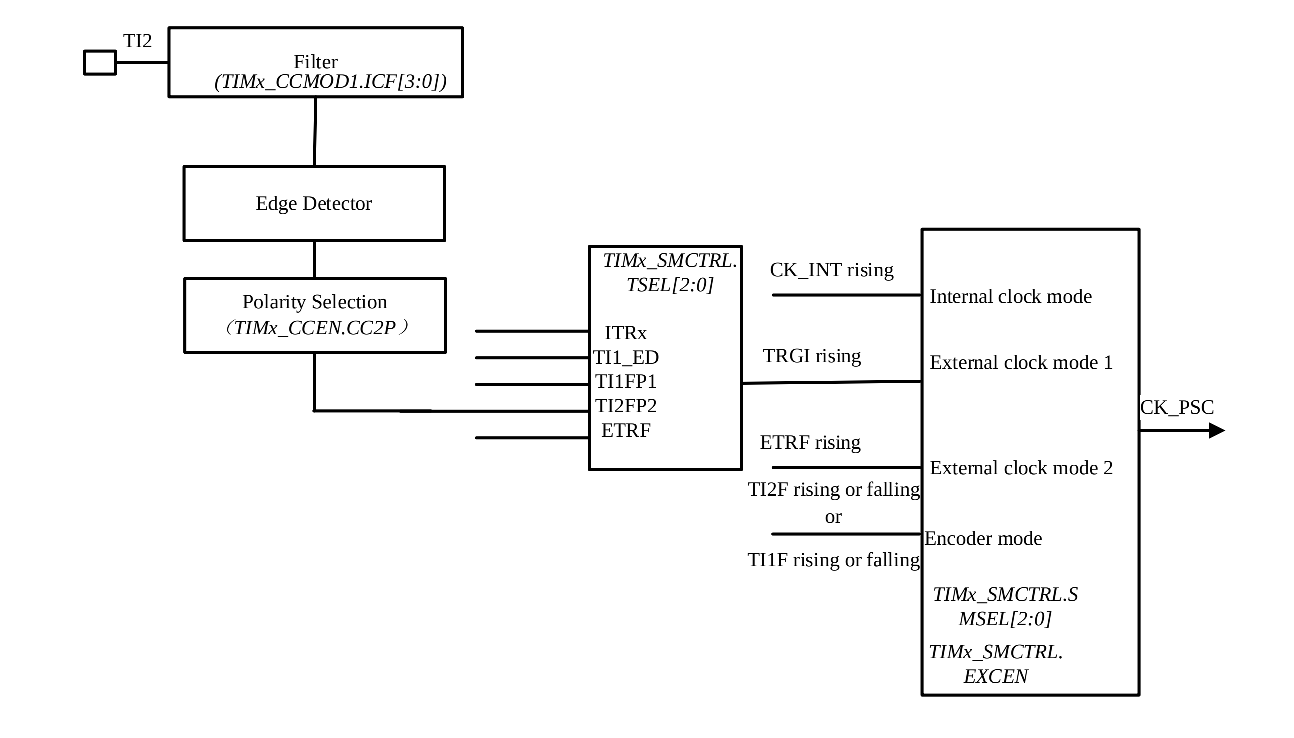
10.3.4.2 External clock source mode 1

Figure 10-12 TI2 external clock connection example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the TI2 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note: The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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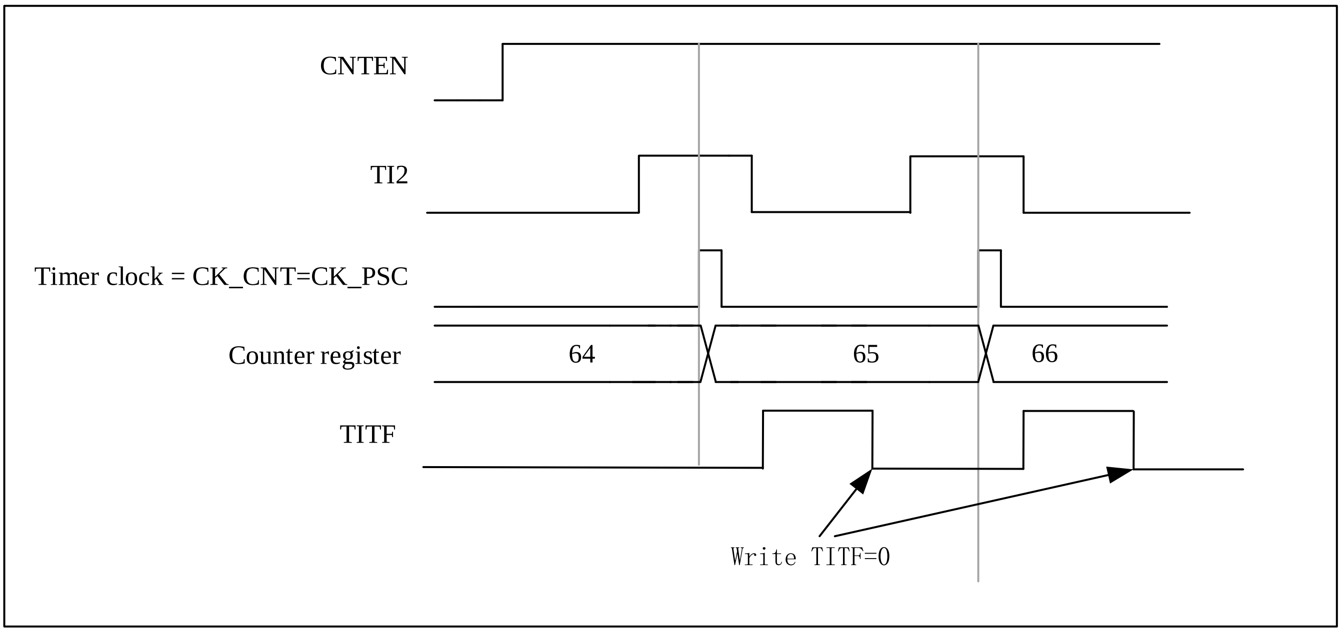
Figure 10-13 Control circuit in external clock mode 1

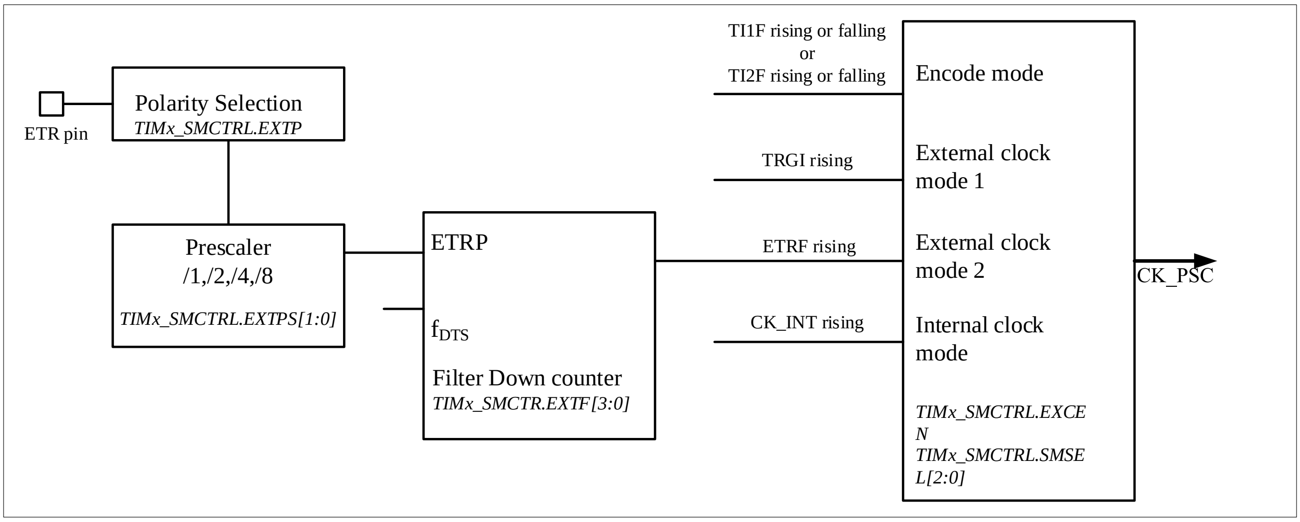


10.3.4.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 10-14 External trigger input block diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to ‘0000’
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to ‘01’
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to ‘0’, The rising edge of ETR is valid

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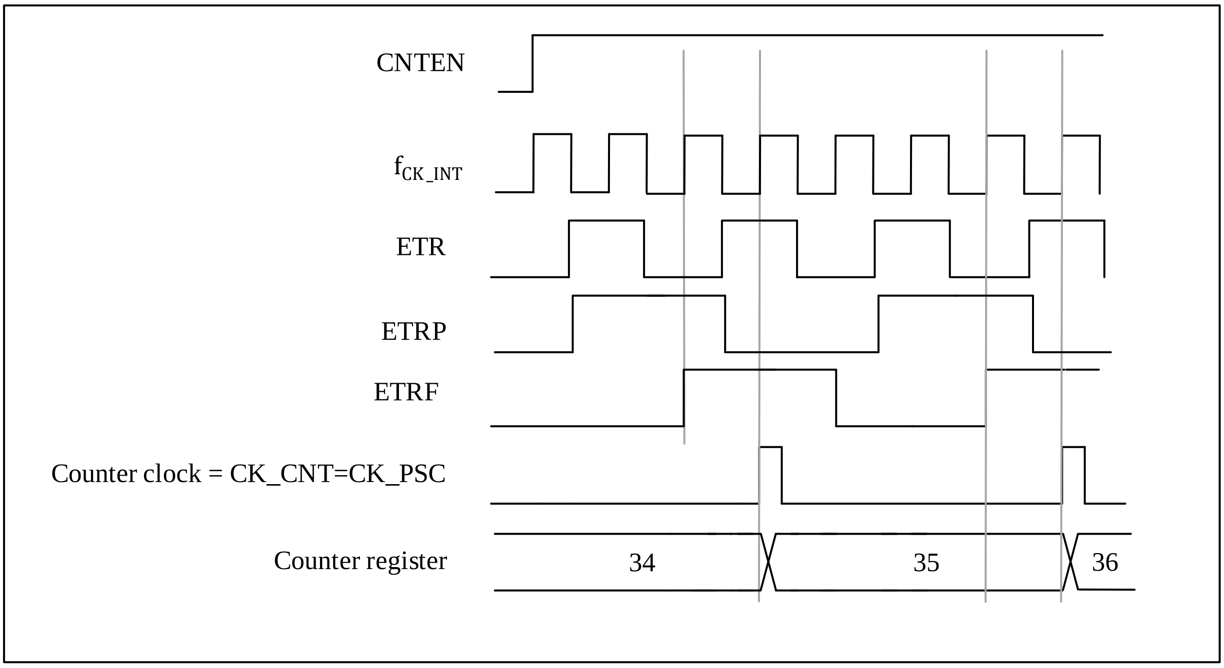
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 10-15 Control circuit in external clock mode 2



10.3.5 Capture/compare channels

Capture/compare channels include capture/compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequency division. The following figure shows a block diagram of a capture/compare channel.

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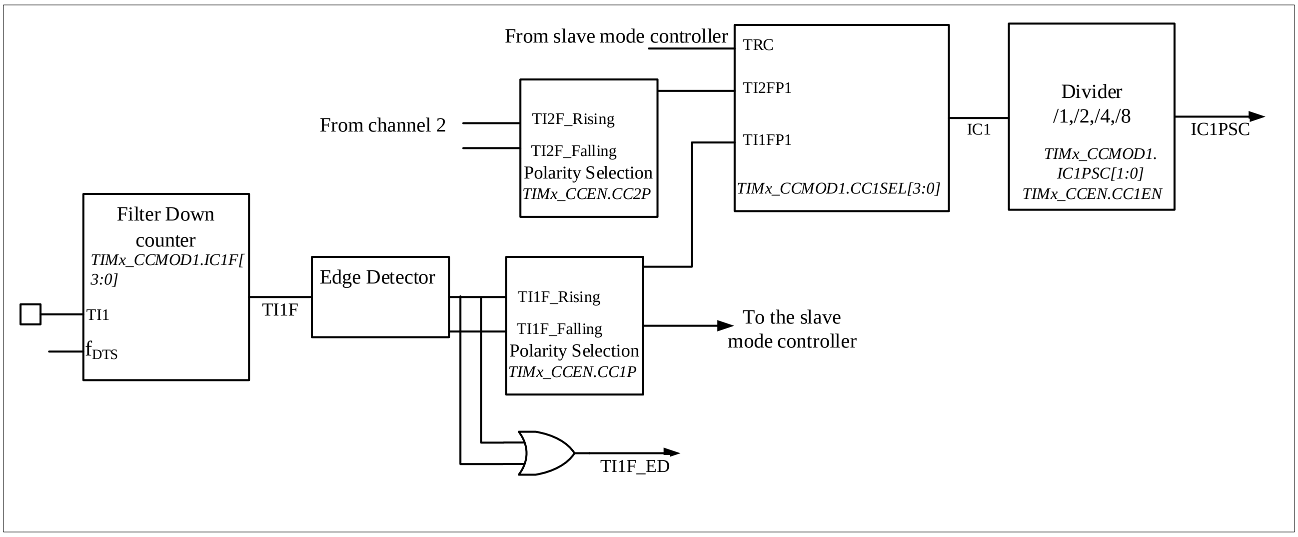
Figure 10-16 Capture/compare channel (example: channel 1 input stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 10-17 Capture/compare channel 1 main circuit

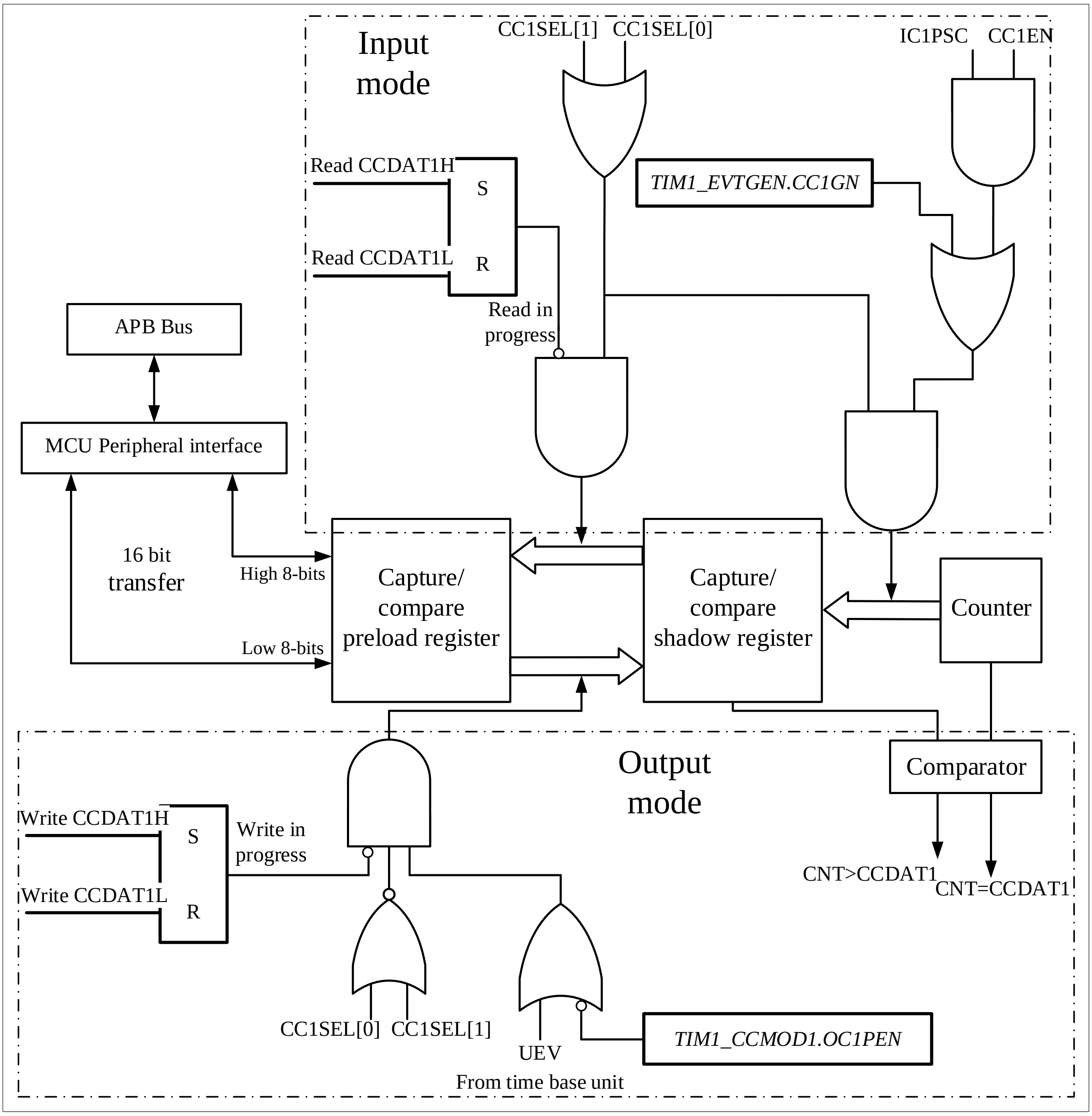

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Figure 10-18 Output part of channelx (x= 1,2,3, take channel 1 as example)

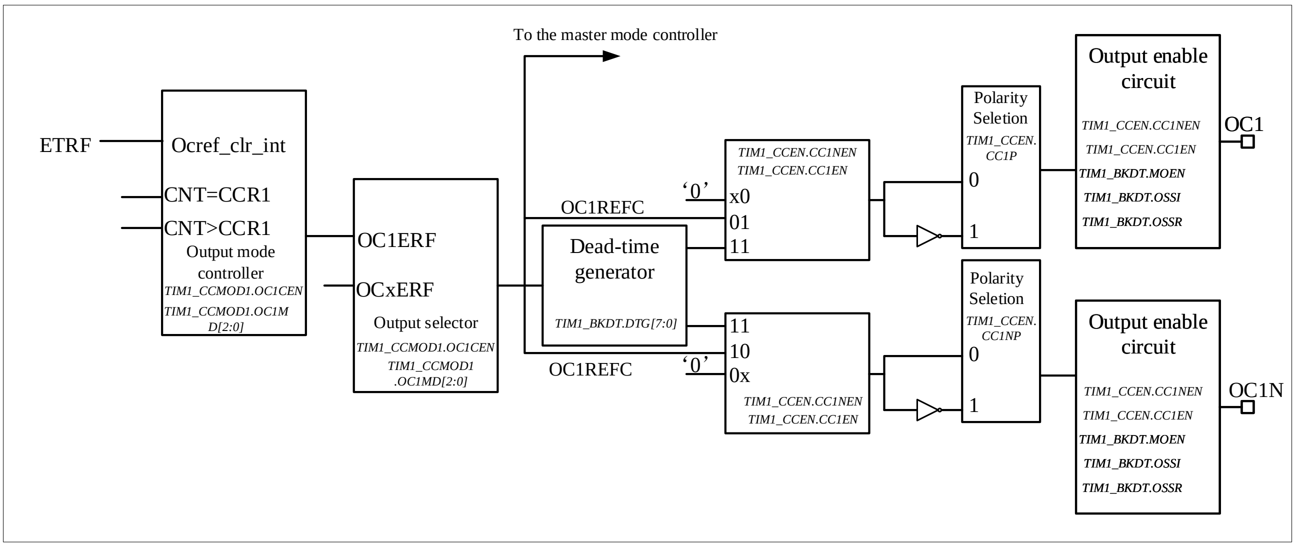
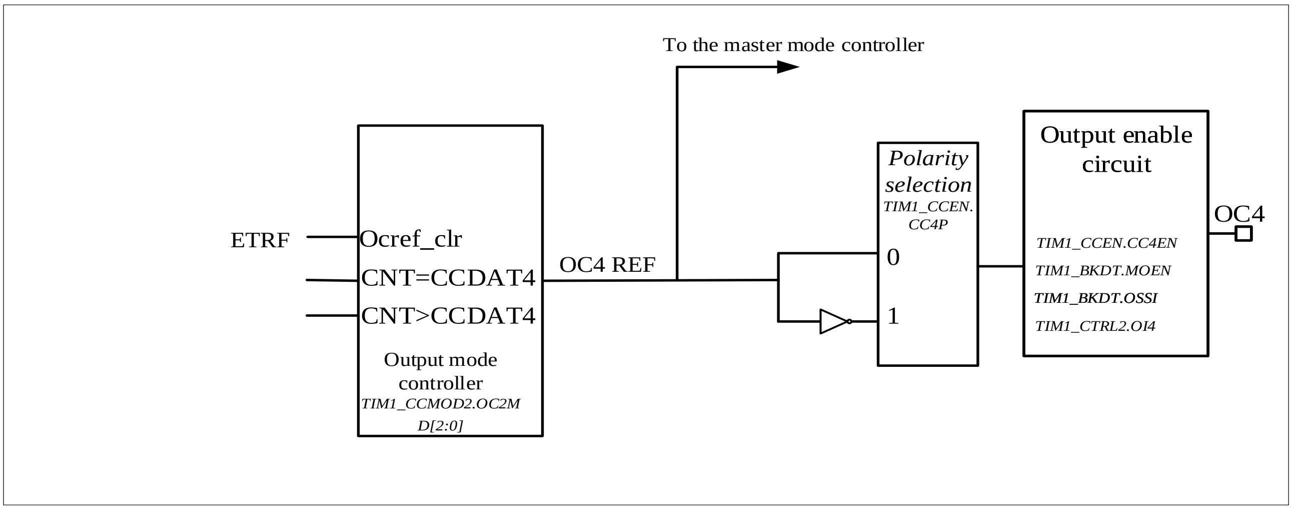


Figure 10-19 Output part of channelx (x= 4)



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

10.3.6 Input capture mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the

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corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to ‘01’. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Program the desired input filter duration:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to ‘0011’.

- By configuring TIMx_CCEN .CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= ‘00’ to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = ‘1’.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

10.3.7 PWM input mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to ‘01’ to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to ‘0’ to select the active polarity of filtered timer input 1(TI1FP1), valid on the rising edge.

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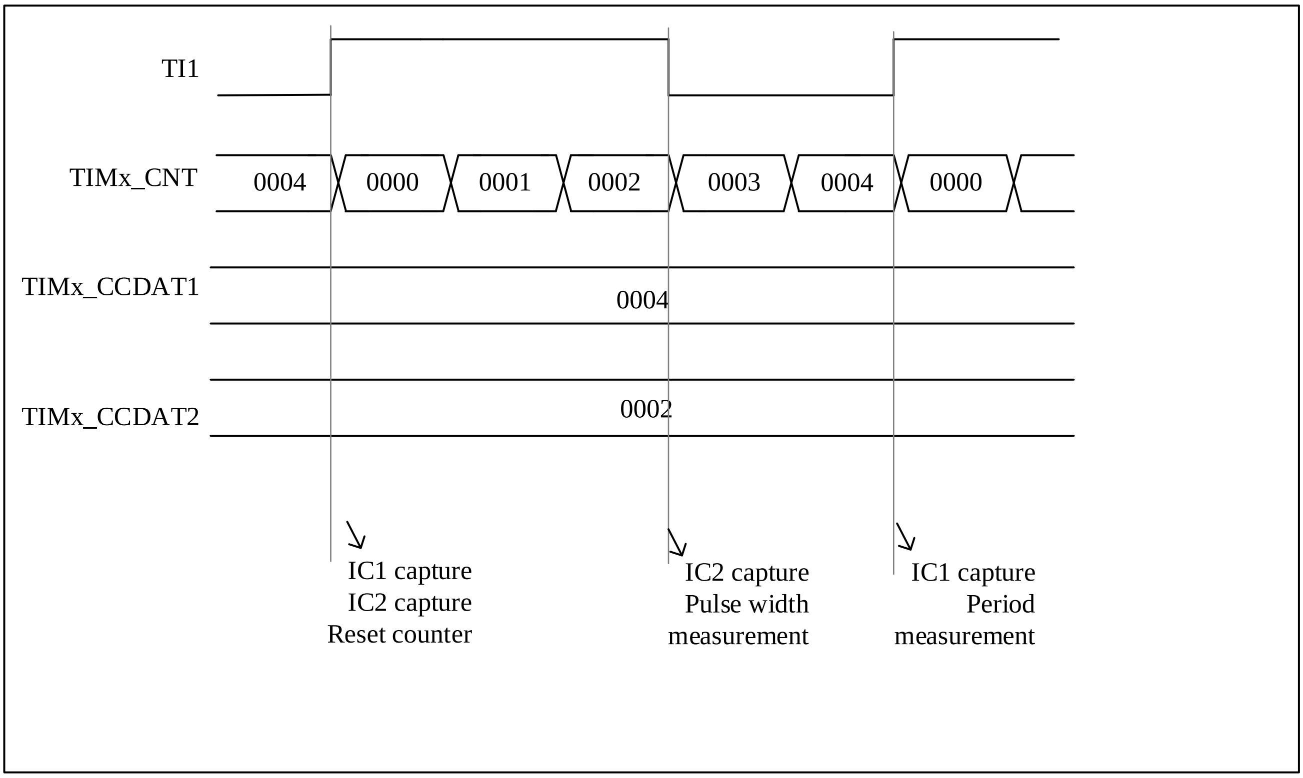
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), valid on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

Figure 10-20 PWM input mode timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

10.3.8 Forced output mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

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10.3.9 Output compare mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.
- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers(TIMx_CCDATx) or not.

The time resolution is one count of the counter.

In one-pulse mode, the output compare mode can also be used to output a single pulse.

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with desired data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

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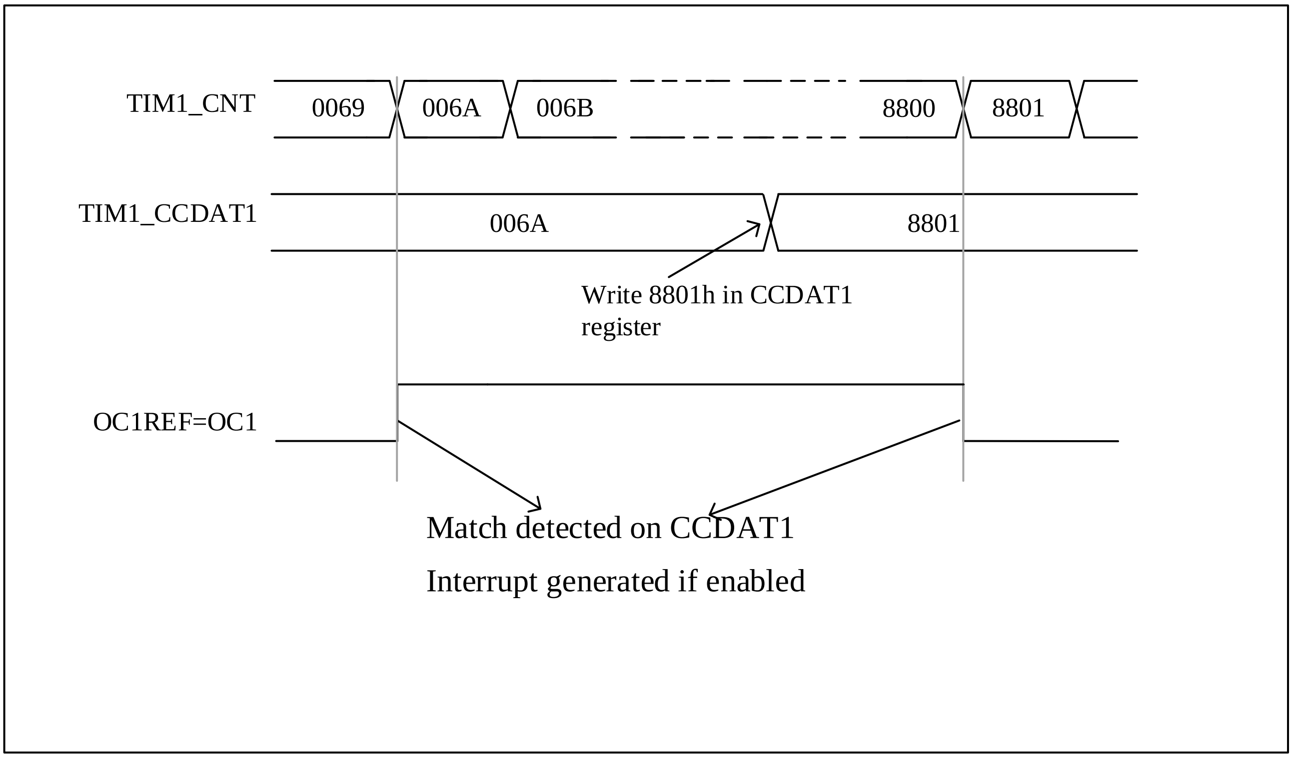
Figure 10-21 Output compare mode, toggle on OC1



10.3.10 PWM mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. On the other hand, to enable the output of OCx, user need to set the combination of the value of CCxEN, CCxNEN, MOEN, OSSI, and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

10.3.10.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts

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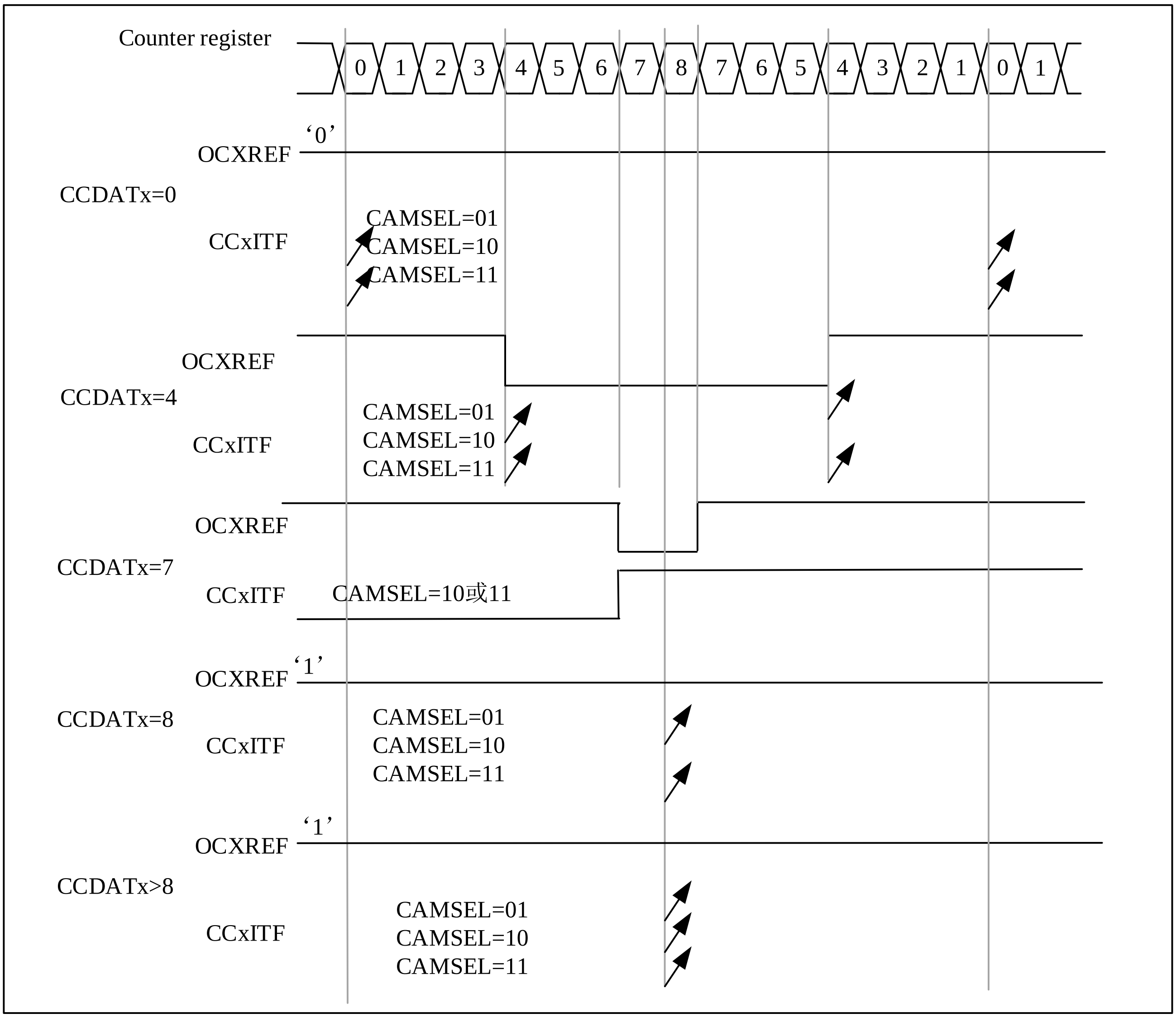
up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

Figure 10-22 Center-aligned PWM waveform (AR=8)



Notes that user should know when using center-aligned mode are as follow:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.

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■ To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and not writing the counter while it is running.

10.3.10.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

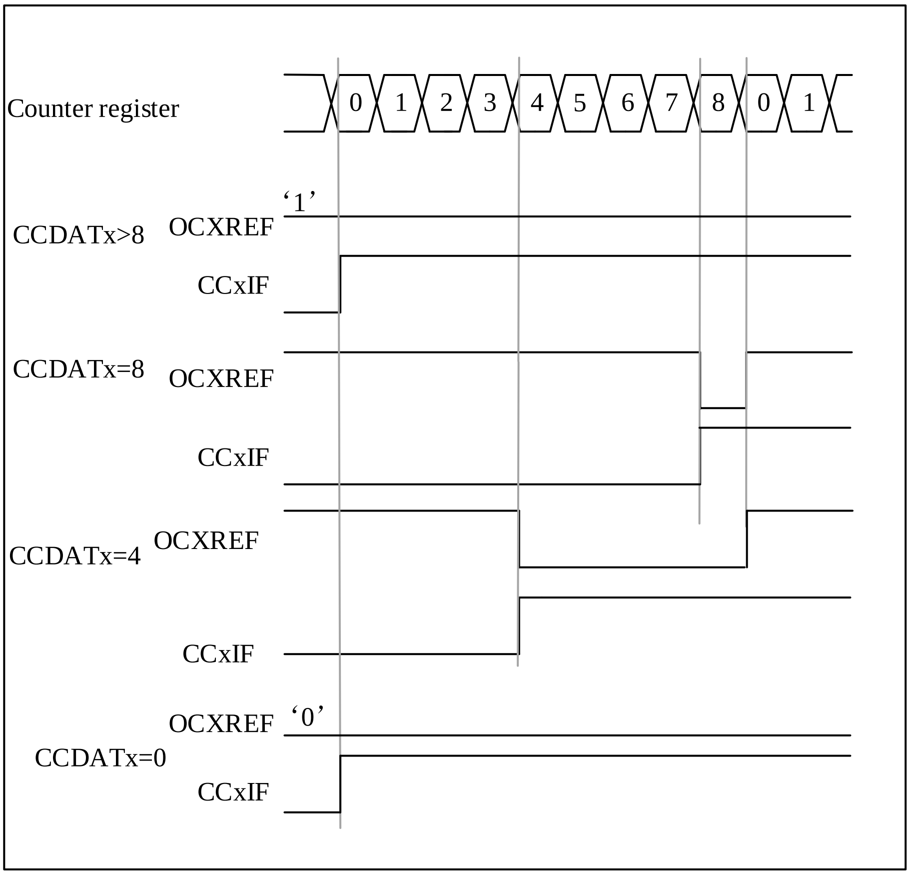
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Here is an example for PWM mode1.

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow.

Figure 10-23 Edge-aligned PWM waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Here is an example for PWM mode1.

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

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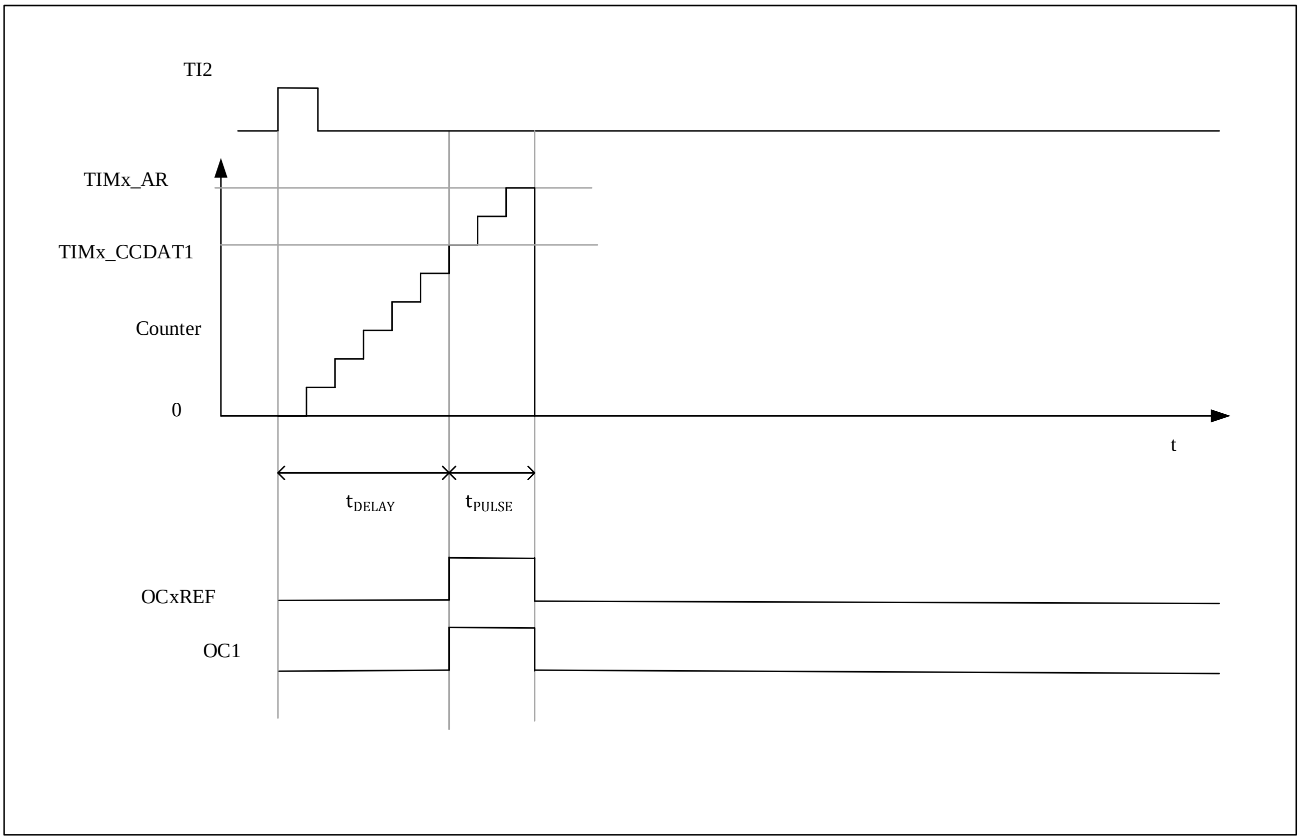
Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

10.3.11 One-pulse mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 9-41 Example of One-pulse mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;

2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= '01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= '0';

3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL= '110' (trigger mode);

4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of

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the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = ‘111’to select PWM2 mode;

6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

10.3.11.1 Special case: OCx fast enable:

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

10.3.12 Clearing the OCxREF signal on an external event

If user set TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Here is an example for it. To control the current, user can connect the ETR signal to the output of a comparator, and the operation for ETR should be as follow:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

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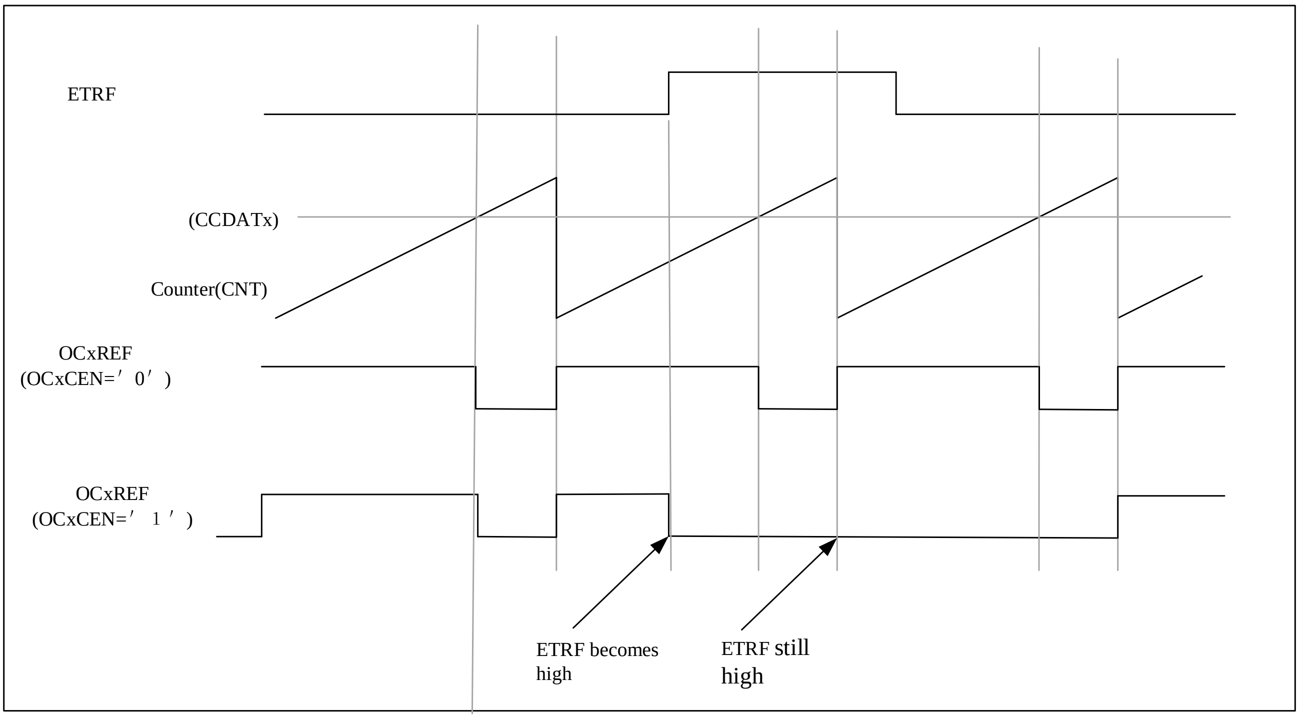
Figure 10-24 Clearing the OCxREF of TIMx



10.3.13 Complementary outputs with dead-time insertion

Advanced-control timer can output two complementary signals, and manage the switching-off and switching-on of outputs. This is called dead-time. User should adjust dead-time depending on the devices connected to the outputs and their characteristics.

User can select the polarity of outputs by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP. And this selection is independently for each output.

User can control the complementary signals OCx and OCxN by setting the combination of several control bits, which are TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. When switching to the IDLE state, the dead-time will be activated.

If user set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN at the same time, a dead-time will be insert. If there is a break circuit, the TIMx_BKDT.MOEN should be set too. There are 10-bit dead-time generators for each channel.

Reference waveform OCxREF can generates 2 outputs OCx and OCxN. And if OCx and OCxN are active high, the OCx ouput signal is the same as the reference signal and the OCxN output signal is the opposite of the reference signal. However, OCx output signal will be delayed relative to the reference rising edge and the OCxN output signal will be delayed relative to the reference falling edge. If the delay is greater than the width of the active OCx or OCxN output, the corresponding pulse will not generated.

The relationships between the output signals of the dead-time generator and the reference signal OCxREF are as follow.

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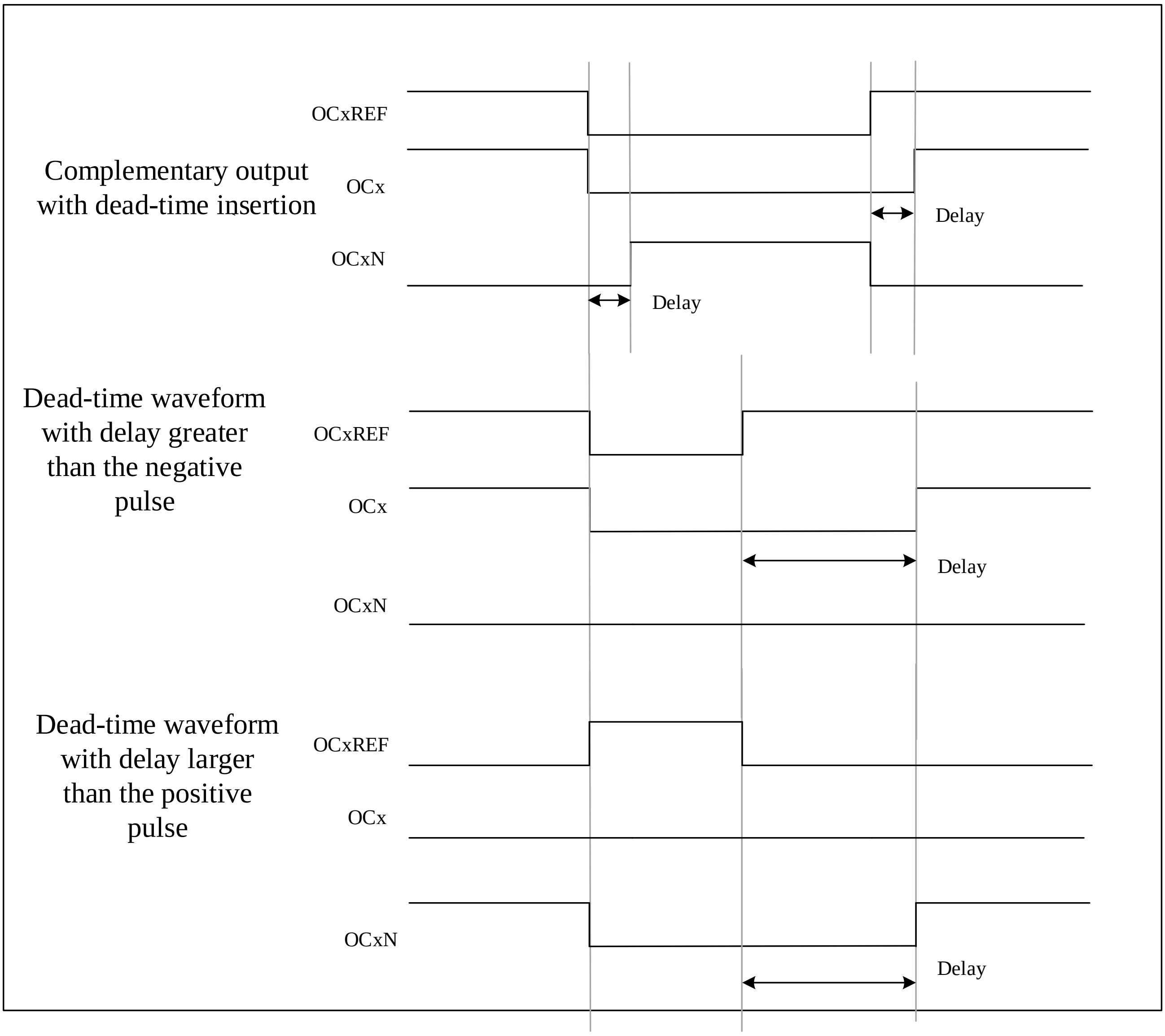
Assume that TIMx_CCEN.CCxP=0, TIMx_CCEN.CCxNP=0, TIMx_BKDT.MOEN=1, TIMx_CCEN.CCxEN=1, TIMx_CCEN.CCxNEN=1.

Figure 10-25 Complementary output with dead-time insertion



User can set TIMx_BKDT.DTGN to programme the dead-time delay for each of the channels.

10.3.13.1 Redirecting OCxREF to OCx or OCxN

User can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to re-directed OCxREF to the OCx output or to OCxN output, in output mode.

Here are two ways to use this function. When the complementary remains at its inactive level, user can use this function to send a specific waveform, such as PWM or static active level. User can also use this function to set both outputs in their inactive level or both outputs active and complementary with dead-time.

If user set TIMx_CCEN.CCxEN=0 and TIMx_CCEN.CCxNEN=1, it will not complemented, and OCxN will become active when OCxREF is high. On the other hand, if user set TIMx_CCEN.CCxEN=1 and

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TIMx_CCEN.CCxNEN=1, OCx will become active when OCxREF is high. On the contrary, OCxN will become active when OCxREF is low.

10.3.14 Break function

The output enable signals and inactive levels will be modified when setting the corresponding control bits when using the break function. However, the output of OCx and OCxN cannot at the active level at the same time no matter when, that is, (CCxP^OIx) ^(CCxNP^OIxN)!=0.

When multiple break signals are enabled, each break signal constitutes an OR logic. Here are some signal which can be the source of breaking.

- The break input pin
- A clock failure event, generated by the clock security system in the clock controller.
- A PVD failure event.
- Core Hardfault event.
- The output signal of the comparator (configured in the comparator module, high level break).
- By software through the TIMx_EVTGEN.BGN.

The break circuit will be disable after reset. And the MOEN bit will be low. User can set TIMx_BKDT.BKEN to enable the break function. The polarity of break input signal can be selected by setting TIMx_BKDT.BKP. User can modify the TIMx_BKDT.BKEN and TIMx_BKDT.BKP at the same time. After user set the TIMx_BKDT.BKEN and TIMx_BKDT.BKP, there is 1 APB clock cycle delay before the option take effect. Therefore, user need to wait 1 APB clock cycle to read back the value of the written bit.

The falling edge of MOEN can be asynchronous, so between the actual signal and the synchronous control bit, there set a resynchronization circuit. This circuit will cause a delay between the asynchronous and the synchronous signal. When user set TIMx_BKDT.MOEN while it is low, user need to insert a delay before reading the value. Because an asynchronous signal was written but user read the synchronous signal.

The behaviors that after a break occurs are as follow:

- TIMx_BKDT.MOEN will be cleared asynchronously, and then the outputs will be put in inactive state, idle state or reset state. The state of output is selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is off.
- Once TIMx_BKDT.MOEN=0, the output of each output channel will be driven with the level programmed in TIMx_CTRL2.OIx. Timer will release the enable outputs(taken over by GPIO controller) if TIMx_BKDT.OSSI=0, otherwise it will remains high.
- If user choose to use complementary outputs, the behaviors of TIM are as follow
  - Depends on the polarity, the outputs will be set in reset state first. It is an asynchronous option so it still works even if there is no clock provided to the timer.
  - The dead-time generator will reactivated if the timer clock is still provided, and drive the outputs according to the value of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN after the dead-time when (CCxP ^ OIx) ^

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(CCxNP^OIxN)! = 0, that is, the OCx and OCxN still cannot be driven to active level at the same time. Note that the dead-time will be longer than usual because of the resynchronization on MOEN (almost 2 cycles of ck_tim).

- ◆ Timer will release the output control if TIMx_BKDT.OSSI=0. Otherwise, if the enable output was high, it will remain high. If it was low, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is high.

- If TIMx_DINTEN.BIEN=1, when TIMx_STS.BITF=1, an interrupt will be generated.
- If user set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will be set automatically when the next UEV happened. User can use this to regulate. If user did not set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will remain low until been set 1 again. At this situation, user can use this for security. User can connect the break input to thermal sensors, alarm for power drivers, or other security components.
- When the break input is active, TIMx_BKDT.MOEN cannot be set automatically or by software at the same time, and the TIMx_STS.BITF cannot be cleared. Because the break inputs are active on level.

To insure the security of application, the break circuit has the write protection function, and there is break input and output management too. It allow user to freeze some parameters, such as dead-time duration, OCx/OCxN polarities and state when disabled, OCxMD configurations, break enable and polarity. User can choose one of the 3 levels of protection to use by setting TIMx_BKDT.LCKCFG. However, the TIMx_BKDT.LCKCFG can only be written once after an MCU reset.

An example for output behavior in response to a break is as follow

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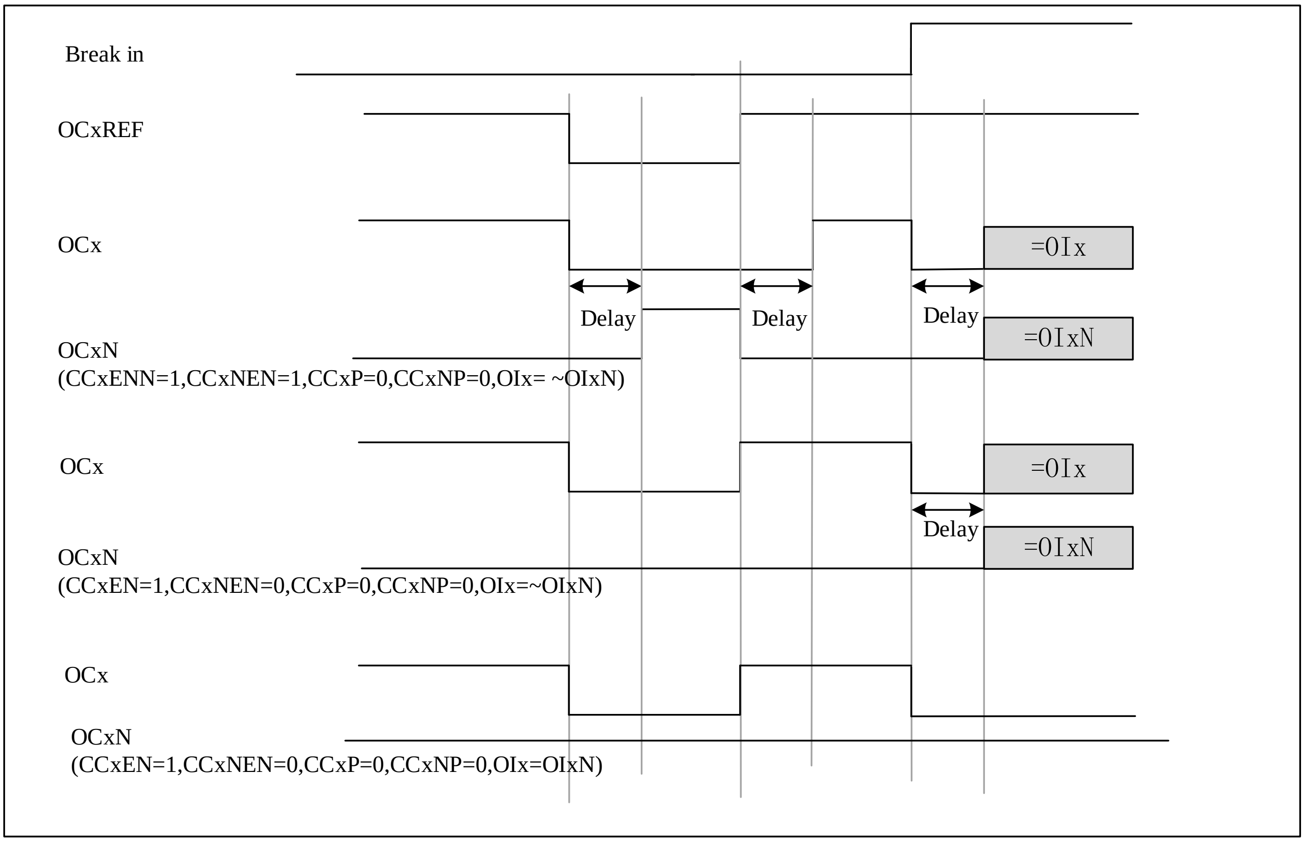
Figure 10-26 Output behavior in response to a break



10.3.15 Debug mode

When the microcontroller is in debug mode (the Cortex-M4 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details, see 29.4.3.

10.3.16 TIMx and external trigger synchronization

TIMx timers can be synchronized by a trigger in slave modes (reset, trigger and gated).

10.3.16.1 Slave mode: Reset mode

In reset mode, the trigger event can reset the counter and the prescaler updates the preload registers TIMx_AR, TIMx_CCDATx, and generates the update event UEV (TIMx_CTRL1.UPRS=0).

The following is an example of a reset mode:

1. Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);

2. The slave mode is selected as reset mode (TIMx_SMCTRL.SMSEL=100), and the trigger input is selected as TI1 (TIMx_SMCTRL.TSEL=101);

3. Start counter (TIMx_CTRL1.CNTEN = 1)

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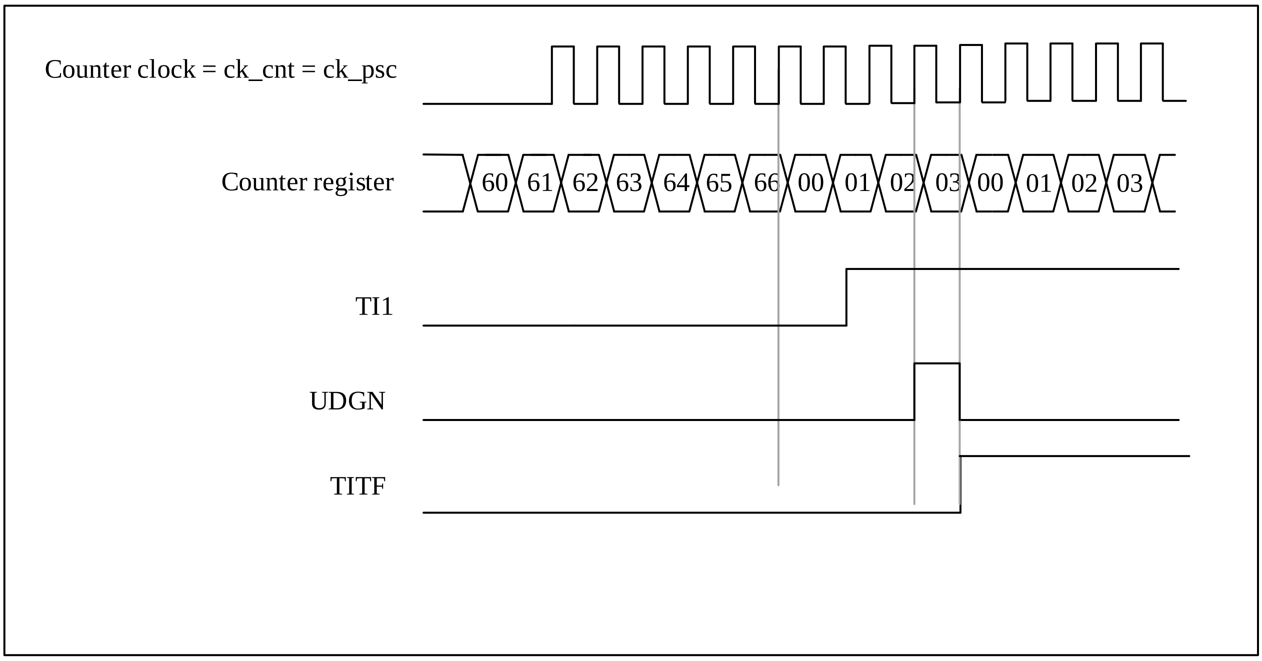
After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI1 and the actual reset of the counter is due to the resynchronization circuit on TI1 input.

Figure 10-27 Control circuit in reset mode



10.3.16.2 Slave mode: Trigger mode

In trigger mode, the trigger event (rising edge/falling edge) of the input port can trigger the counter to start counting.

The following is an example of a trigger pattern:

1. Channel 2 is configured as input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01, TIMx_CCEN.CC2P=0);

2. Select from mode to trigger mode (TIMx_SMCTRL.SMSEL=110), select TI2 for trigger input (TIMx_SMCTRL.TSEL=110);

When TI2 detects a rising edge, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI2 and the actual start of the counter is due to the resynchronization circuit on TI2 input.

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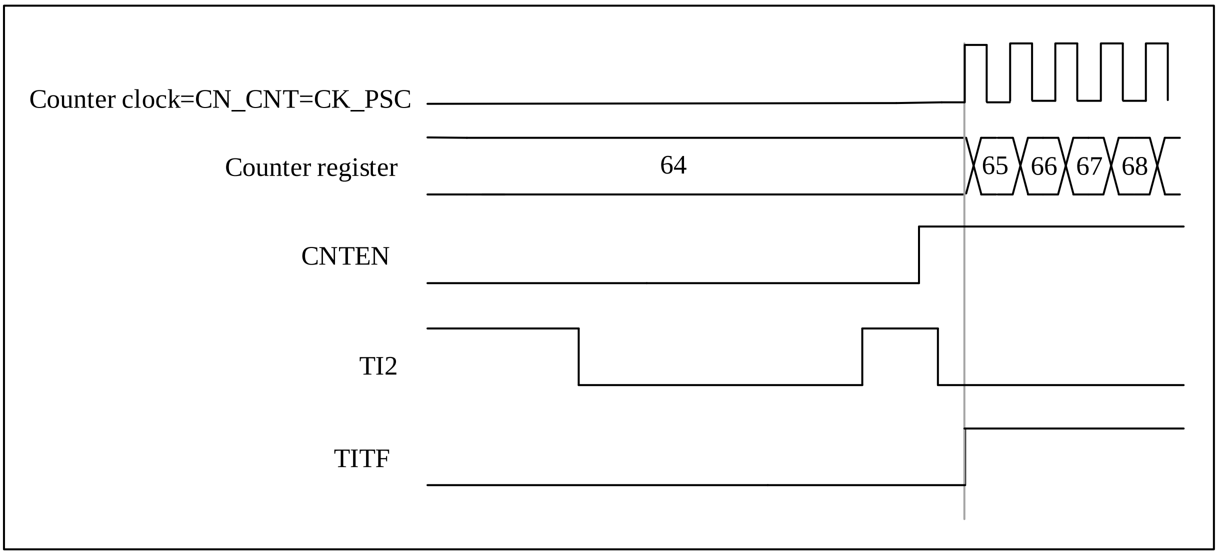
Figure 10-28 Control circuit in Trigger mode



10.3.16.3 Slave mode: Gated mode

In gate control mode, the level polarity of the input port can control whether the counter counts.

The following is an example of a gated pattern:

1. Channel 1 is configured as input detection active low on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1);

2. Select the slave mode as the gated mode (TIMx_SMCTRL.SMSEL=101), and select TI1 as the trigger input (TIMx_SMCTRL.TSEL=101);

3. Start counter (TIMx_CTRL1.CNTEN = 1)

When TI1 detects that the level changes from low to high, the counter stops counting, and when TI1 detects that the level changes from high to low, the counter starts counting, and the trigger flag will be set when it starts or stops counting (TIMx_STS.TITF=1);

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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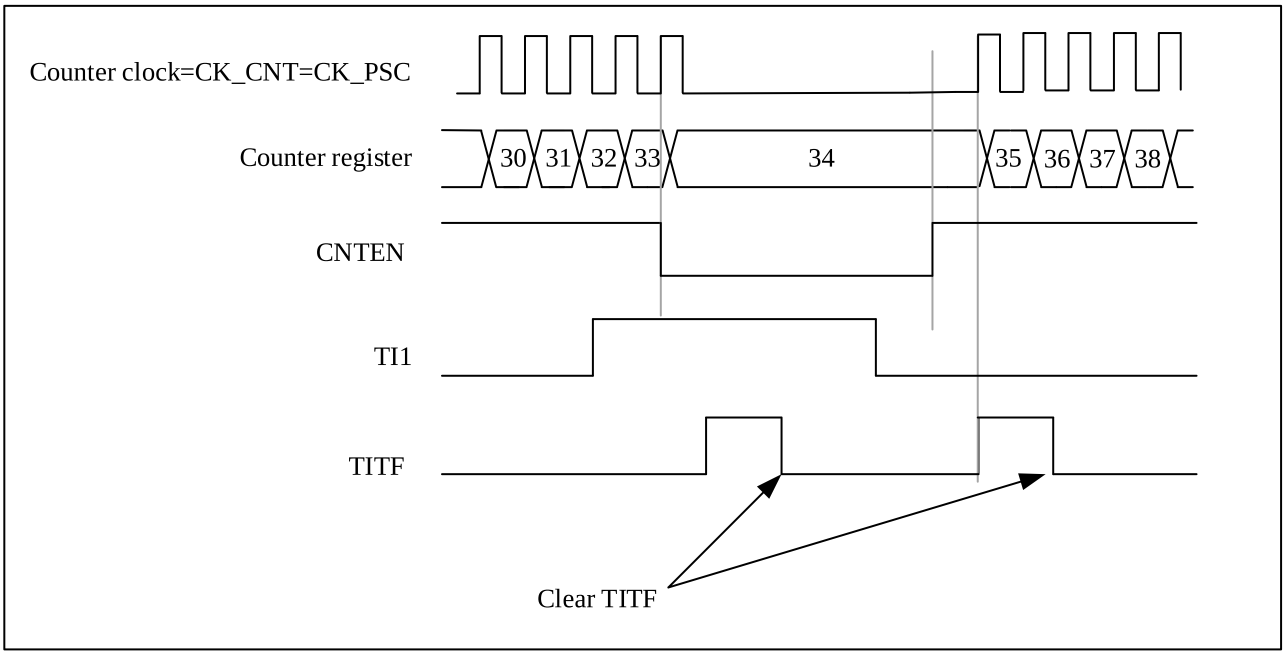
Figure 10-29 Control circuit in Gated mode



10.3.16.4 Slave mode: Trigger Mode + External Clock Mode 2

In reset mode, trigger mode and gate control mode, the counter clock can be selected as external clock mode 2, and the ETR signal is used as the external clock source input. At this time, the trigger selection needs to select non-ETRF (TIMx_SMCTRL.TSEL=111).

Here is an example:

1. Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);

2. Enable external clock mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=110), select TI1 for trigger input (TIMx_SMCTRL.TSEL=101);

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and the trigger flag is set (TIMx_STS.TITF=1);

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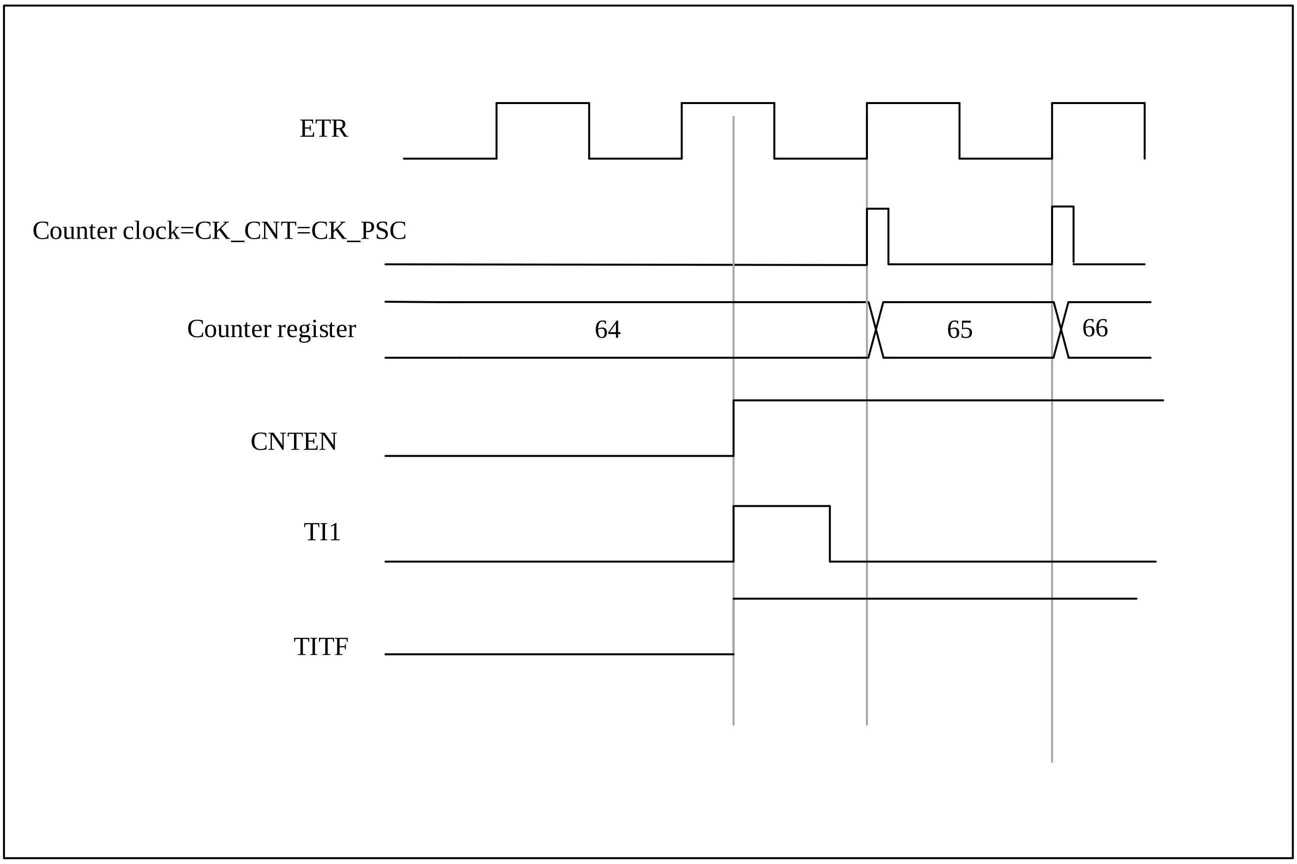
Figure 10-30 Control circuit in Trigger Mode + External Clock Mode2



10.3.17 Timer synchronization

All TIM timers are internally connected for timer synchronization or chaining. For more details, see 11.3.14.

10.3.18 6-step PWM generation

In order to modify the configuration of all channels at the same time, the configuration of the next step can be set in advance (the preloaded bits are OCxMD, CCxEN and CCxNEN). When a COM commutation event occurs, the OCxMD, CCxEN, and CCxNEN preload bits are transferred to the shadow register bits.

COM commutation event generation method:

1. The software sets TIMx_EVTGEN.CCUDGN;

2. Generated by hardware on the rising edge of TRGI;

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, enabling interrupts (TIMx_DINTEN.COMIEN) will generate interrupts, and enabling DMA requests (TIMx_DINTEN.COMDEN) will generate DMA requests.

The following figure shows the output timing diagram of OCx and OCxN when a COM commutation event occurs in three different configurations:

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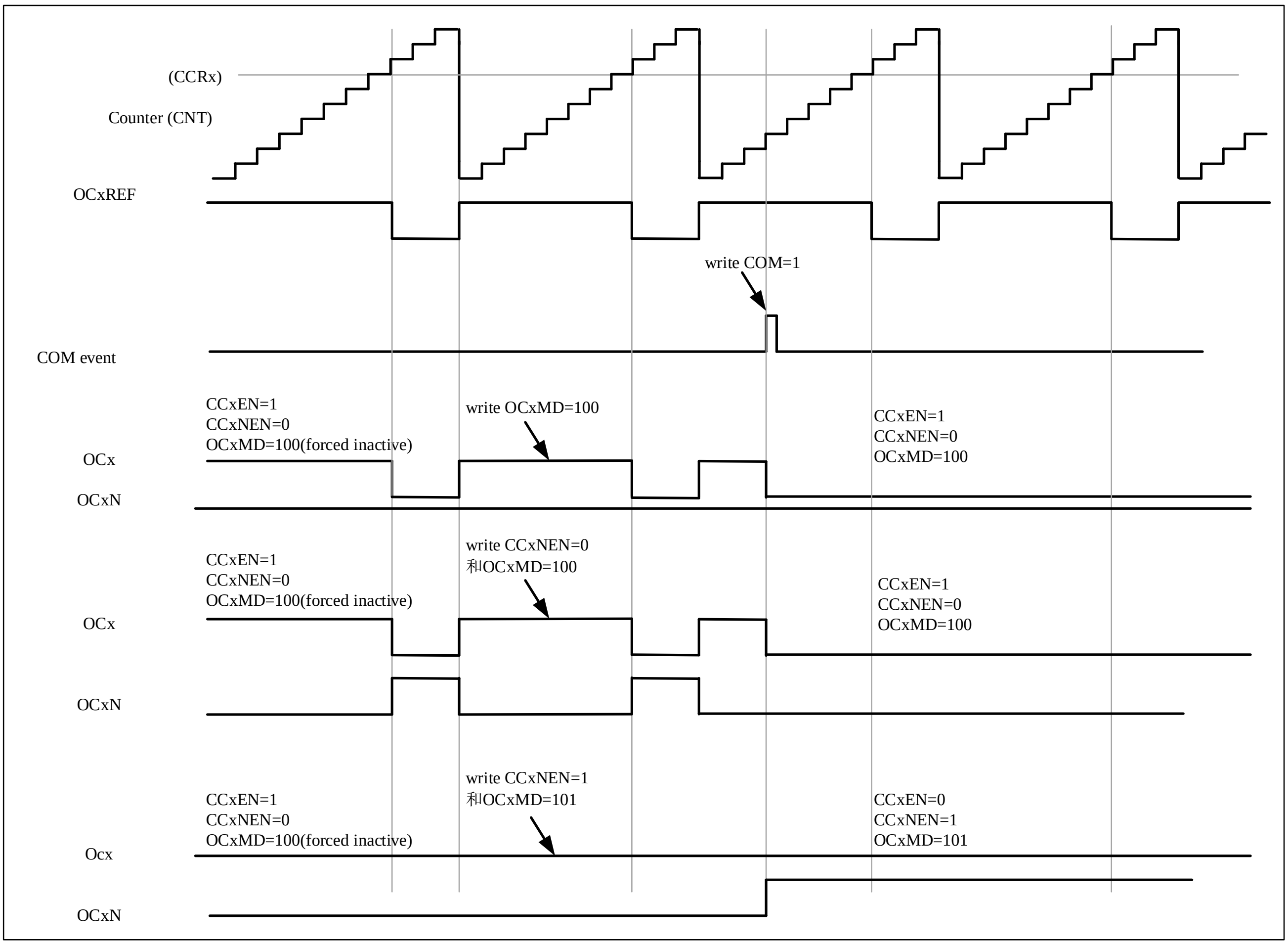
Figure 10-31 6-step PWM generation, COM example (OSSR=1)



10.3.19 Encoder interface mode

The encoder uses two inputs TI1 and TI2 as an interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are three types of encoder counting modes:

1. The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘001’;

2. The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’010’;

3. The counter counts on the edges of TI1 and TI2 at the same time, TIMx_SMCTRL.SMSEL = ‘011’;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in Table 10-1 Counting direction versus encoder signals:

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Table 10-1 Counting direction versus encoder signals

Active edge	Level on opposite signals (TI1FP1 forTI2, TI2FP2 for TI1)	TI1FP1 signal		TI2FP2 signal	
		Rising	**Falling**	**Rising**	**Falling**
Counting only at TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only at TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edge triggering selected to suppress input jitter:

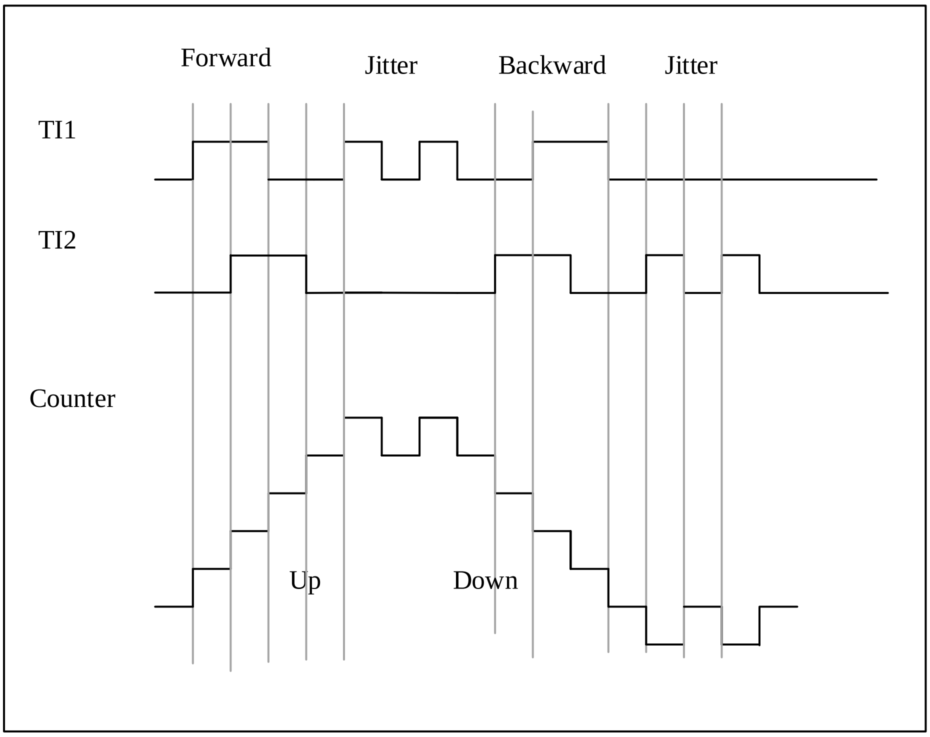
1. IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= '01'), IC1FP1 is not inverted (TIMx_CCEN.CC1P= '0');

2. IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= '01'), IC2FP2 is not inverted (TIMx_CCEN.CC2P= '0');

3. The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = '011');

4. Enable counter TIMx_CTRL1.CNTEN= '1';

Figure 10-32 Example of counter operation in encoder interface mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above)

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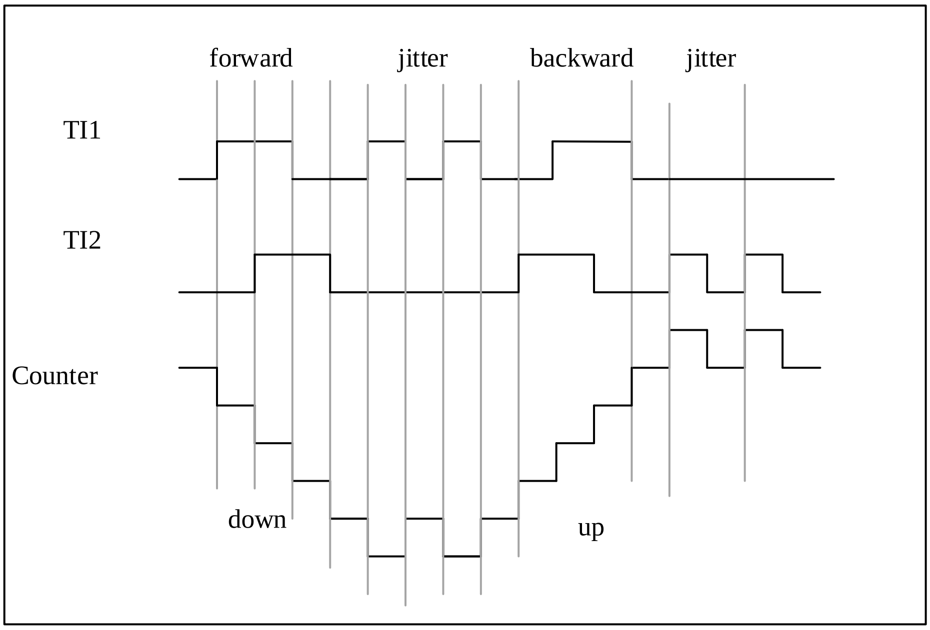
Figure 10-33 Encoder interface mode example with IC1FP1 polarity inverted



10.3.20 Interfacing with Hall sensor

Connect the Hall sensor to the three input pins (CC1, CC2 and CC3) of the timer, and then select the XOR function to pass the inputs of TIMx_CH1, TIMx_CH2 and TIMx_CH3 through the XOR gate as the output of TI1 to channel 1 for capture signal.

The timer needs to be configured as the reset mode in slave mode (TIMx_SMCTRL.SMSEL= ‘100’); the edge of the trigger select TI1 triggers TI1F_ED (TIMx_SMCTRL.TSEL= ‘100’), any change in the Hall 3 inputs will trigger the counter to recount, so it is used as a time reference; the capture/compare channel 1 is configured to capture the TRC signal in capture mode (TIMx_CCMOD1.CC1SEL= ‘11’), which is used to calculate the two input time intervals, thereby reflecting the motor speed.

Select timer channel 2 to output pulses to the advanced timer to trigger the COM event of the advanced timer to update the control bits of the output PWM. The trigger selection of the advanced timer needs to select the corresponding internal trigger signal (TIMx_SMCTRL.TSEL="ITRx"), the capture/compare preload control bit needs to be configured to support preload (TIMx_CTRL2.CCPCTL=1) and support the rising edge of TRGI Trigger an update (TIMx_CTRL2.CCUSEL=1).

This example is shown in the following figure.

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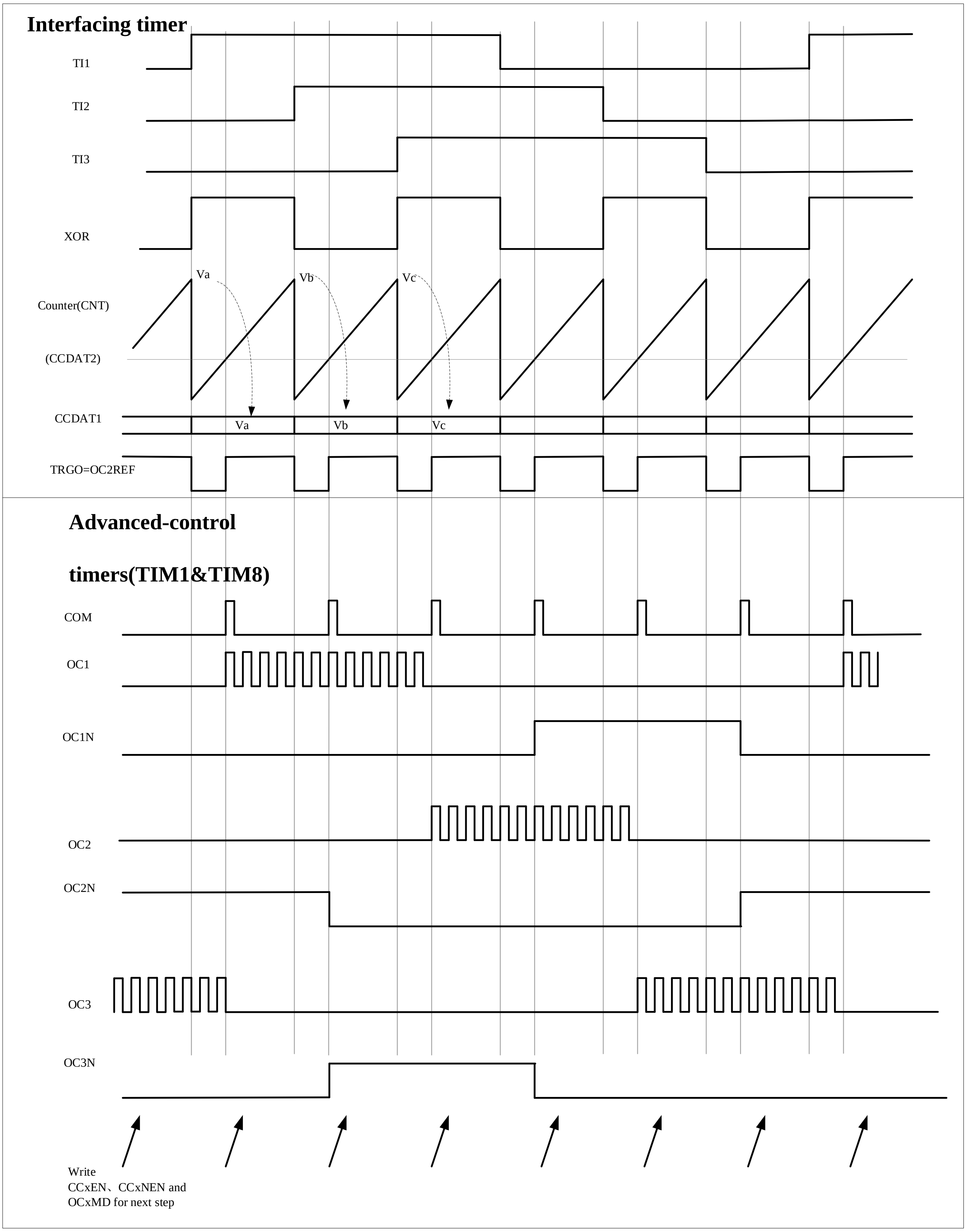
Figure 10-34 Example of Hall sensor interface



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10.4 TIMx registers(x=1, 8)

For abbreviations used in registers, see section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

10.4.1 TIMx register overview

Table 10-2 TIMx register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved														PBKPEN	LBKPEN	CLRSEL	Reserved	Reserved	Reserved	C1SEL	IOMBKPEN	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
	Reset Value															0	0	0				0	0	0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved													OI6	Reserved	OI5	Reserved	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1	TI1SEL	MMSEL[2:0]			CCDSEL	CCUSEL	Reserved	CCPCTL
	Reset Value														0		0		0	0	0	0	0	0	0	0	0	0	0	0	0		0
008h	TIMx_SMCTRL	Reserved																EXTP	EXCEN	EXTPS[1:0]		EXTF[3:0]				MSMD	TSEL[2:0]			Reserved	SMSEL[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
00Ch	TIMx_DINTEN	Reserved																	TDEN	COMDEN	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	BIEN	TIEN	COMIEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	TIMx_STS	Reserved														CC6ITF	CC5ITF	Reserved			CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved	BITF	TITF	COMITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	Reset Value															0	0				0	0	0	0		0	0	0	0	0	0	0	0
014h	TIMx_EVTGEN	Reserved																								BGN	TGN	CCUDGN	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	Reset Value																									0	0	0	0	0	0	0	0
018h	TIMx_CCMOD1	Reserved																OC2CEN	OC2MD[2:0]			OC2PEN	OC2FEN	CC2SEL[1:0]		OC1CEN	OC1MD[2:0]			OC1PEN	OC1FEN	CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved																IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																OC4CEN	OC4MD[2:0]			OC4PEN	OC4FEN	CC4SEL[1:0]		OC3CEN	OC3MD[2:0]			OC3PEN	OC3FEN	CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCEN	Reserved										CC6P	CC6EN	Reserved		CC5P	CC5EN	Reserved		CC4P	CC4EN	CC3NP	CC3NEN	CC3P	CC3EN	CC2NP	CC2NEN	CC2P	CC2EN	CC1NP	CC1NEN	CC1P	CC1EN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value											0	0			0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	TIMx_CNT	Reserved																CNT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved																PSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved																AR[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
030h	TIMx_REPCNT	Reserved																								REPCNT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
034h	TIMx_CCDAT1	Reserved																CCDAT1[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT2	Reserved																CCDAT2[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	TIMx_CCDAT3	Reserved																CCDAT3[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	TIMx_CCDAT4	Reserved																CCDAT4[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	TIMx_BKDT	Reserved																MOEN	AOEN	BKP	BKEN	OSSR	OSSI	LCKCFG[1:0]		DTGN[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	TIMx_DCTRL	Reserved																			DBLEN[4:0]					Reserved			DBADDR[4:0]				
	Reset Value																				0	0	0	0	0				0	0	0	0	0
04Ch	TIMx_DADDR	Reserved																BURST[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	TIMx_CCMOD3	Reserved																OC6CEN	OC6MD[2:0]			OC6PEN	OC6FEN	Reserved		OC5CEN	OC5MD[2:0]			OC5PEN	OC5FEN	Reserved	
	Reset Value																	0	0	0	0	0	0			0	0	0	0	0	0		
054h	TIMx_CCDAT5	Reserved																CCDAT5[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
058h	TIMx_CCDAT6	Reserved																CCDAT6[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

10.4.2 Control register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31–18	17	16
Reserved	PBKPEN	LOCKUPEN
	rw	rw

15	14–12	11	10	9–8	7	6–5	4	3	2	1	0
CLRSEL	Reserved	C1SEL	IOMBKPEN	CLKD[1:0]	ARPEN	CAMSEL[1:0]	DIR	ONEPM	UPRS	UPDIS	CNTEN
rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	PBKPEN	PVD as BKP enable 0: Disable 1: Enable
16	LBKPEN	LockUp as BKP enable 0: Disable 1: Enable
15	CLRSEL	OCxREF clear selection 0: Select the external OCxREF clear from ETR 1: Select the internal OCxREF clear from comparator
14:12	Reserved	Reserved, the reset value must be maintained
11	C1SEL	Channel 1 selection 0: Select external CH1 signal from IOM 1: Select internal CH1 signal from COMP
10	IOMBKPEN	Enabling IOM as BKP 0: Enable. Select external break (from IOM) signal. 1: Disable. Select internal break (from COMP) signal.
9:8	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and DTS (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK\_INT}$ 01: $t_{DTS} = 2 \times t_{CK\_INT}$ 10: $t_{DTS} = 4 \times t_{CK\_INT}$ 11: Reserved, do not use this configuration
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:5	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
4	DIR	Direction 0: Up-counting 1: Down-counting

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Bit field	Name	Description
		Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.
3	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
1	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

10.4.3 Control register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

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31–19	18	17	16
Reserved	OI6	Reserved	OI5
	rw		rw

15	14	13	12	11	10	9	8	7	6–4	3	2	1	0
Reserved	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1	TI1SEL	MMSEL[2:0]	CCDSEL	CCUSEL	Reserved	CCPCTL
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	OI6	Output idle state 6 (OC6 output). See TIMx_CTRL2.OI1 bit.
17	Reserved	Reserved, the reset value must be maintained
16	OI5	Output idle state 5 (OC5 output). See TIMx_CTRL2.OI1 bit.
15	Reserved	Reserved, the reset value must be maintained
14	OI4	Output idle state 4 (OC4 output). See TIMx_CTRL2.OI1 bit.
13	OI3N	Output idle state 3 (OC3N output). See TIMx_CTRL2.OI1N bits.
12	OI3	Output idle state 3 (OC3 output). See TIMx_CTRL2.OI1 bit.
11	OI2N	Output idle state 2 (OC2N output). See TIMx_CTRL2.OI1N bits.
10	OI2	Output idle state 2 (OC2 output). See TIMx_CTRL2.OI1 bit.
9	OI1N	Output Idle state 1 (OC1N Output) 0: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 0 1: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 1
8	OI1	Output Idle state 1 0: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 0 1: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 1
7	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler.

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Bit field	Name	Description
		011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 100: Compare - OC1REF signal is used as the trigger output (TRGO). 101: Compare - OC2REF signal is used as the trigger output (TRGO). 110: Compare - OC3REF signal is used as the trigger output (TRGO). 111: Compare - OC4REF signal is used as the trigger output (TRGO).
3	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
2	CCUSEL	Capture/compare control update selection 0: If TIMx_CTRL2.CCPCTL = 1, they can only be updated by setting CCUDGN bits 1: If TIMx_CTRL2.CCPCTL = 1, they can be updated by setting CCUDGN bits or a rising edge on TRGI. *Note: This bit only applied to channels with complementary outputs.*
1	Reserved	Reserved, the reset value must be maintained
0	CCPCTL	Capture/ Compare preloaded control 0: No preloading of CCxEN, CCxNEN and OCxMD bits occurs. 1: Preloading of CCxEN, CCxNEN and OCxMD bits occurs. they are updated only when a commutation event COM occurs (CCUDGN bit set or rising edge on TRGI depending on CCUSEL bit) *Note: This bit only applied to channels with complementary outputs.*

10.4.4 Slave mode control register (TIMx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

15	14	13-12	11-8	7	6-4	3	2-0
EXTP	EXCEN	EXTPS[1:0]	EXTF[3:0]	MSMD	TSEL[2:0]	Reserved	SMSEL[2:0]
rw	rw	rw	rw	rw	rw		rw

Bit field	Name	Description
15	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use ETR or the inversion of ETR. 0: ETR active at high level or rising edge. 1: ETR active at low level or falling edge.
14	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable.

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Bit field	Name	Description
		Note 1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF. *Note 2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
13:12	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
11:8	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
7	MSMD	Master/ Slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.
6:4	TSEL[2:0]	Trigger selection

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Bit field	Name	Description
		These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: TI1 edge detector (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1(TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External triggered Input (ETRF) For more details on ITRx, see Table 10-3 below. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*
3	Reserved	Reserved, the reset value must be maintained
2:0	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*

Table 10-3 TIMx internal trigger connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM5	TIM2	TIM3	TIM4
TIM8	TIM1	TIM2	TIM4	TIM5

10.4.5 DMA/Interrupt enable registers (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TDEN	COMDEN	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	BIEN	TIEN	COMIEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	Reserved	Reserved, the reset value must be maintained
14	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
13	COMDEN	COM DMA request enable 0: Disable COM DMA request 1: Enable COM DMA request
12	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
11	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
10	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
9	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
8	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
7	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
6	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
5	COMIEN	COM interrupt enable 0: Disable COM interrupt 1: Enable COM interrupt
4	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
3	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
2	CC2IEN	Capture/Compare 2 interrupt enable

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Bit field	Name	Description
		0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
1	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

10.4.6 Status registers (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000 0000

31–18	17	16
Reserved	CC6ITF	CC5ITF
	rc_w0	rc_w0

15–13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved	BITF	TITF	COMITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	rc_w0	rc_w0	rc_w0	rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit field	Name	Description
31：18	Reserved	Reserved, the reset value must be maintained
17	CC6ITF	Capture/Compare 6 interrupt flag See TIMx_STS.CC1ITF description.
16	CC5ITF	Capture/Compare 5 interrupt flag See TIMx_STS.CC1ITF description.
15：13	Reserved	Reserved, the reset value must be maintained
12	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
11	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
10	CC2OCF	Capture/Compare 2 overcapture flags See TIMx_STS.CC1OCF description.
9	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
8	Reserved	Reserved, the reset value must be maintained
7	BITF	Break interrupt flag

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Bit field	Name	Description
		This bit is set by hardware once the brake input is active. This bit is cleared by software when the brake input becomes inactive. 0: No break event occurred 1: An active level has been detected
6	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred 1: Trigger interrupt occurred
5	COMITF	COM interrupt flag This bit is set by hardware once a COM event is generated (when TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_CCMOD1.OCxMD have been updated). This bit is cleared by software. 0: No COM event occurred 1: COM interrupt pending
4	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.
3	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
2	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
1	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions:

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Bit field	Name	Description
		– When TIMx_CTRL1.UPDIS = 0, and repeat counter value overflow or underflow (An update event is generated when the repeat counter equals 0). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

10.4.7 Event generation registers (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0x0000

15–8	7	6	5	4	3	2	1	0
Reserved	BGN	TGN	CCUDGN	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	w	w	w	w	w	w	w	w

Bit field	Name	Description
15：8	Reserved	Reserved, the reset value must be maintained
7	BGN	Break generation This bit can generate a brake event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a break event
6	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
5	CCUDGN	Capture/Compare control update generation This bit is set by software. And if TIMx_CTRL2.CCPCTL = 1 at this time, the CCxEN, CCxNEN and OCxMD bits are allowed to be updated. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event *Note: This bit is only valid for channels with complementary outputs.*
4	CC4GN	Capture/Compare 4 generation

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Bit field	Name	Description
		See TIMx_EVTGEN.CC1GN description.
3	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
2	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
1	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. When the corresponding channel of CC1 is in output mode: The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The TIMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event
0	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event

10.4.8 Capture/compare mode register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

15	14 12	11	10	9 8	7	6 4	3	2	1 0
OC2CEN	OC2M[2:0]	OC2PEN	OC2FEN	CC2SEL[1:0]	OC1CEN	OC1M[2:0]	OC1PEN	OC1FEN	CC1SEL[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	OC2CEN	Output Compare 2 clear enable

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Bit field	Name	Description
14:12	OC2MD[2:0]	Output Compare 2 mode
11	OC2PEN	Output Compare 2 preload enable
10	OC2FEN	Output Compare 2 fast enable
9:8	CC2SEL[1:0]	Capture/compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by ETRF input level 1: OC1REF is cleared immediately when the ETRF input level is detected as high
6:4	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
3	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into

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Bit field	Name	Description
		the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
2	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
1：0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:

15–12	11–10	9–8	7–4	3–2	1–0
IC2F[3:0]	IC2PSC[1:0]	CC2SEL[1:0]	IC1F[3:0]	IC1PSC[1:0]	CC1SEL[1:0]
rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15:12	IC2F[3:0]	Input Capture 2 Filter
11:10	IC2PSC[1:0]	Input Capture 2 Prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input Capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2

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Bit field	Name	Description
		0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

10.4.9 Capture/compare mode register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000

See the description of the CCMOD1 register above

Output comparison mode:

15	14 12	11	10	9 8	7	6 4	3	2	1 0
OC4CEN	OC4MD[2:0]	OC4PEN	OC4FEN	CC4SEL[1:0]	OC3CEN	OC3MD[2:0]	OC3PEN	OC3FEN	CC3SEL[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
15	OC4CEN	Output compare 4 clear enable
14:12	OC4MD[2:0]	Output compare 4 mode
11	OC4PEN	Output compare 4 preload enable
10	OC4FEN	Output compare 4 fast enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7	OC3CEN	Output compare 3 clear enable
6:4	OC3MD[2:0]	Output compare 3 mode
3	OC3PEN	Output compare 3 preload enable
2	OC3FEN	Output compare 3 fast enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

15–12	11–10	9–8	7–4	3–2	1–0
IC4F[3:0]	IC4PSC[1:0]	CC4SEL[1:0]	IC3F[3:0]	IC3PSC[1:0]	CC3SEL[1:0]
rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15:12	IC4F[3:0]	Input Capture 4 filter
11:10	IC4PSC[1:0]	Input Capture 4 Prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input Capture 3 filter

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Bit field	Name	Description
3:2	IC3PSC[1:0]	Input Capture 3 Prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

10.4.10 Capture/compare enable registers (TIMx_CCEN)

Offset address: 0x20

Reset value: 0x0000 0000

31–22	21	20	19–18	17	16
Reserved	CC6P	CC6EN	Reserved	CC5P	CC5EN
	rw	rw		rw	rw

15–14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CC4P	CC4EN	CC3NP	CC3NEN	CC3P	CC3EN	CC2NP	CC2NEN	CC2P	CC2EN	CC1NP	CC1NEN	CC1P	CC1EN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	CC6P	Capture/Compare 6 output polarity See TIMx_CCEN.CC1P description.
20	CC6EN	Capture/Compare 6 output enable See TIMx_CCEN.CC1EN description.
19：18	Reserved	Reserved, the reset value must be maintained
17	CC5P	Capture/Compare 5 output polarity See TIMx_CCEN.CC1P description.
16	CC5EN	Capture/Compare 5 output enable See TIMx_CCEN.CC1EN description.
15:14	Reserved	Reserved, the reset value must be maintained
13	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
12	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
11	CC3NP	Capture/Compare 3 Complementary output polarity See TIMx_CCEN.CC1NP description.
10	CC3NEN	Capture/Compare 3 complementary output enable See TIMx_CCEN.CC1NEN description.

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Bit field	Name	Description
9	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
8	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
7	CC2NP	Capture/Compare 2 complementary output polarity See TIMx_CCEN.CC1NP description.
6	CC2NEN	Capture/Compare 2 complementary output enable See TIMx_CCEN.CC1NEN description.
5	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
4	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
3	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N active high 1: OC1N active low
2	CC1NEN	Capture/Compare 1 complementary output enable 0: Disable - Disable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN. 1: Enable - Enable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN.
1	CC1P	Capture/Compare 1 output polarity When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low When the corresponding channel of CC1 is in input mode: At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted.
0	CC1EN	Capture/Compare 1 output enable When the corresponding channel of CC1 is in output mode: 0: Disable - Disable output OC1 signal. The level of OC1 depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. 1: Enable - Enable output OC1 signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN.

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Bit field	Name	Description
		When the corresponding channel of CC1 is in input mode: At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture

Table 10-4 Output control bits of complementary OCx and OCxN channels with break function

Control bits					Output state[1)]	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output state	OCxN Output state
1	X	0	0	0	Output disabled（not driven by timer） OCx=0，OCx_EN=0	Output disabled（not driven by timer） OCxN=0，OCxN_EN=0
		0	0	1	Output disabled（not driven by timer） OCx=0，OCx_EN=0	OCxREF + polarity， OCxN= OCxREF xor CCxNP，OCxN_EN=1
		0	1	0	OCxREF + polarity， OCx= OCxREF xor CCxP，OCx_EN=1	Output disabled（not driven by timer） OCxN=0，OCxN_EN=0
		0	1	1	OCxREF + polarity + dead-time， OCx_EN=1	Complementary to OCxREF + polarity + dead-time，OCxN_EN=1
		1	0	0	Output disabled（not driven by timer） OCx=CCxP，OCx_EN=0	Output disabled（not driven by timer） OCxN=CCxNP，OCxN_EN=0
		1	0	1	Off-state (Output enabled with inactive state) OCx=CCxP，OCx_EN=1	OCxREF + polarity， OCxN= OCxREF xor CCxNP，OCxN_EN=1
		1	1	0	OCxREF + polarity， OCx= OCxREF xor CCxP， OCx_EN=1	Off-state (Output enabled with inactive state) OCxN=CCxNP，OCxN_EN=1
		1	1	1	OCxREF + polarity + dead-time， OCx_EN=1	Complementary to OCxREF + polarity + dead-time， OCxN_EN=1
0	0	X	0	0	Output disabled（not driven by timer） Asynchronously： OCx=CCxP， OCx_EN=0， OCxN=CCxNP，OCxN_EN=0； Then if the clock is present：OCx=OIx and OCxN=OIxN after a dead-time, when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0.	
	0		0	1		
	0		1	0		
	0		1	1		
	1		0	0	Off-state (Output enabled with inactive state) Asynchronously： OCx=CCxP， OCx_EN=1， OCxN=CCxNP，OCxN_EN=1； Then if the clock is present：OCx=OIx and OCxN=OIxN after a dead-time, when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0	
	1		0	1		
	1		1	0		
	1		1	1		

1. If both outputs of a channel are not used (CCxEN = CCxNEN = 0), OIx, OIxN, CCxP and CCxNP must all be cleared.

Note: The status of external I/O pins connected to complementary OCx and OCxN channels depends on the OCx and OCxN channel states and GPIO and AFIO registers.

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10.4.11 Counters (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

15 … 0
CNT[15:0]
rw

Bit field	Name	Description
15:0	CNT[15:0]	Counter value

10.4.12 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

15 … 0
PSC[15:0]
rw

Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}$/ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

10.4.13 Auto-reload register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF

15 … 0
AR[15:0]
rw

Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See Section 10.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

10.4.14 Repeat count registers (TIMx_REPCNT)

Offset address: 0x30

Reset value: 0x0000

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15		8	7		0
Reserved			REPCNT[7:0]		
			rw		

Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value Repetition counter is used to generate the update event or update the timer registers only after a given number (N+1) cycles of the counter, where N is the value of TIMx_REPCNT.REPCNT . The repetition counter is decremented at each counter overflow in up-counting mode, at each counter underflow in down-counting mode or at each counter overflow and at each counter underflow in center-aligned mode. Setting the TIMx_EVTGEN.UDGN bit will reload the content of TIMx_REPCNT.REPCNT and generate an update event.

10.4.15 Capture/compare register 1 (TIMx_CCDAT1)

Offset address: 0x34

Reset value: 0x0000

15	0
CCDAT1[15:0]	
rw/r	

Bit field	Name	Description
15:0	CCDAT1[15:0]	Capture/Compare 1 value ■ CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 and CCDDAT1 are only readable. When configured as output mode, register CCDAT1 and CCDDAT1 are readable and writable.

10.4.16 Capture/compare register 2 (TIMx_CCDAT2)

Offset address: 0x38

Reset value: 0x0000

15	0
CCDAT2[15:0]	
rw/r	

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Bit field	Name	Description
15:0	CCDAT2[15:0]	Capture/Compare 2 values ■ CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 and CCDDAT2 are only readable. When configured as output mode, register CCDAT2 and CCDDAT2 are readable and writable.

10.4.17 Capture/compare register 3 (TIMx_CCDAT3)

Offset address: 0x3C

Reset value: 0x0000

15 … 0
CCDAT3[15:0]
rw/r

Bit field	Name	Description
15:0	CCDAT3[15:0]	Capture/Compare 3 value ■ CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 and CCDDAT3 are only readable. When configured as output mode, register CCDAT3 and CCDDAT3 are readable and writable.

10.4.18 Capture/compare register 4 (TIMx_CCDAT4)

Offset address: 0x40

Reset value: 0x0000

15 … 0
CCDAT4[15:0]
rw/r

Bit field	Name	Description

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15:0	CCDAT4[15:0]	Capture/Compare 4 value ■ CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 and CCDDAT4 are only readable. When configured as output mode, register CCDAT4 and CCDDAT4 are readable and writable.

10.4.19 Break and Dead-time registers (TIMx_BKDT)

Offset address: 0x44

Reset value: 0x0000

15	14	13	12	11	10	9-8	7-0
MOEN	AOEN	BKP	BKEN	OSSR	OSSI	LCKCFG[1:0]	DTGN[7:0]
rw	rw	rw	rw	rw	rw	rw	rw

Note: AOEN, BKP, BKEN, OSSI, OSSR, and DTGN [7:0] bits can all be write protected depending on the LOCK configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit field	Name	Description
15	MOEN	Main Output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the brake input is active. It is only valid for channels configured as outputs. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set. For more details, see Section 10.4.10 Capture/Compare enable registers (TIMx_CCEN).
14	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.
13	BKP	Break input polarity 0: Low level of the brake input is valid 1: High level of the brake input is valid *Note: Any write to this bit requires an APB clock delay to take effect.*
12	BKEN	Break enable 0: Disable brake input (BRK and CCS clock failure events) 1: Enable brake input (BRK and CCS clock failure events) *Note: Any write to this bit requires an APB clock delay to take effect.*

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Bit field	Name	Description
11	OSSR	Off-state Selection for Run Mode This bit is used when TIMx_BKDT.MOEN=1 and the channel is a complementary output. The OSSR bit does not exist in timer without complementary outputs. 0: When inactive, OCx/OCxN outputs are disabled (OCx/OCxN enable output signal=0). 1: When inactive, OCx/OCxN outputs are enabled with their inactive level as soon as CCxEN=1 or CCxNEN=1. Then, OCx/OCxN enable output signal=1 For more details, See Section 10.4.10, capture/compare enablement registers (TIMx_CCEN).
10	OSSI	Off-state Selection for Idle Mode This bit is used when TIMx_BKDT.MOEN=0 and the channels configured as outputs. 0: When inactive, OCx/OCxN outputs are disabled (OCx/OCxN enable output signal=0). 1: When inactive, OCx/OCxN outputs are enabled with their idle level as soon as CCxEN=1 or CCxNEN=1. Then, OCx/OCxN enable output signal=1 For more details, See Section 10.4.10, capture/compare enablement registers (TIMx_CCEN).
9:8	LCKCFG[1:0]	Lock Configuration These bits offer a write protection against software errors. 00: – No write protected. 01: – LOCK Level 1 TIMx_BKDT.DTGN, TIMx_BKDT.BKEN, TIMx_BKDT.BKP, TIMx_BKDT.AOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN bits enable write protection. 10: – LOCK Level 2 Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection. 11: – LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: After the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*
7:0	DTGN [7:0]	Dead-time Generator These bits define the dead-time duration between inserted complementary outputs. The relationship between the DTGN value and the dead time is as follows:: DTGN[7:5] = 0xx: dead time = DTGN[7:0] ×(t_{DTS}) DTGN[7:5] = 10x: dead time =(64+DTGN[5:0]) ×(2 ×t_{DTS}) DTGN[7:5]=110:

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Bit field	Name	Description
		dead time =(32+DTGN[4:0]) ×(8 × t_{DTS}) DTGN [then] = 111: dead time = (32 + DTGN [4:0]) ×(16 × t_{DTS}) t_{DTS} value see TIMx_CTRL1.CLKD [1:0].

10.4.20 DMA Control register (TIMx_DCTRL)

Offset address: 0x48

Reset value: 0x0000

15 - 13	12 - 8	7 - 5	4 - 0
Reserved	DBLEN[4:0]	Reserved	DBADDR[4:0]
	rw		rw

Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained, kept at 0.
12:8	DBLEN[4:0]	DMA Burst Length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 00000:1 time transfer 00001: 2 times transfers 00010: 3 times transfers … 10001: 18 times transfers
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	DBADDR[4:0]	DMA Base Address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 00000: TIMx_CTRL1, 00001: TIMx_CTRL2, 00010: TIMx_SMCTRL, … 10001：TIMx_BKDT, 10010：TIMx_DCTRL

10.4.21 DMA transfer buffer register (TIMx_DADDR)

Offset address: 0x4C

Reset value: 0x0000

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15															0
BURST[15:0]															
rw															

Bit field	Name	Description
15:0	BURST[15:0]	DMA access buffer. When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

10.4.22 Capture/compare mode registers 3(TIMx_CCMOD3)

Offset address: 0x54

Reset value: 0x0000

15	14:12	11	10	9:8	7	6:4	3	2	1:0
OC6CEN	OC6MD[2:0]	OC6PEN	OC6FEN	Reserved	OC5CEN	OC5MD[2:0]	OC5PEN	OC5FEN	Reserved
rw	rw	rw	rw		rw	rw	rw	rw	

Bit field	Name	Description
15	OC6CEN	Output compare 6 clear enable
14:12	OC6MD[2:0]	Output compare 6 mode
11	OC6PEN	Output compare 6 preload enable
10	OC6FEN	Output compare 6 fast enable
9:8	Reserved	Reserved, the reset value must be maintained
7	OC5CEN	Output compare 5 clear enable
6:4	OC5MD[2:0]	Output compare 5 mode
3	OC5PEN	Output compare 5 Preload enable
2	OC5FEN	Output compare 5 fast enable
1：0	Reserved	Reserved, the reset value must be maintained

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10.4.23 Capture/compare register 5 (TIMx_CCDAT5)

Offset address: 0x58

Reset value: 0x0000

15 ... 0
CCDAT5[15:0]
rw

Bit field	Name	Description
15:0	CCDAT5[15:0]	Capture/Compare 5 value ■ CC5 channel can only configured as output: CCDAT5 contains the value to be compared to the counter TIMx_CNT, signaling on the OC5 output. If the preload feature is not selected in TIMx_CCMOD3.OC5PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. TIM1_CC5 and TIM8_CC5 is used for comparator blanking.

10.4.24 Capture/compare register 6 (TIMx_CCDAT6)

Offset address: 0x5C

Reset value: 0x0000

15 ... 0
CCDAT6[15:0]
rw

Bit field	Name	Description
15:0	CCDAT6[15:0]	Capture/Compare 6 value ■ CC6 channel can only configured as output: CCDAT6 contains the value to be compared to the counter TIMx_CNT, signaling on the OC6 output. If the preload feature is not selected in TIMx_CCMOD3.OC6PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 can switch the input channel of OPAMP2

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11 General-purpose timers (TIM2, TIM3, TIM4, TIM5 and TIM9)

11.1 General-purpose timers introduction

The general-purpose timers (TIM2, TIM3, TIM4, TIM5 and TIM9) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

11.2 Main features of General-purpose timers

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4, TIM5 and TIM9 up to 4 channels.
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers are linked internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;
- Supports capture of internal comparator output signal. TIM9 supports capture of internal HSE, LSI, and LSE signal

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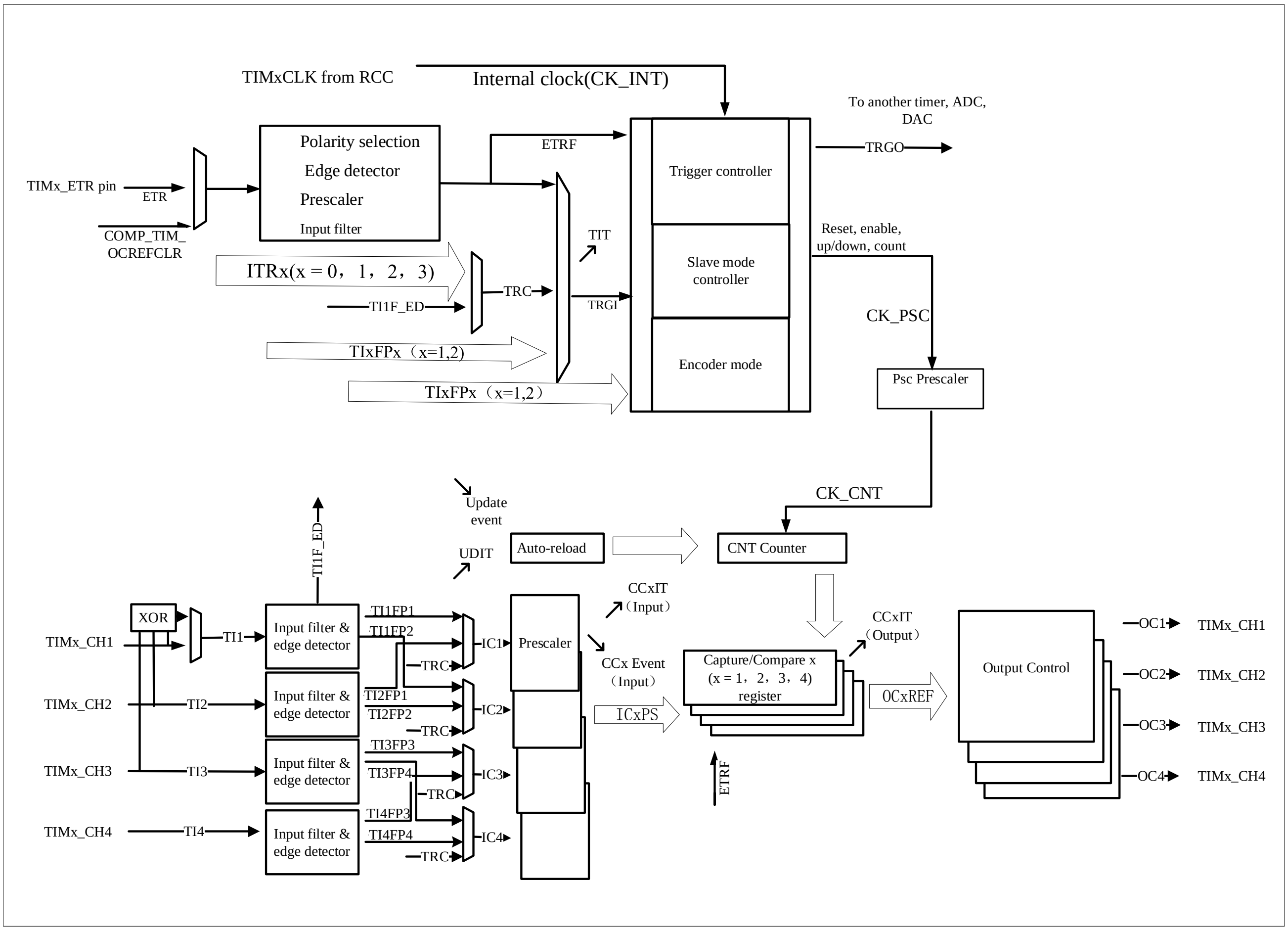
Figure 11-1 Block diagram of TIMx（x=2, 3 ,4 ,5 and 9）



↘ *The event* ↗ *Interrupt and DMA output*

For TIM4 and TIM5, ETR input is not support.

For TIMx（x = 2, 3, 4, 5 and 9）, The capture channel 1 input can come from IOM or comparator output

For TIM9, capture channel 2 comes from IOM or LSE, for TIM2, TIM3, TIM4 and TIM5, capture channel 2 comes from IOM only

For TIM9, capture channel 3 comes from IOM or LSI, for TIM2, TIM3, TIM4 and TIM5, capture channel 3 comes from IOM only

For TIM9, capture channel 4 comes from IOM or HSE, for TIM2, TIM3, TIM4 and TIM5, capture channel 4 comes from IOM only

11.3 General-purpose timers description

11.3.1 Time-base unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated

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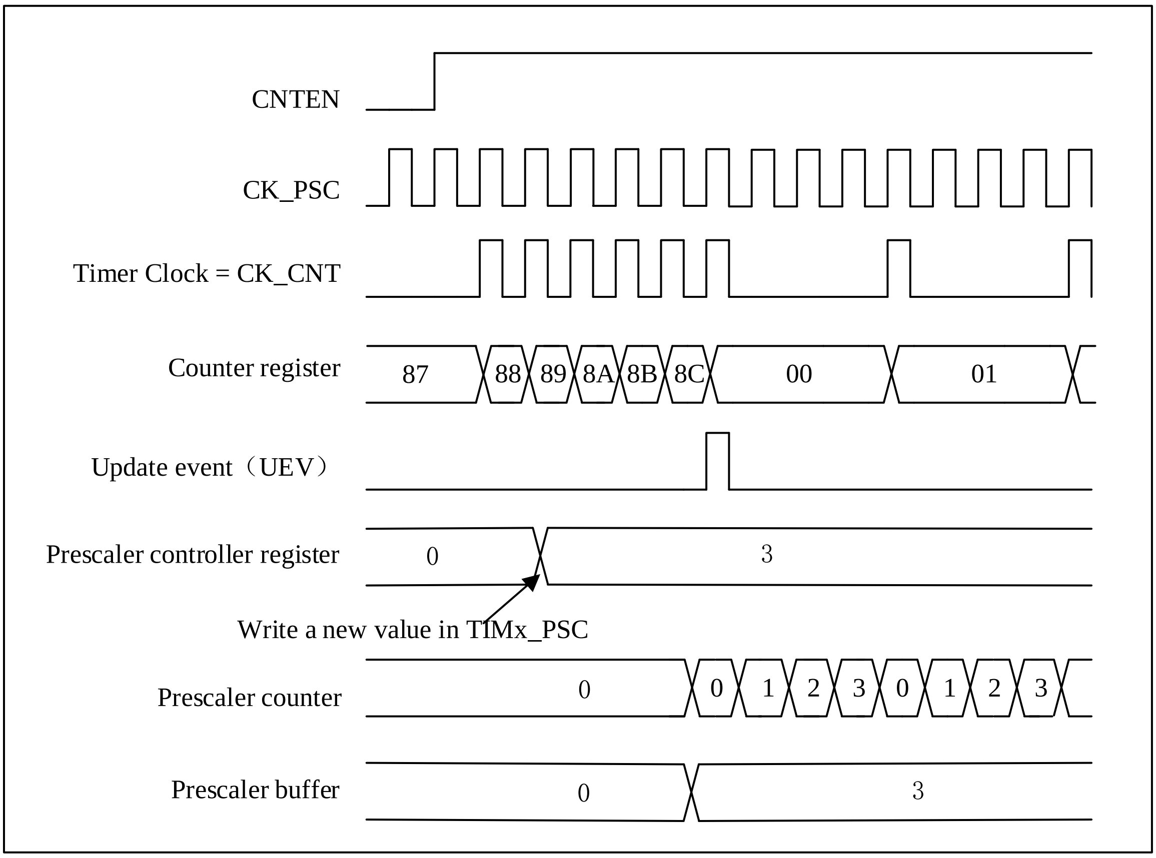
when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

11.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 11-2 Counter timing diagram with prescaler division change from 1 to 4



11.3.2 Counter mode

11.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs,

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TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

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Figure 11-3 Timing diagram of up-counting. The internal clock divider factor = 2/N

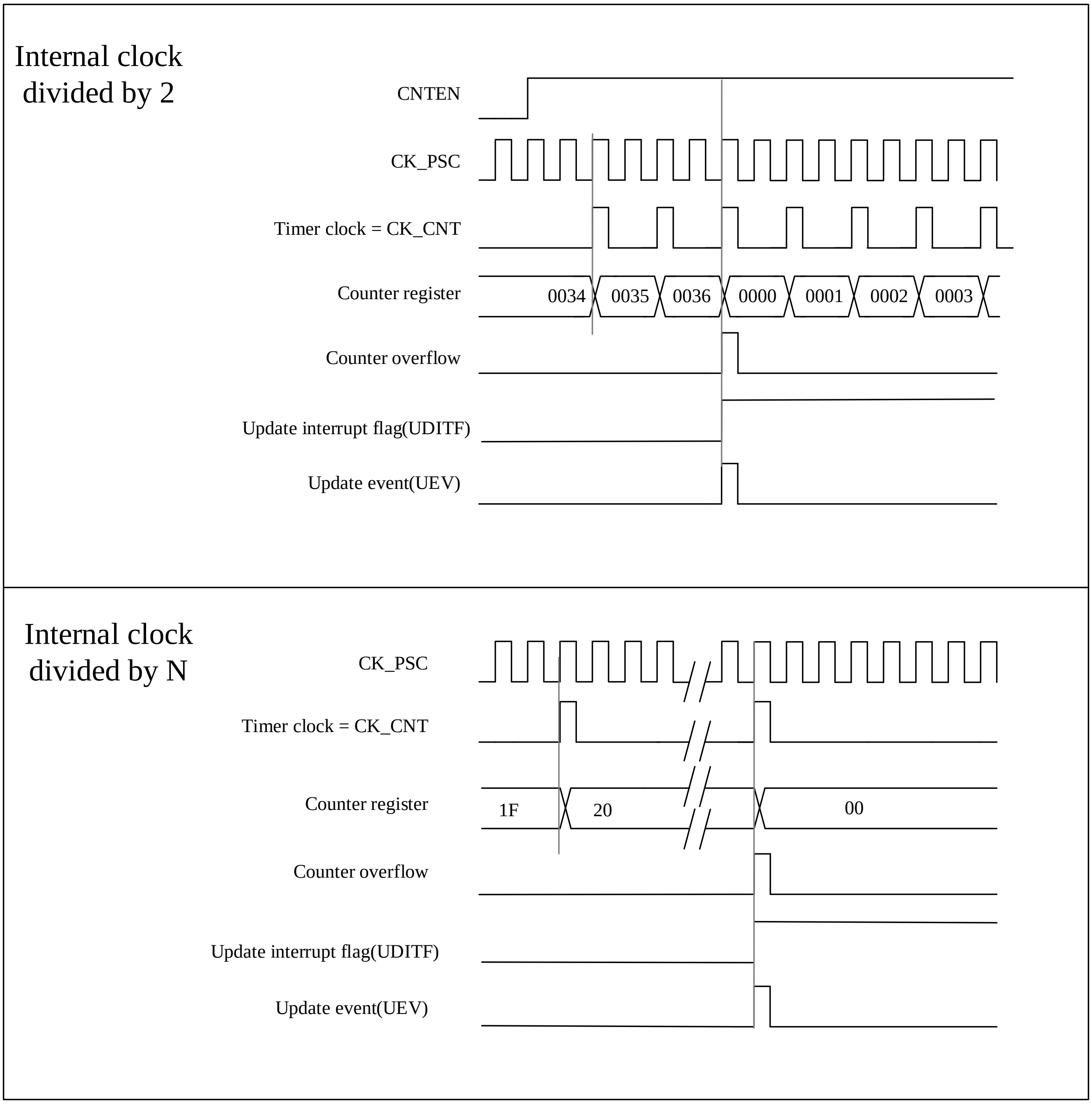

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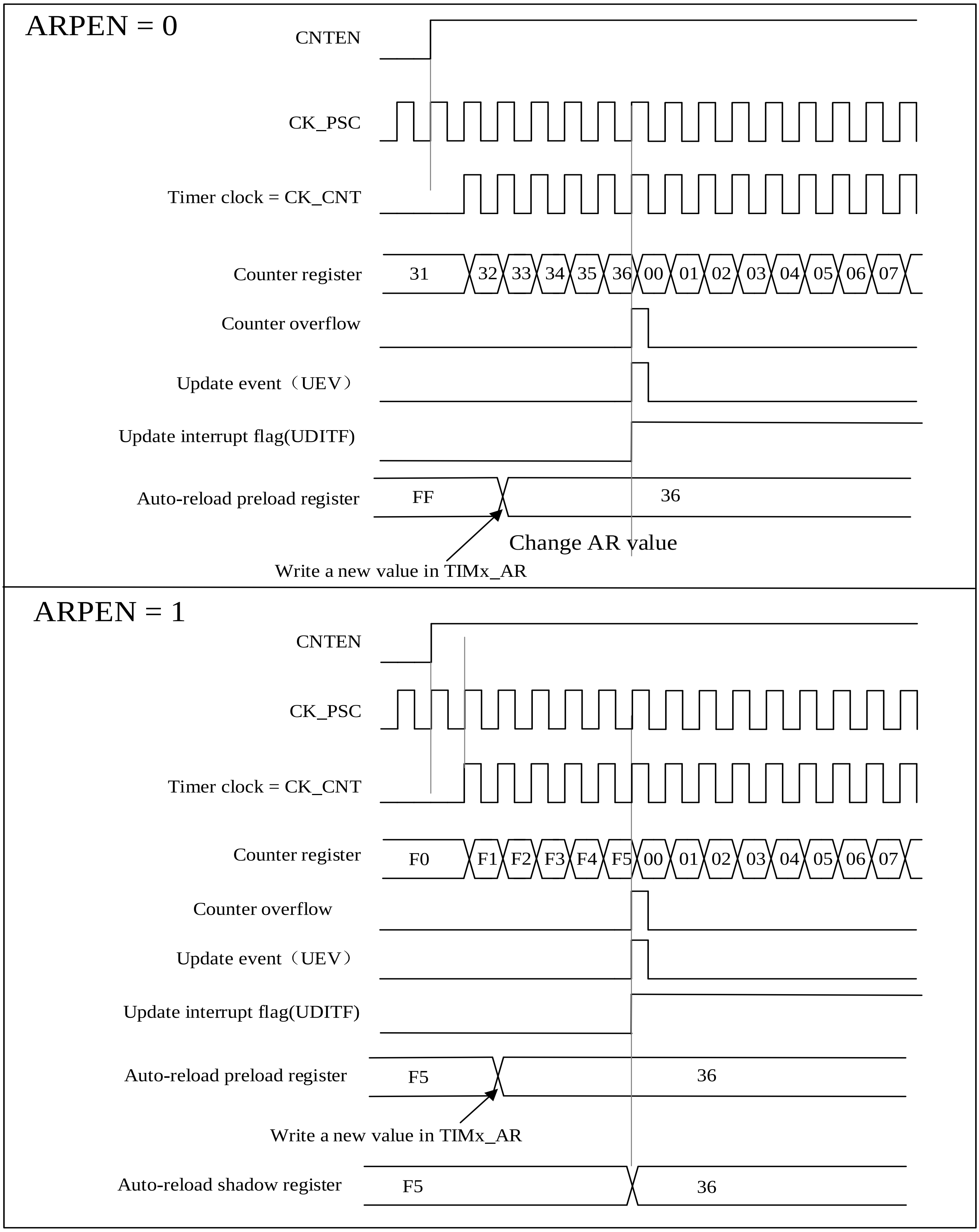
Figure 11-4 Timing diagram of the up-counting, update event when ARPEN=0/1



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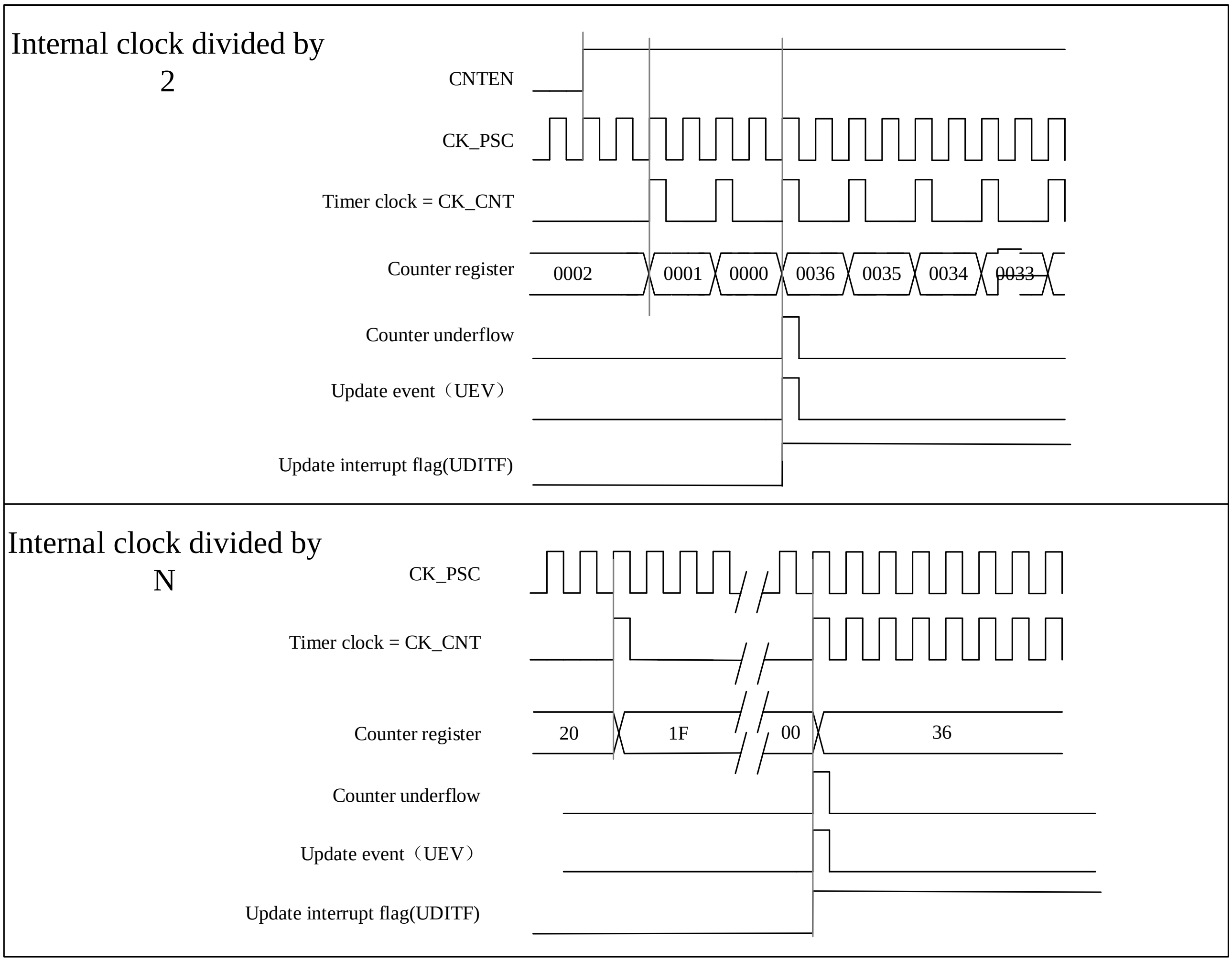
11.3.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see 11.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 11-5 Timing diagram of the down-counting, internal clock divided factor = 2/N



11.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

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The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Please note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 11-6 Timing diagram of the Center-aligned, internal clock divided factor =2/N

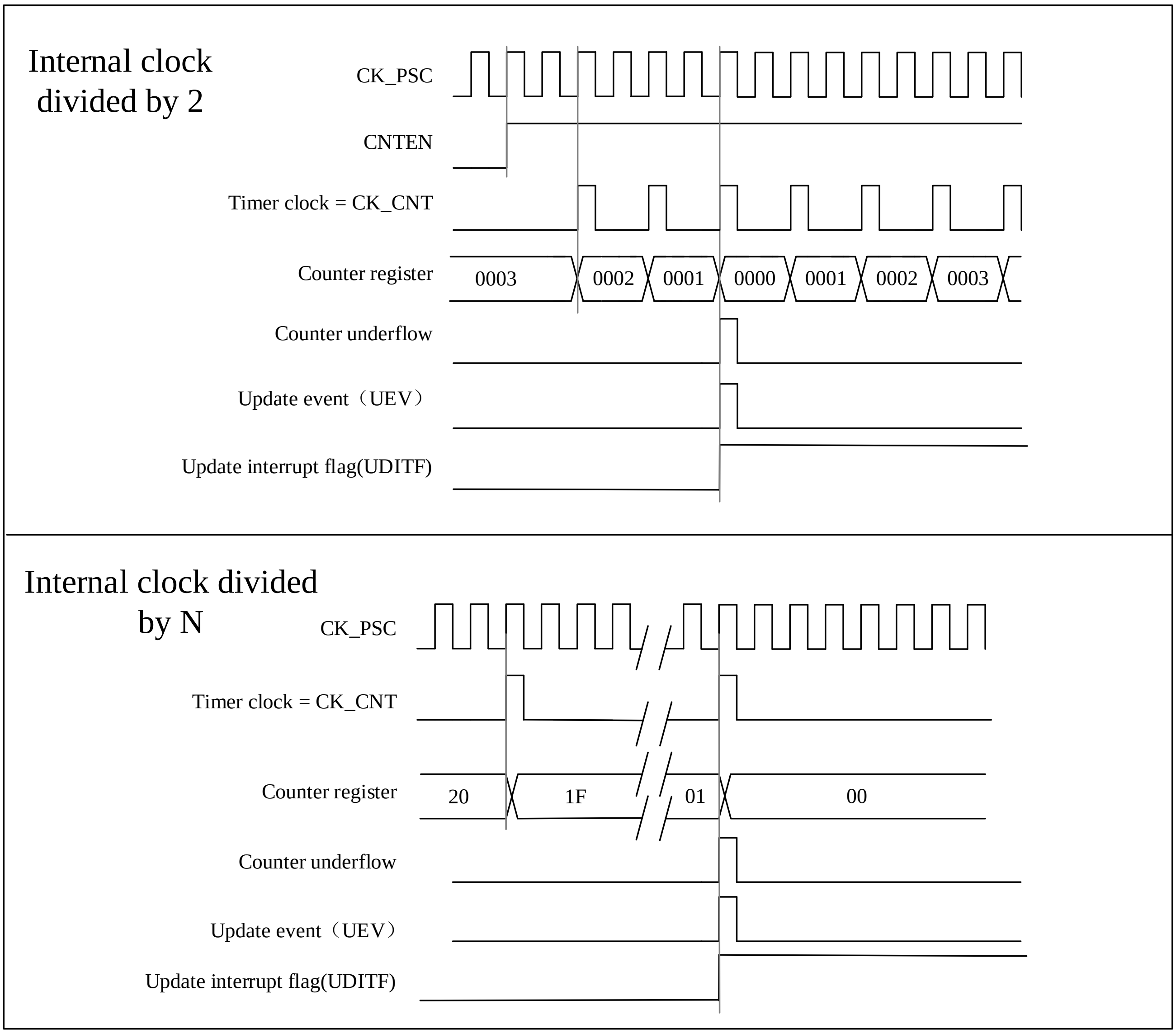

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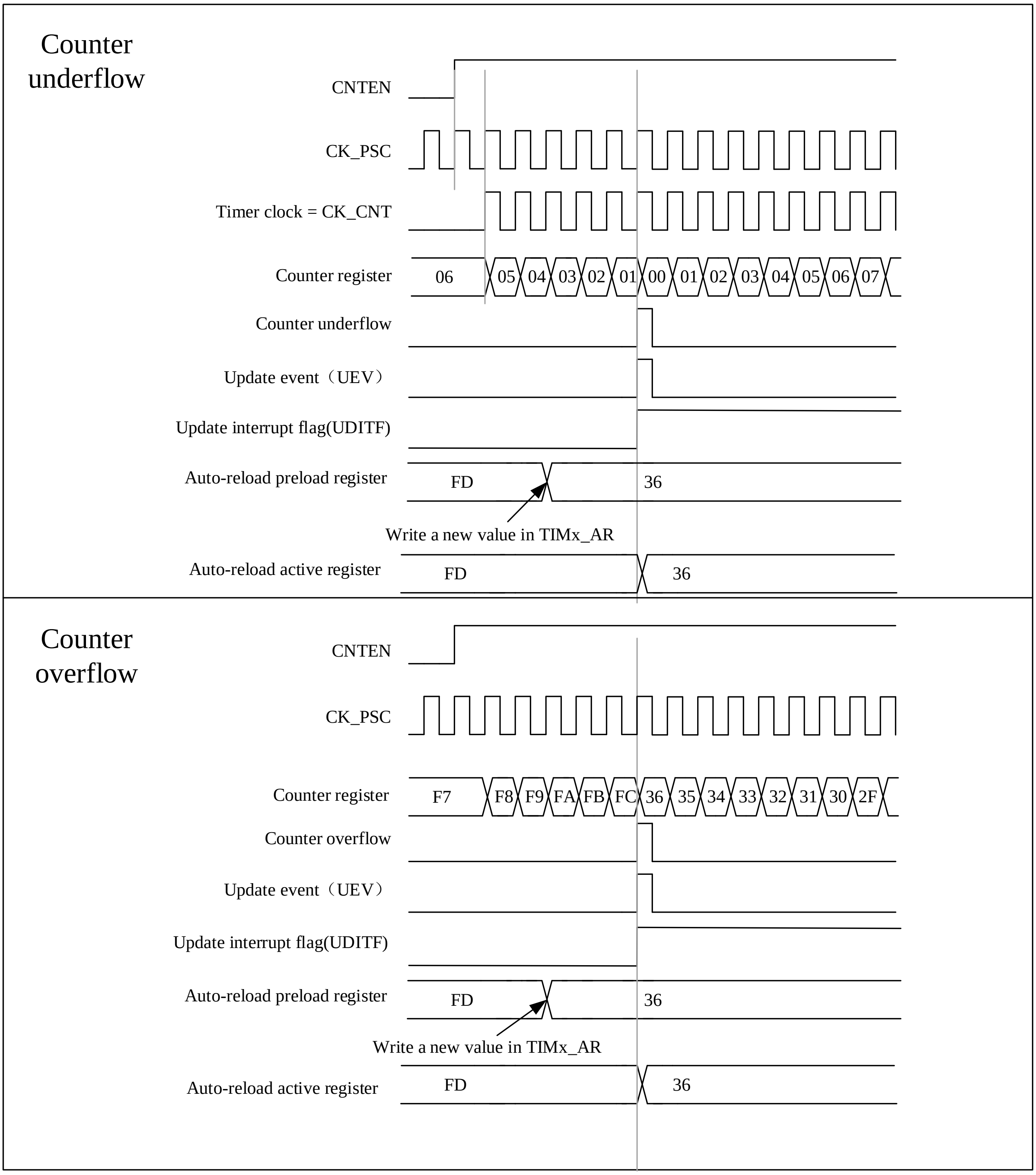
Figure 11-7 A center-aligned sequence diagram that includes counter overflows and underflows (ARPEN = 1)



11.3.3 Clock selection

- The internal clock of timers: CK_INT
- Two kinds of external clock mode :

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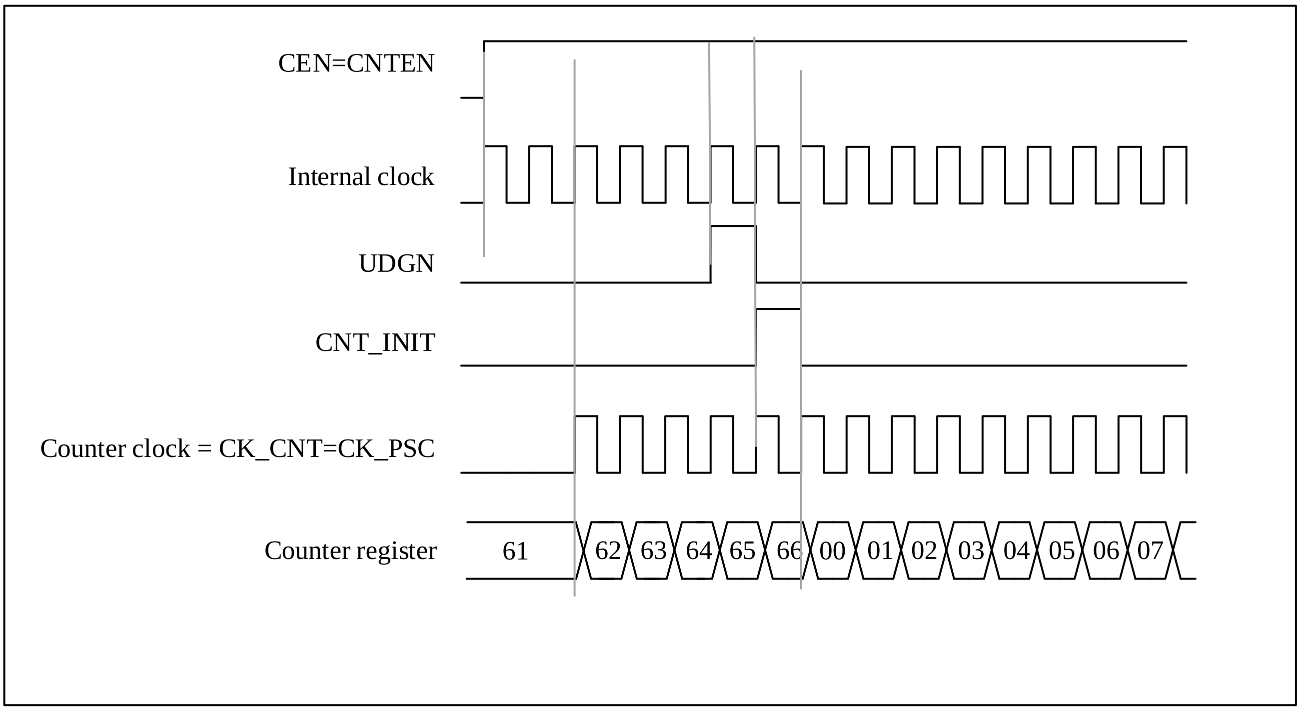
- external input pin
- external trigger input ETR

- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

11.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by soft, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 11-8 Control circuit in normal mode, internal clock divided by 1



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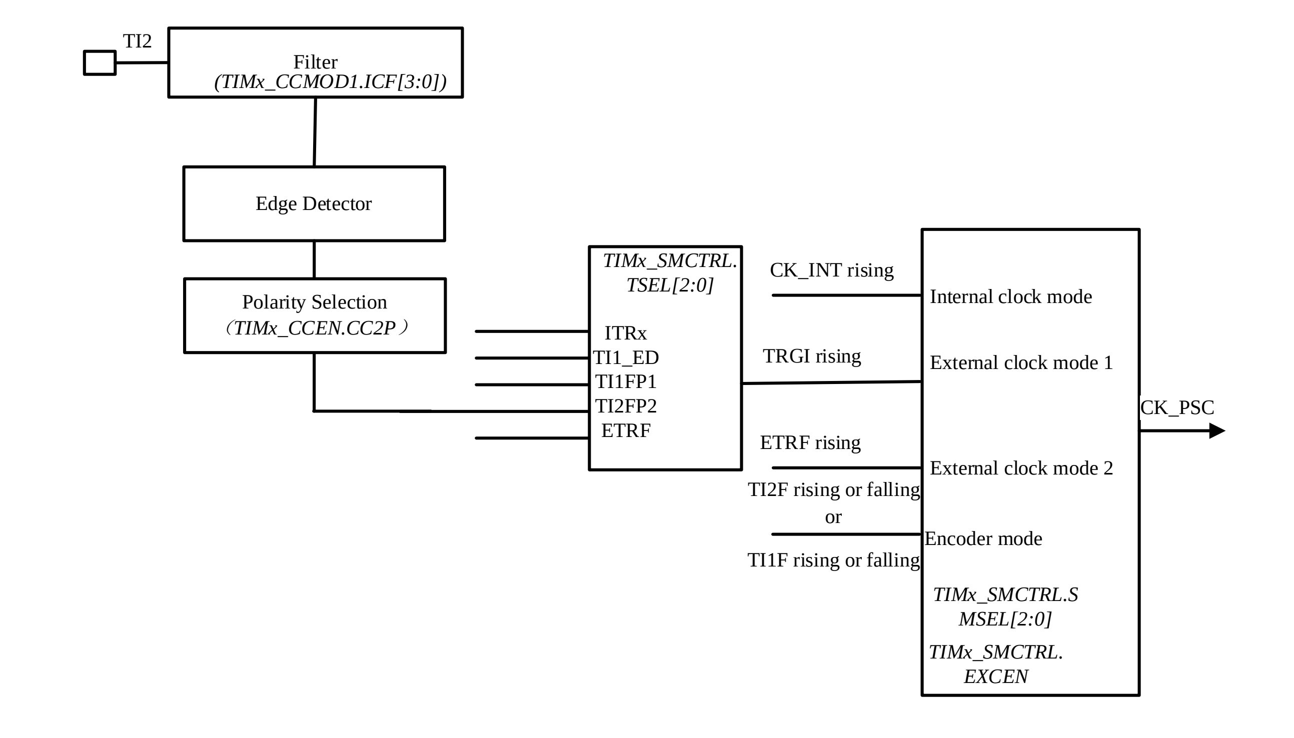
11.3.3.2 External clock source mode 1

Figure 11-9 TI2 external clock connection example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to ‘01’, CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to ‘0’, select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at ‘0000’)
- Configure TIMx_SMCTRL.SMSEL equal to ‘111’, select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to ‘110’, select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to ‘1’ to start the counter

Note: The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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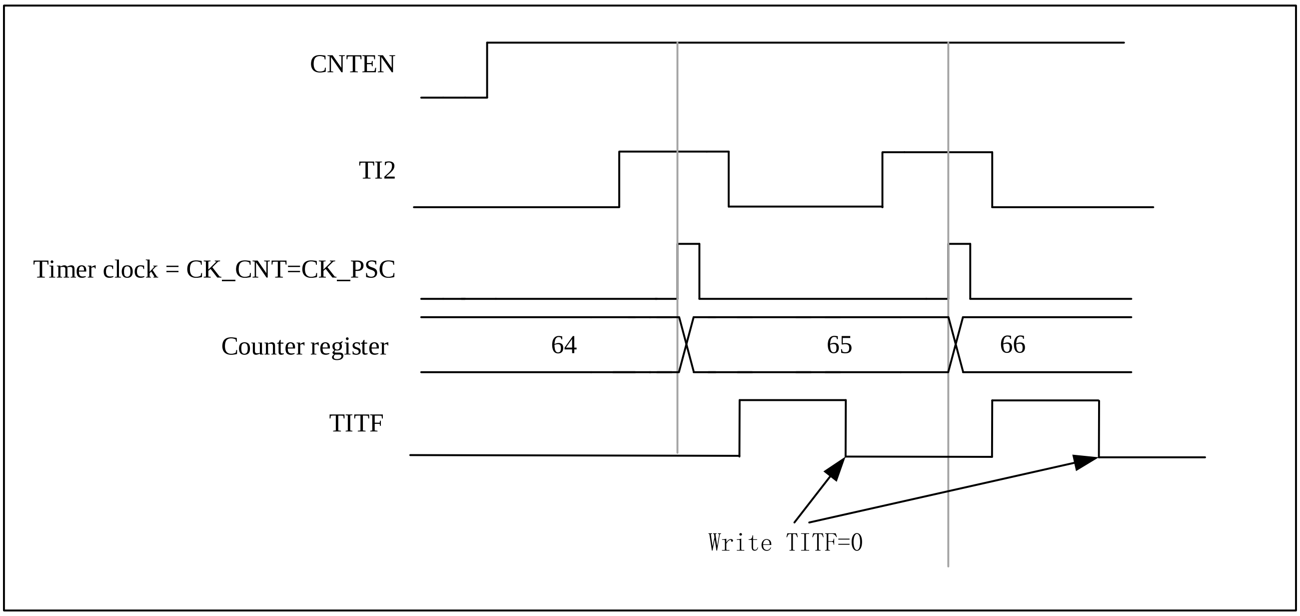
Figure 11-10 Control circuit in external clock mode 1

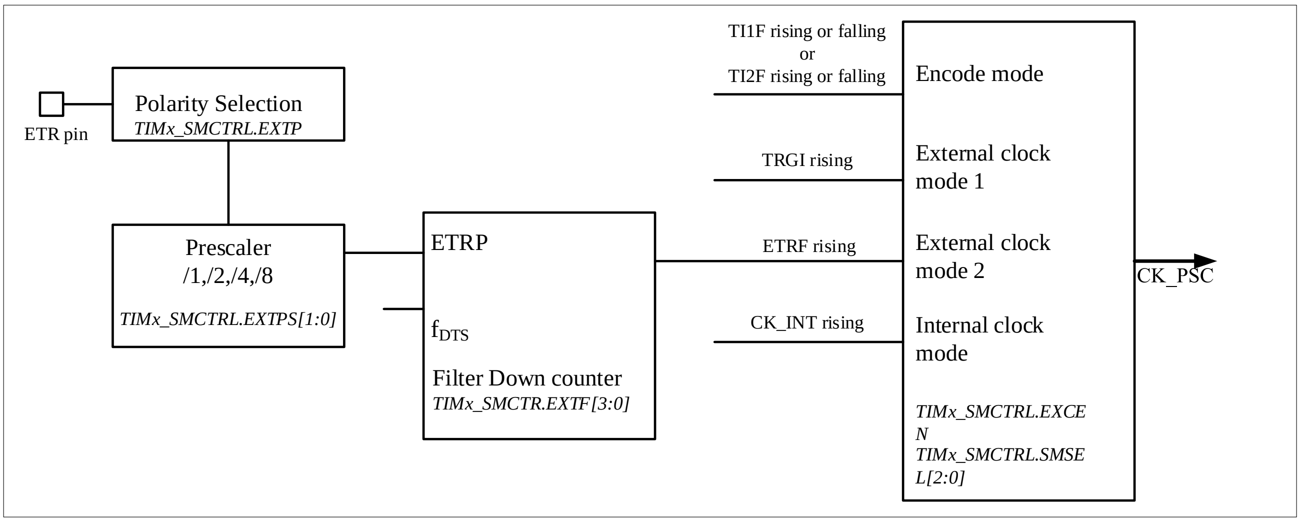


11.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 11-11 External trigger input block diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to ‘0000’
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to ‘01’
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to ‘0’, The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to ‘1’

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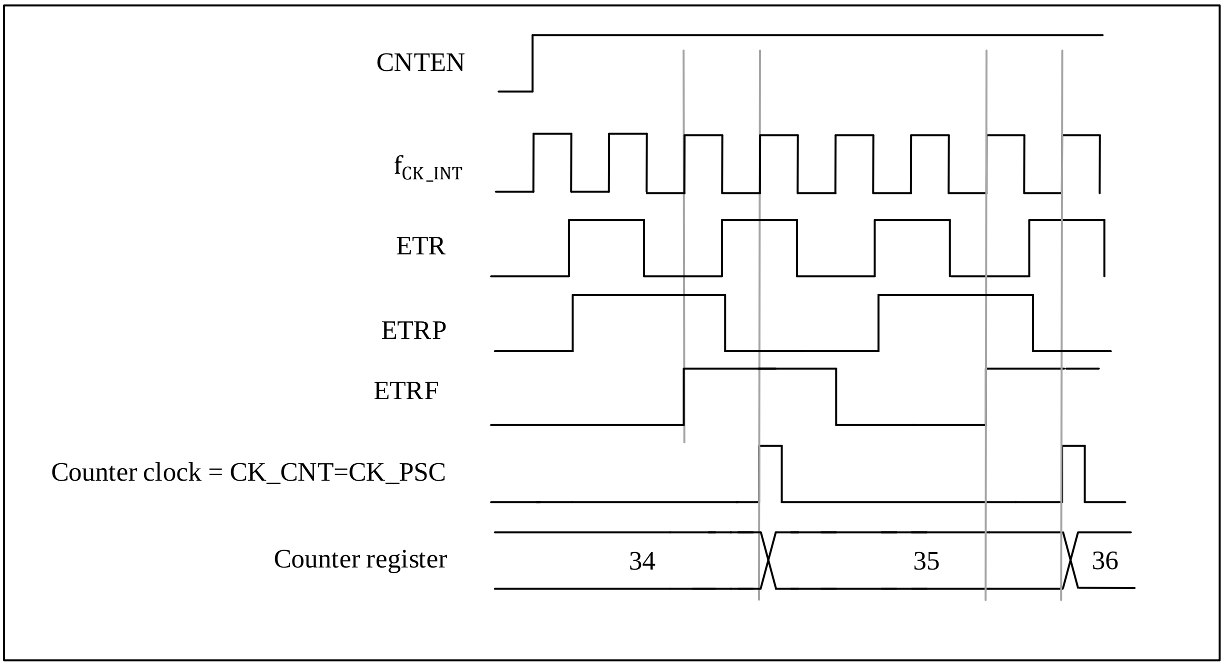
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 11-12 Control circuit in external clock mode 2



11.3.4 Capture/compare channels

Capture/compare channels include capture/compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequency division. The following figure shows a block diagram of a capture/compare channel.

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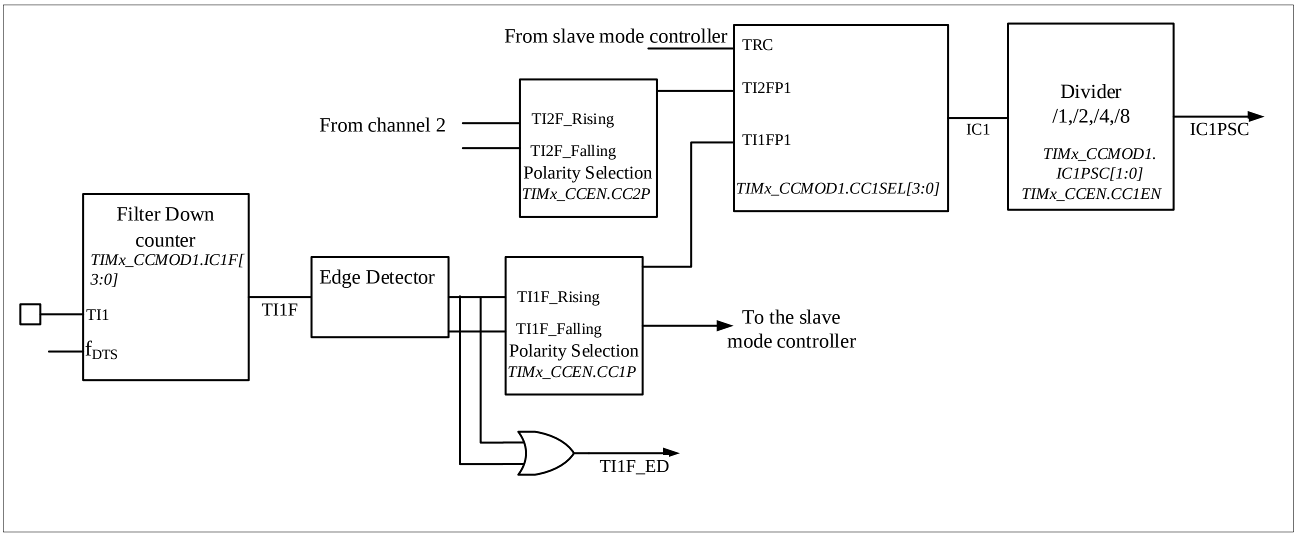
Figure 11-13 Capture/compare channel (example: channel 1 input stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 11-14 Capture/compare channel 1 main circuit

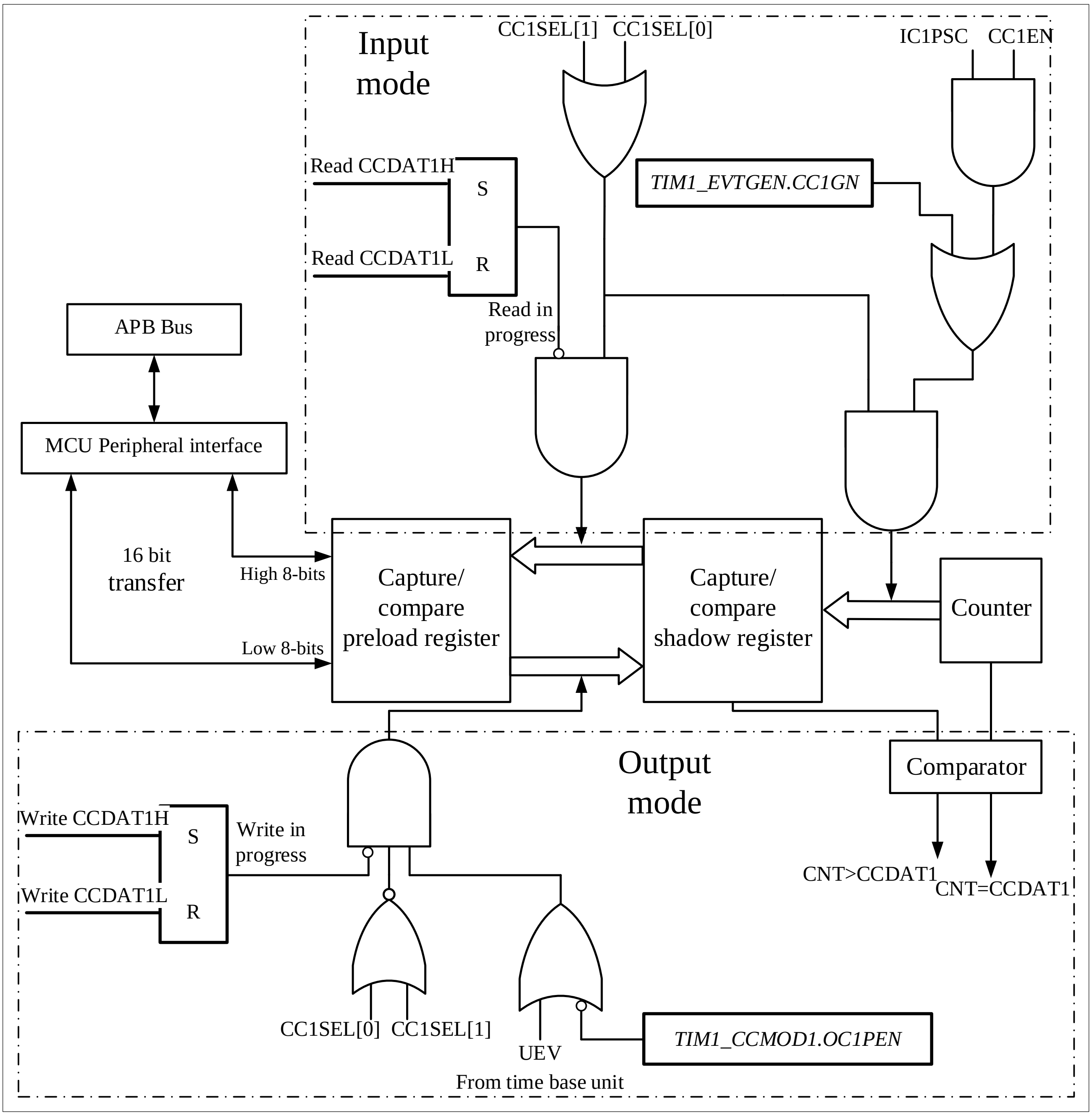

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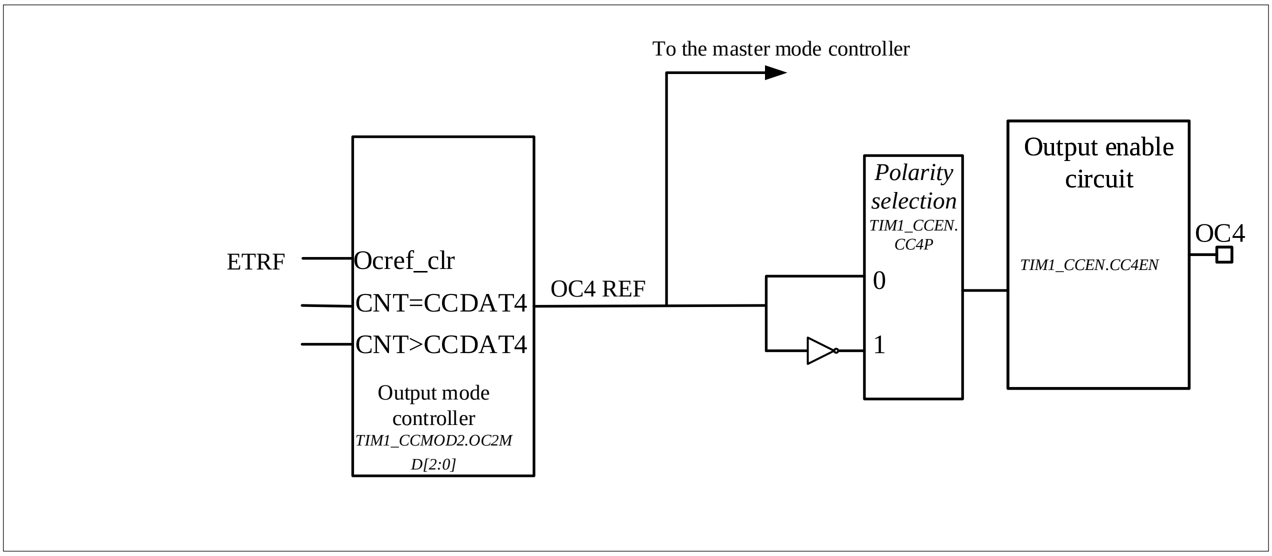
Figure 11-15 Output part of channelx （x = 1,2,3,4;take channel 4 as an example）



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

11.3.5 Input capture mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to ‘01’. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Program the desired input filter duration:

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Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to ‘0011’.

- By configuring TIMx_CCEN .CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= ‘00’ to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = ‘1’.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

11.3.6 PWM input mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to ‘01’ to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to ‘0’ to select the active polarity of filtered timer input 1(TI1FP1), valid on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to ‘10’ select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), valid on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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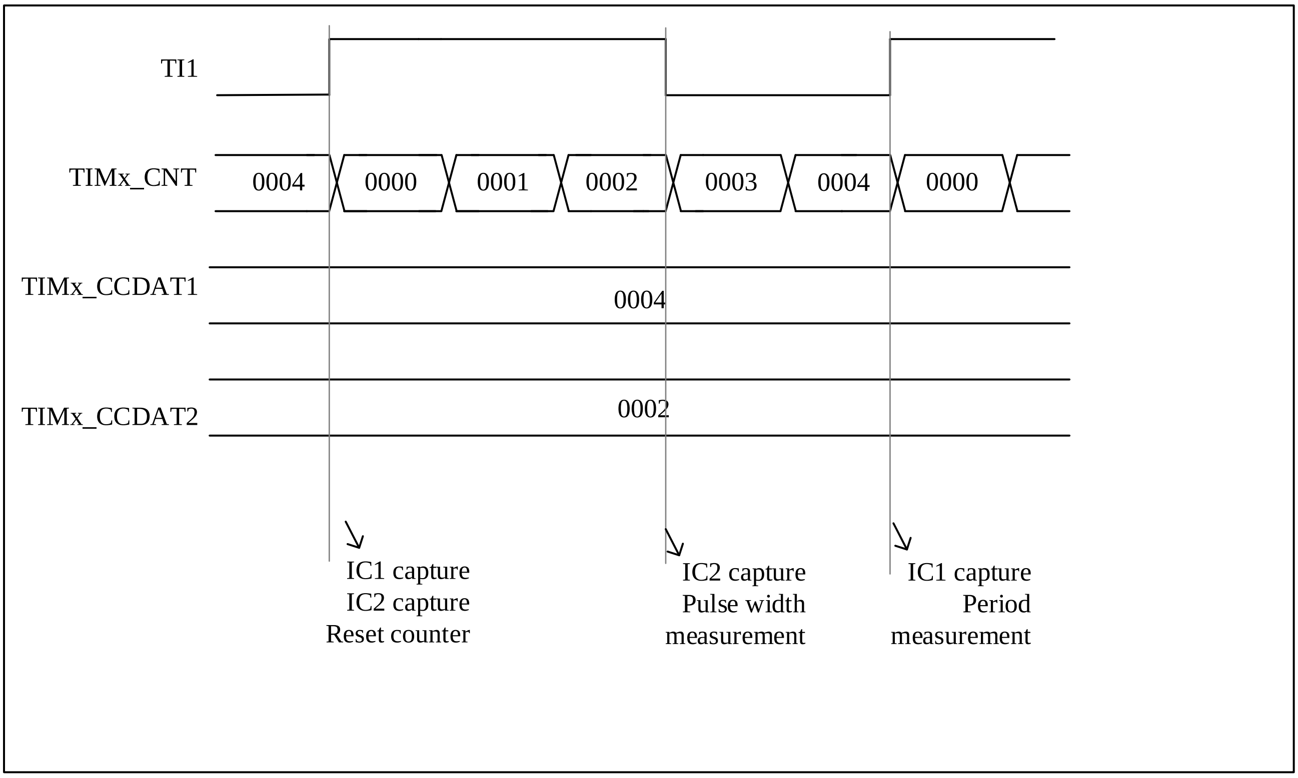
Figure 11-16 PWM input mode timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

11.3.7 Forced output mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

11.3.8 Output compare mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When

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the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers(TIMx_CCDATx) or not.

The time resolution is one count of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse.

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with desired data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

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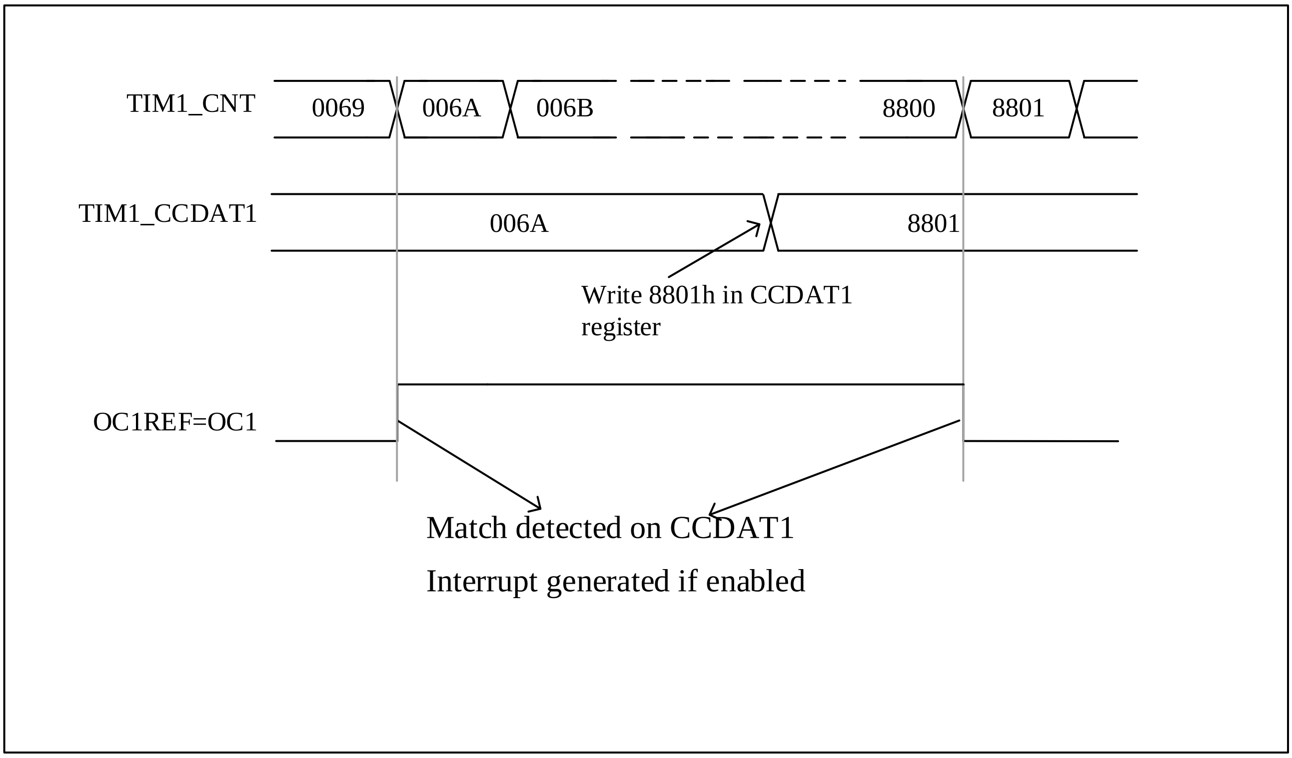
Figure 11-17 Output compare mode, toggle on OC1



11.3.9 PWM mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. To enable the output of OCx, user need to set the combination of the value of CCxEN.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

11.3.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

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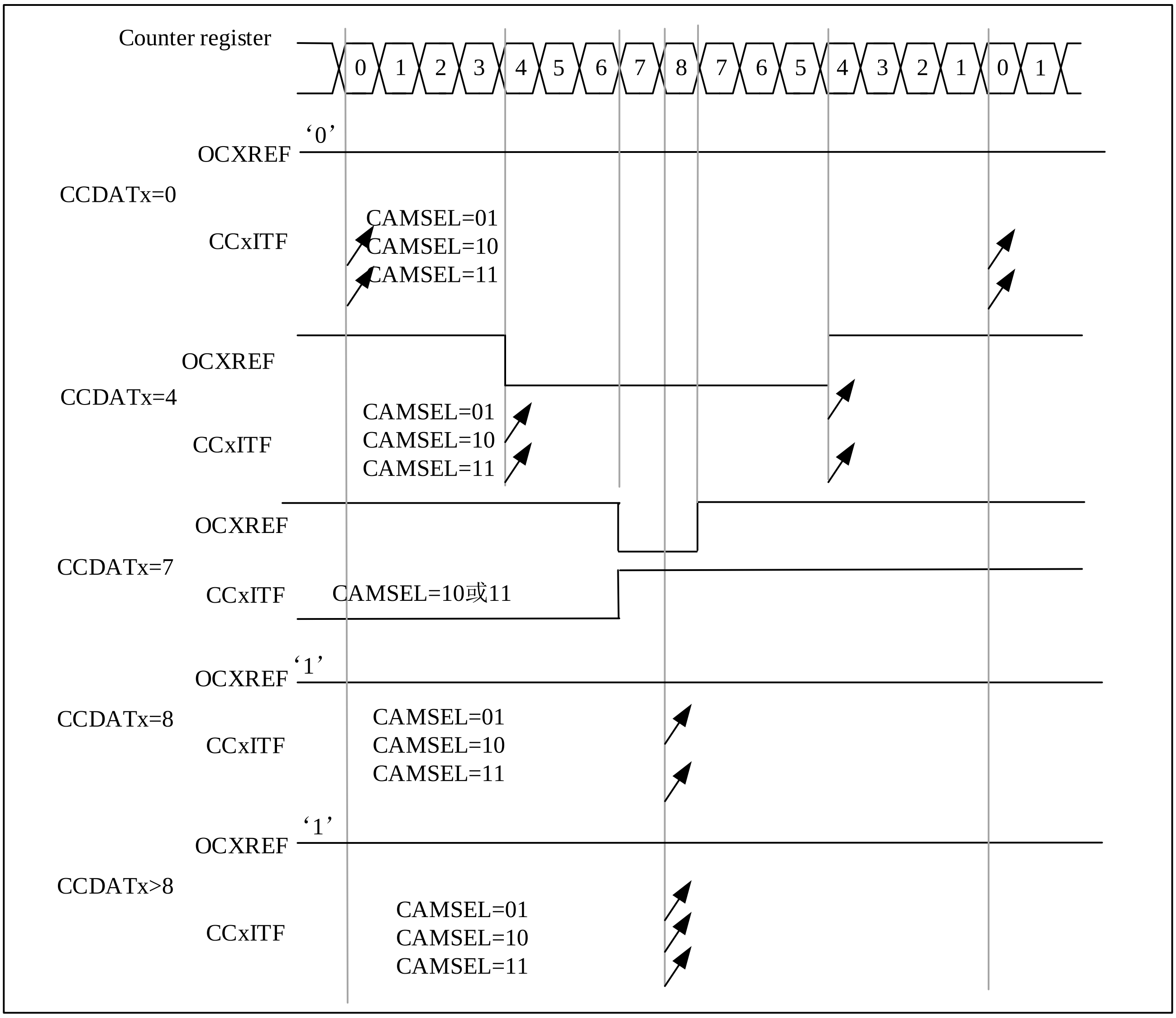
Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

Figure 11-18 Center-aligned PWM waveform (AR=8)



Notes that user should know when using center-aligned mode are as follow:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software

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before starting the counter, and not writing the counter while it is running.

11.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

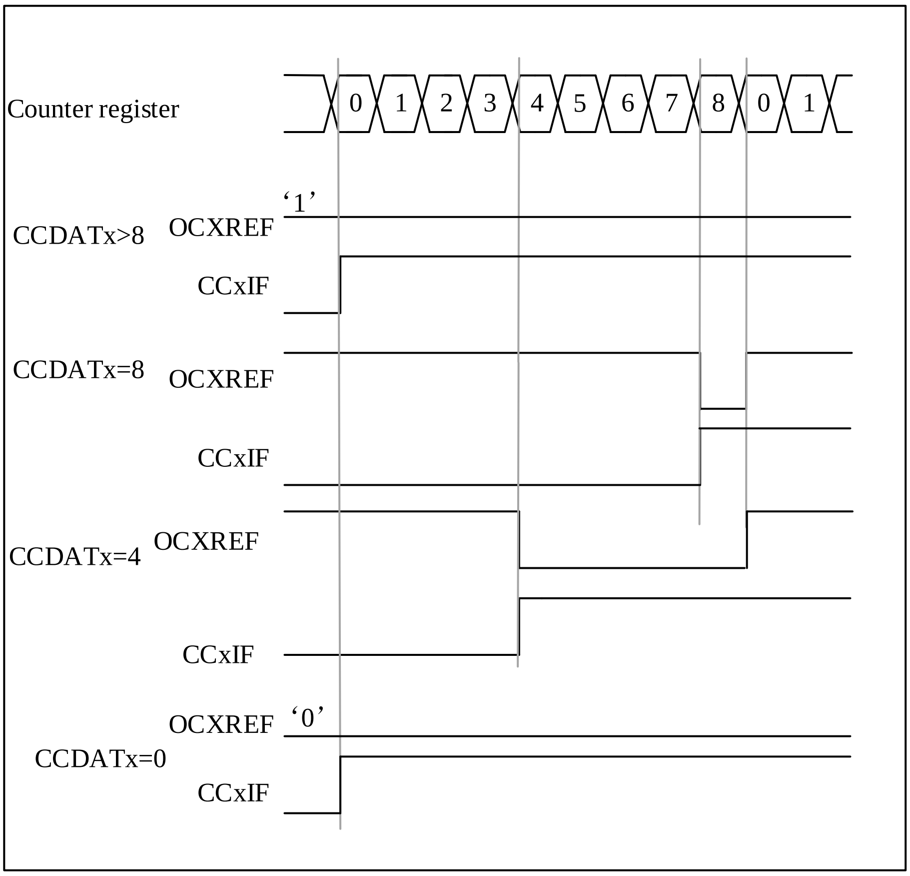
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Here is an example for PWM mode1.

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow.

Figure 11-19 Edge-aligned PWM waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Here is an example for PWM mode1.

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

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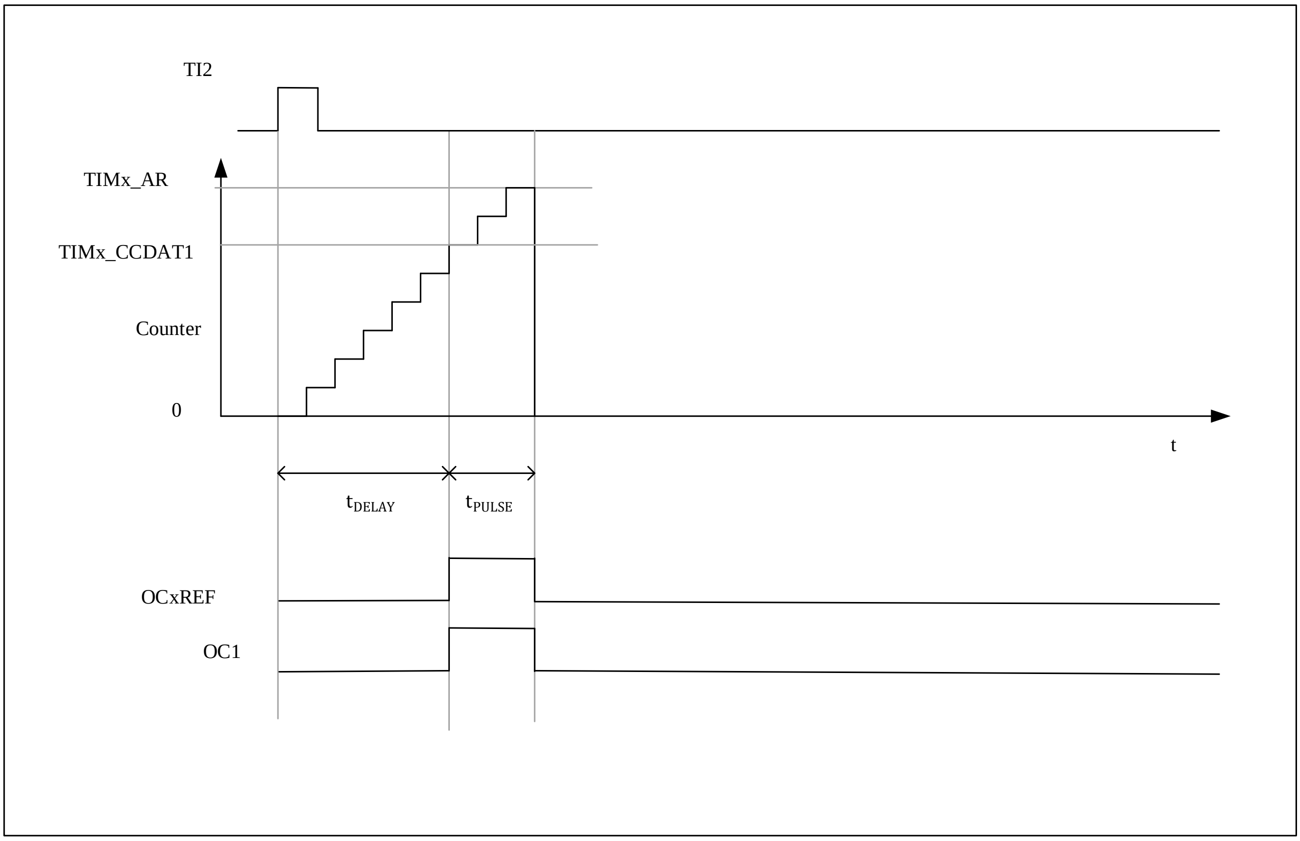
Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

11.3.10 One-pulse mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 11-20 Example of One-pulse mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;

2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= ‘01’; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= ‘0’;

3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= ‘110’, TIMx_SMCTRL.SMSEL= ‘110’ (trigger mode);

4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of

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the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = ‘111’ to select PWM2 mode;

6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

11.3.10.1 Special case: OCx fast enable:

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

11.3.11 Clearing the OCxREF signal on an external event

If user set TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Here is an example for it. To control the current, user can connect the ETR signal to the output of a comparator, and the operation for ETR should be as follow:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

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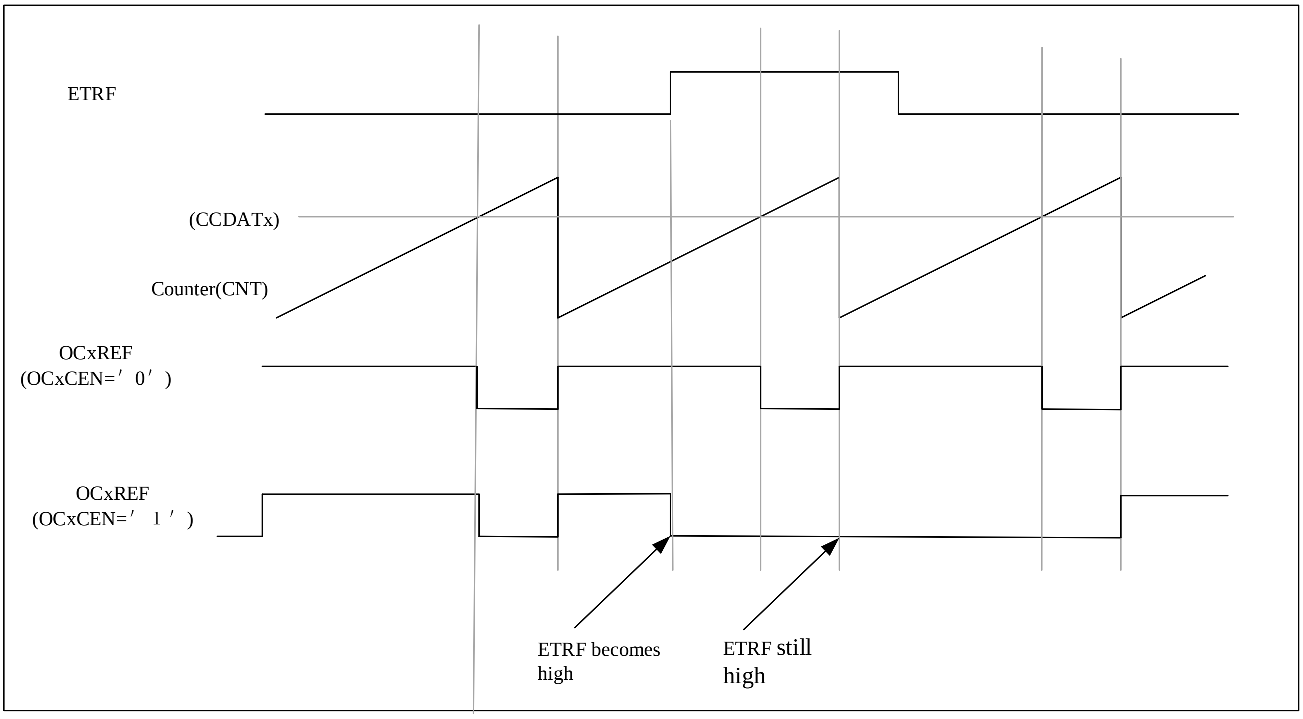
Figure 11-21 Control circuit in reset mode



11.3.12 Debug mode

When the microcontroller is in debug mode (the Cortex-M4 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details, see 29.4.3.

11.3.13 TIMx and external trigger synchronization

Same with advanced-control timer. See 10.3.16.

11.3.14 Timer synchronization

All TIMx timers are internally connected to each other. This implementation allows any master timer to provide trigger to reset, start, stop or provide a clock for the other slave timers. The master clock is used for internal counter and can be prescaled. Below figure shows a Block diagram of timer interconnection.

The synchronization function does not support dynamic change of the connection. User should configure and enable the slave timer before enable the master timer's trigger or clock.

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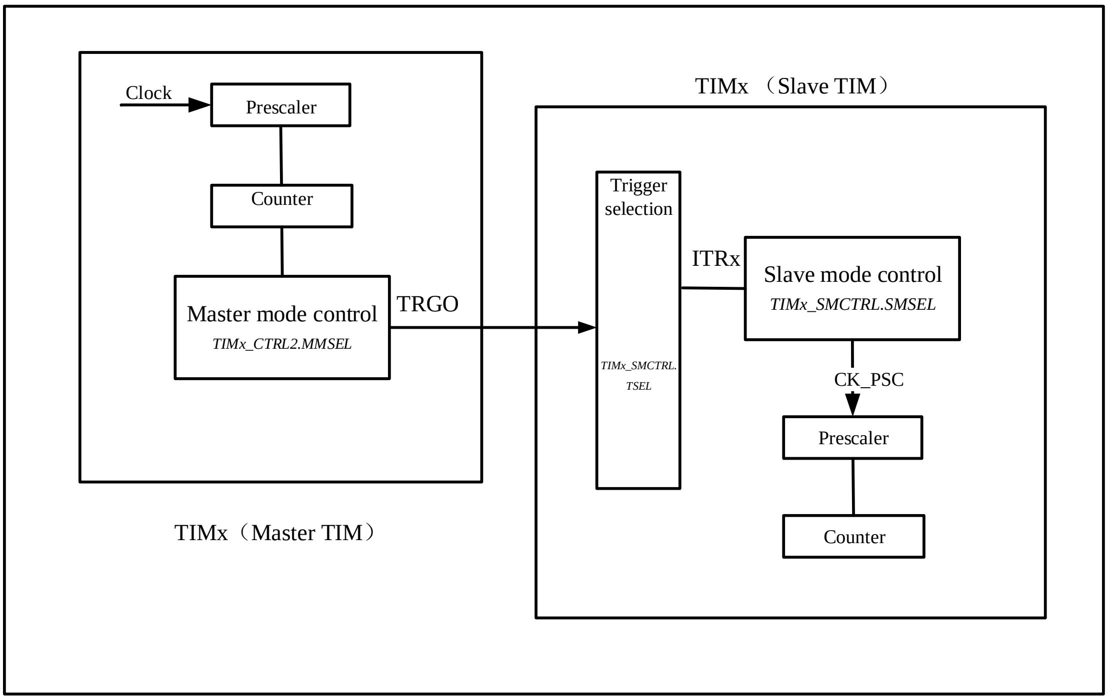
Figure 11-22 Block diagram of timer interconnection



11.3.14.1 Master timer as a prescaler for another timer

TIM1 as a prescaler for TIM2. TIM1 is maser, TIM2 is slave.

User need to do the following steps for this configuration.

- Setting TIM1_CTRL2.MMSEL=' 010' to use the update event of TIM1 as trigger output.
- Configure TIM2_SMCTRL. TSEL= '000' , connect the TRGO of TIM1 to TIM2.
- Configure TIM2_SMCTRL.SMSEL = '111', the slave mode controller will be configured in external clock mode 1.
- Start TIM2 by setting TIM2_CTRL1. CNTEN = '1'.
- Start TIM1 by setting TIM1_CTRL1. CNTEN = '1'.

Note: If user select OCx as the trigger output of TIM1 by configuring MMSEL = '1xx', OCx rising edge will be used to drive timer2.

11.3.14.2 Master timer to enable another timer

In this example, TIM2 is enabled by the output compare of TIM1. TIM2 counter will start to count after the OC1REF output from TIM1 is high. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below.

- Setting TIM1_CTRL2.MMSEL='100' to use the OC1REF of TIM1 as trigger output.
- Configure TIM1_CCMOD1 register to configure the OC1REF output waveform.
- Setting TIM2_SMCTRL.TSEL = '000' to connect TIM1 trigger output to TIM2.

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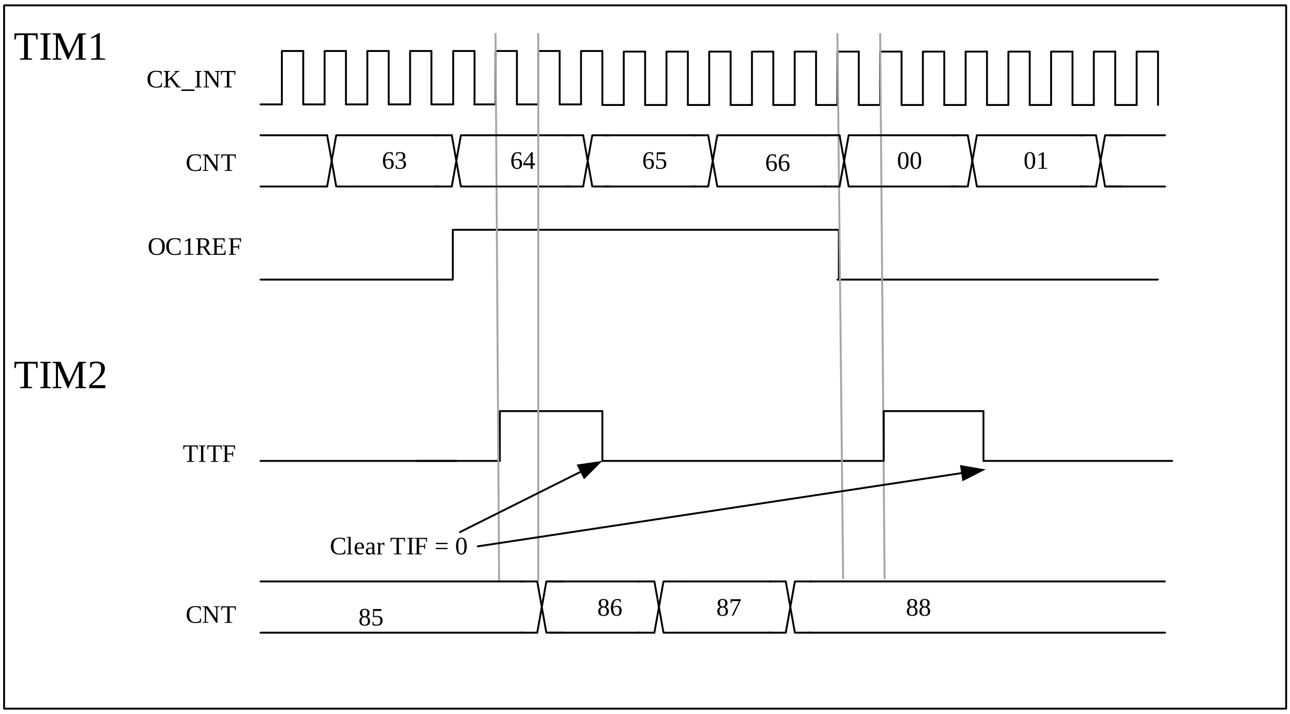
■ Setting TIM2_SMCTRL.SMSEL= ‘101’ to set TIM2 to gated mode.

■ Setting TIM2_CTRL1.CNTEN= ‘1’ to start TIM2.

■ Setting TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.

Note: The TIM2 clock is not synchronized with the TIM1 clock, this mode only affects the TIM2 counter enable signal.

Figure 11-23 TIM2 gated by OC1REF of TIM1



In the next example, Gated TIM2 with enable signal of TIM1, Setting TIM1.CTRL1.CNTEN = ‘0’ to stop TIM1. TIM2 counts on the divided internal clock only when TIM1 is enable. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below

■ Setting TIM1_CTRL2.MMSEL=’ 001’ to use the enable signal of TIM1 as trigger output

■ Setting TIM2_SMCTRL.TSEL = ‘000’ to configure TIM2 to get the trigger input from TIM1

■ Setting TIM2_SMCTRL.SMSEL = ‘101’ to configure TIM2 in gated mode.

■ Setting TIM2_CTRL1.CNTEN= ‘1’ to start TIM2.

■ Setting TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.

■ Setting TIM1_CTRL1.CNTEN= ‘0’ to stop TIM1.

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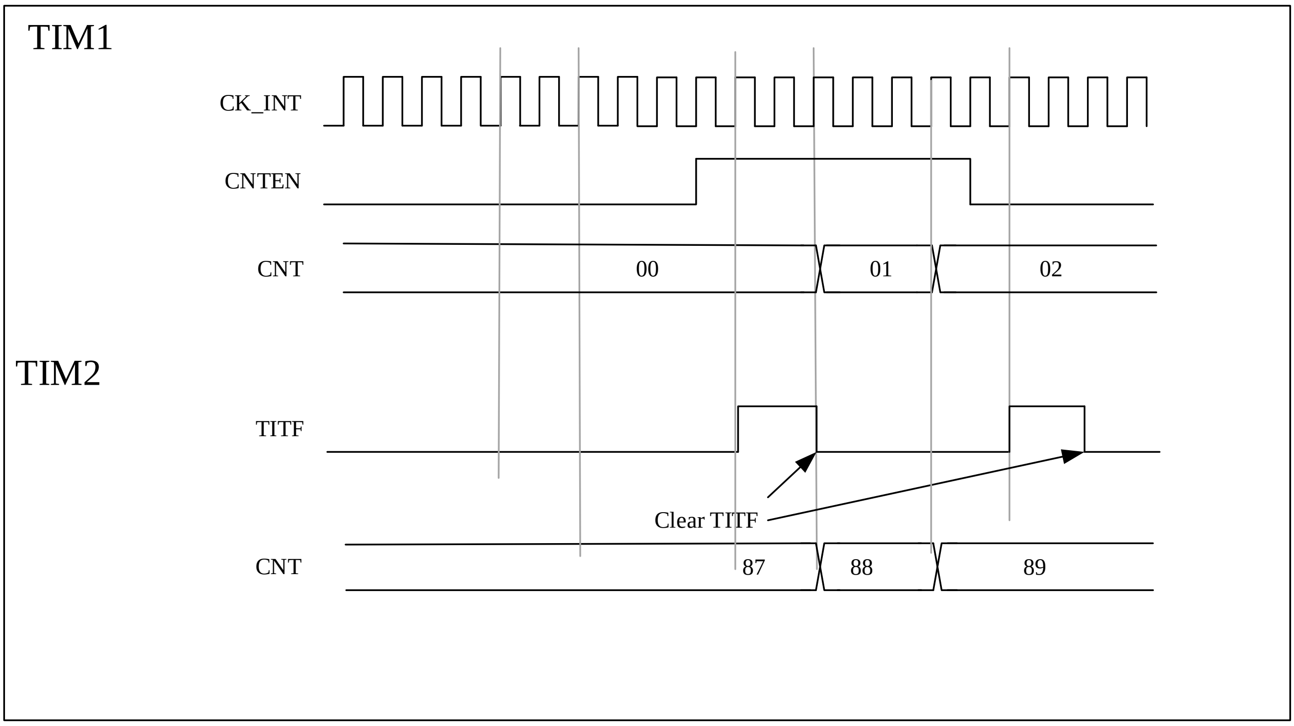
Figure 11-24 TIM2 gated by enable signal of TIM1



11.3.14.3 Master timer to start another timer

In this example, we can use update event as trigger source.TIM1 is master, TIM2 is slave.

The configuration steps are shown as below:

- Setting TIM1_CTRL2.MMSEL=' 010' to use the update event of TIM1 as trigger output
- Configure TIM1_AR register to set the output period.
- Setting TIM2_SMCTRL .TSEL= '000' to connect TIM1 trigger output to TIM2.
- Setting TIM2_SMCTRL. SMSEL = '110' to set TIM2 to trigger mode.
- Setting TIM1_CTRL1.CNTEN=1 to start TIM1.

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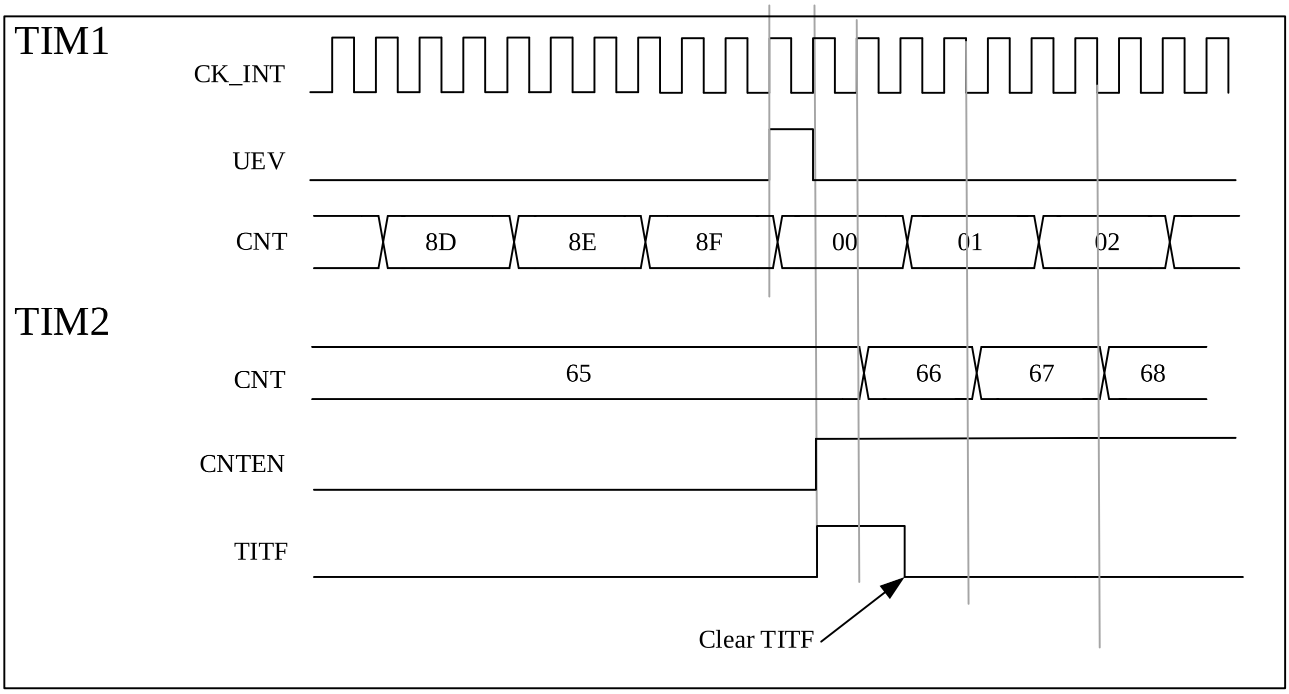
Figure 11-25 Trigger TIM2 with an update of TIM1



11.3.14.4 Start 2 timers synchronously using an external trigger

In this example, TIM1 is enabled when TIM1's TI1 input rises, and TIM2 is enabled when TIM1 is enabled. To ensure the alignment of counters, TIM1 must be configured in master/slave mode. For TI1, TIM1 is the slave; for TIM2, TIM1 is the master.

The configuration steps are shown as below:

- Setting TIM1.MMSEL = ‘001’ to use the enable signal as trigger output
- Setting TIM1_SMCTRL.TSEL = ‘100’ to configure the TIM1 to slave mode and receive the trigger input of TI1.
- Setting TIM1_SMCTRL .SMSEL = ‘110’ to configure TIM1 to trigger mode.
- Setting TIM1_SMCTRL .MSMD = ‘1’ to configure TIM1 to master/slave mode.
- Setting TIM2_SMCTRL .TSEL = ‘000’ to connect TIM1 trigger output to TIM2.
- Setting TIM2_SMCTRL.SMSEL = ‘110’ to configure TIM2 to trigger mode.

When TI1 rising edge arrives, both timers start counting synchronously according to the internal clock, and both TITF flags are set simultaneously.

The following figure shows a delay between CNTEN and CK_PSC of TIM1 in master/slave mode.

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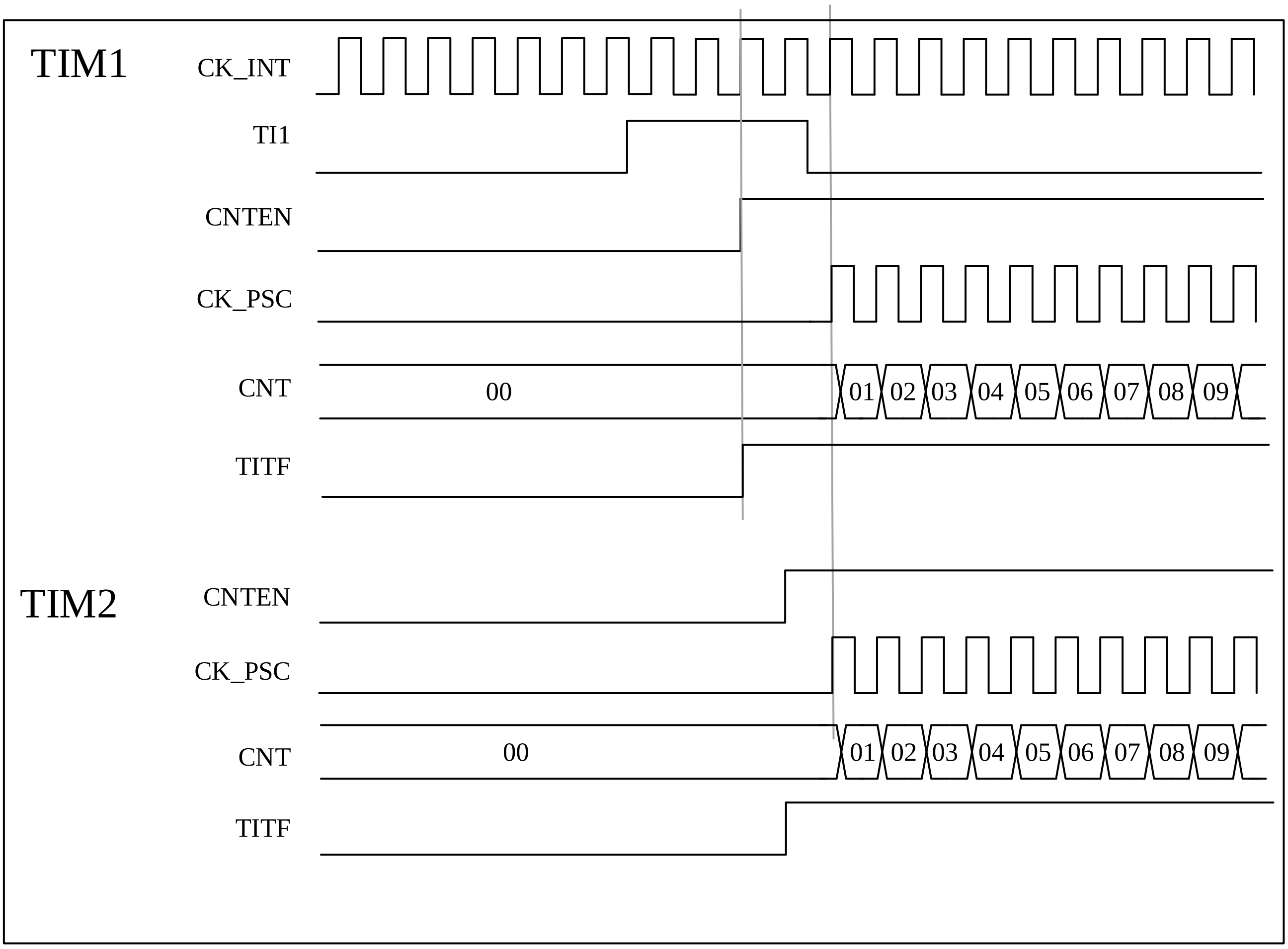
Figure 11-26 Triggers timers 1 and 2 using the TI1 input of TIM1



11.3.15 Encoder interface mode

The encoder uses two inputs TI1 and TI2 as an interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are three types of encoder counting modes:

1. The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘001’;

2. The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’010’;

3. The counter counts on the edges of TI1 and TI2 at the same time, TIMx_SMCTRL.SMSEL = ‘011’;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in Table 11-1:

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Table 11-1 Counting direction versus encoder signals

Active edge	Level on opposite signals (TI1FP1 forTI2, TI2FP2 for TI1)	TI1FP1 signal		TI2FP2 signal	
		Rising	Falling	Rising	Falling
Counting only at TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only at TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edge triggering selected to suppress input jitter:

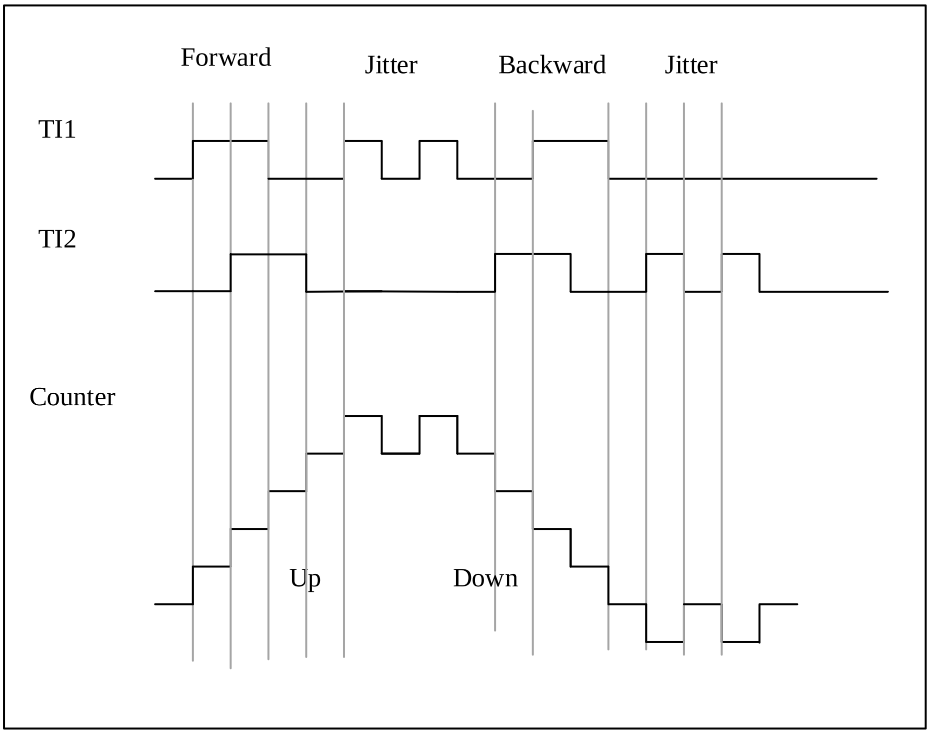
1. IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= ‘01’), IC1FP1 is not inverted (TIMx_CCEN.CC1P= ‘0’);

2. IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= ‘01’), IC2FP2 is not inverted (TIMx_CCEN.CC2P= ‘0’);

3. The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = ‘011’);

4. Enable counter TIMx_CTRL1.CNTEN= ‘1’;

Figure 11-27 Example of counter operation in encoder interface mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above)

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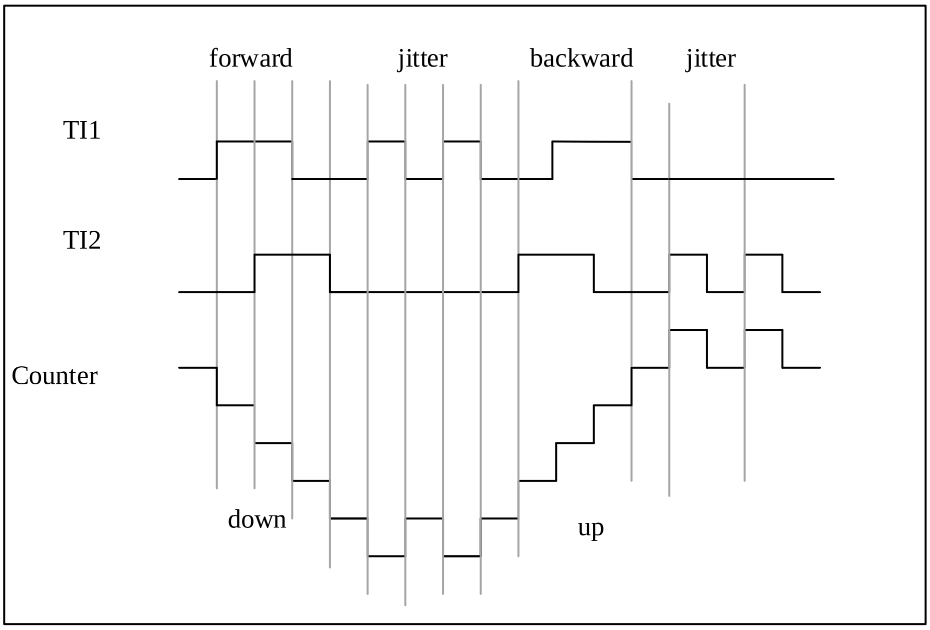
Figure 11-28 Encoder interface mode example with IC1FP1 polarity inverted



11.3.16 Interfacing with Hall sensor

Please refer to 10.3.20

11.4 TIMx registers(x=2, 3 ,4 ,5 and 9)

For abbreviations used in registers, see section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

11.4.1 TIMx register overview

Table 11-2 TIMx register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																CLRSEL	C4SEL	C3SEL	C2SEL	C1SEL	Reserved	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
	Reset Value																	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved																							ETRSEL	TI1SEL	MMSEL[2:0]			CCDSEL	Reserved		
	Reset Value																								0	0	0	0	0	0			
008h	TIMx_SMCTRL	Reserved																EXTP	EXCEN	EXTPS[1:0]		EXTF[3:0]				MSMD	TSEL[2:0]			Reserved	SMSELEL[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	TIMx_DINTEN	Reserved																	TDEN	Reserved	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	Reserved	TIEN	Reserved	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	Reset Value																		0		0	0	0	0	0		0		0	0	0	0	0
010h	TIMx_STS	Reserved																			CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved		TITF	Reserved	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	Reset Value																				0	0	0	0			0		0	0	0	0	0
014h	TIMx_EVTGEN	Reserved																									TGN	Reserved	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	Reset Value																										0		0	0	0	0	0
018h	TIMx_CCMOD1	Reserved																OC2CEN	OC2MD[2:0]			OC2PEN	OC2FEN	CC2SEL[1:0]		OC1CEN	OC1MD[2:0]			OC1PEN	OC1FEN	CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved																IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																OC4CEN	OC4MD[2:0]			OC4PEN	OC4FEN	CC4SEL[1:0]		OC3CEN	OC3MD[2:0]			OC3PEN	OC3FEN	CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCEN	Reserved																		CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN
	Reset Value																			0	0			0	0			0	0			0	0
024h	TIMx_CNT	Reserved																CNT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved																PSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved																AR[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
030h	Reserved																																
034h	TIMx_CCDAT1	Reserved																CCDAT1[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT2	Reserved																CCDAT2[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	TIMx_CCDAT3	Reserved																CCDAT3[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	TIMx_CCDAT4	Reserved																CCDAT4[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	Reserved																																
048h	TIMx_DCTRL	Reserved																			DBLEN[4:0]					Reserved			DBADDR[4:0]				
	Reset Value																				0	0	0	0	0				0	0	0	0	0
04Ch	TIMx_DADDR	Reserved																BURST[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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11.4.2 Control register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31–16
Reserved

15	14	13	12	11	10	9–8	7	6–5	4	3	2	1	0
CLRSEL	Reserved	C3SEL	C2SEL	C1SEL	Reserved	CLKD[1:0]	ARPEN	CAMSEL[1:0]	DIR	ONEPM	UPRS	UPDIS	CNTEN
rw		rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	CLRSEL	OCxREF clear selection 0: Select the external OCxREF clear from ETR 1: Select the internal OCxREF clear from comparator *Note: For TIM5, setting to 1 is invalid*
14	C4SEL	Channel 4 Selection 0: Select external CH4 (from IOM) signal 1: Select internal CH4 (from HSE) signal *Note：For TIM2, TIM3, TIM4, TIM5, setting to 1 is invalid. For TIM9, setting to 1 is valid*
13	C3SEL	Channel 3 Selection 0: Select external CH3 (from IOM) signal 1: Seleect internal CH3 (from LSI) signal *Note：For TIM2, TIM3, TIM4, TIM5, setting to 1 is invalid. For TIM9, setting to 1 is valid*
12	C2SEL	Channel 2 Selection 0: Select external CH2 (from IOM) signal 1: Seleect internal CH2 (from LSE) signal *Note：For TIM2, TIM3, TIM4, TIM5, setting to 1 is invalid. For TIM9, setting to 1 is valid*
11	C1SEL	Channel 1 selection 0: Select external CH1 (from IOM) signal 1: Select internal CH1 (from COMP) signal
10	Reserved	Reserved, the reset value must be maintained
9:8	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and t_{DTS} (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK\_INT}$ 01: $t_{DTS} = 2 \times t_{CK\_INT}$ 10: $t_{DTS} = 4 \times t_{CK\_INT}$ 11: Reserved, do not use this configuration
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register

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Bit field	Name	Description
		1: Shadow register enable for TIMx_AR register
6:5	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
4	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
3	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
1	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter

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Bit field	Name	Description
		1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

11.4.3 Control register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000

15–9	8	7	6–4	3	2–0
Reserved	ETRSEL	TI1SEL	MMSEL[2:0]	CCDSEL	Reserved
	rw	rw	rw	rw	

Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained
8	ETRSEL	External Triggered Selection storage (ETR Selection) 0: Select external ETR (from IOM) signal; 1: Reserved *Note: For TIM4 and TIM5, ETR input is not support.*
7	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 100: Compare - OC1REF signal is used as the trigger output (TRGO).

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Bit field	Name	Description
		101: Compare - OC2REF signal is used as the trigger output (TRGO). 110: Compare - OC3REF signal is used as the trigger output (TRGO). 111: Compare - OC4REF signal is used as the trigger output (TRGO).
3	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
2:0	Reserved	Reserved, the reset value must be maintained

11.4.4 Slave mode control register (TIMx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

15	14	13:12	11:8	7	6:4	3	2:0
EXTP	EXCEN	EXTPS[1:0]	EXTF[3:0]	MSMD	TSEL[2:0]	Reserved	SMSEL[2:0]
rw	rw	rw	rw	rw	rw		rw

Bit field	Name	Description
15	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use ETR or the inversion of ETR. 0: ETR active at high level or rising edge. 1: ETR active at low level or falling edge.
14	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
13:12	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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Bit field	Name	Description
11:8	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
7	MSMD	Master/ Slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.
6:4	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: TI1 edge detector (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1 (TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External triggered Input (ETRF) For more details on ITRx, see Table 11-3 below. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*
3	Reserved	Reserved, the reset value must be maintained
2:0	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock.

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Bit field	Name	Description
		001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*

Table 11-3 TIMx internal trigger connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM2	TIM1	TIM8	TIM3	TIM4
TIM3	TIM1	TIM2	TIM5	TIM4
TIM4	TIM1	TIM2	TIM3	TIM8
TIM5	TIM2	TIM3	TIM4	TIM8
TIM9	TIM1	TIM2	TIM5	TIM4

11.4.5 DMA/Interrupt enable registers (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TDEN	Reserved	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	Reserved	TIEN	Reserved	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	rw		rw	rw	rw	rw	rw		rw		rw	rw	rw	rw	rw

Bit field	Name	Description
15	Reserved	Reserved, the reset value must be maintained
14	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
13	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
12	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
11	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
10	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
9	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
8	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
7	Reserved	Reserved, the reset value must be maintained
6	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
5	Reserved	Reserved, the reset value must be maintained
4	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
3	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
2	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
1	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

11.4.6 Status registers (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000

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15:13	12	11	10	9	8:7	6	5	4	3	2	1	0
Reserved	CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved	TITF	Reserved	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	rc_w0	rc_w0	rc_w0	rc_w0		rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained
12	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
11	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
10	CC2OCF	Capture/Compare 2 overcapture flags See TIMx_STS.CC1OCF description.
9	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
8:7	Reserved	Reserved, the reset value must be maintained
6	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred 1: Trigger interrupt occurred
5	Reserved	Reserved, the reset value must be maintained
4	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.
3	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
2	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
1	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:**

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Bit field	Name	Description
		This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, overflow or underflow (An update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

11.4.7 Event generation registers (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0 x0000

15–7	6	5	4	3	2	1	0
Reserved	TGN	Reserved	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	w		w	w	w	w	w

Bit field	Name	Description
15：7	Reserved	Reserved, the reset value must be maintained.
6	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
5	Reserved	Reserved, the reset value must be maintained
4	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
3	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
2	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
1	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically

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Bit field	Name	Description
		cleared by hardware. When the corresponding channel of CC1 is in output mode: The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event
0	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event

11.4.8 Capture/compare mode register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:

15	14-12	11	10	9-8	7	6-4	3	2	1-0
OC2CEN	OC2MD[2:0]	OC2PEN	OC2FEN	CC2SEL[1:0]	OC1CEN	OC1MD[2:0]	OC1PEN	OC1FEN	CC1SEL[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	OC2CEN	Output Compare 2 clear enable
14:12	OC2MD[2:0]	Output Compare 2 mode
11	OC2PEN	Output Compare 2 preload enable
10	OC2FEN	Output Compare 2 fast enable
9:8	CC2SEL[1:0]	Capture/compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2

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Bit field	Name	Description
		10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by ETRF input level 1: OC1REF is cleared immediately when the ETRF input level is detected as high
6:4	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
3	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
2	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input

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Bit field	Name	Description
		is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
1：0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:

15–12	11–10	9–8	7–4	3–2	1–0
IC2F[3:0]	IC2PSC[1:0]	CC2SEL[1:0]	IC1F[3:0]	IC1PSC[1:0]	CC1SEL[1:0]
rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15:12	IC2F[3:0]	Input Capture 2 Filter
11:10	IC2PSC[1:0]	Input Capture 2 Prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input Capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6

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Bit field	Name	Description
		1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

11.4.9 Capture/compare mode register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000

See the description of the CCMOD1 register above

Output comparison mode:

15	14 12	11	10	9 8	7	6 4	3	2	1 0
OC4CEN	OC4MD[2:0]	OC4PEN	OC4FEN	CC4SEL[1:0]	OC3CEN	OC3MD[2:0]	OC3PEN	OC3FEN	CC3SEL[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	OC4CEN	Output compare 4 clear enable
14:12	OC4MD[2:0]	Output compare 4 mode
11	OC4PEN	Output compare 4 preload enable
10	OC4FEN	Output compare 4 fast enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output

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Bit field	Name	Description
		01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7	OC3CEN	Output compare 3 clear enable
6:4	OC3MD[2:0]	Output compare 3 mode
3	OC3PEN	Output compare 3 preload enable
2	OC3FEN	Output compare 3 fast enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:

15–12	11–10	9–8	7–4	3–2	1–0
IC4F[3:0]	IC4PSC[1:0]	CC4SEL[1:0]	IC3F[3:0]	IC3PSC[1:0]	CC3SEL[1:0]
rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15:12	IC4F[3:0]	Input Capture 4 filter
11:10	IC4PSC[1:0]	Input Capture 4 Prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input Capture 3 filter
3:2	IC3PSC[1:0]	Input Capture 3 Prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when

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Bit field	Name	Description
		the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

11.4.10 Capture/compare enable registers (TIMx_CCEN)

Offset address: 0x20

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1OP	CC1EN
		rw	rw			rw	rw			rw	rw			rw	rw

Bit field	Name	Description
15:14	Reserved	Reserved, the reset value must be maintained.
13	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
12	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
11:10	Reserved	Reserved, the reset value must be maintained
9	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
8	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
7:6	Reserved	Reserved, the reset value must be maintained
5	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
4	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
3:2	Reserved	Reserved, the reset value must be maintained
1	CC1P	Capture/Compare 1 output polarity When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low When the corresponding channel of CC1 is in input mode: At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: If TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*
0	CC1EN	Capture/Compare 1 output enable

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Bit field	Name	Description
		When the corresponding channel of CC1 is in output mode: 0: Disable - Disable output OC1 signal. 1: Enable - Enable output OC1 signal. When the corresponding channel of CC1 is in input mode: At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture

Table 11-4 Output control bits of standard OCx channel

CCxEN	OCx output status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: The state of external I/O pins connected to standard OCx channels depends on the OCx channel state and GPIO and AFIO registers.

11.4.11 Counters (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

15 … 0
CNT[15:0]
rw

Bit field	Name	Description
15:0	CNT[15:0]	Counter value

11.4.12 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

15 … 0
PSC[15:0]
rw

Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

11.4.13 Auto-reload register (TIMx_AR)

Offset address: 0x2C

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Reset values: 0xFFFF

15	0
AR[15:0]	
rw	

Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See Section 11.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

11.4.14 Capture/compare register 1 (TIMx_CCDAT1)

Offset address: 0x34

Reset value: 0x0000

15	0
CCDAT1[15:0]	
rw/r	

Bit field	Name	Description
15:0	CCDAT1[15:0]	Capture/Compare 1 value ■ CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

11.4.15 Capture/compare register 2 (TIMx_CCDAT2)

Offset address: 0x38

Reset value: 0x0000

15	0
CCDAT2[15:0]	
rw/r	

Bit field	Name	Description
15:0	CCDAT2[15:0]	Capture/Compare 2 values ■ CC2 channel is configured as output:

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Bit field	Name	Description
		CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

11.4.16 Capture/compare register 3 (TIMx_CCDAT3)

Offset address: 0x3C

Reset value: 0x0000

15 ... 0
CCDAT3[15:0]
rw/r

Bit field	Name	Description
15:0	CCDAT3[15:0]	Capture/Compare 3 value ■ CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 is only readable. When configured as output mode, register CCDAT3 is readable and writable.

11.4.17 Capture/compare register 4 (TIMx_CCDAT4)

Offset address: 0x40

Reset value: 0x0000

15 ... 0
CCDAT4[15:0]
rw/r

Bit field	Name	Description
15:0	CCDAT4[15:0]	Capture/Compare 4 value ■ CC4 channel is configured as output:

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		CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. ■ CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 is only readable. When configured as output mode, register CCDAT4 is readable and writable.

11.4.18 DMA Control register (TIMx_DCTRL)

Offset address: 0x48

Reset value: 0x0000

15:13	12:8	7:5	4:0
Reserved	DBLEN[4:0]	Reserved	DBADDR[4:0]
	rw		rw

Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained
12:8	DBLEN[4:0]	DMA Burst Length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 00000:1 time transfer 00001: 2 times transfers 00010: 3 times transfers … 10001: 18 times transfers
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	DBADDR[4:0]	DMA Base Address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 00000: TIMx_CTRL1, 00001: TIMx_CTRL2, 00010: TIMx_SMCTRL, … 01011：TIMx_AR, 01100：Reserved, 01101：TIMx_CCDAT1, … 10000：TIMx_CCDAT4, 10001：Reserved,

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Bit field	Name	Description
		10010：TIMx_DCTRL

11.4.19 DMA transfer buffer register (TIMx_DADDR)

Offset address: 0x4C

Reset value: 0x0000

15 … 0
BURST[15:0]
rw

Bit field	Name	Description
15:0	BURST[15:0]	DMA access buffer. When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length ×4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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12 Basic timers (TIM6 and TIM7)

12.1 Basic timers introduction

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter.

These two timers are independent of each other and do not share any resources.

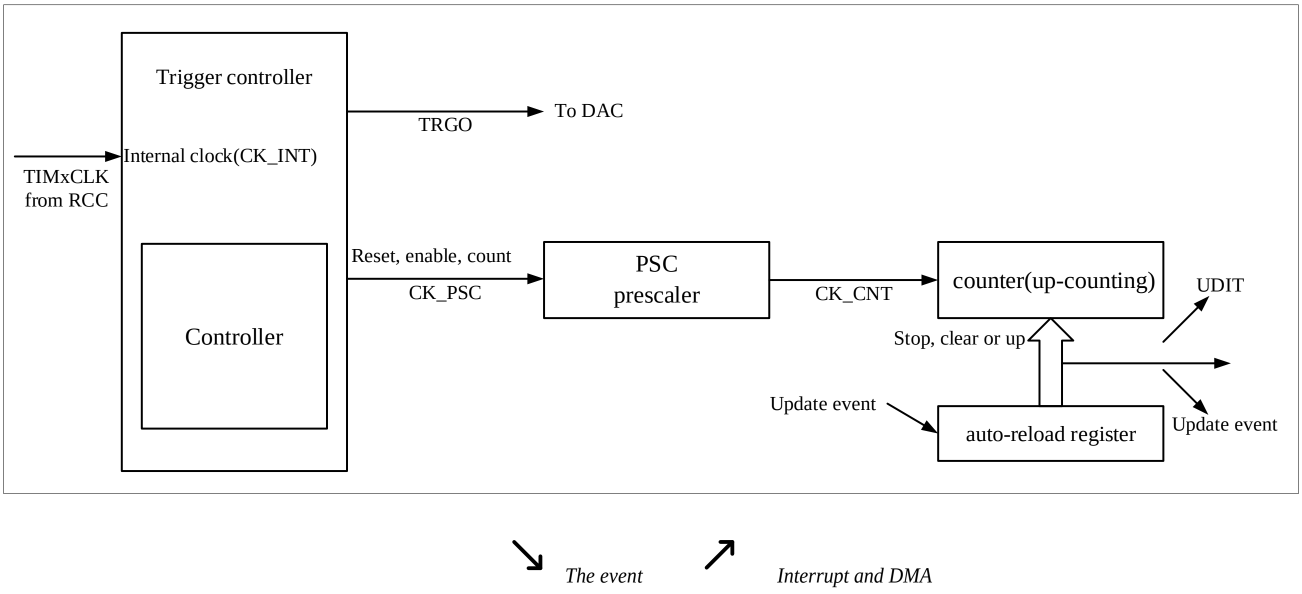
The basic timer can provide a time reference for general purpose timers, and in particular can provide a clock for a digital-to-analog converter (DAC).

The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

12.2 Main features of Basic timers

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- The events that generate the interrupt/DMA are as follows:
  - Update event

Figure 12-1 Block diagram of TIMx（x = 6 and 7）



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12.3 Basic timers description

12.3.1 Time-base unit

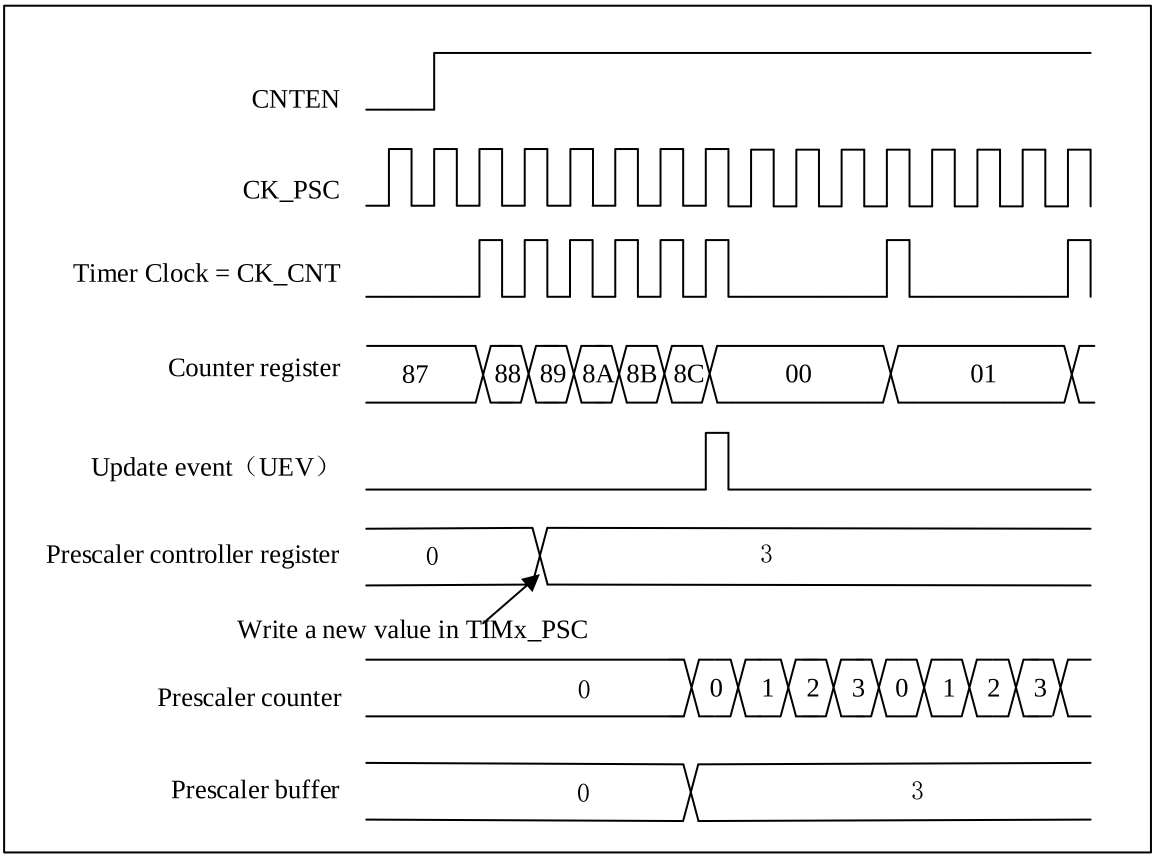
The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

12.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 12-2 Counter timing diagram with prescaler division change from 1 to 4



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12.3.2 Counter mode

12.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate, and TIMx_STS.UDITF will not be set by hardware. Therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in TIMx_CTRL1.UPRS, When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC)

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

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Figure 12-3 Timing diagram of up-counting. The internal clock divider factor = 2/N

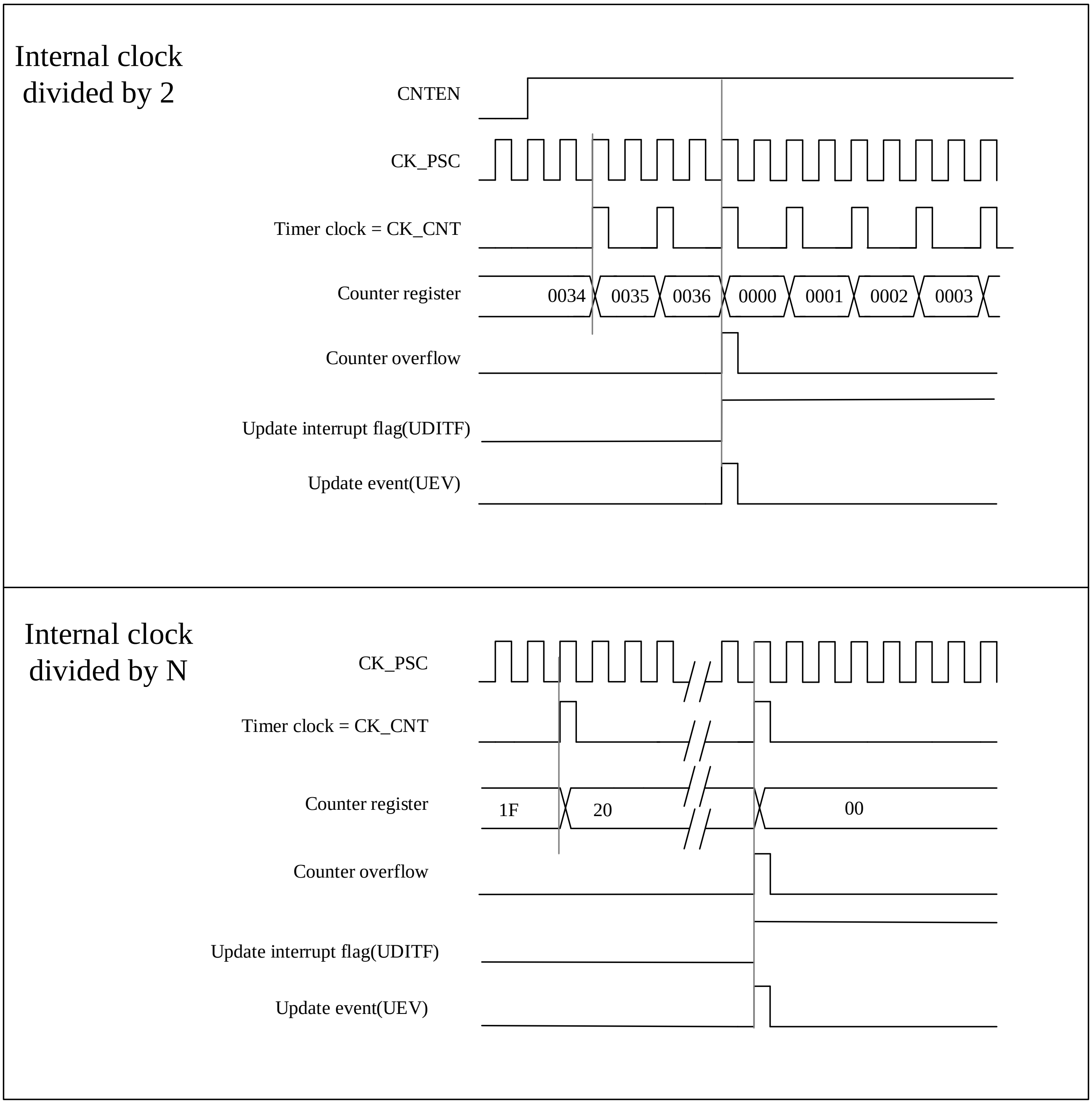

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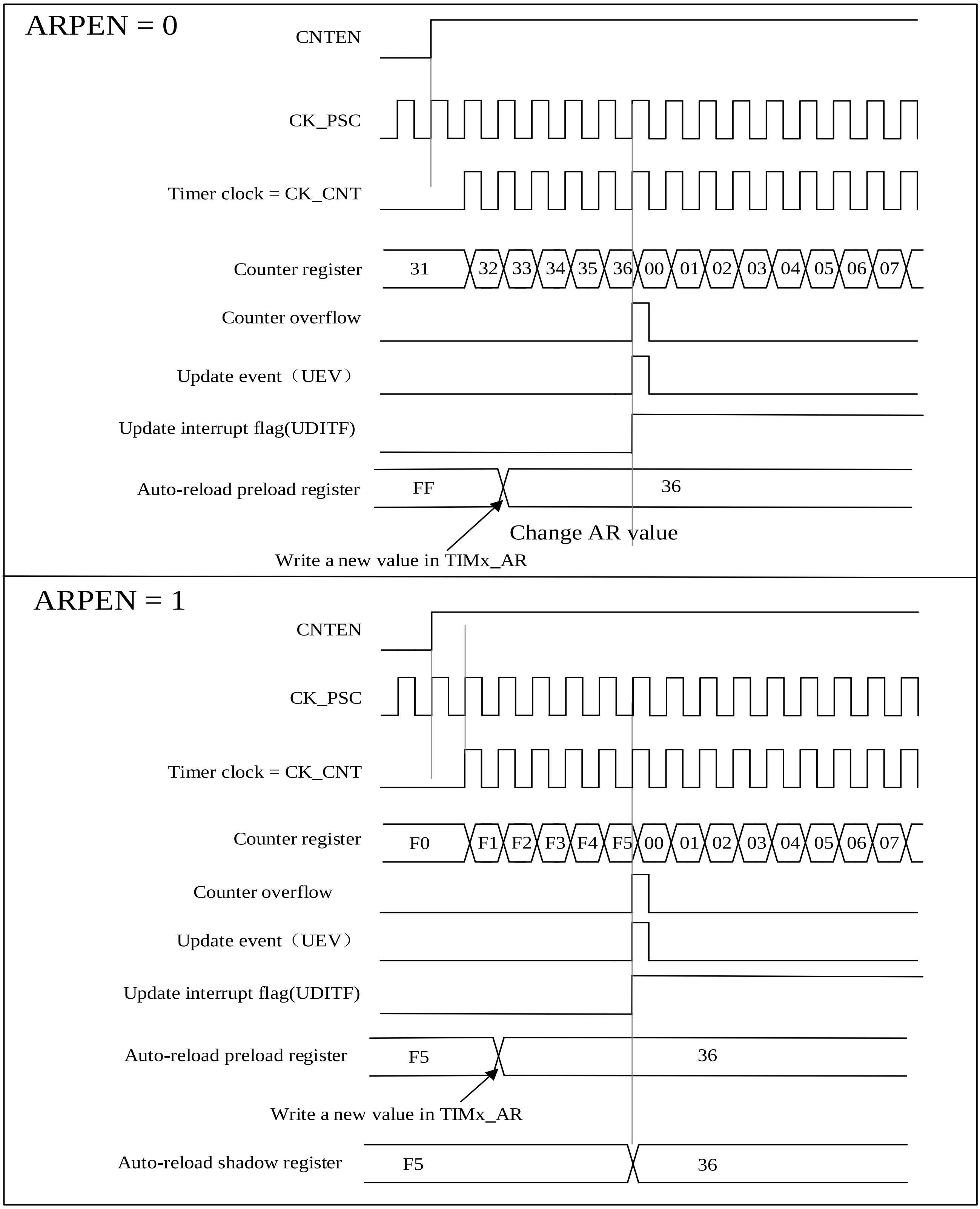
Figure 12-4 Timing diagram of the up-counting, update event when ARPEN=0/1



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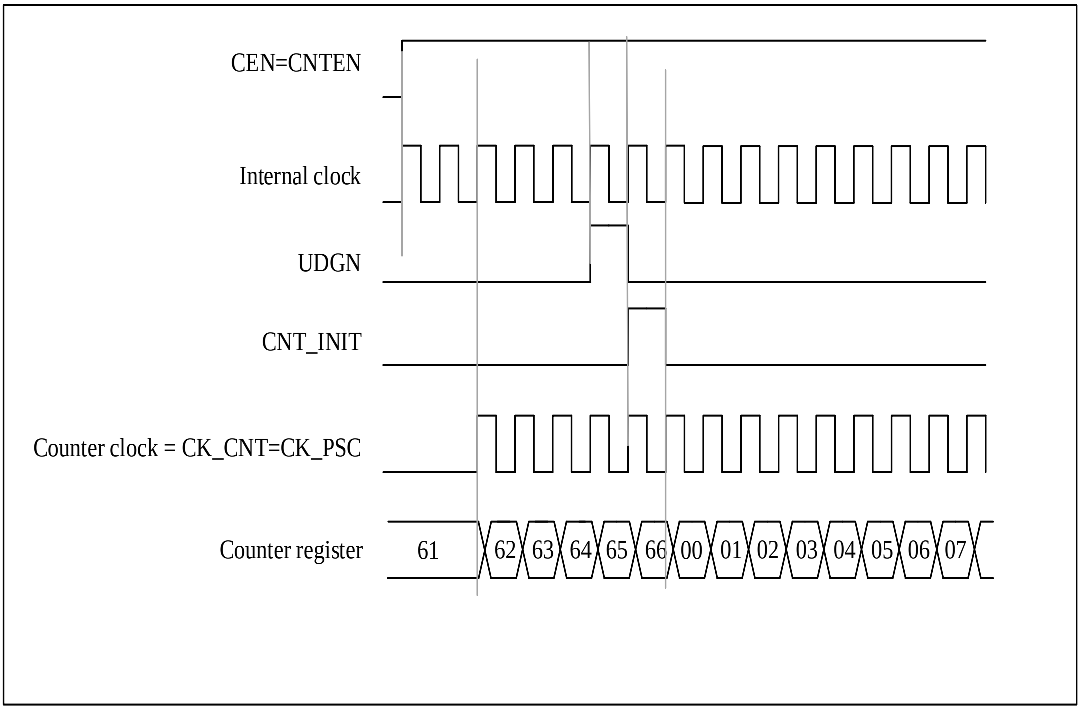
12.3.3 Clock selection

■ The internal clock of timers ： CK_INT

12.3.3.1 Internal clock source (CK_INT)

It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 12-5 Control circuit in normal mode, internal clock divided by 1



12.3.4 Debug mode

When the microcontroller is in debug mode (the Cortex-M4 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details, see 29.4.3.

12.4 TIMx registers(x = 6 and 7)

For abbreviations used in registers, see section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

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12.4.1 TIMx register overview

Table 12-1 TIMx register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																								ARPEN	Reserved			ONEPM	UPRS	UPDIS	CNTEN
	Reset Value																									0				0	0	0	0
004h	TIMx_CTRL2	Reserved																									MMSEL[2:0]			Reserved			
	Reset Value																										0	0	0				
008h	Reserved																																
00Ch	TIMx_DINTEN	Reserved																							UDEN	Reserved							UIEN
	Reset Value																								0								0
010h	TIMx_STS	Reserved																															UDITF
	Reset Value																																0
014h	TIMx_EVTGEN	Reserved																															UDGN
	Reset Value																																0
018h	Reserved																																
01Ch	Reserved																																
020h	Reserved																																
024h	TIMx_CNT	Reserved																CNT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved																PSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved																AR[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

12.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000

15-8	7	6-4	3	2	1	0
Reserved	ARPEN	Reserved	ONEPM	UPRS	UPDIS	CNTEN
	rw		rw	rw	rw	rw

Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:4	Reserved	Reserved, the reset value must be maintained
3	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow – The TIMx_EVTGEN.UDGN bit is set 1: If update interrupt or DMA request is enabled, only counter overflow will generate update interrupt or DMA request
1	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled: – Counter overflow – The TIMx_EVTGEN.UDGN bit is set Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC) keep their values. If the TIMx_EVTGEN.UDGN bit is set, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter

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12.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000

15–7	6–4	3–0
Reserved	MMSEL[2:0]	Reserved
	rw	

Bit field	Name	Description
15:7	Reserved	Reserved, the reset value must be maintained
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds.
15：1	Reserved	Reserved, the reset value must be maintained.

12.4.4 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000

15–9	8	7–1	0
Reserved	UDEN	Reserved	UIEN
	rw		rw

Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
8	UDEN	Update DMA Request enable 0: Disable update DMA request 1: Enable update DMA request
7:1	Reserved	Reserved, the reset value must be maintained
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

12.4.5 Status Registers (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000

15 … 1	0
Reserved	UDITF
	rc_w0

Bit field	Name	Description
15:1	Reserved	Reserved, the reset value must be maintained
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, and counter value overflow. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

12.4.6 Event Generation registers (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0 x0000

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15 ... 1	0
Reserved	UDGN
	w

Bit field	Name	Description
15：1	Reserved	Reserved, the reset value must be maintained.
0	UDGN	UDGN: Update generation Software can set this bit to update configuration register value and hardware will clear it automatically. 0: No effect. 1: Timer counter will restart and all shadow register will be updated. It will restart prescaler counter also.

12.4.7 Counters (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

15 ... 0
CNT[15:0]
rw

Bit field	Name	Description
15:0	CNT[15:0]	Counter value

12.4.8 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

15 ... 0
PSC[15:0]
rw

Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value PSC register value will be updated to prescaler register at update event. Counter clock frequency is

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Bit field	Name	Description
		input clock frequency divide PSC + 1.

12.4.9 Automatic reload register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF

15 … 0
AR[15:0]
rw

Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See 12.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

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13 Low Power Timer (LPTIM)

13.1 Introduction

The LPTIM is a 16-bit timer with multiple clock sources, it can keep running in all power modes except for Standby mode. LPTIM can run without internal clock source, it can be used as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extreme low power consumption.

13.2 Main Features

- 16-bit upcounter
- Clock prescaler with 3-bit to provide 8 dividing factors (1,2,4,8,16,32,64,128)
- Multiple clock sources

  Internal : LSE, LSI, HSI, APB1 or COMP clock

  External : LPTIM Input1 (working with no LP oscillator running used by Pulse Counter application)
- 16-bit auto-reload register
- 16-bit compare register
- Continuous or One-shot counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for filtering glitch
- Configurable output: Pulse, PWM
- Configurable I/O polarity
- Encoder mode, Encoder mode Pulse counting mode, support single pulse counting, double pulse counting (orthogonal and non-orthogonal)

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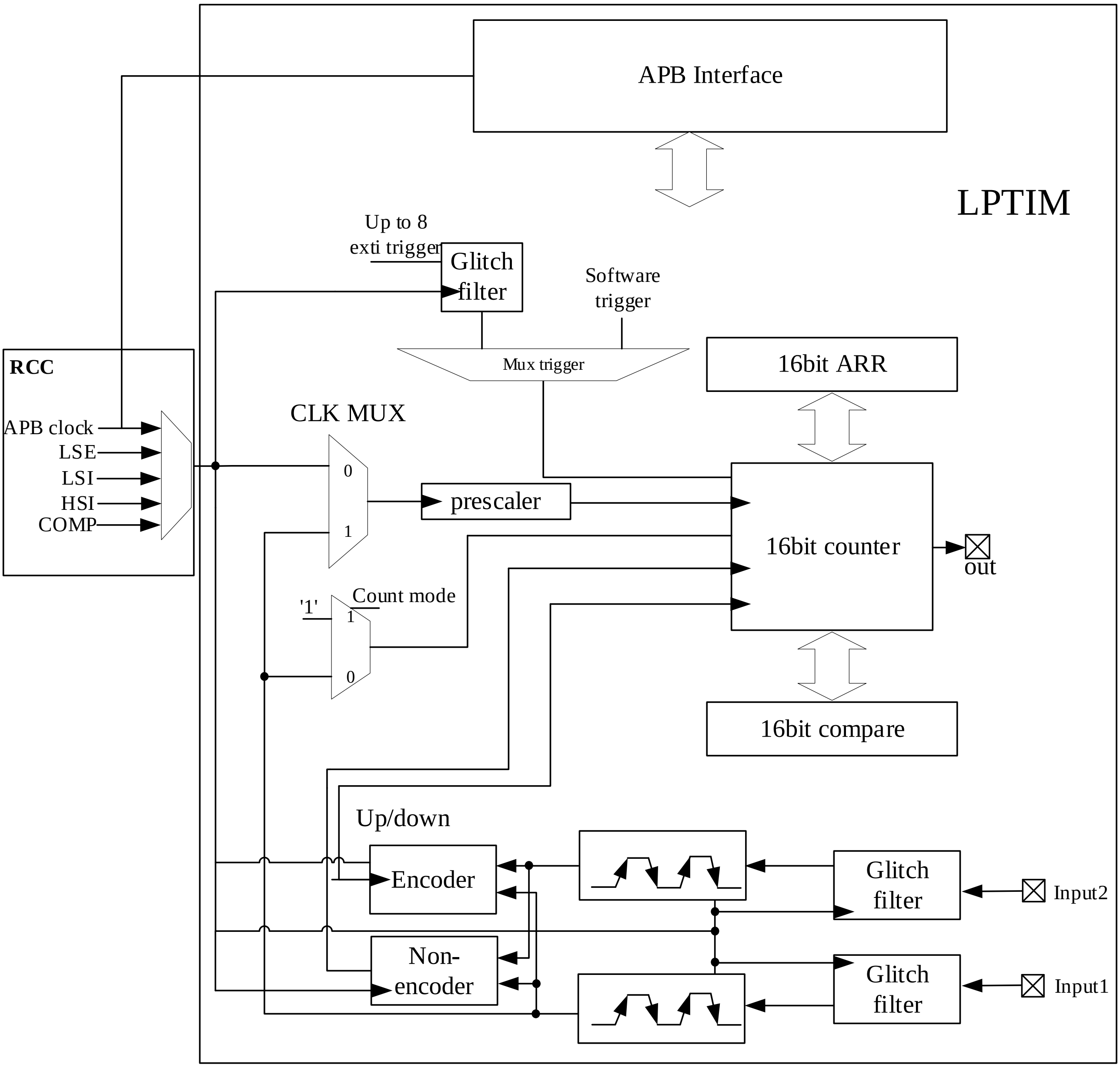
13.3 Block diagram

Figure 13-1 LPTIM Diagram



13.4 Function description

13.4.1 LPTIM clocks and on-off control

The LPTIM can use either internal clock source or external clock source.

The LPTIM can use an internal clock source or an external clock source. The internal clock source can be selected between APB, LSI, LSE, HSI or Comparator 1, 2 by configuring the RCC_RDCTRL.LPTIMSEL[2:0] bits. The

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external clock source can be selected from GPIO. For clock source, the LPTIM has two configurations:

- The LPTIM uses both external clock and internal clock.
- The LPTIM only use clock from comparator or external Input1. This configuration is suitable for LOW POWER application.

LPTIM_CFG.CLKSEL and LPTIM_CFG.CNTMEN bits are used for the clock source configuration. The active clock edge is configured through LPTIM_CFG.CLKPOL[1:0] bits.

When the LPTIM only uses external clock source, it can only select one active clock edge. LPTIM can select both active clock edges only when it is using internal clock source or both external and internal clock sources.

Note: When both active edges for external clock, LPTIM needs to use an internal clock to oversample the external clock. The internal clock frequency should be at least 4 times higher than the external clock frequency.

13.4.2 Prescaler

The LPTIM counter is preceded by a configurable power-of-2 pre-scaler. The prescaler ratio is controlled by the LPTIM_CFG.CLKPRE[2:0] field. The table below lists all the possible division ratios:

Table 13-1 Pre-scaler division ratios

Control bits	The corresponding frequency division factor
000	/1
001	/2
010	/4
011	/8
100	/16
101	/32
110	/64
111	/128

13.4.3 Glitch filter

LPTIM has glitch filters for inputs to remove glitches and prevent unexpected counts or triggers.

Glitch filter needs an internal clock source to operate. And the clock source should be provided before the glitch filter is enabled. This is necessary to guarantee the proper operation of the filters.

The glitch filters has two major purposes:

- For the external inputs: The filter sensitivity is configured through the LPTIM_CFG.CLKFLT[1:0] bits.
- For the internal trigger inputs: The filter sensitivity is configured through the LPTIM_CFG.RIGFLT[1:0] bits.

Note: The detection configuration is only applicable for its corresponding inputs.

The filter sensitivity acts on the number of consecutive equal samples that should be detected on one of the LPTIM inputs to consider a signal level change as a valid transition.

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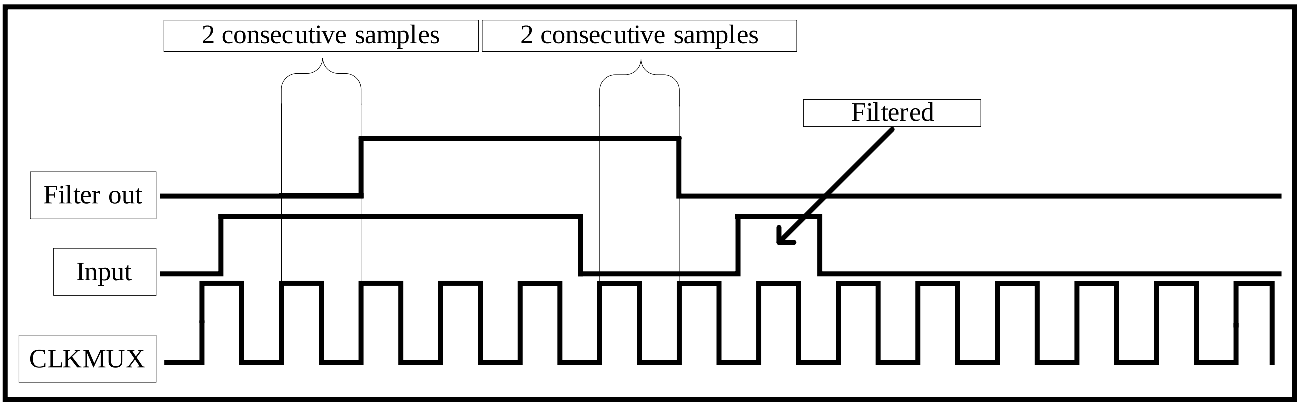
Figure 13-2 shows an example of glitch filter behavior when detected a 2 consecutive samples.

Figure 13-2 Glitch filter timing diagram



Note: If no internal clock is used, the glitch filter needs to be turned off by clearing LPTIM_CFG.CLKFLT[1:0] and LPTIM_CFG.TRIGFLT[1:0] bits. If glitch filter is not used, the user can use a digital filter in the comparator or an external analog filter to remove the glitch.

13.4.4 Timer enable

The LPTIM_CTRL.LPTIMEN bit is used to enable/disable the LPTIM kernel logic. After setting the LPTIM_CTRL.LPTIMEN bit, a delay of two counter clock is needed before the LPTIM is turned on.

The LPTIM_CFG and LPTIM_INTEN registers must be modified only when the LPTIM is turned off.

13.4.5 Trigger multiplexer

The LPTIM counter can be triggered either by software or by an active edge on one of the 8 trigger inputs.

The trigger source is configured through LPTIM_CFG.TRGEN[1:0] bits. LPTIM_CFG.TRGEN[1:0] = ‘00’, the trigger is selected as LPTIM_CTRL.TSTCM or LPTIM_CTRL.SNGMST bit, which can be set by software. The other values of LPTIM_CFG.TRGEN[1:0] are for the active edge configuration of the trigger. The internal counter will start once an active edge is detected.

LPTIM_CFG.TRGSEL[2:0] is used to select one of the 8 trigger inputs only when LPTIM_CFG.TRGEN[1:0] is not equal to ‘00’.

If LPTIM is using external trigger, which will be considered as asynchronous triggers. For asynchronous triggers, the LPTIM needs two counter clock cycles latency for synchronization.

If timeout function is disabled, new trigger event will be ignored if the LPTIM is already started.

Note: Any write to the LPTIM_CTRL.SNGMST/ LPTIM_CTRL.TSTCM bit will be discarded if the LPTIM is not enabled.

Table 13-2 9 trigger inputs corresponding to LPTIM_CFG.TRGSEL[2:0] bits

Control bits	Corresponding trigger input

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000	PB6 or PC3
001	RTC alarm A
010	RTC alarm B
011	RTC_TAMP1
100	RTC_TAMP2
101	RTC_TAMP3
110	COMP1_OUT
111	COMP2_OUT

13.4.6 Operating mode

The LPTIM has two operating modes:

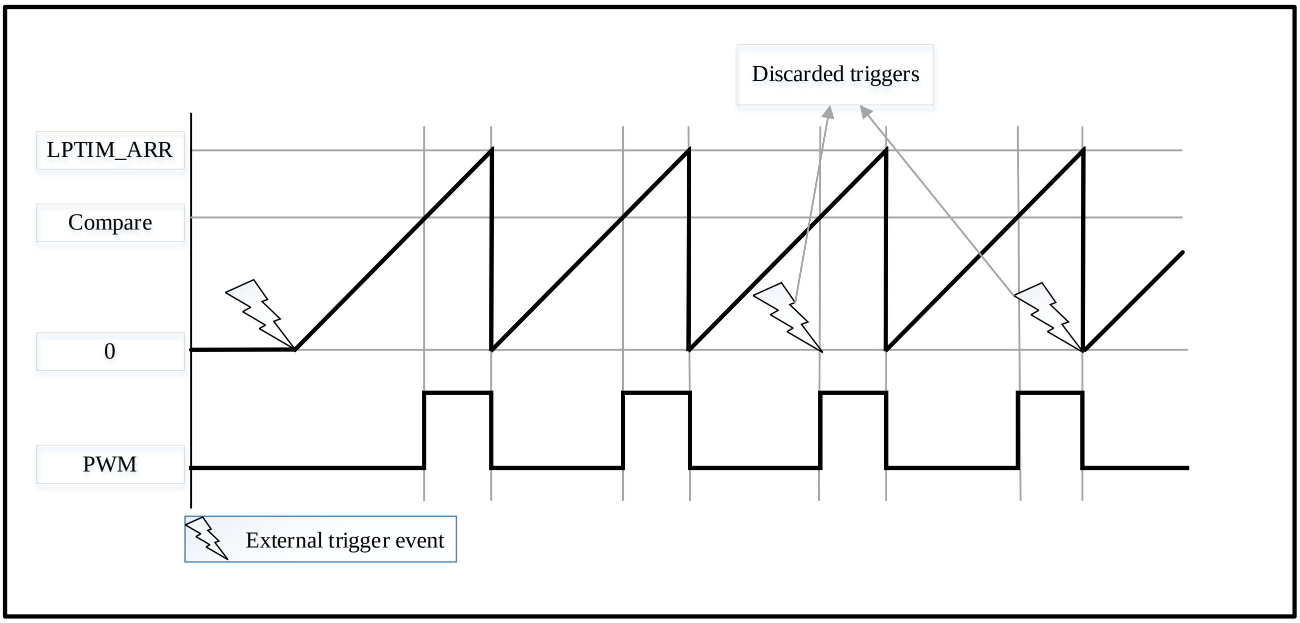
- Continuous mode: A trigger event will start the LPTIM and it will continue running until the user switched off the LPTIM.
- One-shot mode: A trigger event will start the LPTIM and it will stop when the counter value reached LPTIM_ARR.ARRVAL[15:0].

Continuous mode:

LPTIM_CTRL.TSTCM bit must be set to enable the continuous mode. If LPTIM uses external trigger, the internal counter will start when an external trigger event arrives after LPTIM_CTRL.TSTCM bit is set. After the continuous mode starts, hardware will discard any subsequent external trigger event.

If software trigger is used, setting LPTIM_CTRL.TSTCM bit will start the internal counter for continuous mode. Any subsequent external trigger event will be discarded as shown in Figure 13-3.

Figure 13-3 LPTIM output waveform, Continuous counting mode configuration



LPTIM_CTRL.SNGMST and LPTIM_CTRL.TSTCM bits can only be set when the LPTIM is enabled (The LPTIM_CTRL. LPTIMEN bit is set to '1').

It is possible to switch from one-shot mode to continuous mode. Setting LPTIM_CTRL.SNGMST bit will switch the

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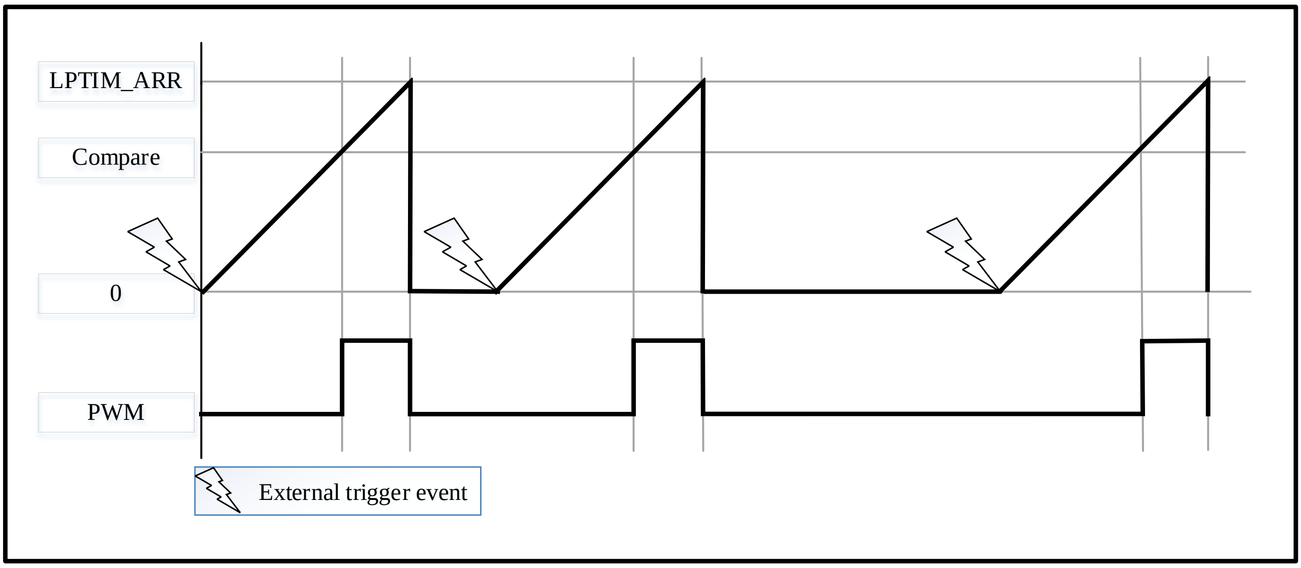
LPTIM to one-shot counting mode if continuous counting mode was previously selected. The counter stops as soon as it reaches the LPTIM_ARR register value if timer enable. If the one-shot counting mode was previously selected, setting LPTIM_CTRL.TSTCM bit to 1 will switch the LPTIM to continuous counting mode. Counter will restart as soon as LPTIM_ARR register value is reached if timer enable.

One-shot mode:

LPTIM_CTRL.SNGMST bit must be set to enable the one-shot mode. A trigger event will re-start the LPTIM. Hardware will abandon all the trigger events after the internal counter starts and before the counter value equal to LPTIM_ARR.ARRVAL[15:0] value.

If an external trigger is selected, after each external trigger event that arrivers after the LPTIM_CTRL.SNGMST bit is set, and after the timer register is stopped (containing a zero value), the timer is restarted for a new count cycle, as shown in Figure 13-4.

Figure 13-4 PTIM output waveform, single counting mode configuration



One-time mode activated:

The one-time mode is used when the LPTIM_CFG.WAVE bit is set. In one-time mode, the counter is started once when the first trigger event happens, the hardware will discard any subsequent trigger event, as shown Figure 13-5.

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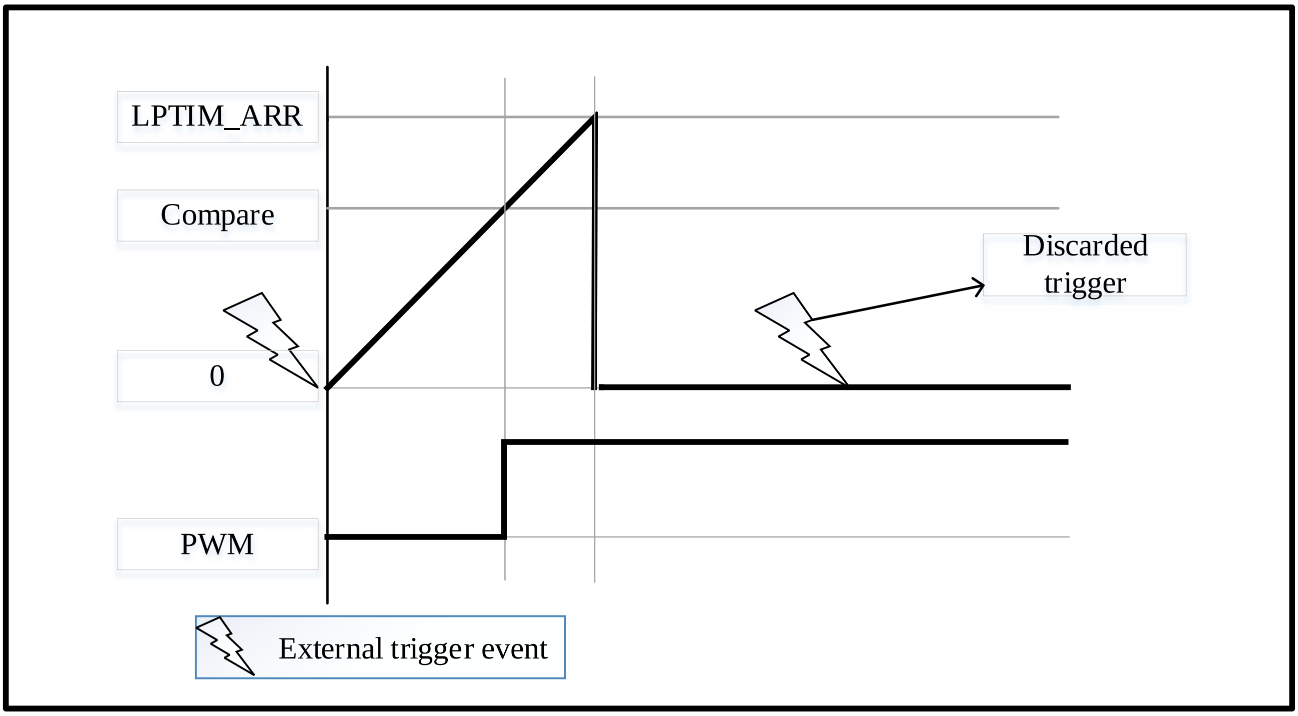
Figure 13-5 LPTIM output waveform, Single counting mode configuration and One-time mode activated



In case of software start (LPTIM_CFG.TRGEN[1:0] = '00'), the LPTIM_CTRL.SNGMST setting will start the counter for one-shot counting.

13.4.7 Waveform generation

The LPTIM auto-reload register(LPTIM_ARR) and compare register(LPTIM_COMP) are used for generating LPTIM output waveforms.

LPTIM supported waveforms are shown as below:

- PWM waveform: LPTIM output is set when a COMP match event happens. (I.E. the LPTIM_CNT register value matched the LPTIM_COMP register value.) The LPTIM output is reset when a ARR match happens. (I.E. the LPTIM_CNT register value matched the LPTIM_ARR register value.)
- One-pulse waveform: The first pulse is triggered same as PWM waveform, then the output is permanently reset when the ARR match happens.
- One-time mode: the output waveform is similar to the One-pulse mode except that the output is kept to the last signal level (depends on the output configured polarity).

Above waveform configuration require that LPTIM_ARR register value must be configured bigger than the LPTIM_COMP register value.

The LPTIM output waveform can be configured through the LPTIM_CFG.WAVE bit as follow:

- Clearing the LPTIM_CFG.WAVE bit will force the LPTIM to generate a PWM waveform or a single-pulse

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waveform depending on the set bit (LPTIM_CTRL.TSTCM or LPTIM_CTRL.SNGMST).

- LPTIM_CTRL.WAVE bit equals to ‘1’ forces the LPTIM to generate a One-time mode waveform.

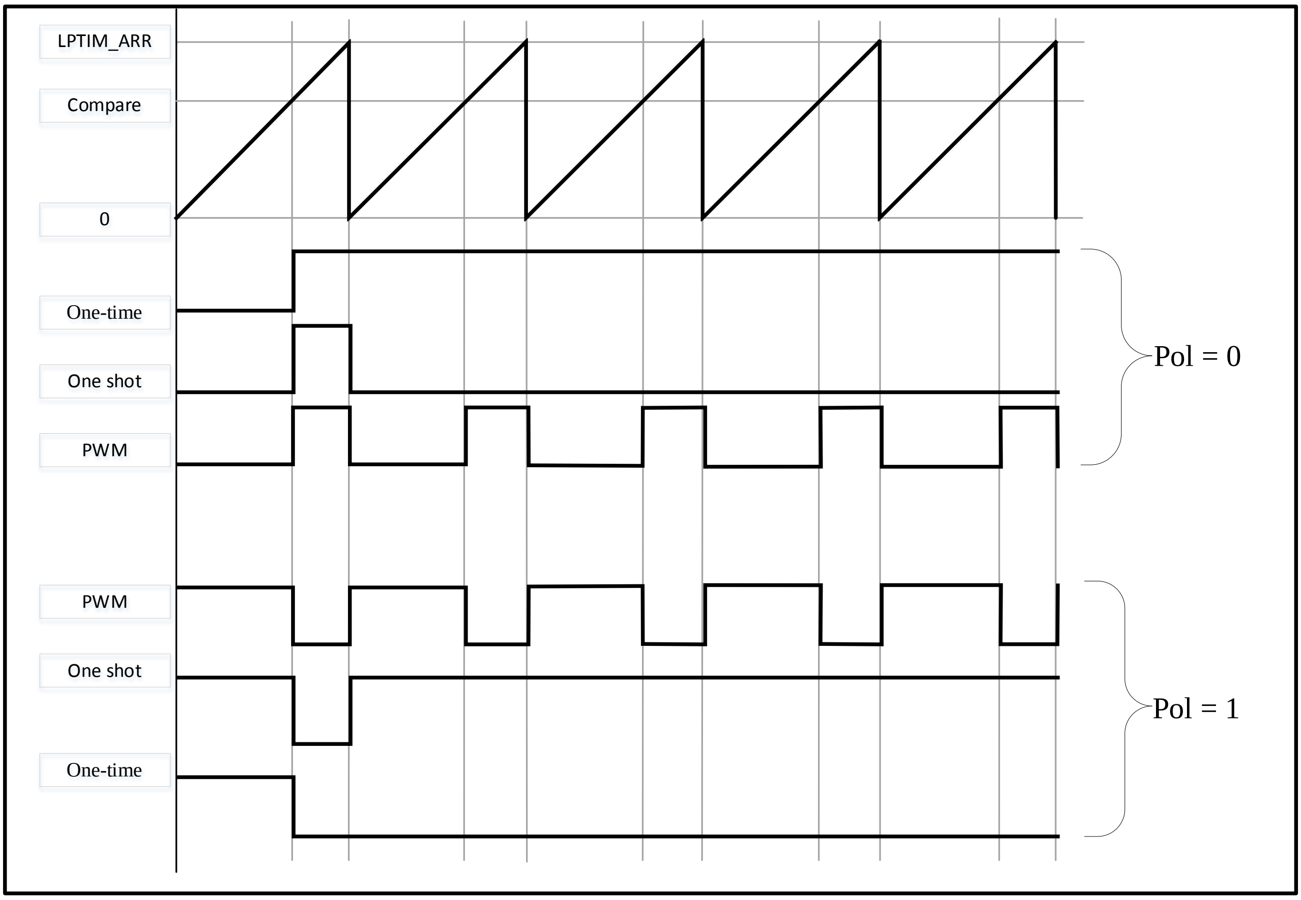
The LPTIM_CFG.WAVEPOL bit controls LPTIM output polarity. The output idle steady level will change immediately after the user configured the polarity, even when the timer is disabled.

Signals with frequencies up to the LPTIM clock frequency divided by 2 can be generated. Only when LPTIM counter counting internal clock active edge can achieve clock frequency divided by 2.

(I.E. LPTIM_CFG.CLKSEL = 0, LPTIM_CFG.CLKPOL[1:0] = 10, LPTIM_COMP.CMPVAL[15:0] = ’d1(50% duty cycle)/’d2, LPTIM_ARR.ARRVAL[15:0] = ’d3. d1,d2 and d3 means decimal 1, 2, 3)

Figure 13-6 below shows the three possible waveforms that can be generated on the LPTIM output. Also, it shows the effect of the polarity change using the LPTIM_CFG.WAVEPOL bit.

Figure 13-6 Waveform generation



13.4.8 Register update

The LPTIM_ARR register and LPTIM_COMP register can be updated immediately after a software write operation. If the LPTIM is started, the LPTIM_ARR register and LPTIM_COMP register can be updated when counter overflow.

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The LPTIM APB interface and the LPTIM kernel logic use different clocks, so there is some latency between the software write through APB bus and the moment when these values are available to the kernel logic. During this latency period, any additional write into these registers must be avoided.

The update method of LPTIM_ARR and LPTIM_COMP registers is determined by the LPTIM_CFG.RELOAD bit:

- LPTIM_CFG.RELOAD bit equals to '1': LPTIM_ARR and LPTIM_COMP registers are updated when counter overflow, if the LPTIM already started. When counter overflow, latency = 2~3 APB clock period.
- LPTIM_CFG.RELOAD bit equals to '0': LPTIM_ARR and LPTIM_COMP registers are updated after any software write access. Latency = 2~3 APB clock period + 2~3 LPTIM internal prescaled clock period.

The LPTIM_INTSTS.ARRUPD flag and the LPTIM_INTSTS.CMPUPD flag indicate when the write operation is completed to respectively the LPTIM_ARR register and the LPTIM_COMP register.

After a write to the LPTIM_ARR register or the LPTIM_COMP register, any successive write before respectively the LPTIM_INTSTS.ARRUPD flag or the LPTIM_INTSTS.CMPUPD flag be set, will lead to unpredictable results. So a new write operation to the same register can only be performed when the previous write operation is completed.

13.4.9 Counter mode

The internal counter can count external trigger events from LPTIM Input1 or internal clock cycles. This can be configured through LPTIM_CFG.CLKSEL and LPTIM_CFG.CNTMEN bits.

If LPTIM is counting external triggers, user can configure LPTIM_CFG.CLKPOL[1:0] bits to select the active edge from rising edge, falling edge or both edges.

The count modes below can be selected, depending on LPTIM_CFG.CLKSEL and LPTIM_CFG.CNTMEN bits values:

- LPTIM_CFG.CLKSEL = 0: the LPTIM use an internal clock source to clock.
  - LPTIM_CFG.CNTMEN = 0, The LPTIM is configured to be clocked by an internal clock source and the LPTIM counter is configured to be updated following each internal clock pulse.
  - LPTIM_CFG.CNTMEN = 1, The LPTIM external Input1 is sampled with the internal clock provided to the LPTIM. In order to not miss any event, the frequency of the changes on the external Input1 signal should never exceed the frequency of the internal clock provided to the LPTIM. Also, the internal clock provided to the LPTIM must not be pre-scaled (LPTIM_CFG.CLKPRE[2:0] = 000).
- LPTIM_CFG.CLKSEL = 1: the LPTIM use an external clock source to clock.
  - LPTIM_CFG.CNTMEN bit value is don't care. In this configuration, the LPTIM has no need for an internal clock source (except if the glitch filters are enabled). The signal injected on the LPTIM external Input1 is used as system clock for the LPTIM. This configuration is suitable for operation modes where no embedded oscillator is enabled.
  - For this configuration, the LPTIM counter can be updated either on rising edges or falling edges of the input1 clock signal but not on both rising and falling edges.
  - Since the signal injected on the LPTIM external Input1 is also used to clock the LPTIM kernel logic, there

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is some initial latency (after the LPTIM is enabled) before the counter is incremented. More precisely, the first five active edges on the LPTIM external Input1 (after LPTIM is enable) are lost.

13.4.10 Encoder mode

The Encoder mode can handle signals from quadrature encoders which used to detect angular position of rotary elements. The encoder mode allows the counter counts the events within 0 and LPTIM_ARR.ARRVAL[15:0] value. (0 up to LPTIM_ARR.ARRVAL[15:0] or LPTIM_ARR.ARRVAL[15:0] to 0). In this case, user must configure LPTIM_ARR.ARRVAL[15:0] before enable the counter. From external Input1 and Input2, a clock is generated for the counter. The counting direction depends on the phase between these two input signals.

The Encoder mode is only available when the LPTIM use an internal clock source to clock. The signals frequency on both Input1 and Input2 inputs must not exceed the LPTIM internal clock frequency divided by 4. This is mandatory in order to guarantee a proper operation of the LPTIM.

The change of counting direction is updated by the two Down and Up flags in the LPTIM_INTSTS register. Also, an interrupt can be generated for both direction change events if enabled through the LPTIM_INTEN register.

User can enable Encoder mode by setting LPTIM_CFG.ENC bit. And the LPTIM need to be configured in continuous mode first.

When Encoder mode is active, the LPTIM counter is modified automatically following the speed and the direction of the incremental encoder. Therefore, its content always represents the encoder’s position. The count direction, signaled by the Up and Down flags, correspond to the rotation direction of the encoder rotor.

According to the edge polarity configured using the LPTIM_CFG.CLKPOL[1:0] bits, different counting scenarios are possible. The following table summarizes the possible combinations, assuming that Input1 and Input2 do not switch at the same time.

Table 13-3 Encoder counting scenarios

Trigger edge	**The signal is opposite (Input1 For Input2, Input2 For Input1)**	**Input1 signal**		**Input2 signal**	
		Rising	**Falling**	**Rising**	**Falling**
Rising Edge	High	Down	No count	Up	No count
	Low	Up	No count	Down	No count
Falling Edge	High	No count	Up	No count	Down
	Low	No count	Down	No count	Up
Both Edges	High	Down	Up	Up	Down
	Low	Up	Down	Down	Up

The following figure shows a counting sequence for Encoder mode where both-edge polarity is configured.

Caution: *In this mode the LPTIM must be clocked by an internal clock source, so the LPTIM_CFG.CLKSEL bit must be maintained to its reset value which is equal to ‘0’. Also, the prescaler division ratio must be equal to its reset value which is 1 (LPTIM_CFG.CLKPRE[2:0] bits must be ‘000’).*

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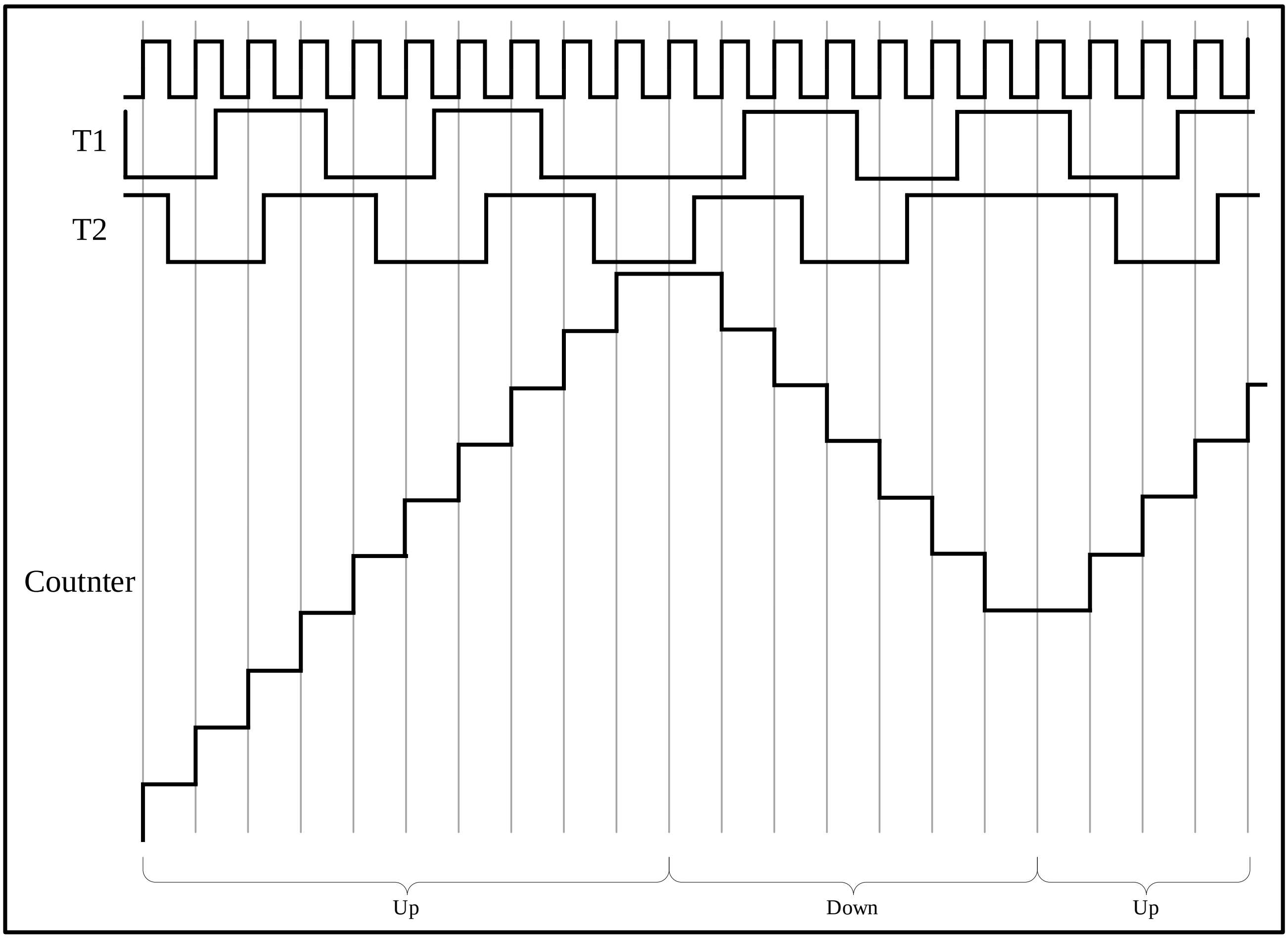
Figure 13-7 Encoder mode counting sequence



13.4.11 Non-orthogonal encoder mode

This mode allows handling signals from non-quadrature encoders, which is used to detect sub-sequent positive pulses from external interface. Non-Encoder interface mode acts simply as an external clock with direction selection. This means that the counter just counts continuously between 0 and the auto-reload value programmed into the LPTIM_ARR register (0 up to ARR or ARR down to 0 depending on the direction). Therefore you must configure LPTIM_ARR before starting. From the two external input signals, Input1 and Input2, a clock signal is generated to clock the LPTIM counter. The order between those two signals determines the counting direction.

The Non-Encoder mode is only available when the LPTIM is clocked by an internal clock source. The signals frequency on both Input1 and Input2 inputs must not exceed the LPTIM internal clock frequency divided by 4. This is mandatory in order to guarantee a proper operation of the LPTIM.

Direction change is signalized by the two Down and Up flags in the LPTIM_INTSTS register. Also, an interrupt can be generated for both direction change events if enabled through the LPTIM_INTEN register.

To activate the Non-Encoder mode the LPTIM_CFG.NENC bit has to be set to ‘1’. The LPTIM must first be configured in Continuous mode.

When Non-Encoder mode is active, the LPTIM counter is modified automatically following the speed and the

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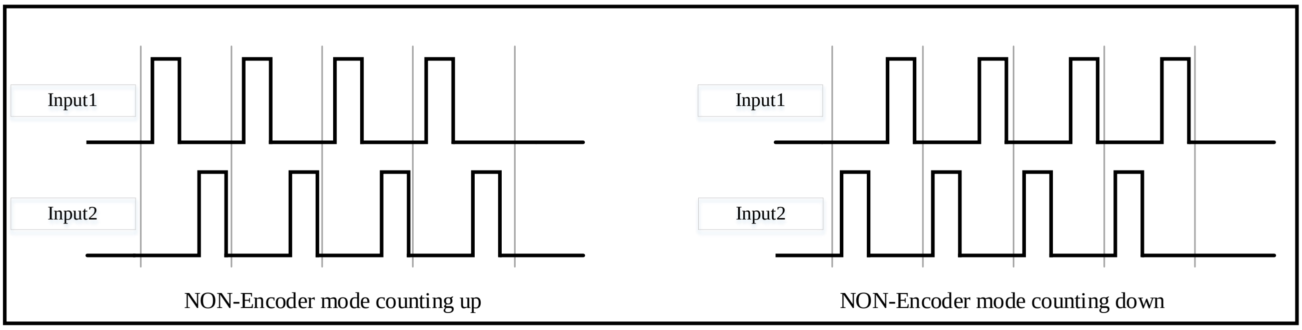
direction of the incremental encoder. Therefore, its content always represents the encoder's position. The count direction, signaled by the Up and Down flags, correspond to the rotation direction of the encoder rotor.

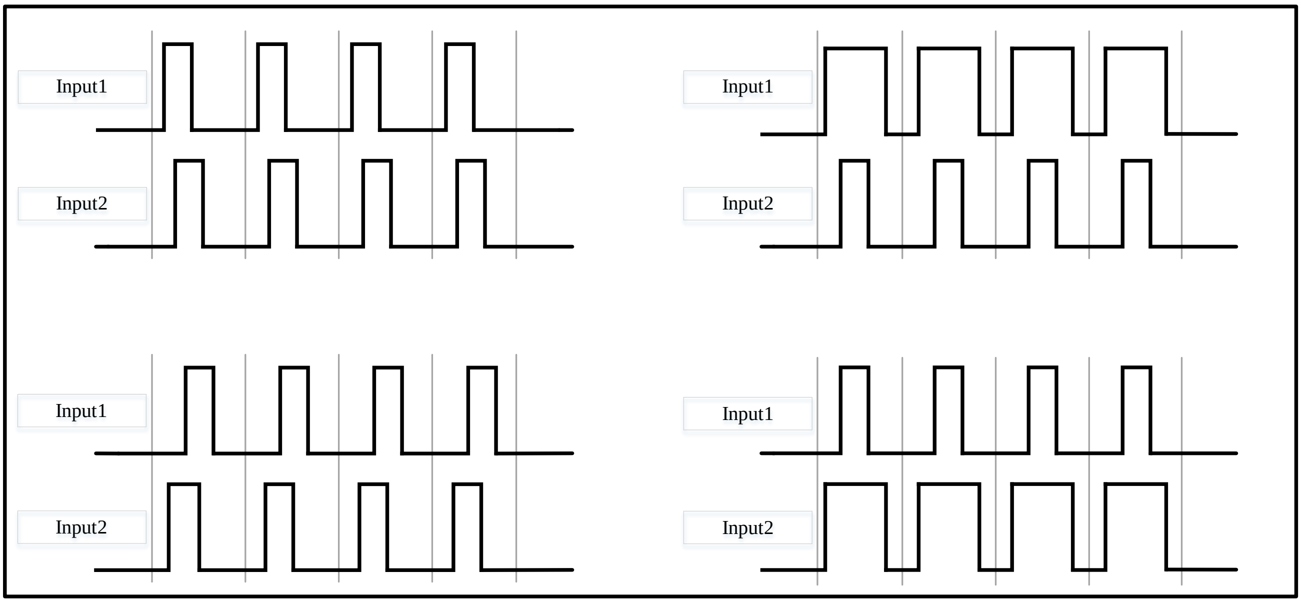
The following two waveforms, the decoder module can work properly, when there is no case that both Input1 and Input2 are high.

Figure 13-8 Input waveforms of Input1 and Input2 when the decoder module is working normally



If the Input1 and Input2 waveform is as following, the decoder module can't work properly. The counter will ignore these waveforms and keep the previous value.

Figure 13-9 Input1 and Input2 input waveforms when decoder module is not working



13.4.12 Timeout function

When LPTIM_CFG.TIMOUTEN bit is enable, the LPTIM counter will be reset by an active edge from one selected trigger input.

When timeout function is used, the LPTIM counter will be reset and re-start by a selected trigger input event. If no trigger occurs within the configured time, the compare match event will happen. The waiting time is configured through the timeout value.

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13.4.13 LPTIM interrupts

The following events generate an interrupt/wake-up event, if they are enabled through the LPTIM_INTEN register:

- Compare match
- Auto-reload match (whatever the direction if encoder mode)
- External trigger event
- Autoreload register write completed
- Compare register write completed
- Direction change (encoder mode), programmable (up / down / both).

Note: If any bit in the LPTIM_INTEN register (Interrupt Enable Register) is set after that its corresponding flag in the LPTIM_INTSTS register (Status Register) is set, the interrupt is not asserted.

Table 13-4 Interruption events

Corresponding interrupt event	**Describe**
Compare match	Interrupt flag is set when LPTIM_CNT(counter register value) = LPTIM_COMP(compare register value).
Auto reload match	Interrupt flag is set when LPTIM_CNT(counter register value) = LPTIM_ARR (auto-reload register value).
External trigger event	Interrupt flag is set when an external trigger event is detected.
Auto-reload register update OK	Interrupt flag is set when the write operation to the LPTIM_ARR register is complete.
Compare register update OK	Interrupt flag is set when the write operation to the LPTIM_COMP register is complete.
Direction change	Used in Encoder mode. Two interrupt flags are embedded to signal direction change: – UP flag indicated that the count direction is changed to count up – DOWN flag indicated that the count direction is changed to count down

13.5 LPTIM registers

13.5.1 LPTIM register overview

Table 13-5 LPTIM register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	LPTIM_INTSTS	Reserved																									DOWN	UP	ARRUPD	CMPUPD	EXTRIG	ARRM	CMPM
	Reset Value																										0	0	0	0	0	0	0
004h	LPTIM_INTCLR	Reserved																									DOWNCF	UPCF	ARRUPDCF	CMPUPDCF	EXTRIGCF	ARRMCF	CMPMCF
	Reset Value																										0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
008h	LPTIM_INTEN	Reserved																									DOWNIE	UPIE	ARRUPDIE	CMPUPDIE	EXTRIGIE	ARRMIE	CMPMIE
	Reset Value																										0	0	0	0	0	0	0
00Ch	LPTIM_CFG	Reserved						NENC	ENC	CNTMEN	RELOAD	WAVEPOL	WAVE	TIMOUTEN	TRGEN[1:0]		Reserved	TRGSEL[2:0]			Reserved	CLKPRE[2:0]			Reserved	TRIGFLT[1:0]		Reserved	CLKFLT[1:0]		CLKPOL[1:0]		CLKSEL
	Reset Value							0	0	0	0	0	0	0	0	0		0	0	0		0	0	0		0	0		0	0	0	0	0
010h	LPTIM_CTRL	Reserved																													TSTCM	SNGMST	LPTIMEN
	Reset Value																														0	0	0
014h	LPTIM_COMP	Reserved																CMPVAL[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LPTIM_ARR	Reserved																ARRVAL[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
01Ch	LPTIM_CNT	Reserved																CNTVAL[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

13.5.2 LPTIM interrupt and status register (LPTIM_INTSTS)

Address offset: 0x00

Reset value: 0x0000 0000

31–16
Reserved

15–7	6	5	4	3	2	1	0
Reserved	DOWN	UP	ARRUPD	CMPUPD	EXTRIG	ARRM	CMPM
	r	r	r	r	r	r	r

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	DOWN	Change counter direction to down. In Encoder mode, hardware will set DOWN bit to inform the application the counter direction.
5	UP	Change counter direction up.

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Bit Field	Name	Description
		In Encoder mode, hardware will set UP bit to inform the application the counter direction.
4	ARRUPD	Auto-reload value updated to register. Hardware sets ARRUPD to inform application that LPTIM_ARR register has been written by the APB1 bus successfully. For more details, see 13.4.8.
3	CMPUPD	Compare value updated to register. Hardware sets COMPUPD to inform application that LPTIM_COMP register has been written by the APB1 bus successfully. For more details, see 13.4.8.
2	EXTRIG	External trigger valid event. Hardware sets EXTRIG to inform application that a valid external trigger edge has occurred. If the trigger is discarded when timer has already started, then this flag is not set.
1	ARRM	Auto-reload match. Hardware set this to inform application that LPTIM_CNT register value reached the LPTIM_ARR register's value.
0	CMPM	Compare match. Hardware set this to inform application that LPTIM_CNT register value reached the LPTIM_COMP register's value.

13.5.3 LPTIM interrupt clear register (LPTIM_INTCLR)

Address offset: 0x04

Reset value: 0x0000 0000

31–16
Reserved

15–7	6	5	4	3	2	1	0
Reserved	DOWN CF	UP CF	ARRUPD CF	CMPUPD CF	EXTRIG CF	ARRM CF	CMPM CF
	w	w	w	w	w	w	w

Bit Field	Name	Description
31：7	Reserved	Reserved, the reset value must be maintained.
6	DOWNCF	Direction change to down Clear Flag Writing 1 to this bit clear the DOWN flag in the LPTIM_INTSTS register
5	UPCF	Direction change to UP Clear Flag Writing 1 to this bit clear the UP flag in the LPTIM_INTSTS register
4	ARRUPDCF	Autoreload register update OK Clear Flag Writing 1 to this bit clears the ARRUPD flag in the LPTIM_INTSTS register
3	CMPUPDCF	Compare register update OK Clear Flag Writing 1 to this bit clears the CMPUPD flag in the LPTIM_INTSTS register

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Bit Field	Name	Description
2	EXTRIGCF	External trigger valid edge Clear Flag Writing 1 to this bit clears the EXTRIG flag in the LPTIM_INTSTS register
1	ARRMCF	Autoreload match Clear Flag Writing 1 to this bit clears the ARRM flag in the LPTIM_INTSTS register
0	CMPMCF	compare match Clear Flag Writing 1 to this bit clears the CMPM flag in the LPTIM_INTSTS register

13.5.4 LPTIM interrupt enable register (LPTIM_INTEN)

Address offset: 0x08

Reset value: 0x0000 0000

Note: The LPTIM_INTEN register must only be modified when the LPTIM is disabled (LPTIM_CTRL.LPTIMEN bit reset to '0')

31–16
Reserved

15–7	6	5	4	3	2	1	0
Reserved	DOWN IE	UP IE	ARRUPD IE	CMPUPD IE	EXTRIG IE	ARRM IE	CMPM IE
	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	DOWNIE	Direction change to down interrupt enable bit. 0: DOWN interrupt disabled 1: DOWN interrupt enabled
5	UPIE	Direction change to up interrupt enable bit. 0: UP interrupt disabled 1: UP interrupt enabled
4	ARRUPDIE	Auto reload register update succeeded interrupt enable bit. 0: ARRUPD interrupt disable 1: ARRUPD interrupt enable
3	CMPUPDIE	Compare register update succeeded interrupt enable bit. 0: CMPUPD interrupt disabled 1: CMPUPD interrupt enabled
2	EXTRIGIE	External trigger valid edge interrupt enable bit. 0: EXTRIG interrupt disabled 1: EXTRIG interrupt enabled
1	ARRMIE	Auto reload match interrupt enable bit. 0: ARRM interrupt disabled 1: ARRM interrupt enabled
0	CMPMIE	Compare match interrupt enable bit. 0: CMPM interrupt disabled

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Bit Field	**Name**	**Description**
		1: CMPM interrupt enabled

13.5.5 LPTIM configuration register (LPTIM_CFG)

Address offset: 0x0C

Reset value: 0x0000 0000

Note: The LPTIM_CFG register must only be modified when the LPTIM is disabled (LPTIM_CTRL.LPTIMEN bit reset to '0')

31:26	25	24	23	22	21	20	19	18:17	16
Reserved	NENC	ENC	CNTMEN	RELOAD	WAVEPOL	WAVE	TIMOUTEN	TRGEN[1:0]	Reserved
	rw	rw	rw	rw	rw	rw	rw	rw	

15:13	12	11:9	8	7:6	5	4:3	2:1	0
TRGSEL[2:0]	Reserved	CLKPRE[2:0]	Reserved	TRIGFLT[1:0]	Reserved	CLKFLT[1:0]	CLKPOL[1:0]	CLKSEL
rw		rw		rw		rw	rw	rw

Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	NENC	Non-Orthogonal Encoder mode enable 0: Non-Orthogonal Encoder mode disabled 1: Non-Orthogonal Encoder mode enabled
24	ENC	Encoder mode enable 0: Encoder mode disabled 1: Encoder mode enabled
23	CNTMEN	counter mode enabled The CNTMEN bit selects clock source for the LPTIM counter: 0: Counter is incremented following each internal clock pulse 1: Counter is incremented following each valid clock pulse on the LPTIM external Input1
22	RELOAD	Registers update mode The RELOAD bit controls the LPTIM_ARR and the LPTIM_COMP registers update mode 0: Registers are updated after each APB1 bus write access 1: Registers are updated at the end of the current LPTIM period *Note: When RELOAD=0, ARRUPD and CMPUPD interrupts cannot be generated, the LPTIM_ARR and LPTIM_COMP registers need to be configured before enabling LPTIM*
21	WAVEPOL	Waveform shape polarity The WAVEPOL bit controls the output polarity 0: The LPTIM output reflects the compare results between LPTIM_ARR and LPTIM_COMP registers 1: The LPTIM output reflects the inverse of the compare results between

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Bit Field	Name	Description
		LPTIM_ARR and LPTIM_COMP registers
20	WAVE	Waveform shape The WAVE bit controls the output shape 0: Deactivate Set-once mode, PWM / One Pulse waveform (depending on LPTIM_CTRL.TSTCM or LPTIM_CTRL.SNGMST bit) 1: Activate the Set-once mode
19	TIMOUTEN	Timeout enable 0: A trigger event arriving when the timer is already started will be ignored 1: A trigger event arriving when the timer is already started will reset and restart the counter
18:17	TRGEN[1:0]	Trigger enable and polarity The TRGEN bits controls whether the LPTIM counter is started by an external trigger or not. If the external trigger option is selected, three configurations are possible for the trigger active edge: 00: Software trigger (counting start is initiated by software) 01: Rising edge is the active edge 10: Falling edge is the active edge 11: Both edges are active edges
16	Reserved	Reserved, the reset value must be maintained.
15:13	TRGSEL[2:0]	Trigger selector The TRGSEL bits select the trigger source that will serve as a trigger event for the LPTIM among the below 8 available sources: 000: PB6 or PC3 001: RTC alarm A 010: RTC alarm B 011: RTC_TAMP1 100: RTC_TAMP2 101: RTC_TAMP3 110: COMP1_OUT 111: COMP2_OUT
12	Reserved	Reserved, the reset value must be maintained.
11:9	CLKPRE[2:0]	Clock division factor bit. 000: / 1 001: / 2 010: / 4 011: / 8 100: / 16 101: / 32 110: / 64 111: / 128
8	Reserved	Reserved, the reset value must be maintained.

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Bit Field	Name	Description
7:6	TRIGFLT[1:0]	Configure the data filter trigger bit. The TRIGFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an internal trigger before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: Any trigger active level change is considered as a valid trigger. 01: Trigger active level change must be stable for at least 2 clock periods before it is considered as valid trigger. 10: Trigger active level change must be stable for at least 4 clock periods before it is considered as valid trigger. 11: Trigger active level change must be stable for at least 8 clock periods before it is considered as valid trigger.
5	Reserved	Reserved, the reset value must be maintained.
4:3	CLKFLT[1:0]	Digital filter external clock input configuration The CLKFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an external clock signal before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: Any external clock signal level change is considered as a valid transition. 01: External clock signal level change must be stable for at least 2 clock periods before it is considered as valid transition. 10: External clock signal level change must be stable for at least 4 clock periods before it is considered as valid transition. 11: External clock signal level change must be stable for at least 8 clock periods before it is considered as valid transition.
2:1	CLKPOL[1:0]	Clock Polarity If LPTIM is clocked by an external clock source: When the LPTIM is clocked by an external clock source, CLKPOL bits is used to configure the active edge or edges used by the counter: 00: The rising edge is the active edge used for counting 01: The falling edge is the active edge used for counting 10: Both edges are active edges. 11: Not allowed *Note: When both external clock signal edges are considered active ones, the LPTIM must also be clocked by an internal clock source with a frequency equal to at least four time the external clock frequency.* If the LPTIM is configured in Encoder mode (LPTIM_CFG.ENC bit is set): 00: The encoder rising edgecounting mode. 01: The encoder falling edge counting mode. 10: The encoder both edges counting mode.
0	CLKSEL	Clock selector The CLKSEL bit selects which clock source the LPTIM will use: 0: LPTIM is clocked by internal clock source (APB1 clock or any of the embedded

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Bit Field	Name	Description
		oscillators) 1: LPTIM is clocked by an external clock source through the LPTIM external Input1

13.5.6 LPTIM control register (LPTIM_CTRL)

Address offset: 0x10

Reset value: 0x0000 0000

31–16
Reserved

15–3	2	1	0
Reserved	TSTCM	SNGMST	LPTIMEN
	rw	rw	rw

Bit Field	**Name**	**Description**
31:3	Reserved	Reserved, the reset value must be maintained.
2	TSTCM	Timer start in Continuous mode This bit is set by software and cleared by hardware. In case of software start (LPTIM_CFG.TRGEN[1:0] = ‘00’), setting this bit starts the LPTIM in Continuous mode. If the software start is disabled (TRGEN[1:0] ≠ ‘00’), setting this bit starts the timer in Continuous mode as soon as an external trigger is detected. If this bit is set when a single pulse mode counting is ongoing, then the timer will not stop at the next match between the LPTIM_ARR and LPTIM_CNT registers and the LPTIM counter keeps counting in Continuous mode. This bit can be set only when the LPTIM is enabled. It will be automatically reset by hardware.
1	SNGMST	LPTIM start in Single pulse mode This bit is set by software and cleared by hardware. In case of software start (LPTIM_CFG.TRGEN[1:0] = ‘00’), setting this bit starts the LPTIM in single pulse mode. If the software start is disabled (LPTIM_CFG.TRGEN[1:0] ≠ ‘00’), setting this bit starts the LPTIM in single pulse mode as soon as an external trigger is detected. If this bit is set when the LPTIM is in continuous counting mode, then the LPTIM will stop at the following match between LPTIM_ARR and LPTIM_CNT registers. This bit can only be set when the LPTIM is enabled. It will be automatically reset by
0	LPTIMEN	LPTIM enable The LPTIMEN bit is set and cleared by software. 0: LPTIM is disabled 1: LPTIM is enabled

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13.5.7 LPTIM compare register (LPTIM_COMP)

Address offset: 0x14

Reset value: 0x0000 0000

Note: The LPTIM_COMP register must only be modified when the LPTIM is enabled (LPTIM_CTRL.LPTIMEN bit reset to '1')

31 ... 16
Reserved

15 ... 0
CMPVAL[15:0]
rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CMPVAL[15:0]	Compare value CMPVAL is the compare value used by the LPTIM.

13.5.8 LPTIM auto-reload register (LPTIM_ARR)

Address offset: 0x18

Reset value: 0x0000 0001

Note: The LPTIM_ARR register must only be modified when the LPTIM is enabled (LPTIM_CTRL.LPTIMEN bit reset to '1')

31 ... 16
Reserved

15 ... 0
ARRVAL[15:0]
rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	ARRVAL[15:0]	Auto reload value ARRVAL is the autoreload value for the LPTIM. This value must be strictly greater than the LPTIM_COMP.CMPVAL[15:0] value.

Note: The LPTIM clock source selects the internal clock source (LPTIM_CFG. CKSLE = 0), and the counter is configured to increment for each valid clock pulse on Input1 (LPTIM_CFG. CNTMEN = 1), and the maximum count value of the counter is ARRVAL - 1.

13.5.9 LPTIM counter register (LPTIM_CNT)

Address offset: 0x1C

Reset value: 0x0000 0000

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31															16
Reserved															

15															0
CNTVAL[15:0]															
r															

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CNTVAL[15:0]	Counter value When the LPTIM is running with an asynchronous clock, reading the LPTIM_CNT register may return unreliable values. So in this case it is necessary to perform two consecutive read accesses and verify that the two returned values are identical. If identical, the reading is reliable.

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14 Real time clock (RTC)

14.1 Introduction

- The real-time clock (RTC) is an independent BCD timer/counter
- The software supports daylight saving time compensation
- Programmable periodic automatic wake-up timer
- Two programmable alarm clocks
- Two 32-bit registers contain programming alarm clock, hour, minute, second, year, month, day (day), week (day of the week)
- Two independent 32-bit registers contain programming alarm, sub-second
- Digital precision calibration function
- Reference clock detection: a more accurate external clock source (50 or 60Hz) can be used to improve calendar accuracy
- Three tamper detection events with configurable filtering and internal pull-ups
- Timestamp function
- 20 backup registers to save data in low power mode
- Multiple interrupt/event wake-up sources, including alarm A, alarm B, wake-up timer, timestamp, tamper
- Automatically perform monthly compensation for 28, 29 (leap year), 30 and 31 days
- After the Backup domain is reset, all RTC registers are protected against possible accidental write access
- As long as the RTC is enabled and the voltage remains within the operating range, the RTC will not stop regardless of the device state (RUN, LP RUN, LP SLEEP, SLEEP, STOP2 or STANDBY state)
- Support to wake up MCU from supporting low power consumption mode (LP RUN mode,SLEEP mode, LP SLEEP mode, STOP2 mode and STANDBY mode).

14.2 Main feature

Main function	Describe
Clock	RTC clock can be selected from LSI, LSE and HSE, which are 40KHz, 32.768KHz and HSE / 32 respectively
Reset	The APB interface is reset by the system, and some registers synchronized by the RTC module through the APB will be reset The following registers will be cleared when the system is reset

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Main function	Describe
	● RTC_SUBS ● RTC_TSH ● RTC_DATA ● RTC_INITSTS (some bits) RTC core can be reset by backup domain reset Resets the RTC and preserves the contents of some registers in low power modes, including: ● RTC_CTRL ● RTC_PRE ● RTC_CALIB ● RTC_SCTRL ● RTC_TSSS, RTC_TST and RTC_TSD ● RTC_TMPCFG ● RTC_WKUPT ● RTC_ALRMASS/RTC_ALRMA ● RTC_ALRMBSS/RTC_ALRMB ● RTC_OPT ● RTC_BKP(1~20)
Calendar	Calendars are divided into subseconds, seconds, minutes, hours (12 or 24 format), days (day of the week), date (day), month and year. These data are stored in shadow registers in the APB module.
Wakeup Timer	The output register RTC_OUT can be configured to send wake-up events to GPIO. At the same time, it also can be configured as an interrupt/event to wake up the CPU in SLEEP，LP SLEEP，LP RUN，STOP2 modes.
Alarm	Programmable alarm clock and interrupt function. The alarm can be triggered by any combination of the calendar fields. When the alarm event occurs the alarm flag can be sent to GPIO through RTC_OUT register, and it also can be used to wake up the CPU or exit from the low power state; SLEEP，LP SLEEP, LP RUN，STOP2 and STANDBY modes.
Tamper	3 Tamper detection logic are a source of system Wakeup should a Tamper event happen on one of the input lines. The Tamper event also causes an erase of Back up registers when enabled. It is also a source of hardware trigger to LP Timer.

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Main function	Describe
Timestamp	Time-stamp function for GPIO event saving. It is a source to Wakeup system from low power modes. Alternatively a tamper event could be a source of Time-stamp event.
Interrupts/events	Alarm A/Alarm B interrupt/event Wakeup interrupt/event Timestamp interrupt/event Tamper interrupt/event
Backup registers	20 independent backup registers

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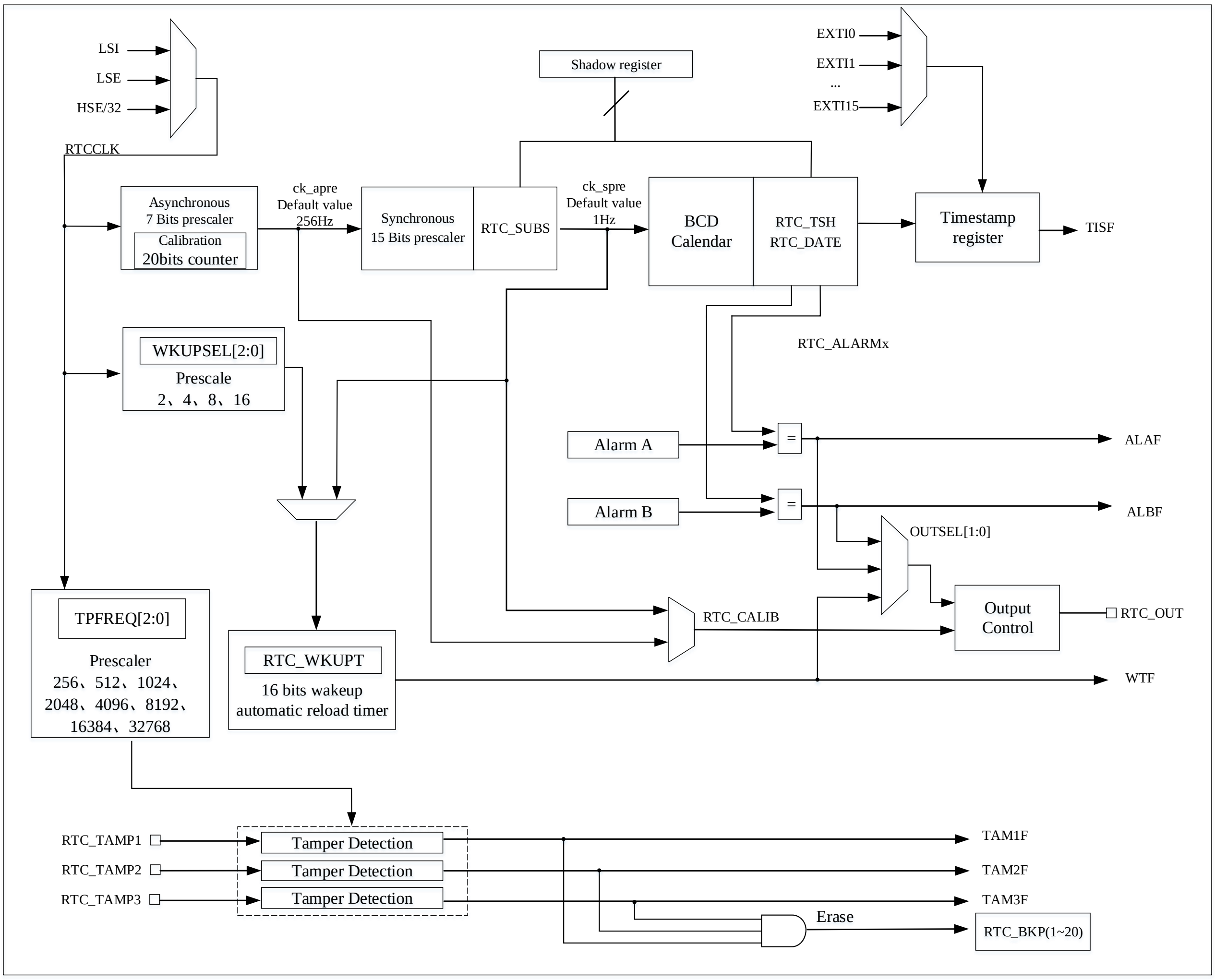
14.3 Function description

14.3.1 RTC block diagram

Figure 14-1 RTC Block Diagram



RTC includes the following modules:

- Alarm A and Alarm B event/interrupts
- Timestamp event/interrupt
- Tamper event/interrupt
- 20 32-bit backup registers
- RTC output function:
  - 256 Hz or 1Hz clock output (LSE frequency is 32.768 kHz).
  - Alarm clock output (polarity configurable), Alarm A and Alarm B are optional.

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- ◆ Auto wakeup output (polarity configurable).

- ■ RTC input function:
  - ◆ Timestamp event detection
  - ◆ 50 or 60Hz reference clock input
  - ◆ Tamper event detection
- ■ Control PC13 by configuring output register:
  - ◆ Set RTC_OPT.TYPE bit to configure open-drain/push-pull output of PC13

14.3.2 GPIO controlled by RTC

Timestamp input come from IOM (mapped to PC13) or EXTI module, if EXIT module is needed to start, please refer to the timestamp trigger source selection register (EXTI_TS_SEL) for details.

RTC_OUT (Alarm, Wakeup event or calibration output (256Hz or 1Hz)) is mapped to PC13. Regardless of the PC13 GPIO configuration, the PC13 pin configuration is controlled by the RTC as an output.

PC13 can be used as RTC TAMPER1 tamper detection pin, PA0 can be used as RTC TAMPER2 tamper detection pin, and PA8 can be used as RTC TAMPER3 tamper detection pin.

PB15 can be used as RTC_REFCLKIN reference clock input pin.

14.3.3 RTC register write protection

PWR_CTRL1.DRBP bit (see Power control register 1 (PWR_CTRL1)) is cleared in default, so PWR_CTRL1.DRBP bit must set to “1” to enable write access to the RTC register. Once the backup domain is reset, all write protection RTC registers are write protected. All write protection RTC registers require the following steps to unlock write protection:

- ■ Write “0xCA” into RTC_WRP register.
- ■ Write “0x53” into RTC_WRP register.

After unlocking these registers, it cannot be write protected unless the RTC is soft reset or power cycled. The unlocking mechanism only checks the write operation to the RTC_WRP register. During or before and after the unlocking process, the write operation to other registers does not affect the unlocking result.

14.3.4 RTC clock and prescaler

RTC clock source:

- ■ LSE clock
- ■ LSI clock
- ■ HSE/32 clock

For the purpose of reduction of power consumption, the prescaler is divided into 2 programmable prescalers, they

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are asynchronous prescaler and synchronous prescaler. If both prescaler are used, it is recommended that the value of the asynchronous divider be as large as possible.

- A 7-bit asynchronous prescaler which is given by RTC_PRE.DIVA[6:0] bits
- A 15-bit synchronous prescaler which is given by RTC_PRE.DIVS[14:0] bits

The formula for f_{ck_apre} and f_{ck_spre} are given below:

$$f_{ck\_apre} = \frac{f_{RTCCLK}}{RTC\_PRE.DIVA[6:0]+1}$$

$$f_{ck\_spre} = \frac{f_{RTCCLK}}{(RTC\_PRE.DIVS[14:0]+1)*(RTC\_PRE.DIVA[6:0]+1)}$$

- The ck_apre clock is used to driven RTC_SUBS sub-second down counter. When it reaches 0, reload RTC_SUBS with the value of RTC_PRE.DIVS[14:0].

14.3.5 RTC calendar

There are three shadow registers, they are RTC_DATE, RTC_TSH and RTC_SUBS. The RTC time and date registers can be accessed through the shadow registers. It is also possible to access them directly to avoid the synchronization waiting time. The three shadow registers are as follow:

- RTC_DATE: set and read date
- RTC_TSH: set and read time
- RTC_SUBS: read sub-second

After every two RTCCLK cycles, the current calendar value is copied to the shadow register, and RTC_INITSTS.RSYF bit is set to 1. This process is not performed in low power (stop & standby) modes. While exiting these modes, the shadow register updates the values after 2 RTCCLK cycles.

By default, when user try to access the calendar register, it accesses the contents of the shadow register instead. User can access the calendar register directly by setting the RTC_CTRL.BYPS bit.

When RTC_CTRL.BYPS=0, calendar values are from shadow registers, when reading RTC_SUBS, RTC_TSH or RTC_DATE register, it is necessary to make ensure the frequency of APB1 clock (f_{APB1}) is at least 7 times the frequency of RTC clock (f_{RTCCLK}), and APB1 clock frequency lower than RTC clock frequency is not allowed in any case. System reset will reset shadow registers.

14.3.6 Calendar initialization and configuration

The value of prescaler and calendar can be initialized by the following steps:

- Enter initialization mode by setting “1” to RTC_INITSTS.INITM bit, then wait for RTC_INITSTS.INITF flag to be set 1.
- Set RTC_PRE.DIVS[14:0] and RTC_PRE.DIVA[6:0] value.
- Write the initial calendar values include time and date into the shadow registers (RTC_TSH and RTC_DATE)

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and configure the time format (12 or 24 hours) by the RTC_CTRL.HFMT bit.

- Exit initialization mode by clearing the RTC_INITSTS.INITM bit.

The values of calendar counter will automatically loaded from shadow registers after 4 RTCCLK clock cycles, then the calendar counter restarts.

Note: Before RTC enters initialization mode,it is necessary to ensure that the RTC_SUBS.SS[15:0] value is not less than 2.

14.3.7 Calendar reading

1. Reading calendar value when RTC_CTRL.BYPS=0

Calendar value is read from shadow registers if RTC_CTRL.BYPS=0. In order to read RTC calendar registers (RTC_SUBS, RTC_TSH and RTC_DATE) correctly, APB1 clock frequency must be set equal to or greater than 7 times of RTC clock frequency. In any case, APB1 clock frequency must not be less than RTC clock frequency.

If APB1 clock frequency is not equal to or greater than 7 times of RTC clock frequency, refer to the following process to read calendar value.

- Read the data of RTC_SUBS ,RTC_TSH and RTC_DATE twice.
- Compare the data read twice, if they are equal, the read data can be considered correct; if they are not equal, read the data for the third time.
- The third time read data can be considered correct.

Shadow registers (RTC_SUBS, RTC_TSH and RTC_DATE) are updated every two RTCCLK cycles. If user want to read calendar value in a short time(less than two RTCCLK cycles), RTC_INITSTS.RSYF bit must be cleared by software after the first time read.

In some cases, it is necessary to wait until RTC_INITSTS.RSYF bit is set 1 before read calendar value.

- After waking up from the low power modes (STOP mode, STANDBY mode), clear RTC_INITSTS.RSYF bit, then wait RTC_INITSTS.RSYF bit is set again.
- System reset.
- Calendar complete initialization.
- Calendar complete synchronization.

2. Reading calendar value when RTC_CTRL.BYPS=1

Reading the calendar value directly from the calendar counter if RTC_CTRL.BYPS=1. The advantage of this configuration is that read calendar value without delay after wakeup from the low power mode, the disadvantage is that these data of RTC_SUBS, RTC_TSH and RTC_DATE may not be at a time.

To ensure the correctness of read calendar value, it is necessary to read RTC_SUBS, RTC_TSH and RTC_DATE twice, then compare the data read twice, if they are equal, the read data can be considered correct.

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14.3.8 Calibration clock output

When RTC_CTRL.COEN set to 1, PC13 pin will output calibration clock. If RTC_CTRL.CALOSEL=0 and RTC_PRE.DIVA[6:0] = 0x7F, the RTC_CALIB frequency results is f_{RTCCLK}/RTC_PRE.DIVA[6:0]. This is equivalent to a calibration output of 256 Hz when the RTCCLK frequency is 32.768 kHz. The rising edge is recommended for there is slight jitter on the falling edge.

When RTC_CTRL.CALOSEL=1 and "RTC_PRE.DIVS[14:0]+1" is a non-zero integer multiple of 256, the RTC_CALIB frequency is given by the formula f_{RTCCLK}/(256 * (DIVA+1)). This is equivalent to 1Hz calibration output when the RTCCLK frequency is 32.768 kHz and RTC_PRE.DIVA[6:0] = 0x7F.

Note: When the RTC_CALIB or RTC_ALARM output is selected, the RTC_OUT pin (PC13) is automatically configured as output,the duty cycle is about $4\%*10^{-6}$.

14.3.9 Programmable Alarm

RTC has 2 programmable alarms: Alarm A and Alarm B.

TC alarm can be enabled or disable by RTC_CTRL.ALxEN bit. If the alarm value match the calendar values, the RTC_INITSTS.ALxF flag will be set 1. Each calendar field can be selected to trigger alarm interrupt if RTC_CTRL.ALxIEN bit is enabled.

Alarm output: Alarm A and Alarm B can be mapped to RTC_ALxRM output when RTC_CTRL.OUTSEL[1:0] is selected, and output polarity can be configured by RTC_CTRL.OPOL bit.

Note: If the second field is selected (RTC_ALARMx.MASK1 bit reset), RTC_PRE.DIVS[14:0] must be larger than 3 to ensure correct operation.

14.3.10 Alarm configuration

Alarm A and Alarm B should be configured in the following below:

- Disable Alarm A/Alarm B by clearing RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit.
- Configure the Alarm x registers (RTC_ALRMxSS/RTC_ALARMx)
- Enable Alarm A/Alarm B interrupt by set RTC_CTRL.ALAIEN/RTC_CTRL.ALBIEN bit(this step can be selected as needed)
- Enable Alarm A/Alarm B by setting RTC_CTRL.ALAEN/ RTC_CTRL.ALBEN bit.

14.3.11 Alarm output

When RTC_CTRL.OUTSEL[1:0] !=0, RTC_ALARM alternate function output is enable. There are Alarm A output, Alarm B output and Wakeup output to choose by the value of RTC_CTRL.OUTSEL[1:0] bits.

RTC_CTRL.OPOL bit control the polarity of the Alarm A, Alarm B or Wakeup output.

RTC_OPT.TYPE bit control the RTC_ALARM pin to output open drain or output pull-up.

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When RTC_CALIB or RTC_ALARM output is selected, the RTC_OUT pin (PC13) is automatically configured as output, the duty cycle is about 4%*10^{-6}.

14.3.12 Periodic automatic wakeup

A 16-bit programmable auto-load down counter can generate periodic wakeup flag when reach 0. Periodic automatic wakeup can be enabled by setting RTC_CTRL.WTEN.

There are two wake-up input clock sources can be selected:

- RTC clock (RTCCLK) divided by 2/ 4/8/16.

  Assume RTCCLK comes from LSE (32.768KHz), wake-up interrupt period can be configured range from 122us to 32s under the resolution down to 61us.

- Internal clock ck_spre.

  Assume ck_spre frequency is 1Hz, the available wake-up time range from 2s to 18h, and the resolution is 1 second.

  - When RTC_CTRL.WKUPSEL [2:0] = 10x, the period is range from 2s to 18h.

After RTC_CTRL.WTEN bit is set to 1, the down counter is running and when it reaches 0, RTC_INITSTS.WTF will be set and the device can exit from low power mode when the periodic wakeup interrupt is enabled by setting the RTC_CTRL.WTIEN bit.

Periodic wakeup output: periodic wakeup can be mapped to RTC_ALxRM output when RTC_CTRL.OUTSEL[1:0] is selected, the RTC_OUT pin(PC13) is automatically configured as output, and output polarity can be configured by RTC_CTRL.OPOL bit.

14.3.13 Wakeup timer configuration

The wakeup timer automatic reload value should be configured in the following below:

- Disable wakeup timer by clearing RTC_CTRL.WTEN bit, then wait for RTC_INITSTS.WTWF flag to be set 1.
- Select wake up timer clock by set RTC_CTRL.WKUPSEL[2:0] bits.
- Configure the wake-up automatic reload value by set RTC_WKUPT.WKUPT[15:0] bits.
- Enable Wakeup interrupt by set RTC_CTRL.WTIEN bit(this step can be selected as needed)
- Enable wakeup timer by setting RTC_CTRL.WTEN bit.

14.3.14 Timestamp function

Timestamp can be enabled by setting RTC_CTRL.TSEN bit to 1. When a timestamp event is detected on the RTC_TS pin, the calendar values of the event will be stored in the timestamp register (RTC_TSSS, RTC_TST, RTC_TSD), and RTC_INITSTS.TISF is set to 1. Timestamp event can generate an interrupt if RTC_CTRL.TSIEN is set to 1. If a new timestamp event is detected when RTC_INITSTS.TISF has been set to 1 already, the hardware sets RTC_INITSTS.TISOVF flag to 1, and the timestamp registers (RTC_TST and RTC_TSD) will continue to hold the

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value of the previous event, which means timestamp registers(RTC_TST and RTC_TSD) data will not change when RTC_INITSTS.TISF=1.

After the timestamp event caused by the synchronization process occurs again, RTC_INITSTS.TISF is set to 1 in 2 RTC_CLK cycles. There is no delay in the generation of RTC_INITSTS.TISOVF. This means that if two timestamp events are very close, this can cause RTC_INITSTS.TISOVF to be "1" and RTC_INITSTS.TISF to be "0". Therefore, after detecting that RTC_INITSTS.TISF is "1", then detect RTC_INITSTS.TISOVF bit.

Tamper event can trigger timestamp event when RTC_TMPCFG.TPTS bit is set to 1.

If timestamp events are enabled, the timestamp will capture the calendar read in the timestamp register. When both tamper events and timestamp events are enabled, tamper events can also result in timestamp capture. Timestamp events can be generated on any of the 16 GPIO ports selected by EXTI. The GPIO pins in each port are selected by setting the corresponding EXTI_TS_SEL.TSSEL[3:0] bits.

14.3.15 Tamper detection

There are three tamper detection pin, RTC_TAMP1 pin is PC13, RTC_TAMP2 pin is PA0, RTC_TAMP3 pin is PA8. RTC_TAMPx pin can be used as tamper event detection function input pin. There are two detection modes, edge detection mode and level detection mode with configurable filtering function.

When RTC_TAMPx event is detected, RTC_BKP(1~20) registers will be erased if RTC_TMPCFG.TPxONE=0.

Tamper detection initialization

There are three tamper detection pins, each of them can be configured independently. User need to configure tamper detection before enable RTC_TMPCFG.TPxEN bit. When the tamper event is detected after tamper detection is enable, if RTC_TMPCFG.TPxINTEN is set to 1, tamper event can generate an interrupt and RTC_INITSTS.TAMxF bit will be set 1.

When RTC_INITSTS.TAMxF is set to 1, a new tamper event on the same pin cannot be detected.

Timestamp on tamper event

Any tamper event can cause a timestamp event when RTC_INITSTS.TPTS is set to 1, and RTC_INITSTS.TISF bit and RTC_INITSTS.TISOVF bit will be set as a normal timestamp event.

Edge detection of tamper input

When RTC_TMPCFG.TPFLT[1:0] bits set to 0, tamper detection is set to edge detection, and one of rising edge or falling edge is controlled by RTC_TMPCFG.TPxTRG bit. The RTC_TAMPx pin will generate a tamper detection event when corresponding edge is detected.

Because of RTC_BKP(1~20) can be reset when tamper event is detected, it is necessary to ensure that tamper event detection and writing to RTC_BKP(1~20) will not occur at the same time. It is recommended to start the tamper detection function after writing RTC_BKP(1~20).

Filtered level detection of RTC_TAMPx input

When RTC_TMPCFG.TPFLT[1:0] bits set to 1/2/3, tamper detection is set to level detection. The value of RTC_TMPCFG.TPFLT[1:0] determines the number of samples.

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The internal pull-up resistance of tamper pin can be precharged before each sampling, and the precharge time is controlled by RTC_TMPCFG.TPPRCH[1:0] bits. Precharge will be disabled when RTC_TMPCFG.TPPUDIS set 1.

Using RTC_TMPCFG.TPFREQ[2:0] to determine the sampling frequency of level detection can optimize the best balance between tamper detection delay and pull-up power consumption.

14.3.16 Daylight saving time configuration

Daylight saving time function can be controlled by RTC_CTRL.SU1H, RTC_CTRL.AD1H, and RTC_CTRL.BAKP bits. Calendar will subtract one hour when set RTC_CTRL.SU1H bit to 1, and add one hour when set RTC_CTRL.AD1H to 1. RTC_CTRL.BAKP can be used to remember this adjustment or not.

14.3.17 RTC reset

All system reset resources will reset some of the calendar shadow registers (RTC_SUBS, RTC_TSH and RTC_DATE) and RTC initialization status register (RTC_INITSTS) to their default values.

On the contrary, the Backup reset is used to reset the following registers and they are not affected by the system reset. The RTC current calendar register, the RTC control register (RTC_CTRL), the pre-divider register (RTC_PRE), the RTC calibration register (RTC_CALIB), the RTC time-stamp register (RTC_TSSS, RTC_TST and RTC_TSD), the wake-up timer registers (RTC_WKUPT), the Alarm A and the Alarm B registers (RTC_ALRMASS/RTC_ALARMA and RTC_ALRMBSS/RTC_ALARMB), and the option registers (RTC_OPT).

In addition, when the LSE clock is used, if the reset source is different from the Backup domain reset the RTC keeps on running under system reset (the list of the RTC domain registers is not affected by system reset, refer to RTC clock). When a Backup domain reset occurs, the RTC stops working and all RTC registers are set to their reset values.

14.3.18 RTC sub-second register shift operation

When the value of calendar has a sub-second deviation compared to the external precision clock, the shift function can be used to improve the precision of calendar.

Calendar can use RTC_SCTRL.AD1S and RTC_SCTRL.SUBF[14:0] bits to control maximum delay or advance 1s. The resolution of the adjustment is 1/(RTC_PRE.DIVS[14:0]+1) second, it means the higher value of RTC_PRE.DIVS[14:0] , the higher of the resolution. However, to keep the synchronous prescaler output at 1Hz, the higher RTC_PRE.DIVS[14:0] means the lower RTC_PRE.DIVA[6:0], then more power consuming.

Note: Before starting a shift operation, user must check RTC_SUBS.SS[15] bit is 0.

Whenever write RTC_SCTRL register, the RTC_INITSTS.SHOPF flag will be set by hardware, which indicate a shift operation is pending. Once this shift operation is complete, the bit is cleared by hardware.

14.3.19 RTC digital clock precision calibration

Digital precision calibration is achieved by adjusting the number of RTC clock pulses in the calibration period. Digital precision calibration resolution is 0.954 PPM with the range from -487.1 PPM to +488.5 PPM.

When the input frequency is 32768 Hz, calibration period can be configured as $2^{20}/2^{19}/2^{18}$ RTCCLK cycles or 32/16/8

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seconds. The precision calibration register (RTC_CALIB) indicates that there has RTC_CALIB.CM[8:0] RTCCLK clock cycles will be reduced during the specified period.

The value of RTC_CALIB.CM[8:0] represents the number of RTCCLK pulses to be reduced during specified period. While RTC_CALIB.CP can be used to increase 488.5 PPM, every 2^{11} RTCCLK cycles will inserts a RTCCLK pulse.

When using RTC_CALIB.CM[8:0] and RTC_CALIB.CP in combination, it can increase cycles range from -511 to +512 RTCCLK cycles, and the calibration range from -487.1 ppm to +488.5 ppm, with the resolution is about 0.954 ppm.

The effective calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * (1 + \frac{RTC\_CALIB.CP*512 - RTC\_CALIB.CM[8:0]}{2^n + RTC\_CALIB.CM[8:0] - RTC\_CALIB.CP * 512})$$

Note: n=20/19/18

Calibrated when RTC_PRE .DIVA[6:0]<3

When the asynchronous prescaler value (RTC_PRE.DIVA[6:0]) is less than 3, the RTC_CALIB.CP cannot be programmed to 1, and RTC_CALIB.CP value will be ignored if the it has been set to 1.

When RTC_PRE .DIVA[6:0]<3, the value of RTC_PRE.DIVS[14:0] should be decrease. Assume RTCCLK frequency is 32768Hz:

- When RTC_PRE .DIVA[6:0] =2, RTC_PRE.DIVS[14:0]=8189.
- When RTC_PRE .DIVA[6:0] =1, RTC_PRE.DIVS[14:0]=16379.
- When RTC_PRE .DIVA[6:0] =0, RTC_PRE.DIVS[14:0]=32759.

The effective calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * \left(1 + \frac{256 - RTC\_CALIB.CM[8:0]}{2^n + RTC\_CALIB.CM[8:0] - 265}\right)$$

Note: n=20/19/18

Verify RTC calibration

RTC output 1Hz waveform for measuring and verifying RTC precision.

Up to 2 RTCCLK cycles measurement error may occur when measure the RTC frequency in a limit measurement period. If the measurement period is the same as calibration period, the error can be eliminated.

- The calibration period is 32 seconds (default).

  Using an accurate 32-second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.447ppm (0.5 RTCCLK cycles within 32 seconds).

- The calibration period is 16 seconds.

  Using an accurate 16-second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.954ppm (0.5 RTCCLK cycles within 16 seconds).

- The calibration period is 8 seconds.

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Using an accurate 8-second period to measure the 1Hz calibration output can ensure that the measurement error is within 1.907ppm (0.5 RTCCLK cycles within 8 seconds).

Dynamic recalibration

When RTC_INITSTS.INITF=0, RTC_CALIB register can update by using following steps:

- Wait RTC_INITSTS.RECPF=0.
- A new value is written to the RTC_CALIB, then RTC_INITSTS.RECPF is automatically set to 1.
- The new calibration settings will take effect within 3 ck_apre cycles after a data write to the RTC_CALIB.

14.3.20 RTC low power mode

Lower Power Mode	RTC Working State	Exit Low Power Mode
SLEEP	Normal work	RTC interrupt
LP RUN	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup, Tamper event and Timestamp event
LP SLEEP	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup, Tamper event and Timestamp event
STOP2	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup, Tamper event and Timestamp event
STANDBY	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B, Tamper event and Timestamp event

14.4 RTC Registers

14.4.1 RTC Register overview

Table 14-1 RTC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RTC_TSH	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SCT[2:0]			SCU[3:0]			
	Reset Value										0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	0
004h	RTC_DATE	Reserved								YRT[3:0]				YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved		DAT[1:0]		DAU[3:0]			
	Reset Value									0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1			0	0	0	0	0	1
008h	RTC_CTRL	Reserved								COEN	OUTSEL[1:0]		OPOL	CALOSEL	BAKP	SU1H	AD1H	TSIEN	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	Reserved	HFMT	BYPS	REFCLKEN	TEDGE	WKUPSEL[2:0]		
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0
00Ch	RTC_INITSTS	Reserved															RECPF	TAM3F	TAM2F	TAM1F	TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
010h	RTC_PRE	Reserved									DIVA[6:0]							Reserved	DIVS[14:0]														

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value										1	1	1	1	1	1	1		0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
014h	RTC_WKUPT	Reserved																WKUPT[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
01Ch	RTC_ALARMA	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	RTC_ALARMB	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	RTC_WRP	Reserved																								PKEY[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
028h	RTC_SUBS	Reserved																SS[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	RTC_SCTRL	AD1S	Reserved																SUBF[14:0]														
	Reset Value	0																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	RTC_TST	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SET[2:0]			SEU[3:0]			
	Reset Value										0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	0
034h	RTC_TSD	Reserved								YRT[3:0]				YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved		DAT[1:0]		DAU[3:0]			
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0
038h	RTC_TSSS	Reserved																SSE[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	RTC_CALIB	Reserved																CP	CW8	CW16	Reserved				CM[8:0]								
	Reset Value																	0	0	0					0	0	0	0	0	0	0	0	0
040h	RTC_TMPCFG	Reserved							TP3MF	TP3NOE	TP3INTEN	TP2MF	TP2NOE	TP2INTEN	TP1MF	TP1NOE	TP1INTEN	TPPUDIS	TPPRCH[1:0]		TPFLT[1:0]		TPFREQ[2:0]			TPTS	TP3TRG	TP3EN	TP2TRG	TP2EN	TPINTEN	TP1TRG	TP1EN
	Reset Value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	RTC_ALRMASS	Reserved				MASKSSA[3:0]				Reserved									SSV[14:0]														
	Reset Value					0	0	0	0										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	RTC_ALRMBSS	Reserved				MASKSSB[3:0]				Reserved									SSV[14:0]														
	Reset Value					0	0	0	0										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	RTC_OPT	Reserved																															TYPE
	Reset Value																																0
050h ~ 09Ch	RTC_BKPx	BF[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.4.2 RTC Calendar Time Register (RTC_TSH)

Address offset: 0x00

Reset value: 0x0000 0000

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31–23	22	21–20	19–16
Reserved	APM	HOT[1:0]	HOU[3:0]
	rw	rw	rw

15	14–12	11–8	7	6–4	3–0
Reserved	MIT[2:0]	MIU[3:0]	Reserved	SCT[2:0]	SCU[3:0]
	rw	rw		rw	rw

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM format. 0:AM format or 24-hour format 1:PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT [2: 0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SCT[2:0]	Describes the second tens value in BCD format
3:0	SCU[3:0]	Describes the second units value in BCD format

14.4.3 RTC Calendar Date Register (RTC_DATE)

Address offset: 0x04

Reset value: 0x0000 2101

31–24	23–20	19–16
Reserved	YRT[3:0]	YRU[3:0]
	r	r

15–13	12	11–8	7–6	5–4	3–0
WDU[2:0]	MOT	MOU[3:0]	Reserved	DAT[1:0]	DAU[3:0]
r	r	r		r	r

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	YRT[3:0]	Describes the year tens value in BCD format
19:16	YRU[3:0]	Describes the year units value in BCD format
15:13	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format

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Bit field	Name	Description
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

14.4.4 RTC Control Register (RTC_CTRL)

Address offset: 0x08

Reset value: 0x0000 0000

31:24	23	22:21	20	19	18	17	16
Reserved	COEN	OUTSEL[1:0]	OPOL	CALOSEL	BAKP	SU1H	AD1H
	rw	rw	rw	rw	rw	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2:0
TSIEN	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	Reserved	HFMT	BYPS	REF CLKEN	TEDGE	WKUPSEL[2:0]
rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	COEN	Calibration output enable This bit controls RTC_CALIB output 0: Disable calibration output 1: Enable calibration output
22:21	OUTSEL[1:0]	Output selection These bits are used to select the alarm/wakeup output 00: Disable output 01: Enable Alarm A output 10: Enable Alarm B output 11: Enable Wakeup output
20	OPOL	Output polarity bit This bit is used to configure the polarity of output. 0: Outputs high level when the selected output triggers(see OUTSEL[1:0]) 1: Outputs low level when the selected output triggers(see OUTSEL[1:0])
19	CALOSEL	Calibration output selection When RTC_CTRL.COEN=1, RTCCLK = 32.768KHz and prescale at their default value (RTC_PRE.DIVA[6:0]=127 and RTC_PRE.DIVS[14:0]=255). 0: Calibration output is 256 Hz 1: Calibration output is 1 Hz
18	BAKP	Daylight saving time record This bit is written by the user 0: Not record daylight saving time 1: Record daylight saving time
17	SU1H	Subtract 1 hour (winter time change)

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Bit field	Name	Description
		1 hour will be subtracted to the calendar time when the current hour value is not 0. This bit is always read as 0. 0: No effect. 1: Subtracts 1 hour to the current time.
16	AD1H	Add 1 hour (summer time change) When this bit is set, 1 hour can be added to the calendar time. This bit is always read as. 0: No effect. 1: Adds 1 hour to the current time.
15	TSIEN	Time-stamp interrupt enable 0: Disable time-stamp interrupt. 1: Enable time-stamp interrupt.
14	WTIEN	Wakeup timer interrupt enable 0: Disable wakeup timer interrupt. 1: Enable wakeup timer interrupt.
13	ALBIEN	Alarm B interrupt enable 0: Disable Alarm B interrupt 1: Enable Alarm B Interrupt
12	ALAIEN	Alarm A interrupt enable 0: Disable Alarm A interrupt 1: Enable Alarm A interrupt
11	TSEN	Timestamp enable 0: Disable timestamp 1: Enable timestamp
10	WTEN	Wakeup timer enable 0: Disable wakeup timer 1: Enable wakeup timer
9	ALBEN	Alarm B enable 0: Disable Alarm B 1: Enable Alarm B
8	ALAEN	Alarm A enable 0: Disable Alarm A 1: Enable Alarm A
7	Reserved	Reserved, the reset value must be maintained
6	HFMT	Hour format bit 0: 24 hour format 1: Am/PM format
5	BYPS	Bypass values from the shadow registers 0: Calendar values are copied from the shadow registers, which are refreshed every two RTCCLK cycles. 1: Calendar values are copied directly from the calendar counters. *Note: If the frequency of the APB1 clock falls below seven times the frequency of*

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Bit field	Name	Description
		RTCCLK, RTC_CTRL.BYPS bit must be set to '1'
4	REFCLKEN	RTC_REFIN reference clock detection enable (50 or 60 Hz) 0: Disable RTC_REFIN detection 1: Enable RTC_REFIN detection *Note: RTC_PRE.DIVS must be 0x00FF*
3	TEDGE	Time-stamp event active edge 0: Input rising edge creates a timestamp event 1: Input falling edge creates a timestamp event TSE need to be reset when TEDGE is changed to avoid unwanted RTC_INITSTS.TISF setting.
2:0	WKUPSEL[2:0]	Wakeup clock selection 000: RTC clock is divided by 16 001: RTC clock is divided by 8 010: RTC clock is divided by 4 011: RTC clock is divided by 2 10x: ck_spre (usually 1Hz) clock is selected

14.4.5 RTC Initial Status Register (RTC_INITSTS)

Address offset: 0x0C

Reset value: 0x0000 0007

31:17	16
Reserved	RECPF
	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAM3F	TAM2F	TAM1F	TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rw	r	rc_w0	r	r	r	r	r

Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	RECPF	Recalibration pending flag The RECPF status flag is automatically set to '1' when software writes to the RTC_CALIB register, indicating that the RTC_CALIB register is blocked. After the new calibration settings are processed, this bit returns to '0'.
15	TAM3F	RTC_TAMP3 detection flag This flag is set to '1' by hardware when a tamper event is detected on the RTC_TAMP3 input pin. This flag can be cleared by software writing 0
14	TAM2F	RTC_TAMP2 detection flag This flag is set to '1' by hardware when a tamper event is detected on the RTC_TAMP2 input pin.

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Bit field	Name	Description
		This flag can be cleared by software writing 0
13	TAM1F	RTC_TAMP1 detection flag This flag is set to '1' by hardware when a tamper event is detected on the RTC_TAMP1 input pin. This flag can be cleared by software writing 0
12	TISOVF	The time-stamp overflow flag This flag is set to '1'by hardware when a time-stamp event happens when TISF bit is set. This flag can be cleared by software writing 0. It is advised to check and clear TISOVF only after clearing the TISF bit. Otherwise, an overflow might not be noticed if a timestamp event occurs immediately before the TISF bit is being cleared.
11	TISF	Time-stamp flag This flag is set to '1' by hardware when a time-stamp event happens. This flag can be cleared by software writing 0
10	WTF	Wake up timer flag This flag is set by hardware when the value of wakeup auto-reload counter reaches 0. This flag is cleared by software by writing 0. This flag must be cleared by software at least 1.5 RTCCLK periods before WTF is set again.
9	ALBF	Alarm B flag This flag is set to '1' by hardware when the time/date registers value match the Alarm B register values. This flag can be cleared by software writing 0
8	ALAF	Alarm A flag This flag is set to '1' by hardware when the time/date registers value match the Alarm A register values. This flag can be cleared by software writing 0
7	INITM	Enter Initialization mode 0: Free running mode 1: Enter initialization mode and set calendar time value, date value, and prescale value.
6	INITF	Initialization flag RTC is in initialization state when this bit is '1', and calendar time, date and prescale value can be updated. 0: Calendar time, date and prescale value can not be updated 1: Calendar time, date and prescale value can be updated
5	RSYF	Register synchronization flag This flag is set to '1' by hardware when the calendar value are copied into the shadow registers. This bit is cleared by hardware when in initialization mode, while a shift operation is pending (SHOPF = 1), or when in bypass shadow register mode (RTC_CTRL.BYPS = 1). This bit can also be cleared by software.

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Bit field	Name	Description
		It is cleared either by software or by hardware in initialization mode. 0: Calendar shadow register not yet synchronized 1: Calendar shadow register synchronized
4	INITSF	Initialization status flag This flag is set to '1' by hardware when the calendar year field is different from 0 (which is the RTC domain reset state). 0: Calendar has not been initialized 1: Calendar has been initialized
3	SHOPF	Shift operation pending flag This flag is set to '1' by hardware as soon as a shift operation is initiated by a write to the RTC_SCTRL register. It is cleared by hardware when the corresponding shift operation has been completed, note that writing to the SHOPF bit has no effect. 0: No shift operation is pending 1: A shift operation is pending
2	WTWF	Wakeup timer write flag 0: Wakeup timer configuration update is not allowed 1: Wakeup timer configuration update is allowed
1	ALBWF	Alarm B write flag This flag is set to '1' by hardware when Alarm B values can be changed, after the RTC_CTRL.ALBEN bit has been set to 0. 0: Alarm B update is not allowed 1: Alarm B update is allowed
0	ALAWF	Alarm A write flag. This flag is set to '1' by hardware when Alarm A values can be changed, after the RTC_CTRL.ALAEN bit has been set to 0. 0: Alarm A update is not allowed 1: Alarm A update is allowed

14.4.6 RTC Prescaler Register (RTC_PRE)

Address offset: 0x10

Reset value: 0x007F 00FF

31–23	22–16
Reserved	DIVA[6:0]
	rw

15	14–0
Reserved	DIVS[14:0]
	rw

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
22:16	DIVA[6:0]	Asynchronous prescaler factor f_{ck_apre} = RTCCLK/(DIVA[6:0]+1)
15	Reserved	Reserved, the reset value must be maintained
14:0	DIVS[14:0]	Synchronous prescaler factor $f_{ck\_spre} = f_{ck\_apre}$/(DIVS[14:0]+1)

14.4.7 RTC Wakeup Timer Register (RTC_WKUPT)

Address offset: 0x14

Reset value: 0x0000 FFFF

31 … 16
Reserved

15 … 0
WKUPT[15:0]
rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WKUPT[15:0]	Wake up auto-reload value bits The RTC_INITSTS.WTF flag is set every (WKUPT[15:0] + 1) ck_wut cycles when the RTC_CTRL.WTEN=1. The wakeup timer becomes 17-bits When RTC_CTRL.WKUPSEL[2]=1. *Note:* *This register change (such as the second setting or later Settings) needs to be changed in the wakeup interrupt, otherwise the changed settings will not take effect immediately, but will take effect after the next wakeup;* *In particular, when RTC_CTRL.WKUPSEL[2:0] is set to 010, the modified setting does not take effect immediately, but will take effect after wake up in the next cycle.;*

14.4.8 RTC Alarm A Register (RTC_ALARMA)

Address offset: 0x1C

Reset value: 0x0000 0000

31	30	29 28	27 … 24	23	22	21 20	19 … 16
MASK4	WKDSEL	DTT[1:0]	DTU[3:0]	MASK3	APM	HOT[1:0]	HOU[3:0]
rw	rw	rw	rw	rw	rw	rw	rw

15	14 … 12	11 … 8	7	6 … 4	3 … 0
MASK2	MIT[2:0]	MIU[3:0]	MASK1	SET[2:0]	SEU[3:0]
rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

14.4.9 RTC Alarm B Register (RTC_ALARMB)

Address offset: 0x20

Reset value: 0x0000 0000

31	30	29 28	27 24	23	22	21 20	19 16
MASK4	WKDSEL	DTT[1:0]	DTU[3:0]	MASK3	APM	HOT[1:0]	HOU[3:0]
rw	rw	rw	rw	rw	rw	rw	rw

15	14 12	11 8	7	6 4	3 0
MASK2	MIT[2:0]	MIU[3:0]	MASK1	SET[2:0]	SEU[3:0]
rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match

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Bit field	Name	Description
		1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

14.4.10 RTC Write Protection register (RTC_WRP)

Address offset: 0x24

Reset value: 0x0000 0000

31–16
Reserved

15–8	7–0
Reserved	PKEY[7:0]
	w

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	PKEY[7:0]	Write protection key Reading this byte always returns 0x00. For detail on how to unlock RTC register write protection, see chapter RTC register

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Bit field	Name	Description
		write protection.

14.4.11 RTC Sub-second Register (RTC_SUBS)

Address offset: 0x28

Reset value: 0x0000 0000

31–16
Reserved

15–0
SS[15:0]
r

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SS[15:0]	Sub-second value. The value is the counter value of synchronous prescaler. This sub-second value is calculated by the below formula: Sub-second value = (RTC_PRE.DIVS[14:0]-SS)/(RTC_PRE.DIVS[14:0]+1) *Note: SS[15:0] can be larger than RTC_PRE.DIVS[14:0] only after the shift operation is finished. In this case, the correct time/date is one second slower than the time/date indicated by RTC_TSH/RTC_DATE.*

14.4.12 RTC Shift Control Register (RTC_SCTRL)

Address offset: 0x2C

Reset value: 0x0000 0000

31	30–16
AD1S	Reserved
w	

15	14–0
Reserved	SUBF[14:0]
	w

Bit field	Name	Description
31	AD1S	Add one second 0: No add one second. 1: Add one second to the clock/calendar This bit can only be written and read as zero. Writing to this bit does not have an impact when RTC_INITSTS.SHOPF=1.
30:15	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
14:0	SUBF[14:0]	Subtract a fraction of a second There bits can only be written and read as zero.. Writing to this bit does not have an impact when RTC_INITSTS.SHOPF=1. The value which is written to SUBF[14:0] is added to the synchronous prescaler counter, and the clock will delay: Delay (seconds) =(SUBF[14:0]+1) / (DIVS[14:0] + 1) AD1S bit can be used together with the SUBF[14:0]bits: Advance (seconds) = (1 – ((SUBF[14:0]+1) / (DIVS[14:0] + 1))). *Note: RTC_INITSTS.RSYF bit will be cleared when write SUBF[14:0]. When RTC_INITSTS.RSYF=1, the shadow registers have been updated with the shifted time.*

14.4.13 RTC Timestamp Time Register (RTC_TST)

Address offset: 0x30

Reset value: 0x0000 0000

31–23	22	21–20	19–16
Reserved	APM	HOT[1:0]	HOU[3:0]
	r	r	r

15	14–12	11–8	7	6–4	3–0
Reserved	MIT[2:0]	MIU[3:0]	Reserved	SET[2:0]	SEU[3:0]
	r	r		r	r

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM notation 0: AM or 24-hour clock 1: PM
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

14.4.14 RTC Timestamp Date Register (RTC_TSD)

Address offset: 0x34

Reset value: 0x0000 0000

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31-24	23-20	19-16
Reserved	YRT[3:0]	YRU[3:0]
	r	r

15-13	12	11-8	7-6	5-4	3-0
WDU[2:0]	MOT	MOU[3:0]	Reserved	DAT[1:0]	DAU[3:0]
r	r	r		r	r

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	YRT[3:0]	Describes the year tens value in BCD format
19:16	YRU[3:0]	Describes the year units value in BCD format
15:13	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

14.4.15 RTC Timestamp Sub-second Register (RTC_TSSS)

Address offset: 0x38

Reset value: 0x0000 0000

31-16
Reserved

15-0
SSE[15:0]
r

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SSE[15:0]	Sub second value SSE[15:0] is the value in the synchronous prescaler counter. The fraction of a second is provided by the formula below: Second fraction = (RTC_PRE.DIVS[14:0] – SSE[15:0]) / (RTC_PRE.DIVS[14:0] + 1) *Note: SSE[15:0] can be larger than RTC_PRE.DIVS[14:0] only after a shift operation. In that case, the correct time/date is one second less than as indicated by RTC_TSH/RTC_DATE.*

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14.4.16 RTC Calibration Register (RTC_CALIB)

Address offset: 0x3C

Reset value: 0x0000 0000

31–16
Reserved

15	14	13	12–9	8–0
CP	CW8	CW16	Reserved	CM[8:0]
rw	rw	rw		rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	CP	Increase frequency of RTC by 488.5 ppm This feature is intended to be used along with CM[8:0]. When RTCCLK frequency is 32768 Hz, the number of RTCCLK pulses added during a 32-second window is ((512 * CP) – CM[8:0]). 0: No add pulse. 1: One RTCCLK pulse is inserted every 2^{11} pulses.
14	CW8	Select an 8-second calibration cycle period 0: Not effect. 1: Select an 8-second calibration period. When CW8 is set to ‘1’, the 8-second calibration cycle period is selected. *Note: when CW8 = 1, CM[1:0] will always be' 00'*
13	CW16	To select a 16-second calibration cycle period 0: Not effect. 1: Select a calibration period of 16 seconds. If CW8 = 1, this bit cannot be set to 1. *Note: when CW16 = 1, CM[0] will always be '0'*
12:9	Reserved	Reserved, the reset value must be maintained
8:0	CM[8:0]	Negative calibration bits The number of mask pulse out of 2^{20} RTCCLK pulses. This effectively decreases the frequency of the calendar with a resolution of 0.9537 ppm.

14.4.17 RTC Tamper Configuration Register (RTC_TMPCFG)

Address offset: 0x40

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							TP3MF	TP3NOE	TP3INTEN	TP2MF	TP2NOE	TP2INTEN	TP1MF	TP1NOE	TP1INTEN
							rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPPUDIS	TPPRCH[1:0]		TPFLT[1:0]		TPFREQ[2:0]			TPTS	TP3TRG	TP3EN	TP2TRG	TP2EN	TPINTEN	TP1TRG	TP1EN
rw	rw		rw		rw			rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained
24	TP3MF	Tamper 3 mask flag 0: Not mask tamper 3 event. 1: Mask tamper 3 event. *Note: The Tamper 3 interrupt must not be enabled when TP3MF is set.*
23	TP3NOE	Tamper 3 no erase 0: Backup registers values are erased by Tamper 3 event. 1: Backup registers values are not erased by Tamper 3 event.
22	TP3INTEN	Tamper 3 interrupt enable 0: Disable tamper 3 interrupt when TPINTEN = 0. 1: Enabled tamper 3 interrupt
21	TP2MF	Tamper 2 mask flag 0: Not mask tamper 2 event. 1: Mask tamper 2 event. *Note: The Tamper 2 interrupt must not be enabled when TP2MF is set.*
20	TP2NOE	Tamper 2 no erase 0: Backup registers values are erased by Tamper 2 event. 1: Backup registers values are not erased by Tamper 2 event.
19	TP2INTEN	Tamper 2 interrupt enable 0: Disable tamper 2 interrupt when TPINTEN = 0. 1: Enabled tamper 2 interrupt
18	TP1MF	Tamper 1 mask flag 0: Not mask tamper 1 event. 1: Mask tamper 1 event. *Note: The Tamper 1 interrupt must not be enabled when TP1MF is set.*
17	TP1NOE	Tamper 1 no erase 0: Backup registers values are erased by Tamper 1 event. 1: Backup registers values are not erased by Tamper 1 event.
16	TP1INTEN	Tamper 1 interrupt enable 0: Disable tamper 1 interrupt when TPINTEN = 0. 1: Enabled tamper 1 interrupt
15	TPPUDIS	RTC_TAMPx Pull-up disable bit. 0: Enable precharge RTC_TAMPx pins before each sampling. 1: Disable precharge RTC_TAMPx pins
14:13	TPPRCH[1:0]	RTC_TAMPx Precharge duration.

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Bit field	Name	Description
		These bits determine the the precharge time before each sampling. 0x0: 1 RTCCLK cycles 0x1: 2 RTCCLK cycles 0x2: 4 RTCCLK cycles 0x3: 8 RTCCLK cycles
12:11	TPFLT[1:0]	RTC_TAMPx filter count These bits determine the number of consecutive samples when occur active level. 0x0: Triggers a tamper event at the active level. 0x1: Triggers a tamper event after 2 consecutive samples at the active level. 0x2: Triggers a tamper event after 4 consecutive samples at the active level. 0x3: Triggers a tamper event after 8 consecutive samples at the active level.
10:8	TPFREQ[2:0]	Tamper sampling frequency This bit determines the frequency at the each RTC_TAMPx input is sampled. 0x0: Sampling once every 32768 RTCCLK (1 Hz when RTCCLK = 32.768 KHz). 0x1: Sampling once every 16384 RTCCLK. 0x2: Sampling once every 8192 RTCCLK. 0x3: Sampling once every 4096 RTCCLK. 0x4: Sampling once every 2048 RTCCLK. 0x5: Sampling once every 1024 RTCCLK. 0x6: Sampling once every 512 RTCCLK. 0x7: Sampling once every 256 RTCCLK.
7	TPTS	Tamper event trigger timestamp 0: Disable tamper event trigger timestamp 1: Enable tamper event trigger timestamp TPTS is valid even if RTC_CTRL.TSEN=0.

6	TP3TRG	Tamper 3 event trigger edge
		if TPFLT[1:0] != 00, tamper detection is in level mode:
		0: low level trigger a tamper detection event.
		1: high level trigger a tamper detection event.
		if TPFLT = 00, tamper detection is in edge mode:
		0: Rising edge trigger a tamper detection event.
		1: Falling edge trigger a tamper detection event

5	TP3EN	Tamper 3 detection enable 0: Disable tamper detection 1: Enable tamper detection

4	TP2TRG	Tamper 2 event trigger edge
		if TPFLT[1:0] != 00, tamper detection is in level mode:
		0: low level trigger a tamper detection event.
		1: high level trigger a tamper detection event.
		if TPFLT = 00, tamper detection is in edge mode:
		0: Rising edge trigger a tamper detection event.

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Bit field	Name	Description
		1: Falling edge trigger a tamper detection event
3	TP2EN	Tamper 2 detection enable 0: Disable tamper detection 1: Enable tamper detection
2	TPINTEN	Tamper event interrupt enable. 0: Disable tamper interrupt 1: Enable tamper interrupt *Note: This bit enables the interrupt of all tamper pins events, regraadless of TPxINTEN level. If this bit is cleared, each tamper event interrupt can be individually enabled by setting TPxINTEN.*

1	TP1TRG	Tamper 1 event trigger edge
		if TPFLT[1:0] != 00, tamper detection is in level mode:
		0: low level trigger a tamper detection event.
		1: high level trigger a tamper detection event.
		if TPFLT = 00, tamper detection is in edge mode:
		0: Rising edge trigger a tamper detection event.
		1: Falling edge trigger a tamper detection event

0	TP1EN	Tamper 1 detection enable 0: Disable tamper detection 1: Enable tamper detection

14.4.18 RTC Alarm A sub-second register (RTC_ALRMASS)

Address offset: 0x44

Reset value: 0x0000 0000

31:28	27:24	23:16
Reserved	MASKSSB[3:0]	Reserved
	rw	

15	14:0
Reserved	SSV[14:0]
	rw

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ...

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Bit field	Name	Description
		0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
23:15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and bit number of compared is controlled by MASKSSB[3:0].

14.4.19 RTC Alarm B sub-second register (RTC_ALRMBSS)

Address offset: 0x48

Reset value: 0x0000 0000

31:28	27:24	23:16
Reserved	MASKSSB[3:0]	Reserved
	rw	

15	14:0
Reserved	SSV[14:0]
	rw

Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ... 0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
23:15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and bit number of compared is controlled by MASKSSB[3:0].

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14.4.20 RTC Option Register (RTC_OPT)

Address offset: 0x4C

Reset value: 0x0000 0000

31 ... 16
Reserved

15 ... 1	0
Reserved	TYPE
	rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	TYPE	RTC_ALARM output type on PC13 0: Open-drain output 1: Push-pull output

14.4.21 RTC Backup registers (RTC_BKP(1~20))

Address offset: 0x50 to 0x9C

Reset value: 0x0000 0000

31 ... 16
BF[15:0]
rw

15 ... 0
BF[15:0]
rw

Bit field	Name	Description
31:0	BF[31:0]	Backup data These registers can be wrote and read by software. These registers are powered by the BKR when MR is turned off, so when the system is reset, these registers are not reset and the contents of the registers are still valid when the device is operating in a low power mode. If RTC_TMPCFG.TPxNOE=0, these registers are reset when tamper x event detection happens.

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15 Independent watchdog (IWDG)

15.1 Introduction

The N32L43x has built-in independent watchdog (IWDG) and window watchdog (WWDG) timers to solve the problems caused by software errors. Watchdog timer is very flexible to use, which improves the security of the system and the accuracy of timing control.

Independent Watchdog (IWDG) is driving by Low-speed internal clock (LSI clock) running at 40 KHz, which will still running event dead loop or MCU stuck is happening. This can provide higher safety level, timing accuracy and flexibility of watchdog. It can reset and resolve system malfunctions due to software failure. The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.

15.2 Main features

- Independent 12-bit down-counter
- RC oscillator provides independent clock source, which can operate in RUN, SLEEP, LOW POWER RUN, LOW POWER SLEEP, STOP2 and STANDBY mode.
- Reset and low-power wake-up can be matched.
- A system reset occurs when the down counter reaches 0x0000 (if watchdog activated).

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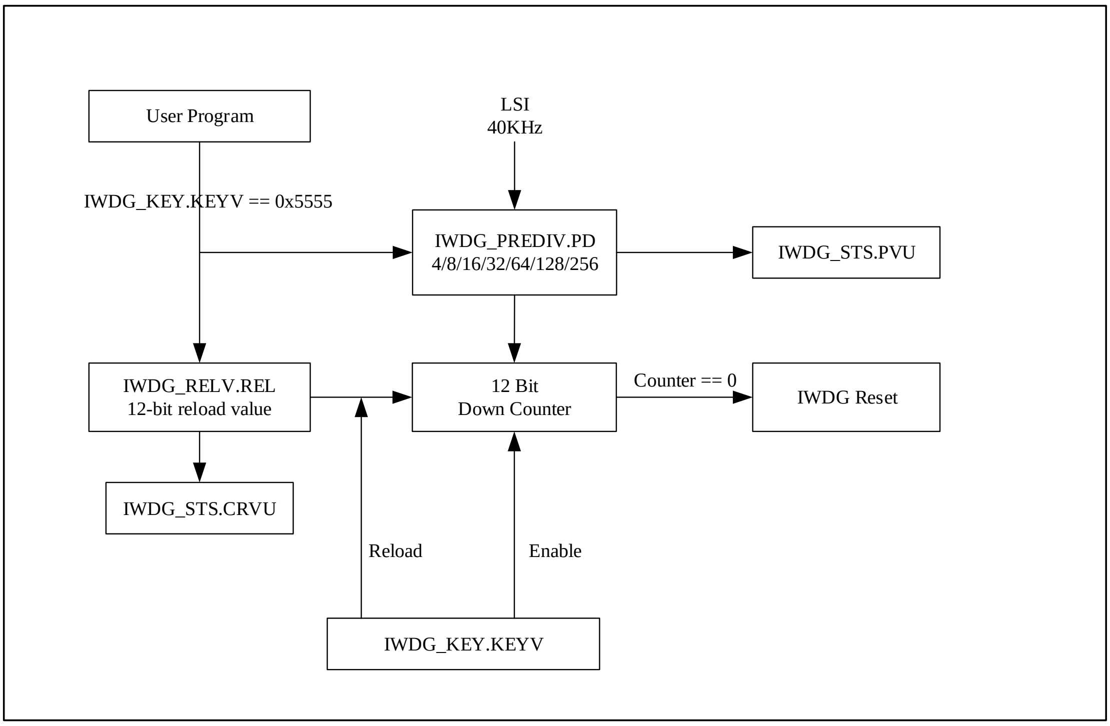
15.3 Function description

Figure 15-1 Functional block diagram of the independent watchdog module



Note: Watchdog function is in V_{DD} power supply area, and it can still work normally in RUN, SLEEP, LOW POWER RUN, LOW POWER SLEEP and STANDBY modes.

To enable IWDG, we need to write 0xCCCC to IWDG_KEY.KEYV[15:0] bits. Counter starts counting down from reset value (0xFFF). When counter count to 0x000, it generates a reset signal (IWDG_RESET) to MCU. Other than that, as long as 0xAAAA (reload request) is write to IWDG_KEY.KEYV[15:0] bits before reset, the counter value is set to the reload value in the IWDG_RELV.REL[11:0] bits and prevents the watchdog from resetting the entire device.

If the "hardware watchdog timer" function is enabled through the selection byte, the watchdog will automatically start running after the system is powered on and will generate a system reset, unless the software reloads the counter before it reaches '0'.

15.3.1 Register access protection

IWDG_PREDIV and IWDG_RELV register are write protected. To modify the value of those two register, user needs to write 0x5555 to IWDG_KEY.KEYV[15:0] bits. Writing other value enables write protections again. IWDG_STS.PVU indicates whether the pre-scaler value update is on going. IWDG_STS.CRVU indicates whether the IWDG is updating the reload value. The hardware sets the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit when the pre-scaler value and/or reload value is updating. After the pre-scaler value and/or reload value update is complete, the hardware clears the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit.

The reload operation (IWDG_KEY.KEYV[15:0] configured with value of 0xAAAA) will also cause the registers to become write protected again.

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15.3.2 Debugging mode

In debug mode (Cortex-M4 core stops), IWDG counter will either continue to work normally or stops, depending on DBG_CTRL.IWDG_STOP bit in debug module. If this bit is set to '1', the counter stops. The counter works normally when the bit is '0'. See the chapter on debugging module for details 29.3.2.

15.4 User interface

IWDG module user interface contains 4 registers: Key Register (IWDG_KEY), Pre-scale Register (IWDG_PREDIV), Reload Register (IWDG_RELV) and Status Register (IWDG_STS).

15.4.1 Operate flow

When IWDG is enable from reset from software (write 0xAAAA to IWDG_KEY.KEYV[15:0] bits) or hardware (clear WDG_SW bit). It starts counting down from 0xFFF. Down counting gap is determined by pre-scale LSI clock. Once the counter is reloaded, each new round will start from the value in IWDG_RELV.REL[11:0] instead of 0xFFF.

When program is running normally, software needs to feed IWDG before counter reaches 0 and start a new round of down counting. When counter reach 0, this indicates program malfunction. IWDG generates reset signal under this circumstance.

If user wants to configure IWDG pre-scale and reload value register, it needs to write 0x5555 to IWDG_KEY.KEYV[15:0] first. Then confirm IWDG_STS.CRVU bit and IWDG_STS.PVU bit. IWDG_STS.CRVU bit indicates reload value update is ongoing, IWDG_STS.PVU indicates Pre-scale divider ratio is updating. Only when those two bit are 0 then user can update corresponding value. When update is on-going, hardware sets corresponding bit to 1. At this time, reading IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] is invalid since data needs sync to LSI clock domain. The value read from IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] will be valid after hardware clears the IWDG_STS.PVU bit or IWDG_STS.CRVU bit.

If the application uses more than one reload value or pre-scaler value, it must wait until the IWDG_STS.CRVU bit is reset before changing the reload value, the same as changing the pre-scaler value. However, after updating the pre-scale and/or the reload value, it is not necessary to wait until IWDG_STS.CRVU bit or IWDG_STS.PVU bit are reset before continuing code execution (even in case of low-power mode entry, the write operation is taken into account and will complete).

Pre-scale register and reload register controls the time that generates reset, as shown in Table 15-1.

Table 15-1 IWDG counting maximum and minimum reset time

Pre-scale factor	PD[2:0]	Minimum（ms） RL[11:0]=0	Maximum（ms） RL[11:0]=0xFFF
/4	000	0.1	409.6
/8	001	0.2	819.2
/16	010	0.4	1638.4

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/32	011	0.8	3276.8
/64	100	1.6	6553.6
/128	101	3.2	13107.2
/256	11x	6.4	26214.4

15.4.2 IWDG configuration flow

Software flow:

1. Write 0x5555 to IWDG_KEY.KEYV[15:0] bits to enable write access of IWDG_PREDIV and IWDG_RELV registers.
2. Check IWDG_STS.PVU bit or IWDG_STS.CRVU bit, if they are 0, continue next step.
3. Configure IWDG_PREDIV.PD[2:0] bits to select pre-scale value.
4. Configure IWDG_RELV.REL[11:0] bits reload value.
5. Writing 0xAAAA to IWDG_KEY.KEYV[15:0] bits to upload counter with reload value.
6. Enable watchdog by software or hardware writing 0xCCCC to IWDG_KEY.KEYV[15:0] bits.

If user wants change pre-scale and reload value, repeat step 1~5. If not, just feed the dog with step 5.

15.5 IWDG registers

15.5.1 IWDG register overview

Table 15-2 IWDG register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IWDG_KEY	Reserved																KEYV[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	IWDG_PREDIV	Reserved																													PD[2:0]		
	Reset value																														0	0	0
0x08	IWDG_RELV	Reserved																				REL[11:0]											
	Reset value																					1	1	1	1	1	1	1	1	1	1	1	1
0x0C	IWDG_STS	Reserved																														CRVU	PVU
	Reset value																															0	0

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15.5.2 IWDG key register (IWDG_KEY)

Address offset: 0x00

Reset value: 0x00000000

31 … 16
Reserved

15 … 0
KEYV[15:0]
rc_w0

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	KEYV[15:0]	Key value register: only certain value will serve particular function 0xCCCC： Start watch dog counter, does not have any effect if hardware watchdog is enable, (if hardware watchdog is selected, it is not limited by this command word) 0xAAAA: Reload counter with REL value in IWDG_RELV register to prevent reset. 0x5555: Disable write protection of IWDG_PREDIV and IWDG_RELV register

15.5.3 IWDG pre-scaler register (IWDG_PREDIV)

Address offset: 0x04

Reset value: 0x00000000

31 … 16
Reserved

15 … 3	2 … 0
Reserved	PD[2:0]
	rw

Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
2:0	PD[2:0]	Pre-frequency division factor Pre-scaler divider: with write access protection when IWDG_KEY.KEYV[15:0] is not 0x5555. The IWDG_STS.PVU bit must be 0 otherwise PD [2:0] value cannot be changed. Divide number is as follow: 000: divider /4 001: divider /8 010: divider /16 011: divider /32 100: divider /64 101: divider /128 Other : divider /256 *Note: Reading this register will return the pre-divided value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.PVU bit is '0'.*

15.5.4 IWDG reload register (IWDG_RELV)

Address offset: 0x08

Reset value: 0x00000FFF

31–16
Reserved

15–12	11–0
Reserved	REL[11:0]
	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	REL[11:0]	Watchdog counter reload value. With write protection. Defines the reload value of the watchdog counter, which is loaded to the counter every time 0xAAAA is written to IWDG_KEY.KEYV[15:0] bits. The counter then starts to count down from this value. The watchdog timeout period can be calculated from this reloading value and the clock pre-scaler value, refer to Table 15-1。 This register can only be modified when the IWDG_STS.CRVU bit is '0'. *Note: Reading this register will return the reload value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.CRVU bit is '0'.*

15.5.5 IWDG status register (IWDG_STS)

Address offset: 0x0C

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Reset value: 0x00000000

31–16
Reserved

15–2	1	0
Reserved	CRVU	PVU
	r	r

Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	CRVU	Watchdog reload value update Reload Value Update: this bit indicates an update of reload value is ongoing. Set by hardware and clear by hardware. Software can only try to change IWDG_RELV.REL[11:0] value when IWDG_KEY.KEYV[15:0] bits' value is 0x5555 and this bit is 0.
0	PVU	Watchdog pre-scaler value update Pre-scaler Value Update: this bit indicates an update of pre-scaler value is ongoing. Set by hardware and clear by hardware. Software can only try to change IWDG_PREDIV.PD[2:0] value when IWDG_KEY.KEYV[15:0] bits' value is 0x5555 and this bit is 0.

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16 Window watchdog (WWDG)

16.1 Introduction

The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock frequency by 4096, and whether the program operation is abnormal is detected through the configuration of the time window. Therefore, WWDG is suitable for precise timing, and is often used to monitor software failures caused by external disturbances or unforeseen logic conditions that cause an application to deviate from its normal operating sequence. A system reset occurs when the WWDG down counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0.

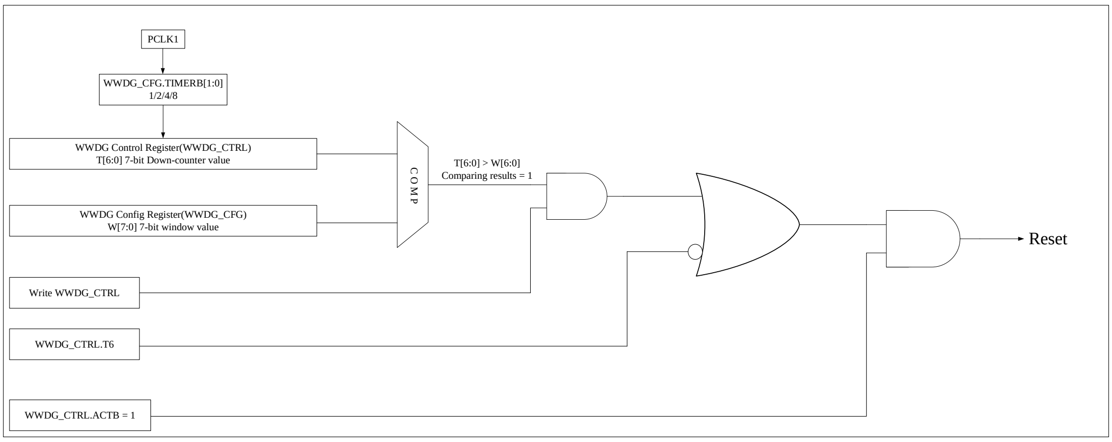
16.2 Main features

- 7-bit independent running down counter programmable
- After WWDG is enabled, a reset occurs under the following conditions
  - The value of the decremented counter is less than 0x40.
  - When the decremented counter value is greater than the value of the window register, it is reloaded.
- Early wake-up interrupt: If the watchdog is started and the interrupt is enabled, wake-up interrupt (WWDG_CFG.EWINT) will be generated when the count value reaches 0x40.

16.3 Function description

If the watchdog is activated (the WWDG_CTRL.ACTB bit), when the 7-bit (WWDG_CTRL.T[6:0]) down-counter reaches 0x3F(WWDG_CTRL.T6 bit is cleared), or the software reloads the counter when the counter value is greater than the value of the window register, a system reset will be generated. In order to avoid system reset, the software must periodically refresh the counter value in the window during normal operation.

Figure 16-1 Watchdog block diagram



Set the WWDG_CTRL.ACTB bit to enable the watchdog, and thereafter, the WWDG will remain on until reset occurs. The 7-bit down-counter runs independently, and the counter keeps counting down whether WWDG is enabled or not. Therefore, before enabling the watchdog, you need to set WWDG_CTRL.T [6] bit to 1, preventing reset right

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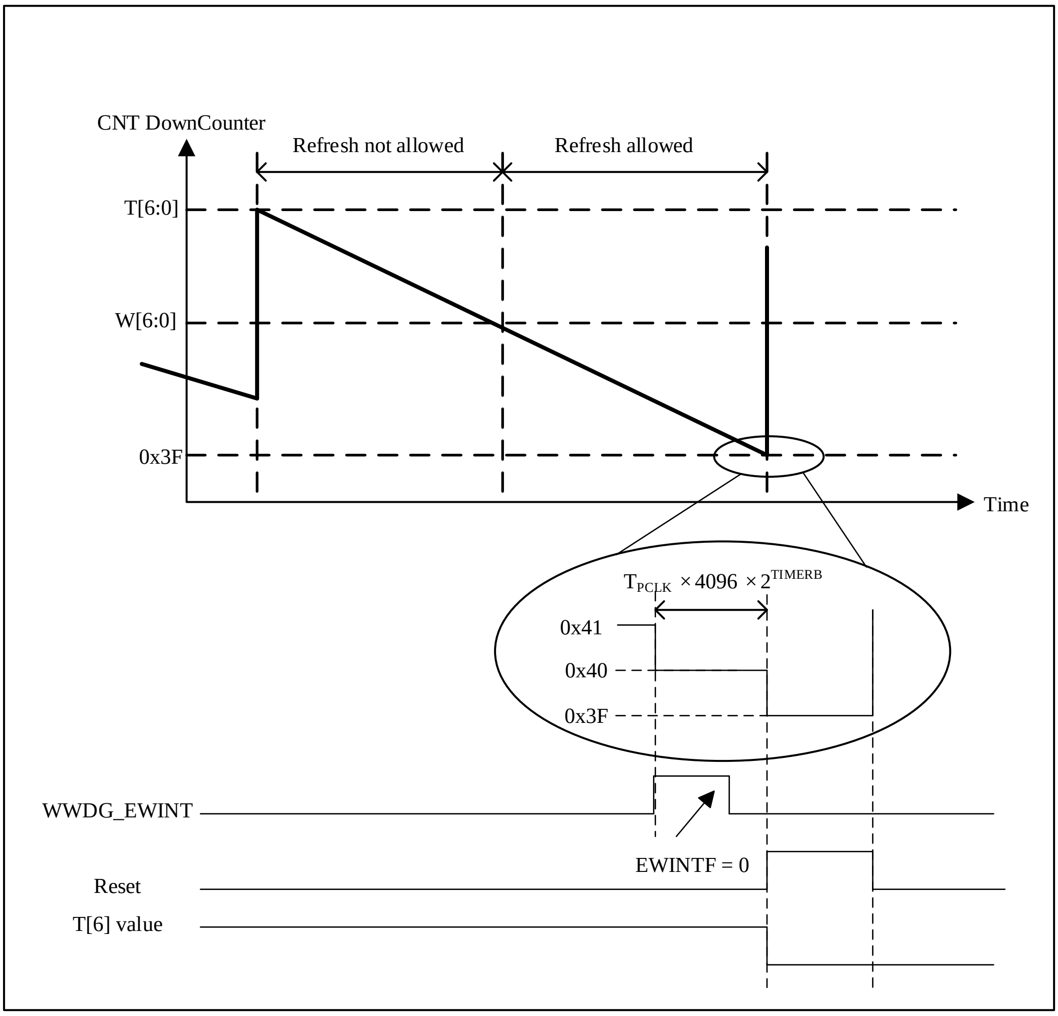
after enable. The pre-scaler value set by the clock APB1 and WWDG_CFG.TIMERB[1:0] bits determine the decrement speed of the counter. WWDG_CFG.W[6:0] bits set the upper limit of the window.

When the down-counter is refreshed before reaching the window register value or after WWDG_CTRL.T6 bit becomes 0, a system reset will be generated. Figure 16-2 describes the working process of the window register.

Set the WWDG_CFG.EWINT bit to enable early wake-up interrupt. When the count-down counter reaches 0x40, an interrupt will be generated. You can analyze the cause of software failure or save important data in the corresponding interrupt service routine (ISR), and reload the counter to prevent WWDG from resetting. Write '0' to the WWDG_STS.EWINTF bit to clear the interrupt.

16.4 Timing for refresh watchdog and interrupt generation

Figure 16-2 Refresh window and interrupt timing of WWDG



Watchdog refreshing window is between WWDG_CFG.W[6:0] value (maximum value 0x7F) and 0x3F, refresh outside this window will generates reset request to MCU. Counter count down from 0x7F to 0x3F using scaled APB1

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clock, the maximum counting time and minimum counting time is shown in Table 16-1 (assuming APB1 clock 27 MHz) with calculate equation:

$$T_{WWDG} = T_{PCLK1} \times 4096 \times 2^{TIMERB} \times (T[6:0] + 1)$$

In which:

T_{WWDG}: WWDG timeout

T_{PCLK1}:APB1 clock interval in ms

Minimum-maximum timeout value at PCLK1 = 27MHz

Table 16-1 Maximum and minimum counting time of WWDG

TIMERB	Minimum counting (ms)	Maximum counting (ms)
0	0.152	9.71
1	0.303	19.42
2	0.607	38.84
3	1.214	77.67

16.5 Debug mode

In debug mode (Cortex-M4 core stops), WWDG counter will either continue to work normally or stops, depending on DBG_CTRL.WWDG_STOP bit in debug module. If this bit is set to ‘1’, the counter stops. The counter works normally when the bit is ‘0’. See the chapter on debugging module for details 29.3.2.

16.6 User interface

16.6.1 WWDG configuration flow

1) Configure RCC_APB1PCLKEN.WWDGEN[11] bit to enable the clock of WWDG module;
2) Software setting WWDG_CFG.TIMERB[8:7] bits to configure pre-scale factor for WWDG.
3) Software configure WWDG_CTRL.T[6:0] bits, setting starting value of counter. Need to set WWDG_CTRL.T[6] bit to 1, preventing reset right after enable.
4) Configure WWDG_CFG.W[6:0] bits to configure upper boundary window value;
5) Setting WWDG_CTRL.ACTB[7] bit to enable WWDG;
6) Software operates WWDG_STS.EWINTF[0] bit to clear wake-up interrupt flag;
7) Configure WWDG_CFG.EWINT[9] bit to enable early wake-up interrupt.

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16.7 WWDG registers

16.7.1 WWDG register overview

Table 16-2 WWDG register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	WWDG_CTRL	Reserved																								ACTB	T[6:0]						
	Reset Value																									0	1	1	1	1	1	1	1
004h	WWDG_CFG	Reserved																						EWINT	TIMERB[1:0]		W[6:0]						
	Reset Value																							0	0	0	1	1	1	1	1	1	1
008h	WWDG_STS	Reserved																															EWINTF
	Reset Value																																0

16.7.2 WWDG control register (WWDG_CTRL)

Address offset : 0x00

Reset value : 0x0000007F

31–16
Reserved

15–8	7	6–0
Reserved	ACTB	T[6:0]
	rs	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	ACTB	Activation bit When ACTB=1, the watchdog can generate a reset. This bit is set by software and only cleared by hardware after a reset. When ACTB = 1, the watchdog can generate a reset. 0: Disable watchdog 1: Enable watchdog
6:0	T[6:0]	These bits contain the value of the watchdog counter. It is decremented every ($4096x2^{TIMERB}$) PCLK1 cycles. A reset is produced when it rolls over from 0x40 to 0x3F (T6 becomes cleared).

16.7.3 WWDG config register (WWDG_CFG)

Address offset: 0x04

Reset value : 0x0000007F

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31–16
Reserved

15–10	9	8–7	6–0
Reserved	EWINT	TIMERB[1:0]	W[6:0]
	rs	rw	rw

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	EWINT	Early wake-up interrupt When set, an interrupt occurs whenever the counter reaches the value 0x40. This interrupt is only cleared by hardware after a reset.
8:7	TIMERB[1:0]	Timer base. The time base of the pre-scaler can be modified as follows: 00: CK Counter Clock (PCLK1 div 4096) div 1 01: CK Counter Clock (PCLK1 div 4096) div 2 10: CK Counter Clock (PCLK1 div 4096) div 4 11: CK Counter Clock (PCLK1 div 4096) div 8
6:0	W[6:0]	7-bit window value These bits contain the window value to be compared to the down counter.

16.7.4 WWDG status register (WWDG_STS)

Address offset: 0x08
Reset value : 0x0000

31–16
Reserved

15–1	0
Reserved	EWINTF
	rc_w0

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EWINTF	Early wake-up interrupt flag This bit is set by hardware when the counter has reached the value 0x40. It must be cleared by software by writing ‘0’. A write of ‘1’ has no effect. This bit is also set if the interrupt is not enabled.

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17 Analog to digital conversion (ADC)

17.1 Introduction

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. It has multiple channels, 19 channels, measuring 16 external and 3 internal signal sources. The A/D conversion of each channel has four execution modes: single, continuous, scan or discontinuous. ADC measurements are stored (left-aligned/ right-aligned) in 16-bit data registers. The application can detect that the input voltage is within user-defined high/low thresholds by analog watchdog and the maximum frequency of the input clock to the ADC is 72MHz.

17.2 Main features

- Supports 1 ADC, supports single-ended and differential inputs, and can measure up to 16 external and 3 internal sources
- Support 12-bit, 10-bit, 8-bit, 6-bit resolution configurable.
  - The maximum sampling rate is 5.14MSPS under 12bit resolution.
  - The maximum sampling rate is 6MSPS under 10bit resolution.
  - The highest sampling rate is 7.2MSPS under 8bit resolution.
  - The highest sampling rate is 9MSPS under 6bit resolution.

  Note: The highest sampling rate is measured under Fast Channel.
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - Only AHB_CLK can be configured as the working clock source.
  - PLL can be configured as a sampling clock source, up to 72MHz, support frequency division 1,2,4,6,8,10,12,16,32,64,128,256
  - The AHB_CLK can be configured as the sampling clock source, up to 72MHz, and supports frequency division 1,2,4,6,8,10,12,16,32
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Support trigger sampling, Including EXTI/TIMER.
- Programmable channel sampling interval
- Support scanning mode
- Support single conversion mode
- Support continuous conversion mode
- Support discontinuous mode
- Support self-calibration
- Support DMA

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- Interrupt generation
  - At the end of conversion
  - At the end of injection conversion
  - Analog watchdog event
- Data alignment with embedded data consistency
- Both regular conversions and injection conversions have external triggering options
- ADC power requirements: 1.8V to 3. 6V
- ADC input voltage range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- Internal channel supports TempSensor, V_{REFINT} (internal 1.2V BG), $V_{REFBUFF}$ (2.048V)
- Supports internal reference voltage (2.048V), please refer to the data sheet for specific parameters

17.3 Function Description

Figure 17-1 is a functional block diagram of an ADC.

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Figure 17-1 Block diagram of a single ADC

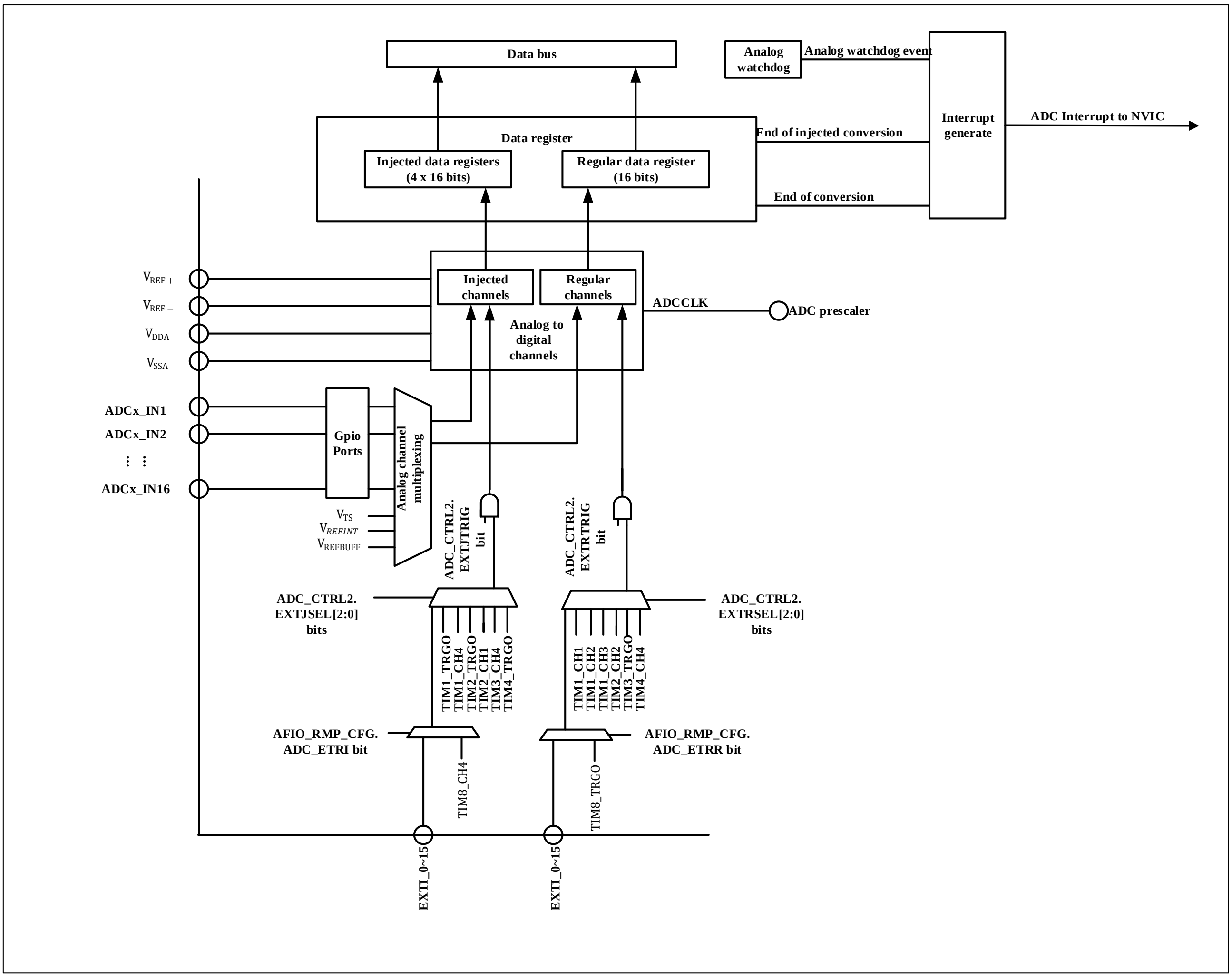

Table 17-1 ADC pins

Name	Types	Description
V_{DDA}	Input, analog power supply	Equivalent to V_{DD} analog power supply and: $1.8V \le V_{DDA} \le V_{DD}(3.6V)$
V_{SSA}	Input, analog power supply ground	Equivalent to V_{SS} Analog power supply ground
V_{REF+}	Input, analog reference positive	Positive reference voltage used by ADC, $1.8V \le V_{REF+} \le V_{DDA}$
V_{REF-}	Input, analog reference negative	Negative reference voltage used by the ADC, $V_{REF-} = V_{SSA}$
ADCx_IN[16:1]	Analog input signal	16 analog external input channels

Note: V_{DDA} and V_{SSA}. They should be separately connected to V_{DD} and V_{SS}.

17.3.1 ADC clock

An ADC requires three clocks, HCLK, ADC_CLK and ADC_1MCLK.

- HCLK is used for the register access.

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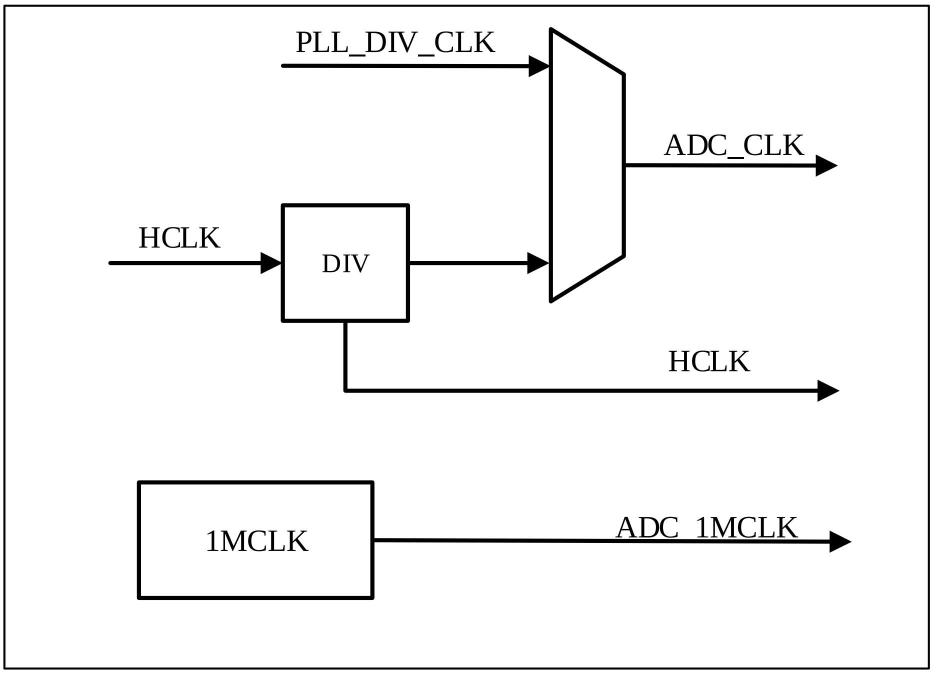
- ADC_CLK is the working clock of ADC. ADC_CLK has two sources (HCLK divider or PLL divider). HCLK divider and system are synchronous clock, while PLL divider and system are asynchronous clock. The advantage of using a synchronous clock is that there is no uncertainty when triggering the ADC to respond to the trigger. The advantage of using PLL's divider clock is that the ADC's working clock can be handled independently without affecting other modules attached to the HCLK
- ADC_1MCLK for internal timing function, configured in RCC, frequency size must be configured to 1MHz

Note:

1. *Configuration PLL as a clock source, up to 72 MHz, support frequency division 1,2,4,6,8,10,12,16,32, 64,128,256*
2. *The AHB_CLK frequency division can be configured as a working clock up to 72MHz. The AHB_CLK frequency division can be 1,2,4,6,8,10,12,16,32*
3. *When switching the ADC_1M clock source, you need to ensure that the HSI clock is turned on*

Figure 17-2 ADC clock



17.3.2 ADC switch control

You can proceed to the next step only after the power-up process is complete. You can check if the power-up is complete by polling the ADC_CTRL3.RDY bit.

You can set the ADC_CTRL2.ON bit to turn on the ADC. When the ADC_CTRL2.ON bit is set for the first time, it wakes up the ADC from the power-off state. After a power-on delay of ADC (t_{STAB}), and the conversion begins when the ADC_CTRL2.ON bit is set again.

The conversion can be stopped by clearing the ADC_CTRL2.ON bit and placing the ADC in power-off mode. In this

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mode, the ADC consumes almost no power (just a few μA). Power-down can be checked by polling the ADC_CTRL3.PDRDY bit.

When the ADC is disabled, the default mode is power-down. In this mode, as long as the power is on, there is no need to re-calibrate, and the calibration value is automatically maintained in the ADC. To further reduce power consumption, the ADC has a deep sleep mode. When ADC Disable will enter deep sleep mode, the calibration value inside the ADC is lost and needs to be recalibrated. Deep sleep saves about 0.2μA of power consumption.

Note: Register ADC_CTRL3.DPWMOD which controls ADC deep sleep mode.

17.3.3 Channel selection

Each channel can be configured as a regular sequence and an injection sequence.

Injection sequence consists of multiple conversions, up to a maximum of 4. The ADC_JSEQ register specifies the injection channel and the conversion order of the injection channel. The ADC_JSEQ.JLEN[1:0] bits specified injection sequence length.

Regular sequence consists of multiple conversions, up to a maximum of 16. The ADC_RSEQx registers specify the regular channels and the conversion order of the regular channels. The ADC_RSEQ1.LEN[3:0] bits specified regular channel sequence length.

Note: During conversion, changes to the ADC_RSEQx or ADC_JSEQ registers are prohibited; the ADC_RSEQx or ADC_JSEQ registers can only be changed when the ADC is idle.

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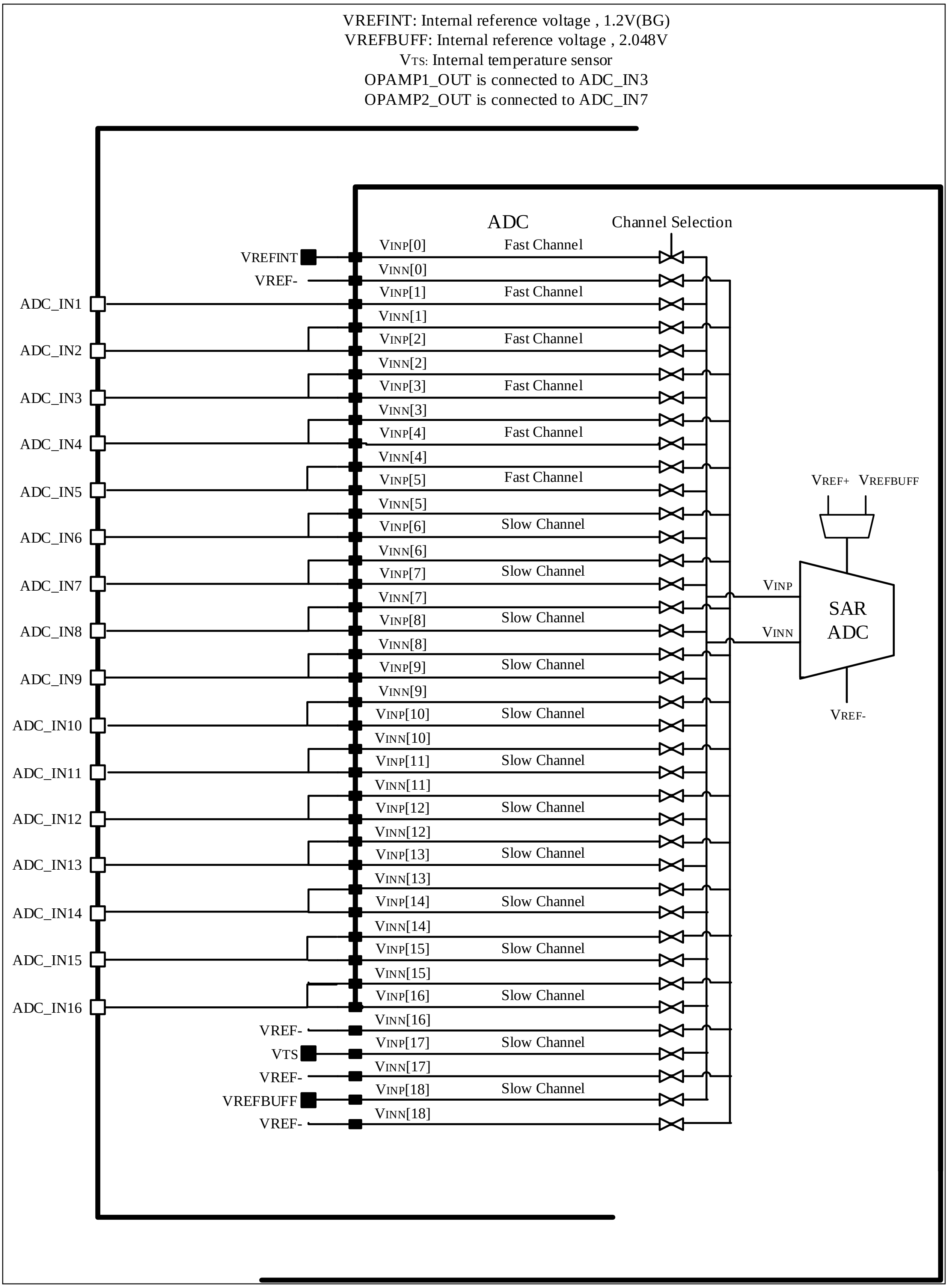
Figure 17-3 ADC channels and Pin connections



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17.3.4 Internal channel

- The temperature sensor is connected to channel ADC_IN17.
- V_{REFINT} is connected to channel ADC_IN0.
- V_{OP1OUT} output is connected to channel ADC_IN3.
- V_{OP2OUT} output is connected to channel ADC_IN7.

Internal channels can be converted by injection or regular channels.

Note: For the use of $V_{REFBUFF}$,please contact Nations to obtain relevant information.

17.3.5 Single conversion mode

The ADC can enter the single conversion mode by configuring ADC_CTRL2.CTU to 0. In this mode, external triggering(for regular channels or injection channels) or setting ADC_CTRL2.ON=1(for regular channels only) can start the ADC to start conversion, and the ADC only performs one conversion.

After the conversion starts, when an injection channel conversion is completed, the injection channel conversion end flag(ADC_STS.JENDC) will be set to 1. If the injection channel conversion end interrupt enable (ADC_CTRL1.JENDCIEN) bit is set to 1, an interrupt will be generated at this time, and the converted data will be stored in the ADC_JDATx register.

After the conversion starts, when a regular channel conversion is completed, the regular channel conversion end flag(ADC_STS.ENDC) will be set to 1. If the regular channel conversion end interrupt enable (ADC_CTRL1.ENDCIEN) bit is set to 1, an interrupt will be generated at this time, and the converted data will be stored in the ADC_DAT register.

After single conversion, the ADC stops.

17.3.6 Continuous conversion mode

The ADC can enter the continuous conversion mode by configuring ADC_CTRL2.CTU to 1. In this mode, external triggering or setting ADC_CTRL2.ON to 1 can start the ADC to start conversion, and the ADC will continuously convert the selected channel. Continuous mode is only valid for regular channels, not for injection channels.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of conversion flag bit (ADC_STS.ENDC) will be set to 1. If the regular channel conversion end interrupt enable bit (ADC_CTRL1.ENDCIEN) is set to 1 at this time, an interrupt will be generated . The converted data will be stored in the ADC_DAT register.

17.3.7 Timing diagram

When ADC_CTRL2.ON is set to 1 for the first time, the ADC is powered on. After the ADC is powered on, the ADC needs a certain time(t_{STAB}) to ensure its stability. After the ADC is stable, write 1 to ADC_CTRL2.ON again, the ADC starts to convert, and the conversion end flag will be set to 1 after the conversion is completed.

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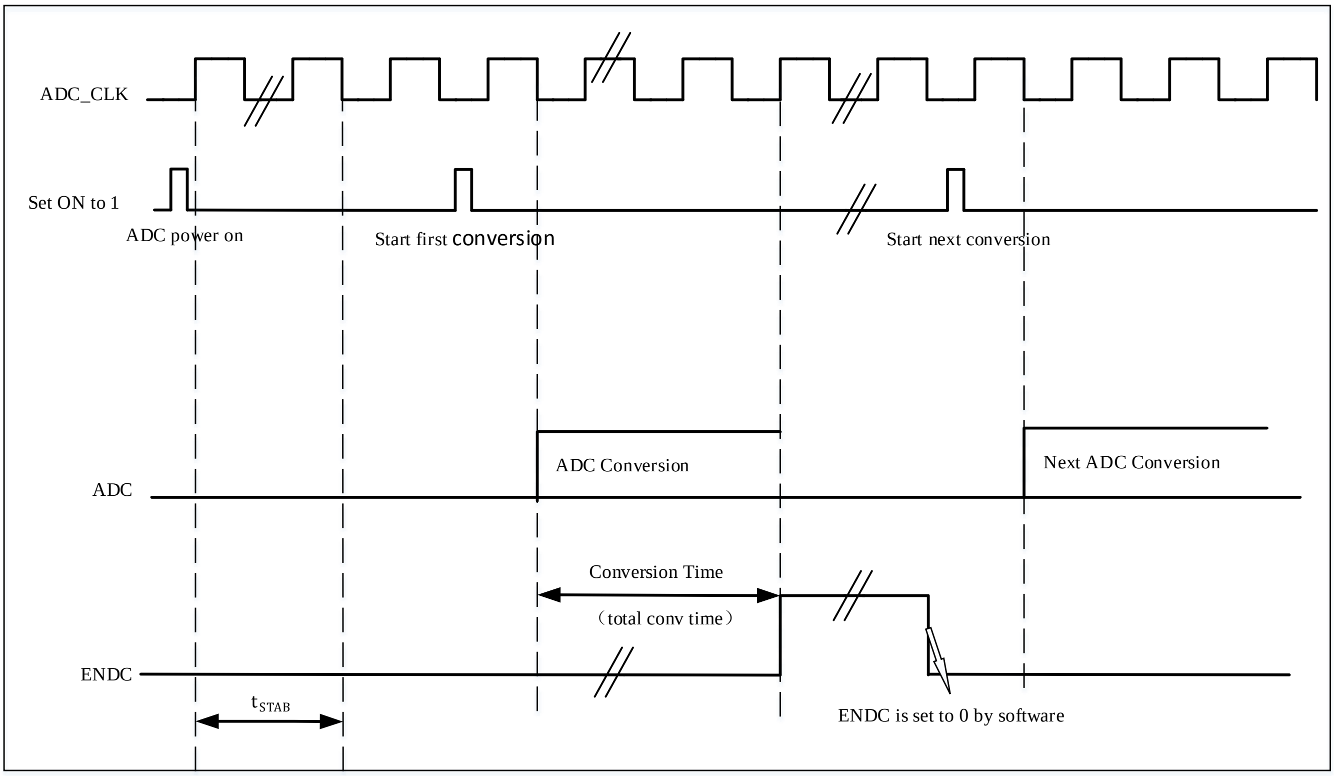
Figure 17-4 Timing diagram



17.3.8 Analog watchdog

The analog watchdog can be enabled on the regular channel by setting ADC_CTRL1.AWDGERCH to 1, or the analog watchdog on the injection channel can be enabled by setting ADC_CTRL1.AWDGEJCH to 1. The high threshold of the analog watchdog can be set by configuring ADC_WDGHIGH.HTH, and the low threshold of the analog watchdog can be set by configuring ADC_WDGLOW.LTH. The threshold of the analog watchdog has nothing to do with the way of data alignment, because the comparison of the ADC's conversion value with the threshold is done before the alignment .When the value of ADC analog conversion is higher than the high threshold of the analog watchdog or lower than the low threshold of the analog watchdog, the analog watchdog flag (ADC_STS.AWDG) will be set to 1, if ADC_CTRL1.AWDGIEN has been configured to 1, an interrupt will be generated at this time. The analog watchdog can be controlled for one or more channels by configuring ADC_CTRL1.AWDGSGLEN and ADC_CTRL1.AWDGCH[4:0].

Table 17-2 Analog watchdog channel selection

Channel	ADC_CTRL1 register control bit		
	AWDGSGLEN	AWDGERCH	AWDGEJCH
There is none	Any value	0	0
All injection channels	0	0	1
All regular channels	0	1	0
All injection and regular channels	0	1	1
A single injection channel	1	0	1

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A single regulars of the channel	1	1	0
A single injection or regular channels	1	1	1

17.3.9 Scanning mode

By configuring ADC_CTRL1.SCAMD to 1, the scan conversion mode can be turned on, and by configuring the four registers ADC_RSEQ1, ADC_RSEQ2, ADC_RSEQ3, ADC_JSEQ, the conversion sequence can be selected, and the ADC will scan and convert all the regular or Injected channels. After the conversion is started, the channels will be converted one by one. If ADC_CTRL2.CTU is 1 at this time, the conversion will be restarted from the first channel of the conversion sequence after the conversion of all regular channels is completed. Injected channel does not support continuous mode. The DMA function can be turned on by setting ADC_CTRL2.ENDMA to 1, and the DMA will transfer the data to the SRAM after the regular channel conversion is completed.

17.3.10 Injection channel management

17.3.10.1 Automatic injection

If ADC_CTRL1.AUTOJC bit is set, then the Injected channels are automatically converted following the regular channels mentioned by ADC_RSEQx and ADC_JSEQx. A single trigger can conver up to 16+ 4 channels. Setting ADC_CTRL2.CTU the conversion sequence will be converted continuously.

When this function is turned on, the external trigger of the injection channel needs to be turned off.

This function cannot be used with the discontinuous mode at the same time.

When the ADC clock prescale factor is 2, there is a delay of two ADC clock intervals when the conversion sequence changes from regular to injection or injection to regular. When the ADC clock prescale factor is 4 to 8, there is a delay of one ADC clock intervals when the conversion sequence changes from regular to injection or injection to regular.

17.3.10.2 Trigger injection

Set ADC_CTRL1.AUTOJC to 0 and ADC_CTRL1.SCAMD to 1 to enable the trigger injection function. In this function, the regular channel of continuous conversion is triggered by setting ADC_CTRL2.ON or by external trigger. When the regular channel is converted, if an external injection trigger is generated, the current conversion will be suspended, and the injection sequence channel will start conversion. When the injection sequence channel conversion is completed, the interrupted conversion of regular sequence channel will be resumed. If a regular event is generated during the injection conversion, the regular sequence channel will start conversion after the injection sequence channel conversion is completed.

When using this function, the time interval between the injection channel triggers needs to be greater than the time required for the injection sequence to complete the conversion.

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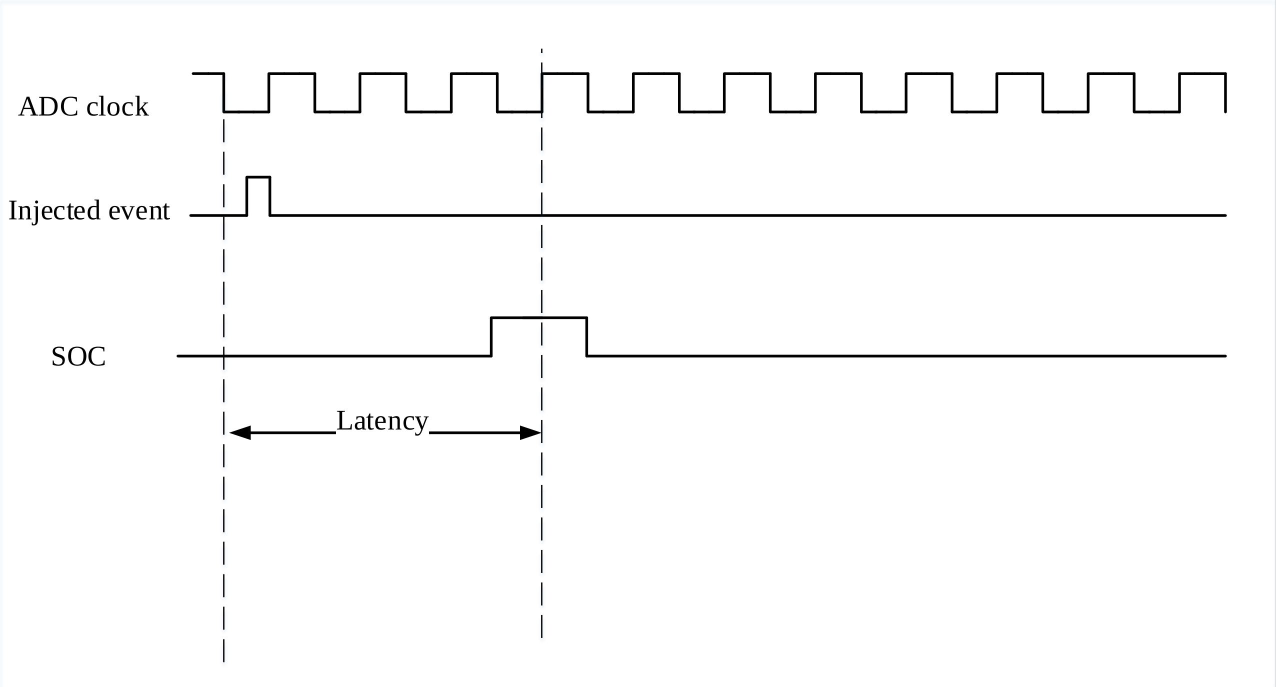
Figure 17-5 Injection conversion delay



Note:For the maximum delay value, please refer to the electrical characteristics section in the data manual.

17.3.11 Discontinuous mode

17.3.11.1 Regular channels

Configure ADC_CTRL1.DREGCH to 1 to enable the discontinuous mode on the regular channel, obtain the regular sequence by configuring ADC_RSEQ1, ADC_RSEQ2, ADC_RSEQ3, and configure ADC_CTRL1.DCTU[2:0] to control the conversion of n channels each time a trigger signal is generated.

When the trigger signal is generated, it will convert n channels of the regular sequence and then stop, until the next trigger signal is generated. Next trigger will continue to convert n channels from the point where the previous conversion stopped, until all channels of the regular sequence are converted (If the last trigger occurs and the remaining channels in the conversion sequence are less than n, only the remaining channels will be converted and the conversion will be stopped), and the end of conversion flag bit will also be set to 1. When the conversion of all channels in the conversion sequence is completed, when the next trigger signal occurs ,the conversion starts from the first channel of the regular sequence again.

17.3.11.2 Injection channels

Configure ADC_CTRL1.DJCH to 1 to enable the discontinuous mode on the injection channel, obtain the injection sequence by configuring ADC_JSEQ.

When the trigger signal is generated, it will convert 1 channel of the injection sequence and then stop. Until the next trigger signal is generated. Next trigger will continue to convert 1 channel from the point where the previous conversion stopped until all channels of the injection sequence are converted, and the end of conversion flag bit will also be set to 1. When the conversion of all channels in the conversion sequence is completed, when the next trigger

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signal occurs ,the conversion starts from the first channel of the injection sequence again.

Only one of injection conversion and regular conversion can be set to discontinuous mode at the same time, and the automatic injection function and discontinuous mode cannot be set at the same time.

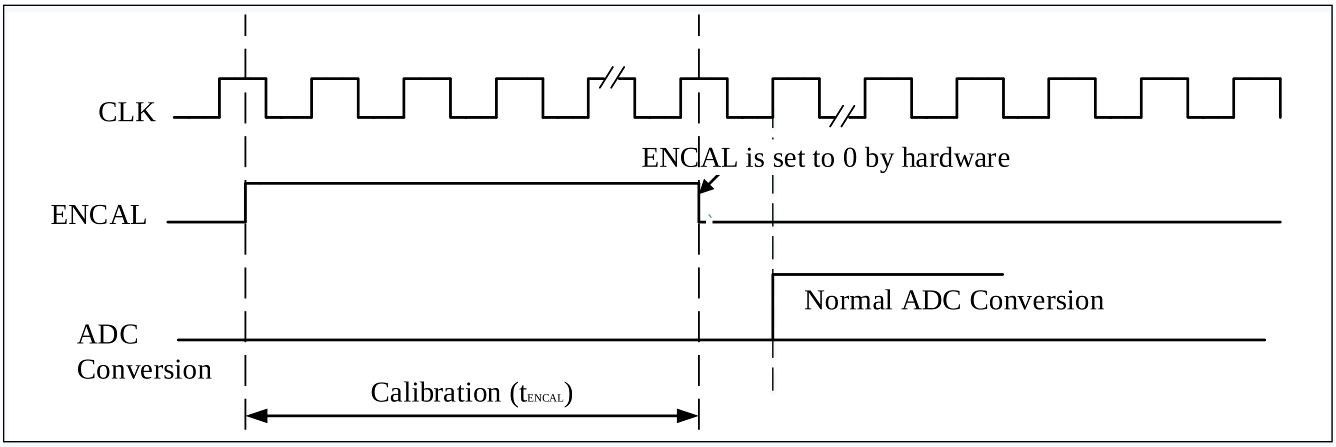
17.4 Calibration

In order to reduce the error, the ADC will have a built-in self-calibration mechanism. Before the A/D conversion, this self-calibration mechanism is used to calculate a calibration factor on each capacitor. Errors due to changes in the internal capacitor bank during conversion are eliminated by this calibration factor. The application program sets the ADC_CTRL2.ENCAL bit to 1 to start self-calibration. During the calibration, the ADC_CTRL2.ENCAL bit remains 1. After the calibration, the ADC_CTRL2.ENCAL bit is cleared by hardware, and then the A/D conversion starts. After the calibration phase, the calibration code is stored in ADC_DAT.

Note:

1. *It is recommended to perform a calibration after each power-on. If the ADC has been converted and is in continuous conversion mode, the calibration operation cannot be completed..*
2. *The default is single-end calibration, and for differential automatic calibration, you must set ADC_CTRL3.CALDIF to 1. Then write 1 to ADC_CTRL2.ENCAL bit and wait for calibrationto complete (ADC_CTRL2.ENCAL bit will clear 0 automatically after calibration).*
3. *After waking up from low power mode, the ADC module needs to be reset to reconfigure the calibration function.*

Figure 17-6 Calibration sequence diagram



17.5 Data aligned

There are two alignment methods for data storage after conversion: left-aligned and right-aligned. The alignment can be set by the ADC_CTRL2.ALIG bit. ADC_CTRL2.ALIG = 0 is right-aligned, as shown in Table 17-3, ADC_CTRL2.ALIG = 1 is left-aligned, as shown inTable 17-4.

For injection sequence , the SYM bit is the extended sign value, and the data stored in the register is the conversion result minus the user-defined offset in the ADC_JOFFSETx register, so the result can be a negative value; for regular sequence , there is no need to subtract offset value.

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Table 17-3 Right-align data

The Injection sequence

(12bit resolution)

SYM	SYM	SYM	SYM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The regular sequence

(12bit resolution)

0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 17-4 Left-aligne data

Injection sequence

(12bit resolution)

SYM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0

The regular sequence

(12bit resolution)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

Note: When the conversion digits are 10, 8, and 6, refer to the alignment with 12 conversion digits

17.6 Programmable channel sampling time

Specify the number of sampling cycles of ADC in ADC_SAMPTx.SAMPx[2:0], and then the ADC samples the input voltage in the specified sampling cycle. For different channels, you can select different sampling time. The total conversion time is calculated as follows:

$$T_{CONV} = \text{Sampling time} + 12.5 \text{ cycles}$$

Example:

ADCCLK=72MHz, the sampling time is 1. 5 cycles.

$$T_{CONV} = 1.5 + 12.5 = 14 \text{ cycle} = 0.1944\mu s$$

17.7 Externally triggered conversion

For the regular sequence , software sets the ADC_CTRL2.EXTRTRIG bit to 1, then the regular channel can use the rising edge of the external event to trigger the start conversion, and then the software sets the ADC_CTRL2.EXTRSEL[2:0] bits to select the external trigger source of the regular sequence. The external trigger source selection is shown in the table below. If you select EXTI line 0~15 or TIM8_TRGO as the external trigger source, you can set the AFIO_RMP_CFG.ADC_ETRR and AFIO_RMP_CFG.EXTI_ETRR[3:0] bits to implement;

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if you select SWSTRRCH as the external trigger source, you can start the regular channel conversion by setting ADC_CTRL2.SWSTRRCH to 1.

Table 17-5 ADC is used for external triggering of regular channels

EXTRSEL[2:0]	Trigger source	Type
000	TIM1_CC1 event	Internal signal from the on-chip timer
001	TIM1_CC2 event	
010	TIM1_CC3 event	
011	TIM2_CC2 event	
100	TIM3_TRGO event	
101	TIM4_CC4 event	
110	EXTI line 0~15/TIM8_TRGO event	External pin/internal signal from on-chip timer
111	SWSTRRCH	Software control bit

For the injection sequence , the software sets the ADC_CTRL2.EXTJTRIG bit to 1, then the injection channel can use the rising edge of the external event to trigger the start conversion, and the software sets the ADC_CTRL2.EXTJSEL[2:0] bits to select the external trigger source of the injection sequence. The external trigger source selection is shown in the table below. If you select EXTI line 0~15 or TIM8_CC4 as the external trigger source, you can set the AFIO_RMP_CFG.ADC_ETRI and AFIO_RMP_CFG.EXTI_ETRI[3:0] bits to implement; if you select SWSTRJCH as the external trigger source, you can start the injection channel conversion by setting ADC_CTRL2.SWSTRJCH to 1.

Table 17-6 ADC is used for external triggering of injection channels

EXTJSEL[2:0]	Trigger source	Type
000	TIM1_TRGO event	Internal signal from the on-chip timer
001	TIM1_CC4 event	
010	TIM2_TRGO event	
011	TIM2_CC1 event	
100	TIM3_CC4 event	
101	TIM4_TRGO event	
110	EXTI line 0~15/TIM8_CC4 event	External pin/internal signal from on-chip timer
111	SWSTRJCH	Software control bit

Note: Injection triggers can interrupt conversion of the regular sequence.

17.8 DMA requests

In order to avoid the loss of the regular channel conversion result saved in the ADC_DAT register due to excessive data when multiple regular channels are converted, the ADC_CTRL2.ENDMA bit can be set to 1 to use DMA. When the ADC regular channel conversion ends, a DMA request is generated. After the DMA receives the request, it will transfer the converted data from the ADC_DAT register to the destination address specified by the user.

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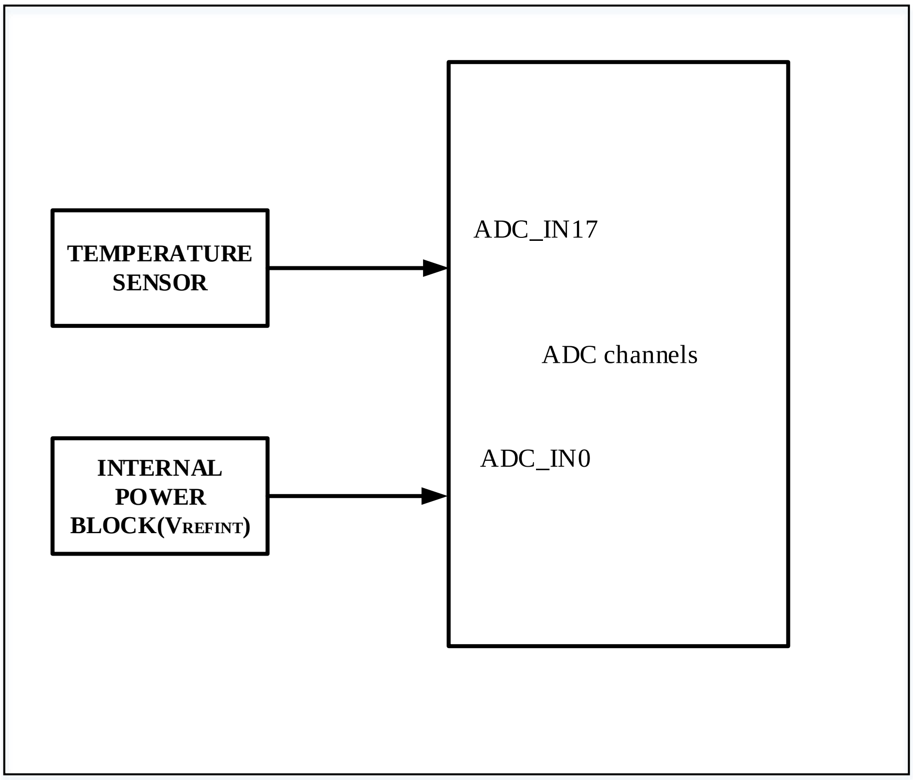
17.9 Temperature sensor

Set the ADC_CTRL2.TEMPEN bit to 1, enable the temperature sensor and VREFINT, and use the temperature sensor to detect the ambient temperature when the device is working. The output voltage sampled by the temperature sensor is converted into a digital value by the ADC_IN17 channel. When the temperature sensor is working, the ideal sampling time is 17.1us; when the temperature sensor is not working, the ADC_CTR2.TEMPEN bit can be cleared by software to reduce power consumption. Figure 17-7 is a block diagram of a temperature sensor.

The output voltage of the temperature sensor changes linearly with temperature. Different chips will have different offsets in the temperature curve due to different production processes. Through testing, it is found that the maximum offset is 3℃. This characteristic makes the internal temperature sensor more suitable for detecting temperature changes. Not suitable for measuring absolute temperature. When accurate temperature measurement is required, an external temperature sensor should be used.

Figure 17-7 Temperature sensor and VREFINT Diagram of the channel



17.9.1 Temperature sensor using flow

1) Configure the channel (ADC_IN17) and sampling time of the channel to be 17.1 us
2) Set ADC_CTRL2.TEMPEN bit to 1 to enable temperature sensor and V_{REFINT}
3) Set ADC_CTRL2.ON bit to 1 to start ADC conversion (or through external trigger)
4) Read the temperature data in the ADC data register, and calculate the temperature value by the following formula:

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Temperature (℃) = {(V_{30} - V_{SENSE}) / Avg_Slope} + 30- T_{offset}

In which:

V_{30} = V_{SENSE} at 30 degrees celsius

Avg_Slope = temperature and Average slope of a V_{SENSE} curve (mV/°C or µV/°C)

T_{offset} = empirical value for temperature error compensation (℃)

Refer to the values of V_{30} and Avg_Slope in the electrical characteristics chapter of the datasheet.

Note: There is a settling time before the sensor wakes up from the power-off mode to the correct output of VSENSE; there is also a settling time after the ADC is powered on, so in order to shorten the delay, the ADC_CTRL2.TEMPEN and ADC_CTRL2.ON bits should be set at the same time.

17.10 ADC interrupt

ADC interrupts can be from an end of regular or injection sequence conversion, an analog watchdog event when input voltage exceeds the threshold, any end of regular or injection channel conversion. These interrupts have independent interrupt enable bits.

There are 2 status flags in the ADC_STS register: injection sequence channel conversion started (JSTR) and regular sequence channel conversion started (STR). But there are no interrupts associated with these two flags in the ADC.

Table 17-7 ADC interrupt

Interrupt event	Event flags	Enable control bit
Regular or injection sequence conversion is complete	ENDC	ENDCIEN
Injection sequence conversion is complete	JENDC	JENDCIEN
Analog watchdog status bit is set	AWDG	AWDGIEN
Any regular channel interruption is enabled	ENDCA	ENDCAIEN
Any injection channel interruption is enabled	JENDCA	JENDCAIEN

17.11 ADC registers

17.11.1 ADC register overview

Table 17-8 ADC register overview

<table>
<tr><td>Offset</td><td>Register</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td rowspan="2">000h</td><td>ADC_STS</td><td colspan="25" rowspan="2">Reserved</td><td>JENDCA</td><td>ENDCA</td><td>STR</td><td>JSTR</td><td>JENDC</td><td>ENDC</td><td>AWDG</td></tr>
<tr><td>Reset Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">004h</td><td>ADC_CTRL1</td><td colspan="8" rowspan="2">Reserved</td><td>AWDGERCH</td><td>AWDGEJCH</td><td colspan="6" rowspan="2">Reserved</td><td colspan="3">DCTU[2:0]</td><td>DJCH</td><td>DREGCH</td><td>AUTOJC</td><td>AWDGSGLEN</td><td>SCANMD</td><td>JENDCIEN</td><td>AWDGIEN</td><td>ENDIEN</td><td colspan="5">AWDGCH[4:0]</td></tr>
<tr><td>Reset Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>008h</td><td>ADC_CTRL2</td><td colspan="8">Reserved</td><td>TEMPEN</td><td>SWSTRRCH</td><td>SWSTRJCH</td><td>EXTRTRIG</td><td colspan="3">EXTRSEL[2:0]</td><td>Reserved</td><td>EXTJTRIG</td><td colspan="3">EXTJSEL[2:0]</td><td>ALIG</td><td colspan="2">Reserved</td><td>ENDMA</td><td colspan="5">Reserved</td><td>ENCAL</td><td>CTU</td><td>ON</td></tr>
</table>

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value									0	0	0	0	0	0	0		0	0	0	0	0			0						0	0	0
00Ch	ADC_SAMPT1	Reserved								SAMP17[2:0]			SAMP16[2:0]			SAMP15[2:0]			SAMP14[2:0]			SAMP13[2:0]			SAMP12[2:0]			SAMP11[2:0]			SAMP10[2:0]		
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	ADC_SAMPT2	Reserved		SAMP9[2:0]			SAMP8[2:0]			SAMP7[2:0]			SAMP6[2:0]			SAMP5[2:0]			SAMP4[2:0]			SAMP3[2:0]			SAMP2[2:0]			SAMP1[2:0]			SAMP0[2:0]		
	Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	ADC_JOFFSET1	Reserved																				OFFSETJCH1[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
018h	ADC_JOFFSET2	Reserved																				OFFSETJCH2[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
01Ch	ADC_JOFFSET3	Reserved																				OFFSETJCH3[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
020h	ADC_JOFFSET4	Reserved																				OFFSETJCH4[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
024h	ADC_WDGHIGH	Reserved																				HTH[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
028h	ADC_WDGLOW	Reserved																				LTH[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
02Ch	ADC_RSEQ1	Reserved								LEN[3:0]				SEQ16[4:0]					SEQ15[4:0]					SEQ14[4:0]					SEQ13[4:0]				
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	ADC_RSEQ2	Reserved		SEQ12[4:0]					SEQ11[4:0]					SEQ10[4:0]					SEQ9[4:0]					SEQ8[4:0]					SEQ7[4:0]				
	Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	ADC_RSEQ3	Reserved		SEQ6[4:0]					SEQ5[4:0]					SEQ4[4:0]					SEQ3[4:0]					SEQ2[4:0]					SEQ1[4:0]				
	Reset Value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	ADC_JSEQ	Reserved										JLEN[1:0]		JSEQ4[4:0]					JSEQ3[4:0]					JSEQ2[4:0]					JSEQ1[4:0]				
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	ADC_JDAT1	Reserved																JDAT1[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	ADC_JDAT2	Reserved																JDAT2[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	ADC_JDAT3	Reserved																JDAT3[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	ADC_JDAT4	Reserved																JDAT4[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	ADC_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	ADC_DIFSEL	Reserved													DIFSEL[17:0]																		Reserved
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
054h	ADC_CALFACT	Reserved									CALFACTD[6:0]							Reserved									CALFACTS[6:0]						
	Reset Value										0	0	0	0	0	0	0										0	0	0	0	0	0	0
058h	ADC_CTRL3	Reserved																				VABTMEN	DPWMOD	JENDCAIEN	ENDCAIEN	BPCAL	PDRDY	RDY	CKMOD	CALALD	CALDIF	RES[1:0]	
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
05Ch	ADC_SAMPT3	Reserved																												SAMPSEL	SAMP[2:0]		
	Reset Value																													0	0	0	0

17.11.2 ADC status register (ADC_STS)

Address offset: 0x00

Reset value: 0x0000 0000

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31															16
Reserved															

15								7	6	5	4	3	2	1	0
Reserved									JENDCA	ENDCA	STR	JSTR	JENDC	ENDC	AWDG
									rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
6	JENDCA	Any injected channel end of conversion flag This bit is set by hardware at the end of any injection channel conversion and cleared by software. 0: Conversion is not complete; 1: Conversion is complete.
5	ENDCA	Any channel end of conversion flag This bit is set by hardware at the end of any channel (regular or injection) conversion and cleared by software. 0: Conversion is not complete; 1: Conversion is complete.
4	STR	Regular channel start flag This bit is set by hardware at the start of regular channel conversion and cleared by software. 0: Regular channel conversion has not started. 1: Regular channel conversion has started.
3	JSTR	Injected channel start flag This bit is set by hardware at the start of the injection channel conversion and cleared by software. 0: Injection sequence channel conversion has not started. 1: Injection sequence channel conversion has started.
2	JENDC	Injected channel end of conversion This bit is set by hardware at the end of all injection sequence channel conversions and cleared by software 0: Conversion is not complete. 1: Conversion is complete.
1	ENDC	Conversion sequence channel end of conversion This bit is set by hardware at the end of all regular(or injection) sequence channel conversion and cleared by software 0: Conversion is not complete. 1: Conversion is complete.
0	AWDG	Analog watchdog flag This bit is set by hardware and cleared by software when converted voltage values are outside the range defined by the ADC_LTR and ADC_HTR registers 0: Analog watchdog event not occurs; 1: Analog watchdog event occurs.

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17.11.3 ADC control register 1 (ADC_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000

31:24	23	22	21:16
Reserved	AWDGERCH	AWDGEJCH	Reserved
	rw	rw	

15:13	12	11	10	9	8	7	6	5	4:0
DCTU[2:0]	DJCH	DREGCH	AUTOJC	AWDGSGLEN	SCANMD	JENDCIEN	AWDGIEN	ENDCIEN	AWDGCH[4:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	AWDGERCH	Analog watchdog enable on regular channels This bit is set and cleared by the software. 0: Disables analog watchdog on regular channel. 1: Use analog watchdog on regular channels.
22	AWDGEJCH	Analog watchdog enable on injected channels This bit is set and cleared by the software. 0: Disables analog watchdog on injection channel. 1: Use analog watchdog on the injection channel.
21:16	Reserved	Reserved, the reset value must be maintained
15:13	DCTU[2:0]	Discontinuous mode channel count The software uses these bits to define the number of channels for converting regulars after receiving an external trigger in discontinuous mode 000: 1 channel 001: 2 channels ... 111: 8 channels
12	DJCH	Discontinuous mode on injected channels This bit is set and cleared by the software. It is used to turn on or off discontinuous mode on injected channels. 0: Disable discontinuous mode on injection sequence channel 1: Enable discontinuous mode on injection sequence channel
11	DREGCH	Discontinuous mode is on regular channels. This bit is set and cleared by the software. It is used to turn on or off discontinuous mode on regular channels. 0: Disable discontinuous mode on regular sequence channel 1: Enable discontinuous mode on regular sequence channel
10	AUTOJC	Automatic injected sequence conversion This bit is set and cleared by the software to enable or disable automatic injection sequence channel conversion after regular sequence channel conversion is complete

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Bit field	Name	Description
		0: Disable automatic injection channel conversion. 1: Enable automatic injection channel conversion.
9	AWDGSGLEN	Enable the watchdog on a single channel in scan mode This bit is set and cleared by software to enable or disable analog watchdog functions on channels specified by ADC_CTRL1.AWDGCH[4:0] 0: Use watchdog on all channels. 1: Use watchdog on single channel.
8	SCANMD	Scan mode This bit is set and cleared by the software to enable or disable scan mode. In scan mode, the conversion is made by ADC_RSEQx or the selected channel of the ADC_JSEQ register. 0: Disable scan mode. 1: Enable scan mode. *Note: If the ADC_CTRL1.ENDCIEN or ADC_CTRL1.JENDCIEN bits are set separately, ADC_STS.ENDC or ADC_STS.JENDC interrupts occur only after the last channel has been converted.*
7	JENDCIEN	Interrupt enable for injected channels This bit is set and cleared by the software to disallow or allow interrupts after all injection channel conversions have finished. 0: Disable JENDC interruption. 1: Enable JENDC interruption.
6	AWDGIEN	Analog watchdog interrupt enable This bit is set and cleared by software to disallow or allow interrupt generated by analog watchdog. In scan mode, if the watchdog detects an out-of-range value, the scan is aborted only when that bit is set. 0: Disable analog watchdog interruption. 1: Enable analog watchdog interruption.
5	ENDCIEN	Interrupt enable for any channel This bit is set and cleared by the software to disallow or allow interrupts to occur after the regular or injected channel conversion ends. 0: Disable ENDC interruption. 1: Enable ENDC interruption.
4:0	AWDGCH[4:0]	Analog watchdog channel select bits These bits are set and cleared by software to select input channels that analog watchdog protection. 00000: ADC analog input channel 0 00001: ADC analog input channel 1 ... 01111: ADC analog input channel 15 10000: ADC analog input channel 16 10001: ADC analog input channel 17 10010: ADC analog input channel 18

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Bit field	Name	Description
		Reserved all other values.

17.11.4 ADC control register 2 (ADC_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000

31:24	23	22	21	20	19:17	16
Reserved	TEMPEN	SWSTRRCH	SWSTRJCH	EXTRTRIG	EXTRSEL[2:0]	Reserved
	rw	rw	rw	rw	rw	

15	14:12	11	10:9	8	7:3	2	1	0
EXTJTRIG	EXTJSEL[2:0]	ALIG	Reserved	ENDMA	Reserved	ENCAL	CTU	ON
rw	rw	rw		rw		rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	TEMPEN	Temperature sensor and V_{REFINT} Enable This bit is set and cleared by the software to enable or disable the temperature sensor and V_{REFINT} Channel. 0: Disables the temperature sensor and V_{REFINT}. 1: Enable the temperature sensor and V_{REFINT}.
22	SWSTRRCH	Start conversion of regular channels This bit is set by the software to start the conversion and cleared by the hardware as soon as the conversion begins. If SWSTRRCH is selected as the trigger event in the ADC_CTRL2.EXTRSEL[2:0] bit, which is used to initiate the conversion of a set of regular channels 0: Reset state. 1: Starts converting the regular channel.
21	SWSTRJCH	Start conversion of injected channels This bit is set by the software to initiate the conversion and can be cleared by the software or by the hardware as soon as the conversion begins. If SWSTRJCH is selected as the trigger event in the ADC_CTRL2.EXTJSEL[2:0] bit, which is used to initiate a conversion of a set of injected channels 0: Reset state. 1: Starts converting the injection channel.
20	EXTRTRIG	External trigger conversion mode for regular channels This bit is set and cleared by software to enable or disable external triggering events that can start regular sequence conversion. 0: Start conversion without external events. 1: Use an external event to start the conversion.
19:17	EXTRSEL[2:0]	External event select for regular sequence These bits select external events to start the regular sequence conversion The triggering configuration of ADC is as follows

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Bit field	Name	Description
		000: indicates the CC1 event of timer 1 100: indicates the TRGO event of timer 3 001: indicates the CC2 event of timer 1 101: indicates the CC4 event of timer 4 010: indicates the CC3 event of timer 1 110: EXTI line 0~15/TIM8_TRGO event 011: indicates the CC2 event of timer 2 111: SWSTRRCH
16	Reserved	Reserved, the reset value must be maintained
15	EXTJTRIG	External trigger conversion mode for injected channels This bit is set and cleared by software to enable or disable external triggering events that can start injection sequence conversion. 0: Start conversion without external events. 1: Use an external event to start the conversion.
14:12	EXTJSEL[2:0]	External event select for injected sequence These bits select the External event used to trigger the injected sequence conversion. The triggering configuration of ADC is as follows 000: indicates the TRGO event of timer 1 100: indicates the CC4 event of timer 3 001: indicates the CC4 event of timer 1 101: indicates the TRGO event of timer 4 010: indicates the TRGO event of timer 2 110: EXTI line 0~15/TIM8_CC4 event 011: indicates the CC1 event of timer 2 111: SWSTRJCH
11	ALIG	Data alignment This bit is set and cleared by the software. Refer to Table 17-3 and Table 17-4. 0: Right-aligned. 1: Left-aligned.
10:9	Reserved	Reserved, the reset value must be maintained
8	ENDMA	Direct memory access mode This bit is set and cleared by the software. See the DMA Controller chapter for details. 0: Do not use DMA mode. 1: Use DMA mode.
7:3	Reserved	Reserved, the reset value must be maintained
2	ENCAL	A/D calibration This bit is set by software to start calibration and cleared by hardware at the end of calibration. 0: Calibration completed; 1: Starts calibration.
1	CTU	Continuous conversion This bit is set and cleared by the software. If this bit is set, the conversion continues until the bit is cleared. 0: Single conversion mode. 1: Continuous conversion mode.
0	ON	A/D converter ON/OFF This bit is set and cleared by the software. When the bit is' 0 ', writing '1' will wake the ADC from power-off mode. When the bit is' 1 ', writing '1' starts the conversion. The application should note that there is a delay t_{STAB} between the time the converter is powered on and the time the conversion begins, see

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Bit field	Name	Description
		Figure 17-4. 0: Close ADC conversion/calibration and enter power-down mode. 1: Start ADC and start conversion. Note: If there are other bits changed in this register along with ON, the conversion will not be triggered. This is to prevent the wrong conversion from being triggered.

17.11.5 ADC sampling time register 1 (ADC_SAMPT1)

Address offset: 0x0C

Reset value: 0x0000 0000

31-24	23-21	20-18	17-16
Reserved	SAMP17[2:0]	SAMP16[2:0]	SAMP15[2:1]
	rw	rw	rw

15	14-12	11-9	8-6	5-3	2-0
SAMP 15_0	SAMP14[2:0]	SAMP13[2:0]	SAMP12[2:0]	SAMP11[2:0]	SAMP10[2:0]
rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:0	SAMPx[2:0]	Channel x sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bit must remain constant during the sampling period. ADC_SAMPT3.SAMPSEL = 0, the sampling time is set as follows: 000: 1.5 cycles 100: 41.5 cycles 001: 7.5 cycles 101: 55.5 cycles 010: 13.5 cycles 110: 71.5 cycles 011: 28.5 cycles 111: 239.5 cycles ADC_SAMPT3.SAMPSEL = 1, the sampling time is set as follows: 000: 1.5 cycles 100: 19.5 cycles 001: 2.5 cycles 101: 61.5 cycles 010: 4.5 cycles 110: 181.5 cycles 011: 7.5 cycles 111: 601.5 cycles

17.11.6 ADC sampling time register 2 (ADC_SAMPT2)

Address offset: 0x10

Reset value: 0x0000 0000

31-30	29-27	26-24	23-21	20-18	17-16
Reserved	SAMP9[2:0]	SAMP8[2:0]	SAMP7[2:0]	SAMP6[2:0]	SAMP5[2:1]
	rw	rw	rw	rw	rw

15	14-12	11-9	8-6	5-3	2-0
SAMP5_0	SAMP4[2:0]	SAMP3[2:0]	SAMP2[2:0]	SAMP1[2:0]	SAMP0[2:0]
rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:0	SAMPx[2:0]	Channel x sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bit must remain constant during the sampling period. ADC_SAMPT3.SAMPSEL = 0, the sampling time is set as follows: 000: 1.5 cycles 100: 41.5 cycles 001: 7.5 cycles 101: 55.5 cycles 010: 13.5 cycles 110: 71.5 cycles 011: 28.5 cycles 111: 239.5 cycles ADC_SAMPT3.SAMPSEL = 1, the sampling time is set as follows: 000: 1.5 cycles 100: 19.5 cycles 001: 2.5 cycles 101: 61.5 cycles 010: 4.5 cycles 110: 181.5 cycles 011: 7.5 cycles 111: 601.5 cycles

17.11.7 ADC injected channel data offset register x (ADC_JOFFSETx) (x=1…4)

Address offset: 0x14-0x20

Reset value: 0x0000 0000

31–16
Reserved

15–12	11–0
Reserved	OFFSETJCHx
	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	OFFSETJCHx[11:0]	Data offset for injected channel x These bits define the values used to subtract from the original conversion data when the conversion is injected into the channel. The result of the conversion can be read in the ADC_JDATx register.

17.11.8 ADC watchdog high threshold register (ADC_WDGHIGH)

Address offset: 0x24

Reset value: 0x0000 0FFF

31–16
Reserved

15–12	11–0
Reserved	HTH[11:0]
	rw

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Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	HTH[11:0]	Analog watchdog high threshold These bits define the high thresholds for analog watchdog.

17.11.9 ADC watchdog low threshold register (ADC_WDGLOW)

Address offset: 0x28

Reset value: 0x0000 0000

31-16
Reserved

15-12	11-0
Reserved	LTH[11:0]
	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	LTH[11:0]	Analog watchdog low threshold These bits define the low thresholds for analog watchdog.

17.11.10 ADC regular sequence register 1 (ADC_RSEQ1)

Address offset: 0x2C

Reset value: 0x0000 0000

31-24	23-20	19-16
Reserved	LEN[3:0]	SEQ16[4:1]
	rw	rw

15	14-10	9-5	4-0
SEQ16_0	SEQ15[4:0]	SEQ14[4:0]	SEQ13[4:0]
rw	rw	rw	rw

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	LEN[3:0]	Regular channel sequence length These bits are software-defined as the number of channels in the regular sequence channel conversion. 0000: 1 conversion 0001: 2 conversions ... 1111: 16 conversions
19:15	SEQ16[4:0]	16th conversion in regular sequence These bits are software-defined as the number (0 to 18) of the 16th conversion channel in the conversion sequence.
14:10	SEQ15[4:0]	15th conversion in regular sequence

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Bit field	Name	Description
9:5	SEQ14[4:0]	14th conversion in regular sequence
4:0	SEQ13[4:0]	13th conversion in regular sequence

17.11.11 ADC regular sequence register 2 (ADC_RSEQ2)

Address offset: 0x30

Reset value: 0x0000 0000

31 30	29 25	24 20	19 16
Reserved	SEQ12[4:0]	SEQ11[4:0]	SEQ10[4:1]
	rw	rw	rw

15	14 10	9 5	4 0
SEQ10_0	SEQ9[4:0]	SEQ8[4:0]	SEQ7[4:0]
rw	rw	rw	rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ12[4:0]	12th conversion in regular sequence These bits are software-defined as the number (0 to 18) of the 12th conversion channel in the conversion sequence.
24:20	SEQ11[4:0]	11th conversion in regular sequence
19:15	SEQ10[4:0]	10th conversion in regular sequence
14:10	SEQ9[4:0]	9th conversion in regular sequence
9:5	SEQ8[4:0]	8th conversion in regular sequence
4:0	SEQ7[4:0]	7th conversion in regular sequence

17.11.12 ADC regular sequence register 3 (ADC_RSEQ3)

Address offset: 0x34

Reset value: 0x0000 0000

31 30	29 25	24 20	19 16
Reserved	SEQ6[4:0]	SEQ5[4:0]	SEQ4[4:1]
	rw	rw	rw

15	14 10	9 5	4 0
SEQ4_0	SEQ3[4:0]	SEQ2[4:0]	SEQ1[4:0]
rw	rw	rw	rw

Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ6[4:0]	6th conversion in regular sequence These bits are software-defined as the number (0 to 18) of the 6th transition channel in the conversion sequence.
24:20	SEQ5[4:0]	5th conversion in regular sequence
19:15	SEQ4[4:0]	4th conversion in regular sequence

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Bit field	Name	Description
14:10	SEQ3[4:0]	3rd conversion in regular sequence
9:5	SEQ2[4:0]	2nd conversion in regular sequence
4:0	SEQ1[4:0]	1st conversion in regular sequence

17.11.13 ADC Injection sequence register (ADC_JSEQ)

Address offset: 0x38

Reset value: 0x0000 0000

31 … 22	21 … 20	19 … 16
Reserved	JLEN[1:0]	JSEQ4[4:1]
	rw	rw

15	14 … 10	9 … 5	4 … 0
JSEQ4_0	JSEQ3[4:0]	JSEQ2[4:0]	JSEQ1[4:0]
rw	rw	rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21:20	JLEN[1:0]	Injected sequence length These bits are software-defined as the number of channels in the injected channel conversion sequence. 00: 1 conversion 01: 2 conversions 10: 3 conversions 11: 4 conversions
19:15	JSEQ4[4:0]	This is the 4th conversion in the injected sequence. These bits are software-defined as the number (0 to 18) of the fourth transition channel in the *conversion* sequence. *Note: Different from regular conversion sequences, if the length of ADC_JSEQ.JLEN[1:0] is less than 4, the sequence of conversion starts from (4-JLEN). For example, ADC_JSEQ[21:0] = 10 00011 00011 00111 00010 means that the scan conversion will be converted in the following channel order: 7, 3, 3 instead of 2, 7, 3.*
14:10	JSEQ3[4:0]	3rd conversion in injected sequence
9:5	JSEQ2[4:0]	2nd conversion in injected sequence
4:0	JSEQ1[4:0]	1st conversion in injected sequence

17.11.14 ADC injection data register x (ADC_JDATx) (x= 1…4)

Address offset: 0x3C - 0x48

Reset value: 0x0000 0000

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31–16
Reserved

15–0
JDAT
r

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	JDAT[15:0]	Injected data for conversions These bits are read-only and contain the conversion results of the injected channel. The data is left-aligned or right-aligned

17.11.15 ADC regulars data register (ADC_DAT)

Address offset: 0x4C

Reset value: 0x0000 0000

31–16
Reserved

15–0
DAT[15:0]
r

Bit field	Name	Description
32:16	Reserved	Reserved, the reset value must be maintained
15:0	DAT[15:0]	Regular data for conversion These bits are read-only and contain the conversion results of the regular channel. The data is left-aligned or right-aligned as shown in Table 17-3 and Table 17-4.

17.11.16 ADC differential mode selection register (ADC_DIFSEL)

Address offset: 0x50

Reset value: 0x0000 0000

31–19	18–16
Reserved	DIFSEL[17:0]
	rw

15–1	0
DIFSEL[17:0]	Reserved
rw	

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
18:1	DIFSEL[17:0]	Differential mode for channels 18 to 1 DIFSEL[i] = 0: ADC channel input i+1 is configured in single-ended mode; DIFSEL[i] = 1: ADC channel input i+1 is configured in differential mode
0	Reserved	Reserved, the reset value must be maintained

17.11.17 ADC calibration factor (ADC_CALFACT)

Address offset: 0x54

Reset value: 0x0000 0000

31 … 23	22 … 16
Reserved	CALFACTD[6:0]
	rw

15 … 7	6 … 0
Reserved	CALFACTS[6:0]
	rw

Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22:16	CALFACTD[6:0]	Calibration factors in differential mode This bit can be written by hardware or software After the differential input calibration is complete, the hardware will update it according to the calibration coefficient. Software can write these bits with a new calibration factor. If the new calibration coefficient is different from the current coefficient stored in the analog ADC, the coefficient will be applied after a new differential calibration is initiated. *Note: software allows write only when ADC_CTRL2.ON=1, ADC_STS.STR =0, ADC_STS.JSTR =0 (ADC does not process conversion or start conversion)*
15:7	Reserved	Reserved, the reset value must be maintained
6:0	CALFACTS[6:0]	Calibration factors in Single-Ended mode This bit can be written by hardware or software After the single-end input calibration is completed, the hardware will update it according to the calibration coefficient. Software can write these bits with a new calibration factor. If the new calibration coefficient is different from the current coefficient stored in the analog ADC, the coefficient will be applied after a new single-ended calibration is initiated. *Note: software allows write only when ADC_CTRL2.ON=1, ADC_STS.STR =0, ADC_STS.JSTR =0 (ADC does not process conversion or start conversion)*

17.11.18 ADC control register 3 (ADC_CTRL3)

Address offset: 0x58

Reset value: 0x0000 0043

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31 … 16
Reserved

15 … 11	10	9	8	7	6	5	4	3	2	1 … 0
Reserved	DPWMOD	JENDC AIEN	ENDC AIEN	BPCAL	PDRDY	RDY	CKMOD	CALALD	CALDIF	RES[1:0]
	rw	rw	rw	rw	r	r	rw	rw	rw	rw

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	VBATMEN	Vbat monitor enable 0: Disable 1: Enable
10	DPWMOD	Deep power mode 0: When the ADC is disabled, the ADC enters low power mode 1: When the ADC is disabled, the ADC enters deep sleep mode
9	JENDCAIEN	Interrupt enable for any injected channels This bit is set and cleared by the software to enable/disable any channel conversion end interrupt 0: ADC_STS.JENDCA interrupt is disabled 1: ADC_STS.JENDCA interrupt is enabled
8	ENDCAIEN	Interrupt enable for any regular channels This bit is set and cleared by the software to enable/disable regular channel conversion to end the interrupt 0: ADC_STS.ENDCA interrupt is disabled 1: ADC_STS.ENDCA interrupt is enabled
7	BPCAL	Bypass calibration 0: Disable 1: Enabled
6	PDRDY	ADC power down ready 0: Not ready 1: Get ready
5	RDY	ADC ready 0: Not ready 1: Get ready
4	CKMOD	Clock mode 0: Select AHB for synchronization clock 1: Select PLL for asynchronous clock
3	CALALD	Calibration auto load 0: Disables automatic loading 1: Enables automatic loading
2	CALDIF	Differential mode for calibration This bit is set and cleared by software to configure the calibrated single-ended or differential input mode

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Bit field	Name	Description
		0: Writing ADC_CTRL2.ENCAL bits will start calibration in single-ended input mode 1: Writing ADC_CTRL2.ENCAL bits will start calibration in differential input mode
1:0	RES[1:0]	Data resolution This bit is set and cleared by the software to select the resolution of the conversion 00: 6-bits 01: 8-bits 10: 10-bits 11: 12-bits

17.11.19 ADC sampling time register 3 (ADC_SAMPT3)

Address offset: 0x5C

Reset value: 0x0000 0000

15 … 4	3	2 … 0
Reserved	SAMPSEL	SAMP18[2:0]
	rw	rw

Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3	SAMPSEL	Sample Time Selection When SAMPSEL = 0, the value of SAMPx[2:0] is set as follows: 000: 1.5 cycles 100: 41.5 cycles 001: 7.5 cycles 101: 55.5 cycles 010: 13.5 cycles 110: 71.5 cycles 011: 28.5 cycles 111: 239.5 cycles When SAMPSEL = 1, the value of SAMPx[2:0] is set as follows: 000: 1.5 cycles 100: 19.5 cycles 001: 2.5 cycles 101: 61.5 cycles 010: 4.5 cycles 110: 181.5 cycles 011: 7.5 cycles 111: 601.5 cycles
2:0	SAMP18[2:0]	Channel Sample Time The channel sampling time definition is consistent with ADC_SAMPT2

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18 Digital to analog conversion (DAC)

18.1 Introduction

DAC is a digital/analog converter, mainly digital input, voltage output.DAC data can be 8-bit or 12-bit and supports DMA functionality.When the DAC is configured in 12-bit mode, the DAC data can be right-aligned or left-aligned.When the DAC is configured in 8-bit mode, the DAC data can be right-aligned.The DAC output channel has 1, with independent converter.VREF+ is used as the DAC reference voltage through the pin input to make the DAC conversion data more accurate.

18.2 Main features

- One independent DAC converter, corresponding to one output channel
- Monotonous output
- Support 8-bit or 12-bit output, data in 12-bit mode right-aligned and left-aligned two modes
- Synchronous update
- DMA support
- Noise wave, triangular waveform generation
- Input reference voltage VREF+
- External event triggers the conversion

DAC block diagram and pins are shown below.

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Figure 18-1 Block diagram of a DAC channel

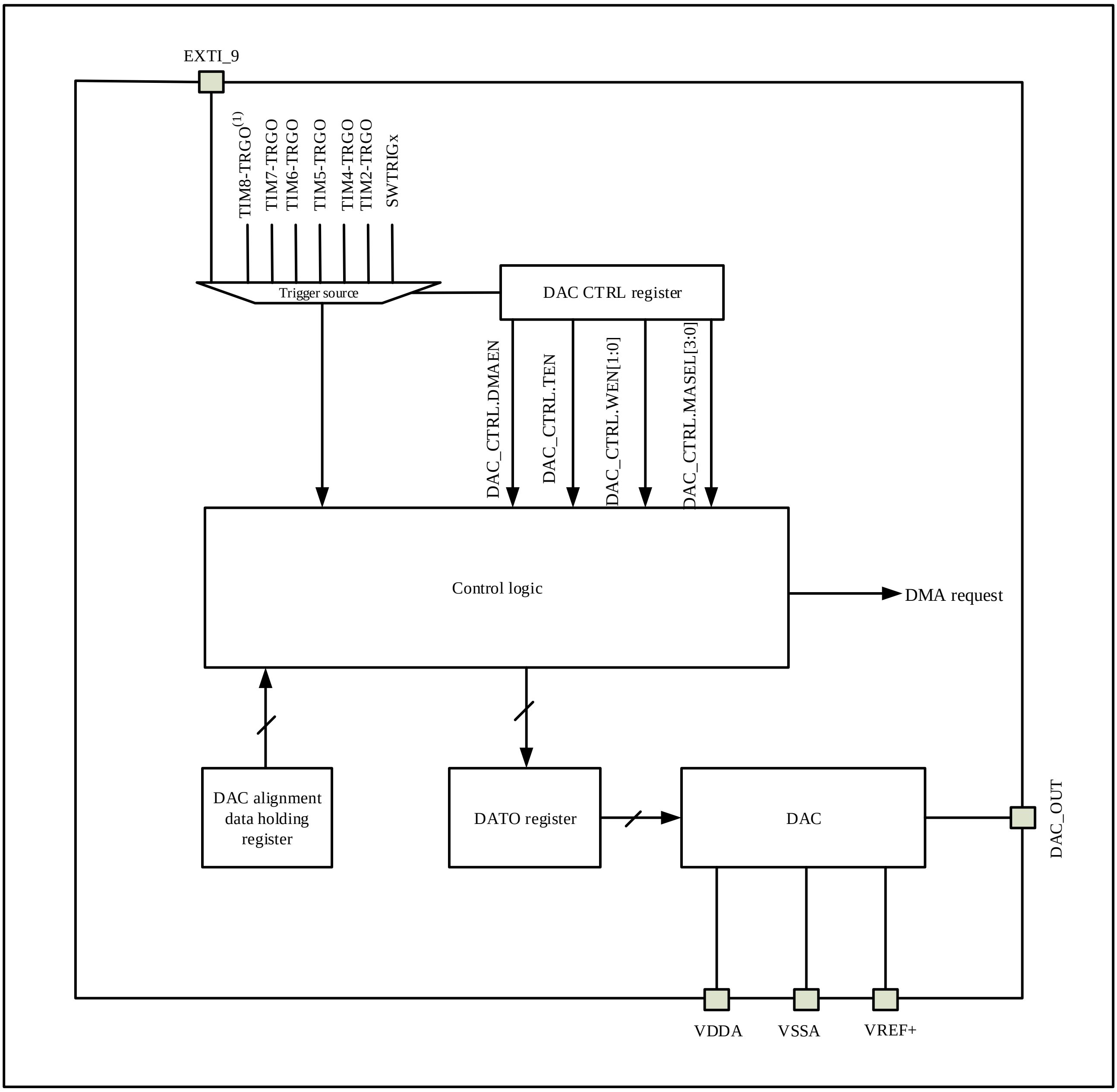

Table 18-1 DAC pins

Name	Description	Type
V_{REF+}	The positive reference voltage used by the DAC,2.4 V≤ V_{REF+}≤V_{DDA} (3.3 V)	Input, analog reference voltage
V_{DDA}	Analog power supply	Input, analog power supply
V_{SSA}	Analog power supply ground	Input, analog power supply ground
DAC_OUT	DAC analog output	Analog output signal

Note: When the DAC is enabled, PA4 needs to be configured as analog input mode. PA4 will automatically connect

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to the output of the DAC.

18.3 DAC function description and operation description

18.3.1 DAC enable

Powering on the DAC can be done by configuring DAC_CTRL. CHEN = 1. It takes some time for t_{WAKEUP} to open the DAC.

18.3.2 DAC output buffer.

By configuring DAC_CTRL.BEN to disable or enable the output buffer of DAC, if the output buffer is enable, the output impedance is reduced, the driving ability is enhanced, and the external load can be driven without the external operational amplifier.

18.3.3 DAC data format

When the configuration data is written to the DAC_DR12CH register, the data is written to DAC_DR12CH [11:0], and the 12-bit data is right-aligned. (Actually stored in the register DACCHD [11:0] bits, DACCHD is the internal data storage register)

When the configuration data is written to the DAC_DL12CH register, the data is written to DAC_DL12CH [15:4], and the 12-bit data is left-aligned. (Actually stored in the register DACCHD [11:0] bits, DACCHD is the internal data storage register)

When the configuration data is written to the DAC_DR8CH register, the data is written to DAC_DR8CH [7:0], and the 8-bit data is right-aligned. (Actually stored in the register DACCHD[11:4] bits, DACCHD is the internal data storage register)

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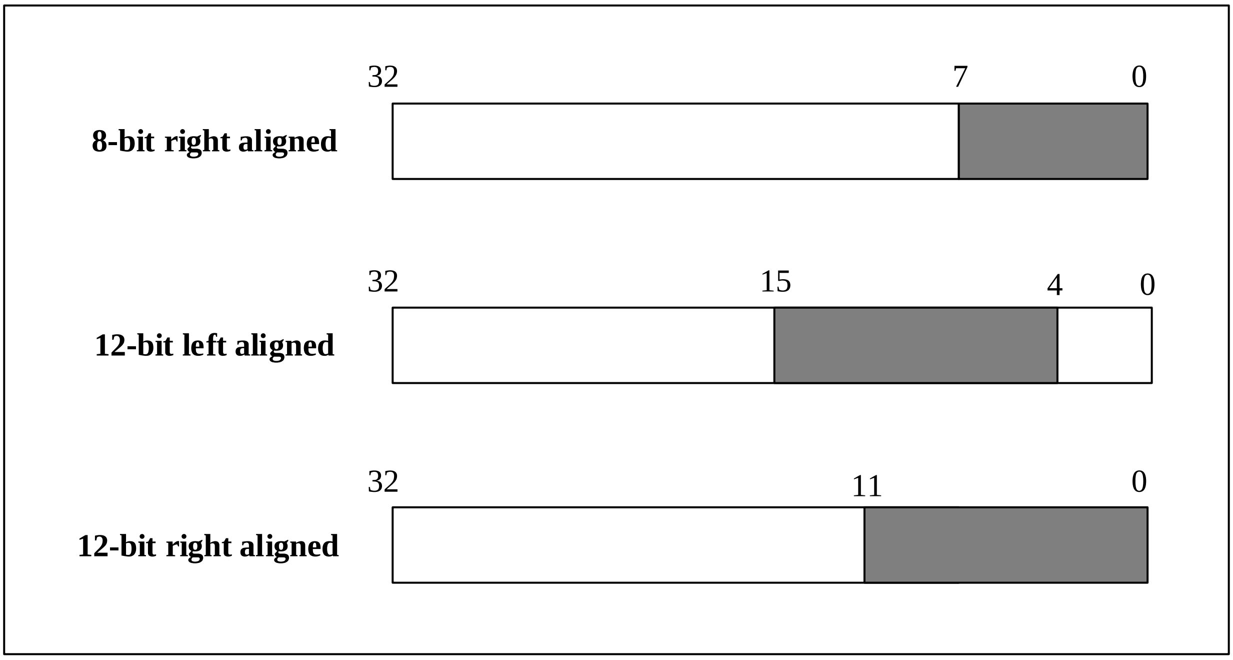
Figure 18-2 Data register of single DAC channel mode



18.3.4 DAC trigger

Configure DAC_CTRL. TEN = 1 can enable external trigger of DAC, and DAC_CTRL. TSEL [2:0] is configured to select an external triggering event as the external triggering source for the DAC.

Table 18-2 DAC external trigger

Trigger source	Type	TSEL[2:0]
Timer 6 TRGO events	Internal signal from the on-chip timer	000
Timer 8 TRGO events		001
Timer 7 TRGO events		010
Timer 5 TRGO events		011
Timer 2 TRGO events		100
Timer 4 TRGO events		101
EXTI line 9	External pins	110
SWTRIG (Software Triggered)	Software control bit	111

When the DAC is triggered by timer output or the rising edge of EXTI line 9, when triggered, the data in the aligned data hold register will be transferred to the DAC_DATO register. This data transfer process takes 3 APB1 clock cycles.

DAC_SOTTR.TREN = 1 can enable the DAC software trigger. When the DAC is triggered by the software, the data of the aligned data hold register will be transmitted to the DAC_DATO register.

Note:

1. Do not change the DAC_CTRL.TSEL[2:0] bit when the DAC is enabled.

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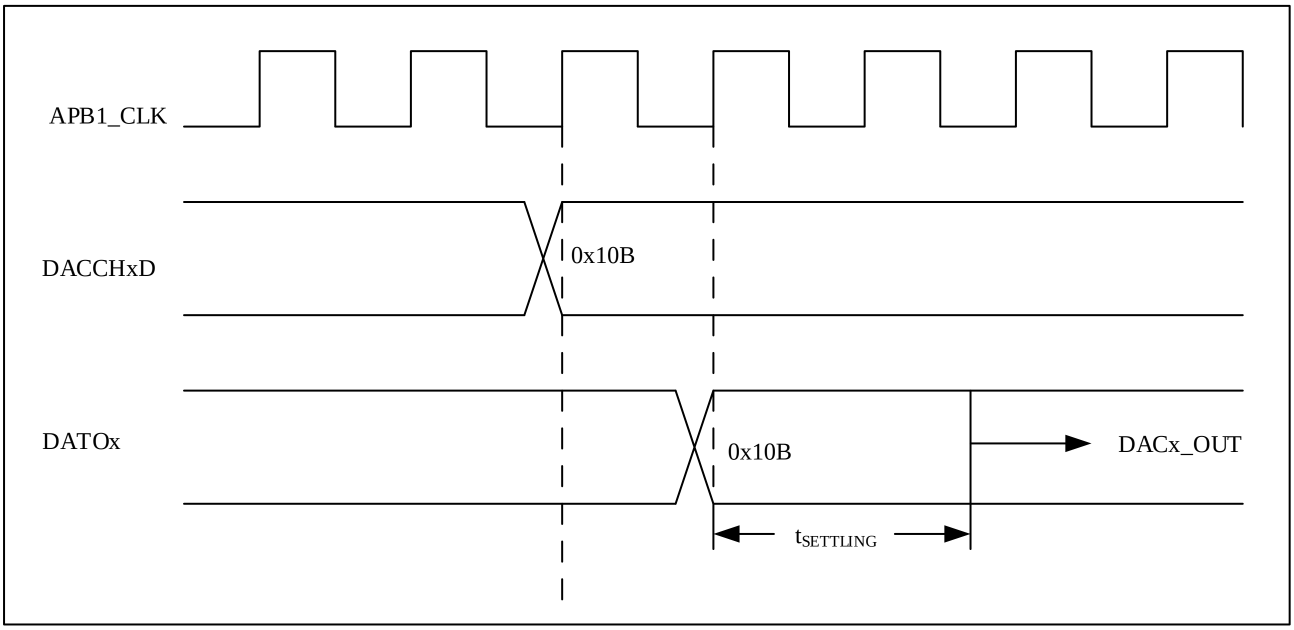
2. It takes 1 APB1 clock cycle for the data of the aligned data holding register to be transferred to the DAC_DATO register when triggered by software.

18.3.5 DAC conversion

If DAC trigger is on, the data in the DAC alignment data hold register will be transferred to the DAC_DATO register after three APB1 cycles according to the selected trigger event when the hardware trigger occurs. When the software trigger occurs, the data in the DAC alignment data hold register is transferred to the DAC_DATO register after one APB1 cycle.If trigger is not enabled, data in the DAC alignment data hold register is automatically transferred to the DAC_DATO register after one APB1 cycle.

After the DAC transfers data to the DAC_DATO register from its data hold register, the output is valid for the time tSETTTLING, which is related to the supply voltage and the analog output load.

Figure 18-3 Time diagram of transitions with trigger disable



18.3.6 DAC output voltage

The digital input is converted to analog voltage output by a DAC module in a linear relationship ranging from 0 to VREF+.The output voltage of DAC is calculated as follows:

DAC output = V_{REF} X (DATO / 4095).

18.3.7 DMA requests

DAC_CTRL1. DMAEN = 1 is configured to enable DMA function. When an external trigger occurs (not a software trigger), a DMA request is generated and the data aligned with the data hold register is then transferred to the DAC_DATO register.

Note: DMA requests for DAC have no accumulative function, and when the second external trigger occurs before the

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response to the first external trigger, the second DMA request cannot be processed and there is no error reporting mechanism.

18.3.8 The noise

DAC can generate noise, by configuring DAC_CTRL.WEN[1:0] to "01" to turn on the noise function, by configuring DAC_CTRL.MASEL[3:0] to select which bits of the linear feedback shift register (LFSR) are masked, the value of LFSR is added to the value of the DAC alignment data holding register and written to the DAC_DATO register (overflow bits are discarded). The initial value of LFSR is 0xAAA, and the value of LFSR is updated after 3 APB1 cycles after the trigger event occurs.

Figure 18-4 LFSR algorithm for DAC

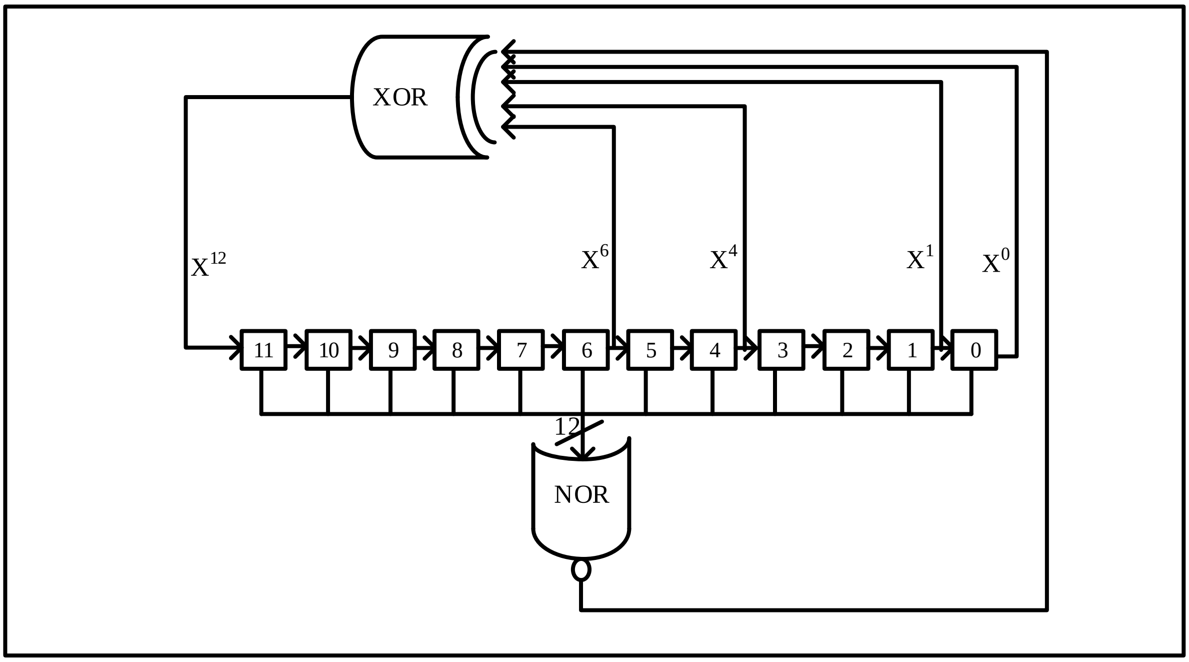

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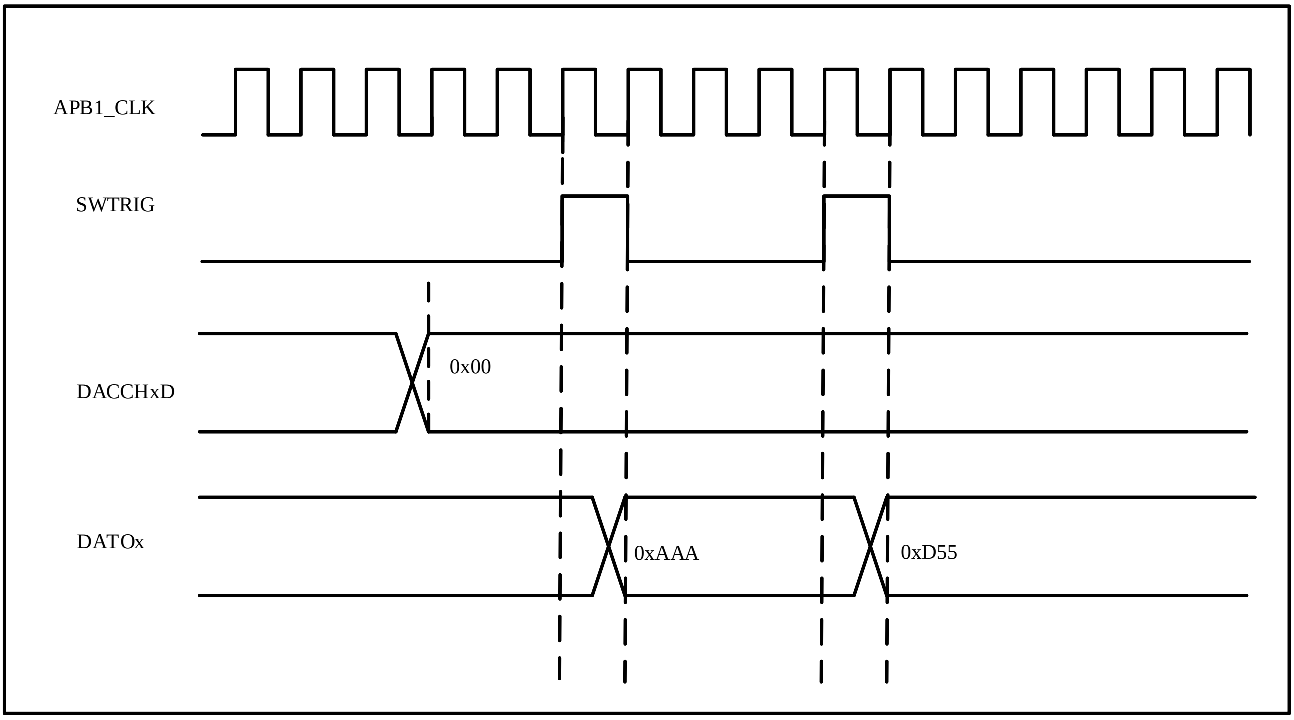
Figure 18-5 DAC conversion with LFSR waveform generation (enable software trigger)



Note: The DAC is configured to trigger to generate noise.

18.3.9 Triangular wave generation

The DAC can generate a triangle wave. The triangle wave function can be turned on by configuring DAC_CTRL.WEN[1:0] as "10", and the amplitude of the triangle wave can be selected by configuring DAC_CTRL.MASEL[3:0].The value of the internal triangle wave counter is added to the value of the DAC alignment data holding register and written to the DAC_DATO register (overflow bits are discarded).The value of the triangular wave counter is updated 3 APB1 cycles after the trigger event occurs, the triangular wave counter will accumulate to the maximum amplitude value set, and then decrement to 0, and so on.

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Figure 18-6 Triangle wave generation of DAC

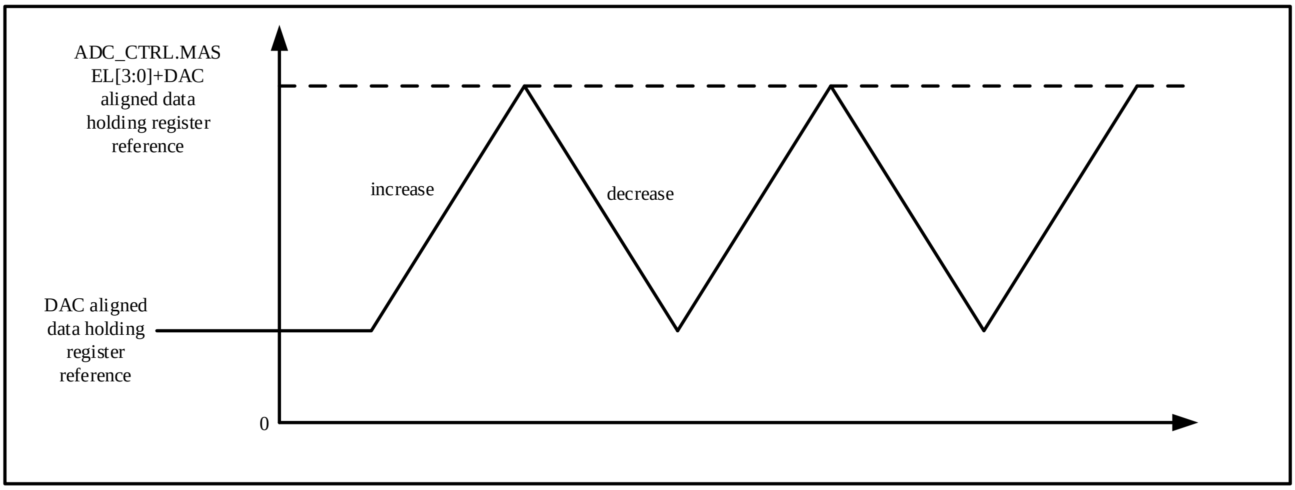
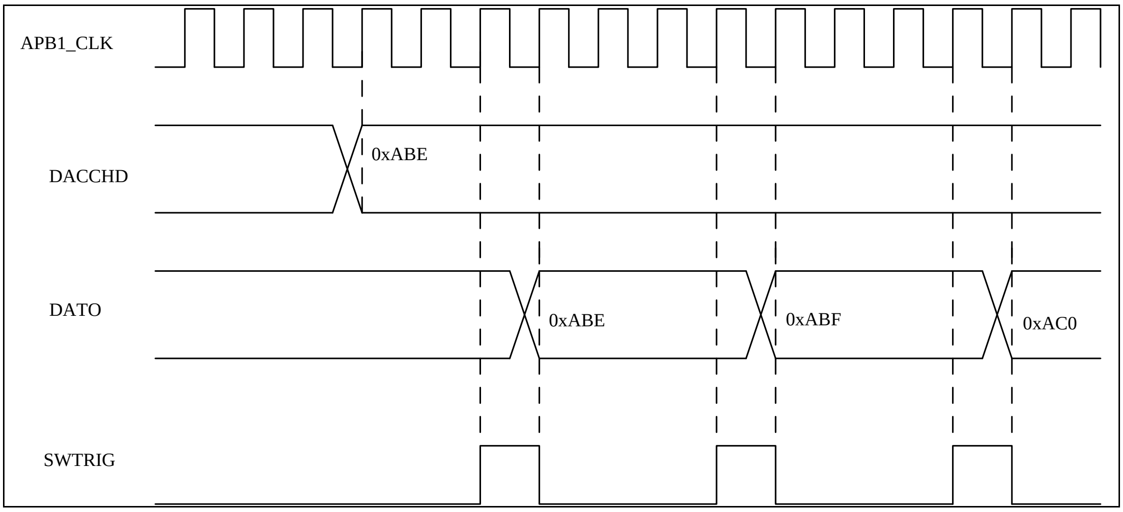


Figure 18-7 DAC conversion with trigonometry generation (enable software trigger)



Note: 1. Only when the DAC is configured to trigger can the triangle wave be generated

2. DAC_CTRL.MASEL[3:0] *cannot be set after DAC is enabled.*

18.4 DAC register

18.4.1 DAC registers overview

Table 18-3 DAC registers overvie

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DAC_CTRL	Reserved																			DMAEN	MASEL[3:0]				WEN[1:0]		TSEL[2:0]			TEN	BDIS	CHEN
	Reset Value																				0	0	0	0	0	0	0	0	0	0	0	0	0
004h	DAC_SOTTR	Reserved																															TREN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																																0
008h	DAC_12DRCH	Reserved																				DACCHD[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
00Ch	DAC_12DLCH	Reserved																DACCHD[11:0]												Reserved			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0				
010h	DAC_8DRCH	Reserved																								DACCHD[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
02Ch	DAC_DATO	Reserved																				DACCHDO[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0

18.4.2 DAC control register (DAC_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

31:16
Reserved

15:13	12	11:8	7:6	5:3	2	1	0
Reserved	DMAEN	MASEL[3:0]	WEN[1:0]	TSEL[2:0]	TEN	BEN	CHEN
	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	DMAEN	The DMA function of the DAC is enabled The bit is set to 1 and cleared by the software. 0: Disable DMA for the DAC 1: Enable DMA for the DAC
11:8	MASEL[3:0]	DAC shield/amplitude selector. These bits are configured by software to set the LFSR shielding bits for the noise function and the amplitude of the triangular wave.0000: unmasked LFSR bit 0 / delta amplitude equals 1 0001: unmasked LFSR bit [1:0] / triangular amplitude is equal to 3 0010: unmasked LFSR bit [2:0] / triangular amplitude equals 7 0011: unmasked LFSR bit [3:0] / triangular amplitude equals 15 0100: unmasked LFSR bit [4:0] / triangular amplitude equals 31 0101: Unmasked LFSR bit [5:0] / triangular amplitude equals 63 0110: unmasked LFSR bit [6:0] / triangular amplitude equals 127 0111: Unmasked LFSR bit [7:0] / triangular amplitude equals 255 1000: unmasked LFSR bit [8:0] / triangular amplitude equals 511 1001: Unmasked LFSR bit [9:0] / triangular amplitude equals 1023 1010: unmasked LFSR bit [10:0] / triangular amplitude equals 2047 ≥1011: unmasked LFSR bit [11:0] / triangular amplitude is equal to 4095
7:6	WEN[1:0]	DAC noise/triangle wave function selection. The bits are set to 1 and cleared by the software.

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Bit field	Name	Description
		00: Disable noise and triangle wave 01: Enable the noise function 1x: Enables the triangle wave function
5:3	TSEL[2:0]	DAC triggers selection. This bit is used for selection of DAC external triggers. 000: TIM6 TRGO event 001: TIM8 TRGO event 010: TIM7 TRGO event 011: TIM5 TRGO event 100: TIM2 TRGO event 101: TIM4 TRGO event 110: External interrupt line 9 111: Software trigger
2	TEN	DAC trigger on This bit is set to 1 and cleared by the software to enable/disable DAC triggering. 0: disables DAC triggering 1: enables DAC triggering
1	BEN	Enable the DAC output cache. This bit is set to 1 and cleared by the software to enable/disable the DAC's output buffer. 0: Disable the DAC channel output buffer 1: Enable the DAC channel output buffer
0	CHEN	DAC. This bit is set to 1 and cleared by the software to enable/disable the DAC. 0: disables the DAC 1: Enable the DAC

18.4.3 DAC software trigger register (DAC_SOTTR)

Offset address: 0x04

Reset value: 0x0000 0000

31–16
Reserved

15–1	0
Reserved	TREN
	w

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	TREN	DAC software trigger

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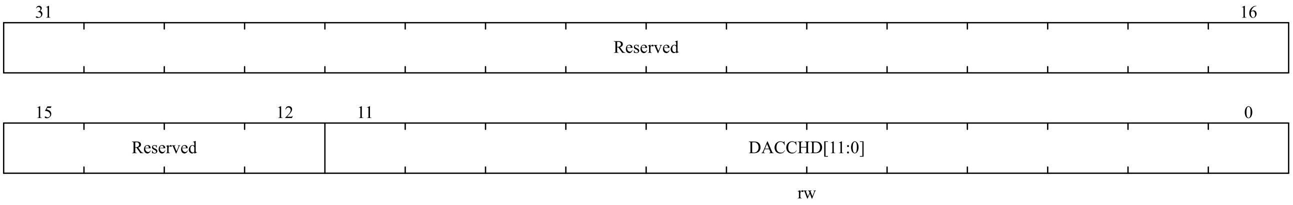
Bit field	Name	Description
		This bit is setting by software to enable/disable software trigger. 0: Disable the DAC software trigger. 1: Enable the DAC software trigger. *Note: After the alignment data hold register transfers data to the DAC_DATO register, this bit will be cleared by the hardware after an APB1 clock.*

18.4.4 12 bit right aligned data hold register for DAC (DAC_DR12CH)

Offset address: 0x08

Reset value: 0x0000 0000

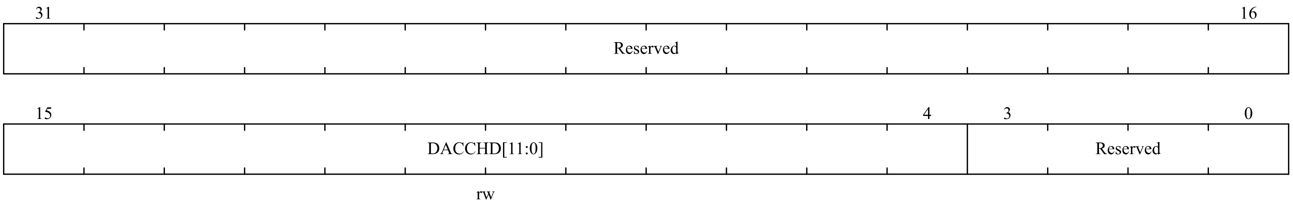


Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	DACCHD[11:0]	DAC12 bits right aligned data The bits are configured by the software and the DAC converts the data.

18.4.5 12 bit left aligned data hold register for DAC (DAC_DL12CH)

Offset address: 0x0c

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:4	DACCHD[11:0]	DAC12 bits left aligned data The bits are configured by the software and the DAC converts the data.
3:0	Reserved	Reserved, the reset value must be maintained.

18.4.6 8-bit right-aligned data hold register for DAC (DAC_DR8CH)

Offset address: 0x10

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Reset value: 0x0000 0000

31 … 16
Reserved

15 … 8	7 … 0
Reserved	DACCHD[7:0]
	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DACCHD[7:0]	DAC8 bits right aligned data The bits are configured by the software and the DAC converts the data.

18.4.7 DAC data output register (DAC_DATO)

Offset address: 0x2C

Reset value: 0x0000 0000

31 … 16
Reserved

15 … 12	11 … 0
Reserved	DACCHDO[11:0]
	r

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	DACCHDO[11:0]	DAC data output. These bits are read-only and represent the output data of the DAC channel

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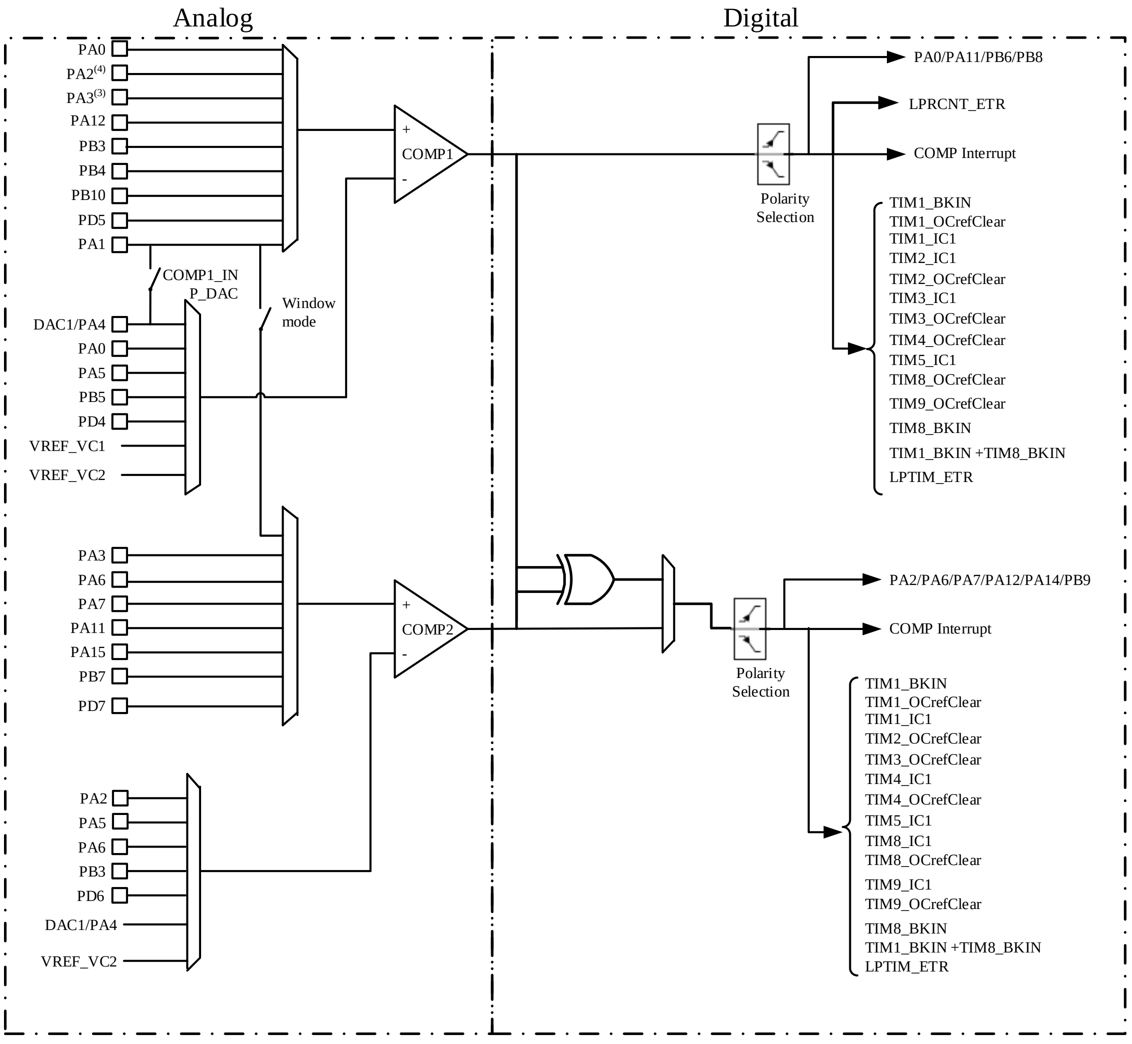
19 Comparator (COMP)

The COMP module is used to compare the analog voltages of two inputs and output high/low levels based on the comparison results. When "INP" input voltage is higher than "INM" input voltage, the comparator output is high level, when "INP" input voltage is lower than "INM" input voltage, the comparator output is low level.

19.1 COMP system connection block diagram

The COMP module supports a maximum of two independent comparators, which are connected to the APB1 bus..

Figure 19-1 Comparator Controller Functional Diagram



Notice:

1. VREF_VC1 is the output of the internal low-power 6bit DAC, and VREF_VC2 is the output of the internal non-low-power 6bit DAC;

2. COMP1 supports dual mode (supports both low power mode and normal mode), COMP2 only supports single mode (supports normal mode);

3. The second character in the 8-bit code of the last line of the chip printed in the factory setting is not "B"

4. The second character in the 8-bit code of the last line of the chip printed in the factory setting is "B"

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19.2 COMP features

- Up to 2 independent comparators
- Share the internal reference input of two independent 6bit DAC
- Support filter clock, filter reset
- Output polarity can be configured high and low
- Hysteresis The value can be none, low, medium, or high
- The comparison result can be output to the I/O port or trigger timer, which is used to capture events, OCREF_CLR events, brake events, and generate interrupts
- Input channel can select I/O port, channel output of general 12bit DAC, dedicated 6bit DAC
- It can be read - only or read - write, and can be unlocked only after a reset
- Blanking support, Blanking source can be configured to produce Blanking
- COMP1/COMP2 can form window comparators
- You can wake the system from Sleep mode mode by generating an interrupt
- Filter window size can be configured
- Filter threshold size can be configured
- The sampling frequency for filtering can be configured

19.3 COMP configuration process

Complete configuration items are as follows. If the default configuration is used, skip the corresponding configuration items.

1. Configurable hysteresis level COMPx_CTRL.HYST[1:0]
2. Configure the output polarity COMPx_CTRL.POL
3. Configuration input selection, comparator non-inverting input COMPx_CTRL.INPSEL[3:0], inverting input COMPx_CTRL. INMSEL [2:0]
4. Select COMPx_CTRL.OUTSEL[3:0]for configuration output
5. Configure the blanking source COMPx_CTRL.BLKING[2:0]
6. Configure the comparator window mode COMP_WINMODE. CMP12MD
7. Configure the filter sampling window COMPx_FILC.SAMPW[4:0]
8. Configure the threshold COMPx_FILC.THRESH[4:0] (threshold should be greater than COMPx_FILC.SAMPW[4:0]/2)
9. Configure the filter sampling frequency (for timer applications, sampling frequency should be greater than 5MHz)

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10. Enable COMPx_FILC.FILEN filter

11. Enable COMPx_CTRL.EN on the comparator

Note: For the above steps, the filter should be enabled first and then the comparator should be enabled. The comparator should be enabled after the filtering (if enabled) is configured and enabled. In addition, when the comparator control register is locked, the LOCK can be cancelled only through reset.

19.4 COMP working mode

19.4.1 Window mode

Comparator 1 and comparator 2 share PA1 to form window comparators.

19.4.2 Independent comparator

The two comparators can be configured independently to complete the comparator function. The output of a comparator can be output to an I/O port. Each comparator has a different remapped port. You can configure the comparator register COMPx_CTRL. OUTTRG[3:0] to enable the corresponding feature pin at the output.

Comparator output, support trigger events, such as can be configured as timer 1, timer 8 brake function.

Note: Refer to the comparator interconnection for specific configuration

19.5 Comparator interconnection

For the interconnection of the output port of the comparator, please refer to the chapter on the multiplexing function of GPIO, which defines the value of the remapping of the comparator OUT.

The comparator INP pin has the following configuration.

INPSEL	COMP1	COMP2
0xxx	Float	Float
1000	PA0	PA1/DAC1/PA4
1001	PA1/DAC1	PA3
1010	PA2	PA6
1011	PA12	PA7
1100	PB3	PA11
1101	PB4	PA15
1110	PB10	PB7
1111	PD5	PD7

Note 1: In window mode, COMP2 automatically selects PA1

Note 2: The selection of the comparator's PA1/DAC1 is done by configuring COMP1_CTRL.INPDAC

The comparator INM pins have the following configuration.

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INMSEL	COMP1	COMP2
000	Float	Float
001	DAC1/PA4	PA2
010	PA0	PA5
011	PA5	PA6
100	PB5	PB3
101	PD4	PD6
110	VREF_VC1	DAC1/PA4
111	VREF_VC2	VREF_VC2

Note: DAC1/PA4, indicating that the output pin of DAC1 is PA4

Comparator output TRIG signal has the following interconnection.

TRIG	COMP1	COMP2
0000	NC	NC
0001	TIM1_BKIN	TIM1_BKIN
0010	TIM1_OCrefclear	TIM1_OCrefclear
0011	TIM1_IC1	TIM1_IC1
0100	TIM2_IC1	TIM2_OCrefclear
0101	TIM2_OCrefclear	TIM3_OCrefclear
0110	TIM3_IC1	TIM4_IC1
0111	TIM3_OCrefclear	TIM4_OCrefclear
1000	TIM4_OCrefclear	TIM5_IC1
1001	TIM5_IC1	TIM8_IC1
1010	TIM8_IC1	TIM8_OCrefclear
1011	TIM8_OCrefclear	TIM9_IC1
1100	TIM9_OCrefclear	TIM9_OCrefclear
1101	TIM8_BKIN	TIM8_BKIN
1110	TIM1_BKIN+TIM8_BKIN	TIM1_BKIN + TIM8_BKIN
1111	LPTIM_ETR	LPTIM_ETR

19.6 Interrupt

COMP supports interrupt response, and COMP1, and COMP2 each occupy one interrupt entry. There are two cases of interrupt generation as follows.

- The polarity of COMPx_CTRL.POL is not reversed, and the interrupt is enabled. When INPSEL > INMSEL, the comparator interrupt will be generated when COMPx_CTRL.OUT is set to 1 by hardware.
- The polarity of COMPx_CTRL.POL is reversed, and the interrupt is enabled. When INPSEL < INMSEL, the comparator interrupt is generated when COMPx_CTRL.OUT is set to 1 by hardware.

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19.7 COMP register

19.7.1 COMP register overview

Table 19-1 COMP register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	COMP_INTEN	Reserved																														CMP2IEN	CMP1IEN
	Reset Value																															0	0
004h	COMP_LPCKSEL	Reserved																															LPCKSEL
	Reset Value																																0
008h	COMP_WINMODE	Reserved																															CMP12MD
	Reset Value																																0
00Ch	COMP_LOCK	Reserved																														CMP2LK	CMP1LK
	Reset Value																															0	0
010h	COMP1_CTRL	Reserved										PWRMODE	INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTTRG[3:0]				INPSEL[3:0]				Reserved	INMSEL[2:0]			EN
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0
014h	COMP1_FILC	Reserved																					SAMPWIN[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
018h	COMP1_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	Reserved																																
020h	COMP2_CTRL	Reserved												OUT	BLKING[2:0]			HYST[1:0]		POL	OUTTRG[3:0]				INPSEL[3:0]				Reserved	INMSEL[2:0]			EN
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0
024h	COMP2_FILC	Reserved																					SAMPWIN[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
028h	COMP2_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
02Ch	COMP2_OSEL	Reserved																															CMP2XO
	Reset Value																																0
030h	COMP_VREFSCL	Reserved																		VV2TRM[5:0]						VV2EN	VV1TRM[5:0]						VV1EN
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	COMP_TEST	Reserved																															EN
	Reset Value																																0
038h	COMP_INTSTS	Reserved																														CMP2IS	CMP1IS
	Reset Value																															0	0

19.7.2 COMP interrupt enable register (COMP_INTEN)

Address offset : 0x00

Reset value : 0x0000 0000

15 ... 2	1	0
Reserved	CMP2IEN	CMP1IEN
	rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained
1	CMP2IEN	Software controlled Interrupt enable of COMP2. 0: Disable 1: Enable
0	CMP1IEN	Software controlled Interrupt enable of COMP1. 0: Disable 1: Enable

19.7.3 COMP low power select register (COMP_LPCKSEL)

Address offset : 0x04

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Reset value : 0x0000 0000

31–16
Reserved

15–1	0
Reserved	LPCKSEL
	rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	LPCKSEL	Comparator clock select 0: Configure this bit to 0 in normal mode, use PCLK1 clock; 1: Configure this bit to 1 during STOP2 or low power operation, using a 32 KHz clock.

19.7.4 COMP window mode register (COMP_WINMODE)

Address offset : 0x08

Reset value : 0x0000 0000

31–16
Reserved

15–1	0
Reserved	CMP12MD
	rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	CMP12MD	This bit selects the window mode: Both non inverting inputs of comparators share the Pin PA1 input. 0: Comparators 1 and 2 are not in window mode. 1: Comparators 1 and 2 are in window mode.

19.7.5 COMP lock register (COMP_LOCK)

Address offset : 0x0C

Reset value : 0x0000 0000

15–2	1	0
Reserved	CMP2LK	CMP1LK
	rw	rw

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Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2	CMP2LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP2_ CTRL register to be read-only. 0: COMP2_ CTRL is read-write. 1: COMP2_CTRL is read-only
2	CMP1LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP1_ CTRL register to be read-only. 0: COMP1_ CTRL is read-write. 1: COMP1_CTRL is read-only

19.7.6 COMP1 control register (COMP1_CTRL)

Address offset : 0x10

Reset value : 0x0000 0000

31–22	21	20	19	18–16
Reserved	PWRMODE	INPDAC	OUT	BLKING[2:0]
	rw	rw	r	rw

15–14	13	12–9	8–5	4	3–1	0
HYST[1:0]	POL	OUTTRG[3:0]	INPSEL[3:0]	Reserved	INMSEL[2:0]	EN
rw	rw	rw	rw		rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	PWRMODE	Power mode of Comparator 1 These bits are set and cleared by software. They control the power/speed of Comparator1. 0: Normal mode 1: Low power mode
20	INPDAC	The connection selection bit of the PA1 of the INP of the comparator 1 and the DAC output 0: Connect to PA1; 1: Connect to DAC output.
19	OUT	This read-only bit is a copy of comparator 1 output state. 0: Output is low (non-inverting input below inverting input). 1: Output is high (non-inverting input above inverting input).
18：16	BLKING[2:0]	These bits select which Timer output controls the comparator 1 output blanking. 000: No blanking 001: TIM1 OC5 selected as blanking source 010: TIM8 OC5 selected as blanking source Other configurations: reserved
15:14	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis

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Bit field	Name	Description
		01: Low hysteresis 10: Medium hysteresis 11: High hysteresis
13	POL	This bit is used to invert the comparator 1 output. 0: Output is not inverted 1: Output is inverted
12:9	OUTTRG[3:0]	These bits select which Timer input must be connected with the comparator1 output. 0000：Reserved； 0001：TIM1_BKIN； 0010：TIM1_OCrefclear； 0011：TIM1_IC1； 0100：TIM2_IC1； 0101：TIM2_OCrefclear； 0110：TIM3_IC1； 0111：TIM3_OCrefclear； 1000：TIM4_OCrefclear； 1001：TIM5_IC1； 1010：TIM8_IC1； 1011：TIM8_OCrefclear； 1100：TIM9_OCrefclear； 1101：TIM8_BKIN； 1110：TIM1_BKIN+TIM8_BKIN； 1111：LPTIM_ETR。
8:5	INPSEL[3:0]	Comparator 1 non-inverting input selection. 0000 to 0111：Floating input； 1000：PA0； 1001：PA1/DAC； 1010：PA3(PA2)； 1011：PA12； 1100：PB3； 1101：PB4； 1110：PB10； 1111：PD5。 *Note: When the configuration is 1010, PA3 is suitable for factory setting the second character in the 8-bit code of the last line of the chip silk screen to be non-"B". PA2 is suitable for factory setting the second character in the 8-bit code of the last line of the chip silk screen to be "B".*
4	Reserved	Reserved, the reset value must be maintained
3:1	INMSEL[2:0]	These bits allows to select the source connected to the inverting input of the comparator 1. 000：floating； 001：DAC1；

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Bit field	Name	Description
		010：PA0； 011：PA5； 100：PB5； 101：PD4； 110：VREF_VC1； 111：VREF_VC2。
0	EN	This bit switches COMP1 ON/OFF. 0: Comparator disabled 1: Comparator enabled

19.7.7 COMP1 filter register (COMP1_FILC)

Address offset : 0x14

Reset value : 0x0000 0000

31–16
Reserved

15–11	10–6	5–1	0
Reserved	SAMPW[4:0]	THRESH[4:0]	FILEN
	rw	rw	rw

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable. 0: Disable 1: Enable

19.7.8 COMP1 filter frequency division register (COMP1_FILP)

Address offset : 0x18

Reset value : 0x0000 0000

31–16
Reserved

15–0
CLKPSC[15:0]
rw

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Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low filter sample clock prescale. System clock divider = CLK_PRE_CYCLE + 1, e.g. 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle …

19.7.9 COMP2 control register (COMP2_CTRL)

Address offset : 0x20

Reset value : 0x0000 0000

31:20	19	18:16
Reserved	OUT	BLKING[2:0]
	r	rw

15:14	13	12:9	8:5	4	3:1	0
HYST[1:0]	POL	OUTTRG[3:0]	INPSEL[3:0]	Reserved	INMSEL[2:0]	EN
rw	rw	rw	rw		rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
19	OUT	This read-only bit is a copy of comparator 2 output state. 0: Output is low (non-inverting input below inverting input). 1: Output is high (non-inverting input above inverting input).
18：16	BLKING[2:0]	These bits select which Timer output controls the comparator 2 output blanking. 000: No blanking 001: TIM1 OC5 selected as blanking source 010: TIM8 OC5 selected as blanking source Other configurations: reserved
15:14	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis 01: Low hysteresis 10: Medium hysteresis 11: High hysteresis
13	POL	This bit is used to invert the comparator 2 output. 0: Output is not inverted 1: Output is inverted
12:9	OUTTRG[3:0]	These bits select which Timer input must be connected with the comparator 2 output. 0000：Reserved.； 0001：TIM1_BKIN； 0010：TIM1_OCrefclear；

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Bit field	Name	Description
		0011：TIM1_IC1； 0100：TIM2_OCrefclear； 0101：TIM3_OCrefclear； 0110：TIM4_IC1； 0111：TIM4_OCrefclear； 1000：TIM5_IC1； 1001：TIM8_IC1； 1010：TIM8_OCrefclear； 1011：TIM9_IC1； 1100：TIM9_OCrefclear； 1101：TIM8_BKIN； 1110：TIM1_BKIN + TIM8_BKIN； 1111：LPTIM_ETR。
8:5	INPSEL[3:0]	Comparator 2 non-inverting input selection. 0000 to 0111：floating； 1000：PA1(window mode)/DAC1/PA4(window mode && COMP1_CTRL1.INPDAC=1); 1001：PA3； 1010：PA6； 1011：PA7； 1100：PA11； 1101：PA15； 1110：PB7； 1111：PD7。
4	Reserved	Reserved, the reset value must be maintained
3:1	INMSEL[2:0]	These bits allows to select the source connected to the inverting input of the comparator 2. 000：floating； 001：PA2； 010：PA5； 011：PA6； 100：PB3； 101：PD6； 110：DAC1/PA4； 111：VREF_VC2。
0	EN	This bit switches COMP2 ON/OFF. 0: Comparator disabled 1: Comparator enabled

19.7.10 COMP2 filter register (COMP2_FILC)

Address offset : 0x24

Reset value : 0x0000 0000

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31	16
Reserved	

15-11	10-6	5-1	0
Reserved	SAMPW[4:0]	THRESH[4:0]	FILEN
	rw	rw	rw

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable. 0: Disable 1: Enable

19.7.11 COMP2 filter frequency division register (COMP2_FILP)

Address offset : 0x28

Reset value : 0x0000 0000

31	16
Reserved	

15	0
CLKPSC[15:0]	
rw	

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low filter sample clock prescale. System clock divider = CLK_PRE_CYCLE + 1, e.g. 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle …

19.7.12 COMP2 output select register (COMP2_OSEL)

Address offset : 0x2C

Reset value : 0x0000 0000

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31															16
Reserved															

15														1	0
Reserved															CMP2XO
															rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	CMP2XO	Bit select to choose COPM2 output or the XOR output(comparison of COMP1&2) outputs 0: COMP2 Output 1: XOR(comparison) output between results of COMP1 and COMP2

19.7.13 COMP reference voltage register (COMP_VREFSCL)

Address offset : 0x30

Reset value : 0x0000 0000

15	14	13					8	7	6					1	0
Reserved		VV2TRM[5:0]						VV2EN	VV1TRM[5:0]						VV1EN
		rw						rw	rw						rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	VV2TRM [5:0]	VREF2 (DAC2)voltage scaler trim value.
7	VV2EN	VREF2(DAC2) voltage scaler: 0: disable; 1: enable.
6:1	VV1TRM [5:0]	VREF1 (DAC1)voltage scaler trim value.
0	VV1EN	VREF1(DAC1) voltage scaler: 0: disable; 1: enable.

19.7.14 COMP test register(COMP_TEST)

Address offset : 0x34

Reset value : 0x0000 0000

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15 … 1	0
Reserved	EN
	rw

Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	EN	Comparator test enable: 0: disable 1: enable

19.7.15 COMP interrupt status register (COMP_INTSTS)

Address offset : 0x38

Reset value : 0x0000 0000

15 … 2	1	0
Reserved	CMP2IS	CMP1IS
	rc_w0	rc_w0

Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained
1	COMP2IS	This bit indicate the interrupt status of COMP2,write 0 to clear.
0	COMP1IS	This bit indicate the interrupt status of COMP1,write 0 to clear.

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20 Operational Amplifier (OPAMP)

The OPAMP module can be flexibly configured, suitable for applications such as independent op amp mode and follower mode. OPAMP has an input range of 0V to VDDA and an output range of 0.15V to VDDA-0.15V.

20.1 Main features

- Two independently configured operational amps
- Support track-to-track input, input range is 0 to VDDA, output range is 0.15 to VDDA-0.15 programmable gain
- The OPAMP can be configured as an instrument amplifier through an external resistor connection
- The following modes can be configured
  - General Purpose OPAMP
  - Voltage follower
  - In-phase input PGA
  - Cascade in-phase PGA
  - Differential op amps of two op amps
- Internal resistance feedback network configurable, 1% accuracy
- Programmable gain Settings are 2X, 4X, 8X, 16X, 32X times
- As low as +/-1mV(typical value) offset voltage
- Gain bandwidth: 4MHz
- Supports TIM1_CC6 to automatically switch OPAMP1 and OPAMP2 PIN input
- Independent write protection is supported

20.1.1 OPAMP function description

Two OPAMP can be configured for various PGA modes through register selection, and can also be configured for the user to use the OPAMP function of external components.The output of OPAMP can be used as the channel input to the ADC. The two OPAMP outputs are connected to the analog channel of the ADC as follows.

The output of OPAMP1 is connected to the analog input channel 3 of the ADC

The output of OPAMP2 is connected to the analog input channel 7 of the ADC

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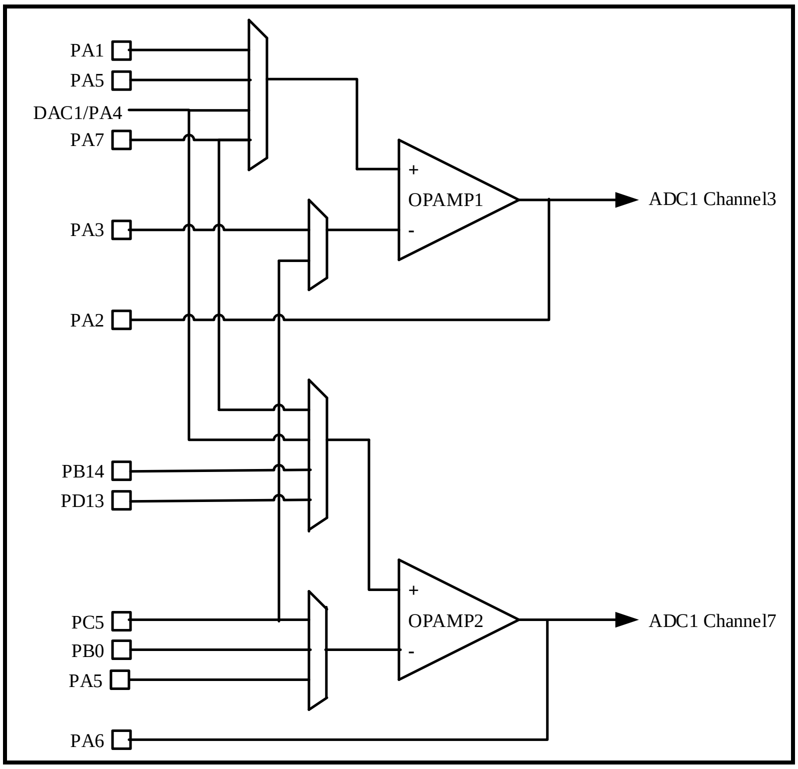
Figure 20-1 Block diagram of OPAMP1 and OPAMP2 connection diagram



20.2 OPAMP working mode

20.2.1 OPAMP independent op amp mode

The amplification factor of the independent op amp mode is determined by the connected resistance and capacitance. When OPAMP_CS.MOD is set to 2'b00 or 2'b01, it is the op amp function, OPAMPx_CS.VPSSEL or OPAMPx_CS.VPSEL selects the positive input, and OPAMPx_CS.VMSSEL or OPAMPx_CS.VMSEL selects the negative input. Use an external resistor to form a closed-loop amplification system.

Two completely independent OPAMPs. At this time, the gain is determined by the external resistor network. It can also be cascaded as required to form the required amplification gain. As shown in the figure below, the positive terminal, negative terminal and output terminal of the OPAMP are connected to the external port. , the amplification factor is determined by the external RC network.

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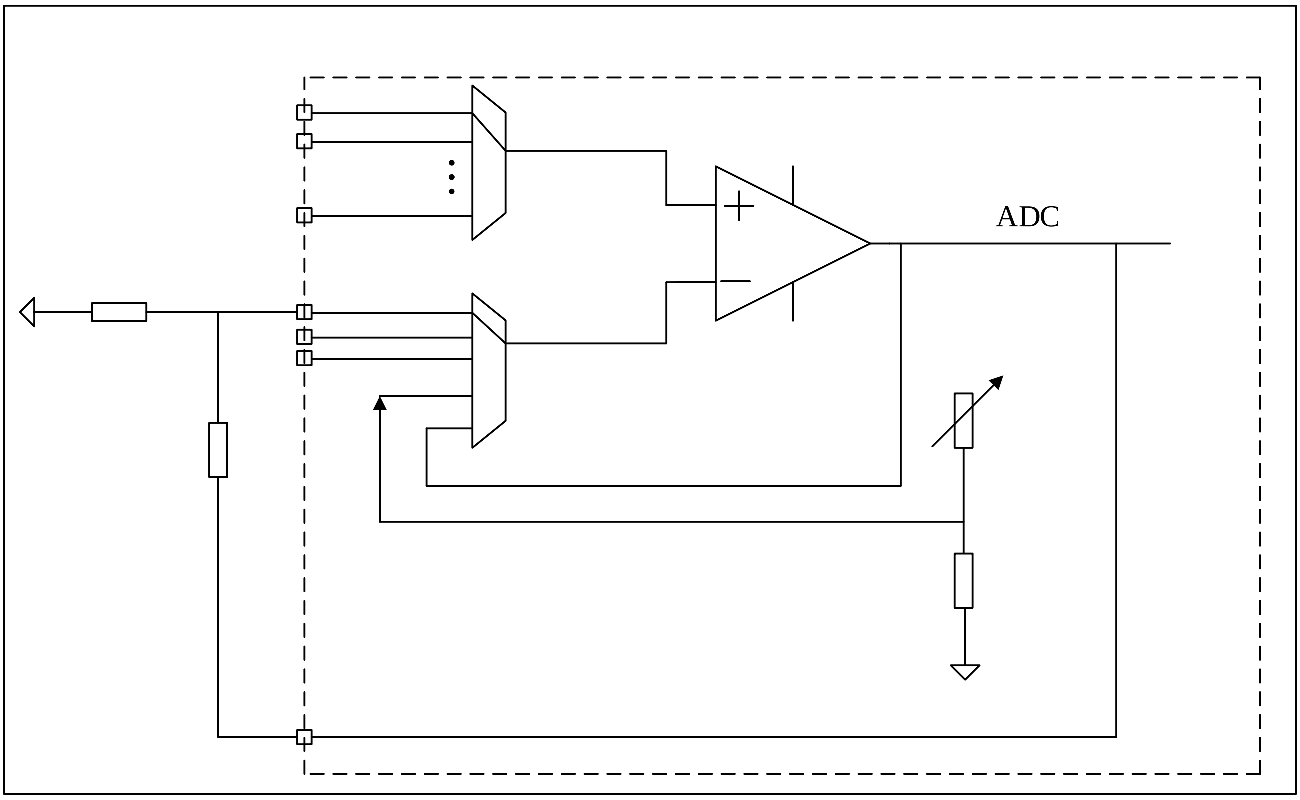
Figure 20-2 OPAMP independent op amp mode



20.2.2 OPAMP follow mode

In follow mode, the voltage is directly follow. The VMSEL terminal must be configured to connected to the OPAMP output port.

OPAMPx_CS. MOD = 2b’11 is the internal follow function, OPAMPx_CS. VPSSEL or OPAMPx_CS. VPSEL selects the positive end input, OPAMPx_CS. VMSSEL or OPAMPx_CS. VMSEL is connected to the output port from the chip interior.

A VM pin that is not occupied can be used as another GPIO.

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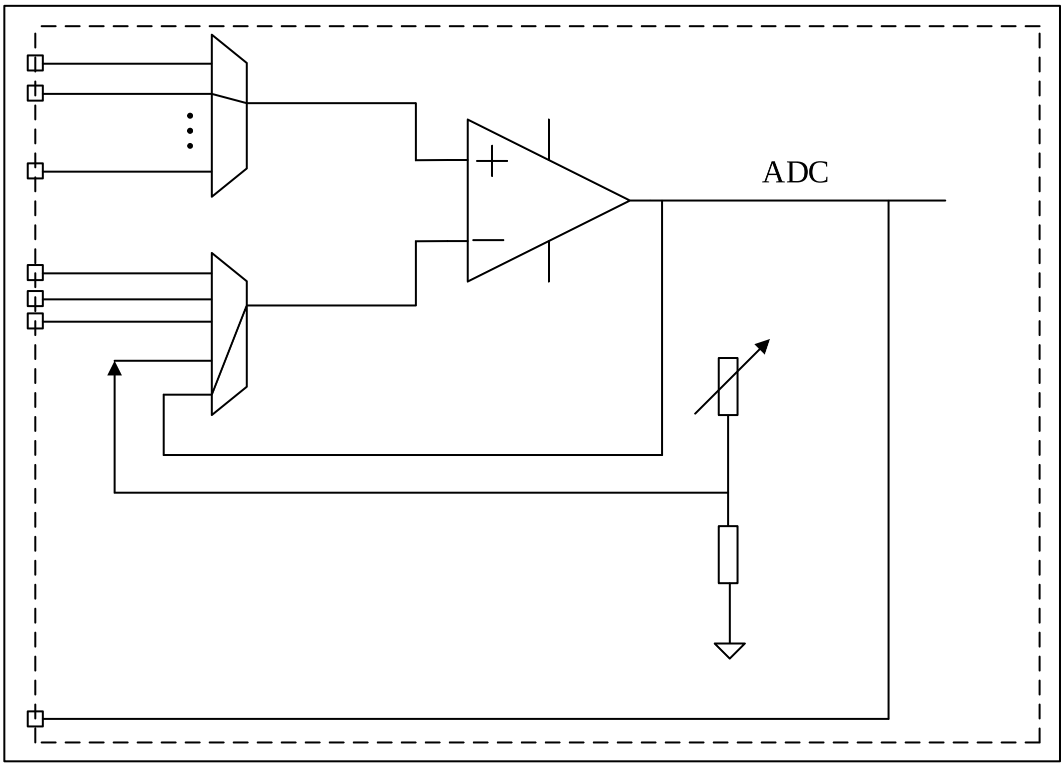
Figure 20-3 Follow mode



20.2.3 OPAMP internal gain (PGA) mode

The internal amplification mode, amplifies the input voltage through a built-in resistor feedback network.

OPAMPx_CS. MOD = 2b'10 is a PGA function that supports 2/4/8/16/32 magnification. OPAMPx_CS. VMSSEL or OPAMPx_CS. VMSEL pins must be set to float.OPAMPx_CS. VPSSEL or OPAMPx_CS. VPSEL select positive input.The positive input can be connected to an external pin, which can be an output port for another OPAMP or a resistive network.Set OPAMPx_CS. PGAGAN to gain selection.The output of an OPAMP can be input to another OPAMP or a resistive network.

OPAMP's VM input pin can be used as a normal GPIO.

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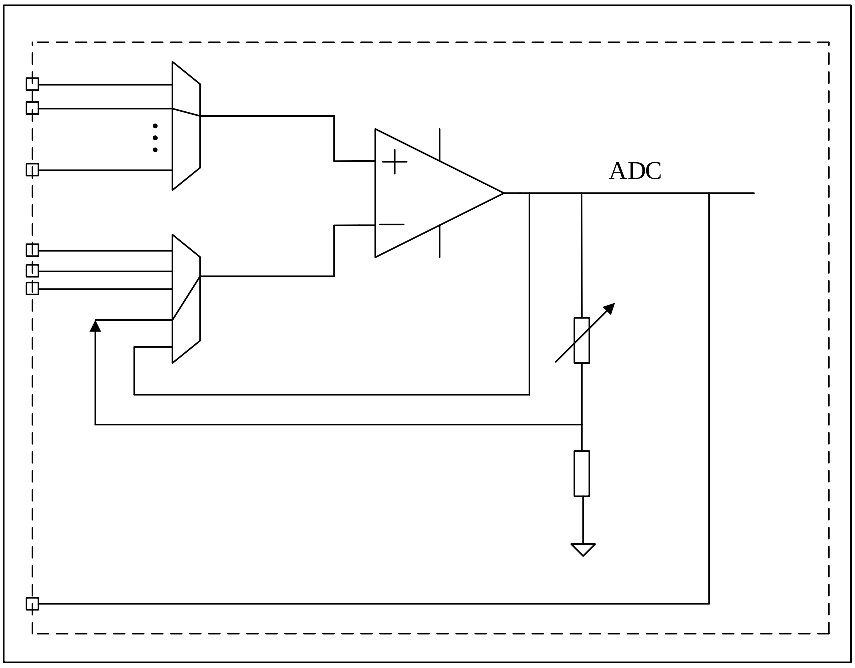
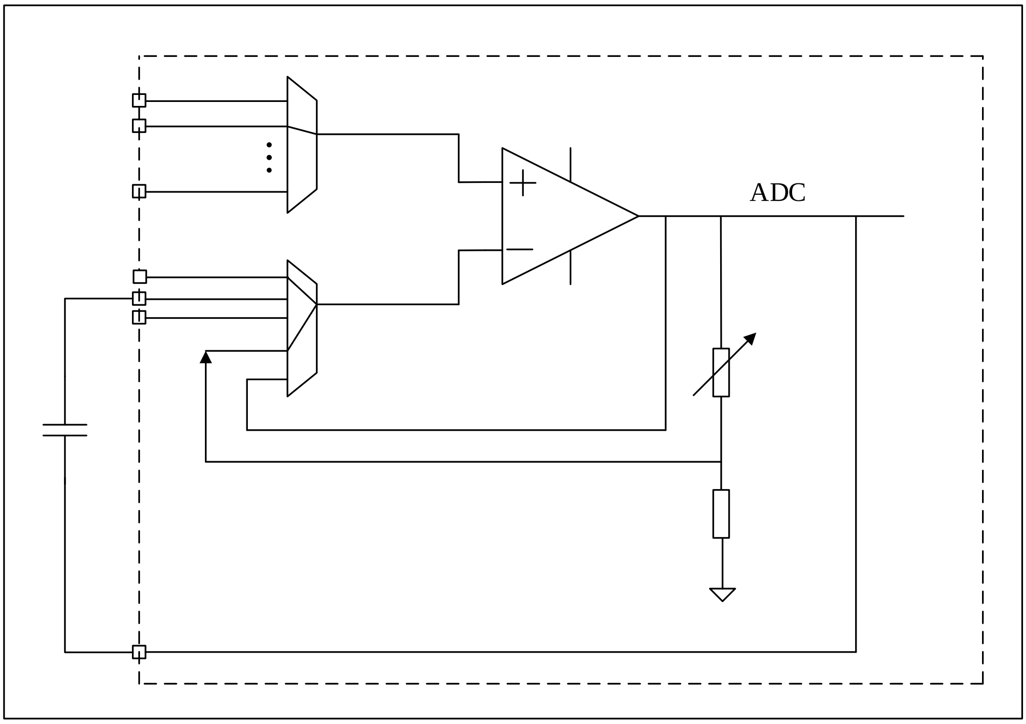
Figure 20-4 Internal gain mode



20.2.4 OPAMP with filtered internal gain mode

In this mode, the amplification voltage is adjustable, supports 2/4/8/16/32, and the OPAMPx_CS.VPSSEL or OPAMAPx_CS.VPSEL is set to be connected to the external pin, and the negative of OPAMP can be connected to components such as capacitors.

Figure 20-5 Internal gain mode with filtering



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20.2.5 OPAMP calibration

The chip has been calibrated before delivery. Users can calibrate the chip again according to the actual environment.

20.2.6 OPAMP Independent write protection

By configuring the OPAMP_LOCK register, the write protection of OPAMP can be set independently.After the write protection is set, the software cannot write to the corresponding OPAMP register. Only after the chip is reset, the write protection can be cancelled.

20.2.7 OPAMP TIMER controls the switching mode

In some applications, the input switching of the OPAMP can be performed through TIMx_CC6.TIM1_CC6 controls the input switching between OPAMP1 and OPAMP2. OPAMP2 can also accept the control input switching between TIM8_CC6.

When TIM1_CC6 is high, OPAMP1 and OPAMP2 select the port configured by VPSSEL/VMSSEL as input, otherwise use VPSEL/VMSEL. When TIM8_CC6 is high, OPAMP2 selects the port configured by VPSSEL/VMSSEL as input, otherwise VPSEL/VMSEL is used.

Set OPAMPx_CS.TCMEN to 1 to enable the automatic switchover input function. The process for configuring the automatic switchover is as follows:

- Enable automatic switching function OPAMPx_CS.TCMEN(2 OPAMP independent control)
- Configure OPAMP2_CS.TIMSRCSEL select TIM1_CC6 or TIM8_CC6
- Configured two conversion MUX configuration (VPSEL,VMSEL, VPSSEL, VMSSEL)
- Start OPAMP and TIM

20.3 OPAMP register

20.3.1 OPAMP register overview

Table 20-1 OPAMP register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	OPAMP_CS1	Reserved										VPSSEL[2:0]			VMSSEL[1:0]		TCMEN	RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL[2:0]			VMSEL[1:0]		PGAGAN[2:0]			MOD[1:0]		EN
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	OPAMP_CS2	Reserved							TIMSRCSEL	Reserved		VPSSEL[2:0]			VMSSEL[1:0]		TCMEN	RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL[2:0]			VMSEL[1:0]		PGAGAN[2:0]			MOD[1:0]		EN
	Reset Value								0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
020h	OPAMP_LOCK	Reserved																														OPAMP2LK	OPAMP1LK
	Reset Value																															0	0

20.3.2 OPAMP Control Status Register (OPAMP1_CS)

Offset address: 0x00

Reset value: 0x0000 0000

31:22	21:19	18:17	16
Reserved	VPSSEL	VMSSEL	TCMEN
	rw	rw	rw

15	14	13	12	11	10:8	7:6	5:3	2:1	0
RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL	VMSEL	PGAGAN	MOD	EN
rw	r	rw		rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21:19	VPSSEL[2:0]	OPAMP non-inverted input secondary selection 000: VP0 (PA1); 001: VP1 (PA5); 010: VP2 (PA4); 011: VP3 (PA7); Others: VP4(NC).
18:17	VMSSEL[1:0]	OPAMP inverted input secondary selection 00: VM0 (PA3); 01: VM1 (PC5); 10: VM2 (NC); 11: VM float (for internal PGA(no filter) mode and follow mode).
16	TCMEN	The Timer Controlled Mux mode is enabled. This bit is set or cleared by the software to control the automatic switching of primary and secondary inputs (VPSEL,VMSEL and VPSSEL,VMSSEL). TIM1_CC6 Automatically switches between OPAMP1 and OPAMP2. 0: the automatic switchover is disabled. 1: Automatic switchover is allowed.
15	RANGE	OPAMP Operational Amplifier Power supply range. 0: low voltage range (VDDA < 2.4V); 1: high voltage range.
14	CALOUT	OPAMP Operation amplifier Calibration Output When this signal switches, the offset during calibration mode is calibrated.
13	TSTREF	Reserved, the reset value must be maintained.

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Bit field	Name	Description
12	Reserved	Reserved, the reset value must be maintained.
11	CALON	Calibration mode enabled 0: Normal mode; 1: Calibration mode.
10:8	VPSEL[2:0]	OPAMP non-inverted input selection 000: VP0 (PA1); 001: VP1 (PA5); 010: VP2 (PA4); 011: VP3 (PA7); Others: VP4(NC).
7:6	VMSEL[1:0]	OPAMP inverted input selection 00: VM0 (PA3); 01: VM1 (PC5); 10: VM2 (NC); 11: VM float (for internal PGA(no filter) mode and follow mode).
5:3	PGAGAN[2:0]	Operational Amplifier Programmable amplifier Gain Value 000: internal PGA gain 2; 001: Internal PGA gain 4; 010: Internal PGA gain 8; 011: Internal PGA gain 16; 100: internal PGA gain 32; Others: Internal PGA gain 2.
2:1	MOD[1:0]	Operational Amplifier PGA Mode 0x: external amplification mode; 10: Enable internal PGA. 11: Internal follow mode.
0	EN	Operational amplifier Enable 0: disable; 1: enable.

20.3.3 OPAMP Control Status Register (OPAMP2_CS)

Offset address: 0x10

Reset value: 0x0000 0000

31-25	24	23-22	21-19	18-17	16
Reserved	TIM SRCSEL	Reserved	VPSSEL	VMSSEL	TCMEN
	rw		rw	rw	rw

15	14	13	12	11	10-8	7-6	5-3	2-1	0
RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL	VMSEL	PGAGAN	MOD	EN
rw	r	rw		rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24	TIMSRCSEL	Primary/secondary input port switch clock source selection 0: TIM1_CC6; 1: TIM8_CC6.
23:22	Reserved	Reserved, the reset value must be maintained
21:19	VPSSEL[2:0]	OPAMP non-inverted input secondary selection 000: VP0 (PA7); 001: VP1 (PA4); 010: VP2 (PB14); 011: VP3 (PD13); Others :(NC).
18:17	VMSSEL[1:0]	OPAMP inverted input secondary selection 00: VM0 (PC5); 01: VM1 (PB0); 10: VM2 (PA5); 11: VM float (for internal PGA(no filter) mode and follow mode).
16	TCMEN	The Timer Controlled Mux mode is enabled. This bit is set or cleared by the software to control the automatic switching of primary and secondary inputs (VPSEL,VMSEL and VPSSEL,VMSSEL). TIM1_CC6 Automatically switches between OPAMP1 and OPAMP2. 0: the automatic switchover is disabled. 1: Automatic switchover is allowed.
15	RANGE	OPAMP Operational Amplifier Power supply range. 0: low voltage range (VDDA < 2.4V); 1: high voltage range.
14	CALOUT	OPAMP Operation amplifier Calibration Output When this signal switches, the offset during calibration mode is calibrated.
13	TSTREF	Reserved, the reset value must be maintained.
12	Reserved	Reserved, the reset value must be maintained.
11	CALON	Calibration Mode Enabled 0: normal mode. 1: calibration mode.
10:8	VPSEL[2:0]	OPAMP non-inverted input selection 000: VP0 (PA7); 001: VP1 (PA4); 010: VP2 (PB14); 011: VP3 (PD13); Others :(NC).
7:6	VMSEL[1:0]	OPAMP inverted input selection 00: VM0 (PC5); 01: VM1 (PB0);

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Bit field	Name	Description
		10: VM2 (PA5); 11: VM float (for internal PGA (no filter) mode and follow mode).
5:3	PGAGAN[2:0]	Operational Amplifier Programmable amplifier Gain Value 000: internal PGA gain 2; 001: Internal PGA gain 4; 010: Internal PGA gain 8; 011: Internal PGA gain 16; 100: internal PGA gain 32; Others: Internal PGA gain 2.
2:1	MOD[1:0]	Operational Amplifier PGA Mode 0x: external amplification mode; 10: Enable internal PGA. 11: Internal follow mode.
0	EN	Operational amplifier Enable 0: disability; 1: enable.

20.3.4 OPAMP Lock register (OPAMP_LOCK)

Offset address: 0x20

Reset value: 0x0000 0000

31–16
Reserved

15–2	1	0
Reserved	OPAMP 2LK	OPAMP 1LK
	rw	rw

Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained
1	OPAMP2LK	OPAMP2 Lock (OPAMP2 lock bit) After the reset, this bit can be written only once 0: OPAMP2 register can read and write; 1: The OPAMP2 register is read-only.
0	OPAMP1LK	With OPAMP2LK.

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21 Low Power Rotation Counter (LPRCNT)

21.1 Introduction

LPRCNT (Low-Power Rotation Counter) is a functional module that can count the number of rotations of a metal object rotating in a circle in low power modes (SLEEP, LP RUN, LP SLEEP and STOP2). The module integrates a sensor interface and a digital state decoding module, which determines the position of the rotating object by detecting the attenuation change of the external LC damping oscillation.LPRCNT has two modes: calibration mode and normal operation. The calibration mode is used to calibrate and adjust the channel parameters. The normal mode is the operating mode of the module system. This function can be applied to flow detection and measurement.

21.2 Main features

- Support 3 independent LC sensor access, each sensor can be individually configured with parameters
- Programmable dynamic adaptive sampling frequency (1Hz~2KHz) to obtain lower power consumption
- Programmabl metering circle overflow interrupt
- Support automatic wake-up in low power mode
- Various working modes
  - Calibration mode (for user parameter adjustment)
  - Normal working mode, automatic detection and counting
- Programmable excitation time, discharge time, and damped oscillation time
- Sensor falling off alarm
- Support cumulative error correction

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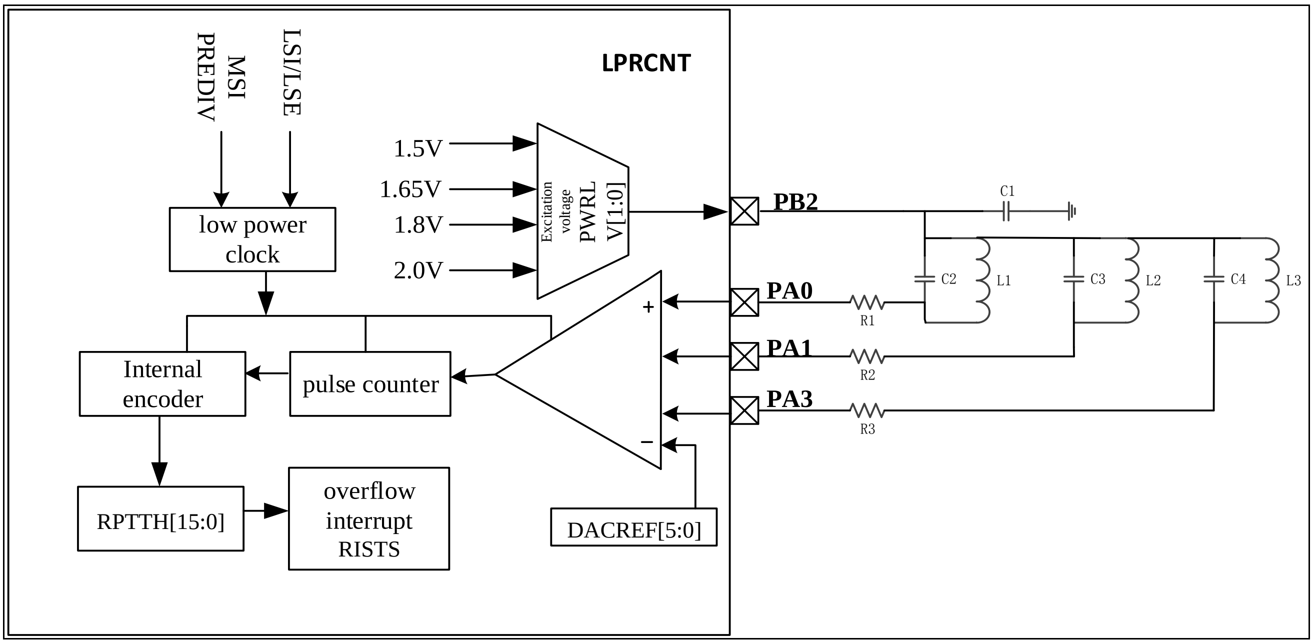
21.3 Functional description

21.3.1 LPRCNT diagram

Figure 21-1 LPRCNT block diagram



LPRCNT is a module that can automatically monitor external circular rotating objects with little or no MCU intervention. It integrates a low-power comparator inside. It is used to detect the external channel sensor signal, and can control the DAC to accurately output the voltage you want. It is recommended to use 1.65V to charge C1. There are also pulse counters and internal encoders inside the LPRCNT. The pulse counter is used to count the square wave number of the signal. The internal encoder can identify 4 kinds of state machines and count the square wave circles. The entire module works with extremely low power consumption.

21.3.2 Introduction to the principle of damped oscillation

The basic principle of the LPRCNT module is to detect the difference in LC oscillation attenuation in different environments to distinguish the location of the sensor. The following figure is a typical LC damping oscillation circuit. In this circuit, by adjusting the switch K, a damped oscillation waveform can be generated on the LC circuit. Charge the capacitor C through K. After it is fully charged, connect K to the inductor L. The electricity of the capacitor will be discharged through L, and the discharged power will charge the capacitor C. In an ideal environment, an undamaged oscillating waveform will be generated, but because both the inductor L and the capacitor C have impedances, as well as the influence of the actual environment, the energy will be gradually consumed, so in the actual situation, a gradually attenuated sine wave output will be generated. As shown below:

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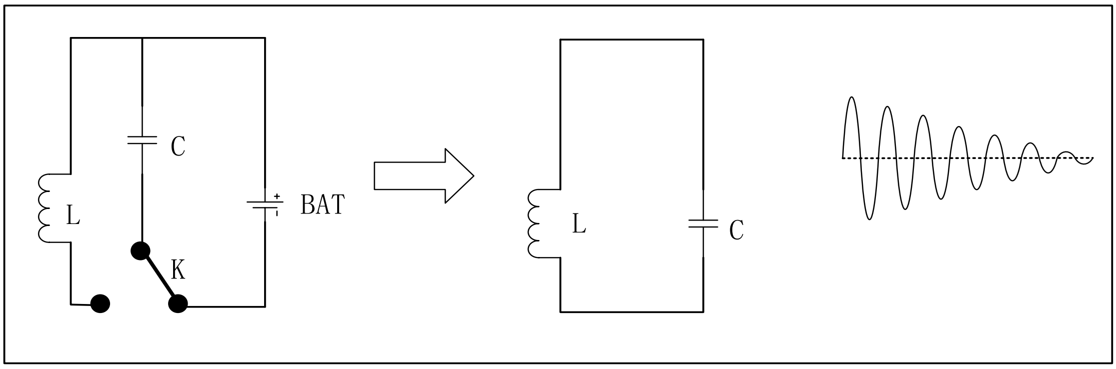
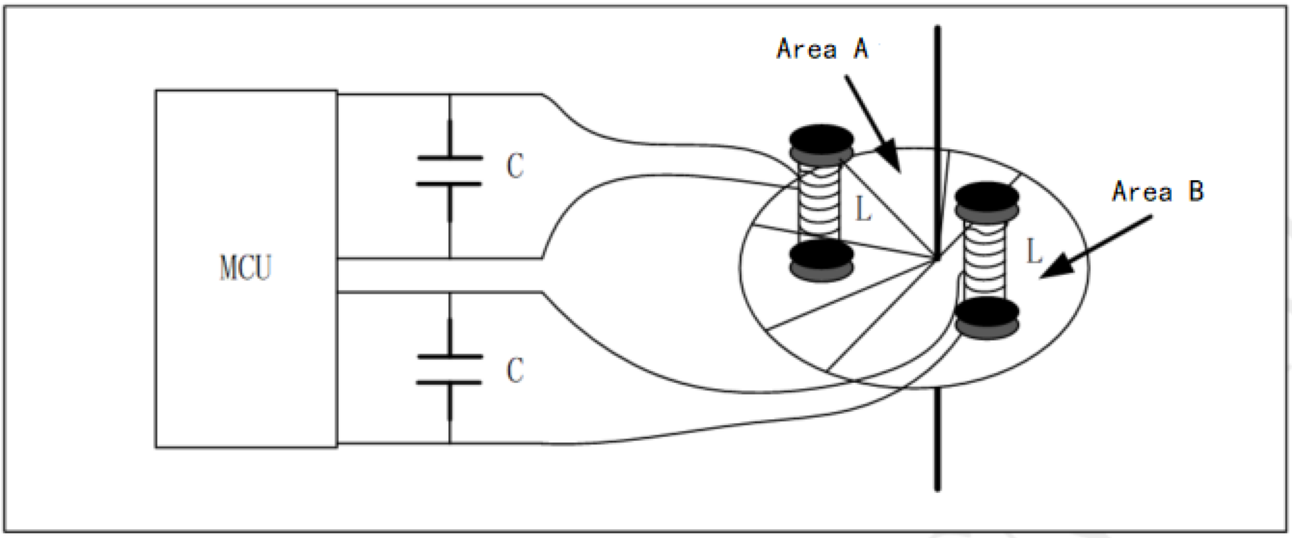


Using this principle, LPRCNT realizes rotating object counting by detecting the sine wave decay process. In the circuit on the right part of the figure below, the disc represents the dial rotor of the rotating object, the slashed area (area A) represents the metal dial area, the white area (area B) represents the non-metal dial area, and L is the fixed inductive coil. After charging the LC circuit, the MCU can obtain the sine wave in the LC oscillation circuit by detecting the voltage across the fixed capacitor C. When the inductance coil is in the metal area, an inductive eddy current will be formed, resulting in greater power consumption and faster attenuation of the sine wave;When the inductor coil is in the non-metallic area, there is basically no eddy current, and the decay speed of the sine wave is relatively slow. Detecting the decay speed of the sine wave through the MCU can accurately identify which area the dial rotor is in, and then judge the dial position and the number of turns, so as to achieve the purpose of counting rotating objects.



21.3.3 State machine judgment and rotation position

The LPRCN module uses two sensors to implement state machine detection. During the rotation of the dial, the close position of the metal will increase the attenuation of the damped oscillation waveform. If the non-metal is regarded as 0, then the metal area is 1. As shown in Figure 21-2 below, the state machine composed of sensors is "10".

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Figure 21-2 Rotating object damping oscillation detection principle

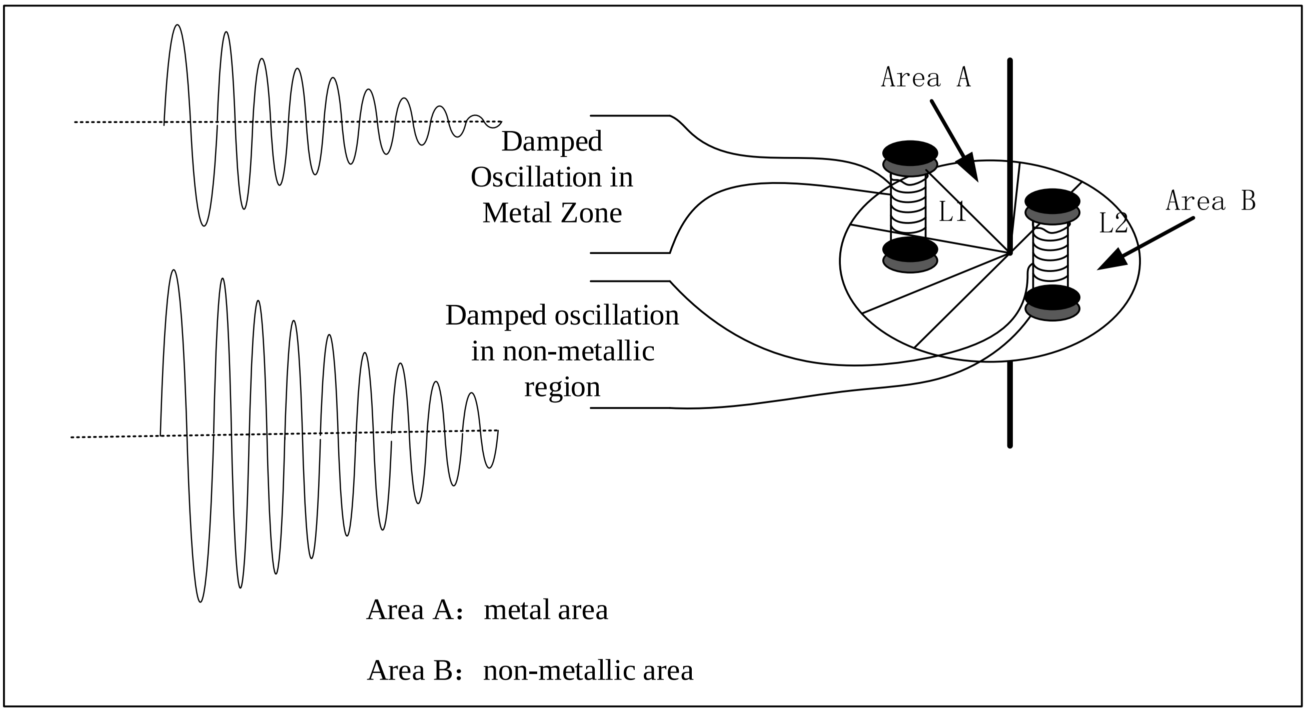

Table 21-1 Sensor damped oscillation state machine comparison table

Sensor number	Turntable position	Corresponding state
Sensor NO.1	metal area	1
Sensor NO.2	non-metallic area	0

Through analysis, it is obtained that the state of sensor 1/sensor 2 is A(0/1)->B(0/0)->C(1/0)->D(1/1)->A(0/1)->B(0/0)->C(1/0)... cyclically appear, we obtain the corresponding state by detecting the sine wave attenuation trend of sensor 1/sensor 2, and then through different combined states, and then obtain the position of the dial and calculate the rotational speed. Therefore, the process of the turntable traversing ABCD represents one rotation of the dial.

21.3.4 Calibration mode and normal mode

When the LPRCNT module is used for the first time, it needs to switch to the calibration mode for parameter adjustment. Since each channel of LC damping oscillation frequency is different, it is recommended to set parameters separately for each channel. It includes the damping oscillation time control parameters of each sensor and the detection threshold setting.

The LPRCNT needs to be switched to the LPRCNT working mode after the above calibration. In this mode, the power consumption is extremely low, and the internal decoder will continuously monitor the peripheral LC signal. When the set number of turns is reached, an overflow interrupt will be generated, and the MCU will be woken up to exit the STOP2 mode.

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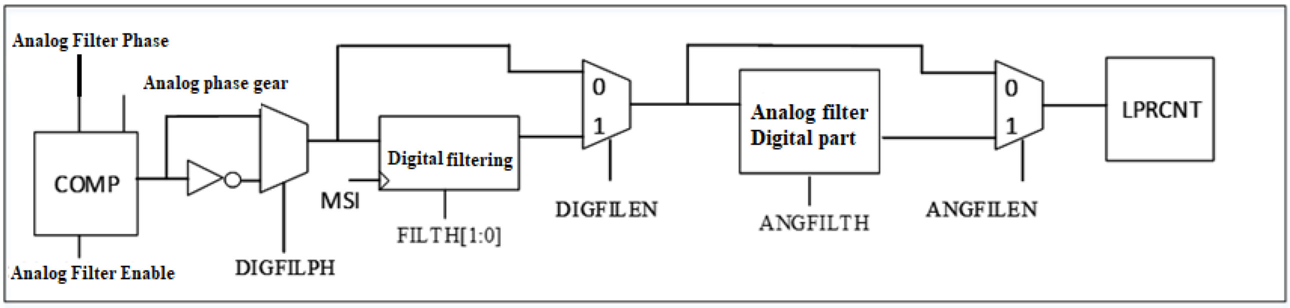
21.3.5 LPRCNT comparator filtering

The signal of the LPRCNT module sensor is input through the comparator, and the corresponding square wave is obtained after being processed by the comparator. Due to the existence of voltage disturbance, channel mutual disturbance, etc, some square waves are not the number of square waves we need to damp vibration, so a filter is required to filter out these disturbing square waves.

Figure 21-3 LPRCNT module comparator filtering block diagram



The comparator of LPRCNT integrates digital and analog filters. It is recommended to use analog filters by default. Generally speaking, analog filters have better filtering effect. In use, you only need to open the LPRCNT_CAL3.ANGFILEN bit.

Alternatively, digital filters can be used as required. Digital filters have phase and gating settings. Bit LPRCNT_CAL3.DIGFILPH sets the filtering of positive and negative glitches. Bits LPRCNT_CAL3. FILTH[1:0] can set the filter gate limit value.

Note: When using the comparator digital filter and analog filter, the comparator controller filter can no longer be turned on.

21.4 LPRCNT operation instructions

21.4.1 Channel configuration

As shown in LPRCNT block **diagram**,the excitation voltage of the external sensor circuit can be provided by the internal DAC, and the ETX pin (PB2) directly charges the capacitor C1. It is the source of the entire LC excitation power, and the corresponding voltage output can be configured through LPRCNT_CTRL. PWRLVL [1:0]. There are four gears: 1.5V, 1.65V, 1.8V and 2.0V, and 1.65V is recommended. CH0, CH1, CH2 (PA0, PA1, PA2) are three-way sensor input interfaces.

21.4.1.1 LPRCNT clock

The LPRCNT module has three clock sources, namely MSI, LSX (LSI or LSE). MSI mainly provides the time reference for the excitation time, discharge time and comparator working time in the LPRCNT module. There are 1, 2, 4, and 8 frequency division factors, which can be configured through the LPRCNT_CTRL.CLKDIV bit. LSX mainly provides the time base for sensor scanning.

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21.4.1.2 LPRCNT scaning frequency

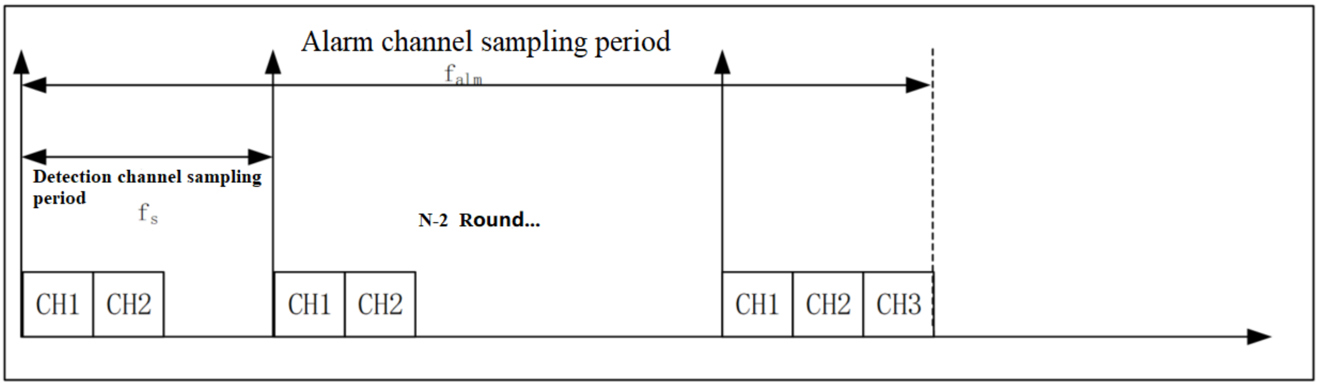
The sampling frequency of the LC sensor supports the adaptive mode and the fixed sampling rate mode. When the user configures different values for the low-speed sampling rate and the high-speed sampling rate, the system will change the sampling rate within a certain period of time (the sampling time can be set through the registers LPRCNT_SCTRL and LPRCNT_CTRL. ALMPRD [1: 0] to configure) If the rotation of the rotating object is not detected, it will automatically switch to the low-speed sampling mode. When the system detects the sudden rotation of the rotating object, it will automatically switch back to the high-speed sampling to achieve adaptive sampling mode, which can minimize system power consumption. If you need to use the fixed sample rate mode, you only need to configure the low-speed and high-speed sampling to the same rate. The specific sampling rate configuration can be adjusted according to the actual application requirements to achieve accurate measurement and reduce power consumption as much as possible. The specific configuration is as follows:

Mode	Sampling Frequency	Register Settings	Entry Conditions
low speed	Detection channel f_L	LPRCNT_SCTRL.LSPRD[9:0]	The rotating object remains inactive for the duration of LPRCNT_SCTRL.SWT[7:0]
high speed	Detection channel f_H	LPRCNT_SCTRL.HSPRD[7:0]	A rotating object is in a rotating state
low speed	Alarm channel f_L	LPRCNT_CTRL.ALMPRD [1:0]	The rotating object remains inactive for the duration of LPRCNT_SCTRL.SWT[7:0]
high speed	Alarm channel f_H	LPRCNT_CTRL.ALMPRD [1:0]	A rotating object is in a rotating state

Note:

1. Two of the three-way sensors are used as detection channels for rotating objects, and the sampling frequencies of the detection channels are the same. The other sensor is used as auxiliary detection to monitor illegal operation and alarm. Its period is N times the detection channel period (4, 8, 16, 32).

The three-way sensor adopts a single polling sampling, and only has an initial value after N rounds of sampling. Therefore, when entering the normal working mode, the value of the sensor you read is not the signal value from time to time, but the average value of N times. If you want to see the time signal value, you need to enter the calibration mode.



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21.4.1.3 LPRCNT module damped oscillation timing

The module needs to generate stable damped oscillation under specific timing. It mainly includes excitation time, discharge time and damping oscillation time (as shown in Figure 21-4). The LPRCNT module needs to maintain extremely low power consumption, so each stage of the damped oscillation needs to be completed as quickly as possible. At the same time, each channel is polling, and only one is working at a time. As shown Figure 21-5, LC_EXT is first turned on, charging the capacitor C1, and disconnecting immediately after the capacitor is fully charged. Then each LC_CHx channel will discharge. After the set discharge time, the LC_CHx channel will switch back to the comparator input analog state, and damped oscillation will occur at this time.

Figure 21-4 LC damped oscillation process

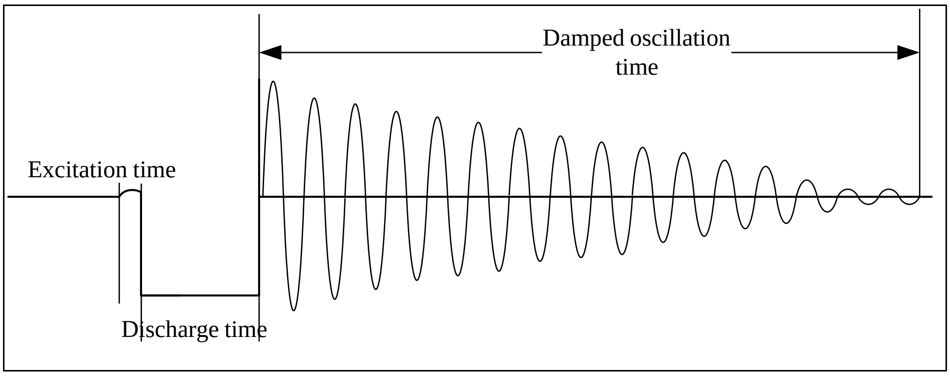
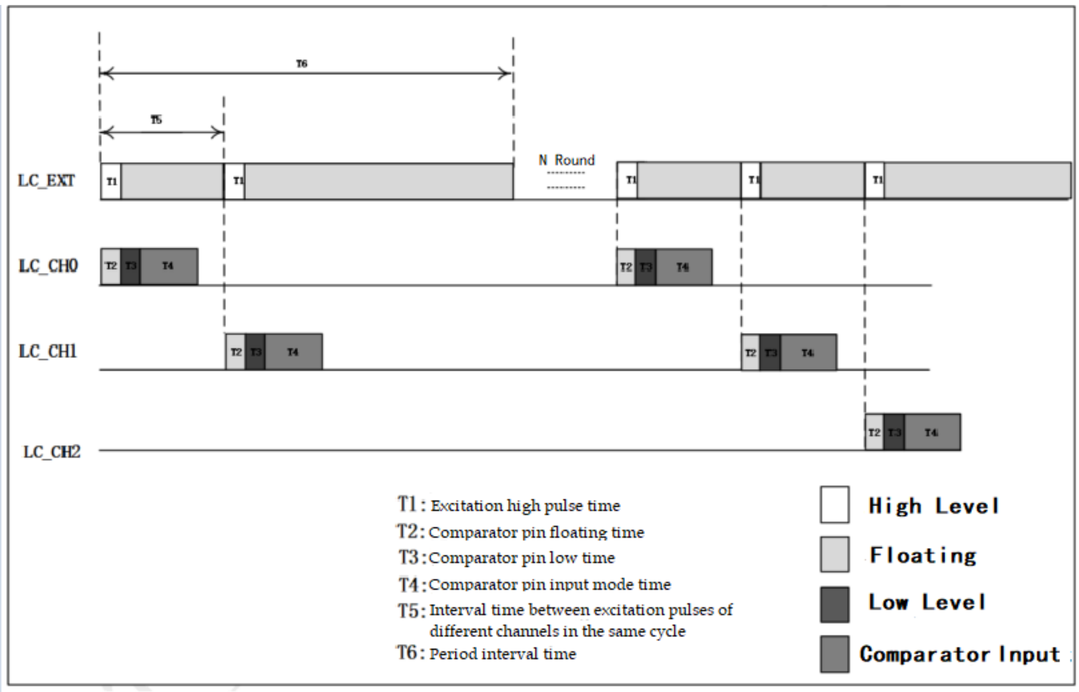


Figure 21-5 Three-way LC working timing diagram



21.4.2 LPRCNT module operation in calibration mode

LPRCNT module for parameter adjustment. Proceed as follows:

■ LPRCNT_SCTRL configures the sampling period of the detection channel, LPRCNT_CTRL.ALMPRD[1:0]

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configures the sampling period of the alarm channel

■ LPRCNT_CTRL. CLKDIV[1:0] set the MSI clock frequency division

■ LPRCNT_CTRL. PWRLVL [1:0] select the corresponding excitation voltage

■ Enter calibration mode by LPRCNT_CTRL. RCNTM =0

■ Set the sampling method in calibration mode through LPRCNT_CTRL. CALM

■ Set the damping oscillation trigger threshold and comparator reference voltage parameters of each channel of LPRCNT (LPRCNT_CHxCFG0)

■ Set the damping oscillation time control parameters of each channel of LPRCNT (LPRCNT_CHxCFG1)

■ Read the CHxCNT in LPRCNT_CAL0, whether the STATEx corresponds correctly (metal and non-metal distinction)

21.4.3 LPRCNT normal working mode operation

After the LPRCNT module is set to the working mode, the entire module will work all the time. When the set number of acquisition turns is reached, the system will automatically wake up the MCU. The entire register configuration is concentrated in LPRCNT_CHx CFG0, LPRCNT_CHx CFG1 and LPRCNT_CTRL, and the settings are as follows:

■ LPRCNT_SCTRL configures the sampling period of the detection channel, and LPRCNT_CTRL.PRD[1:0] configures the sampling period of the alarm channel

■ LPRCNT_CTRL.CLKDIV sets the MSI clock frequency division

■ LPRCNT_CTRL.PWRLV[1:0] select the corresponding excitation voltage

■ Set the damping oscillation trigger threshold and comparator reference voltage parameters of each channel of LPRCNT (LPRCNT_CHxCFG0)

■ Set the damping oscillation time control parameters of each channel of LPRCNT (LPRCNT_CHxCFG1)

■ Choose the number of laps to wake up through the configuration register LPRCNT_CTRL. RPTTH[15:0]

■ LC excitation voltage is selected by configuration register LPRCNT_CTRL.PWRLV[1:0] (1.65V recommended)

■ Set the sensor sampling period by configuring the register LPRCNT_SCTRL

■ Enter normal working mode through configuration register LPRCNT_CTRL. RCNTM=1

NOTE: The LPRCNT revolution counter does not have an auto-reload function and therefore needs to be updated all the time. Fast cutting and slow speed must ensure that more than half a circle does not move.

21.5 LPRCNT registers

21.5.1 LPRCNT register overview

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Table 21-2 LPRCNT register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	LPRCNT_CTRL	Reserved	CALIE	RPTIE	ALMIE	ALMPRD[1:0]		CALM	RCNTM	CMPAUT	PWRLVL[1:0]		CNTDIR	AVGSEL[1:0]		CLKDIV[1:0]		RPTTH[15:0]															
	Reset Value		0	1	1	1	0	1	1	1	0	1	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
004h	LPRCNT_INTSTS	Reserved													CALIF	RPTIF	ALMIF	RPTVAL[15:0]															
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	LPRCNT_SCTRL	Reserved						LSPRD[9:0]										SWT[7:0]								HSPRD[7:0]							
	Reset Value							0	1	0	1	0	0	1	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	1
00Ch	LPRCNT_CH0TH	Reserved										DACREF[5:0]						UNDTH[7:0]								DAMTH[7:0]							
	Reset Value											1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0
010h	LPRCNT_CH0TIM	Reserved								DAMDUR[7:0]								Reserved		DSCDUR[5:0]						Reserved		CHGDUR[5:0]					
	Reset Value									0	1	0	1	0	0	0	0			0	0	0	0	1	1			0	0	0	0	1	0
014h	LPRCNT_CH1TH	Reserved										DACREF[5:0]						UNDTH[7:0]								DAMTH[7:0]							
	Reset Value											1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0
018h	LPRCNT_CH1TIM	Reserved								DAMDUR[7:0]								Reserved		DSCDUR[5:0]						Reserved		CHGDUR[5:0]					
	Reset Value									0	1	0	1	0	0	0	0			0	0	0	0	1	1			0	0	0	0	1	0
01Ch	LPRCNT_CH2TH	Reserved										DACREF[5:0]						UNDTH[7:0]								DAMTH[7:0]							
	Reset Value											1	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0
020h	LPRCNT_CH2TIM	Reserved								DAMDUR[7:0]								Reserved		DSCDUR[5:0]						Reserved		CHGDUR[5:0]					
	Reset Value									0	1	0	1	0	0	0	0			0	0	0	0	1	1			0	0	0	0	1	0
024h	LPRCNT_CMD	Reserved																													CLRRCNT	STOP	START
	Reset Value																														0	0	0
030h	LPRCNT_CAL0	Reserved						CH1STS[1:0]		CH1CNT[7:0]								Reserved						CH0STS[1:0]		CH0CNT[7:0]							
	Reset Value							0	0	0	0	0	0	0	0	0	0							0	0	0	0	0	0	0	0	0	0
034h	LPRCNT_CAL1	Reserved																						CH2STS[1:0]		CH2CNT[7:0]							
	Reset Value																							0	0	0	0	0	0	0	0	0	0
038h	LPRCNT_CAL2	Reserved								RCNTADJ[3:0]				GAP[3:0]				Reserved		CMPSET[5:0]						Reserved		DACSET[5:0]					
	Reset Value									0	0	0	0	0	0	0	1			0	0	1	1	1	1			0	0	1	1	1	1
03Ch	LPRCNT_CAL3	CH2MAP[1:0]		CH1MAP[1:0]		CH0MAP[1:0]		DIGFILEN	FILTH[1:0]		DIGFILPH	ANGFILEN	Reserved					CMPLPEN	CMPINMSEL[2:0]			CMPHYSEL[1:0]		DACCMPALWSON	STATCLRCTRL	PWRDUREN	CMPAUTOMODE	Reserved					
	Reset Value	1	0	0	1	0	0	0	0	1	0	0						1	1	1	0	0	1	0	0	0	0						

21.5.2 LPRCNT control register (LPRCNT_CTRL)

Address offset: 0x00

Reset value: 0x3ba60400

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31	30	29	28	27:26	25	24	23	22:21	20	19:18	17:16
Reserved	CALIE	RPTIE	ALMIE	ALMPRD[1:0]	CALM	RCNTM	CMPAUT	PWRLVL[1:0]	CNTDIR	AVGSEL[1:0]	CLKDIV[1:0]
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15:0
RPTTH[15:0]
rw

Bit field	Name	Description
31	Reserved	Reserved,the reset value must be maintained.
30	CALIE	Calibration mode damped oscillator interrupt enable 0: disable 1: enable
29	RPTIE	Turns overflow interrupt enable 0: disable 1: enable
28	ALMIE	Alarm interrupt enable 0: disable 1: enable
27:26	ALMPRD[1:0]	Alarm sensor period configuration 00: RCNT_SLW_PRD* 4 01: RCNT_SLW_PRD* 8 10: RCNT_SLW_PRD* 16 11: RCNT_SLW_PRD* 32
25	CALM	Work manners in calibration mode 0: single sample 1: continuous sampling
24	RCNTM	LPRCNT mode enable bit 0: calibration mode 1: LPRCNT mode
23	CMPAUT	Comparator auto-stop mode enable 0: disable 1: enable
22:21	PWRLVL[1:0]	Excitation voltage select bits 00: 1.5V 01: 1.65V 10: 1.8V 11: 2.0V
20	CNTDIR	Turntable count direction This bit is used to calibrate the direction of rotation 0: positive direction 1: opposite direction
19:18	AVGSEL[1:0]	How many times to sample and average Automatically calculate the average data of multiple excitations and samples in 1 round of sampling, N is mapped to 2^N, (data smoothing algorithm: bit shift for

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Bit field	Name	Description
		averaging)
17:16	CLKDIV[1:0]	MSI clock divider 00: MSI CLOCK /1 01: MSI CLOCK /2 10: MSI CLOCK /4 11: MSI CLOCK /8
15:0	RPTTH[15:0]	Wake up lap settings When the set value is reached, LPRCNT can automatically wake up the CPU, and then actively report the number of laps

21.5.3 LPRCNT interrupt status register

Address offset: 0x04

Reset value: 0x0000 0000

31–19	18	17	16
Reserved	CALIF	RPTIF	ALMIF
	rc_w1	rc_w1	rc_w1

15–0
RPTVAL[15:0]
r

Bit field	Name	Description
31:19	Reserved	Reserved,the reset value must be maintained.
18	CALIF	Calibration mode damped oscillation interrupt flag bit
17	RPTIF	Numbers of turn overflow interrupt flag
16	ALMIF	Alarm interrupt flag
15:0	RPTVAL[15:0]	LPRCNT voluntarily reported lap value

21.5.4 LPRCNT scan control register(LPRCNT_SCTRL）

Address offset:0x08

Reset value: 0x014d 3c05

31–26	25–16
Reserved	LSPRD[9:0]
	rw

15–8	7–0
SWT[7:0]	HSPRD[7:0]
rw	rw

Bit field	Name	Description
31:26	Reserved	Reserved,the reset value must be maintained.
25:16	LSPRD[9:0]	Low speed mode sensor processing period,unit:T(LSX_CLK)*32,default value:333
15:8	SWT[7:0]	Time from sensor state machine unchanged to switching to low-speed sampling mode,

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Bit field	Name	Description
		unit:T(LSX_CLK)*2048 default value:60
7:0	HSPRD[7:0]	High speed mode sensor sampling period,unit:T(LSX_CLK)*16, default value:5

21.5.5 LPRCNT sensor channel 0 threshold register(LPRCNT_CH0CFG0)

Address offset: 0x0C

Reset value: 0x0021 2C24

31–22	21–16
Reserved	DACREF[5:0]
	rw

15–8	7–0
UNDTH[7:0]	DAMTH[7:0]
rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved,the reset value must be maintained.
21:16	DACREF[5:0]	Comparator internal reference voltage setting,64 gears in total.
15:8	UNDTH[7:0]	Judgment of non-metallic state threshold when damping oscillation
7:0	DAMTH[7:0]	Judgment of metallic state threshold when damping oscillation

21.5.6 LPRCNT sensor channel 0 time control register (LPRCNT_CH0CFG1)

Address offset: 0x10

Reset value: 0x0050 0302

31–24	23–16
Reserved	DAMDUR[7:0]
	rw

15–14	13–8	7–6	5–0
Reserved	DSCDUR[5:0]	Reserved	CHGDUR[5:0]
	rw		rw

Bit field	Name	Description
31:22	Reserved	Reserved,the reset value must be maintained.
23:16	DAMDUR[7:0]	The damped oscillation duration Comparator processing duration, if no auto stop is enabled, it will last until the set time, unit: T(MSI_CLK_DIV)*1, default value: 80 (damping oscillation time)
15:14	Reserved	Reserved,the reset value must be maintained.
13:8	DSCDUR[5:0]	The discharge duration, unit: T(MSI_CLK_DIV)*1, default value:3
7:6	Reserved	Reserved,the reset value must be maintained.
5:0	CHGDUR[5:0]	The charge duration, unit:T(MSI_CLK_DIV)*1,default value:2

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21.5.7 LPRCNT sensor channel 1 threshold register (LPRCNT_CH1CFG0)

Address offset: 0x14

Reset value: 0x0021 2C24

31 … 22	21 … 16
Reserved	DACREF[5:0]
	rw

15 … 8	7 … 0
UNDTH[7:0]	DAMTH[7:0]
rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved,the reset value must be maintained.
21:16	DACREF[5:0]	Comparator internal reference voltage setting,64 gears in total.
15:8	UNDTH[7:0]	Judgment of non-metallic state threshold when damping oscillation
7:0	DAMTH[7:0]	Judgment of metallic state threshold when damping oscillation

21.5.8 LPRCNT sensor channel 1 time control register (LPRCNT_CH1CFG1)

Address offset: 0x18

Reset value: 0x0050 0302

31 … 24	23 … 16
Reserved	DAMDUR[7:0]
	rw

15 … 14	13 … 8	7 … 6	5 … 0
Reserved	DSCDUR[5:0]	Reserved	CHGDUR[5:0]
	rw		rw

Bit field	Name	Description
31:22	Reserved	Reserved,the reset value must be maintained.
23:16	DAMDUR[7:0]	The damped oscillation duration Comparator processing duration, if no auto stop is enabled, it will last until the set time, unit: T(MSI_CLK_DIV)*1, default value: 80 (damping oscillation time)
15:14	Reserved	Reserved,the reset value must be maintained.
13:8	DSCDUR[5:0]	The discharge duration, unit: T(MSI_CLK_DIV)*1, default value:3
7:6	Reserved	Reserved,the reset value must be maintained.
5:0	CHGDUR[5:0]	The charge duration, unit:T(MSI_CLK_DIV)*1,default value:2

21.5.9 LPRCNT sensor channel 2 threshold register (LPRCNT_CH2CFG0)

Address offset: 0x1C

Reset value: 0x0021 2C24

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31 … 22	21 … 16
Reserved	DACREF[5:0]
	rw

15 … 8	7 … 0
UNDTH[7:0]	DAMTH[7:0]
rw	rw

Bit field	Name	Description
31:22	Reserved	The reset value must be maintained.
21:16	DACREF[5:0]	Comparator internal reference voltage setting ,64 gears in total.
15:8	UNDTH[7:0]	Judgment of non-metallic state threshold when damping oscillation
7:0	DAMTH[7:0]	Judgment of metallic state threshold when damping oscillation

21.5.10 LPRCNT sensor channel 2 time control register (LPRCNT_CH2CFG1)

Address offset: 0x20

Reset value: 0x0050 0302

31 … 24	23 … 16
Reserved	DAMDUR[7:0]
	rw

15 14	13 … 8	7 6	5 … 0
Reserved	DSCDUR[5:0]	Reserved	CHGDUR[5:0]
	rw		rw

Bit field	Name	Description
31:22	Reserved	Reserved,the reset value must be maintained.
23:16	DAMDUR[7:0]	The damped oscillation duration Comparator processing duration, if no auto stop is enabled, it will last until the set time, unit: T(MSI_CLK_DIV)*1, default value: 80 (damping oscillation time)
15:14	Reserved	Reserved,the reset value must be maintained.
13:8	DSCDUR[5:0]	The discharge duration, unit: T(MSI_CLK_DIV)*1, default value:3
7:6	Reserved	Reserved,the reset value must be maintained.
5:0	CHGDUR[5:0]	The charge duration, unit:T(MSI_CLK_DIV)*1,default value:2

21.5.11 LPRCNT command register (LPRCNT_CMD)

Address offset: 0x24

Reset value: 0x0000 0000

31 … 16
Reserved

15 … 3	2	1	0
Reserved	CLRCNT	STOP	START
	w	w	rw

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Bit field	Name	Description
31:3	Reserved	Reserved,the reset value must be maintained.
2	CLRCNT	Clear the count value of RCNT
1	STOP	Write 1 to stop LPRCNT, the hardware will automatically clear it after the operation is over.
0	START	Write 1 to start LPRCNT, the hardware will automatically clear it after the operation is over

21.5.12 LPRCNT calibration register 0 (LPRCNT_CAL0)

Address offset: 0x30

Reset value: 0x0000 0000

31:26	25:24	23:16
Reserved	CH1STS[1:0]	CH1CNT[7:0]
	r	r

15:10	9:8	7:0
Reserved	CH0STS[1:0]	CH0CNT[7:0]
	r	r

Bit field	Name	Description
31:26	Reserved	Reserved,the reset value must be maintained.
25:24	CH1STS [1:0]	Sensor channel 1 state 00: non-metallic area 01: intermediate state 10: metal area
23:16	CH1CNT[7:0]	Channel 1 comparator valid square wave count value
15:10	Reserved	Reserved,the reset value must be maintained.
9:8	CH0STS[1:0]	Sensor channel 0 state 00: non-metallic area 01: intermediate state 10: metal area
7:0	CH0CNT[7:0]	Channel 0 comparator valid square wave count value

21.5.13 LPRCNT calibration register 1(LPRCNT_CAL1)

Address offset : 0x34

Reset value: 0x0000 0000

31:16
Reserved

15:10	9:8	7:0
Reserved	CH2STS[1:0]	CH2CNT[7:0]
	r	r

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Bit field	Name	Description
31:26	Reserved	Reserved,the reset value must be maintained.
9:8	CH2STS [1:0]	Sensor channel 2 state 00: non-metallic area 01: intermediate state 10: metal area
7:0	CH2CNT[7:0]	Channel 2 comparator valid square wave count value

21.5.14 LPRCNT calibration register 2(LPRCNT_CAL2）

Address offset : 0x38

Reset value: 0x0301 0F0F

31–26	25	24	23–20	19–16
Reserved	SAMP MODE	Reserved	RCNT ADJ[3:0]	GAP[3:0]
	r		rw	rw

15–14	13–8	7–6	5–0
Reserved	CMPSET[5:0]	Reserved	DACSET[5:0]
	rw		rw

Bit field	Name	Description
31:26	Reserved	Reserved,the reset value must be maintained.
25	SAMPMODE	sample mode 0: High-speed sampling mode 1: Low-speed sampling mode
24	Reserved	Reserved,the reset value must be maintained.
23:20	RCNTADJ [3:0]	Accumulated rotation error adjustment value at low speed, default 0.
19:16	GAP [3:0]	Charge and discharge time gap
15:14	Reserved	Reserved,the reset value must be maintained.
13:8	CMPSET[5:0]	Comparator setup time, turned on before configuration.
7:6	Reserved	Reserved,the reset value must be maintained.
5:0	DACSET[5:0]	DAC excitation voltage setup time

21.5.15 LPRCNT calibration register 3 (LPRCNT_CAL3)

Address offset : 0x3C

Reset value: 0x9088 E400

31–30	29–28	27–26	25	24–23	22	21	20–16
CH2MAP[1:0]	CH1MAP[1:0]	CH0MAP[1:0]	DIG FILEN	FILTH[1:0]	DIG FILPH	ANG FILEN	Reserved
rw	rw	rw	rw	rw	rw	rw	

15	14–12	11–10	9	8	7	6	5–0
CMP LPEN	CMP INMSEL[2:0]	CMP HYSEL[1:0]	DAC CMP ALWSON	STAT CLRCTRL	PWR DUREN	CMP AUTO MODE	Reserved
rw	rw	rw	rw	rw	rw	rw	

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Bit field	Name	Description
31:30	CH2MAP[1:0]	CH2 map to which sensor select 00: map to sensor 0 01: map to sensor 1 10: map to sensor 2
29:28	CH1MAP[1:0]	CH1 map to which sensor select 00: map to sensor 0 01: map to sensor 1 10: map to sensor 2
27:26	CH0MAP[1:0]	CH0 map to which sensor select 00: map to sensor 0 01: map to sensor 1 10: map to sensor 2
25	DIGFILEN	Digital filtering enable 0: disable 1: enable
24:23	FILTH[1:0]	Filter threshold control 00: T/2 01: T 10: 3/2T
22	DIGFILPH	Digital filter phase control 0: positive pulse 1: negative pulse
21	ANGFILEN	Analog filtering enable 0: disable 1: enable
20:16	Reserved	Reserved,the reset value must be maintained.
15	CMP_LPEN	Comparator low power mode enable 0: disable 1: enable
14:12	CMP_INMSEL[2:0]	The negative end of camparator 1 inputs the selection bit. 000：floating 001：DAC1 010：PA0 011：PA5 100：PB5 101：PD4 110：VREF_VC1 111：VREF_VC2
11:10	CMP_HYSEL[1:0]	Comparator hysteresis selection 00: no hysteresis 01: low hysteresis

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Bit field	Name	Description
		10: middle hysteresis 11: high hysteresis
9	DAC_CMP_ALWSON	DAC & CMP enable in sample mode Controls whether the comparator and DAC are always enabled when sampling, not enabled by default. 0: disable 1: enable
8	STAT_CLR_CTRL	Whether clear state on fast mode to slow mode Controls whether to clear the state from fast mode to slow mode, 0: clear 1: not clear
7	PWR_DUR_EN	Auto charge enable control enable 0: enable (automatically shuts off when the capacitor is full) 1: disable(Automatic charging is turned off, charging according to the time set by LPRCNT_CHxCFG1.CHGDUR bit)
6	CMP_AUTO_MODE	Automatic detection of damped oscillation end cycle control bits This bit needs to be used in conjunction with the LPRCNT_CTRL.CMPAUT bit 0: Ends after 4 cycles 1: Ends after 8 cycles
5:0	Reserved	Reserved,the reset value must be maintained.

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22 Liquid Crystal Display Controller (LCD)

22.1 Introduction

The LCD controller is suitable for monochrome passive Segment LCD, with a maximum of 8 common terminals (COM) and 44 Segment terminals (SEG), the specific number of terminals depends on the package of pin, refer to the data manual for details.The Segment LCD consists of a number of segments that can be turned on or off. Each segment contains a layer of liquid crystal molecules aligned between the two electrodes.The corresponding segment is visible when a voltage greater than the threshold voltage is applied to the liquid crystal.To avoid electrophoretic effects in the liquid crystal, the segment voltage must be AC.

The LCD controller can work in low power mode except STANDBY mode.

22.2 Main features

- Frame rate is configurable.
- Duty cycle is configurable: static, 1/2, 1/3, 1/4 and 1/8 duty cycle are supported.
- Voltage bias can be configured: static, 1/2, 1/3 and 1/4 bias are supported.
- Double buffering mechanism allows the user to update the data (pixel active/inactive information) in the display memory registers at any time.
- LCD power supply optional: add power supply from V_{LCD} pin (you can also connect V_{LCD} directly to VDD); Use a built-in DC-DC step-up converter (external 1μF capacitor is required).
- LCD clock source Optional: HSE/32, LSI, or LSE
- Two contrast control methods: adjust dead time of up to 7 phase cycles between frames; adjust V_{LCD} in V_{LCDmin}~ V_{LCDmax} range (when using internal step-up converter only).
- Built-in resistor network is used to generate LCD intermediate voltage, which can be configured by software to match the capacitive load of LCD panel.
- Built-in voltage output buffer
- It can be displayed in SLEEP, LOW-POWER RUN, LOW-POWER SLEEP, and STOP2 modes. It can also be disabled in these modes for lower POWER consumption.
- Built-in phase inversion reduces electromagnetic interference (EMI) and power consumption.
- Support blink function: 1, 2, 3, 4, 8 or all pixels can blink at the specified frequency (0.5Hz, 1Hz, 2Hz or 4Hz)
- Pins used for SEG and COM functions should be configured with the appropriate AFIO.

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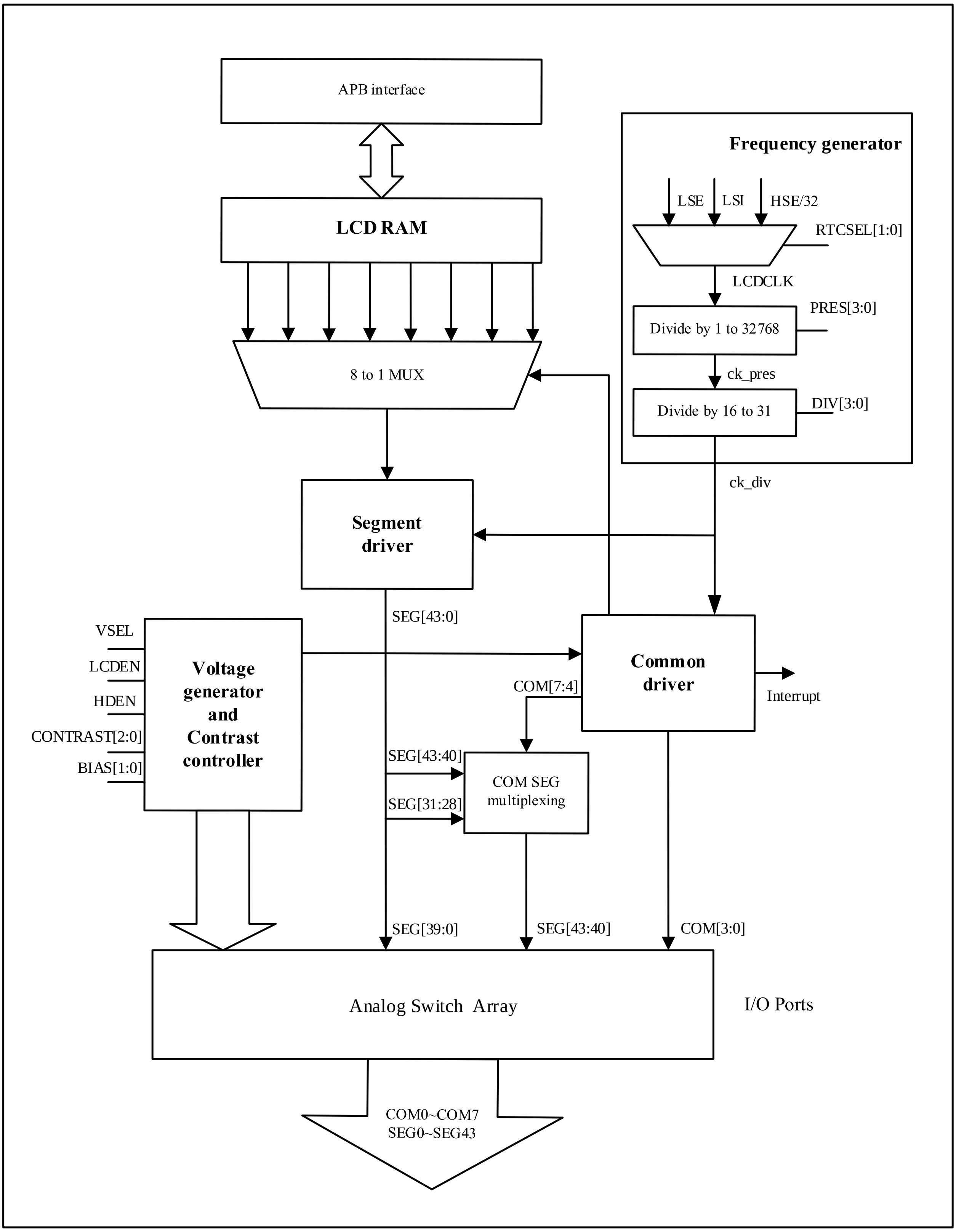
22.3 Functional block diagram

Figure 22-1 LCD controller block diagram



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22.4 Functional description

The LCD controller provides a fully configurable interface to support a variety of monochrome passive LCD with flexible frame frequencies. Each COM has same waveforms, but different phases. The number of COM ports depends on the duty cycle configuration, with the same waveform in a frame, but only one COM is active in each phase. LCD controllers support a variety of bias and duty cycles for a wide range of display features.

Optical contrast is the difference between the transparency of the on and off segments, that is, contrast can be defined as the difference between the RMS voltage of the on and off segments:

Optical contrast = [V_on(rms)- V_off(rms)]

Contrast also depends on the difference between the on voltage V_on(rms) and the threshold voltage V_th.

Where V_on(rms) and V_off(rms) are related to the duty cycle used to drive the display. As the number of COM terminals required to drive the LCD increases, the gap between V_on(rms) and V_off(rms) increases and the contrast decreases. In addition, for higher V_{LCD}, higher bias levels should be used to better separate V_on(rms) from V_off(rms) for better contrast.

Note: LCDCLK is the same as RTCCLK, please refer to the description of RTC/LCD clock in the RCC section.

22.4.1 Frequency generator

The frequency generator consists of a prescaler and a 16~31 clock divider.Configure LCD_FCTRL.PRES[3:0] to select LCDCLK divided by $2^{PRES[3:0]}$.Configure LCD_FCTRL.DIV[3:0] and divide the clock further by 16 to 31 for better frequency division.

Frequency generator output clock frequency f_{ck_div} is the time base of the entire LCD controller. f_{ck_div} is the LCD phase frequency, not the frame frequency (they are only equal in the static duty cycle case).Frame frequency (f_{frame}) is through f_{ck_div} divided by the number of effective COM terminals (or multiplied by duty cycle).

Frequency generator input clock frequency f_{LCDCLK} and its output clock frequency f_{ck_div} relationship:

$$f_{ck\_div} = \frac{f_{LCDCLK}}{2^{PRES} \times (DIV + 16)}$$

Output clock frequency f_{ck_div} and the frame frequency f_{frame} relationship:

$$f_{frame} = f_{ck\_div} \times \text{Duty}$$

By controlling LCD_FCTRL.BLINKF[2:0](configurable to 0,1,2...7), blink frequency in the range of 0.5Hz, 1Hz, 2Hz or 4Hz.Output clock frequency f_{ck_div} and blink frequency F_{BLINK} relationship:

$$f_{BLINK} = f_{ck\_div}/2^{(3+BLINKF)}$$

Example of frame frequency calculation is shown in the following table:

Table 22-1 Frame rate calculation example

LCDCLK	PRES[3:0]	DIV[3:0]	Ratio	Duty	f_{frame}
32.768kHz	3	1	136	1/8	30.12Hz
32.768kHz	4	1	272	1/4	30.12Hz

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32.768kHz	4	6	352	1/3	31.03Hz
32.768kHz	5	1	544	1/2	30.12Hz
32.768kHz	6	1	1088	static	30.12Hz
32.768kHz	1	4	40	1/8	102.4Hz
32.768kHz	2	4	80	1/4	102.4Hz
32.768kHz	2	11	108	1/3	101.14Hz
32.768kHz	3	4	160	1/2	102.4Hz
32.768kHz	4	4	320	static	102.4Hz
1.00MHz	6	3	1216	1/8	102.8Hz
1.00MHz	7	3	2432	1/4	102.8Hz
1.00MHz	7	10	3328	1/3	100.16Hz
1.00MHz	8	3	4864	1/2	102.8Hz
1.00MHz	9	3	9728	static	102.8Hz

Note: in order to achieve low power consumption and high refresh rate, the frame frequency range must be within 40Hz to 100Hz.

22.4.2 Common end driver

22.4.2.1 COM signal bias

Bias is the number of voltage levels used to drive the LCD. Select COM signal bias by LCD_CTRL.BIAS[1:0], which can be configured as 1/2 bias, 1/3 bias, and 1/4 bias.

COM[n] is active at n phase, and COM pin is driven to V_{LCD} on odd frames and to VSS on even frames.COM[n] is inactive in other phases, so at 1/3 or 1/4 bias: COM pin is driven to 1/3 or 1/4 V_{LCD} on odd frames and to 2/3 or 3/4 V_{LCD} on even frames; at 1/2 bias: both odd and even frames are always driven to 1/2 V_{LCD}.

When COM and SEG corresponding to a pixel are both active at the same phase, the voltage difference between COM and SEG is maximum and the pixel is activated. As shown in Figure 22-2, electromagnetic interference is reduced by phase inversion and the average voltage is 1/2 V_{LCD} at the end of each odd period.

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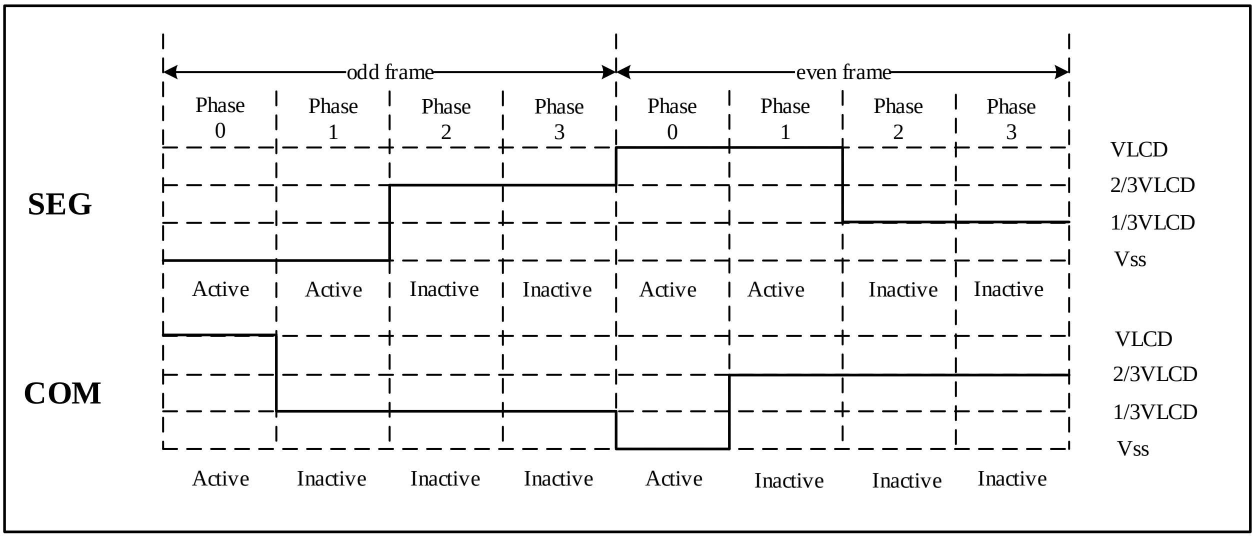
Figure 22-2 Odd-even frames example(1/4 duty cycle, 1/3 bias)



22.4.2.2 COM signal duty cycle

Duty cycle is 1/ (the number of common terminals on the LCD display).Select COM signal duty by LCD_CTRL.DUTY[2:0], which can be configured as static duty, 1/2 duty, 1/3 duty, 1/4 duty, and 1/8 duty. For example, if 1/4 duty cycle is selected and a total of four COMs are available, then there are four phases in a frame, where COM[0] is active during phase 0, COM[1] is active during phase 1, COM[2] is active during phase 2, and COM[3] is active during phase 3.

When static duty cycle is selected, COM[0] is always active, whereas COM[7:1] is not used and is driven to VSS, with only one phase in each frame, so f_{frame} is equal to f_{LCD}. At this time, SEG and COM only have two voltage levels, V_{LCD} and VSS. If the voltage difference between the corresponding SEG terminal and COM terminal is 0, the pixel is inactive; otherwise, the pixel is active and the LCD has the maximum contrast. As shown in Figure 22-3, pixel 0 is active while pixel 1 is inactive.

When the LCD_CTRL.LCDEN bit is disabled, all COM is pulled to VSS and the LCD_STS.ENSTS flag becomes 0.

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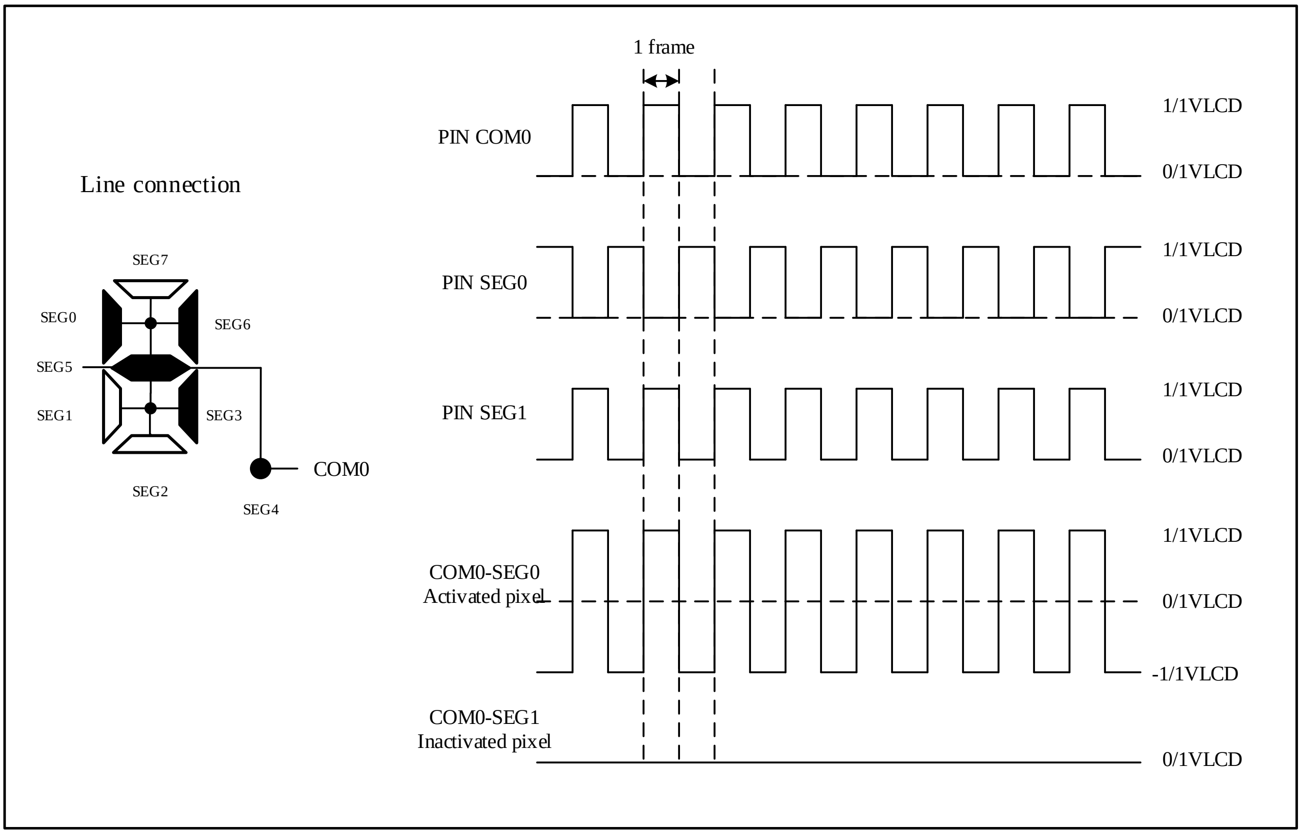
Figure 22-3 Static duty cycle example



22.4.2.3 Eight to one multiplexer selector

When COM[0] is activated, the COM driver module drives an eight-to-one multiplexer (refer to the LCD controller block diagram in Figure 22-1) to select the first two RAM registers data as the current display content. When COM[7] is active, the output of the eight-to-one multiplexer is the last two RAM registers data.

22.4.3 Segment driver

If pixel n is active, In 0 phase of odd frames, the SEG[n] pin is driven to VSS; In 0 phase of even frames, the SEG[n] pin is driven to V_{LCD}.

If pixel n is inactive, the SEG[n] pin is driven to 2/3 (2/4) V_{LCD} in odd frames and to 1/3 (2/4) V_{LCD} in even frames; if bias is 1/2, the SEG[n] pin is driven to V_{LCD} in odd frames and to VSS in even frames.

When the LCD_CTRL.LCDEN bit is disabled, all SEG ports are pulled down to VSS.

Below figure shows the waveform with different duty cycles and bias

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Figure 22-4 1/2 duty cycle, 1/2 bias

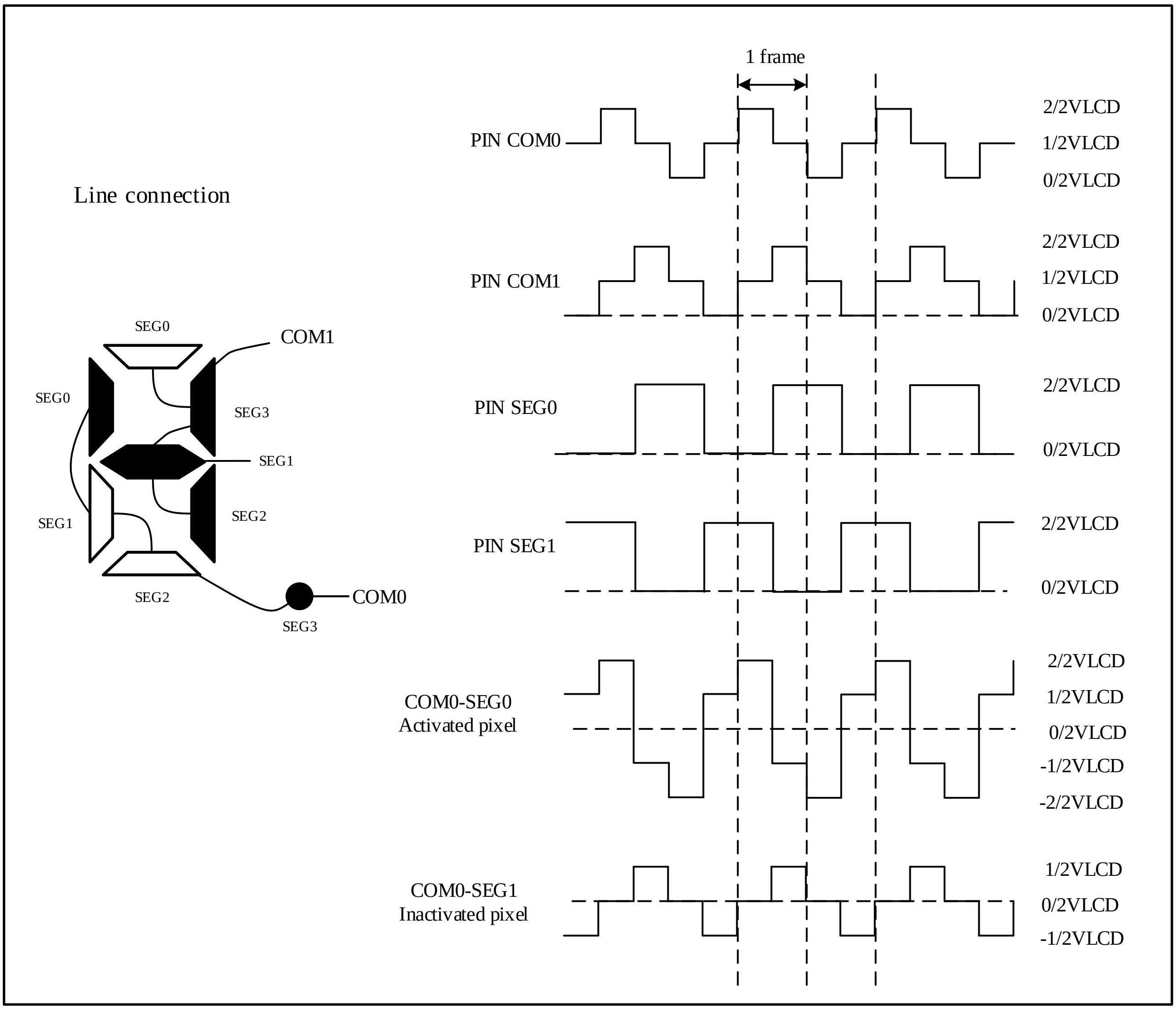

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Figure 22-5 1/3 duty cycle, 1/3 bias

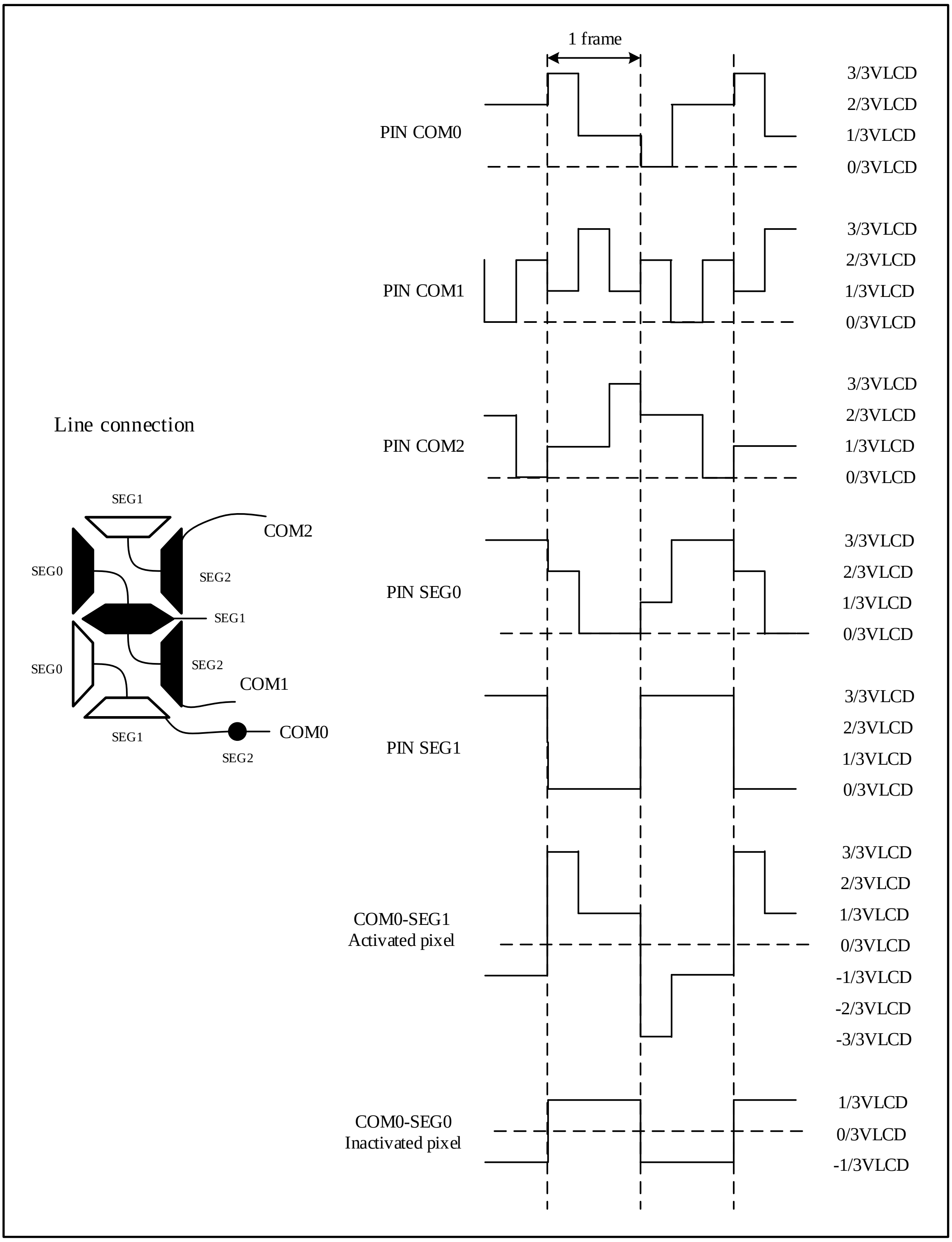

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Figure 22-6 1/4 duty cycle, 1/3 bias

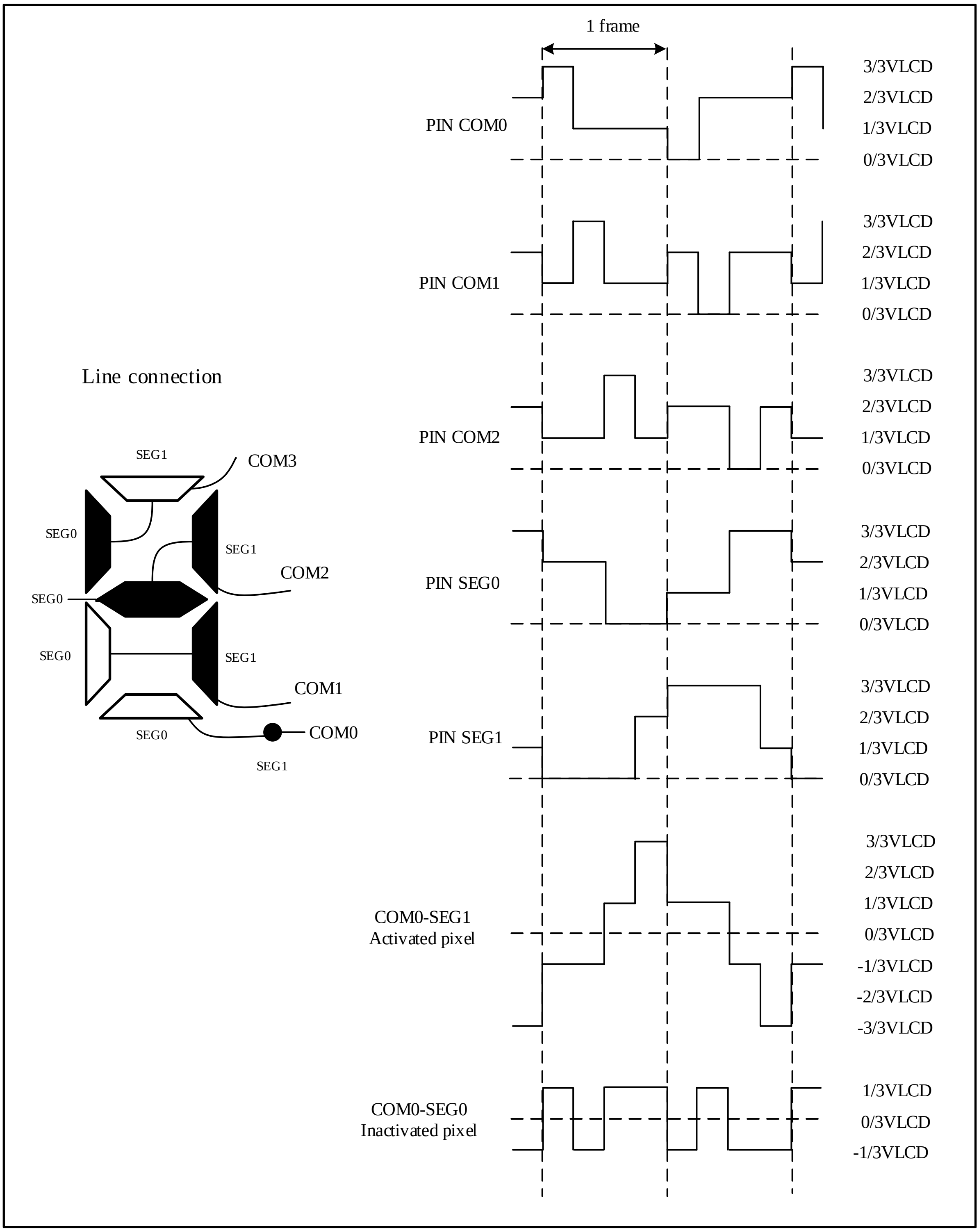

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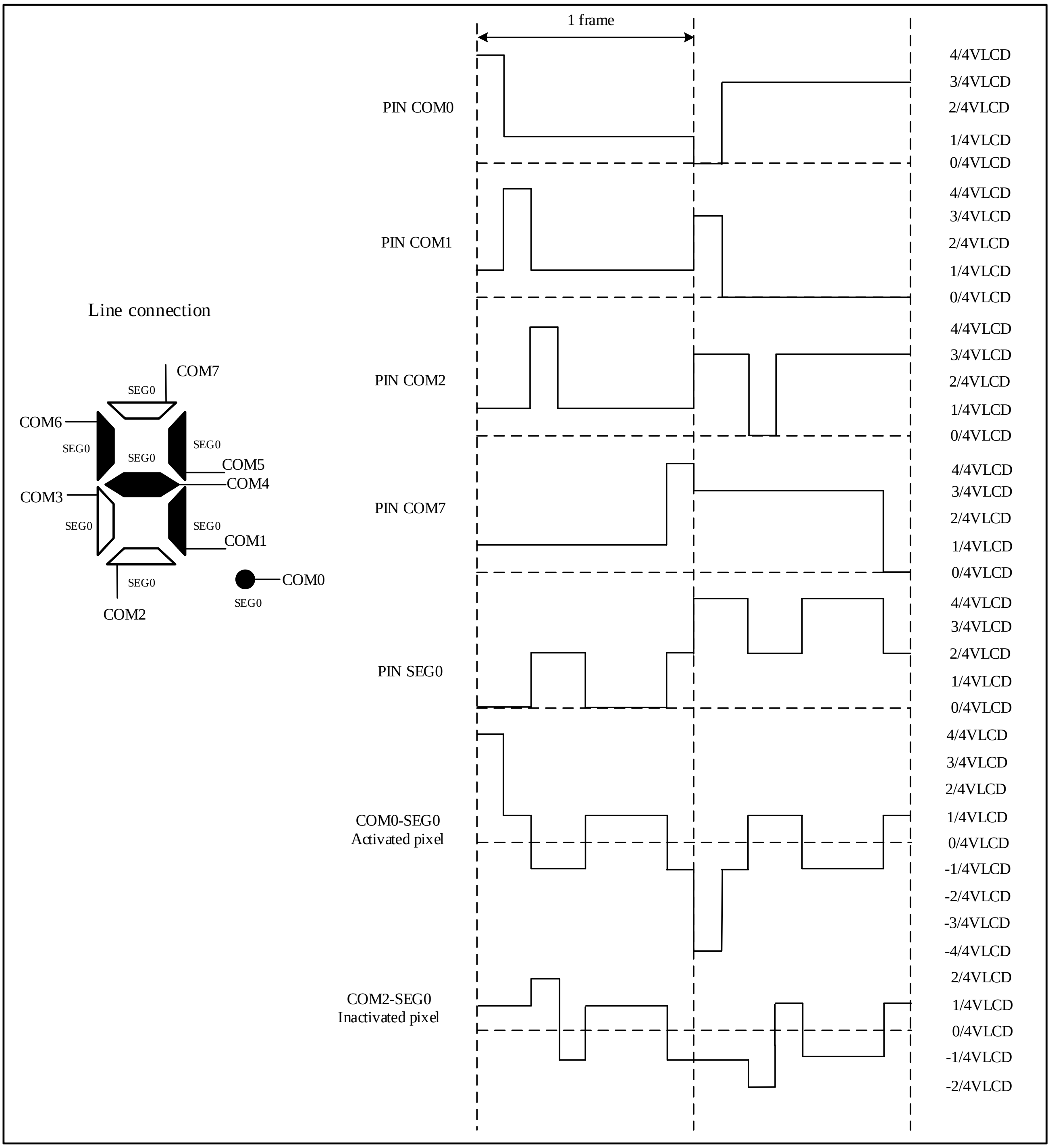
Figure 22-7 1/8 duty cycle, 1/4 bias



22.4.3.1 Blink function

The blink function of the SEG driver causes some pixels to blink continuously at a specific frequency. Blink mode is configured with LCD_FCTR.BLINK [1:0] bit to make up to 1, 2, 4, 8 or all pixels blink. Configure the blink frequency through LCD_FCTRL.BLINKF[2:0] bits and divide f_{ck_div}. Table 22-2 lists configuration examples for different blink frequencies.

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Table 22-2 Blink frequency configure example

BLINKF[2:0]			ck_div(LCDCLK = 32.768kHz)			
			32Hz	64Hz	128Hz	256Hz
0	0	0	4.0Hz	N/A	N/A	N/A
0	0	1	2Hz	4.0Hz	N/A	N/A
0	1	0	1Hz	2Hz	4.0Hz	N/A
0	1	1	0.5Hz	1Hz	2Hz	4.0Hz
1	0	0	0.25Hz	0.5Hz	1Hz	2Hz
1	0	1	N/A	0.25Hz	0.5Hz	1Hz
1	1	0	N/A	N/A	0.25Hz	0.5Hz
1	1	1	N/A	N/A	N/A	0.25Hz

22.4.4 Voltage generator and contrast control

22.4.4.1 Power supply selection

Configure LCD power from internal step-up converter or external voltage through LCD_CTRL.VSEL. When internal step-up converter is selected, the contrast ratio can be controlled in the range of V_{LCDmin} to V_{LCDmax} through LCD_FCTRL.CONTRAST[2:0] bits, and the new value of V_{LCD} takes effect at the beginning of a new frame; when external power supply is selected, the internal step-up converter is disabled to reduce power consumption, and the V_{LCD} voltage must be controlled within the range of V_{LCDmin} to V_{LCDmax}. At this time, the contrast ratio can be controlled by adjusting the dead time between frames.

When the LCD controller is disabled, configure as follows:

When using the internal step-up converter, you need to set LCD_CTRL.VSEL = 0, wait for C_{EXT} to charge (C_{EXT} is connected to the V_{LCD} pin, about 2 ms for C_{EXT} = 1 μF), and then enable the LCD_CTRL.LCDEN bit to enable the LCD controller.

When using the LCD external power supply, you need to set LCD_CTRL.VSEL = 1, then enable the LCD_CTRL.LCDEN bit to enable the LCD controller.

22.4.4.2 Drive selection

The LCD voltage generator generates an intermediate voltage between V_{LCD} and VSS through an internal resistor divider network, as shown in Figure 22-8.

There are two resistor networks inside the LCD driver, respectively using a low-value resistor R_L and a high-value resistor R_H to increase the drive current or reduce static power consumption.

For LCD_CTRL.LCDEN bit:

If the LCD_CTRL.LCDEN bit is set, the LCDEN switch in the block diagram is closed; when the LCD_CTRL.LCDEN bit is cleared, the LCDEN switch in the block diagram is opened in the end of the even frame to avoid intermediate voltages different from VSS in the odd-even frame .

For LCD_FCTRL.PULSEON[2:0] bits:

LCD_FCTRL.PULSEON[2:0] configures the time that R_L is enabled by the HDEN switch when the COM and SEG

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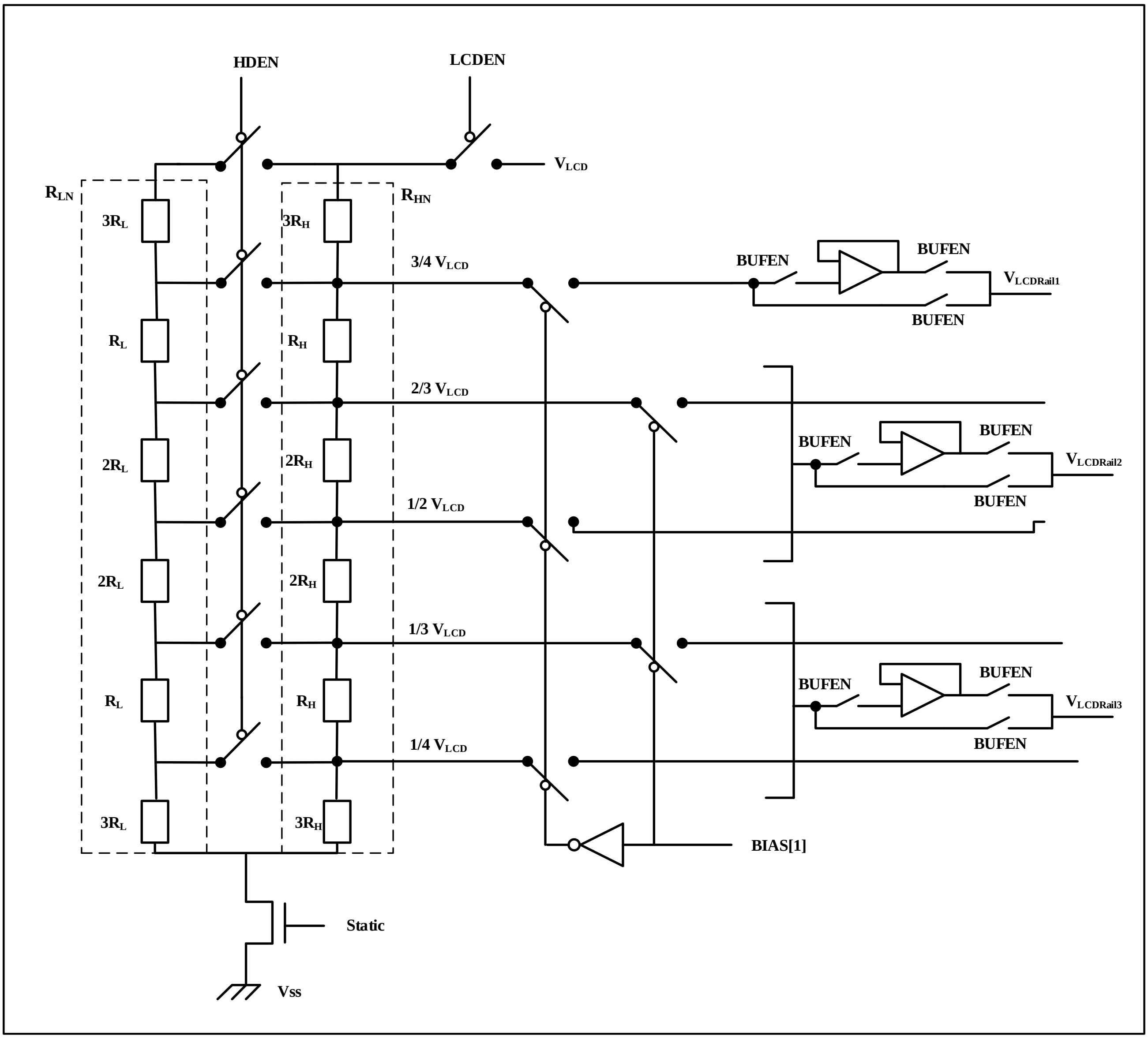
levels change. The shorter the driving time, the lower the power consumption, but the display with high internal resistance needs a longer driving time to obtain a good contrast ratio.

For LCD_FCTRL.HDEN bit:

If the LCD_FCTRL.HDEN bit and the LCD_FCTRL.PULSEON[2:0] bit are cleared, the HDEN switch is opened; if the LCD_FCTRL.HDEN bit is cleared and the LCD_FCTRL.PULSEON[2:0] bit is not 0, the HDEN switch closed during the number of pulses defined in the LCD_FCTRL.PULSEON[2:0] bits; if the HDEN bit in the LCD_FCTRL register is 1, the HDEN switch is always closed.

R_{LN} and R_{HN} represent the low value resistor divider network and high value resistor divider network respectively, R_{LN} can always be turned on by LCD_FCTRL.HDEN bit.

Figure 22-8 LCD drive voltage control



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22.4.4.3 Voltage buffer mode

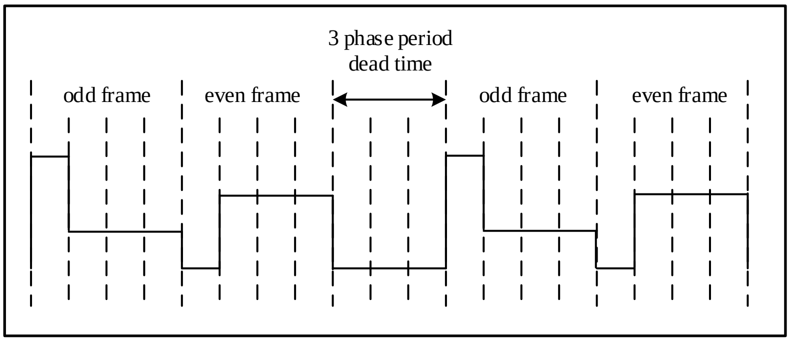
When the LCD_CTRL.BUFEN bit is configured (configured when LCD_CTRL.LCDEN is disabled) to enable the voltage output buffer, the high-value resistor network R_{HN} generates an intermediate voltage to reduce power consumption, and the low-value resistor network R_{LN} is automatically disabled(ignore LCD_FCTRL.HDEN bit or LCD_FCTRL.PULSEON bit configuration). After the LCD_CTRL.LCDEN bit is set, the LCD_STS.RDY bit is automatically set after the voltage level stabilizes, and the LCD controller starts to work.

Since the buffer prevents the LCD capacitive load from directly loading the resistive network and interfering with its voltage generation, the LCD drive capability is improved and the intermediate voltage is more stable, thereby increasing the rms voltage applied to the LCD pixels.

22.4.4.4 Dead time

Contrast can be controlled by setting the LCD_FCTR.DEAD[2:0] bit between frames.COM and SEG ports are set to VSS during dead time.

Figure 22-9 Dead time



22.4.5 Double buffer display

The LCD controller has built-in double buffer memory to ensure the consistency of display information without the need to use interrupt synchronization to control the modification of LCD_RAM. The application program can access the first buffer LCD_RAM through the APB interface. After modifying LCD_RAM, the software sets the LCD_STS.UDR flag, and the hardware copies the information to be updated to the second buffer LCD_DISPLAY. The update operation is synchronized with the frame (at the start of the next frame) until the update is complete, while LCD_RAM write is protected and the LCD_STS.UDR flag remains set. When the update is complete, LCD_STS.UDD is automatically set. If the LCD_FCTR.UDDIE bit is enabled, an interrupt will occur. Update operations take at most two frames time. Update operations are not performed until LCD_CTRL.LCDEN=1 (LCD_STS.UDR =1 and LCD_STS.UDD =0).

22.4.6 COM and SEG multiplexing

All output pins include: SEG[43:0] and COM[3:0].

LCD_CTRL.DUTY[2:0] automatically selects the number of SEG pins.In static, 1/2, 1/3 and 1/4 duty cycle modes, a maximum of 44 SEG pins and 1, 2, 3 and 4 COM pins are available.In 1/8 duty cycle mode, there are up to 40 SEG pins, and SEG[43:40] can be used as COM[7:4].

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If the duty cycle mode is not 1/8 and the device has few external pins, you can set the LCD_CTRL.MUXSEG bit to remap 4 SEG pins. When LCD_CTRL.MUXSEG=1, the output pin SEG[43:40] has the same function as SEG[31:28], while the original SEG[31:28] pin is unavailable.

The relationship between COM and SEG functions and duty cycle and pin remapping configuration is shown in Table 22-3.

Table 22-3 COM and SEG pins mapping table

Configure bits		SEG × COM			MCU output pins	LCD module function (3)
DUTY	MUXSEG	48 PIN	64PIN	80 PIN		
1/8	0/1	——	——	40×8	SEG[43:40]/ COM[7:4]	COM[7:4]
					COM[3:0]	COM[3:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	SEG[31:28]
					SEG[27:0]	SEG[27:0]
1/8(2)	0/1(2)	——	30×8(2)	——	SEG[43:40]/ COM[7:4]	COM[7:4] (2)
					COM[3:0]	COM[3:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not available
					SEG[27:0]	SEG[27:0]
1/4	0	——	——	44×4	SEG[43:40]/ COM[7:4]	SEG[43:40]
					COM[3:0]	COM[3:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	SEG[31:28]
					SEG[27:0]	SEG[27:0]
	1	——	——	40×4	SEG[43:40]/ COM[7:4]	SEG[31:28]
					COM[3:0]	COM[3:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	Not used
					SEG[27:0]	SEG[27:0]
1/4	0	——	34×4	——	SEG[43:40]/ COM[7:4]	Not available(1) SEG[43:40] (2)
					COM[3:0]	COM[3:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	SEG[31:28] (1) Not available(2)
					SEG[27:0]	SEG[27:0]
	1	——	30× 4(1) 34× 4(2)	——	SEG[43:40]/ COM[7:4]	Not available(1) SEG[31:28] (2)
					COM[3:0]	COM[3:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not used(1) Not available(2)

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Configure bits		SEG × COM			MCU output pins	LCD module function [3]
DUTY	MUXSEG	48 PIN	64PIN	80 PIN		
					SEG[27:0]	SEG[27:0]
	0/1	20×4	——	——	SEG[43:40]/ COM[7:4]	Not available
					COM[3:0]	COM[3:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not available
					SEG[17:0]	SEG[17:0]
1/3	0	——	——	44×3	SEG[43:40]/ COM[7:4]	SEG[43:40]
					COM[3]	Not used
					COM[2:0]	COM[2:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	SEG[31:28]
					SEG[27:0]	SEG[27:0]
	1	——	——	40×3	SEG[43:40]/ COM[7:4]	SEG[31:28]
					COM[3]	Not used
					COM[2:0]	COM[2:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	Not used
					SEG[27:0]	SEG[27:0]
1/3	0	——	34×3	——	SEG[43:40]/ COM[7:4]	Not available[1] SEG[43:40] [2]
					COM[3]	Not used
					COM[2:0]	COM[2:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	SEG[31:28] [1] Not available[2]
					SEG[27:0]	SEG[27:0]
	1	——	30× 3[1] 34× 3[2]	——	SEG[43:40]/ COM[7:4]	Not available[1] SEG[31:28] [2]
					COM[3]	Not used
					COM[2:0]	COM[2:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not used[1] Not available[2]
					SEG[27:0]	SEG[27:0]
	0/1	20×3	——	——	SEG[43:40]/ COM[7:4]	Not available
					COM[3]	Not used
					COM[2:0]	COM[2:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not available

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Configure bits		SEG × COM			MCU output pins	LCD module function [3]
DUTY	MUXSEG	48 PIN	64PIN	80 PIN		
					SEG[17:0]	SEG[17:0]
1/2	0	——	——	44×2	SEG[43:40]/ COM[7:4]	SEG[43:40]
					COM[3:2]	Not used
					COM[1:0]	COM[1:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	SEG[31:28]
					SEG[27:0]	SEG[27:0]
	1	——	——	40×2	SEG[43:40]/ COM[7:4]	SEG[31:28]
					COM[3:2]	Not used
					COM[1:0]	COM[1:0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	Not used
					SEG[27:0]	SEG[27:0]
1/2	0	——	34×2	——	SEG[43:40]/ COM[7:4]	Not available[1] SEG[43:40] [2]
					COM[3:2]	Not used
					COM[1:0]	COM[1:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	SEG[31:28] [1] Not available[2]
					SEG[27:0]	SEG[27:0]
	1	——	30×2[1] 34×2[2]	——	SEG[43:40]/ COM[7:4]	Not available[1] SEG[31:28] [2]
					COM[3:2]	Not used
					COM[1:0]	COM[1:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not used[1] Not available[2]
					SEG[27:0]	SEG[27:0]
	0/1	20×2	——	——	SEG[43:40]/ COM[7:4]	Not available
					COM[3:2]	Not used
					COM[1:0]	COM[1:0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not available
					SEG[17:0]	SEG[17:0]
STATIC	0	——	——	44×1	SEG[43:40]/ COM[7:4]	SEG[43:40]
					COM[3:1]	Not used
					COM[0]	COM[0]
					SEG[39:32]	SEG[39:32]

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Configure bits		SEG × COM			MCU output pins	LCD module function (3)
DUTY	MUXSEG	48 PIN	64PIN	80 PIN		
					SEG[31:28]	SEG[31:28]
					SEG[27:0]	SEG[27:0]
	1	——	——	40×1	SEG[43:40]/ COM[7:4]	SEG[31:28]
					COM[3:1]	Not used
					COM[0]	COM[0]
					SEG[39:32]	SEG[39:32]
					SEG[31:28]	Not used
					SEG[27:0]	SEG[27:0]
STATIC	0	——	34×1	——	SEG[43:40]/ COM[7:4]	Not available(1) SEG[43:40] (2)
					COM[3:1]	Not used
					COM[0]	COM[0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	SEG[31:28] (1) Not available(2)
					SEG[27:0]	SEG[27:0]
	1	——	30×1(1) 34×1(2)	——	SEG[43:40]/ COM[7:4]	Not available(1) SEG[31:28] (2)
					COM[3:1]	Not used
					COM[0]	COM[0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not used(1) Not available(2)
					SEG[27:0]	SEG[27:0]
	0/1	20×1	——	——	SEG[43:40] /COM[7:4]	Not available
					COM[3:1]	Not used
					COM[0]	COM[0]
					SEG[32], SEG[35]	SEG[32], SEG[35]
					SEG[31:28]	Not available
					SEG[17:0]	SEG[17:0]

1. Only applicable to version B chips, that is, the second character in the 8-bit code in the last line of the chip silkscreen is "B". The 64PIN package of version B chip does not support 1/8 duty cycle mode.

2. Only applicable to version C chips and above, that is, the second character in the 8-bit code in the last line of the chip silkscreen is not "B".

3. Not available: The pin is not lead out in the current package; Not used: The pin is lead out in the current package, but this function is not supported according to the current configuration.

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22.5 Working process

LCD controller workflow is as follows:

1. Configure LCD module parameters, clock source, COM/SEG port;
2. Write the default data to LCD_RAM, and set LCD_STS.UDR by software;
3. After configuring the frame frequency and contrast, set LCD_CTRL.LCDEN to enable the LCD module;
4. If you need to adjust the contrast, you can modify LCD_FCTRL.PRES[3:0], LCD_FCTRL.DIV[3:0], LCD_FCTRL.CONTRAST[2:0], LCD_FCTRL.PULSEON[2:0], LCD_FCTRL.DEAD[2:0] or LCD_FCTRL.HDEN bit;
5. If you need to modify the display data, you need to judge LCD_STS.UDR first, if it is 1, you need to wait; if it is 0, you can update the data to LCD_RAM, and then the software sets LCD_STS.UDR;
6. If you need to modify the blinking pixel and frequency, you can modify LCD_FCTRL.BLINK[1:0] and LCD_FCTRL.BLINKF[2:0].

22.6 Low power mode

The LCD controller can be displayed in STOP2 mode or completely disabled. The following table lists LCD behavior in various low-power modes.

Low power mode	Describe
SLEEP	Available. LCD interrupt triggers the device to exit SLEEP mode.
LOW POWER RUN	Available.
LOW POWER SLEEP	Available. LCD interrupt triggers the device to exit the LOW POWER SLEEP mode.
STOP2	Available. LCD interruption triggers the device to exit STOP2 mode.
STANDBY	Unavailable. LCD peripheral is powered down and must be re-initialized after exiting.

22.7 Interrupt request

LCD interrupt request is as follows:

Interrupt event	Flag	Interrupt enable control bit	Clear flag/interrupt methods
Start of frame interrupt	LCD_STS.SOF	LCD_FCTRL.SOFIE	LCD_CLR.SOFCLR write 1
Update display done interrupt	LCD_STS.UDD	LCD_FCTRL.UDDIE	LCD_CLR.UDDCLR write 1

22.8 LCD controller registers

LCD registers must be read and written by 32 bits

Start address of the LCD controller register is 0x40004000

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22.8.1 LCD controller register overview

Table 22-4 LCD controller register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	LCD_CTRL	Reserved																							BUFEN	MUXSEG	BIAS[1:0]		DUTY[2:0]			VSEL	LCDEN
	Reset Value																								0	0	0	0	0	0	0	0	0
004h	LCD_FCTRL	Reserved						PRES[3:0]				DIV[3:0]				BLINK[1:0]		BLINKF[2:0]			CONTRAST[2:0]			DEAD[2:0]			PULSEON[2:0]			UDDIE	Reserved	SOFIE	HDEN
	Reset Value							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
008h	LCD_STS	Reserved																										FCRSF	RDY	UDD	UDR	SOF	ENSTS
	Reset Value																											0	0	0	0	0	0
00Ch	LCD_CLR	Reserved																												UDDCLR	Reserved	SOFCLR	Reserved
	Reset Value																													0		0	
014h	LCD_RAM1_COM0	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LCD_RAM2_COM0	Reserved																				S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
01Ch	LCD_RAM1_COM1	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	LCD_RAM2_COM1	Reserved																				S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
024h	LCD_RAM1_COM2	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	LCD_RAM2_COM2	Reserved																				S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
02Ch	LCD_RAM1_COM3	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	LCD_RAM2_COM3	Reserved																				S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
034h	LCD_RAM1_COM4	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	LCD_RAM2_COM4	Reserved																								S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																									0	0	0	0	0	0	0	0
03Ch	LCD_RAM1_COM5	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	LCD_RAM2_COM5	Reserved																								S39	S38	S37	S36	S35	S34	S33	S32

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																									0	0	0	0	0	0	0	0
044h	LCD_RAM1_COM6	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	LCD_RAM2_COM6	Reserved																								S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																									0	0	0	0	0	0	0	0
04Ch	LCD_RAM1_COM7	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	LCD_RAM2_COM7	Reserved																								S39	S38	S37	S36	S35	S34	S33	S32
	Reset Value																									0	0	0	0	0	0	0	0

22.8.2 LCD control register (LCD_CTRL)

Address offset: 0x00

Reset value: 0x0000 0000

31:16
Reserved

15:9	8	7	6:5	4:2	1	0
Reserved	BUFEN	MUXSEG	BIAS[1:0]	DUTY[2:0]	VSEL	LCDEN
	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	BUFEN	Voltage output buffer enable This bit is used to enable or disable high drive capability voltage output. 0: Disable. 1: Enable.
7	MUXSEG	Mux segment enable This bit is used to enable SEG pin remapping. Four SEG pins can be multiplexed with SEG[31:28]. 0: SEG pin remapping is disabled. 1: SEG[43:40] pin remapping is SEG[31:28], and SEG[31:28] pin is disabled. See the COM and SEG pins mapping table.
6:5	BIAS[1:0]	Bias selector 00:1/2 Bias; 01:1/3 Bias; 10:1/4 Bias; 11: Reserved.
4:2	DUTY[2:0]	Duty selection 000: static LCD; 001:1/2 DUTY; 010:1/3 duty; 011:1/4 duty;

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Bit field	Name	Description
		100:1/8 duty; other: Reserved.
1	VSEL	Voltage source selection 0: Internal source (voltage step-up converter); 1: External source (V_{LCD} pin).
0	LCDEN	LCD controller enable This bit is set/reset by software to enable/disable the LCD controller. Software reset will turn off the LCD before the start of the next frame, and all COM and SEG will be pulled down to VSS after disable. 0: Disable. 1: Enable.

Note: LCD_CTRL.VSEL, LCD_CTRL.DUTY, LCD_CTRL.BIAS, LCD_CTRL.MUXSEG and LCD_CTRL.BUFEN are write protected after LCD_CTRL.LCDEN is enabled. If you want to modify these bits, you must disable the LCD controller first.

22.8.3 LCD frame control register (LCD_FCTRL)

Address offset: 0x04

Reset value: 0x0000 0000

31:26	25:22	21:18	17:16
Reserved	PRES[3:0]	DIV[3:0]	BLINK[1:0]
	rw	rw	rw

15:13	12:10	9:7	6:4	3	2	1	0
BLINKF[2:0]	CONTRAST[2:0]	DEAD[2:0]	PULSEON[2:0]	UDDIE	Reserved	SOFIE	HDEN
rw	rw	rw	rw	rw		rw	rw

Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25:22	PRES[3:0]	16-bit prescaler $ck\_pres = LCDCLK/2^n$ 0000: ck_pres = LCDCLK; 0001: ck_pres = LCDCLK/2; 0010: ck_pres = LCDCLK/4; … 1111: ck_pres = LCDCLK/32768.
21:18	DIV[3:0]	DIV clock divider ck_div = ck_pres/(16+n) 0000: ck_div = ck_pres/16; 0001: ck_div = ck_pres/17; 0010: ck_div = ck_pres/18; ... 1111: ck_div = ck_pres/31.

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Bit field	Name	Description
17:16	BLINK[1:0]	Blink mode selection 00: Disable blink; 01: Enable SEG[0], COM[0] blink (1 pixel); 10: Enable SEG[0], all COM flashing (up to 8 pixels, depending on duty cycle); 11: Enable all SEG and COM flashing (all pixels).
15:13	BLINKF[2:0]	Blink frequency selection 000: ck_div / 8; 001: ck_div / 16; 010: ck_div / 32; 011: ck_div / 64; 100: ck_div / 128; 101: ck_div / 256; 110: ck_div / 512; 111: ck_div / 1024.
12:10	CONTRAST[2:0]	Contrast control These bits specify the maximum V_{LCD} voltage (independent of the VDD), which ranges from 2.60V to 3.58V. 000: V_{LCD0} (2.6V); 001: V_{LCD1} (2.73V); 010: V_{LCD2} (2.86V); 011: V_{LCD3} (3.01V); 100: V_{LCD4} (3.16V); 101: V_{LCD5} (3.28V); 110: V_{LCD6} (3.42V); 111: V_{LCD7} (3.58V).
9:7	DEAD[2:0]	Dead time duration These bits configure the dead time between frames by software. During dead time, COM and SEG voltage levels stabilize at 0V, allowing contrast to be reduced without modifying the frame rate. 000: no dead time; 001: 1 phase period dead time; 010: 2 phase period dead time; 011: 3 phase period dead time; 100: 4 phase period dead time; 101: 5 phase period dead time; 110: 6 phase period dead time; 111: 7 phase period dead time.
6:4	PULSEON[2:0]	Pulse on duration This bit configures the pulse duration based on ck_pres. 000: 0; 001: 1 / ck_pres;

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Bit field	Name	Description
		010: 2 / ck_pres; 011: 3 / ck_pres; 100: 4 / ck_pres; 101: 5 / ck_pres; 110: 6 / ck_pres; 111: 7 / ck_pres. *Note: Pulse should not exceed half of LCD clock cycle.*
3	UDDIE	Update display done interrupt enable This bit is set and cleared by the software. 0: Disable. 1: Enable.
2	Reserved	Reserved, the reset value must be maintained.
1	SOFIE	Start of frame interrupt enable This bit is set and cleared by the software. 0: Disable. 1: Enable.
0	HDEN	High Drive Enable (High drive enable) This bit enables low resistance voltage divider. 0: Permanent high drive disabled; 1: Permanent high drive enabled. *Note: When HDEN is 1, the LCD_FCTRL.PULSEON bit must be set to 001.*

Note: the LCD_FCTRL register can be modified at any time, and the new configuration takes effect at the start of the next frame (except for the LCD_FCTRL.UDDIE and LCD_FCTRL.SOFIE bits, which take effect immediately after modification).When LCD_CTRL.BUFEN is 1, the low resistance network is automatically disabled, and LCD_FCTRL.HDEN and LCD_FCTRL.PULSEON configurations are ignored.

22.8.4 LCD status register (LCD_STS)

Address offset: 0x08

Reset value: 0x0000 0020

31:16
Reserved

15:6	5	4	3	2	1	0
Reserved	FCRSF	RDY	UDD	UDR	SOF	ENSTS
	r	r	r	rs	r	r

Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	FCRSF	LCD frame control register synchronization flag Every time the LCD_FCTRL register is updated in the LCDCLK domain, the bit is

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Bit field	Name	Description
		set to 1 by the hardware. When writing to the LCD_FCTRL register, this bit is cleared by the hardware. 0: Not yet synchronized. 1: Synchronized.
4	RDY	Ready flag (voltage converter ready state) This bit is set and cleared by hardware. 0: Voltage converter is not ready. 1: Voltage converter is enabled and provides the correct voltage.
3	UDD	Update display done The bit is set to 1 by hardware.If LCD_FCTR.UDDIE set to 1, a UDD interrupt is generated. The bit is cleared when LCD_CLR.UDDCLR bit is written to 1.Setting has a higher priority than clearing. 0: No event. 1: Update display request is complete.
2	UDR	Update display request After modification LCD_RAM each time, the software must set the UDR bit to 1 inform the hardware to transfer the updated data to the secondary buffer. 0: Invalid. 1: Updates display request.
1	SOF	Start of frame flag This bit is set by the hardware at the start of a new frame. If LCD_FCTRL.SOFIE set to 1, a SOF interrupt is generated.. The bit is cleared when LCD_CLR.SOFCLR bit is written to 1.Clearing has a higher priority than setting. 0: No event. 1: Start of frame event occurred.
0	ENSTS	LCD controller status. This bit is set and cleared by hardware. 0: LCD controller is disabled. 1: LCD controller is enabled.

22.8.5 LCD clear register (LCD_CLR)

Address offset: 0x0C

Reset value: 0x0000 0000

31–16
Reserved

15–4	3	2	1	0
Reserved	UDDCLR	Reserved	SOFCLR	Reserved
	w		w	

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Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	UDDCLR	Update display done clear 0: Invalid. 1: Clears the UDD flag.
2	Reserved	Reserved, the reset value must be maintained.
1	SOFCLR	Start of frame flag clear 0: Invalid. 1: Clears the SOF flag.
0	Reserved	Reserved, the reset value must be maintained.

22.8.6 LCD display memory register (LCD_RAM1_COMx x = 0...7)

Address offset: 0x14 + x*8

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:0	Sy	Display memory LCD_RAM1_COMx (x = 0...7) Pixel bits (y = 0...31), each bit corresponds to a pixel. The pixel value 1 represents activity, and 0 represents inactivity.

22.8.7 LCD display memory register (LCD_RAM2_COMx x = 0...3)

Offset address: 0x18 + x*8

Reset value: 0x0000 0000

31															16
Reserved															
15			12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
11:0	Sy	Display memory LCD_RAM2_COMx (x = 0...3) Pixel bit (y = 0...11), each bit corresponds to a pixel. The pixel value 1 represents activity, and 0 represents inactivity.

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22.8.8 LCD display memory register (LCD_RAM2_COMx x = 4...7)

Address offset: 0x18 + x*8

Reset value: 0x0000 0000

31–16
Reserved

15–8	7	6	5	4	3	2	1	0
Reserved	S39	S38	S37	S36	S35	S34	S33	S32
	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	Sy	Display memory LCD_RAM2_COMx (x = 4...7) Pixel bits (y = 0...7), each bit corresponds to a pixel. The pixel value 1 represents activity, and 0 represents inactivity.

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23 I^2C interface

23.1 Introduction

I2C(Inter-Integrated Circuit) bus is a widely used bus structure, it has only two bidirectional lines, namely data bus SDA and clock bus SCL. All devices compatible with I2C bus can communicate directly with each other through I2C bus with these two lines.

I2C interface connects microcontroller and serial I2C bus, and can be used for communication between MCU and external I2C devices. It supports standard speed mode and fast mode, it supports CRC calculation and verification, SMBus (System Management Bus) and PMBus (Power Management Bus), it also provides multi-master function to control all I2C bus specific timing, protocol, arbitration. I2C interface module also supports DMA mode, which can effectively reduce the CPU overload.

23.2 Main features

- Same interface can have both master function and slave function
- Parallel-bus to I^2C protocol converter
- Supports 7-bit/10-bit address mode and broadcast addressing
- As I^2C master, it can generate clock, start and stop signal
- As I^2C slave, it supports address detection, stop bit detection function
- Support standard speed mode(up to 100 kHz) ,fast mode(up to 400 kHz)and fast plus mode(up to 1MHz)
- Support interrupt vector, byte transfer successfully interrupt and error event interrupt
- Optional clock extending function
- Support DMA mode
- Optional PEC (Packet Error Check) generation and verification
- Compatible with SMBus 2.0 and PMBus

Note: not all of the above features are included in all products. Please refer to the relevant data manual to confirm the I^2C functions supported by the product.

23.3 Function description

I2C interface is connected to I2C bus through data pin (SDA) and clock pin (SCL) to communicate with external devices. It can be connected to standard (up to 100kHz) or fast (up to 400kHz, 1MHz) I2C bus. I2C module converts data from serial to parallel when receiving, and converts data from parallel to serial when sending. It support interrupt mode, users can enable or disable interrupt according to their needs.

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23.3.1 SDA and SCL line control

I2C module has two interface lines: serial data line (SDA) and serial clock line (SCL). Devices connected to the bus and transmit information to each other through these two wires. SDA and SCL are two-way wires, it should connected to a current source or the positive of the power supply with a pull-up resistor. When the bus is idle, both lines are high level. The output of device which is connected to the bus must have open drain or open collector to provide wired-AND functionality. The data on I2C bus can reach 100 kbit/s in standard mode and 1000 kbit/s in fast mode. Since devices of different processors may be connected to the I2C bus, the levels of logic '0' and logic '1' are not fixed and depend on the actual level of VDD.

If the clock extending is allowed, the SCL line is pulled down which can be avoided the overload error during receiving and the under load error during transmission.

For example, when in the transmission mode, if the transmit data register is empty and the byte transmit end bit is set (I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1), the I2C interface keeps the clock line low before transmission to wait for the software to read STS1 and write the data into the data register (both buffer and shift register are empty); when In the receive mode, if the data register is not empty and the byte sending end bit is set (I2C_STS1.RXDATNE = 1, I2C_STS1.BSF = 1), the I2C interface keeps the clock line low after receiving the data byte, waiting for the software to read STS1, and then read the data register(buffer and shift register are full).

If clock extending is disable in slave mode, if the receive data register is not empty (I2C_STS1.RXDATNE = 1) in the receive mode, and the data has not been read before receiving the next byte, an overrun error will issue and the last word byte will be discarded. In transmit mode, if the transmit data register is empty (I2C_STS1.TXDATE = 1), no new data is written into the data register before the next byte must be sent, an underrun error will issue. The same byte will be send repeatedly. In this case, duplicate write conflicts are not controlled.

23.3.2 Software communication process

The data transmission of I2C device is divided into master and slave. Master is the device responsible for initializing the transmission of data on the bus and generating clock signal. At this time, any addressed device is a slave. Whether the I2C device is a master or a slave, it can send or receive data. Therefore, the I2C interface supports four operation modes:

- Slave transmitter mode
- Slave receiver mode
- Master transmitter mode
- Master receiver mode

After system reset, I2C works in slave mode by default. The I2C interface is configured by software to send a start bit on the bus, and then the interface automatically switches from the slave mode to the master mode. When arbitration is lost or a stop signal is generated, the interface will switched to the slave mode from the receive mode.

The block diagram of I^2C interface is shown in the figure below.

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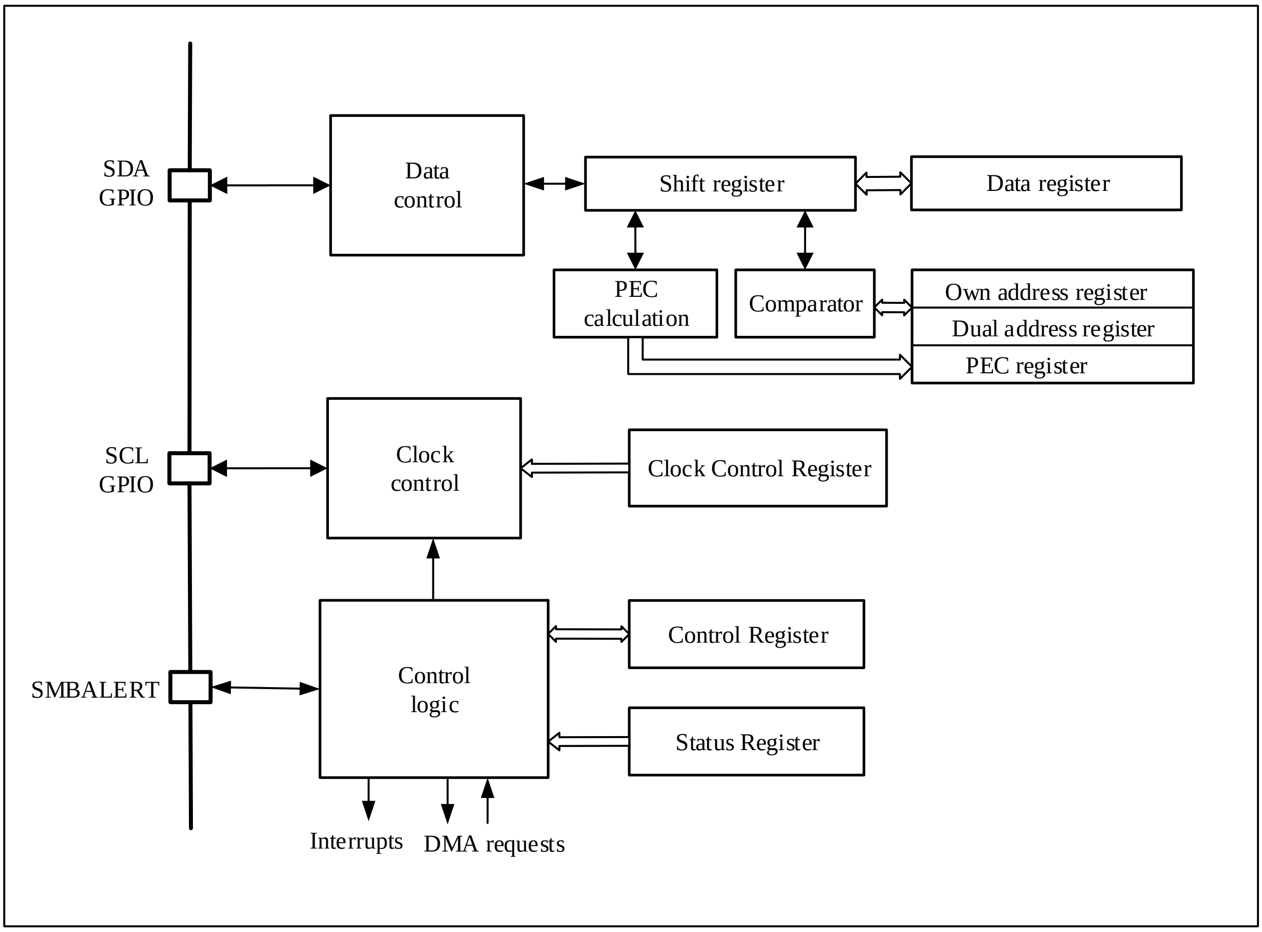
Figure 23-1 I²C functional block diagram

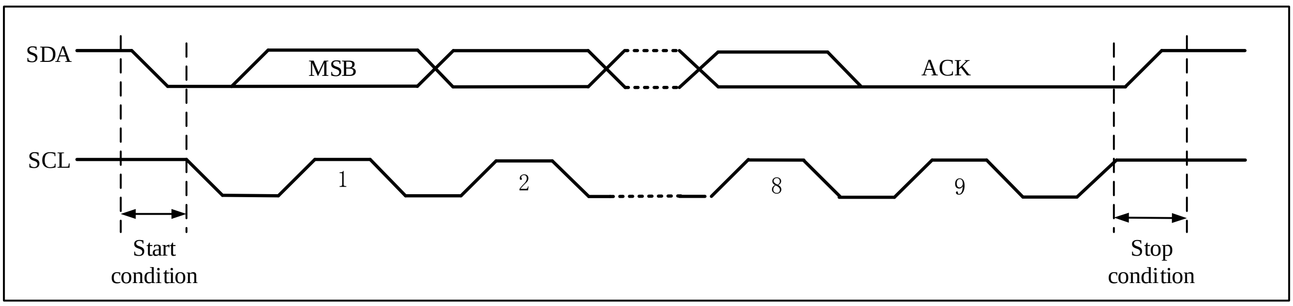


Note: in SMBus mode, SMBALERT is an optional signal. If SMBus is disabled, the signal cannot be used

23.3.2.1 Start and stop conditions

All data transfers always start with the start bit and end with the stop bit. The start and stop conditions are generated by software in the master mode. Start bit is a level conversion from high to low on SDA line when SCL is high. Stop bit is a level transition from low to high on SDA line when SCL is high. as shown in the figure below.

Figure 23-2 I2C bus protocol



23.3.2.2 Clock synchronization and Arbitration

The I2C module supports multi-master arbitration, which means two masters can initiate an I2C START

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operation concurrently when the bus is inactive. So some mechanisms are needed to grant a master the access to the bus. This process is generally named Clock Synchronization and Arbitration.

I2C module has two key features:

- SDA and SCL are drain open circuit structures, and the signal "wire-and" logic is realized through an external pull-up resistor.
- SDA and SCL pins will also detect the level on the pin while outputting the signal to check whether the output is consistent with the previous output. This provides the hardware basis for "Clock Synchronization" and "Bus Arbitration".

The I2C device on the bus is to output logic 0 by "grounding the line". Based on the characteristics of the I2C bus, if one device sends logic 0 and the other sends logic 1, then the line sees only logic 0, so there is no possibility of level conflicts on the line.

The physical connection of the bus allows the master to read data while writing data to the bus. In this way, when two masters are competing for the bus, the one that sends logic 0 does not know the occurrence of the competition. Only the one that sends logic 1 will find the conflict (when writing a logic 1, but read 0) and exit the competition.

Clock synchronization

The high-to-low switching of the SCL line causes the devices to begin counting their low-level periods, and once the device's clock goes low, it keeps the SCL line in this state until the high-level of the clock is reached. However, if another clock is still in the low period, the low-to-high switch of this clock will not change the state of the SCL line. Therefore, the SCL line is kept low by the device with the longest low-level period. A device with a short low-level period will enter a high-level wait state.

When all related devices have counted their low-level periods, the clock line is released and goes high-level, after which there is no difference in the state of the device clock and SCL lines, and all devices will begin counting their high-level periods, the device that completes the high-level period first will pull the SCL line low again.

In this way, the low-level period of the generated synchronous SCL clock is determined by the device with the longest low-level clock period, and the high-level period is determined by the device with the shortest high-level clock period.

Arbitration

Arbitration, like synchronization, is to resolve bus control conflicts in the case of multiple masters. The arbitration process has nothing to do with the slave. When the two masters both produce a valid start bit when the bus is idle, in this case, it is necessary to decide which master will complete the data transmission. This is the process of arbitration.

Each master controller does not have the priority level of controlling the bus, which is all determined by arbitration. The bus control is determined and carried out bit by bit. They follow the principle of "low level first", that is, whoever sends the low level first will control the bus. During the arbitration of each bit, when SCL is high, each host checks whether its own SDA level is the same as that sent by itself. In theory, if the content transmitted by two hosts is exactly the same, then they can successfully transmit without errors. If a host sends a high level but detects that the SDA line is low, it considers that it has lost arbitration and shuts down its SDA output driver, while the other host continues to complete its own transmission.

23.3.2.3 I2C data communication flow

Each I2C device is identified by a unique address. According to the device function, they can be either a transmitter

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or a receiver.

The I2C host is responsible for generating the start bit and the end bit in order to start and end a transmission. And is responsible for generating the SCL clock.

The I2C module supports 7-bit and 10-bit addresses, and the user can configure the address of the I2C slave through software. After the I2C slave detects the start bit on the I2C bus, it starts to receive the address from the bus, and compares the received address with its own address. Once the two addresses are matched, the I2C slave will send an acknowledgement (ACK) and respond to subsequent commands on the bus: send or receive the requested data. In addition, if the software opens a broadcast call, the I2C slave always sends a confirmation response to a broadcast address (0x00).

Data and address are transmitted in 8-bit width, with the most significant bit first. The 1 or 2 bytes following the start condition is the address (1 byte in 7-bit mode, 2 bytes in 10-bit mode). The address is only sent in master mode. During the 9th clock period after 8 clocks of a byte transmission, the receiver must send back an acknowledge bit (ACK) to the transmitter, as shown in the Figure 23-2 I2C bus protocol.

Software can enable or disable acknowledgement (ACK), and can set the I2C interface address (7-bit, 10-bit address or general call address).

23.3.2.4 I2C slave transmission mode

In slave mode, the transmission reception flag bit (I2C_STS2.TRF) indicates whether it is currently in receiver mode or transmission mode. When sending data to I2C bus in transmission mode, the software should follow the following steps:

1、 First, enable I2C peripheral clock and configure the clock related register in I2C_CTRL1, ensuring the correct I2C timing. After these two steps are completed, I2C runs in slave mode, waiting for receiving start bit and address.

2、 I2C slave receives a start bit first, and then receives a matching 7-bit or 10-bit address. I2C hardware will set the I2C_STS1.ADDRF(received address and matched its own address). The software should monitor this bit regularly or have an interrupt to monitor this bit. After this bit is set, the software reads I2C_STS1 register and then read I2C_STS2 register to clear the I2C_STS1.ADDRF bit. If the address is in 10 bit format, the I2C master should then generate a START and send an address header to the I2C bus. After detecting START and the following address header, the slave will continue to set I2C_STS1.ADDRF bit. The software continues to read I2C_STS1 register and read I2C_STS2 register to clear the I2C_STS1.ADDRF bit a second time.

3、 I2C enters the data sending state, and now shift register and data register I2C_DAT are all empty, so the hardware will set the I2C_STS1.TXDATE(send data empty). At this time, the software can write the first byte data to I2C_DAT register, however, because the byte of the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit is not cleared to zero. When the shift register is not empty, I2C starts to send data to I2C bus.

4、 During the sending of the first byte, the software writes the second byte to I2C_DAT, neither the I2C_DAT register nor the shift register is empty. The I2C_STS1.TXDATE bit is cleared to 0.

5、 After the first byte is sent, I2C_STS1.TXDATE is set again, and the software writes the third byte to I2C_DAT, the same time, the I2C_STS1.TXDATE bit is cleared.After that, as long as there is still data to be sent and I2C_STS1.TXDATE is set to 1, the software can write a byte to I2C_DAT register.

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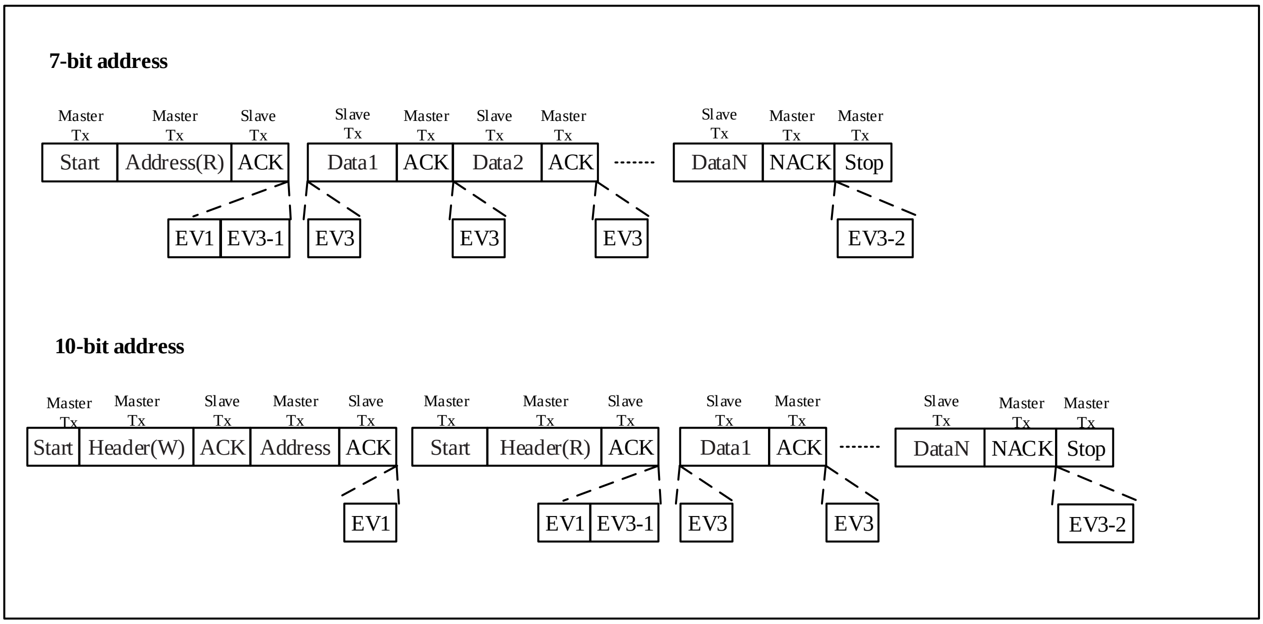
6、 During the sending of the second last byte, the software writes the last data to the I2C_DAT register to clear the I2C_STS1.TXDATE flag bit, and then the I2C_STS1.TXDATE status is no longer concerned. I2C_STS1.TXDATE bit is set after the second last byte is sent until the stop end bit is detected.

7、 According to the I2C protocol, the I2C master will not send a ACK to the last byte received. Therefore, after the last byte is sent, the I2C_STS1.ACKFAIL bit (acknowledge fail) of the I2C slave will be set to notify the software of the end of sending. The software writes 0 to the I2C_STS1.ACKFAIL bit to clear this bit.

Figure 23-3 Slave transmitter transfer sequence diagram



Instructions：

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 register to clear the event.
2. EV3-1: I2C_STS1.TXDATE=1, shift register is empty, data register is empty, write DAT.
3. EV3: I2C_STS1.TXDATE=1, shift register is not empty, data register is empty, write DAT will clear the event.
4. EV3-2: I2C_STS1.ACKFAIL=1, ACKFAIL bit of STS1 register write "0" to clear the event.

Note: a) EV1 and EV3_1 event prolongs the low SCL time until the end of the corresponding software sequence.

b) The software sequence of EV3 must be completed before the end of the current byte transfer.

23.3.2.5 I2C slave receiving mode

When receiving data in slave mode, the software should operate as follows:

1、 First, enable I2C peripheral clock and configure the clock related register in I2C_CTRL1 ensuring the correct I2C timing. After these two steps are completed, I2C runs in slave mode, waiting for receiving start bit and address.

2、 After receiving the START condition and the matched 7-bit or 10-bit address, I2C hardware will set I2C_STS1.ADDRF bit(the address received and matched with its own address) to 1. This bit should be detected by software polling or interrupt. After it is found that it is set, the software clears the I2C_STS1.ADDRF bit by

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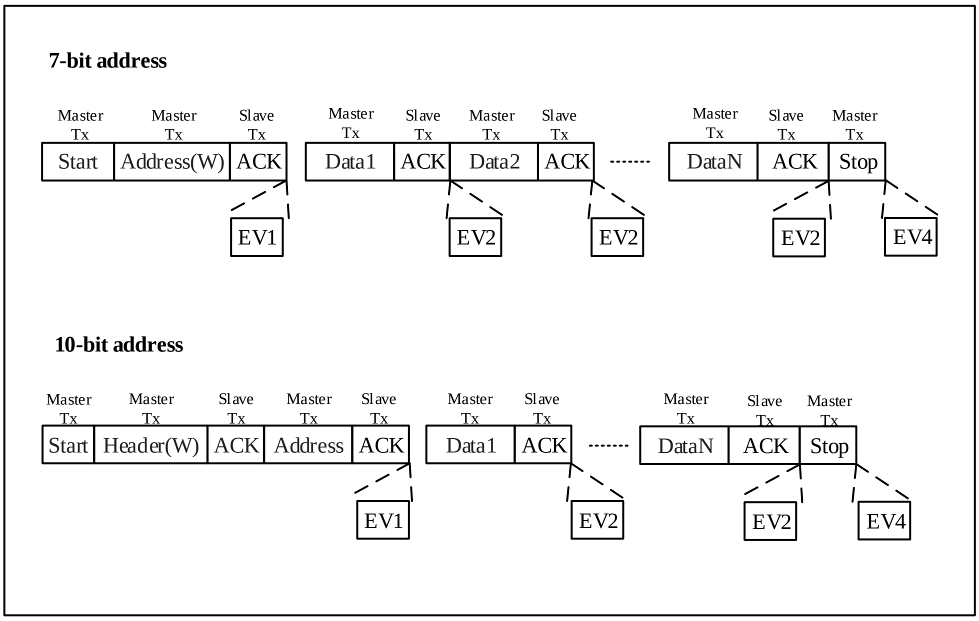
reading I2C_STS1 register first and then I2C_STS2 register. Once the I2C_STS1.ADDRF bit is cleared,The I2C slave starts to receive data from the I2C bus.

3、 When the first byte is received, the I2C_STS1.RXDATNE bit (the received data is not empty) is set to 1 by hardware. If the I2C_CTRL2.EVTINTEN and I2C_CTRL2.BUFINTEN bits are set, an interrupt is generated. The software should check this bit by polling or interrupt. Once it is found that it is set, the software can read the first byte of I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. Note that if the I2C_CTRL1.ACKEN bit is set, after receiving a byte,the slave should generate a response pulse.

4、 At any time, as long as the I2C_STS1.RXDATNE bit is set to 1, the software can read a byte from the I2C_DAT register. When the last byte is received, I2C_STS1.RXDATNE is set to 1 and the software reads the last byte.

5、 When the slave detects the STOP bit on I2C bus, set I2C_STS1.STOPF to 1, and if the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. The software clears the I2C_STS1.STOPF bit by reading the I2C_STS1 register before writing the I2C_CTRL1 register (see EV4 in the following figure).

Figure 23-4 Slave receiver transfer sequence diagram



Instructions：

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.

2. EV2: I2C_STS1.RXDATNE =1, reading DAT will clear this event.

3. EV4: I2C_STS1.STOPF=1, reading STS1 and then writing the CTRL1 register will clear this event.

Note: a)EV1 event prolongs the time when SCL is low until the end of the corresponding software sequence.

b) The software sequence of EV2 must be completed before the end of the current byte transmission.

23.3.2.6 I2C master transmission mode

In the master mode, the I2C interface starts data transmission and generates a clock signal. Serial data transmission always starts with a start condition and ends with a stop condition. When the START condition is generated on the bus through the start bit, the device enters the master mode.

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When sending data to I2C bus in master mode, the software should operate as follows:

1. First, enable the I2C peripheral clock, and configure the clock-related registers in I2C_CTRL1 to ensure the correct I2C timing. When these two steps are completed, I2C runs in the slave mode by default, waiting for receiving the start bit and address.
2. When BUSY=0, I2C_CTRL1.STARTGEN bit set to 1, and the I2C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE bit set to "1").
3. Once the start condition is issued, I2C hardware will set I2C_STS1.STARTBF bit(START bit flag)and then enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bit address bit or a 10-bit address bit with an address header to the I2C_DAT register to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I2C starts sending addresses or address headers to I2C bus.

   In 10-bit address mode, sending a header sequence will generate the following events:

- I2C_STS1.ADDR10F bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, and then writes the second address byte into the DAT register.
- I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, followed by the STS2 register.

  Note: In the transmitter mode, the master device first sends the header byte (11110xx0) and then sends the lower 8 bits of the slave address. (where xx represents the highest 2 bits of the 10-bit address).

  In the 7-bit address mode, only one address byte needs to be sent out. Once the address byte is sent out:

- I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master device waits for reading the STS1 register once, followed by reading the STS2 register.

  Note: in the transmitter mode, when the master sends the slave address, set the lowest bit to "0".

  Note:In 7-bit address mode, don't set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bit or 10-bit address bit is sent, the I2C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1, if the I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated, and the software is cleared by reading the I2C_STS1 register and then the I2C_STS2 register I2C_STS1.ADDRF.
5. I2C enters the data transmission state. Because the shift register and the data register (I2C_DAT) are empty, the hardware sets the I2C_STS1.TXDATE bit (transmission data empty) to 1, and then the software writes the first byte of data to the I2C_DAT register, but because the byte written into the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit will not be cleared at this time. Once the shift register is not empty, I2C starts sending data to the bus.
6. During the transmission of the first byte, the software writes the second byte to I2C_DAT, and I2C_STS1.TXDATE is cleared at this time. At any time, as long as there is data waiting to be sent and the I2C_STS1.TXDATE bit is set to 1, the software can write a byte to the I2C_DAT register.
7. In the process of sending the penultimate byte, the software writes the last byte of data to I2C_DAT to clear the I2C_STS1.TXDATE flag bit. After that, there is no need to care about the status of the I2C_STS1.TXDATE bit.

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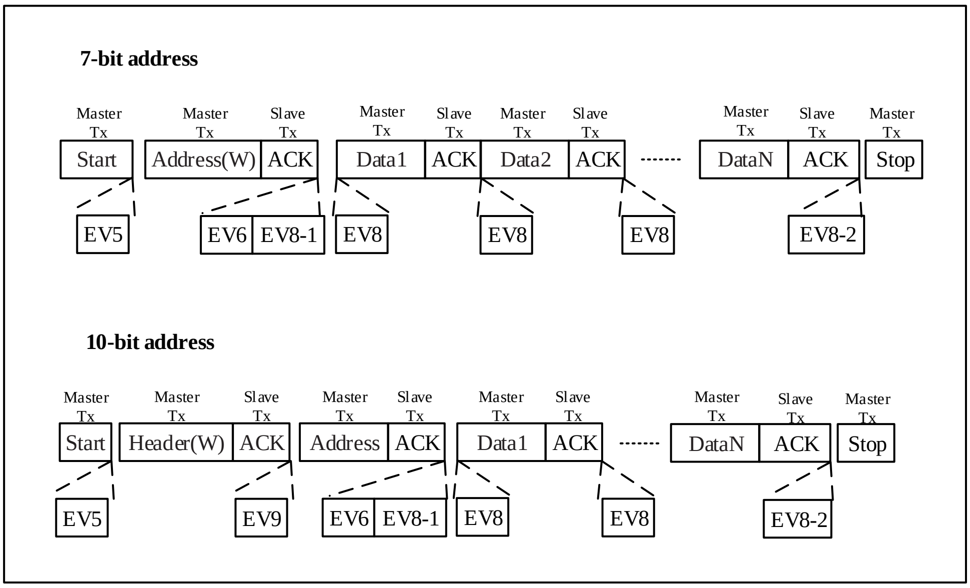
The I2C_STS1.TXDATE bit will be set after the penultimate byte is sent, and will be cleared when the stop bit (STOP) is sent.

8. After the last byte is sent, because the shift register and the I2C_DAT register are empty at this time, the I2C host sets the I2C_STS1.BSF bit (byte transmission end), and the I2C interface will keep SCL low before clearing the I2C_STS1.BSF bit. After reading I2C_STS1, writing to the I2C_DAT register will clear the I2C_STS1.BSF bit. The software sets the I2C_CTRL1.STOPGEN bit at this time to generate a stop condition, and then the I2C interface will automatically return to the slave mode (I2C_STS2.MSMODE bit is cleared).

Figure 23-5 Master transmitter transfer sequence diagram



Instructions：

1. EV5: I2C_STS1.STARTBF = 1, reading STS1 and writing the address to the DAT register will clear the event.
2. EV6: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
3. EV8_1: I2C_STS1.TXDATE = 1, shift register is empty, data register is empty, write DAT register.
4. EV8: I2C_STS1.TXDATE = 1, shift register is not empty, data register is empty, write to DAT register will clear the event.
5. EV8_2: I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1, request to set stop bit. These two events are cleared by the hardware when a stop condition is generated.
6. EV9: I2C_STS1.ADDR10F = 1, read STS1 and then write to DAT register to clear the event.

Note: a) EV5, EV6, EV9, EV8_1 and EV8_2 event prolonged the low SCL time until the end of the corresponding software sequence.

b) The software sequence of EV8 must be completed before the end of the current byte transfer.

c) When I2C_STS1.TXDATE or I2C_STS1.BSF bit is set, stop condition should be arranged when EV8_2 occurs.

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23.3.2.7 I2C master receiving mode

In master mode, software receiving data from I2C bus should follow the following steps:

1、 First, enable the I2C peripheral clock and configure the clock-related registers in I2C_CTRL1, in order to ensure that the correct I2C timing is output. After enabling and configuring, I2C runs in slave mode by default, waiting to receive the start bit and address.

2、 When BUSY=0, set the I2C_CTRL.STARTGEN bit, and the I2C interface will generate a start condition and switch to the master mode (I2C_STS2.MSMODE bit is set to 1).

3、 Once the start condition is issued, the I2C hardware sets I2C_STS1.STARTBF(start bit flag) and enters the host mode. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bits address or a 10-bits address with an address header to the I2C_DAT register, in order to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I2C begins to send the address or address header to the I2C bus.
In 10-bits address mode, sending a header sequence will generate the following events:

- The I2C_STS1.ADDR10F bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register, and then writes the second byte of address into the DAT register.
- The I2C_STS1.ADDRF bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register and the STS2 register in sequence.

Note: In the receiver mode, the master device sends the header byte (11110xx0) firstly, then sends the lower 8 bits of the slave address, and then resends a start condition followed by the header byte (11110xx1) (where xx represents the highest 2 digits of the 10-bits address).

In the 7-bits address mode, only one address byte needs to be sent, once the address byte is sent:

- The I2C_STS1.ADDRF bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device waits to read the STS1 register once, and then reads the STS2 register.

Note: In the receiving mode, the master device sets the lowest bit as '1' when sending the slave address.

4、 After the 7-bits or 10-bits address is sent, the I2C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. The software clears the I2C_STS1.ADDRF bit by reading the I2C_STS1 register and the I2C_STS2 register in sequence. If in the 10-bit address mode, software should set the I2C_CTRL1.STARTGEN bit again to regenerate a START. After the START is generated, the I2C_STS1.STARTBF bit will be set. The software should clear the I2C_STS1.STARTBF bit by reading I2C_STS1 firstly and then writing the address header to I2C_DAT, and then the address header is sent to the I2C bus, I2C_STS1.ADDRF is set to 1 again. The software should clear the I2C_STS1.ADDRF bit again by reading I2C_STS1 and I2C_STS2 in sequence.

5、 After sending the address and clearing the I2C_STS1.ADDRF bit, the I2C interface enters the host receiving mode. In this mode, the I2C interface receives data bytes from the SDA line and sends them to the DAT register through the internal shift register. Once the first byte is received, the hardware will set the I2C_STS1.RXDATNE bit (not empty flag bit of received data) to 1, and if the I2C_CTRL1.ACKEN bit is set to 1, an acknowledge pulse will be sent. At this time, the software can read the first byte from the I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. After that, as long as I2C_STS1.RXDATNE is

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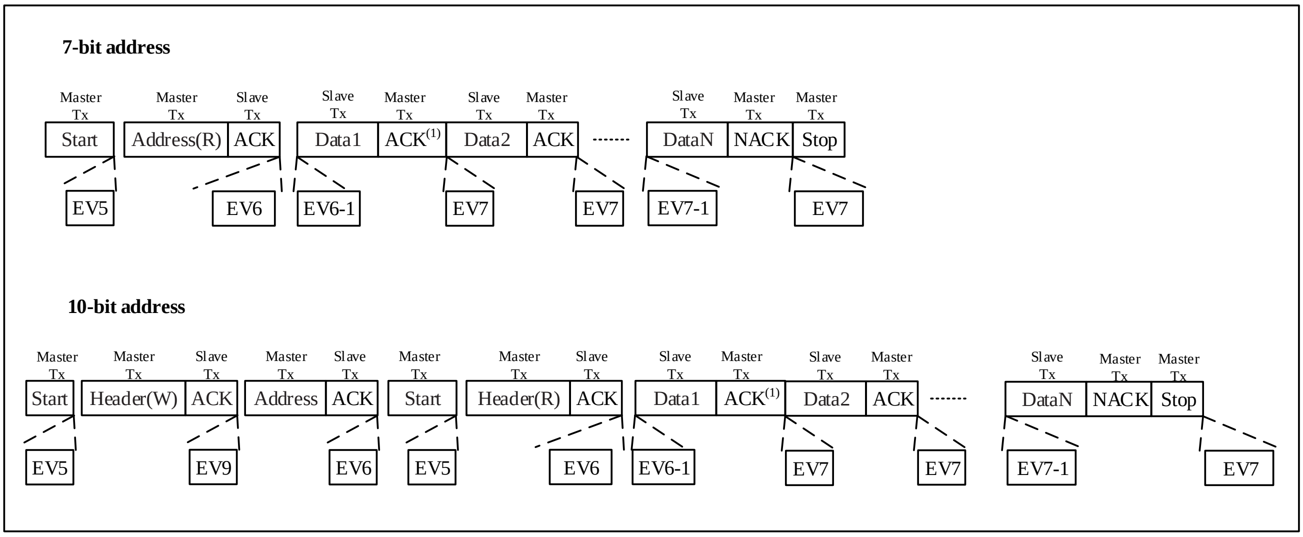
set to 1, the software can read a byte from the I2C_DAT register.

6、 The master device sends a NACK after receiving the last byte from the slave device. After receiving the NACK, the slave device releases the control of SCL and SDA lines; the master device can send a stop/restart condition. In order to generate a NACK pulse after receiving the last byte, the software should clear the I2C_CTRL1.ACKEN bit immediately after receiving the penultimate byte (N-1). In order to generate a stop/restart condition, the software must set the I2C_CTRL1.STOPGEN bit or I2C_CTRL1.STARTGEN to 1 after reading the penultimate data byte. This process needs to be completed before the last byte is received to ensure that the NACK is sent for the last byte.

7、 After the last byte is received, the I2C_STS1.RXDATNE bit is set to 1, and the software can read the last byte. Since I2C_CTRL1.ACKEN has been cleared to 0 in the previous step, I2C no longer sends ACK for the last byte, and generates a STOP bit after the last byte is sent.

Note: The above steps require the number of bytes N>1. If N=1, step 6 should be executed after step 4, and it needs to be completed before the reception of byte is completed.

Figure 23-6 Master receiver transfer sequence diagram



Instructions:

1. EV5: I2C_STS1.STARTBF=1, reading STS1 and then writing the address into the DAT register will clear this event.
2. EV6: I2C_STS1.ADDRF=1, reading STS1 and STS2 in sequence will clear this event. In the 10-bits master receiving mode, the I2C_CTRL1.STARTGEN should be set to 1 after this event.
3. EV6_1: There is no corresponding event flag, only suitable for receiving 1 byte. Just after EV6 (that is after clearing I2C_STS1.ADDRF), the generation bits for acknowledge and stop condition should be cleared.
4. EV7: I2C_STS1.RXDATNE=1, read the DAT register to clear this event.
5. EV7_1: I2C_STS1.RXDATNE =1, read the DAT register to clear this event. Set I2C_CTRL1.ACKEN=0 and I2C_CTRL1.STOPGEN=1.
6. EV9: I2C_STS1.ADDR10F=1, reading STS1 and then writing to the DAT register will clear this event.

Note:

a) If a single byte is received, it is NA.

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b) *EV5, EV6, and EV9 events extend the low level of SCL until the corresponding software sequence ends.*

c) *The EV7 software sequence shall be completed before the end of the current byte transmission.*

d) *The software sequence of EV6_1 or EV7_1 shall be completed before the ACK pulse of the current transmission byte.*

23.3.3 Error conditions description

I2C errors mainly include bus error, acknowledge error, arbitration loss, overload\ underload error. These errors may cause communication failure.

23.3.3.1 Acknowledge Failure (ACKFAIL)

The interface have a acknowledge bit is detected that does not match the expectation, it will occurs acknowledge fail error, I2C_STS1.ACKFAIL bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

When transmitter receives a NACK, The communication must be reset: Device in slave mode, hardware release the bus; Device in master mode, it must generate a stop condition from software.

23.3.3.2 Bus Error (BUSERR)

when address or data is transmissing,I2C interface receive external stop or start condition,it will happen a bus error, I2C_STS1. BUSERR bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

I2C device as master, the hardware does not release bus, as the same time it done not affect the current status of transfer,The current transfer will determined by software whether suspend.

I2C device as slave, when data is discarded in transmission and the bus releases by hardware, it will have two situation: If an error start condition is detected, the slave device considers a restart condition and waits for an address or a stop condition. If an error stop condition is detected, the slave device operates as a normal stop condition and the hardware releases the bus.

23.3.3.3 Arbitration Lost (ARLOST)

The interface have arbitration lost is detected, hardware release the bus, it will occurs arbitration lost error, I2C_STS1.ARLOST bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

I2C interface will go to slave mode automatically(I2C_STS2.MSMODE bit is cleared). When the I2C interface lost the arbitration, in the same communication, it can not respond to its slave address, but it can respond when master win the bus retransmits a start signal.

23.3.3.4 Overrun/Underrun Error (OVERRUN)

In slave mode, disable clock extend prone to Overrun/Underrun Error:

When I2C interface is receiving data (I2C_STS1.RXDATNE=1, data have received in register), and I2C_DAT register still have previous byte has not been read, it will occurs an overrun error. In this situation, the last received data is discarded. And software should clear I2C_STS1.RXDATNE bit, transmitter retransmit last byte.

When I2C interface is sending data (I2C_STS1.TXDATE=1, new data have not sending to register), and I2C_DAT register still empty, it will occurs an underrun error. In this situation, the previous byte in the I2C_DAT register is sending repeatedly. And User make sure that in the event of an underrun error, the receiver discard repeatedly byte,

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and transmitter should update the I2C_DAT register at the specified time according to the I2C bus standard.

In sending the first byte, I2C_DAT register must be written after I2C_STS1.ADDRF bit is cleared and the before the first SCL rising edge. If cannot make sure do that, the first byte should be discard by receiver.

23.3.4 DMA application

DMA can generate a requests when transfer data register empty or full. DMA can oprate write data to I2C or read data from I2C reduce burden of CPU.

Before transfer current byte at the end DMA requests must be answered. If set the DMA channel transfer data is done, DMA will send EOT(End Of Transmission) to I2C, and ocurrs a interrupt when enable interrupt bit.

In the master transfer mode, in EOT interrupt handler DMA request need to be disbale, and set stop condition after waiting for I2C_STS1.BSF event.

In the master receive mode, the data of received is great than or equal to 2, DMA will send a hardware signal EOT_1 in DMA transmission(byte number-1). If set I2C_CTRL2.DMALAST bit, when hardware have send the EOT_1 next byte it will send a NACK automatically. The user can set a stop condition in the interrupt handler after the DMA transfer is completed if interrupt enable.

23.3.4.1 Transmit process

If use the DMA mode need set the I2C_CTRL2.DMAEN bit. When I2C_STS1.TXDATE bit is set, the data will send to I2C_DAT from storage area by the DMA. DMA assign a channle for I2C transmission, (x is the channel number) the following step must be opreate:

1. In the DMA_PADDRx register set the I2C_DAT register address. Data will be send to address in every I2C_STS1.TXDATE event.
2. In the DMA_MADDRx register set the memory address. Data will send to I2C_DAT address in every I2C_STS1.TXDATE event.
3. In the DMA_TXNUMx register set the number of need to be transferred.In every I2C_STS1.TXDATE event this number-1 until 0.
4. In the DMA_CHCFGx register set PRIOLVL[1:0] bit to configure the priority of channel.
5. In the DMA_CHCFGx register set DIR bit to configure when ocurrs an interrupt whether send a half data or all completed.
6. In the DMA_CHCFGx register set CHEN bit to enable transfer channel.
7. When DMA transfer data is done, DMA need send a EOT/EOT_1 signal to I2C indicate this transfer is done. If interrupt is enable, DMA ocurrs a interrrupt.

Note: if DMA is used for transmission, do not set I2C_CTRL2.BUFINTEN bit.

23.3.4.2 Receive process

If use DMA mode need set I2C_CTRL2.DMAEN bit. When data byte is received,DMA will send I2C data to storage area, set DMA channel for I2C reception. The following steps must be opreate:

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1. In DMA_PADDRx register set the address of the I2C_DAT register. In every I2C_STS1.RXDATEN event, data will send from address to storage area.
2. In DMA_MADDRx register set the memory area address. In every I2C_STS1.RXDATEN event,data will send from I2C_DAT register to storage area.
3. In DMA_TXNUMx register set the number of need to be transferred. In every I2C_STS1.RXDATEN event the number-1 until 0.
4. In DMA_CHCFGx register set PRIOLVL[0:1] to configure the priority of channel.
5. In DMA_CHCFGx register clear DIR to configure when ocurrs a interrupt request whether received half data or all data is received.
6. In the DMA_CHCFGx register set CHEN bit to activate the channle.
7. When DMA tansfer data is done, DMA need to send EOT/EOT_1 signal to I2C indicate this transfer is done, if interrupt is enbale, DMA ocurrs a interrupt.

Note: If DMA is used for receiving, do not set I2C_CTRL2.BUFINTEN bit.

23.3.5 Packet error check

Setting the I2C_CTRL1.PECEN bit to 1 enables the PEC function. PEC uses CRC-8 algorithm to calculate all information bytes including address and read/write bits.it can improve the reliability of communication. The CRC-8 polynomial uses by the PEC calculator is $C(x) = x^8 + x^2 + x + 1$.

In transmit mode, software sets I2C_CTRL1.PEC transfer bit in the last I2C_STS1.TXDATE event, and then PEC will be transferred in the last byte. In receiving mode, software sets I2C_CTRL1.PEC transfer bit after the last I2C_STS1.RXDATNE event, and then receives the PEC byte and compares the received PEC byte to the internally calculated PEC value. If it is not equal to the internally calculated PEC value, the receiver needs to send a NACK. If it is host receiver mode, NACK will be sent after PEC regardless of the calculated result. It should pay attention that I2C_CTRL1.PEC bit has to be set before receiving.

If both DMA and PEC calculator are activated, I2C will automatically send or check the PEC value.

In transfer mode, when I2C interface receives EOT signal from DMA controller, it will automatically send PEC following the last byte. In receiving mode, when I2C interface receives an EOT_1 signal from DMA, it will automatically consider the next byte as PEC and compare it with the internally calculated PEC. It will happen a DMA request after receiving PEC.

In order to allow intermediate PEC transfer, I2C_CTRL2.DMALAST bit is used to determine whether it is the last DMA transfer. And if it does the last DMA request of the master receiver, NACK will be sent automatically after receiving the last byte.

When arbitration is lost, PEC calculation is invalid.

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23.3.6 SMBus

23.3.6.1 Introduction

The System Management Bus(SMBus or SMB) is a dual-wire bus interface. Using SMBus can communicate with other device or other parts of the system, it able to commnicate with multiple devices without other independent control wire. SMBus base on I2C commincate standard. SMBus have a control bus for system and power management related tasks. If you want browse more information, please refer to the SMBus specification V2.0(http://smbus.org/specs/).

SMBus have three types of device standard.

- Master: device send command,generate clocks and stop transmmissions;
- Slave: device receive,respond to commands;
- Host: system have only one host. a device provides a master to system CPU. host have function of master and slave, it support SMBus alert protocol.

SMBus is a subset of the data transmission format of the I2C specification.

Similarities between SMBus and I2C:

- Both bus protocols contain of 2 wires (a clock wire SCL and a data wire SDA), with an optional SMBus alert wire.
- The data format is similar. SMBus data format is similar to 7-bit address format of I2C(See Figure 23-2).
- Both are master-slave communication modes, and the master device provides the clock.
- Both support multi master

Differences between SMBus and I2C:

Table 23-1 Comparison between SMBus and I2C

SMBus	I^2C
Maximum transmission speed 100kHz	Maximum transmission speed 1MHz
Minimum transmission speed 10kHz	No minimum transmission speed
Low clock timeout 35ms	No clock timeout
Fixed logic level	VDD determined logic level
Different address types (reserved, dynamic, etc.)	7-bit, 10-bit, and broadcast call slave address types
Different bus protocols (quick command, call handling, etc.)	No bus protocol

23.3.6.2 SMBus usage

SMBus uses the system management bus to meet lightweight communication requirements. In general, SMBus is commonly used on the computer motherboard. It is mainly used to transmit ON/OFF instructions for power unit and provide a control bus for system and power management-related tasks.

23.3.6.3 Device identification

On the SMBus, as a slave have a only address for any device, named slave address.

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In order to distribute addres for each devices, it must have a unique device identifier(UDID) to distinguish devices.

23.3.6.4 Bus protocol

SMBus specification include eight bus protocols. If want browse the details on protocols or SMBus address types,it can refer to the SMBus specification v2.0(http://smbus.org/specs/). User’s software can device what protocols are implemented.

Every packet through the SMBus complies with the SMBus protocol predefined format. SMBus is a subset of the data transfer format of I2C specification. As long as an I2C device can be accessed through one of the SMBus protocols, it is considered to be SMBus compliant.

Note: SMBus does not support Quick command protocol.

23.3.6.5 Address resolution protocol

The SMBus resolves address conflicts by dynamically assigning a new unique address to each slave device. This is the address resolution protocol(ARP) .

Any master device can connected bus to access all devices.

SMBus physical layer arbitration enable to distribute addresses.When device power on, the device’s distribute address is not change, the protocol allows address retain when device power off.

When address is distributed, there is no extra SMBus packaging cost(the cost time that access distribute address device and access fixed address device is same).

23.3.6.6 Timeout function

A kind of feature related to timeout on SMBus: if it has taken too long time during the communication, it automatically resets the device. This is the reason why SMBus has a minimum transmission rate limitation -- to prevent the bus from locking up for a long time after the timeout occurs. I2C bus is essentially a "DC" bus, that is to say, if the slave is executing some subroutines and cannot respond in time while the master is accessing the slave, it can hold the clock. That can remind the host that the slave is busy but does not want to give up the current communication. This session can continue after the current task of the slave is over. I2c doesn’t have a maximum limitation for the delay, but it is limited to 35ms in the SMBus system. According to the SMBus protocol, if a session takes too long, it means something is wrong with the bus, and all devices should be reset to eliminate this state. Like this, the slave device is not allowed to pull the clock down for too long. I2C_STS1.TIMOUT bit indicates the status of this feature.

23.3.6.7 SMBus alter mode

SMBus offer a optional interrupt signal SMBALERT(like SCL and SDA,is a wired-and signal) that devices uses to extend their control capabilities at expense of a pin. SMBus broadcast call address often combine with SMBALERT. There is 2 bytes message about SMBus.

A device which only has slave function can set I2C_CTRL1.SMBALERT bit to indicate it want to communicate with host. The host handles the interrupt and accesses all SMBALERT devices through the ARA (Alert Response Address, address value 0001100x). Only those devices that pull SMBALERT low can respond to ARA. This state is identified by the I2C_STS1.SMBALERT. The 7-bit device address provided from the sending device is placed on the 7 most significant bits of the byte, the eighth bit can be either '0' or '1'.

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When more than one device's SMBALERT is low, the highest priority(The smaller the address, the higher the priority) can win bus communication through the standard arbitration during address transmission. If confirming the slave address, device's SMBALERT is no longer pulled low. If message transmitted completely,device's SMBALERT still is low,it mean host will read ARA again. The host can periodically access the ARA when the SMBALERT signal is not used.

23.3.6.8 SMBus communication process

The communication process on SMBus is similar to that on I2C.To use the SMBus mode, you need to configure SMBus specific registers in the program, respond and process SMBus specific flag, to implement the upper-layer protocols described in the SMBus manual.

1. At first, set I2C_CTRL1.SMBMODE bit, and configure I2C_CTRL1.SMBTYPE bit and I2C_CTRL1.ARPEN bit according to the application requirements. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=0, use the default address of the SMB device. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=1, use the SMB master header field.
2. In order to support ARP (I2C_CTRL1.ARPEN=1), in SMBus host mode (I2C_CTRL1.SMBTYPE=1), software needs to respond to the I2C_STS2.SMBHADDR bit (in SMBus slave mode, respond to I2C_STS2.SMBDADDR bit) and implement the functions according to the ARP protocol.
3. To support the SMBus warning mode, software should respond to the I2C_STS1.SMBALERT bit and implement the corresponding functions.

23.4 Debug mode

When the microcontroller enters the debug mode (Cortex-M4 core is in the stop state), configure the DBG_CTRL.I2CxSMBUS_TIMEOUT bit in the DBG module, Select SMBUS timeout to continue normal work or stop. See section 29.3.2 for details.

23.5 Interrupt request

All I2C interrupt requests are listed in the following table.

Table 23-2 I²C interrupt request

Interrupt function	Interrupt event	Event flag	Set control bit
I2C event interrupt	Start bit sent (master)	STARTBF	EVTINTEN
	Address sent (master) or address matched (slave)	ADDRF	
	10-bit header sent (master)	ADDR10F	
	Received stop (slave)	STOPF	
	Data byte transfer completed.	BSF	
	Receive buffer is not empty.	RXDATNE	EVTINTEN and BUFINTEN
	Send buffer is empty.	TXDATE	
I2C error interrupt	Bus error	BUSERR	ERRINTEN
	Lost arbitration (master)	ARLOST	
	Acknowledge fail	ACKFAIL	

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Interrupt function	Interrupt event	Event flag	Set control bit
	Overrun/underrun	OVERRUN	
	PEC error	PECERR	
	Timeout /Tlow error	TIMOUT	
	SMBus Alert	SMBALERT	

Note: 1. STARTBF, ADDRF, ADDR10F, STOPF, BSF, RXDATNE and TXDATE are merged into the event interrupt channel through logical OR.

2. BUSERR, ARLOST, ACKFAIL, OVERRUN, PECERR, TIMEOUT and SMBALERT are merged into the error interrupt channel through logical OR.

23.6 I2C registers

These peripheral registers can be operated by half word (16 bits) or word (32 bits)

23.6.1 I2C register overview

Table 23-3 I2C register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	I2C_CTRL1	Reserved																SWRESET	Reserved	SMBALERT	PEC	ACKPOS	ACKEN	STOPGEN	STARTGEN	NOEXTEND	GCEN	PECEN	ARPEN	SMBTYPE	Reserved	SMBMODE	EN
	Reset Value																	0		0	0	0	0	0	0	0	0	0	0	0		0	0
004h	I2C_CTRL2	Reserved																			DMALAST	DMAEN	BUFINTEN	EVTINTEN	ERRINTEN	Reserved		CLKFREQ[5:0]					
	Reset Value																				0	0	0	0	0			0	0	0	0	0	0
008h	I2C_OADDR1	Reserved																ADDRMODE	Reserved	Reserved				ADDR[9:8]		ADDR[7:1]							ADDR0
	Reset Value																	0						0	0	0	0	0	0	0	0	0	0
00Ch	I2C_OADDR2	Reserved																								ADDR2[7:1]							DUALEN
	Reset Value																									0	0	0	0	0	0	0	0
010h	I2C_DAT	Reserved																								DATA[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	I2C_STS1	Reserved																SMBALERT	TIMOUT	Reserved	PECERR	OVERRUN	ACKFAIL	ARLOST	BUSERR	TXDATE	RXDATNE	Reserved	STOPF	ADDR10F	BSF	ADDRF	STARTBF
	Reset Value																	0	0		0	0	0	0	0	0	0		0	0	0	0	0
018h	I2C_STS2	Reserved																PECVAL[7:0]								DUALFLAG	SMBHADDR	SMBDADDR	GCALLADDR	Reserved	TRF	BUSY	MSMODE
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
01Ch	I2C_CLKCTRL	Reserved																FSMODE	DUTY	Reserved		CLKCTRL[11:0]											
	Reset Value																	0	0			0	0	0	0	0	0	0	0	0	0	0	0
020h	I2C_TMRISE	Reserved																										TMRISE[5:0]					

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	Reset Value		0	0	0	0	0	0

23.6.2 I2C Control register 1 (I2C_CTRL1)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW RESET	Reserved	SMB ALERT	PEC	ACK POS	ACKEN	STOP GEN	START GEN	NO EXTEND	GCEN	PECEN	ARPEN	SMB TYPE	Reserved	SMB MODE	EN
rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

Bit field	Name	Description
15	SWRESET	Software reset Make sure the I2C bus is idle before resetting this bit. 0:I2C not reset; 1:I2C reset. *Note: This bit can be used when the I2C_STS2.BUSY bit is set to 1 and no stop condition is detected on the bus.*
14	Reserved	Reserved, the reset value must be maintained.
13	SMBALERT	SMBus alert It can be set or cleared by software. When I2C_CTRL1.EN=0, it will be cleared by hardware. 0: SMBAlert pin go high. The response address header is followed by the NACK signal; 1: SMBAlert pin go low. The response address header is followed by the ACK signal.
12	PEC	Packet error checking It can be set or cleared by software. It will be cleared by hardware when PEC has been transferred, or by start or stop condition, or when I2C_CTRL1.EN=0. 0: No PEC transfer 1: PEC transfer. *Note: When arbitration is lost, the calculation of PEC is invalid.*
11	ACKPOS	Acknowledge/PEC Position（for data reception） It can be set or cleared by software. Or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: I2C_CTRL1.ACKEN bit determines whether to send an ACK to the byte currently being received; I2C_CTRL1.PEC bit indicates that the byte in the current shift register is PEC. 1: I2C_CTRL1.ACKEN bit etermines whether to send an ACK to the next received byte; I2C_CTRL1.PEC bit indicates that the next byte received in the shift register is PEC. *Note：* *ACKPOS bit can only be used in 2-byte receiving configuration and must be configured before receiving data.* *For the second byte of NACK, the I2C_CTRL1.ACKEN bit must be cleared after the I2C_STS1.ADDRF bit is cleared.* *To detect the PEC of the second byte, the I2C_CTRL1.PEC bit must be set after the ACKPOS bit is configured and when the ADDR event is extended.*
10	ACKEN	Acknowledge enable

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Bit field	Name	Description
		It can be set or cleared by software. Or when I2C_CTRL1.EN equals to 0, it will be cleared by hardware. 0：No acknowledge send; 1：Send an acknowledge after receiving a byte
9	STOPGEN	Stop generation It can be set or cleared by software. Or it will be cleared by hardware when a stop condition is detected. Or it will be set by hardware when SMBus timeout error is detected,. In the master mode: 0：No stop condition generates; 1：Generate a stop condition. In the slave mode: 0：No stop condition generates; 1：Release SCL and SDA lines after the current byte. *Note：When the STOPGEN, STARTGEN or PEC bit is set, the software should not take any write operation to I2C_CTRL1 until this bit is cleared by hardware. Otherwise, the STOPGEN, STARTGEN or PEC bits may be set twice.*
8	STARTGEN	Start generation It can be set or cleared by software. Or it will be cleared by hardware when the start condition is transferred or I2C_CTRL1.EN=0. 0: No start condition generates; 1: Generate a start conditions.
7	NOEXTEND	Clock extending disable (Slave mode) This bit determines whether to pull SCL low when the data is not ready(I2C_STS1.ADDRF or I2C_STS1.BSF flag is set) in slave mode, and is cleared by software reset 0: Enable Clock extending. 1: Disable Clock extending.
6	GCEN	General call enable 0：Disable General call. not respond(NACK) to the address 00h; 1：Enable General call. respond(ACK) the address 00h.
5	PECEN	PEC enable 0：Disable PEC module; 1：Enable PEC module.
4	ARPEN	ARP enable 0: Disable ARP； 1: Enable ARP. If I2C_CTRL1.SMBTYPE=0, the default address of SMBus device is used. If I2C_CTRL1.SMBTYPE=1, the host address of SMBus is used.
3	SMBTYPE	SMBus type 0: Device 1: Host
2	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
1	SMBMODE	SMBus mode 0：I2C mode； 1：SMBus mode.
0	EN	I2C Peripheral enable 0：Disable I2C module; 1：Enable I2C module *Note: If this bit is cleared when the communication is in progress, the I2C module is disabled and returns to the idle state after the current communication ends,all bits will be cleared.* *In master mode,this bit must never be cleared until the communication has ended.*

23.6.3 I2C Control register 2 (I2C_CTRL2)

Address offset: 0x04

Reset value: 0x0000

15:13	12	11	10	9	8	7:6	5:0
Reserved	DMA LAST	DMA EN	BUFINT EN	EVTINT EN	ERRINT EN	Reserved	CLKFREQ[5:0]
	rw	rw	rw	rw	rw		rw

Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained.
12	DMALAST	DMA last transfer 0: Next DMA EOT is not the last transfer 1: Next DMA EOT is the last transfer *Note: This bit is used in the master receiving mode, so that a NACK can be generated when data is received for the last time.*
11	DMAEN	DMA requests enable 0: Disable DMA 1: Enable DMA
10	BUFINTEN	Buffer interrupt enable 0: When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE=1, any interrupt is not generated. 1: If I2C_CTRL2.EVTINTEN= 1,When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE= 1, interrupt will be generated.
9	EVTINTEN	Event interrupt enable 0：Disable event interrupt； 1：Enable event interrupt This interrupt is generated when: I2C_STS1.STARTBF = 1 (Master) I2C_STS1.ADDR F = 1 (Master/Slave) I2C_STS1.ADD10F = 1 (Master) I2C_STS1.STOPF = 1 (Slave) I2C_STS1.BSF = 1 with no I2C_STS1.TXDATE or I2C_STS1.RXDATNE event

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Bit field	Name	Description
		I2C_STS1.TXDATE = 1 if I2C_CTRL2.BUFINTEN = 1 I2C_STS1.RXDATNE = 1 if I2C_CTRL2.BUFINTEN = 1
8	ERRINTEN	Error interrupt enable 0：Disable error interrupt； 1：Enable error interrupt. This interrupt is generated when: I2C_STS1.BUSERR = 1； I2C_STS1.ARLOST = 1； I2C_STS1.ACKFAIL = 1； I2C_STS1.OVERRUN = 1； I2C_STS1.PECERR = 1； I2C_STS1.TIMOUT = 1； I2C_STS1.SMBALERT = 1.
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	CLKFREQ[5:0]	I2C Peripheral clock frequency CLKFREQ[5:0] should be the APB clock frequency to generate the correct timming. 000000：Disable 000001：Disable 000010：2MHz 000011：3MHz ... 100100：36MHz 100101~111111：Disable.

23.6.4 I2C Own address register 1 (I2C_OADDR1)

Address offset: 0x08

Reset value: 0x0000

15	14	13:10	9:8	7:1	0
ADDR MODE	Reserved	Reserved	ADDR[9:8]	ADDR[7:1]	ADDR0
rw			rw	rw	rw

Bit field	Name	Description
15	ADDRMODE	Addressing mode (slave mode) 0: 7-bit slave address 1: 10-bit slave address
14	Reserved	Must always be kept as' 1' by the software.
13:10	Reserved	Reserved, the reset value must be maintained.
9:8	ADDR[9:8]	Interface address 9~8 bits of the address. *Note: don't care these bits in 7-bit address mode*

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Bit field	Name	Description
7:1	ADDR[7:1]	Interface address 7~1 bits of the address.
0	ADDR0	Interface address 0 bit of the address. *Note: don't care these bits in 7-bit address mode*

23.6.5 I2C Own address register 2 (I2C_OADDR2)

Address offset: 0x0C

Reset value: 0x0000

15 ... 8	7 ... 1	0
Reserved	ADDR2[7:1]	DUALEN
	rw	rw

Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:1	ADDR2[7:1]	Interface address 7~1 bits of address in dual address mode.
0	DUALEN	Dual addressing mode enable 0: Disable dual address mode, only OADDR1 is recognized; 1: Enable dual address mode, both OADDR1 and OADDR2 are recognized. *Note: Valid only for 7-bit address mode*

23.6.6 I2C Data register (I2C_DAT)

Address offset: 0x10

Reset value: 0x0000

15 ... 8	7 ... 0
Reserved	DATA[7:0]
	rw

Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	DATA[7:0]	8-bit data register Send or receive data buffer. *Note: In the slave mode, the address will not be copied into the data register;* *Note: if* I2C_STS1.*TXDATE =0, data can still be written into the data register;* *Note: If the ARLOST event occurs when processing the ACK pulse, the received byte will not be copied into the data register, so it cannot be read.*

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23.6.7 I2C Status register 1 (I2C_STS1)

Address offset: 0x14

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMB ALERT	TIM OUT	Reserved	PEC ERR	OVER RUN	ACK FAIL	AR LOST	BUS ERR	TXDATE	RXDAT NE	Reserved	STOPF	ADDR10F	BSF	ADDRF	START BF
rc_w0	rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	r	r		r	r	r	r	r

Bit field	Name	Description
15	SMBALERT	SMBus alert Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No SMBus alert(host mode) or no SMB alert response address header sequence(slave mode); 1: SMBus alert event is generated on the pin(host mode) or receive SMBAlert response address(slave mode)
14	TIMOUT	Timeout or Tlow error Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Timeout error; 1: A timeout error occurred Error in the following cases: ■ SCL has kept low for 25ms (Timeout). ■ Master cumulative clock low extend time more than 10 ms (Tlow:mext). ■ Slave cumulative clock low extend time more than 25 ms (Tlow:sext). Timeout in slave mode: slave device resets the communication and hardware frees the bus. Timeout in master mode: hardware sends the stop condition.
13	Reserved	Reserved, the reset value must be maintained.
12	PECERR	PEC Error in reception Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No PEC error 1: PEC error: receiver will returns NACK Whether the I2C_CTRL1.ACKEN bit is enabled
11	OVERRUN	Overrun/Underrun Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Overrun/Underrun 1: Overrun/Underrun Set by hardware in slave mode when I2C_CTRL1.NOEXTEND=1, and when receiving a new byte in receiving mode, if the data within DAT register has not been read yet, over-run occurs,the new received byte will be lost.When transferring a new byte in transfer mode, but there is not new data that has not been written in DAT register, under-run occurs which leads that the same byte will be send twice.

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Bit field	Name	Description
10	ACKFAIL	Acknowledge failure Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No acknowledge failed; 1: Acknowledge failed.
9	ARLOST	Arbitration lost (master mode) Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No arbitration lost; 1: Arbitration lost. When the interface loses control of the bus to another host, the hardware will set this bit to '1', and the I2C interface will automatically switch back to slave mode (I2C_STS2.MSMODE=0). *Note: In SMBUS mode, the arbitration of data in slave mode only occurs in the data stage or the acknowledge transfer interval (excluding the address acknowledge).*
8	BUSERR	Bus error Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No start or stop condition error 1: Start or stop condition error
7	TXDATE	Data register empty (transmitters) Writing data to DAT register by software can clear this bit; Or after a start or stop condition occurs, or automatically cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is not empty; 1: Data register is empty. When sending data, this bit is set to' 1' when the data register is empty, and it is not set at the address sending stage. If a NACK is received, or the next byte to be sent is PEC(I2C_CTRL1.PEC=1), this bit will not be set. *Note: After the first data to be sent is written, or data is written when BSF is set, the TXDATE bit cannot be cleared, because the data register is still empty.*
6	RXDATNE	Data register not empty(receivers) This bit is cleared by software reading and writing to the data register, or cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is empty; 1: Data register is not empty. During receiving data, this bit is set to' 1' when the data register is not empty, and it is not set at the address receiving stage. RXDATNE is not set when the ARLOST event occurs. *Note: When BSF is set, the RXDATNE bit cannot be cleared when reading data, because the data register is still full.*
5	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
4	STOPF	Stop detection (slave mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No stop condition is detected; 1: Stop condition is detected. After a ACK, the hardware sets this bit to' 1' when the slave device detects a stop condition on the bus. *Note: I2C_STS1.STOPF bit is not set after receiving NACK.*
3	ADDR10F	10-bit header sent (Master mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No ADD10F event; 1: Master has sent the first address byte. In 10-bit address mode, when the master device has sent the first byte, the hardware sets this bit to' 1'. *Note: After receiving a NACK, the I2C_STS1.ADDR10F bit is not set.*
2	BSF	Byte transfer finished After the software reads the STS1 register, reading or writing the data register will clear this bit; Or after sending a start or stop condition in sending mode, or when I2C_CTRL1.EN=0, this bit is cleared by hardware. 0：Byte transfer does not finish. 1：Byte transfer finished. When I2C_CTRL1.NOEXTEND =0, the hardware sets this bit to' 1' in the following cases: In receiving mode, when a new byte (including ACK pulse) is received and the data register has not been read (I2C_STS1.RXDATNE=1).In sending mode, when a new data is to be transmitted and the data register has not been written with the new data (I2C_STS1.TXDATE=1). *Note: After receiving a NACK, the BSF bit will not be set.* *If the next byte to be transferred is PEC (I2C _STS2.TRF is' 1' and I2C_CTRL1.PEC is' 1'), the BSF bit will not be set.*
1	ADDRF	Address sent (master mode) / matched (slave mode) After the STS1 register is read by software, reading the STS2 register will clear this bit, or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: Address mismatch or no address received(slave mode) or Address sending did not end(master mode); 1: Received addresses matched(slave mode) or Address sending ends(master mode) In master mode: In 7-bit address mode, this bit is set to' 1' after receiving the ACK of the address.In 10-bit address mode, this bit is set to' 1' after receiving the ACK of the second byte of the address. In slave mode:

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Bit field	Name	Description
		Hardware sets this bit to' 1' (when the corresponding setting is enabled) when the received slave address matches the content in the OADDR register, or a general call or SMBus device default address or SMBus host or SMBus alter is recognized. *Note: After receiving NACK, the I2C_STS1.ADDRF bit will not be set.*
0	STARTBF	Start bit (Master mode) After the STS1 register is read by software, writing to the data register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: Start condition was not sent; 1: Start condition has been sent. This bit is set to' 1' when the start condition is sent.

23.6.8 I2C Status register 2 (I2C_STS2)

Address offset: 0x18

Reset value: 0x0002

15–8	7	6	5	4	3	2	1	0
PECVAL[7:0]	DUAL FLAG	SMBH ADDR	SMBD ADDR	GCALL ADDR	Reserved	TRF	BUSY	MS MODE
r	r	r	r	r		r	r	r

Bit field	Name	Description
15:8	PECVAL[7:0]	Packet error checking register Stores the internal PEC value When I2C_CTRL1.PECEN =1.
7	DUALFLAG	Dual flag(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: Received address matches the content in OADDR1; 1: Received address matches the content in OADDR2.
6	SMBHADDR	SMBus host header（Slave mode） Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: SMBus host address was not received; 1: when I2C_CTRL1.SMBTYPE=1 and I2C_CTRL1.ARPEN=1, SMBus host address is received.
5	SMBDADDR	SMBus device default address（Slave mode） Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: The default address of SMBus device has not been received; 1: when I2C_CTRL1.ARPEN=1, the default address of SMBus device is received.
4	GCALLADDR	General call address(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0.

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Bit field	Name	Description
		0: No general call address was received; 1: when I2C_CTRL1.GCEN=1, general call address was received.
3	Reserved	Reserved, the reset value must be maintained.
2	TRF	Transmitter/receiver After detecting the stop condition (I2C_STS1.STOPF=1), repeated start condition or bus arbitration loss (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0, the hardware clears it. 0: Data receiving mode; 1: Data transmission mode; At the end of the whole address transmission stage, this bit is set according to the R/W bit of the address byte.
1	BUSY	Bus busy Hardware clears this bit when a stop condition is detected. 0: No data communication on the bus; 1: Data communication on the bus. When detecting that SDA or SCL is low level, the hardware sets this bit to' 1'; *Note:This bit indicates the bus communication currently in progress, and this information is still updated when the interface is disabled (I2C_CTRL1.EN=0).*
0	MSMODE	Master/slave mode Hardware clears this bit when a stop condition is detected on the bus, arbitration is lost (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0. 0: In slave mode; 1: In master mode. When the interface is in the master mode (I2C_STS1.STARTBF=1), the hardware sets this bit;

23.6.9 I2C Clock control register (I2C_CLKCTRL)

Address offset: 0x1c

Reset value: 0x0000

Note: 1. F_{PCLK1} *is required to be an integer multiple of 10 MHz, so that a fast clock of 400KHz can be generated correctly.*

2. The CLKCTRL register can only be set when I^2C *is turned off (I2C_CTRL1.EN=0)*

15	14	13-12	11-0
FSMODE	DUTY	Reserved	CLKCTRL[11:0]
rw	rw		rw

Bit field	Name	Description
15	FSMODE	I2C master mode selection 0: I2C in standard mode(duty cycle defaults to 1/1); 1: I2C in fast mode(duty cycle can be configured).
14	DUTY	Duty cycle in fast mode 0：Tlow/Thigh = 2；

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Bit field	Name	Description
		1：Tlow/Thigh = 16/9
13:12	Reserved	Reserved, the reset value must be maintained.
11:0	CLKCTRL[11:0]	Clock control register in Fast/Standard mode (Master mode) This division factor is used to set the SCL clock in the master mode. ■ If duty cycle = Tlow/Thigh = 1/1: CLKCTRL = f_{PCLK1}(Hz)/100000/2 Tlow = CLKCTRL ×T_{PCLK1} Thigh = CLKCTRL ×T_{PCLK1} ■ If duty cycle = Tlow/Thigh = 2/1: CLKCTRL = f_{PCLK1}(Hz)/100000/3 Tlow = 2 ×CLKCTRL ×TPCLK1 Thigh = CLKCTRL ×T_{PCLK1} ■ If duty cycle = Tlow/Thigh = 16/9: CLKCTRL = f_{PCLK1}(Hz)/100000/25 Tlow = 16 ×CLKCTRL ×T_{PCLK1} Thigh = 9 ×CLKCTRL ×T_{PCLK1} For example, if f_{PCLK1}(Hz) = 8MHz, duty cycle = 1/1, CLKCTRL = 8000000/100000/2 = 0x28. *Note: 1. The minimum setting value is 0x04 in standard mode and 0x01 in fast mode;* *2.* $T_{high}= T_{r(SCL)}+T_{w(SCLH)}$*. See the definitions of these parameters in the data sheet for details.* *3.* $T_{low}= T_{f(SCL)}+T_{w(SCLL)}$*, see the definitions of these parameters in the data sheet for details;* *4. These delays have no filters;*

23.6.10 I2C Rise time register (I2C_TMRISE)

Address offset: 0x20

Reset value: 0x0002

Note: The I2C_TMRISE register function is only valid in master mode. changed when I2C is disabled (I2C_CTRL1.EN=0).

15–6	5–0
Reserved	TMRISE[5:0]
	rw

Bit field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5:0	TMRISE[5:0]	Maximum rise time in fast/standard mode (master mode). These bits must be set to the maximum SCL rising time given in the I2C bus specification, and incremented step is 1. For example, the maximum allowable SCL rise time in standard mode is 1000ns. if the value in I2C_CTRL2.CLKFREQ [5:0] is equal to 0x08 and TPCLK1=125ns ,09h(1000ns/125 ns + 1) must be written in TMRISE[5:0] ,. If the result is not an integer, write the integer part to TMRISE[5:0] to ensure the t_{HIGH} parameter.

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24 Universal synchronous asynchronous receiver transmitter (USART)

24.1 Introduction

USART is a full-duplex universal synchronous/asynchronous serial transceiver module. This interface is a highly flexible serial communication device that can perform full-duplex data exchange with external devices.

The USART has programmable transmit and receive baud rates and can communicate continuously using DMA. It also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smart card asynchronous protocol, IrDA SIR ENDEC function, and hardware flow control function.

24.2 Main features

- Full-duplex operation
- Single-wire half-duplex operation
- Baud rate generator, the highest baud rate can reach 3.375Mbit/s
- Support serial data frame structure with 8 or 9 data bits, 1 or 2 stop bits
- Generation and checking of supported parity bits
- Support hardware flow control: RTS flow control and CTS flow control
- Support DMA receiving and sending
- Support multi-processor communication mode, can enter mute mode, wake up by idle detection or address mark detection
- Synchronous mode, allowing users to control bidirectional synchronous serial communication in master mode
- Comply with ISO7816-3 standard, support smart card asynchronous protocol
- IrDA SIR ENDEC function: IrDA normal mode and IrDA low power mode
- LIN (Local Area Network) mode
- Support data overflow error detection, frame error detection, noise error detection, parity error detection
- Interrupt requests include: transmit data register empty, CTS flag, transmit complete, receive data ready to read, data overflow detected, idle line detected, parity error, LIN break frame detection, noise flag/overflow error/frame error in multi-buffer communication

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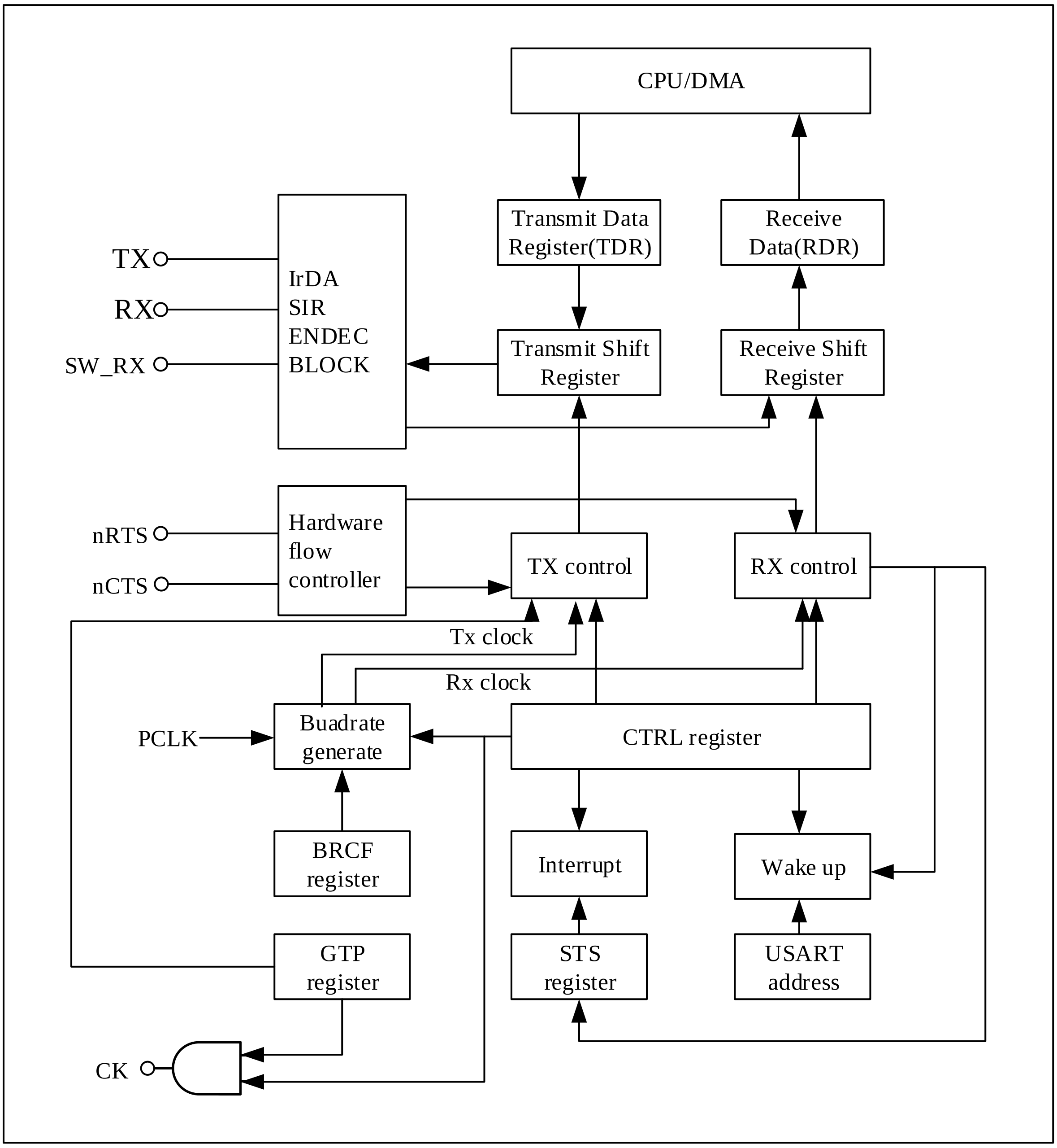
24.3 Functional block diagram

Figure 24-1 USART block diagram



24.4 Function description

As shown in the Figure 24-1, the bidirectional communication of any USART needs to use the RX and TX pins of the external connection. Among them, TX is the output pin for serial data transmission. When the transmitter is active and not sending data, the TX pin is pulled high. When the transmitter is inactive, the TX pin reverts to the I/O port configuration. RX is an input pin for serial data reception, data is recovered by oversampling technique.

The data packets of serial communication are transmitted from the sending device to the RX interface of the receiving

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device through its own TX interface, and the bus is in an idle state before sending or receiving. Frame format is: 1 start bit + 8 or 9 data bits (least significant bit first) + 1 parity bit (optional) + 0.5,1,1.5 or 2 stop bit.

Use the fractional baud rate generator to configure transmit and receive baud rates.

According to the block diagram, when using the hardware flow control mode, the nRTS output and nCTS input pins are required. When the USART receiver is ready to receive new data, nRTS becomes low level. If nCTS is valid (pulled to a low level), the next data is sent, otherwise the next frame of data is not sent.

When using synchronous mode, the CK pin is required. The CK pin is used for clock output for synchronous transfers. Clock phase and polarity are software programmable. During the start and stop bits, the CK pin does not output clock pulses.The CK pin is also used when using smart card mode.

24.4.1 USART frame format

The start bit of the data frame is low.

The word length can be selected as 8 or 9 bits by programming the USART_CTRL1.WL bits, least significant bit first.

The stop bit of the data frame is high.

An idle frame is a complete data frame consisting of '1's, including the start bit. followed by the start bit of a data frame containing the data .

A break frame is a complete data frame consisting of '0's, including the stop bit. at the end of the break frame, the transmitter inserts 1 or 2 more stop bits ('1') to acknowledge the start bit.

Figure 24-2 Word length = 8 setting

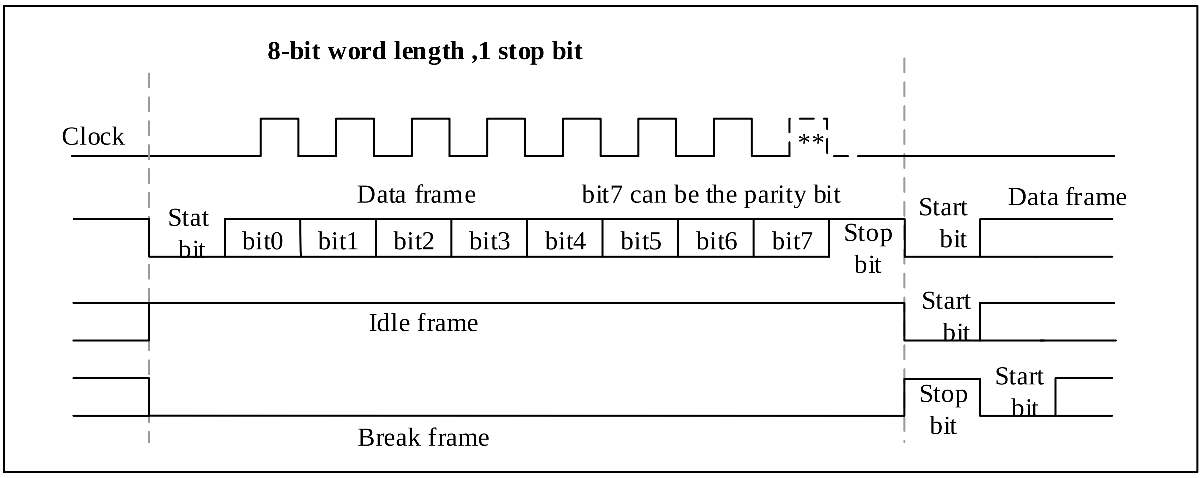

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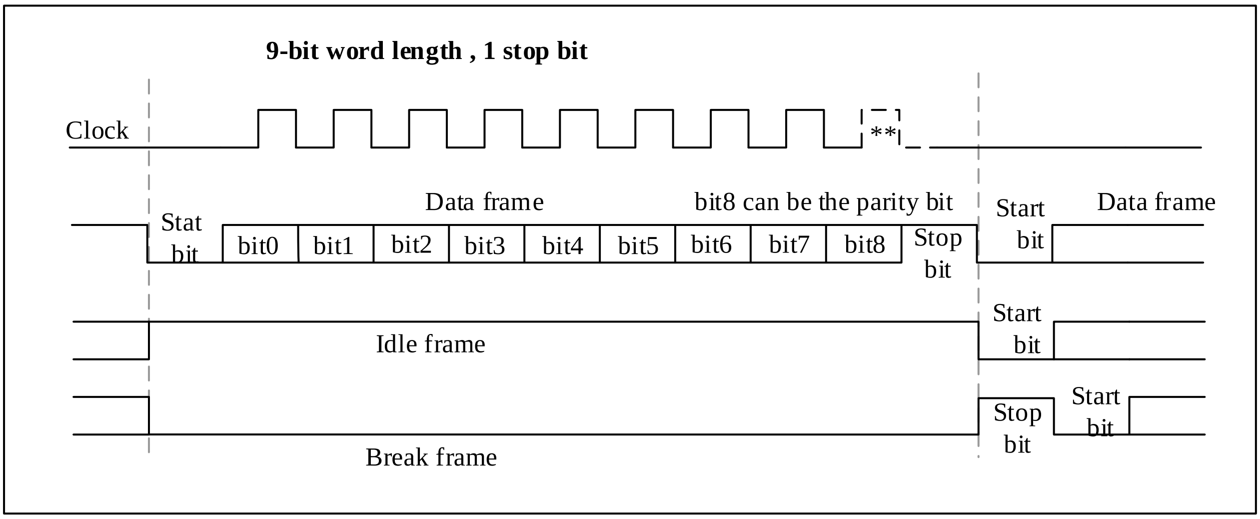
Figure 24-3 Word length = 9 setting



24.4.2 Transmitter

After the transmitter is enabled, the data entered into the transmit shift register is sent out through the TX pin.

24.4.2.1 Idle frame

Setting USART_CTRL1.TXEN will cause the USART to transmit an idle frame before the first data frame.

24.4.2.2 Character send

Idle frames are followed by characters sent. Each character is preceded by a low start bit. The transmitter sends 8-bit or 9-bit data according to the configuration of the data bit length, with the least significant bit first. If USART_CTRL1.TXEN is reset during a data transfer, it will cause the baud rate counter to stop counting and the data being transferred will be corrupted.

24.4.2.3 Stop bit

The characters are followed by stop bits, the number of which can be configured by setting USART_CTRL2. STPB[1:0].

Table 24-1 Stop bit configuration

USART_CTRL2.STPB[1:0]	Stop bit length (bits)	functional description
00	1	default
01	0.5	Receiving in Smartcard mode
10	2	General USART mode, single-wire mode and modem mode.
11	1.5	Transmitting and receiving in Smartcard mode

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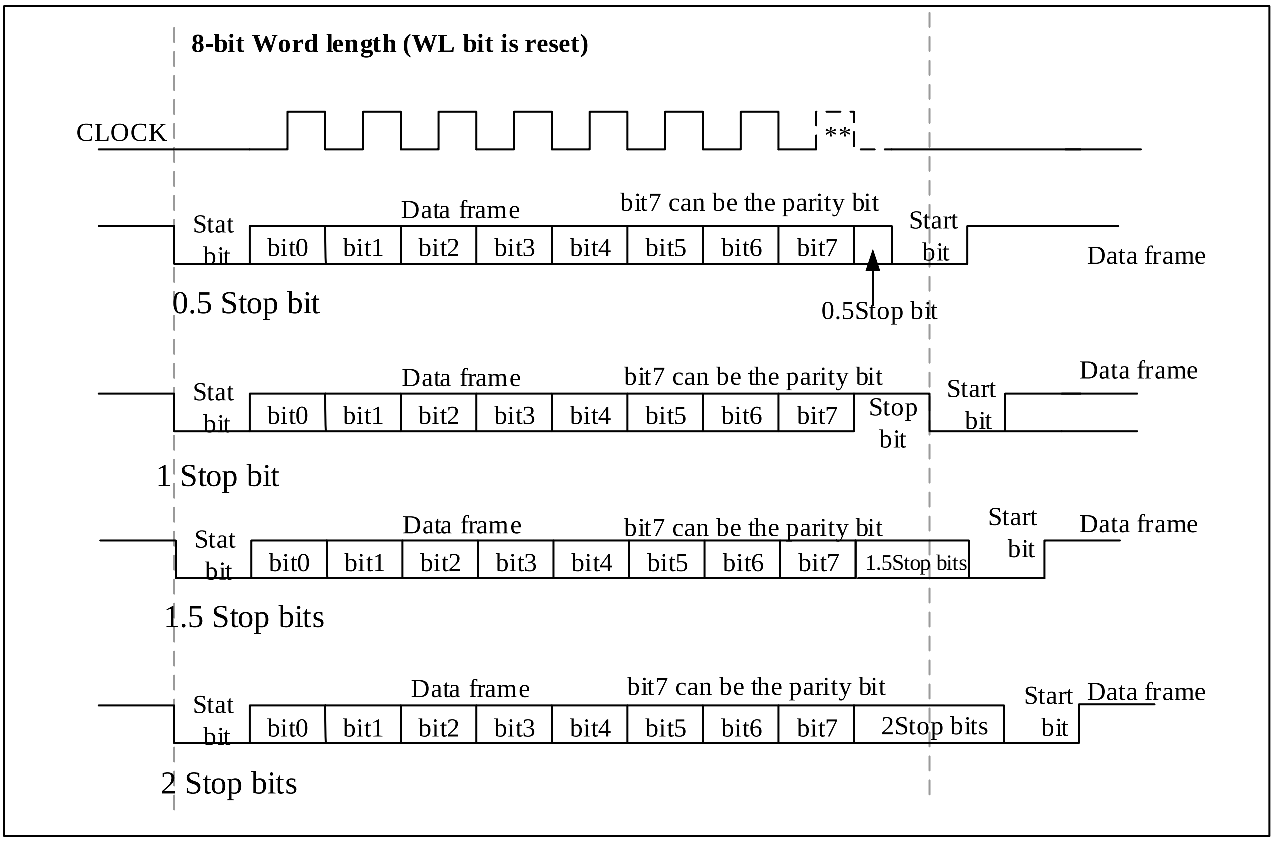
Figure 24-4 Configuration stop bit



24.4.2.4 Break frame

Use USART_CTRL1.SDBRK to send the break character. When there is 8-bit data, the break frame consists of 10 bits of low level, followed by a stop bit; when there is 9-bit data, the break frame consists of 11 bits of low level, followed by a stop bit.

After the break frame is sent, USART_CTRL1.SDBRK is cleared by hardware, and the stop bit of the break frame is being sent. Therefore, to send a second break frame, USART_CTRL1.SDBRK should be set after the stop bit of the previous break frame has been sent.

If software resets the USART_CTRL1.SDBRK bit before starting to send the break frame, the break frame will not be sent.

24.4.2.5 Transmitter process

1. Enable USART_CTRL1.UEN to activate USART;
2. Configure the transmitter's baud rate, data bit length, parity bit (optional), the number of stop bits or DMA configuration;
3. Activate the transmitter (USART_CTRL1.TXEN);
4. Send each data to be sent to the USART_DAT register through the CPU or DMA, and the write operation to the USART_DAT register will clear USART_STS.TXDE;
5. After writing the last data word in the USART_DAT register, wait for USART_STS.TXC =1, which indicates

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the end of the transmission of the last data frame.

24.4.2.6 Single byte communication

A write to the USART_DAT register clears the USART_STS.TXDE bit.

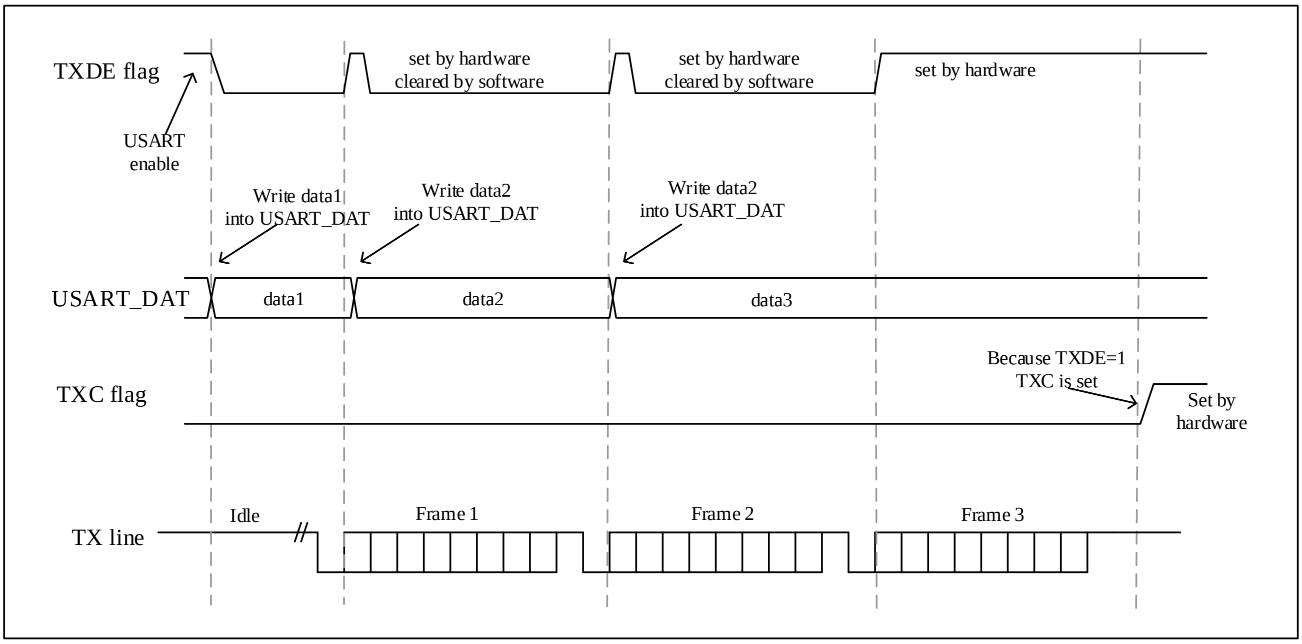
The USART_STS.TXDE bit is set by hardware when the data in the TDR register is transferred to the transmit shift register (indicating that data is being transmitted). An interrupt will be generated if USART_CTRL1.TXDEIEN is set. At this point, the next data can be sent to the USART_DAT register because the TDR register has been cleared and will not overwrite the previous data.

Write operation to USART_DAT register:

- When the transmit shift register is not sending data and is in an idle state, the data is directly put into the shift register for transmission, and the USART_STS.TXDE bit is set by hardware;
- When the transmit shift register is sending data, the data is stored in the TDR register, and after the current transmission is completed, the data is put into the shift register.

When a frame containing data is sent and USART_STS.TXDE=1, the USART_STS.TXC bit is set to '1' by hardware. An interrupt is generated if USART_CTRL1.TXCIEN is '1'. USART_STS.TXC bit is cleared by a software sequence (read USART_STS register first, then write USART_DAT register).

Figure 24-5 TXC/TXDE changes during transmission



24.4.3 Receiver

24.4.3.1 Start bit detection

When the received sampling sequence is: 1 1 1 0 X 0 X 0 X 0 0 0 0, it is considered that a start bit is detected.

The samples at the 3rd, 5th, and 7th bits, and the samples at the 8th, 9th, and 10th bits are all '0' (that is, 6 '0'), then confirm the receipt of the start bit, the USART_STS.RXDNE flag bit is set, and if USART_CTRL1.RXDNEIEN=1,

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an interruption occurs and will not Set the NEF noise flag.

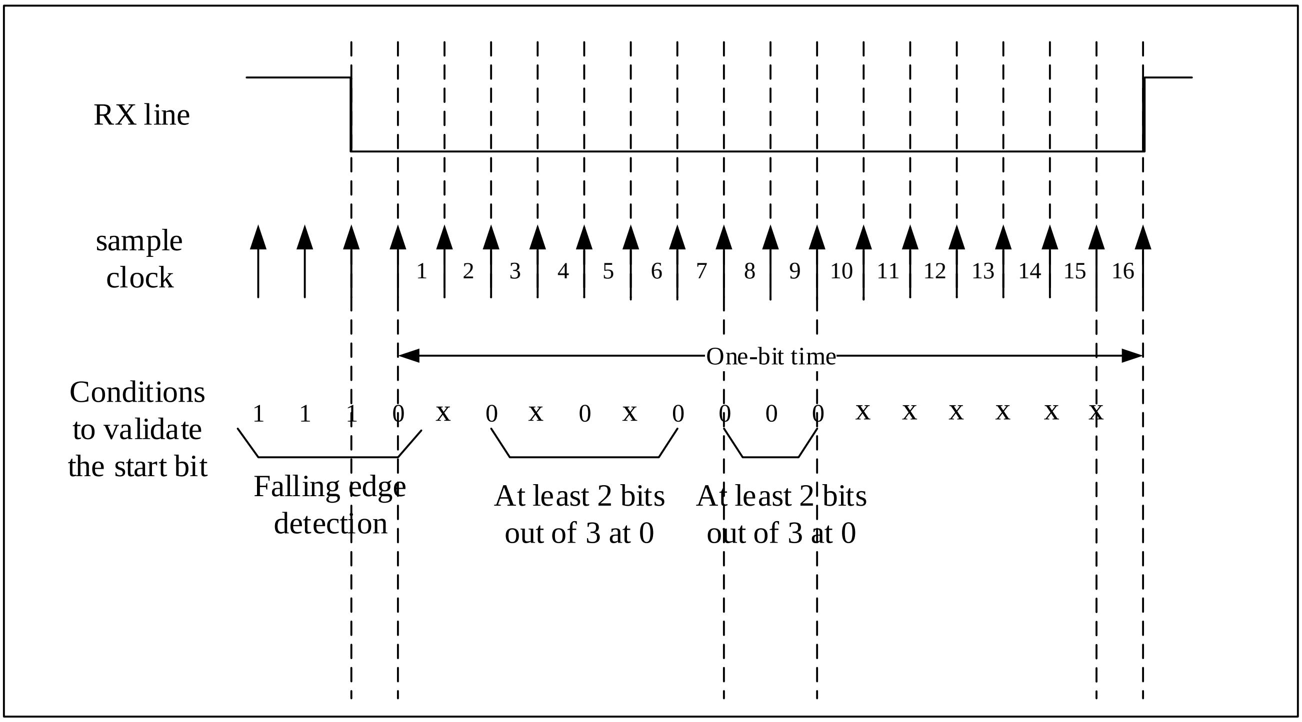
The samples of the 3rd, 5th, and 7th bits have two '0' points, and at the same time, the samples of the 8th, 9th, and 10th bits have three '0' points, then the start bit is confirmed, but it will be set NEF noise flag.

The samples of the 3rd, 5th, and 7th bits have three '0' points, and at the same time, the samples of the 8th, 9th, and 10th bits have two '0' points, then the start bit is confirmed, but it will be set NEF noise flag.

The samples of the 3rd, 5th, and 7th bits have two '0' points, and at the same time, the samples of the 8th, 9th, and 10th bits have two '0' points, then it is confirmed that the start bit is received, but it will be set bit NEF noise flag.

If the sampling values in the 3rd, 5th, 7th, 8th, 9th and 10th bits cannot meet the above four requirements, the USART receiver thinks that it has not received the correct start bit, and will exit the start bit detection and Return to idle state and wait for falling edge.

Figure 24-6 Start bit detection



24.4.3.2 Stop bit description

During data reception, the number of data stop bits can be configured by the USART_CTRL2.STPB[1:0]. In normal mode, 1 or 2 stop bits can be selected. In Smartcard mode, 0.5 or 1.5 stop bits can be selected.

1. 0.5 stop bits (receive in smartcard mode): 0.5 stop bits are not sampled. Therefore, if 0.5 stop bits is selected, framing errors and broken frames cannot be detected.
2. 1 stop bit: the sampling of one stop bit is carried out through three points, and the 8th, 9th and 10th sampling bits are selected.
3. 1.5 stop bit (Smartcard mode): when sending in Smartcard mode, the device must check whether the data is sent correctly. So the receiver function block must be activated (USART_CTRL1.RXEN=1) and sample the signal

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on the data line during the transmission of the stop bit. If a parity error occurs, the smartcard will pull down the data line when the transmitter samples the NACK signal, that is, within the time corresponding to the stop bit on the bus, indicating that a framing error has occurred. The USART_STS.FEF is set together with the USART_STS.RXDNE at the end of the 1.5th stop bit. The 1.5 stop bits were sampled at points 16, 17 and 18. The 1.5 stop bits can be divided into two parts: one is 0.5 clock cycles, during which nothing is done. This is followed by the stop bit of 1 clock cycle, which is sampled at the midpoint of this period of time. For details, see 24.4.14 Smartcard mode.

4. 2 stop bits: the sampling of the 2 stop bits is completed at the 8th, 9th and 10th sampling points of the first stop position. If a frame error is detected during the first stop bit, the frame error flag is set. The second stop bit does not detect framing error. The USART_STS.RXNE flag will be set at the end of the first stop bit.

24.4.3.3 Receiver process

1. Enable USART_CTRL1.UEN to activate USART;
2. Configure the receiver's baud rate, data bit length, parity bit (optional), stop bit number or DMA configuration;
3. Activate the receiver (USART_CTRL1.RXEN) and start looking for the start bit;
4. The receiver receives 8-bit or 9-bit data according to the configuration of the data bit length, and the least significant bit of the data is first shifted from the RX pin into the receive shift register;
5. When the data of the received shift register is moved to the RDR register, USART_STS.RXDNE is set, and the data can be read out. If USART_CTRL1.RXNEIEN is 1, an interrupt will be generated;
6. When an overflow error, noise error, or frame error is detected in the received frame, the corresponding error flag status bit will be set. If USART_CTRL1.RXEN is reset during data transmission, the data being received will be lost;
7. USART_STS.RXDNE is set after receiving data, and a read operation of USART_DAT can clear this bit:

- During multi-buffer communication, the data register is cleared by the DMA read operation;
- During single-buffer communication, it is cleared by software reading the USART_DAT register.

24.4.3.4 Idle frame detection

The receiver of the USART can detect idle frames. An interrupt is generated if USART_CTRL1.IDLEIEN is '1'. USART_STS.IDLEF bit is cleared by a software sequence (read USART_STS register first, then read USART_DAT register).

24.4.3.5 Break frame detection

The frame error flag(USART_STS.FEF) is set by hardware when the receiver detects a break frame. It can be cleared by a software sequence (read USART_STS register first, then read USART_DAT register).

24.4.3.6 Framing error

A framing error occurs when a stop bit is not received and recognized at the expected time. At this time, the frame error flag USART_STS.FEF will be set by hardware, and the invalid data will be transferred from the shift register to the USART_DAT register. During single-byte communication, no framing error interrupt will be generated because it occurs with USART_STS.RXDNE and the hardware will generate an interrupt when the USART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt will be generated if the USART_CTRL3.ERRIEN bit

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is set.

24.4.3.7 Overrun error

When USART_STS.RXDNE is still '1', when the data currently received in the shift register needs to be transferred to the RDR register, an overflow error will be detected, and the hardware will set USART_STS.OREF. When this bit is set, the value in the RDR register is not lost, but the data in the shift register is overwritten. It is cleared by a software sequence (read USART_STS register first, then write USART_DAT register).

When an overflow error occurs, USART_STS.RXDNE is '1', and an interrupt is generated. If the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the USART_STS.OREF flag is set in multi-buffer communication mode.

24.4.3.8 Noise error

USART_STS.NEF is set by hardware when noise is detected on a received frame. It is cleared by software sequence (read USART_STS register first, then write USART_DAT register). During single-byte communication, no noise interrupt generated because it occurs with USART_STS.RXDNE and the hardware will generate an interrupt when the USART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt is generated when the USART_STS.NEF flag is set if the USART_CTRL3.ERRIEN bit is set.

Table 24-2 Data sampling for noise detection

Sample value	NE status	Received bits	Data validity
000	0	0	Effective
001	1	0	be invalid
010	1	0	be invalid
011	1	1	be invalid
100	1	0	be invalid
101	1	1	be invalid
110	1	1	be invalid
111	0	1	Effective

24.4.4 Generation of fractional baud rate

The baud rate of the USART can be configured in the USART_BRCF register. This register defines the integer and fractional parts of the baud rate divider. The baud rate of the transmitter and receiver should be configured to the same value. Be careful not to change the value of the USART_BRCF register during communication, because the baud rate counter will be replaced by the new value of the baud rate register.

$$\text{TX / RX baud rate} = f_{PCLK} /(16 * \text{USARTDIV})$$

where f_{PCLK} is the clock provided to the peripheral:

- PCLK1 is used for USART2, USART3, up to 27MHz;

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- PCLK2 is used for USART1, UART4, UART5, up to 54MHz.

USARTDIV is an unsigned fixed-point number.

24.4.4.1 USARTDIV and USART_BRCF register configuration

Example 1:

If USARTDIV = 27.75, then：

DIV_Decimal = 16*0.75 = 12 = 0x0C

DIV_Integer = 27=0x1B

So USART_BRCF = 0x1BC

Example 2:

If USARTDIV = 20.98, then：

DIV_Decimal = 16*0.98 = 15.68

Nearest integer: DIV_Decimal = 16 = 0x10, out of configurable range, so a carry to integer is required

So DIV_Integer = 20+1 = 21 = 0x15

DIV_Decimal = 0x0

So USART_BRCF = 0x150

Example 3:

If USART_BRCF = 0x19B：

DIV_Integer = 0x19 = 25

DIV_Decimal = 0x0B = 11

So USARTDIV = 25+11/16 = 25.6875

Table 24-3 Error calculation when setting baud rate

Baud rate		**f_{PCLK}=27MHz**			**f_{PCLK}=54MHz**		
serial number	Kbps	reality	Set value in register	Error(%)	reality	Set value in register	Error(%)
1	2.4	2.4	703.125	0%	2.4	1406.25	0%
2	9.6	9.6	175.8125	0.02%	9.6	351.5625	0%
3	19.2	19.2	87. 8755	0.02%	19.2	175.8125	0.02%
4	57.6	57.6	29.3125	0.05%%	57.6	78.125	0.05%
5	115.2	115.384	14.625	0.16%	115.2	29.3125	0.05%

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6	230.4	230.769	7.3125	0.16%	230.769	14.625	0%
7	460.8	461.538	3.6875	0.69%	461.538	7.3125	0%
8	921.6	923.076	1.8125	1%	923.076	4.875	0.8%
9	1687.5	1687.7	1	0%	2250	1.5	0%
10	3375	impossible	impossible	impossible	3375	1	0%

Notes: The lower the clock frequency of the CPU, the lower the error for a particular baud rate.

24.4.5 Receiver's tolerance clock deviation

Variations due to transmitter errors (including transmitter side oscillator variations), receiver side baud rate rounding errors, receiver side oscillator variations, variations due to transmission lines (usually due to The inconsistency between the low-to-high transition timing of the transceiver and the high-to-low transition timing of the transceiver), these factors will affect the overall clock system variation. Only when the sum of the above four changes is less than the tolerance of the USART receiver, the USART asynchronous receiver can work normally.

When receiving data normally, the tolerance of the USART receiver depends on the selection of the data bit length and whether it is generated using a fractional baud rate. The tolerance of the USART receiver is equal to the maximum tolerable variation.

Table 24-4 When DIV_Decimal = 0. Tolerance of USART receiver

WL bit	NF is an error	NF is don't care
0	3.75%	4.375%
1	3.41%	3.97%

Table 24-5 When DIV_Decimal != 0. Tolerance of USART receiver

WL bit	NF is an error	NF is don't care
0	3.33%	3.88%
1	3.03%	3.53%

24.4.6 Parity control

Parity can be enabled by configuring the USART_CTRL1.PCEN bit.

When the parity bit is enabled for transmission, A parity bit is generated, parity check is performed on reception.

Table 24-6 Frame format

WL bit	PCEN bit	USART frame

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0	0	| Start bit | 8-bit data | Stop bit |
0	1	| Start bit | 7 bits of data | Parity bit | Stop bit |
1	0	| Start bit | 9-bit data | Stop bit |
1	1	| start bit | 8-bit data | parity bit | stop bit |

Even parity

Configure USART_CTRL1.PSEL to 0, and even parity can be selected.

Make the number of '1' in the transmitted data (including parity bit) be an even number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total). After the data and check digit are sent to the receiver, the receiver calculates the number of 1s in the data again. If it is an even number, the check is passed, indicating that no errors occurred during the transmission process. If it is not even, it means that an error has occurred, the USART_STS.PEF flag is set to '1', and if USART_CTRL1.PEIEN is enabled, an interrupt is generated.

Odd parity

Configure USART_CTRL1.PSEL to 1, you can choose odd parity.

Make the number of '1' in the transmitted data (including parity bit) be an odd number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total). After the data and check digit are sent to the receiver, the receiver calculates the number of 1s in the data again. If it is an odd number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an odd number, it means that an error has occurred, the USART_STS.PEF flag is set to '1', and if USART_CTRL1.PEIEN is enabled, an interrupt is generated.

24.4.7 DMA application

The USART supports the DMA mode using multi-buffer configuration, which can realize high-speed data communication.

24.4.7.1 Using DMA transmission

Set USART_CTRL3.DMATXEN to enable DMA mode when transmitting. When the USART's transmit shift register is empty (USART_STS.TXDE=1), the DMA will transfer the data from the SRAM to the USART_DAT register of the USART.

When using DMA transmission, the process of configuring the DMA channel is as follows:

1. Set the address of the data memory. When a data transfer request occurs, the transferred data will be read from this address.
2. Set the address of the USART_DAT register. When a data transfer request occurs, this address will be the destination address of the data transfer.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the channel.

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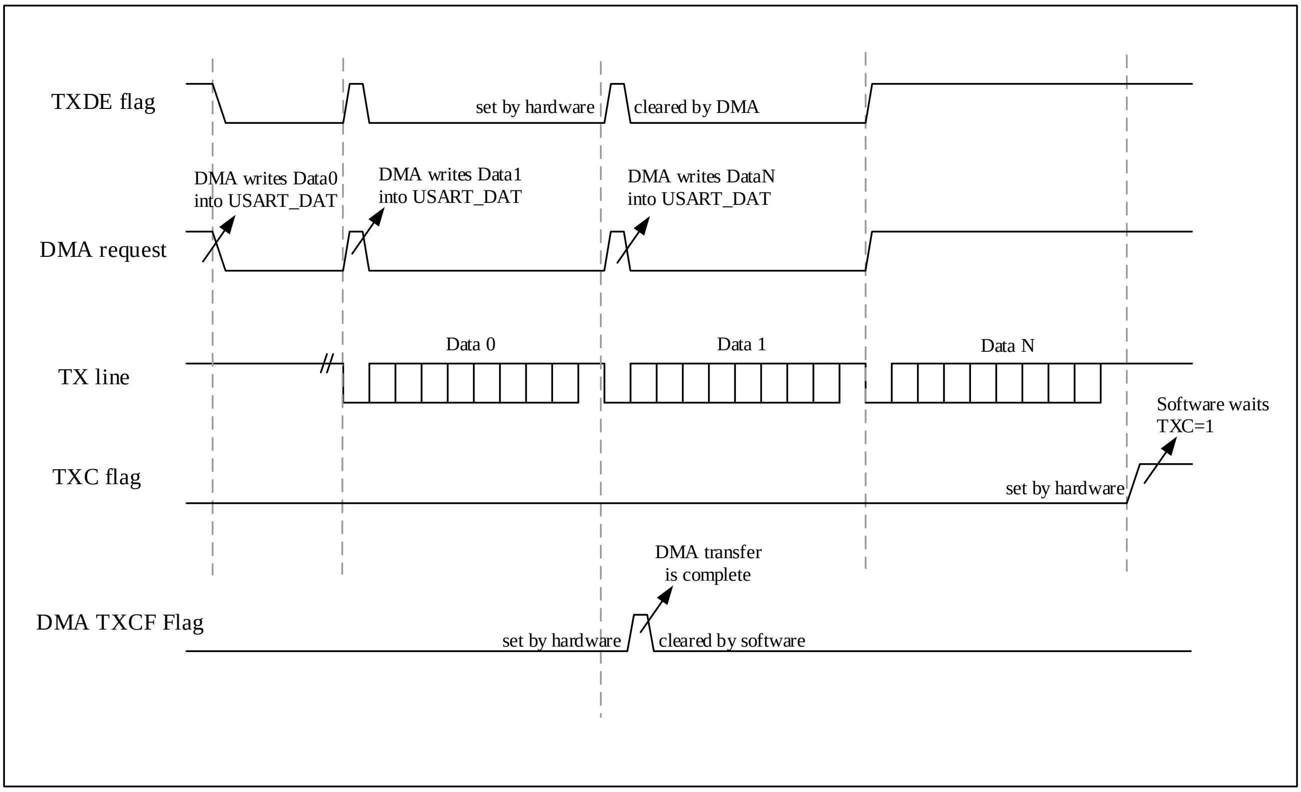
6. After the data transfer is completed, the transfer complete flag (DMA_INTSTS.TXCFx) is set to 1.

Figure 24-7 Transmission using DMA



24.4.7.2 Using DMA reception

Set USART_CTRL3.DMARXEN to enable DMA mode when receiving. When a byte is received (USART_STS.RXDNE=1), the DMA will transfer the data from the USART_DAT register of the USART to the SRAM.

When using DMA reception, the process of configuring the DMA channel is as follows:

1. Set the address of the USART_DAT register. When a data transfer request occurs, this address will be the source address of the data transfer.
2. Set the address of the data memory. When a data transfer request occurs, the transferred data will be written to this address.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the channel.

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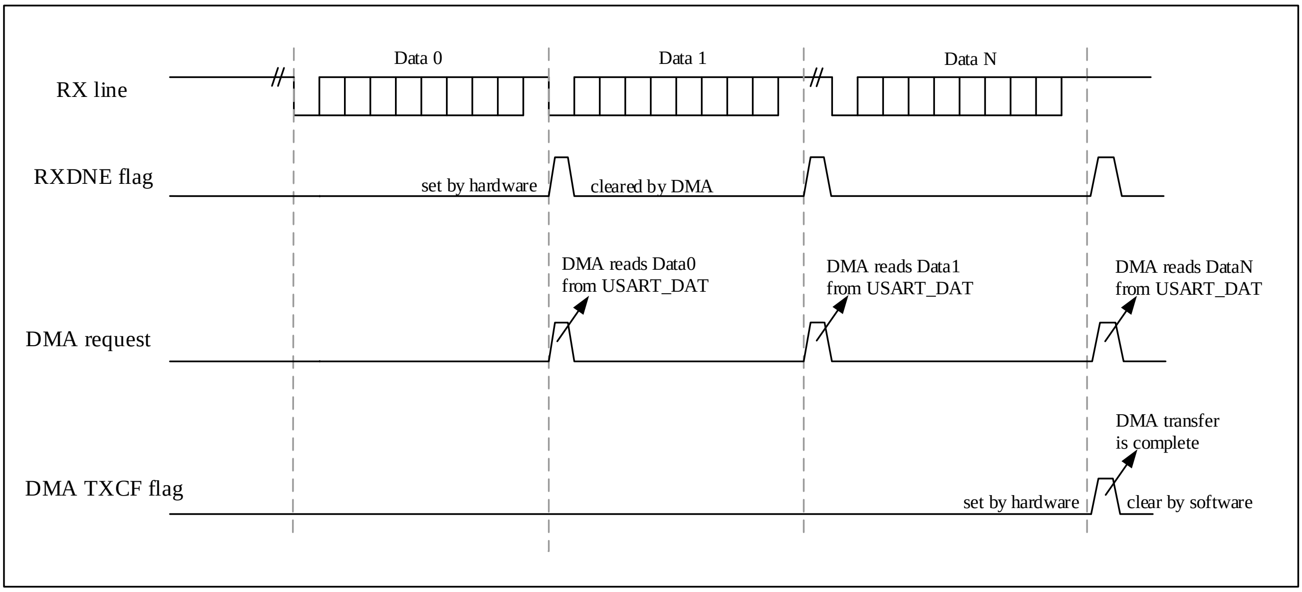
Figure 24-8 Reception using DMA

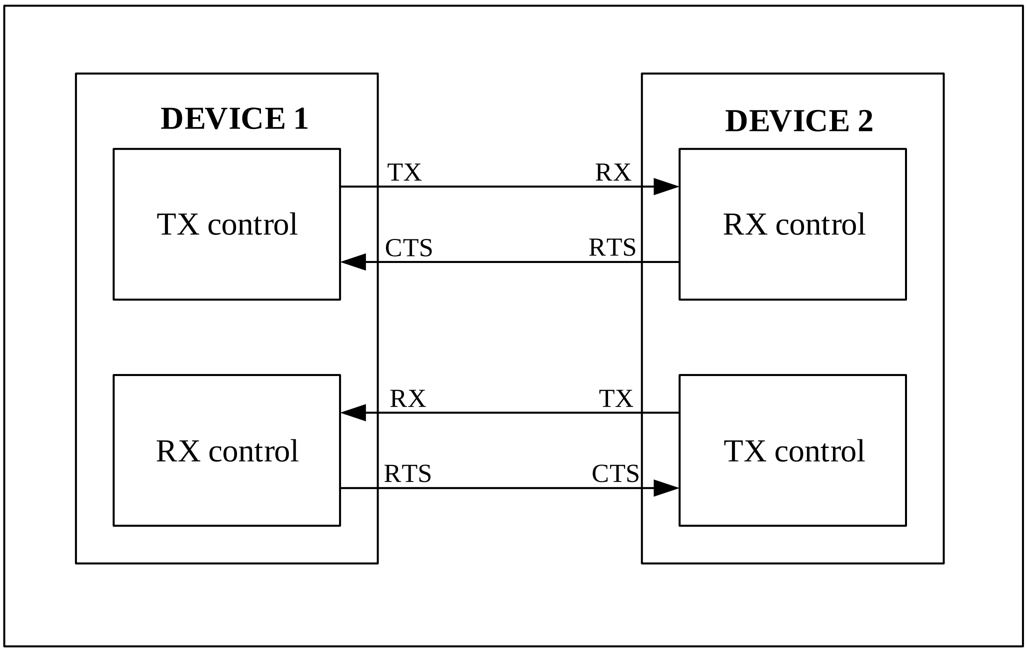


In multi-buffer communication mode, the error flag will be set when there is a frame error, overrun or noise error. An interrupt will be generated if the error interrupt is enabled (USART_CTRL3.ERRIEN=1).

24.4.8 Hardware flow control

USART supports hardware flow control. The purpose is to coordinate the sending and receiving parties so that the data will not be lost. The connection method is shown in the following figure.

Figure 24-9 hardware flow control between two USART



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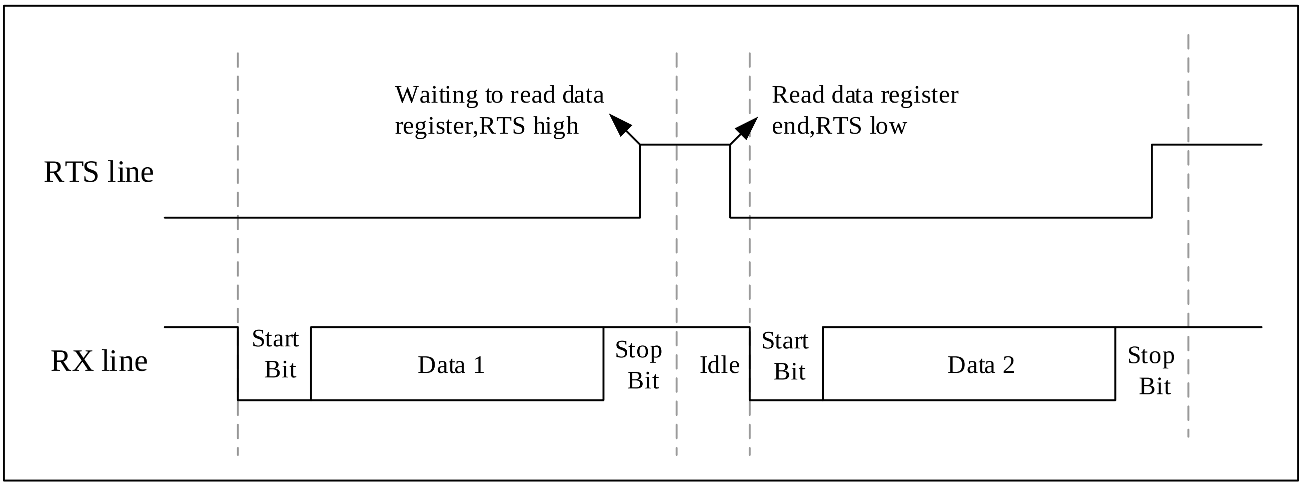
24.4.8.1 RTS flow control

Set USART_CTRL3.RTSEN to enable RTS. RTS is the output signal used to indicate that the receiver is ready. When data arrives in RDR, pull high nRTS output, notifying the sender to stop data transmission at the end of the current frame. when receiver is ready to receive new data, assert (pull low) the nRTS output.

Figure 24-10 RTS flow control



24.4.8.2 CTS flow control

Set USART_CTRL3.CTSEN to enable CTS. CTS is an input signal, used to judge whether data can be sent to the other device. The low level is valid, and the low level indicates that the device can send data to the other device. If the nCTS signal becomes invalid during data transmission, the transmission will stop after sending the data. If you write data to the data register when nCTS is invalid, the data will not be sent until nCTS is valid.

If the USART_CTRL3.CTSEN bit is set, the USART_STS.CTSF bit will be set high by hardware when the nCTS input changes state. An interrupt will be generated if USART_CTRL3.CTSIEN is enabled.

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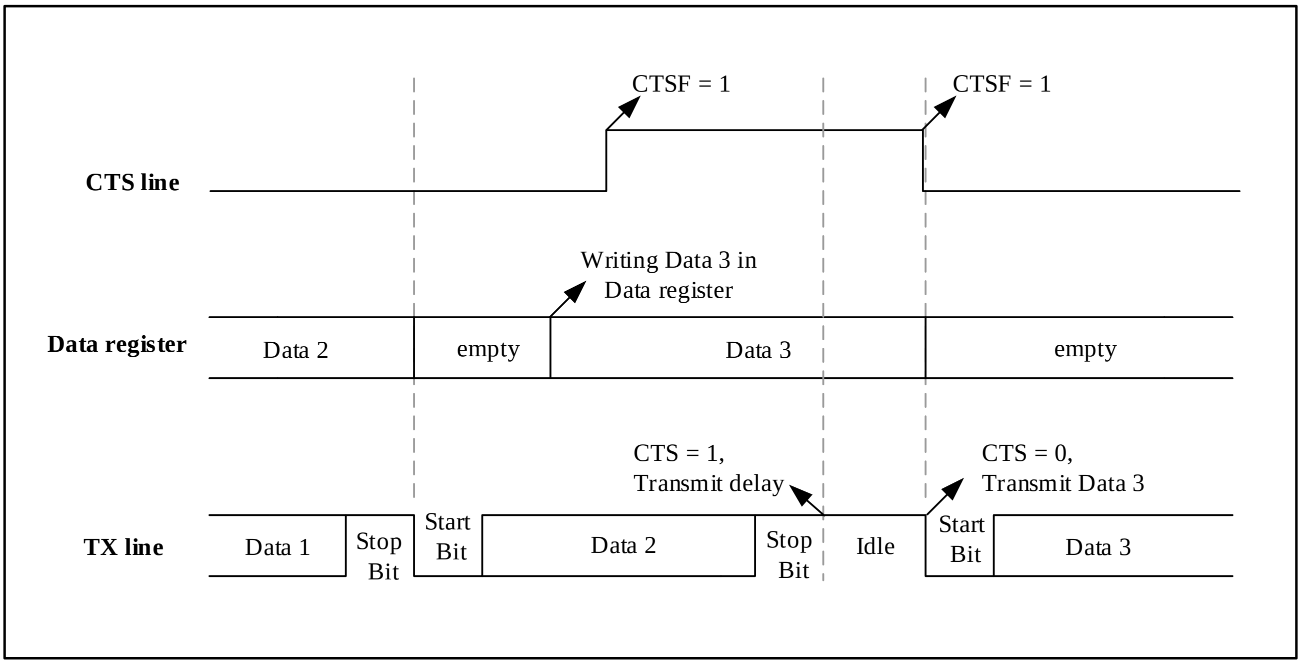
Figure 24-11 CTS flow controls



24.4.9 Multiprocessor communication

USART allows multiprocessor communication. The principle is: multiple processors communicate through USART, and it is necessary to determine who is the master device, and the remaining processors are all slave devices. The TX output of the master device is directly connected to the RX port of all slave device. The TX outputs of the slaves are logically AND together and connected to the RX inputs of the master.

When multi-processor communication is performed, the slave devices are all in mute mode, and the host uses a specific method to wake up a slave device to be communicated when needed, so that the slave device is in an active state and transmits data with the master device.

The USART can wake up from mute mode by idle line detection or address mark detection.

24.4.9.1 Idle line detection

The idle line detection configuration process is as follows:

1. Configure the USART_CTRL1.WUM bit to 0, and the USART performs idle line detection;
2. When USART_CTRL1.RCVWU is set (which can be automatically controlled by hardware or written by software under certain conditions), USART enters mute mode. In mute mode, none of the receive status bits are set, and all receive interrupts are disabled;
3. As shown in the Figure 24-12 below, when an idle frame is detected, USART is woken up, and then USART_CTRL1.RCVWU is cleared by hardware. At this time, USART_STS.IDLEF is not set.

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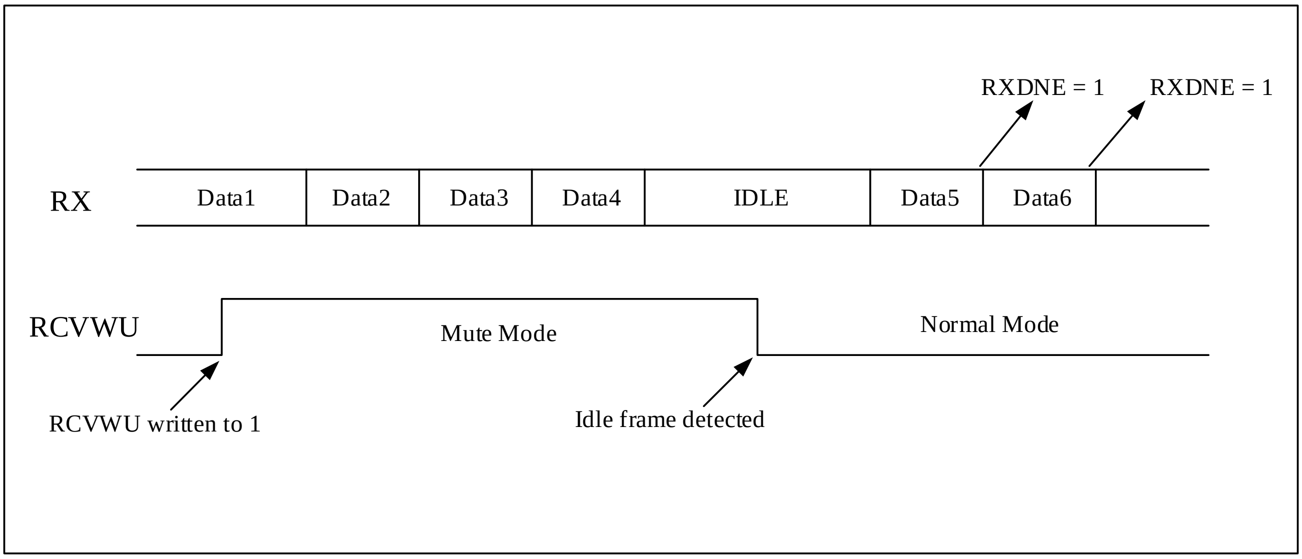
Figure 24-12 Mute mode using idle line detection



24.4.9.2 Address mark detection

By configuring the USART_CTRL1.WUM bit to 1, the USART performs address mark detection. The address of the receiver is programmable through the USART_CTRL2.ADDR[3:0] bits. If the MSB is 1, the byte is considered an address, otherwise it is considered data.

In this mode, the USART can enter mute mode by:

- When the receiver does not contain data, USART_CTRL1.RCVWU can be written to 1 by software, and USART enters mute mode;

  Note: When the receive buffer contains no data (RXNE=0 in USART_SR), the USART_CTRL1.RCVWU bit can be written to 0 or 1. Otherwise, the write operation is ignored.

- When the received address does not match the address of the USART_CTRL2.ADDR[3:0] bits, USART_CTRL1.RCVWU is written to 1 by hardware.

In mute mode, none of the receive status bits are set and all receive interrupts are disabled.

When the received address matches the address of the USART_CTRL2.ADDR[3:0] bits, the USART is woken up and USART_CTRL1.RCVWU is cleared. The USART_STS.RXDNE bit will be set when this matching address is received. Data can then be transmitted normally.

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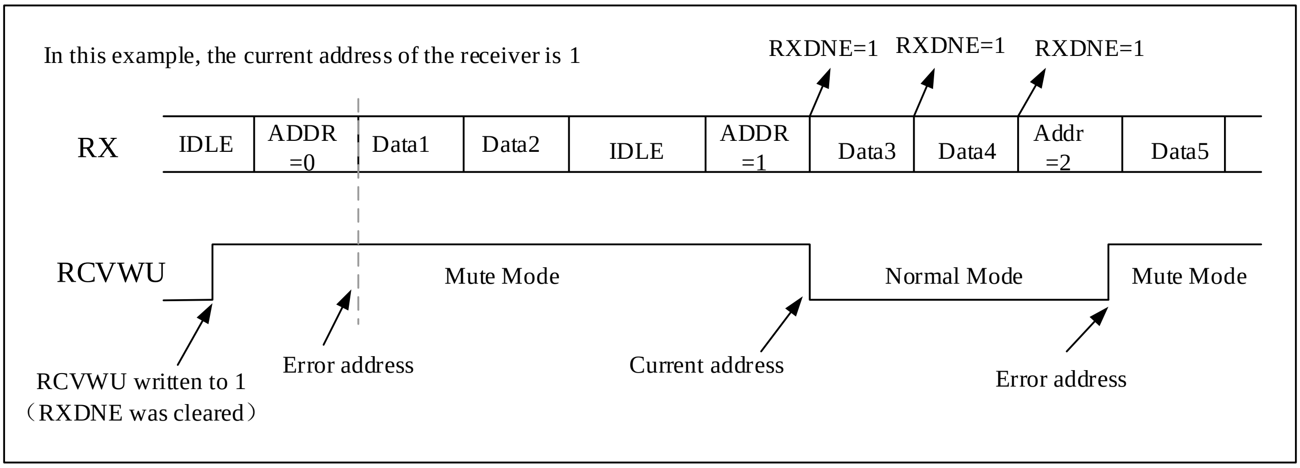
Figure 24-13 Mute mode detected using address mark



24.4.10 Synchronous mode

USART supports synchronous serial communication. The USART only supports the master mode, and cannot use the input clock from other devices to receive and transmit data. Synchronous mode can be enabled by configuring the USART_CTRL2.CLKEN bit.

Note: When using synchronous mode, USART_CTRL2.LINMEN, USART_CTRL3.SCMEN, USART_CTRL3.HDMEN, USART_CTRL3. IRDAMEN, these bits need to be kept clear.

24.4.10.1 Synchronized clock

The CK pin is the output of the USART transmitter clock. During the bus idle period, before the actual data arrives and when the break symbol is sent, the clock not output.

Clock phase and polarity are software programmable and need to be configured when both the transmitter and receiver are disabled. When the clock polarity is 0 (USART_CTRL2.CLKPOL=0), the default level of CLK is low; when the clock polarity is 1 (USART_CTRL2.CLKPOL=1), the default level of CLK is high. When the phase polarity is 0 (USART_CTRL2.CLKPHA=0), the data is sampled on the first edge of the clock; when the phase polarity is 1 (USART_CTRL2.CLKPHA=1), the data is sampled on the second edge.

During the start and stop bits, the CK pin does not output clock pulses.

A sync data cannot be received when no data is sent. Because the clock is only available when the transmitter is activated and data is written to the USART_DAT register.

The USART_CTRL2.LBCLK bit controls whether to output the clock pulse corresponding to the last data byte (MSB) sent on the CK pin. This bit needs to be configured when both the transmitter and receiver are disabled. If USART_CTRL2.LBCLK is 1, the clock pulse of the last bit of data will be output from CK. If USART_CTRL2.LBCLK is 0, the clock pulse of the last bit of data is not output from CK.

24.4.10.2 Synchronized transmitting

The transmitter in synchronous mode works the same as in asynchronous mode. Data on the TX pin is sent out synchronously with CK.

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24.4.10.3 Synchronized receiving

The receiver in synchronous mode works differently than in asynchronous mode. Data is sampled on CK without any oversampling. But setup time and hold time (depending on baud rate, 1/16 bit time) must be considered.

Figure 24-14 USART synchronous transmission example

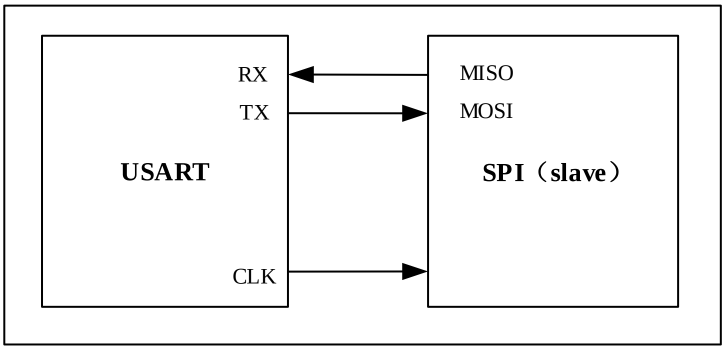

Figure 24-15 USART data clock timing example (WL=0)

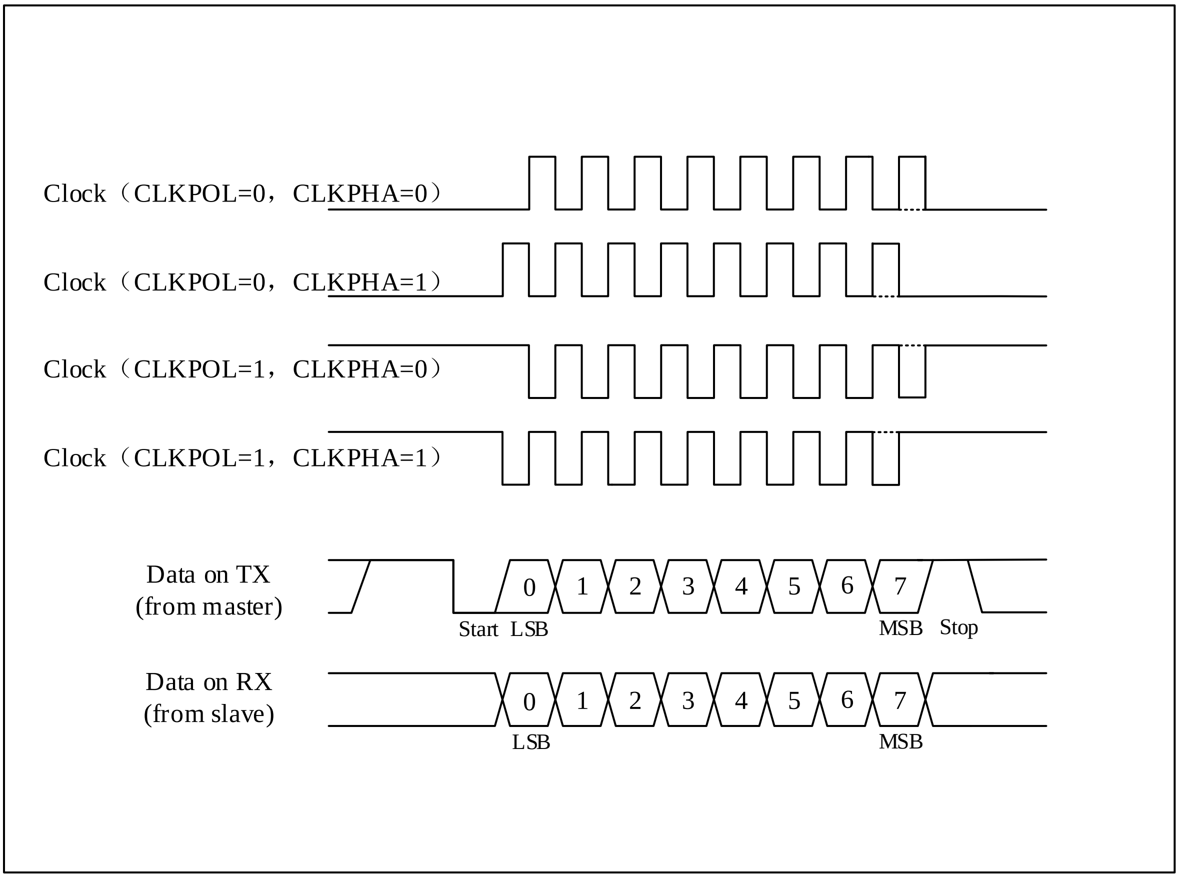

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Figure 24-16 USART data clock timing example (WL=1)

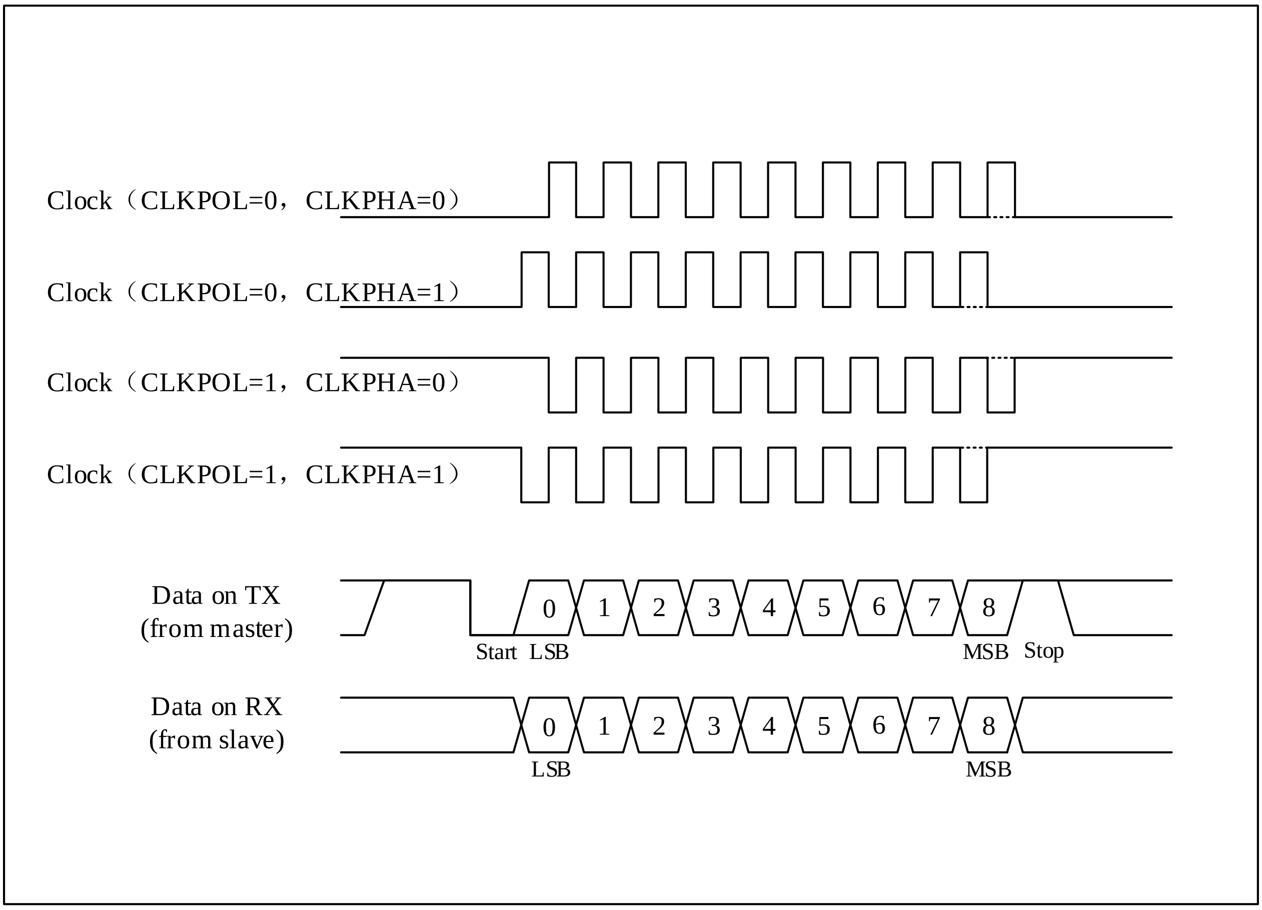
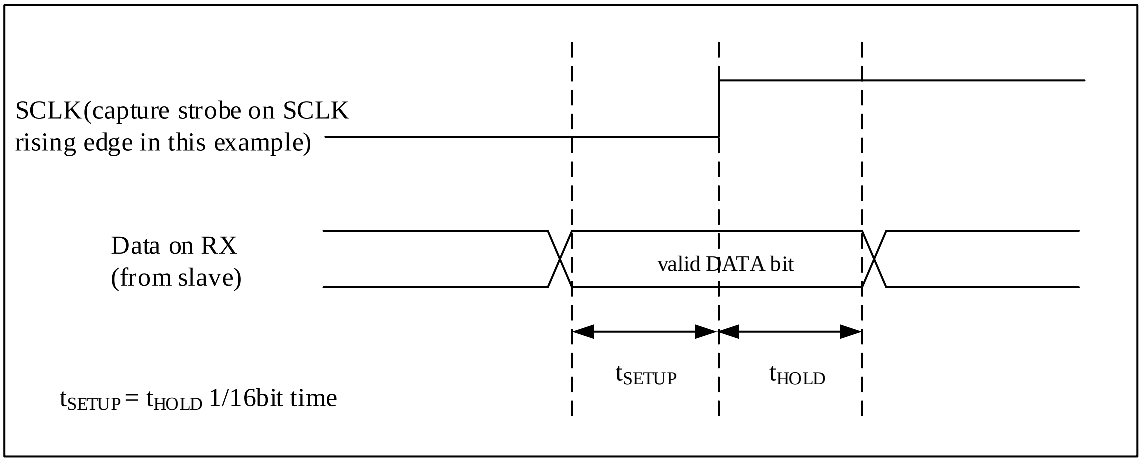


Figure 24-17 RX data sampling / holding time



Note: the function of CK is different in Smartcard mode, please refer to the Smartcard mode section for details.

24.4.11 Single-wire half-duplex mode

USART supports single-wire half-duplex communication, allowing data to be transmitted in both directions, but only

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allows data to be transmitted in one direction at the same time. Communication conflicts are managed by software.

Through the USART_CTRL3.HDMEN bit, you can choose whether to enable half-duplex mode. When using single-wire half-duplex, USART_CTRL2. CLKEN, USART_CTRL2. LINMEN, USART_CTRL3. SCMEN, USART_CTRL3. IRDAMEN, these bits should be kept clear.

After the half-duplex mode is turned on, the TX pin and the RX pin are interconnected inside the chip, and the Rx pin is no longer used. When there is no data to transmit, TX is always released. Therefore, when not driven by the USART, the TX pin must be configured as a floating input or an open-drain output high.

24.4.12 IrDA SIR ENDEC mode

USART supports the IrDA (Infrared Data Association) SIR ENDEC specification.

Through the USART_CTRL3. IRDAMEN bit, you can choose whether to enable the infrared mode. When using the infrared function, USART_CTRL2.CLKEN, USART_CTRL2.STPB[1:0], USART_CTRL2.LINMEN, USART_CTRL3.HDMEN, USART_CTRL3.SCMEN, these bits should be kept clear.

Through the USART_CTRL3. IRDALP bit, it can be used to select normal mode or low power infrared mode.

24.4.12.1 IrDA normal mode

When USART_CTRL3.IRDALP=0, select normal infrared mode.

IrDA is a half-duplex communication protocol, so there should be a minimum delay of 10ms between sending and receiving.that uses a inverted return-to-zero modulation scheme (RZI), which uses an infrared light pulse to represent a logic '0', and the pulse width is specified as 3/16 of a bit period in normal mode, as shown in the Figure 24-19.USART only supports up to 115200bps for SIR ENDEC.

The USART sends data to the SIR encoder, and the bit stream output by the USART will be modulated. A modulated stream of pulses is sent from the infrared transmitter and then received by the infrared receiver. The SIR receiver decoder demodulates it and outputs the data to the USART.

The transmit encoder output has opposite polarity to the decoder input. When idle, SIR transmit is low, while SIR receive is high. The high pulse sent by SIR is '0' and the low level is '1', while SIR reception is the opposite.

If the USART is sending data to the IrDA transmit encoder, then the IrDA receive decoder will ignore any data on the IrDA receive line. If the USART is receiving data sent from the SIR receiver decoder, the data sent by the USART to the IrDA transmitter encoder will not be encoded.

Pulse width is programmable. The IrDA specification requires pulses to be wider than 1.41us. For pulse widths less than 2 cycles, the receiver will filter them out. PSCV is the prescaler value programmed in the USART_GTP register.

24.4.12.2 IrDA low power mode

When USART_CTRL3.IRDALP=1, select low power infrared mode.

For the transmitter, when in low power mode, the pulse width is 3 times the low power baud rate, which is a minimum of 1.42MHz. Typically this value is 1.8432MHz (1.42 MHz < PSC < 2.12 MHz).

For the receiver, the requirement for a valid signal is that the duration of the low level signal must be greater than 2 cycles of the IrDA low power baud rate clock.

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Figure 24-18 IrDASIRENDEC-Block diagram

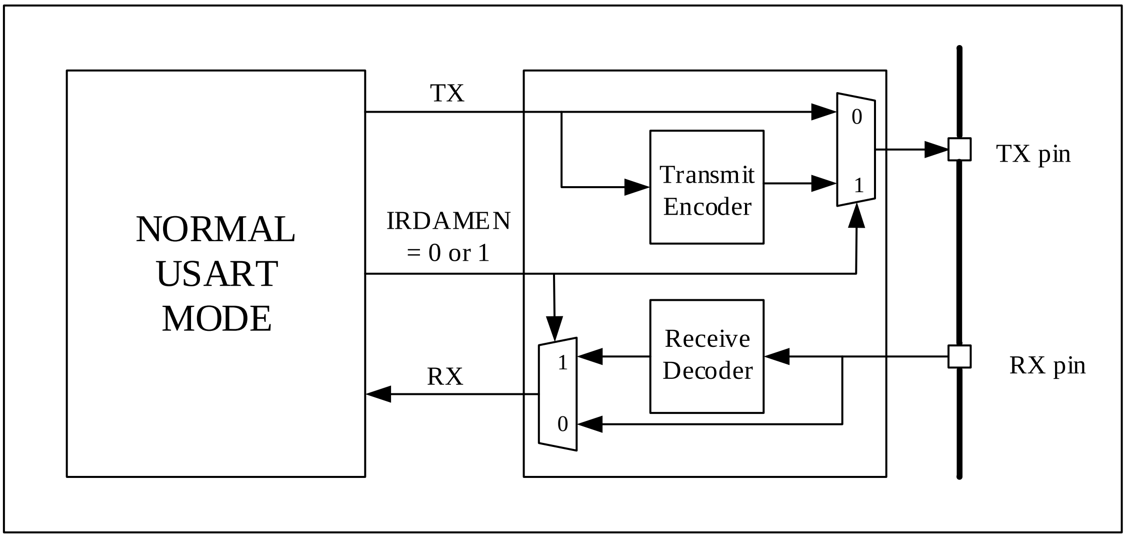
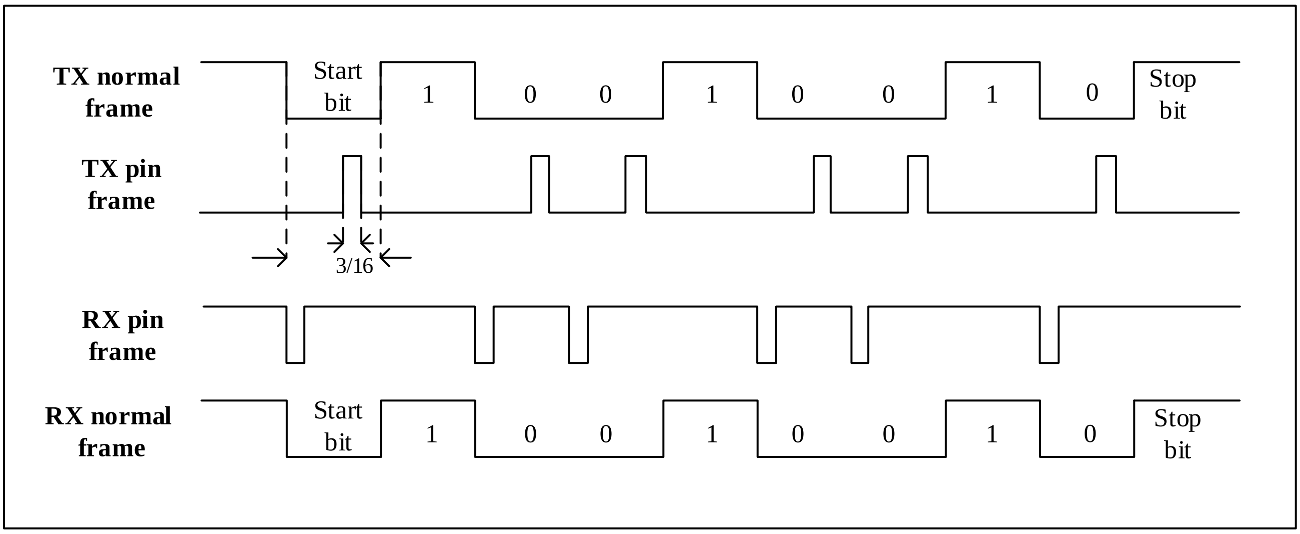


Figure 24-19 IrDA data Modulation (3/16)-normal mode



24.4.13 LIN mode

USART supports the ability of a LIN(Local interconnection Network) master to send a synchronization break and the ability of a LIN slave to detect a break. LIN mode can be enabled by configuring the USART_CTRL2.LINMEN bit.

Note: When using LIN mode, USART_CTRL2.STPB[1:0], USART_CTRL2.CLKEN, USART_CTRL3.SCMEN, USART_CTRL3.HDMEN, USART_CTRL3. IRDAMEN, these bits should be kept clear.

24.4.13.1 LIN transmitting

When LIN is sent, the length of the data bits sent can only be 8 bits. By setting USART_CTRL1.SDBRK, a 13-bit '0' will be sent as the break symbol, and insert a stop bit.

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24.4.13.2 LIN receiving

Whether the bus is idle or during the transmission of a data frame, as long as the break frame appears, it can be detected. the break symbol detection is independent of the USART receiver.

By configuring the USART_CTRL2.LINBDL bit, 10-bit or 11-bit break character detection can be selected.

After the receiver detects the start bit, the circuit samples each subsequent bit at the 8th, 9th, and 10th oversampling clock points of each bit. When 10 or 11 consecutive bits are detected as '0' and followed by a delimiter, it means that a LIN break is detected, and USART_STS.LINBDF is set. Before confirming the break symbol, check the delimiter as it means the RX line has gone back to high.An interrupt is generated if the LIN breaker detection interrupt (USART_CTRL2.LINBDIEN) is enabled.

If a '1' is sampled before the 10th or 11th sample point, the current detection is canceled and the start bit is searched again.

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Figure 24-20 Break detection in LIN mode (11-bit break length-the LINBDL bit is set)

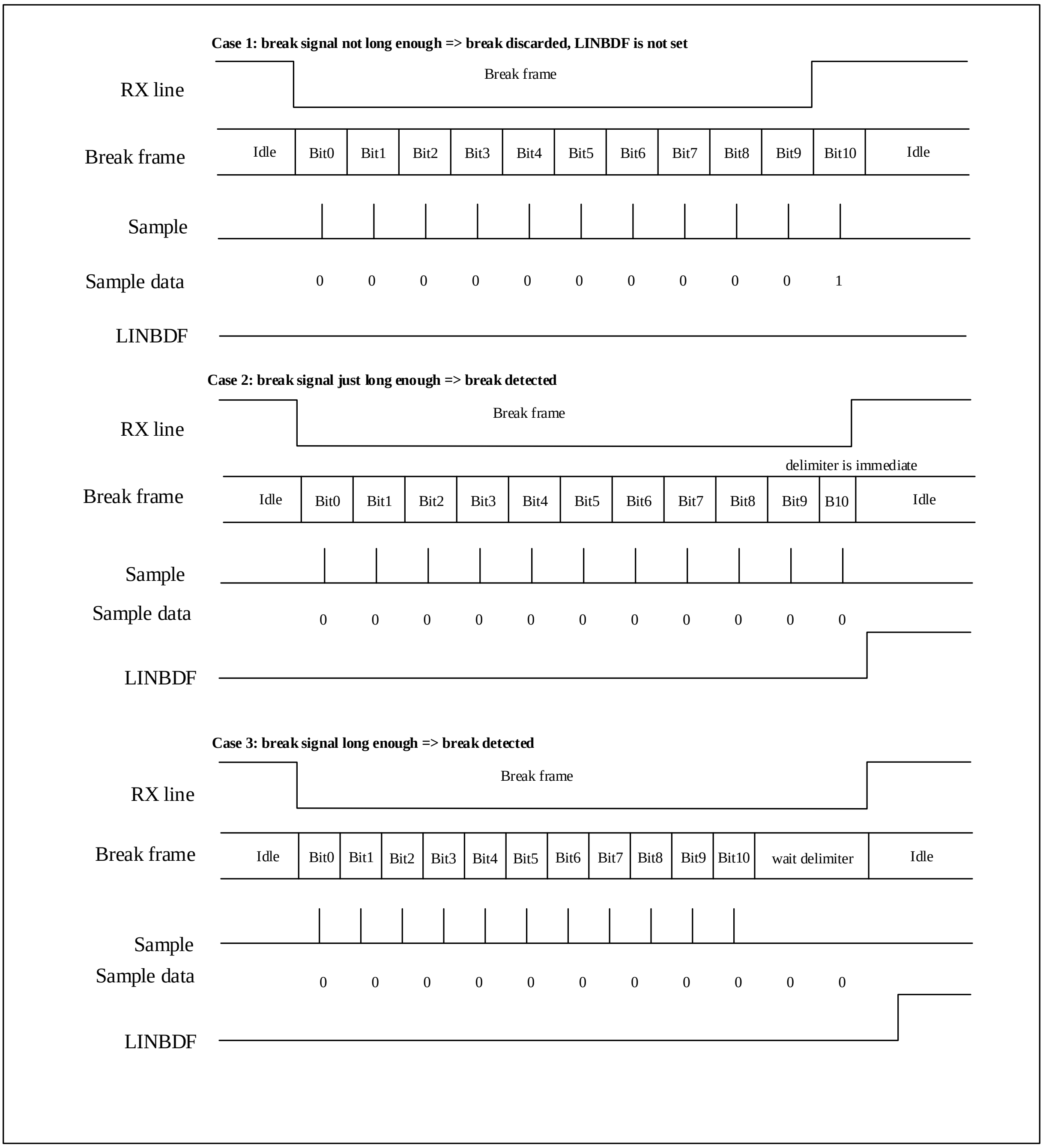

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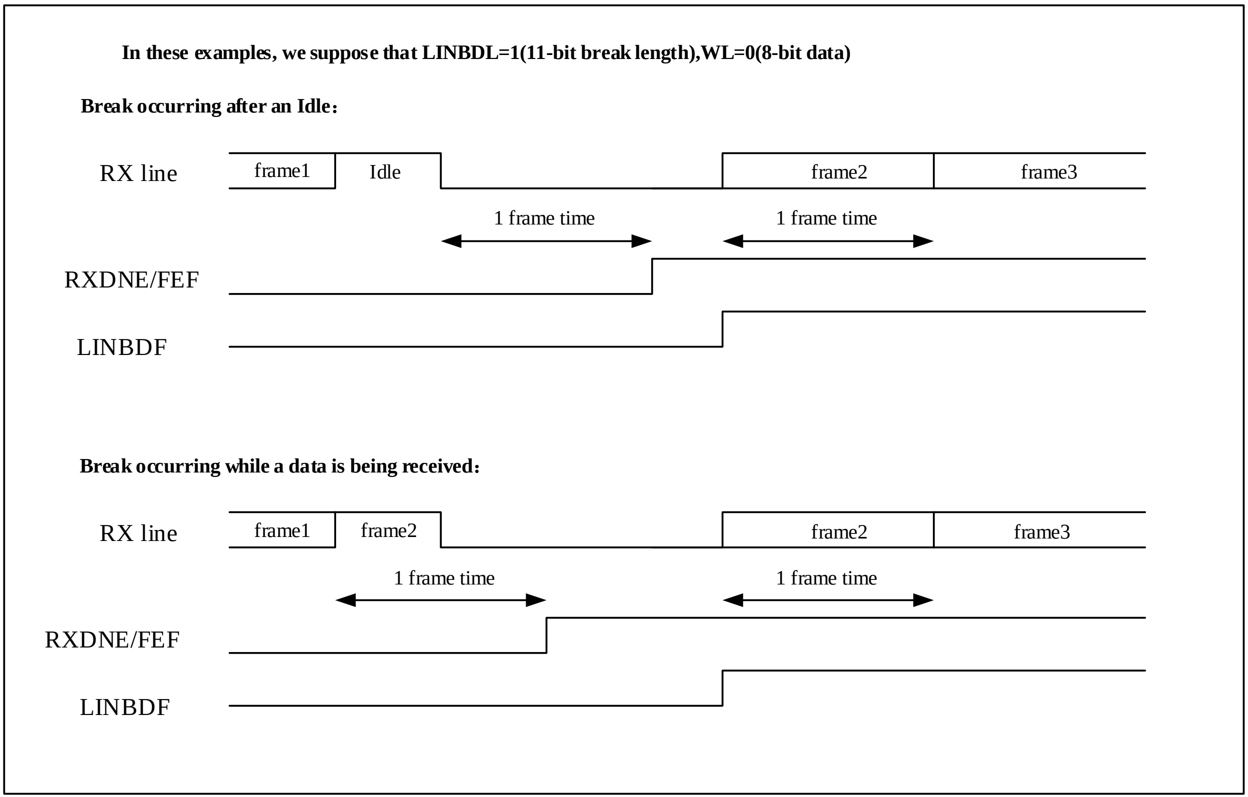
Figure 24-21 Break detection and framing error detection in LIN mode



24.4.14 Smartcard mode (ISO7816)

USART supports smart card protocol. The smart card interface supports the asynchronous smart card protocol defined in the ISO7816-3 standard.

Through the USART_CTRL3.SCMEN bit, you can choose whether to enable smart card mode. When using smart card mode, USART_CTRL2.LINMEN, USART_CTRL3.HDMEN, USART_CTRL3.IRDAMEN, these bits should be kept clear.

In smart card mode, the USART can provide a clock through the CK pin. The system clock is divided by the prescaler register to provide the clock to the smart card. The CK frequency can be from $f_{CK}/2$ to $f_{CK}/62$, where f_{CK} is the peripheral input clock.

In smart card mode, 0.5 and 1.5 stop bits can be used when receiving data, and only 1.5 stop bits can be used when sending data. So 1.5 stop bits are recommended as this avoids configuration transitions.

In smart card mode, the data bits should be configured as 8 bits, and the parity bit should be configured.

When a parity error is detected by receiver, the transmit data line is pulled low for one baud clock cycle at the end of the stop bit as NACK signal(If USART_CTRL3.SCNACK is set). This NACK signal will generate a framing error on the transmit side (transmit side is configured with 1.5 stop bits).

When the transmitter receives a NACK signal (framing error) from the receiver, it does not detect the NACK as a start bit (according to the ISO protocol, the duration of the received NACK can be 1 or 2 baud clock cycles).

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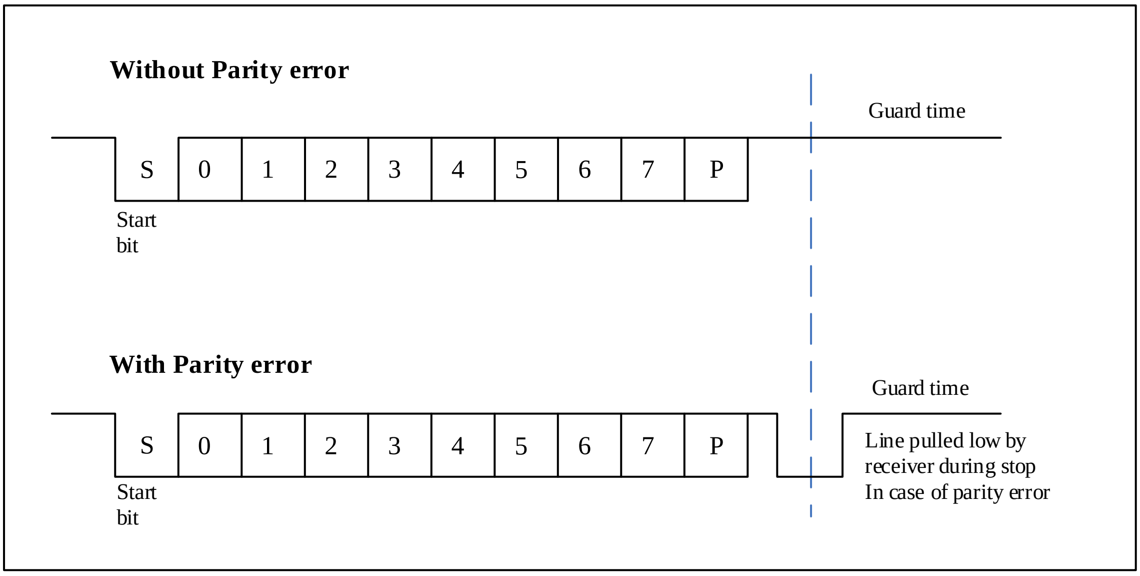
The example given in the following figure illustrates the signal on the data line with and without parity errors.

Figure 24-22 ISO7816-3 Asynchronous Protocol



The break frame has no meaning in smart card mode. A 00h data with a framing error will be treated as data instead of a break symbol.

Under normal operation, data will be shifted out of the transmit shift register on the next baud clock. The smart card mode is delayed by a minimum of 1/2 baud clock than normal operation.

In normal operation, USART_STS.TXC is set when a frame containing data is sent and USART_STS.TXDE=1.In smart card mode, the transmission completion flag (USART_STS.TXC) is set high when the guard time counter reaches the value (USART_GTP.GTV[7:0]). The clearing of the USART_STS.TXC flag is not affected by the smart card mode.

The following figure details how USART samples NACK signals.

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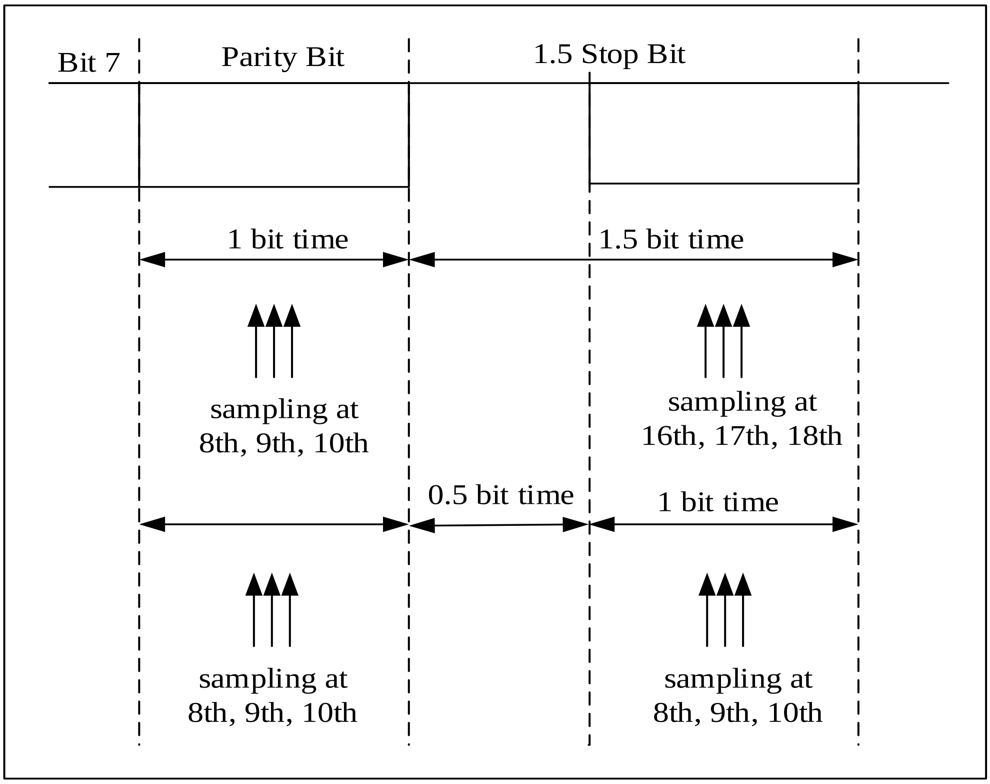
Figure 24-23 Use 1.5 stop bits to detect parity errors



24.5 Interrupt request

The various interrupt events of USART are logical OR relations, if the corresponding enable control bit is set, these events can generate their own interrupts, but only one interrupt request can be generated at the same time.

Table 24-7 USART interrupt request

Interrupt function	Interrupt event	Event flag	Enable bit
USART global interrupt	Transmission data register is empty.	TXDE	TXDEIEN
	CTS flag	CTSF	CTSIEN
	Transmission complete	TXC	TXCIEN
	Receive data ready to be read	RXDNE	RXDNEIEN
	Data overrun error detected.	ORERR	
	Idle line detected	IDLEF	IDLEIEN
	Parity error	PEF	PEIEN
	Disconnect flag	LINBDF	LINBDIEN

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	Noise, overrun error and framing error in multi-buffer communication	NEF/OREF/FEF	ERRIEN(1)

(1) This flag bit is used only when DMA is used to receive data(USART_CTRL3.DMARXEN=1).

24.6 Mode support

Table 24-8 USART mode setting (1)

Communication mode	USART1	USART2	USART3	UART4	UART5
Asynchronous mode	Y	Y	Y	Y	Y
Hardware flow control mode	Y	Y	Y	N	N
DMA communication mode	Y	Y	Y	Y	Y
Multiprocessor	Y	Y	Y	Y	Y
Synchronous mode	Y	Y	Y	N	N
Smartcard mode	Y	Y	Y	N	N
Single-wire half duplex mode	Y	Y	Y	Y	Y
IrDA infrared mode	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y

(1) Y = support this mode, N = do not support this mode

24.7 USART registers

24.7.1 USART register overview

Table 24-9 USART register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	USART_STS	Reserved																						CTSF	LINBDF	TXDE	TXC	RXDNE	IDLEF	OREF	NEF	FEF	PEF
	Reset Value																							0	0	1	1	0	0	0	0	0	0
004h	USART_DAT	Reserved																							DATV[8:0]								
	Reset Value																								0	0	0	0	0	0	0	0	0
008h	USART_BRCF	Reserved																DIV_Integer[11:0]												DIV_Decimal[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	USART_CTRL1	Reserved																		UEN	WL	WUM	PCEN	PSEL	PEIEN	TXDEIEN	TXCIEN	RXDNEIEN	IDLEIEN	TXEN	RXEN	RCVWU	SDBRK
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	USART_CTRL2	Reserved																	LINMEN	STPB [1:0]		CLKEN	CLKPOL	CLKPHA	LBCLK	Reserved	LINBDIEN	LINBDL	Reserved	ADDR[3:0]			
	Reset Value																		0	0	0	0	0	0	0		0	0		0	0	0	0
014h	USART_CTRL3	Reserved																					CTSIEN	CTSEN	RTSEN	DMATXEN	DMARXEN	SCMEN	SCNACK	HDMEN	IRDALP	IRDAMEN	ERRIEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
018h	USART_GTP	Reserved																GTV[7:0]								PSCV[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24.7.2 USART Status register (USART_STS)

Address offset : 0x00

Reset value : 0x0000 00C0

31–16
Reserved

15–10	9	8	7	6	5	4	3	2	1	0
Reserved	CTSF	LINBDF	TXDE	TXC	RXDNE	IDLEF	OREF	NEF	FEF	PEF
	rc_w0	rc_w0	r	rc_w0	rc_w0	r	r	r	r	r

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained
9	CTSF	CTS flag If USART_CTRL3.CTSEN bit is set, this bit is set by hardware when the nCTS input changes. If USART_CTRL3.CTSIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0:nCTS status line has not changed. 1:nCTS status line changes. *Note: This bit is invalid for UART4/5.*
8	LINBDF	LIN break detection flag. If USART_CTRL2.LINMEN bit is set, this bit is set by hardware when LIN disconnection is detected. If USART_CTRL2.LINBDIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0: LIN break character not detected. 1: LIN break character detected.
7	TXDE	The Transmit data register empty.

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Bit field	Name	Description
		Set to 1 after power-on reset or data to be sent has been sent to the shift register. Setting USART_CTRL1.TXDEIEN will generate an interrupt. This bit is cleared to 0 when the software writes the data to be sent into USART_DAT. 0: Send data buffer is not empty. 1: The transmitting data buffer is empty.
6	TXC	Transmission complete. This bit is set to 1 after power-on reset. If USART_STS.TXDE is set, this bit is set when the current data transmission is completed. Setting USART_CTRL1.TXCIEN bit will generate an interrupt. This bit is cleared by software. 0: Transmitting did not complete. 1: Send completed.
5	RXDNE	The Read data register not empty. This bit is set when the read data buffer receives data from the shift register. When USART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. Software can clear this bit by writing 0 to it or reading the USART_DAT register. 0: The read data buffer is empty. 1: The read data buffer is not empty.
4	IDLEF	IDLE line detected flag. Within one frame time, the idle state is detected at the RX pin, and this bit is set to 1. When USART_CTRL1.IDLEIEN bit is set, an interrupt will be generated. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No idle frame detected. 1: idle frame detected. *Note: IDLEF bit will not be set high again until USART_STS.RXDNE bit is set (that is, an idle line is detected again).*
3	OREF	Overrun error With RXDNE set, this bit is set if the USART_DAT register receives data from the shift register. When USART_CTRL3.ERRIEN bit is set, an interrupt will be generated. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No overrun error was detected. 1: Overflow error detected.
2	NEF	Noise error flag. When noise is detected in the received frame, this bit is set by hardware. It is cleared by the software sequence (read first USART_STS, read USART_DAT again). 0: No noise error detected. 1: Noise error detected. *Note: this bit will not generate an interrupt because it appears with USART_STS.RXDNE, and the hardware will generate an interrupt when setting the*

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Bit field	Name	Description
		USART_STS.RXDNE flag. In the multi-buffer communication mode, if the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the NEF flag is set.
1	FEF	Framing error. When the data is not synchronized or a large amount of noise is detected, and the stop bit is not received and recognized at the expected time, it will be judged that a framing error has been detected, and this bit will be set to 1. First read USART_STS, then read USART_DAT can cleared this bit. 0: No framing errors were detected. 1: A framing error or a Break Character is detected. *Note: this bit will not generate an interrupt because it appears with USART_STS.RXDNE, and the hardware will generate an interrupt when setting the USART_STS.RXDNE flag. If the currently transmitted data has both framing errors and overload errors, the hardware will continue to transmit the data and only set the USART_STS.OREF flag bit.* *In the multi-buffer communication mode, if the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the FEF flag is set.*
0	PEF	Parity error. This bit is set when the parity bit of the received data frame is different from the expected check value. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No parity error was detected. 1: Parity error detected.

24.7.3 USART Data register (USART_DAT)

Address offset : 0x04

Reset value : undefined (uncertain value)

31–16
Reserved

15–9	8–0
Reserved	DATV[8:0]
	rw

Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	DATV[8:0]	Data value Contains the data sent or received; Software can change the transmitted data by writing these bits, or read the values of these bits to obtain the received data.

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Bit field	Name	Description
		If parity is enabled, when the transmitted data is written into the register, the highest bit of the data (the 7th or 8th bit depends on USART_CTRL1.WL bit) will be replaced by the parity bit.

24.7.4 USART Baud rate register (USART_BRCF)

Address offset : 0x08

Reset value : 0x0000 0000

Note: When USART_CTRL1.UEN=1, this register cannot be written;The baud counter stops counting if USART_CTRL1.TXEN or USART_CTRL1.RXEN are disabled respectively.

31–16
Reserved

15–4	3–0
DIV_Integer[11:0]	DIV_Decimal[3:0]
rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:4	DIV_Integer[11:0]	Integer part of baud rate divider.
3:0	DIV_Decimal[3:0]	Fractional part of baud rate divider.

24.7.5 USART control register 1 register (USART_CTRL1)

Address offset : 0x0C

Reset value : 0x0000 0000

31–16
Reserved

15–14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	UEN	WL	WUM	PCEN	PSEL	PEIEN	TXDE IEN	TXC IEN	RXDNE IEN	IDLE IEN	TXEN	RXEN	RCVWU	SDBRK
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13	UEN	USART enable When this bit is cleared, the divider and output of USART stop working after the current byte transmission is completed to reduce power consumption. Software can set or clear this bit. 0:USART is disabled.

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Bit field	Name	Description
		1:USART is enabled.
12	WL	Word length. 0:8 data bits. 1:9 data bits. *Note: If data is in transit, this bit cannot be configured.*
11	WUM	Wake up mode from mute mode. 0: Idle frame wake up. 1: Address identifier wake up.
10	PCEN	Parity control enable 0: Parity control is disabled. 1: Parity control is enabled.
9	PSEL	Parity selection. 0: even check. 1: odd check.
8	PEIEN	PE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.PEF bit is set. 0: Parity error interrupt is disabled. 1: Parity error interrupt is enabled.
7	TXDEIEN	TXDE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.TXDE bit is set. 0: Send buffer empty interrupt is disabled. 1: Send buffer empty interrupt is enabled.
6	TXCIEN	Transmit complete interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.TXC is set. 0: Transmission completion interrupt is disabled. 1: Transmission completion interrupt is enabled.
5	RXDNEIEN	RXDNE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.RXDNE or USART_STS.OREF is set. 0: Data buffer non-empty interrupt o and overrun error interrupt are disabled. 1: Data buffer non-empty interrupt o and overrun error interrupt are enabled.
4	IDLEIEN	IDLE interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.IDLEF is set. 0:IDLE line detection interrupt is disabled. 1: IDLE line detection interrupt is enabled.
3	TXEN	Transmitter enable. 0: The transmitter is disabled. 1: the transmitter is enabled.
2	RXEN	Receiver enable 0: The receiver is disabled. 1: the receiver is enabled.

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Bit field	Name	Description
1	RCVWU	The receiver wakes up Software can set this bit to 1 to make USART enter mute mode, and clear this bit to 0 to wake up USART. In idle frame wake-up mode (USART_CTRL1.WUM=0), this bit is cleared by hardware when an idle frame is detected. In address wake-up mode (USART_CTRL1.WUM=1), when an address matching frame is received, this bit is cleared by hardware. Or when an address mismatch frame is received, it is set to 1 by hardware. 0: The receiver is in normal operation mode. 1: The receiver is in mute mode.
0	SDBRK	Send Break Character. The software transmits a break character by setting this bit to 1. This bit is cleared by hardware during stop bit of the break frame transmission. 0: No break character was sent. 1: Send a break character.

24.7.6 USART control register 2 register (USART_CTRL2)

Address offset : 0x10

Reset value : 0x0000 0000

31:16
Reserved

15	14	13:12	11	10	9	8	7	6	5	4	3:0
Reserved	LINMEN	STPB[1:0]	CLKEN	CLKPOL	CLKPHA	LBCLK	Reserved	LINBD IEN	LINBDL	Reserved	ADDR[3:0]
	rw	rw	rw	rw	rw	rw		rw	rw		rw

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
14	LINMEN	LIN mode enable 0:LIN mode is disabled 1:LIN mode enabled
13:12	STPB[1:0]	STOP bits. 00:1 stop bit. 01:0.5 stop bit. 10:2 stop bit. 11:1.5 stop bit. *Note: For UART4/5, only one stop bit and two stop bits are valid.*
11	CLKEN	Clock enable 0:CK pin is disabled 1:CK pin enabled

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Bit field	Name	Description
		Note: This bit cannot be used for UART4/5.
10	CLKPOL	Clock polarity. This bit is used to set the polarity of CK pin in synchronous mode. 0: CK pin remains low when it is not transmitted to the outside. 1: CK pin remains high when it is not sent to the outside. *Note: This bit is invalid for UART4/5.*
9	CLKPHA	Clock phase. This bit is used to set the phase of CK pin in synchronous mode. 0: Sample the first data at the first clock edge. 1: Sample the first data at the second clock edge. *Note: This bit cannot be used for UART4/5.*
8	LBCLK	The Last bit clock pulse. This bit is used to set whether the clock pulse corresponding to the last transmitted data byte (MSB) is output on CK pin in synchronous mode. 0: The clock pulse of the last bit of data is not output from CK. 1: The clock pulse of the last bit of data will be output from CK. *Note: This bit cannot be used for UART4/5.*
7	Reserved	Reserved, the reset value must be maintained
6	LINBDIEN	LIN break detection interrupt enable. If this bit is set to 1, an interrupt will be generated when USART_STS.LINBDF bit is set. 0: Disconnect signal detection interrupt is disabled. 1: Turn-off signal detection interrupt enabled
5	LINBDL	LIN break detection length. This bit is used to set the length of the break frame. 0:10 bit break detection 1:11 bit break detection *Note: LINBDL can be used to control the detection length of Break Characters in LIN mode and other modes, and the detection length is the same as that in LIN mode.*
4	Reserved	Reserved, the reset value must be maintained
3:0	ADDR[3:0]	USART address. Used in the mute mode of multiprocessor communication, using address identification to wake up a USART device. In address wake-up mode (USART_CTRL1.WUM=1), if the lower four bits of the received data frame are not equal to the ADDR[3:0] value, USART will enter the mute mode; If the lower four bits of the received data frame are equal to the ADDR[3:0] value, USART will be awakened.

24.7.7 USART control register 3 register (USART_CTRL3)

Address offset : 0x14

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Reset value : 0x0000 0000

31–16										
Reserved										

15–11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CTSIEN	CTSEN	RTSEN	DMATXEN	DMARXEN	SCMEN	SCNACK	HDMEN	IRDALP	IRDAMEN	ERRIEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	CTSIEN	CTS interrupt enable. If this bit is set to 1, an interrupt will be generated when USART_STS.CTSF bit is set. 0:CTS interrupt is disabled. 1:CTS interrupt is enabled. *Note: This bit cannot be used for UART4/5*
9	CTSEN	CTS enable. This bit is used to enable the CTS hardware flow control function. 0:CTS hardware flow control is disabled. 1:CTS hardware flow control is enabled. *Note: This bit cannot be used for UART4/5*
8	RTSEN	RTS enable. This bit is used to enable RTS hardware flow control function. 0:RTS hardware flow control is disabled. 1:RTS hardware flow control is enabled. *Note: This bit cannot be used for UART4/5*
7	DMATXEN	DMA transmitter enable. 0:DMA transmission mode is disabled. 1:DMA transmission mode is enabled.
6	DMARXEN	DMA receiver enable. 0:DMA receive mode is disabled. 1:DMA receive mode is enabled.
5	SCMEN	Smartcard mode enable. This bit is used to enable Smartcard mode. 0: Smartcard mode is disabled. 1: Smartcard mode is enabled. *Note: This bit cannot be used for UART4/5*
4	SCNACK	Smartcard NACK enable. This bit is used for Smartcard mode to enable transmitting NACK when parity error occurs. 0: Do not send NACK when there is a parity error. 1: send NACK when there is a parity error. *Note: This bit cannot be used for UART4/5*

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Bit field	Name	Description
3	HDMEN	Half-duplex mode enable. This bit is used to enable half-duplex mode. 0: Half-duplex mode is disabled. 1: Half-duplex mode is enabled.
2	IRDALP	IrDA low-power mode. This bit is used to select the low power consumption mode for IrDA mode. 0: Normal mode. 1: Low power mode.
1	IRDAMEN	IrDA mode enable. 0:IrDA is disabled. 1:IrDA is enabled.
0	ERRIEN	Error interrupt enable. When DMA receive mode (USART_CTRL3.DMARXEN=1) is enabled, an interrupt will be generated when USART_STS.FEF, USART_STS. OREF or USART_STS. NEF bit is set. 0: Error interrupt is disabled. 1: Error interrupt enabled.

24.7.8 USART guard time and prescaler register (USART_GTP)

Address offset : 0x18

Reset value : 0x0000 0000

31–16	
Reserved	

15–8	7–0
GTV[7:0]	PSCV[7:0]
rw	rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	GTV[7:0]	Guard time value in Smartcard mode. This bit field specifies the guard time in baud clock. In Smartcard mode, this function is required. The setting time of USART_STS.TXC flag is delayed by GTV[7:0] baud clock cycles. *Note: This bit is invalid for UART4/5.*
7:0	PSCV[7:0]	Prescaler value. In IrDA low power consumption mode: these bits are used to set the frequency division coefficient for dividing the peripheral clock (PCLK1/PCLK2) to generate low power consumption frequency. 00000000: reserved-do not write this value.

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		00000001: divide the source clock by 1. … 11111111: divide the source clock by 255. In IrDA normal mode: PSCV can only be set to 00000001. In Smartcard mode: PSCV[4:0] is used to set the frequency division of Smartcard clock generated by peripheral clock (PCLK1/ PCLK2). Coefficient. The actual frequency division coefficient of is twice the set value of PSCV[4:0]. 0000: reserved-do not write this value. 0001: Divide the source clock by 2. 0010: Divide the source clock by 4. … 1111: Divide the source clock by 62. In Smartcard mode, PSCV[7:5] is reserved. *Note: This bit is invalid for UART4/5.*

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25 Low power universal asynchronous receiver transmitter (LPUART)

25.1 Introduction

Low power universal asynchronous receiver transmitter (LPUART) is a low power, full duplex, asynchronous serial communication interface. The LPUART can be clock provided by LSE, HSI, SYSCLK and PCLK1. When 32.768kHz LSE is selected as the clock source, the LPUART can work in STOP2 low-power mode with a maximum communications up to 9600bps. LPUART supports receiving data wake-up. By configuring wake-up events, the CPU in STOP2 mode can be woken up.

At the same time, when MCU works in RUN mode, LPUART can also be used as a common asynchronous serial port. Users can switch the clock source to HSI, SYSCLK and PCLK1 to obtain higher communication speed.

25.2 Main features

- Full duplex asynchronous communication
- Selectable clock source of HSI, LSE, SYSCLK, or PCLK1
- Fractional baud rate generator system: Programmable baud rate shared by sending and receiving up to 1Mbits/s;baud rates from 300bps to 9600bps when using 32.768 kHz clock source (LSE)
- Fixed 8-bit data word length, 1 stop bit and optional 1 parity bit
- Support DMA data transfer
- Support hardware flow control
- Transfer detection flag: Receive buffer full, Receive buffer half full, Receive buffer not empty, Receive buffer overrun, Transmission complete
- Parity control: Odd and even parity selection, Parity can be disable
- Error detection flag: Parity error, Overrun error, Noise error
- 32 byte receive buffer
- Baud rate error correction at low frequencies
- Configurable sampling method of 1 or 3 samples
- Noise detection
- Configurable flow control RTS threshold
- Support STOP2 mode Configurable source mode
    - Start bit detection
    - Receive buffer non-empty detection
    - A configurable receive byte
    - A programmable 4-byte frame

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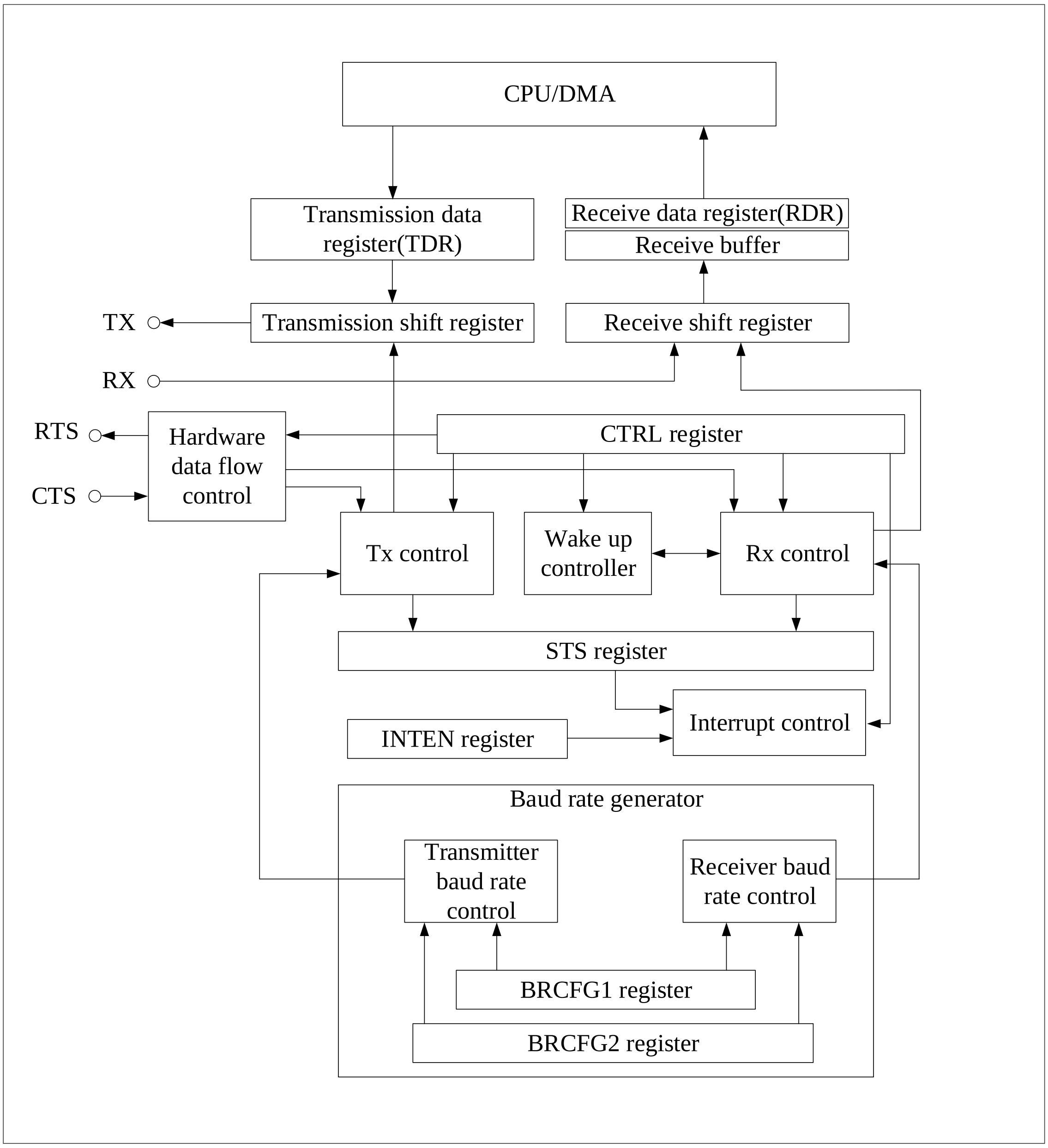
25.3 Functional block diagram

Figure 25-1 LPUART block diagram



25.4 Function description

As shown in Figure 25-1, LPUART bidirectional communication requires at least two pins: receiving data input (RX) and sending data output (TX).

RX: Serial data input. When the number of samples is 3, data and noise can be distinguished.

TX: Serial data output. When sending is enabled, the pin defaults to be high level.

The following pins are required in hardware flow control mode:

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CTS (Clear To Send): When transmitter detects that CTS is valid (low level), the next data is sent.

RTS (Request To Send): When receiver is ready to receive new data, pull the RTS pin low.

LPUART has the following characteristics:

- Idle status without sending or receiving
- A start bit
- A data word (8 bits) with the least significant bits first
- A stop bit, indicating the end of a data frame
- A status register (LPUART_STS)
- Data register (LPUART_DAT)
- Two baud rate configuration registers (LPUART_BRCFG1 and LPUART_BRCFG2) using fractional baud rate generators:16-bit integer and 8-bit decimal representations

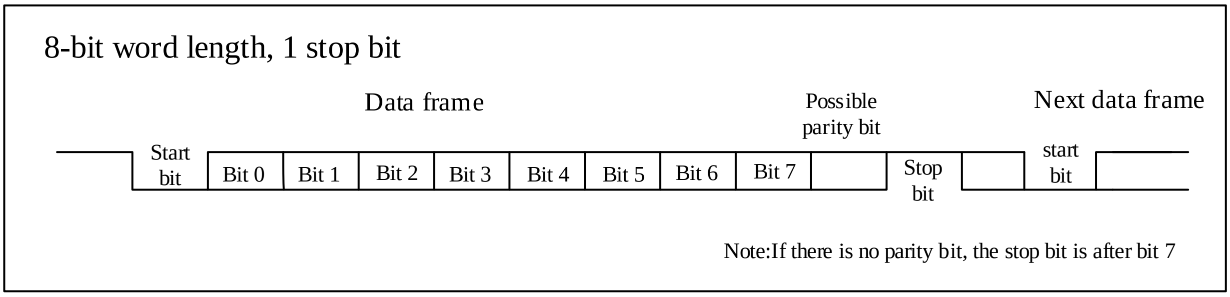
For specific definitions of each bit in the registers above, please refer to Section 25.6 of register Description.

25.4.1 LPUART frame format

The LPUART data word length is fixed at 8 bits (see Figure 25-2). During the start bit, TX pin is at a low level and during the stop bit it is at a high level. The parity bit follows the data word when enabled.

Both sending and receiving are driven by two different baud clock generators. When the LPUART_CTRL.TXEN of transmitter is set, the corresponding baud clock generator generates baud clock. When the start bit is received, the receiver's corresponding baud clock generator generates the clock.

Figure 25-2 frame format



Note: in this chapter, unless special instruction, setting means that a register is set to state '1', and resetting or clearing means that a register is set to state '0'. Hardware or programs may set or clear a register. Please refer to this chapter for details.

25.4.2 Transmitter

When the Transmit Enable bit (LPUART_CTRL.TXEN) is set and there is data in the buffer, the transmitter sends 8-bit data words. The data in the shift register is output on the TX pin.

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25.4.2.1 Transmi process

During an LPUART transmission, the least significant bit of the data is shifted out on TX pin. In this mode, the LPUART_DAT register contains a buffer between the internal bus and the transmitter shift register (see Figure 25-1).

Each character is preceded by a low level starting bit; and is terminated by a stop bit.

Note: You cannot reset the LPUART_CTRL.TXEN bit during data transfer, otherwise the data on the TX pin will be corrupted because the baud rate counter stops counting. The current data being transferred will be lost.

The LPUART sends data as follows:

1. Configure baud rate, parity check, DMA, flow control, etc.
2. Set the LPUART_CTRL.TXEN bit to enable data transmission.
3. Write data to the LPUART_DAT register.
4. Check if the LPUART_STS.TXC flag is set, it means the transmission is over. If the flag is set, write 1 to the LPUART_STS.TXC bit to clear the flag.
5. Check the LPUART_STS.PEF bit to confirm whether the parity is wrong.
6. Otherwise, go to Step 3 and send the next data.

Note: Be sure to initialize the LPUART module before using the transmitter.

LPUART initialization as follows:

1. Set all flag bits in the LPUART_STS register to clear the interrupt flag.
2. To enable the interrupt function, configure LPUART_INTEN.
3. Set LPUART_CTRL.FLUSH clear the RX buffer.

When send data:

- After configuring the baud rate and setting LPUART_CTRL.TXEN, the CPU can write directly to the LPUART_DAT register to send data.
- When a frame transmission is completed (after the stop bit is sent), the LPUART_STS.TXC bit is set. If the LPUART_INTEN.TXCIE bit is set, an interrupt occurs immediately.
- After the last data byte is written to the LPUART_DAT register, you must wait for LPUART_STS.TXC=1 before shutting down the LPUART module or setting the microcontroller into low-power mode.

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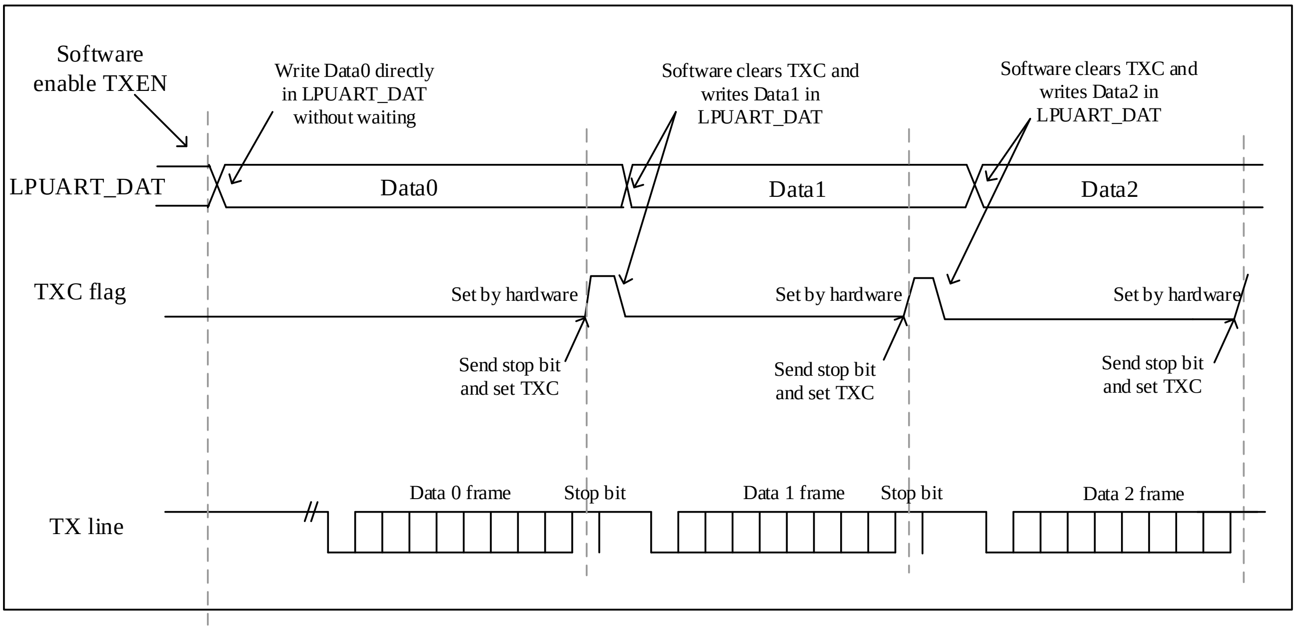
Figure 25-3 TXC changes during transmission



25.4.3 Receiver

25.4.3.1 Start bit detection

If the LPUART_CTRL.SMPCNT bit is 0, that is, the number of samples is 3, when there are at least two 0s in the three sample numbers, the start bit is valid. Otherwise it will be invalid.

Sampling values	NF state	Received bit value	Start bit validity
000	0	0	effective
001	1	0	effective
010	1	0	effective
011	1	1	invalid
100	1	0	effective
101	1	1	invalid
110	1	1	invalid
111	0	1	invalid

25.4.3.2 Receive process

During LPUART reception, the least significant bits of data are first moved in from the RX pin. In this mode, the LPUART_DAT register contains a buffer between the internal APB bus and the receive shift register.

The steps for LPUART to receive data are as follows:

1. Configure baud rate, parity check, wake up event/enable, sampling mode, DMA, flow control, etc.

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2. Check the interrupt flags of the LPUART_STS register: buffer is not empty, buffer is half full, buffer is full, buffer overrun;
3. Read the data by reading the LPUART_DAT register.
4. Return to Step 2 and continue receiving data.

Note: Please be sure to initialize the LPUART module before using the receiver.

When receiving a data frame:

- The LPUART_STS.FIFO_NE bit is set, and the contents of the shift register are transferred to the RDR (Receiver Data Register). In other words, the data has been received and can be read (including its associated error flags).
- If the LPUART_INTEN.FIFO_NEIEN bit is set, an interrupt is generated.
- Frame errors (parity detection errors), noise or overrun errors are detected during reception, so the error flag will be set.
- In multi-buffer communication mode, the LPUART_STS.FIFO_NE flag bit is placed after each byte received and cleared by DMA's read operation on the data register.
- In single buffer mode, the software can clear LPUART_STS.FIFO_NE bits by reading the LPUART_DAT register or by writing 0.The LPUART_STS.FIFO_NE bit must be cleared before the end of the next frame of data reception to avoid overrun errors.

25.4.3.3 Overrun error

The LPUART receiving data buffer has a total of 32 bytes. The LPUART_STS.FIFO_FU flag will be set after receiving 32 bytes of data. When the buffer data is not read out and causes LPUART_STS.FIFO_FU to be not reset in time, if next character is received, an overrun error occurs. This character will be discarded by the hardware. Data can only be transferred from the shift register to the receiving data buffer if the LPUART_STS.FIFO_FU bit is cleared. If the next data has been received or the previous DMA request has not been served, the LPUART_STS.FIFO_FU flag is still set and an overrun error occurs.

When an overrun error occurs:

- The LPUART_STS.FIFO_OV bit is set.
- The receiving data buffer content will not be lost. Reading the LPUART_DAT register still returns the previous data.
- The contents of the shift register will be overwritten. Any subsequent data received will be lost.
- If the LPUART_INTEN.FIFO_OVIE bit is set, an interrupt is generated.
- LPUART_DAT register read operation, reset LPUART_STS.FIFO_OV.

25.4.3.4 Noise error

Noise errors use an over-sampling technique (if the LPUART_CTRL.SMPCNT bit is 0, that is, the number of samples is 3) to recover data by distinguishing valid input data from noise.

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Figure 25-4 Data sampling for noise detection

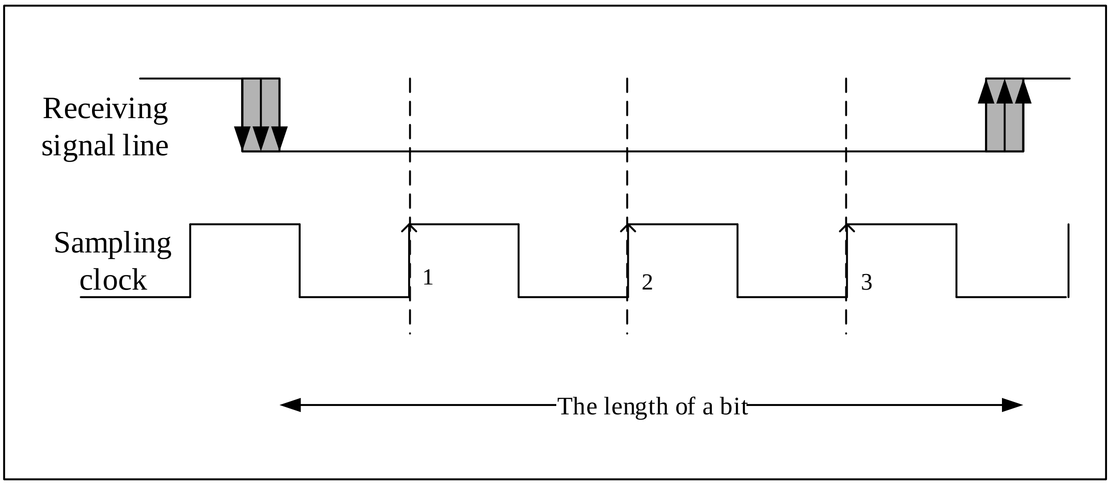

Table 25-1 Data sampling for noise detection

Sampling values	NF state	Received bit value
000	0	0
001	1	0
010	1	0
011	1	1
100	1	0
101	1	1
110	1	1
111	0	1

When noise is detected in a receiving frame, you can do the following:

- If three sample values are inconsistent, set the LPUART_STS.NF flag immediately.
- The received data is transferred from the shift register to the buffer.
- Software write 1 clears the LPUART_STS.NF flag bit.

25.4.4 Fractional baud rate generation

Baud rate frequency division coefficient is divided into 16-bit integer part and 8-bit decimal part. The baud rate generator uses the value of the combination of these two parts to determine the baud rate. The fractional baud rate divider will enable the LPUART to generate all standard baud rates.

Baud rate frequency division coefficient (LPUARTDIV) has the following relationship with system clock (PCLK) :

$$\text{TX/RX baud rate} = f_{CLK}/(\text{LPUARTDIV})$$

Here the f_{CLK} is the clock for LPUART (the clock source of LPUART can be HSI, LSE, SYSCLK, or PCLK1).

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The value of LPUARTDIV is set in the baud rate configuration registers LPUART_BRCFG1 and LPUART_BRCFG2

Note: After writing LPART_BRCFG1 and LPUART_BRCFG2, the baud rate counter is replaced with the new value of the baud rate register. Therefore, do not change the value of the baud rate register during communication.

25.4.4.1 Configure baud rates through LPUART_BRCFG1 and LPUART_BRRCFG2

For example, baud rate = 4800bps, clock frequency = 32768Hz.

LPUARTDIV = 32768/4800 = 6.82667.LPUART_BRCFG1 = 6 and the value of LPUART_BRCFG2 is calculated by adding fractions in the table below (the value of LPUART_BRCFG2 is 0xEFh).

Decimal addition	Carry to the next integer	Bit field	Value
0.82667 + 0.82667 = 1.65333	YES	DECIMAL0	1
1.65333 + 0.82667 = 2.48000	YES	DECIMAL1	1
2.48000 + 0.82667 = 3.30667	YES	DECIMAL2	1
3.30667 + 0.82667 = 4.13333	YES	DECIMAL3	1
4.13333 + 0.82667 = 4.96000	NO	DECIMAL4	0
4.96000 + 0.82667 = 5.78667	YES	DECIMAL5	1
5.78667 + 0.82667 = 6.61333	YES	DECIMAL6	1
6.61333 + 0.82667 = 7.44000	YES	DECIMAL7	1

When LSE clock (32.768KHz) is used, the values of baud rate configuration registers LPUART_BRCFG1 and LPUART_BRCFG2 with different baud rate Settings are as follows:

Baud rate	Divisor	LPUART_BRCFG1	LPUART_BRCFG2
300	109.2267	6Dh	88h
600	54.6133	36h	ADh
1200	27.3067	1Bh	24h
2400	13.6533	0Dh	6Dh
4800	6.8267	06h	EFh
9600	3.4133	03h	4Ah

Note: The lower the clock frequency of the CPU, the lower the accuracy of a particular baud rate.

If the MCU is powered by 3.3V, the LPUART baud rate should be within 1Mbps, and if the MCU is powered by 1.8V, the LPUART baud rate should be within 115200bps.

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25.4.5 Parity control

Reset the LPUART_CTRL.PCDIS bit, enable parity control (generate a parity bit when sending, parity check when receiving), set or reset the LPUART_CTRL.PSEL bit selection to use odd or even check. LPUART frame formats are listed in the table below.

Table 25-2 Parity frame format

PCDIS bit	LPUART frame
0	| Start bit | 8-bit data | parity bit | stop bit |
1	| Start bit | 8 bits data | stop bit |

Transfer mode: Parity is enabled by resetting the LPUART_CTRL.PCDIS bit. If parity fails, the LPUART_STS.PEF flag is set to '1', and an interrupt occurs if LPUART_INTEN.PEIE is set.

Odd parity: LPUART_CTRL.PSEL＝1.

Make the number of '1' in one frame data (including parity bit) be an odd number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total).

Even parity: LPUART_CTRL.PSEL＝0.

Make the number of '1' in one frame data (including parity bit) be an even number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total).

25.4.6 DMA application

LPUART can access the transmit data register (TDR) and receive buffer respectively through DMA.

25.4.6.1 DMA transmission

The steps for assigning a DMA channel to the LPUART transmissions are as follows (x indicates the channel number) :

1. Configure the LPUART_DAT register address as the destination address for DMA transfer, and the memory address as the source address for DMA transfer.
2. Set the total number of bytes to be transmitted.
3. Set the channel priority.
4. Configure to generate DMA interrupts when the transfer is half or all complete.
5. Activate the channel.

Completing a DMA transfer will generate an interrupt on the corresponding DMA channel. In transmission mode, when the DMA has finished the data transfer, the DMA controller sets the DMA_INTSTS.TXCFx flag. The LPUART_STS.TXC flag bit is asserted by the hardware to indicate that the transfer is completed. The software needs wait for LPUART_STS.TXC=1.

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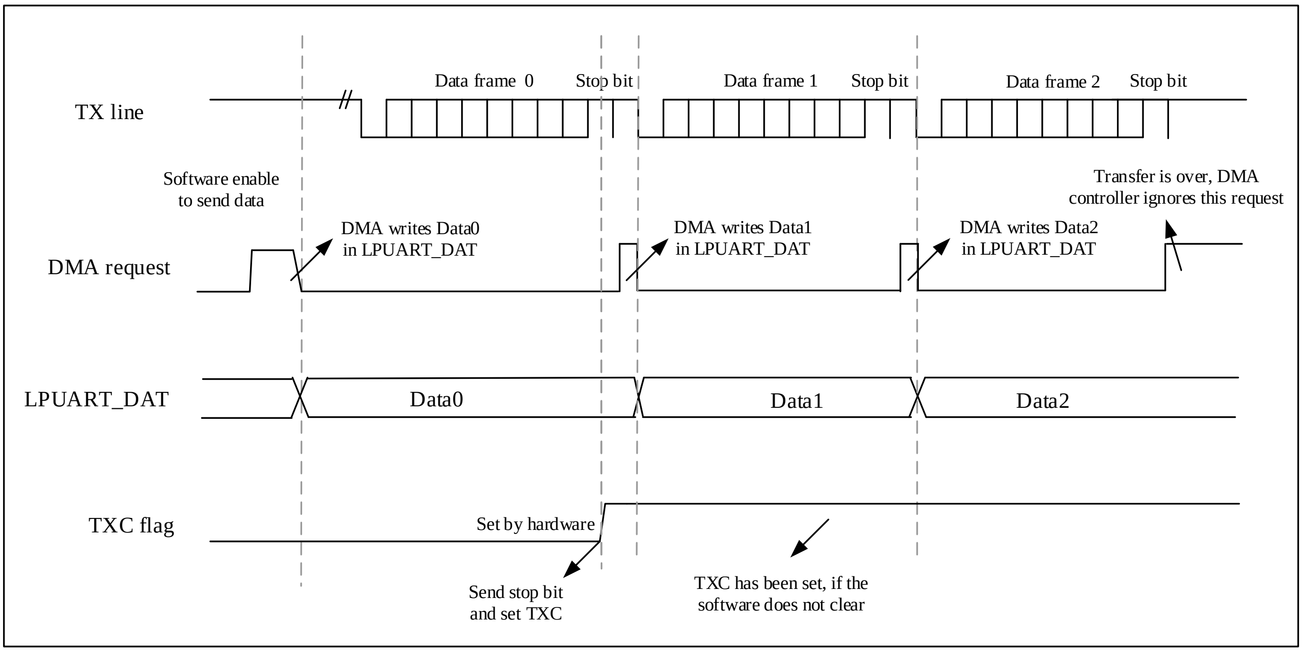
Figure 25-5 Sending using DMA



25.4.6.2 DMA reception

The steps for assigning a DMA channel to the LPUART receiving are as follows (x indicates the channel number) :

1. Configure the LPUART_DAT register address as the source address for transmission and the memory address as the destination address for transmission through the DMA configuration register.
2. Configure the number of DMA bytes to be transferred.
3. Configure the channel priority on the DMA register for data transfer.
4. Configure interrupts to generate DMA interrupts when the transfer is half or all complete.
5. Activate the channel.

When completing the transfer specified by the DMA controller, the DMA controller generates an interrupt on the DMA channel's interrupt vector.

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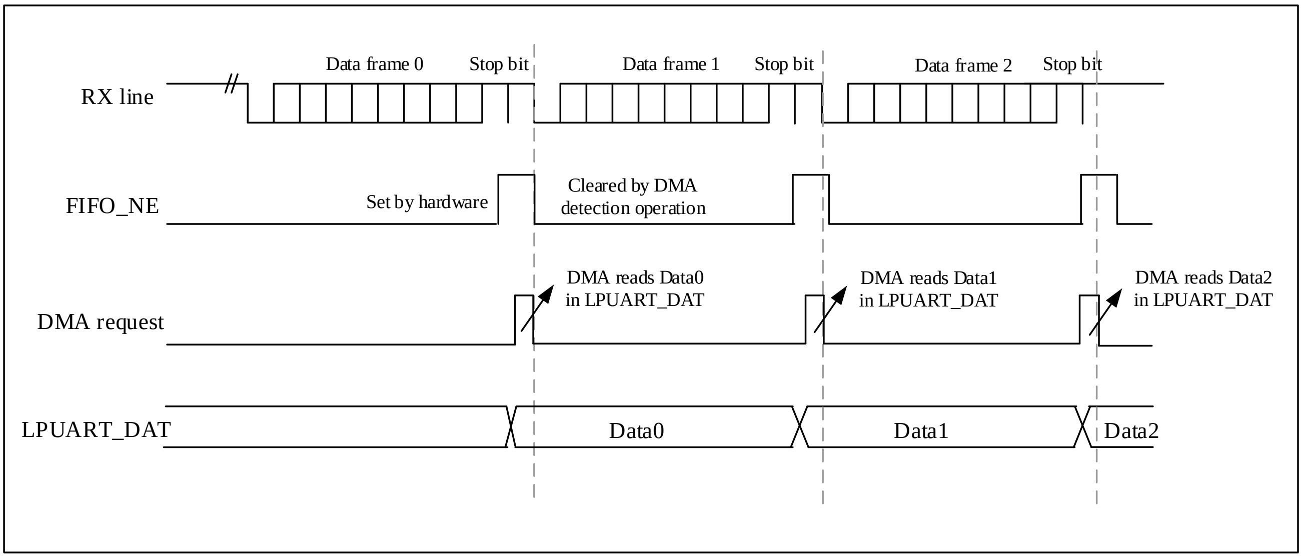
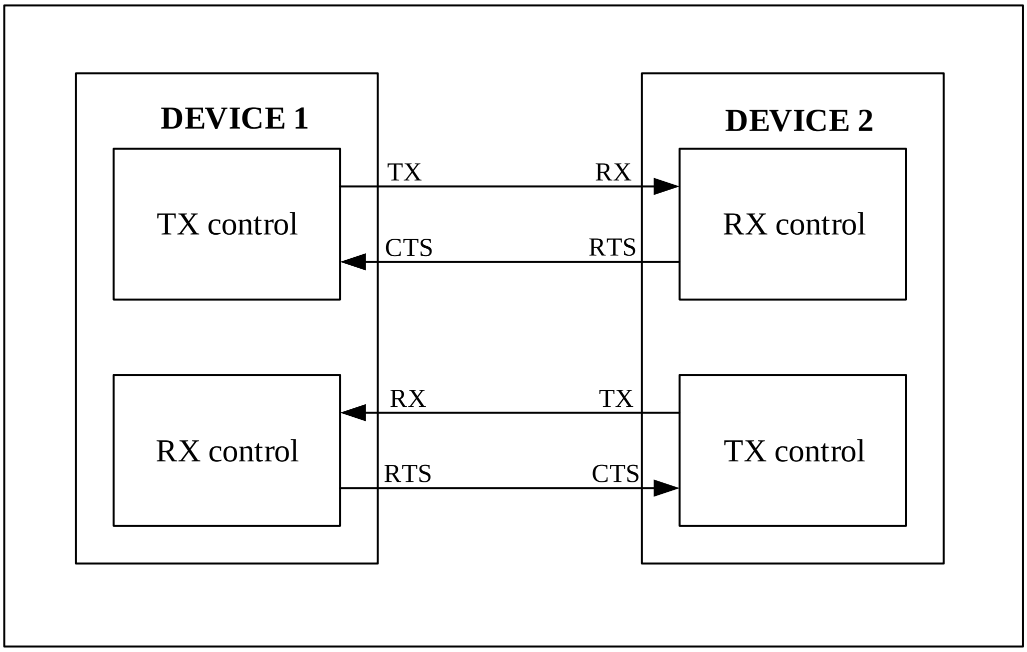
Figure 25-6 Receiving with DMA



25.4.7 Hardware flow control

Hardware flow control functions through CTS input and RTS output. The following figure shows how two devices are connected in this mode.

Figure 25-7 Hardware flow control between two LPUART



RTS and CTS flow control can be independently enabled by setting LPUART_CTRL.RTSEN and LPUART_CTRL.CTSEN.

25.4.7.1 RTS flow control

If RTS flow control is enabled (LPUART_CTRL.RTSEN=1), the RTS will be driven high (active) when the RTS

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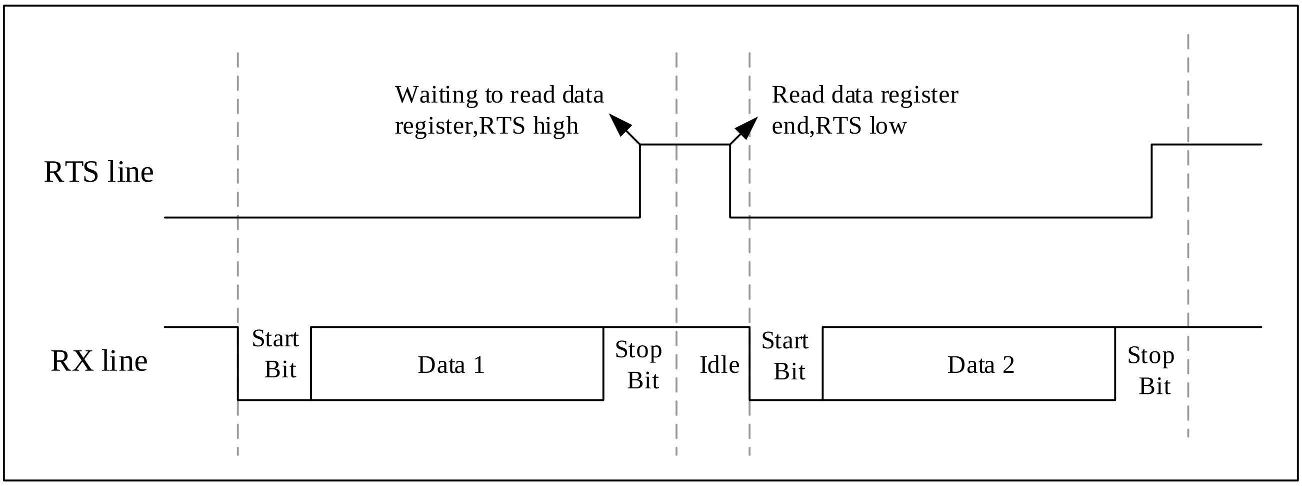
threshold condition is achieved, otherwise it will be driven low.How is the RTS valid can be selected by the LPUART_CTRL.RTS_THSEL[1:0] bits. The RTS threshold can be selected to be effective when the FIFO is half full, 3/4 full, or full. Below is an example of communication with RTS flow control enabled.

Figure 25-8 RTS flow control

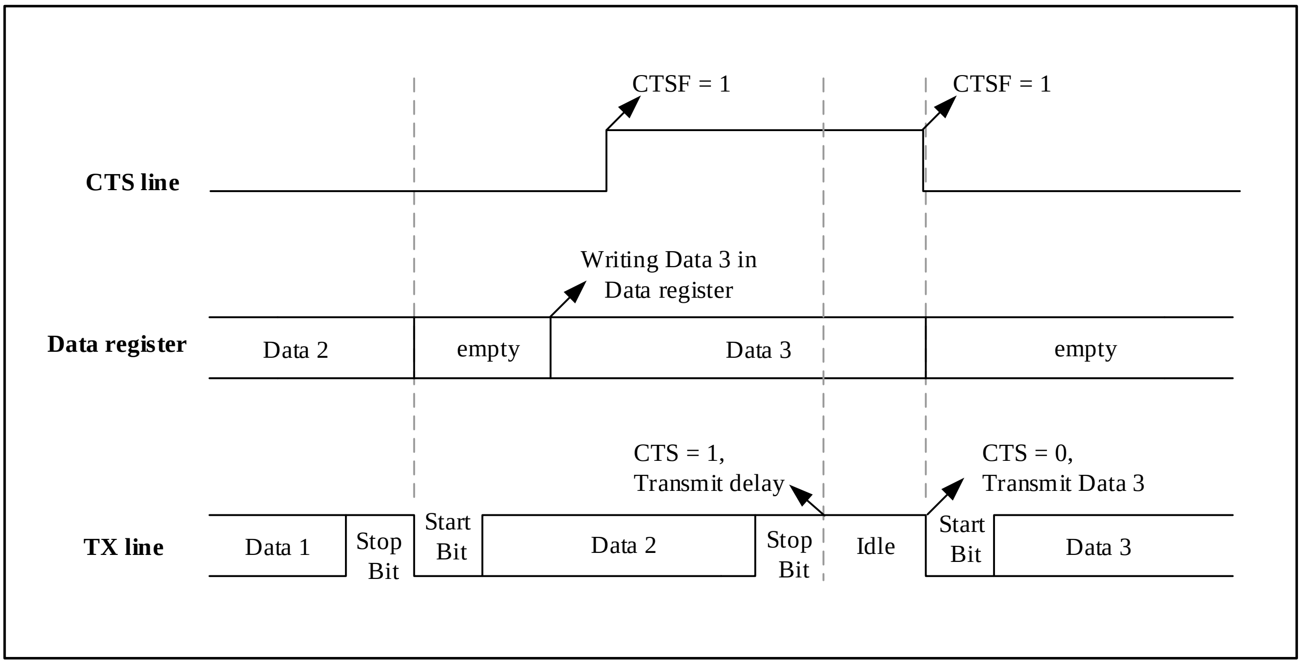


25.4.7.2 CTS flow control

If CTS flow control is enabled (LPUART_CTRL.CTSEN=1), the sender will check the CTS pin to decide whether or not send data before sending the next frame. If the CTS is pulled low (valid), the sender sends data (assuming that data is ready to be sent). If the CTS is pulled up during transmission, the transmission of the current data frame is stopped after transmission.

If CTS flow control is enabled (LPUART_CTRL.CTSEN=1), the signal of CTS pin will be changed. See Figure 25-9 for enabling CTS flow control.

Figure 25-9 CTS flow control



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25.4.8 Low power wake up

LPUART can work in STOP2 mode, if the LPUART_CTRL.WUSTP is set, it can wake up the system on EXTI line 23 when a specific waking up event occurs.

The LPUART waking up event can be handled in the following ways (through the LPUART_CTRL.WUSEL[1:0]) :

- A waking up event is generated when a start bit is detected
- A waking up event is generated when the receive buffer non-empty flag is set
- A waking up event is generated when data is received and the first byte matches LPUART_WUDAT[7:0]
- A waking up event is generated when data is received and four bytes match LPUART_WUDAT[31:0]

When waking up event occurs, the LPUART_STS.WUF bit will be set.

25.5 Interrupt request

Table 25-3 LPUART interrupt requests

Interrupt	Interrupt event	Event flag	Enable bit
LPUART global interrupt	Parity check error	PEF	PEIE
	TX complete	TXC	TXCIE
	Receive buffer overrun	FIFO_OV	FIFO_OVIE
	Receive buffer full	FIFO_FU	FIFO_FUIE
	Receive buffer half full	FIFO_HF	FIFO_HFIE
	Receive buffer not empty	FIFO_NE	FIFO_NEIE
	Wake up in STOP2 mode	WUF	WUFIE

LPUART interrupt events are logical OR. If the corresponding enable control bit is set, these events can generate their own interrupt, but only one interrupt request can be generated at the same time.

25.6 LPUART registers

25.6.1 LPUART register overview

Table 25-4 LPUART register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	LPUART_STS	Reserved																							NF	WUF	CTS	FIFO_NE	FIFO_HF	FIFO_FU	FIFO_OV	TXC	PEF
	Reset Value																								0	0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
004h	LPUART_INTEN	Reserved																									WUFIE	FIFO_NEIE	FIFO_HFIE	FIFO_FUIE	FIFO_OVIE	TXCIE	PEIE
	Reset Value																										0	0	0	0	0	0	0
008h	LPUART_CTRL	Reserved																	SMPCNT	WUSEL[1:0]		RTSEN	CTSEN	RTS_THSEL[1:0]		WUSTP	DMA_RXEN	DMA_TXEN	LOOPBACK	PCDIS	FLUSH	TXEN	PSEL
	Reset Value																		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
00Ch	LPUART_BRCFG1	Reserved																INTEGER[15:0]															
	Reset Value																	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0
010h	LPUART_DAT	Reserved																								DAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	LPUART_BRCFG2	Reserved																								DECIMAL[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
018h	LPUART_WUDAT	WUDAT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.6.2 LPUART status register (LPUART_STS)

Address offset: 0x00

Reset value: 0x0000 0000

31:16
Reserved

15:9	8	7	6	5	4	3	2	1	0
Reserved	NF	WUF	CTS	FIFO_NE	FIFO_HF	FIFO_FU	FIFO_OV	TXC	PEF
	rc_w1	rc_w1	r	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	NF	Noise detected flag. When noise is detected in the received frame, this bit is set by hardware.This bit is cleared by the software. 0: No noise is detected. 1: Noise is detected.
7	WUF	Wakeup from STOP2 mode Flag. 0: No wake up event is detected. 1: A wake up event is detected.
6	CTS	CTS signal (hardware flow control) flag. Once the sender requests to send data, it is ready to receive it. 0: CTS line is reset. 1: CTS line is set.
5	FIFO_NE	FIFO non-empty flag.

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Bit field	Name	Description
		0: Buffer is empty. 1: Buffer is not empty.RX data is ready to be read
4	FIFO_HF	FIFO half full flag. 0: Buffer is not half full. 1: Buffer is half full.RX data should be read before the buffer is full
3	FIFO_FU	FIFO full flag. 0: Buffer is not full. 1: Buffers is full.RX data should be read out in preparation for receiving new data
2	FIFO_OV	FIFO overrun flag. 0: Buffer did not overrun 1: Buffer overrun.
1	TXC	TX complete flag. 0: TX is disabled or not complete. 1: TX transmission is complete.
0	PEF	Parity check error flag. 0: No parity error detected. 1: Parity error detected

25.6.3 LPUART interrupt enable register (LPUART_INTEN)

Address offset: 0x04

Reset value: 0x0000 0000

31–16
Reserved

15–7	6	5	4	3	2	1	0
Reserved	WUFIE	FIFO_NEIE	FIFO_HFIE	FIFO_FUIE	FIFO_OVIE	TXCIE	PEIE
	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained.
6	WUFIE	Wake up interrupt enable 0: Disable wake up interrupt 1: Enable wake up interrupt
5	FIFO_NEIE	Receive buffer not empty interrupt enable 0: Disable buffer non-empty interrupt 1: Enable buffer non-empty interrupt
4	FOFO_HFIE	Receive buffer half-full interrupt enable 0: Disables buffer half-full interrupt 1: Enables buffer half-full interrupt
3	FOFO_FUIE	Receive buffer full interrupt enable 0: Disables buffer full interrupt

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Bit field	Name	Description
		1: Enable buffer full interrupt
2	FIFO_OVIE	Receive buffer overrun interrupt enable 0: Disables buffer overrun interrupt 1: Enable buffer overrun interrupt
1	TXCIE	TX complete interrupt enable 0: Disable TX complete interrupt 1: Enable TX complete interrupt
0	PEIE	Parity check error interrupt enable 0: Disable parity error interrupt 1: Enable parity error interrupt

25.6.4 LPUART control register (LPUART_CTRL)

Address offset: 0x08

Reset value: 0x0000 0200

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SMPCNT	WUSEL[1:0]		RTSEN	CTSEN	RTS_THSEL[1:0]		WUSTP	DMA_RXEN	DMA_TXEN	LOOP BACK	PCDIS	FLUSH	TXEN	PSEL
	rw	rw		rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	SMPCNT	Specify sampling method 0: 3 sample bits, noise detection is allowed (LPUARTDIV should be large enough, such as greater than 10) 1: 1 sample bits, closed noise detection
13:12	WUSEL[1:0]	Wake up event selection. 00: Start bit detection 01: Non-empty detection of receive buffer 10: A configurable receive byte 11: A programmable 4-byte frame
11	RTSEN	RTS hardware flow control enable 0: Disables RTS hardware flow control 1: Enables RTS hardware flow control
10	CTSEN	CTS hardware flow control enable 0: Disables CTS hardware flow control 1: Enables CTS hardware flow control
9:8	RTS_THSEL[1:0]	RTS threshold selection 00: When FIFO is half full, RTS is effective (pull up)

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Bit field	Name	Description
		x1: When FIFO is 3/4 full, RTS effective (pull up) 10: When FIFO is full, RTS effective (pull up)
7	WUSTP	LPUART STOP2 mode wakeup enabled 0: Cannot wake up STOP2 mode 1: Can wake up the STOP2 mode
6	DMA_RXEN	DMA RX request enable
5	DMA_TXEN	DMA TX request enable
4	LOOKBACK	Loopback self-test 0: Normal mode 1: Loopback self-test mode
3	PCDIS	Parity control 0: Enables parity bit 1: Disables parity bit
2	FLUSH	Clear receive buffer 0: Disables buffer clear 1: Clear buffer content
1	TXEN	TX enable 0: Disables TX 1: Enables TX
0	PSEL	Odd parity enable 0: Even parity 1: Odd parity

25.6.5 LPUART baud rate configuration register 1 (LPUART_BRCFG1)

Address offset: 0x0C

Reset value: 0x0000 0174

31–16
Reserved

15–0
INTEGER[15:0]
rw

Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	INTEGER[15:0]	Baud rate configuration register 1. The calculation of baud rate configuration register 1 is as follows: If the baud rate is 9600bps and the clock frequency is 32768Hz. LPUARTDIV = 32768/9600 = 3.4133 In this case, the integer part of the LPUARTDIV is 3 and the decimal part is 0.4133.LPUART_BRCFG1 = 3.LPUART_BRCFG2 will be used for baud rate

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Bit field	Name	Description
		error correction.For the 3-bit sampling method with noise detection characteristics, LPUARTDIV is not large enough at this time, so 1-bit sampling method should be adopted to avoid sampling error.

25.6.6 LPUART data register (LPUART_DAT)

Address offset: 0x10

Reset value: 0x0000 0000

31 ... 16
Reserved

15 ... 8	7 ... 0
Reserved	DAT[7:0]
	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DAT[7:0]	Write to the data register when sending Read the data register when receiving, that is

25.6.7 LPUART baud rate configuration register 2 (LPUART_BRCFG2)

Address offset: 0x14

Reset value: 0x0000 0000

31 ... 16
Reserved

15 ... 8	7 ... 0
Reserved	DECIMAL[7:0]
	rw

Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DECIMAL[7:0]	Baud rate configuration register 2 is used for baud rate error correction at low frequencies.For example, If the baud rate is 4800bps and the clock frequency is 32768Hz. LPUARTDIV = 32768/4800 = 6.8266 LPUART_BRCFG1 = 6.In this case, to correct the baud rate error, you should configure register 2 with baud rate. For details on how to configure register 2, refer to the section "Fractional baud rate generation".

25.6.8 LPUART wake up data register (LPUART_WUDAT)

Address offset: 0x18

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Reset value: 0x0000 0000

31	16
WUDAT[31:0]	
rw	

15	0
WUDAT[31:0]	
rw	

Bit field	Name	Description
31:0	WUDAT[31:0]	When LPUART_CTRL.WUSEL[1:0] = 1x, WUDAT[31:0] is used to check whether the conditions for wake up from STOP2 mode is matched (byte match or frame match): LPUART_CTRL.WUSEL[1:0] = 10 is used to wake up byte matching. In this case, the first byte is valid LPUART_CTRL.WUSEL[1:0] = 11 is used to wake up frame matching. In this case, all 4 bytes are valid

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26 Serial peripheral interface/Inter-IC Sound (SPI/I^{2}S)

26.1 Introduction

This module is about SPI/I^{2}S. It works in SPI mode by default and users can choose to use I^{2}S by setting the value of registers.

Serial peripheral interface (SPI) is able to work in master or slave mode, support full-duplex and simplex high-speed communication mode, and have hardware CRC calculation and configurable multi-master mode.

On-chip audio interface (I^{2}S) is able to work in master and slave modes in simplex communication, and supports four audio standards: Philips I^{2}S standard, MSB alignment standard, LSB alignment standard and PCM standard.

Both of them are synchronous serial interface communication protocols.

26.2 Main features

26.2.1 SPI features

- Full duplex mode and simplex synchronous mode.
- Support master mode, slave mode and multi-master mode.
- Supports 8-bit or 16-bit data frame format.
- Data bit sequence programmable.
- NSS management by hardware or software.
- Clock polarity and phase programmable.
- Sending and receiving support hardware CRC calculation and check.
- Supports DMA function.

26.2.2 I2S features

- Simplex synchronous mode.
- Supports master mode and slave mode operation.
- Four audio standards are supported: Philips I^{2}S standard, MSB alignment standard, LSB alignment standard and PCM standard.
- The audio sampling frequency from 8kHz to 96kHz can be configured.
- Supports 16-bit, 24-bit or 32-bit data length and data frame format (configured according to requirements).
- Steady state clock polarity programmable.
- The data direction is always MSB first.
- Supports DMA function.

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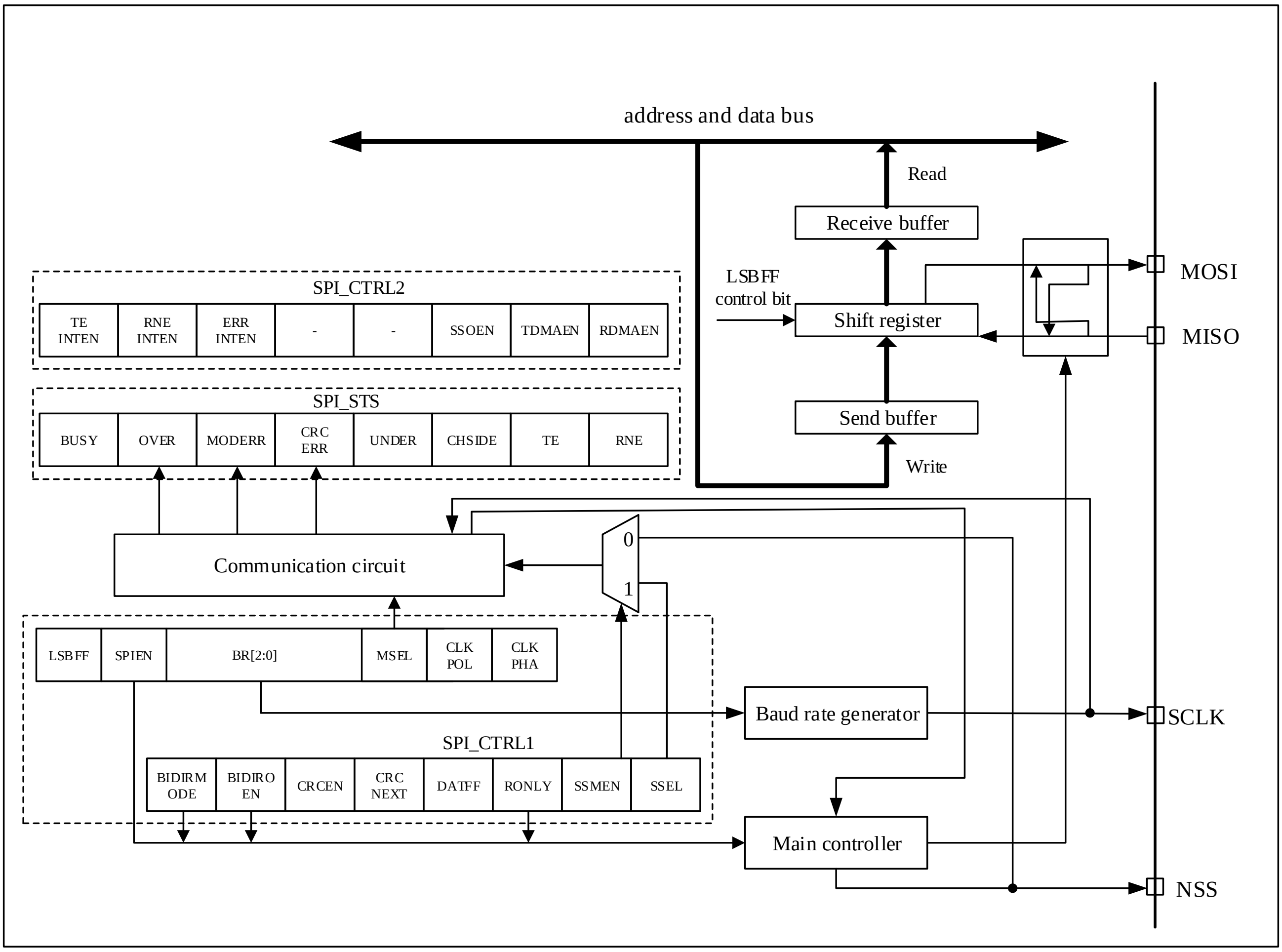
26.3 SPI function description

26.3.1 General description

Figure 26-1 SPI block diagram



To connected external devices, SPI has four pins, which are as follows:

- SCLK: serial clock pin. Serial clock signal is output from the SCLK pin of master device and input to SCLK pin of slave device.
- MISO: master input/slave output pin. Data is received from the MISO pin of master device and send by the MISO pin of slave device.
- MOSI: master output/slave input pin. Data is send by the MOSI pin of master device and received from the MOSI pin of slave device.
- NSS: chip select pin. There are two types of NSS pin, internal pin and external pin. If the internal pin detects a high level, SPI works in the master mode. Conversely, SPI works in the slave mode. Users can use a standard I/O pin of the master device to control the NSS pin of the slave device.

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Software NSS mode

The software slave device management is enabled when SPI_CTRL1.SSMEN = 1 (Figure 26-2).

The NSS pin is not used in software NSS mode. In this mode the internal NSS signal level is driven by writing the SPI_CTRL1.SSEL bit (master mode SPI_CTRL1.SSEL = 1, slave mode SPI_CTRL1.SSEL = 0).

Hardware NSS mode

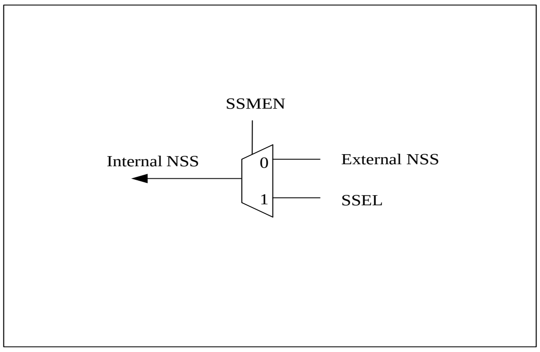
The software slave device management is disabled when SPI_CTRL1.SSMEN = 0.

NSS input mode: The NSS output of the master device is disabled (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 0), allowing operation in multi-master mode. The master should connect NSS pin to the high level and the slave should connect NSS pin to the low level during the entire data frame transfer.

NSS output mode: NSS output of the master device is enable (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 1). SPI as the master device must pull the NSS pin to low level, all device which connected to the master device and set to NSS hardware mode, will detect low level and enter the slave mode automatically. If the master device cannot pull the NSS pin to low level, device will enter the slave mode and generates the master mode failure error.

Note: The choice of software mode or hardware mode depends on whether NSS control is needed in the communication protocol. If not, you can choose the software mode, and release a GPIO pin for other purposes.

Figure 26-2 Selective management of hardware/software



The following figure is an example of the interconnection of single master and single slave devices

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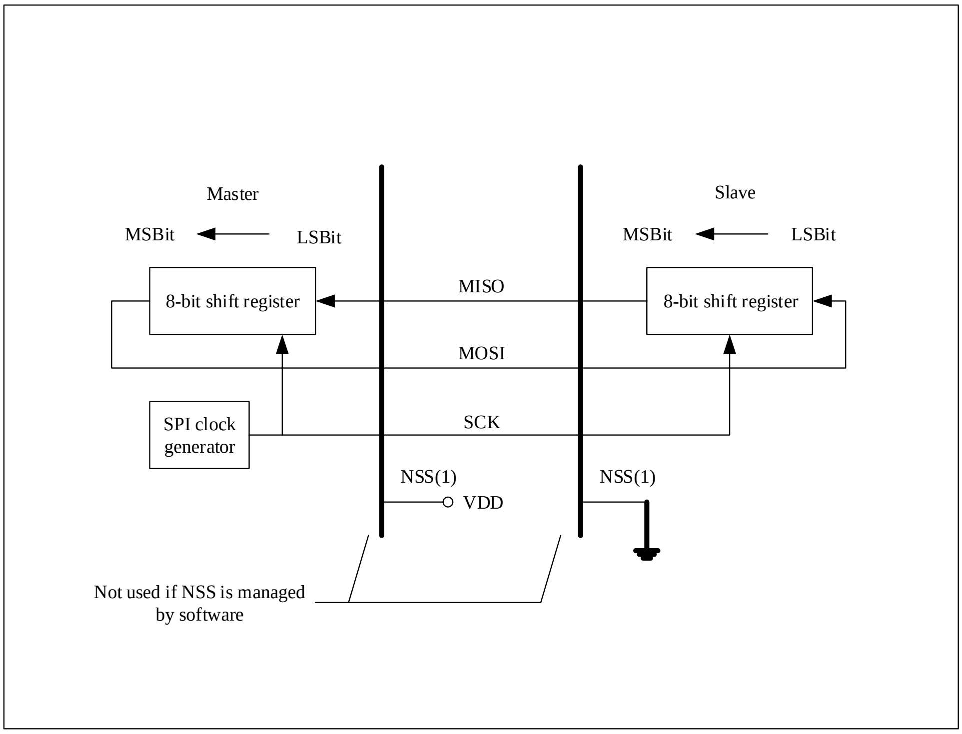
Figure 26-3 Master and slave applications



Note: NSS pin is set as input

SPI is a ring bus structure. The master device outputs a synchronous clock signal through the SCK pin, the MOSI pin of the master device is connected to the MOSI pin of the slave device, and the MISO pin of the master device is connected to the MISO pin of the slave device, so that data can be transferred between devices. Continuous data transfer between master and slave, sending data to slave through MOSI pin and slave sending data to master through MISO pin.

SPI timing mode

User can selects the clock edge of data capture by setting SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit.

- When CLKPOL = 0, CLKPHA = 0, the SCLK pin will keep low in idle state, and the data will be sampled at the first edge, which is rising edge.
- When CLKPOL = 0, CLKPHA = 1, the SCLK pin will keep low in idle state, and the data will be sampled at the second edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 0, the SCLK pin will keep high in idle state, and the data will be sampled at the first edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 1, the SCLK pin will keep high in idle state, and the data will be sampled at the second edge, which is rising edge.

Regardless of the timing mode used, the master and slave configuration must be the same.

Figure 26-4 is the combination timing of four CLKPHA and CLKPOL bits transmitted by SPI when the SPI_CTRL1.LSBFF=0.

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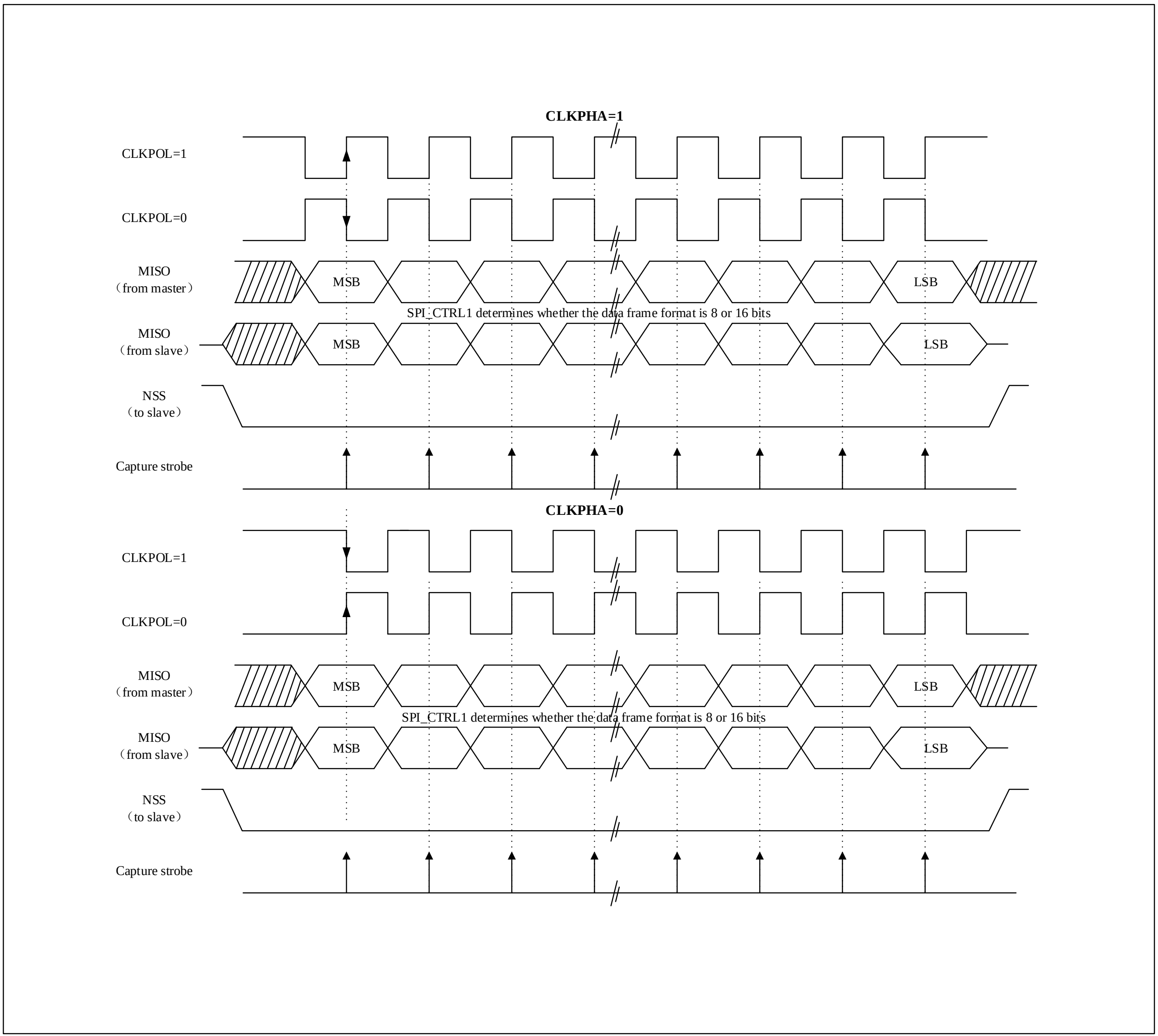
Figure 26-4 Data clock timing diagram



Data format

User can selects the data order by setting the SPI_CTRL1.LSBFF bit. When SPI_CTRL1.LSBFF = 0, SPI will send the high-order data (MSB) first; When SPI_CTRL1.LSBFF = 1, SPI will send low-order data (LSB) first.

User can selects the data frame by setting the SPI_CTRL1.DATFF bit.

26.3.2 SPI work mode

- **Master full duplex mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

After the first data is written to the SPI_DAT register, the transmission will start. When the first bit of the data is sent, the data bytes are loaded from the data register into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the data bits follow the MSB or LSB order is serially shifted to the

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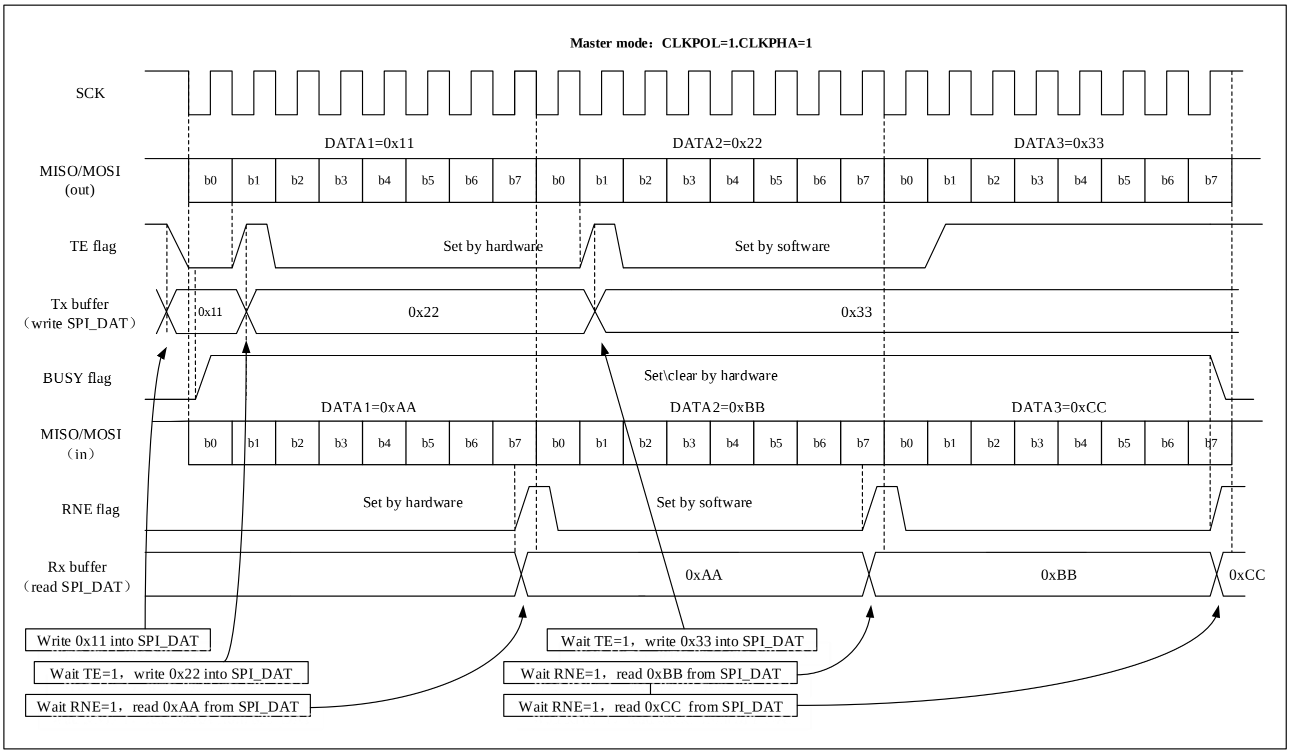
MOSI pin. At the same time, the data received on the MISO pin is serially shifted into the shift register in the same order and then loaded into the SPI_DAT register in parallel. The software operation process is as follows:

1. Set SPI_CTRL1.SPIEN = 1, enable SPI module.
2. Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
3. Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Wait for SPI_STS.RNE bit to be set to '1', read SPI_DAT to get the first received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT. Repeat the above operation, sending subsequent data and receiving n-1 data at the same time;
4. Wait for SPI_STS.RNE bit to be set to '1' to receive the last data;
5. Wait for SPI_STS.TE to be set to '1', then wait for SPI_STS.BUSY bit to be cleared and turn off SPI module.

The process of data sending and data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE or SPI_STS.TE flag.

Figure 26-5 Schematic diagram of the change of TE/RNE/BUSY when the host is continuously transmitting in full duplex mode



- **Master two-wire one-way send-only mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

Master two-wire one-way send-only mode is similar to master full-duplex mode. The difference is that this mode will not read the received data, so the SPI_STS.OVER bit will be set to '1', and the software will ignore it. The software operation process is as follows:

1. Set SPI_CTRL1.SPIEN = 1, enable SPI module.
2. Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).

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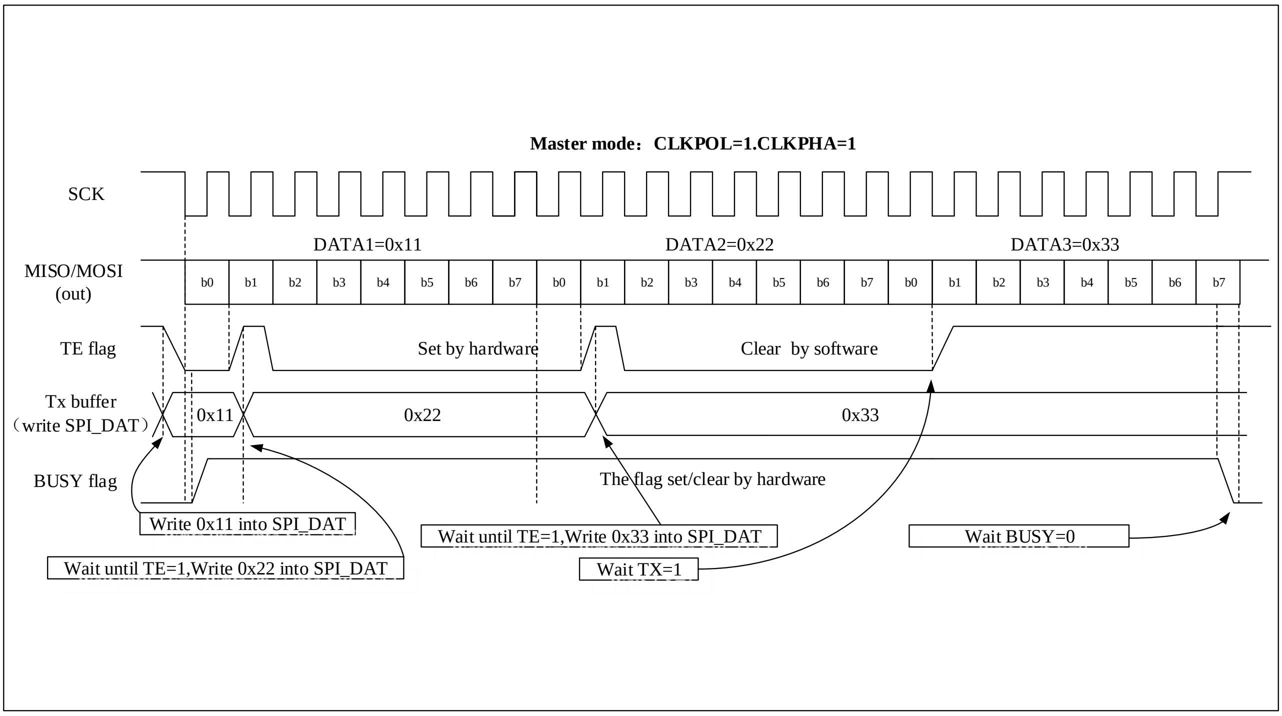
3. Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Repeat this operation to send subsequent data;
4. After writing the last data to SPI_DAT, wait for SPI_STS.TE bit to set '1'; then wait for SPI_STS.BUSY bit to be cleared to complete the transmission of all data.

The process of data sending can also be implemented in the interrupt handler generated by the rising edge of the TE flag.

Figure 26-6 Schematic diagram of TE/BUSY change when host transmits continuously in one-way only mode



- **Master two-wire one-way receive-only mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 1)**

When SPI_CTRL1.SPIEN = 1, the receiving process starts. The data bits from the MISO pin are sequentially shifted into the shift register and then loaded into the SPI_DAT register (receive buffer) in parallel. The software operation process is as follows:

1. Enable the receive-only mode (SPI_CTRL1.RONLY = 1).
2. Enable SPI module, set SPI_CTRL1.SPIEN = 1: in master mode, SCLK clock signal is generated immediately, and serial data is continuously received before SPI is turned off (SPI_CTRL1.SPIEN = 0); in slave mode, serial data is continuously received when the SPI master device pulls low the NSS signal and generates SCLK clock.
3. Wait for SPI_STS.RNE bit to be set to '1', read the SPI_DAT register to get the received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT register. Repeat this operation to receive all data.

The process of data receiving can also be implemented in the interrupt handler generated by the rising edge of the RNE flag (SPI_STS.RNE).

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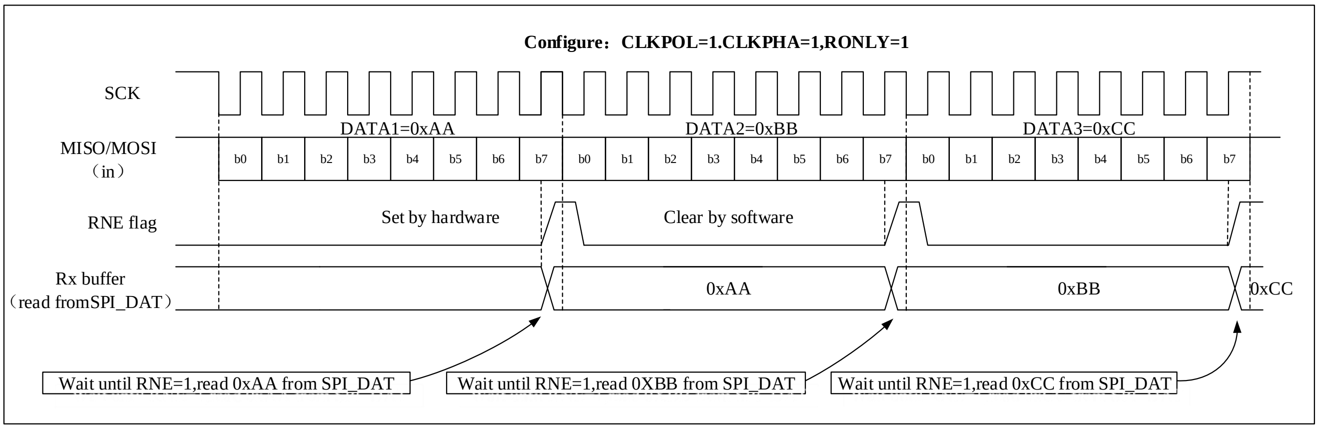
Figure 26-7 Schematic diagram of RNE change when continuous transmission occurs in receive-only mode (BIDIRMODE = 0 and RONLY = 1)



- **Master one-wire bidirectional send mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 1, SPI_CTRL1.RONLY = 0)**

After the data is written to the SPI_DAT register (send buffer), the transmission process starts. This mode does not receive data. At the same time as the first data bit is send, the data to be sent is loaded into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the SPI serially shifts the data bits to the MOSI pin in MSB or LSB order

The software operation flow of the master one-wire bidirectional send mode is the same as that of the send-only mode.

- **Master one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 0, SPI_CTRL1.RONLY = 0)**

When SPI_CTRL1.SPIEN = 1, the receiving process starts. There is no data output in this mode, the received data bits are sequentially and serially shifted into the shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel.

The software operation flow of the master one-wire bidirectional receive mode is the same as that of the receive-only mode.

- **Slave full duplex mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

The data transfer process begins when the slave device receives the first clock edge. Before the master starts data transfer, software must ensure that the data to be send is written to the SPI_DAT register.

Figure 26-8 Schematic diagram of the change of TE/RNE/BUSY when the slave is continuously transmitting in full duplex

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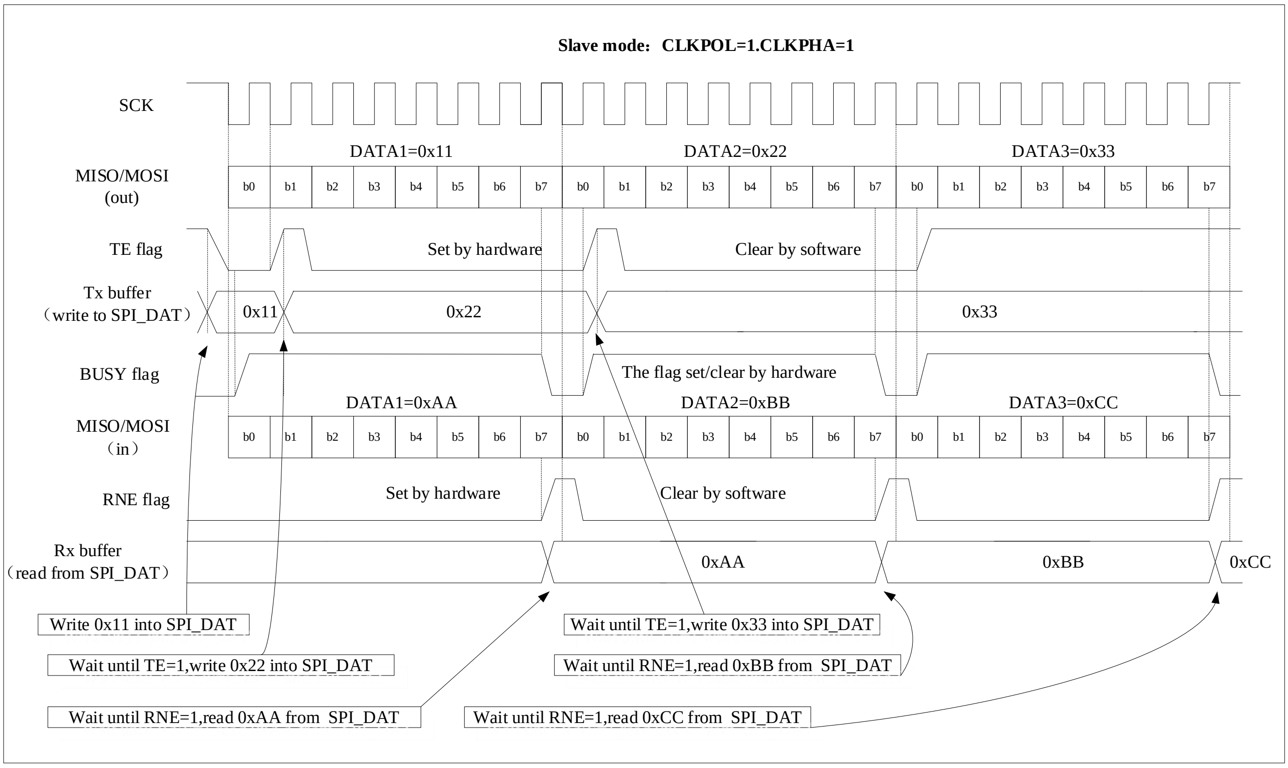
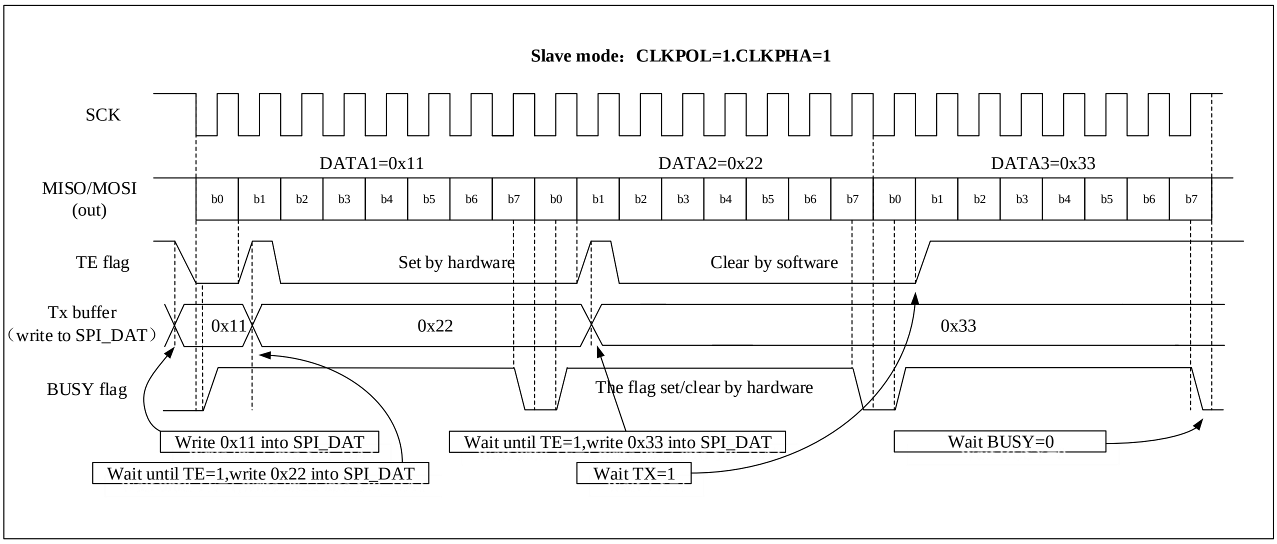
mode



■ **Slave two-wire one-way send-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 0)**

Figure 26-9 Schematic diagram of TE/BUSY change during continuous transmission in slave unidirectional transmit-only mode



■ **Slave two-wire one-way receive-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 1)**

The data receiving process begins when the slave device receives the clock signal and the first data bit from the MOSI pin. The received data bits are sequentially and consecutively shifted serially into an shift register and then

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loaded into the SPI_DAT register (receive buffer) in parallel.

- **Slave one-wire bidirectional send mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 1)**

When the slave device receives the first edge of the clock signal, the sending process starts. No data is received in this mode, and the software must ensure that the data to be sent has been written in the SPI_DAT register before the SPI master device starts data transmission.

- **Slave one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 0)**

Data receiving begins when the slave device receives the first clock edge and a data bit from the MOSI pin. There is no data output in this mode, the received data bits are sequentially and consecutively shifted serially into an shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel.

Note: The software operation process of the slave can refer to the master.

SPI initialization process

1. The baud rate of serial clock is defined by the SPI_CTRL1.BR[2:0] bits (this step is ignored if it is working in slave mode).
2. Select SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit to define the phase relationship between data transmission and serial clock (see Figure 26-4).
3. Set SPI_CTRL1.DATFF bit to define 8-bit or 16-bit data frame format.
4. Configure the SPI_CTRL1.LSBFF bit to define the frame format.
5. Configure the NSS mode as described above for the NSS function.
6. Run mode is configured by SPI_CTRL1.MSEL bit, SPI_CTRL1.BIDIRMODE bit, SPI_CTRL1.BIDIROEN bit and SPI_CTRL1.RONLY bit.
7. Set the SPI_CTRL1.SPIEN = 1 to enable SPI.

Basic send and receive process

When SPI sends a data frame, it first loads the data frame from the data buffer into the shift register, and then starts to send the loaded data. When the data is transferred from the send buffer to the shift register, the send buffer empty flag is set (SPI_STS.TE = 1), and the next data can be loaded into the send buffer; if the TEINTEN bit is set (SPI_CTRL2.TEINTEN = 1), an interrupt will be generated; writing data to the SPI_DAT register will clear the SPI_STS.TE bit.

At the last edge of the sampling clock, when the data is transferred from the shift register to the receive buffer, the receive buffer non-empty flag is set (SPI_STS.RNE = 1), at this time the data is ready and can be read from the SPI_DAT register; if the receive buffer non-empty interrupt is enabled (SPI_CTRL2.RNEINTEN = 1), an interrupt will be generated; the SPI_STS.RNE bit can be cleared by reading the SPI_DAT register data.

In master mode, the sending process starts when data is written to the send buffer. If the next data has been written into the SPI_DAT register before the current data frame sending is completed, the continuous sending function can be achieved.

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In slave mode, the NSS pin is low, and when the first clock edge arrives, the transmission process begins. In order to avoid accidental data transmission, software must write data to the transmit buffer before data transmission (it is recommended to enable the SPI module before the host sends the clock).

In some configurations, when the last data is sent, the BUSY flag (SPI_STS.BUSY) can be used to wait for the end of the data sending.

Continuous and discontinuous transmission.

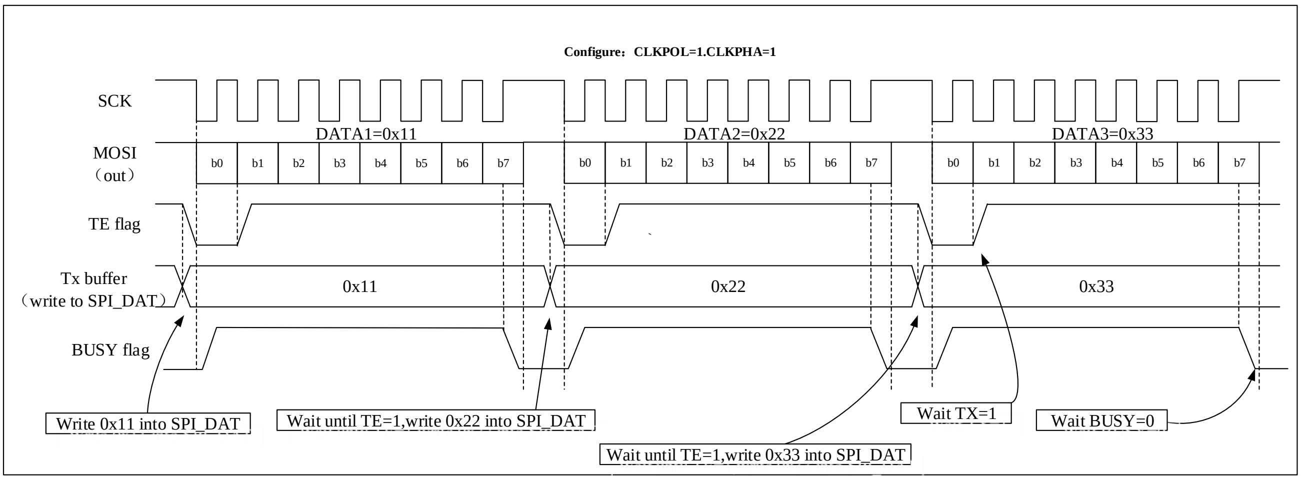
When sending data in master mode, if the software is fast enough to detect each TE (SPI_STS.TE) rising edge (or TE interrupt), and the data is written to the SPI_DAT register immediately before the end of the ongoing transmission. At this time, the SPI clock remains continuous between the transmission of data items, and the SPI_STS.BUSY bit will not be cleared, continuous communication can be achieved.

If the software is not fast enough, it will result in discontinuous communication; in this case, the SPI_STS.BUSY bit is cleared between the transmission of each data items (see Figure 26-10 below).

In master receive-only mode (SPI_CTRL1.RONLY = 1), communication is always continuous and the BUSY flag (SPI_STS.BUSY) is always high.

In slave mode, the continuity of communication is determined by the SPI master device. However, even if the communication is continuous, the BUSY flag (SPI_STS.BUSY) will be low for at least one SPI clock cycle between each data item (see Figure 26-9).

Figure 26-10 Schematic diagram of TE/BUSY change when BIDIRMODE = 0 and RONLY = 0 are transmitted discontinuously



26.3.3 Status flag

The SPI_STS register has 3 flag bits to monitor the status of the SPI:

Send buffer empty flag bit (TE)

When the send buffer is empty, the TE flag (SPI_STS.TE) is set to 1, which means that new data can be written into the SPI_DAT register. When the send buffer is not empty, the hardware will clear this flag to 0.

Receive buffer non-empty flag bit (RNE)

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When the receive buffer is not empty, the RNE flag (SPI_STS.RNE) is set to 1, so the user knows that there is data in the receive buffer. After reading the SPI_DAT register, the hardware will set this flag to 0.

BUSY flag bit (BUSY)

When the transmission starts, the hardware sets the BUSY flag (SPI_STS.BUSY) to 1, and after the transmission ends, the hardware sets the BUSY flag to 0.

Only when the device is in the master one-wire bidirectional receive mode, the BUSY flag (SPI_STS.BUSY) will be set to 0 when the communication is in progress.

The BUSY flag (SPI_STS.BUSY) will be cleared to 0 in the following cases:

- End of transmission (except for continuous communication in master mode);
- Turn off the SPI module (SPI_CTRL1.SPIEN = 0);
- The master mode error occurs (SPI_STS.MODERR = 1)

When the communication is discontinuous: the BUSY flag (SPI_STS.BUSY) is cleared to '0' between the transmission of each data item.

When communication is continuous: in master mode, the BUSY flag (SPI_STS.BUSY) remains high during the entire transfer process; In slave mode, the BUSY flag (SPI_STS.BUSY) will be low for 1 SPI clock cycle between each data item transfer. So do not use the BUSY flag to handle the sending and receiving of each data item.

26.3.4 Disabling the SPI

In order to turn off the SPI module, different operation modes require different operation steps:

Master or slave full duplex mode

1. Wait for the RNE flag (SPI_STS.RNE) to be set to 1 and the last byte to be received;
2. Wait for the TE flag (SPI_STS.TE) to be set to 1;
3. Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
4. Turn off the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire one-way send-only mode or one-wire bidirectional send mode for master or slave

1. After writing the last byte to the SPI_DAT register, wait for the TE flag (SPI_STS.TE) to be set to 1;
2. Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
3. Turn off the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire one-way receive-only mode or one-wire bidirectional receive mode for master

1. Wait for the penultimate RNE (SPI_STS.RNE) to be set to 1;
2. Before closing the SPI module (SPI_CTRL1.SPIEN = 0), wait for 1 SPI clock cycle (using software delay);
3. Wait for the last RNE (SPI_STS.RNE) to be set before entering shutdown mode (or turning off the SPI module clock).

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Two-wire one-way receive-only mode or one-wire bidirectional receive mode for slave

1. The SPI module can be turned off at any time (SPI_CTRL1.SPIEN = 0), and after the current transfer is over, the SPI module will be turned off;
2. If you want to enter the shutdown mode, you must wait for the BUSY flag (SPI_STS.BUSY) to be set to 0 before entering the shutdown mode (or turn off the SPI module clock).

26.3.5 SPI communication using DMA

Users can choose DMA for SPI data transfer, the application program can be released, and the system efficiency can be greatly improved.

When the send buffer DMA is enabled (SPI_CTRL2.TDMAEN = 1), each time the TE flag (SPI_STS.TE) bit is 1, a DMA request will be generated, and the DMA will automatically write the data to the SPI_DAT register, which will clear the TE flag (SPI_STS.TE) bit. When the receive buffer DMA is enabled (SPI_CTRL2.RDMAEN = 1), each time the RNE flag (SPI_STS.RNE) bit is set to 1, a DMA request will be generated, and the DMA will automatically read the SPI_DAT register, which will clear the RNE flag (SPI_STS.RNE) bit.

When the SPI is only used for sending data, only the send DMA channel of the SPI needs to be enabled (SPI_CTRL2.TDMAEN = 1).

When the SPI is only used for receiving data, only the receive DMA channel of the SPI needs to be enabled (SPI_CTRL2.RDMAEN = 1).

In send mode, after DMA has sent all the data to be sent (DMA_INTSTS.TXCF = 1), BUSY flag (SPI_STS.BUSY) can monitor to confirm whether SPI communication is over, which can avoid destroying the transmission of the last data when the SPI is turned off or enters the shutdown mode. Therefore, the software needs to wait for the TE flag (SPI_STS.TE) bit to be set to 1, and wait for the BUSY flag (SPI_STS.BUSY) bit to be set to 0.

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Figure 26-11 Transmission using DMA

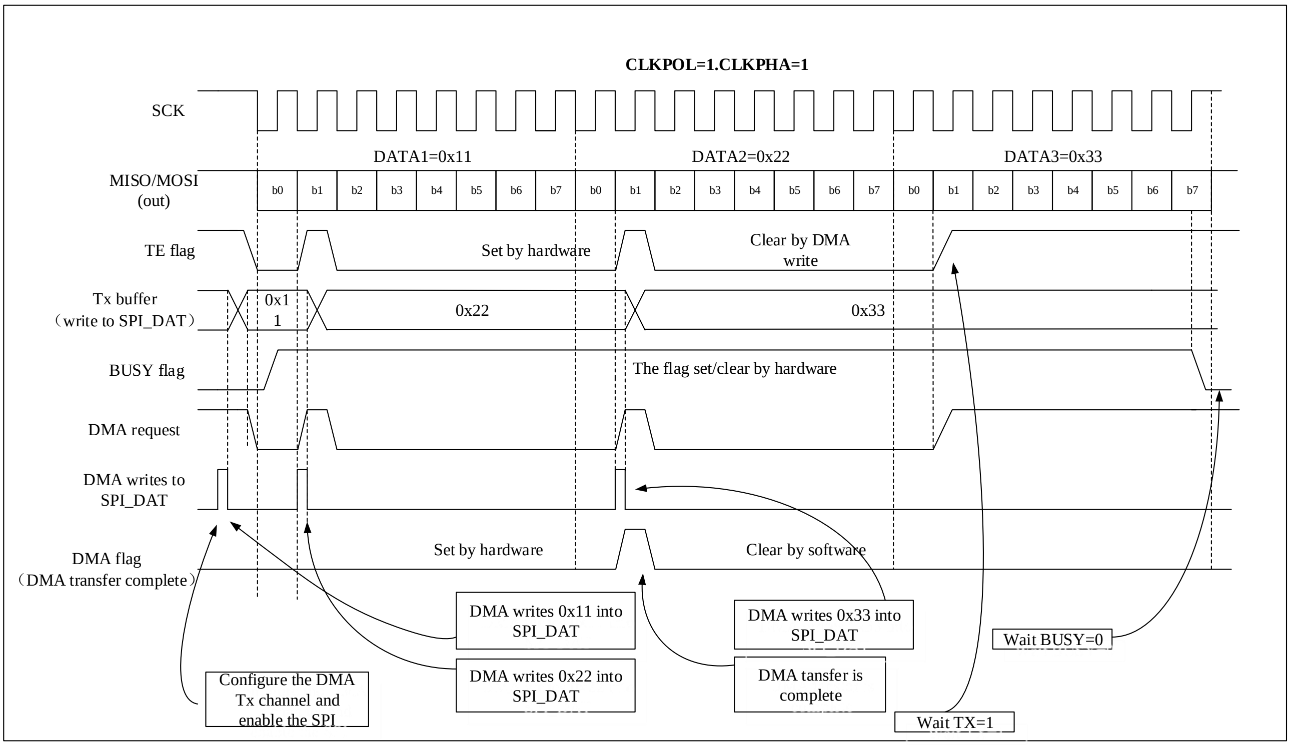
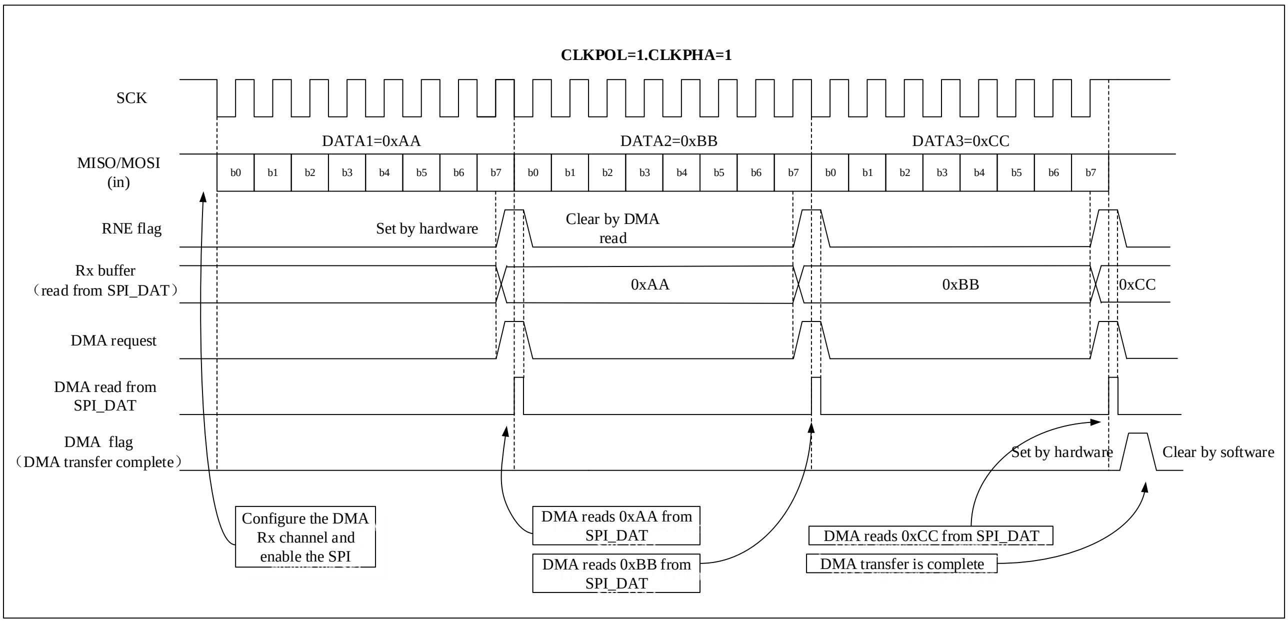


Figure 26-12 Reception using DMA



26.3.6 CRC calculation

SPI contains two independent CRC calculators for data sending and data receiving to ensure the correctness of data transmission. According to the sending and receiving data frame format, CRC adopts different calculation methods, the 8-bit data frame format adopts CRC8, and the 16-bit data frame format adopts CRC16. The polynomial used in

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the SPI CRC calculation is set by the SPI_CRCPOLY register, and the user enables the CRC calculation by setting the SPI_CTRL1.CRCEN = 1.

In send mode, after the last data is written into the send buffer, set the SPI_CTRL1.CRCNEXT = 1, which indicates that the hardware will start sending the CRC value (SPI_CRCTDAT value) after sending the data. When the CRC is sent, the CRC calculation will stop.

In receive mode, after the penultimate data frame is received, set the SPI_CTRL1.CRCNEXT = 1. The received CRC and SPI_CRCRDAT values are compared, if they are different, the SPI_STS.CRCERR bit is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt will be generated.

In order to keep the synchronization of the next CRC calculation result of the master-slave device, the user should clear the CRC value of the master-slave device. Setting the SPI_CTRL1.CRCEN bit resets the SPI_CRCRDAT and SPI_CRCTDAT registers. Take the following steps in order: SPI_CTRL1.SPIEN = 0; SPI_CTRL1.CRCEN = 0; SPI_CTRL1.CRCEN = 1; SPI_CTRL1.SPIEN = 1.

Most importantly, when the SPI is configured in slave mode and CRC is enabled, as long as there is a clock pulse on SCLK pin, the CRC calculation will still be performed even if the NSS pin is high. This situation is common when the master device communicates with multiple slave devices alternately, so it is necessary to avoid CRC misoperation.

When the SPI hardware CRC check is enabled (SPI_CTRL1.CRCEN = 1) and the DMA is enabled, the hardware automatically completes the sending and receiving of CRC bytes when the communication ends.

26.3.7 Error flag

Master mode failure error (MODERR)

The following two conditions will cause the master mode failure error:

- NSS pin hardware management mode, the master device NSS pin is pulled low;
- NSS pin software management mode, the SPI_CTRL1.SSEL bit is set to 0.

When a master mode failure error occurs, the SPI_STS.MODERR bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1). The SPI_CTRL1.SPIEN bit and SPI_CTRL1.MSEL bit will be write protected and both are cleared by hardware. SPI is turned off and forced into slave mode

Software performs a read or write operation to the SPI_STS register, and then writes to the SPI_CTRL1 register to clear the SPI_STS.MODERR bit (in multi-master mode, the master's NSS pin must be pulled high first).

Normally, the SPI_STS.MODERR bit of the slave cannot be set to 1. However, in a multi-master configuration, the slave's SPI_STS.MODERR bit may be set to 1. In this case, the SPI_STS.MODERR bit indicates that there is a multi-master collision. The interrupt routine can perform a reset or return to the default state to recover from an error state.

Overflow error (OVER)

When the SPI_STS.RNE bit is set to 1, but there is still data sent into the receive buffer, an overflow error will occur. At this time, the overflow flag SPI_STS.OVER bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1). All received data is lost, and the SPI_DAT register retains only previously unread data.

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Read the SPI_DAT register and the SPI_STS register in turn to clear the SPI_STS.OVER bit.

CRC error (CRCERR)

The CRC error flag is used to check the validity of the received data. A CRC error occurs when the received CRC value does not match the SPI_CRCRDAT value. At this time, the SPI_STS.CRCERR flag bit is set to '1', and an interrupt will be generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1).

26.3.8 SPI interrupt

Table 26-1 SPI interrupt request

Interrupt event	Event flag bit	Enable control bit
Send buffer empty flag	TE	TEINTEN
Receive buffer non empty flag	RNE	RNEINTEN
Master mode failure event	MODERR	ERRINTEN
Overflow error	OVER	
CRC error flag	CRCERR	

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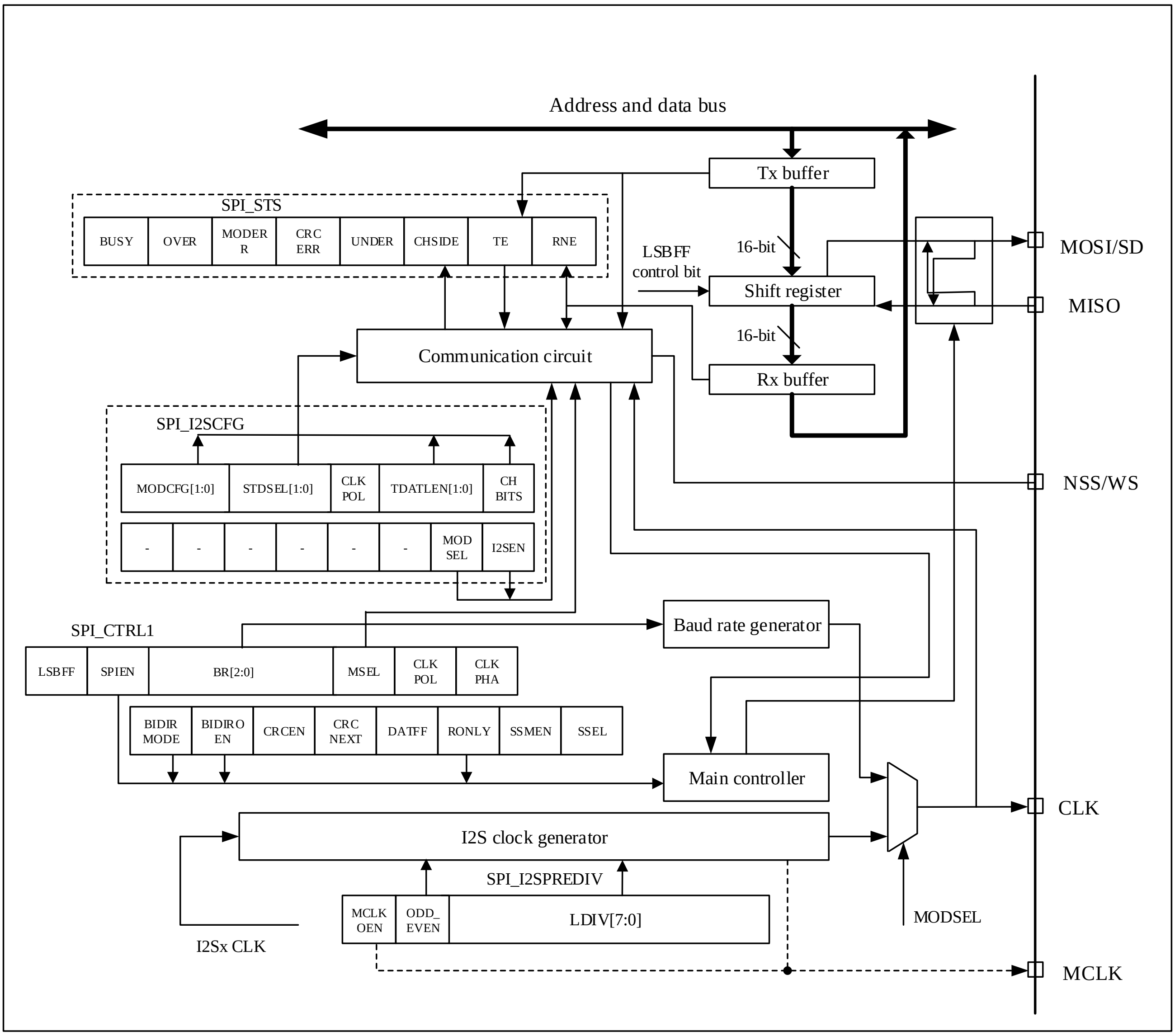
26.4 I²S function description

The block diagram of I2S is shown in the figure below:

Figure 26-13 I²S block diagram



The I2S interface uses the same pins, flags and interrupts as the SPI interface. Setting the SPI_I2SCFG.MODSEL = 1 selects the I2S audio interface.

I2S has a total of 4 pins, 3 of which are shared with SPI:

- CLK: Serial clock (shared with SCLK pin), CLK generates a pulse every time 1-bit audio data is sent.
- SD: Serial data (shared with MOSI pin), used for data send and receive;
- WS: Channel selection (shared with NSS pin), used as data control signal output in master mode, and used as input in slave mode;

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- MCLK: master clock (independent mapping, optional), output 256 × Fs clock signal to ensure better synchronization between systems.

Note: F_S is the sampling frequency of audio signal

In master mode, I2S uses its own clock generator to generate clock signals for communication, and this clock generator is also the clock source of the master clock output (SPI_I2SPREDIV.MCLKOEN = 1, the master clock output is enabled).

26.4.1 Supported audio protocols

Four audio standards can be selected by setting the SPI_I2SCFG.STDSEL[1:0] bits:

- I^2S Philips standard
- MSB alignment standard
- LSB alignment standard
- PCM standard

The audio data of the left channel and the right channel are usually time-division multiplexed, and the left channel always sends data before the right channel. By checking the SPI_STS.CHSIDE bit, the user can distinguish which channel the received data belongs to. However, in the PCM audio standard, the CHSIDE bit has no meaning.

By setting the SPI_I2SCFG.TDATLEN bits, the user can set the length of the data to be transmitted, and set the data bit width of the channel by setting the SPI_I2SCFG.CHBITS bits. There are 4 data formats for sending data as follows:

- 16-bit data is packed into 16-bit data frame
- 16-bit data is packed into a 32-bit data frame (the first 16 bits are meaningful data, and the last 16 bits are set to 0 by hardware)
- 24-bit data is packed into 32-bit data frame (the first 24-bit data is meaningful data, and the latter 8-bit data is set to 0 by hardware)
- 32-bit data is packed into 32-bit data frame

I2S uses the same SPI_DAT register as SPI to send and receive 16-bit wide data. If I2S needs to send or receive 24-bit or 32-bit wide data, the CPU needs to read or write the SPI_DAT register twice. On the other hand, when I2S sends or receives 16-bit wide data, the CPU only needs to read or write the SPI_DAT register once.

Regardless of which data format and communication standard is used, I2S always sends the data high-order bit (MSB) first.

I^2S Philips standard

Using the I2S Philips standard, the device that sends data changes the data on the falling edge of the clock, and the device that receives data samples the data on the rising edge of the clock. The WS signal should be valid one clock before the first data bit (MSB) is sent and will change on the falling edge of the clock signal.

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Figure 26-14 I²S Philips protocol waveform (16/32-bit full precision, CLKPOL = 0)

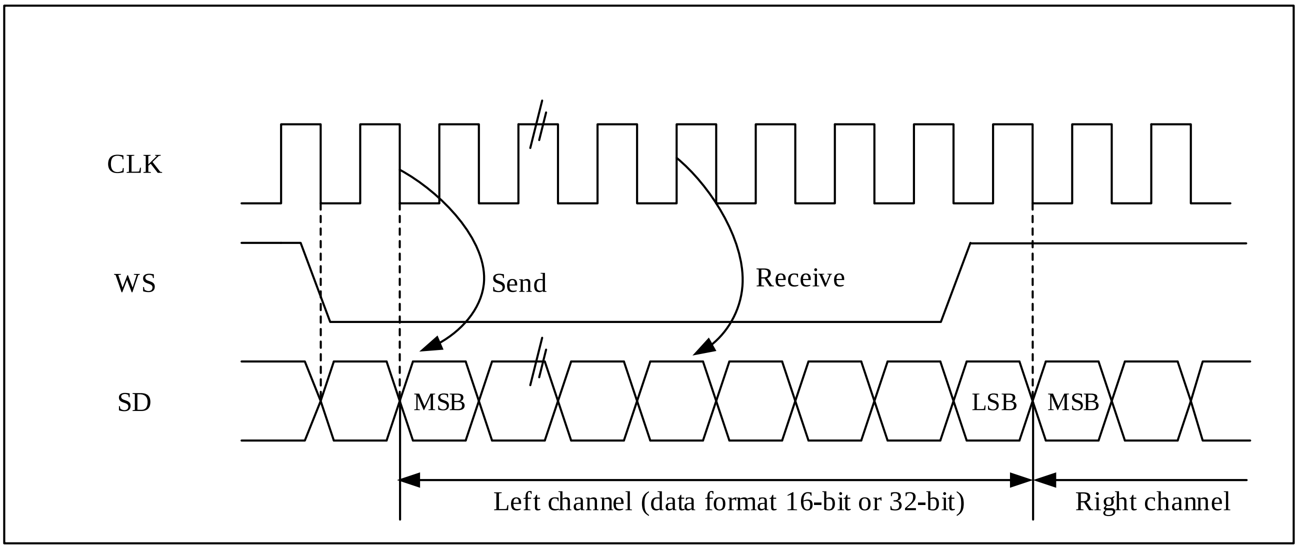
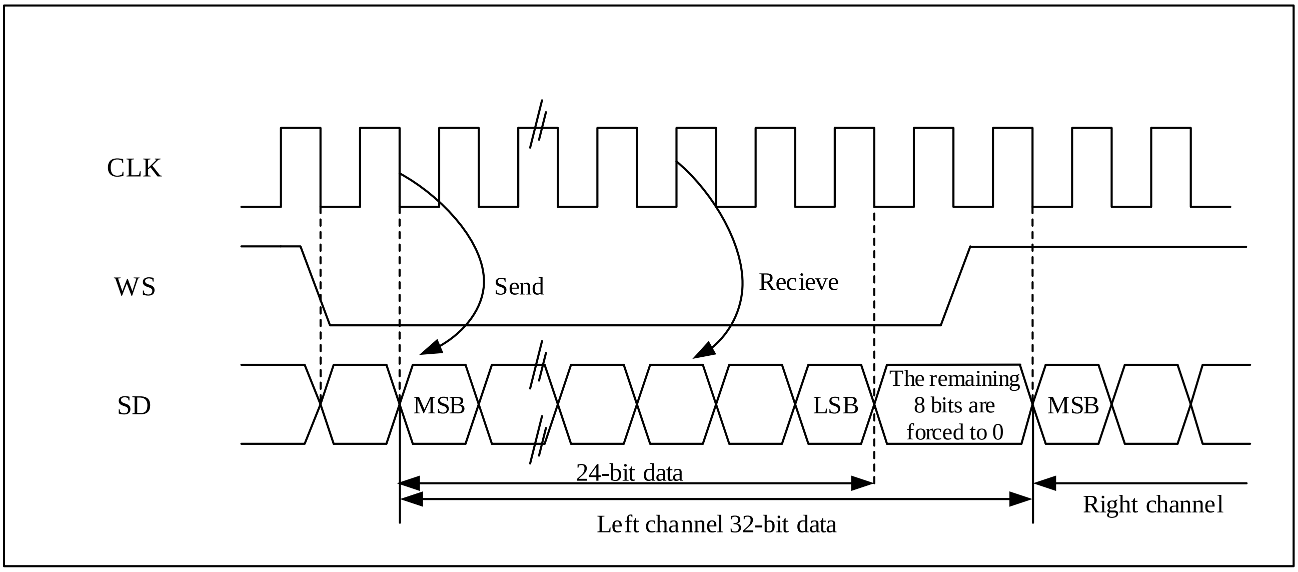


Figure 26-15 I²S Philips protocol standard waveform (24-bit frame, CLKPOL = 0)



If the 24-bit data needs to be packaged into 32-bit data frame format, the CPU needs to read or write the SPI_DAT register twice during each frame of data transmission. For example, if the user sends 24-bit data 0x95AA66, the CPU will first write 0x95AA into the SPI_DAT register, and then write 0x66XX into the SPI_DAT register (only the upper 8-bit data is valid, the lower 8-bit data is meaningless and can be any value); if the user receives 24-bit data 0x95AA66, the CPU will first read the SPI_DAT register to get 0x95AA, and then read the SPI_DAT register to get 0x6600 (only the upper 8-bit data is valid, and the lower 8-bit data is always 0).

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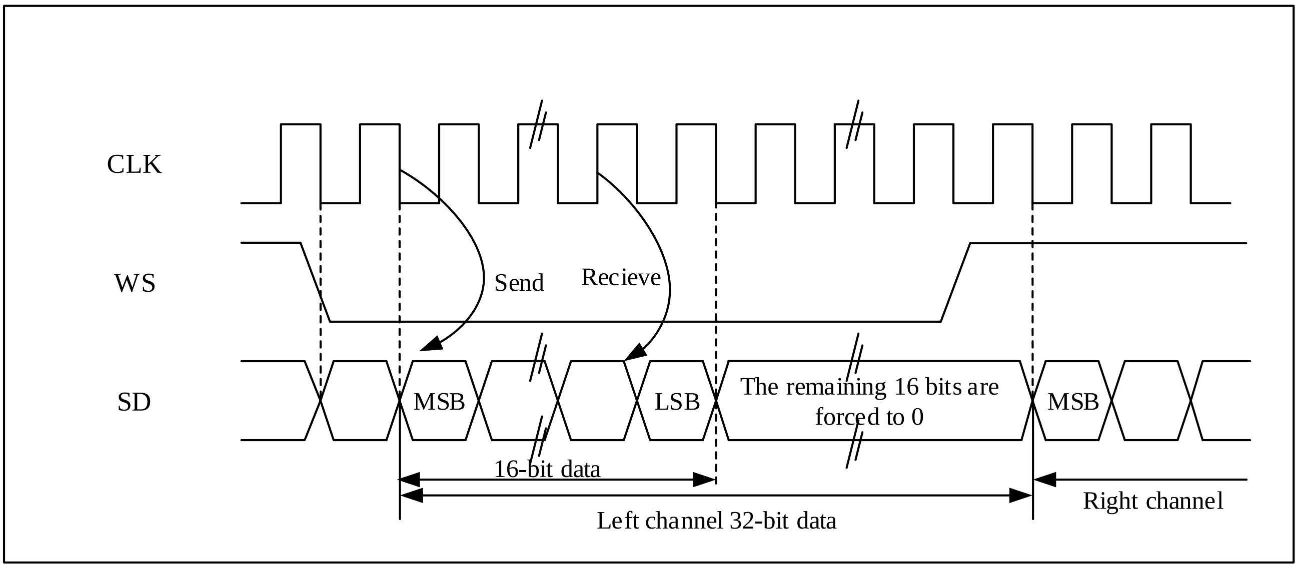
Figure 26-16 I^{2}S Philips protocol standard waveform (16-bit extended to 32-bit packet frame, CLKPOL = 0)



If 16-bit data needs to be packed into 32-bit data frame format, the CPU only needs to read or write the SPI_DAT register once for each frame of data transmission. The lower 16 bits of data for expansion to 32 bits are always set to 0x0000. For example, if the user sends or receives 16-bit data 0x89C1 (extended to 32-bit data is 0x89C10000). In the process of sending data, the upper 16-bit half word (0x89C1) needs to be written into the SPI_DAT register; the user can write new data until the SPI_STS.TE bit is set. An interrupt is generated if the user enables the corresponding interrupt. The sending is performed by hardware, even if the last 16 bits (0x0000) are not sent, the hardware will set the TE (SPI_STS.TE) bit to 1 and the corresponding interrupt will be generated. In the process of receiving data, the RNE flag (SPI_STS.RNE) will be set to 1 after each time the device receives the upper 16-bit halfword (0x89C1). An interrupt is generated if the user enables the corresponding interrupt. In this way, there is more time between 2 reads and writes, which can prevent underflow or overflow from happening.

MSB alignment standard

In the MSB alignment standard, the device sending the data will change the data on the falling edge of the clock, and the device receiving the data will sample the data on the rising edge of the clock. The WS signal and the first data bit (MSB) are generated simultaneously.

The standard data receiving and sending processing mode is the same as I^{2}S Philips standard.

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Figure 26-17 The MSB is aligned with 16-bit or 32-bit full precision, CLKPOL = 0.

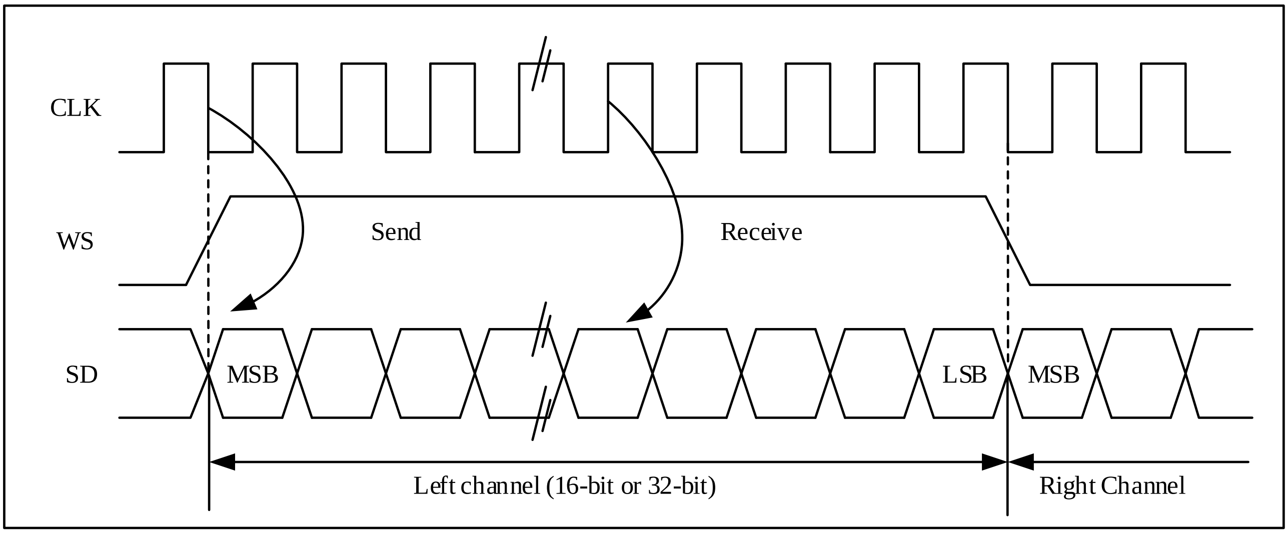

Figure 26-18 MSB aligns 24-bit data, CLKPOL = 0

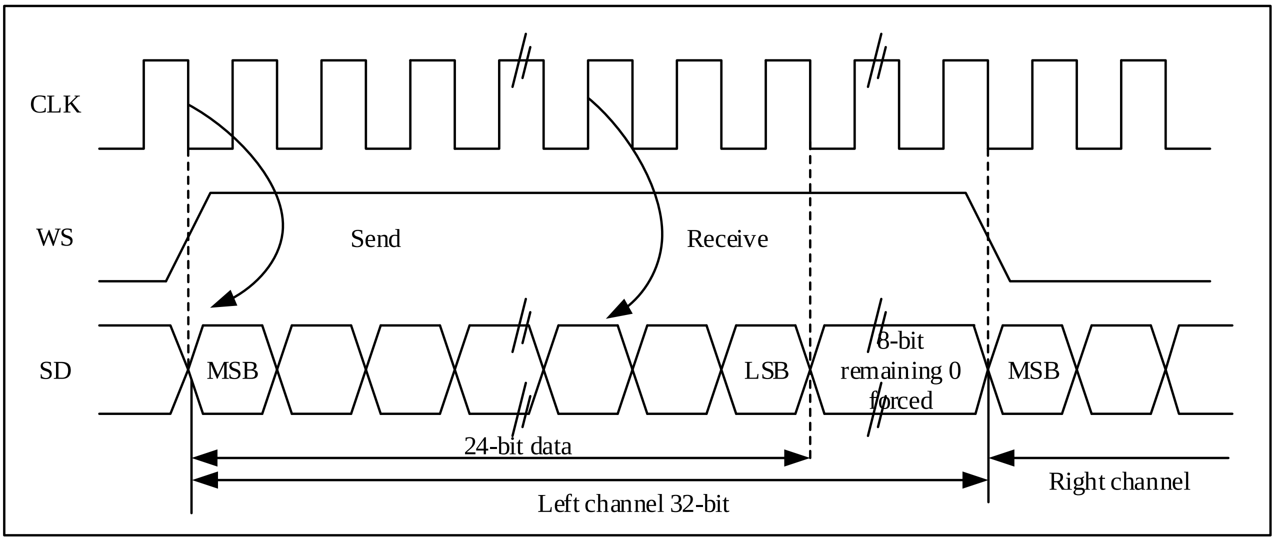

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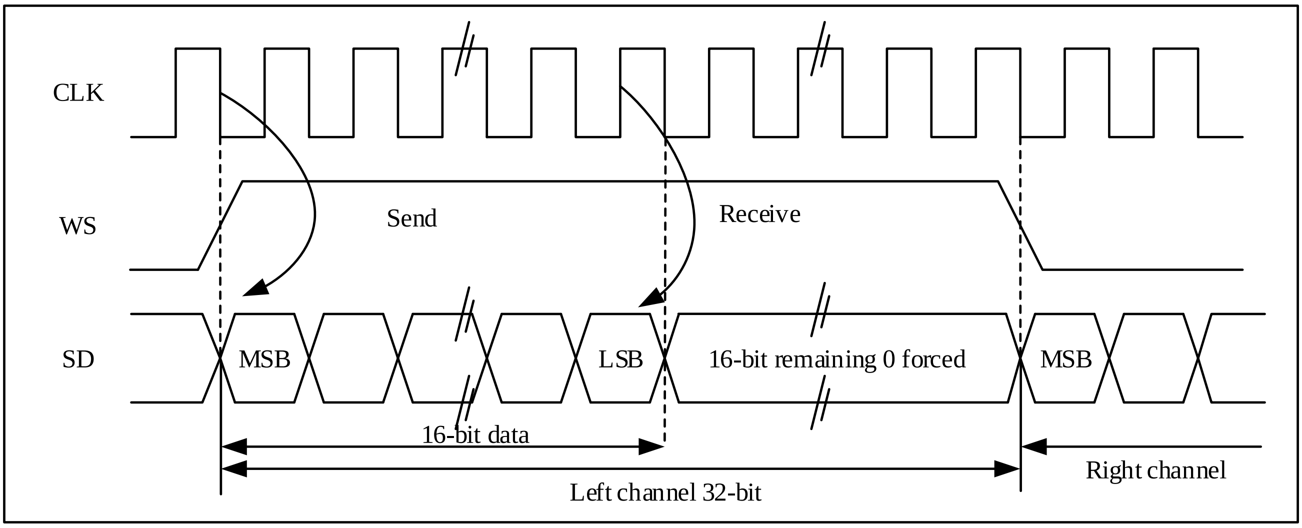
Figure 26-19 MSB-aligned 16-bit data is extended to 32-bit packet frame, CLKPOL = 0



LSB alignment standard

In 16-bit or 32-bit full-precision frame format, LSB alignment standard is the same as MSB alignment standard.

Figure 26-20 LSB alignment 16-bit or 32-bit full precision, CLKPOL = 0

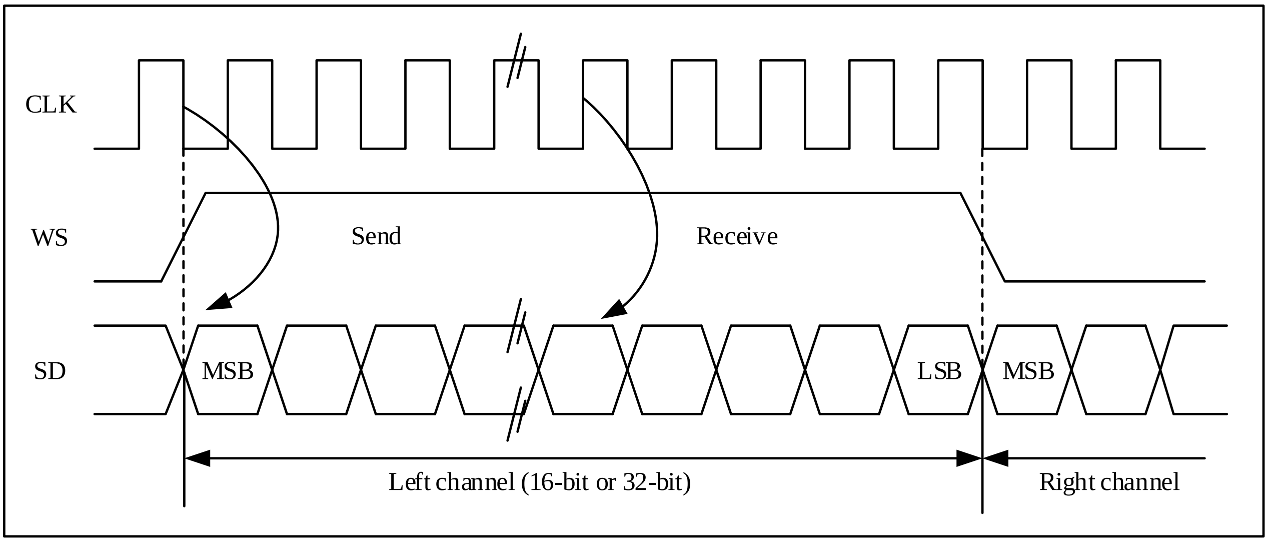


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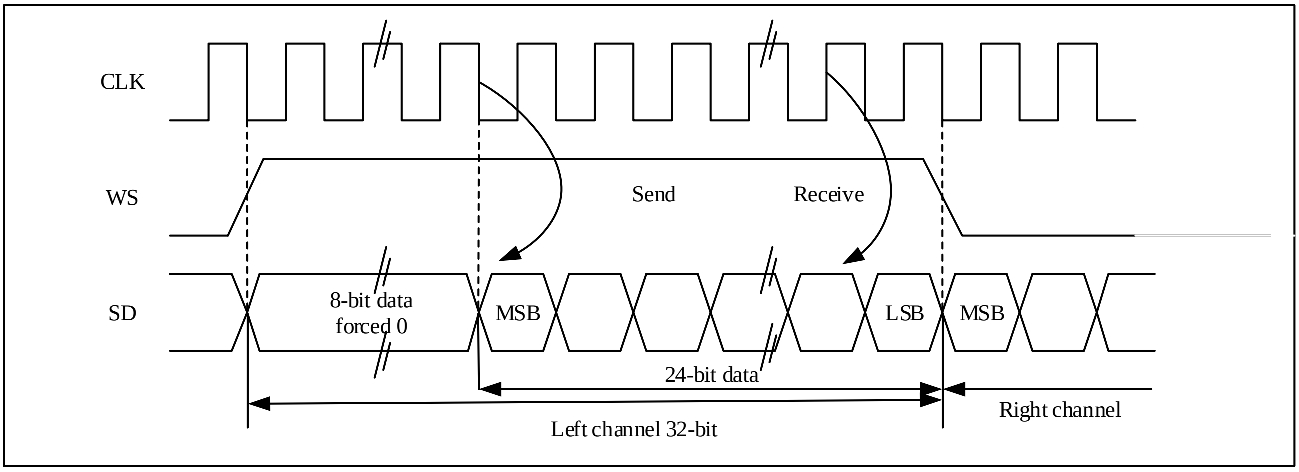
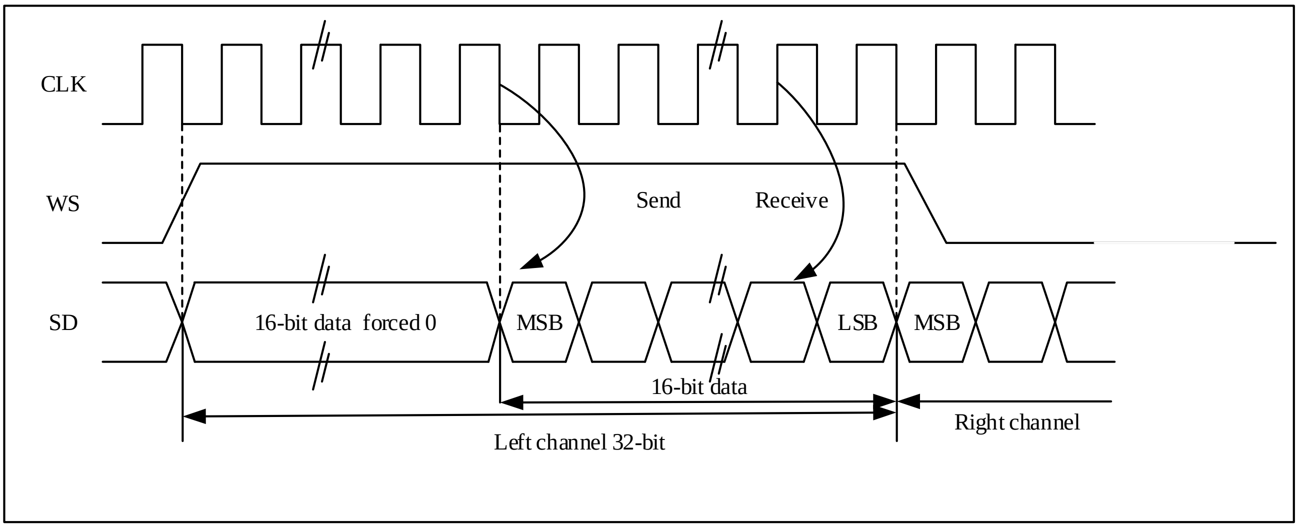
Figure 26-21 LSB aligns 24-bit data, CLKPOL = 0



If the 24-bit data needs to be packed into the 32-bit data frame format, the CPU needs to read or write the SPI_DAT register twice during each frame of data transmission. For example, if the user sends 24-bit data 0x95AA66, the CPU will first write 0xXX95 (only the lower 8-bit data is valid, the upper 8-bit data is meaningless and can be any value) into the SPI_DAT register, and then write 0xAA66 into the SPI_DAT register. If the user receives 24-bit data 0x95AA66, the CPU will first read the SPI_DAT register to get 0x0095 (only the lower 8 bits are valid, the upper 8 bits are always 0), and then read the SPI_DAT register to get 0xAA66.

Figure 26-22 LSB aligned 16-bit data is extended to 32-bit packet frame, CLKPOL = 0



If the 16-bit data needs to be packaged into a 32-bit data frame format, the CPU only needs to read or write the SPI_DAT register once for each frame of data transmission. The upper 16 bits of extended to 32 bits data are set to 0x0000 by hardware, if the user sends or receives 16-bit data 0x89C1 (extended to 32-bit data is 0x000089C1). In the process of sending data, the upper 16-bit halfword (0x0000) needs to be written to the SPI_DAT register first; once the valid data starts to be send, the next TE (SPI_STS.TE) event will be generated. In the process of receiving data, once the device receives valid data, the RNE (SPI_STS.RNE) event will be generated. In this way, there is more time between 2 reads and writes, which can prevent underflow or overflow from happening.

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PCM standard

In the PCM standard, there are two frame structures, short frame and long frame. The user can select the frame structure by setting the SPI_I2SCFG.PCMFSYNC bits. The WS signal indicates frame synchronization information. The WS signal for synchronizing long frames is 13 bits effective; the WS signal length for synchronizing short frames is 1 bit.

The standard data receiving and sending processing mode is the same as I^2S Philips standard.

Figure 26-23 PCM standard waveform (16 bits)

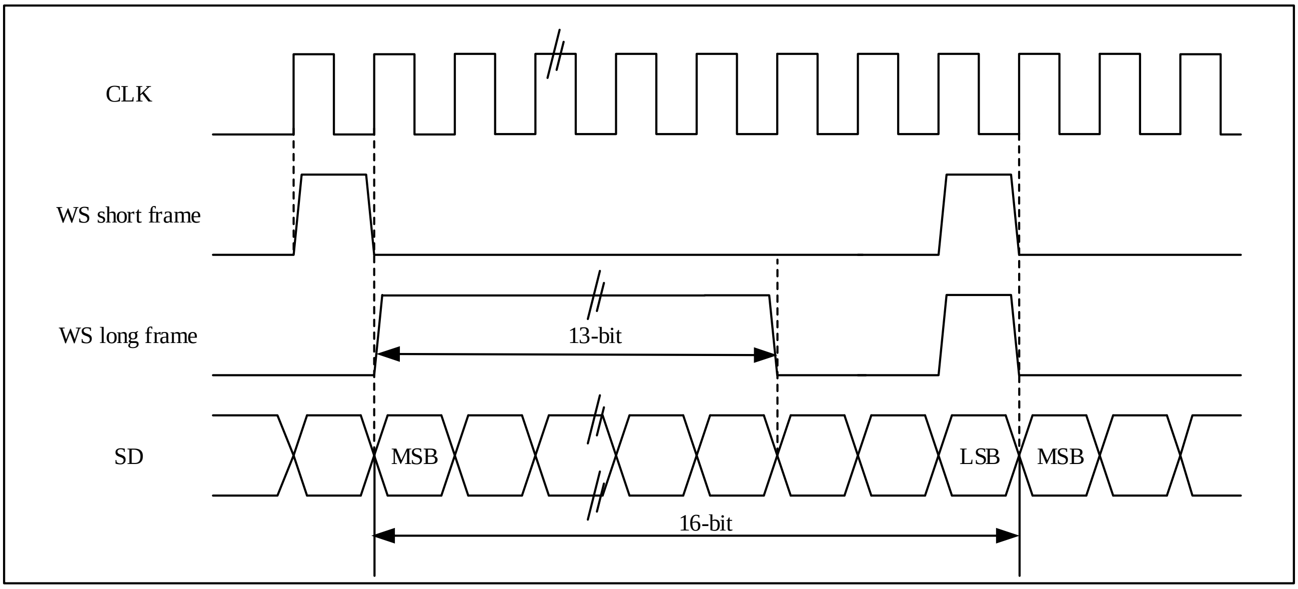
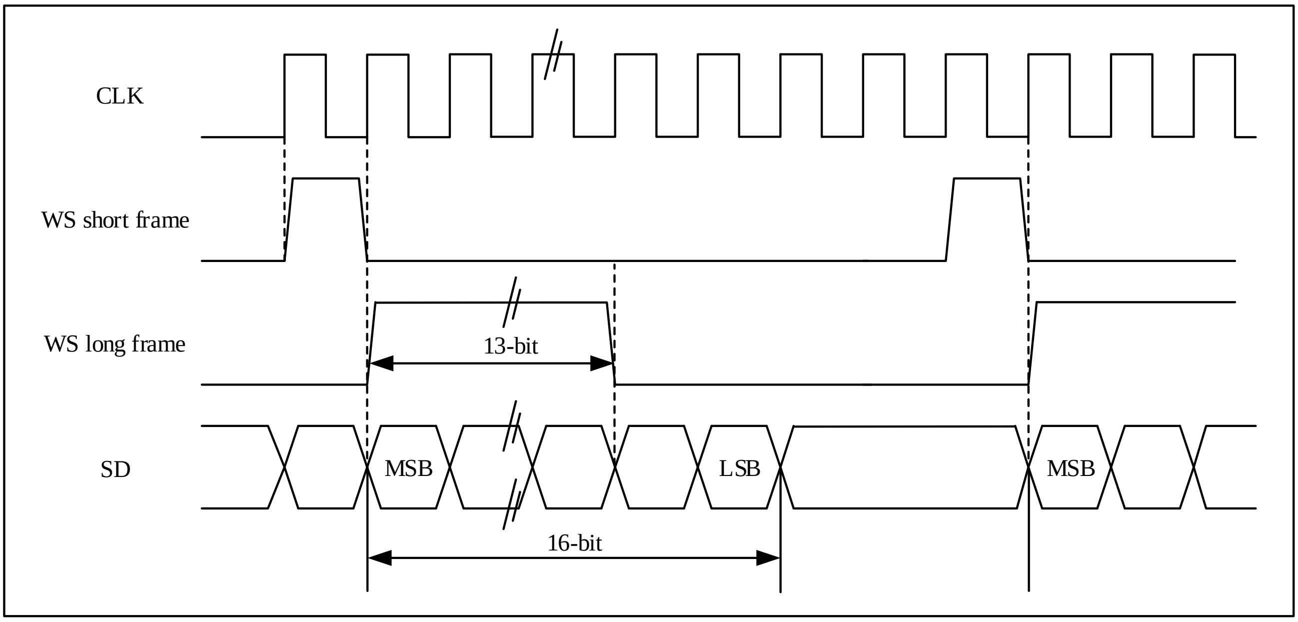


Figure 26-24 PCM standard waveform (16-bit extended to 32-bit packet frame)



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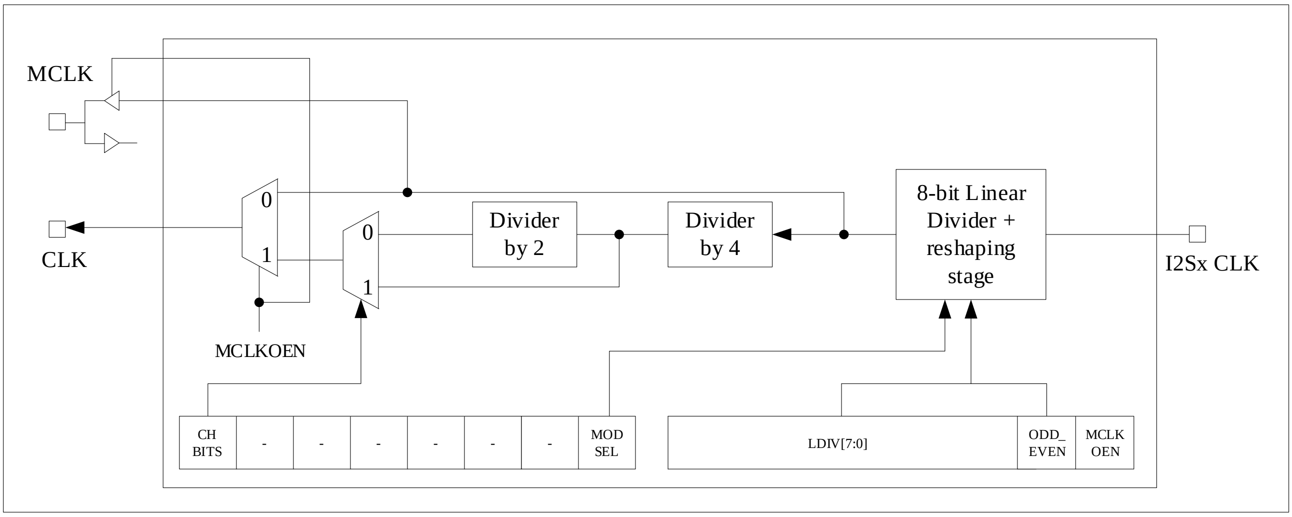
26.4.2 Clock generator

In the master mode, the linear divider needs to be set correctly in order to obtain the desired audio frequency.

Figure 26-25 I^2S clock generator structure



Note: The clock source of I^2Sx CLK is MSI, HSI, HSE or PLL system clock that drives AHB clock.

The bit rate of I2S determines the data flow on the I2S data line and the frequency of the I2S clock signal.

I^2S bit rate = number of bits per channel × number of channels × audio sampling frequency

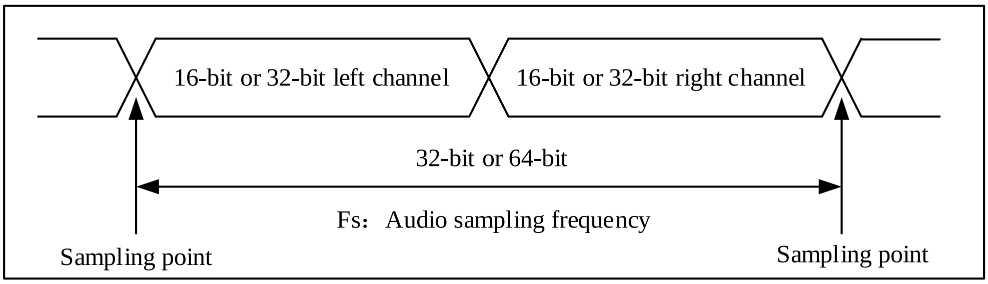
For a signal with left and right channels and 16-bit audio, the I2S bit rate is calculated as:

I^2S bit rate = 16 × 2 × F_S

If the packet length is 32 bits, there are:

I^2S bit rate = 32 × 2 × F_S

Figure 26-26 Audio sampling frequency definition



The sampling signal frequency of the audio can be set by setting the SPI_I2SPREDIV.ODD_EVEN bit and the SPI_I2SPREDIV.LDIV[7:0] bits. Audio can be sampled at 96kHz, 48kHz, 44.1kHz, 32kHz, 22.05kHz, 16kHz, 11.025kHz, or 8kHz (or any value within this range). Set the linear divider according to the following formula:

When MCLKOEN = 1 and CHBITS= 0, $F_S = I^2Sx\,CLK/[(16 \times 2) \times ((2 \times LDIV) + ODD\_EVEN) \times 8]$

When MCLKOEN = 1 and CHBITS = 1, $F_S = I^2Sx\,CLK/[(32 \times 2) \times ((2 \times LDIV) + ODD\_EVEN) \times 4]$

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When MCLKOEN = 0 and CHBITS = 0, $F_S = I^2Sx\ CLK/[(16 \times 2) \times ((2 \times LDIV) + ODD\_EVEN)]$

When MCLKOEN = 0 and CHBITS = 1, $F_S = I^2Sx\ CLK/[(32 \times 2) \times ((2 \times LDIV) + ODD\_EVEN)]$

The exact audio frequency can be obtained by referring to the clock configuration in the table below.

Table 26-2 Use the standard 8MHz HSE clock to get accurate audio frequency.

SYSCLK (MHz)	I^2S_LDIV		I^2S_ODD_EVEN		MCLK	Target F_S(Hz)	Real F_S(Hz)		Error	
	16 bits	32 bits	16 bits	32 bits			16bit	16 bits	32 bits	16 bits
54	9	4	0	1	without	96000	93750	93750	2.34%	2.34%
54	17	9	1	0	without	48000	48214.29	46875	0.45%	2.34%
54	19	9	0	1	without	44100	44407.89	44407.89	0.70%	0.70%
54	26	13	1	0	without	32000	31839.62	32451.92	0.50%	1.41%
54	38	19	1	0	without	22050	21915.58	22203.95	0.61%	0.70%
54	53	26	0	1	without	16000	15919.81	15919.81	0.50%	0.50%
54	76	38	1	1	without	11025	11029.41	10957.79	0.04%	0.61%
54	105	52	1	1	without	8000	7997.63	8035.71	0.03%	0.45%
54	1	1	0	0	yes	96000	105468.75	105468.75	9.86%	9.86%
54	2	2	0	0	yes	48000	52734.37	52734.37	9.86%	9.86%
54	2	2	1	1	yes	44100	42187.5	42187.5	4.34%	4.34%
54	3	3	1	1	yes	32000	30133.93	30133.93	5.83%	5.83%
54	5	5	0	0	yes	22050	21093.75	21093.75	4.34%	4.34%
54	6	6	1	1	yes	16000	16225.96	16225.96	1.41%	1.41%
54	9	9	1	1	yes	11025	11101.97	11101.97	0.70%	0.70%
54	13	13	0	0	yes	8000	8112.98	8112.98	1.41%	1.41%

26.4.3 I^2S Transmission and reception sequence

I^2S initialization sequence

1. The user can set the SPI_I2SPREDIV.LDIV [7:0] bits and SPI_I2SPREDIV.ODD_EVEN bit to configure the related prescaler and serial clock baud rate;
2. If the user needs the master device to provide the main clock MCLK to the external DAC/ADC audio device, set the SPI_I2SPREDIV.MCLKOEN = 1. (Calculate LDIV and ODD_EVEN according to different clock outputs, see section 26.4.2).
3. The user can set the SPI_I2SCFG.CLKPOL bit to define the polarity of the communication clock when idle; the user can set the SPI_I2SCFG.MODSEL = 1 to configure the device to be in I2S mode, and set SPI_I2SCFG.MODCFG[1:0] bits to select the I2S master-slave mode and transmission direction (send or receive); set SPI_I2SCFG.STDSEL[1:0] bits to select the corresponding I2S standard (under the PCM standard, set the SPI_I2SCFG.PCMFSYNC bit to select the PCM frame synchronization mode); set SPI_I2SCFG.TDATLEN [1: 0] bits to select length of data to be transmitted, and select the number of data bits of per channel by set the SPI_I2SCFG.CHBITS bit;
4. When user needs to enable interrupt or DMA, the configuration operation is the same as SPI;

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5. Finally, set the SPI_I2SCFG.I2SEN = 1 to start I2S communication.

Sending sequence

Master mode

When I2S works in master mode, the CLK pin outputs the serial clock, the WS pin generates the channel selection signal, and set the SPI_I2SPR.MCLKOEN bit to select whether to output the master clock (MCLK).

The sending process begins when data is written to the send buffer. When the data of the current channel is moved from the send buffer to the shift register in parallel, the flag bit TE (SPI_STS.TE) is set to '1'. At this time, the data of the other channel should be written into SPI_DAT. The channel corresponding to the current data to be transmitted is confirmed by the flag bit CHSIDE (SPI_STS. CHSIDE). The value of CHSIDE (SPI_STS. CHSIDE) is updated when TE (SPI_STS.TE) is set to '1'. A complete data frame includes left and right channels, and only part of the data frame cannot be transmitted. When the flag bit TE (SPI_STS.TE) is set to '1', if the SPI_CTRL2.TEINTEN = 1, an interrupt will be generated.

The operation of writing data depends on the selected I2S standard. See chapter 26.4.1 for details.

When the user wants to turn off the I2S function, wait for the TE flag (SPI_STS.TE) bit to be 1 and the BUSY flag (SPI_STS.BUSY) bit to be 0, and then clear the SPI_I2SCFG.I2SEN bit to 0.

Slave mode

The sending process of the slave mode is similar to that of the master mode, the difference is as follows:

When I2S works in slave mode, there is no need to configure the clock, and the CLK pin and WS pin are connected to the corresponding pins of the master device. The sending process begins when an external master sends a clock signal, and when a WS signal requires data transfer. Only when the slave device is enabled and the data has been written to the I2S data register, the external master device can start communication.

When the first clock edge representing the next data transfer arrives, the new data has not been written into the SPI_DAT register, an underflow occurs, and the SPI_STS.UNDER flag bit is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated to indicate that an error has occurred.

The SPI_STS.CHSIDE flag indicates which channel the currently transmitted data corresponds to. Compared with the master mode sending process, in the slave mode, CHSIDE depends on the WS signal of the external master I2S device (WS signal is 1 means the left channel)

Receiving sequence

Master mode

Audio is always received in 16-bit packets. According to the configured data and channel length, the received audio data will need to be transferred to the receive buffer once or twice.

When the data is transferred from the shift register to the receive buffer, the SPI_STS.RNE flag bit is set to 1, at this time, the data is ready and can be read from the SPI_DAT register. If the SPI_CTRL2.RNEINTEN bit is set to 1, an interrupt will be generated. Reading the SPI_DAT register to clear the SPI_STS.RNE flag. If the previously received data is not read, new data is received again, an overflow occurs, and the SPI_STS.OVER flag is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated to indicate that an error has occurred.

The channel corresponding to the currently transmitted data can be confirmed by the SPI_STS.CHSIDE bit. When

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the SPI_STS.RNE flag bit is set to 1, the SPI_STS.CHSIDE value is updated.

The operation of reading data depends on the selected I^2S standard. See Section 26.4.1 for details.

When I^2S function is turned off, different audio standards, data length and channel length adopt different operation steps:

- Data length is 16 bits, channel length is 32 bits (SPI_I2SCFG.TDATTLEN = 00, SPI_I2SCFG.CHBITS = 1), LSB alignment standard (SPI_I2SCFG.STDSEL = 10).
  1. Wait for the penultimate RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2. Software delay, waiting for 17 I^2S clock cycles.
  3. Turn off I^2S (SPI_I2SCFG.I2SEN = 0).
- The data length is 16 bits, the channel length is 32 bits (SPI_I2SCFG.TDATLEN = 00 and SPI_I2SCFG.CHBITS = 1), the MSB alignment standard (SPI_I2SCFG.STDSEL = 01), I^2S Philips standard (SPI_I2SCFG.STDSEL = 00) or PCM standard (SPI_I2SCFG.STDSEL = 11)
  1. Wait for the last RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2. Software delay, waiting for 1 I^2S clock cycle.
  3. Turn off I^2S (SPI_I2SCFG.I2SEN = 0).
- Other combinations of SPI_I2SCFG.TDATLEN and SPI_I2SCFG.CHBITS and any audio mode selected by SPI_I2SCFG.STDSEL:
  1. Wait for the penultimate RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2. Software delay, waiting for 1 I^2S clock cycle.
  3. Turn off I^2S (SPI_I2SCFG.I2SEN = 0).

Slave mode

The receiving process of the slave mode is similar to that of the master mode, with the following differences:

The CHSIDE flag (SPI_STS.CHSIDE) indicates which channel corresponds to the currently transmitted data. Compared with the master mode receiving process, in the slave mode, SPI_STS.CHSIDE depends on the WS signal of the external master device. When the I2S function is turned off, clear the SPI_I2SCFG.I2SEN bit to 0 when the SPI_STS.RNE flag is 1.

26.4.4 Status flag

There are the following 4 flag bits in the SPI_STS register for monitoring the status of the I2S bus.

TX buffer empty flag (TE)

When the send buffer is empty, this flag is set to 1, indicating that new data can be written into the SPI_DAT register. When the send buffer is not empty, this flag is cleared to 0.

RX buffer not empty flag (RNE)

When the receive buffer is not empty, this flag is set to 1, indicating that valid data has been received into the receive

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buffer. When reading the SPI_DAT register, this flag is set to 0.

BUSY flag (BUSY)

When the transfer starts, the BUSY flag (SPI_STS.BUSY) is set to 1, and when the transfer ends, the BUSY flag (SPI_STS.BUSY) is set to 0 by hardware (software operation is invalid).

In master receiving mode (SPI_I2SCFG.MODCFG=11), the BUSY flag (SPI_STS.BUSY) is set to 0 during receiving. When the I2S module is turned off or the transmission is completed, this flag is set to 0.

In the slave continuous communication mode, between each data item transmission, the BUSY flag (SPI_STS.BUSY) goes low in 1 I^2S clock cycle. Therefore, do not use the BUSY flag (SPI_STS.BUSY) to handle the sending and receiving of each data item.

Channel Side flag (CHSIDE)

The CHSIDE (SPI_STS.CHSIDE) bit is used to indicate the channel where the data currently sent and received is located. Under the PCM standard, this flag has no meaning.

In send mode, the flag is updated when the TE flag (SPI_STS.TE) is set; in receive mode, the flag is updated when the RNE flag (SPI_STS.RNE) is set. In the process of sending and receiving, if an overflow (SPI_STS.OVER) or underflow (SPI_STS.UNDER) error occurs, this flag is meaningless, and the I2S needs to be turned off and then turned on again.

26.4.5 Error flag

The SPI_STS register has 2 error flag bits.

Overflow flag (OVER)

When the RNE flag (SPI_STS.RNE) is set to 1, but there is still data sent to the receive buffer, an overflow error will occur. At this time, the OVER flag (SPI_STS.OVER) is set to 1. An interrupt will be generated if the user enables the corresponding interrupt. All data received after this time will be lost, and the SPI_DAT register only retains the previously unread data.

Reading the SPI_DAT register and the SPI_STS register in turn to clear the SPI_STS.OVER bit.

Underflow flag (UNDER)

In slave send mode, when the first clock edge of sending data arrives, if the send buffer is still empty, the UNDER flag (SPI_STS.UNDER) is set to 1. An interrupt will be generated if the user enables the corresponding interrupt.

Reading the SPI_STS register to clears the SPI_STS.UNDER bit.

26.4.6 I^2S interrupt

The following table lists all I^2S interrupts.

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Table 26-3 I²S interrupt request

Interrupt event	Event flag bit	Enable control bit
Send buffer empty flag	TE	TEINTEN
Receive buffer non empty flag	RNE	RNEINTEN
Underflow flag bit	UNDER	ERRINTEN
Overflow flag bit	OVER	

26.4.7 DMA function

Working in I2S mode, it does not need data transmission protection function, so it does not need to support CRC, other DMA functions are the same as SPI mode.

26.5 SPI and I²S registers

26.5.1 SPI register overview

Table 26-4 SPI register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	SPI_CTRL1	Reserved																BIDIRMODE	BIDIROEN	CRCEN	CRCNEXT	DATFF	RONLY	SSMEN	SSEL	LSBFF	SPIEN	BR[2:0]			MSEL	CLKPOL	CLKPHA
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	SPI_CTRL2	Reserved																								TEINTEN	RNEINTEN	ERRINTEN	Reserved		SSOEN	TDMAEN	RDMAEN
	Reset Value																									0	0	0			0	0	0
008h	SPI_STS	Reserved																								BUSY	OVER	MODERR	CRCERR	UNDER	CHSIDE	TE	RNE
	Reset Value																									0	0	0	0	0	0	1	0
00Ch	SPI_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	SPI_CRCPOLY	Reserved																CRCPOLY[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
014h	SPI_CRCRDAT	Reserved																CRCRDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	SPI_CRCTDAT	Reserved																CRCTDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	SPI_I2SCFG	Reserved																				MODSEL	I2SEN	MODCFG[1:0]		PCMFSYNC	Reserved	STDSEL[1:0]		CLKPOL	TDATLEN[1:0]		CHBITS
	Reset Value																					0	0	0	0	0		0	0	0	0	0	0
020h	SPI_I2SPREDIV	Reserved																						MCLKOEN	ODD_EVEN	LDIV[7:0]							
	Reset Value																							0	0	0	0	0	0	0	0	1	0

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26.5.2 SPI control register 1 (SPI_CTRL1) (not used in I2S mode)

Address: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDIRMODE	BIDIROEN	CRCEN	CRCNEXT	DATFF	RONLY	SSMEN	SSEL	LSBFF	SPIEN	BR[2:0]			MSEL	CLKPOL	CLKPHA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw			rw	rw	rw

Bit field	name	describe
15	BIDIRMODE	Bidirectional data mode enable 0: Select the "two-wire one-way" mode. 1: Select the "one-wire bidirectional " mode. *Note: Not used in I^2S mode.*
14	BIDIROEN	Output enable in bidirectional mode 0: Output disable (receive-only mode). 1: Output enabled (send-only mode). In master mode, the "one-wire" data line is the MOSI pin, and in slave mode, the "one-wire" data line is the MISO pin. *Note: Not used in I^2S mode.*
13	CRCEN	Hardware CRC check enable 0: Disable CRC calculation. 1: Enable CRC calculation. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* This bit can only be used in full duplex mode. *Note: Not used in I^2S mode.*
12	CRCNEXT	Send CRC next 0: The next sent value comes from the send buffer. 1: The next send value comes from the CRC register. *Note: This bit should be set immediately after the last data is written in SPI_DAT register.* *Note: Not used in I^2S mode.*
11	DATFF	Data frame format 0: 8-bit data frame format is used for sending/receiving. 1: 16-bit data frame format is used for sending/receiving. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* *Note: Not used in I^2S mode.*
10	RONLY	Only receive mode This bit, together with the SPI_CTRL1.BIDIRMODE bit, determines the transfer direction in two-wire one-way mode. In the application scenario of multiple slave devices, this bit is only set to 1 by the accessed slave device, and only the accessed slave device can output, so as to avoid data line conflicts.

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Bit field	name	describe
		0: Full duplex (sending mode and receiving mode). 1: Disable output (receive-only mode). *Note: Not used in I^2S mode.*
9	SSMEN	Software slave device management When the SPI_CTRL1.SSMEN bit is set to 1, the NSS pin level is determined by the value of the SPI_CTRL1.SSEL bit. 0: Disable software slave device management. 1: Enable software slave device management. *Note: Not used in I^2S mode.*
8	SSEL	Internal slave device selection This bit only has meaning when the SPI_CTRL1.SSMEN bit is set. It determines the NSS level, and I/O operations on the NSS pin have no effect. *Note: Not used in I^2S mode.*
7	LSBFF	Frame format 0: Send MSB first. 1: Send LSB first. *Note: This bit cannot be changed during communication.* *Note: Not used in I^2S mode.*
6	SPIEN	SPI enable 0: Disable SPI device. 1: Enable the SPI device. *Note: Not used in I^2S mode.* *Note: When turning off the SPI device, please follow paragraph 26.3.4 Section's procedure operation.*
5:3	BR[2:0]	Baud rate control 000: fPCLK/2 001: fPCLK/4 010: fPCLK/8 011: fPCLK/16 100: fPCLK/32 101: fPCLK/64 110: fPCLK/128 111: fPCLK/256 *Note: This bit cannot be changed during communication.* *Note: Not used in I^2S mode.*
2	MSEL	Master device selection 0: Configure as the slave device. 1: Configure as the master device. *Note: This bit cannot be changed during communication.* *Note: Not used in I^2S mode.*
1	CLKPOL	Clock polarity

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Bit field	name	describe
		0: In idle state, SCLK remains low. 1: In idle state, SCLK remains high. *Note: This bit cannot be changed during communication.* *Note: Not used in I^2S mode.*
0	CLKPHA	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.* *Note: Not used in I^2S mode.*

26.5.3 SPI control register 2 (SPI_CTRL2)

Address: 0x04

Reset value: 0x0000

15 ... 8	7	6	5	4 ... 3	2	1	0
Reserved	TE INTEN	RNE INTEN	ERR INTEN	Reserved	SSOEN	TDMAEN	RDMAEN
	rw	rw	rw		rw	rw	rw

Bit field	name	describe
15:8	Reserved	Reserved, the reset value must be maintained.
7	TEINTEN	Send buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when TE flag (SPI_STS.TE) is set to '1'.
6	RNEINTEN	Receive buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when RNE flag (SPI_STS.RNE) is set to ‘1’.
5	ERRINTEN	Error interrupt enable When an error (SPI_STS.CRCERR, SPI_STS.OVER, SPI_STS.UNDER, SPI_STS.MODERR) is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
4:3	Reserved	Reserved, the reset value must be maintained.
2	SSOEN	NSS output enable 0: Disable NSS output in master mode, the device can work in multi-master mode. 1: When the device is turned on, enable NSS output in the master mode, the device cannot work in the multi-master device mode. *Note: Not used in I^2S mode.*
1	TDMAEN	Send buffer DMA enable When this bit is set, a DMA request is issued as soon as the TE flag(SPI_STS.TE) is set

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Bit field	name	describe
		0: Disable send buffer DMA. 1: Enable send buffer DMA.
0	RDMAEN	Receive buffer DMA enable When this bit is set, a DMA request is issued as soon as the RNE flag(SPI_STS.RNE) is set 0: Disable receive buffer DMA. 1: Enable receive buffer DMA.

26.5.4 SPI status register (SPI_STS)

Address: 0x08

Reset value: 0x0002

15-8	7	6	5	4	3	2	1	0
Reserved	BUSY	OVER	MODERR	CRCERR	UNDER	CHSIDE	TE	RNE
	r	r	r	rc_w0	r	r	r	r

Bit field	name	describe
15:8	Reserved	Reserved, the reset value must be maintained.
7	BUSY	Busy flag 0: SPI is not busy. 1: SPI is busy communicating or the send buffer is not empty. This bit is set or reset by hardware. *Note: special attention should be paid to the use of this sign, see Section 26.3.3 and Section 26.3.4 for details.*
6	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to 26.4.5 for details.*
5	MODERR	Mode error 0: No mode error. 1: A mode error occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to 26.3.7 for details.* *Note: Not used in I^2S mode.*
4	CRCERR	CRC error flag 0: The received CRC value matches the value the SPI_CRCRDAT register value. 1: The received CRC value does not match the SPI_CRCRDAT register value. *Note: this bit is set by hardware and cleared by software by writing 0.* *Note: Not used in I^2S mode.*

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Bit field	name	describe
3	UNDER	Underflow flag 0: No underflow occurred. 1: Underflow occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to 26.4.5 for details.* *Note: not used in SPI mode.*
2	CHSIDE	Channel 0: The left channel needs to be sent or received; 1: The right channel needs to be sent or received. *Note: not used in SPI mode. No meaning in PCM mode.*
1	TE	The send buffer is empty 0: The send buffer is not empty. 1: The send buffer is empty.
0	RNE	Receive buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.

26.5.5 SPI data register (SPI_DAT)

Address: 0x0C

Reset value: 0x0000

15 ... 0
DAT[15:0]
rw

Bit field	name	describe
15:0	DAT[15:0]	Data register Data to be sent or received The data register corresponds to two buffers: one for write (send buffer); The other is for read (receive buffer).Write operation writes data to send buffer; The read operation will return the data in the receive buffer. Note on SPI mode: According to the selection of the data frame format by the SPI_CTRL1.DATFF bit, the data sending and receiving can be 8-bit or 16-bit. To ensure correct operation, the data frame format needs to be determined before enabling the SPI. For 8-bit data, the buffer is 8-bit, and only SPI_DAT[7:0] is used when sending and receiving. When receiving, SPI_DAT[15:8] is forced to 0. For 16-bit data, the buffer is 16-bit, and the entire data register is used when sending and receiving, that is, SPI_DAT[15:0].

26.5.6 SPI CRC polynomial register (SPI_CRCPOLY) (not used in I²S mode)

Address: 0x10

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Reset value: 0x0007

15	0
CRCPOLY[15:0]	
rw	

Bit field	name	describe
15:0	CRCPOLY [15:0]	CRC polynomial register This register contains the polynomial used for the CRC calculation. The reset value is 0x0007, other values can be set according to the application. *Note: not used in I^2s mode.*

26.5.7 SPI RX CRC register (SPI_CRCRDAT) (not used in I^2S mode)

Address offset: 0x14

Reset value: 0x0000

15	0
CRCRDAT[15:0]	
r	

Bit field	name	describe
15:0	CRCRDAT	Receive CRC register When CRC calculation is enabled, CRCRDAT[15:0] will contain the calculated CRC value of subsequent received bytes. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag(SPI_STS.BUSY) is '1' may read incorrect values.* *Note: not used in I^2s mode.*

26.5.8 SPI TX CRC register（SPI_ CRCTDAT）

Address offset: 0x18

Reset value: 0x0000

15	0
CRCTDAT[15:0]	
r	

Bit field	Name	Description
15:0	CRCTDAT	Send CRC register When CRC calculation is enabled, CRCTDAT[15:0] contains the CRC value calculated by the bytes sent subsequently. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY.

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Bit field	Name	Description
		When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag(SPI_STS.BUSY) is '1' may read incorrect values.* *Note: not used in I^{2}s mode.*

26.5.9 SPI_I^{2}S configuration register（SPI_I2SCFG）

Address offset: 0x1c

Reset value: 0x0000

15 … 12	11	10	9 … 8	7	6	5 … 4	3	2 … 1	0
Reserved	MODSEL	I2SEN	MODCFG[1:0]	PCM FSYNC	Reserved	STDSEL[1:0]	CLKPOL	TDATLEN[1:0]	CHBITS
	rw	rw	rw	rw		rw	rw	rw	rw

Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	MODSEL	I^{2}S mode selection 0: Select SPI mode. 1: Select I^{2}S mode. *Note: this bit can only be set when SPI or I^{2}S is turned off.*
10	I^{2}SEN	I^{2}S enable 0: Disable I^{2}S. 1: Enable I^{2}S. *Note: not used in SPI mode.*
9:8	MODCFG	I^{2}S mode setting 00: Slave device sends. 01: Slave device receives. 10: Master device sends. 11: Master device receives. *Note: This bit can only be set when I^{2}S is turned off.* *Note: not used in SPI mode.*
7	PCMFSYNC	PCM frame synchronization 0: Short frame synchronization. 1: Long frame synchronization. *Note: This bit is only meaningful when SPI_I2SCFG.STDSEL = 11 (used by the PCM standard).* *Note: not used in SPI mode.*
6	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
5:4	STDSEL	Selection of I^2S standard 00: I^2S Philips standard. 01: High byte alignment standard (left alignment). 10: Low byte alignment standard (right alignment). 11: PCM standard. See for details of I^2S standard on section 26.4.1. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Not used in SPI mode.*
3	CLKPOL	Static clock polarity 0: I2S clock static state is low level. 1: I2S clock static state is high level. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Note: not used in SPI mode.*
2:1	TDATLEN	Length of data to be transmitted 00: 16-bit data length. 01: 24-bit data length. 10: 32-bit data length. 11: Not allowed. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Note: not used in SPI mode.*
0	CHBITS	Channel length (number of data bits per audio channel) 0: 16 bits wide. 1: 32 bits wide. Writing to this bit is meaningful only when SPI_I2SCFG.TDATLEN = 00, otherwise the channel length is fixed to 32 bits by hardware. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Note: not used in SPI mode.*

26.5.10 SPI_I2S prescaler register (SPI_I2SPREDIV)

Address: 0x20

Reset value: 0x0002

15–10	9	8	7–0
Reserved	MCLKOEN	ODD_EVEN	LDIV[7:0]
	rw	rw	rw

Bit field	Name	Description
15:10	Reserved	Reserved, the reset value must be maintained.
9	MCLKOEN	Master clock output enable 0: Disable master clock output. 1: Enable master clock output.

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Bit field	Name	Description
		Note: For correct operation, this bit can only be set when I^2S is turned off. *Note: not used in SPI mode.*
8	ODD _EVEN	Coefficient prescaler 0: actual frequency division coefficient = LDIV ×2. 1: actual frequency division coefficient = (LDIV ×2) + 1. See Section 26.4.2 for details. *Note: For correct operation, this bit can only be set when I^2S is turned off. Use this bit only in I^2S master mode.* *Not used in SPI mode.*
7:0	LDIV	I^2S linear prescaler Setting LDIV [7:0] = 0 or LDIV [7:0] = 1 is prohibited. See Section 26.4.2 for details. *Note: For correct operation, this bit can only be set when I^2S is turned off. Use this bit only in I^2S master mode.* *Not used in SPI mode.*

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27 Controller area network (CAN)

27.1 Introduction to CAN

As CAN network interface, basic extended CAN supports CAN protocols 2.0A and 2.0B. It can efficiently process a large number of received messages and greatly reduce the consumption of CPU resources. The priority characteristics of message sending can be configured by software, and the hardware function of CAN can support time-triggered communication mode for some applications with high security requirements.

27.2 Main features of CAN

- Baud rate supports up to 1Mbit/s
- CAN protocol 2.0A/B are supported.
- Support time-triggered communication function
- Support individual interrupt control.
- CAN Core Manages the communication between the CAN and the 512 bytes SRAM memory (see Figure 27-3)

Time triggered communication mode

- 16-bit free-running timer
- Automatic retransmission mode is prohibited.
- The last 2 data bytes of a message can be configured as the timestamp.

Send

- There are 3 sending mailboxes.
- Time stamp function for recording the time of sending SOF
- Software can configure the priority characteristics of sending messages.

Receive

- Filter groups support identifier list mode.
- There are two receiving FIFOs, each with a depth of 3 levels.
- A total of 14 filter groups
- Configurable FIFO overrun handling method
- Time stamp function for recording the time of receiving SOF

27.3 CAN overall introduction

With the wide application of CAN, the nodes of CAN network are growing rapidly. Multiple CAN nodes are connected through CAN network. With increase number of CAN nodes, messages in CAN network also increase dramatically which will occupides lots of CPU resource. In this CAN controller, receive FIFOs and filter mechanism

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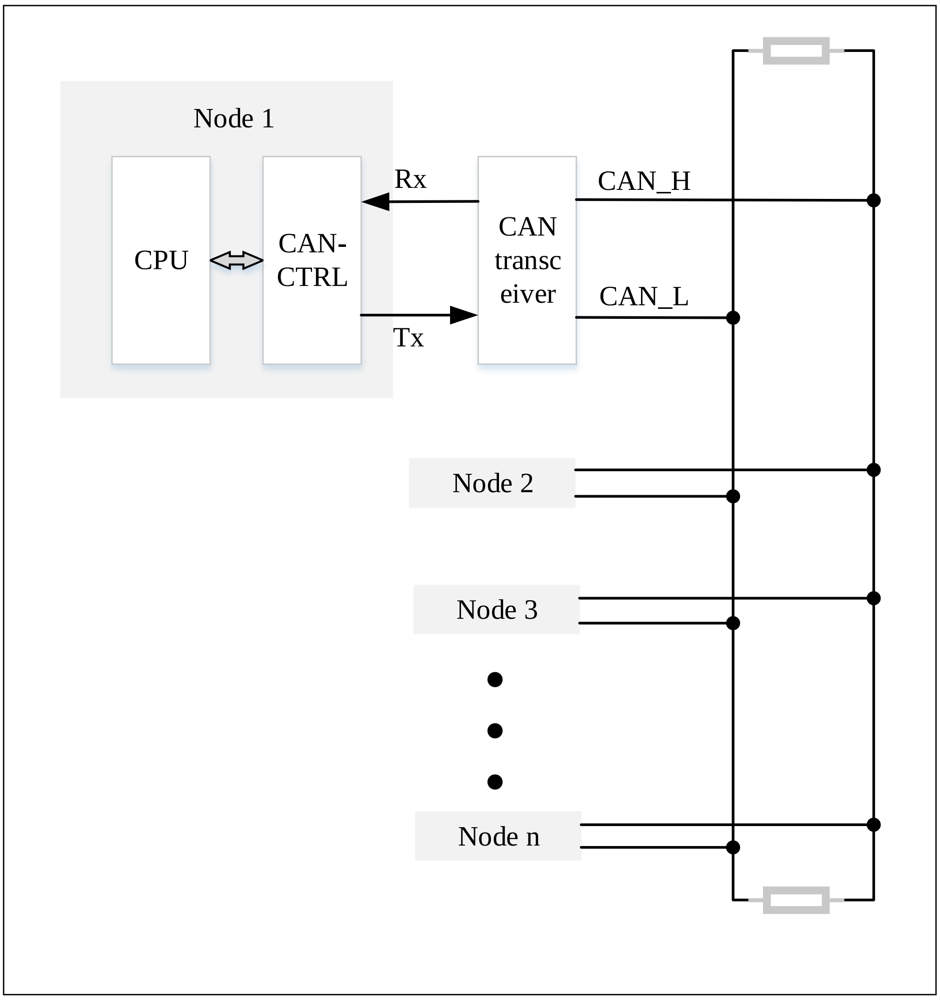
are added as hardware support for CPU message processing and reduce real-time response requirement of CAN message.

Figure 27-1 Topology of CAN network



27.3.1 CAN module

CAN module can automatically receive and send CAN messages, and supports standard identifiers (11 bits) and extended identifiers (29 bits).

27.3.2 CAN working mode

Initialization, normal and sleep mode are three main working modes of CAN. The internal pull-up resistor of CANTX pin is activated after hardware reset, and CAN works in sleep mode to reduce power consumption.

The software can set CAN_MCTRL.INIRQ and CAN_MCTRL.SLPRQ bit to configure CAN to enter **initialization** or **sleep** mode. The software reads values of the CAN_MSTS.INIAK or CAN_MSTS.SLPAK bit to confirm whether the **initialization** or **sleep** mode is entered, at this time the internal pull-up resistor of the CANTX pin is disabled.

CAN is in **normal** mode when CAN_MSTS.INIAK and CAN_MSTS.SLPAK bits are both '0', and it must

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synchronize with CAN bus to enter **normal** mode. When 11 consecutive recessive bits are monitored on the CANRX pin, the CAN bus is idle and synchronization is completed.

27.3.2.1 Normal mode

After the initialization is completed, the software configures CAN to enter normal mode. Clear the CAN_MCTRL.INIRQ and wait for the hardware to clear the CAN_MSTS.INIRQ bit to confirm that CAN enters normal mode. Only after the synchronization with CAN bus is completed, CAN can receive and send messages normally.

Setting the bit width and mode of the filter group must be completed when the filter is in the initialization mode (the CAN_FMC.FINITM bit is 1). Setting the initial value of the filter must be completed when it is inactive (the corresponding CAN_FA1.FAC bit is 0).

27.3.2.2 Initialization mode

The software can perform initialization configuration only when CAN is in initialization mode. Set the CAN_MCTRL.INIRQ bit and clear CAN_MCTRL.SLPRQ bit, and wait for the hardware to set the CAN_MSTS.INIAK bit to confirm that CAN enters the initialization mode. When entering the initialization mode, the register configuration will not be affected. When CAN is in initialization mode, message receiving and sending are prohibited, and the CANTX pin outputs a recessive bit (high level). To exit initialization mode, clear the CAN_MCTRL.INIRQ bit, and wait for the hardware to clear the CAN_MSTS.INIAK bit to confirm that CAN exits the initialization mode.

To perform initialization configuration for CAN by software, at least the bit time characteristic register (CAN_BTIM) and the control register (CAN_MCTRL) need to be configured. The software needs to set the CAN_FMC.FINITM bit to initialize the filter group (mode, bit width, FIFO association, activation and filter value) that configures CAN. Configuring the filter group of CAN does not necessarily need to be in initialization mode.

Specially,when CAN_FMC.FINITM=1, it is forbidden to receive messages. If you want to modify the value of the corresponding filter, you need to first clear the filter activation bit (in CAN_FA1). It is necessary to keep the unused filter group inactive (keep its CAN_FA1.FAC bit to '0').

27.3.2.3 Sleep mode (low power)

To enters sleep mode, set the CAN_MCTRL.SLPRQ bit, and wait for the hardware to set the CAN_MSTS.SLPAK bit to confirm that CAN enters sleep mode. CAN can configure to sleep modeto reduce power consumption when unused. In sleep mode, the clock of CAN stops working, but the software can still access the sending/receiving mailbox register. When CAN is in sleep mode, the CAN_MCTRL.INIRQ bit must be set and the CAN_MCTRL.SLPRQ bit must be clear at the same time so as to enter the initialization mode.

There are two situation to wake up CAN(CAN exits sleep mode):

- When the CAN_MCTRL.AWKUM bit is set(enable hardware wake up automatically), once the activity of the CAN bus is detected, the hardware will automatically clear the CAN_MSTS.SLPRQ bit to wake up CAN.
- When the CAN_MCTRL.AWKUM bit is clear(enable software wake up), and wake-up interrupt occurred ,then the software must clear the CAN_MCTRL.SLPRQ bit to exit the sleep state.

If the wake-up interrupt (set the CAN_INTE.WKUITE bit) is enabled, the wake-up interrupt will be generated once the CAN bus activity is detected, regardless of whether the hardware is enabled to automatically wake up CAN.

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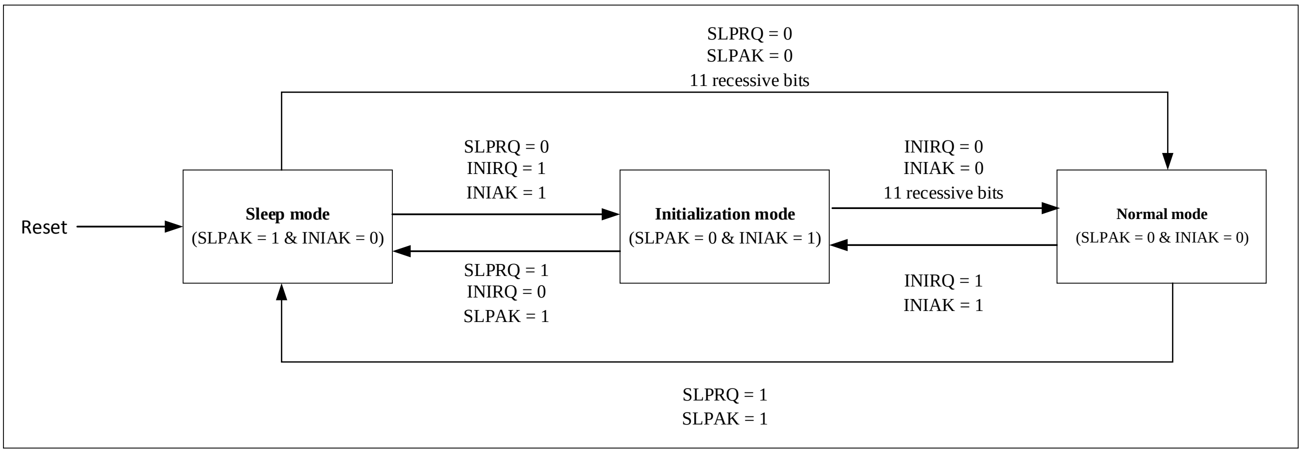
The CAN must be synchronized with the CAN bus before entering Normal mode Wait until the CAN_MSTS.SLPAK bit cleared to confirm the sleep mode has exited.Please refer to Figure 27-2.

Figure 27-2 CAN working mode



Notes: the state that the hardware sets the CAN_MSTS.INIAK or CAN_MSTS.SLPAK bit in response to a sleep or initialization request.

27.3.3 Send mailbox

Applications can send messages through three sending mailboxes. The order of sending three mailbox messages is determined by the sending scheduler according to the priority of the messages, and the priority can be determined by the identifier of the messages or by the order of sending requests.

27.3.4 Receiving filter

CAN has 14 configurable identifier filter groups. After the application configures the identifier filter group, the receiving mailbox will automatically receive the required messages and discard other messages.

27.3.5 Receive FIFO

CAN has two receiving FIFOs, each of which can store three complete messages. No application program is needed to manage it, and it is managed by hardware.

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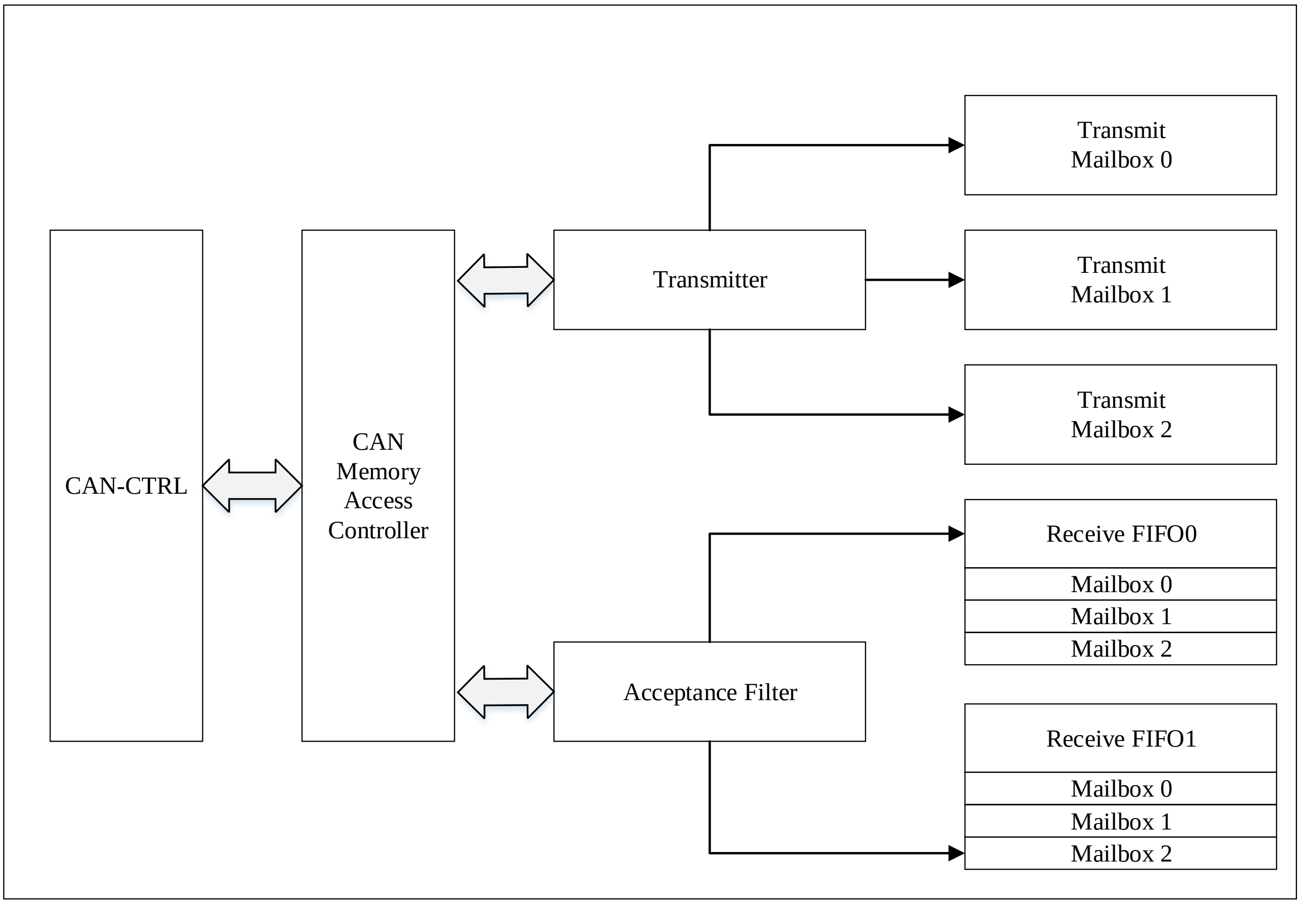
Figure 27-3 Single CAN block diagram



27.3.6 CAN Test mode

In the initialization mode, a test mode must be selected by combining the CAN_BTIM.SLM bit and CAN_BTIM.LBM bit. After selecting a test mode, the software needs to clear the CAN_MCTRL.INIRQ bit to exit the initialization mode and enter the test mode.

27.3.6.1 Loopback mode

Loopback mode can be used for self-test. In loopback mode, CAN saves the sent message in the receiving mailbox as received message (if it can be filtered by reception). In loopback mode, CAN internally feeds back the Tx output to the Rx input, completely ignoring the actual state of the CANRX pin. The message sent can be detected on the CANTX pin. In order to avoid external influence, the CAN kernel ignores the acknowledgement error(at the moment of acknowledgement bit of data/remote frame, it does not detect whether there is an dominant bit). To enter loopback mode, the CAN_BTIM.SLM bit should be cleared and the CAN_BTIM.LBM bit should be set.

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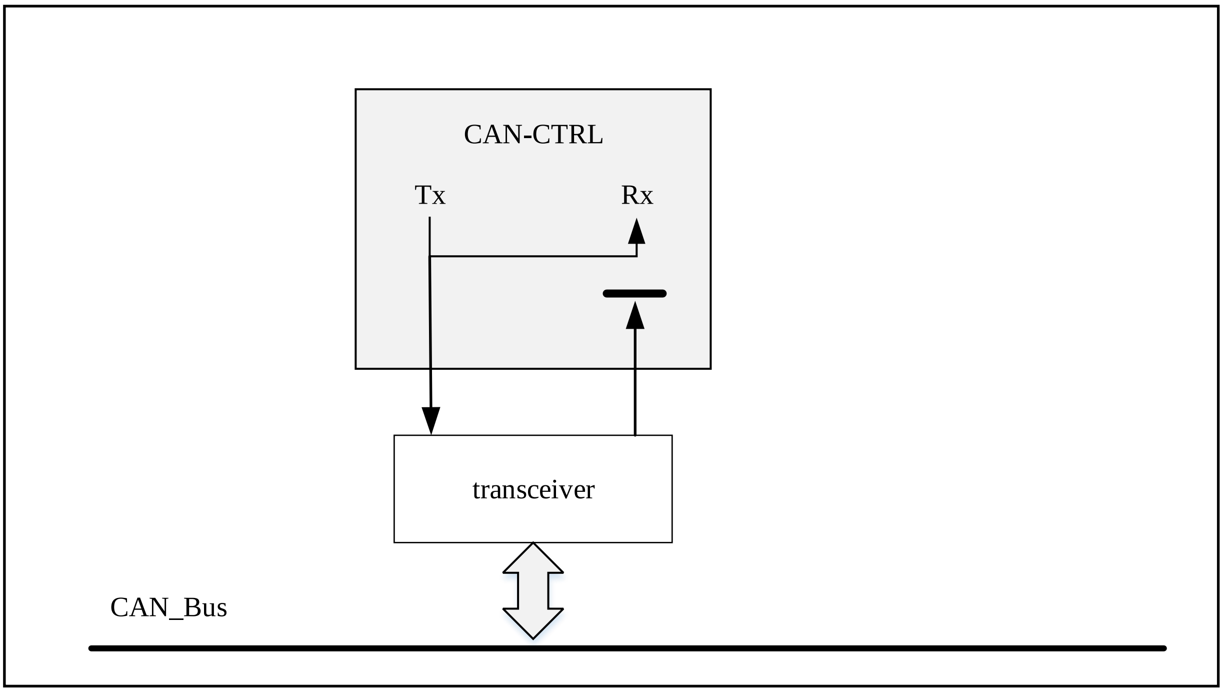
Figure 27-4 Loopback mode



27.3.6.2 Silent mode

In silent mode , CAN can normally receive data frames and remote frames, but can only send recessive bits, and can't really send messages. If CAN needs to send overload flag, active error flag or ACK bit(these are dominant bits), such dominant bits are internally connected back so as to be detected by the CAN core. At the same time, the CAN bus will not be affected and still remain in the recessive bit state. Therefore, the silent mode is usually used to analyze the activity of the CAN bus, without affecting the bus because dominant bits is not actually sent to the bus.

To enter silent mode, the CAN_BTIM.SLM bit should be set and the CAN_BTIM.LBM bit should be cleared.

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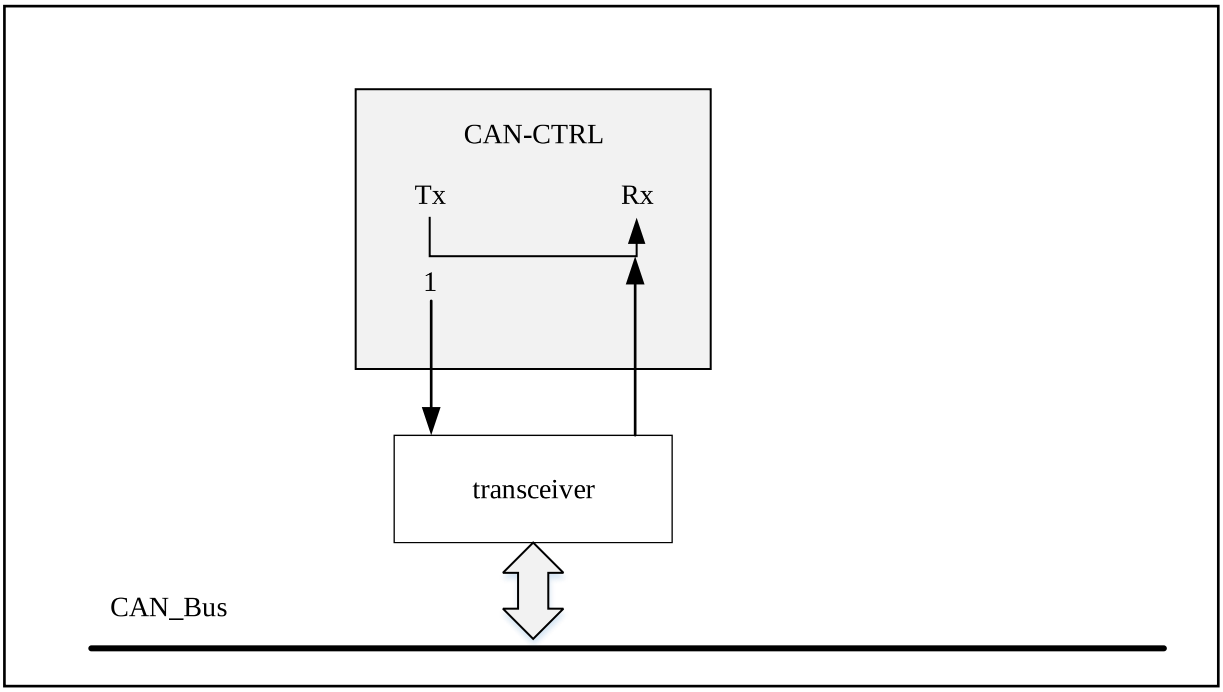
Figure 27-5 Silent mode

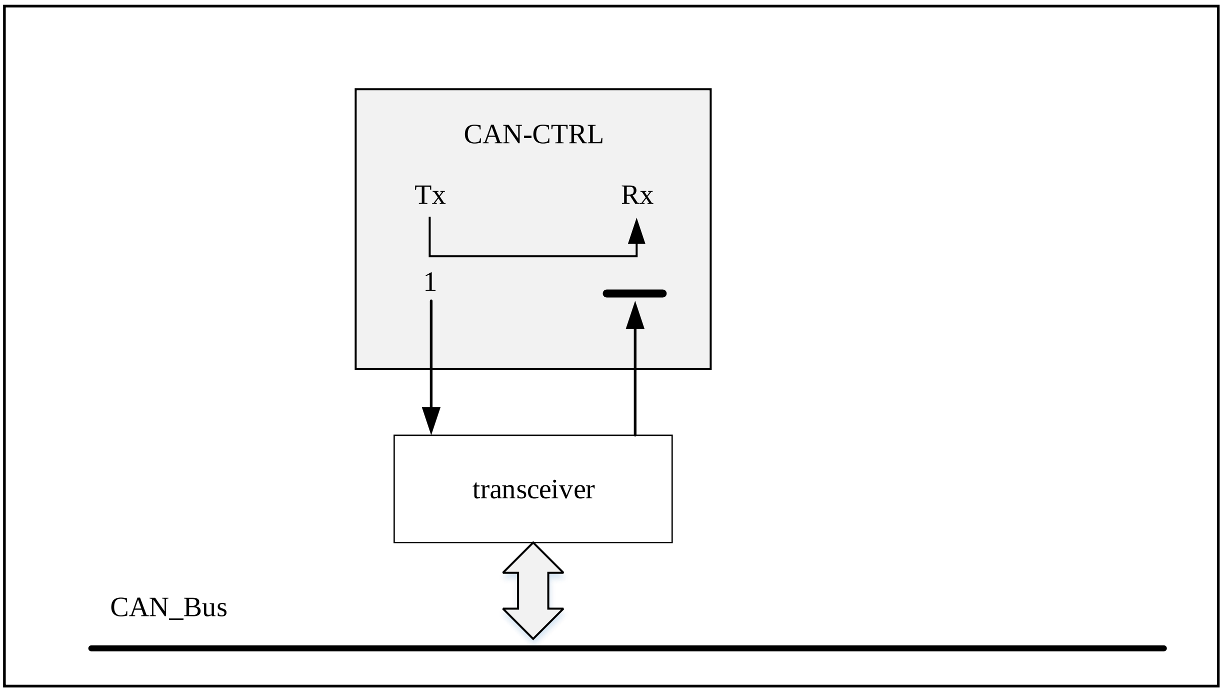


27.3.6.3 Loopback silence mode

In loopback silent mode, the CANRX pin is disconnected from the CAN bus, while the CANTX pin is driven to the recessive bit state. It can be used for "Run-time self diagnose" just like CAN can be tested in loop-back mode, but not affect the whole CAN system connected by CANTX and CANRX.

To enter loopback silence mode, both the CAN_BTIM.SLM bit and the CAN_BTIM.LBM bit should be set.

Figure 27-6 Loopback silent mode



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27.3.7 CAN Debugging mode

CAN can continue to work normally or stop working according to the state of the following configuration bits:

- DBG_CTRL.CAN_STOP bit of CAN in the debug support(DBG) module.See paragraph 29.3.2 Section: Peripheral debugging support.
- CAN_MCTRL.DBGF bit see paragraph 27.7.3.1 Section: CAN_MCTRL.

When the microcontroller is in debug mode, Cortex-M4F core is in a suspended state.

27.4 CAN function description

27.4.1 Send processing

The process of sending messages is as follows:

- The application program selects an **empty** sending mailbox;
- Writes the identifier, data length and data to be sent in the sending mailbox register;
- Set the CAN_TMIx.TXRQ bit to request transmission(after CAN_TMIx.TXRQ is set the mailbox is no longer an empty mailbox and the software has no permission to write to the mailbox register);
- The mailbox enter the **pending** state and wait to be the highest priority, see 27.4.1.1 Send priority;
- Changing to the **Ready** sending status once the mailbox becomes the highest priority mailbox;
- The messages in the **Ready** state mailbox is sent as soon as the CAN bus enters the idle state, then enter the sending state.
- Become an **empty** mailbox when the message in the mailbox is successfully sent;
- Hardware set the RQCPM and TXOKM bits of the corresponding mailbox in CAN_TSTS register to indicate a successful transmission.

However, if the transmission fails, the CAN_TSTS.ALSTM bit will be set to indicate that the failure is caused by arbitration or the CAN_TSTS.TERRM bit will be set to indicates that it is caused by the transmission error (for specific errors, please check the CAN_ESTS.LEC[2:0] error code bits of the error status).

27.4.1.1 Send priority

Determined by the order of sending requests.

Set the CAN_MCTRL.TXFP bit, and the sending mailbox can be configured as a sending FIFO. At this time, the priority of sending is determined by the order of sending requests. This mode is useful for segmented transmission.

Determined by the identifier.

According to CAN protocol, the message with the lowest identifier has the highest priority. If the values of identifiers are equal, the message with small mailbox number is sent first. When more than one sending mailbox is registered, the sending order is determined by the identifier of the message in the mailbox.

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27.4.1.2 Cancel sending

Set the CAN_TSTS.ABRQM bit can abort sending the request. If the mailbox is ready or pending, the sending request will be aborted immediately. If the mailbox is in the transmitting state, the request to abort may lead to two kinds of results:

- if the message in the mailbox fails to be sent, the mailbox becomes ready state, then the sending request is aborted, the mailbox becomes an empty mailbox and the CAN_TSTS.TXOKM bit is cleared;
- if the message in the mailbox is successfully sent, the mailbox becomes an empty mailbox, and the CAN_TSTS.TXOKM bit will be set by hardware.

Therefore, when the sending mailbox is in the sending state, regardless of the sending result, the mailbox will become an empty mailbox after the sending operation is finished.

27.4.2 Time triggered communication mode

The internal timer of CAN is activated in time triggered communication mode. It is incremented at each CAN bit time (see 27.4.7 Section). CAN samples the value of the internal timer at the sampling point position of the received and sent frame start bits, and the sampled value is the time stamp of the sending and receiving mailboxes. Timestamps generate form the internal timer will be stored in the CAN_RMDTx/CAN_TMDTx registers respectively.

27.4.3 Non-automatic retransmission mode

To enable non-automatic retransmission mode the CAN_MCTRL.NART bit should be set. This mode corresponds to the function of time-triggered communication option in CAN standard.In non-automatic retransmission mode , the sending operation will only be executed once. If the sending operation fails, whether due to arbitration loss or error, the hardware will not automatically send the message again.At the end of a transmission operation, the hardware judge that the transmission request has been completed, and the hardware sets the CAN_TSTS.RQCPM bit. At the same time, the transmission result can query the CAN_TSTS.TXOKM, CAN_TSTS.ALSTM and CAN_TSTS.TERRM bits.

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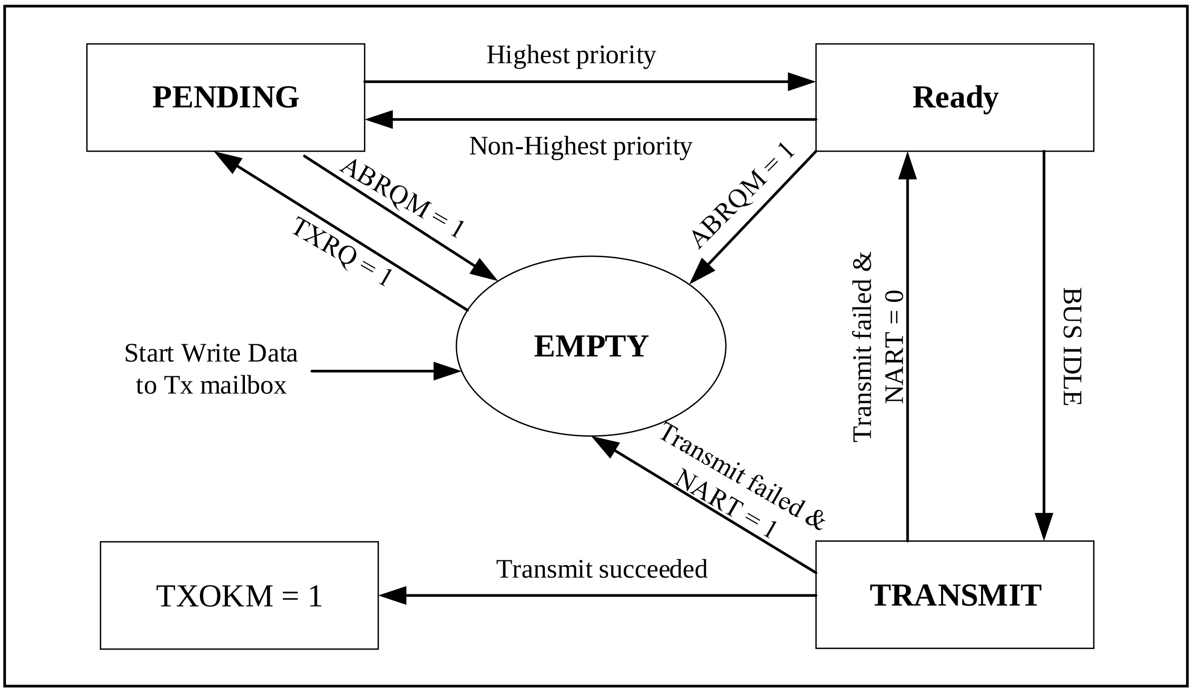
Figure 27-7 Send mailbox status



27.4.4 Receiving management

FIFOs with 3 levels depth are used to store received messages. When the application reads the FIFO output mailbox, it reads the first received message in the FIFO. FIFO is completely managed by hardware, which can simplify the application program, ensure the consistency of data and reduce the processing time of CPU.

27.4.4.1 Valid message

According to CAN protocol, when the message is correctly received (no errors are sent up to the last bit of the EOF field) and passes the identifier filtering, then the message is token as a valid message. Please refer to 27.4.5 Section: identifier filtering.

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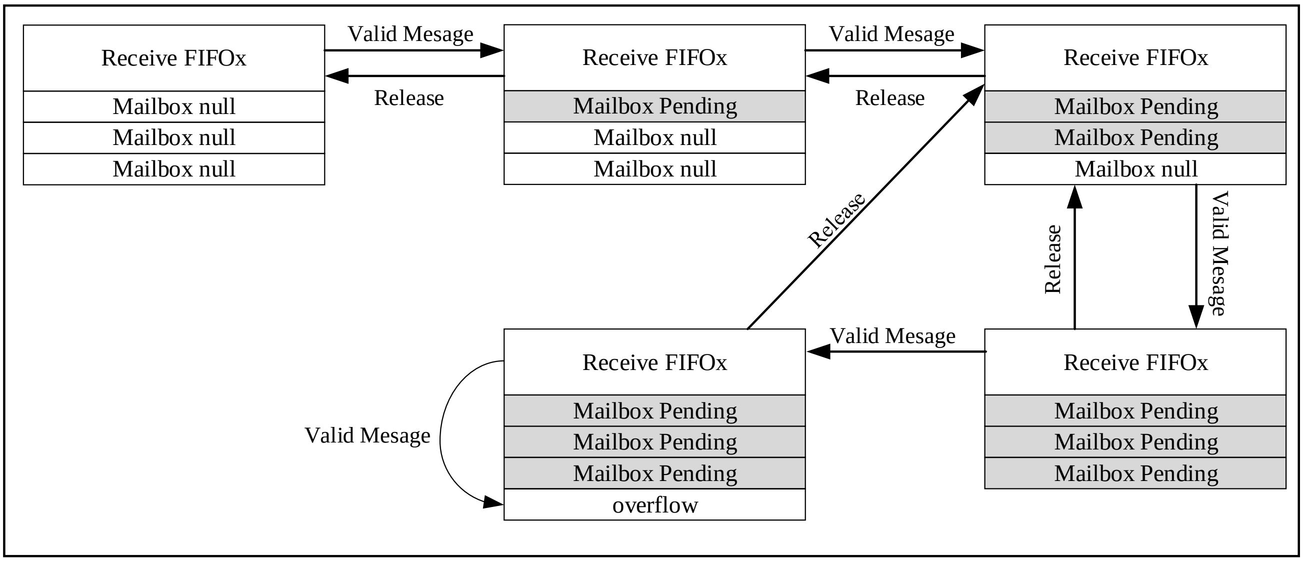
Figure 27-8 Receive FIFO status



27.4.4.2 FIFO receive

A FIFO includes mailboxes with three levels of depth, and the initial state is empty. After receiving the first valid message, one of the mailboxes will be suspended, and the hardware will set the CAN_RFF.FFMP[1:0] bits to 1 to indicate the receipt of a valid message. A valid message is received again before the mailbox is released. At this time, two mailboxes will be suspended at the same time, and the hardware will set the CAN_RFF.FFMP[1:0] bits to 2 to indicate that two valid messages are pending. As above, the third valid message will suspend all three mailboxes and set the CAN_RFF.FFMP[1:0] bits to 3.

When the three-level mailboxes of the FIFO are all suspended, receiving a valid message again will cause the mailbox to overflow and lose a message, and the hardware will set the CAN_RFF.FFOVR bit to 1 to indicate the occurrence of the event. The rules for lost messages depend on the configuration of the FIFO. If the FIFO lock function is disabled (clear the CAN_MCTRL.RFLM bit), then the last message received in the FIFO will be overwritten by the new message. In this way, the latest received message will not be discarded;If the FIFO lock function is enabled (set the CAN_MCTRL.RFLM bit), then the newly received messages will be discarded, and the software can read the first three messages in the FIFO.

27.4.4.3 FIFO release

The message stored in the FIFO will be read through the corresponding receive mailbox. The software reads the mailbox message and releases the mailbox by setting the CAN_RFR.RFOM bit to 1 , and he CAN_RFF.FFMP[1:0] bit is decremented by 1 until it is 0.

27.4.4.4 Receive related interrupts

The hardware will update the CAN_RFF.FFMP[1:0] bits when a message is stored in the receiving FIFO. If the FIFO message pending interrupt is currently enabled (the CAN_INTE.FMPITE bit is set), then the FIFO message pending interrupt request will be generated.

When the third message is stored ,the FIFO becomes full, then the CAN_RFF.FFULL bit will be set, and if the FIFO full interrupt is currently enabled (the CAN_INTE.FFITE bit is set), a FIFO full interrupt request will be generated.

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When the FIFO overrun, the FFOVR bit will be set . If the FIFO overrun interrupt is currently enabled (the CAN_INTE.FOVITE bit is set), a FIFO overrun interrupt request will be generated.

27.4.5 Identifier filtering

In the CAN network, when basic CAN is in the transmitter state, it broadcasts a message to each node by sending a message to the bus; when basic CAN is in the receiver state, it determines whether the node needs the message according to the identifier of the message after receiving the message. If message is vaild, CAN core copies the message to SRAM(CAN's own SRAM); If it is not needed, the message will be discarded. This process does not require software intervention. Compared with software filtering, hardware filtering reduces the CPU usage. CAN controller provides 14 configurable filter banks (0~13) with variable bit width for application programs to meet this demand. These filter banks are used to receive only those messages needed by software. Each filter bank x contains two 32-bit registers, namely CAN_FxR0 and CAN_FxR1.

27.4.5.1 Setting of filter bit width and mode

Each filter in a filter bank is numbered (filter number, from 0 to a certain maximum value) depending on the mode and bit width setting of the filter bank. See the figure below for the filter configuration.The filter group can be configured through the corresponding CAN_FMC register. Filter banks that are not used by the application should be kept disabled. Before configuring a filter bank, it must be set to the disabled state by clearing the CAN_FA1.FAC bit.

By setting the corresponding CAN_FS1.FSCx bit you can configure the bit width of a filter bank, see Figure 27-9.

By means of the CAN_FM1.FBx bit, the corresponding mask/identifier register can be configured to be the **identifier list** or **identifier mask** mode.The filter group should be set to work in the mask mode in order to filter out a group of identifiers. And the filter group should be set to work in identifier list mode in order to filter out an identifier.

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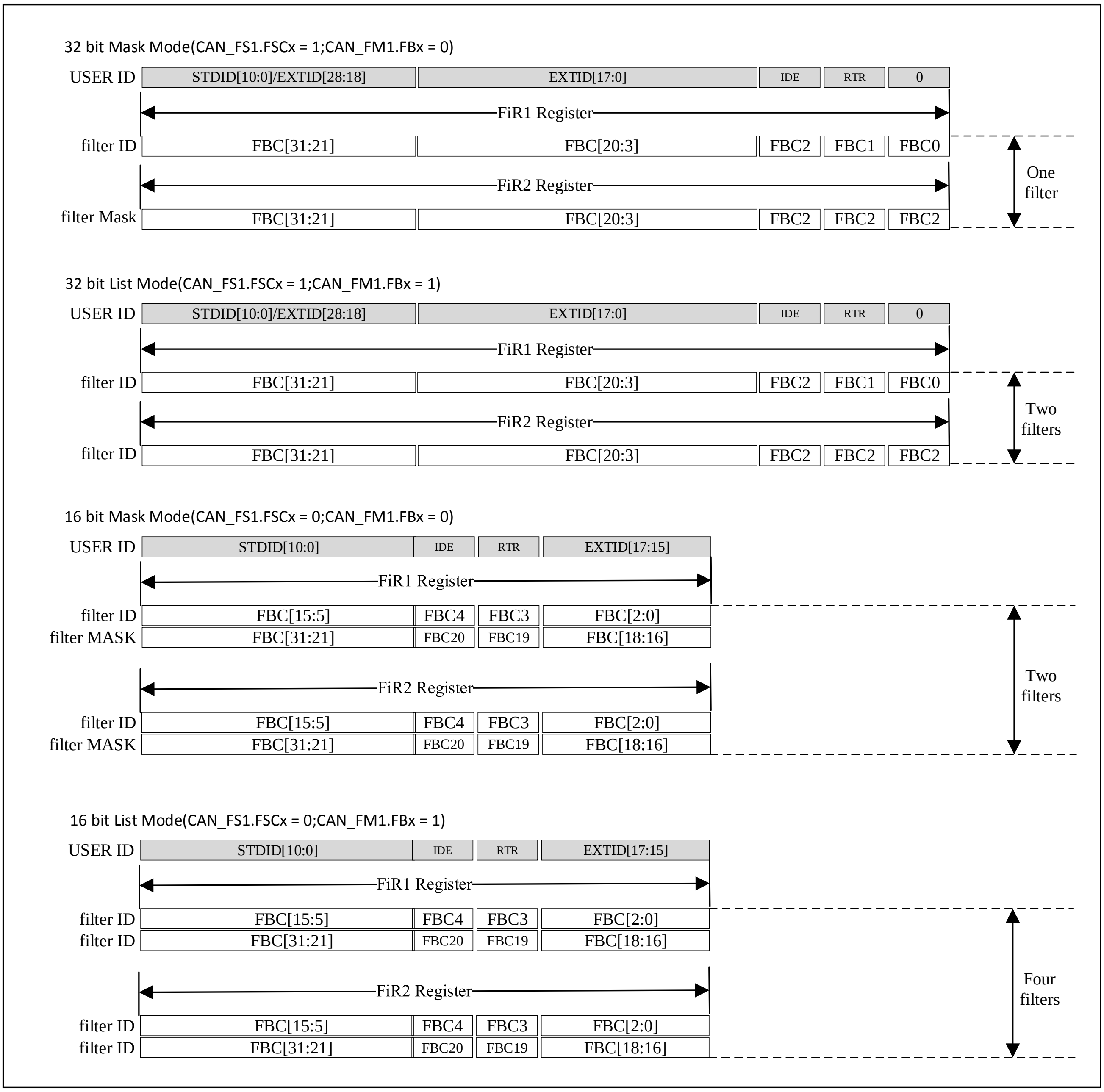
Figure 27-9 Filter bit width setting-register organization



27.4.5.2 Variable bit width

The bit width of each filter bank can be independently configured. Each filter bank can be configured to be one 32-bit filter: including STDID[10:0], EXTID[17:0], IDE and RTRQ bits; or two 16-bit filters,:including STDID[10:0], IDE, RTRQ and EXTID[17:15] bits, see Figure 27-9. In addition, the filter can be configured in two different modes, namely, the mask mode and the identifier list mode.

Mask mode

The filter ID is used to store the identifier format, and the filter MASK is used to indicate which bits must be checked and which bits can be ignored.

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Identifier list mode

The filter ID is used to store the identifier format. At this time, there is no mask for comparison, and the mask bit can be used to store one more filter ID. However, at this time, the identifier of the message needs to be exactly the same as the filter ID format, otherwise it will fail to pass the filter.

27.4.5.3 Filter matching sequence number

After CAN core received an valid message it will matching the message ID with filters one by one until there is one filter pass or all filters failed. If this message failed to pass any enabled filter then it will be discarded. Otherwise when CAN core finds the first filter that the ID can pass, it pack filter index with the CAN message and stores inside receive FIFO in SRAM according to filter setting (CAN_FFA1 decides store in which FIFO). User can find filter index in FMI [7:0] bits of CAN_RMDTx register. This filter matching index can help to identify which types of message it is in this receive FIFO.

The filter matching sequence number can be used two ways. The first one is comparing the filter matching sequence number with a series of expected values. The another is using the filter matching sequence number as an index to access the target address. When numbering filters, whether the filter group is active or not is not considered. In addition, each FIFO numbers its associated filter. Please refer to the example below.

For the filter in mask mode, the software only needs to compare the mask bits that are needed (bits that must be matched). For the filter in identifier list mode (non-screening filter), the software does not need to directly compare with the identifier.

Table 27-1 Examples of filter numbers

Point to FIFOx	Filter group	Filter mode	FIFO0 filter number
FIFO	0	32 bit mask mode	0
	2	16 bit mask mode	1/2
	5	32 bit list mode	3/4
	7	16 bit list mode	5/6/7/8
	9	32 bit list mode	9/10
	11	16 bit list mode	11/12/13/14
	13	32 bit mask mode	15
Point to FIFOx	Filter group	Filter mode	FIFO1 filter number
FIFO1	1	32 bit list mode	0/1
	3	16 bit list mode	2/3/4/5

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	4	32 bit mask mode	6
	6	16 bit mask mode	7/8
	8	32 bit mask mode	9
	10	16 bit mask mode	10/11
	12	32 bit list mode	12/13

27.4.5.4 Filter priority rule

According to different configurations of filters, it is possible that a message identifier can be filtered by multiple filters; In this case, the filter matching serial number stored in the receiving mailbox is first determined according to bit width,32-bit-wide filters have higher priority than 16-bit-wide filters. For filters with the same bit width, then the identifier list mode takes precedence over the mask mode. If filters have the same bit width and mode, the priority is determined by the filter group number, and the filter group with lower number has the higher priority.Within a filter group,the lower the filter number,the higher the priority.

Figure 27-10 Examples of filter mechanisms

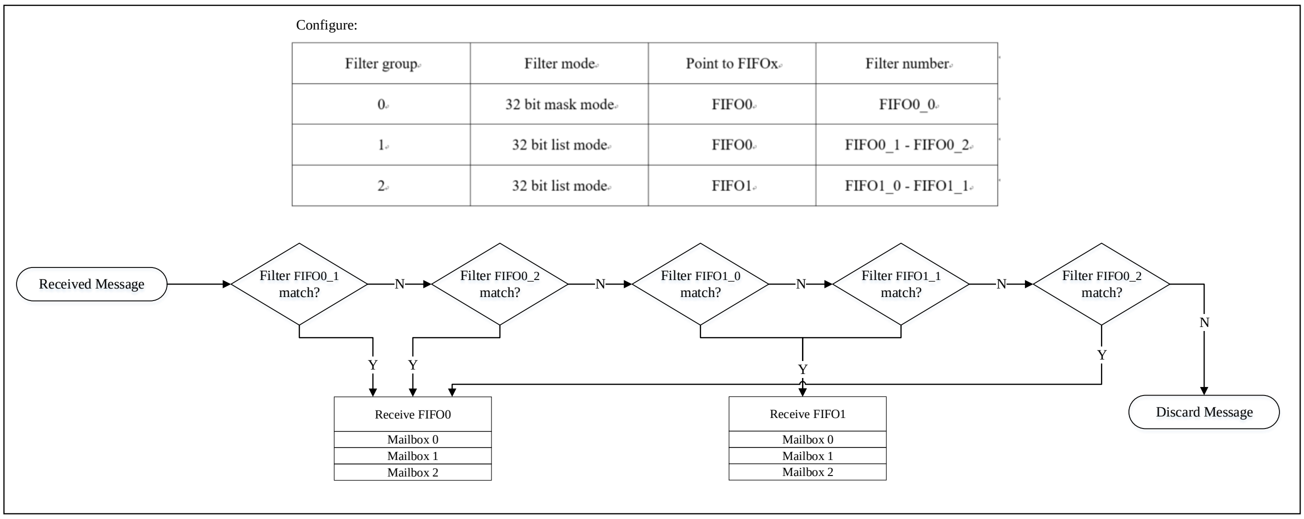

Figure 27-10 illustrates the filter rules of CAN. When receiving a message, its identifier is first compared with the filter configured in identifier list mode. If there is a match, the message will be stored in the associated FIFO, and the serial number of the matched filter will be stored in the filter matching serial number.

If there is no match, the message identifier is then compared with the filter configured in the mask mode. And the hardware will automatically discard the message without software intervention if the message identifier does not match any identifier in the filter.

27.4.6 Message storage

A mailbox contains all information related to a message: identifier, data, control, status and time stamp information. The mailbox is the interface between software and hardware to transfer messages.

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27.4.6.1 Send mailbox

Message should be written into an empty sending mailbox by software before enable the sending request. You can query the sending status through the CAN_TSTS register.

Table 27-2 Send mailbox register list

Offset from the base address of the sending mailbox	Register name
0	CAN_TMIx
4	CAN_TMDTx
8	CAN_TMDLx
12	CAN_TMDHx

27.4.6.2 Receiving mailbox (FIFO)

CAN_RMDTx.FMI[7:0] field can store the filter matching serial number and CAN_RMDTx.MTIM[15:0] field can store the 16-bit timestamp.The software can access the output mailbox of the receiving FIFO to read the received message. Once the software has processed the message, such as reading it out, the software should set the CAN_RFFx.RFFOM bit to release the corresponding receive FIFO, so as to reserve storage space for later messages.

Table 27-3 Receive mailbox register list

Offset from the base address of the receiving mailbox	Register name
0	CAN_RMIx
4	CAN_RMDTx
8	CAN_RMDLx
12	CAN_RMDHx

27.4.7 Bit time characteristic

The bit time characteristic logic monitors the serial CAN bus by sampling, and adjusts its sampling point by synchronizing with the edge of the frame start bit and resynchronizing with the following edge. To avoid programming errors in software, setting the bit time characteristic register (CAN_BTIM) can only be done when CAN is initialized.

Its operation can be simply understood as dividing each bit time into three segments: Synchronization segment (SYNC_SEG), Time period 1(BS1) and Time period 2(BS2).

Usually, it is expected that the change of bits will occur in SYNC_SEG. Its value is fixed to 1 time unit (1 $\times t_{CAN}$).

BS1 defines the position of the sampling point. It includes PROP_SEG and PHASE_SEG1 in CAN standard. Its value can be programmed into 1 to 16 time units, but in order to compensate the forward drift of phase caused by the frequency difference of different nodes in the network, it can also be automatically extended.

In BS2, it defines the location of the sending point. It stands for PHASE_SEG2 in CAN standard. Its value can be programmed into 1 to 8 time units, but it can also be automatically shortened to compensate for the negative drift of phase.

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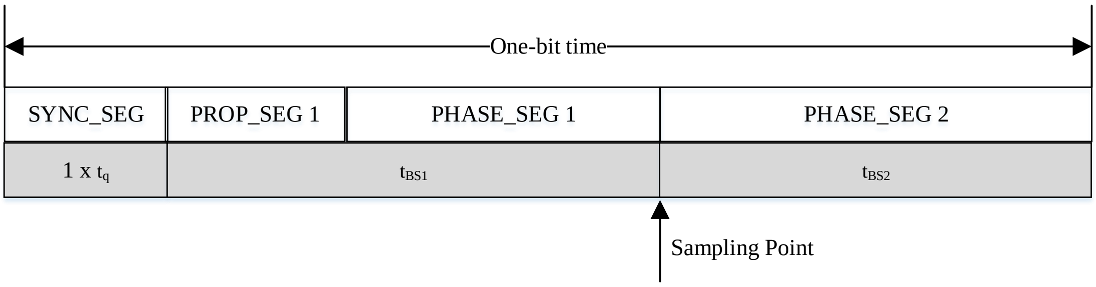
If a valid transition is detected in BS1 but not in SYNC_SEG, then the time of BS1 is extended by at most RSJW to delay the sampling point. On the contrary, if a valid transition is detected in BS2 but not in SYNC_SEG, then the time of BS2 is shortened at most RSJW to advance the sampling point.

In the above description, RSJW(the resynchronization hop width) defines the upper limit of how many time units can be extended or shortened in each bit. Its value can be programmed into 1 to 4 time units. The effective transition is defined as the first transition from the dominant bit to the recessive bit when CAN itself does not send the recessive bit.

Note: 1. The time characteristics and resynchronization mechanism of CAN bits are detailed in the ISO11898 standard.

2. In order to improve the CAN bit time accuracy, it is not recommended to use HSI as the clock source.

Figure 27-11 Bit sequence



Notes：

t_{PCLK} = *time period of the APB1 clock,*

$t_q = (CAN\_BTIM.BRTP[9:0] + 1) \times t_{PCLK}$,

$t_{BS1} = t_q \times (CAN\_BTIM.TBS1[3:0] + 1)$,

$t_{BS2} = t_q \times (CAN\_BTIM.TBS2[2:0] + 1)$,

$\text{One-bit time} = 1 \times t_q + t_{BS1} + t_{BS2}$

$$BaudRate = \frac{1}{\text{One-bit time}}$$

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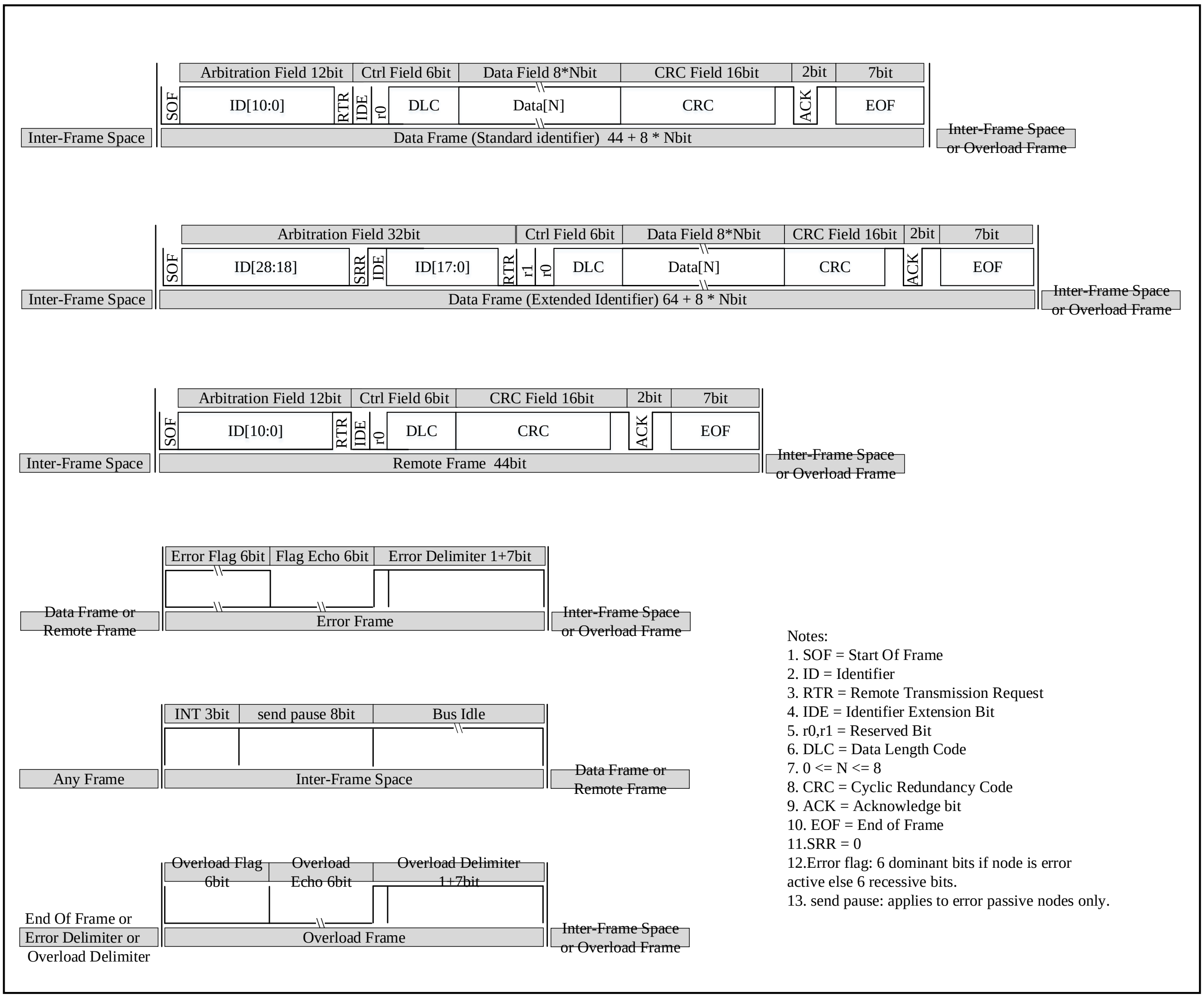
Figure 27-12 Various CAN frames



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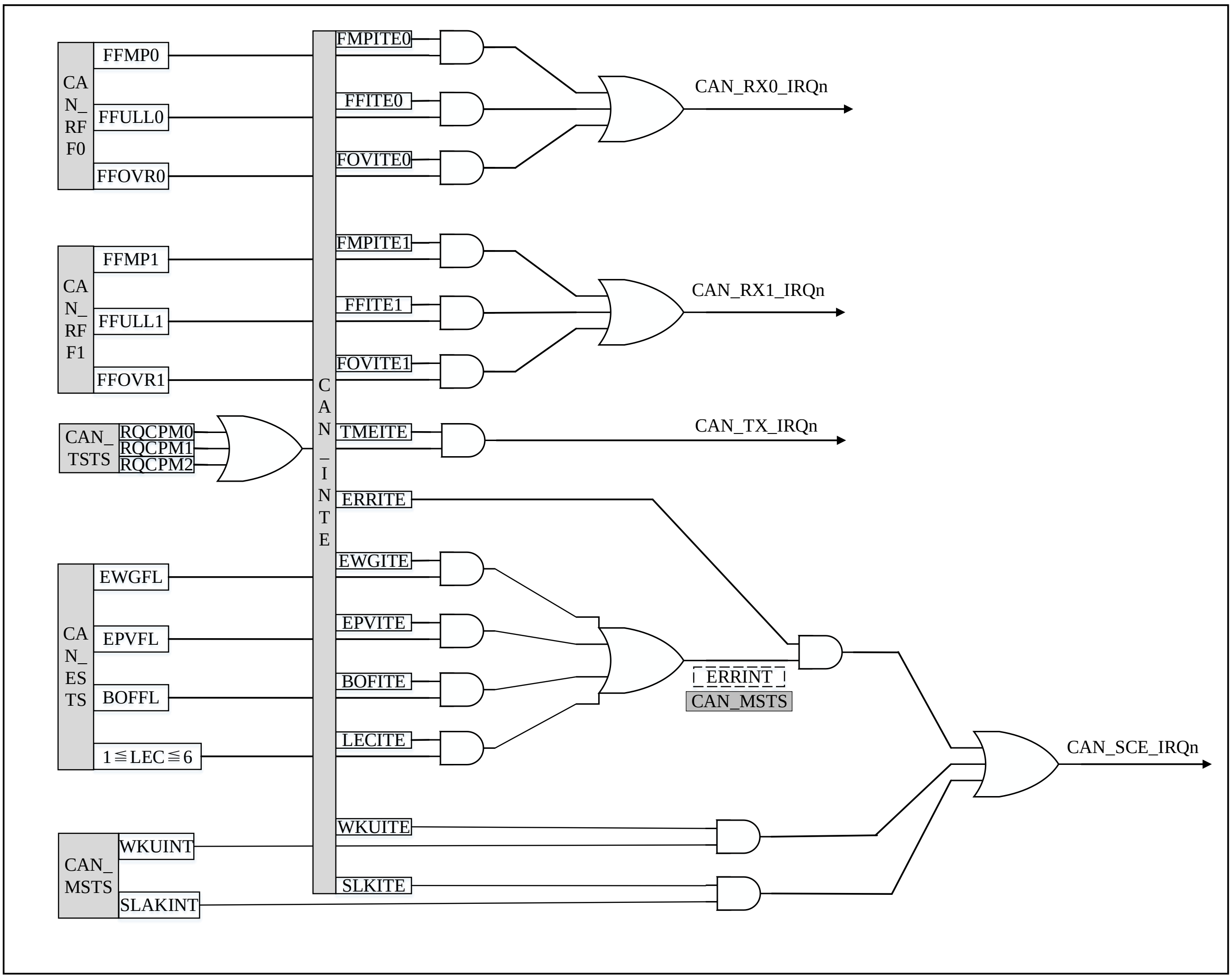
27.5 CAN interrupt

Figure 27-13 Event flag and interrupt generation



CAN has four interrupt vectors. By setting the CAN interrupt enable register (CAN_INTE), you can individually enable or disable each interrupt source. The following are the events that can generate each interrupt.

- FIFO0 interrupt(CAN_RX0_IRQn):

  FIFO0 receives a new message, and the CAN_RFF0.FFMP0 bit is not '00' ;

  When FIFO0 becomes full, and the CAN_ RFF0.FFULL0 bit is set;

  When FIFO0 overruns, and the CAN_ RFF0.FFOVR0 bit is set.

- FIFO1 interrupt(CAN_RX1_IRQn):

  FIFO1 receive a new message, and the CAN_RFF1.FFMP1 bit is not '00'.

  When FIFO1 becomes full, and the CAN_RFF1.FFULL1 bit is set.

  When FIFO1 overruns, and the CAN_ RFF1.FFOVR1 bit is set.

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- Send interrupts(CAN_TX_IRQn):

  Send mailbox x becomes empty, and the corresponding CAN_TSTS.RQCPMx bit is set(x=1/2/3).

- **Error and status change interrupt**(CAN_SCE_IRQn):

  CAN enters sleep mode;

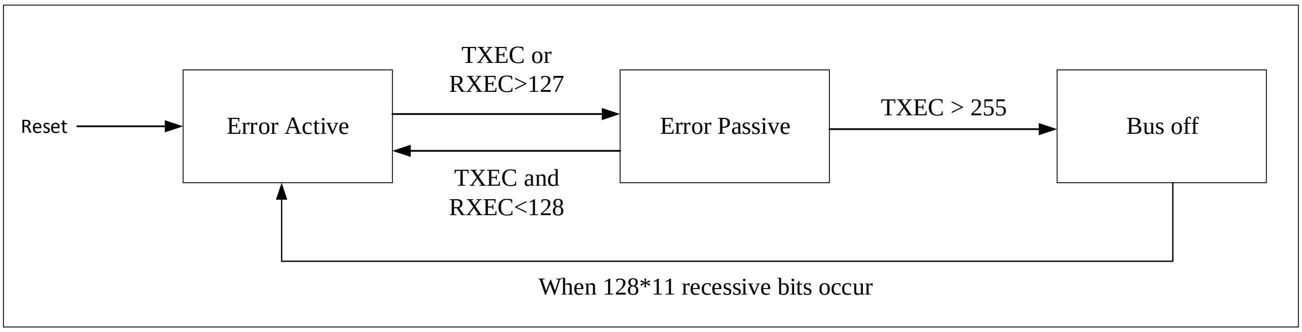
  Wake-up condition, the start of frame bit (SOF) is monitored on the CAN receiving pin.

  Error condition, please refer to the CAN error status register (CAN_ESTS) for details of the error.

27.5.1 Error management

As described in CAN protocol, the error management is completely realized by hardware through sending error counter (CAN_ESTS.TXEC field) and receiving error counter (CAN_ESTS.RXEC field). The counter value will increase or decrease according to the error situation. Please refer to CAN standard if you want to know more detailed information about CAN_ESTS.TXEC and CAN_ESTS.RXEC management.

Figure 27-14 CAN error state diagram



Software can read out the value of the sending/receiving error counter to judge the stability of CAN network, and CAN_ESTS.LEC[2:0] bits can be read to get the detailed information of the current error status. What's more, by setting the CAN_INTE register (such as CAN_INTE. LECITE bit), the software can flexibly control the generation of interrupts when an error is detected.

27.5.2 Bus-Off recovery

When TXEC is greater than 255, the CAN_ESTS.BOFFL bit is set indicating that CAN goes bus-off. at this time, CAN can't receive and send messages.

In normal mode, according to the CAN_MCTRL.ABOM bit, CAN can automatically or at the request of software, recover from bus-off state, and change to error active state. If the CAN_MCTRL.ABOM bit is set, the recovery process will be started automatically after it has entered bus-off state. Otherwise, the recovery process will be started after software must request CAN to enter and then exit initialization mode. In both cases, CAN must wait for a recovery process described in CAN standard, that is 128*11 consecutive recessive bits are detected on CAN RX pin.

In initialization mode, CAN will not monitor the status of CAN RX pin, so the recovery process cannot be completed.

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27.6 CAN Configuration Flow

This chapter will introduce common configuration procedure of CAN while other details like functions of each mode and register bits are revealed in other part of this manual. CAN configuration flow can divided into serval phases. Some of the configurations can be changed anytime as long as prior requirements are satisfyied (e.g., filter value).

- **Preparation Stage:**

1. Configure RCC to enable CAN clock
2. Configure RCC to enable AFIO and GPIO clock
3. Write into GPIO registers to map CAN TX and CAN RX signals to desired GPIO pins.

- **Basic Configuration Stage:**

1. After reset CAN device starts with Sleep mode.
2. Exit Sleep mode by clearing CAN_MCTRL.SLPRQ bit.
3. Enter Initialization mode by setting CAN_MCTRL.INIRQ bit.
4. Wait for CAN_MSTS.INIAK bit become 1 (enter Initilization mode).
5. Configure bit timing for CAN by writing value to CAN_BTIM.BSJW, CAN_BTIM.TBS2, CAN_BTIM.TBS1 and CAN_BTIM.BRTP bits. Baud rate of CAN bus is defined by the formula below:

$$BaudRate = \frac{1}{\left(1 + (TBS1 + 1) + (TBS2 + 1)\right) * (BRTP * t_{pclk})}$$

6. Configure work mode options for CAN by writing to CAN_BTIM.SLM (silent) or CAN_BTIM.LBM in register.
7. Configure CAN behavior(TTCM,ABOM,AWKUM,NART,RFLM,TXFP) through CAN_MCTRL. Most of the configuration in this register can be changed on the fly but its advised not to do so. Otherwise during few cycles, CAN behavior will become unpredictable.
8. Exit Initialization mode by clearing CAN_MCTRL.INIRQ bit.
9. Wait for CAN_MSTS.INIAK bit become 0 (exit Initilization mode).
10. User can use filters to filter the messages they want to receive. To configure filter, user needs to write ‘1’ to CAN_FMC.FINITM bit to request the filters to enter initialization mode. When filter is in initialization mode, CAN stops reception.
11. Configure each filter for working mode (CAN_FM1), filter scale (CAN_FS1) and filter assignment (CAN_FFA1). User can also change filter value (CAN_FiRx) during this time. After completing filter configuration, clear CAN_FMC.FINITM bit to exit initialization for filters.

- **For transmission:**

1. Enable the necessary transmit related interrupt CAN_INTE.TMEITE bit.
2. Check status bits of each mailbox in CAN_TSTS. If any mailbox with TMEMx (x = 0~2) is ‘1’, user can write the message, which is waiting for transmission, to the corresponding mailbox address. CAN_TMIx.TXRQ(x = 0~2) bit must be written to ‘1’ after this mailbox is programed.

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3. After some time or after waiting for transmit interrupts, come back to check transmit status in CAN_TSTS. Repeat step 2~3 for new message transmission.

- **For Reception:**

1. User can also change a filter value (**CAN_FiRx**) when the corresponding filter is deactivated. To deactivate certain filter, user needs to write '0' to the corresponding bit in **CAN_FA1** register.
2. Configure reception related interrupts in CAN_INTE register.
3. Once CAN has received message and stored them inside reception FIFO, user needs to read the corresponding FIFO on time and release reception mailbox by writing '1' to RFFOMx in register CAN_RFFx (x = 0,1).

27.7 CAN Registers

These peripheral registers must be operated as words (32 bits).

27.7.1 Register Description

27.7.1.1 Register access protection

When a CAN node is working normally, incorrect access/modification of some configuration registers may cause hardware errors in the node and temporarily interfere with the entire CAN network. Therefore, modification of the CAN_BTIM register is only allowed when the CAN core is in initialization mode.

Only when the send mailbox status bit CAN_TSTS.TMEM = 1 then the user can modify data to the send mailbox.

27.7.1.2 Control and status registers

By configuring these registers, user can: configure CAN parameters, such as working mode and baud rate; start message sending; handling message reception; interrupt setting; read diagnostic information.

27.7.1.3 Mailbox Register Description

The sending and receiving mailboxes are basically the same except that the receiving mailbox is read-only and contains the CAN_RMDTx.FMI field. The sending mailbox is writable when it is empty.

Notes: *the corresponding CAN_TSTS.TMEM bit is set, which means that the sending mailbox is empty.*

There are 3 sending mailboxes and 2 receiving FIFO. Each receiving FIFO has three mailboxes, and only the first received message in the FIFO can be accessed.

Each mailbox contains 4 registers:

FIFO0 contains CAN_RMI0, CAN_RMDT0, CAN_RMDL0, CAN_RMDH0;

FIFO1 contains CAN_RMI1, CAN_RMDT1, CAN_RMDL1, CAN_RMDH1;

Send mailbox (x) contains CAN_TMIx, CAN_TMDTx, CAN_TMDLx, CAN_TMDHx; x = 0,1,2.

27.7.1.4 Filter Register Description

The value of the filter can only be modified when the corresponding filter group is closed or the CAN_FMC.FINITM bit is set. In addition, only when the whole filter is set to the initialization mode (that is, CAN_FMC.FINITM=1), the

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settings of the filter can be modified, that is, the CAN_FM1,CAN_FS1 and CAN_FFA1 registers can be modified.

27.7.2 CAN register overview

Table 27-4 CAN register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	CAN_MCTRL	Reserved															DBGF	MRST	Reserved							TTCM	ABOM	AWKUM	NART	RFLM	TXFP	SLPRQ	INIRQ
	Reset Value																1	0								0	0	0	0	0	0	1	0
004h	CAN_MSTS	Reserved																				RXS	LSMP	RXMD	TXMD	Reserved			SLAKINT	WKUINT	ERRINT	SLPAK	INIAK
	Reset Value																					1	1	0	0				0	0	0	1	0
008h	CAN_TSTS	LOWM[2:0]			TMEM[2:0]			CODE[1:0]		ABRQM2	Reserved			TERRM2	ALSTM2	TXOKM2	RQCPM2	ABRQM1	Reserved			TERRM1	ALSTM1	TXOKM1	RQCPM1	ABRQM0	Reserved			TERRM0	ALSTM0	TXOKM0	RQCPM0
	Reset Value	0	0	0	1	1	1	0	0	0				0	0	0	0	0				0	0	0	0	0				0	0	0	0
00Ch	CAN_RFF0	Reserved																										RFFOM0	FFOVR0	FFULL0	Reserved	FFMP0[1:0]	
	Reset Value																											0	0	0		0	0
010h	CAN_RFF1	Reserved																										RFFOM1	FFOVR1	FFULL1	Reserved	FFMP1[1:0]	
	Reset Value																											0	0	0		0	0
014h	CAN_INTE	Reserved														SLKITE	WKUITE	ERRITE	Reserved			LECITE	BOFITE	EPVITE	EWGITE	Reserved	FOVITE1	FFITE1	FMPITE1	FOVITE0	FFITE0	FMPITE0	TMEITE
	Reset Value															0	0	0				0	0	0	0		0	0	0	0	0	0	0
018h	CAN_ESTS	RXEC[7:0]								TXEC[7:0]								Reserved									LEC[2:0]			Reserved	BOFFL	EPVFL	EWGFL
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										0	0	0		0	0	0
01Ch	CAN_BTIM	SLM	LBM	Reserved				RSJW[1:0]		Reserved	TBS2[2:0]			TBS1[3:0]				Reserved						BRTP[9:0]									
	Reset Value	0	0					0	1		0	1	0	0	0	1	1							0	0	0	0	0	0	0	0	0	0
020h - 17Fh	Reserved																																
180h	CAN_TMI0	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
184h	CAN_TMDT0	MTIM[15:0]																Reserved							TGT	Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
188h	CAN_TMDL0	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
18Ch	CAN_TMDH0	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
190h	CAN_TMI1	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
194h	CAN_TMDT1	MTIM[15:0]																Reserved							TGT	Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
198h	CAN_TMDL1	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
19Ch	CAN_TMDH1	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1A0h	CAN_TMI2	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
1A4h	CAN_TMDT2	MTIM[15:0]																Reserved							TGT	Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
1A8h	CAN_TMDL2	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1ACh	CAN_TMDH2	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1B0h	CAN_RMI0	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	Reserved
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1B4h	CAN_RMDT0	MTIM[15:0]																FMI[7:0]								Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x	x	x	x
1B8h	CAN_RMDL0	DATA3[7;0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1BCh	CAN_RMDH0	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1C0h	CAN_RMI1	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	Reserved
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1C4h	CAN_RMDT1	MTIM[15:0]																FMI[7:0]								Reserved				DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x	x	x	x

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1C8h	CAN_RMDL1	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1CCh	CAN_RMDH1	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1D0h - 1FFh	Reserved																																
200h	CAN_FMC	Reserved																															FINITM
	Reset Value																																1
204h	CAN_FM1	Reserved																		FB[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
208h	Reserved																																
20Ch	CAN_FS1	Reserved																		FSC[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
210h	Reserved																																
214h	CAN_FFA1	Reserved																		FAF[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
218h	Reserved																																
21Ch	CAN_FA1	Reserved																		FAC[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
220h	Reserved																																
224h - 23Fh	Reserved																																
240h	CAN_F0B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
244h	CAN_F0B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
248h	CAN_F1B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24Ch	CAN_F1B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
. . .	. . .	Reserved																															
2A8h	CAN_F13B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
2ACh	CAN_F13B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

27.7.3 CAN control and status register

Abbreviations used in register descriptions, please refer to 1.1 section.

27.7.3.1 CAN master control register (CAN_MCTRL)

Address offset: 0x00

Reset value: 0x0001 0002

31:17	16
Reserved	DBGF
	rw

15	14:8	7	6	5	4	3	2	1	0
MRST	Reserved	TTCM	ABOM	AWKUM	NART	RFLM	TXFP	SLPRQ	INIRQ
rs		rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Describe
31:17	Reserved	Reserved, the reset value must be maintained.
16	DBGF	Debug freeze 0: During debugging, CAN works as usual. 1: Freeze the reception/transmission of CAN during debugging. The receiving FIFO can still be read, written and controlled normally. ***Notes****: DBG_CTRL.CAN_STOP bit must be set when CAN is frozen, please refer to 27.3.7: Debugging mode.*
15	MRST	CAN software master reset 0: This peripheral works normally; 1: enforce reset CAN, after which CAN enters sleep mode and CAN_RFFx.FFMP bit and CAN_MCTRL register are initialized to their reset values. After that, the hardware automatically clears this bit.
14:8	Reserved	Reserved, the reset value must be maintained.
7	TTCM	Time triggered communication mode 0: disable time triggered communication mode;

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Bit field	Name	Describe
		1: enable time trigger communication mode. ***Notes**: For more information about time-triggered communication mode, please refer to 27.4.2: Time-triggered communication mode.*
6	ABOM	Automatic bus-off management This bit determines the conditions under which the CAN hardware can exit the bus-off state. 0: The process of exiting the bus-off state is that after the software sets the CAN_MCTRL.INIRQ bit and then clears it, once the hardware detects 128 consecutive 11-bit recessive bits, it exits the bus-off state; 1: Once the hardware detects 128 consecutive 11-bit recessive bits, it will automatically exit the bus-off state. ***Notes**: For more information about bus-off status, please refer to 27.5.1: Error management.*
5	AWKUM	Automatic wake up mode This bit determines whether CAN is awakened by hardware or software when it is in sleep mode. 0: The sleep mode is awakened by the software by clearing the CAN_MCTRL.SLPRQ bit; 1: Sleep mode is automatically awakened by hardware by detecting CAN messages. At the same time of wake-up, the hardware automatically clears the CAN_MSTS.SLPRQ and CAN_MSTS.SLPAK bits.
4	NART	No automatic retransmission 0: According to the CAN standard, when the CAN hardware fails to send a message, it will automatically retransmit it until it is successfully sent; 1: CAN message is only sent once, regardless of the sending result (success, error or arbitration loss).
3	RFLM	Receive FIFO locked mode. 0: the FIFO is not locked when receiving overflows, and when the message of the receiving FIFO is not read out, the next received message will overwrite the last message; 1: FIFO is locked when receiving overflow. When the message of receiving FIFO is not read out, the next received message will be discarded.
2	TXFP	Transmit FIFO priority When there are multiple messages waiting to be sent at the same time, this bit determines the sending order of these messages. 0: Priority is determined by the identifier of the message; 1: Priority is determined by the order in which requests are sent.
1	SLPRQ	Sleep mode request The software can request the CAN to enter the sleep mode by setting this bit, and once the current CAN activity (sending or receiving messages) ends, the CAN will enter the sleep mode.

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Bit field	Name	Describe
		Clear by software to make CAN exit sleep mode. When the CAN_MCTRL.AWKUM bit is set and the SOF bit is detected in the CAN Rx signal, the hardware clears this bit. This bit is set after reset, that is, CAN is in sleep mode after reset.
0	INIRQ	Initialization request clear this bit by software can make CAN exit from initialization mode: when CAN leaves Initialization mode and entering normal mode, it needs to detect 11 consecutive recessive bits at the receiving pin, CAN will be synchronized and ready for receiving and sending data. To this end, the hardware correspondingly the CAN_MSTS.INIAK bit is cleared. Setting this bit by software enables CAN to enter initialization mode from normal operation mode: once the current CAN activity (sending or receiving) is over, the hardware sets the CAN_MSTS.INIAK bit and CAN enters initialization mode.

27.7.3.2 CAN master status register (CAN_MSTS)

Address offset: 0x04

Reset value: 0x0000c02

31-16
Reserved

15-12	11	10	9	8	7-5	4	3	2	1	0
Reserved	RXS	LSMP	RXMD	TXMD	Reserved	SLAKINT	WKUINT	ERRINT	SLPAK	INIAK
	r	r	r	r		rc_w1	rc_w1	rc_w1	r	r

Bit field	Name	Describe
31:12	Reserved	Reserved, the reset value must be maintained.
11	RXS	CAN Rx signal This bit reflects the actual level of the CAN receive pin (CAN_RX).
10	LSMP	Last sample point The last sampled value of the CAN receive pin (corresponding to the value of the current receive bit).
9	RXMD	Receive mode if this bit equals to 1 indicates CAN is currently the receiver.
8	TXMD	Transmit mode if this bit equals to 1 indicates CAN is currently the transmitter.
7:5	Reserved	Reserved, the reset value must be maintained.
4	SLAKINT	Sleep acknowledge interrupt When CAN_INTE.SLKITE=1, once CAN enters sleep mode, hardware will set this bit, and then the corresponding interrupt will be triggered. When this bit is set, if the CAN_INTE.SLKITE bit is set, a state change interrupt will be generated.

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Bit field	Name	Describe
		Software can clear this bit, and hardware also clears this bit when CAN_MSTS.SLPAK bit is cleared. ***Notes****: When CAN_INTE.SLKITE=0, this bit should not be queried, but the CAN_MSTS.SLPAK bit should be queried to know the sleep state.*
3	WKUINT	Wakeup interrupt When CAN is in sleep state, once the start of frame bit (SOF) is detected, the hardware will set this bit; And if the CAN_INTE.WKUITE bit is set, a state change interrupt is generated. This bit is cleared by software.
2	ERRINT	Error interrupt When an error is detected, a bit of the CAN_ESTS register will be set, and if the corresponding interrupt enable bit of the CAN_INTE register is also set, the hardware will set this bit; If the CAN_INTE.ERRITE bit is set, a state change interrupt is generated. This bit is cleared by software.
1	SLPAK	Sleep acknowledge This bit is set by hardware, indicating that the software CAN module is in sleep mode. This bit is the confirmation of the software request to enter sleep mode (the CAN_MCTRL.SLPRQ bit is set). Hardware clears this bit when CAN exits sleep mode (CAN leaves Sleep mode and entering normal mode,it needs to be synchronized with CAN bus). Synchronization with CAN bus here means that the hardware needs to detect 11 consecutive recessive bits on the RX pin of CAN. ***Notes****: clearing CAN_MCTRL.SLPRQ bit by software or hardware will start the process of exiting sleep mode. See the description of CAN_MCTRL.AWKUM bit for details of clearing CAN_MCTRL.SLPRQ bit.*
0	INIAK	Initialization acknowledge This bit is set by hardware, indicating that the software CAN module is in initialization mode. This bit is the confirmation of the software request to enter the initialization mode (the CAN_MCTRL.INIRQ bit is set). Hardware clears this bit when CAN exits initialization mode (CAN leaves Initialization mode and entering normal mode,it needs to be synchronized with CAN bus). Synchronization with CAN bus here means that the hardware needs to detect 11 consecutive recessive bits on the RX pin of CAN.

27.7.3.3 CAN transmit status register (CAN_TSTS)

Address offset: 0x08

Reset value: 0x1C00 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOWM2	LOWM1	LOWM0	TMEM2	TMEM1	TMEM0	CODE		ABRQM2	Reserved			TERRM2	ALSTM2	TXOKM2	RQCPM2
r	r	r	r	r	r	r		rs				rc_w1	rc_w1	rc_w1	rc_w1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABRQM1	Reserved			TERRM1	ALSTM1	TXOKM1	RQCPM1	ABRQM0	Reserved			TERRM0	ALSTM0	TXOKM0	RQCPM0
rs				rc_w1	rc_w1	rc_w1	rc_w1	rs				rc_w1	rc_w1	rc_w1	rc_w1

Bit field	Name	Describe
31	LOWM2	Lowest priority flag for mailbox 2 When multiple mailboxes are waiting to send messages, and the priority of mailbox 2 is the lowest, hardware sets this bit.
30	LOWM1	Lowest priority flag for mailbox 1 When multiple mailboxes are waiting to send messages, and the priority of mailbox 1 is the lowest, hardware sets this bit.
29	LOWM0	Lowest priority flag for mailbox 0 When multiple mailboxes are waiting to send messages, and the priority of mailbox 0 is the lowest, hardware sets this bit. ***Notes**: If there is only one mailbox waiting, CAN_TSTS.LOW[2:0] is cleared*
28	TMEM2	Transmit mailbox 2 empty When there is no message waiting to be sent in mailbox 2, hardware sets this bit.
27	TMEM1	Transmit mailbox 1 empty When there is no message waiting to be sent in mailbox 1, hardware sets this bit.
26	TMEM0	Transmit mailbox 0 empty When there is no message waiting to be sent in mailbox 0, hardware sets this bit .
25:24	CODE[1:0]	Mailbox code When at least one sending mailbox is empty, these two bits represent the next empty sending mailbox number. When all sending mailboxes are empty, these two bits represent the sending mailbox number with the lowest priority.
23	ABRQM2	Abort request for mailbox 2 Set this bit, software can stop the sending request of mailbox 2, and hardware clears this bit when the sending message of mailbox 2 is idle. If there is no message waiting to be sent in mailbox 2, it will have no effect to set this bit.
22:20	Reserved	Reserved, hardware force is 0.
19	TERRM2	Transmission error of mailbox 2 failed. When the mailbox 2 fails to send due to an error, set this bit.
18	ALSTM2	Arbitration lost for mailbox 2 When the mailbox 2 fails to send due to the loss of arbitration, set this bit.
17	TXOKM2	Transmission OK of mailbox 2 The hardware updates this bit after each sending attempt of mailbox 2: 0: The last sending attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 2 is successfully completed, hardware sets

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Bit field	Name	Describe
		this bit. See Figure 27-7.
16	RQCPM2	Request completed mailbox 2 When the last request (send or abort) for mailbox 2 is completed, the hardware will set this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clear this bit (the CAN_TMI2.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM2, CAN_TSTS.ALSTM2 and CAN_TSTS.TERRM2 bits) of mailbox 2 are also cleared.
15	ABRQM1	Abort request for mailbox 1 Set this bit, the software can stop the sending request of mailbox 1, and the hardware clears this bit when the sending message of mailbox 1 is idle. If there is no message waiting to be sent in mailbox 1, it will have no effect to set this bit.
14:12	Reserved	Reserved, the reset value must be maintained.
11	TERRM1	Transmission error of mailbox 1 When the mailbox 1 fails to send due to an error, set this bit.
10	ALSTM1	Arbitration lost for mailbox 1 When the mailbox 1 fails to send due to the loss of arbitration, set this bit
9	TXOKM1	Transmission OK of mailbox 1 The hardware updates this bit after each sending attempt of mailbox 1: 0: The last sending attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 1 is successfully completed, the hardware sets this bit. See Figure 27-7.
8	RQCPM1	Request completed mailbox 1 When the last request (send or abort) for mailbox 1 is completed, the hardware sets this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clears this bit (the CAN_TMI1.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM1, CAN_TSTS.ALSTM1 and CAN_TSTS.TERRM1 bits) of mailbox 1 are also cleared.
7	ABRQM0	Abort request for mailbox 0 The software can stop the sending request of mailbox 0 by setting this bit , and the hardware clears this bit when the sending message of mailbox 0 is idle. If there is no message waiting to be sent in mailbox 0, it will have no effect to set this bit.
6:4	Reserved	Reserved, the reset value must be maintained.
3	TERRM0	Transmission error of mailbox 0 When the mailbox 0 fails to send due to an error, set this bit.
2	ALSTM0	Arbitration lost for mailbox 0 When the mailbox 0 fails to send due to the loss of arbitration, set this bit

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Bit field	Name	Describe
1	TXOKM0	Transmission OK of mailbox 0 The hardware updates this bit after each attempt to send mailbox 0: 0: The last send attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 0 is successfully completed, the hardware sets this bit. See Figure 27-7.
0	RQCPM0	Request completed mailbox 0 When the last request (send or abort) for mailbox 0 was completed, the hardware sets this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clears this bit (the CAN_TMI0.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM0, CAN_TSTS.ALSTM0 and CAN_TSTS.TERRM0 bits) of mailbox 0 are also cleared.

27.7.3.4 CAN receive FIFO 0 register (CAN_RFF0)

Address offset: 0x0c

Reset value: 0x0000 0000

31–16
Reserved

15–6	5	4	3	2	1–0
Reserved	RFFOM0	FFOVR0	FFULL0	Reserved	FFMP0[1:0]
	rs	rc_w1	rc_w1		r

Bit field	Name	Describe
31:6	Reserved	Reserved, the reset value must be maintained.
5	RFFOM0	Release FIFO 0 output mailbox. The software releases the output mailbox of the receive FIFO by setting this bit. If the receiving FIFO is empty, it will have no effect on setting this bit, that is, it will be meaningful to set this bit only when there is a message in the FIFO. If there are more than two messages in FIFO, because of the characteristics of FIFO, the software needs to release the output mailbox to access the second message. When the output mailbox is released, the hardware clears this bit.
4	FFOVR0	FIFO 0 overrun When FIFO 0 is full, a new message is received and the message meets the filtering conditions, the hardware sets this bit. This bit is cleared by software.
3	FFULL0	FIFO 0 full When there are 3 messages in FIFO 0, the hardware sets this bit'. This bit is cleared by software.
2	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Describe
1:0	FFMP0[1:0]	FIFO 0 message pending Number of FIFO messages 0 These two bits reflect the number of messages currently stored in the receiving FIFO 0. Every time a new message is stored in the receiving FIFO 0, the hardware adds 1 to the CAN_RFF0.FFMP0. Every time the software writes '1' to the CAN_RFF0.RFFOM0 bit to release the output mailbox, CAN_RFF0.FFMP0 is decremented by 1 until it is 0.

27.7.3.5 CAN receive FIFO 1 register (CAN_RFF1)

Address offset: 0x10

Reset value: 0x0000 0000

31–16
Reserved

15–6	5	4	3	2	1–0
Reserved	RFFOM1	FFOVR1	FFULL1	Reserved	FFMP1[1:0]
	rs	rc_w1	rc_w1		r

Bit field	Name	Describe
31:6	Reserved	Reserved, the reset value must be maintained.
5	RFFOM1	Release FIFO 1 output mailbox. The software releases the output mailbox of the receive FIFO by setting this bit. If the receiving FIFO is empty, it will have no effect on setting this bit, that is, it will be meaningful to set this bit only when there is a message in the FIFO. If there are more than two messages in FIFO, because of the characteristics of FIFO, the software needs to release the output mailbox to access the second message. When the output mailbox is released, the hardware clears this bit.
4	FFOVR1	FIFO 1 overrun When FIFO 1 is full, a new message is received and the message meets the filtering conditions, the hardware sets this bit. This bit is cleared by software.
3	FFULL1	FIFO 1 full When there are 3 messages in FIFO 1, the hardware sets this bit. This bit is cleared by software.
2	Reserved	Reserved, the reset value must be maintained.
1:0	FFMP1[1:0]	FIFO 1 message pending Number of messages in FIFO 1 These two bits reflect the number of messages stored in the current receiving FIFO 1. Every time a new message is stored in receiving FIFO 1, the hardware adds 1 to CAN_RFF1.FFMP1. Every time the software releases the output mailbox by writing '1' to CAN_RFF1.RFFOM1 bit, CAN_RFF1.FFMP1 is decremented by 1 until it is 0.

27.7.3.6 CAN interrupt enable register (CAN_INTE)

Address offset: 0x14

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Reset value: 0x0000 0000

31–18	17	16
Reserved	SLKITE	WKUITE
	rw	rw

15	14–12	11	10	9	8	7	6	5	4	3	2	1	0
ERRITE	Reserved	LECITE	BOFITE	EPVITE	EWGITE	Reserved	FOVITE1	FFITE1	FMPITE1	FOVITE0	FFITE0	FMPITE0	TMEITE
rw		rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Describe
31:18	Reserved	Reserved, the reset value must be maintained.
17	SLKITE	Sleep interrupt enable 0: when the CAN_MSTS.SLAKINT bit is set, no interrupt is generated; 1: when the CAN_MSTS.SLAKINT bit is set, an interrupt is generated.
16	WKUITE	Wakeup interrupt enable 0: when CAN_MSTS.WKUINT bit is set, no interrupt is generated; 1: when CAN_MSTS.WKUINT bit is set, an interrupt is generated.
15	ERRITE	Error interrupt enable 0: When there is an error registration in the CAN_ESTS register, no interrupt is generated; 1: When there is an error registration in the CAN_ESTS register, an interrupt is generated.
14:12	Reserved	Reserved, the reset value must be maintained.
11	LECITE	Last error code interrupt enable 0: When an error is detected, when the hardware sets CAN_ESTS.LEC[2:0], the CAN_MSTS.ERRINT bit is not set; 1: When an error is detected, when the hardware sets CAN_ESTS.LEC[2:0], the CAN_MSTS.ERRINT bit is set.
10	BOFITE	Bus-off interrupt enable 0: When CAN_ESTS.BOFFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: When the CAN_ESTS.BOFFL bit is set, set the CAN_MSTS.ERRINT bit.
9	EPVITE	Error passive interrupt enable 0: when CAN_ESTS.EPVFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: when CAN_ESTS.EPVFL bit is set, set the CAN_MSTS.ERRINT bit.
8	EWGITE	Error warning interrupt enable 0: When CAN_ESTS.EWGFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: when the CAN_ESTS.EWGFL bit is set, set the CAN_MSTS.ERRINT bit.
7	Reserved	Reserved, the reset value must be maintained.
6	FOVITE1	FIFO 1 overflow interrupt enable 0: When CAN_RFF1.FFOVR bit is set, no interrupt is generated; 1: When CAN_RFF1.FFOVR bit is set, an interrupt is generated.
5	FFITE1	FIFO 1 full interrupt enable 0: When CAN_RFF1.FFULL bit is set, no interrupt is generated;

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Bit field	Name	Describe
		1: When CAN_RFF1.FFULL bit is set, an interrupt is generated.
4	FMPITE1	FIFO 1 message pending interrupt enable 0: When CAN_RFF1.FFMP[1:0] bits are non-0, no interrupt is generated; 1: When CAN_RFF1.FFMP[1:0] bits are not 0, an interrupt is generated.
3	FOVITE0	FIFO 0 overflow interrupt enable 0: When CAN_RFF0.FFOVR bit is set, no interrupt is generated; 1: When CAN_RFF0.FFOVR bit is set, an interrupt is generated.
2	FFITE0	FIFO 0 full interrupt enable 0: When CAN_RFF0.FFULL bit is set, no interrupt is generated; 1: When CAN_RFF0.FFULL bit is set, an interrupt is generated.
1	FMPITE0	FIFO 0 message pending interrupt enable 0: When CAN_RFF0.FFMP[1:0] bits are non-0, no interrupt is generated; 1: When CAN_RFF0.FFMP[1:0] bits are not 0, an interrupt is generated.
0	TMEITE	Transmit mailbox empty interrupt enable. 0: When CAN_TSTS.RQCPMx bit is set, no interrupt is generated; 1: When CAN_TSTS.RQCPMx bit is set, an interrupt is generated. ***Notes**: Please refer to 27.5 Section CAN interrupt.*

27.7.3.7 CAN error status register (CAN_ESTS)

Address offset: 0x18

Reset value: 0x0000 0000

31–24	23–16
RXEC[7:0]	TXEC[7:0]
r	r

15–7	6–4	3	2	1	0
Reserved	LEC[2:0]	Reserved	BOFFL	EPVFL	EWGFL
	rw		r	r	r

Bit field	Name	Describe
31:24	RXEC[7:0]	Receive error counter This counter is implemented according to the receiving part of the fault definition mechanism of CAN protocol. According to the standard of CAN, when receiving error, the counter is incremented by 1 or incremented by 8 according to the error condition; After each successful reception, the counter is decremented by 1, or when the value of the counter is greater than 127, its value is set to 120. When the value of this counter exceeds 127, CAN enters the error passive state.
23:16	TXEC[7:0]	Least significant byte of the 9-bit transmit error counter Similar to the above, this counter is implemented according to the sending part of the fault definition mechanism of CAN protocol.
15:7	Reserved	Reserved, the reset value must be maintained.
6:4	LEC[2:0]	The Last error code.

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Bit field	Name	Describe
		When an error is detected on the CAN bus, the hardware is set according to the error situation. When the message is sent or received correctly, the hardware clears its value to '0'. The hardware does not use error code 7, and the software can set this value, so that the code update can be detected. 000: there is no error; 001: Bit padding error; 010: wrong Format (form); 011: Acknowledgment (ack) error; 100: recessive dislocation（CAN transmits recessive but detect dominant on the bus）; 101: dominant dislocation(CAN transmits dominant but detect recessive on the bus); 110: CRC error; 111: Set by software.
3	Reserved	Reserved, the reset value must be maintained.
2	BOFFL	Bus-off flag When going bus-off, hardware sets this bit. When the transmission error counter CAN_TSTS.TXEC overflows, that is, it is greater than 255, CAN goes bus-off. Please refer to 27.5.1 section.
1	EPVFL	Error passive flag When the number of errors reaches the threshold of error passivity, the hardware sets the bit. (The value of the receiving error counter or the sending error counter is > 127).
0	EWGFL	Error warning flag When the number of errors reaches the warning threshold, the hardware sets the bit. (The value of the receiving error counter or the sending error counter is ≥96).

27.7.3.8 CAN bit timing register (CAN_BTIM)

Address offset: 0x1C

Reset value: 0x0123 0000

***Notes**: This register CAN only be accessed by software when CAN is in initialization mode.*

31	30	29-26	25-24	23	22-20	19-16
SLM	LBM	Reserved	RSJW[1:0]	Reserved	TBS2[2:0]	TBS1[3:0]
rw	rw		rw		rw	rw

15-10	9-0
Reserved	BRTP[9:0]
	rw

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Bit field	Name	Describe
31	SLM	Silent mode（debug） 0: Normal state; 1: Silent mode.
30	LBM	Loop back mode（debug） 0: Loopback mode is prohibited; 1: Loopback mode is allowed.
29:26	Reserved	Reserved, the reset value must be maintained.
25:24	RSJW[1:0]	Resynchronization jump width For resynchronization, this bit field defines the upper limit of how many time units CAN be extended or shortened by CAN hardware in each bit. $t_{RJW} = t_{CAN} \times (RSJW[1:0] + 1)$.
23	Reserved	Reserved, the reset value must be maintained.
22:20	TBS2[2:0]	Time segment 2 This bit field defines how many time units time period 2 occupies. $t_{BS2} = t_{CAN} \times (TBS2[2:0] + 1)$.
19:16	TBS1[3:0]	Time segment 1 This bit field defines how many time units time period 1 occupies. $t_{BS1} = t_{CAN} \times (TBS1[3:0] + 1)$ For details of bit time characteristics, please refer to section 27.4.7 secton: bit time characteristics.
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	BRTP[9:0]	Baud rate prescaler This bit field defines the time length of the time unit (tq) $t_q = (BRTP[9:0]+1) \times t_{PCLK}$

27.7.4 CAN mailbox register

This section describes the sending and receiving mailbox registers. For more information about register mapping, refer to 27.4.6 section: message storage.

27.7.4.1 Tx mailbox identifier register(CAN_TMIx)(x=0..2)

Address offset: 0x180, 0x190, 0x1A0

Reset value: 0xXXXX XXXX,X= undefined bit (except bit 0, TXRQ=0 at reset)

***Notes**: 1.This register is write-protected when the mailbox to which it belongs is waiting to be sent;*

2.This register implements the send request control function (bit 0)-the reset value is 0.

31–21	20–16
STDID[10:0]/EXTID[28:18]	EXTID[17:13]
rw	rw

15–3	2	1	0
EXTID[12:0]	IDE	RTRQ	TXRQ
rw	rw	rw	rw

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Bit field	Name	Describe
31:21	STDID[10:0]/EXTID[28:18]	Standard identifier or extended identifier Depending on the content of CAN_TMIx.IDE bits, these bits are either standard identifiers or high bytes of extended identity.
20:3	EXTID[17:0]	Extended identifier Low byte of extended identity.
2	IDE	Identifier extension. This bit determines the type of identifier used for sending messages in the mailbox. 0: Use standard identifier; 1: Use extended identifiers.
1	RTRQ	The Remote transmission request 0: data frame; 1: Remote frame.
0	TXRQ	Transmit mailbox request It is set by the software to request to send the data of the mailbox. When the data transmission is completed and the mailbox is empty, hardware clears it.

27.7.4.2 Tx mailbox data length and time stamp register (CAN_TMDTx)(x=0..2)

When the mailbox is not empty, all bits in this register are write-protected.

Address offset: 0x184, 0x194, 0x1A4

Reset value: undefined

31–16
MTIM[15:0]
rw

15–9	8	7–4	3–0
Reserved	TGT	Reserved	DLC[3:0]
	rw		rw

Bit field	Name	Describe
31:16	MTIM[15:0]	Message time stamp This field contains the value of the 16-bit timer at the time of sending the message SOF.
15:9	Reserved	Reserved, the reset value must be maintained.
8	TGT	Transmit global time This bit is valid only when the CAN is in time-triggered communication mode, that is, the CAN_MCTRL.TTCM bit is set. 0: Do not send the time stamp CAN_TMDTx.MTIM[15:0]; 1: send the time stamp CAN_TMDTx.MTIM[15:0]. In a message of length 8, the time stamp CAN_TMDTx.MTIM[15:0] is the last two bytes sent: CAN_TMDTx.MTIM[7:0] is the seventh byte and CAN_TMDTx.MTIM[15:8] is the eighth byte. They replace the data written in CAN_TMDHx[31:16]

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Bit field	Name	Describe
		(CAN_TMDLx.DATA6[7:0] and CAN_TMDLx.DATA7[7:0]). In order to send the 2 bytes of the timestamp, DLC must be programmed to 8.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DLC[3:0]	Data length code This field specifies the data length of the data message or the data length requested by the remote frame. One message contains 0 to 8 bytes of data, which is determined by DLC.

27.7.4.3 Tx mailbox low byte data register(CAN_TMDLx) (x=0..2)

When the mailbox is not empty, all bits in this register are write-protected.

Address offset: 0x188, 0x198, 0x1A8

Reset value: undefined

31 ... 24	23 ... 16
DATA3[7:0]	DATA2[7:0]
rw	rw
15 ... 8	**7 ... 0**
DATA1[7:0]	DATA0[7:0]
rw	rw

Bit field	Name	Describe
31:24	DATA3[7:0]	Data byte 3 Data byte 3 of the message.
23:16	DATA2[7:0]	Data byte 2 Data byte 2 of the message.
15:8	DATA1[7:0]	Data byte 1 Data byte 1 of the message.
7:0	DATA0[7:0]	Data byte 0 Data byte 0 of the message. *Notes:the message contains 0 to 8 bytes of data, starting from byte 0.*

27.7.4.4 Tx mailbox high byte data register(CAN_TMDHx) (x=0..2)

When the mailbox is not empty, all bits in this register are write protected.

Address offset: 0x18c, 0x19c, 0x1ac

Reset value: undefined

31 ... 24	23 ... 16
DATA7[7:0]	DATA6[7:0]
rw	rw
15 ... 8	**7 ... 0**
DATA5[7:0]	DATA4[7:0]
rw	rw

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Bit field	Name	Describe
31:24	DATA7[7:0]	Data byte 7 Data byte 7 of the message. *Notes: If the CAN_MCTRL.TTCM bit is '1' and the CAN_TMDTx.TGT bit of this mailbox is also '1', then DATA7 and DATA6 will be replaced by TIME stamps.*
23:16	DATA6[7:0]	Data byte 6 Data byte 6 of the message.
15:8	DATA5[7:0]	Data byte 5 Data byte 5 of the message.
7:0	DATA4[7:0]	Data byte 4 Data byte 4 of the message.

27.7.4.5 Receive FIFO mailbox identifier register (CAN_RMIx) (x=0..1)

Address offset: 0x1B0, 0x1C0

Reset value: undefined

Notes: All receiving mailbox registers are read-only.

31–21	20–16
STDID[10:0]/EXTID[28:18]	EXTID[17:13]
r	r

15–3	2	1	0
EXTID[12:0]	IDE	RTRQ	Reserved
r	r	r	

Bit field	Name	Describe
31:21	STDID[10:0]/EXTID[28:18]	Standard identifier or extended identifier Depending on the content of CAN_RMIx.IDE bits, these bits are either standard identifiers or high bytes of extended identity.
20:3	EXTID[17:0]	Extended identifier Low byte of extended identity.
2	IDE	Identifier extension. This bit determines the type of identifier used for sending messages in the mailbox. 0: Use standard identifier; 1: Use extended identifiers.
1	RTRQ	Remote transmission request 0: data frame; 1: Remote frame.
0	Reserved	Reserved, the reset value must be maintained.

27.7.4.6 Receive FIFO mailbox data length and time stamp register(CAN_RMDTx)(x=0..1)

Address offset: 0x1B4, 0x1C4

Reset value: undefined

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***Notes**: All receiving mailbox registers are read-only.*

31–16
MTIM[15:0]
r

15–8	7–4	3–0
FMI[7:0]	Reserved	DLC[3:0]
r		r

Bit field	Name	Describe
31:16	MTIM[15:0]	Message time stamp This field contains the value of the 16-bit timer at the time of sending the message SOF.
15:8	FMI[7:0]	Filter match index Here is the filter serial number of the information transfer stored in the mailbox. For details of identifier filtering, please refer to 27.4.5 section: Identifier filtering.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DLC[3:0]	Data length code This field indicates the data length (0~8) of the received data frame. For remote frame requests, the data length DLC is always 0.

27.7.4.7 Receive FIFO mailbox low byte data register(CAN_RMDLx)(x=0..1)

Address offset: 0x1B8, 0x1C8

Reset value: undefined

***Notes**: All receiving mailbox registers are read-only.*

31–24	23–16
DATA3[7:0]	DATA2[7:0]
r	r

15–8	7–0
DATA1[7:0]	DATA0[7:0]
r	r

Bit field	Name	Describe
31:24	DATA3[7:0]	Data byte 3 Data byte 3 of the message.
23:16	DATA2[7:0]	Data byte 2 Data byte 2 of the message.
15:8	DATA1[7:0]	Data byte 1 Data byte 1 of the message.
7:0	DATA0[7:0]	Data byte 0 Data byte 0 of the message. Notes: the message contains 0 to 8 bytes of data, starting from byte 0.

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27.7.4.8 Receive FIFO mailbox high byte data register(CAN_RMDHx) (x=0..1)

Address offset: 0x1BC, 0x1CC

Reset value: undefined

Note: All receiving mailbox registers are read-only.

31–24	23–16
DATA7[7:0]	DATA6[7:0]
r	r

15–8	7–0
DATA5[7:0]	DATA4[7:0]
r	r

Bit field	Name	Describe
31:24	DATA7[7:0]	Data byte 7 Data byte 7 of the message.
23:16	DATA6[7:0]	Data byte 6 Data byte 6 of the message.
15:8	DATA5[7:0]	Data byte 5 Data byte 5 of the message.
7:0	DATA4[7:0]	Data byte 4 Data byte 4 of the message.

27.7.5 CAN filter register

27.7.5.1 CAN filter master control register (CAN_FMC)

Address offset: 0x200

Reset value: 0x2A1C 0E01

***Notes**: The unreserved bits of this register are completely controlled by software.*

31–16
Reserved

15–1	0
Reserved	FINITM
	rw

Bit field	Name	Describe
31:1	Reserved	Reserved, the reset value must be maintained.
0	FINITM	Filter init mode Initialization mode settings for all filter groups. 0: The filter group works in normal mode; 1: The filter group works in initialization mode.

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27.7.5.2 CAN filter mode register (CAN_FM1)

Address offset: 0x204

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

31															16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FB13	FB12	FB11	FB10	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Describe
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FBx	Filter mode Working mode of filter group X 0: Two 32-bit registers of CAN_FiRx work in identifier mask mode; 1: Two 32-bit registers of CAN_FiRx work in identifier list mode.

27.7.5.3 CAN filter scale register (CAN_FS1)

Address offset: 0x20C

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

31															16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FSC13	FSC12	FSC11	FSC10	FSC9	FSC8	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Describe
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FSCx	Filter scale configuration Bit width of filter group x (13~0). 0: The filter bit width is 2 16-bits; 1: The filter bit width is a single 32-bit.

27.7.5.4 CAN filter FIFO assignment register (CAN_FFA1)

Address offset: 0x214

Reset value: 0x0000 0000

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***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

17	16
Reserved	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FAF13	FAF12	FAF11	FAF10	FAF9	FAF8	FAF7	FAF6	FAF5	FAF4	FAF3	FAF2	FAF1	FAF0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Describe
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FAFx	Filter FIFO assignment for filter x After the message is filtered by a certain filter, it will be stored in its associated FIFO. 0: the filter is associated to FIFO0; 1: the filter is associated to FIFO1.

27.7.5.5 CAN filter activation register (CAN_FA1)

Address offset: 0x21C

Reset value: 0x0000 0000

31															16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		FAC13	FAC12	FAC11	FAC10	FAC9	FAC8	FAC7	FAC6	FAC5	FAC4	FAC3	FAC2	FAC1	FAC0
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Describe
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FACx	Filter active The software sets '1' for someone to activate the corresponding filter. The corresponding filter register i(CAN_FiR[2:1]) can only be modified after the CAN_FA1.FACx bit is cleared or the CAN_FMC.FINITM bit is set. 0: The filter is disabled; 1: The filter is activated.

27.7.5.6 CAN filter i register x（CAN_FiRx）（i＝0..13;x=1..2）

Address offset: 0x240h, 0x31C

Reset value: undefined

***Notes**: 14 groups of filters: i = 0 ... 13. Each group of filters consists of two 32-bit registers, CAN_FiR[2:1].*

Only when the corresponding CAN_FA1.FACx bit is cleared or the CAN_FMC.FINIT bit is set, the corresponding filter register can be modified.

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FBC31	FBC30	FBC29	FBC28	FBC27	FBC26	FBC25	FBC24	FBC23	FBC22	FBC21	FBC20	FBC19	FBC18	FBC17	FBC16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FBC15	FBC14	FBC13	FBC12	FBC11	FBC10	FBC9	FBC8	FBC7	FBC6	FBC5	FBC4	FBC3	FBC2	FBC1	FBC0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	**Name**	**Describe**
31:0	FBC[31:0]	Filter bits Identifier pattern Each bit of the register corresponds to the level of the corresponding bit of the expected identifier. 0: the corresponding bit is expected to be dominant; 1: The corresponding bit is expected to be recessive. Mask bit pattern Each bit of the register indicates whether the corresponding identifier register bit must be consistent with the corresponding bit of the expected identifier. 0: Don't care, this bit is not used for comparison; 1: Must match, and the incoming identifier bit must be consistent with the identifier register bit corresponding to the filter.

***Notes**: According to the different settings of filter bit width and mode, the functions of the two registers in the filter bank are different. For the mapping of filters, function description and association of mask registers, see 27.4.5 Section: identifier filtering.*

Mask/identifier register in **mask mode** has the same definition as register bit in **identifier list mode**.

See for the address of the filter bank register Table 27-4.

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28 Universal serial bus full-speed device interface (USB_FS_Device)

28.1 Introduction

Universal serial bus full-speed device interface (USB_FS_Device) module is a peripheral that conforms to the USB2.0 full-speed protocol. It contains the USB PHY of the physical layer and does not require an additional PHY chip. USB_FS_Device supports four transfer types defined in USB2.0 protocol: control transfer, bulk transfer, interrupt transfer and isochronous transfer.

28.2 Main features

- Comply with USB2.0 full-speed device specification
- Supports up to 8 configurable USB endpoints
- Each endpoint supports four transfer types in the USB2.0 protocol:
  - Control transfer
  - Bulk transfer
  - Interrupt transfer
  - Isochronous transfer
- Bulk endpoint/isochronous endpoint supports double buffering mechanism
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding and bit-stuffing
- Support USB suspend/resume operation
- Frame lock clock pulse generation

Figure 28-1 is a functional block diagram of a USB peripheral.

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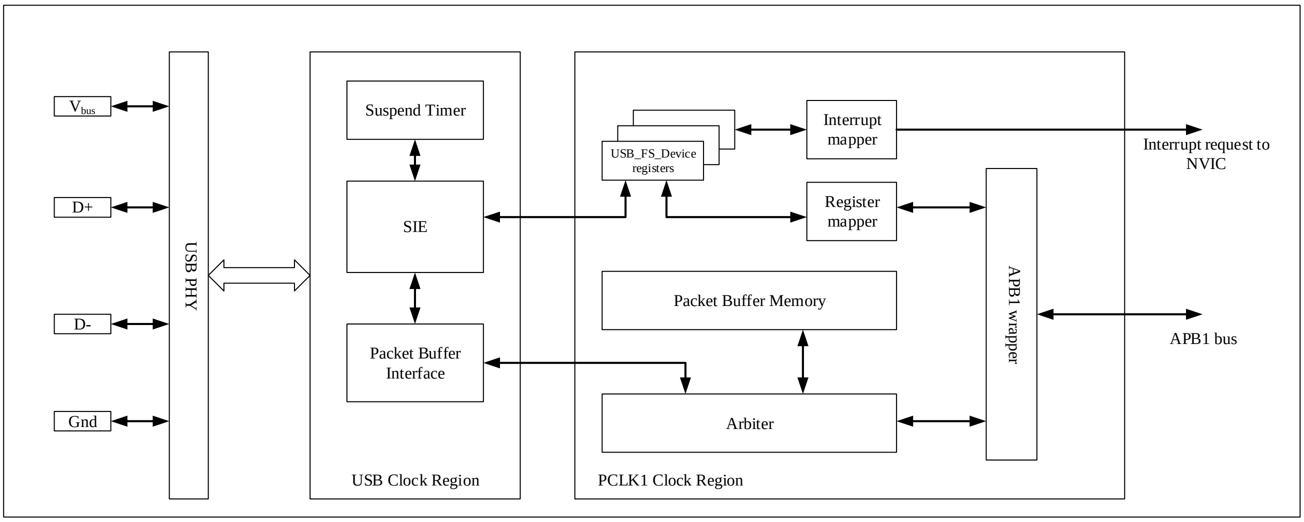
Figure 28-1 USB device block diagram



28.3 Clock configuration

The USB 2.0 protocol specification stipulates that the USB full-speed module uses a fixed 48MHz clock. In order to provide an accurate 48MHz clock to USB_FS_Device, a two-stage clock configuration is required, as follows:

- In the first stage, the 48MHz working clock is obtained by accurate frequency division of PLLCLK, so when using USB_FS_Device, it is necessary to ensure that the PLLCLK clock is 48MHz/72MHz/96MHz, otherwise USB_FS_Device cannot work normally;
- In the second stage, enable the USB peripheral clock mounted on the APB1 bus, that is, the APB1 bus clock. Its frequency does not have to be equal to 48MHz, but can be greater or less than 48MHz.

Note:

1、The frequency of the APB1 bus clock must be greater than 8MHz, otherwise the data buffer may overflow/underflow.

28.4 Functional description

Based on this module, data exchange can be realized between the microcontroller and the PC host through a USB connection. The data transfer between the microcontroller and the PC host is based on a 512-byte dedicated SRAM, which is the Packet Buffer Memory in Figure 28-1. USB peripherals can directly access this SRAM. The actual usage size of this dedicated SRAM is determined by the number of endpoints used and the endpoint packet buffer size of each endpoint. Each endpoint has a buffer description table entry, which describes the buffer address, size and the number of bytes that need to be transferred. For details, please refer to 28.4.2 Buffer Description Table. The SRAM is mapped to the APB1 peripheral memory area, its address is from 0x4000 6000 to 0x4000 63FF, the total capacity is 1KB, but only 512 bytes are used due to the bus width, and the buffer description table of each endpoint is also stored in this SRAM, so the maximum endpoint packet buffer that can be used by each endpoint is less than 512 bytes.

Note:

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1、USB and CAN share this SRAM, so USB and CAN cannot be used at the same time.

28.4.1 Access Packet Buffer Memory

As shown in Figure 28-1, the microcontroller communicates with the USB module through the APB1 bus, and the microcontroller accesses the Packet Buffer Memory through the APB1 wrapper. When the microcontroller and the USB module both access the Packet Buffer Memory, the Arbiter decides who can access, the arbitration logic is that half of the APB1 bus cycle is used for the microcontroller to access the Packet Buffer Memory, and the other half of the cycle is used for the USB module to access the Packet Buffer Memory, in this way, the access conflicts caused by the continuous access of the microcontroller to the Packet Buffer Memory can be avoided.

Note:

1、 APB1 bus and USB module access Packet Buffer Memory in different ways.

28.4.1.1 USB module access Packet Buffer Memory

The USB module accesses the Packet Buffer Memory in 16-bit mode, refer to Figure 28-2. When the USB module accesses the Packet Buffer Memory, first find the location of the buffer description table in the Packet Buffer Memory through the USB_BUFTAB register. The value of the USB_BUFTAB register indicates the starting address of the buffer description table, which must be within the memory range of the Packet Buffer Memory and be 8-byte aligned. If only endpoint 0 and endpoint 1 are used, the buffer description table only needs 16 bytes. If only endpoint 0 and endpoint 7 are used, the buffer description table needs 64 bytes. Although endpoint 1 to endpoint 6 are not used, but The description table of endpoint 7 starts from 56 bytes, so it will occupy 64 bytes of space.

28.4.1.2 User application access Packet Buffer Memory

The user application program on the microcontroller needs to access the Packet Buffer Memory from the APB1 bus according to 32-bit alignment and 16-bit read and write access, that is, the address of the operation data must be 32-bit aligned, and only 16-bit data can be read or written at a time, can't be 8-bit nor 32-bit. Figure 28-2 shows the way in which the user application program on the microcontroller and the USB module accesses the Packet Buffer Memory.

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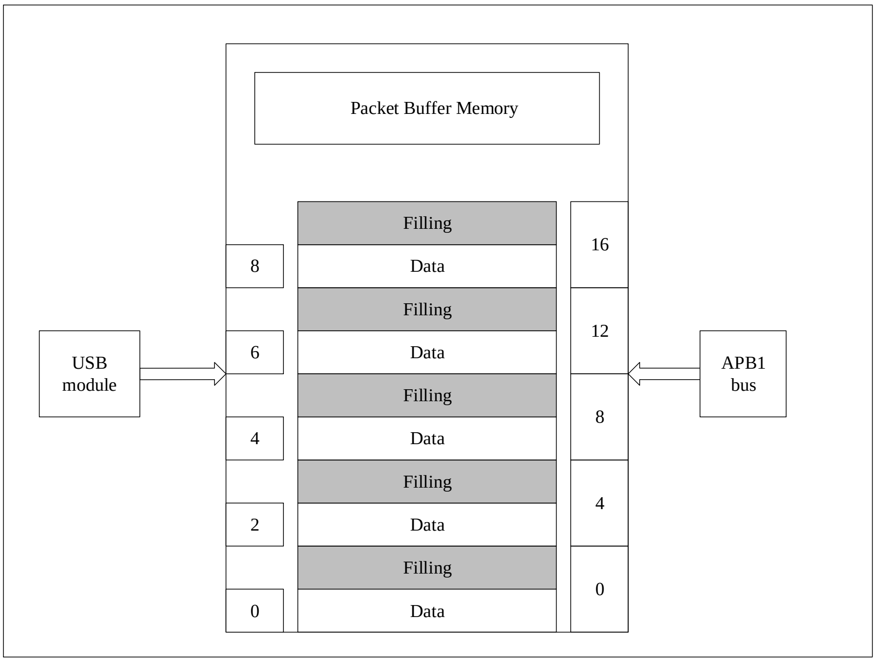
Figure 28-2 The user applications on the microcontrollers and the USB modules access Packet Buffer Memory



28.4.2 Buffer description table

The buffer description table defines the buffer address, size and the number of bytes to be transmitted for the endpoint used in the communication process. Each endpoint corresponds to two endpoint data packet buffers, one for sending and one for receiving. These endpoint packet buffers can be stored anywhere in the entire Packet Buffer Memory, and the buffer description table is also located in the Packet Buffer Memory, whose starting address is determined by the USB_BUFTAB register.

The buffer description table has a total of 8 entries, each entry corresponds to an endpoint register, each register has two directions of sending and receiving, and each direction requires two 16-bit word buffer description tables, so each table items consist of four 16-bit words, so the start address of the buffer description table must be 8-byte aligned. Endpoint packet buffers for unused endpoints or in the unused direction of a used endpoint may be used for other purposes. The relationship between the buffer description table and the endpoint packet buffer is shown in Figure 28-3 below.

Whether the endpoint is used for receiving or sending, the buffer description table starts with the first entry, which is the very bottom of the buffer description table. The USB module cannot access/modify the data of other endpoint packet buffers other than the currently allocated endpoint packet buffer area, For example: when the endpoint 0 packet receive buffer receives a data larger than the current endpoint 0 packet receive buffer from the PC host, the endpoint 0 only receives data up to the endpoint 0 packet receive buffer size, other redundant data is discarded and a buffer overflow exception occurs.

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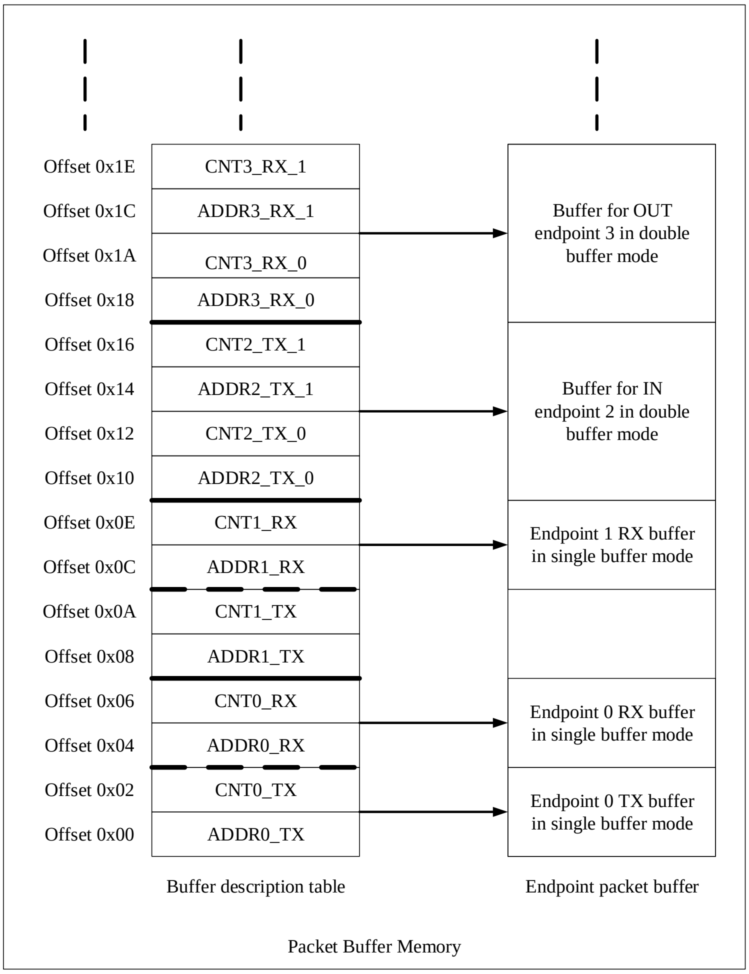
Figure 28-3 The relationship between the buffer description table and the endpoint packet buffer



28.4.3 Double-buffered endpoints

28.4.3.1 Double buffer endpoint function introduction

When a large amount of data needs to be transmitted between the PC host and the USB device, the use of bulk transmission allows the PC host to transmit data with maximum efficiency within one frame. However, when the transmission speed is too fast, the USB device will receive a new data packet when the USB device is processing the previous data transmission. In order to correctly complete the previous data transmission, the USB can only reply the NAK handshake signal to the PC host. Due to the retransmission mechanism of bulk transfer, the PC host will continue to retransmit the same data packet until the USB device can process the data packet and reply to the PC host with an ACK handshake signal, the PC host will stop retransmitting the data packet. Such retransmission will occupy a lot of bandwidth, thereby reducing the rate of bulk transfer. In order to solve this problem, a double buffering mechanism is introduced to improve the efficiency of bulk transfer, and flow control is implemented.

When the unidirectional endpoint uses the double buffer mechanism, both the receive buffer and the transmit buffer on the endpoint will be used, one of the buffers is used by the USB module, and the other buffer is used by the microcontroller, use the data toggle bit in the endpoint register to select which buffer is currently used, and introduce two flags for this: DATTOG and SW_BUF. DATTOG indicates the buffer currently being used by the USB module,

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and SW_BUF indicates the buffer currently being used by the application on the microcontroller. The definitions of DATTOG and SW_BUF are shown in Table 28-1 shown. A unidirectional endpoint using the double buffer mechanism only needs to use one USB_EPn register.

Table 28-1 DATTOG and SW_BUF definitions

Buffer flag	Sending endpoint	Receiving endpoint
DATTOG	DATTOG_TX (Bit 6 of the USB_EPn register)	DATTOG_RX (Bit 14 of the USB_EPn register)
SW_BUF	Bit 14 of the USB_EPn register	Bit 6 of the USB_EPn register

As shown in Figure 28-3, when an endpoint uses the double buffer mechanism, all four buffer description table entries of the endpoint will be used. DATTOG and SW_BUF are responsible for flow control. When a transfer is complete, the USB hardware toggles the DATTOG bit; when the application on the microcontroller has finished processing the data, the software toggles SW_BUF bit. After the first transfer starts, in the subsequent transfer process, if the values of DATTOG and SW_BUF are equal, a buffer access conflict occurs between the USB module and the application, the transfer is paused, and a NAK handshake packet is sent to the host; when the values of DATTOG and SW_BUF are not equal, normal USB communication can be performed.

Table 28-2 How to use double buffering

Endpoint type	DATTOG	SW_BUF	Buffer used by the USB module	Buffers used by the application
IN Endpoint	0	1	ADDRn_TX_0/CNTn_TX_0	ADDRn_TX_1/CNTn_TX_1
	1	0	ADDRn_TX_1/CNTn_TX_1	ADDRn_TX_0/CNTn_TX_0
	0	0	Endpoint is in NAK state	ADDRn_TX_0/CNTn_TX_0
	1	1	Endpoint is in NAK state	ADDRn_TX_1/CNTn_TX_1
OUT Endpoint	0	1	ADDRn_RX_0/CNTn_RX_0	ADDRn_RX_1/CNTn_RX_1
	1	0	ADDRn_RX_1/CNTn_RX_1	ADDRn_RX_0/CNTn_RX_0
	0	0	Endpoint is in NAK state	ADDRn_RX_0/CNTn_RX_0
	1	1	Endpoint is in NAK state	ADDRn_RX_1/CNTn_RX_1

Note:

1、The double-buffered bulk endpoint will only set the endpoint to the NAK state when there is a buffer access conflict, and will not set the endpoint to the NAK state after each correct transmission is completed.

28.4.3.2 Double-buffered endpoint usage

If you want to use double-buffered bulk endpoints, you can set them up as follows:

- Set USB_EPn.EP_TYPE = 00, define the endpoint as a bulk endpoint
- Set USB_EPn.EP_KIND = 1, define endpoint as double buffer endpoint

As shown in Figure 28-3, when double-buffered bulk endpoint 3 performs data transmission in the OUT direction, assuming DATTOG = 1 and SW_BUF = 0, it means that the application can process the data in buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, after receiving the data from the USB bus, the USB module fills the data into the buffer1 corresponding to ADDR3_RX_1/CNT3_RX_1. When a transaction transfer on the USB bus is completed, the hardware will toggle DATTOG = 0. If the application has not finished processing the data in buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, the software will not toggle SW_BUF (SW_BUF = 0). If there is

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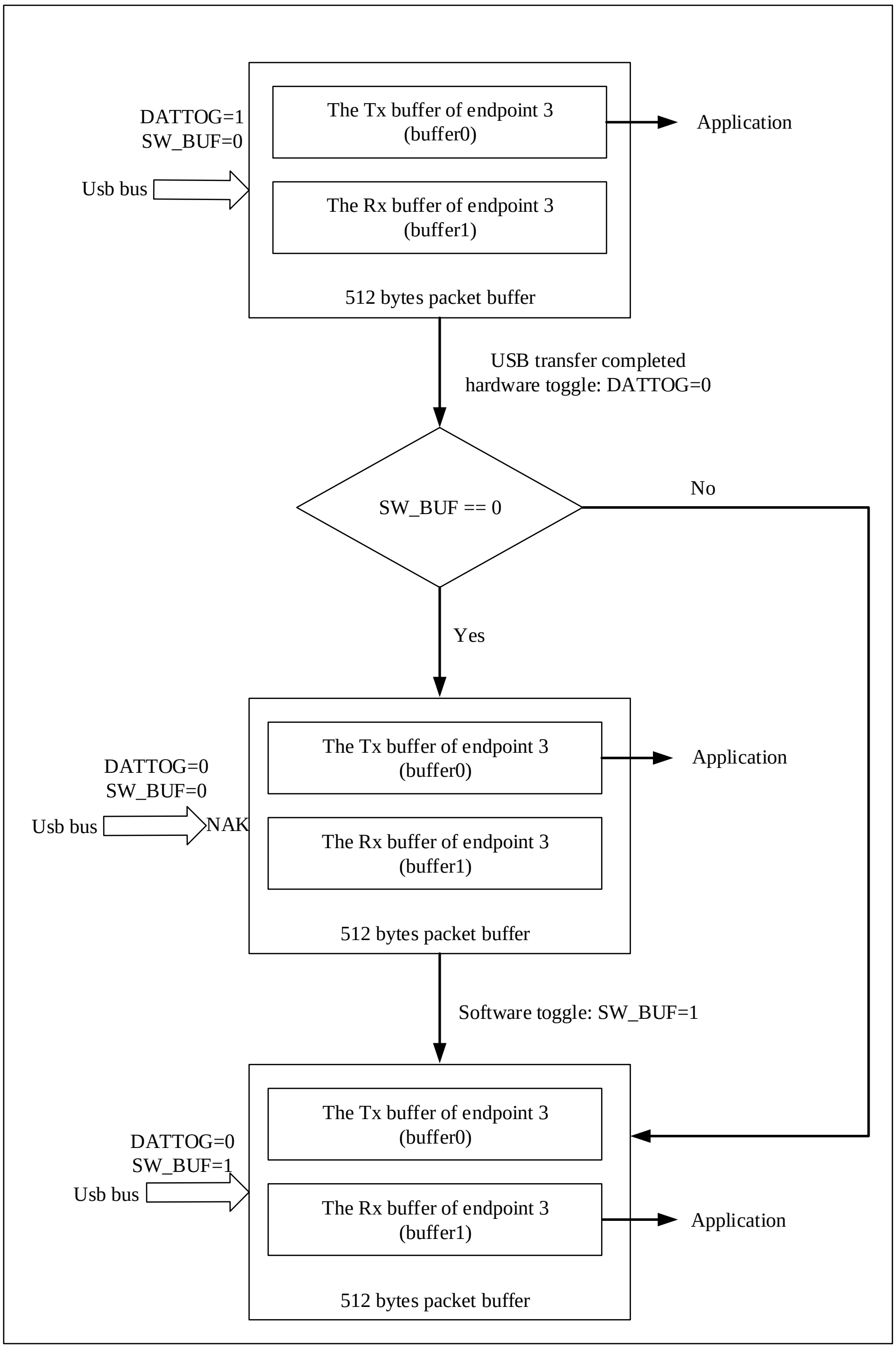
another OUT data packet transmission on the USB bus at this time, the USB device will automatically reply the NAK handshake signal to indicate flow control until the application finishes processing the data in buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, and the software toggle SW_BUF = 1. In this case, the DATTOG and SW_BUF values are different. If there is another OUT data packet transmission on the USB bus, the USB device can receive data normally, and fill the received data into buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, and the application can process the buffer1 corresponding to ADDR3_RX_1/CNT3_RX_1. As shown in Figure 28-4 below.

Figure 28-4 Double buffered bulk endpoint example



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28.4.4 USB transfer

28.4.4.1 Overview of USB transfer

A USB transfer consists of multiple transactions, and a transaction consists of multiple packets.

A packet is the basic unit of USB transmission. All data must be packaged before being transmitted on the USB bus. The process of one time receiving or sending data on the USB is called a transaction, and there are three types of transactions: Setup transaction, Data IN transaction, and Data OUT transaction.

28.4.4.2 IN transaction

When the host wants to read the data of the USB device, the host sends a PID IN token packet to the USB device. After the USB device receives the IN token packet correctly, if the address matches a configured endpoint address, the USB module will access the corresponding USB_ADDRn_TX and USB_CNTn_TX registers according to the buffer description table entry of the endpoint, and store the values in these two registers to the internal 16-bit ADDR register and CNT register that cannot be accessed by the application. The ADDR register is used as a pointer to the endpoint's corresponding endpoint packet send buffer, and the CNT register is used to record the number of remaining untransferred bytes. The USB bus uses the low byte first method to read data from the endpoint data packet sending buffer. The data starts to read data from the endpoint data packet sending buffer pointed to by USB_ADDRn_TX, and the length is USB_CNTn_TX/2 words. If the data packet sent is an odd number of bytes, only the lower 8 bits of the last word are used.

After the USB device receives the PID IN token packet sent by the host, the USB processing flow for the IN transaction is as follows:

- If the device address information and endpoint information in this IN token packet are valid, and the status of the endpoint specified in the token packet is VALID, the USB device sends a PID DATA0 or DATA1 packet according to the USB_EPn.DATTOG_TX bit, send the prepared data to the host, when the last data byte is sent, the calculated data CRC will also be sent to the host. After the USB device receives the PID ACK handshake packet returned by the host. The hardware toggles the USB_EPn.DATTOG_TX bit, the hardware sets the endpoint's sending state to NAK state (USB_EPn.STS_TX = 10), and the hardware sets USB_EPn.CTRS_TX bit to generate a correct sending interrupt. The software responds to the CTRS_TX interrupt, identifies which endpoint the communication is on by checking the USB_STS.EP_ID bit, identifies the communication direction through USB_STS.DIR, clears the interrupt flag, and prepares the next data to be sent, and then the software sets the endpoint sending status to VALID status (USB_EPn.STS_TX = 11).
- If the endpoint specified in this IN token packet is invalid, the USB device does not send data packets, but sends PID NAK or STALL handshake packets according to USB_EPn.STS_TX.

28.4.4.3 OUT and SETUP transaction

When the host wants to send data or commands to the USB device, the host will send the PID OUT or SETUP token packet to the USB device. After the USB device receives the OUT or SETUP token correctly, if the address matches a configured endpoint address, the USB module will access the corresponding USB_ADDRn_RX and USB_CNTn_RX registers according to the buffer description table entry of the endpoint. Store the value of the USB_ADDRn_RX register into the internal ADDR register, and reset the internal CNT register at the same time. The ADDR register is used as a pointer to the endpoint data packet receiving buffer corresponding to the endpoint, and

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the CNT register is used to record the number of received data bytes, and initialize the internal 16-bit BUF_COUNT register that cannot be accessed by the application program with the BL_SIZE and NUM_BLK values in the USB_CNTn_RX register, which is used for buffer overflow detection. When the USB module receives data from the USB bus, the USB module organizes the received data in words (the first received is the low byte), and store it in the endpoint data packet receiving buffer pointed to by ADDR, at the same time, the CNT value is automatically incremented, and the BUF_COUNT value is automatically decremented.

After the USB device receives the PID OUT or SETUP token packet sent by the host, the USB processing flow for OUT or SETUP is as follows:

- If the device address information and endpoint information in the OUT or SETUP token packet are valid, and the status of the endpoint specified in the token packet is VALID, USB device moves data from the hardware buffer that cannot be accessed by the application to the endpoint data packet receiving buffer that can be accessed by the application. Then the USB device checks the received CRC. If the CRC is correct, the USB device replies to the host with a PID ACK handshake packet; If there is an error in the CRC or other error types (bit stuffing, frame error, etc.), the USB device will not reply to the host with an ACK handshake packet, and USB_STS.ERROR is set, at this time, the application does not need to do any processing, the USB device will automatically recover to be ready to receive the next transfer. If the received data size exceeds the data packet buffer size of the receiving endpoint, the USB device will stop receiving data, and the hardware will reply to the STALL handshake packet and set the buffer overflow error, but no interrupt will be generated. After the USB device replies the PID ACK handshake packet to the host, the USB device toggles the USB_EPn.DATTOG_RX bit by the hardware, the hardware sets the endpoint receiving state to NAK state (USB_EPn.STS_RX = 10), and the hardware sets USB_EPn.CTRS_RX to generate a correct receive interrupt. The software responds to the CTRS_RX interrupt, identifies the communication on which endpoint by checking the USB_STS.EP_ID bit, identifies the communication direction through USB_STS.DIR, clears the interrupt flag, processes the data received from the host, and after processing the received data, the software then sets the receiving state of the endpoint to the VALID state (USB_EPn.STS_RX = 11) to enable the next transmission.
- If the endpoint specified in this OUT or SETUP token packet is invalid, the USB device sends a PID NAK or STALL handshake packet according to USB_EPn.STS_RX.

Note:

1、When the USB device receives data from the host, if the size of the received data exceeds the size of the data packet buffer of the receiving endpoint, the hardware will automatically stop writing, that is, the data in the data packet buffer of other endpoints will never be overwritten.

28.4.4.4 Control transfer

Control transfer consists of 3 stages, 1 Setup stage + 0/multiple Data stages in the same direction + 1 Status stage. SETUP transaction can only be completed by the control endpoint, and the process of SETUP transaction and OUT transaction is similar. When a Setup transaction is completed correctly, the hardware generates a USB_EPn.CTRS_RX interrupt. In the interrupt, the software first changes the Tx and Rx direction states of the USB device endpoint to NAK, and then checks the USB_EPn.SETUP bit to determine whether it is a SETUP transaction or an OUT transaction. And according to the corresponding fields in the SETUP token packet, it is judged whether there is a data stage in the future, and if there is a Data stage, whether the Data stage is IN transmission or OUT transmission. As shown in Figure 28-5, take control write transfer as an example. Before enabling subsequent Data

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stages, determine whether the Data stage is the last Data stage:

- If it is not the last Data stage, that is, it is not the last data packet, before enabling the reception of OUT transactions, set the unused direction Tx status to STALL to prevent the host from prematurely ending the Data stage and entering the Status stage, the USB device can return a PID STALL handshake packet, and the Rx state of the direction to be used is set to VALID. When the first OUT transaction is completed correctly, the hardware generates the USB_EPn.CTRS_RX interrupt, and changes the Rx direction state of the USB device endpoint to NAK, the Tx direction state remains unchanged, the software judges whether the next OUT transaction to be enabled is the last Data stage in the interrupt. If it is not the last Data stage, before enabling the receiving OUT transaction, the software then sets the Rx direction status of the USB device endpoint to VALID, and the Tx direction status remains unchanged;
- If it is the last Data stage, before enabling the reception of the last OUT transaction, the software sets the Tx direction status that was not used in the previous Data stage to NAK, so that even if the host starts the Status stage immediately after the last Data stage, the USB device can still remain in the state of waiting for the end of the control transfer, and the Rx direction state is set to VALID, ready to receive the last packet of data;

After the last OUT transaction is completed correctly, the hardware generates the USB_EPn.CTRS_RX interrupt, and sets the Rx direction state of the USB device endpoint to NAK, and the TX direction state remains unchanged. When the software prepares the 0-length data packet that needs to be sent in the Status stage in the interrupt, the software changes the Tx direction status of the USB device endpoint to VALID.

Control read transfers are similar to control write transfers with the following differences:

- To control read transfer, after the last IN transaction in the Data stage is completed correctly, before enabling the Status stage in the OUT direction, in addition to setting the Rx direction status of the USB device endpoint to VALID, you also need to set STATUS_OUT (USB_EPn.EP_KIND) to 1, indicates that the next stage will be the Status stage in the OUT direction, and the subsequent OUT transaction must be a 0-length data packet, otherwise an error will be generated.
- After the Status stage is over, the software clears the STATUS_OUT (USB_EPn.EP_KIND) bit, the Rx direction status of the USB device endpoint is set to VALID, ready to receive a new command request, and the Tx direction status is set to NAK, indicating that before the next SETUP packet transmission is completed, the request for data transfer is not accepted.

Note:

1、 *Bidirectional endpoint 0 is used as the default control endpoint to handle control transfers.*

2、 *As defined in the USB2.0 specification, after the USB device receives the PID SETUP token packet, it cannot reply with the PID NAK or STALL handshake packet, but only with the PID ACK handshake packet. If the transmission of the SETUP packet fails, the next SETUP packet will be raised. If the Rx state of endpoint 0 is set to STALL or NAK, the USB module can still receive the SETUP token packet.*

3、 *When USB_EP0.CTRS_RX = 1, the USB module receives the SETUP token packet again, the USB module will discard the SETUP token packet, and will not reply any handshake packet to the host, forcing the host to send the SETUP token packet again.*

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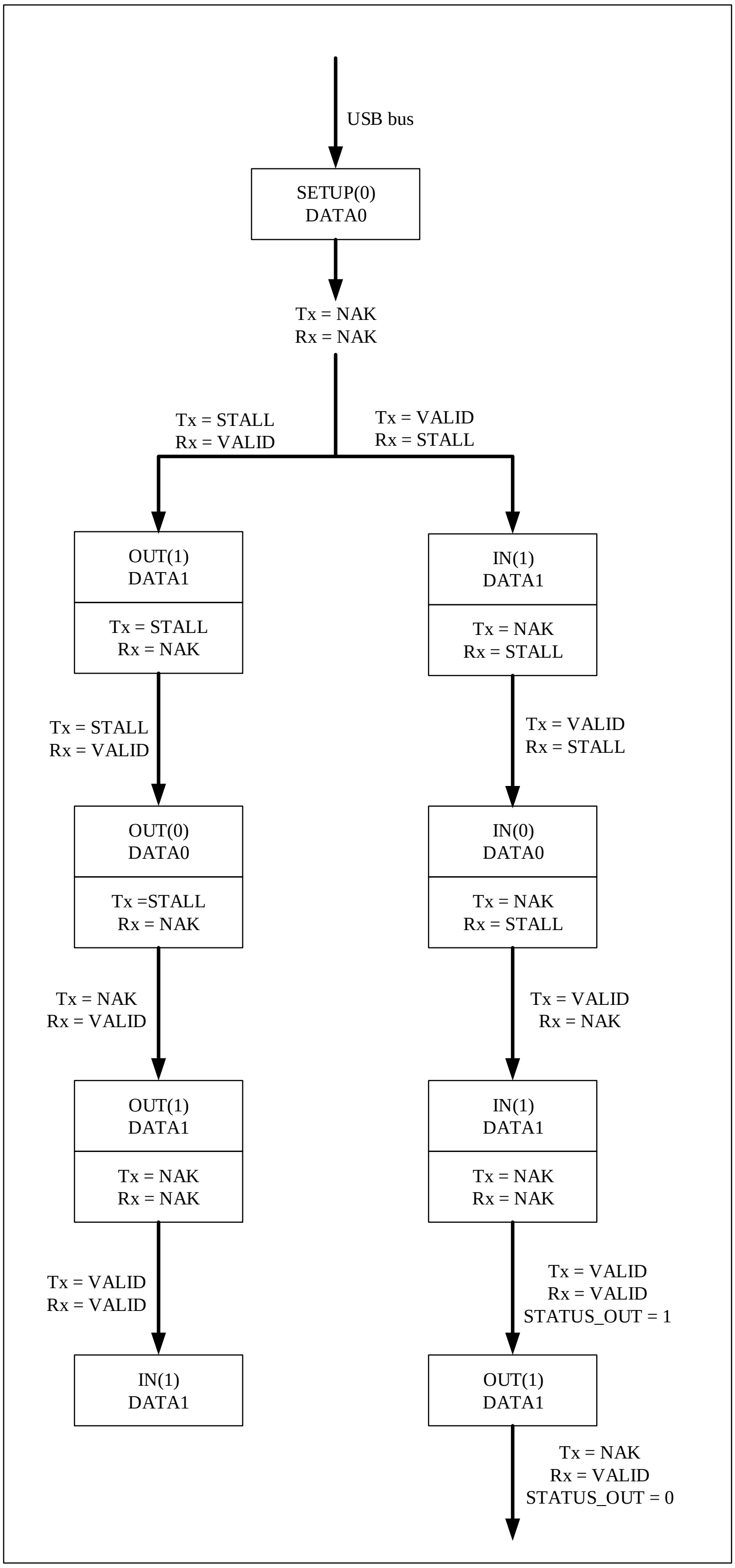
Figure 28-5 Control transfer



28.4.4.5 Isochronous transfer

Transmissions that require a fixed and precise data rate are defined as isochronous transfer. If an endpoint is defined as a isochronous endpoint during enumeration, the USB host will allocate the required bandwidth for the endpoint in

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each frame of transmission, but in order to save bandwidth, isochronous transfer does not have a retransmission mechanism, that is, there is no handshake stage, there is no handshake packet after the data packet, so there is no need to use the data toggle mechanism, and the isochronous transfer only transmits the PID DATA0 data packet.

The isochronous endpoint uses a double buffer mechanism to reduce the processing pressure of the application. The buffer used by the USB module is identified by the DATTOG bit. In the same register, the USB_EPn.DATTOG_RX bit identifies the receiving isochronous endpoint, and the USB_EPn.DATTOG_TX bit identifies the sending isochronous endpoint. Compared with the bulk double buffering mechanism, the isochronous double buffering mechanism has no SW_BUF, because the buffer that the application can access is the one not indicated by DATTOG, so to achieve bidirectional isochronous transmission, two USB_EPn registers need to be used. The use of double-buffered isochronous endpoints is shown in Table 28-3.

Table 28-3 How to use isochronous double buffering

Endpoint type	DATTOG	Buffer used by the USB module	Buffers used by the application
IN Endpoint	0	ADDRn_TX_0/CNTn_TX_0	ADDRn_TX_1/CNTn_TX_1
	1	ADDRn_TX_1/CNTn_TX_1	ADDRn_TX_0/CNTn_TX_0
OUT Endpoint	0	ADDRn_RX_0/CNTn_RX_0	ADDRn_RX_1/CNTn_RX_1
	1	ADDRn_RX_1/CNTn_RX_1	ADDRn_RX_0/CNTn_RX_0

The application initializes the DATTOG bits based on the buffer to be used the first time. Each time the transfer is completed, USB_EPn.CTRS_RX or USB_EPn.CTRS_TX is set according to the direction in which the transmission is enabled, and a corresponding interrupt is generated. If a CRC error or buffer overflow error occurs, the USB_EPn.CTRS_RX or USB_EPn.CTRS_TX interrupt event can still be triggered, but if it is a CRC error, the hardware will set the USB_STS.ERROR bit, indicating that the data may be corrupted. At the same time, the hardware toggles the DATTOG bit, but the USB_EPn.STS_RX or USB_EPn.STS_TX bits are not affected.

Isochronous endpoint definition: set USB_EPn.EP_TYPE = 10. Since the isochronous endpoint has no handshake mechanism, the status of the isochronous endpoint can only be set to VALID or DISABLED, and it is illegal to set it to STALL or NAK.

Note:

1、*Compared with bulk double buffering, since* isochronous *double buffering has no handshake mechanism,* isochronous *double buffering has no flow control mechanism.*

28.4.5 USB events and interrupts

Every USB behavior is initiated by the application and driven by USB interrupts or events. After a system reset, the application needs to wait for a series of USB interrupts and events.

28.4.5.1 Reset events

28.4.5.1.1 System reset and power-on reset

After a system reset or power-on reset occurs, the software first needs to enable the clock signal of the USB module, then clear the reset signal to access the registers of the USB module, and finally open the analog part connected to the USB transceiver. The software operation process is as follows:

- Enable the clock signal of the USB module

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- Clear the USB_CTRL.PD bit
- Wait for the internal reference voltage to stabilize, because it takes a start-up time to turn on the internal voltage, during which the USB transceiver is in an indeterminate state
- Clear the USB_CTRL.FRST bit
- Clear the USB_STS register, remove pending interrupts, and enable other units

Note:

1、 Every time the USB module is enabled after system reset or power-on reset, the pull-up resistor on the DP signal line needs to be configured. This control bit is located in bit25 of the base address 0x4000 1824 register. Set bit25 to 1 to enable the pull-up resistor on the DP signal line, otherwise disable the pull-up resistor. Modification of other bits of this register is not allowed.

28.4.5.1.2 USB reset (reset interrupt)

When a USB reset occurs, the state of the USB module is the same as after a system reset: all endpoints are disabled for communication. The software needs to do the following:

- After the reset interrupt is generated, the software must enable the transmission of endpoint 0 within 10ms
- Set the USB_ADDR.EFUC bit
- Initialize the USB_EP0 register and its associated endpoint packet buffer

28.4.5.2 Suspend and resume events

28.4.5.2.1 Suspend events

When full-speed USB is communicating normally, the host will send a PID SOF token packet every millisecond. If the USB module detects that 3 consecutive SOF packets are lost, that is, the USB bus is in an idle state within 3ms, the hardware sets the USB_STS.SUSPD bit, triggers a suspend interrupt, and the USB device enters the suspend state. The USB2.0 standard stipulates that in the suspend state, the average current consumption on the USB bus does not exceed 2.5mA, but self-powered devices do not need to strictly abide by this regulation.

Note:

1、 After the USB device enters the suspend state, it must still have the function of detecting the RESET signal.

28.4.5.2.2 Resume events

After the USB device enters the suspend state, to resume normal USB communication, the USB host can initiate a resume sequence or a reset sequence, or the USB device itself can trigger the resume sequence, but the resume sequence can only be ended by the USB host. If the reset sequence initiated by the USB host resumes the USB device, according to the regulations in the USB2.0 standard, it must be ensured that the resume process does not exceed 10ms.

Table 28-4 lists the USB_FN.RXDP_STS bit and the USB_FN.RXDM_STS bit to identify what triggers the resume event and the corresponding software action.

Table 28-4 Resume event detection

[USB_FN.RXDP_STS, USB_FN.RXDM_STS]	Wake-up event	Software operation
00	Root reset	None

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01	Root resume	None
10	None (noise on bus)	Go back in Suspend mode
11	Not allowed (noise on bus)	Go back in Suspend mode

Note:

1、The USB_CTRL.RESUM bit can only be set when USB_CTRL.FSUSPD = 1, i.e. the USB module is in suspend state.

28.4.5.3 USB interrupt

The USB controller has 3 interrupt lines, which are as follows:

- USB low priority interrupt (channel 21): can be triggered by all USB events;
- USB high-priority interrupt (channel 20): can only be triggered by correct transfer events for isochronous and double-buffered bulk transfers;
- USB resume interrupt (channel 42): triggered by a resume event from USB suspend mode.

28.4.6 Endpoint initialization

1. Initialize the USB_ADDRn_TX or USB_ADDRn_RX register, configure the endpoint Tx or Rx packet buffer start address;
2. According to the actual usage scenario of the endpoint, configure the USB_EPn.EP_TYPE bit and the USB_EPn.EP_KIND bit to set the endpoint type and buffer type;
3. Perform different operations based on the endpoint direction:
   - If it is a sending endpoint
   1) Set the USB_EPn.STS_TX bit to enable the sending function of the endpoint
   2) Configure the USB_CNTn_TX.CNTn_TX bit, set the endpoint data packet send buffer size
   - If it is a receiving endpoint
   1) Set the USB_EPn.STS_RX bit to enable the receiving function of the endpoint
   2) Configure the USB_CNTn_RX.BL_SIZE bit and the USB_CNTn_RX.NUM_BLK bit to set the endpoint packet receive buffer size

28.5 USB registers

The peripheral registers can be accessed by half-words (16-bit) or words (32-bit).

USB base address: 0x4000 5C00

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28.5.1 USB register overview

Table 28-5 USB register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	USB_EP0	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	USB_EP1	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	USB_EP2	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	USB_EP3	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	USB_EP4	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	USB_EP5	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	USB_EP6	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	USB_EP7	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	USB_CTRL	Reserved																CTRSM	PMAOM	ERRORM	WKUPM	SUSPDM	RSTM	SOFM	ESOFM	Reserved			RESUM	FSUSPD	LP_MODE	PD	FRST
	Reset Value																	0	0	0	0	0	0	0	0				0	0	0	1	1
044h	USB_STS	Reserved																CTRS	PMAO	ERROR	WKUP	SUSPD	RST	SOF	ESOF	Reserved			DIR	EP_ID[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0				0	0	0	0	0
048h	USB_FN	Reserved																RXDP_STS	RXDM_STS	LOCK	LSTSOF[1:0]		FN[10:0]										
	Reset Value																	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
04Ch	USB_ADDR	Reserved																Reserved									ADDR[6:0]						
	Reset Value																										0	0	0	0	0	0	0
050h	USB_BUFTAB	Reserved																BUFTAB[15:3]													Reserved		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0			

28.5.2 USB endpoint n register (USB_EPn), n=[0..7]

Address offset: 0x00 to 0X1C

Reset value: 0x0000 0000

31:16
Reserved

15	14	13:12	11	10:9	8	7	6	5:4	3:0
CTRS_RX	DATTOG_RX	STS_RX[1:0]	SETUP	EP_TYPE[1:0]	EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]	EPADDR[3:0]
rc_w0	t	t	r	rw	rw	rc_w0	t	t	rw

Bit Field	Name	Description
31：16	Reserved	Reserved, the reset value must be maintained.
15	CTRS_RX	Correct receive flag This bit is set by hardware when an OUT or SETUP transaction on this endpoint completes successfully. If USB_CTRL.CTRSM = 1, the corresponding interrupt will be generated. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.*
14	DATTOG_RX	Receive data PID toggle bit If the endpoint is not isochronous, this bit represents the toggle data bit (0 = DATA0, 1 = DATA1). Double-buffered endpoint, this bit is used to implement the flow control mechanism for double-buffered endpoints. Isochronous endpoint, this bit is used for double buffer exchange. *Note:* *1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.* *2、 Control endpoint, the hardware clears this bit after the USB module correctly receives the PID SETUP token packet.* *3、 In isochronous transfer, hardware toggles this bit just after the end of data packet reception.*
13：12	STS_RX[1:0]	Receive status This bit indicates the current state of the endpoint, Table 28-6 lists the available states

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<table>
<tr><th>Bit Field</th><th>Name</th><th>Description</th></tr>
<tr><td></td><td></td><td>of the endpoint. Hardware sets this bit to the NAK state when a correct OUT or SETUP transaction completes.
Note:
1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.
2、 Double-buffered bulk endpoint, which controls the transmission status according to the buffer status used, refer to section 28.4.3.
3、 Isochronous endpoint, the hardware will not change the state of the endpoint after the transaction is successfully completed</td></tr>
<tr><td>11</td><td>SETUP</td><td>SETUP transfer completion flag
This bit is set by hardware when the USB module correctly receives the PID SETUP token packet.
Note:
1、 Software can only read this bit, not write this bit.
2、 This bit USB_EPn.SETUP is only valid for control endpoints.</td></tr>
<tr><td>10：9</td><td>EP_TYPE[1:0]</td><td>Endpoint type
<table>
<tr><th>EP_TYPE[1:0]</th><th>Description</th></tr>
<tr><td>00</td><td>BULK: bulk endpoint</td></tr>
<tr><td>01</td><td>CONTROL: control endpoint</td></tr>
<tr><td>10</td><td>ISO: isochronous endpoint</td></tr>
<tr><td>11</td><td>INTERRUPT: interrupt endpoint</td></tr>
</table></td></tr>
<tr><td>8</td><td>EP_KIND</td><td>Endpoint special type
<table>
<tr><th colspan="2">EP_TYPE[1:0]</th><th>EP_KIND meaning</th></tr>
<tr><td>00</td><td>BULK</td><td>DBL_BUF: double buffered endpoint</td></tr>
<tr><td>01</td><td>CONTROL</td><td>STATUS_OUT</td></tr>
<tr><td>10</td><td>ISO</td><td>Undefined</td></tr>
<tr><td>11</td><td>INTERRUPT</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>7</td><td>CTRS_TX</td><td>Correct send flag
This bit is set by hardware when an IN transaction on this endpoint completes successfully. If USB_CTRL.CTRSM = 1, the corresponding interrupt will be generated.
Note:
1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.</td></tr>
<tr><td>6</td><td>DATTOG_TX</td><td>Send data PID toggle bit
If the endpoint is not isochronous, this bit represents the toggle data bit (0 = DATA0, 1 = DATA1).
Double-buffered endpoint, this bit is used to implement the flow control mechanism for double-buffered endpoints.
Isochronous endpoint, this bit is used for double buffer exchange.
Note:</td></tr>
</table>

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Bit Field	Name	Description
		1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit. *2、 Control endpoint, the hardware will set this bit after the USB module correctly receives the PID SETUP token packet.* *3、 In isochronous transfer, hardware toggles this bit just after the end of data packet transmission.*
5：4	STS_TX[1:0]	Send status This bit indicates the current state of the endpoint, Table 28-7 lists the available states of the endpoint. When a correct IN transaction completes, the hardware sets this bit to the NAK state. *Note:* *1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.* *2、 Double-buffered bulk endpoint, which controls the transmission status according to the buffer status used, refer to section 28.4.3.* *3、 Isochronous endpoint, the hardware will not change the state of the endpoint after the transaction is successfully completed.*
3：0	EPADDR[3:0]	Endpoint address This bit indicates the destination endpoint of the communication and must be written before enabling the corresponding endpoint.

Note:

1、 When the USB module receives the USB bus reset signal, or USB_CTRL.FRST = 1, the USB module will be reset. Except for the CTRS_RX and CTRS_TX bits that remain unchanged to process the following USB transfer, all other bits are reset.

Table 28-6 Receive status code

STS_RX[1:0]	Description
00	DISABLED: ignore all receive requests for this endpoint
01	STALL: the status of the handshake packet is STALL
10	NAK: the status of the handshake packet is NAK
11	VALID: endpoints can be used to receive

Table 28-7 Send status code

STS_TX[1:0]	Description
00	DISABLED: ignore all send requests for this endpoint
01	STALL: the status of the handshake packet is STALL
10	NAK: the status of the handshake packet is NAK
11	VALID: endpoints can be used to send

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28.5.3 USB control register (USB_CTRL)

Address offset: 0x40

Reset value: 0x0000 0003

31–16
Reserved

15	14	13	12	11	10	9	8	7–5	4	3	2	1	0
CTRSM	PMAOM	ERRORM	WKUPM	SUSPDM	RSTM	SOFM	ESOFM	Reserved	RESUM	FSUSPD	LP_MODE	PD	FRST
rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CTRSM	Correct transfer interrupt enable 0: Disable correct transfer interrupt 1: Enable correct transfer interrupt, when USB_STS.CTRS = 1, an interrupt is generated.
14	PMAOM	Packet buffer overflow/underflow interrupt enable 0: Disable packet buffer overflow/underflow interrupt 1: Enable packet buffer overflow/underflow interrupt, when USB_STS.PMAO = 1, an interrupt is generated.
13	ERRORM	Error interrupt enable 0: Disable error interrupt 1: Enable error interrupt, when USB_STS.ERROR = 1, an interrupt will be generated.
12	WKUPM	Wake-up interrupt enable 0: Disable wake-up interrupt 1: Enable wake-up interrupt, when USB_STS.WKUP = 1, an interrupt will be generated.
11	SUSPDM	Suspend mode interrupt enable 0: Disable suspend mode interrupt 1: Enable suspend mode interrupt, when USB_STS.SUSPD = 1, an interrupt will be generated.
10	RSTM	USB reset interrupt enable 0: Disable USB reset interrupt 1: Enable USB reset interrupt, when USB_STS.RST = 1, an interrupt will be generated.
9	SOFM	Start of frame interrupt enable 0: Disable start of frame interrupt 1: Enable start of frame interrupt, when USB_STS.SOF = 1, an interrupt will be generated.
8	ESOFM	Expected start of frame interrupt enable 0: Disable the expected start of frame interrupt

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Bit Field	Name	Description
		1: Enable the expected start of frame interrupt, when USB_STS.ESOF = 1, generate an interrupt.
7：5	Reserved	Reserved, the reset value must be maintained.
4	RESUM	Resume request 0: No resume request 1: Send a resume request to the PC host *Note:* *1、 If USB_CTRL.RESUM = 1 remains active for 1ms to 15ms, the PC host will implement a resume operation for the USB module.*
3	FSUSPD	Force suspend Software must set this bit when the USB_STS.SUSPD interrupt is triggered. 0: Suspend mode not entered 1: Enter suspend mode, but the clock and static power consumption of the USB analog transceiver are still present *Note:* *1、 To enter the low power consumption mode (bus powered device), the software must first set USB_CTRL.FSUSPD, and then set USB_CTRL.LP_MODE.*
2	LP_MODE	Low power mode 0: No effect 1: Enter low power mode in suspend mode. Activity on the USB bus (wake event) resets this bit (software can also reset this bit) *Note:* *1、 In low power mode, only the external pull-up resistor is used for power supply, and the system clock will also be stopped or reduced to a certain frequency to reduce power consumption.*
1	PD	Power-down mode 0: Exit power-down mode 1: Enter power-down mode *Note:* *1、 When USB_CTRL.PD = 1, the USB module is completely shut down, disconnected from the host, and the USB module will not work.*
0	FRST	Force USB reset 0: No effect 1: Reset the USB module, if USB_CTRL.RSTM = 1, a reset interrupt will be generated *Note:* *1、 When USB_CTRL.FRST = 1, the USB module will remain in reset state until software clears this bit.*

28.5.4 USB interrupt status register (USB_STS)

Address offset: 0x44

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Reset value: 0x0000 0000

31–16
Reserved

15	14	13	12	11	10	9	8	7–5	4	3–0
CTRS	PMAO	ERROR	WKUP	SUSPD	RST	SOF	ESOF	Reserved	DIR	EP_ID[3:0]
r	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0		r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CTRS	Correct transmission interrupt flag Set by hardware when the endpoint has completed a data transfer correctly. *Note:* *1、 Software can only read this bit, not write this bit.*
14	PMAO	Packet buffer overflow/underflow interrupt flag This bit is set by hardware when the packet buffer cannot hold all the transmitted data. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 This interrupt will not be generated during isochronous transfer.*
13	ERROR	Error interrupt flag Hardware sets this bit when the following errors occur: 1) No response, the host response timed out 2) CRC error, CRC check error in data or token packet 3) Bit stuffing error, bit stuffing error detected in PID, data or CRC 4) Frame format error, non-standard frame received *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, writing 1 is invalid.*
12	WKUP	Wake-up interrupt flag In the suspend state, when the wake-up signal is detected, the hardware sets this bit, and the hardware resets the USB_CTRL.LP_MODE bit at the same time. *Note:* 1、 *Software can read and write this bit, but only writing 0 is valid, writing 1 is invalid.*
11	SUSPD	Suspend mode interrupt flag This bit is set by hardware when there is no activity on the USB bus for more than 3ms, indicating a suspend request. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 In suspend mode, the USB hardware will not detect the suspend signal until the*

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Bit Field	Name	Description
		wake-up is over. *3、 After the USB is reset, the hardware will immediately enable the detection of the suspend signal.*
10	RST	USB reset interrupt flag This bit is set by hardware when a USB reset signal is detected. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 When the USB reset interrupt is generated, the address and endpoint registers of the device will be reset, but the configuration registers will not be reset unless cleared by software.*
9	SOF	Start of frame interrupt flag This bit is set by hardware when a PID SOF token packet is detected on the USB bus. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.*
8	ESOF	Expected start of frame interrupt flag This bit is set by hardware when the USB module does not receive the expected PID SOF token packet. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 When the USB module does not receive the PID SOF token packet for 3ms in a row, that is, 3 ESOF interrupts occur in a row, and a SUSPD interrupt will be generated.*
7：5	Reserved	Reserved, the reset value must be maintained.
4	DIR	Transmission direction 0: IN packet transfer is completed, and USB_EPn.CTRS_TX is set by hardware 1: OUT packet transfer is complete, and USB_EPn.CTRS_RX is set by hardware *Note:* *1、 Software can only read this bit, not write this bit.* *2、 When USB_EPn.CTRS_TX and USB_EPn.CTRS_RX are set at the same time, it indicates that there are OUT group and IN group at the same time.*
3：0	EP_ID[3:0]	Endpoint number After the USB module completes the data transmission and generates an interrupt, it is written by the hardware according to the endpoint number of the interrupt request. *Note:* *1、 Software can only read this bit, not write this bit.* *2、 When multiple endpoint requests are interrupted at the same time, the hardware writes the endpoint number with the highest priority. Isochronous endpoints and double-buffered bulk endpoints have high priority, other endpoints have low*

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Bit Field	Name	Description
		priority (the lower the endpoint number, the higher the priority).

28.5.5 USB frame number register (USB_FN)

Address offset: 0x48

Reset value: 0x0000 0XXX, X stands for undefined value

31–16
Reserved

15	14	13	12–11	10–0
RXDP_STS	RXDM_STS	LOCK	LSTSOF[1:0]	FNUM[10:0]
r	r	r	r	r

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	RXDP_STS	D+ status Represents the state of the USB D+ line, and can detect the occurrence of a resume condition in the suspend state.
14	RXDM_STS	D- status Represents the state of the USB D- line, and can detect the occurrence of a resume condition in the suspend state.
13	LOCK	Lock USB This bit is set by hardware if at least 2 PID SOF token packets are detected continuously after the end of an USB reset condition or after the end of an USB resume sequence. *Note:* *1、 When USB_FN.LOCK = 1, the frame counter will stop counting before the USB module is reset or the USB bus is suspended.*
12:11	LSTSOF[1:0]	Lost SOF flag The hardware increments this bit every time the USB_STS.ESOF event occurs, and once the PID SOF token packet is received, the hardware clears this bit.
10:0	FNUM[10:0]	Number of frames Hardware increments this bit every time the USB module receives a PID SOF token packet.

28.5.6 USB device address register (USB_ADDR)

Address offset: 0x4C

Reset value: 0x0000 0000

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31–16
Reserved

15–8	7	6–0
Reserved	EFUC	ADDR[6:0]
	rw	rw

Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	EFUC	USB module enable 0: The USB module stops working and does not respond to any USB communication 1: Enable USB module
6：0	ADDR[6:0]	USB device address This bit holds the address value assigned to the USB device by the USB host during enumeration. After a USB bus reset, this bit is reset to 0x00.

28.5.7 USB packet buffer description table address register (USB_BUFTAB)

Address offset: 0x50

Reset value: 0x0000 0000

31–16
Reserved

15–3	2–0
BUFTAB[12:0]	Reserved
rw	

Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:3	BUFTAB[12:0]	Buffer table This bit holds the starting address of the buffer description table. The buffer description table is used to indicate the address and size of the endpoint packet buffer of each endpoint, aligned by 8 bytes (the lowest 3 bits are 000).
2:0	Reserved	Reserved, the reset value must be maintained.

28.6 Buffer description table

The buffer description table is located in the packet buffer memory and is used to configure the address and size of the endpoint packet buffer shared by the USB module and the microcontroller core. Since the APB1 bus is addressed by 32 bits, the data packet buffer memory addresses use 32-bit aligned addresses, not the addresses used by the USB_BUFTAB register and the buffer description table.

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28.6.1 Send buffer address register n (USB_ADDRn_TX)

Address offset: [USB_BUFTAB] + n×16

USB local address: [USB_ BUFTAB] + n×8

15 … 1	0
ADDRn_TX[14:0]	-
rw	rw

Bit Field	Name	Description
15：1	ADDRn_TX[14:0]	Send buffer address The starting address of the endpoint packet buffer of the endpoint that needs to send data when the next PID IN token packet is received
0	-	Since packet buffer memory addresses are word (32-bit) aligned, this bit must be 0

28.6.2 Send data byte number register n (USB_CNTn_TX)

Address offset: [USB_ BUFTAB] + n×16 + 4

USB local address: [USB_ BUFTAB] + n×8 + 2

15 … 10	9 … 0
Reserved	CNTn_TX[9:0]
	rw

Bit Field	Name	Description
15:10	Reserved	Reserved, the reset value must be maintained.
9：0	CNTn_TX[9:0]	Number of bytes sent The number of data bytes to send on the next PID IN token packet

Note: As shown in Table 28-2 and Table 28-3, the double-buffered IN endpoint and the isochronous IN endpoint require two USB_CNTn_TX registers: USB_CNTn_TX_0 and USB_CNTn_TX_1.

31 … 26	25 … 16
Reserved	CNTn_TX_1[9:0]
	rw

15 … 10	9 … 0
Reserved	CNTn_TX_0[9:0]
	rw

28.6.3 Receive buffer address register n (USB_ADDRn_RX)

Address offset: [USB_ BUFTAB] + n×16 + 8

USB local address: [USB_ BUFTAB] + n×8 + 4

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15 … 1	0
ADDRn_RX[14:0]	-
rw	rw

Bit Field	Name	Description
15:1	ADDRn_RX[14:0]	Receive buffer address Endpoint packet buffer start address for the endpoint to hold data when the next PID SETUP or OUT token packet is received
0	-	Since packet buffer memory addresses are word (32-bit) aligned, this bit must be 0

28.6.4 Receive data byte number register n (USB_CNTn_RX)

Address offset: [USB_ BUFTAB] + n×16 + 12

USB local address: [USB_ BUFTAB] + n×8 + 6

15	14 … 10	9 … 0
BLSIZE	NUM_BLK[4:0]	CNTn_RX[9:0]
rw	rw	r

Bit Field	Name	Description
15	BLSIZE	Memory block size 0: The memory block size is 2 bytes 1: The memory block size is 32 bytes
14:10	NUM_BLK[4:0]	Number of memory blocks Records the number of memory blocks allocated to the endpoint packet receive buffer and determines the size of the endpoint packet receive buffer that is ultimately used. For details, please refer to the following Table 28-8.
9:0	CNTn_RX[9:0]	Number of bytes received Written by the USB module to record the actual number of bytes of the latest PID SETUP or OUT token packet received by the endpoint.

Note: As shown in Table 28-2 and Table 28-3 double buffered OUT endpoints and isochronous OUT endpoints require two USB_CNTn_RX registers: USB_CNTn_RX_0 and USB_CNTn_RX_1.

31	30 … 26	25 … 16
BLSIZE_1	NUM_BLK_1[4:0]	CNTn_RX_1[9:0]
rw	rw	r

15	14 … 10	9 … 0
BLSIZE_0	NUM_BLK_0[4:0]	CNTn_RX_0[9:0]
rw	rw	r

Table 28-8 Endpoint packet receive buffer size definition

NUM_BLK[4:0]	BLSIZE = 0	BLSIZE = 1
00000	Not allowed	32 bytes
00001	2 bytes	64 bytes

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NUM_BLK[4:0]	BLSIZE = 0	BLSIZE = 1
00010	4 bytes	96 bytes
00011	6 bytes	128 bytes
…	…	…
01111	30 bytes	512 bytes
10000	32 bytes	Reserved
10001	34 bytes	Reserved
10010	36 bytes	Reserved
…	…	…
11110	60 bytes	Reserved
11111	62 bytes	Reserved

Note:

1、 *The size of the endpoint packet receive buffer is defined during the device enumeration process and is defined by the wMaxPacketSize field of the standard endpoint descriptor in the USB 2.0 protocol specification.*

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29 Debug support (DBG)

29.1 Overview

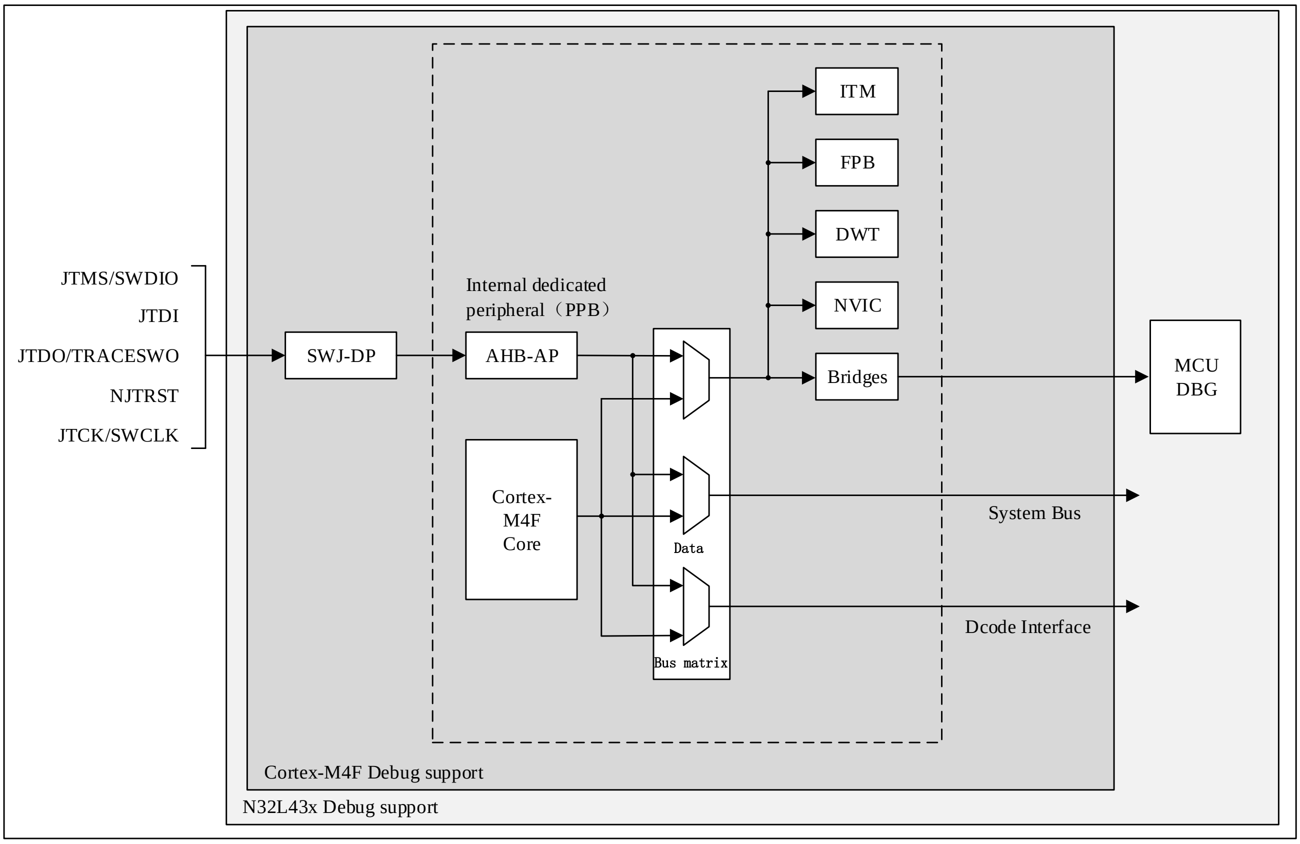
N32L43x uses Cortex^{TM}-M4F core, which integrates hardware debugging module. Support instruction breakpoint (stop when instruction fetches value) and data breakpoint (stop when data access). When the kernel is stopped, the user can view the internal state of the kernel and the external state of the system. After the user's query operation is completed, the kernel and peripherals can be restored, and the corresponding program can continue to be executed.

The hardware debugging module of the N32L43x core can be used when it is connected to the debugger (when it is not disabled).

N32L43x supports the following debugging interfaces:

- Serial interface
- JTAG debugging interface

Figure 29-1 N32L43x level and Cortex^{TM}-M4F level debugging block diagram



The ARM Cortex^{TM}-M4F core hardware debugging module can provide the following debugging functions:

- SWJ-DP: serial /JTAG debug port
- AHP-AP: AHB access port

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- ITM: execution tracking unit
- FPB: Flash instruction breakpoint
- DWT: data trigger

Reference:

- Cortex^{TM}-M4 Technical Reference Manual (TRM)
- ARM debugging interface V5 structure specification
- ARM CoreSight development tool set (r1p0 version) technical reference manual

The system supports low-power mode debugging and debugging of some peripherals. The peripherals supporting debugging include: CAN, I2C, TIMER, WWDG and IWDG modules. The user needs to set the corresponding bit of the debug control register (DBG_CTRL) to 1 when debugging with low power consumption or peripherals.

29.2 JTAG/SWD function

The debugging tool can call the debugging function through the SWD debugging interface or JTAG debugging interface mentioned above.

29.2.1 Switch JTAG/SWD interface

The chip uses JTAG debug interface by default. If you need to switch the debug interface, you can switch between SWD interface and JTAG interface through the following operations:

JTAG debug to SWD debug switch:

1. Send JTMS = 1 signal with more than 50 JTCK cycles;
2. Send 16-bit JTMS = 1110011110011110(0xE79E LSB) signal;
3. Send JTMS = 1 signal with more than 50 JTCK cycles.

Switch from SWD debugging to JTAG debugging:

1. Send JTMS = 1 signal with more than 50 JTCK cycles;
2. Send 16-bit JTMS = 1110011100111100(0xE73C LSB) signal;
3. Send JTMS = 1 signal with more than 50 JTCK cycles.

29.2.2 Pin allocation

JTAG debugging interface includes five pins: JTCK (JTAG clock pin), JTMS (JTAG mode selection pin), JTDI (JTAG data input pin), JTDO (JTAG data output pin) and NJTRST (JTAG data reset pin, low level reset pin).

SWD (serial debugging) interface includes two pins: SWCLK (clock pin) and SWDIO (data input and output pin), which provide the interface of two pins: data input and output pin (SWDIO) and clock pin (SWCLK).

See the following Table for the pin allocation of JTAG debugging interface and SWD debugging interface (SWDIO is alternated with JTMS, SWCLK is alternated with JTCK):

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Table 29-1 Debug port pin

Debug port	Pin allocation
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

- When both JTAG debugging interface and SWD debugging interface are enabled, the 5-wire JTAG debugging interface will be used by default after reset.
- When using JTAG interface, users can not use NJTRST pin. In this case, NJTRST pin (PB4, internal hardware pull-up) can be used as a general-purpose GPIO.
- When SWD interface is used, three pins JTDI (PA15), JTDO (PB3) and NJTRST (PB4) can be used as general GPIO.
- When the debugging function is not used, the above five pins can be used as general-purpose GPIO.

29.3 MCU debug function

29.3.1 Low-power mode debug support

N32L43x provides various low-power modes (See chapter Power control (PWR) for details). By default, if the MCU enters SLEEP, STOP2, or STANDBY mode while the application is using the debug feature, the debug connection will be lost. When debugging, make sure that the FCLK and HCLK of the core are turned on, and provide the necessary clock for the core debugging. Users can perform software debugging in low power mode according to specific operations.

To do this, a debugger or software first needs to configure the debug control registers associated with the low power modes:

- DBG_SLEEP mode:

  The DBG_CTRL.SLEEP bit needs to be configured to provide HCLK with the same clock as provided to FCLK (ie: the original configured system clock).

- DBG_STOP mode:

  The DBG_CTRL.STOP bit needs to be configured to start the internal RC oscillator to provide the clock for HCLK and FCLK.

- DBG_STANDBY mode:

  The DBG_CTRL.STDBY bit needs to be configured to start the internal RC oscillator to provide the clock for HCLK and FCLK.

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29.3.2 Peripherals debug support

When the corresponding bit of the peripheral control bit in the DBG_CTRL register is set to 1, the corresponding peripheral enters the debugging state after the core stops:

- Timer peripheral: the timer counter stops and debugs.
- I2C peripheral: the SMBUS of I2C keeps the state and carries out debugging.
- WWDG/IWDG peripheral: WWDG/IWDG counter clock stops and debugs.
- CAN peripheral: the CAN interface receiving register stops counting and debugs.

29.4 DBG registers

29.4.1 DBG register overview

The DBG register map and reset values are listed below. These peripheral registers must be operated as words (32 bits). The base address of the register is 0xE0042000.

Table 29-2 DBG register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DBG_ID	SRAM[3:0]				SER_NUM[3:0]				DEV_NUM_L[3:0]				FLASH[3:0]				DEV_NUM_H[3:0]				DEV_NUM_M[3:0]				REV_NUM_H[3:0]				REV_NUM_L[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
004h	DBG_CTRL	Reserved										TIM9_STOP	TIM7_STOP	TIM6_STOP	TIM5_STOP	TIM8_STOP	I2C2SMBUS_TIMEOUT	I2C1SMBUS_TIMEOUT	CAN_STOP	TIM4_STOP	TIM3_STOP	TIM2_STOP	TIM1_STOP	WWDG_STOP	IWDG_STOP	Reserved					STDBY	STOP	SLEEP
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0						0	0	0

29.4.2 ID register (DBG_ID)

31-28	27-24	23-20	19-16
SRAM[3:0]	SER_NUM[3:0]	DEV_NUM_L[3:0]	FLASH[3:0]
r		r	r

15-12	11-8	7-4	3-0
DEV_NUM_H[3:0]	DEV_NUM_M[3:0]	REV_NUM_H[3:0]	REV_NUM_L[3:0]
r	r	r	r

Address offset: 0x00

Only 32-bit access is supported, fixed values cannot be modified.

Bit field	**Name**	**Description**
31:28	SRAM[3:0]	SRAM capacity indication bit (capacity: (N+1)*8K).

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Bit field	Name	Description
27:24	SER_NUM[3:0]	Series type indication bit. 1 is G series, 2 is L series.
23:20	DEV_NUM_L[3:0]	Lower 4 digits of equipment model. Device model consists of 12 bits, including high, medium and low, representing the model of MCU.
19:16	FLASH[3:0]	FLASH capacity indicator (capacity: N*32K).
15:12	DEV_NUM_H[3:0]	The upper 4 bits of device. See the description of DEV_NUM_L[3:0].
11:8	DEV_NUM_M[3:0]	The middle 4 bits of device. See the description of DEV_NUM_L[3:0].
7:4	REV_NUM_H[3:0]	High 4 bits of MCU version number
3:0	REV_NUM_L[3:0]	Low 4 bits of MCU version number

29.4.3 Debug control register (DBG_CTRL)

Address offset: 0x04

POR reset value: 0x0000 0000 (not reset by system reset)

31-22	21	20	19	18	17	16
Reserved	TIM9_STOP	TIM7_STOP	TIM6_STOP	TIM5_STOP	TIM8_STOP	I2C2SMBUS_TIMEOUT
	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7-3	2	1	0
I2C1SMBUS_TIMEOUT	CAN_STOP	TIM4_STOP	TIM3_STOP	TIM2_STOP	TIM1_STOP	WWDG_STOP	IWDG_STOP	Reserved	STDBY	STOP	SLEEP
rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw

Bit field	Name	Description
31:22	Reserved	Reserved, must keep the reset value.
21:17	TIMx_STOP	TIMx debug pause bit (x = 9, 7, 6, 5, 8). Set or cleared by software. 0: TIMx running state has no effect. 1: Pause the counter of TIMx.
16:15	I2CxSMBUS_TIMEOUT	I2Cx SMBUS timeout controls debug pause bits (x = 2, 1). Set or cleared by software. 0: SMBUS timeout control has no effect. 1: Pause SMBUS timeout control.
14	CAN_STOP	CAN debug pause bit. Set or cleared by software. 0: CAN running state has no effect. 1: Pause the receive function of the CAN receive register.
13:10	TIMx_STOP	TIMx debug pause bits (x = 4, 3, 2, 1). Set or cleared by software. 0: TIMx running state has no effect. 1: Pause the counter of TIMx.

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Bit field	Name	Description
9	WWDG_STOP	WWDG debug pause bit. Set or cleared by software. 0: WWDG running state has no effect. 1: Pause the WWDG counter.
8	IWDG_STOP	IWDG debug pause bit. Set or cleared by software. 0: IWDG running state has no effect. 1: Pause the IWDG counter.
7:3	Reserved	Reserved, must keep the reset value.
2	STDBY	DBG_STANDBY mode. Set or cleared by software. 0: (FCLK off, HCLK off) The entire digital circuit section is powered down. From a software point of view, exiting STANDBY mode is the same as a reset (except that some status bits indicate that the microcontroller has just exited from STANDBY state). 1: (FCLK on, HCLK on) The digital circuit part is not powered off, and the FCLK and HCLK clocks are clocked by the internal RC oscillator (MSI). In addition, the microcontroller exits STANDBY mode by generating a system reset is the same as a reset.
1	STOP	DBG_STOP mode. Set or cleared by software. 0: (FCLK off, HCLK off) In STOP2 mode, the clock controller disables all clocks (including HCLK and FCLK). When exiting STOP2 mode, the configuration of the clock is the same as before entering STOP2 mode. 1: (FCLK on, HCLK on) In DBG_STOP2 mode, the FCLK and HCLK clocks are provided by the internal RC oscillator (MSI). When exiting STOP2 mode, the software does not need to reconfigure the clock system to start the PLL, crystal oscillator, etc., and the held registers will not be reset (same operation as configuring this bit to 0).
0	SLEEP	DBG_SLEEP mode. Set or cleared by software. 0: (FCLK on, HCLK off) In SLEEP mode, FCLK is provided by the previously configured system clock, and HCLK is off. Since SLEEP mode does not reset the configured clock system, software does not need to reconfigure the clock system when exiting from SLEEP mode. 1: (FCLK on, HCLK on) In DBG_SLEEP mode, both FCLK and HCLK clocks are provided by the previously configured system clock.

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30 Unique device serial number (UID)

30.1 Introduction

MCU series products have two built-in unique device serial numbers with different lengths, namely 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory, and the information is programmed during manufacture, and any MCU microcontroller is guaranteed to be unique under any circumstances. It can be read by user applications or external devices through CPU or SWD interface and cannot be modified.

UID is 96 bits, which is usually used as serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory, and it can also be used to activate Secure Bootloader with security function.

UCID is 128 bits and complies with the definition of the Nations Technologies chip serial number. It contains information about chip production and version.

30.2 UID register

Start address: 0x1FFF_F7F0, 96 bits in length.

30.3 UCID register

Start address: 0x1FFF_F7C0, 128 bits in length.

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31 Version history

Date	Version	Modify
2022.07.08	V2.0	Initial version.
2022.09.05	V2.1	1. Add RTC OUT(PC13) duty cycle description 2. Add PB3 description in Debug mode at chapter 5.2.2 3. Add MCO output LSE duty cycle at chapter 4.2.13 4. 3.2.3 Chapter LPRUN mode supports CAN/ADC 5. Modify BOR_LEVEL0 in chapter 2.2.4.7 6. Delete RTC periodic wake-up support Standby mode 7. 4.2.6 Chapter LSE clock add switch wait clock 8. Modify USART3 mode setting in table 24-8 9. Modify SRAM capacity calculation formula in chapter 28.4.2 10. Modify the WWDG T register to 7 bit in chapter 16.7.2
2023.02.10	V2.2	1. Add note 1 to MSI clock in chapter 4.2.4 2. Add note 1 to HSI clock in chapter 4.2.3 3. Add note to RTC initialization in chapter 14.3.6 4. Modify figure I2S clock generator structure in chapter 24.4.2 5. Add “don’t set the slave address to 0xF0” in chapter 23.3.2.6 6. Add Clock Tree Figure note: When PLL is selected as system clock source, PLL minimum clock output is 32MHz

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