N32G455xB/xC/xE Product Brief

N32G455 series uses a 32-bit ARM Cortex-M4 core with a maximum operating frequency of 144MHz, supporting floating point unit and DSP instructions, integrating up to 512KB Flash,144KB SRAM, and built-in four 12bit 5Msps ADC. four independent rail-to-rail operational amplifiers, seven high-speed comparators, two 1Msps 12bit DAC, integrated multi-channel U(S)ART, I2C, SPI, QSPI, USB, CAN, SDIO communication interface, Built-in cryptographic algorithm hardware acceleration engine

Main features

- **CPU core**
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply and divide instructions, support DSP instructions and MPU
  - Built-in 8KB instruction Cache, support Flash acceleration unit execution program 0 wait
  - Run up to 144MHz, 180DMIPS
- **Memory**
  - Up to 512KByte embedded Flash memory, support encrypted storage, partition management and data protection, support hardware ECC verification, 100,000 erasing times, 10 years data retention
  - 144KByte embedded SRAM (including 16KByte Retention RAM), supporting hardware parity check
- **High-performance analog interface**
  - 4x 12bit 5Msps high-speed ADCs, available in 12/10/8/6 bit mode, sampling rate up to 9Msps in 6bit mode and up to 38 external single-ended input channels, supporting differential mode
  - 4x rail-to-rail operational amplifiers with built-in programmable gain amplification up to 32 times
  - Up to 7x high-speed analog comparators with built-in 64 level adjustable comparison datum
  - 2x 12bit DAC, sampling rate 1Msps
  - Support external input independent reference voltage source
  - All analog interfaces support full voltage from 1.8 to 3.6V
- **Clock**
  - 4MHz~32MHz external high-speed crystal
  - 32.768KHz external low-speed crystal
  - Internal high-speed RC 8MHz
  - Internal low-speed RC 40KHz
  - Built-in high-speed PLL

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- Supports one-way clock output, which can be configured with system clock, HSE, HSI, or PLL frequency division output

- **Reset**
  - Supports power on, power down, brown-out and external pin reset
  - Support watchdog reset, software reset
- **Up to 80 GPIOs with multiplexing function. The maximum flip speed is 50MHz. Most GPIO supports 5V voltage resistance.**
- **Communication interface**
  - 7x U(S)ART interfaces with speeds up to 4.5Mbps, including 3x USART interfaces (supporting ISO7816, IrDA, LIN) and 4x UART interfaces
  - 3x SPI interfaces with speeds up to 36MHz, two of which support I2S
  - 1x QSPI interface with speeds up to 144Mbps
  - 4x I2C interfaces with speeds up to 1MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 1x USB2.0 Full Speed Device port
  - 2x CAN 2.0B bus interfaces
  - 1x SDIO interface, supporting SD/MMC format
- **2x high-speed DMA controllers, each controller supports 8 channels, channel source address and destination address can be arbitrarily configurable**
- **RTC real-time clock, support leap year perpetual calendar, alarm clock event, periodic wake up, support internal and external clock calibration**
- **Timing counter**
  - 2x 16bit advanced timer counters, support input capture, complementary output, orthogonal coding input and other functions, the highest control accuracy of 6.9ns;Each timer has four independent channels, three of which support 6 complementary PWM output
  - 4x 16bit general timer counters, each timer has four independent channels, support input capture/output comparison /PWM output
  - 2x 16bit basic timer counters
  - 1x 24bit SysTick
  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming mode**

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- Support SWD/JTAG online debugging interface
- Support UART and USB Bootloader

- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Supports AES, DES, SHA, SM1, SM3, SM4, SM7, and MD5 algorithms
  - Flash Storage encryption, Multi-user Partition Management (MMU)
  - TRNG true random number generator
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support security startup, program encryption download, security updates
  - Support clock failure detection, anti-disassembly detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - LQFP64(10mm x 10mm)
  - LQFP80(12mm x 12mm)
  - LQFP100(14mm x 14mm)
  - LQFP128(14mm x 14mm)
- **Order model**

Series	Model
N32G455xB	N32G455CBL7,N32G455RBL7,N32G455MBL7,N32G455VBL7
N32G455xC	N32G455CCL7,N32G455RCL7,N32G455MCL7,N32G455VCL7
N32G455xE	N32G455CEQ7,N32G455REL7,N32G455MEL7,N32G455VEL7

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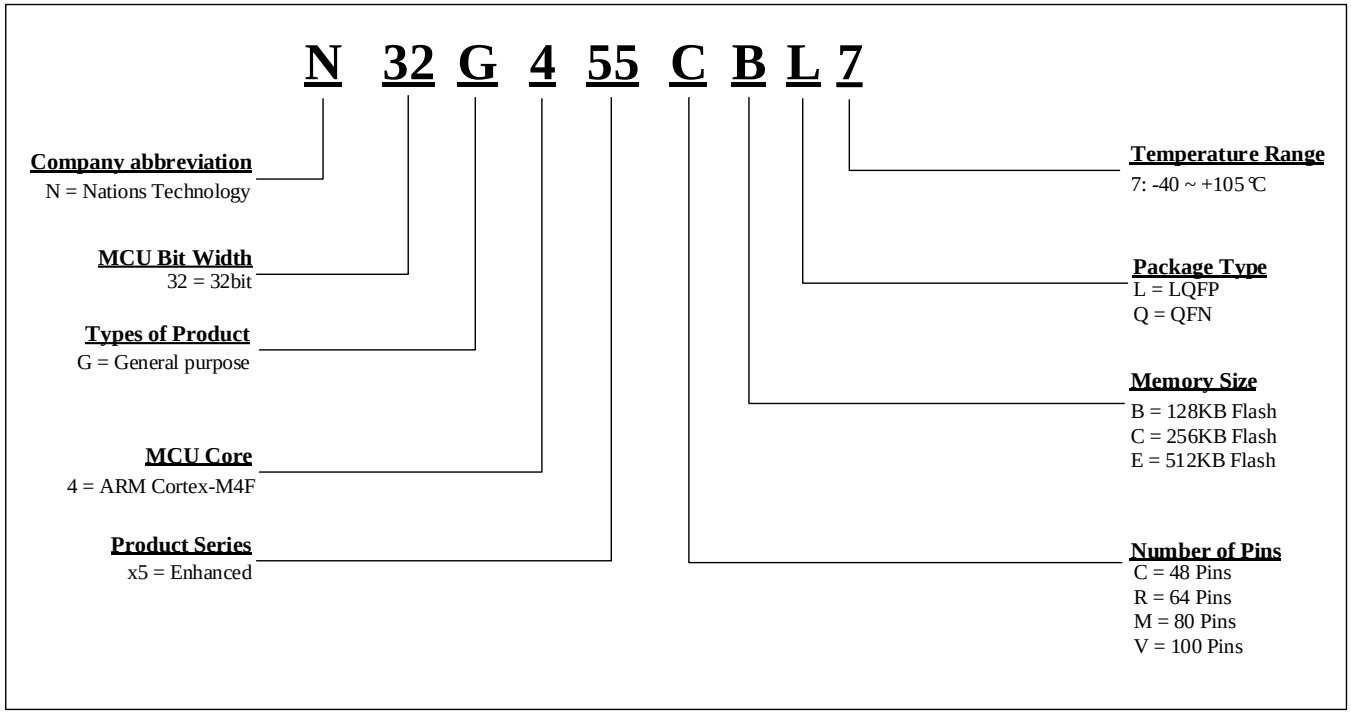
1 Naming rules



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2 Product Model Resource configuration

Device type		N32G455CB/C/E			N32G455RB/C/E			N32G455MB/C/E			N32G455VB/C/E		
Flash size（KB）		128	256	512	128	256	512	128	256	512	128	256	512
SRAM size（KB）		80	144	144	80	144	144	80	144	144	80	144	144
CPU frequency		ARM Cortex-M4 @144MHz,180DMIPS											
Work environment		1.8~3.6V/-40~105℃											
Timer	General	4											
	Advanced	2											
	Basic	2											
Communication Interface	SPI	3											
	I2S	2											
	QSPI	Only Single Wire		1									
	I2C	3			4								
	USART	3											
	UART	3	4		4								
	USB	1	No		1								
	CAN	2											
	SDIO	No		1									
GPIO		37	42		51			65			80		
DMA		2											
Number of Channels		16Channel											
12bit ADC		4			4			4			4		
Number of channels		16Channel			22Channel			33Channel			38Channel		
12bit DAC		2											
Number of channels		2Channel											
OPA/COMP		4/5	4/7		4/7			4/7			4/7		
Algorithm support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG											
Security protection		Read/write protection（RDP/WRP）, storage encryption, partition protection, secure startup											
Package		LQFP48	QFN48		LQFP64			LQFP80			LQFP100		

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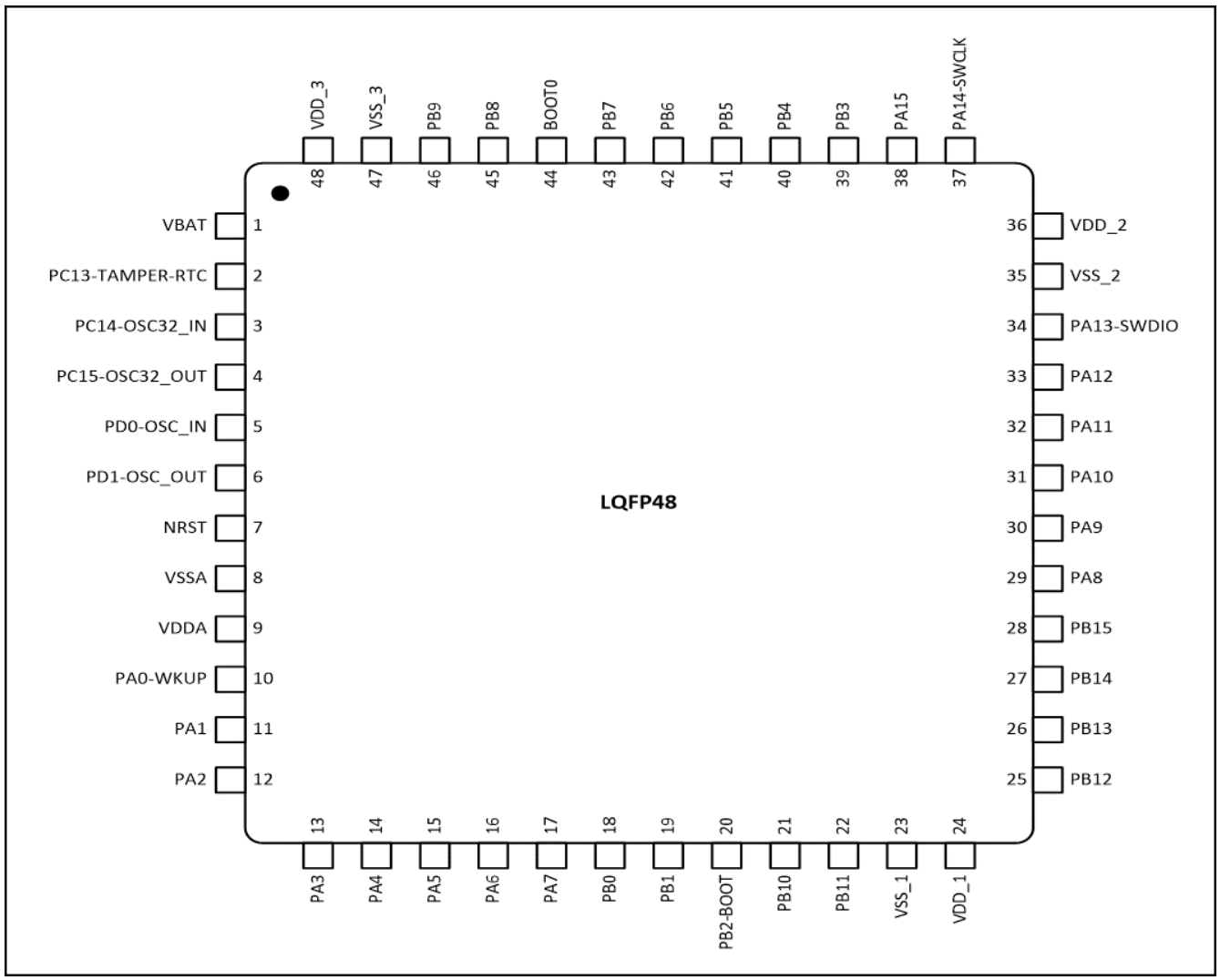
3 Package

3.1 LQFP48 package

3.1.1 LQFP48 pin distribution



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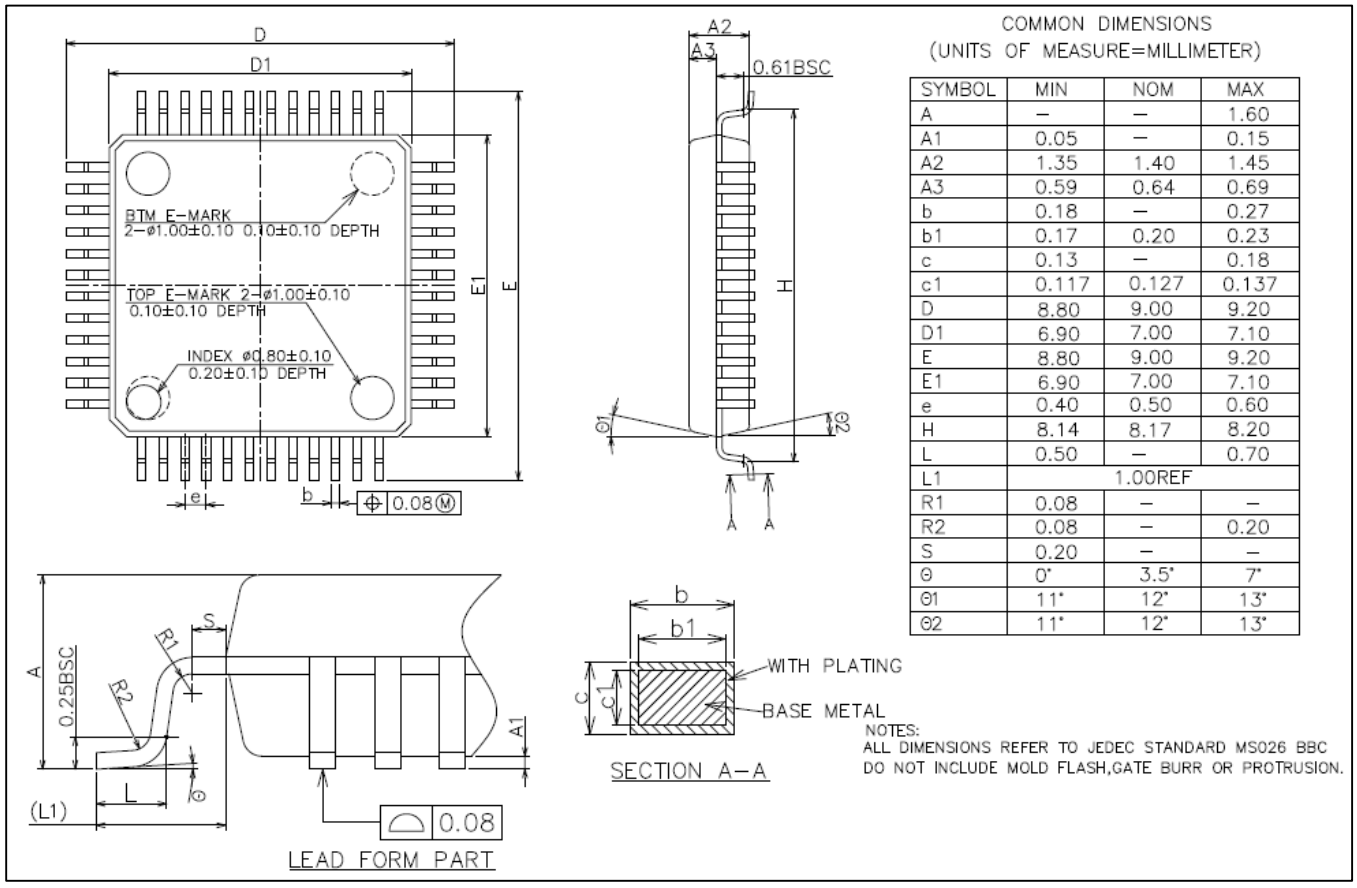
3.1.2 LQFP48 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1	1.00REF		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBC
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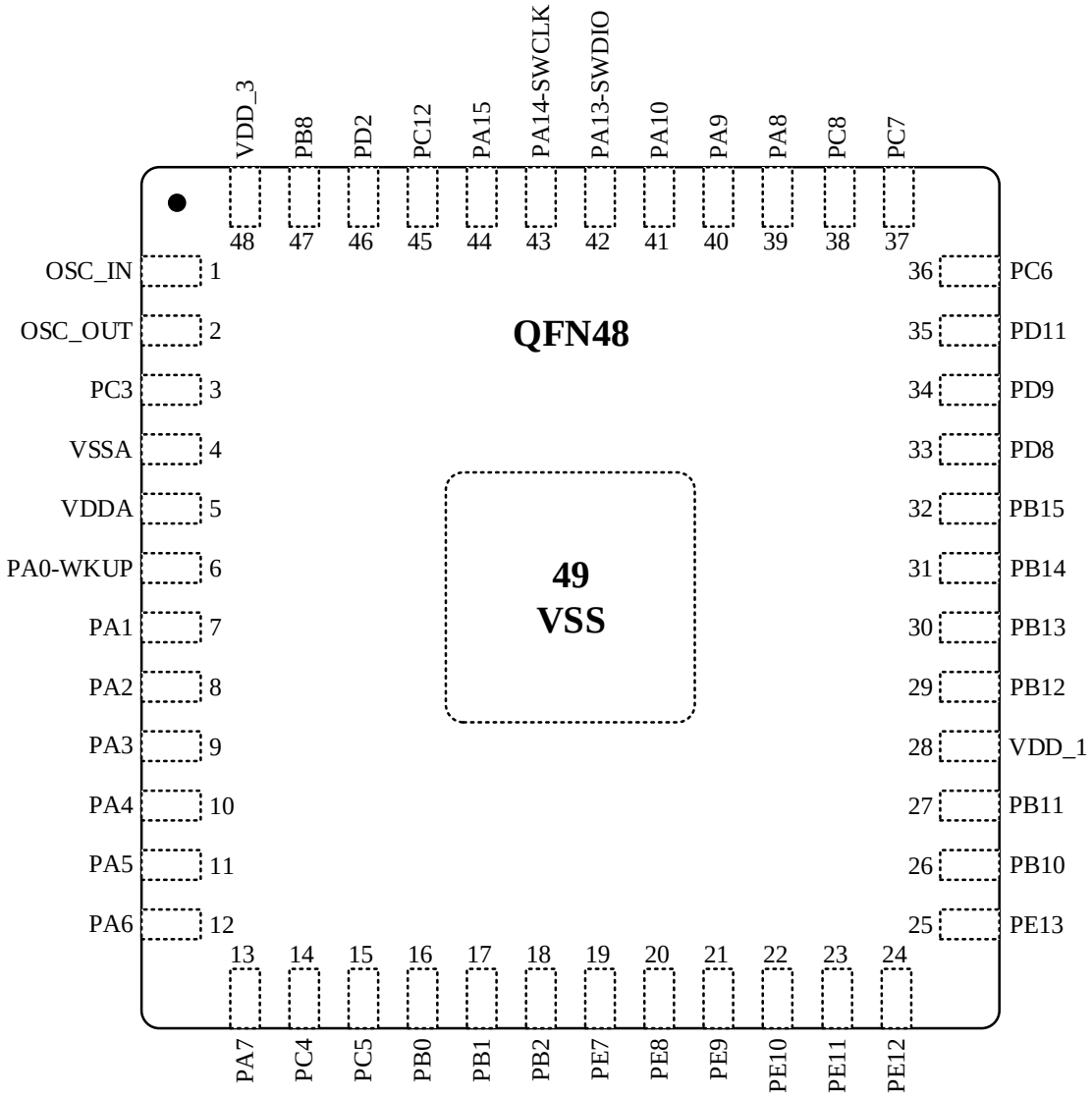
3.2 QFN48 package

3.2.1 QFN48 pin distribution



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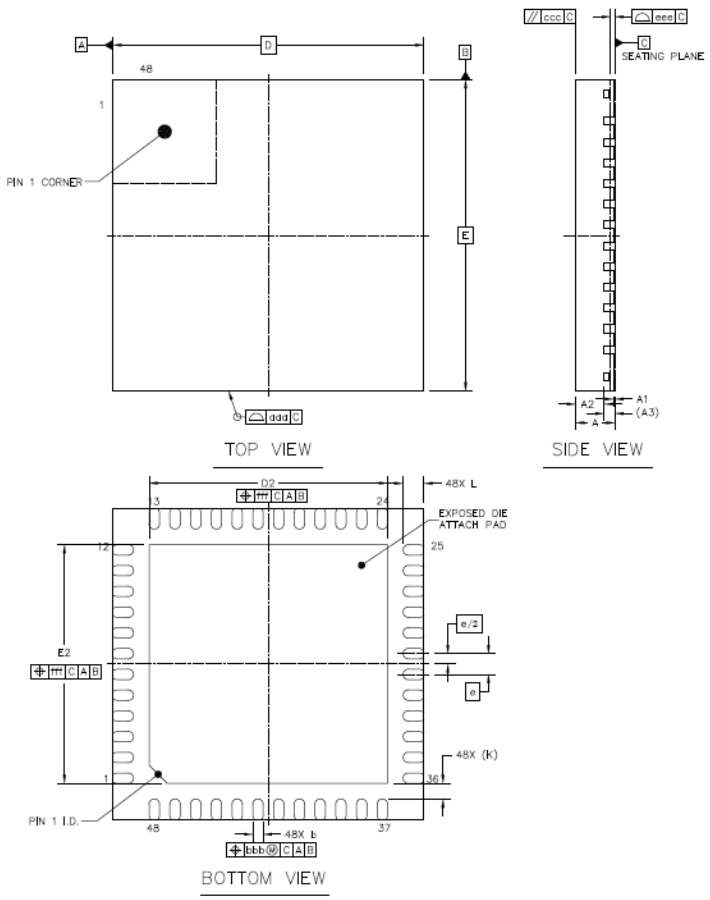
3.2.2 QFN48 package size



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.5	4.6	4.7
	Y	E2	4.5	4.6	4.7
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP *Sn8~20s

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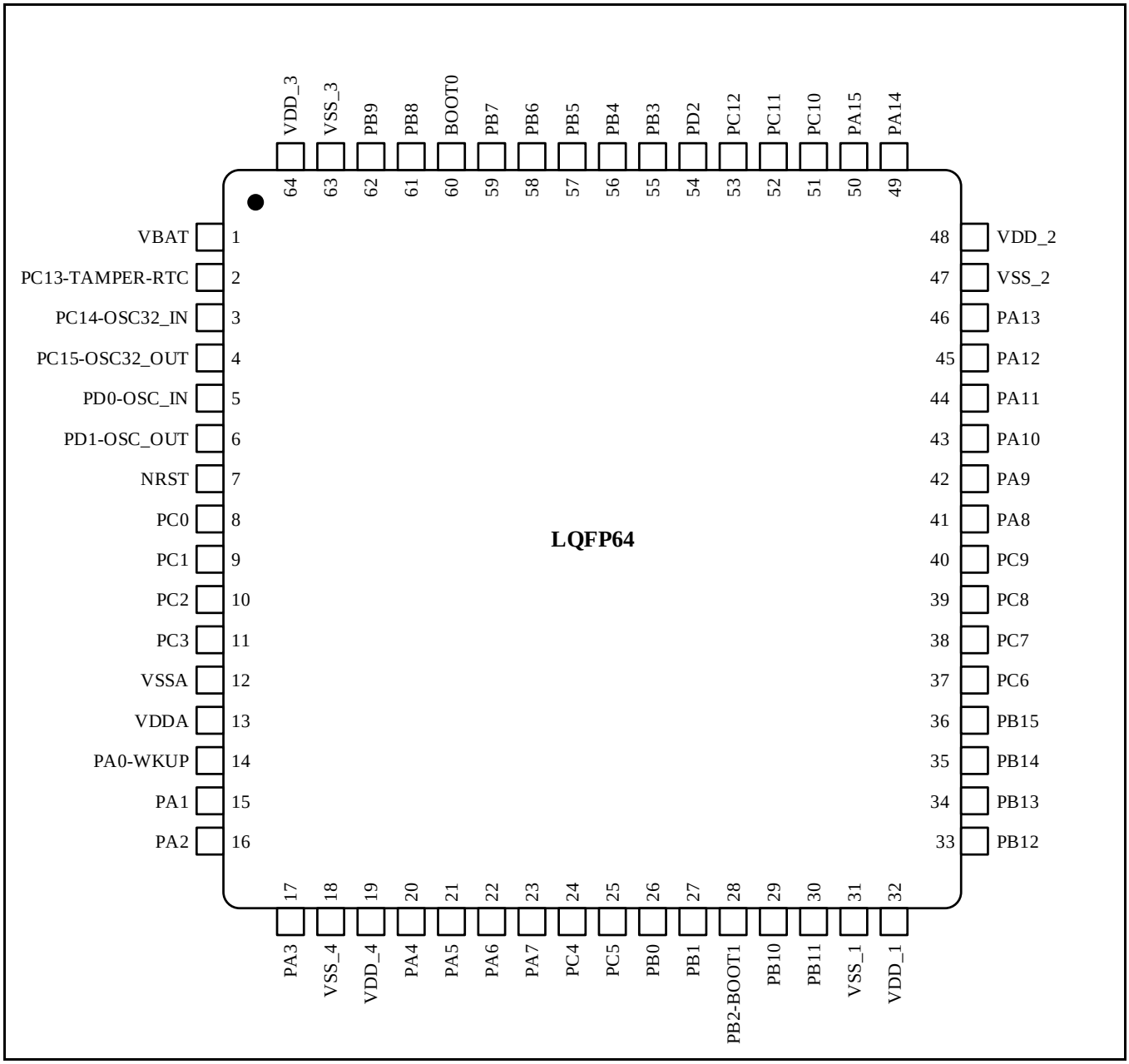
3.3 LQFP64 package

3.3.1 LQFP64 pin distribution



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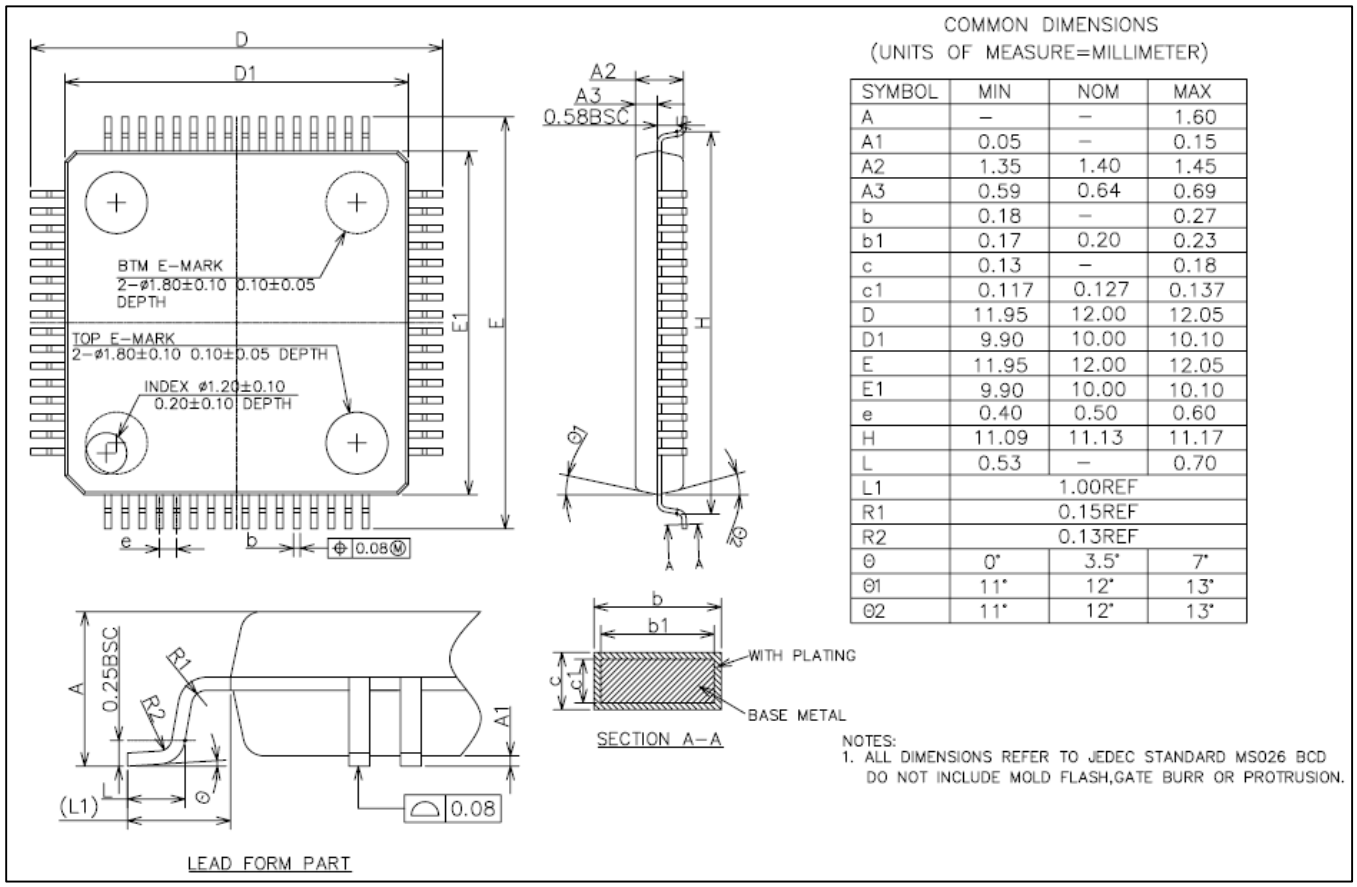
3.3.2 LQFP64 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1		1.00REF	
R1		0.15REF	
R2		0.13REF	
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
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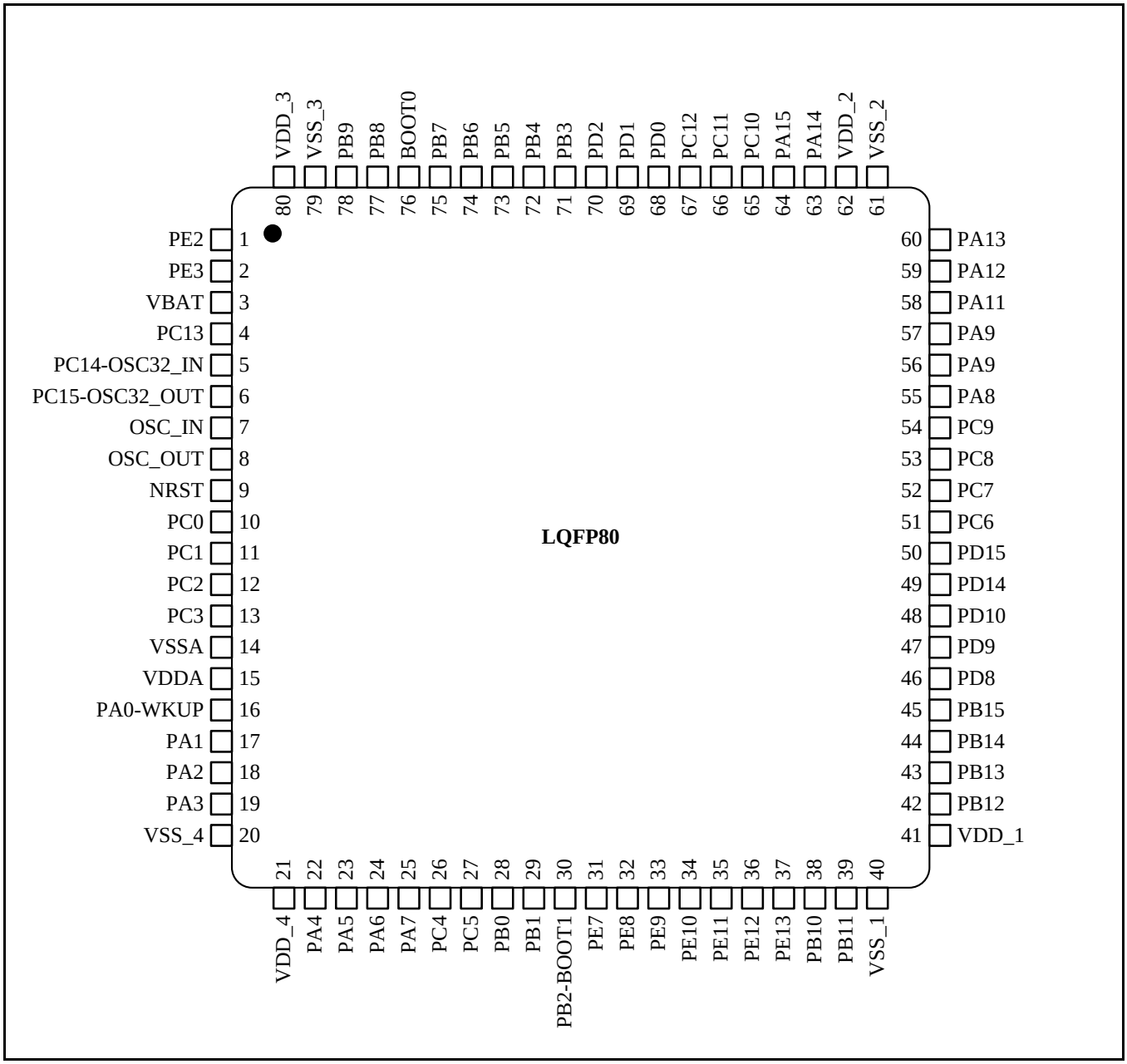
3.4 LQFP80 package

3.4.1 LQFP80 pin distribution



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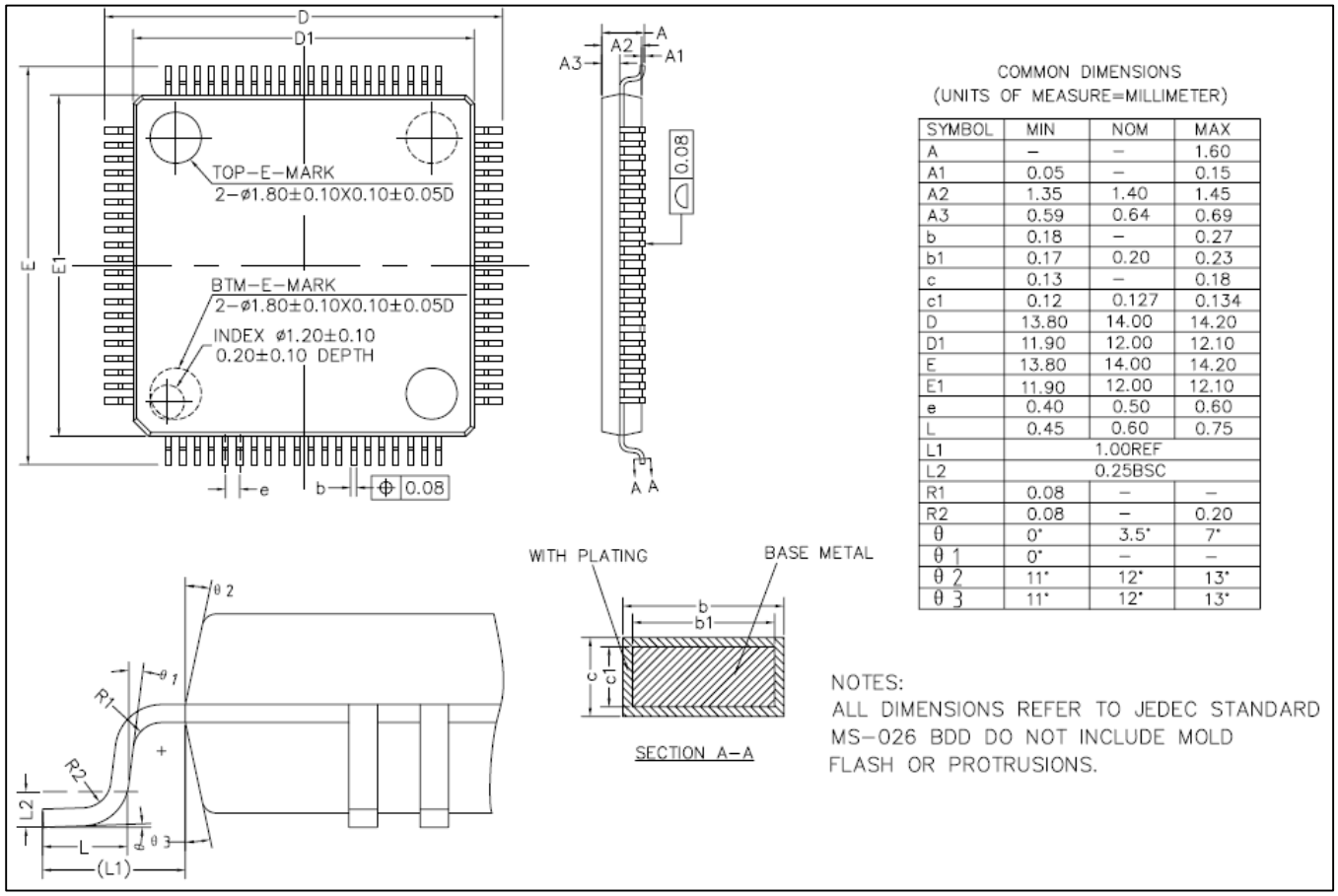
3.4.2 LQFP80 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
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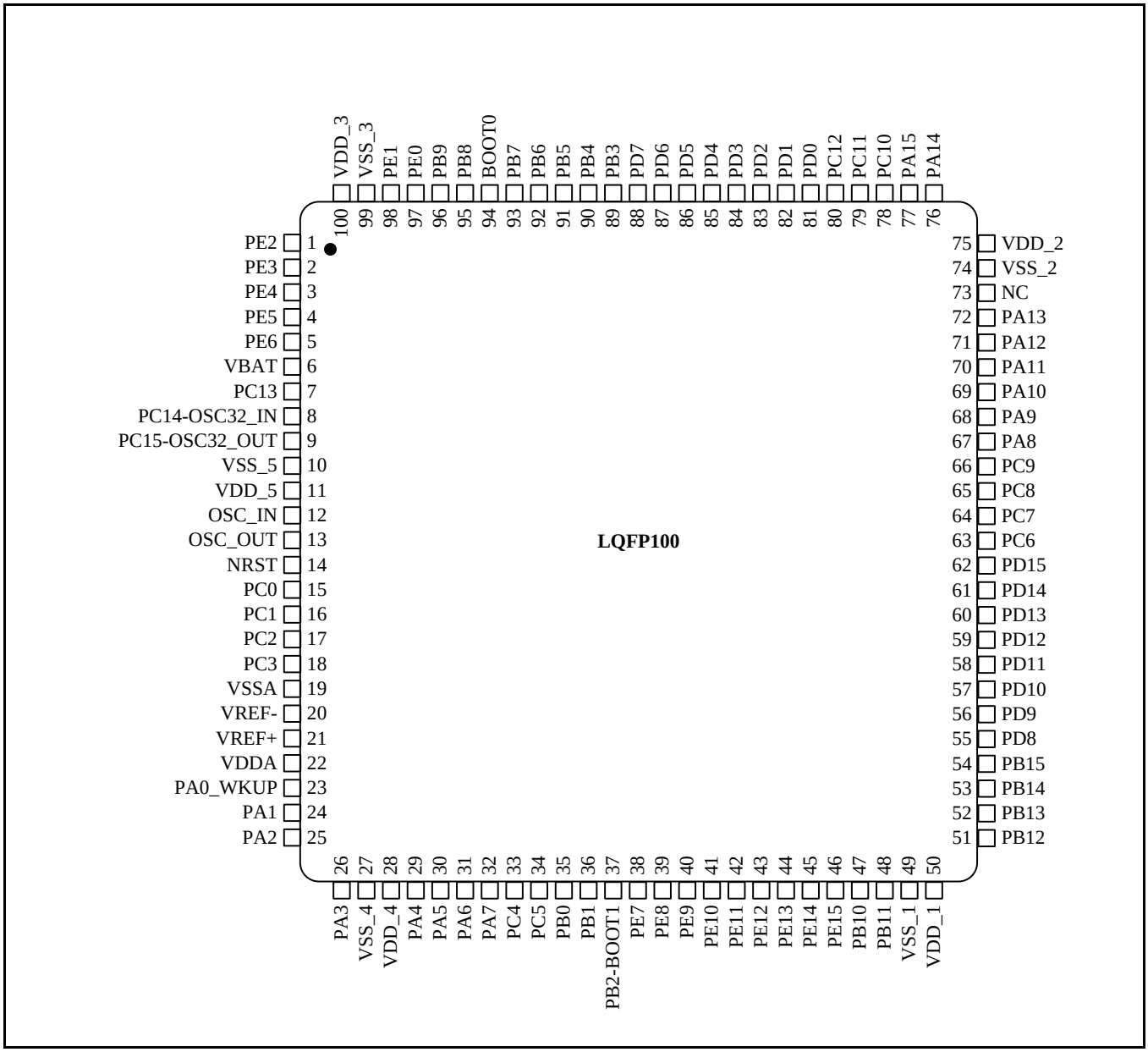
3.5 LQFP100 package

3.5.1 LQFP100 pin distribution



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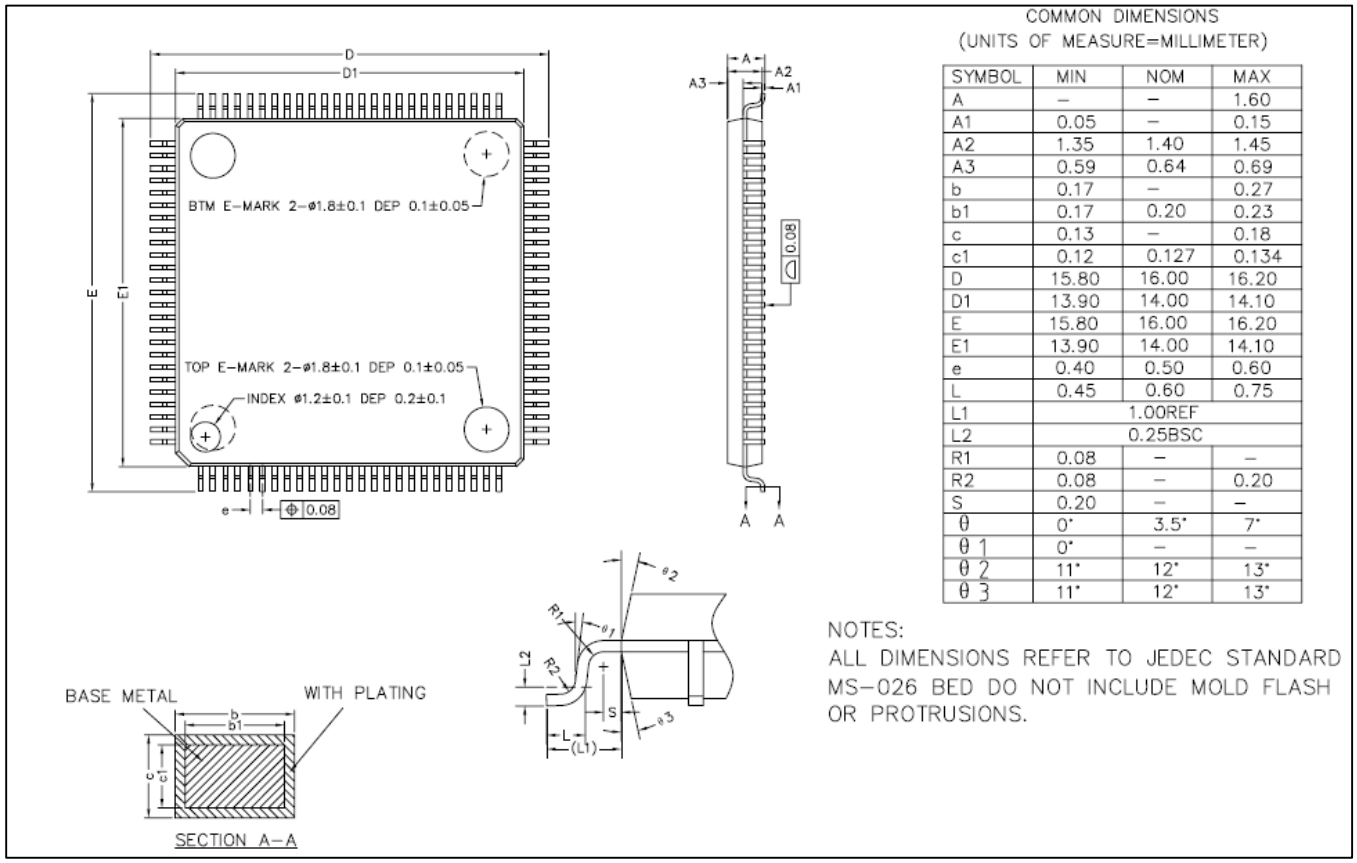
3.5.2 LQFP100 package size



COMMON DIMENSIONS
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SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
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4 Version history

Version	The date	Note
V1.0	2020.02.12	New document
V1.0.1	2020.11.10	1. Modify 3.2.1 pinout diagram 2. Added QFN48 package 3. Added N32G455CEQ7 model
V1.1	2022.04.26	1. Updated QFN48 package size 2. Delete SDIO eMMC format 3. Modified reset description in Key features

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