Design guide

N32A455 series hardware design guide

Introduction

This document details the hardware design checklist for N32A455 series MCUs to provide users with hardware design guidance.

CONTENS

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1. N32A455 Series MCU Hardware Design Checklist

1.1 Introduction to Power Supply

The operating voltage (VDD) of N32A455 series chips is 1.8V~3.6V. Mainly: VDD, VDDA pins. For details, please refer to the relevant datasheet.

1.2 VDD power supply scheme

VDD is the main power supply of MCU, which must be powered by a stable external power supply, the voltage range is 1.8V~3.6V, all VDD pins need to place a 0.1uF decoupling capacitor nearby, and one VDD pin needs to add a 4.7uF decoupling capacitors. For the specific design of the decoupling capacitor, please refer to the reference design schematic diagram of the minimum system of each package in Chapter 3.

VDDA is an analog power supply, which provides power for ADC, DAC, OPAMP, COMP, and TSC. It is recommended to place a 0.1uF and a 1uF capacitor on the VDDA input pin.

1.3 Spare battery

The VBAT pin mainly supplies power to the RTC unit, so that the RTC can still operate normally when the main power supply (VDD) is turned off. If there is no external battery in the application, VBAT must be connected externally to VDD.

1.4 External pin reset circuit

A system reset occurs when a low level (external reset) occurs on the NRST pin. The external NRST pin reset reference circuit is as follows.

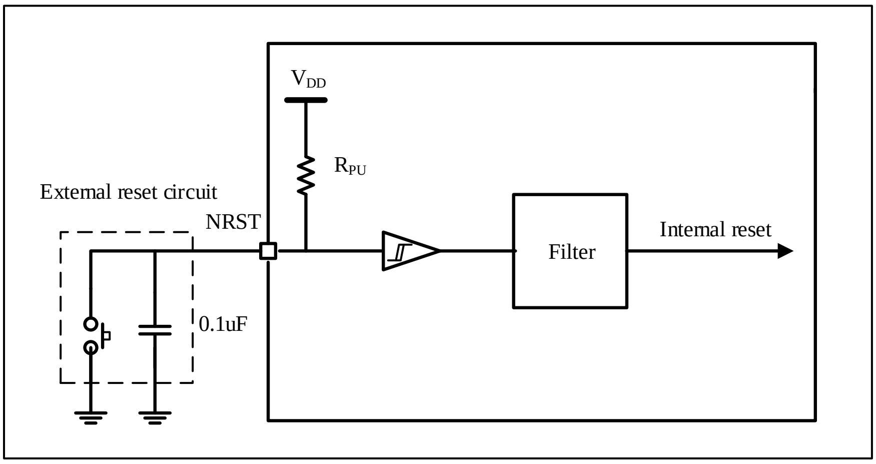

Figure 1-1 System reset diagram

Note: The reset pin NRST cannot be left floating during design, and the external capacitor 0.1uF is given as a typical reference value. If the reset time needs to be accelerated, the NRST pin can be pulled up externally, and the typical value of the pull-up resistor is 10K. In addition, the user can decide whether to add a reset button according to the

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actual needs of the product

1.5 External clock circuit

N32A455 series MCU contains 2 external clocks: external high-speed clock HSE (4MHz~32MHz) and external low-speed clock LSE (usually 32.768KHz).

HSE and LSE configure the corresponding load capacitance according to the characteristics of the crystal oscillator. For details, please refer to the description of the external clock characteristics in the relevant datasheet.

When using LSE, the adjacent IO pins (take LQFP64 package pins as an example: PC13 and PD0) cannot have GPIO toggle level signals. Refer to Figure 1-2 for adjacent pins. Inverted level signal will cause unstable LSE operation.

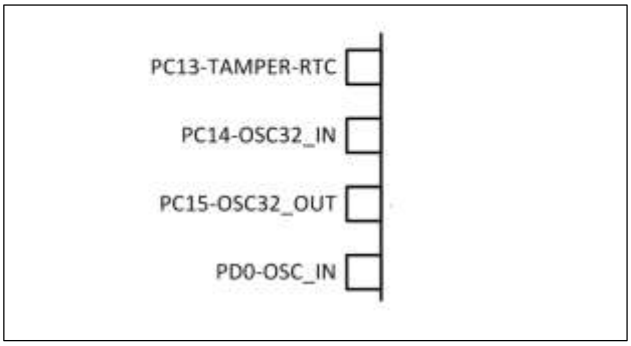

Figure 1-2 PC13/PD14 pins cannot have flip signals

1.6 Boot Pin Connection

The figure below shows the external connections required for the N32A455 series chip to select the boot memory. Please refer to the relevant section of the datasheet for the startup mode.

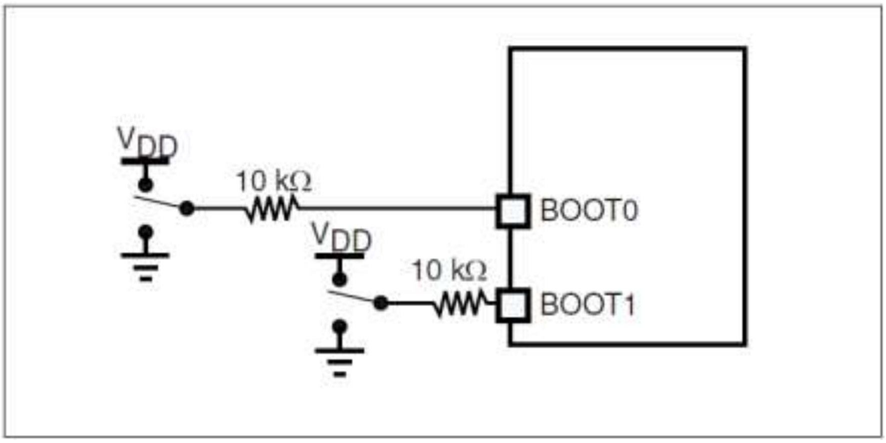

Figure 1-3 Implementation example of startup mode

The BOOT pin is pulled high, and the chip is started from the BOOT area after reset; the BOOT pin is pulled low, and the chip is started from the user area after reset.

Note: The resistance values in the figure are given as typical reference values only.

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1.7 Independent ADC Converter

In order to improve the conversion accuracy, the ADC has a pair of independent power supplies, an independent VDDA pin powers the ADC, and the VSSA pin is used as the ground terminal of the analog power supply. It can be separately filtered and shielded from noise on the PCB to power the ADC.

Regarding the ADC circuit design, please pay attention to the following points:

1） When using ADC sampling, it is recommended to shorten the external wiring distance;

2） It is recommended to keep away from some high frequency inversion signals around the input signal of ADC;

3） Note the maximum supported rates for slow and fast channels:

When the input frequency of N32A455 series is 72MHZ, the sampling rate of ADC fast channel should not exceed 5Msps, and the sampling rate of ADC slow channel should not exceed 2.5Msps;

4） During ADC conversion, the chip does not support modifying the ADC configuration. If you need to modify the configuration, you need to wait for the current conversion to end or turn off the ADC before configuring;

5） When a certain ADC channel is used, negative voltage (such as -0.2V) cannot be applied to other unused ADC sampling channels. If this negative voltage is applied, the voltage of the normally sampled ADC channel will be pulled down, resulting in sampling. data is inaccurate;

6） When a certain ADC channel is used, high voltage (greater than VDD voltage) cannot be applied to other unused ADC sampling channels. If this high voltage is applied, the voltage of the normally sampled ADC channel will be pulled up, resulting in incorrect data read. allow;

7） When using ADC, the maximum value of RAIN cannot be too large, and it needs to comply with the following formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

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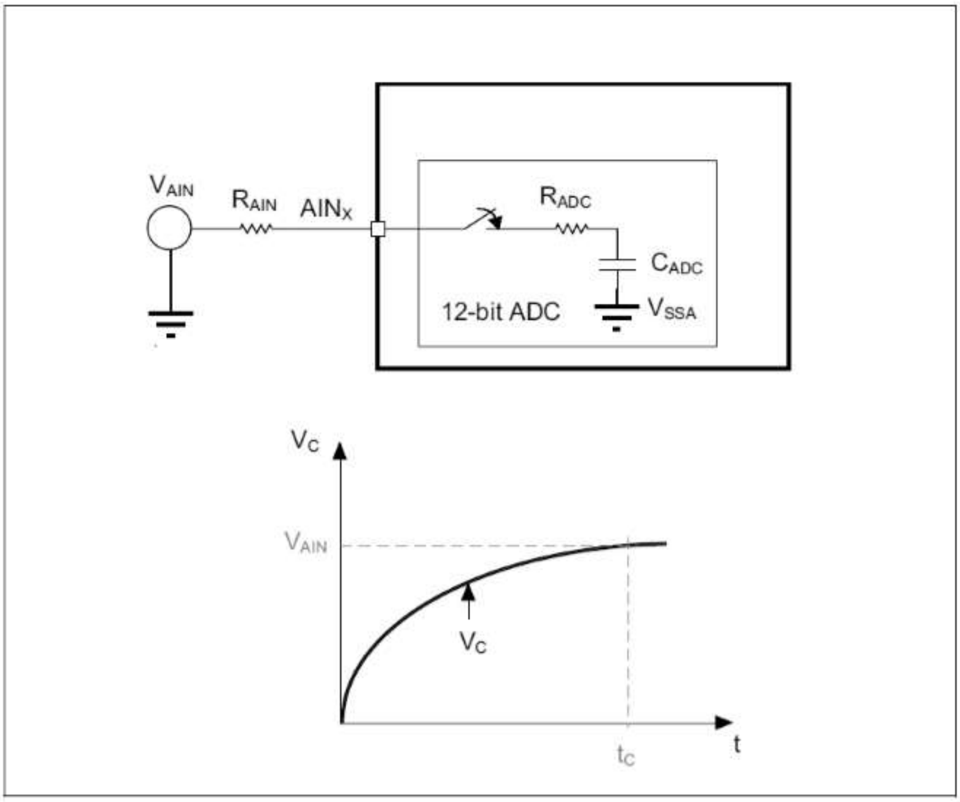

Figure 1-4 Influence of series resistance of ADC input port

The following figure shows the ADC sampling configuration rule table under typical input impedance:

ADC input clock frequency:72MHz				
Equivalent impedance(Ω)	Min Sampling cycle	Min Sampling Time(ns)	ADC Sampleing+ Convert Time(us)	ADC maximum sample rate (Ksps)
0	1.75	24.26	0.198	5053.8
100	2.10	29.11	0.203	4932.8
330	2.90	40.27	0.214	4675.5
470	3.39	47.06	0.221	4531.5
1000	5.24	72.78	0.246	4058.6
2200	9.43	131.00	0.305	3282.8
4700	18.17	252.31	0.426	2347.9
10000	36.68	509.46	0.683	1464.0
30000	106.55	1479.87	1.653	604.8
51000	179.91	2498.80	2.672	374.2
100000	351.09	4876.29	5.050	198.0
470000	1643.67	22828.80	23.002	43.5
1000000	3495.21	48544.56	48.718	20.5

Figure 1-5 N32A455 series ADC sampling configuration rule table

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Note: The sampling time needs to be comprehensively configured according to the input clock and the optional sampling period of the ADC register. In principle, the ADC sampling period configuration should be greater than or equal to the minimum number of sampling periods in the table.

1.8 IO power-on pulse processing

During the power-on process, because the IO is in a high-impedance state and the internal circuit coupling characteristics, a high-level pulse will appear on the IO at the moment of power-on (the actual high-pulse voltage value should be measured by the user). If the pulse will affect its application, it is recommended to add an appropriate capacitor (1nF~100nF) or an appropriate pull-down resistor (10K~100K) on the corresponding IO.

The following picture shows the waveform of IO (PB12) during the power-on process of the development board N32A455REL7-STB_V1.0:

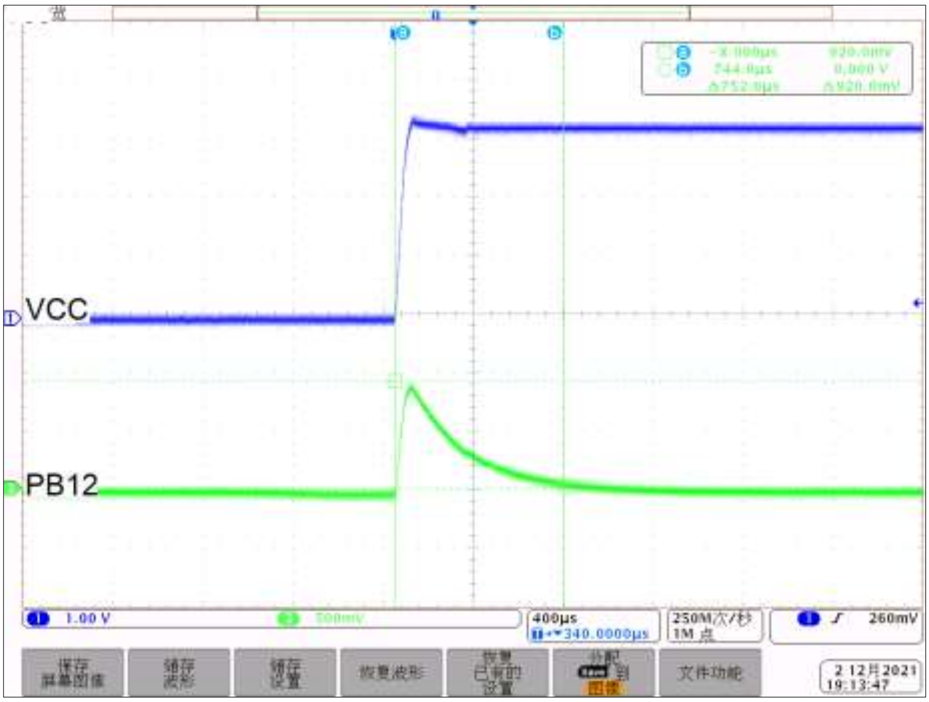

Figure 1-6 IO (PB12) waveform during power-on

The following figure shows the waveform of the development board N32A455REL7-STB_V1.0 after the IO (PB12) is added with a 10K pull-down resistor during the power-on process:

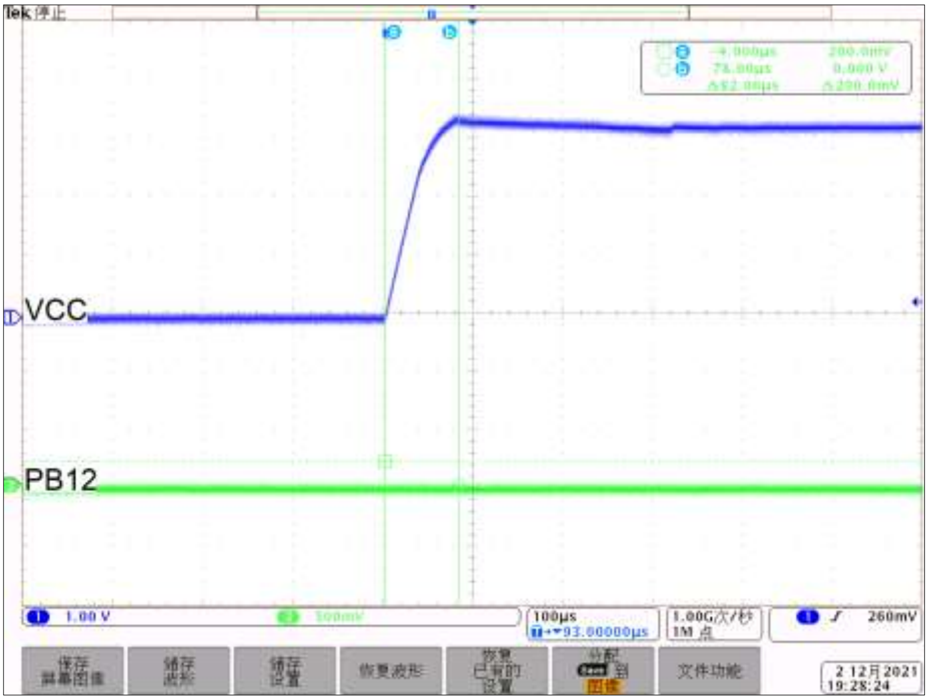

Figure 1-7 Waveform after IO (PA9) plus pull-down resistor during power-on process

1.9 IO withstand voltage

When using the chip, please pay attention to the withstand voltage value of each IO. In the column of the I/O structure defined by the pin reuse in the data sheet, FT: 5V tolerance, TTa: 3.3V tolerance, TC: ordinary 3.3V IO, this type of IO When communicating with other external IOs of different voltage domains, level conversion is required.

Package			Pin name	Type (1)	I / O structure(2)	Fail-safe support(8)	Main functions(3) (after reset)	Optional multiplexing function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefine
-	-	1	PE2	I/O	FT	Yes	PE2	UART6_TX	-
-	-	2	PE3	I/O	FT	Yes	PE3	UART6_RX	-
-	-	3	PE4	I/O	FT	Yes	PE4	-	-
-	-	4	PE5	I/O	FT	Yes	PE5	-	-
-	-	5	PE6	I/O	FT	Yes	PE6	-	-
1	1	6	VBAT	S	-	-	VBAT	-	-
2	2	7	PC13-TAMPER- RTC(4)	I/O	TC	Yes	PC13(5)	TAMPER-RTC	-

Figure 1-8 I/O structure defined by pin multiplexing in the datasheet

Note: FT: 5V standard IO, TC/TTa: 3.3V standard IO, when using the chip, pay attention to the influence of signals higher than the tolerance voltage on IO.

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1.10 Anti-static design

1.10.1 PCB Design

For the PCB design of ordinary two-layer boards, it is recommended to do wrapping around the signal lines, and try to cover the edges of the PCB as much as possible. If the cost allows, it can be designed with a four-layer board or a multi-layer board. In a multi-layer PCB, the ground plane acts as an important charge source, which can offset the charge on the electrostatic discharge source, which is conducive to reducing the electrostatic field band. The ground plane of the PCB can also be used as a shield for the signal line (of course, the larger the opening of the ground plane, the lower the shielding effectiveness). In addition, if a discharge occurs, since the ground plane of the PCB board is large, the charge is easily injected into the ground plane, rather than into the signal line. This will help protect the component, because the charge can be drained before causing component damage.

1.10.2 ESD Protection Devices

In the actual product design, the chip itself has a certain anti-static ability. The static level of N32A455 series MCU ESD (HBM) mode is +/-4KV, but if there is a higher ESD protection level requirement, and the pins of the chip need Direct external connection is used as the output or input port of the product. At this time, the pins of the chip are directly exposed to the outermost part of the product, and cannot be isolated by laying the ground or other means. Under this condition, it is generally necessary to consider an external ESD protection device. TVS diode is a typical ESD protection device. The following is an example of a typical connection method.

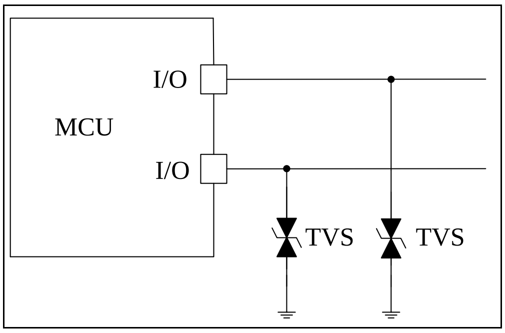

Figure 1-9 TVS connection on I/O pins

1.11 Debug Interface

N32A455 series chips support serial interface (SWD) and JTAG debug interface, please refer to the relevant user manual for detailed application.

Debug Signal	GPIO Pins
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
JNTRST	PB4

Table 1-1 Debug Interface

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1.12 CAN interface

Comply with the CAN physical layer characteristics specified in ISO-11898-2. The standard specifies the use of parallel wire cables with a nominal impedance of 120Ω (minimum 95Ω, maximum 140Ω). For electromagnetic compatibility (EMC) reasons, shielded twisted-pair cables are generally required, although ISO-11898-2 also allows the use of unshielded cables. CAN specifies a maximum communication line length of 40m at a data rate of 1Mbps. Longer communication lines may be supported at lower communication data rates.

Compatible with specifications 2.0A and 2.0B, support standard frame and extended frame transmission and reception, bit rate up to 1Mbps. Designed to meet the specific requirements of a vehicle's serial data bus: real-time processing, reliable operation in the vehicle's EMI environment, cost-effectiveness, and required bandwidth.

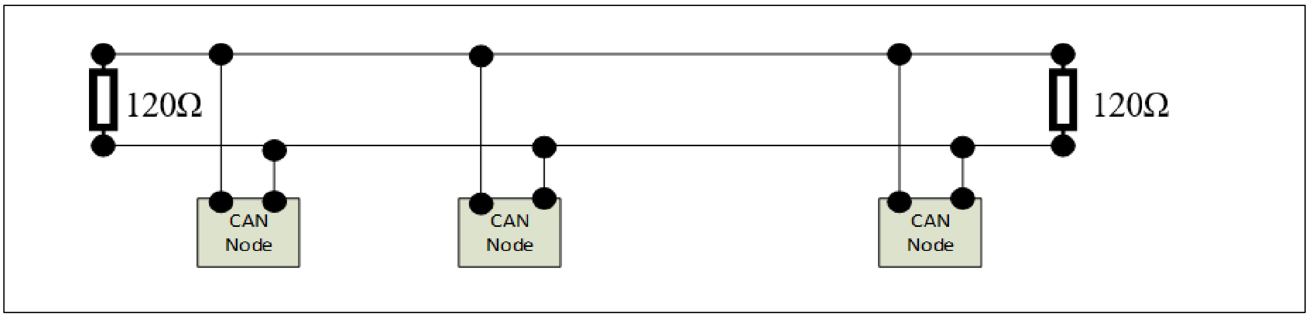

Figure 1-10 CAN topology

Typical CAN interface circuit diagram:

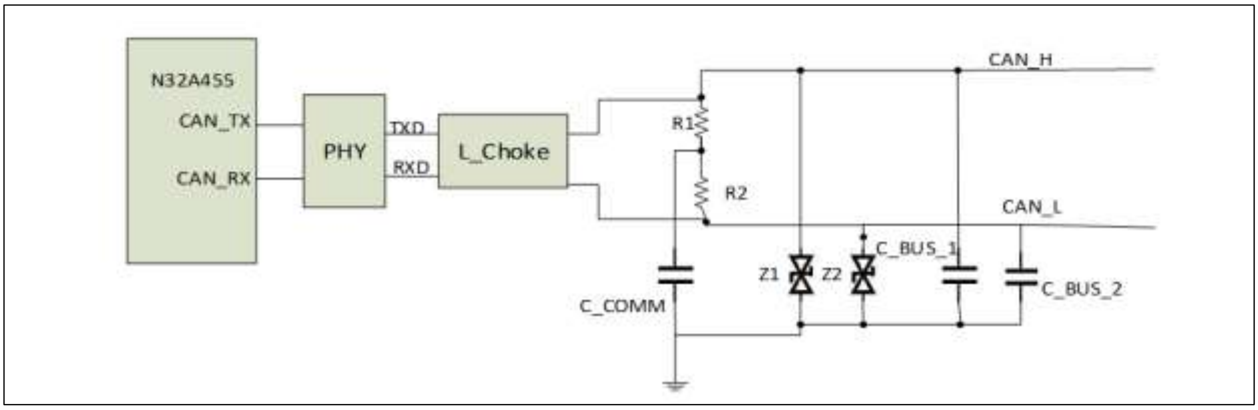

Figure 1-11 CAN typical interface circuit

Circuit Description:

Component tag number	illustrate
R1,R2, C_COMM	R1, R2: terminal resistance; C_COMM: terminal filter capacitor. In a CAN network, two nodes at both ends of the bus have terminating resistors and the other nodes do not. The design needs to be selected according to the position of the node in the network. ISO-11898-2 recommends not to integrate termination resistors into nodes, but to connect independent termination resistors at the farthest

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	ends of the bus. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistor is nominally 120Ω. The terminal resistance can be divided into two parts R1 and R2, and a filter capacitor can be added during the period to better filter out high-frequency noise and reduce common-mode emissions. R1=60Ω; R2=60Ω; C_COMM = 4.7uF.
Z1,Z2	Automotive EMC requirements (especially ESD) can be met by using Zener tubes Z1 and Z2. These devices should be placed near the connector.
C_BUS_1, C_BUS_2	Capacitors C_BUS_1 and C_BUS_2 are not required. For EMC reasons, these two capacitors can be added. The recommended value is 120pF.
L_Choke	common mode choke, not required. Common mode chokes on the CANH and CANL lines can help reduce coupled EMI and meet automotive EMC requirements. This choke, together with a transient suppressor on the transceiver pins, can greatly reduce coupled electromagnetic noise and high frequency transients.

Table 1-2 CAN typical interface circuit description

1.13 LIN interface

LIN is a serial communication protocol designed to support automotive networking, enabling low-cost and efficient communication with sensors and actuators.

Typical LIN network:

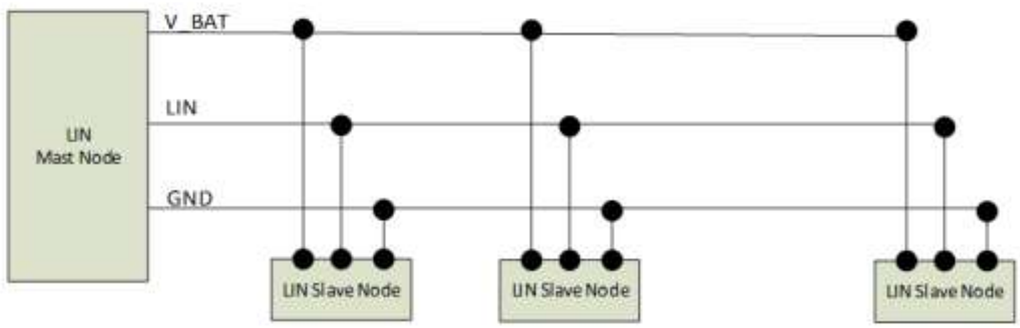

Figure 1-12 LIN typical interface circuit

Circuit Description:

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Component tag number	illustrate
L_R1, L_R2, L_D1	Mandatory for LIN master nodes only. L_R1, L_R2: The recommended value is 2kΩ. If more than 2 resistors are connected in parallel, the value must be selected based on the principle of total resistance 1 kΩ and minimum power loss of the entire main terminal.
L_C1	Slave node: typical value 220pF; master node: starting from 560pF, which is about 10 times the capacitance of the slave node.
L_C2	optional.
L_Z1	optional. Can meet the requirements of automotive EMC (especially ESD).

Table 1-3 LIN typical interface circuit description

1.14 BOOT serial interface

N32A455 series chips support BOOT serial communication. The serial interface is as follows:

BOOT Serial Port	GPIO Pins
USART1_TX	PA9
USART1_RX	PA10

Table 1-4 Serial port interface

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2. Overall Design Suggestions

1) Printed circuit board

It is recommended to use a multi-layer printed circuit board with a dedicated independent ground plane (VSS) and a dedicated independent power supply plane (VDD), which can provide good coupling performance and shielding effect. In practical applications, if a multi-layer printed circuit board cannot be used considering the economical reason, a good grounding and power supply structure must be ensured when designing the circuit.

2) Component layout

In PCB design, different circuits need to be laid out separately according to the different effects of each device on EMI. For example, high-current circuits, low-voltage circuits, and high-frequency devices. Thereby reducing cross-coupling on the PCB.

3) ground and Power (VSS, VDD)

Each module (analog circuit, digital circuit, low-sensitivity circuit) should be grounded separately, the digital ground and the analog ground should be separated, and all the grounds should be connected together at one point eventually. According to the size of the printed circuit board current, try to increase the width of the power line to reduce the loop resistance. At the same time, the direction of the power wire and the ground wire and the direction of the current should be as consistent as possible, and the power supply should be as close to the ground wire as possible to reduce the area of the loop. This helps to enhance noise immunity. The area on the PCB without devices needs to be filled with ground to provide good shielding effect.

4) Decoupling

All power pins need to be properly connected to power. These connections, including pads, wires, and vias, should have as low impedance as possible. The method of increasing the wiring width is usually adopted, and decoupling capacitors must be placed close to the chip for each pair of VDD and VSS pins. The figure below shows a typical layout of the power/ground pins.

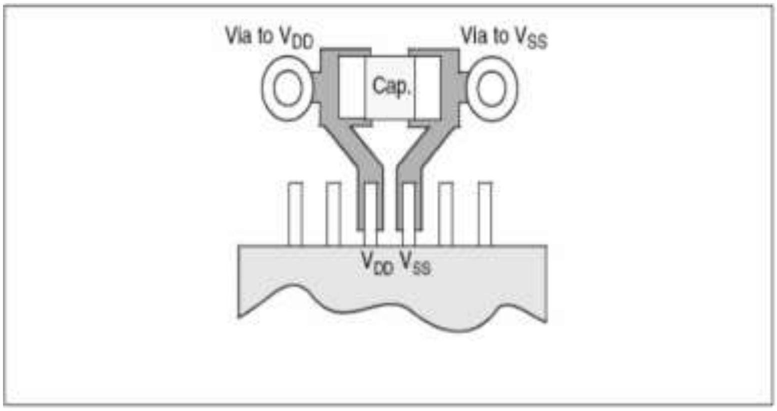

Figure 2-1 Typical layout of VDD/VSS pins

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3. Minimum System Reference Design Schematic

3.1 LQFP100

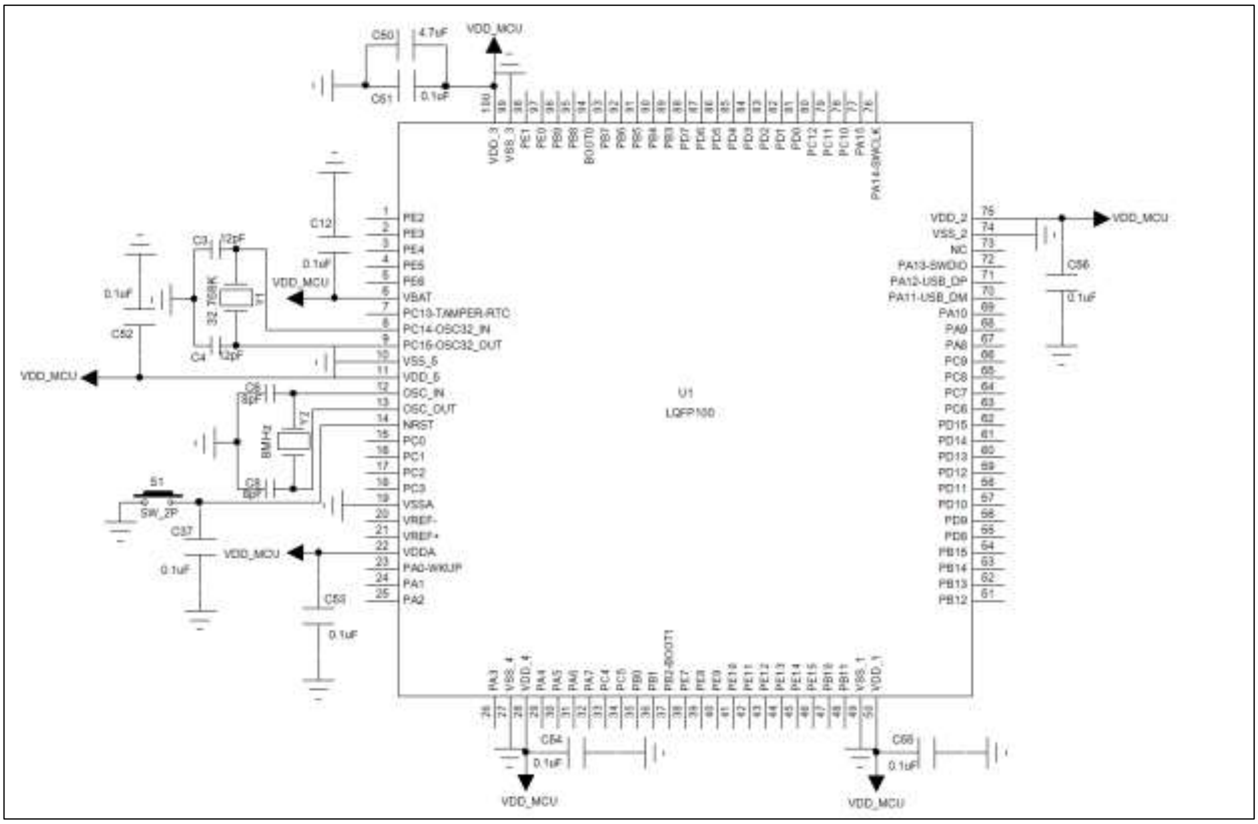

Figure 3-1 LQFP100 Package Minimum System Reference Design Schematic

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3.2 LQFP64

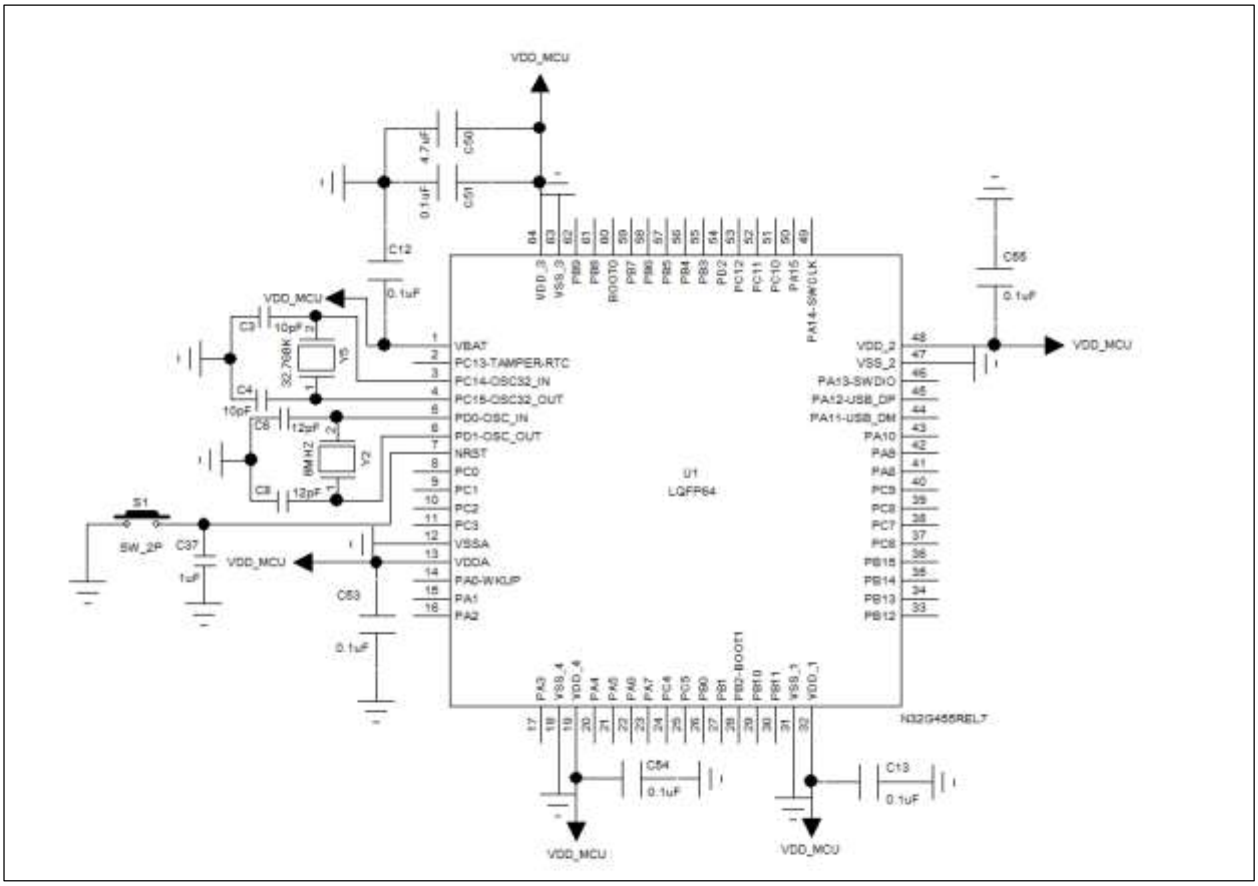

Figure 3-2 LQFP64 Package Minimum System Reference Design Schematic

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3.3 LQFP48

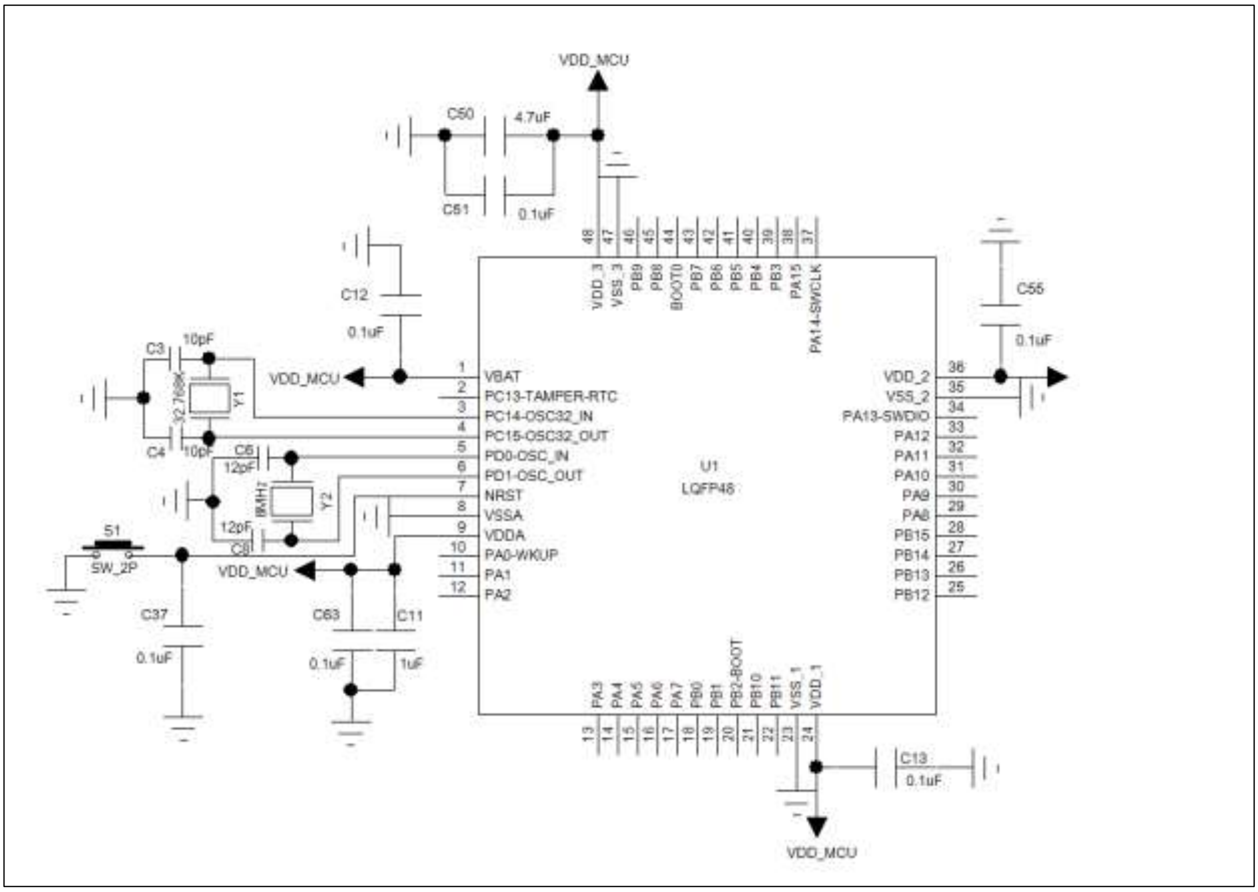

Figure 3-3 LQFP48 Package Minimum System Reference Design Schematic

Figure 3-1 to Figure 3-4 are the schematic diagrams of the minimum system reference design of each package of the N32A455 series, which mainly reflect the design of power supply decoupling capacitors, clocks, reset circuits, etc. The clock circuit depends on the user's design, and the chip supports internal high-speed and low-speed clocks available to the user for selection.

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4. PCB LAYOUT Reference

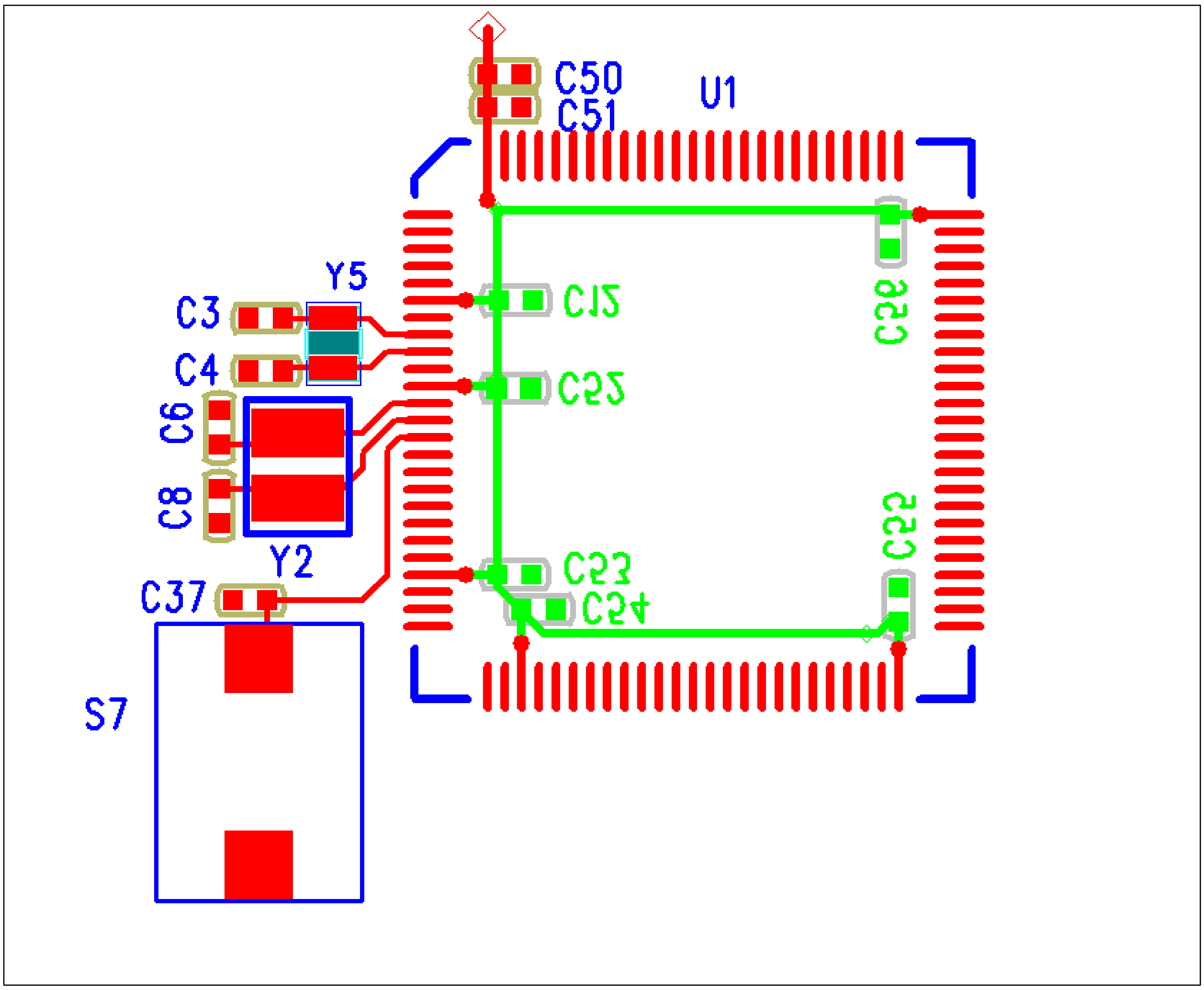

Figure 4-1 LQFP100 Package PCB LAYOUT reference diagram

During PCB LAYOUT design, decoupling capacitors need to be placed near each power pin. The external crystals and traces of the HSE and LSE should be grounded as much as possible. The area below the crystals close to the crystals also needs to be grounded, and no signal lines can pass through them to prevent the signal lines from interfering with the crystal signals.

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5. Typical failure analysis

The common problems and analysis methods encountered by customers in the process of using the chip are described as follows.

5.1.1 Short circuit between power pins and ground

Problem Description:

The VDD pin of the chip is short-circuited with the GND test, and the chip is abnormally hot after power-on.

Problem check:

1) Whether the VDD decoupling capacitor has insufficient withstand voltage to cause the capacitor to break down and short circuit.
2) When the product starts up, whether the VDD voltage exceeds the specified maximum value.
3) Whether there is an overshoot voltage exceeding the maximum value of VDD during the operation of the product.
4) In the process of production and use, whether there is static electricity that causes chip damage.

5.1.2 GPIO damage

Problem Description:

The chip GPIO cannot output a high level or a low level normally, the GPIO is used as an input to detect the level error, the VIH or VIL test value is abnormal, and the pin impedance is abnormal.

Problem check:

1) Whether the external input voltage to the chip GPIO exceeds the maximum value, such as the 5V-tolerant I/O input voltage exceeding 5V.
2) In the process of product production and testing, whether there is a high voltage input to the GPIO port.
3) In product design, whether there is a high-voltage signal near the GPIO trace coupled to the GPIO input port.
4) In the process of production and use, whether there is static electricity that causes chip damage.

5.1.3 ADC sampling inaccurate

Problem Description:

When sampling the voltage at the ADC input port of the chip, the sampling voltage is inaccurate.

Problem check:

Refer to Section 1.7 to confirm whether the hardware and software settings meet the requirements of ADC

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6. Version history

Version	Date	Remark
V1.0.0	2022-4-6	Create documentation
V1.1.0	2023-02-10	Updated description of some chapters

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