N32G003 Series Errata Sheet V1.2.0

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1 Errata List

Errata overview

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		Version A	**Version B**
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●: there is this problem -: there is no this problem

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2 Power Control (PWR)

2.1 Power on and down failure problem

Description

When the chip is in a low temperature environment, there will be a probabilistic power on and down failure, and the chip cannot be started normally.

Resolution

When power down, ensure that the chip VDD voltage drops below 100mV, and then power on to the normal working voltage.

2.2 Option byte configuration LVR function cannot be used

Description

The LVR voltage threshold bit and enable bit are configured via the option byte, but no reset occurs when the actual voltage falls below this threshold.

Resolution

The LVR reset function is enabled by configuring the LVR reset enable bit of the PWR module register.

3 GPIO and AFIO

3.1 PA0 affects reset when used as a normal GPIO

Description

When the PA0 pin turns off the Reset function (for normal GPIOs) through the configuration option byte, the NVIC system soft reset and watchdog reset will not take effect.

Resolution

Do not configure PA0 for normal GPIOs.

3.2 PA9 cannot be used as UART2_RX

Description

Pin PA9 cannot be used as UART2_RX, and dose not support serial port reception.

Resolution

Do not use PA9 as serial port to receive.

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4 Flash

4.1 The Flash main memory after 3k area under the L1 level can be read\written\erased by SWD

Description

Under the L1 read protection level, the area after 3KB of the Flash main memory can be read\written\erased by SWD.

Resolution

Not.

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5 Version history

Date	Version	Remark
2023.2.27	V1.0	Initial release
2023.3.31	V1.1	Add L1 level SWD access instructions
2023.7.17	V1.2.0	1. Added B version chip errata 2. Added Section 3.2 PA9 usage problem

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